

**DOCTORAL THESIS**

# Isolated Matrix Converters

Oleksandr Korkh

TALLINNA TEHNIKAÜLIKOOL  
TALLINN UNIVERSITY OF TECHNOLOGY  
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**Declaration:**

Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for doctoral or equivalent academic degree.

Oleksandr Korkh

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# **Isoleeritud maatriksmuundurid**

OLEKSANDR KORKH







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## List of Publications

The list of author's publications on the basis of which the thesis has been prepared:

- I Korkh, O.; Blinov, A.; Vinnikov, D.; Chub, A. Review of Isolated Matrix Inverters: Topologies, Modulation Methods and Applications. *Energies* 2020, 13, 2394.
- II O. Korkh, A. Blinov and D. Vinnikov, „Analysis of Oscillation Suppression Methods in the AC-AC Stage of High Frequency Link Converters,“ 2019 IEEE 60th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia, 2019, pp. 1–5, doi: 10.1109/RTUCON48111.2019.8982259.
- III O. Korkh, A. Blinov, R. Kosenko and D. Vinnikov, „Comparison of Soft Switching Methods of DC-AC Full Bridge High-Frequency Link Converter,“ 2018 IEEE 59th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia, 2018, pp. 1–6, doi: 10.1109/RTUCON.2018.8659898.
- IV A. Blinov, O. Korkh, D. Vinnikov, I. Galkin and S. Norrga, „Soft-Switching Modulation Method for Full-Bridge DC-AC HF-Link Inverter,“ *IECON 2019 – 45th Annual Conference of the IEEE Industrial Electronics Society*, Lisbon, Portugal, 2019, pp. 4417–4422, doi: 10.1109/IECON.2019.8927186.
- V A. Blinov, O. Korkh, A. Chub and D. Vinnikov, „Improved Modulation Method for Full-Bridge AC-DC HF-Link Converter,“ 2020 IEEE International Conference on Industrial Technology (ICIT), Buenos Aires, Argentina, 2020, pp. 1173–1177, doi: 10.1109/ICIT45562.2020.9067128.
- VI D. Zinchenko, O. Korkh, A. Blinov, P. Waind and D. Vinnikov, „Characterisation of 1200 V Reverse-Blocking IGBTs for Naturally Commutated HF-Link Inverter,“ 2019 IEEE 2nd Ukraine Conference on Electrical and Computer Engineering (UKRCON), Lviv, Ukraine, 2019, pp. 382–387, doi: 10.1109/UKRCON.2019.8879900.
- VII O. Korkh, A. Blinov, D. Vinnikov, V. Shevchenko, „Optimization and Design of Planar Transformer for the High Frequency Link Converter,“ 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Virtual event organized in Croatia, 2020, pp. 509–515, doi: 10.1109/PEDG.2020.8807722.

## **Author's Contribution to the Publications**

Contribution to the papers in this thesis is as follows:

- I Oleksandr Korkh, as the main author of the paper, has provided the literature review, the classification, and co-authored writing.
- II Oleksandr Korkh, as the main author of the paper, has provided the simulation and experimental verification in the experimental prototype developed by him, and co-authored writing. He presented the paper at 2019 IEEE 60th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia, 7-9 October 2019.
- III Oleksandr Korkh, as the main author of the paper, has provided the literature analysis, simulation, and co-authored writing. He presented the paper at 2018 IEEE 59th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia, 12-13 November 2018.
- IV Oleksandr Korkh has co-authored the paper and provided the simulation and experimental verification in the experimental prototype developed by him.
- V Oleksandr Korkh has co-authored the paper and was responsible for the simulation and design of the experimental prototype.
- VI Oleksandr Korkh has co-authored the paper and was responsible for the experimental measurements of the RB-IGBTs, and co-authored writing.
- VII Oleksandr Korkh, as the main author of the paper, has provided the literature review, the experimental transformer design, verification, and co-authored writing. He presented the paper at 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG).

## Abbreviations

AC	Alternating current
DC	Direct current
CS	Current source
FB	Full bridge
GTO	Gate turn-off thyristor
IGBT	Insulated-gate bipolar transistor
IMC	Isolated matrix converter
HF	High frequency (switching frequency)
HFT	High-frequency transformer
HV	High voltage
LF	Low frequency (grid frequency)
LV	Low voltage
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed circuit board
PF	Power factor
PSM	Phase shift modulation
PWM	Pulse width modulation
RB-IGBT	Reverse blocking IGBT
SiC	Silicon Carbide
ZCS	Zero current switching
ZVS	Zero voltage switching
WBG	Wide bandgap semiconductor

# 1 Introduction

## 1.1 Background

Climate change requires reduction of CO<sub>2</sub> pollution in the world [1]. To address this, renewable and alternative energy sources are continuously growing, extending the application area of the power electronic interfaces. Such an increase in renewable sources provides a shift to the decentralized power system, and the amount of energy generated by the power plants is continuously decaying. Renewable sources such as solar and wind, together with the storage technologies, including the batteries, fuel cells, supercapacitors, require various converters to match the different voltage levels and provide smooth and efficient control of power [2]-[4]. As a result, the concept of zero-energy building has emerged where the on-site renewable power generation is combined with the storage systems to provide reduced energy consumption from external energy sources and potentially give benefits in the economic aspects [5]. This has resulted in the increased interest and demand in the various types of residential energy generation systems, like building-integrated and rooftop photovoltaic systems, fuel cells and battery energy storages, or small-scale wind turbines [6]. Such energy sources and generators require an interface between different voltage levels, generally managed by various power electronic converter types, which often have to be capable of operation with different voltage levels of the common DC or AC power line [7]. Thanks to very fast response times, the energy storages interfaced with such power electronic converters can participate in the balancing of the AC grid and to support the grid in the case of the different power generation variations from the renewable sources and support the uninterruptible power supply for some critical loads [8].

The power electronics converter technology is continuously improved with the developments in the semiconductor and passive component technologies. Another direction of the improvements lies in the smart functionality and user-friendly user interface of the converters, which gives benefits today and, in most cases, is a requirement. It allows for provisioning information about the parameters to the user and provides the control of the device when it is required. Other continuously growing markets for the power electronic converters are chargers for electric bikes and vehicles, railway applications, various variable speed drives, and the design of the new converter topologies at a lower price, cost, size, and high reliability.

## 1.2 Motivation of the Thesis

Today's converters in the power distribution systems have to work with the variable DC voltage sources and connect them to the utility AC grid. The converter also may include the galvanic isolation to provide safe operation. In most cases, the task is to provide the voltage step-up of the low DC voltage, which is typically achieved with the two-stage topology (Figure 1.1) [9]. First, the input DC voltage is stepped up using a DC-DC stage (may also include the HFT) and stabilized with an HV DC-link capacitor. Then, the inverter stage converts the constant DC voltage to the required AC voltage. The benefits of this approach are the wide range of regulation and overall simplicity, which has enabled its wide adoption in different practical applications [9]-[12]. Also, this converter type can be capable of bidirectional application, but in some cases, it requires a complicated control system to provide proper regulation.

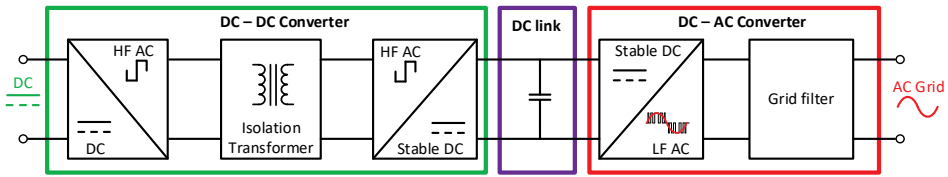


Figure 1.1 Typical structure of two-stage DC/AC converter [1].

The other option is to utilize the single-stage solution or the IMC without an intermediate DC link. These types of converters allow direct conversion between the DC and AC sources [13]-[20]. Similarly, such converters can transfer power in both directions and provide a wide range of soft-switching. The IMCs have been proposed for a range of applications with various voltage and power ratings, demonstrating their scalability and versatility [1]. These features can potentially lead to a wide range of industrial applications, giving the motivation for research in this area.

The design of the IMC for a specific application depends on the design requirements and limitations of topologies and existing technologies. The advantages of IMCs can be summarized as:

1. They could provide soft-switching in all semiconductors, with the utilization of special modulation methods.
2. They avoid the bulky HV DC-link capacitors. Only an electrolytic capacitor for filtering the double grid frequency current ripple at the DC-side can be used.
3. The efficiency and cost could be reduced using semiconductors with the reverse blocking capability.

The main limitation of the IMCs compared to two-stage topologies is its relatively narrow input DC voltage regulation range, which limits their applicability where wide voltage variations could occur. Many limitations of the IMCs are related to the available technologies and materials rather than the concept itself. The control complexity did not allow the use of the IMCs due to the limitation of the microcontrollers when the first solutions of this type were proposed around 30 years ago. Nowadays, the IMCs gain popularity despite the complicated control system due to the availability of low-cost high-performance microcontrollers, which proves the timeliness of the given research.

In the recent few years, the IMCs have attracted more research attention. The main trend has focused on the topological aspects, the system component optimization, optimization, and improvements of the system efficiency and switching transients, reduction of the voltage overshoots and stresses of the semiconductor components. Another trend is the study and optimization of rectifier (AC-DC) operation mode. Today's technologies allow for reaching IMC efficiencies comparable to that of the two-stage converters. Nevertheless, various design challenges still exist and require additional research and improvements. For example, the transformer design optimization and improvements in operating conditions of the semiconductor components are needed to improve power conversion efficiency and silicon utilization further.

This thesis research was conducted based on one of the main research directions of the Power Electronics Group of Tallinn University of Technology. The activities aim to study and design the IMCs that include the CS switching stage in the AC-side and to improve industrial awareness of such systems. The current work was supported in part by European grants VE19058 and EMP474 (involving the study of the current source-based converters and their suitability for the battery chargers and storages), and

in part by the Estonian Centre of Excellence in Zero Energy and Resource Efficient Smart Buildings and Districts (focused on the research of the optimal usage of the resources and improving energy conversion efficiency).

### **1.3 Aims, Hypotheses and Research Tasks**

The power electronic converters based on the IMC topologies are not as widely adopted by the industry as the two-stage topologies though both have been under development for some time and are offering many potential areas of application.

The current Ph.D. research aims to design and experimentally evaluate the performance of current source-based IMCs. The author sets a goal to demonstrate that the IMCs are a versatile technology with reduced number of conversion stages that has potential in certain applications. The contributions of this thesis are intended to outline and address the existing challenges of IMCs from multiple directions and to advance the emerging field of IMCs, bringing it closer to wider industrial adoption.

#### **Hypotheses:**

1. New modulation methods can extend the IMC operation to four-quadrant on the AC-side and provide the operation with non-unity PF without using active snubber circuits. This allows for providing operation with inductive and capacitive loads.
2. The modulation methods for the IMCs could be extended and improved for providing ZVS in the DC-side semiconductors during the whole grid frequency period and in both power transfer directions.
3. The replacement of the anti-series connection of the regular IGBTs in the AC-side of the IMC by the anti-parallel RB-IGBTs could improve the efficiency of the IMC.
4. Combining the novel modulation methods with tailored design of the hardware part allows for realizing high step-up IMCs to extend the application range of the IMC family.

#### **Research Tasks:**

1. Review of the existing IMC topologies, analysis of their drawbacks and limitations in different applications.
2. Research and improvement of the existing modulation methods for the FB IMC; extension of the ZVS range for the DC-side semiconductors.
3. Research the operation of the case study FB IMC for non-unity PF and investigation of possibilities of revoking the additional active snubber requirement for this operation mode.
4. Characterization of the RB-IGBTs and experimental evaluation of their performance in the AC-side of the case study FB IMC.
5. Research, design, and experimental verification of the high step-up isolation transformers for the integration of the low-voltage DC sources to the utility grid with FB IMC.



## 1.4 Contribution and Dissemination

This research contributes to the advancement of the IMC technology and, in particular, the emerging field of the high-step-up IMCs. The main scientific and practical contributions of the Thesis are listed below.

### ***Scientific contributions:***

- Systematization and classification of IMCs, identification of their benefits and limitations.
- Synthesis of novel modulation methods for the inverter and rectifier operation modes of the IMC with improved soft-switching performance.
- Development of novel characterization methodology for the reverse blocking discrete and composite semiconductors with controlled current slope ( $di/dt$ ).

### ***Practical contributions:***

- Implementation and characterization of RB-IGBTs in the IMC.
- Demonstration of the four-quadrant operation capability of the IMCs without active snubbers.
- Derivation of design guidelines for the implementation of high step-up IMC.

Main findings related to this Ph.D. thesis are based on 7 papers attached and listed in the List of Author's Publications. Among them, 6 papers were reported at different international conferences of IEEE, and 1 paper was published in the international peer-reviewed journal.

## 1.5 Experimental setup

The experimental verification was done using the simulation models and three different converter prototypes. During the verification various laboratory equipment was utilized. The prototypes were supplied from DC sources Elektro-Automatik EA-PSI 9080-60 and Chroma 2150H- 1000S and loaded by the passive-resistive load. For capturing of the experimental waveforms, the digital oscilloscopes Tektronix DPO7254 and MSO4034B with the current probes Tektronix TCP0150A, TCP0030A, Rogowski coil CWTUM/015/R and high voltage differential voltage probes Tektronix P5205A were used. For measurement of the efficiency of the IMCs the power analyzer YOKOGAWA WT1800 was utilized. The photo of the experimental setup shown in Figure 1.2.

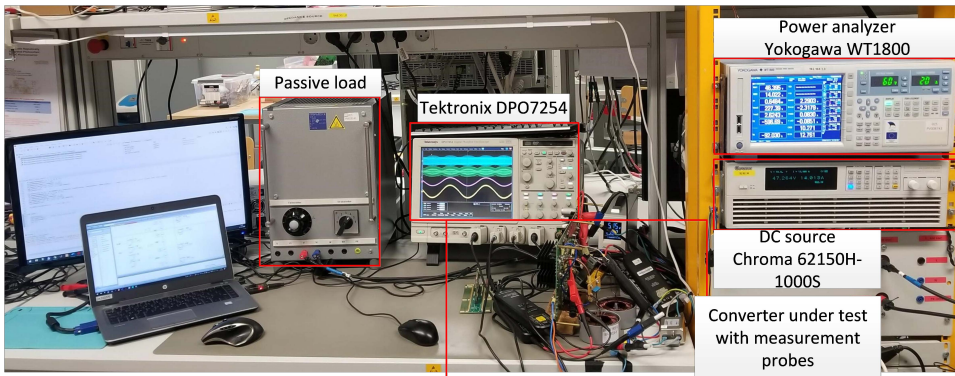


Figure 1.2 The experimental setup workplace

## 1.6 Outline

The main findings of the research are discussed in Sections 2 to 5. In Section 6, the summary of the work and future research directions is shown.

Section 2 addresses the current state of the art of the existing IMCs. It includes the general classification of the existing topologies and modulation as well as identification of the drawbacks and challenges of the FB IMC.

Section 3 presents the new modulation methods for the inverter and rectifier operation modes for the unity PF as well as the power factor correction functionality for the non-unity PF. The operation principles, benefits, and drawbacks of the proposed methods are presented and analyzed.

Section 4 discusses the implementation possibilities of the RB-IGBTs in the AC-side of the IMC. The novel characterization methodology for the reverse blocking discrete and composite semiconductors is proposed.

Section 5 focuses on the design and practical verification of the high step-up transformer for the IMC, providing the direct connection between the low voltage DC source such as the battery or fuel-cell with the utility grid.

## 2 State of the Art of IMCs

The section is based on the paper [1], where a detailed analysis of different IMC topologies, modulation methods, and control algorithms is presented and the potential applications are discussed.

### 2.1 Topologies

The IMC is the subclass of the matrix converters, which have bidirectional semiconductors on one side in the topology and provide galvanic isolation between the stages. At the same time, they do not require the HV DC-link capacitor and interface the DC and AC sides with only one conversion stage, as compared to the two-stage topologies [12] that comprise the HV DC-link and two conversion stages. The general structure of the IMC is presented in Figure 2.1.

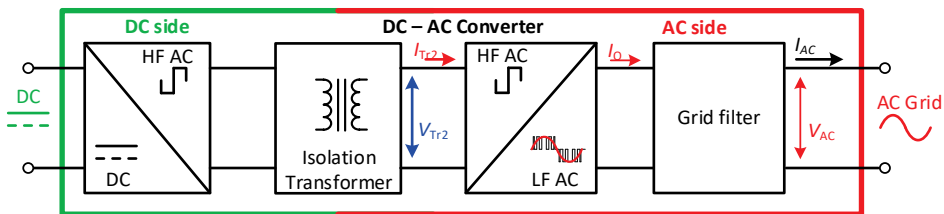


Figure 2.1 General structure of the IMC [1].

Starting from 1990s, more than 30 topologies have been reported as a result of the research and development of the IMCs; a review is presented in [1]. In the 1990s, the topologies based on thyristors and IGBTs were proposed, with the operation frequencies up to 20 kHz. At that time, the available components and quite complex control limited demonstration of high efficiency, which usually did not exceed 90% [14]. The main research trends in the IMC topologies were dedicated to converter circuit aspects, the optimization of the components (used semiconductors, transformer, grid filter, etc.), optimization, and improvements in the switching conditions of the semiconductors, losses in passive components based on existing industrial technologies. As a result, continuous improvements in converter efficiency were achieved. Other research efforts were focused on the implementation of the rectifier operation mode and modulation methods thereof. Besides, the interest of researchers was directed toward the synthesis of new modulation techniques that either utilized parasitic components for soft switching or minimized their influence on the converter operation as some of them are unavoidable, e.g., leakage inductance, the parasitic capacitances of the transformer, semiconductors, and PCB, etc. These improvements, together with developments in the technologies of the semiconductor components and magnetic materials, enabled the use of significantly increased switching frequencies (up to 200 kHz, which could be potentially increased further with the utilization of the GaN semiconductors), improved power density resulting from the reduced size of the magnetic components. Moreover, today's IMC efficiency is close to 96%, for example, in [15], [16], which now is comparable and sometimes superior to the two-stage conversion systems. Nevertheless, various design challenges related to IMCs still exist; the majority of them are related to the optimization of switching sequences, improving

the converter efficiency, and switching conditions for semiconductors, and consideration of transformer design.

The applications of the IMC are various and span from the low voltage and power [16], [17] to high voltage and high power converters [18]-[21], which show the versatility of this power conversion technology. The most prominent applications include uninterruptible power supplies [14], photovoltaic microinverters [16], [17] and inverters [22], fuel cells [23], Li-ion battery storages [24], electric vehicle charging [20], railroad [25], and electric drives [26]. It is worth mentioning that three-phase implementation of the IMCs could be used in applications where operating power exceeds the limit of single-phase systems (typically, 16 A per phase in residential and small commercial settings).

The study [1] proposed the classification of the existing IMC topologies shown in Figure 2.2. The topologies can be divided by type – current source and voltage source converter based IMCs. In the current source converter-based topologies, the current flowing through semiconductors in the AC-side  $I_o$  is continuous, and the grid filter is usually of LC- or LCL-type. On the contrary, in the voltage source converter-based topologies, the AC-side diagonals are commutated with certain dead-time intervals, the current through the semiconductors  $I_o$  is discontinuous, and usually a CL-type filter is used. Secondly, the IMCs are classified in terms of the presence of the resonant tank in the topology. Thirdly, the division by the configuration of the topology type is performed. It comprises different topology types, including the variety of bridge, half-bridge, and push-pull configurations. Finally, the classification includes the existing modulation strategies.

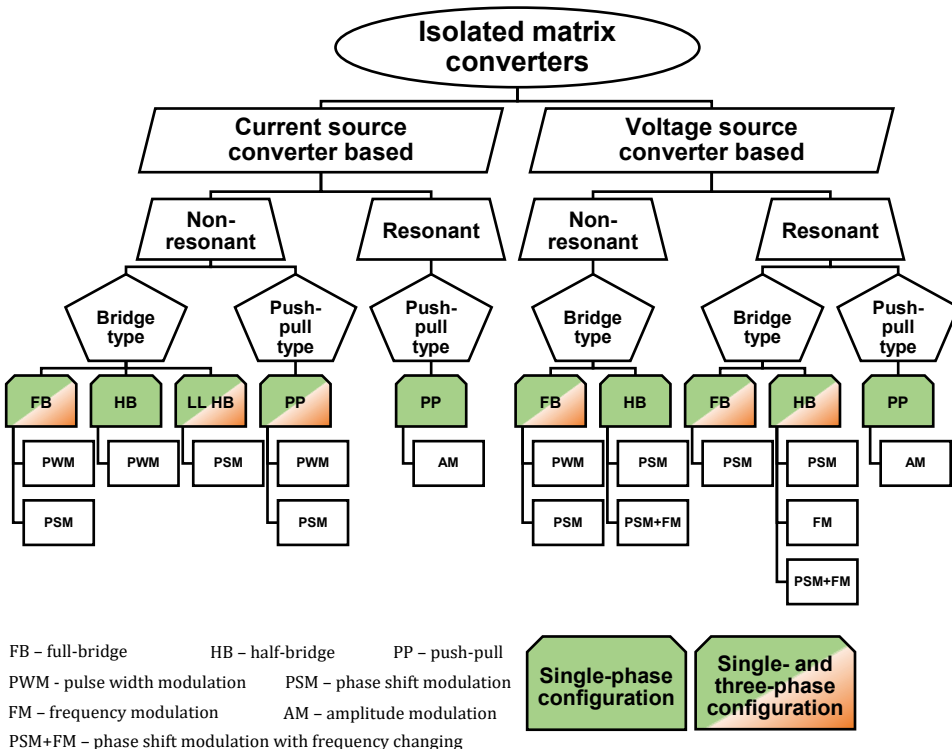


Figure 2.2 The classification of the IMCs [1].

In this work, the research is focused on the FB IMC, which is shown in Figure 2.3. In the current research the different prototypes with different DC voltages (48, 350, 400) and transformers (1.1:1, 1:10) were built and studied. This topology consists of two FB switching stages. The DC-side voltage source bridge utilizes the unidirectional semiconductors  $T_1 - T_4$ . The AC-side is represented by the bridge with the bidirectional semiconductors  $S_1 - S_4$ , connected to the HFT. The capacitor  $C_{DC}$  is used for damping the double grid frequency current ripple. The LCL filter is used for the grid connection, which allows providing a lower current ripple magnitude and current sensing with one current sensor [27], [28]. The topology is suitable for an extensive range of power and voltage levels [16]-[26] and features a number of possible switching states, which allow using various modulation strategies [15], [16], [23], [25]. The main research directions for this topology include improvement of the switching transients to reduce losses and voltage overshoots across semiconductors (using sophisticated modulation strategies and topology modifications), optimization of the transformer parameters and implementation of different semiconductor technologies.

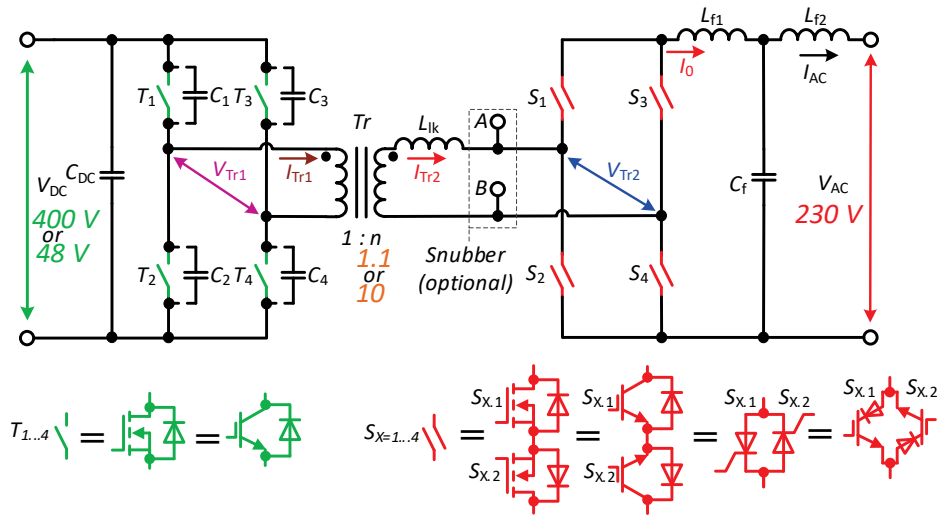


Figure 2.3 The current source converter based FB IMC topology.

## 2.2 Modulation Methods

Most of the IMCs topologies today feature soft-switching or partial soft-switching of almost all semiconductors, achieved with the utilization of special modulation strategies.

For forming the output voltage, the sinusoidal modulation strategy can be used in the DC- or AC-side of the FB topology. In the case of the DC-side modulation (also referred to as primary side modulation), the sinusoidal output is formed by modulation based on the PWM [16] or PSM [23], which is applied to the DC-side semiconductors. At the same time, the AC-side semiconductors could also have a special modulation utilized for the rectification of the modulated shape of voltage/current. The second, more widely addressed modulation method is applied to the AC-side semiconductors (also referred to as secondary side modulation). In this case, the DC-side semiconductors work with the constant duty cycle resulting in fixed duration high-frequency pulses applied to the HFT. The PWM [15] or PSM [25] is applied to AC-side semiconductors, which are forming the

sinusoidal voltage and current. Hence, a control system for an IMC could contain main and auxiliary modulators. The main modulator is controlled in a closed-loop to ensure the IMC output follows the reference sinusoidal signal. In contrast, the auxiliary modulator usually provides fixed periodic gating signals synchronous with the carriers of the main modulator.

To control the value of the duty cycle or phase shift of the main modulator, a voltage/current controller with feedback is required (Figure 2.4). This controller defines the shape of the input modulation signals for the main modulator. Typically, the sinusoidal reference and the feedback from the converter output are given to the controller inputs. The main modulator defines the gating signals for the semiconductors based on the main controller input signal. Single-phase systems typically utilize sinusoidal modulation [14], while both sinusoidal and space vector modulation was addressed for three-phase systems [30]-[32]. Moreover, recently the model predictive control was proposed for voltage source IMC [33].

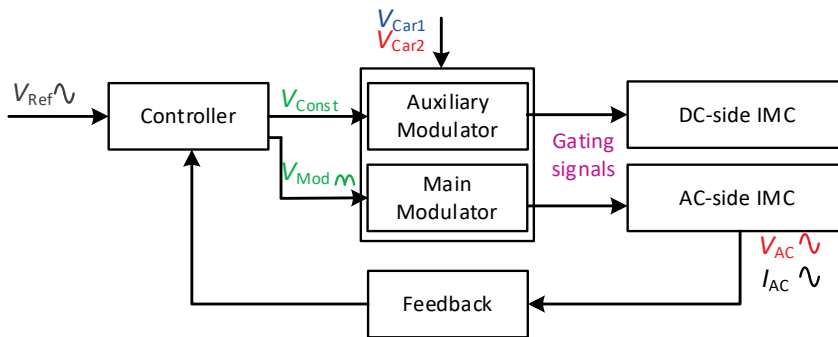


Figure 2.4 General representation of the control system for the IMC.

One of the challenges of the current source IMCs is that the transformer leakage inductance and the output filter are acting as two current sources during switching transients. The current mismatch between the inductances creates high voltage spikes across the AC-side semiconductors [II]. Adding the commutation overlap to these semiconductors allows to achieve the ZCS turn-off [15], [16], [25]. The paper [III] provides a comparison of the modulation methods presented in [15], [25], and the extended version of the method [34], focusing on the analysis of transient intervals, regulation range and power losses.

The study in [15] proposes two methods utilizing the unipolar sine PWM. These methods differ in the number of semiconductors working either at high or low frequency, at the same time achieving the ZVS in DC-side semiconductors and ZCS in the AC-side semiconductors. In one of them, four of the AC-side semiconductors operate at grid frequency. To achieve the ZCS in the semiconductors in the AC-side, the leakage inductance current must decrease to zero before the semiconductors are gated to turn off. To achieve ZVS in the DC-side, the output capacitance of the semiconductors should be discharged, allowing the body diodes to start conducting current before the semiconductors is gated to turn on. These soft-switching conditions are limited to a certain current value, and thus, soft-switching is lost around the grid current zero-crossing point. The second method is based on the same principle, with six AC-side semiconductors operating with switching frequency, while the other two operate at grid frequency. In this case the synchronous rectification is provided, improving the efficiency of the IMC.

The paper [16] proposed a PWM based modulation method for the DC-side semiconductors. In this case, the AC-side semiconductors operate as a rectifier, where two of the semiconductors are working at grid frequency, and all other at the switching frequency. Similar to the previously described methods, the value and slope of the leakage inductance current determine the duty cycle required for the ZCS of the AC-side semiconductors, while ZVS can be lost near the grid current zero-crossing point. These issues can be alleviated with the specific design of the transformer and precise control of switching sequence time intervals for all semiconductors. For operation with the non-unity PF, an active flyback-type snubber is utilized. Also, in [16], an evaluative comparison with the methods from [15] and [23] is presented.

The study [25] proposed the PSM based modulation based on the utilization of a quasi-resonant switching state, which allows recharging the parasitic capacitances of the semiconductors (together with external snubber capacitances) at the DC-side, when the current in the circuit is relatively small. This state is introduced near grid current zero-crossing points for achieving the ZVS in the DC-side semiconductors. At the higher values of the current, another PSM modulation is applied, which means that this method utilizes the multimode modulation. The control system must select an appropriate modulation method on-line, which increases the complexity of the converter control.

Existing methods of providing non-unity PF operation involve the use of an additional active snubber. Despite providing additional functionality, like voltage overshoot reduction across the AC-side semiconductors [16],[35], such active snubbers require sophisticated control and add significant complexity to the topology. Subsection 3.3 proposes a method aimed at simplifying the control system and allow to avoid the additional active snubber.

## 2.3 Design Considerations

### Transformer

The HFT is one of the most important components of the IMC, whose design needs special care to ensure the desired performance of the converter. The general design challenges of the HFT for IMC are as follows: the core losses from the eddy currents and magnetic hysteresis losses, the high-frequency losses due to the skin and proximity effects in the transformer windings, losses of the winding connectors in the case of the high current application, inter-winding capacitance and leakage inductance. The impact of the transformer losses on the total power loss of the IMC is mostly determined by the operating frequency. In the case of frequencies around or below 20 kHz, mostly GTOs and IGBTs are applied, and their switching losses mostly determine the total power losses of the IMC. At higher switching frequencies, the Si and SiC MOSFETs are mostly utilized, and the impact of the losses in transformer on the total power loss is increased.

The isolated power electronic converters generally utilize the ferrite core with RM or PQ shape for converters of up to 1 kW of power and EE or toroid cores for the higher power applications. The improvement can be achieved with the utilization of advanced magnetic materials. For example, the nanocrystalline and amorphous materials can be used, which can reduce the volume but increase the cost of the transformer [39], [40].

For the IMCs with voltage gain close to unity, the transformer designs with good trade-off between various constraints can be relatively easily achieved [15]. On the other hand, for transformers with high step-up ratio, the problem of increased leakage inductance becomes much more prominent and more sophisticated design is required to obtain optimal characteristics. In this thesis several transformers with high turn ratio design were build and evaluated to further extend the potential application range of the IMCs.

## Semiconductors

Research in the IMC topologies has benefited from improvements of the power semiconductor technology – from the silicon GTOs and IGBTs to MOSFETs and WBGs. New manufacturing and packaging technologies of the semiconductors allow for the increase of the switching frequency and reduction of the switching and conduction losses in the semiconductors and reverse recovery losses in the diodes. The FB IMCs require many semiconductors due to the bidirectional voltage blocking requirement of switches in the AC-side, which are usually formed by two identical semiconductors with the anti-series connection. However, in fact the total number of semiconductors is similar to the accepted and widely used two-stage topology solutions. Recent developments of the single-chip reverse and bidirectional blocking semiconductors opened up the new possibilities of the industrial implementation of the IMC, due to the capability of reducing the number of series-connected AC-side semiconductor components by a factor of two. The relevant technologies for the Si, SiC, and WBG semiconductors has been reported in [41]-[44].

Figure 2.5 shows the existing current and voltage limits of the various reverse blocking semiconductors available from Mitsubishi (reverse blocking thyristor), ABB (reverse blocking insulated gate commutated thyristor), Infineon (electrically triggered thyristor), Dynex (reverse blocking thyristor), IXYS, and Fuji Electric (RB-IGBT). In section 4, the feasibility and benefits of the RB-IGBTs will be described for the IMC.

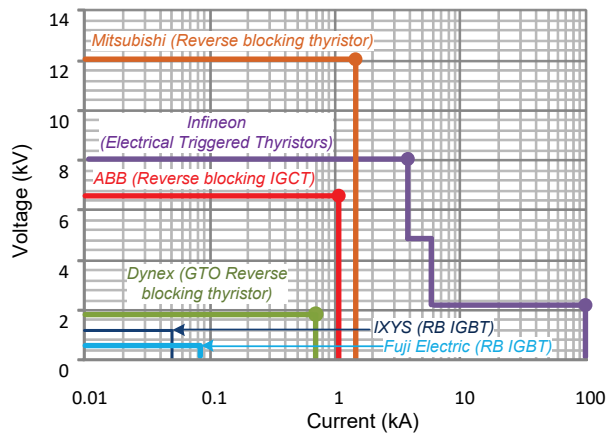


Figure 2.5 General voltage and current ratings of different reverse blocking semiconductor technologies [45].

## Snubber circuits

One of the challenges in the IMC is that the AC-side FB works as a current breaker between the leakage and the output filter inductances and could create the current mismatch and voltage overshoots. Utilizing the ZCS at the AC-side using special modulation methods allows to partially solve the problem. However, the resonance process between the leakage inductance and parasitic capacitance is still present in the circuit. It could cause the avalanche effect in the semiconductors, increasing the total power losses and decreasing the reliability. Figure 2.6 shows different snubber circuits, which are connected to the transformer AC-side terminals for the voltage overshoot reduction. Passive snubbers (a) and (b) provide the heat dissipation from resistance,



which deteriorates the converter efficiency, while active snubber (c) and (d) allow regeneration of the oscillatory energy to the DC-side. The paper [II] presents the comparison of various snubber circuits for the IMC.

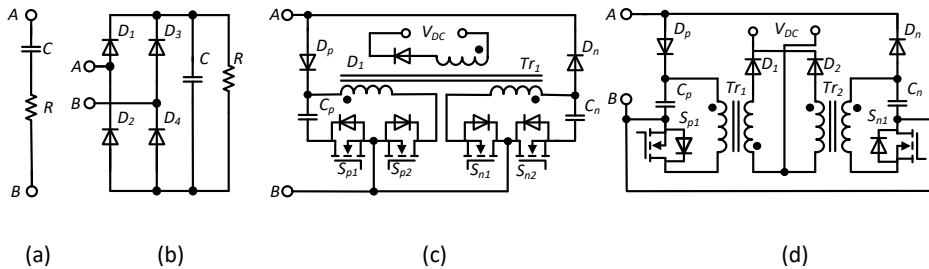


Figure 2.6 Different snubber circuits for clamping voltage overshoots in IMC: passive (a, b) and active (c, d).

## 2.4 Generalizations

This section described the current state of the art of the existing IMCs. The main highlights are the following:

- The classification of the existing IMCs based on the AC-side topology type is proposed. It provides systematization of the existing state-of-the-art in the field and highlights their typical applications, advantages, and constraints.
- The existing modulation strategies for the FB IMC do not usually provide ZVS conditions for the whole fundamental grid period and further research and improvements in the area of modulation strategies are possible.
- The operation with non-unity PF is generally supported with additional circuits (active snubbers) that increases the overall complexity of the IMC. Further research is necessary to cease this requirement.
- The HFT and the AC-side semiconductors are among the most critical components of the IMC. The design of the HFT should meet a number of design constraints for achieving the optimal operation of IMC, particularly in high step-up application. From the power semiconductor point, solutions aimed for reduction of number of series connected devices for reduction of on-state losses need to be evaluated.

### 3 New Modulation Methods for IMCs

In the previous section, the FB IMC topology and associated design constraints were described and highlighted. One of the possible options to improve the switching sequences and reduce the influence of the parasitic parameters is the utilization of special modulation strategies, which allows providing the soft-switching conditions and reduction of the voltage overshoots. Sections 3.1 and 3.2 will describe the new proposed modulation methods for the inverter and rectifier operation modes with the unity PF. The subsection 3.3 presents the operation of the IMC in the case of the non-unity PF.

The new inverter modulation method described in subsection 3.1 uses the constant duty cycle to control the DC-side semiconductors, while the output current is formed by the PSM applied to the AC-side semiconductors. The proposed method allows ZVS in the DC-side semiconductors during the entire grid frequency period. Moreover, it reduces the turn-off losses by adding the lossless snubber capacitor to the DC-side, without the requirement of additional active components or increased switching frequency. This method allows regulation with a single control variable throughout the whole grid frequency period and does not require the multimode operation, as in the previously presented modulation methods [25]. In the AC-side, two semiconductors are switched with the fundamental grid frequency, while in all the other operate at the switching frequency with ZCS. The proposed method is described in detail in [IV].

Subsection 3.2 describes the modulation method for the rectifier mode, which is also based on the modulation applied to the AC-side of topology and described in detail in [IV]. Unlike other methods that require the additional active snubber [35] circuit or the double switching frequency [48], the proposed method can utilize only a passive snubber capacitor across the DC-side semiconductors and provide ZVS at the DC-side throughout the whole grid frequency period.

Subsection 3.3 describes the operation of the converter in the case of non-unity PF and allows for operation with capacitive or inductive loads.

For the verification of the proposed methods, the simulation model in the PSIM software was created. The model is based on idealized components, but includes the on-state resistances of semiconductors, their parasitic capacitances, and transformer leakage inductance, to reflect the parasitic oscillations in the topology. Detailed specifications of the converter are presented in Table 1.

For the experimental verification of the proposed methods, a converter prototype with a rated power of 1.2 kW was built (Figure 3.1, Table 1). For simplicity of design and analysis, the prototype is based on the transformer with the turns ratio close to unity. During the tests, the converter was powered by TDK-Lambda power supplies and the converter output was loaded by the resistive or resistive-inductive load. The experimental waveforms were acquired using the Tektronix MS04034B digital oscilloscope with the Rogowski coil current probe PEM CWTUM/015/R, current probe Tektronix TCP0030A, and the differential high-voltage probes Tektronix P5205A.

Table 1. Specifications of the case study converter

Parameter	Symbol	Value, type
DC-side voltage	$V_{DC}$	400 VDC
AC-side voltage	$V_{AC}$	230 VAC
Switching frequency	$f_{sw}$	50 kHz
Transformers turns ratio	$n$	1:1.1
Rated power	$P_{rated}$	1.2 kW
Snubber capacitor	$C_s$	3.3 nF
Leakage inductance	$L_{eq}$	5.1 $\mu$ H
Magnetizing inductance	$L_m$	10 mH
Parasitic capacitance of AC side semiconductors	$C_p$	60 pF
Filter inductors	$L_{f1}, L_{f2}$	1 mH; 0.4 mH
Filter capacitor	$C_f$	0.47 $\mu$ F
SiC MOSFET	$T_1..T_4,$ $S_1..S_4$	C3M0280090D $V_{DS} = 900$ V, $I_{DS} = 11.5$ A, $R_{DS} = 280$ m $\Omega$ , $C_{OSS} = 20$ pF

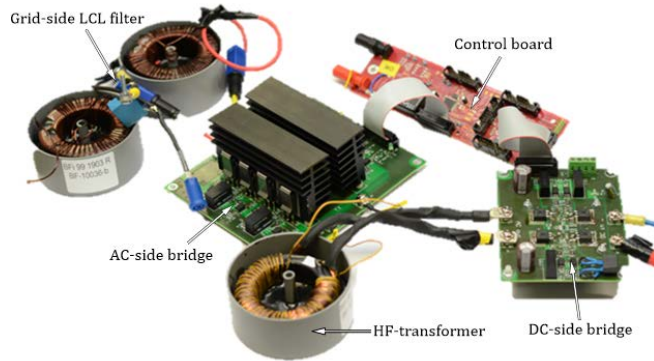


Figure 3.1 Photo of the experimental prototype for verification of the proposed modulation methods.

### 3.1 New Modulation Method for Inverter Operation Mode

The main novelty of the proposed modulation method is that it ensures the ZVS in the DC-side semiconductors during the whole grid frequency period. Moreover, it allows to reduce the turn-off energy losses in the DC-side semiconductors with the utilization of the capacitive snubber across these semiconductors. The motivation for the development of this method was to overcome the following drawbacks: the existing methods require quite complex multimode control [25] or have the problem with ZVS near the zero-crossing point [15]. The benefits of the proposed method are:

- ZVS in the DC-side semiconductors during the whole grid frequency period, even with the utilization of the snubber capacitor across the DC-side semiconductors for their turn-off loss reduction;
- two of the eight semiconductors in the AC-side are switched with the grid fundamental frequency;
- no requirement for the external active clamping circuits across the HFT.

The design constraints are in the optimization of the circulation current when converter is operating with the light load, and the requirements of the special type of the capacitors across DC-side semiconductors, such as COG/NPO, for example, with lower resistance and capacitance drift and more stable dielectrics. The detailed description of the proposed method is presented in [IV]. The next switching states (Figure 3.2a) can be:

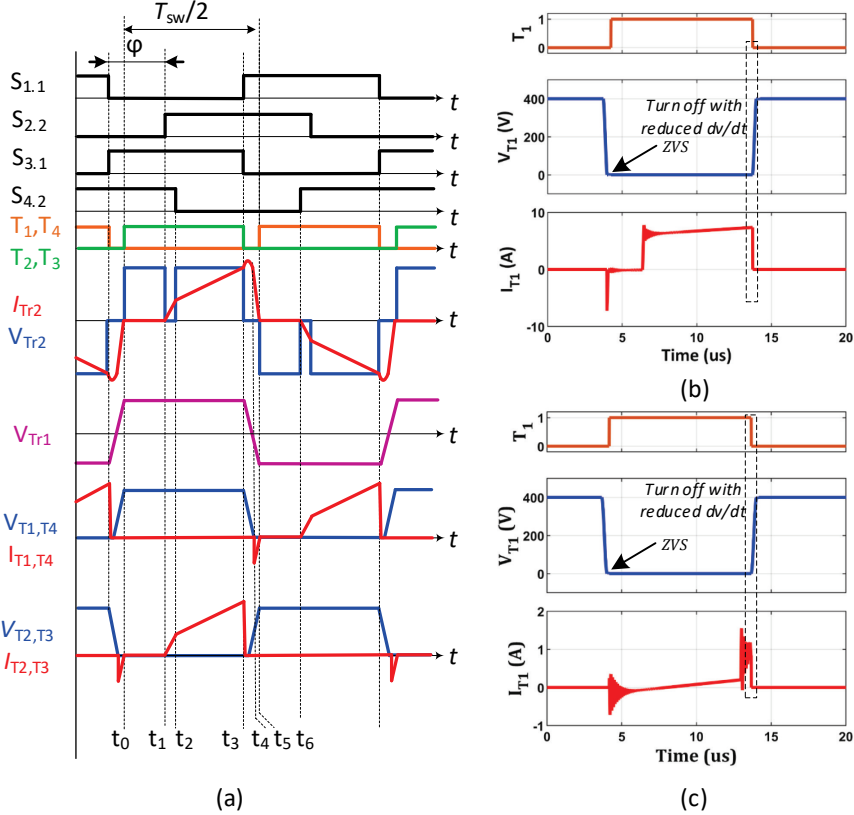


Figure 3.2 The generalized waveforms of the proposed inverter operation mode (a) and simulated ZVS transient of the semiconductor  $T_1$  with  $I_{AC}$  at amplitude value (b) and close to zero (c) [IV].

- $t_0 - t_1$ : The  $T_2, T_3, S_{3,1}, S_{4,2}$  are conducting and converter in freewheeling state. The current freewheeling in semiconductors  $S_{3,1}, S_{4,2}$  and load.
- $t_1 - t_2$ : The  $S_{2,2}$ , is turn on and converter in active state, the current redistributed between  $S_{4,2}$  to  $S_{2,2}$ .
- $t_2 - t_3$ : The  $T_2, T_3, S_{2,2}, S_{3,1}$  are conducting, while others are in the off-state. The converter in the active state, power is transferred from the DC-side to the AC-side through the semiconductors  $T_2$  and  $T_3$ .
- $t_3 - t_4$ : The  $T_2, T_3$ , are turned off, while  $S_{1,1}$  is turned on, the resonance between the  $C_{eq}$  ( $C_{eq} = C_s \cdot n^2$ ) and  $L_{lk}$  appears. The circulation current is added to the load current  $I_{AC}$  and it reduces the time for the recharging  $C_{eq}$  and, at the same time, the value of the transformer voltage  $V_{Tr1}$  changes polarity and is reducing.
- $t_4 - t_5$ : The resonant process continues, while the resonant current starts to decrease. The snubber capacitors of the  $T_1, T_4$  and their body diode forward biased and

taking  $I_{AC}$ , which start decreasing and transferred from the  $S_{3.1}$  to  $S_{1.1}$ . Starting from this point  $T_1$ ,  $T_4$  can be turned on with ZVS.

$t_5 - t_6$ : The converter enters the freewheeling state when current of the body diodes of  $T_1$ ,  $T_4$  reduces to zero.

The converter operation continues with the analogous sequence during the other half of the period.

To demonstrate the ZVS capabilities, in the PSIM simulation the snubber capacitor  $C_s=3.3$  nF was used for the DC-side semiconductors. In Figure 3.2b, the simulation of the switching transient on the example of the DC-side transistor  $T_1$  is shown. As demonstrated, the proposed method allows to fully discharge of the semiconductor output capacitance together with paralleled snubber capacitor during a relatively short time and provide the ZVS. The method is independent of the amount of the current present in the circuit and achieves ZVS even near the zero-crossing point of the output current (Figure 3.2c). Figure 3.3 presents the experimental waveforms, which confirm the simulation results; the voltage at the output has low distortion, and the zero-crossing point is free of distortions.

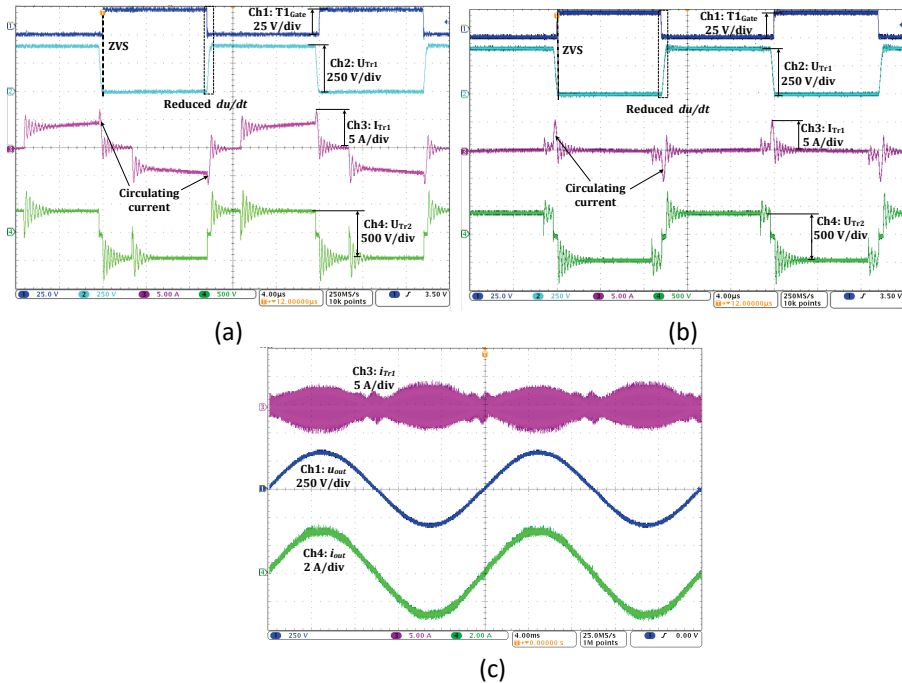


Figure 3.3 Experimental verification of ZVS transient of the semiconductor  $T_1$  at  $I_{AC}$  at amplitude value (a) and close to zero (b); the experimental waveforms for two fundamental grid period(c) [IV].

### 3.2 New Modulation Method for Rectifier Operation Mode

The novelty of the new modulation method for the rectifier mode is that this method provides ZVS and reduces the turn-off energy losses, similarly to the inverter mode presented in the previous section. The motivation for the development of this method lies in the general lack of research in area of modulation methods for the rectifier mode and significant disadvantages of the few existing ones: dependency on the active

snubbers or operation with double switching frequency [35],[49],[48]. The benefits and challenges of the method are similar to the ones of the inverter modulation method. A detailed description of the proposed method for the rectifier operation mode is presented in [V]. The next switching states (Figure 3.4a) can be:

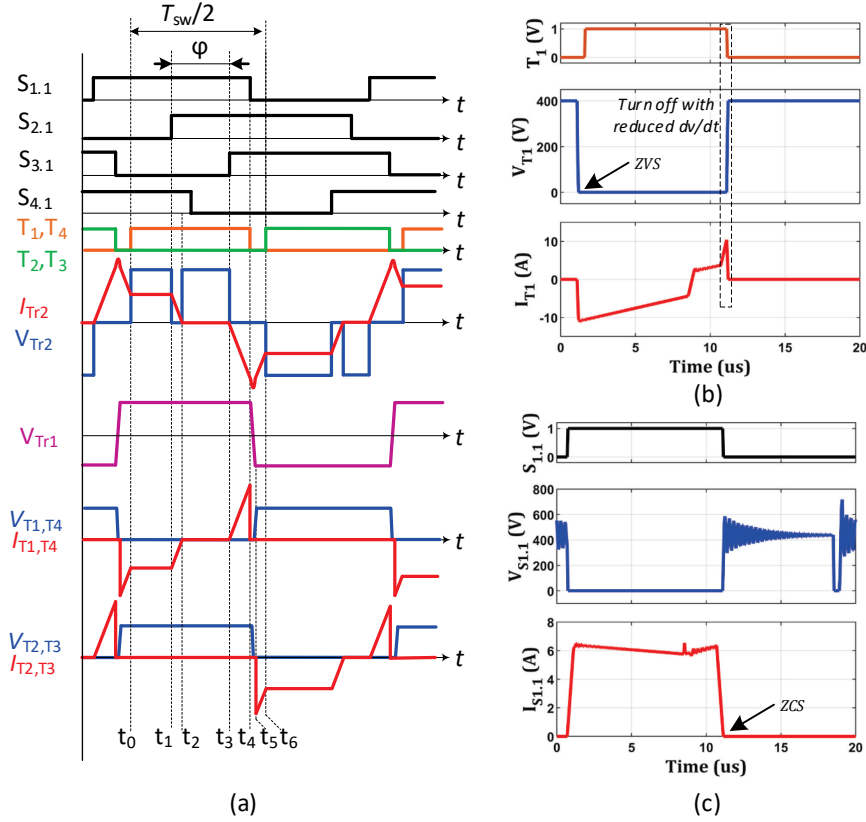


Figure 3.4 The generalized waveforms of the proposed rectifier operation mode (a) and simulated ZVS transient of  $S_{1.1}$  (b) and  $T_1$  (c) at the amplitude of  $I_{AC}$  [V].

- $t_0 - t_1$ : The  $S_{1.1}$ ,  $S_{1.2}$ , and  $S_{4.1}$  are conducting, while others are in the off-state. In the converter in the active state, power is transferred from the AC-side to the DC-side through the semiconductors  $T_1$  and  $T_4$ , which turn on with ZVS.
- $t_1 - t_2$ : The transition interval starts with the turn-on of the  $S_{2.1}$ . The voltage polarity of  $L_{f1}$  is reversed, and the current  $I_{Tr2}$  is decreasing during the time while the  $V_{Tr2}$  is zero.
- $t_2 - t_3$ : The current in the  $S_{2.1}$  and  $S_{2.2}$  reaches the inductor  $L_{f1}$  current level, the transition interval is finished, when the, and  $V_{Tr2}$  increases to the amplitude value.
- $t_3 - t_4$ : The  $S_{3.1}$  turns on, the second transition interval starts. The current in the  $S_{3.1}$ ,  $S_{3.2}$ ,  $T_1$ ,  $T_4$  starts to rise, while in the  $S_{1.1}$ ,  $S_{1.2}$  decreases.
- $t_4 - t_5$ : The current  $I_{Tr2}$  is rising more than  $L_{f1}$  current, the semiconductor  $S_{1.1}$  is turned off with the ZCS along with  $T_1$  and  $T_4$ . The resonant interval starts, and the snubber capacitor  $C_s$  recharges, while the  $V_{Tr1}$  is changing polarity.

$t_5 - t_6$ : The snubber capacitors are recharged, the  $V_{Tr2}$  reaches a peak value, and at the moment  $t_6$ , the converter starts to operate in the active state with other diagonal in the DC-side.

The converter operation continues with the analogous procedure in the other half of the period, where semiconductors  $S_{2,1}$  and  $S_{4,2}$  are in one state, and the modulation is applied to other semiconductors correspondingly.

The PSIM simulation of the switching waveforms is shown in Figure 3.4b for the positive half-period. It presents the switching transient of the  $S_{1,1}$  turn-off with ZCS. The reverse recovery losses are also reduced since  $L_{lk}$  limits the current  $di/dt$ . The other AC-side semiconductors also operate either with ZCS or in synchronous rectification mode. At the DC-side, the semiconductors transfer active power through the antiparallel diode or operate with synchronous rectification with the ZVS turn on transient. After the end of the boost interval, the current is reversed for a short time to provide ZCS for another semiconductor diagonal (Figure 3.4b). The experimental waveforms of the switching transients of the  $S_{1,1}$  and  $T_1$ , voltages and current across the transformer and the input-output waveforms are presented in Figure 3.5.

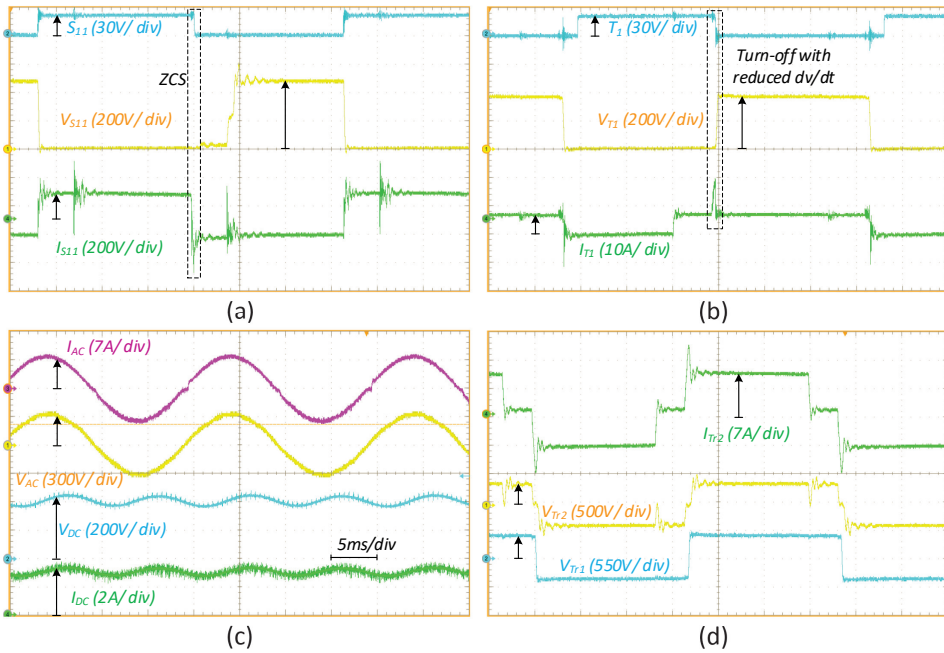


Figure 3.5 Experimental verification of transient of  $S_{1,1}$  (a) and  $T_1$  (b), experimental waveform at grid period (c) and current  $I_{Tr1}$  and voltages  $V_{Tr1}$ ,  $V_{Tr2}$  across the transformer (d) [V].

### 3.3 Operation with Non-unity PF

The modulation methods presented in subsections 3.1 and 3.2 allow the IMC to achieve ZVS together with soft turn-off at the DC-side without active snubber circuits, by using lossless snubber capacitors. The methods were verified with simulations and experimentally for unity PF. This section will describe how the IMC can operate with non-unity PF by taking advantage of the combination of previously presented methods. In this mode, an IMC is connected between the source on the DC-side and the utility grid

on the AC-side. This functionality is essential for the converter in order to enhance its functionality and be capable of providing ancillary services, such as power factor correction [35]. Previously, only few studies have reported IMC concepts capable of such functionality, where it was achieved by the use of an active snubber circuits [16],[35] and the multimode control operation [37]. The novelty of the proposed unified approach is the possibility of the power factor correction without the need for the additional active snubber circuit in the IMC. The challenge is attributed to the requirement of quite a fast and precise control system to achieve a better current transient in the zero-crossing point where the current changes its polarity.

The converter operation is represented by four modes, depending on the utility grid's current and voltage (Figure 3.6a) [37]. In mode 1, the voltage and current  $V_{AC} > 0, I_{AC} > 0$ , and the energy is flowing from the DC source to the grid and the IMC operates as an inverter during the positive half period. Mode 2 denotes an operation, where the voltage and current are negative  $V_{AC} < 0, I_{AC} < 0$  and the IMC operates as an inverter during the negative half period. Both of the converter operations are similar to the inverter mode in the case of the unity PF. In mode 3, the current and voltage have the opposite signs, and the converter operates in the rectifier mode ( $V_{AC} > 0, I_{AC} < 0$ ); in this case, the operation is identical to the negative half period of the rectifier. In mode 4, the voltage and current also have the opposite signs ( $V_{AC} < 0, I_{AC} > 0$ ), and another rectifier mode is applied. Therefore, the converter can operate with any PF value, assuming that an appropriate sequence of the operating modes is selected. An example of an operation with an inductive load is illustrated in Figure 3.6b.

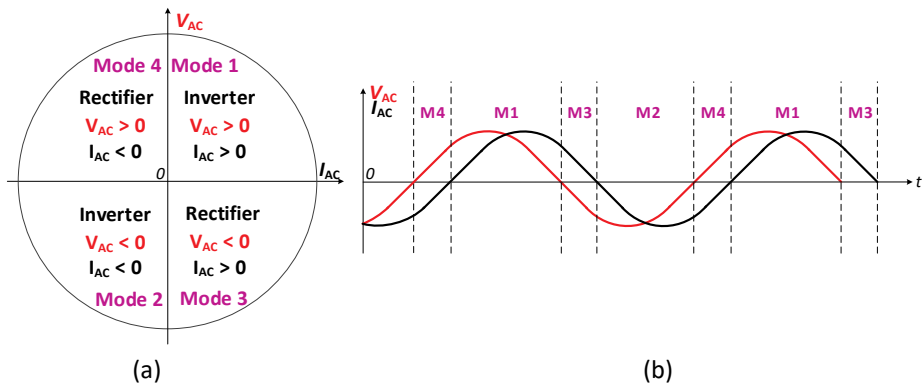


Figure 3.6 Operation modes (a) and the generalized line frequency cycle waveforms (b) in the case of operation with non-unity PF.

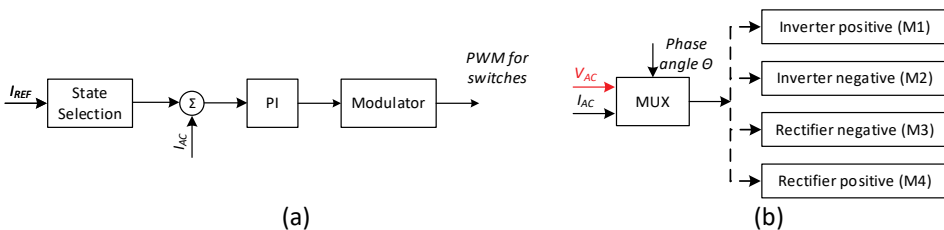


Figure 3.7 The generalized structure of the control system (a) and state selector (b) used for the simulation.



To verify the possibilities of regulation and reactive power injection, a simulation model was created in PSIM. In the unified modulation, the semiconductors  $S_{2,1}$ ,  $S_{2,2}$ , and  $S_{4,1}$ ,  $S_{4,2}$ , are phase-shifted depending on the instantaneous value of the reference current. For the sake of simplicity, no synchronous rectification was applied. The reference current is provided externally, and the mode selector defines the appropriate modulation mode, depending on the value of the reference current and the grid voltage. A PI regulator provides the regulation — the generalized principle of the control model is presented in Figure 3.7. The simulation results for the capacitive (a) and inductive (b) loads are given in Figure 3.8.

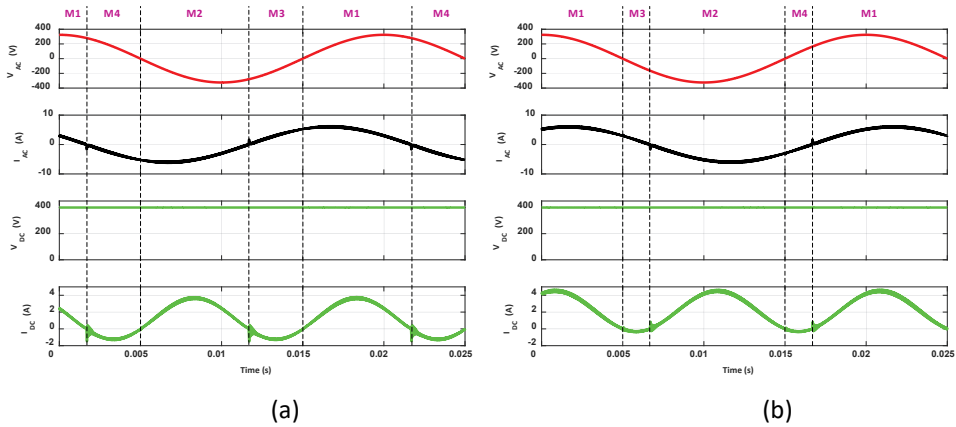


Figure 3.8 The simulation of the operation for capacitive (a) and inductive (b) load.

### 3.4 Generalizations

This section addressed the two novel modulation methods for the IMC, allowing the converter operation in the inverter and rectifier operating modes. The main findings are the following:

1. The proposed modulation methods allow ZVS during the whole grid period and allows to utilize the lossless snubber capacitors across the DC-side semiconductors. Moreover, in each mode two of the eight semiconductors at the AC-side operate at grid frequency.
2. Using the unified modulation, the IMC can operate in four quadrants without active snubbers or semiconductors operating with increased switching frequency.

## 4 Implementation of RB-IGBTs in IMCs

This section focuses on the characterization of the evaluation samples of RB-IGBTs and study of their application feasibility in IMCs. Subsection 4.1 describes the methodology proposed for the characterization of the semiconductors under soft-switching conditions with the utilization of the modified double pulse test method. Subsection 4.2 describes the RB-IGBT evaluation using models created in PSIM Thermal Module and theoretical comparison with the regular IGBTs in the IMC [VI]. Subsection 4.2 presents the verification of regular IGBTs and the RB-IGBTs using an experimental IMC.

### 4.1 Novel Characterization Methodology for RB-IGBTs

Typically, in the switching converters, the main aim is to achieve the optimal trade-off between the conduction and switching losses under certain operating frequencies. In the converters with soft-switching, the main contributors to power losses are the conduction losses. For the RB-IGBTs, the effect of the reverse recovery losses must be considered due to their high impact on the total losses even under soft-switching with the reduced  $di/dt$  [50].

To evaluate the losses in the semiconductors, a double pulse test methodology is commonly used [51],[52]. The main goal is to capture the waveforms during the turn-on and turn-off transients under different operating conditions of the evaluated semiconductor and based in this data calculate the corresponding values of the energy losses as in [45],[53]. Figure 4.1a presents the circuit proposed for the characterization of the IGBT and RB-IGBTs in the IMC. Compared to the common double pulse circuit, in this case, the additional inductor and clamping circuit were added to emulate the soft switching transients in the IMC. Figure 4.1b shows the test samples selected for the characterization. The experimental prototype is shown in Figure 4.2. The  $RB_2$  semiconductor allows obtaining information about turn-on transient, while the  $RB_1$  provides the information during the reverse recovery process. The interval  $t_1$  is adjusted to charge the required current in the inductor, intervals  $t_2$  and  $t_3$  were set long enough to finish the transient process of the switching. The proposed circuit allows external current limiting through the semiconductors. Although, the switching process of the proposed circuit is not fully identical to the switching in the AC-side of IMC, it can emulate the switching transients in semiconductors. The parameters of the test setup are shown in Table 2. The clamp circuit allows providing the required value of  $di/dt$  for the tested device. In this case, with the inductance  $L_{CL}$  and the time changing, we can provide the different values of the current, and tested semiconductors will have the switching transient close to the real condition in the case of the current source IMC topology.

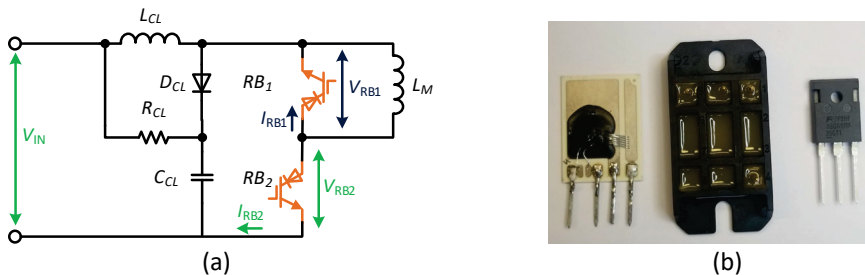


Figure 4.1 The double pulse test circuit (a) and test samples (b) selected for characterization [45].

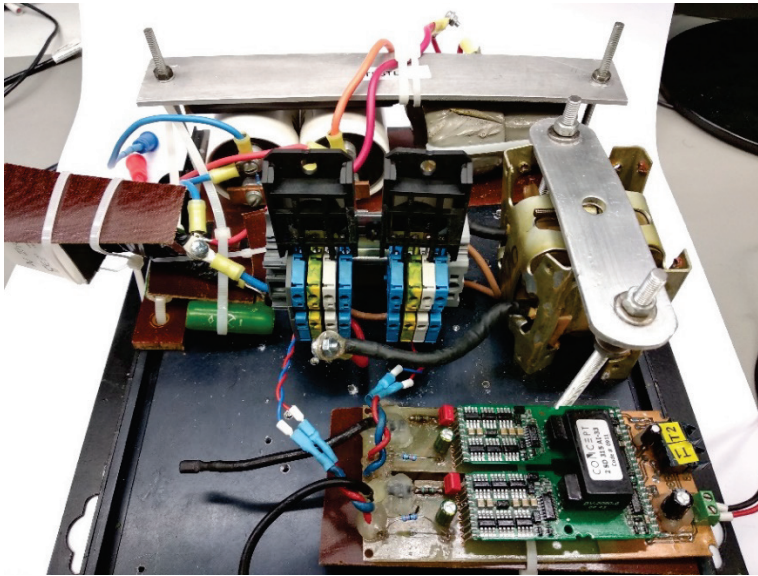


Figure 4.2 The developed double pulse test setup.

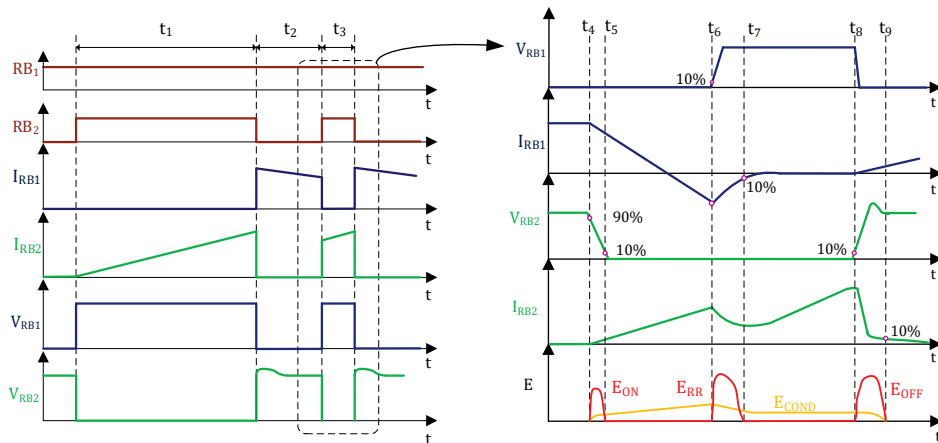


Figure 4.3 The proposed double pulse test methodology.

Table 2. Specifications of the test setup for characterization of RB-IGBTs

Parameter	Symbol	Value, type
Input voltage	$V_{IN}$	600 V
Test current	$I_{RB2}$	5...40 A
Main inductor	$L_M$	744 $\mu$ H
Clamp inductor	$L_{CL}$	5...100 $\mu$ H
Clamp capacitor	$C_{CL}$	470 nF
Clamp resistor	$R_{CL}$	5 $\Omega$
Clamp diode	$D_{CL}$	C4D10120
Gate resistance	$R_G$	33-180 $\Omega$
RB-IGBT	$RB_1, RB_2$	600 V / 85 A

During the time interval  $t_1$ , the inductor is charged up to the desired current value (Figure 4.3) and within the time interval  $t_2$ , turn-on, turn-off, and reverse recovery switching transients are captured. The turn-on energy  $E_{ON}$  of the semiconductor  $RB_2$  can be calculated as:

$$E_{RR} = \int_{t_4}^{t_5} I_{RB2} \cdot V_{RB2} \cdot dt, \quad (1)$$

where  $I_{RB2}$  is the collector current and  $V_{RB2}$  is the collector-emitter voltage of the second RB-IGBT, respectively;  $t_4$  is the time instance when the  $I_{RB2}$  rises 10 % of the constant required steady-state value, and  $t_5$  is the time instance when the  $V_{RB2}$  decreases to 10 % of the nominal input voltage  $V_{IN}$  value for the test. The value of the reverse recovery losses is measured in the semiconductor  $RB_1$  with the analogy to turn-off losses, where  $t_5$  is the time instance when the  $V_{RB1}$  rises to 10 % of nominal  $V_{IN}$  value and  $t_6$  is the time instance when the  $I_{RB1}$  decreases to 10 % of the constant required steady-state value:

$$E_{RR} = \int_{t_5}^{t_6} I_{RB1} \cdot V_{RB1} \cdot dt, \quad (2)$$

The turn-off energy  $E_{OFF}$  of  $RB_2$  can be found as:

$$E_{OFF} = \int_{t_7}^{t_8} I_{RB2} \cdot V_{RB2} \cdot dt, \quad (3)$$

where  $t_7$  is the time instance when the  $V_{RB2}$  rises 10 % of the nominal  $V_{IN}$  value, and  $t_8$  is the time instance when the  $I_{RB2}$  decreases to 10 % of the constant required steady-state value.

The total switching energy dissipated in a semiconductor is defined as:

$$E_{TOTAL} = E_{ON} + E_{RR} + E_{OFF} \quad (4)$$

Energy losses were measured for different samples and under various current  $I_{RB2}$  and the  $di/dt$  values, defined by the inductance to determine the switching loss dependencies. The performance of RB-IGBTs was characterized in terms of turn-on energy ( $E_{ON}$ ), turn-off energy ( $E_{OFF}$ ), and reverse recovery energy ( $E_{RR}$ ). Figure 4.4a compares the power dissipation during the turn-on transition for the sample under different  $di/dt$  values. It is notable that for the hard-switching transition (450 A/ $\mu$ s), the amount of energy losses exceeds 5 mJ and that the implementation of soft-switching reduces these losses by an order of magnitude, even using relatively small clamp inductance. At the same time, further reduction of  $di/dt$  has a minor effect. Figure 4.4b shows energy losses during the turn-off transient. It is not affected by the clamp circuit, and remains significant due to the long tail current, which amount depends on the manufacturing technology [54].

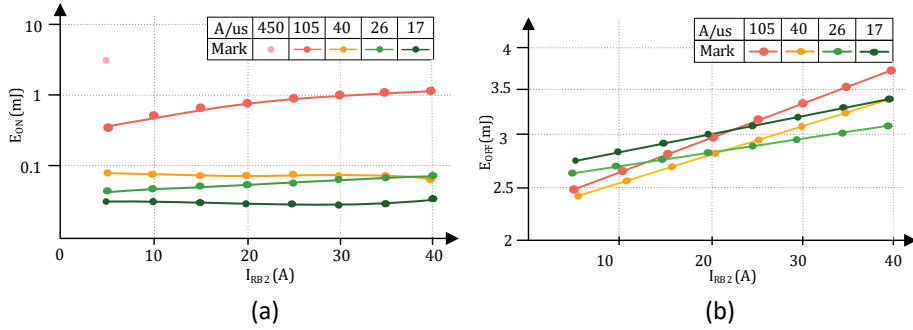


Figure 4.4 Turn-on (a) and turn-off (b) losses under different switching conditions.

Figure 4.5a shows the reverse recovery current under different conditions. As for the typical diode, the higher value of the  $di/dt$  results in higher peak reverse recovery current, while the recovery time is shorter. The initial value of the collector current also affects reverse recovery current and dissipated energy. Figure 4.5b shows the reverse recovery losses under different switching conditions. With the low initial collector current, the reverse recovery losses are similar, while for the higher currents, the lower  $di/dt$  allows decreasing the reverse recovery losses.

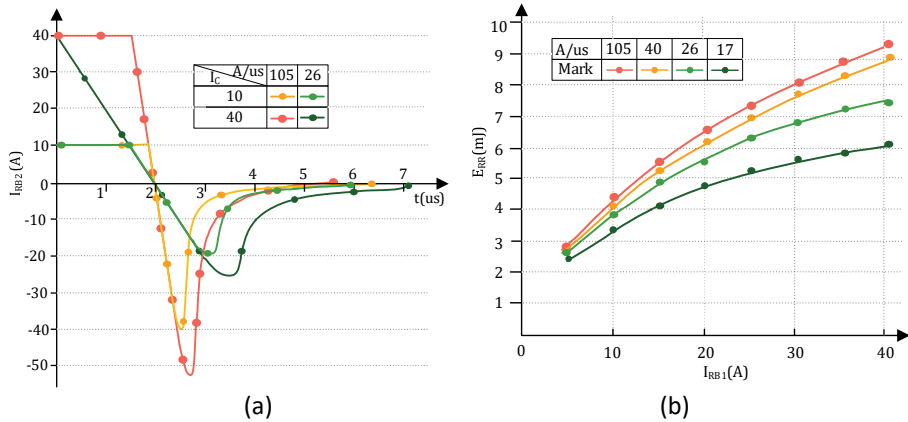


Figure 4.5 The turn-off collector current shape of the different current values (a) and reverse recovery losses (b) under different switching conditions.

## 4.2 Thermal Models of RB-IGBTs

For the verification of the RB-IGBT performance in the IMC, the thermal model of the semiconductors was created in the PSIM Thermal Module software package. The model was based on the data obtained from the evaluation samples of the RB-IGBTs with the modified double pulse methodology described in the previous section. The main aim is used this data to estimate switching and conduction losses as well as overall power losses in the IMC. Also, the simulation model includes the parasitic capacitance and leakage inductance of the transformer, which can influence the switching transient. The estimation was done in the inverter mode, with the modulation method described in subsection 3.1. The comparative analysis was done with regular low loss IGBTs, having similar voltage and current ratings. The summary of the case study system and the components for the converter is presented in Table 3.

Table 3. Specifications of the case study converter with RB-IGBTs

Parameter	Symbol	Value, type
DC-side voltage	$V_{DC}$	350 VDC
AC-side voltage	$V_{AC}$	230 VAC
Switching frequency	$f_{sw}$	20 kHz
Transformer turns ratio	$n$	1:1.1
Rated power	$P_{rated}$	4 kW
Snubber capacitor	$C_s$	0.5...1 nF
Leakage inductance	$L_{eq}$	7 $\mu$ H
Magnetizing inductance	$L_m$	40 mH
Filter inductor	$L_{f1}, L_{f2}$	2.8 mH, 1mH
Filter capacitor	$C_f$	50 nF
DC-side IGBT	$T_{1..T_4}$	IRG7PH30K10DPbF $V_{CE} = 1200$ V, $I_{CE} = 30$ A, $C_{OSS} = 63$ pF
AC-side IGBT	$S_{1..S_4}$	FGH75T65SHDT-F155 $V_{CE} = 650$ V, $I_{CE} = 75$ A, $C_{OSS} = 43$ pF
AC-side RB-IGBT	$S_{1..S_4}$	FGW85N60RB $V_{DS} = 600$ V, $I_{DS} = 85$ A, $C_{OSS} = 74$ pF

Figure 4.6 presents the simulation result of the losses under different switching frequencies. As shown, the RB-IGBTs will have lower losses in IMC with the switching frequency lower than 25 kHz, while the usage of the IGBTs will provide benefits with the higher frequency. The simulation was done with the same output filter, which can also be optimized for the chosen frequency and operating power. Figure 4.7 presents the total power losses in the converter for RB-IGBTs and regular IGBTs under the constant frequency of 20 kHz and power of 3.3 kW. As observed from the graph, in the case of RB-IGBTs at the AC-side, the predominant part of the losses are the switching losses, that also include the diode reverse recovery in the regular IGBTs. At the same time, the amount of the conduction losses is lower compared to the regular IGBTs. In this case, the value of the total losses is higher, which is also confirmed experimentally and presented in the next subsection.

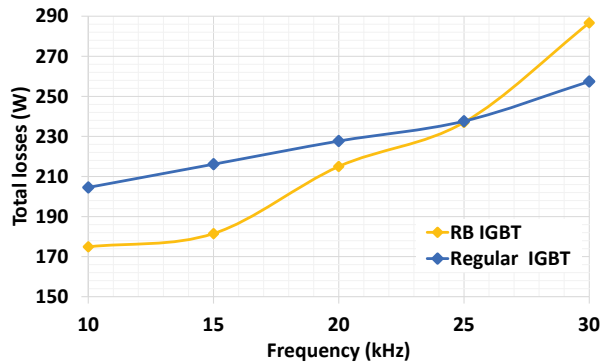


Figure 4.6 The losses of the IMC under constant power (3.3 kW) and at different switching frequencies the RB-IGBT and regular IGBT based prototypes.

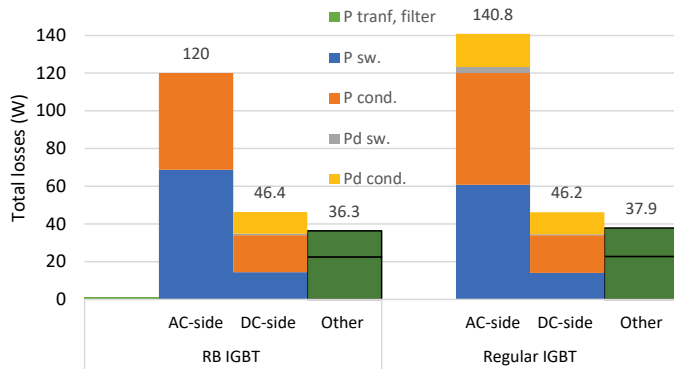


Figure 4.7 The losses of the IMC under constant power (3.3 kW) for the RB-IGBT and regular IGBT prototypes.

### 4.3 Experimental Verification of the 600 V RB-IGBTs

For the practical verification of the simulation models, the experimental converter with RB-IGBTs and regular IGBTs and rated power of 4k W was designed and built (Figure 4.8, Table 3). During the experiments, the converter was supplied by TDK-Lambda power supply and operating with the resistive load. The measurements of the experimental waveforms were done using the Tektronix MS04034B digital oscilloscope with the Rogowski coil current probe PEM CWTUM/015/R, current probe Tektronix TCP0030A, and the differential high-voltage probes Tektronix P5205A.

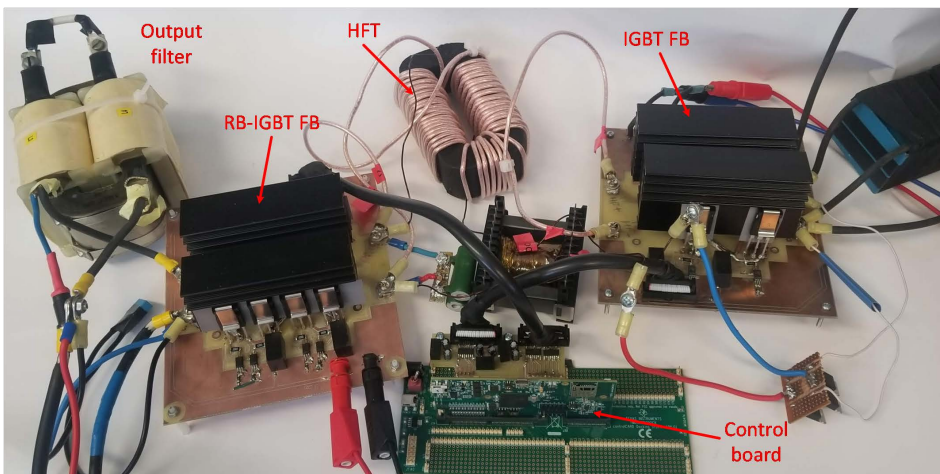


Figure 4.8 Experimental prototype of the IMC with RB-IGBTs.

Figure 4.9 presents the experimental waveforms of the IMC with RB-IGBTs. The results are similar to the simulation result in section 3.1. Figure 4.9a presents the waveforms across the transformer at the amplitude value of the output current, while Figure 4.9b shows those close to the current zero-crossing point and Figure 4.9c presents the output AC waveforms. As observed, the output voltage and current waveforms are distortion-free, proving that the IMC with RB-IGBTs is fully functional.

Figure 4.10 presents the experimentally measured efficiency of the IMC with the RB-IGBTs and regular IGBTs in the AC-side. All other parts of the converter remained the same. As predicted, the implementation of RB-IGBTs results in lower losses at higher power due to the lower conduction losses. As it seen from Figure 4.10, the efficiency trends are growing up to 3500 W, and after that start decreasing. The peak efficiency of the converter is 94 %. At the same time, the efficiency under other frequencies followed the simulation result presented before.

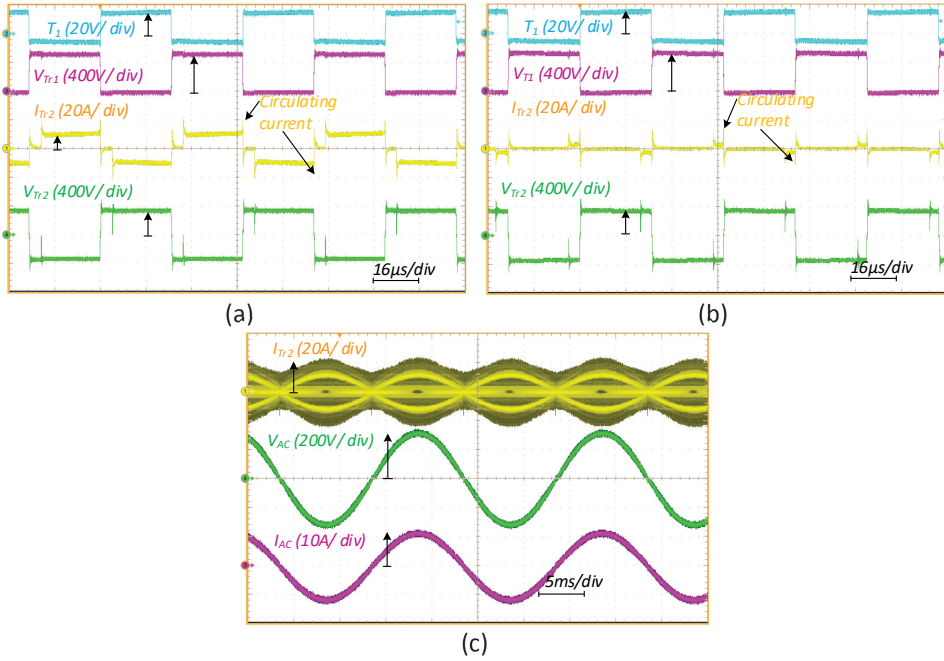


Figure 4.9 The experimental verification of ZVS transient of the semiconductor  $T_1$  at  $I_{AC}$  at amplitude value (a), close to zero (b) and output AC waveforms (c).

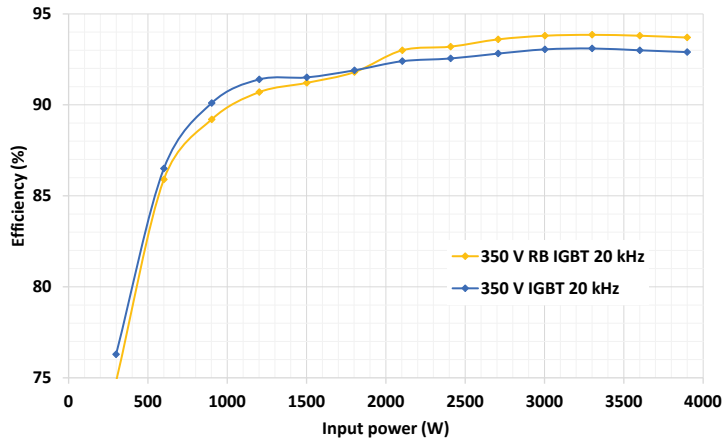


Figure 4.10 Measured efficiency of the IMC with RB-IGBTs and regular IGBTs in the AC-side.



## 4.4 Generalizations

In this section, the application feasibility of RB-IGBTs to reduce the amount of conduction losses in IMC was evaluated. The main outcomes are listed below.

1. The modified double pulse test methodology was proposed. It allows creating the semiconductor switching transients close to the ones that appear at the AC-side of IMC and extract information about the energy dissipated during the turn-on, turn-off, and reverse recovery. Because the method utilizes the impulse current, it is suitable for the test of the non-packaged semiconductor samples.
2. Based on the received data from evaluated samples, the thermal model of the RB-IGBTs was developed in the PSIM software, and the power losses in the IMC were estimated.
3. The 4 kW IMC prototype with RB-IGBT in the AC-side was built and successfully tested, demonstrating the required functionality. The efficiency was compared with the same IMC having regular IGBTs in the AC-side. The RB-IGBTs, as predicted, showed lower conduction losses, which resulted in better overall IMC efficiency at higher power levels, when compared to the regular IGBTs.

## 5 Design and Benchmarking of High Step-Up HFT for IMCs

The presence of a transformer potentially provides a wide range of DC and AC voltages to be matched by the IMC. As mentioned in subsection 2.3, the transformer design is among the issues that must be carefully considered during the design of IMC. The values of the DC- and AC-side voltages provide the required value of the transformer turns ratio and the design with good trade-off between the leakage inductance and the interwinding capacitance allows better switching transient in semiconductors [II]. It reduces current spikes and peak voltage overshoot in the AC-side, which results in converter efficiency improvement.

For simplicity of design, in the previous sections, the ideas were verified with the transformer turns ratio close to 1:1, which assumes interfacing of a rather high voltage (350-450 VDC) source, such as an HV battery, with the grid voltage of 230 VAC. However, if a lower voltage source (24-48 VDC) has to be matched with the same grid voltage level, the IMC based on a transformer with a turns ratio of 1:10 or higher is necessary. This makes the mentioned problem of parasitic oscillations much more pronounced since with the high turn's ratio, increased transformer leakage inductance is much harder to avoid.

One of the challenges in the current-source IMC is related to the voltage overshoots and oscillations at the AC side. A possible way to reduce the amount of this oscillating energy is to minimize the transformer leakage inductance, while keeping the interwinding capacitance low. The modulation methods proposed previously do not require the magnetizing current to provide soft-switching. Therefore, a transformer can be designed with the large value of the magnetizing inductance, which will reduce the circulation current in the topology. Various designs based on different cores could be applied to achieve different sizes/dimensions of the magnetic components. In the current section, several transformer designs with turns ratio of 1:10 are compared for high step-up IMC, which should interface a 48 V DC source with the 230 VAC grid.

### 5.1 Study of Implementation Possibilities of High Step-up HFTs

In the frame of this study a toroidal transformer was chosen as the reference design for IMC. This type is quite popular nowadays due to its high efficiency, compact shape, high working frequencies, and low stray magnetic field [55]. In these applications the Litz-wire is usually utilized to reduce the resistance at high frequency and minimize the skin effect [56]. However, the proximity effect must also be considered due to high  $di/dt$ . The parameters of the reference transformer are shown in Table 4. The transformer uses three Litz-wires with 60 parallel bundles, each having 22 strands in the primary (DC-side) winding connected in parallel, which allows transfer of the high current. The secondary winding (AC-side) consists of 31 turns. The primary Litz-wire winding covers almost the whole toroidal core, while the secondary winding creates the second row with copper wire (Figure 5.5). The manufacturing cost of this transformer type for high current applications could be high due to the specific realization of the primary winding.

Some approaches that allow for reduction of the cost and size of magnetic components are presented in [55],[57]. The planar structure provides effective solutions for various power systems, aiming to minimize the volume of the magnetic elements and increase the converters power density. The other benefit of the planar transformer is that the windings have a flat structure and can be made using the printed circuit board layers or copper foils, potentially reducing the production cost. This approach is also

more suitable for the high-frequency operation because the planar transformer has a lower sensitivity to the proximity effect. The main benefits of the planar structure over the conventional structures are high power density with a low profile, good thermal characteristics, good modularity, and repeatability. The drawback is low copper utilization with a limited number of turns, large footprint and high interwinding capacitance [58], [59].

*Table 4. Specifications of the reference toroidal transformer*

<b>Parameter</b>	<b>Value</b>
Core type	ferrite
Number of turns in the primary side	3
Number of turns in the secondary side	31
Primary Litz-wire	60×(0.09mm×22)
Secondary copper wire	1mm
Transformer leakage inductance $L_{lk}$	28 $\mu$ H
Transformer magnetizing inductance $L_m$	10 mH
Transformer turns ratio, $N$	10

Various interleaving approaches were analyzed and compared by simulations and experiments. Table 5 presents the parameters of the case study converter and experimental setup used for the transformer verification. Figure 5.1 shows the simulation model and the designed planar transformer, which was described and verified experimentally. The main efforts were focused on getting the best trade-off between the leakage inductance and parasitic capacitance and different designs are described in [VII]. Figure 5.1b shows three interleaving types— first, one primary and one secondary winding, second, double and third, triple interleaving, respectively. Figure 5.2 presents the simulation results of the estimated leakage inductance and interwinding capacitance with the different distance between the layers. The planar design allows minimizing the leakage inductance value when compared to the transformer on toroidal one. Table 6 summarizes the measured parameters. For the measurements, the RLC meter Agilent U1733C was used and the parameters referred to the secondary winding. The magnetizing and equivalent leakage inductance were measured with the primary winding open and short-circuited, respectively. The interwinding capacitance was measured between the short-circuited primary and secondary winding.

To minimize the interwinding capacitance, the hybrid type planar transformer was designed and tested, which showed the most promising results. This design utilizes the ten Litz-wire turns of the secondary winding with the flat placement in the middle of the primary copper foil, represented by ten parallel winding layers. A detailed explanation of the planar design is presented in [VII].

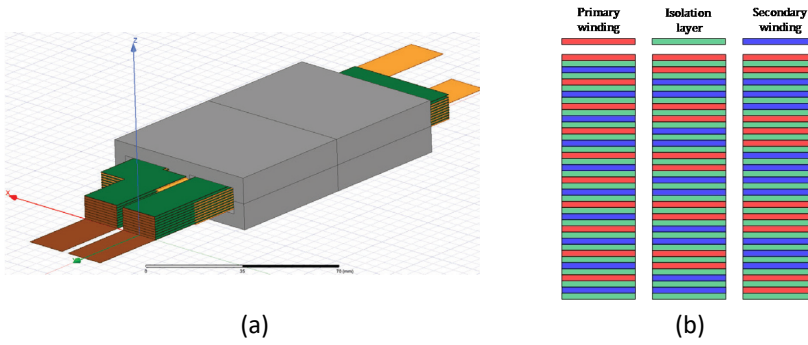


Figure 5.1 Simulation model of the designed planar transformer (a) and its different winding arrangements (b) [VII].

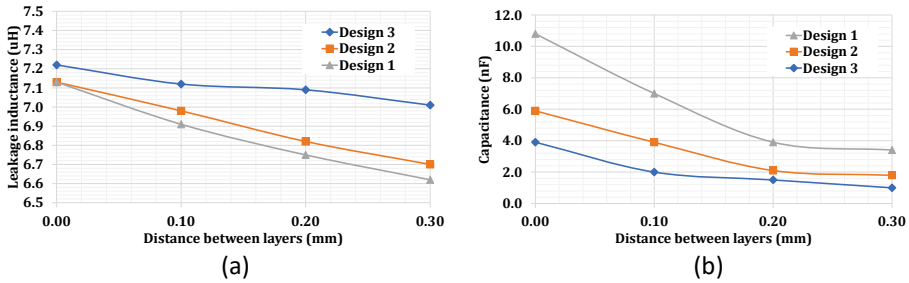


Figure 5.2 The simulation of leakage inductance (a) and interwinding capacitance (b) of the designed planar transformers [VII].

Finally, the transformer based on the ETD core was designed, verified, and tested. For this design, the ETD59 core made of ferrite N97 material was chosen. The core has a large copper area due to higher transformer dimensions. The two Litz-wires were chosen for the winding, on the primary winding, 6 turns Litz-wire 3000x0.04 mm stand was used, while the secondary winding was represented by 60 turns with Litz-wire 130x0.1 mm. The current design allows providing the transformer magnetizing current below the ten percent of the maximum working current, similar to that presented in [IV]. Simultaneously, the interleaving structure when the primary transformer winding is located between the two rows of the secondary (Figure 5.3) allows minimizing the interwinding capacitance and leakage inductance. This design was assembled, and the measured parameters are given in Table 6. As shown, the value of the leakage inductance is close to the planar transformer values, while the interwinding capacitance is two times smaller than in the hybrid type planar transformer. Figure 5.5 shows the photo of the designed transformers.

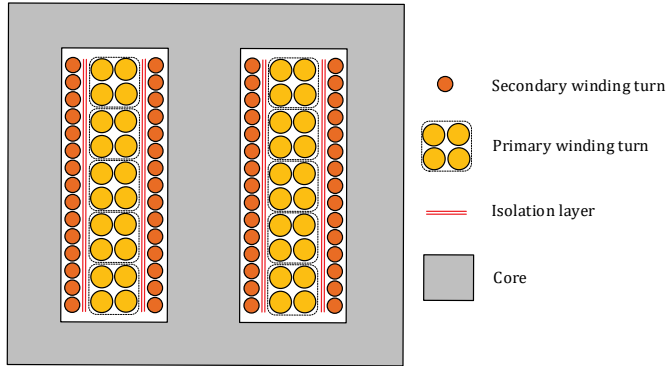


Figure 5.3 Generalized design of the high step-up HFT based on ETD59 core.

## 5.2 Benchmarking of High Step-up HFTs

To compare various transformer designs, a prototype (Figure 5.4) of an IMC based on the parameters specified in Table 5 was assembled. The IMC is capable of integrating the 42-54 VDC LV DC source to the utility grid. In the DC-side, the MOSFETs are used, while the AC-side utilizes the anti-series connection of the SiC MOSFET. The designed transformers (Figure 5.5) were evaluated in the inverter operation of the IMC. Figure 5.6 presented the experimental waveforms of the current and voltage across the primary and secondary windings of the transformer.

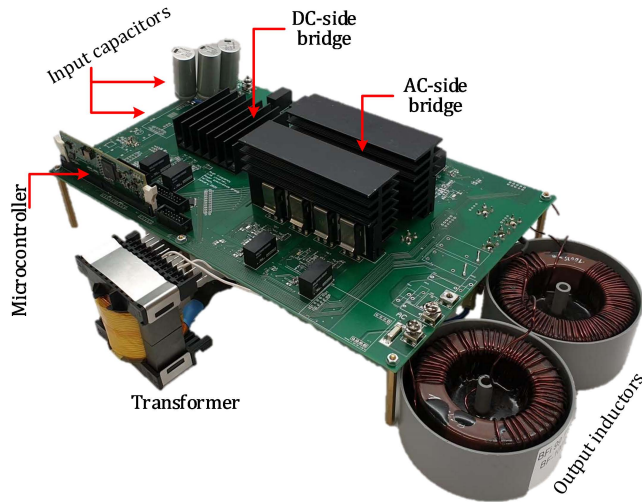


Figure 5.4 Photo of the experimental IMC with high step-up HFT.

Table 5. Specifications of the case study IMC with a high step-up transformer

Parameter	Symbol	Value, type
DC-side voltage	$V_{DC}$	42..54 VDC
AC-side voltage	$V_{AC}$	230 VAC
Switching frequency	$f_{sw}$	50 kHz
Transformer turns ratio	$n$	1:10
Rated power	$P_{rated}$	1 kW
Snubber capacitor	$C_s$	100 nF
Leakage inductance	$L_{eq}$	13..28 $\mu$ H
Magnetizing inductance	$L_m$	3..15 mH
Filter inductors	$L_{f1}, L_{f2}$	1 mH; 0.4 mH
Filter capacitor	$C_f$	0.47 $\mu$ F
DC-side MOSFET	$T_{1..T4}$	IPB017N08N5 $V_{DS} = 80$ V, $I_{DS} = 177$ A, $R_{DS} = 1.7$ m $\Omega$
AC-side SiC MOSFET	$S_{1..S4}$	C3M0280090D $V_{DS} = 900$ V, $I_{DS} = 11.5$ A, $R_{DS} = 280$ m $\Omega$ , $C_{OSS} = 20$ pF

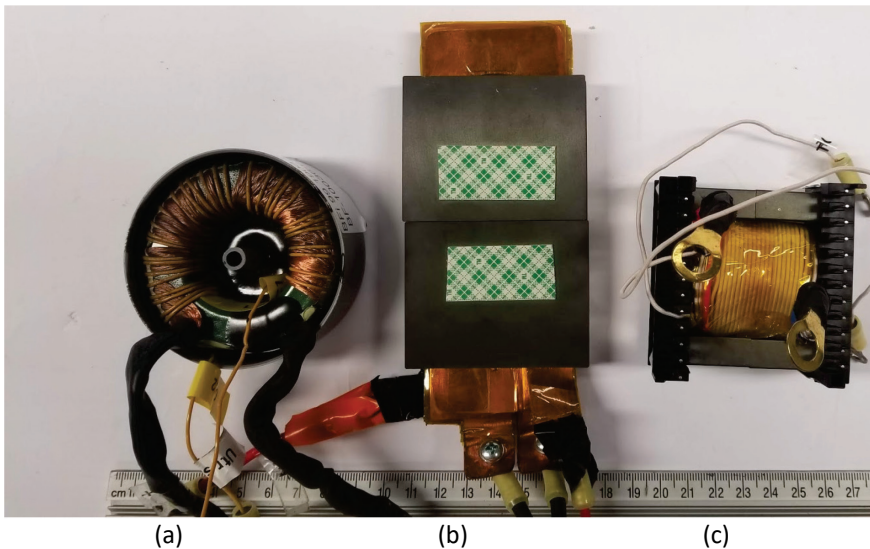


Figure 5.5 The experimental HFTs with toroidal (a), planar (b) and ETD core (c).

Figure 5.7 presents the general transformer current and voltage waveforms. Table 6 presents the results of the IMC efficiency measurements with different transformers. Despite the values of the peak voltage with the ETD core transformer are higher than the toroidal one, the better trade-off between the core loss, interwinding capacitance and leakage inductance resulted in higher power conversion efficiency.

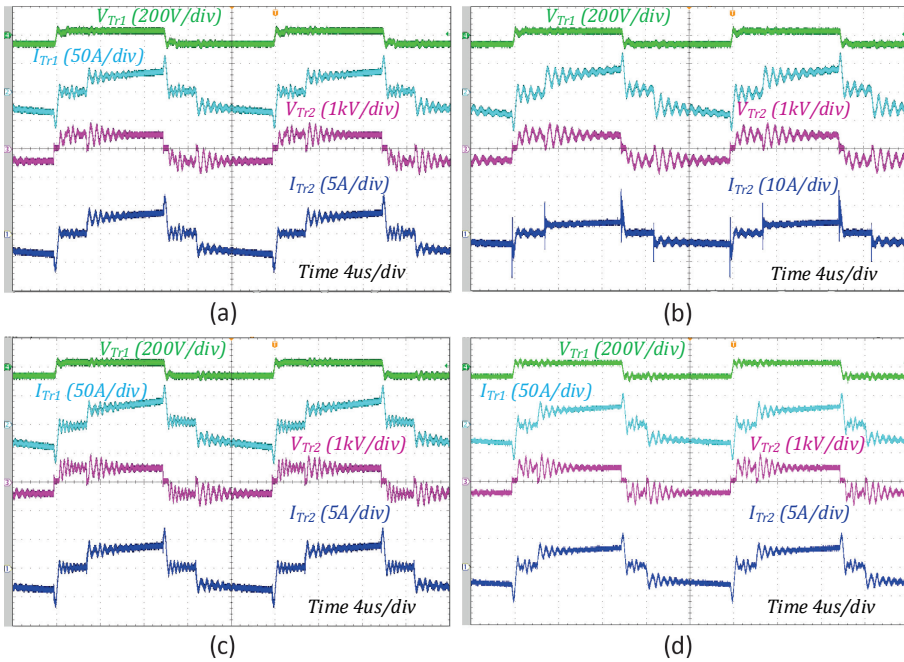


Figure 5.6 Voltages and currents across toroidal (a), planar design 3 (b), planar with hybrid structure (c) and ETD core (d) transformer

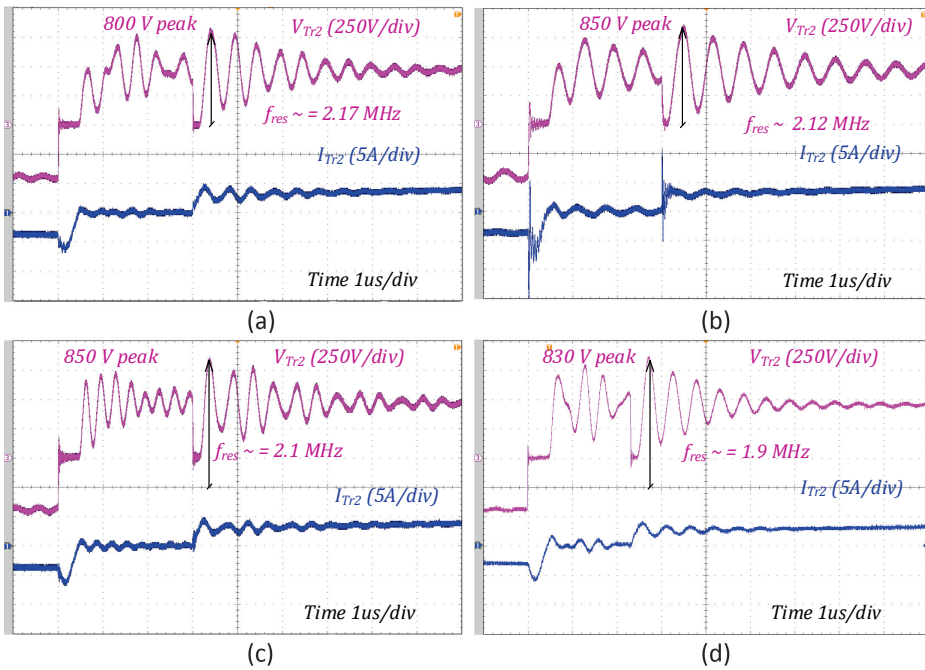


Figure 5.7 Zoomed view of the voltage and current on transformer AC-side of a converter with the toroidal (a), planar design 3 (b), planar with hybrid structure (c), and ETD core (d) transformer

Table 6. Experimentally measured data of different transformers and converter efficiency with input voltage  $V_{DC} = 48V$  and power  $P = 1 kW$

Parameter	Magnetizing inductance, $L_m, mH$	Leakage inductance, $L_{lk}, \mu H$	Interwinding capacitance, $C_0, nF$	Experimentally measured efficiency	
Toroidal core	10	28	0.5	93.4	
Planar E34 core	Non-interleaving	3.3	19.1	0.19	92
	Design 1	3.3	13.6	2.0	92.8
	Design 2	3.3	13.8	2.69	92.5
	Design 3	3.3	14.5	1.5	92.2
	Hybrid design	3.3	15	0.3	93.3
ETD59 core	13.4	13.1	0.15	94.4	

Figure 5.8 presents the experimental waveforms of the IMC with the high step-up transformer based on the ETD59 core. As shown, the converter operation fully follows the description in section 3.1. The converter can provide ZVS during the amplitude and zero values of the output current and simultaneously provides no distortion near zero crossings in the AC output waveforms. Figure 5.9 presents the experimentally measured efficiency of the converter under different DC voltages. The voltage levels were chosen based on the generic voltage levels of the 48 V battery. As shown, the peak efficiency of the converter is 95 %.

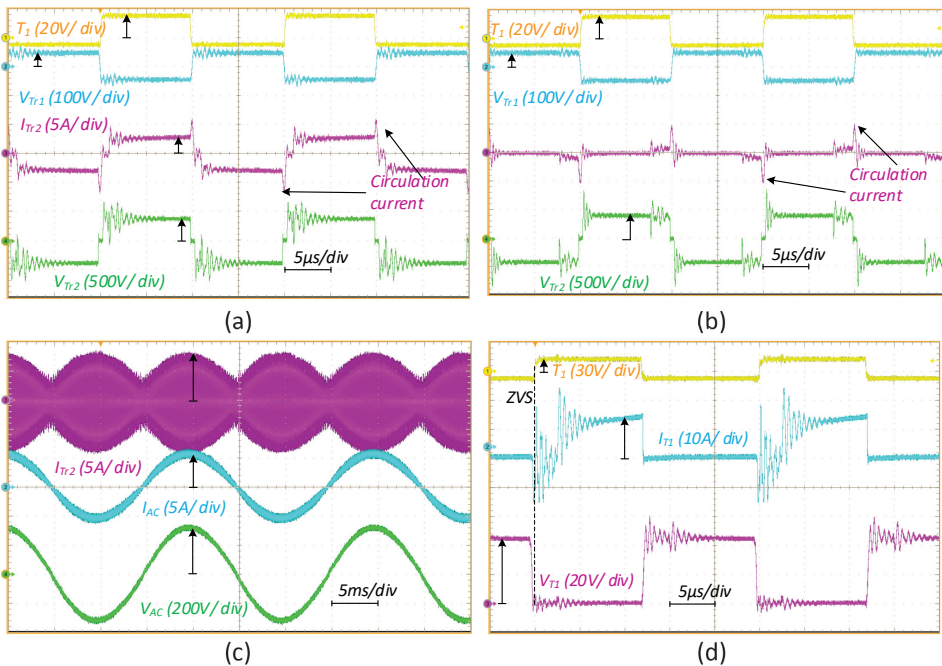


Figure 5.8 The experimental verification of the operation of the converter at  $I_{AC}$  at peak(a) and close to zero(b), the experimental waveform at grid period(c), and zoomed waveforms of the switch  $T_1$  (d)



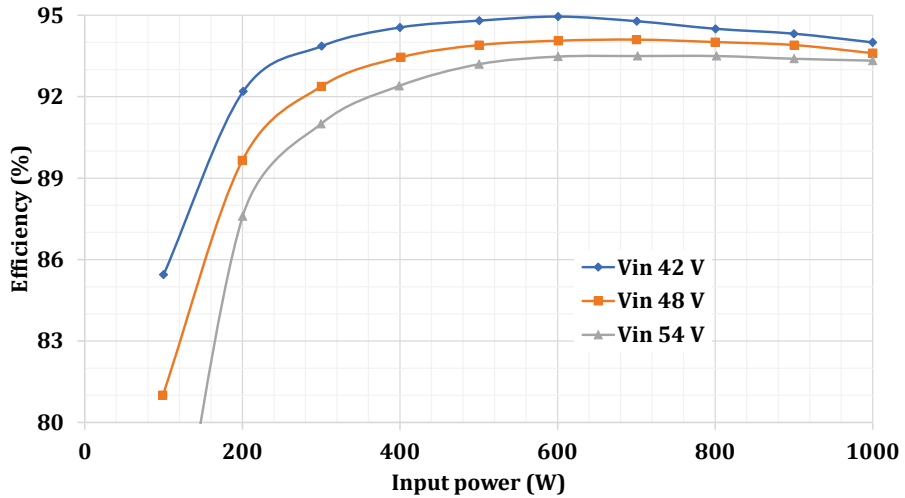


Figure 5.9 The experimentally measured efficiency with the different input voltage levels, with the transformer on the ETD59 core

### 5.3 Generalizations

In this section, different transformer designs were compared. The transformers based on three different cores (toroidal core, planar E-core, and ETD59 core) were studied, designed, and evaluated in the experimental converter. The main conclusions are listed below.

1. The toroidal transformer allows provision of good characteristics, but at the same time, the design of the primary winding for high current is quite complicated and requires special arrangement, which could be complicated for mass manufacturing.
2. The planar transformer utilizing Litz-wire at the AC side can achieve comparable performance to the toroidal one and potentially reduce production costs. It also features smaller height and could suit for the IMC that has the size/height limitation.
3. Among the compared designs, the transformer with the ETD59 core provided better converter efficiency and was relatively easy in the assembly, but at the same time, it has slightly larger size when compared to the toroidal and planar transformers.

## 6 Conclusions and Future Work

The widespread use of renewable energy sources together with battery energy storages leads to a pervasive use of various power electronic converters to provide interface with the power grid. In the case voltage step-up or galvanic isolation requirement, a two-stage power conversion is typically used in the industry. In this case the source voltage (DC) is matched with the AC level by an isolated DC-DC converter, followed by a sine-wave DC-AC inverter. The main aim of the study performed in the frame of this thesis is to increase industrial awareness regarding an alternative approach, where the galvanic isolation and DC-AC conversion are provided using a single-stage IMC. The focus was on the FB IMC based on current source inverter topology.

The initial goal was to collect and organize existing knowledge in the field of IMC to analyze their advantages, drawbacks, and limitations in different applications. The IMCs avoid the use of high-voltage electrolytic capacitors and could achieve ZVS/ZCS conditions in semiconductors using sophisticated modulation techniques, taking advantage of the parasitic parameters of the components. This allows IMCs to demonstrate efficiencies typical to those of the two-stage solutions. On the other hand, these converters typically have relatively narrow DC voltage regulation range and require reverse-blocking semiconductors, specific transformer design and necessity of complex methods for optimal operation (particularly with non-unity PF). These aspects together limit the applicability of IMCs in practical applications.

In the frame of the Ph.D. study the problems of IMCs were addressed from multiple directions. Three different experimental prototypes were designed, built, and evaluated by the author.

- The systematization and classification of existing IMC solutions was done to analyze the main shortcomings, challenges, and potential opportunities of this types of topologies.
- Two new synthesized modulation methods for both energy transfer directions were proposed and experimentally demonstrated using 1.2 kW 400 VDC to 230 VAC IMC. They provide ZVS/ZCS during the whole grid frequency period and allow using the lossless capacitive snubber in the DC-side. Furthermore, the combination of the methods with the high-level control allows providing the ability for the power factor regulation without the requirement of any additional active snubber circuits.
- The 4 kW 350 VDC/230 VAC IMC with the reverse blocking IGBT semiconductors was built and evaluated. It was experimentally demonstrated that reverse blocking semiconductors at the AC side provide up to 1% higher IMC efficiency at higher power levels, as compared to the regular IGBT devices.
- The application feasibility of IMC was evaluated for high step-up applications. One the main challenges in this case lie in achievement of optimal design of isolation transformer, which needs to have high turns ratio, while keeping both leakage inductance and interwinding capacitance as low as possible. Obviously, both core and winding losses should also be low in order not to comprise IMC efficiency. Several transformer designs were compared using 1.2 kW 48 VDC to 230 VAC IMC, which demonstrated maximum efficiency of 95%.

The results obtained confirmed the hypotheses proposed by the author. The IMCs are perspective and versatile, but still an emerging technology that needed further improvements in order to reach industrial maturity. Some of these challenges were

highlighted and addressed in the frame of this work. As a result, the existing knowledge in the area was further developed, potentially bringing IMCs few steps closer to wider industrial adoption. At the same time, there are several potential directions for further research that can be highlighted.

- Optimization of IMC operation during light load conditions in order to increase part-load efficiency and improve total harmonic distortion.
- Extension of the proposed modulation strategies to three-phase topologies with higher power ratings.
- Development of techniques to improve DC voltage regulation range, without adding significant circuit complexity
- Validation of benefits of the IMCs for other applications, such as electric aircraft, electric transportation or as interfaces between DC and AC grids.
- Investigation of IMC fault ride-through capabilities and development of control methods with enhanced functionality, allowing advanced grid support.

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I want to dedicate this thesis in memory of my mother Natalia, I love you....

Oleksandr Korkh

## **Abstract**

### **Isolated Matrix Converters**

The PhD thesis is dedicated to the research and design of the FB IMCs. The main focus was on the study of the modulation techniques of the converter, which allow extending the soft-switching range. Also, the research included the implementation of the RB-IGBTs in the AC-side and the design and implementation of the high step-up transformer for the IMCs.

The author divided the existing IMCs into two types based on the types of the input current of the grid filter. In the current source topologies, the output current of the AC-AC stage is continuous, while in the voltage source ones, the current is not continuous. Next, the presence of the resonant tank utilized for soft-switching were shown, the classification was followed by the topological configuration (bridge, full-bridge, push-pull). Depending on the types and configuration, the different modulation strategies could be applied in the converter shown in the classification.

For the current source FB-FB IMC, two new modulation strategies were proposed for DC-AC and AC-DC energy transfer directions, which were verified in the simulation and with the experimental prototype designed by the author. Both of the strategies were based on the phase shift modulation for the AC-side in the topology while the DC-side is working with the constant duty cycle. The proposed algorithms utilized the special resonance process, which with an additional snubber capacitor across the DC-side semiconductors reduces the turn-off losses in these devices. At the same time, the regulation for the proposed methods is based on one control variable. The challenge of the methods is attributed to the optimization of the resonant current in the light load condition. Based on the newly proposed methods, the control method for regulating the reactive power was described. The benefit of this method is that the FB IMC does not require additional external active circuit components, which are usually required in the case of other modulation strategies.

The study addressed the benchmarking of the RB-IGBT semiconductors at the AC-side of topology. Firstly, the double pulse test methodology was proposed, which provided the information about semiconductor characteristics in conditions close to the ones that occur in the IMC. Based on the received data, the losses based on thermal modelling with PSIM were estimated. The experimental prototype confirms the expected results. The results show that the RB-IGBT can be more suitable for the high-power application against the regular IGBT semiconductors.

Another part of the work includes the design and evaluation of the transformer with a high step-up turns ratio. This allows the integration of the low voltage DC source to the utility grid and extends the possible applications of the converter. Different transformer approaches were simulated, designed, and verified in the experimental setup for the current approach.

## Lühikokkuvõte

### Isoleeritud maatriksmuundurid

Käesolevas doktoritöös keskendutakse voolutoiteliste täissild-skeemilahendusega isoleeritud maatriksmuundurite uurimisele. Uurimistöö fookus on modulatsioonimeetoditel, mis võimaldavad laiendada pehmelülituse ulatust. Lisaks uuritakse ka RB-IGBT transistoride kasutamist muundurite vahelduvpinge poolel ja suure pingetõstmisvõimekusega isolatsioonitrafode kasutamist maatriksmuundurites.

Olemasolevad isoleeritud maatriksmuundurite tüübid võib jagada kahte gruppi, mida eristavad sisendvoolu tüüp ning võrgufiltri skeemilahendus. Voolutoitelistel muunduritel on sisendvool pidev ent pingetoiteliste muundurite sisendvool on katkev. Mõlemad muunduritüübid kasutavad jõupooljuhtlülitites kadude, häiringute ja ülepingepeikide vähendamiseks pehmelülitust. Järgnevalt ongi antud töö sissejuhatavas osas käsitletud resonantsahelaid pehmelülituse saavutamiseks. Pärast skeemilahenduste klassifikatsiooni analüüsi võimalikke muundurite skeemilahendusi (poolsild, täissild, vastastakt jne.) ning nende realiseerimist raskendavaid tehnilisi probleeme (kõrgsageduslike trafode projekteerimine, summutusahelate disain jne.), kuna skeemilahendus ning seadme üldine konfiguratsioon määravad ära kasutatava juhtimisstrateegia ja modulatsioonitüübi.

Töö esimene osa käsitleb uudseid modulatsioonistrateegiaid ülalmainitud muundurite juhtimiseks. Uuritava muunduritüübi jaoks loodi kaks uut modulatsioonistrateegiat. Üks kasutatav alalisvool-vahelduvvool ning teine vahelduvvool-alalisvool energivoogude korral. Modulatsioonimeetodite toimimist hinnati nii arvutisimulatsioonide kui ka eksperimentaalse prototüübi abil.

Mõlemad modulatsioonimeetodid põhinevad vahelduvvoolu muunduripool juhtimisel faasinihkega ning alalisvoolu muunduripoolse konstantse täteteguriga juhtimisel. Antud modulatsioonistrateegiad kasutavad alalisvoolu muunduripoolel lisakondensaatori abil tekkivat resonantsi, mis võimaldab vähendada lülituskadusid ning kasutada kõigi transistoridega pehmelülitust. Samamoodi võimaldavad uued modulatsioonimeetodid ka kahe vahelduvvoolu muunduripoolse transistori samaaegset juhtimist, vähendades sealgi energiakadu. Keeruliseks osutus antud resonantsi saavutamine väikese koormuse tingimustes. Välja pakutud modulatsioonimeetodite üheks eeliseks on lisaks väiksemale energiakaale ka reaktiivenergia reguleerimise võimalus ilma tavapäraste juurdelisatavate skeemielementideta.

Töö teises osas uuriti modulatsioonimeetodite kõrval ka RB-IGBT jõupooljuhtlülitite kasutamist maatriksmuundurite vahelduvvoolu poolel. Esiteks pakuti välja uudne topelpulsiga transistoride katsetamiskava, mis võimaldab kestata transistoride tunnusjooni salvestada. Teiseks loodi arvutisimulatsiooni ning termilised mudelid transistoride energiakao mõõtmiseks simulatsioonitarkvaraga PSIM. Tulemuste hindamiseks loodi laboratoorne prototüüp, millega sooritatud katsed kinnitasid RB-IGBT edukat kasutamist suure võimsusega jõupooljuhtmuundureis sarnaselt tavapärase IGBT transistoriga.

Doktoritöö kolmandas osas keskenduti suure pingetõstmisvõimekusega isolatsioonitrafo disainile ja katselisele kontrollile. Antud trafod on vajalikud madalapingeliste alalispingeallikate sidumiseks elektrivõrguga. Erinevaid trafode konstruktsioonilisi lahendusi hinnati nii analüütiliselt, arvutisimulatsioonidega kui ka prototüüpseadmete eksperimentidega.

# Appendix

## Publication I

Korkh, O.; Blinov, A.; Vinnikov, D.; Chub, A. Review of Isolated Matrix Inverters: Topologies, Modulation Methods and Applications. *Energies* 2020, 13, 2394.



Review

# Review of Isolated Matrix Inverters: Topologies, Modulation Methods and Applications

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**Abstract:** This paper presents a review of isolated matrix inverters. The study contributes to creating a point of reference for a comprehensive classification of existing solutions. Over 30 topologies were reviewed, and the main advantages and disadvantages discussed. Applications of isolated matrix inverters are summarized in a tabular form to demonstrate their flexibility for different power and voltage levels achieved due to the presence of a transformer. These inverters have been proposed for the uninterruptible power supplies, high and low-voltage/power photovoltaic systems, low-power fuel cell, different low- and high-voltage battery and/or electric vehicle chargers, audio amplifiers. The fully controlled switches on both terminals of these converters typically can provide the bidirectional power transfer capability, which is also addressed for most of the topologies, but requires some modification in their modulation strategy. Average efficiency of today's isolated matrix inverters is comparable with the two-stage power converters; however, they can provide higher reliability and lower cost.

**Keywords:** isolated matrix inverter; current source inverter; voltage source inverter; bridge; push–pull; modulation methods; soft switching

## 1. Introduction

Climate change caused by human activities resulting in excessive pollution by greenhouse gases is considered the main threat to the sustainable development of humanity [1]. The first attempt to limit the pollution was reflected in the Kyoto Protocol of 1992 [2]. Later, it was recognized that this initiative is not sufficient to adequately address climate change [3]. Eventually, the Paris Agreement of 2016 was introduced to strengthen national efforts towards climate change mitigation [4]. The energy intensity is considered the key metric for national economies and reflects energy use in equivalent kilograms of oil needed to produce a unity of the national global domestic product [5]. This can be improved via decarbonization of energy generation facilities and improvement of energy efficiency of industry, building stock, agriculture, etc.

Renewable energy generation is considered the main solution for decarbonization of the energy generation industry [6,7]. Even though hydroelectric and biomass technologies dominate this sector, non-conventional renewables are projected to increase their share to over 60% with the dominance of electrical energy generation [8]. This will be supported by accelerated rates of electrification of the industry and the private sector. It is expected that even heating will be widely electrified in the next 30 years [9]. Evidently, electrification will require new approaches to energy processing and transportation. Power electronics is becoming a critical technology that can enable the paradigm shift to decentralized renewable energy generation and massive electrification [10]. Emerging applications of power electronics are countless: renewable energy generation from multi-MW to sub-kW scale, electric

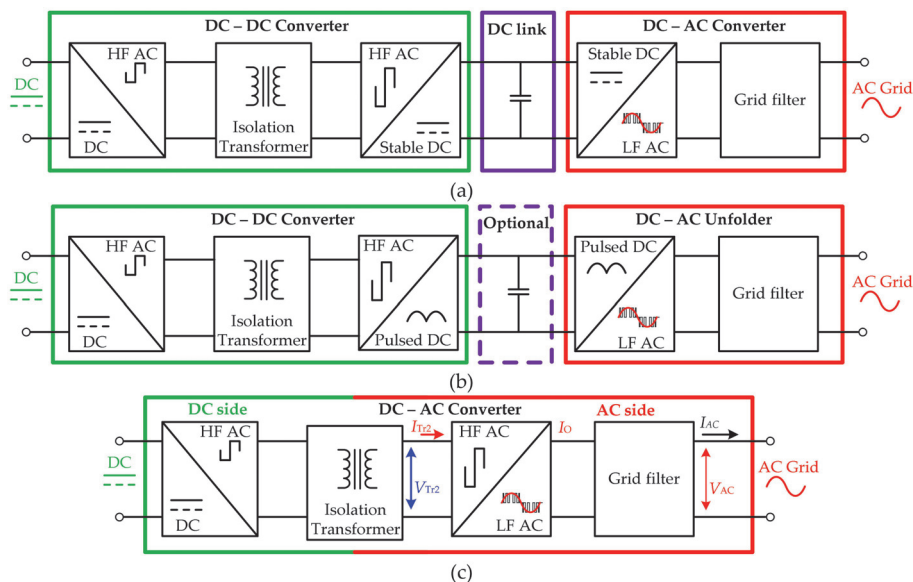
and hybrid electric vehicles and their on- and off-board charging, high-voltage DC energy transmission, battery energy storage systems (BESS) from utility level to the behind-the-meter applications, energy harvesting for Internet of Things devices, wearables, microgrids (AC, DC and hybrid) and their interconnection, energy-efficient buildings with on-site energy generation, etc.

The increased use of alternative and renewable energy sources, like wind and solar, together with the development of energy storage technologies, such as Li-ion batteries, supercapacitors and fuel cells, fosters the need for various power electronic converters in the present electric energy systems [11–15]. Electronic power technology for large-scale renewable energy generation is approaching maturity and sees evolutionary improvements in topologies, used semiconductor and passive components. At the same time, disruptive innovation is expected in their control by the integration of smart functionalities secured with blockchain (distributed ledger) technology [16,17]. Meanwhile, the dispersion of energy generation is associated with the new incentives for decarbonization of building stock. It has been shown that nearly zero energy buildings can be economically viable when energy-saving construction technologies are complemented with on-site generation of heat and electricity [18]. This has resulted in the rapid growth of residential renewable energy generation technologies, such as rooftop and building integrated photovoltaic (PV) systems, low-voltage residential BESSs, small wind turbines, fuel cells (FCs), etc. [19,20]. All of these feature different voltage and power levels and thus require numerous power electronic converter types. Moreover, additional converters are required to interface systems having various voltage levels with common DC or AC bus [21,22]. Increased electrification will require energy storage not only to balance the utility grid to withstand intermittent variations in renewable energy generation, but also to provide an uninterruptible power supply to critical loads [23,24]. Other growing markets that benefit from advancements in power electronic technologies are hybrid and electric vehicles [25], electrified railway [26], variable speed drives across industry [27] and flexible power systems [28]. Increased demand for the development of technologies based on power electronic converters put additional pressure on the industry to provide new solutions with minimal cost and high reliability to facilitate faster decarbonization.

In the BESS, PV and FC applications, a power electronic converter has to operate with a variable DC source that should be interfaced with the AC grid. In such systems, the main challenges are mostly associated with providing voltage step-up from a low-voltage energy source, like a battery or to provide galvanic isolation as a safety measure, such as required in EV charging. Typically, to achieve demanded functionality, a two-stage power electronic system is used (Figure 1a) [29–33]. Variable input DC voltage is first stabilized at a DC-link capacitor by a DC–DC converter that often features a high-frequency (HF) transformer (HFT) for both voltages matching and the galvanic isolation. It is then followed by an inverter stage that converts the stabilized DC voltage of the appropriate level into the AC voltage. These systems offer a good regulation range and are widely used in practical applications [29–34].

An alternative approach is to apply isolated DC–AC topologies without an evident intermediate DC-link. In these converters, the HFT secondary voltage can be converted to low frequency (LF) AC using an active rectifier and unfold (Figure 1b) [35–42], or by using single HF AC to LF AC conversion (Figure 1c) [43–53]. Despite both of these approaches are commonly referred to as single-stage DC–AC converters, the systems with unfolding stage technically feature an additional low-frequency link (with rectified sine-wave) and, therefore, are considered as a quasi-single stage in this paper. On the other hand, the topologies with unified HF AC to LF AC stage are performing AC–AC conversion directly, using bidirectional semiconductor switches, which is a distinctive feature of matrix converters [54]. In the literature, such systems are also referred to as HF-link inverters [39,52], cycloconverters [43,48] or single-stage inverters (converters) [30,32], but are all considered as isolated matrix inverters in this review. These systems are often capable of transferring power in both directions and can achieve soft switching conditions in semiconductors with advanced modulation methods [46–56]. Such features, together with a wide range of possible industrial applications, have attracted increased interest of research groups in isolated matrix inverters for many years.

Modern single-stage converters with fully controlled semiconductor devices started to appear in the literature in the late 1980s [57], mostly targeting uninterruptible power supplies [58,59]. Later, their application area was extended to PV microinverters [60,61], FC [42,62,63], Li-ion battery storage [64], railroad [65], electric vehicle charging [66], motor drive [67] and residential applications [22,62]. Currently, the two-stage galvanically isolated inverters are an industry-accepted technology established in numerous applications, while the quasi-single-stage has also been used in emerging applications such as PV microinverters [68,69], recently adopted in residential BESSs [70–73]. The isolated matrix inverters are an emerging technology that has not yet reached maturity and good industrial awareness; however, this technology shows good potential for industrial adoption, as was demonstrated in [53,74].



**Figure 1.** General structure of isolated matrix inverters: (a) two-stage, (b) quasi single-stage, (c) single-stage. LF AC—grid frequency; HF AC—switching frequency.

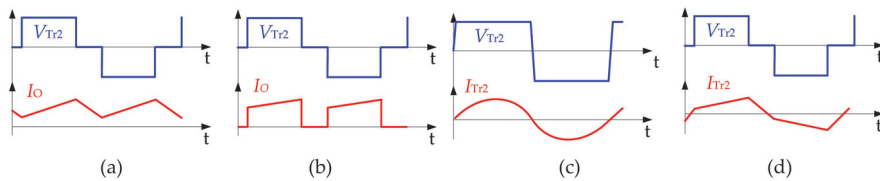
Despite a multitude of isolated matrix inverter concepts presented for various applications, no classifications or reviews summarizing the features and potential of this technology have been reported. The aim of this paper is to give an overview of existing single-stage matrix inverters, classify their topologies, modulation methods and applications in order to get the reader a better understanding of the potential and limitations of such systems. The paper is arranged as follows: in Section 2, the classification based on topology types and modulation methods is proposed. Section 3 addresses the current source inverter (CSI) based topologies, followed by the description of the voltage source inverter (VSI) based topologies in Section 4. Section 5 discusses the main features and applications of the highlighted topologies. Finally, the conclusions and further research directions are presented.

## 2. Systematization and Classification

Various isolated matrix inverter topologies have been reported for different applications, ranging from low-voltage and low-power [60,61,75] to high-voltage high-power [76], which proves the versatility of this technology and justifies the need for systematization of existing knowledge to establish points of reference. As mentioned in the previous section, a common property of such converters lies in the absence of an evident DC-link and presence of the direct AC-to-AC conversion stage. Generally, the DC-side of an isolated matrix inverter features a half-bridge (HB), full-bridge (FB) or push–pull (PP) stage that is connected to the primary winding of HFT. The AC-side connects the HFT secondary



to the grid using HF AC to LF AC stage. The AC-side can be a current-source inverter (CSI) type [46] or a voltage-source inverter (VSI) type [77]. In the CSI-type, the current  $I_O$  is constantly flowing in one of the legs and either LC or LCL filter is used (Figure 2a), whereas the VSI-type has the diagonals switched with certain dead time and generally utilizes a CL filter, and in this case, the current  $I_O$  is not continuous (Figure 2b).



**Figure 2.** Generalized representation over one switching period of currents and voltages for different isolated matrix inverter types and availability of resonant tank: (a) current source inverter (CSI), (b) voltage-source inverter (VSI), (c) resonant, (d) non-resonant.

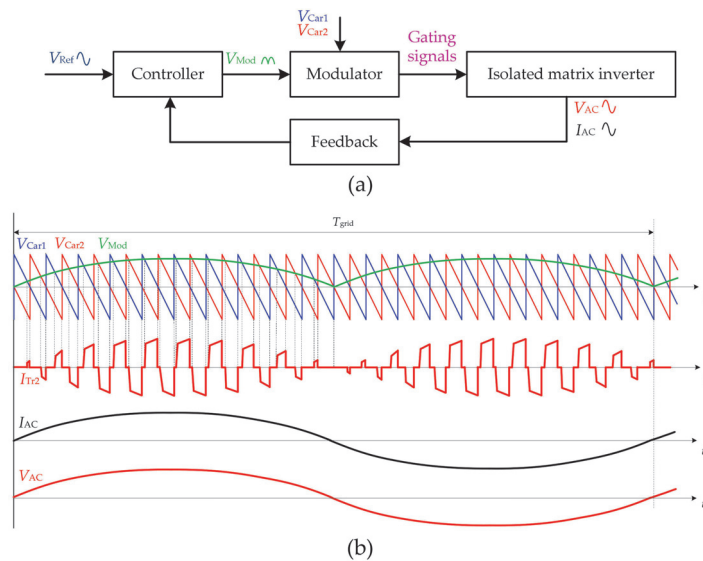
The converters that are based on the two-winding transformer are typically HB- or FB-type [57,60,61]. On the other hand, central-tapped or multi-winding transformers enable the use of other configurations, like PP [78] or three-leg [79]. The PP topologies generally employ the central tap transformer, and the semiconductor have double voltage stress, but, at the same time, they allow for the reduction of the number of semiconductor devices.

Most modern isolated matrix inverters feature soft switching in semiconductors that is achieved using special modulation strategies [46–56], resonant circuits [60,66,80] or active auxiliary circuits [81–85]. In addition, these methods aim to reduce semiconductor voltage stresses [85]. For the resonant topologies, the transformer current  $I_{Tr2}$  is usually close to the sinusoidal (Figure 2c), whereas in the case of non-resonant topologies, the shape of current  $I_{Tr2}$  is typically close to square-wave or trapezoidal (Figure 2d).

The sine wave modulation can be applied either for DC or AC sides of the converter. In the case of the DC-side modulation (primary side modulation), the shape of the output voltage (current) is formed using pulse width modulation (PWM) [47] or phase shift modulation (PSM) [48] applied to the DC-side switches. The AC side, in this case, is usually working as a rectifier. Another common strategy is the secondary side modulation. In this case, the DC switches are working as an inverter, forming the square wave voltage pulses at the HFT primary. After this, the AC-side switches are forming the required shape of the voltage (current) based on PSM [46] or PWM [47]. For the resonant topologies, the frequency modulation (FM) [66] is usually applied, which allows changing the gain under different power ratings.

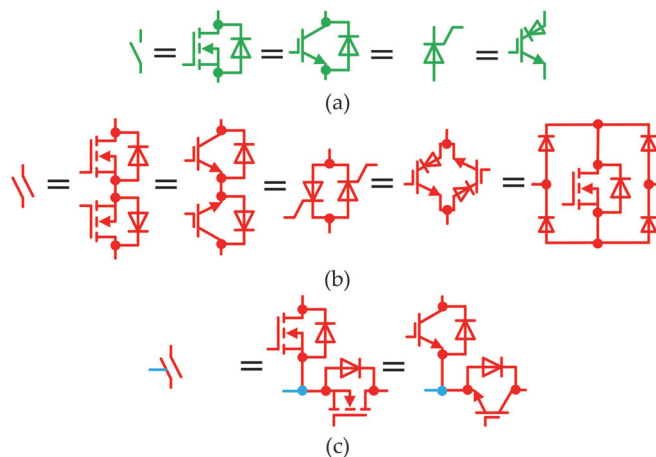
Two main strategies of the PWM are used—unipolar and bipolar. Unipolar PWM (UPWM) [47,49,75] is widely employed and allows achieving zero voltage switching (ZVS) for the AC-side switches. The utilization of the bipolar PWM (BPWM) [81] has been reported to have lower total harmonic distortion than the UPWM. The PSM modulation is usually based on only one shift carrier for the CSI [46,48], while in the VSI based topologies, PSM with more than one phase shift is typically used to achieve better quality of the output voltage [86]. More sophisticated methods additionally use FM to increase the ZVS range [66]; moreover, the amplitude modulation (AM) [80] was also addressed. These are the low-level modulation techniques that are employed in converter modulators to generate the switching sequence within a single switching period and ensure that an inverter can perform the input voltage regulation and the output current control (Figure 3). Hence, this paper considers modulation strategy as the main control feature in each reviewed topology. To achieve the LF sinusoidal voltage/current at the output, a higher-level control/modulation (controller in Figure 3a) method has to be applied to define the control variables applied to the low-level modulators ( $V_{mod}$ ) across the grid frequency period, i.e. PWM duty cycle, PSM phase shift or both. Typical higher-level control/modulation methods are the sinusoidal modulation [58] in the one-phase system, the space vector modulation [87]

in the three-phase, or model predictive control [88]. They define the input parameters applied to the low-level modulator(s) typically based on PWM or PSM, as discussed above.



**Figure 3.** Generalized representation of (a) control and (b) modulation for the isolated matrix inverters.

The isolated matrix inverters could be realized with the metal oxide semiconductor field-effect transistor (MOSFET) [89], the insulated-gate bipolar transistor (IGBT) [90], gate turn-off thyristor (GTO) [91] or the reverse blocking IGBT (RB IGBT) [92–95] semiconductors, depending on the power and voltage level and application. The DC side is generally formed by unidirectional devices (Figure 4a), while the AC side usually features bidirectional switches (Figure 4b). The bidirectional switches for the AC side are typically realized by two identical devices in common source (emitter, cathode) configuration or the antiparallel reverse blocking switches can be applied. In some cases, the bidirectional switches with the middle connection point can also be used (Figure 4c) (see also [96–107]).



**Figure 4.** The types of the semiconductors (a) unidirectional switch, (b) bidirectional switch, (c) bidirectional switch with the middle connection point.

The classification presented in Figure 5 divides the isolated matrix inverters by the type of the AC side: CSI- or VSI-based. Second, they are classified by the conversion type—resonant or non-resonant, and third, by the configuration of the topology: bridge, PP. Finally, the reported modulation types for the particular configuration are given.

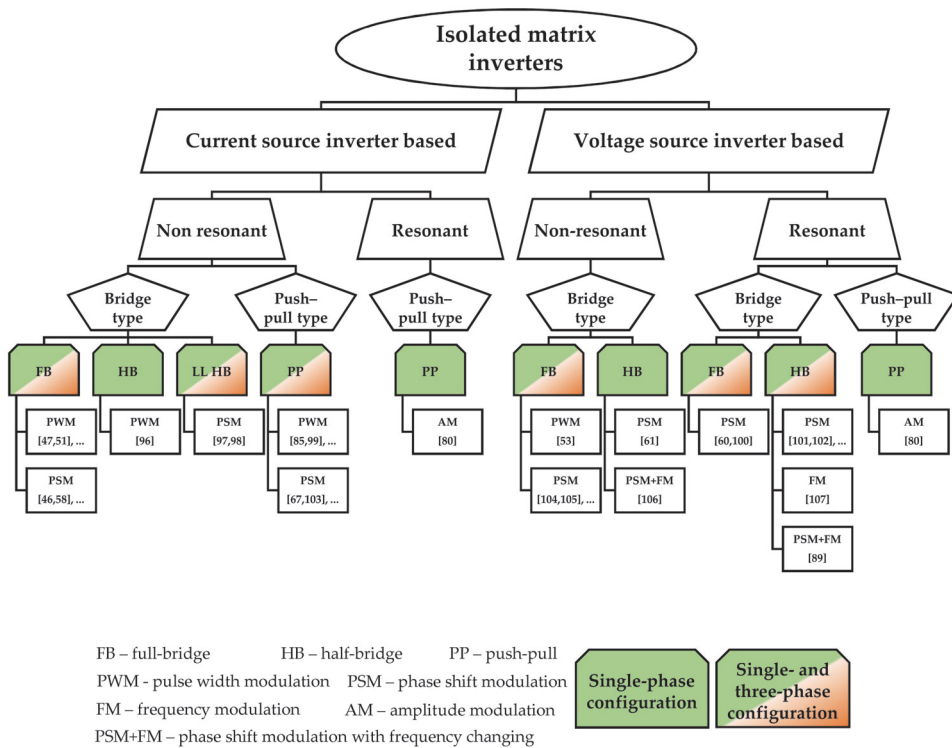


Figure 5. Classification of the isolated matrix inverters.

### 3. CSI Based Topologies

This section addresses the topologies of the isolated matrix inverters with a grid side switching stage based on the CSI. The subsections are organized according to the fourth hierarchical level of the classification from Figure 5.

#### 3.1. Non-Resonant Bridge Topologies

##### 3.1.1. FB Configuration

The history of the FB inverter configuration presented in Figure 6 started close to 1980, when this type of topology was proposed for railroad applications [57] and afterwards for uninterruptible power supplies [58]. At that time, the developments of the new types of the ferrite materials and possibilities to increase the switching frequency with new types of semiconductors allowed for a decrease of losses and sizes of the magnetic components, resulting in the improvement of the efficiency of the system in general. The topology consists of four main parts: the DC-side bridge, the AC-side bridge, the HFT and the output grid filter. The DC-side bridge consists of four switches that work as an inverter, which forms the high-frequency pulses. The transformer provides galvanic isolation between the two sides and allows them to step up/step down voltage. The AC-side bridge can form the sinusoidal voltage output or work as a rectifier, depending on the modulation method. The output AC-side LCL filter is

used to filter the high-frequency pulses. Given the realization of bidirectional switches in the AC side using two discrete devices, this leads to a distinct disadvantage—a relatively high number of active semiconductor devices required.

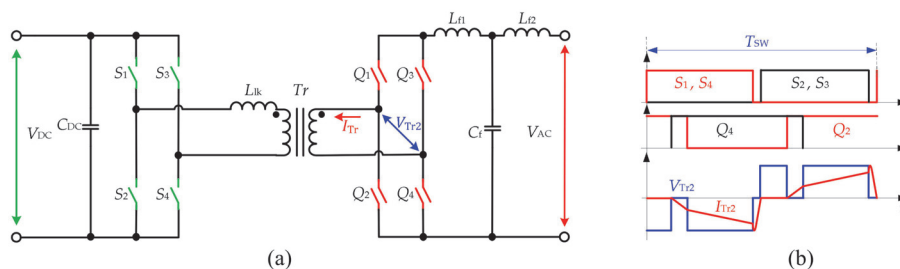


Figure 6. Full-bridge (FB) configuration (a) and modulation (b) proposed in [52].

Another major challenge for the isolated FB configuration inverter topology is that the transformer leakage inductance and the output filter inductor both serve as current sources for the AC-side bridge. Thus, the AC-side bridge operates as a current breaker, which endures high-voltage spikes due to the cutoff of the leakage inductor current. The natural commutation principle for this converter was proposed in [59]. In addition, various other modulation methods using DC- or AC-side switches were presented for the current topology [46–52]. These methods typically allow utilizing energy stored in the leakage inductance to create soft switching conditions for semiconductors, which also particularly or fully solves the mentioned problem of high-voltage overshoots. The topology features the capability of bidirectional power flow without any additional auxiliary circuit.

In [46], the 40 kVA bidirectional converter for medium voltage converter (MVC) application was proposed. This work presents a special multi-mode quasi-resonant PSM method, which allows achieving soft switching in all semiconductor devices. The additional snubber capacitor is added for DC-side semiconductors and RCD for the AC side to reduce turn-off losses and ringing. Special multi-mode modulation allows the creation of the additional quasi-resonant interval, which is activated near the zero-crossing point. It is utilizing the resonant circuit formed by the DC-side snubber capacitor and transformer leakage inductance to achieve soft switching at the current zero-crossing point. The details of the modulation method are described in [65]. The experimental waveforms confirm that the method is verified, and the converter can operate without any additional damping circuit for the leakage inductance energy. At the same time, the optimization of the transformer and snubber capacitance can be a point of the discussion, because this can significantly influence of the converter efficiency, especially at the higher step-up ratio of the transformer.

Two UPWM based modulation methods for the FB isolated matrix inverter are reported in [47], both of these methods allow achieving the soft switching for the AC-side switches. In contrast, the DC side has only the ZVS turn-on transient. The first method allows operating four switches at the AC side at line frequency, further reducing the remaining switching loss and improving the efficiency. The authors applied the hybrid structure of the switches at the AC side—four of them are IGBT with grid frequency switching and four MOSFET with high working frequency. This allows price reduction of the converter, which was the authors' aim. The second modulation method is proposed for the full MOSFET bridge configuration. In this method, two of the switches working with the line frequency, two—as synchronous switches, and all the other are forming the output voltage. The authors verified the experimental 1.2-kW prototype with 400-V DC input voltage and 240-V AC RMS output using one to one isolation transformer. The peak efficiency of the system is 96% for the full silicon carbide (SiC) MOSFET design. In [108], the same group of authors presented applications for this converter in the high-frequency distributed power delivery system. This utilization allows elimination of the traditional low-frequency transformer and its replacement it with HFT. The potential target application is air and ground transportation and renewable energy systems.

In some studies, the leakage inductor energy is redirected to the additional auxiliary circuit, which allows the clamp of the voltage overshoot. In [48], the new modulation method based on the DC-side PSM is addressed for the FB inverter operation. For the minimization of voltage overshoot across AC-side switches, the clamping circuit with the rectifier bridge, capacitor and DC–DC converter is applied. The energy from the AC side is returned to the DC input and reused again in the converter. The topology is verified with 1 kW with 270 V of input and 100-V RMS at the output as UPS inverter. Other clamping circuit approaches were addressed in [49–51,109]. These papers present different types of regenerative flyback snubber. Since this snubber is technically a separate converter, in addition to voltage clamping, it can provide additional features for the topology: reduce the amount of the circulation current through the main switches, improve the soft-start procedure or improve the quality of the current in the case of non-unity power factor. The energy stored in the snubber capacitor can be utilized in two ways—being reused in the next switching cycle of the conversion, as proposed in [49,50] or transferred back to the DC side and reused again as shown in [109]. In addition, it is claimed to allow improving the efficiency of the converter in general. In [110], different snubbers for the minimization of the influence of high step-up transformer are analyzed for the case of the integration of low-voltage DC source to the grid. On the other hand, the utilization of the snubbers requires an additional transformer or two flyback transformers, switches, diodes, capacitors and additional control channels and isolated drivers. The utilization of this snubber can be more suitable for the high-power converter. For the lower-power converters, this solution can be less optimal, considering the price and overall complexity.

Many high-power converters commonly use bridge-type topologies due to the better utilization of the switches and lower stresses. The FB topologies can be extended to the three-phase grid system, as presented in [53,59,76,111]. In this case, at the AC side, an additional leg is supplied and the modulation method is extended for the three-phase system (Figure 7).

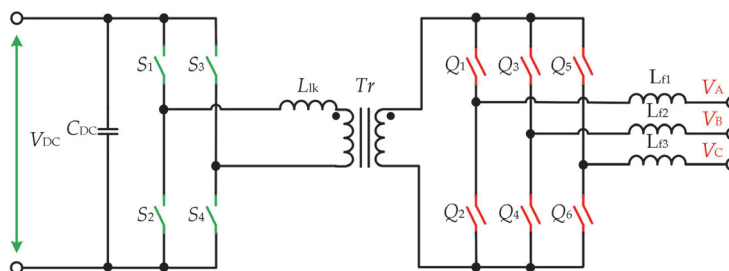


Figure 7. Three-phase FB configuration.

### 3.1.2. FB Configuration with Three Legs at the DC Side

In [79], the AC side PSM modulated PV microinverter is proposed (Figure 8). The topology utilizes three switching legs and a special high-frequency transformer. The additional bridge leg operates with a phase shift to the main bridge and allows generation of the two-step voltage waveforms, which are afterwards converted to the AC voltage. The two-step voltage allows reducing the ringing of the AC-side switches. The topology allows achieving the soft switching in all semiconductors at the AC side, while on the DC side, only two switches have hard transients. This solution is suggested to improve the efficiency of the system compared to the topology with the RCD snubber at the AC side. The peak efficiency reported is 95%.

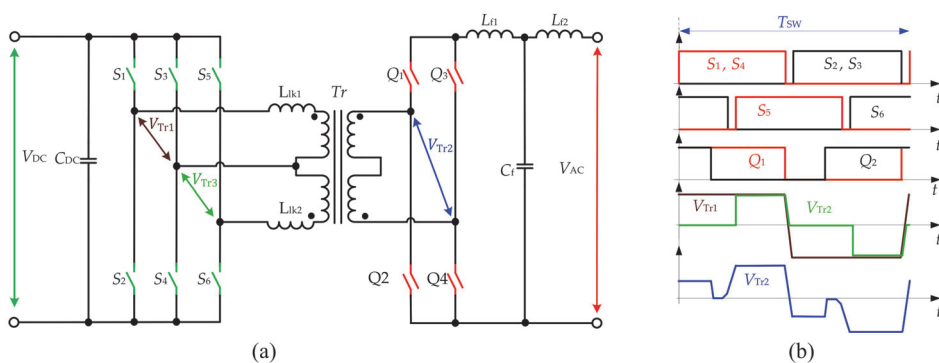


Figure 8. FB topology with the three switching legs at the DC side (a) and modulation (b) in [79].

### 3.1.3. FB Configuration with the Reconfigurable AC Side

The topology reported in [42,62] is proposed as a unidirectional inverter for the FC applications (Figure 9). It features two transformers and two bidirectional AC side bridges, which can be connected in series or in parallel, providing the universal output. The topology utilizes the SPWM at the DC side, while half of the AC-side switches work with the grid frequency to minimize the switching losses in the converter. The design focuses on the universality of the output voltage and is suitable for both 230 V and 110 V and has a high step-up factor to achieve the connection 30–60-V fuel cell and is claimed to be optimal in terms of weight and cost. The authors achieved a peak efficiency of 92.5% for the proposed concept. The leakage inductances of the transformer are utilized for the soft switching in the semiconductors, but at the same time, the voltage overshoot appears across the AC-side switches. This suggests that the design and optimization of the transformer can be further considered to achieve better efficiency and reduce the stresses in the topology.

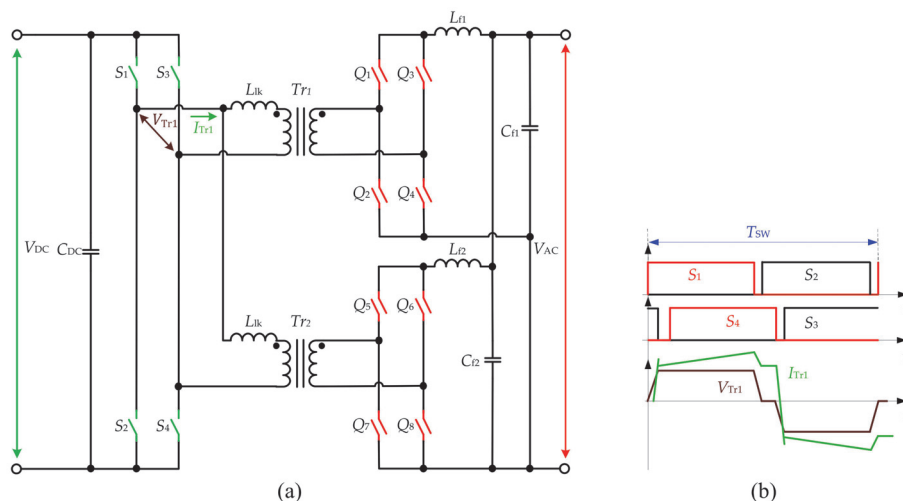


Figure 9. FB topology with the reconfigurable AC side (a) and modulation (b) shown in [62].

### 3.1.4. The FB Configuration with PP at the DC Side

Figure 10 shows the topology reported in [78] as a unidirectional inverter for renewable energy sources. The topology has two switches at the DC side connected to a central-tapped transformer, forming the PP configuration. The AC side features the FB configuration. The multiple-carrier PWM is



proposed for this topology. It was suggested that this technique allows reducing the complexity of the control algorithm for the inverter. The topology is suitable for low power applications; the simulation results of the 200-W prototype were shown for 48 VDC input voltage and 127-V RMS output voltage, using a transformer with a turns ratio of 1 to 4.2. An alternative configuration of a bidirectional converter based on the Cuk, SEPIC, Zeta converters is presented in [112] where the 400-W prototype of the SEPIC converter is demonstrated.

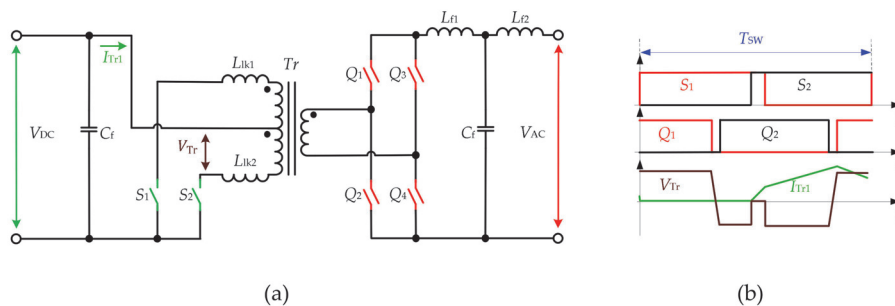


Figure 10. FB configuration with push–pull (PP) at the DC side (a) and modulation (b) in [78].

In [113], the focus is on a multilevel PP inverter configuration. It utilizes the central tap transformer on both the DC and the AC side and includes an additional bidirectional switch at the AC side. The presence of the additional switch at the AC side and a special modulation strategy based on PSM allows avoiding the current interruption at the AC side, and as a result, voltage overshoots. The paper provides experimental verification on a 162-W prototype with 24-V input DC voltage and 100-V output AC voltage. In addition, the topology is suitable for bidirectional operation.

### 3.1.5. HB Configuration

The topology in Figure 11 [61] is proposed as a unidirectional microinverter for PV applications. It features two transformer windings and two bidirectional switches at the AC side, which work at the line frequency. Thus, the total number of AC-side transistors is reduced by a factor of two when compared to the topology in Figure 6. The DC side, as described, could be configured as a FB, HB or PP, which can allow reducing the total number of the semiconductors even further. SPWM is applied to the DC side semiconductors, realized by a comparison of two 180° phase-shifted sinewaves with a dual-sided ramp wave. At the AC side, the IGBT switches are utilized with line switching frequency to minimize the losses in the converter. The reported peak efficiency of the 250-W prototype is 94.5%. On the other hand, the ZVS for the DC-side switches has a limited range (occurs at peak power), and the AC-side switches have higher voltage stresses.

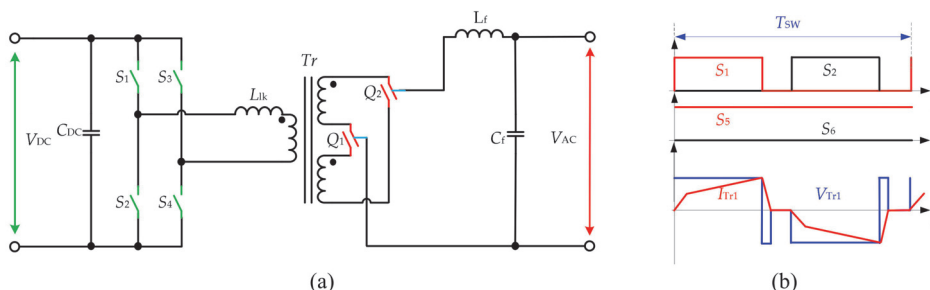
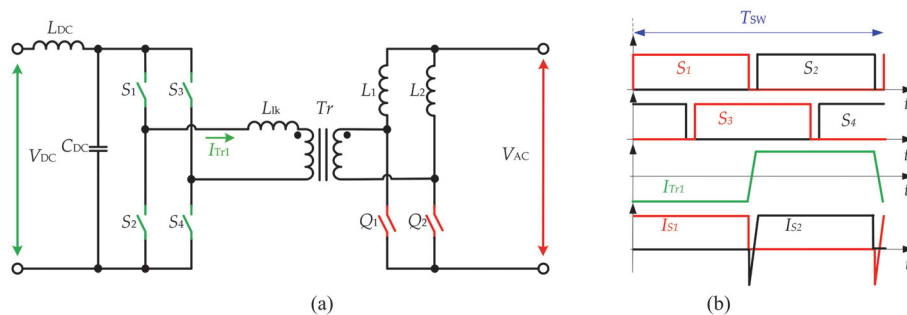


Figure 11. Half-bridge (HB) configuration (a) and modulation (b) in [61].

### 3.1.6. LL (dual inductor) HB Configuration

The dual inductor half-bridge (LL HB) converter type is a popular solution in the DC–DC converters due to the low current ripple. Figure 12 presents the bidirectional converter topology proposed for electric vehicle battery charging applications in [97,114]. The original paper describes it as “single-stage bidirectional converter for EV”; however, it will be referred here as LL HB due to the topology configuration. The converter features a full-bridge on the DC side with an additional filter inductor  $L_{DC}$  and LL-type HB at the AC side. The converter with the input of 120-V RMS AC is connected to a 220–336 VDC battery through a converter that has a high-frequency transformer with a turn ratio of 0.5. In the rectifier mode, the converter operates as a two-phase boost converter, while in the inverter mode, it acts similar to a FB converter with the current doubler rectifier the output voltage regulation is achieved by PSM. The converter features reduced current ripple due to the presence of two inductances at the AC side, allowing the ZCS to be achieved at the AC side, and ZVS turn-on at the DC side. Moreover, it can operate in four quadrants with active and reactive power regulation for both directions of the power flow. In the inverter mode, the PSM is implemented for the DC-side switches, while the AC-side switches are continuously on or off depending on the polarity of the grid voltage. Peak efficiency of 96.5% at full power is reported for the 1.5-kW prototype. At the same time, the topology requires an additional inductor, the voltage stress on the switches is increased, and it is estimated to have substantial energy circulation at partial load. The simulation results of the three-phase system shown in [98].



**Figure 12.** Single-stage bidirectional converter for EV (LL HB) configuration (a) and modulation (b) proposed in [114].

## 3.2. Non-Resonant PP Topologies

### 3.2.1. PP Configuration

The topology in Figure 13a was introduced in [103] for the UPS. The topology utilizes the central tapped transformer and two bidirectional switches at the AC side, while the DC side has a FB inverter. In [104], the converter was controlled with SPWM modulation at the DC side. In [99], an improved modulation method is introduced to handle the non-unity power factor without snubbers. A novel digital control using the bipolar double modulation wave was addressed in [108], which is shown in Figure 13b. The sinusoidal output voltage is formed by AC-side semiconductors using PSM. It allows achieving the ZVS turn-on on the DC side, and the ZVS turn-off at the AC side. The experimental verification of the topology was presented using an experimental 250-W prototype with and 46-V output voltage. In [96], the topology with four additional snubber capacitors for switches  $S_1$ – $S_4$  is presented. The aim is to achieve the ZVS and ZCS in all semiconductor devices using PSM. The experimental waveforms of the prototype with 24-V input voltage and transformer 1:2.74 are shown. Another version of the PSM is used in [115] to achieve the ZVS in the topology, which was confirmed with a 1-kW experimental setup. Reference [116] presents the unidirectional converter for PV application, which utilizes the additional two inductors at the AC side.



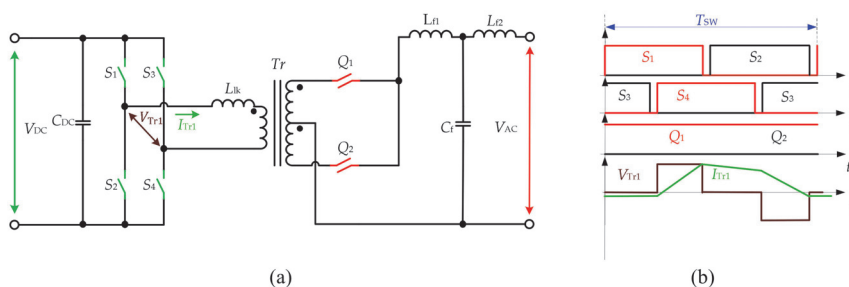


Figure 13. PP configuration (a) and modulation (b) in [117].

The three-phase system for the three-phase drive reported in [67] is shown in Figure 14. The topology has three parallel ports to support bidirectional operation with the source commutation method. The topology is also suitable for the UPS, PV and battery storage systems.

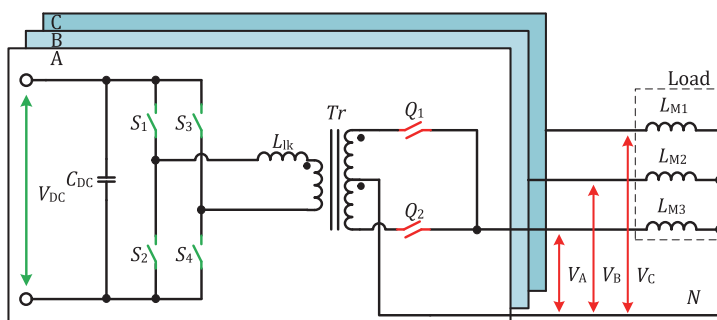


Figure 14. The three-phase PP configuration.

A novel ZVS approach for the flyback—PP inverter for low-power PV application is presented in [118]. The AC part of the topology is similar to that in Figure 13, while the input DC bridge is replaced by one switch, forming the flyback configuration. The soft-switching on the DC-side switch is achieved by additional circulating energy from the grid filter capacitor. To optimize this reactive current, the variable frequency control was proposed. Experimental results confirm the feasibility and show 94.5% peak efficiency of the system.

### 3.2.2. PP Configuration with voltage clamper

The topology of the bidirectional inverter presented in Figure 15 was introduced in [82] for the UPS system. The topology configuration consists of FB on the DC side, a central-tapped transformer with two bidirectional switches on the AC side and an additional clamping circuit. This active clamping circuit is proposed for the minimization of the voltage overshoots. It consists of four switches, which form the bridge, two diodes and clamp capacitor (the configuration without the capacitor is also possible [82]). The energy stored in the capacitor is transferred back to the DC source and reutilized. The SPWM is used to control the DC side, while AC-side switches are rectifying. The drawbacks could be attributed to a limited ZVS range, extra two diodes and a capacitor when compared to the FB solution without a snubber circuit.

Other approaches to control the configuration of the bridge clamp are reported in [75,81,83,119]. In [83,84], a detailed analysis of the operation of the bidirectional topology and clamping circuits is given. The experimental waveforms of the 500-W prototype with efficiency around 90% are provided, and the converter is proposed for renewable, naval and aerospace applications. In [75,119], the topology was proposed for the low-power audio amplifier. The operation principle of the uni- and bipolar PSM

strategy is described and verified. In [81], an alternative bipolar PWM is proposed. It is suggested to allow achieving lower voltage distortion of the output compared to the unipolar PWM.

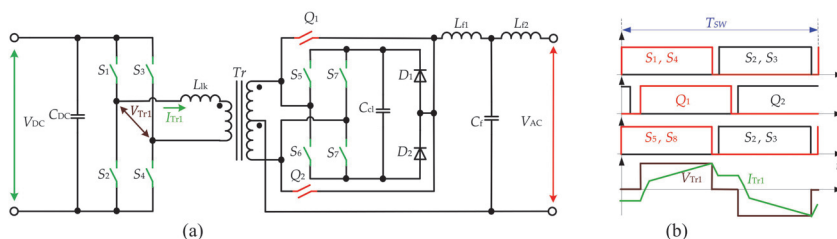


Figure 15. PP configuration with voltage clamber (a) and modulation (b) in [83].

### 3.2.3. PP Configuration with the Current Clamping Switch

The topology presented in Figure 16 [120–122] uses a standard full-bridge at the DC side. However, the AC side is realized with a center-tapped transformer and three bidirectional switches. In the original paper, the AC side structure was described as “three bidirectional switching arms” and referred to as PP configuration with the current clamping switch in this review due to the topology configuration. The DC side FB converts the DC voltage to the HF AC square wave. On the AC side, the switching signals are obtained by comparing the modulating waveform with the sawtooth carrier waveform. The bidirectional switch Q3 connected to the center tap is turned on when both Q1 and Q2 are in the off-state to provide a freewheeling path for the output current. The additional overlap is added to realize the natural commutation of semiconductor devices and reduce overvoltage. The converter realizes ZVS and ZCS for the semiconductor switches and requires three bidirectional switches instead of four for the FB–FB topology. The bidirectional operation capability is reported, but not addressed.

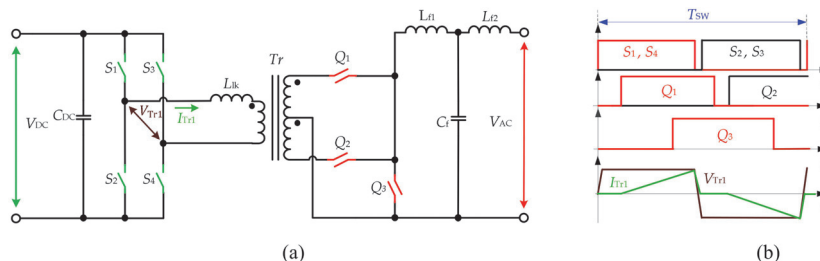


Figure 16. PP configuration with the current clamping switch (a) and modulation (b) in [121].

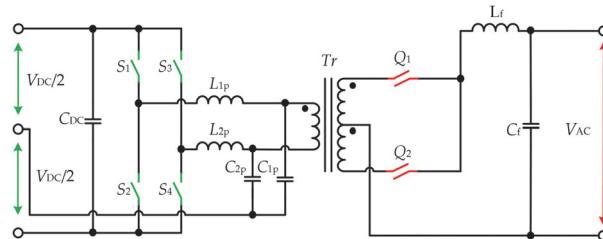
Other versions of the topology for the bidirectional battery charger are reported in [85]. It utilizes three bidirectional switches with regenerative flyback clamp circuit at the AC side, while the DC side is FB. The presence of the clamping circuit allows the reduction of the voltage overshoot in AC and also helps to achieve the ZCS in the AC switches. The energy stored in the clamp capacitor is returned to the DC side and reused. The unipolar SPWM modulation strategy is used for both power transfer directions. The concept is verified with a 1.5-kW prototype with a 96% peak efficiency conversion from 300-V battery to the 120-V RMS grid.

### 3.3. Resonant PP Topologies

#### PP Configuration with a Parallel Resonant Tank at the DC Side

In [80], the sine AM modulation (SAM) was proposed as an alternative approach for the conventional PWM with varied duty cycles. The topology consists of the PP configuration at the AC side and the FB with the parallel resonant tank at the DC side (Figure 17). The resonant tank

is connected between the middle point of the bridge legs and the middle point of the input voltage source. The bridge leg is operated with a varying duty cycle and a constant phase shift. The switching frequency of the converter is slightly higher than the resonant to extend the load independence and enable ZVS in the semiconductors.



**Figure 17.** PP configuration with a parallel resonant tank at the DC side.

The results are verified with a simulation model of a 2-kW converter. The converters with the parallel and with the series resonant tank were analyzed for the connection 450-V DC source with the utility grid. It is shown that the topology in Figure 17 has lower efficiency than the voltage source version on the topology with the series resonant tank, which will be described later.

The resonant inverter based on the topology from Figure 13 was introduced in [123,124] and described in more detail in [125]. It uses a resonant capacitor in series to the leakage inductance. The topology is proposed for the UPS application and features a lower output voltage ripple. It allows soft switching in the semiconductors using the SPWM modulation applied for FB thanks to the presence of the resonant tank at the DC side. The AC-side switches are forming, working at the grid AC waveforms.

#### 4. VSI Based Topologies

This section presents the topologies of the isolated matrix inverters with a grid side switching stage based on the VSI. The subsections are organized according to the fourth hierarchical level of the classification from Figure 5.

##### 4.1. Non-Resonant Bridge Topologies

###### 4.1.1. FB Configuration

Many different configurations of the VSI-based converters have been reported (also known as a dual active bridge) [55,56,77,125–136]. In [105], the topology consists of two voltage source full-bridges, as shown in Figure 18. The advanced modulation strategy proposed is based on the triple-phase shift. The method allows for achieving soft-switching in a wide range of voltage and load. The experimental 300-W prototype microinverter for the integration of the low-voltage DC source to the AC confirmed theoretical descriptions in that work. The authors proposed the extension of this configuration for the 3-port converter. In this case, in the first port is the PV module, the second—a battery and the third the AC grid. The connection of this part was made through the three-winding transformer. In general, the topology is suitable for different voltage levels, but the design of the high-frequency transformer can be a challenging part.

For the high-power applications, the VSI three-phase topologies can also be utilized (Figure 19). References [101,106,126–128] present PV inverter, battery storage and EV charger systems. In those systems, the PSM modulation strategy was used and is extended for the three-phase implementation. In [127], the three-port three-phase converter was proposed for interfacing between the renewable source, battery and the utility grid controlled by PSM.

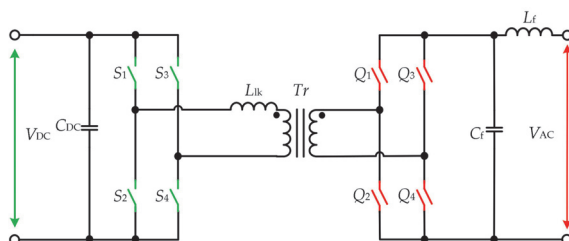


Figure 18. FB configuration.

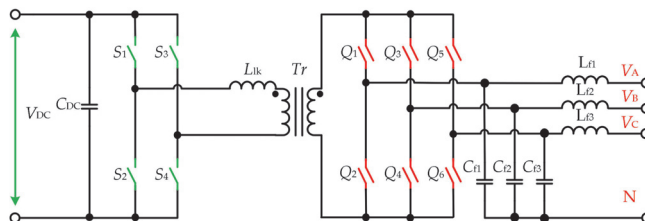


Figure 19. Three-phase FB configuration.

### 4.1.2. HB Configuration

The bidirectional converter in Figure 20 is proposed for electric vehicle charging with power factor correction functionality [66,100]. The topology features a voltage source converter with two bidirectional switches and two capacitors on the AC side. At the DC side, a standard FB is applied. Additional inductors are supplied to both sides of the converter to reduce the current ripple. Thus, the DC side has the same number of switches, while the AC side has a twice reduced number of switches when compared to the FB–FB topology. The converter control algorithm is based on a general trapezoidal current mode modulation of the voltage source DC–DC converter and is operating with a combined phase shift and frequency modulation for shaping the transformer leakage inductance current. This method is used to transfer high power with small peak current and achieve ZVS at any time interval. Peak efficiency of 95% is obtained at half load for a 3.3-kW prototype and is claimed to potentially reach 97%, the value of efficiency depending on the battery voltage. At the same time, the converter requires rather complex multi-mode control with lookup tables to guarantee ZVS within the full range of operating conditions. The wide ratio of operating frequencies (1:6) imposes additional requirements on the design of passive elements. In practical systems, the efficiency is limited since certain minimum commutation current is required to guarantee ZVS over the whole AC grid cycle. The aim was to design a converter suitable for the medium/high voltage battery energy system. In this case, the converter submodules are connected per phase in series and share one filter inductance.

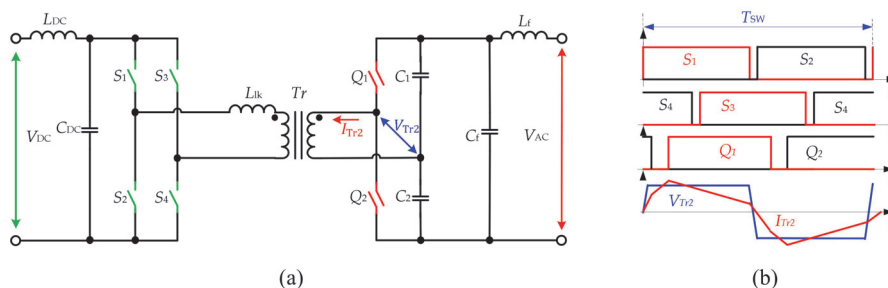


Figure 20. HB configuration (a) and modulation (b) in [66].

In [128], a 3-phase HB configuration of the VSI is proposed for the bidirectional conversion between the renewable source and the grid using the novel PSM modulation for the converter.

### 4.2. Resonant Bridge Topologies

#### 4.2.1. FB Configuration with the Series Resonant Tank

Application of the series resonant FB inverter is shown in Figure 21 [60,129]. A converter for the photovoltaic application was proposed and verified in [60]. The converter consists of two full-bridges and transformer leakage inductance with the resonance capacitor forming the series resonant tank. As a result, the DC side PSM strategy and resonant tank allow achieving the soft switching in all devices. In [129], the topology was reported as the bidirectional charger for the electric vehicle. The converter operation is similar to that previously discussed, but it is shown for both power flow directions: from the grid to electric vehicle and back.

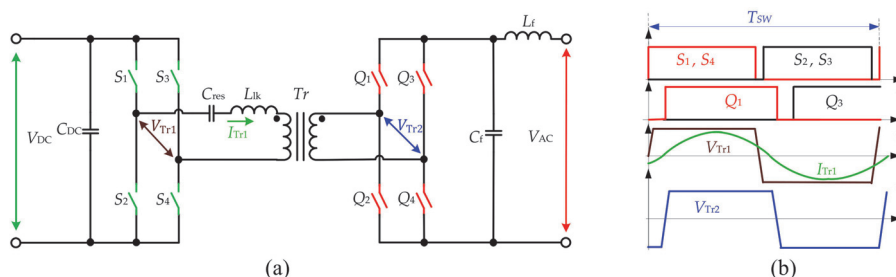


Figure 21. FB configuration with the series resonant tank (a) and modulation (b) in [60].

#### 4.2.2. FB Configuration with the Series Resonant Tank and HB at the DC Side

The topology in Figure 22 is a FB topology with the series resonant tank and HB DC side, which is described in detail in [130] and proposed for UPS. The inverter uses the modulation of the DC side and allows achieving quasi ZCS on the switches. A small-scale converter prototype was shown, along with experimental waveforms with linear and nonlinear loads. As the drawback of the topology is that the current in the DC-side switches is higher compared to the FB–FB converter, the topology is more suitable for low-power applications.

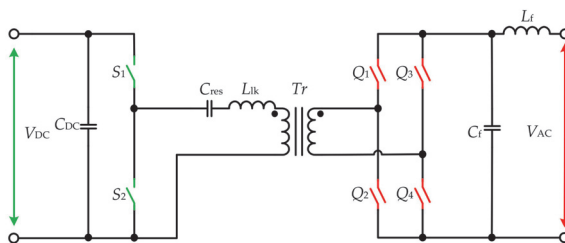


Figure 22. FB configuration with the series resonant tank and HB at the DC side.

#### 4.2.3. HB Configuration with the Series Resonant Tank

The circuit (Figure 23) for a PV microinverter is presented in [86]. The topology is based on a series resonant inverter at the DC side and HB voltage-doubler configuration at the AC side. The special dual-phase shift modulation strategy for the topology allows achieving ZVS for all semiconductors. The experimental prototype for the integration of the low-voltage DC to AC grid with almost 96% CEC efficiency was shown.

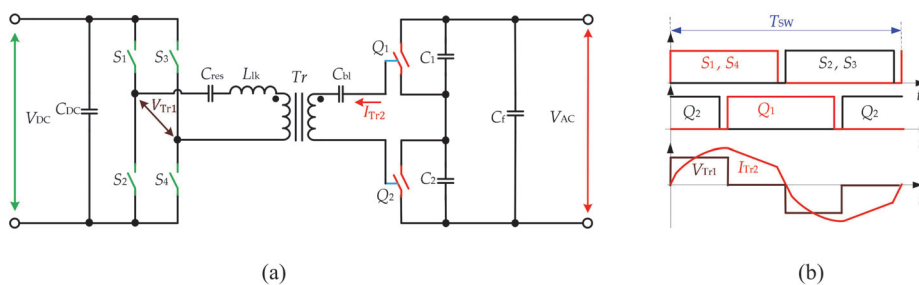


Figure 23. HB with the series resonant tank (a) and modulation (b) in [86].

An alternative version of the topology is addressed in [102]. The topology has similarity with Figure 23, but does not contain the resonant tank and blocking capacitor. Instead, the additional snubber capacitor at the AC side is used, which provides the current path and no overshoot from leakage energy is present at the AC-side switches. The topology was built in gallium nitride (GaN) switches and used the dual-phase shift with variable frequency modulation to achieve ZVS. The hardware prototype is shown to have the rectification from 230-V AC to 48-V DC. The topology is also capable of DC AC conversion; however, this operation is not described.

#### 4.2.4. HB Configuration with the Series Resonant Tank and HB at the DC Side

The converter in Figure 24 is recommended for an electric vehicle battery charger [107,131]. The topology utilizes resonant HB with an active shunt circuit, which absorbs the current ripple at the DC side. In addition, at the AC side, the HB configuration is used. The presence of the active filter at the DC side allows the reduction of the double grid frequency ripple in the current and reduces the overheating of the battery. A special four-part control PSM strategy is proposed for the system, which allows operation with different power ranges and achieving ZVS for all semiconductors.

In [132], a variation of this topology is suggested for the on-board electric vehicle charger. This converter includes the resonant tank and additional boost–buck stage for the additional gain on the DC side, while the AC side is an HB. The topology does not require a bulky DC link between the boost–buck stage and the inverter stage. The authors proposed the harmonic modulation strategy, which allows improving the power factor in DCM. The 3-kW experimental bidirectional prototype was built with an efficiency of 93% at rated power.

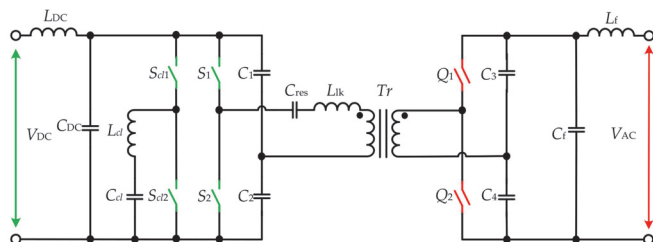


Figure 24. HB configuration with the series resonant tank and HB at the DC side for the electric vehicle battery charger.

### 4.3. Resonant PP Topologies

#### PP Configuration with the Series Resonant Tank

In [80], a topology consisting of the PP configuration at the AC side and the FB with the series resonant tank at the DC side is described (Figure 25). The series resonant tank is connected between the

middle point of the bridge legs, transformer AC sidewinding and the middle point of the input voltage source. The SAM modulation for the DC side semiconductor is presented. The 2-kW simulation model of the inverter was made for the connection 450-V DC source with the utility grid. Resulting from the comparative analysis in the paper, this topology has lower energy circulation, but higher THD, particularly at low power when compared to the CSI version of the topology in Figure 17 with the parallel resonant tank.

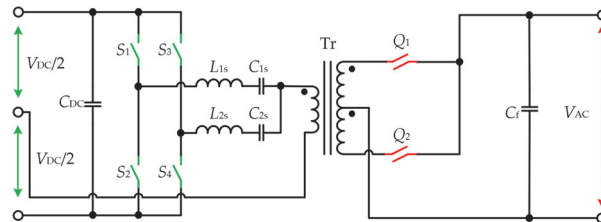


Figure 25. PP configuration with the series resonant tank.

## 5. Discussion and Future Trends

### 5.1. Critical Overview

An important contribution of this work is that it establishes the isolated matrix inverters as a class of true single-stage topologies separate from the quasi-single-stage class. This division is important as the isolated matrix inverters can provide a wider range of features. Besides being the true single-stage solution, these inverters have the following advantages:

- they could provide the soft switching in all semiconductor switches using special modulation strategies;
- in the voltage step-up applications, they avoid unreliable high-voltage electrolytic capacitor(s) with a limited lifetime and utilize much more reliable low-voltage electrolytic capacitor(s) for the filtering of 100/120 Hz voltage ripple;
- their cost can be reduced considerably with the implementation of emerging bidirectional monolithic semiconductors or the ones with the reverse blocking capability.

The main disadvantage of the isolated matrix inverters compared to their two-stage counterparts is their relatively narrow input DC voltage range, which limits their applicability in demanding applications. Other disadvantages can be associated with the limitations of the general level of technologies rather than the concept itself. For example, the level of control complexity was not compatible with the existing technology when the first topologies appeared around 30 years ago. This was holding back the adoption of these inverters for some time. Nowadays, available low-cost microcontrollers can realize control of the isolated matrix inverters. Moreover, recent appearance of numerous two- and quasi-single-stage solutions had gained popularity despite even more complicated control. Therefore, the isolated matrix inverters can also be accepted by industry if sufficient awareness is raised.

Among the two main families of topologies, the CSI based isolated matrix inverters attracted more attention of researchers compared to the VSI based counterparts, which resulted in twice as many topologies developed. It can be attributed to their use of conventional LC and LCL filters, which makes them a logical replacement of two-stage counterparts with the same filter type. In both groups, around half of the reported topologies were developed in the last five years, which shows high activity in this field of research. Nevertheless, both converter groups demonstrate efficiency growth from roughly 90% in early works up to 96% in later developments. It is worth mentioning that the CSI based topologies have demonstrated high efficiency in a wider range of applications. Most of the research was dedicated to the bridge type isolated matrix inverters, where the most prominent example is the single-phase



full-bridge implementation. The widest number of modulations was applied to full-bridge topologies as they provide the widest range of the possible switching states and thus ensure the best controllability. In addition, they were justified for most of the possible applications. The push–pull type isolated matrix inverters are the second most used type. They allow reduction of the amount of the active component and, in some cases, can avoid auxiliary clamping circuits. However, the utilization of an auxiliary clamping circuit could result in the number of the switches lower than that in the full-bridge type counterparts. Push–pull type isolated matrix inverters can be more beneficial in low-power applications. For example, they were mostly proposed for the PV microinverter and chargers with the power rating below two kilowatts. Meanwhile, three-phase implementations are feasible for both full-bridge and push–pull type inverters. They can be useful in high-power applications rated for over one kilowatt, which is justified by application examples for the high voltage BESS and PV inverters. Among possible derivations of the bridge type topologies, the LL HB type inverters were used in battery chargers due to their very low current ripple and simple modulation. The other examples of the half-bridge type inverters were mostly used to reduce the number of active semiconductors and associated costs.

The isolated matrix inverters reported and analyzed in the review are typically two-level topologies. The main properties and features of two-stage, quasi-single-stage and isolated matrix inverters are summarized in Table 1.

**Table 1.** Evaluative comparison of various isolated inverter topologies.

Topology	DC Link	Number of Conversion Stages	Soft Switching in Transistors	Use of Bidirectional Switches	DC Voltage Regulation Range
Two-stage	Bulky	2 stages	DC/DC—soft DC/AC—hard	No	Moderate-wide
Quasi-single-stage	Small (optional)	1 stage	Soft	No	Limited
Single-stage	Absent	1 stage	Soft	Yes	Limited

## 5.2. Design Challenges

During the 30-year history of the research and developments of the isolated matrix inverters, numerous topologies were proposed. In the 1990s, the proposed topologies were based on thyristors and IGBT devices, with the switching frequencies up to 10–15 kHz. Their demonstrated efficiency usually did not exceed 90%. The main research trends in the field were dedicated to topological aspects, the optimization of the components (especially AC side filters), optimization and improvements of the system efficiency, improvements of the rectifier mode operation capability. In addition, research directed toward synthesis of new modulation techniques that either utilize parasitic components for soft switching or limit their influence on converter operation as some of them are unavoidable, e.g., leakage inductance, the capacitance of the transformer, the capacitance of the switches and PCB. These improvements together with development in component semiconductor and magnetic material technologies enabled the use of significantly increased switching frequencies (up to 200 kHz), improved power density, resulting from the reduced size of the magnetic components. Moreover, this allowed an increase in the efficiency to 96%, which now is comparable and sometimes superior to the two-stage conversion systems. Nevertheless, various design challenges related to isolated matrix converters still exist, the majority pertaining to optimization of operating conditions for semiconductors and transformer design aspects.

### 5.2.1. Semiconductors

The isolated matrix inverter technology evolved together with power semiconductor devices, moving from Si thyristor, IGBTs and MOSFETs to WBG semiconductors. New generation power semiconductor devices, such as GaN HEMTs, SiC MOSFETs and Schottky diodes, enable substantial reduction of the losses associated with transistor switching and diode reverse recovery, allowing much higher switching frequencies to be used. On the other hand, the use of bidirectional switches and high



number of discrete semiconductor components could discourage industrial adoption of the isolated matrix inverters. However, this number is in fact similar to that of industry-approved two-stage and quasi-single-stage solutions. Moreover, a new impulse for industrialization can be given by the recent developments in monolithic reverse-blocking and bidirectional semiconductor devices that have been reported for Si, SiC and GaN technologies [137–142]. This technology can make the isolated matrix inverters attractive to the industry by reducing the number of discrete devices by up to twofold at the AC side.

### 5.2.2. Isolation Transformer

The use of the HF transformers imposes challenges on the scalability of the isolated matrix inverters. The limiting factors are core losses (losses from eddy current and magnetic losses), high-frequency losses (skin and proximity effects and winding losses in the high current application), parasitic resonances (usually between the capacitance and leakage inductance of the transformer, but the topology has some influence on it) [143]. Depending on the operating switching frequency, the impact of the total transformer losses in the total power loss will be different. For switching frequencies of up to a few dozen kHz, GTOs and IGBTs are commonly utilized, which results in the dominant impact of their switching losses on the overall efficiency. At higher switching frequencies, where the implementation of Si, SiC and GaN devices is favored, an increased impact of the transformer losses is expected. The soft switching range in the CSI based galvanically isolated matrix inverters is usually determined by the values of the transformer leakage inductance and parasitic capacitance. In the VSI based solutions, the value of the leakage inductance has an effect on regulation near the voltage zero-crossing point. The transformer power and turns ratio significantly influence the values of the parasitic parameters and, consequently, limit the overall efficiency. The scaling of the transformer is mostly defined by the required power rating and power density. A compact design usually requires increasing the working frequency but results in lower efficiencies. Finding the tradeoff between the target power density and efficiency of an inverter may require an iterative search for the optimal topology as a compact transformer design could result in such a combination of switching frequency and the leakage inductance that may limit the feasibility of some of the topologies. The isolated matrix converter prototypes reported in the literature have been mainly using ferrite RM cores for powers <1 kW and toroid or E cores for powers over one kilowatt. Improved transformer characteristics may be obtained with amorphous and nanocrystalline magnetic materials, which can result in core losses reduction by up to 70% than conventional solutions [144,145].

### 5.3. Application Examples

The practical realization of the isolated matrix inverters for a target application depends on the engineering design and limitations of existing technologies of semiconductor and magnetic components. Hence, it is important to compile a comprehensive list of application examples with key operating parameters to provide an initial suggestion regarding the suitability of a topology to a certain application. Therefore, application examples of the isolated matrix inverters were summarized in Table 2 to provide a critical view of the practical value of each of the roughly thirty topologies and support claims of this section. The comparison considers the number of switches on both sides separately, transformer turns ratio, maximum power and reported experimental efficiency, input and output voltage level or range, switching frequency and the used modulation technique. As can be seen from the table, the technology of isolated matrix inverters is a versatile solution that suits different applications.

Table 2. Summary of the existing solutions of the isolated matrix inverters.

AC Side-Based Topology	Reference	Peak Efficiency	Year	Number of DC Side Switches	Number of AC Side Switches	Modulation Strategy	The Ratio of HF Transformer	Power, kW	DC Voltage, V	AC Voltage, Vrms	Switching Frequency, kHz	Application
CSI-based												
FB	[58]	89	1990	4	8	PSM	—	1	180	100	20	UPS
	[46]	—	2006	4	8	PSM	1:1	10	600	230	6	MVC
	[47]	96	2018	4	8	PWM	1:1	1.2	400	240	54	HF AC grid
	[51]	96.5	2018	4	8	PWM	1:1	1.2	300	120	50	—
	[52]	—	2019	4	8	PSM	1:1.1	1.2	400	220	50	PV
FB with reconfig. output	[62]	92.5	2010	4	16	PWM	2x1.6.5	1	30–60	120/240	—	FC
FB 3-leg DC side	[79]	95.1	2020	6	8	PSM	—	0.34	34	240	25, 50	PV MIC*
FB	[58]	—	1990	4	12	PSM	—	1	200	100	20	UPS
3-phase	[76]	—	2006	4	12	PSM	1:1	40	600	230	6	MVC
HB	[115]	—	2011	4	4	PWM	3:1.3	1	36	98–100	20	PV MIC
LL HB	[97]	96.5	2017	2	4	PSM	1:5	1.5	220–336	120	100	EV
LL HB	[98]	—	2019	6	12	PSM	—	10	220–336	120	100	EV
3-phase PP	[67]	89	2011	12	12	PWM	—	1	90	90 <sup>~</sup>	20	AC drive
3-phase PP resonant	[80]	—	2018	4	4	AM	—	2	450	230	50	—
	[82]	88	1990	4	4+4(cl)	PWM	—	10	—	100	20	UPS
	[83]	90	2016	4	4+4(cl)	PWM	24:23.8	1	60	100	20	—
PP with voltage clamper	[75]	96	2016	4	4+4(cl) <sup>~</sup>	PWM	14:4	0.08	10	25 <sup>~</sup>	200	D AMP*
	[81]	93.5	2018	4	4+4(cl)	PWM	7:7.20	0.2	340–370	40	200	—
PP with current clamper	[112]	—	2004	4	6	PWM	—	—	150	230	25	—
	[85]	96	2019	4	6+4(cl)	PWM	3:8	1.5	300	120	50	EV
VSI-based												
FB	[105]	91	2020	4	8	PSM	1:5	0.2	48	110	50	PV MIC
FB resonant	[60]	—	2011	4	16	PSM	1:6.5	1	30–60	120	100	PV, EV
	[129]	94.5	2016	4	4	PSM	1:6.6	0.25	30–48	110	50	PV MIC
HB	[61]	—	2016	4	4	PSM + FM	1:1.3	3.3	280–420	230	20–120	EV
	[127]	95.5	2014	4	4	FM	1:0.7	3	280–450	230/110	100	EV
HB resonant	[86]	96	2010	4	4	PSM+FM	1:7.5	0.175	25–40	240	45–350	PV MIC
	[131]	—	2016	4	4	PSM	—	3	400	230	60	EV
FB	[53]	—	2018	4	12	PWM	—	10	200	100	20	Battery storage
3-phase	[126]	—	2012	4	12	PSM	—	10	600	230	36	PV inverter
HB	[127]	—	2019	6+2(cl)	6	PSM	1:1	1.1	530	311	20	—

\* PV MIC—PV microinverter, D AMP—D class audio amplifier, cl—additional clamping switch<sup>~</sup>—from oscillograms

It is worth mentioning that the compiled list of application examples is reflecting the current state-of-the-art and does not limit future applications. It could be expected that they can be used in more electric aircraft [146], where conventional matrix converters were justified. Currently, only VSI based solutions were adopted by industry for PV microinverter applications. However, in the last few years, early attempts of industrialization of the CSI based isolated matrix inverters have emerged. For example, “ACDC cube” project of INESC TEC in Portugal [147]. More commercial products employing CSI based solutions can be expected in the future. This paper aims to facilitate its wider industrial acceptance.

## 6. Conclusions

This paper provides a fresh view of existing galvanically isolated inverters and establishes their division into three main classes: two-stage, quasi-single-stage and single-stage. The superiority of features provided by the single-stage solutions makes the isolated matrix inverters a promising solution. Currently, over thirty topologies have been reported where two-thirds belong to the group based on current-source inverters. They have attracted more research interest as the logical replacement of two-stage solutions with the same LC or LCL grid side filter. Nevertheless, the VSI-based topologies can demonstrate equally high efficiencies of 96% and have been industrialized already in the PV microinverter applications. Regardless of the basic inverter topology, full-bridge solutions are the most popular due to their high control and modulation flexibility. This trend is expected to continue in the future, but push–pull converters with voltage or current clamping will also gain momentum in development.

Vast majority of the topologies presented in this review were found to use either PWM or PSM. The CSI-based isolated matrix inverters are using PWM twice as often as PSM. However, both modulations have shown the capability of achieving 96.5% efficiency under similar operation parameters. At the same time, the voltage source-based topologies are using PSM three times more often than PWM. Here, PSM showed better efficiency levels than in the case of PWM mainly due to utilization of more than one phase shift. More sophisticated methods additionally apply FM to obtain even better characteristics.

The suggested range of existing applications is wide, but most of the topologies were proposed for photovoltaic, battery energy storage, electric vehicle charging and uninterruptible power supply applications. Less common applications include D class audio amplifiers, adjustable speed drives, medium voltage converters, fuel cells and local high-frequency AC grid forming. This proves the versatility of the isolated matrix inverters and shows that much wider application areas can be expected to appear in the near future.

Future research is expected to be focused on the development of new modulation techniques (mostly based on PWM and PSM), voltage range extension at the DC side, optimization of component sizes (especially AC side filter), experimental validation of benefits of the isolated matrix inverters in new applications (e.g., more electric aircraft, electric transportation, grid-connected rectifiers, etc.). Another important research topic relevant to industrial acceptance lies in the accumulation of additional knowledge in control and regulation methods for these inverters. For example, it is required to investigate the use of isolated matrix inverters in reactive power regulation, power quality and grid code compatibility potential, including fault ride-through capabilities.

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**Publication II**

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# Analysis of Oscillation Suppression Methods in the AC-AC Stage of High Frequency Link Converters

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**Abstract** — This paper addresses various oscillation suppression methods in the AC-AC cycloconverter stage of a high frequency link inverter. Such oscillations occur after the natural commutation of the switches due to parasitic parameters of the converter circuit. A mathematic analysis of the resonance process in the cycloconverter stage is presented, followed by a comparative analysis of different snubber circuits that allow to minimize the effect of oscillations. The theoretical analysis is verified with software models and experimental prototype of 1 kW DC-AC converter.

**Keywords:** DC-AC power converters, cycloconverter, high frequency link, soft switching, zero voltage switching (ZVS), zero current switching (ZCS).

## I. INTRODUCTION

The intermittent behaviour of the renewable generation promotes application of energy storage and associated energy management systems to increase self-consumption and enable more optimal use of available energy. Power electronic converters are providing an interface between various generators and storages with the electrical AC grid.

In residential applications, low voltage (LV) batteries (around 48 V nominal) are a popular solution due to higher modularity, safety and possibility for reduced initial investments. For integration of such systems, power electronic systems with two stages of conversion are typically used [1]. In the first stage (DC-DC), the low voltage of a battery is stepped up and, after stabilization at the DC-link, the following inverter stage is converting it to the AC grid voltage. The main drawback lies in the requirement of the high voltage DC capacitor, which can compromise reliability and cost.

Alternatively, single stage converters, such as high frequency link-based converter (HFLC) can be applied. These converters can perform bidirectional power conversion without intermediate DC-link, allowing to reduce the system price and increase reliability. Different types of the DC-AC HFLCs have been developed [2]-[4], [6]-[11]. With the implementation of advanced control and design approaches, it is possible to achieve soft switching of converter switches and reduce the switching frequency of some devices, thus reducing the power losses and improving the efficiency [2]. These features make these converters a promising solution for battery energy storage systems.

Converter selected for the present study includes the full bridge inverter at the DC battery side and a cycloconverter stage at the AC side, connected through the high frequency transformer (Fig. 1). The voltage source inverter is formed by four unidirectional switches T1–T4, that convert the DC

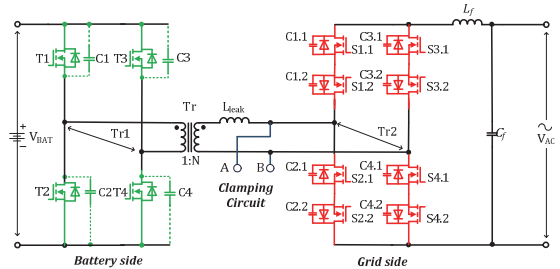


Fig. 1 High-frequency link converter topology (HFLC)

voltage from the source to the high frequency (HF) AC square pulses, which are stepped up by a HF transformer (Tr).

The cycloconverter stage forms the output grid voltage by the sine pulse width modulation (SPWM). This stage could be realized with the anti-series connection of two MOSFETs / IGBTs or anti-parallel connection of two GTOs or reverse blocking IGBTs [12]-[13], forming the four-quadrant bidirectional switch (4Q). The capacitors C1...C4 represent switch intrinsic capacitances or additional snubber capacitors in parallel. The capacitors C1.1...C4.2 present the output capacitance of the high voltage switches. The cycloconverter stage is interfaced with the grid with LC filter.

The major challenge of HFLC bidirectional DC/AC HFLC topology is that both the transformer leakage inductance and output filter inductor serve as current sources. The current mismatch that occurs due to commutations generates high-voltage overshoots across the cycloconverter switches [6]-[8]. Special circuits and modulation algorithms are used to address this problem and utilize the leakage energy to enable soft switching conditions for the semiconductors [6]-[11], [13]. Typically, the strategies take advantage of the natural commutation of the semiconductors for their turn-off. These measures generally solve the problem related to current mismatch. However, due to resonance between the circuit inductance (mainly determined by transformer leakage inductance) and parasitic capacitances (of MOSFETs and other circuit components) a voltage overshoot still occurs, followed by parasitic oscillations. Despite that their amplitude is significantly lower than in the case of hard switching, those can still lead to an avalanche effect in the semiconductors. Even if rugged devices, like SiC MOSFETs are applied [14], the total power losses and temperature would increase, resulting in decreased reliability and performance [15][9],[16].

The minimization of the leakage inductance of the high-frequency transformer will reduce the impact of the voltage overshoots. Planar transformers and manufacturing techniques, such as interleaving of the windings, are applied to reduce the value of the magneto-motive force and achieve

lower leakage inductance [17]. However, the problem is more pronounced in the LV battery applications, where, the undesirably high value of leakage inductance is much harder to avoid due to high turns ratio and increased copper thickness requirements [18]. At the same time the utilization of high frequency in the planar transformer can increase the power losses due to the skin and the proximity effects [17],[18][18].

The current study is focused on the analytical description of the parasitic processes that occur during the HFLC operation with phase-shift control strategy presented in [20] for the DC-DC operation. The control strategy was extended to the DC-AC operation, where the phase-shift is changed from the minimum to maximum during one fundamental AC half-period to form the output 50 Hz AC sine-wave.

A simulation model is created to verify the findings and analyse different voltage overshoot suppression methods presented in the literature. The model assumes typical leakage inductance values for a 1:10 transformer with interleaved Litz-wire windings. The model parameters and characteristics are verified using the 1 kW HFLC prototype.

## II. DESCRIPTION OF THE RESONANCE PROCESS

The natural commutation cycloconverter switches assumes synchronous rectification of MOSFETs, with certain interval of body diode conduction. These intervals occur during the switching transients, when the  $di/dt$  in the circuit is defined by its parasitic parameters and not by the switching speed of the MOSFETs. During the reverse bias of the body diode this results in a voltage overshoot across the device, which is also visible across the transformer HV winding.

The overshoot occurs due to extra energy stored in the circuit inductance, which together with parasitic capacitances and equivalent resistance creates a damped RLC circuit. The oscillations in this circuit can impose a significant influence on the converter operation, particularly at high switching frequencies. The resonant frequency of the oscillatory circuit is estimated by

$$\omega_0 = \frac{1}{\sqrt{L_{eq} \cdot C_{eq}}}, \quad (1)$$

where  $L_{eq}$  and  $C_{eq}$  are the equivalent circuit inductance and capacitance, respectively. The damping coefficient is

$$\delta = \frac{R_{eq}}{2 \cdot L_{eq}}, \quad (2)$$

where  $R_{eq}$  is the equivalent high frequency resistance of the circuit. Considering its effect, the actual resonant frequency becomes

$$\omega = \sqrt{\omega_0^2 - \delta^2}. \quad (3)$$

The first overshoot occurs after the transformer polarity change at the start of reverse energy transfer interval. Assuming that there are no oscillations in the circuit since the previous commutation and neglecting the influence of reverse recovery, its peak amplitude can be estimated by:

$$U_{peak1} = U_{Tr2} \cdot (1 + 2 \cdot k), \quad (4)$$

where  $U_{Tr2}$  is the cycloconverter-side steady-state voltage of transformer and  $k_l$  is the damping at one half of the resonant interval:

$$k_l = e^{-\frac{\delta}{2 \cdot f_{res}}}. \quad (5)$$

The second and third overshoots have the amplitude of

$$U_{peak2} = U_{Tr2} \cdot (1 + k). \quad (6)$$

After reaching its peak after one half of the first resonance period the voltage starts to decay according to the following equation:

$$U_{osc1,2}(t) = U_{Tr2} + \frac{(U_{peak1,2} - U_{Tr2}) \cdot \omega_0}{\omega} \cdot \cos\left(\omega \cdot t - \arctg\left(\frac{\delta}{\omega}\right)\right) \cdot e^{-\delta \cdot t}. \quad (7)$$

During this period the current in the circuit follows the equation:

$$i_{osc1}(t) = i_{Tr2} + \frac{U_{peak2} \cdot \omega_0}{2 \cdot \omega^2 \cdot L_{eq}} \cdot \sin(k_2) \cdot e^{-\delta \cdot t}, \quad (8)$$

$$i_{osc2}(t) = i_{Tr2} + \frac{2 \cdot U_{Tr2} \cdot \omega_0}{2 \cdot \omega^2 \cdot L_{eq}} \cdot \sin(k_2) \cdot e^{-\delta \cdot t}, \quad (9)$$

where:

$$k_2 = \omega \cdot t - \arctg\left(\frac{\delta}{\omega}\right). \quad (10)$$

The peak current can be determined by

$$I_{peak1} = \frac{2 \cdot U_{Tr2}}{\omega \cdot L_{eq}}, \quad (11)$$

$$I_{peak2} = \frac{U_{peak2}}{2 \cdot \omega \cdot L_{eq}}. \quad (12)$$

The energy in the circuit decays according to

$$E_{osc1,2}(t) = \frac{1}{2} \cdot L_{eq} \cdot I_{peak1,2}^2 \cdot e^{-2 \cdot \delta \cdot t}. \quad (13)$$

Since the energy return-related overshoot occurs two times and the following overshoots four times during the switching period, the energy dissipated can be estimated according to:

$$P_{osc1} = I_{peak1}^2 \cdot L_{eq} \cdot f_{sw} \cdot \dots \quad (14)$$

$$P_{osc2} = 2 \cdot I_{peak2}^2 \cdot L_{eq} \cdot f_{sw} \cdot \dots$$

Assuming that all of the stored energy is dissipated and considering the circuit parameters listed in Table I, the total power loss equals 42 W. In the real circuit, the dissipation is lower, since the following overshoots occur before the energy from the previous one is dissipated completely.



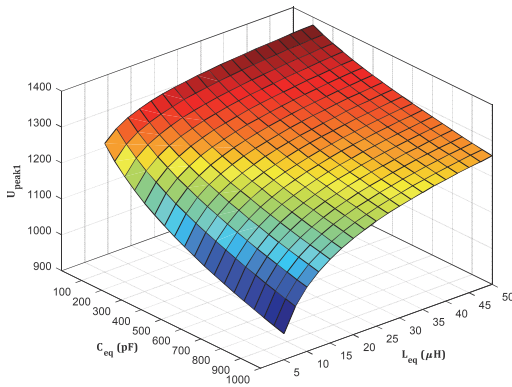

 Fig. 2  $U_{peak1}$  as a function of  $L_{eq}$  and  $C_{eq}$  at  $R_{eq}=30$  Ohm and  $U_{Tr2}=480$  V

TABLE I SIMULATION PARAMETERS DC-AC HFLC

Parameter	Symbol	Value
Converter power rating, kW	$P_r$	1
Battery voltage, V	$V_{BAT}$	48
Output voltage, V	$V_{AC}$	230
Switching frequency, kHz	$f_{sw}$	50
Transformer turns ratio	$N$	10
Transformer leakage inductance, uH	$L_{leak}$	28
Output filter inductance, mH	$L_f$	1
Output filter capacitance, uF	$C_f$	0.47

The Fig 2 presents the amplitude value of the first voltage overshoot across cycloconverter devices for various equivalent inductance and capacitance values. As observed, certain combinations result in values over 1200 V, which would require additional measures in order to optimally use 1.2 kV devices.

### III. OVERTSHOOT SUPPRESSION METHODS

Different ways to minimize the effect of the oscillation overshoots have been presented in the literature. The simplest one is to use the RC snubber circuit (Fig. 3 a). Its main drawback lies in requirement of the powerful resistor and significant power dissipation. Although it is relatively simple to design and apply, the efficiency on HFLC is reduced, especially if leakage inductance is relatively high.

Another passive snubber, which allows reducing overshoots includes a full bridge with Schottky diodes, a capacitor for voltage stabilization and a resistor which converts the energy into heat (further referred to as FB-type) is shown in Fig. 3 b. The method, in general, shares the advantages and drawbacks of the previous one. Reference [6][7] describes the circuit, consisting of two diodes that can clamp the transistor node to DC-side voltage. It can be advantageous in the designs where additional inductance is provided by an external inductance connected in series to the transformer winding. However, it does not solve the problem in the case the transformer internal leakage inductance is high.

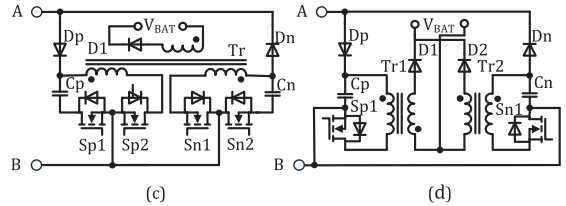
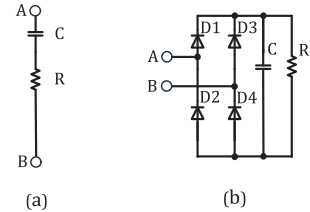


Fig. 3 Different snubbers and clamping circuits: RC snubber (a), passive clamp with R load (FB-type) (b), regenerative snubber (flyback-based) type 1 (c), regenerative snubber (flyback-based) type 2 (d).

The regenerative snubber circuits require the high amount of diodes and controlled switches and isolation transformer rated for full voltage, but this type allow to return the energy causing the oscillations back to the DC side. The regenerative snubber type 1 (RT-1, Fig. 3 c) requires two 4Q switches and three-winding flyback-type transformer with high voltage isolation. It regenerates the energy stored in capacitor Cn and Cp back to the battery and uses the same switching frequency as the main converter.

The regenerative snubber type 2 (RT-2, Fig. 3 d) has similar structure with lower number of switches but features two flyback-type transformers and can use switching frequency that is ten times lower when compared to the one of the main converter. The details of the snubber and clamping methods and indicates the number and type of the components used.

TABLE II COMPARISON OF CLAMPING METHODS

Snubber or clamping topology	Number of additional components				
	Resistor	Capacitor	Diode	Switch	Transformer
RC type snubber	1	1	-	-	-
RCD type snubber	1	1	2	-	-
Active clamp	-	1	-	2	-
Passive clamp with R load (FB-type)	-	1	4	-	-
Regenerative snubber (Flyback based) type 1	-	2	3	4	1
Regenerative snubber (Flyback based) type 2	-	2	4	2	2

### IV. SIMULATION AND EXPERIMENTAL VERIFICATION OF RESULTS

This section presents a simulation study of the different types of the snubber circuits for the full bridge soft switching DC-AC HFLC. The simulations were performed using PSIM 11.0 software. The parameters of the simulated converter are presented in Table I. Si MOSFETs (IPB017N08N5), with a blocking voltage of 80 V were selected for the battery side. SiC MOSFETs (C3M0120090D)



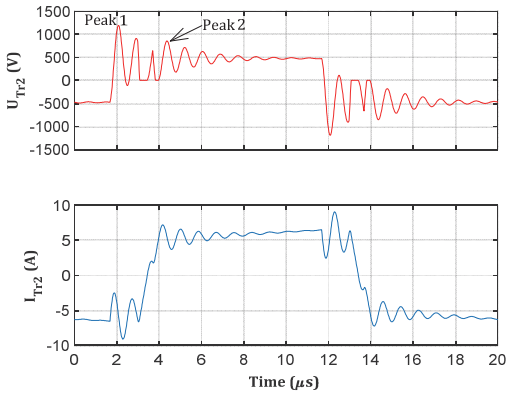


Fig. 4 Voltage and current across cycloconverter stage (Tr2) without snubber circuit

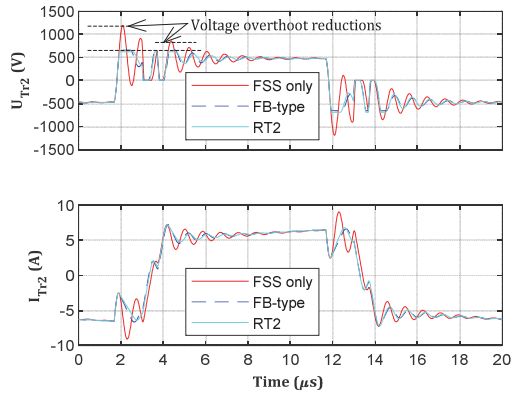


Fig. 5 Simulated voltage and current across cycloconverter stage (Tr2) with different types of snubber circuits

with a blocking voltage of 1200 V were selected for the grid side, which means that the voltage on the cycloconverter stage should not exceed 1200 V, but for safety margin the maximum allowed voltage of the overshoot was set to 700 V.

To achieve this target value, different snubbers circuit are simulated and one of them experimentally verified.

Simulated voltage and current waveforms, without any snubbers are presented in Fig. 4. As observed, the voltage has significant overshoots, which are close to the rated voltage of the chosen devices. To provide safer operation different types of the snubbers which presented in section III can be used.

TABLE III  
SIMULATED SNUBBER LOSSES IN DC-AC HFLC

Snubber circuit	Approximate losses value, W
RC type snubber	80...100
FB-type	10...20
RT-1	20...30
RT-2	15...20

Fig. 5 presents simulated waveforms of the transformer voltage and current at the cycloconverter stage with different types of the snubber's circuits. As observed, better results in terms overshoot suppression and efficiency were achieved using the flyback-type snubber (RT-2), that allows to transfer energy back to the battery. At the same time, this snubber requires the special flyback transformer and high number of the active switches. The utilization of the FB-type snubber results in higher losses (Table III) but provides more simplicity.

In order to verify the findings, the experimental was assembled (Fig. 6). Experimental steady-state waveforms of the cycloconverter stage of the DC-AC converter are presented in Fig.7. For the waveform acquisition the digital probes Tektronix TCP0150A, TCP030A and high-voltage differential voltage probes Tektronix P5205A were used.

The converter was supplied by the programmable power supply oscilloscope Tektronix DPO7254 equipped with the current AE PSI 9080-60 and loaded by the resistive load. First, the converter was tested in the mode without any snubber at  $V_{BAT}=48\text{ V}$  and  $P=1\text{ kW}$  (Fig. 7a, c). After, converter was tested in the same conditions using the passive

clamp with  $R=20\text{ k}\Omega$ , which allowed to reduce overshoot down to the desired value of 700 V.

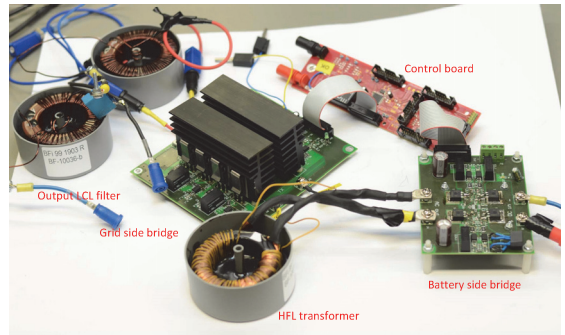


Fig. 6 Photo of the experimental setup

## V. CONCLUSIONS AND FUTURE WORK

Present study was focused on the analysis of the parasitic resonance issue, that occurs during the natural commutation of cycloconverter in the HFCLC and is responsible for voltage overshoot across the semiconductors. The damped oscillatory circuit is formed by leakage inductance of the transformer, switch capacitances and equivalent high frequency resistance. The analytical equations are derived to estimate the amplitude of voltage overshoots and study the oscillations. Several possible solutions for overshoot suppression were analysed. The analytical estimations are verified with the software model and experimental prototype. In the case of relatively small leakage inductance, the FB-type dissipative method can be applied to protect the semiconductors, without significantly affecting the efficiency. On the other hand, in applications, where the transformer leakage inductance is hard to minimize, active methods are more effective. According to the analysis performed, the regenerative snubber RT-2 provides a good balance between the effectiveness and complexity. At the same time, design of the transformer with high turns ratio and low leakage inductance will be addressed in the future research in order to reduce the power losses in the snubber.

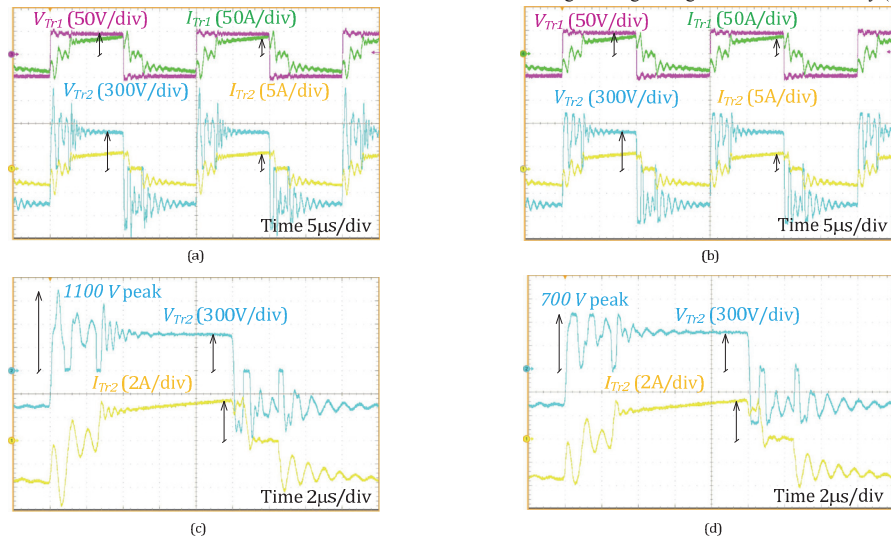


Fig. 7 Experimental steady-state waveforms voltage and current across the DC side and cycloconverter stage without snubber (a) and with FB-type (b); zoomed view of the oscillation without (c) and with snubber FB-type circuit (d)

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**Publication III**

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# Comparison of Soft Switching Methods of DC-AC Full Bridge High-Frequency Link Converter

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**Abstract** — This paper presents a comparative analysis of soft switching methods with modulation on the current-fed (grid) side of a high-frequency link converter. The focus is on methods that provide clamping and soft switching without auxiliary circuits. Firstly, the case study converter topology used for the generation of the AC line voltage from the low DC voltage, such as a battery, is presented in brief. Secondly, the time interval requirements for soft switching conditions are described, and the peculiarities of the studied algorithms are summarized. Finally, the algorithms are verified with a simulation model of a 1 kW converter incorporating thermal models of semiconductor switches. The converter performance in terms of regulation capability, current stresses and semiconductor losses with different modulation methods are analyzed and compared.

**Keywords:** DC-AC power converters, soft switching, zero voltage switching (ZVS), zero current switching (ZCS).

## I. INTRODUCTION

The share of renewable energy in energy supply is continuously increasing. According to recent forecasts, the global photovoltaic installed capacity will double during the years 2017-2026 [1].

Power generation systems are moving from classical central large power station centers (such as nuclear and thermal power stations) to the decentralization systems [2] (small photovoltaic and wind turbine installations located near or on top of buildings, on the roofs of industry companies, shopping centers, etc.). In the decentralized power systems, the roles of each participant are changing dynamically and through cooperation. This development leads towards smart grid systems. It is not a simple task to build these systems because each participant represents a different part of the energy system; at the same time, these systems must work together at full synchronization with each other and other participants in the grid.

The main limitation of photovoltaic systems for the residential applications is that they are working in daylight when most people are away, and the energy consumption is low. In this case, home solar stations generate energy that is not used locally, and after injecting into the distribution grid, this energy is used by another grid participant. On the other hand, this leads to reduced on-site consumption of the energy and increased expenses on the transmission. Another way of building renewable generation systems are hybrid solar systems that have batteries for storing energy. These systems have significant benefit over the former ones: they store energy, which can be used at night and if the weather is unfavorable for generation of sufficient power or provide backup power if the grid is switched off.

For integration of relatively low DC voltage sources, such as a battery, fuel cell or solar panel, often a three-stage conversion is utilized. Such systems consist of three main

parts: DC-AC and AC-DC stages, separated by an isolation transformer, and the DC/AC inverter for interface with the grid. The main feature is the intermediate DC link, which allows more flexible stabilization. On the other hand, this component can reduce the reliability of the system and add to the cost. An alternative approach is to implement a two-stage DC/AC converter, which is also referred to as a cycloconverter or high-frequency link converter (HFLC).

Isolated DC-AC HFLCs could be applied in distributed renewable energy systems [3], [4], [5] and AC grid-connected uninterruptible power supplies [6]. Since HFLCs, in general, allow bidirectional power flow, they can be applied in battery energy storage systems as well [7], [8]. The present study will be focused on the conversion from DC to AC side and comparative analysis of the existing modulation algorithms with modulation on the grid side, that allow soft switching operation without snubbers and auxiliary circuits.

## II. TOPOLOGY DESCRIPTION

There is a number of HFLC topology configurations reported in the literature, such as full bridge [3] half-bridge [4], central tapped [13], voltage clamper [12], etc. The converter selected for the present study is full-bridge type presented in Fig. 1. As shown, the topology consists of two main parts. The voltage source inverter includes four unidirectional switches T1 – T4, that converts the DC voltage from the battery side to the high frequency (HF) AC square pulses. These pulses are stepped up by an HF transformer ( $Tr$ ). The cycloconverter stage forms the output grid voltage by the sine pulse width modulation (SPWM). This stage could be realized with the anti-series connection of two MOSFETs / IGBTs or anti-parallel connection of two GTOs or reverse blocking IGCTs. The snubber capacitors C1...C4 represent switch capacitances or additional capacitor components in parallel.

The major challenge of HFLC bidirectional DC/AC HFLC topology is that the transformer leakage inductance and output filter inductor serve as a current source. It means that the switches in the grid side of the topology operate as a “current breaker” and generate high-voltage spikes during the

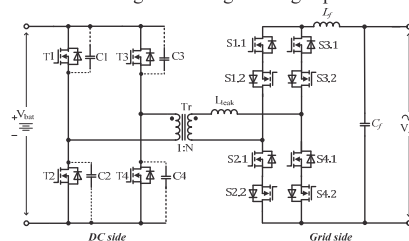


Fig. 1. High-frequency link converter topology (HFLC)



commutations. A natural commutation method for this topology is presented in [9]. Adding a commutation overlap to certain switches allows a natural drop of the leakage current to zero, which creates a condition for soft switched turn-off at the grid side of the topology.

In the current study, four different commutation techniques of full bridge HFCLC that allow voltage clamping and soft switching operation without auxiliary circuits are analyzed.

The first modulation algorithm with no synchronous rectification was introduced. A detailed description of the control system is shown in [3]. In the proposed method (after referred to as method 1), four switches at the grid side operate with the grid frequency, which allows using relatively slow types of semiconductor switches with low on-state losses. The other four switches operate at the switching frequency. At the same time, during the first half-period of the output voltage, only two switches are operating. This converter can be viewed with some analogy to the buck converter. During each HF cycle, the output inductor is energized by the battery for a certain period and is in the freewheeling state during another part of the period. The condition of switching in zero current switching (ZCS) is that the leakage current drops to zero before the switch is turned off. The requirements for the turn-on of the battery side switches in the ZVS condition are that the snubber capacitors of the switches are discharged, and body diodes conduct current before the switch is being turned on. These constraints limit the duty cycle interval for the switches and do not provide soft switching when the output current is near zero. To achieve maximum efficiency of the converter, a combination of various transistors is required, as reported in [3].

The second modulation method (further referred to as method 2) is also presented in [3]. Basically, the modulation technique is the same as the previous one, but with synchronous rectification. As compared to the first method, this technique approaches synchronous rectification from a different angle. In the traditional method, the switches have one bridge leg, and they can block the current in both directions, where as in method 2, it becomes feasible that some switches stay in one state, instead of operating under switching frequency. This method requires switches of the same type because each of them has the working interval at high frequency.

As reported in [3], in modulation methods 1 and 2, to achieve the ZVS condition in the battery side switches, the output switch capacitance and/or snubber capacitance  $C_{sn}$  (capacitors C1...C4) must be discharged to zero and the body diode of the switch must conduct the current before the switch is turned on. The minimal deadtime  $\Delta t_{ms}$  to achieve soft switching is calculated as (1).

$$\Delta t_{bs} = \frac{N \cdot C_{sn} \cdot U_{bs}}{I_L^m} \quad (1)$$

where is  $U_{bs}$  DC input voltage in the battery side of the converter,  $I_L^m$  is the current through the device,  $N$  turns ratio of the isolation transformer.

In the case, when the output current is near zero, the  $C_{sn}$  cannot be discharged, and the soft switching operation is not possible. It means that the method requires a certain amount

of current flowing in the topology to provide ZVS at the battery side. The ZVS condition is satisfied then

$$\frac{L \cdot (I_L^m)^2}{2} > \frac{N \cdot C_{sn} \cdot (U_{bs})^2}{2} \quad (2)$$

To achieve the ZCS condition at the grid side of the converter, the leakage inductance current should drop to zero before the switch is turned off. The minimum interval to obtain ZCS is calculated as

$$\Delta t_{gs} = \frac{2 \cdot C_{sn} \cdot U_{bs}}{I_{leak}^m} + \frac{L_{leak} \cdot I_{leak}^m}{U_{bs}} \quad (3)$$

where  $I_{leak}^m$  is maximum leakage inductance current, and  $L_{leak}$  is the transformer leakage inductance.

The third method was first presented in [9]. This method (further referred to as method 3) is proposed to solve the issues near zero output current by using the quasi-resonant switching state in the topology. By creating a short circuit at the grid side of the transformer during the commutation on the battery side, it is possible to initiate a resonant process between the snubber capacitors and leakage inductance of the transformer. This resonant process can be utilized for recharging snubber capacitors of the battery side of the topology. After this, the process can be blocked by the body diodes on the switches. As a result, a soft switching operation is provided. The time interval of the resonance is calculated as

$$\Delta t_{bs} = \frac{1}{\omega_r} \left( \pi - \arctan \left( \frac{I_r^0 \cdot Z_r}{U_{bs}} \right) \right) \quad (4)$$

where  $I_r^0$  is the total current presented in the resonant circuit.

The resonant frequency  $\omega_r$  and impedance  $Z_r$  of the resonant circuit are calculated as

$$\omega_r = \frac{1}{\sqrt{L_{leak} \cdot C_{sn}}}; Z_r = \sqrt{\frac{L_{leak}}{C_{sn}}} \quad (5)$$

The choice of the resonance parameters allows finding the trade-off between the commutation speed, switching losses, and operating frequency.

The fourth modulation method is described in [11] for the case of the DC-DC converter. The proposed algorithm (further referred to as method 4) uses phase-shift control for the grid side switches. The peculiarity of this method is that it has an additional state when the energy is transferred from the output filter inductor to the battery side. This reverse energy interval should be short to allow soft switching and at the same time avoid excessive high energy circulation. The battery side switches are switched similarly to the previous methods. To satisfy the requirements of soft switching at the battery side of the converter, the following deadtime interval between two switching legs must be provided. To achieve the soft switching in the grid side, it is required to estimate the minimum interval, as derived in (6).

$$\Delta t_{bs} = \Delta t_{rev} + N \cdot \frac{C_{sn} \cdot U_{bs}}{\frac{P_r}{U_{bs}}} \quad (6)$$

where  $P_r$  is the rated power of the converter. The  $\square t_{rev}$  – time of the interval of energy return, it can be calculated as:

$$\square t_{rev} = \frac{2 \cdot (D_0 - D_{bs}^c) - D_{bs} - D_{gs}}{2 \cdot f_{sw}} \quad (7)$$

where  $D_0$  – the minimum phase shift value between the battery and the grid sides,  $D_{bs}^c$  – the maximum duty cycle of the battery side transistors,  $D_{bs}, D_{gs}$  – the actual duty cycles of the battery and grid side transistors, respectively;  $f_{sw}$  – switching frequency.

To achieve the soft switching at the grid side, it is required to provide the minimum overlap interval

$$\square t_{gs} = \frac{1}{N} \cdot \frac{2 \cdot L_{leak} \cdot \left( \frac{P_r}{U_{bs}} + \frac{\square L_f}{2} \right)}{U_{bs}} \quad (8)$$

where  $\square L_f$  is the ripple of the output inductor

To further analyze and assess the differences between the described control techniques, simulation models of each method are presented. The following switching states have been distinguished:

*Shoot-through (STS) interval* — absolute value of the voltage on the grid side of the transformer equals  $U_{max}$ , transformer current is at zero and the output inductor current is decreasing and the energy is transferred to the load.

*Active state (AS)* — the battery side switches T2 and T3 are conducting current, the transformer and the output current is increasing.

*The transition state 1* — voltage on the grid side of the transformer equals 0, the transformer current is increasing, the output inductor discharges energy continuously to the load.

*The transition state 2* — the snubber capacitors of the switches T1 and T4 are recharging with the snubber capacitors of the switches T2, T3. The voltage of the secondary side of the transformer is changing the polarity (Fig. 3a)

The switching sequences of the switches for half of the switching period are listed and described in Table 1. The equivalent circuits of the described intervals are presented in Figs. 2 and 3, where the dotted line defines the current direction. During the next half-period, similar processes are repeated with another switching diagonal. Similar switching intervals of the methods analyzed are grouped together, while the differences are outlined. The Method 4 has additional interval with reverse energy transfer, which is followed by the STS. The duration of transition states 1 and 2 together with the interval of energy return (for Method 4) define the maximum gain of the topology. Thus, the trade-off between the switching losses and gain must be achieved.

### III. SIMULATION RESULTS

This section presents a simulation study of the full bridge soft switching DC-AC HFLC. The simulations were made using PSIM 9.0 software. To estimate the semiconductor losses, the models based on the datasheet parameters of the transistors were used. For each method, the topology used the same filter components.

TABLE I  
SWITCHING STATES IN HFLCS WITH DIFFERENT MODULATION METHODS

State	Method	1	2	3	4
Initial state T1, T2, T3, T4 OFF		S1.2 S2.2, S3.2, S4.2 ON S1.1, S2.1, S3.1, S4.1 OFF	S1.2, S2.2, S3.2, S4.2 ON S1.1, S2.1, S3.1, S4.1 OFF	S1.1, S1.2, S2.1, S2.2, S3.2 ON S3.1, S4.1, S4.2 OFF	S1.1, S1.2, S4.1, S4.2 ON S2.1, S2.2, S3.1, S3.2 OFF
Interval of energy return		N/A			Energy circulating from grid side to the battery side through T2, T3(Fig. 2 f)
STS. T1, T4 ON	S4.2 OFF (Fig. 2 a)	S2.1, S4.1 ON S4.2OFF (Fig.2b)	Resonant interval (Fig. 2 c) after S1.1 OFF (Fig. 2 d)		S1.1, S1.2 ON S3.1 OFF(Fig. 2 g)
			S3.2 OFF (Fig. 2 e)		S3.2 OFF (Fig. 2 h)
Transition state 1	S4.2 ON Active state is initiated. The current redistributed from S2.1 and S2.2 to S4.1 and S4.2				
AS (Fig. 2 i)	(Fig. 2 i)	S2.1 OFF (Fig. 3 a)	S2.1 OFF (Fig. 3 b)		S4.1 ON S2.1 OFF (Fig. 3 d)
			S4.1 ON S2.2 OFF (Fig. 3 c)		
Transition state 2 T1,T4 OFF(Fig. 3 e)		S4.1 OFF	S3.1, S3.2 ON		
Interval of energy return		N/A			Energy circulating from grid side to the battery side
STS T2, T3 ON	S3.2 OFF	S1.1, S3.1 ON, S3.2 OFF	S3.2 OFF		S1.1 ON S3.2 OFF
			S1.2 OFF		S3.1 OFF



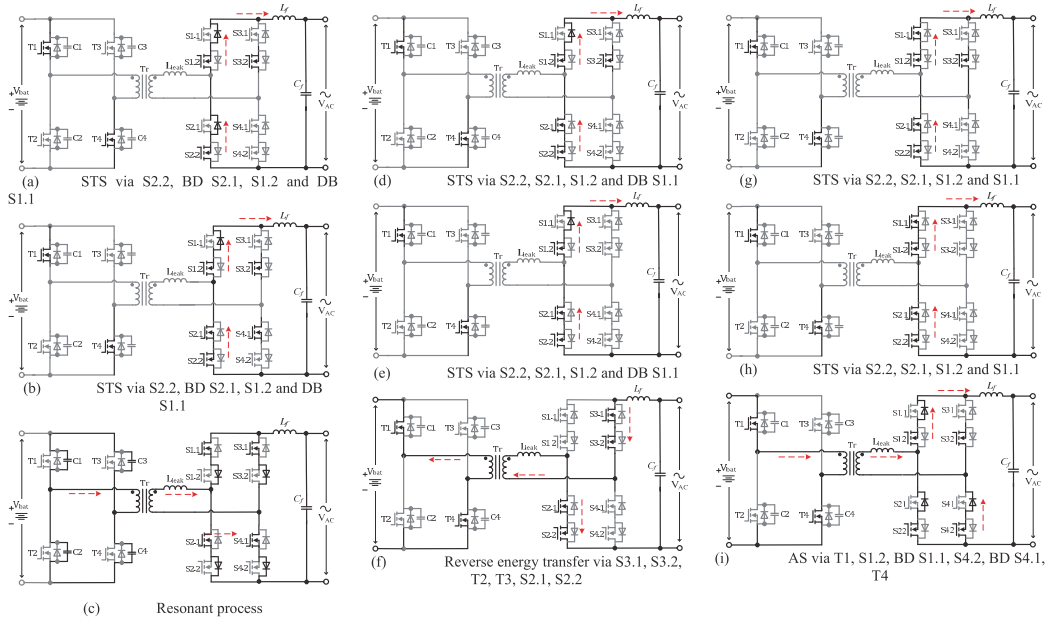


Fig. 2. Equivalent circuits of the HFLC during different operating modes (part 1)

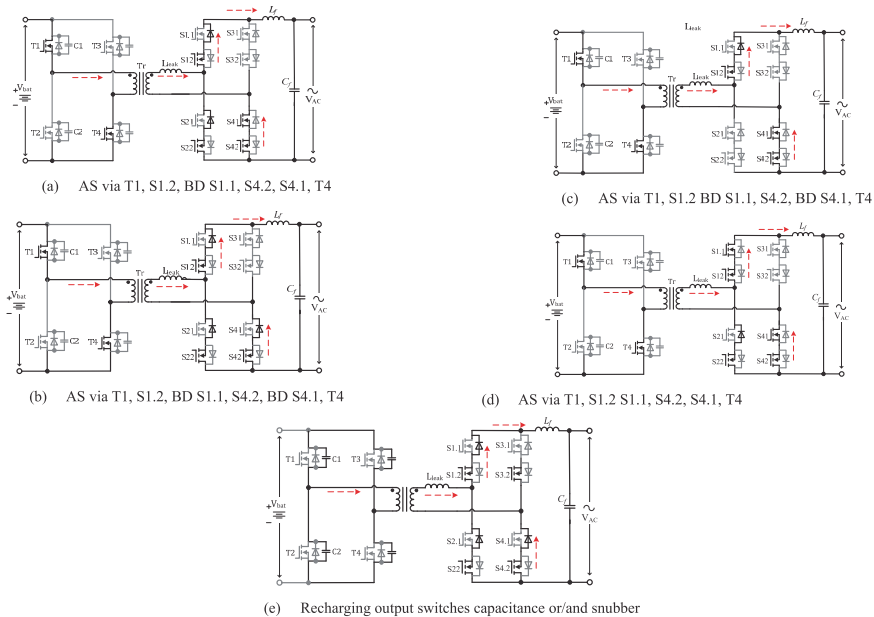


Fig. 3. Equivalent circuit of the HFLC during different operating modes (part 2)

As it was described earlier, the output capacitance of the transistor and/or the snubber capacitance define the maximal duty cycle to achieve soft switching at the battery side. At the grid side, the leakage inductance defines the minimal time interval for the ZCS. To provide the output AC voltage, modulation on the grid side of the HFLC was used. The

following definitions of the modulation coefficient were used: Methods 1 and 2: the relation between the maximum transformer secondary and the output voltages; Methods 3 and 4: the relation between the actual phase shift and the maximum phase shift values.

The modulation index in studied HFCL has some limitations when compared to the standard modulation index of the traditional two-level hard switching inverter supplied from DC link capacitor. The reason is that the converter must provide a stable and standards-compliant network voltage, while the input voltage can vary significantly. In the case of 48 V battery, the working input voltage range can be from 40 up to 58 V (RNS B48025). Moreover, the gain is limited due to transient intervals required for soft switching operation.

The parameters of the simulated converter are presented in Table II. Si MOSFETs (FDMT80080DC), with a blocking voltage of 80 V were selected for the battery side, while SiC MOSFETs (C3M0065090D) with a blocking voltage of 900 V were selected for the grid side. Datasheet parameters of the switches, were utilized in Thermal Module to assess semiconductor conduction losses and approximate the total losses of the converter. The total losses calculated as sum of losses in the switches during one grid period of grid frequency. Table IV presents the results of the simulation and losses for one full load (resistive). The semiconductor losses over wide load range are presented in Fig. 7. In the Method 1, the conduction losses of switches operating at 50 Hz contribute a large part of the losses. If an external diode with low voltage drop is applied, the losses will decrease substantially. Comparative analysis of the characteristics of different modulation methods is presented in Table III.

TABLE II SIMULATION PARAMETERS DC-AC HFCL

Parameter	Symbol	Value
Converter power rating, W	$P_r$	1000
Input voltage, V	$V_{in}$	48
Output voltage, V	$V_{out}$	230
Input current, A	$I_{in}$	20.8
Switching frequency, kHz	$f_{sw}$	100
Transformer turns ratio	N	10
Transformer leakage inductance, uH	$L_{leak}$	28
Output filter inductance, mH	$L_f$	1
Output filter capacitance, uF	$C_f$	0.47

TABLE III CHARACTERISTICS OF THE DC-AC HFCL

	Method 1	Method 2	Method 3	Method 4
RMS output voltage, V	223.1	249.29	222.73	213
Duty cycle battery side	0.47			
Modulation coefficient	0.85			
Gain	0.4798	0.5323	0.4766	0.4582

$$I_n^{tr} = \frac{I_{tr}}{I_{load}}; I_n^{sw} = \frac{I_{sw}}{I_{load}} \quad (9)$$

Fig. 4 show the normalized transformer and switch currents calculated by (9). According to the analysis, the current in Method 4 is the highest, while for other methods the currents are similar. This can be explained by the presence of the additional interval of energy return.

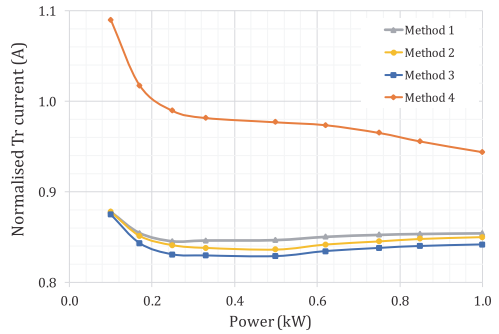


Fig. 4. Normalized current at the grid side of the transformer vs. operating power.

Fig. 6 shows the gain at different power ranges. The gain represents the relation between the amplitude value of the transformer secondary voltage and the maximum output voltage. The gains of Methods 1 and 2 are the largest due to reduced overall transient state durations.

TABLE IV SIMULATION RESULTS

	Method 1	Method 2	Method 3	Method 4
RMS voltage on the load, V	230.31	229.58	230.12	228.36
RMS current on the load, A	4.18	4.17	4.18	4.15
RMS current of the grid side switches, A	23.62	23.5	23.3	26.1
RMS current of the battery side switches, A	2.91	3.3	2.93	2.91
Switching losses of the transistor and diode in battery side switch, W	2.89	2.88	2.05	2.06
Conduction losses of the switch and diode in battery side switch, W	0.44	0.43	0.33	0.28
Sum of losses in the battery side switches, W	13.34	13.27	9.52	9.65
Switching losses in switch and diode in grid side, W	1.76	0.99	0.2	1.12
Conduction losses in switch in grid side, W	0.51	0.71	0.66	0.64
Switching losses in the diode in grid side, W	7.04	0.31	0.21	0.11
Sum of losses in the grid side switches, W	49.67	30.01	8.67	15.09
Total switch losses, W	63.02	43.28	18.20	24.75

#### IV. CONCLUSIONS

Four control algorithms for full bridge HFCL that provide voltage clamping and soft switching without auxiliary circuits were analyzed and compared. The analysis of switching sequences revealed the differences between the methods. The requirements for soft switching conditions were presented together with the limitations of each method. In some cases, the soft switching cannot be provided a near-zero output current, or the performance is deteriorated due to increased energy circulation. The HFCL models with studied algorithms were simulated PSIM software to estimated semiconductor losses and verify the characteristics.

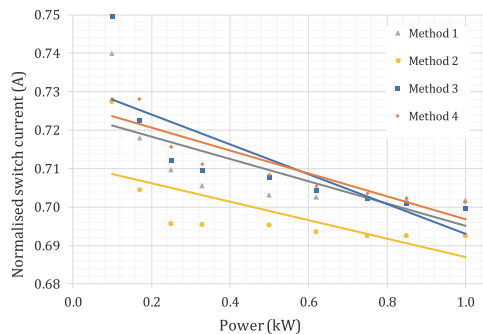


Fig. 5. Normalized grid side switch current vs. operating power.

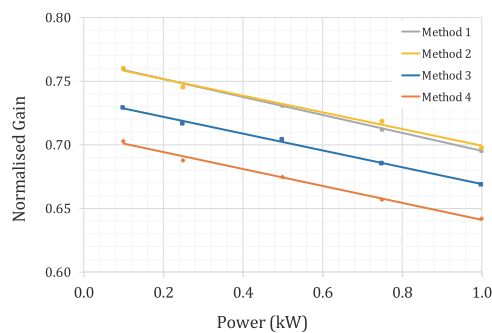


Fig. 6. Normalized gain vs. operating power

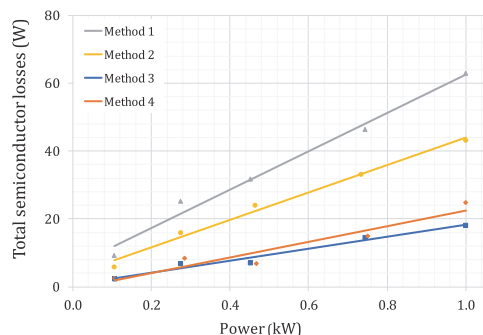


Fig. 7. Total semiconductor losses vs. different operating power

Based on the analysis performed, the following conclusions can be made:

1. Methods 1 and 2 have relatively simple control sequence, but cannot provide soft switching near-zero output voltage and have increased total semiconductor losses (can be reduced by addition of the external Schottky diodes).
2. Method 3 allows soft switching near-zero output voltage but relies on multi-mode control and additional circuitry, which adds to the complexity.

Moreover, the amount of energy circulation is not always optimized.

3. Method 4 provides a more significant degree of freedom when choosing control variables, but exhibits increased energy circulation and require model-based control for optimum performance.

It can be concluded that the highest performance can be achieved by combining the modulation techniques and introducing optimized multi-mode control. Future work will be devoted to the experimental verification of control algorithms and development of optimized modulation methods for this topology.

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**Publication IV**

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# Soft-Switching Modulation Method for Full-Bridge DC-AC HF-Link Inverter

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**Abstract**—This paper presents an improved modulation method for the cycloconverter stage of high frequency-link DC-AC inverters. By applying the quasi-resonant commutation mode during the entire operating period, the fast and reliable discharge of DC-side capacitances can be provided even if the output current is close to zero. This allows to ensure zero voltage switching (ZVS) conditions for the DC-side transistors, while applying small external snubber capacitors to reduce their turn-off losses. The proposed modulation strategy was significantly simplified and requires no external active auxiliary circuits or multi-mode operation. Moreover, two of the AC-side switches can operate at the fundamental frequency, while the rest operate with zero current switching (ZCS). The proposed modulation method is verified with mathematical analysis, simulation model and experimental prototype of full-bridge HF-link inverter.

**Keywords**— Cycloconverter, DC-AC converter, single stage converter, ZCS, ZVS.

## I. INTRODUCTION

Renewable energy and storage applications generally require preliminary voltage stabilisation and matching at the intermediate DC-link before it can be processed by a grid-tie inverter. As an alternative, isolated high frequency link converters (HFLCs) can be used in such applications to provide DC-AC conversion without DC-link. The concept of HF-link DC-AC converters have been presented some time ago [1]-[4] and Fig. 1 presents typical configuration, which uses a voltage source inverter at the DC-side and a cycloconverter with a LCL filter at the AC-side. Recent studies have also adopted Z-source topologies to the DC-side for extended regulation possibilities [5]. The typical advantages of these systems include galvanic isolation, good voltage regulation range, absence of DC-link capacitor and bidirectional operation possibility [6]-[10].

One of the challenges of such systems lies in the requirement for the power switches in the AC stage to have reverse blocking capability. However, since the most widespread devices today are reverse conducting, a (back-to-back) series connection of reverse conducting devices is usually necessary to obtain the required characteristics. This results in the total power semiconductor VA rating and conduction losses to be similar to those of the two-stage systems utilising DC-DC converter with separate grid-tie inverter [11]. In some applications, the conduction losses can be reduced by using reverse-blocking IGBTs [12], however these devices are still not fully

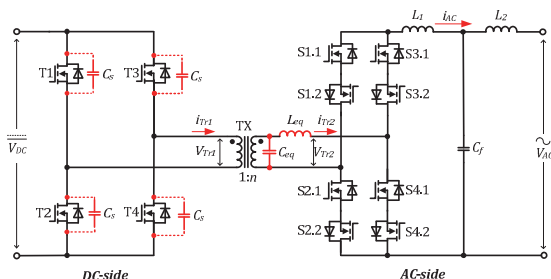


Fig. 1. High-frequency link full bridge inverter.

commercialised. Another issue lies in the transient overvoltages caused by current mismatch between transformer leakage inductance and inductor at the AC stage. The problem could be solved by applying clamping circuits that are used for storing the leakage inductance energy [13]. Special control methods were also proposed and applied to utilise this energy, achieve soft-switching of power semiconductor devices and reduce the switching losses [4],[6]-[15].

The HF-link DC/AC converter technology evolved together with the development of new power semiconductor devices and the most recent studies are focused on application of WBG semiconductors and associated adjustments to the topology design and control [9],[10],[16]-[17]. A new generation of power semiconductor devices, such as SiC MOSFETs and Schottky diodes enable to significantly reduce the losses associated with transistor switching and diode reverse recovery, allowing much higher switching frequencies to be used [18]. The recently proposed secondary-side modulation method [9] for full-SiC MOSFET converter allows two of the AC-side switches to operate at the fundamental frequency, reducing losses associated with transistor switching even further. Similar results were achieved using the primary-side modulation methods proposed in [19] and [20]. In addition, special active snubbers were presented to enhance functionality and reduce the overvoltages associated with the diode reverse recovery process [16],[20].

The limitation of most of these methods lies in the hard-switched turn-off of the DC-side switches. This increases their losses and can create problems at the AC zero-crossing point, when the available load current is not high enough to recharge parasitic capacitances of the DC-side transistors and reach ZVS.

In this case the ZVS conditions have to be provided by the transformer magnetising current. In turn, relatively large magnetising current results in lower efficiency, particularly at partial load. The quasi-resonant commutation, proposed in [7] as a part of the multi-mode modulation strategy, was applied to discharge the equivalent (snubber) capacitance, specifically during low current conditions. It was introduced as an additional mode that was enabled near zero crossing points and used to accumulate certain current during the enhancement stage to recharge the DC-side switch capacitances. At the same time, the energy circulation was not always optimal and rather complex control system was necessary.

In the present paper, the authors aim to improve the method by extending the quasi-resonant commutation mode to the entire operating period. The study focuses on the conventional configuration of the topology, where full-bridge DC-side is interfaced with full-bridge AC-side (consisting of bidirectional switches) by a two-winding high-frequency transformer (Fig. 1). The proposed method is based on phase-shift modulation and omits the enhancement stage used in [7], which allows to simplify the modulation strategy and minimize the energy circulation, while retaining the ZVS and ZCS of semiconductors. Moreover, the proposed method allows to apply external snubber capacitors across the DC-side transistors to reduce their turn-off losses. Finally, 1/4 of the AC-side transistors operate with fundamental frequency, which reduces the losses associated with their switching transients.

## II. PROPOSED MODULATION METHOD

In the following analysis it is assumed that the converter components are lossless, the transformer magnetising inductance is infinitely large and synchronous rectification is not applied. The transformer leakage inductance is represented by equivalent inductance  $L_{eq}$  and the snubber capacitances across DC-side transistors are represented by an equivalent capacitor  $C_{eq}$ :

$$C_{eq} = C_s \cdot n^2. \quad (1)$$

Neglecting the filter inductor current ripple, the instantaneous output current value is defined as

$$i_{L1} \approx i_{AC} = I_m \cdot \sin(\omega \cdot t), \quad (2)$$

where  $I_m$  is the amplitude value of the output sinusoidal current.

When  $i_{AC} > 0$ , the transistors S1.2 and S3.2 are kept in the on-state and the following switching modes can be distinguished (Fig. 2):

**$t_0$ - $t_1$** : T1, T4, S1.2, S3.2 and S4.2 are in the on-state and the other ones are turned off. The converter is in the active state and power is transferred to the output through switches T1, T4, S1.2, S4.2 and the body diodes of transistors S4.1 and S1.1, which can be turned on to reduce on-state losses.

**$t_1$ - $t_2$** : T1 and T4 are turned off and S3.1 is turned on. The active state is finished and the transition interval starts. A resonant process between  $C_{eq}$  and  $L_{eq}$  takes place. The circulating current through S3.1, S3.2, S1.2 and the diode of S1.1 is added to the load current, reducing the recharge time of  $C_{eq}$ . The transformer voltage  $V_{Tr1}$  starts reducing.

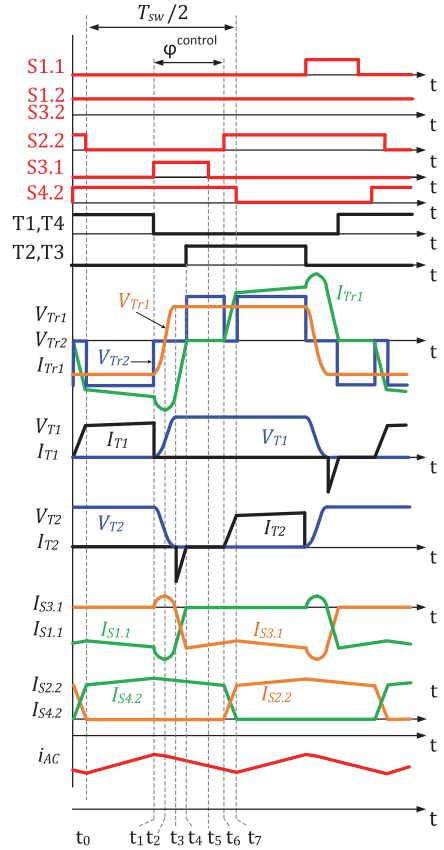


Fig. 2. Generalised operation principle for one switching period.

**$t_2$** : The transformer voltage  $V_{Tr1}$  is zero, while the resonant current reaches the peak value. The value of this current depends on  $C_{eq}$  and  $L_{eq}$  values as well as the load current and can be estimated from

$$i_{Peak} \approx \sqrt{i_{AC}^2 + \left(\frac{V_{DC}}{n \cdot Z_r}\right)^2}, \quad (3)$$

where  $Z_r = \sqrt{L_{eq} / C_{eq}}$  is the equivalent impedance.

**$t_2$ - $t_3$** : The resonant process continues, while the resonant current starts to decrease. At  $t_3$  the transformer DC side voltage  $V_{Tr1}$  reaches the amplitude value and the current decreases back to  $i_{AC}$ . The total duration of the resonant interval  $t_1$ - $t_3$  is estimated as

$$t_{1-3} = t_{res} = \frac{\frac{\pi}{2} - \arctg\left(\frac{n \cdot i_{AC} \cdot Z_r}{V_{DC}}\right)}{\pi \cdot f_r}, \quad (4)$$

where  $f_r = 1 / (2 \cdot \pi \cdot \sqrt{L_{eq} \cdot C_{eq}})$ .



Thus, the duration depends on the operating point and reaches its maximum value when  $i_{AC}$  is close to zero.

**$t_3$ - $t_4$ :** The snubber capacitors of transistors T2 and T3 are discharged. Their body diodes become forward biased, taking full load current, which immediately starts to decay, redistributing from bidirectional switch S1 to S3 with  $di/dt$  limited by  $L_{eq}$ . Starting from this interval T2 and T3 can be turned on with ZVS. The duration of this interval can be estimated as

$$t_{3-4} < \frac{n \cdot I_m \cdot L_{eq}}{V_{DC}}. \quad (5)$$

**$t_4$ - $t_5$ :** The current redistribution is finished, T2 and T3 diode current reduces to zero. The converter enters the freewheeling state, and the current freewheels through bidirectional switches S3, S4 and the load. The duration of this interval can be controlled by the phase shift between the DC- and AC-side switching pairs.

**$t_5$ - $t_6$ :** S2.2 is turned on, starting the transient process. The current is redistributed from bidirectional switch S4 to S2 with  $di/dt$  limited by  $L_{eq}$ . The current through T2, T3 and the transformer rises from zero to the nominal value at the same rate. The duration of this interval can be estimated by (5).

**$t_6$ - $t_7$ :** The transition process is finished, S4.1 and S4.2 can be turned off with ZCS. The converter is in the active state again and the analogous processes are repeated for the other switching half-period.

The modulation principle is the same when  $i_{AC} < 0$ ; in this case the transistors S.2.1 and S4.1 are kept in the on-state and the transistors providing the switching sequence are changed correspondingly.

### III. SIMULATION STUDY

#### A. Design Constrains

The proposed modulation method allows for recharging the equivalent capacitance at the DC-side even at no-current conditions, therefore, unlike in recently presented converters [9],[10],[16],[19],[20], external snubber capacitors can be easily applied to reduce turn-off losses of the DC-side transistors. At the same time, according to (4), a certain trade-off is required when choosing the snubber capacitance, since it leads to duty cycle loss and increased conduction losses.

As discussed in the previous section, the capacitances of DC-side transistors T1-T4 are recharged during the quasi-resonant interval, which duration depends on the circuit parameters and operating point. During this interval all DC-side transistors should be turned off to maintain ZVS conditions. In the general case, the duty cycle of DC-side switches should be selected assuming the worst-case condition for  $i_{AC}=0$ , when the resonant interval duration is maximal:

$$D_{DC} < \frac{1}{2} \cdot \left( 1 - \frac{f_{sw}}{f_r} \right). \quad (6)$$

The duty cycle of the AC-side switches should be longer than one-half of the switching period and chosen taking into account the necessary current redistribution intervals to avoid open-circuit condition of  $L_f$ :

Table I  
SPECIFICATIONS OF CASE STUDY CONVERTER

Parameter	Symbol	Value
DC-side voltage	$V_{DC}$	400 VDC
AC-side voltage	$V_{AC}$	230 VAC
Switching frequency	$f_{sw}$	50 kHz
Transformer turns ratio	$n$	1:1.1
Rated power	$P_{rated}$	1200 W
Snubber capacitor	$C_s$	1-3.3 nF
Leakage inductance	$L_{eq}$	5.1 $\mu$ H
Magnetising inductance	$L_m$	10 mH
Parasitic capacitance of AC switches	$C_p$	60 pF
Filter inductors	$L_1; L_2$	1 mH; 0.4 mH
Filter capacitor	$C_f$	0.47 $\mu$ F

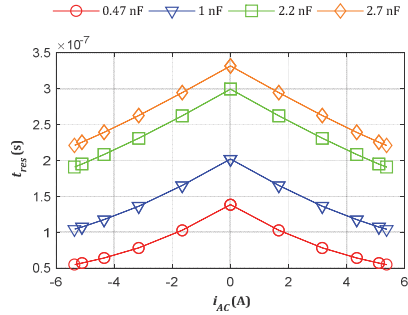


Fig. 3. Duration of the resonant interval  $t_{res}$  vs.  $C_s$  for different  $i_{AC}$  values ( $L_{eq}=5 \mu$ H).

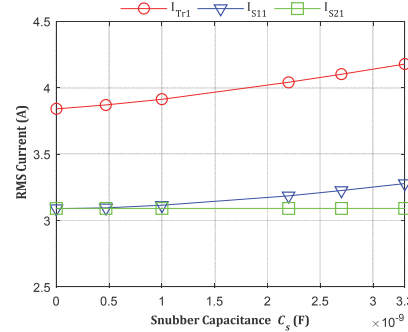


Fig. 4. RMS currents in the topology vs.  $C_s$  at rated power of 1000 W during positive AC half-period ( $L_{eq}=5 \mu$ H).

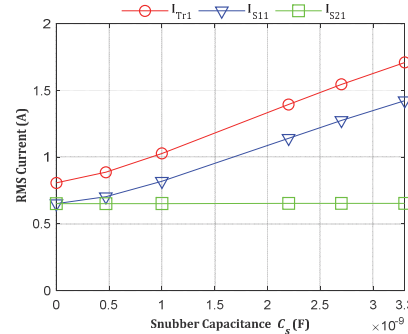


Fig. 5. RMS currents in the topology vs.  $C_s$  at 200 W during positive AC half-period ( $L_{eq}=5 \mu$ H).



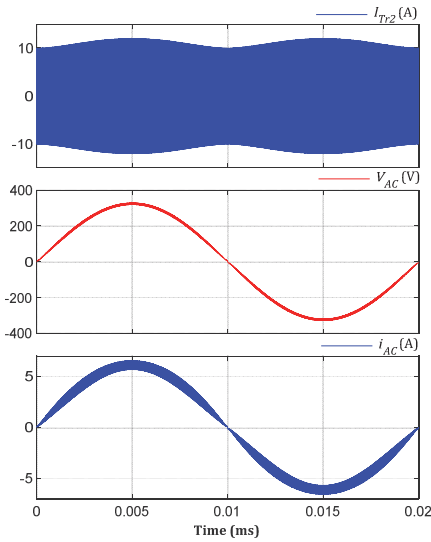


Fig. 6. Simulation waveforms for one output period: transformer current  $I_{Tr1}$ , output AC voltage  $V_{AC}$  and output current  $i_{AC}$  ( $P=1$  kW).

$$D_{AC} < \frac{1}{2} + \frac{2 \cdot n \cdot I_m \cdot I_{eq}}{V_{DC}}. \quad (7)$$

The resulting duty cycle loss of the HFLC depends on the duration of the intervals required for ZVS/ZCS and the switching frequency. Assuming practical design parameters, it should take around 10% of the switching period. Unlike in conventional voltage source inverters, the loss in the output voltage amplitude can be easily compensated by slight adjustment of the transformer turns ratio.

In general, for the optimal design of HFLC with proposed modulation method, the  $L_{eq}$  value should be minimised to reduce duty cycle loss and the energy of oscillations after turn-off of the AC-side switches. A value in range of 5...10  $\mu\text{H}$  is

assumed to be relatively easily achievable using conventional design with interleaved windings. The duration of the resonant interval estimated for different snubber capacitors is shown in Fig. 3, assuming the HFLC parameters listed in Table I. As observed, the duration of this interval varies with output current and is at maximum when  $i_{AC}$  is at zero. Nevertheless, the resonance duration and its variation with current are not very large, which proves that the proposed method can provide ZVS for T1-T4 with a relatively small duty cycle loss.

The currents in the topology for various values of  $C_s$  at rated power are depicted in Fig. 4. As observed, due to increased energy circulation, the rms currents in the transformer and top-side bidirectional switches increase by up to 10% for  $C_s=3.3$  nF when compared to the case with no capacitor. The effect is much more pronounced at partial power operation: the rms current can increase by a factor of 2.2 at 200 W (Fig. 5), assuming that other parameters are kept unchanged. Therefore, the optimal value of  $C_s$  will depend on the parameters of the

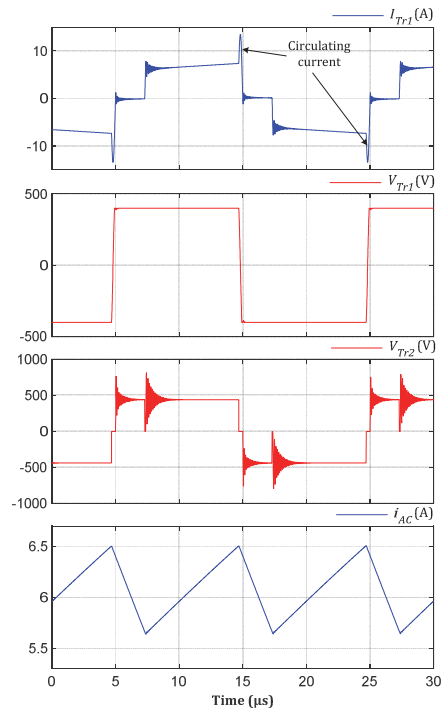


Fig. 7. Simulation waveforms for one switching period transformer current  $I_{Tr1}$  and voltages  $V_{Tr1}$ ,  $V_{Tr2}$  and output current  $i_{AC}$  ( $P=1$  kW,  $C_s=3.3$  nF).

practical circuit: semiconductor type and technology, transformer characteristics, physical layout, operating power, etc.

### B. Simulation Study

The simulation model of the topology in Fig. 1 was created in the PSIM software to verify the proposed modulation method. The parameters of the model are chosen according to the specifications in Table I, with  $C_s=3.3$  nF. The model assumes lossless components and includes the leakage inductance of the transformer along with the parasitic capacitances of the MOSFETs in the AC side, that are responsible for parasitic oscillations after the diode turn-off.

The transformer secondary winding current  $I_{Tr2}$ , output voltage  $V_{AC}$  and output current  $i_{AC}$  are presented in Fig. 6 respectively, from top to bottom. The zoomed in waveforms in Fig. 7 show that the transformer current peak during the resonant interval takes only a fraction of the switching period, without significantly affecting the rms current value. The switching waveforms depicted in Fig. 8a and Fig. 8b demonstrate, that with the proposed method it is possible to completely discharge the snubber capacitance of T1 during relatively short time, independently of the amount of current present in the circuit, which confirms the estimations from the previous section. Finally, the ZCS turn-off of the cycloconverter transistor S2.2 is presented in Fig. 8c, validating the effectiveness of the proposed modulation method.

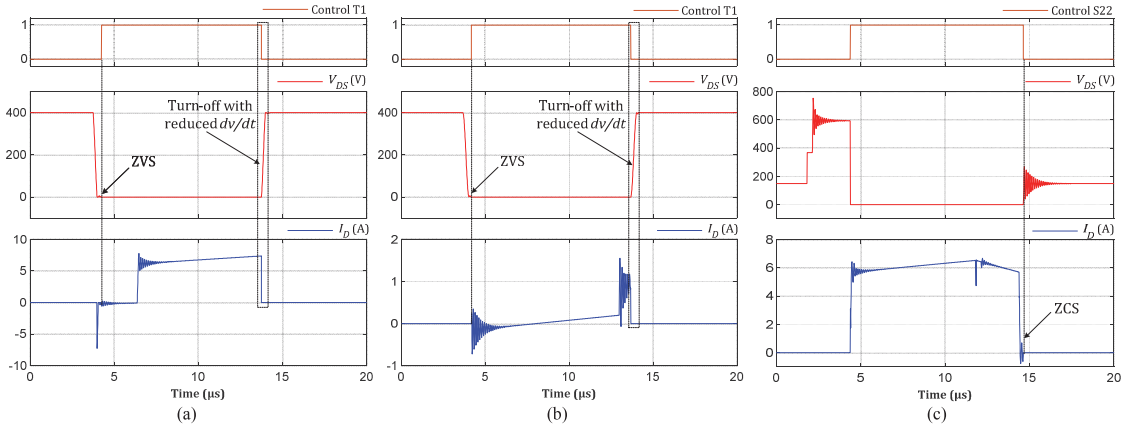


Fig. 8. ZVS turn-on of T1 at  $i_{AC}$  close to  $I_m$ . (a) and  $i_{AC}$  close to zero (b); ZCS turn-off of S2.2 at  $i_{AC}=I_m$ . (c).

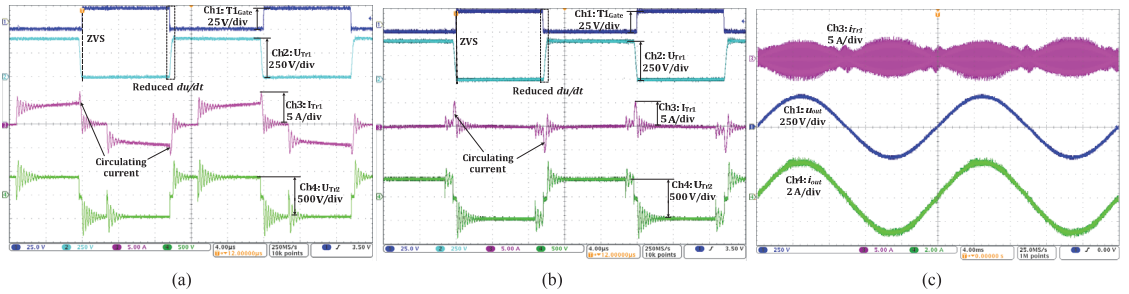


Fig. 9. Experimental waveforms: ZVS of T1 at the output current close to amplitude value (a) and close to the zero-crossing point (b); transformer current  $I_{T1}$ , output AC voltage  $V_{AC}$  and output current  $i_{AC}$ . (c). ( $P_{out}=500$  W,  $C_s=3.3$  nF).

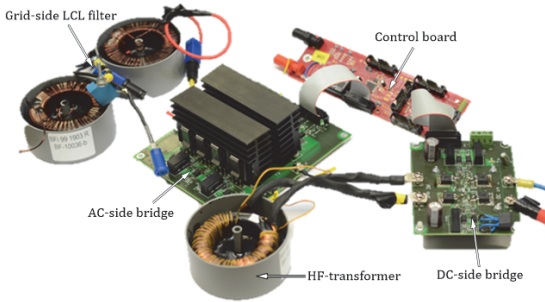


Fig. 10. Photo of the experimental HF-link inverter.

#### IV. EXPERIMENTAL VERIFICATION

For practical verification of the proposed method, a converter prototype (Fig. 10) according to the specifications from Table I was tested. The experimental waveforms are shown in Fig. 9. For the verification of modulation principle, the converter was operating with resistive load and open-loop control. By comparing Fig. 7 with Fig. 9, it can be observed that the experimental results are in general agreement with the estimations. The resonant interval that follows the active state

recharges the capacitances and creates ZVS conditions at the DC-side transistors. This is verified near the amplitude value of  $i_{AC}$  in Fig. 9a and close to the zero-crossing point in Fig. 9b. The low-distortion sinusoidal output voltage of the converter with proposed modulation method is demonstrated in Fig. 9c.

It should be noticed, that the selected values of  $C_s$  were relatively large and not optimised in terms of power losses and overall efficiency for the particular prototype. The main goal of the experiments lied in the verification of the capability of the proposed method to ensure ZVS conditions across DC-side transistors. Previous studies show turn-off loss reduction from  $5 \mu\text{J}$  to  $1.5 \mu\text{J}$  using 1 nF snubber capacitor across Si MOSFET [21]. Similar relative reduction of turn-off losses was demonstrated for SiC devices [22].

#### V. CONCLUSIONS

This paper presents an improved secondary-side modulation method for HF-link DC-AC inverter that features quasi-resonant interval to provide ZVS of the DC-side transistors. Unlike in most of the existing solutions, external snubber capacitors may be easily applied to the DC stage to provide reduction of the turn-off switching losses, without the loss of

ZVS at zero output current and allowing the transformer design with low magnetising current. The proposed method does not require external active clamping circuits or result in significant increase of the duty cycle loss. Similar to the other recent methods, 1/4 of the AC-side transistors are always kept in the on-state, reducing the cycloconverter switching losses. With the additional possibility to choose the value of external snubber capacitors, increased design flexibility of the system is provided. The theoretical findings were verified with a 400 VDC/230 VAC software and hardware models of the DC-AC HF-link inverter and confirmed the effectiveness of the proposed method.

#### ACKNOWLEDGMENT

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**Publication V**

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# Improved Modulation Method for Full-Bridge AC-DC HF-Link Converter

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**Abstract**—This paper presents a new modulation method for the cycloconverter stage of the high frequency (HF) link AC-DC rectifier. The method takes advantage of the parasitic parameters of the circuit to provide zero current switching (ZCS) for the AC and zero voltage switching (ZVS) of the DC-side transistors. Regulation with the power factor correction (PFC) is ensured using only one control variable and no external auxiliary or snubber circuits are required. Moreover,  $\frac{1}{4}$  of the AC-side transistors are operating with fundamental frequency. The proposed modulation strategy and its design constraints are analysed mathematically and verified with the simulation model of 1 kW, 230 VAC/48 VDC HF-link converter.

**Keywords**— Cycloconverter, AC-DC rectifier, single stage converter, ZCS, ZVS.

## I. INTRODUCTION

Increased use of renewable energy sources, electric vehicles and autonomous electronics has instigated growth in the production capacity of battery systems and reductions in their price [1],[2]. For relatively low power systems, batteries with the nominal voltage up to 48 V are typically used [3],[4]. The converters for battery interface with residential AC grid voltage levels generally utilise multi-stage conversion, where isolated DC-DC stage follows the grid-connected rectifier [5],[6]. An alternative approach is to use an isolated high-frequency link converter (HFLC), without an intermediate DC-link or separate bridge rectifier [7]. The typical full-bridge configuration of HFLC is presented in Fig. 1. It features power factor correction (PFC), bidirectional operation capability and galvanic isolation. The presence of the transformer allows the converter to be designed for batteries with various nominal voltage levels by the proper turns ratio selection. In most of the cases, the converters are realised using two anti-series connected transistors at the AC-side to form the bidirectional switch. At the same time, RB-IGBTs can potentially provide reduced power dissipation for higher power systems 0-[10].

The relatively high number of semiconductor switches allows users to implement various modulation strategies that provide soft switching of semiconductors and reduce the transient voltage overshoots due to current mismatch between the filter and the leakage inductances [11],[12]. Despite being bidirectional, most of the strategies are generally focused only on the inverter mode of the HFLC operation. Some of the recently introduced modulation methods allow part of the AC-side switches to operate at the fundamental frequency [13],[14]. Moreover, special active auxiliary snubber

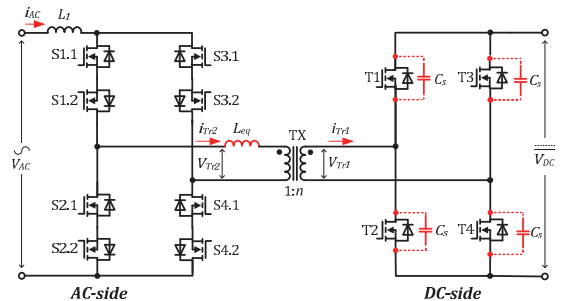


Fig. 1. High-frequency link AC-DC full-bridge converter topology.

circuits were introduced to provide enhanced functionality [15]-[17].

Since the topology is not symmetrical, most of the methods are not directly applicable for the AC-DC conversion. Several studies have addressed this mode of operation [13],[15],[16],[18]. In [13] the rectifier mode assumes hard switching conditions for the semiconductors. The quasi-resonant modulation method [12] provides zero-voltage switching (ZVS) for the DC-side switches near the zero current crossing only for the inverter mode. The methods proposed in [15] and [16] use an additional auxiliary converter and the power reversal occurs only for a brief time near the zero crossing when operating with reactive load. The natural clamping soft switching method for the rectifier operation mode proposed in [18] solves the problem of voltage overshoot and provides soft switching conditions for semiconductors without relying on the auxiliary circuits. However, the modulation is quite complex, with strict dead-time requirements and the DC-side transistors operating at double switching frequency.

It follows that there is a lack of research focused on the HFLC modulation algorithms in the rectifier operating mode. Present paper proposes a new modulation method for continuous AC-DC operation of HFLC without auxiliary circuits, which reduces the voltage overshoot, provides soft switching conditions for semiconductors and requires only one control variable. Moreover, two transistors at the AC-side operate with the fundamental frequency, while another two devices can operate in the synchronous rectification mode. In contrast to other similar methods, neither of the devices exhibit increased operating frequency.



## II. PROPOSED MODULATION PRINCIPLE

The analysis assumes that the converter components are lossless and the influence of the transformer magnetising inductance is negligible. The transformer leakage inductance is represented by an equivalent inductance  $L_{eq}$  connected in series with the grid-side winding and capacitive snubbers  $C_s$  are applied in parallel to the DC-side switches to reduce  $dv/dt$  during turn-off of the devices. The modulation algorithm is described for the condition when  $v_{AC} > 0$  and  $i_{AC} > 0$  and the power flow from the AC- to the DC-side. The transistors S1.2 and S3.2 are kept turned on during the entire fundamental half-period and for simplicity of the analysis, the synchronous rectification at the cycloconverter stage is not applied. The gating signals can be generated using two sawtooth carriers, as shown in Fig. 2. The following operating are as follows (Fig. 3):

**$t_0$ - $t_1$ :** Transistors S1.1, S1.2 and S4.1 are in the on-state, while the other ones are turned off. The converter is in the active state and the power is transferred to the DC side through S1 and the body diodes of S4.2, T1 and T4, which can be turned with ZVS.

**$t_1$ - $t_2$ :** S2.1 turns on and the transition interval starts. While the current of S2.1 and S2.2 rises, the currents of S4.1, S4.2, body diodes of T1, T4 and the transformer decrease linearly with  $di/dt$  limited by  $L_{eq}$ . The input inductor voltage polarity is reversed and its current starts to rise, while the  $V_{Tr2}$  is at zero.

**$t_2$ - $t_3$ :** The current of S2.1 and S2.2 reaches the input inductor current level, the  $V_{Tr2}$  returns to the amplitude value and the transition interval is finished. S1.1, S1.2, S2.1 and S2.2 are conducting and the input inductor  $L_l$  is energised. S4.1 can be turned off with ZCS.

**$t_3$ - $t_4$ :** S3.1 turns on, starting the next transition interval. The currents of S3.1, S3.2, T1, T4 and the transformer start to rise linearly with  $di/dt$  limited by  $L_{eq}$ , while the currents of S1.1 and S1.2 decrease with the same slope. This mode is similar to the interval  $t_1$ - $t_2$ .

**$t_4$ - $t_5$ :** The current in the circuit continues to rise above the value of  $i_{AC}$  with the same slope. The current of S1.1 and S1.2 changes direction and S1.1 can be turned off with ZCS, along with T1 and T4. The snubber capacitors  $C_s$  recharge and the  $V_{Tr1}$  changes polarity.

**$t_5$ - $t_6$ :** Snubber capacitors are recharged, the  $V_{Tr2}$  reaches the amplitude value and the body diodes of T2 and T3 become forward biased. The S1.1 current returns back to zero with the same  $di/dt$ . The current through S3.1, S3.2 and the  $I_{Tr2}$  becomes equal to the input current, while currents of T2 and T3 reduce to  $n \cdot I_{Tr2}$ . From  $t_6$ , the converter operates in the active state. Similar processes are then repeated for another switching half-period.

The operation principle is the same when  $v_{AC} < 0$  and  $i_{AC} < 0$ ; in this case, the transistors S2.1 and S4.1 are kept turned on and the gating signals of transistors responsible for the modulation sequence are changed correspondingly.

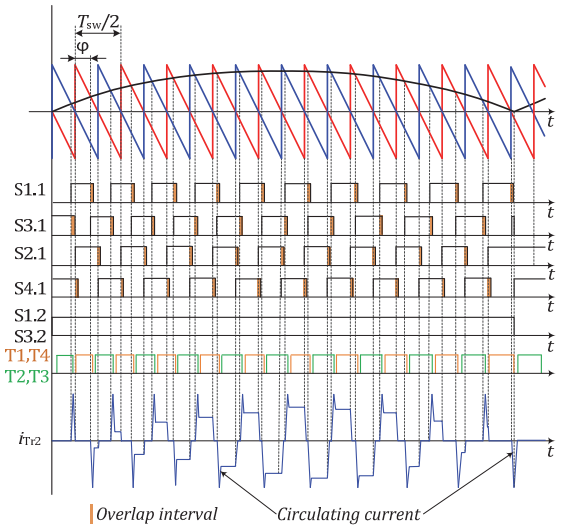


Fig. 2. Generalised modulation principle for one fundamental period.

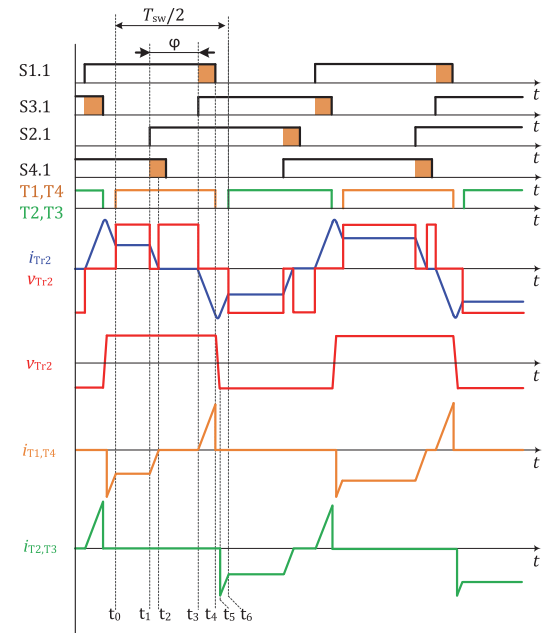


Fig. 3. Generalised operation principle for one switching period.

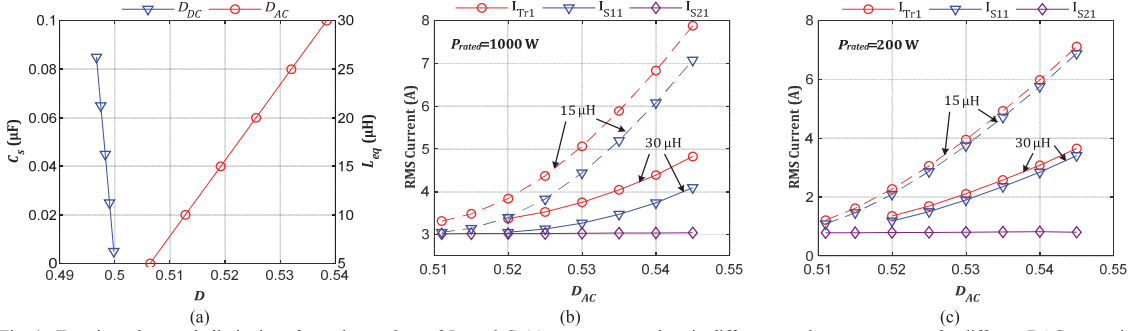


Fig. 4. Transistor duty cycle limitations for various values of  $L_{eq}$  and  $C_s$ ; (a); rms current values in different topology components for different DAC: operation at 1000 W (b) and at 200 W (c).

### III. THEORETICAL STUDY

#### A. Design Constraints

The zero-current switching (ZCS) condition of the outer AC-side transistors is achieved if the peak current in the circuit during  $t_4$ - $t_5$  rises above the absolute value of the input current  $i_{AC}$ . The amplitude of the peak current is controlled by the duty cycle of transistors S1.1 and S3.1 (for  $v_{AC} > 0$  and  $i_{AC} > 0$ ). In the general case, the minimal duty cycle value for all the AC-side devices operating at the switching frequency can be estimated for the case  $i_{AC} = I_m$ :

$$D_{AC} > \frac{1}{2} + \frac{2 \cdot n \cdot I_m \cdot L_{eq} \cdot f_{sw}}{V_{DC}}. \quad (1)$$

It can be noticed that transformer leakage inductance strongly affects the converter operation. To define the peak current  $I_p$  with a relatively low value of leakage inductance, a rather precise timing and control is required to avoid excessive energy circulation.

The value of  $C_s$  affects the maximal duty cycle duration of the DC-side devices. Moreover, relatively large  $C_s$  value can have a noticeable impact on the amplitude of the  $I_p$ . The allowed duration of the DC-side bridge transistors to maintain zero voltage switching (ZVS) is:

$$D_{DC} < \frac{1}{2} - \frac{n \cdot V_{DC} \cdot C_s \cdot f_{sw}}{I_p}. \quad (2)$$

In the practical circuits, the natural turn-off of the AC-side transistors is followed by the parasitic resonance process between the transformer leakage inductance and the output capacitances of semiconductor devices. The amplitude of these oscillations is generally less than twice the steady-state  $V_{Tr2}$  voltage value and the energy is relatively low [17]. On the other hand, they tend to be more pronounced in applications that interface a relatively low DC voltage source, since in this case, the transformer turns ratio is large and it is much harder to avoid high leakage inductance.

#### B. Simulation Analysis

The model of the topology depicted in Fig. 1 was created in the PSIM software to verify the new modulation method. The parameters of the model are listed in Table I. It assumes

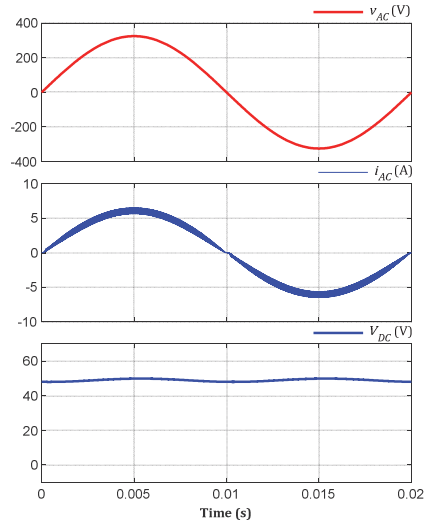


Fig. 5. Simulation waveforms for one output period: grid voltage, AC input current, DC output voltage ( $P=1$  kW).

Table I  
SPECIFICATIONS OF THE CASE STUDY CONVERTER

Parameter	Symbol	Value
AC-side voltage	$V_{AC}$	230 VAC
DC-side voltage	$V_{DC}$	48 VDC
Switching frequency	$f_{sw}$	50 kHz
Transformer turns ratio	$n$	10:1
Rated power	$P_{rated}$	1200 W
Snubber capacitor	$C_s$	100 nF
Leakage inductance	$L_{eq}$	30 $\mu$ H
Magnetising inductance	$L_m$	10 mH
Parasitic capacitance of AC switches	$C_p$	40 pF
Filter inductors	$L_l$	1.3 mH

lossless components and includes the leakage inductance of the transformer along with the parasitic capacitances of the MOSFETs in the AC-side that are responsible for parasitic oscillations after the body diode turn-off.

From Fig. 3 it follows that the recharge of the DC-side snubber capacitor occurs at the peak current  $I_p$ , which is higher than the input current; therefore, the recharge time is



constant and relatively short. As a result, ZVS can be easily achieved over the entire operating range and snubber capacitors can be optimised for the loss reduction of the DC-side transistor turn-off.

The duty cycle limits estimated from (1) and (2) for the case study system are presented in Fig. 4a. Larger values of  $L_{eq}$  and  $C_s$  increase the minimal duration of the  $L_l$  energy accumulation interval, which would result in increased voltage stress at the AC-side and transformer turns ratio requirements. Therefore, the parameters of the transformer, particularly its leakage inductance, have to be optimised carefully.

As was mentioned, the ZCS of outer AC-side transistors requires precise control of  $D_{AC}$  value to minimise rms currents in the converter circuit. Fig. 4b presents the values of rms currents in the converter for various  $D_{AC}$  values. As shown, the rms current increase is not very significant if  $D_{AC}$  is close to the minimal required value. As the chosen  $D_{AC}$  value and associated peak current increase, the amount of energy circulation becomes less optimal, which would result in increased power dissipation and compromised performance. The increased influence of duty cycle variation on the rms current increase in the case of lower  $L_{eq}$  value can also be observed. The effect is more pronounced when the converter operates with partial power: higher  $D_{AC}$  values can make some of the rms currents weakly sensitive to load variations (Fig. 4c). It can be concluded that on-the-fly variation of  $D_{AC}$  is necessary to achieve the lowest energy circulation.

The input voltage  $v_{AC}$ , input current  $i_{AC}$  and output voltage  $V_{DC}$  presented in Fig. 5 demonstrate that the HFLC with the proposed modulation method is capable of operating with high power factor and delivering stable DC voltage to the load. The zoomed in waveforms in Fig. 6 taken at  $i_{AC}=I_m$  show that the energy circulation interval takes only a fraction of the switching period. The oscillations mentioned in the previous section can be clearly observed of the  $V_{Tr2}$  voltage waveforms. In practical applications, 1.2 kV devices, such as SiC MOSFETs, which have the avalanche voltage of around 1.7 kV [19], can be safely applied. The switching waveforms depicted in Fig. 7a for the positive half-period, when  $v_{AC}>0$  and  $i_{AC}>0$ , show that at the top transistors (S1.1 is used as an example) turn-off with ZCS, the current is flowing through the diode. The turn-on loss is also reduced since the current rise is

limited by  $L_{eq}$ . As a result, the transistor switching losses should be minor. The body diode reverse recovery losses will be also reduced due to relatively low  $di/dt$  value. The current of the bottom devices does not have the circulating part and their turn-off is natural (Fig. 7b). The DC-side devices transfer most of the power through the anti-parallel diode or in the synchronous rectification mode; therefore, they turn on with ZVS (Fig. 7c). At the end of the conducting interval, the current is reversed for a short time to provide ZCS for the corresponding AC-side devices. Thanks to the presence of snubber capacitors across the devices, the  $dv/dt$  value during turn-off is lower and the energy losses are reduced [20].

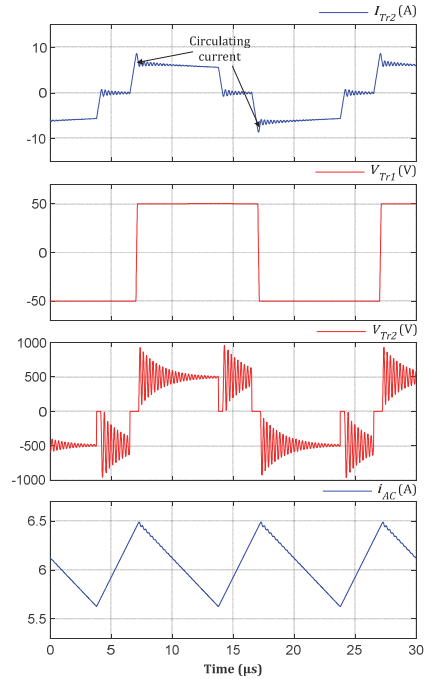


Fig. 6. Simulation waveforms for one output period: transformer current  $I_{Tr2}$ , output AC voltage  $V_{AC}$  and output current  $i_{AC}$  ( $P=1$  kW).

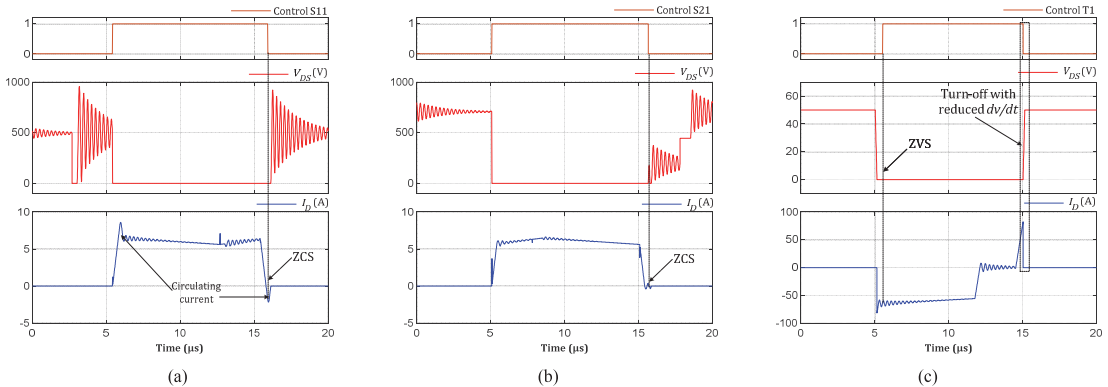


Fig. 7. ZCS turn-off of S1.1 (a) and S2.1 (b) when  $i_{AC}$  close to  $I_m$ ; ZVS turn-on of T1 at  $i_{AC}=I_m$  (c).

On the basis of the simulation waveforms, taking into account realistic parameters of the practical circuit, it can be concluded that the proposed modulation method is effective and has the potential to overcome some of the shortcomings and limitations of the existing methods.

#### IV. CONCLUSIONS

This paper introduced an improved modulation method for the HF-link AC-DC inverter that provides soft switching conditions for all semiconductor devices throughout the entire converter operating range. In contrast to existing solutions, it does not rely on the additional auxiliary circuits or require transistors operate with double switching frequency. Similar to the other recent modulation methods, 1/4 of the AC-side transistors are kept in the on-state during the fundamental half-period, reducing the cycloconverter stage switching losses. The theoretical analysis described the peculiarities and existing design constraints. Proposed ideas were verified with a 230 VAC/48 VDC software model of the DC-AC HF-link inverter and confirmed the advantages and feasibility of the proposed method.

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**Publication VI**

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# Characterisation of 1200 V Reverse-Blocking IGBTs for Naturally Commutated HF-Link Inverter

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**Abstract**— This paper presents an experimental evaluation of 1200V Reverse-Blocking (RB) IGBTs with different manufacturing techniques aiming to reduce the losses associated with reverse recovery. Obtained results were used to estimate the power dissipation of 230 VAC/3.3 kVA high-frequency link cycloconverter stage featuring soft-switching conditions and natural commutation of semiconductors. The performance of RB-IGBT samples with various techniques were compared with the traditional IGBTs connected in common-emitter configuration to form a bidirectional switch. The estimations show, that the samples with local lifetime control have advantage in terms of overall power dissipation and can provide better performance up to switching frequencies of 15 kHz, when compared to standard IGBTs.

**Keywords**— *Insulated gate bipolar transistors, soft switching, DC-AC power converters, switching loss, semiconductor device manufacture*

## I. INTRODUCTION

One of the main development trends of power electronic converters is achieving higher efficiency. A significant part of energy loss in high-power systems occurs in the semiconductor switches and its amount depends on the selected switch type [1][2]. MOSFETs and IGBTs are commonly used for modern medium and high-power systems due to moderate losses at high frequencies and voltages [3][4].

The major part of the total power losses in high-power transistors is related to switching and conduction losses. The amount of dissipated energy due to switching process depend on manufacturing technology, operating frequency and switching conditions. Conduction losses depend on the amount of current flowing through the switch, forward voltage drop or channel resistance [5]. T-type, matrix and high-frequency link converters (HFLC) are using bidirectional switches, which commonly consist of two anti-series-connected MOSFETs or IGBTs [2],[6]-[8]. The conduction loss of this configuration is a sum of losses for both transistors. In order to decrease conduction losses, parallel connected reverse-blocking IGBT (RB-IGBT) could be utilised [8]-[10]. Due to series connection, the bidirectional switch formed with these devices will have superior on-state characteristics. On the other hand, the

switching characteristics, particularly high reverse-recovery-induced losses inhibit wide application of such technology.

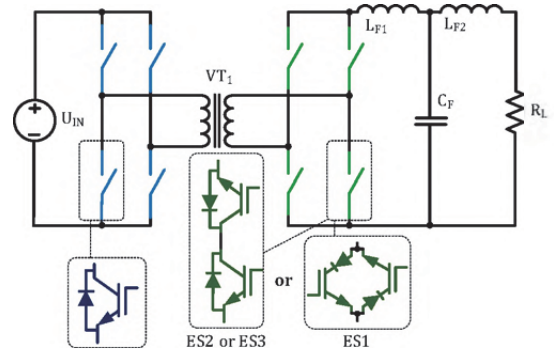


Fig. 1. Full-bridge high-frequency link converter (HFLC) topology.

This study presents power loss characterisation of 1200V RB-IGBT with different manufacturing techniques. RB-IGBT samples were evaluated at 25°C and 125°C under soft-switching conditions, aiming to reduce the negative impact of reverse recovery characteristics. Such conditions are achievable in HFLC operating with special modulation techniques [11]. Based on the obtained results, a power loss estimation and comparison between IGBT and RB-IGBT for soft-switching HFLC topology shown in Fig.1 was done.

## II. RB-IGBT TECHNOLOGY

The latest generations of IGBTs make use of a buffer N type layer between the collector diffusion (P type) and the N-region (the silicon substrate). This buffer layer, sometimes referred to as a field stop layer, stops the electric field penetrating to the collector resulting in low breakdown voltage. This allows a thinner silicon substrate to be used reducing both conduction and switching losses. These IGBTs operate in the punch through (PT) mode, but this is not an option for the RB-IGBT, as the buffer layer will degrade the reverse breakdown voltage. The RB-IGBT must use a non-punch through (NPT) design.

In the conventional IGBTs, the emitter side junction supports the voltage in the off-state. The collector junction is



not required to support a large voltage, only sufficient to stop holes flowing into N- region during the conduction phase of the antiparallel diode. This means that the collector diffusion can be quite shallow and tailored for low injection efficiency to give a suitably low forward volt drop,  $U_{CE(sat)}$ , without excessive injection of holes. Restricting the carrier density in the N- region then improves the turn-off transient without need for lifetime control processes.

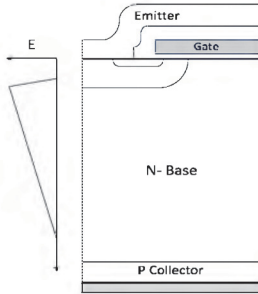


Fig. 2. Generalised RB-IGBT structure.

In the case of the RB-IGBT (Fig. 2), however, the collector junction must be capable of supporting the full rated voltage. To do this the collector diffusion must be of sufficient depth and concentration. With this comes higher injection efficiency leading to higher carrier concentration during the on-state and higher recovery losses. In this work, three techniques to address this problem in the RB-IGBT are compared.

- The dopant concentration in the collector diffusion can be reduced, but at some point, this starts to reduce the reverse blocking voltage and reduces the process yield. Lower dopant concentration in the collector reduces the injection efficiency and consequently the level of conductivity modulating plasma in the N- region in the IGBT on-state.

- Electron irradiation can be used to reduce the lifetime in the N- region. Electron irradiation causes uniform damage throughout the exposed silicon and speeds up turn-off processes but lacks the control needed to target specific areas of silicon for optimum trade-off between conduction and switching losses.

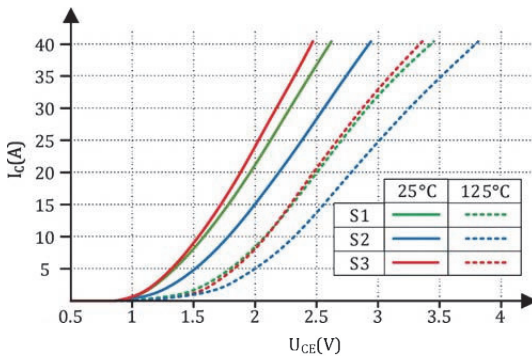


Fig. 3.  $U_{CE}$  vs.  $I_C$  for samples S1-S3 at 25°C and 125°C.

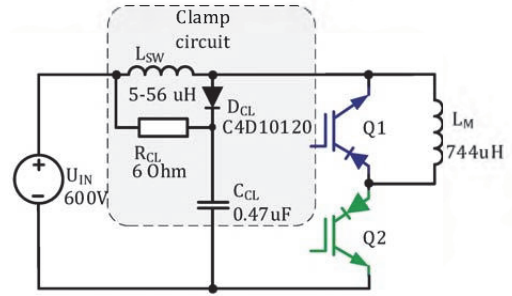


Fig. 4. Test circuit for dynamic losses evaluation.

TABLE I RB-IGBT SAMPLES CHARACTERISED

Samples	Technology
S1	Reduced collector dose 1
S2	Reduced collector dose 2
S3	Standart collector dose, Local lifetime control

- Local lifetime control techniques can be used to reduce the injection efficiency of the collector diffusion without compromising the reverse blocking capability.

### III. EXPERIMENTAL CHARACTERISATION OF RB-IGBTs

In the current section the RB-IGBTs manufactured with reduced dopant concentration and local lifetime control are evaluated in terms of static and dynamic characteristics with different externally defined  $di/dt$  values. Evaluation of RB-IGBT static and dynamic losses was performed for samples listed in Table I. At the end of the section the characteristics of these RB-IGBT are compared to the ones manufactured using the electron irradiation technique and evaluated previously in [13].

#### A. Static losses

The amount of static losses depends on the transistor on-state voltage drop, channel resistance and the value of current flow through this transistor. Fig. 3 presents static losses of S1-S3 at 25°C and 125°C respectively. It could be observed, that the sample S3 has the lowest on state losses, though the difference with S1 is rather small.

#### B. Setup for dynamic losses evaluation

Dynamic losses in typical applications consist of energy dissipated during turn-on and turn-off transitions. The dependency on the operating voltage is generally linear, though not necessarily proportional [12].

Typical design for hard-switching converters generally aims to achieve the balance between the switching and conduction losses at the chosen operating frequency. On the other hand, in soft switching converters the semiconductor total power losses are generally represented by conduction losses. However, as the 1200 V RB-IGBTs have high reverse recovery losses, their contribution in the total dissipated energy can exceed 50%, even under soft switching conditions with reduced  $di/dt$  [13].

The experimental circuit used for dynamic evaluation of RB IGBTs is shown in Fig. 4. As it can be observed, it

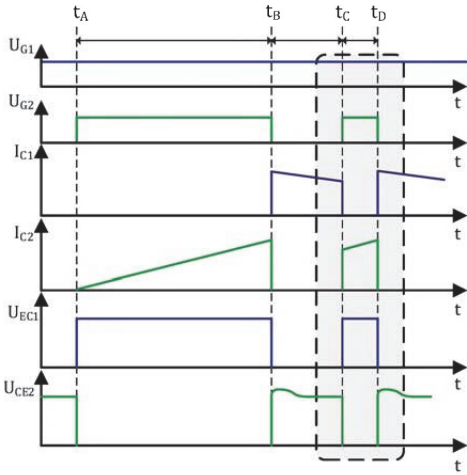


Fig. 5. Double-pulse test circuit switching diagram.

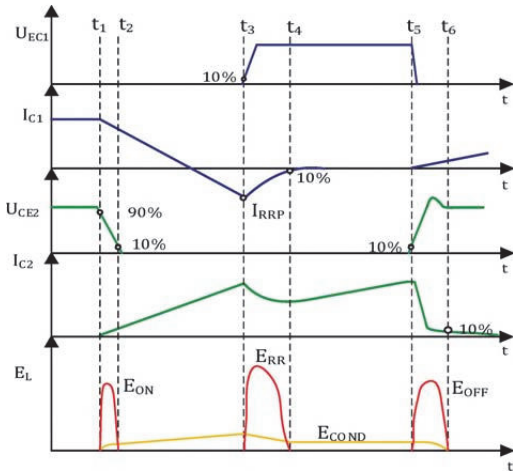


Fig. 6. Energy loss definitions for RB-IGBT.

features an external  $di/dt$  limiting circuit, that is similar to the current clamp applied for IGBTs to limit their turn-on speed. Although the switching processes in this circuit are not completely identical to the ones in the soft-switching high frequency link converters (HFLCs), such circuit can provide a good estimation of switching characteristics of the devices. The device Q2 is evaluated in terms of turn-on transient, while Q1 provides information regarding the reverse recovery process. Table I shows circuit test condition. The switching diagram of the test circuit is shown in Fig. 5. It is identical to conventional double pulse test circuit.

TABLE II. TEST CIRCUIT PARAMETERS

Parameter/device	Symbol	Value / Type
Input voltage	$U_N$	600 V
Test current	$I_C$	5-40 A
Clamp inductor	$di/dt$	17, 26, 40, 105 A/ $\mu$ s
RB IGBT	$S1-S3$	1200 V / 25 A

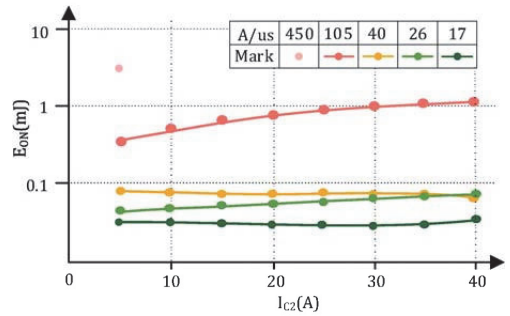


Fig. 7. Turn-on energy losses for sample S1 at 25°C.

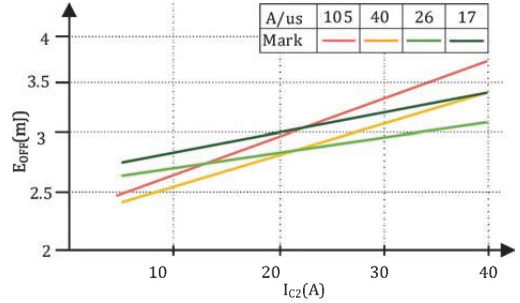


Fig. 8. Turn-off energy losses for sample S1 at 25°C.

The time interval  $t_A-t_B$  was controlled during the experiments to accumulate desired current in the inductor, while the intervals  $t_B-t_C$  and  $t_C-t_D$  were adjusted to be long enough for the clamp circuit to dissipate the energy after turn-off and the transient processes associated with the switching processes to finish (Fig. 5.). The experiments were repeated with different inductances  $L_{SW}$  to investigate the  $di/dt$  influence on the turn-on and reverse recovery characteristics of RB-IGBTs tested. Switching intervals and definitions are presented in Fig. 5.

Dynamically dissipated energy  $E_{LOSS}$  during transition process can be calculated as follows:

$$E_{LOSS} = \int_{t_1}^{t_2} U_q(t) \cdot I_q(t) dt \quad (1)$$

where  $I_q(t)$  is the current through transistor,  $U_q(t)$  is the voltage between collector and emitter.

For the analysed soft-switching circuit, the period for calculation of energy losses during turn-on transition starts, when  $U_{CE}$  drops below 90% of nominal value and ends, when this voltage drops below 10%. Afterwards, the overshoot current starts to flow through transistors Q1 and Q2 and causes additional conduction losses. After the reverse recovery charge of diode being partially recharged,  $U_{EC1}$  starts rising and brings additional losses. For energy calculation this period starts when  $U_{CE1}$  exceeds 10% of nominal voltage and stops, when  $I_C$  drops below 10% of peak reverse-recovery current  $I_{RRP}$ . Energy losses during turn-off transition are calculated for period from  $U_{CE2}$  exceeding 10% of nominal voltage to dropping  $I_C$  below 10% of maximum current [14].



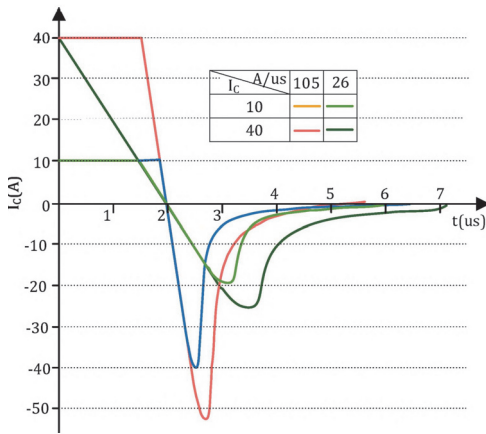


Fig. 9. Q1 collector current shape for different  $di/dt$  values and initial currents.

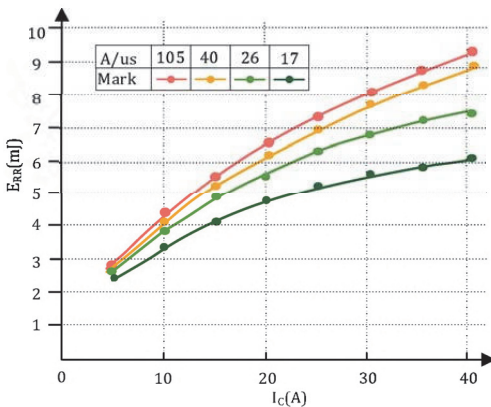


Fig. 10. Reverse recovery losses for sample S1 at 25°C

During the experiments currents and voltages were measured with oscilloscope MSO5034B, voltage probe Tektronix P5205A and current probe Tektronix TCP0150. STM32F3 HRTIM peripheral and Concept 2SD315A1-33 drivers were used to generate signals with required accuracy and strength for the evaluated samples. In order to measure losses at 125°C, commercial heating plates were placed on both sides of the samples and temperature controlled by PID regulator with PT100 sensor placed close to the IGBT sample.

### C. Dynamic losses

Energy losses were measured for samples S1-S3 under different  $I_c$  and the  $di/dt$  values, defined by the clamp inductance to determine the main dependencies. The performance of RB IGBTs was characterised in terms of turn-on energy ( $E_{ON}$ ), turn-off energy ( $E_{OFF}$ ) and reverse recovery energy ( $E_{RR}$ ). Fig. 7 compares the energy dissipation during turn-on transition for sample S1 under different  $di/dt$  values. It is notable that for the hard-switching transition (450A/ $\mu$ s), the amount of energy losses exceeds 5 mJ and that the implementation of soft-switching reduces these losses by an order of magnitude, even using relatively small clamp inductance. At the same time, further reduction of  $di/dt$  has minor effect.

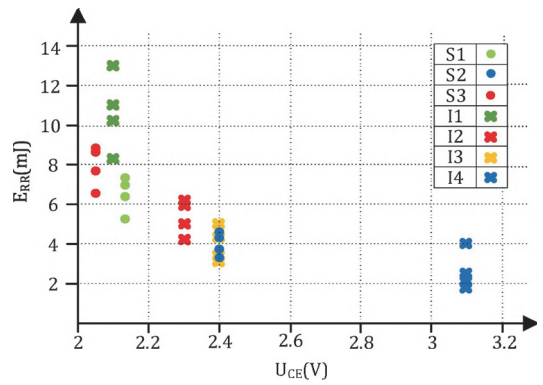


Fig. 11. "Technology curve" reverse recovery losses vs. collector-emitter voltage (25 A;  $di/dt=17...105$ A/us;25°C) for evaluated samples (S1-S3) and samples with different irradiation level (I1-I4) from [13].

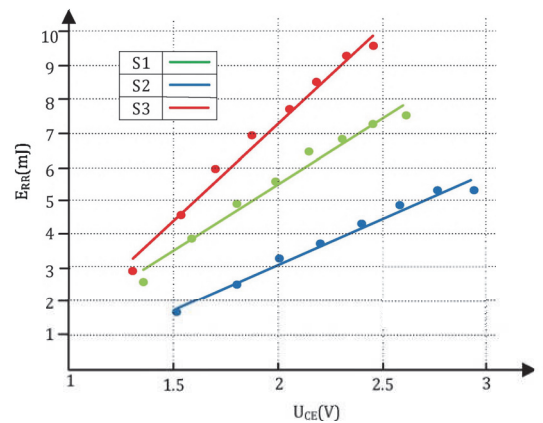


Fig. 12. Reverse recovery losses vs  $U_{CE}$  for samples S1-S3 at 25°C (currents: left-to-right markers 5, 10, 15, 20, 25, 30, 40 A, respectively;  $di/dt=26$  A/us).

Fig. 8 shows energy losses during the turn-off transient defined as  $t_5-t_6$  in Fig. 6. They are not affected by the clamp circuit and they remain significant due to the long tail current and the amount depends on manufacturing technology [15]. Both turn-on and turn-off losses have only small variations for samples S1-S3. As the transistors in HFLC turn off with zero current switching (ZCS), the turn-off losses can be neglected for that application.

As mentioned, the main drawback of RB-IGBTs lies in high reverse-recovery losses and this fact prevents them from wider industrial applicability. Fig. 9 shows Q1 collector current shape under various conditions. As expected, higher  $di/dt$  value causes higher peak reverse recovery current, but the reverse recovery time is reduced. Higher initial current flow  $I_c$  also increases the peak reverse recovery current and in turn the energy dissipated. Fig. 10 shows the reverse recovery losses for S1. At low currents the loss difference between different clamp circuits is relatively small, but at higher values, the soft switching can decrease this loss by up to 30-50%. S2 sample shows the least reverse recovery losses, which are lower by around 30% when compared to S1.

TABLE III. TRANSISTORS FOR HFLC ENERGY LOSS EVALUATION

Eval. sample	Device	Type	$U_{CEsat}(V)$	Dynamic losses
ES1	RB IGBT	S2	2.4	high
ES2	IGBT 1	IXA20IF1200HB	1.8	medium
ES3	IGBT 2	IXYH20N120C3D1	3.4	low

TABLE IV. TRANSISTORS FOR HFLC ENERGY LOSS EVALUATION

Parameter	Symbol	Value
Input voltage	$U_{IN}$	400 V DC
Output voltage	$U_{OUT}$	230 V AC
Load current	$I_L$	1-15 A
Switching frequency	$f_{sw}$	5-30 kHz
Transformer turns ratio	$N$	1:1.1
Leakage inductance	$L_{sbc}$	5 $\mu$ H ( $di/dt=105A/\mu$ s)
Filter inductance 1	$L_{F1}$	2.2 mH
Filter inductance 2	$L_{F2}$	1 mH
Load resistance	$R_L$	15..60 Ohm

#### D. Technology curves

In order to evaluate the RB IGBT two “technology curves” were built. Due to fact that  $E_{ON}$  in the particular application is minor and  $E_{OFF}$  can be omitted due to ZCS, the  $E_{RR}$  and  $U_{CE}$  were taken into consideration. Fig. 11 and Fig. 12 show that the sample S1 is more suitable for low-frequency application due to low forward drop voltage. On the other hand, sample S2 is more suitable for mid-frequency applications due to lower total dynamic losses. In general, sample S2 demonstrates reduced losses of up to 20% compared to the previously evaluated devices (I1-I4 in Fig. 11.), that were manufactured using electron irradiation technique [13].

#### IV. INVERTER LOSS ESTIMATION

In order to evaluate the performance of the RB-IGBTs, a bidirectional switch formed by antiparallel connection of S2 devices was compared with two standard IGBTs in common emitter configuration. The evaluated devices are listed in Table III. For the comparison the following standard IGBT devices were chosen: ES2 optimised for low on-state

The total power losses were estimated for compared devices assuming their operation in full bridge HFLC shown in Fig. 1. In the converter, a special modulation method was applied that allowed the bidirectional switches to turn-off naturally [11].

Table IV lists parameters of the HFLC topology from Fig. 1. The HFLC is intended to generate an isolated 230V AC sine voltage from 400 VDC power supply. Assuming that the voltage variation at the DC side is not significant, the voltage and rate of current rise on the secondary winding remains constant regardless of the instantaneous value of the output AC voltage. As a result, for the case study converter, the  $di/dt$  during switching transients was constant and close to 100 A/ $\mu$ s. loss and ES3 optimised for fast switching.

Fig. 13 shows the total power loss for the evaluated samples S1-S3 at 25°C for 10 and 15 kHz operating frequencies. Sample ES3 has low dynamic loss and the influence of the switching frequency is minor. However,

with the power increase, static loss increases drastically. ES2 demonstrates lower loss increase at high load, however frequency increase shows higher impact on the losses. Finally, RB-IGBT transistor shows high power losses for light load, but demonstrates high efficiency at power levels over 2.2 kVA. Additionally, ES1 loss trendline shows, that the technology could be advantageous for higher power applications.

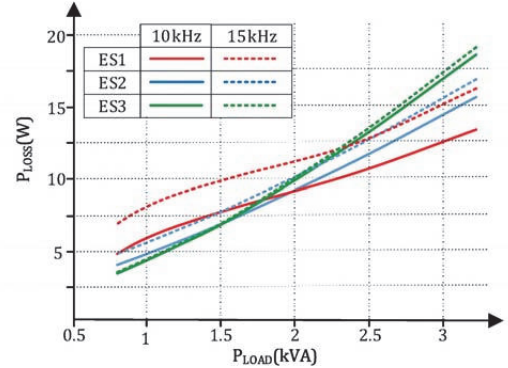
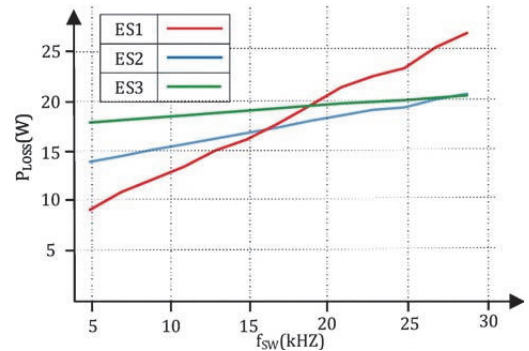
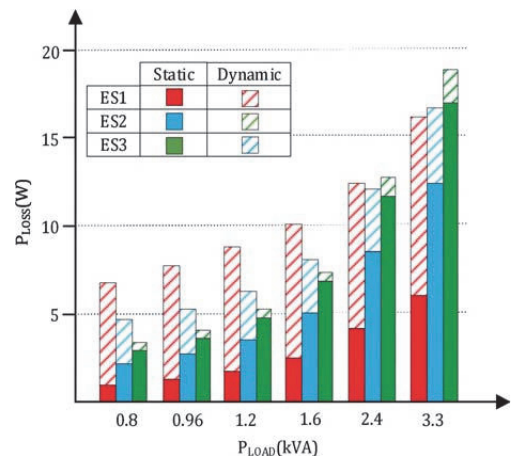
Fig. 13.  $P_{LOSS}$  VS  $P_{LOAD}$  for switching frequency 10 and 15 kHz at 25°C.Fig. 14.  $P_{LOSS}$  vs switching frequency for ES1-ES3 at  $P_{LOAD}=3.3$  kVA.

Fig. 15. Static and dynamic losses for samples ES1-ES3 at 15kHz and 25°C.



On the other hand, the RB-IGBT shows lower efficiency at high frequencies. Fig. 14 demonstrates power loss of switches at different frequencies with fixed converter power of 3.3 kVA. ES1 demonstrates twice lower energy losses at 5 kHz compared to ES3, but with frequency increase the *benefits* of RB-IGBT are lost. Fig. 15 presents comparison of types of power losses for different configurations. As expected, the major source of losses for ES3 are dynamic losses, which makes up 90% at  $P_{LOAD}=0.8$  kVA and 65% at  $P_{LOAD}=3.3$  kVA. At the same time, static loss contribution is twice lower compared with SE2 and 3 times lower than for SE3.

## V. CONCLUSION

This paper presented the characterisation of 1200V RB-IGBT with different manufacturing techniques. Static and dynamic power losses were measured at different operating conditions. The analysis showed that the RB-IGBT samples have turn-on and turn-off characteristics, which are typical of other IGBT transistors manufactured with the same technology. On the other hand, the reverse-recovery losses are quite high, as a result this type of transistor cannot compete with conventional IGBTs in typical circuits with hard switching conditions.

However, utilising anti-parallel connected RB-IGBTs for a bidirectional switch instead of standard IGBTs with common emitter configuration could increase efficiency in the case of high-power converters, featuring soft switching conditions and reduced  $di/dt$ . The measurements show that the RB-IGBT features low static losses, while the dynamic losses can be reduced significantly with  $di/dt$  lowered to around 100 A/ $\mu$ s. Further lowering of  $di/dt$  has smaller impact, also increasing the reverse-recovery time and duty cycle loss. As a result, the trade-off between power loss,  $di/dt$  and the switching frequency should be made. The study shows that the RB-IGBT can be superior to standard IGBTs in a case study of HFLCs with rated power of 3.3 kVA and 230 VAC/50 Hz output for the switching frequencies up to 15 kHz.

## ACKNOWLEDGMENT

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**Publication VII**

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# Optimization and Design of Planar Transformer for the High Frequency Link Converter

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**Abstract** — In this paper, the analysis and experimental verification of a planar transformer for a high-frequency link converter is presented. The known problem of such topologies is strict limitations related to the transformer leakage inductance and parasitic capacitance. This problem is more pronounced in the systems with high transformer turns ratio. The current research aims to find the low-cost solution, at the same time to ensuring that the values of the parasitic parameters are in the acceptable range. The verification of different 1:10 transformer design approaches was experimentally verified with a 1 kW converter prototype.

**Keywords**— Cycloconverter, high frequency link DC-AC converter, single stage converter, power transformers.

## I. INTRODUCTION

With the continuously increasing share of renewable sources, the DC systems are becoming a significant part of the electricity grid [1]. These include photovoltaic, battery, fuel cell, supercapacitor, and other applications. Power electronic converters are essential in order to interface such components with the AC grid. The two-stage power conversion with DC-link is typically used for relatively low voltage sources: a step-up isolated DC-DC converter is followed by a DC-AC inverter [2]. The transformer's presence provides considerable flexibility and scalability in the connection between the DC source and the utility grid, compared to the non-isolated systems. This makes isolated solutions widely used, despite their usually larger volume and weight [3].

High-frequency link converters (HFLCs) are another class of topologies that can provide bidirectional DC-AC conversion together with galvanic isolation (Fig. 1) [4]-[7]. They do not include a high voltage DC-link capacitor and soft switching of semiconductors can be achieved with advanced modulation techniques. Simultaneously, in practical applications, the leakage inductance and output capacitance of transistors together form an oscillatory circuit, which creates the voltage overshoot and oscillations at the AC side [8]. In general, lower leakage inductance value can reduce the oscillatory energy and duty cycle loss associated with the switching transients [9]-[10], reducing its overall impact on the converter operation.

For HFLCs that are intended to interface a relatively low voltage source, the problem of leakage inductance is more pronounced due to higher turns ratio requirement of the isolation transformer. This is the main reason why such converters are usually designed with a transformer with moderate turns ratio.

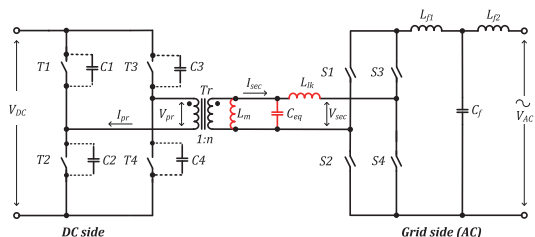


Fig. 1. High frequency link full bridge converter

Table I. SPECIFICATIONS OF THE CASE STUDY CONVERTER

Parameter	Value
Input voltage range, $V_{IN}$	48 V
Input current range, $I_{IN}$	0..30 A
Output voltage, $V_{AC}$	230 V
Operating power range, $P$	1 kW
Switching frequency, $f_{sw}$	50 kHz
Transformer leakage inductance $L_{lk}$	10..28 $\mu$ H
Transformer magnetizing inductance $L_m$	~4 mH
Transformer turns ratio, $N$	10

The current study's object is a 1 kVA full-bridge HFLC intended to interface a source with a nominal DC voltage of 48 VDC with the 230 VAC utility grid (Table I). The converter features a quasi-resonant modulation method [10], which allows the implementation of lossless snubber capacitors at the DC-stage to reduce its switching losses. This paper will focus on the analysis, development, and comparison of different transformer design approaches to elaborate the optimal solution for the case study converter.

## II. ESTIMATION OF THE TRANSFORMER PARAMETERS

### A. Dimensioning of the magnetizing and leakage inductances

The modulation method applied in the case study HFLC allows for soft-switching conditions for semiconductors during a special resonant state, without utilizing the magnetizing current. Therefore, the transformer can be designed for a large value of magnetizing inductance to reduce energy circulation and power losses. In the current study, the values of equivalent inductances are referred to as the secondary transformer winding (the one with higher turns number). The RMS value of the magnetizing current at the primary winding can be estimated as:

$$I_m^{\text{rms}} = \frac{n^2 \cdot V_{DC}}{4 \cdot \sqrt{3} \cdot L_m \cdot f_{sw}} \quad (1)$$

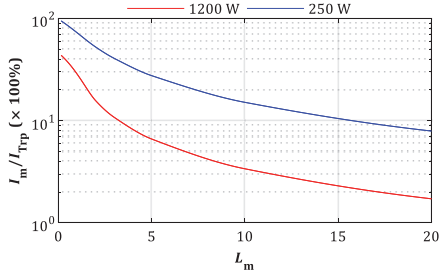


Fig. 2. Estimated ratio between transformer magnetising and primary currents for various magnetising inductance values.

where  $f_{sw}$  is the converter switching frequency,  $V_{DC}$  is the DC side voltage, and  $L_m$  is the magnetizing inductance value, and  $n$  is turns ratio of the transformer.

The ratio between magnetizing and transformer primary currents is shown in Fig. 2. To not compromise the energy circulation and overall efficiency, the optimal value of  $L_m$  should be chosen within 3...10 mH.

The flux in the transformer, which generated the AC current in the primary winding, follows the magnetic core and transferred to the secondary winding. Some of the flux leaks from the transformer core and winding to the air gap, isolating layers, creating non-perfect coupling. The energy associated with the leakage inductance can be calculated using the magnetomotive force distribution. While the precise estimation of the resulting leakage inductance  $L_{lk}$  is relatively hard to estimate initially, the value of  $<0.5\%$  of  $L_m$  can be chosen as the initial target for the leakage inductance-minimized design [11].

### B. Dimensioning of the turns ratio

Certain extra time intervals have to be introduced to provide soft-switching transients between switching modes of the HFLC. This results in the loss of the energy transfer time and reduces the output voltage amplitude. According to [10], this amount is closely related to the values leakage inductance and snubber capacitance. The coefficient value of 0.9 can be used as the first approximation for the target design [6][10].

Assuming that the required amplitude of the output AC voltage ( $230 V_{rms} \pm 10\%$ ) is:

$$\hat{v}_{AC} = 230 \cdot \sqrt{2} \cdot 1.1 = 358 \text{ V}. \quad (2)$$

and the minimal DC voltage  $V_{DC}$  is 42 V, the required transformer turns ratio is:

$$n = \frac{\hat{v}_{AC}}{V_{DC} \cdot 0.9} = 9.47. \quad (3)$$

In order to compensate for the voltage drop across semiconductors and provide a certain design margin, a target turns ratio of 1:10 is chosen.

### C. Reference design

The reference transformer design analyzed is that the current study is based on a toroid core. Nowadays, these are one of the popular types due to compact shape, the low stray magnetic field, high efficiency, ease of mounting, and a wide range of working frequencies. Usually, in this type of transformer uses the litz wire, which allows to reduce the

total resistance of the wire at the high frequency and minimize the skin effect [12]. At the same time, the proximity effect must be considered, especially in the high-current winding. The parameters of the transformer are listed in Table II. The transformer primary winding consists of 3 primary turns formed by 60 parallel litz wire bundles, each having 22 strands. The 31 turns of the copper wire with 1 mm in diameter were used on the secondary winding. As observed from Table II, the reference design meets the general application requirements and provides a relatively low leakage inductance value: 0.3% of  $L_m$ . Simultaneously, such a transformer's manufacturing cost can be relatively high, mainly due to the specific realization of the primary winding.

TABLE II SPECIFICATIONS OF REFERENCE TRANSFORMER

Parameter	Value
Core type	ferrite
Number of turns in primary side	3
Number of turns in secondary side	31
Primary - litz wire	60×(0.09mm×22)
Secondary - copper wire	1mm
Transformer leakage inductance $L_{lk}$	28 $\mu$ H
Transformer magnetizing inductance $L_m$	10 mH
Transformer turns ratio, $N$	10

## III. DESIGN OF THE PLANAR TRANSFORMER

### A. General description

There are known approaches [13], [14] that have been presented to reduce the magnetic components cost and size. The planar structure provides an excellent solution for the power converters and allows them to minimize the magnetic elements height and increase the power density. One of the benefits of the planar transformer is that the windings have a flat structure and can be made using the printed circuit board layers or copper foils. This can be more suitable for the high-frequency operation, because the planar transformer has a lower sensitivity to the proximity effect. Thus, its potential advantages over the conventional wire-wound are low profile, good thermal characteristics, high power density, ease and reduced cost of manufacturing, modularity, repeatability, ease in implementing the interleaved winding designs. The disadvantages are the large footprint, low copper fill factor, limited number of turns and high inter-winding capacitance [15], [16].

The total leakage energy is the sum of the energy stored in each layer of the planar transformer and can be calculated as

$$E_{lk} = \frac{\mu_0}{2} \sum_0^h \int H^2 \cdot l_w \cdot b_w \cdot dx, \quad (4)$$

where  $l_w$  is the length of turn,  $b_w$  is the width of turn,  $h$  is the thickness of the winding layer. The strength  $H$  depends on the numbers of the ampere-turns, which are linked to the flux path. According to the [14] in the full interleaved structure of the transformer, the leakage inductance can be found as:

$$L_{lk} = \mu_0 \cdot \frac{l_w}{b_w} \cdot 4 \left( \frac{h_1 + h_2}{3} + \Delta h \right), \quad (5)$$

where  $h_1$ ,  $h_2$  is the thickness of the primary and secondary layers respectively,  $\Delta h$  is the thickness of the insulator layer.



It is well-known that the interleaving of the windings allows to reduce the leakage inductance [14], [15]. As mentioned, a relatively large value of leakage inductance creates the oscillation at the AC side switches, increasing stresses for the switches and can result in the EMI problems. Simultaneously, in planar transformers, interleaving increases the capacitance between the turns of the transformer. As a result, in the transformer with relatively high number of layers, the negative effects from parasitic capacitances can offset the benefits of low leakage inductance [16].

In general, the capacitance between the two layers of foil in the planar transformer can be easily estimated since this winding is flat and parallel to each other:

$$C_0 = \epsilon_r \cdot \epsilon_0 \frac{S}{\Delta h}, \quad (6)$$

where  $\epsilon_0$  is the permittivity of the air space,  $\epsilon_r$  is the permittivity of the winding material,  $S$  represents the overlapping surface area between the conductor.

### B. Parameter definition

In the case study transformer design, the windings are realized with copper foil. The most straightforward realization would include ten series connected secondary turns and one primary turn, consisting of several paralleled copper layers. Using the datasheet parameters of the Ferroxcube E64/10/50 core (3C95 ferrite), the  $L_m$  can be estimated as:

$$L_m = A_L \cdot n^2, \quad (7)$$

and the maximum flux density as:

$$B_{\max} = \frac{U_{DC}}{4 \cdot n_1 \cdot f_{sw} \cdot A_e}. \quad (8)$$

Where  $A_L$  is the inductance factor and  $A_e$  is effective magnetic cross section.

In order to achieve the desired values of  $L_m$ , avoid core saturation and reduce core losses, a combination of two E64/10/50 core pairs was chosen. The parameters are summarized in Table III.

TABLE III PARAMETERS OF THE DEVELOPED TRANSFORMER

Parameter	Value/Type
AC-side winding copper foil	0.1 mm
DC-side winding copper foil	10×0.05 mm
Switching frequency	50 kHz
Turns ratio	1:10
Rated power	1200 W
Core	E64/10/50
Magnetizing inductance	3.4 mH
Estimated core losses	< 10 W
Isolation (polyamide film)	0.076 mm (6 kV)

## IV. SIMULATION OF THE TRANSFORMER

For the verification of the proposed approach, a series of computer simulations were performed in the ANSYS software to verify and analyses the values of the leakage inductance and capacitance between the transformer winding. Fig. 3 shows the model of the planar transformer with the flat cooper winding, alternative approach is hybrid structure, where for the secondary winding the litz wire was

utilized (Fig. 4). The magnetic field distribution in the cores is shown in Fig. 5.

Unfortunately, ANSYS cannot directly determine the value of the leakage inductance. The value was estimated

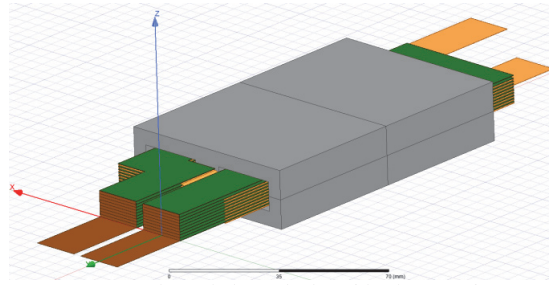


Fig. 3. The isometric view of the planar transformer simulation model

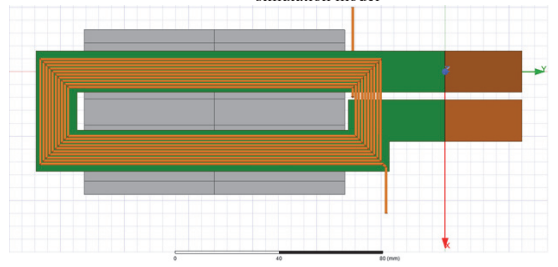


Fig. 4. The top view of the hybrid planar transformer simulation model

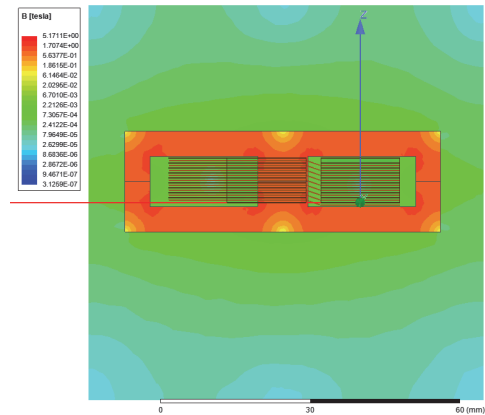


Fig. 5. The magnetic field distribution in the planar transformer

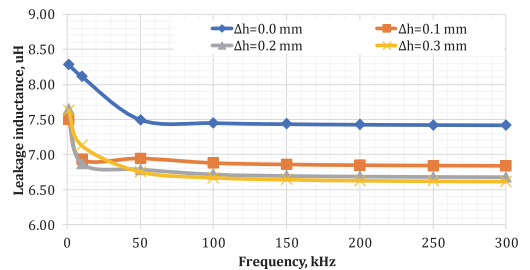


Fig. 6. The leakage inductance with Type 1 interleaving  $L_{ik}$  vs frequency for different distance between windings  $\Delta h$



analytically, based on the sum of self-inductances of the primary and secondary windings separately and referred to the secondary winding. In Eddy's current mode, the value of transformer winding inductance and the coupling factor was investigated for frequencies up to 300 kHz (Fig. 6). At frequencies greater than 50 kHz, the leakage inductance value and the coupling coefficient do not change significantly. The best case is the maximum distance between the turns of windings (0.3 mm).

In general, the leakage inductance is mostly influenced by number of the turns, positions (interleaving of the turns) and geometric dimensions. It is almost independent of the thickness of the winding and distance between layer and changes less than five percent for the range of frequencies analyzed. Several models were created to verify the difference in transformer parameters for various interleaving techniques. Initially, the models without interleaving (Fig. 7a), with full interleaving (Type 1 in Fig. 7b) and double interleaving (Type 2 in Fig. 7c) were created. According to simulations, the full interleaving (Type 1) has the lowest value of leakage inductance. The double interleaving (Type 2) has the average value (Fig. 8), and for design without interleaving the leakage inductance was more than 12  $\mu\text{H}$  (not shown in graph). At the same time, the minimal value of the leakage inductance results in high parasitic capacitance (Fig. 9). The triple interleaving (Type 3 in Fig. 7d) was evaluated to a better trade-off between parasitic parameters of leakage inductance and interwinding capacitance. This allowed to decrease the capacitance two times, while increasing the leakage inductance only 1.2 times when compared to Type 2 interleaving.

It is evident, that the greater distance between the turns allows decreasing the parasitic capacitance. The graph in Fig. 9 has exponential decay and after behavior becomes much smoother. Therefore, in order to obtain similar results in practice, it is necessary to observe the proper distance between the layers, which at the same time complicated due to low planar transformer profile. Also, the capacity of the transformer is almost independent of the thickness of the turns of the winding. Therefore, the effect of this parameter on the parasitic capacitance can be neglected.

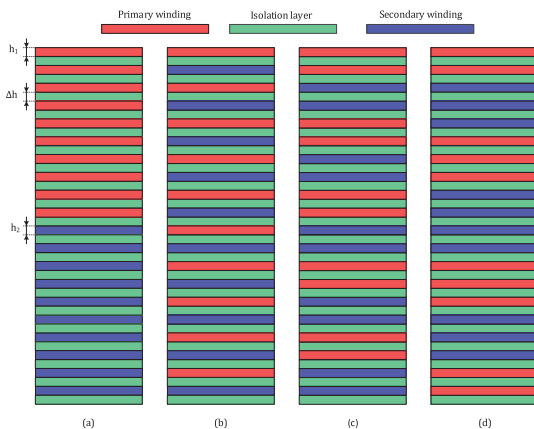


Fig. 7. The different winding interleaving techniques, P- primary winding, S – secondary winding (a – without interleaving, b – Type 1, c – Type 2, d – Type 3)

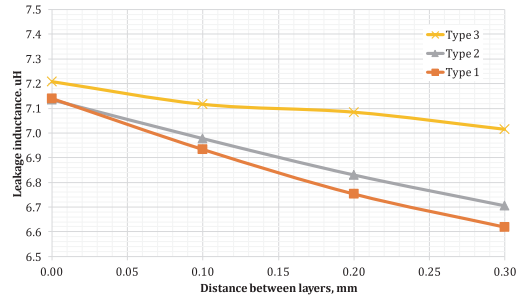


Fig. 8. The leakage inductance of the secondary winding for different interleaving techniques

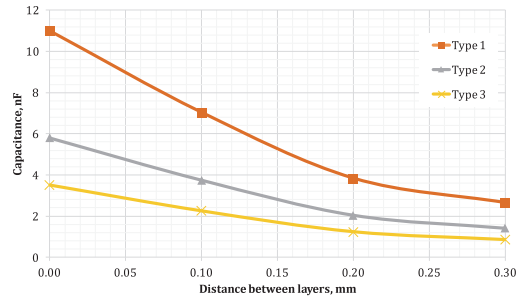


Fig. 9. The capacitance of the transformer for different interleaving techniques

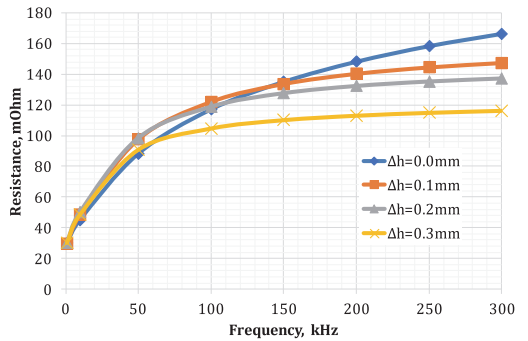


Fig. 10. The resistance of the winding for different frequency and  $\Delta h$

Fig. 10 presents the value of full resistance of the secondary winding under different frequency and different distance between windings  $\Delta h$ . As shown, at 50 kHz the resistance is not strongly influenced by the distance between layers. At higher frequencies, the distance between layers has higher impact on resistance.

## V. EXPERIMENTAL RESULTS

For verification of simulation results, an experimental planar transformer (Fig. 13) was built, and a series of experiments with different interleaving approaches and structures was conducted. The planar transformer is compared to the reference toroidal design (Fig. 12 and Table II). The measurements were carried out with an Agilent U1733C RLC meter and referred to the secondary

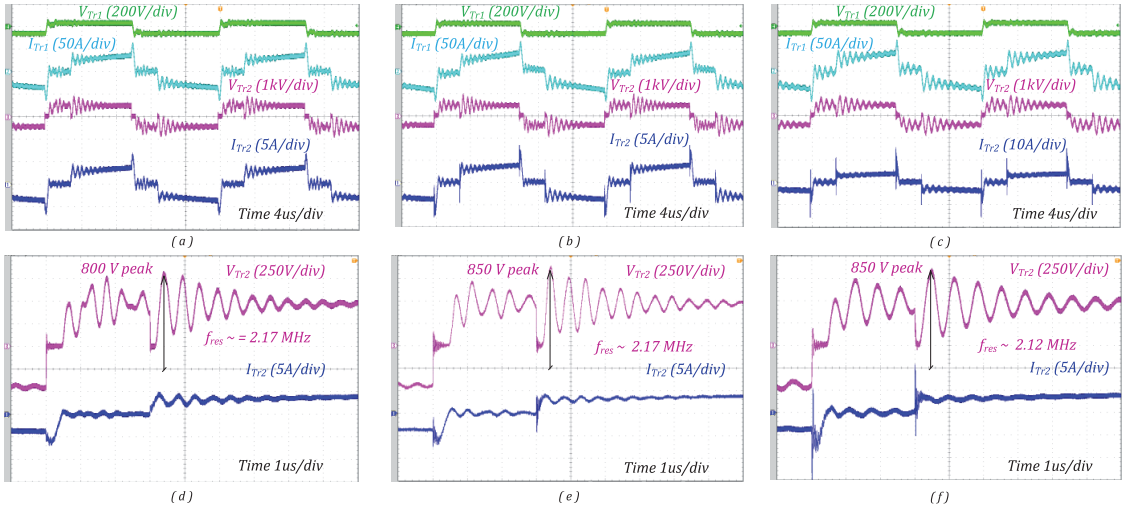


Fig. 11. Experimental waveforms of voltage and current across the transformer at 1 kW with  $V_{IN} = 48$  V, toroidal transformer(a,d), planar transformer without interleaving(b, e) and planar transformer with triple interleaving-Type 3 (c,f).

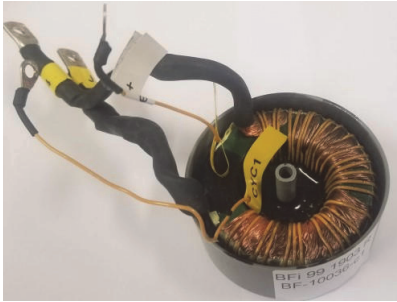


Fig. 12. The reference toroidal transformer design

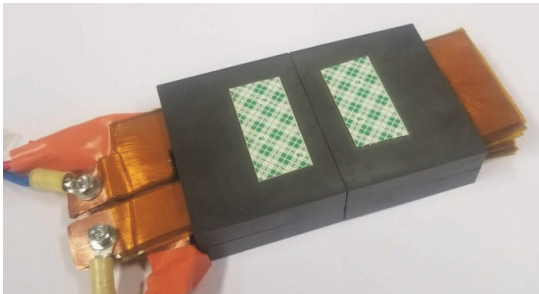


Fig. 13. The developed planar transformer

side of the transformer. The magnetizing and equivalent leakage inductances were measured with primary winding open- and short-circuited, respectively. The capacitance was measured between the short-circuited primary and secondary windings. The measurement results are listed in Table IV.

The difference in the values between the model parameters and practical transformer can be explained by the non- accurate and uniform distance between the layers, the non-perfect fit of the insulating tape, a certain gap between

the ferrite cores, the non-ideal shape of the turns (certain deviations in geometric dimensions, gaps) and not perfect alignment of turns. However, the general trendlines in the model and in a practical transformer are similar.

TABLE IV EXPERIMENTALLY MEASURED PLANAR TRANSFORMER PARAMETERS

Parameter	Magnetizing inductance, $L_m$ , mH	Leakage inductance, $L_{lk}$ , $\mu$ H	Inter-winding capacitance, $C_0$ , nF	Measured converter efficiency	
<b>Toroidal type</b>	10	28	0.5	93.4	
<b>Planar type</b>	<b>Non inter-leaving</b>	3.3	19.1	0.19	92
	<b>Type 1</b>	3.3	13.6	2.0	92.8
	<b>Type 2</b>	3.3	13.8	2.69	92.5
	<b>Type 3</b>	3.3	14.5	1.5	92.2
	<b>Hybrid</b>	3.3	15	0.3	93.3

To verify of the proposed transformer for the HFLC, the experimental laboratory prototype was assembled and tested. The steady state waveforms are shown in Fig. 11. In the experiment, the converter was operating in the DC-DC mode at power of 1 kW, input voltage is 48 VDC and output of 230 VAC. Fig. 11a and Fig. 11d shows the voltage and current across the primary and secondary windings of the transformer and zoomed view of the secondary winding for the reference toroidal transformer. In Fig. 11b the non-interleaved arrangement was tested, in this case we can observe higher current spike when compared to reference transformer. The proposed structure (Fig. 11c) also resulted in the significant voltage spikes. With the Type 3 (Fig. 11c, f) the current spike is noticeable as well, which can be explained by a significant value of the parasitic capacitance of the transformer.

Finally, the hybrid structure of the planar transformer was implemented. In this case the primary winding has the same structure made of copper foil. The secondary side utilises the litz wire that create ten flat turns. The value of capacitance

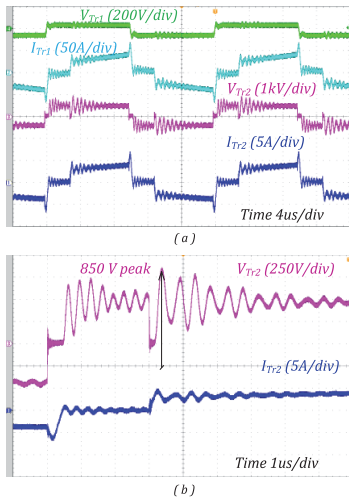


Fig. 14. Steady state waveforms with hybrid planar transformer

is relatively low and equals 0.36 nF, while the value of leakage inductance is 13  $\mu$ H. The measured characteristics listed in Table IV were close to simulated ones and the experimental waveforms of hybrid transformer are presented in Fig. 14. As observed, the waveforms are similar to the reference toroid design. The efficiencies listed in Table IV demonstrate the influence of the transformer design on the overall efficiency of HFLC.

## VI. CONCLUSIONS

In this work the analysis and modelling of the planar transformer with high turns ratio for HFLC was performed. Different interleaving approaches were analyzed and compared by simulations and experiments in order to obtain the best trade-off between the leakage inductance and parasitic capacitance. Planar design allowed to minimize the leakage inductance value when compared to the toroidal one. Nevertheless, the experimental results have shown, that the designs with foil windings result in the current spikes at the transformer due to large inter-winding capacitance. To minimize this issue the hybrid type planar transformer was tested and showed the most promising results. The measured efficiency also shows that the planar hybrid structure could be used in case high turn ratio of transformer and allows to provide design with lower profile, with comparable conversion efficiency. The future research will be focused on the implementation of the planar transformer with high turn ratio using the stacked PCBs.

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- **VE19058** - High-efficient EV charger based on 3-level unifier and current-fed isolated DC-DC converters
- **LEEEE20047** - Flexible Power Electronic Interface for DC Grid Integration of Residential Photovoltaic and Battery Energy Storage Systems (FPEI)
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- **LEEEE20047** - Universaalne jõuelektronika sidumismuundur päikesepaneelide ja akusalvestite integreerimiseks kodumajapidamiste alalisvoolu-elektrivõrkudesse
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