THESIS ON POWER ENGINEERING,
ELECTRICAL ENGINEERING, MINING ENGINEERING D41

Research and Development of Digital Control Systems and Algorithms for High Power, High Voltage Isolated DC/DC Converters

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TUT
PRESS

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Declaration:

Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for any academic degree.

Indrek Roasto.....

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ENERGEETIKA. ELEKTROTEHNIKA. MÄENDUS D41

Võimsate kõrgepingeliste alalisvoolumuundurite arvjuhtimissüsteemide ja -algoritmide uurimine ning väljatöötamine

INDREK ROASTO

TTÜ
KIRJASTUS

Contents

INTRODUCTION

The last ten years in power electronics have seen only minor changes and novelty in the field of converter topologies. On the other hand, developments in semiconductor components have been tremendous. Thus, modern trends in power electronics are directed to the implementation of well-known topologies rather than developing new ones. Using new state of the art components, conventional converter topologies can be used more efficiently and for much higher power levels. The recent efforts in the field of power electronics semiconductors are especially interesting for high power (HP) and high voltage (HV) applications where the voltage blocking capability of components has always been a major issue. In order to achieve the needed voltage blocking capability traditionally many low voltage components are connected in series but, as a result, the number of components and the complexity of a control system will increase, which reduces the efficiency and overall reliability of the converter. Using new generation components the efficiency and the power density of electronic converters and thus, the feasibility of the whole system can be enhanced.

The first implementation of new generation components is always connected to the research and development to find out the behaviour of the component, its characteristics, achievable efficiency, reliability etc. Those parameters all are connected to a specific application and cannot be found inside the component datasheets. Research and development is quite a time-consuming process and involves additional costs that the companies are usually trying to avoid. Therefore, the research and development of new technologies is usually left for the universities and other scientific organizations that have the needed know-how and resources.

Traction applications are a good example where recent achievements of power electronics could be applied. However, due to the risks and high expenses, most of the companies still offer old converter solutions, which have proved their reliability over a decade but have quite low efficiency and power density compared to the new state of the art systems. In this doctoral project new generation high voltage insulated gate bipolar transistors (IGBT) were implemented, which could essentially improve converters performance.

The Department of Electrical Drives and Power Electronics of Tallinn University of Technology (TUT) has long-term experience and know-how in the field of electrical transportation and traction applications. Therefore, the current doctoral project was also directed to this application field.

The research work was done in cooperation with the Estonian company Estel Elektro Ltd. Given company produces auxiliary power supplies (APS) for rolling stock. The weak point of the conventional APS (Fig. 1) is the front-end converter, which is the link between HV (U=2 kV…4 kV) contact line and intermediate DC-bus (350 VDC) as shown in Fig. 1. In order to achieve the needed voltage blocking capability, currently the front-end converter consists of

seven series-connected inverters, as shown in Fig. 2. The main drawbacks of this solution are: high number of components, low reliability and efficiency, complicated control and voltage balancing problems. Researchers of TUT together with the author of this thesis analyzed the problem and proposed to use a half-bridge topology with new generation HV IGBTs.

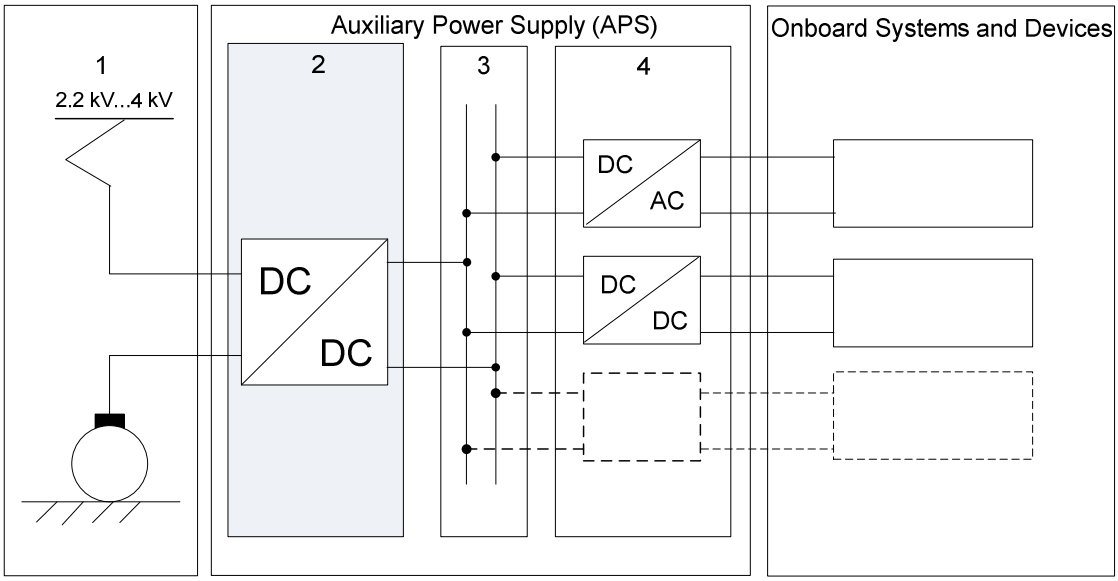

Fig. 1 Auxiliary power supply for traction applications: 1- contact line, 2- front-end converter, 3- intermediate DC-bus (350 VDC), 4- auxiliary output converters

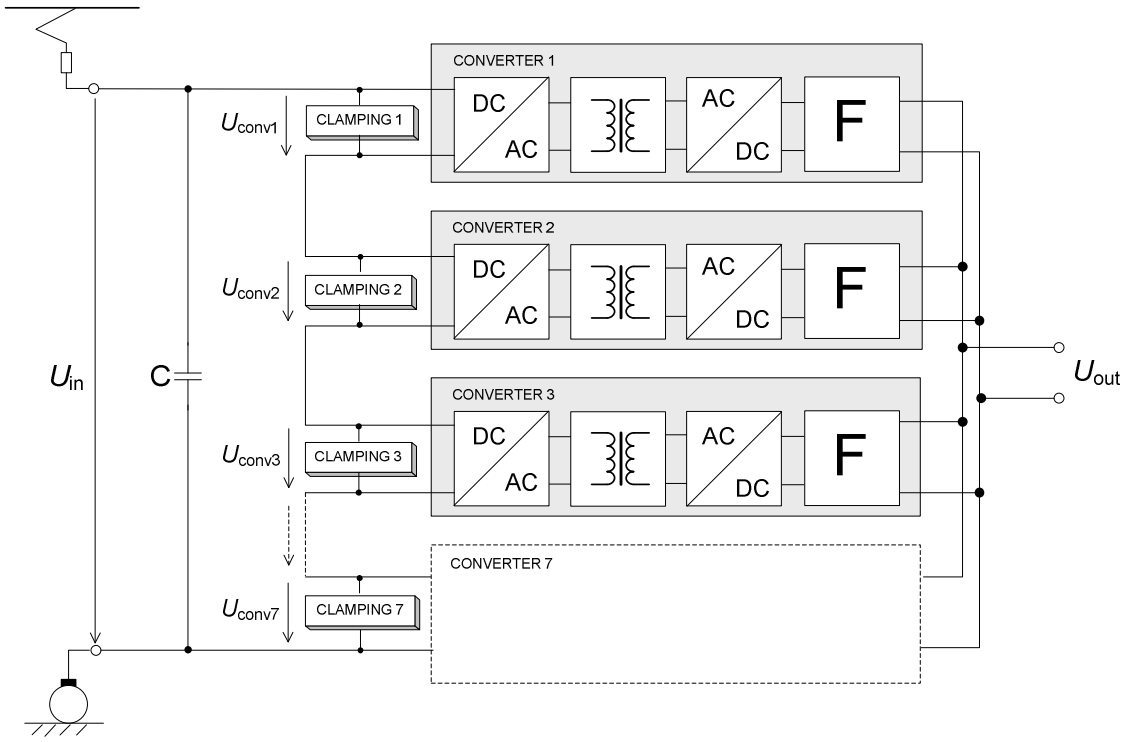

Fig. 2 FEC with 7 series-connected DC/DC converters

Half-bridge (HB) isolated DC/DC converter is widely known as an attractive topology for different low power, low voltage applications, such as telecommunication facilities, fuel cell based power generation systems, compact power supplies and other systems with a power range of 1...2 kW. Advantages of the HB topology are obvious [1][2]:

1. reduced number of primary switches and control signals;
2. half-bridge inverter output voltage rating reduced to half of the input;
3. no centre-tapped transformer required for the input stage.

In this doctoral project the HB topology will be first examined as a candidate topology for the front-end converter (FEC) of the rolling stock auxiliary power supply (APS). Main design problems of converters with high input voltage are the voltage blocking capability of primary inverter switches. Modern trends are to use IGBT in the design of HP and HV applications. With such benefits of IGBTs like ease of use, high switching frequencies and efficiency, the overall design quality of power supplies for traction applications can be drastically improved. The information about new generation HV IGBTs (up to 6.5 kV) on the market was the motivator to propose the two-level HB topology for the FEC. The 6.5 kV IGBT modules are, in general, designed for 3.0 kV DC rolling stock applications with high demands on reliability. The main differences of the conventional and proposed topology of the FEC are shown in Table 1. As can be seen, using recent semiconductor devices the number of components could be remarkably reduced. Moreover, as a logical enhancement of the two-level HB, the three-level HB topology with 3.3 kV IGBTs was proposed and implemented in the current doctoral project.

Table 1 Comparison of the conventional and the proposed topology for FEC of APS

Details	FEC with series-connected DC/DC converters	Proposed two-level HB
IGBTs	28	2
Input capacitors	1	2
Isolation transformers	7	1
Rectifier diodes	28	4
Balancing electronics	7	0

However, such a novel design of the FEC requires also a novel control system. Compared to many low power (P<500 W) applications where HB converters have been conventionally implemented, the HP (P>20 kW) and HV (U>2 kV) FEC for rolling stock is much more demanding application. Not only because of rough environmental conditions but also because of many tasks that the converter must deal with, e.g. controlling inverter switches, monitoring and storing of internal parameters, displaying sensor data, processing of status and error feedback, communication with external devices etc. Additionally, an important issue is a protection system especially in HP and HV applications

where already a small error can have catastrophic results. To achieve maximal protection and fluent operation at least a two level protection system is needed, i.e. some of the most vital protection functions must be duplicated. Hence, general purpose low cost integrated circuits available in different realizations and with different control functions on the market can not be applied in the FEC for traction applications. Such a demanding control and communication system requires a flexible and advanced controller that has sufficient calculation power and peripherals to fulfil all the requirements.

The results of the project will be discussed in two doctoral theses. The first is mostly dealing with the hardware side including a study of switching properties of HV IGBTs, component design issues and parameters optimization etc. (author Tanel Jalakas, Ph.D. student of Tallinn University of Technology). The current thesis is mainly concentrating on the control system research, design and development.

In order to specify and define the exact field of interest of the current doctoral thesis, a functional block diagram of the modern FEC for traction applications was proposed by the author (Fig. 3). The front-end converter could be logically divided into four stages: power electronics stage, power interface stage, signal transmission stage, control and communication stage. The latter three stages are related to the control system. Thus, they are directly associated with the topic of this thesis. The power electronics stage, which in principle includes the hardware of the converter, is the topic of another doctoral thesis.

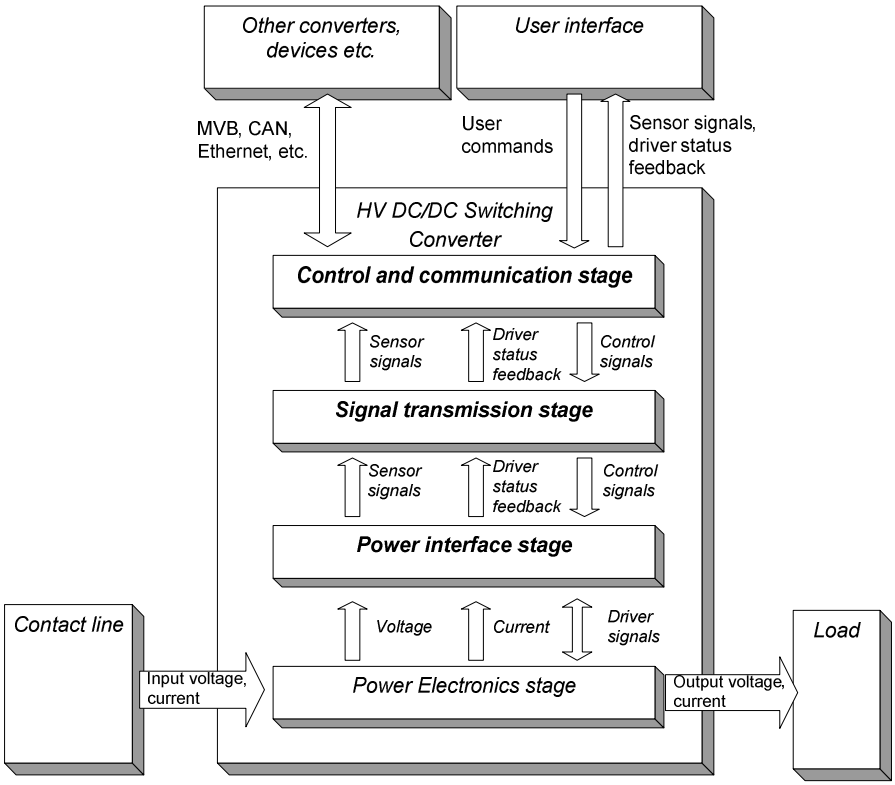

Fig. 3 Energy and data flow block diagram of a modern front-end converter for traction applications

The power interface stage includes sensors and IGBT drivers. In this section mainly different type sensors and IGBT drivers are studied. Important issues are isolation classes and suitability for HV applications like rolling stock. The signal transmission stage concentrates on different signal transmission possibilities. Here the most important properties are the immunity against electromagnetic interferences and also isolation capability. The control and communication stage is responsible for all control actions of the converter. It is the most sophisticated part of the control system and also the main research area of the thesis. The main topics of interest are: control algorithms for HB isolated DC/DC converters, protection and diagnostic functions of modern front-end converters, communication possibilities with external devices.

Current doctoral project was launched in 2006 with an Enterprise Estonia supported contract “Power converters for onboard equipment of electrical transport”. The aim was to develop basic solutions and methods for a new generation power converter based on the innovative high voltage (HV) IGBTs. In 2008 the university financial support BF110 to the project was received and the work was continued until 2009 when the final results were received. The research project was also supported by the two grants G7425 and G8020. The results of this project will be used to prepare and conduct a production development project in Estel Elektro Ltd. in the near future.

Thesis Objectives

The general objective of the doctoral work is to develop and build a state of the art control system that ensures efficient and reliable operation of the front-end converter for traction applications according to user requirements and specific railway norms.

The main research tasks to be achieved are as follows:

1. analysis and classification of user requirements and corresponding railway norms to formulate tasks the control system has to fulfill;
2. research and analysis of recent technologies and development trends used in similar converters and their control systems to develop new state of the art control system;
3. analysis and classification of control algorithms for two- and three-level half-bridge converters to obtain the optimal algorithm for reliable and efficient operation of the FEC;
4. analysis of two- and three-level half-bridge topologies and their implementation possibilities for traction applications;
5. analyses and classification of modulation methods and soft switching techniques for two- and three-level half-bridge isolated DC/DC converters;
6. simulation and testing of different modulation methods to increase the efficiency of the converter and optimize utilization of the components;

7. research of the capacitor-related volt-second unbalance problem (typical issue for half-bridge converters) and analysis of resulting limitations for the FEC;
8. development of computer models to simulate and analyze different control algorithms for half-bridge isolated DC/DC converters;
9. design and development of the control system of the front-end converter for traction applications based on the recent technologies and development trends;
10. elaboration of design guidelines and recommendations;
11. practical verification of the simulation and analysis results on the test prototype;
12. elaboration of proposals for postdoctoral studies.

Scientific novelty

The scientific novelty of the current work involves following:

1. analyses and systematization of the recent state of the art trends and technologies for the FEC for traction applications (on the page 39);
2. classification and comparison of conventional control algorithms for DC/DC converters with the emphases on suitability for digital control systems (Chapter 1.4.3);
3. classification of control algorithms for two- or three-level half-bridge topologies with respect to the chosen modulation method (Fig. 1.14);
4. development of a new control algorithm to solve the volt-second unbalance problem related to the peak current mode control (improved digital peak current mode control algorithm on the page 61);
5. development of a new control method to solve the quantization problem related to the digital average current mode control (improved digital average current mode control on the page 64);
6. classification and systematisation of performance requirements for the specific FEC to design appropriate control system (Chapter 1.1);
7. classification of energy and data flows of the modern FEC for traction applications (Fig. 3);
8. comparative analysis and evaluation of modulation methods and soft switching techniques without additional components for two- and three-level half-bridge isolated DC/DC converters (Chapters 2.2.1 and 2.3.1);

9. general analysis of the capacitor-related volt-second unbalance problems typical for the half-bridge isolated DC/DC converters (Chapter 2.2.3);
10. proposal of new control methods (shoot-through PWM and shoot-through PSM) for the state of the art quasi-z-source based isolated DC/DC converter (Chapter 4.1).

Practical novelty

The practical novelties of the thesis are as follows:

1. design and development of the state of the art control system for the HP (P>20 kW) and HV (U>2 kV) FEC for traction applications based on two-level half-bridge topology;
2. design and development of the state of the art control system for the HP (P>20 kW) and HV (U>2 kV) FEC for traction applications based on three-level half-bridge topology;
3. comparative analysis and evaluation of modern control units to find out the optimal controller for the FEC (Chapter 3.3.3);
4. development and evaluation of dead time generation circuits suitable for two- or three-level half-bridge topologies to provide second level hardware based protection against software errors (Fig. 3.12);
5. development and implementation of the concept of the control signal multiplication to reduce the controller load and to adapt the control system for both two- and three-level half-bridge converters (page 107);
6. development and implementation of an advanced control algorithm to stabilize the output voltage of the FEC in combined regulation conditions (Chapter 3.3.8);
7. investigation and usage of modern HV IGBT driver status feedback signals to speed up error identification and increase the overall reliability of the converter. An interrupt based method was developed to measure status feedback signals with a modern controller (page 124);
8. development of the diagnostic and communication interface with online and offline monitoring mode together with data storage and exchange possibilities. The integrated logger allows to make long term measurements with user adjustable time step (page 118);
9. development of the fault detection and classification algorithm. (page 125);

10. development of computer models of the FEC that enable testing of different control algorithms and prediction of the behaviour of the system in various failure situations (Chapters 2.2.4 and 2.3.2);
11. recommendations and guidelines for design of the control system of the FEC for traction applications (Chapters 1.5 and 3.3.10);
12. two Estonian Utility Model Certificates “Rolling stock HV APS” (EE00687U1) and “Rolling stock HV APS with improved power density” (EE00824U1).

Direct practical output of the thesis

As a result of this doctoral project control system for the FEC for traction applications was designed, assembled and tested. Totally was developed seven printed circuit boards and one IGBT driver board. Design guidelines of the control system were elaborated for Estonian company Estel Elektro Ltd.

Significance for worldwide science and technology development

In the doctoral project first 6.5 kV IGBT modules (FZ200R65KF1) were implemented and tested on a real converter. A detailed report with problems and general improvement suggestions was sent to the producer company EUPEC, Infineon. The feedback led to the development of the second improved edition of the IGBT modules (FZ200R65KF2).

The Infineon Power Simulation program IPOSIM was used to calculate switching losses and estimate maximum switching frequency for the IGBTs. The program suffered under lack of modulation methods and inverter types, which was also reported to Infineon. The feedback was taken into account by the development of the next version of the program.

A valuable feedback was also provided about IXYS fast recovery diodes used in the output stage of the converter.

Dissemination of results and publications

The author has over 30 international scientific publications, 20 of those are directly connected to the topic of the doctoral research. 8 papers connected to the thesis are published in the Institute of Electrical and Electronics Engineers database (IEEE *Xplore*) and 2 papers are published in peer-reviewed International Scientific Journals (Scientific Journal of Riga Technical University and Electrical Engineering Research Report). The results have been presented and discussed in different international conferences all over Europe (Portugal, Spain, Slovenia, Greece, Italy, Poland, Lithuania, and Latvia). The author was granted two Estonian Utility Model Certificates (EE00824U1 and EE00687U1) for the design of the proposed system.

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Tallinn Indrek Roasto
December, 2009

ABBREVIATIONS

ADC – analogue to digital converter
A/D – analogue to digital
APS – auxiliary power supply
AVCMC – average current mode control
CMC – current mode control
DC/DC – direct current
DSP – digital signal protcessor
DSC – digital signal controller
EMC – electromagnetic compatibility
EMI – electromagnetic interference
FEC – front-end converter
FOL – fiber optic link
FPGA – field programmable gate array
GPT – general purpose timer
qZSI – quasi-z-source inverter
HB – half-bridge
HP – high power
HV – high voltage
IGBT – isolated gate bipolar transistor
I/O – input/output
ISR – interrupt service routine
MC – microcontroller
NPC – neutral point clamped
PCB – printed circuit board
PLC – programmable logic controller
PSM – phase shift modulation
PWM – pulse width modulation
RMS – root-mean-square value
STI – surface transfer impedance
VMC – voltage mode control
ZCS – zero current switching
ZVS – zero voltage switching

SYMBOLS

D	duty cycle
D_{max}	maximum duty cycle
D_{min}	minimum duty cycle
D_{TB}	duty cycle of the bottom transistor
D_{TT}	duty cycle of the top transistor
f_{sw}	switching or operating frequency
I_{in}	input current of the front-end converter
I_{out}	output current of the front-end converter
$I_{Tr\text{-}p}$	primary current of the transformer
$I_{Tr\text{-}p\text{-}av}$	rectified average primary current of transformer
I_{Tx}	corresponding IGBT current (x=1…4)
n	turns ratio of the transformer
P_{out}	output active power
P_{Tr}	active power of the isolation transformer
T	temperature
T_T	transistor temperature
T_{rec}	rectifier temperature
T_{Tr}	transformer temperature
t_d	dead time
$t_{d\text{-}min}$	minimum dead time requirement
t_{off}	off-state time of the transistor
$t_{off\text{-}max}$	maximal off-state time of the transistor
$t_{off\text{-}min}$	minimal off-state time of the transistor
t_{on}	on-state time of the transistor
$t_{on\text{-}B}$	on-state time of the bottom transistor
$t_{on\text{-}max}$	maximal on-state time of the transistor
$t_{on\text{-}min}$	minimal on-state time of the transistor
$t_{on\text{-}T}$	on-state time of the top transistor
T_{pwm}	PWM period
U_{c2}	voltage of the input capacitor
$U_{CE\text{-}Tx}$	collector-emitter voltage of corresponding IGBT (x =1…4)
U_{cp}	compare value
U_{in}	input voltage of the front-end converter
$U_{in\text{-}max}$	long-term maximum input voltage
$U_{in\text{-}min}$	long-term minimum input voltage
U_{line}	catenary voltage
$U_{n\text{-}in,}$	nominal input voltage of the front-end converter
$U_{n\text{-}out}$	nominal output voltage of the front-end converter
U_{out}	output voltage
U_{ramp}	amplitude of a saw-tooth signal
U_{ref}	reference voltage in the control loops
$U_{Tr\text{-}p}$	amplitude of the transformer primary voltage
$U_{Tr\text{-}p\text{-}av}$	rectified average primary voltage of transformer
$U_{Tr\text{-}p\text{-}rms}$	rms value of the transformer primary voltage
$U_{Tr\text{-}s}$	amplitude of the transformer secondary voltage

1. STATE OF THE ART

1.1 Classification of Performance Requirements

The requirements for a FEC to be used in rolling stock can be divided into two groups (Fig. 1.1): those of the end-user and specific railway limitations. The end-user requirements are always connected to a better price-quality ratio, while the specific railway limitations are directly based on railway standards. The control system of the FEC must comply with the following end-user requirements: cost efficiency, reliability, easy maintainability, improved dynamic performance, flexible diagnostic and communication interface, and parameter stability.

The most important requirement from a user's point of view is a price/quality relationship. It means that the FEC must be reliable and with a competitive price. Maintenance costs must remain minimal. Thus, easy maintainability is required. The output voltage must be stable while load and input voltage of the converter are variable. The required output voltage range is typically 350 V ± 5 %. A diagnostic and communication interface is required to transmit operational data of the FEC to a personal computer for further analyses and diagnostics or to observe and make adjustments to the control system.

Specific railway standards are generally divided into six groups (Fig. 1.1). Output voltage levels of a static converter like the FEC for traction applications are defined by the standard EN50155. A stabilized output voltage must not exceed the following limits:

$$0.9U_{\mathrm{n-out}} \le U_{\mathrm{n-out}} \le 1.1U_{\mathrm{n-out}}, \quad (1)$$

where $U_{\mathrm{n\text{-}out}}$ is the nominal output voltage [3]. In the current case the end-user requirements are even higher than those of the railway standards.

Supply voltage levels of traction systems are specified in the European standard EN 50163, which defines following values: nominal voltage 3000 V, the lowest permanent voltage 2000 V, the highest non-permanent voltage 3900 V. In Estonia voltage values are based on old Soviet GOST standards, which define the catenary voltage range U_{line}=2400 V…4000 V. In view of the worst case measurement result, the following design requirement for the FEC could be defined: nominal voltage 3300 V, lowest permanent voltage 2200 V, and highest non-permanent voltage 4000 V [4].

In accordance with the standard EN50124-1 and the maximal operating voltage levels, insulation classes can be specified. All the components in the converter input should have the rated insulation voltage at least 15 kV. Low voltage output circuits that are galvanically isolated from the high voltage input should have the rated insulation 2.5 kV [5].

Electromagnetic compatibility requirements, test conditions and allowed interference levels are defined by the standard EN50121-3-2. The equipment should work failure-free in its local electromagnetic environment and without introducing intolerable electromagnetic disturbances by itself [6].

Maintainability requirements are specified in the standard EN50155. In general, maintenance includes the following actions: cleaning, repair, diagnostic tests and electrical insulation tests. Accordingly, the equipment should be designed such that regular maintenance would not be necessary. However, the equipment should include built-in diagnostic and status acknowledgement or indication functions, the system should have modular structure to allow easy testing and replacement of malfunctioning parts.

The FEC control system should be mechanically rugged for reliable operation under very harsh field conditions; the construction should ensure immunity against shock, vibration, dust, moisture, and humidity. The control system must operate in surrounding air temperatures ranging from -40 °C to +70 °C and humidity up to 95 % [3].

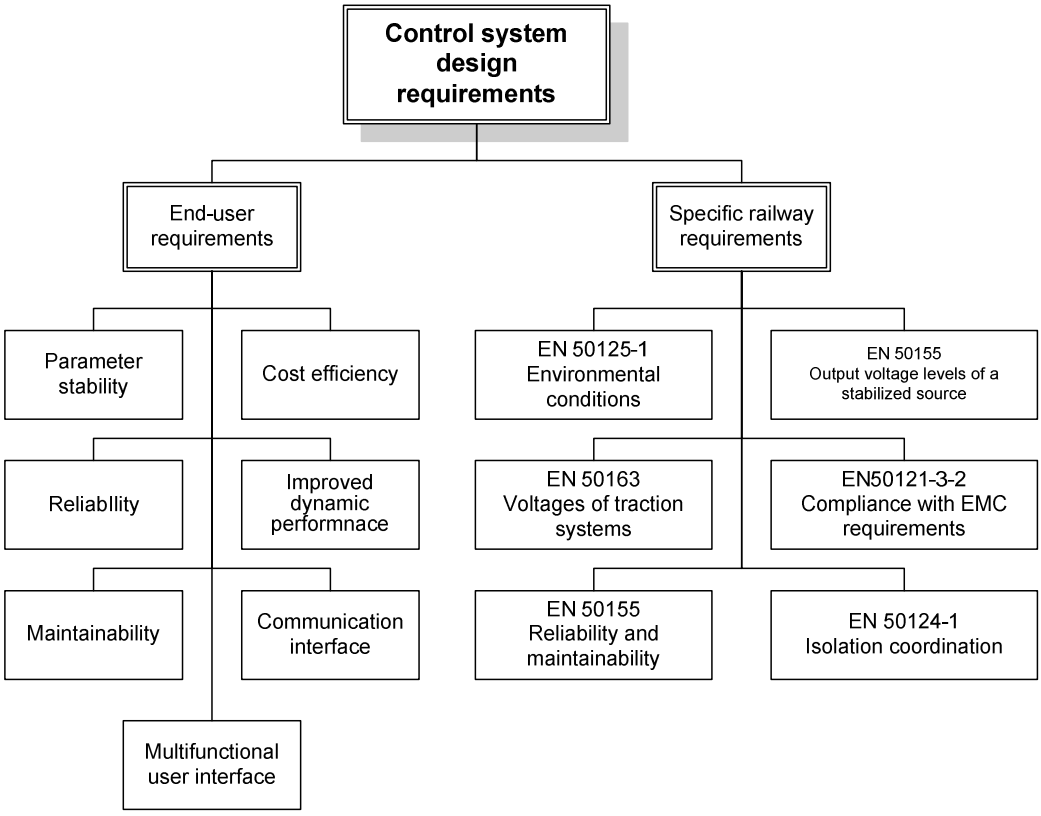


Fig. 1.1 Classification of performance requirements for the control system of the FEC for traction applications

The main functions of the traction FEC are the line regulation, the load regulation and the load transient response. Line regulation is defined as an ability of power supply to provide a stable output voltage under the conditions of changing input voltage. The second demanding function of the FEC for traction applications is the load regulation, which defines the maximum

deviation of the output voltage from its nominal value. A typical FEC for traction applications has to fulfill the combined regulation requirements, i.e. to provide a stable output voltage under the conditions of changing input voltage and load. It is the combined regulation that distinguishes the FEC for traction applications from other power supplies and makes the control of such a system one challenging task.

1.2 Power Interface Stage

Power interface stage (Fig. 3) is the part of the control system of the FEC that includes measurement equipment (sensors, transducers etc.) and IGBT drivers. Since it is the only part which directly gets into contact with the power electronics stage and HV components, emphasis here lies in sufficient isolation and HV capability.

Measurement equipment

The performance of the control system is directly affected by the choice of the measurement devices. The selection of a measurement device is the result of a technical and economic trade-off, considering the measurement equipment as well as the associated subsystems. All aspects of an application must therefore be taken into account. General demands for the measurement equipment to be used in the rolling stock FEC are:

- short-term insulation up to 15 kV;
- high level of noise immunity;
- good linearity;
- low thermal drift;
- wide supply voltage range;
- immunity against vibration and shock;
- cost efficiency;
- wide temperature range;
- compact size and low weight.

General requirements for the measurement equipment to be used in a control system are: high accuracy, fast response time, and wide bandwidth. In the current case the following parameters need to be measured: DC voltage, DC current, and high frequency pulse current. The classification of voltage and current measurement techniques is shown in Fig. 1.2. Two main groups can be distinguished: isolated and non-isolated. As a rule, the non-isolated measurement techniques (current shunt and voltage divider) are the simplest and most accurate but they usually have a high thermal drift, large size, high power consumption and most importantly they do not fulfil the insulation requirement of the rolling stock [7][8][9][10].

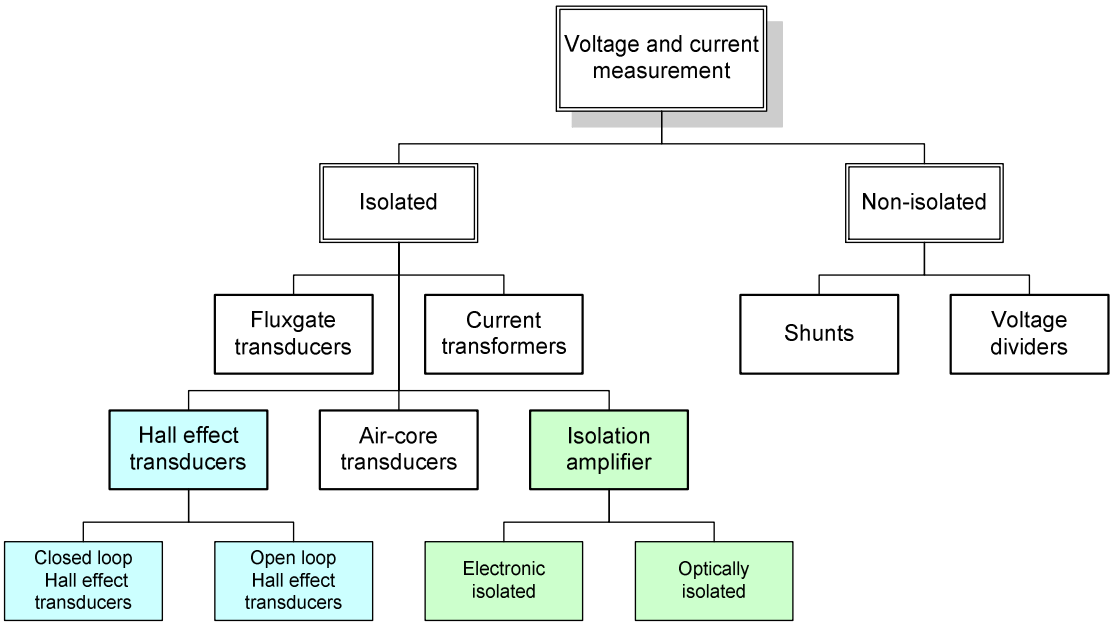


Fig. 1.2 Classification of current and voltage measurement devices

It is relatively easy to implement a current transformer. It acts just like a traditional voltage transformer, but typically has only one primary winding (the wire carrying the current to be measured). Unlike a conventional voltage transformer, there is no physical connection made to the measured line. The current transformer uses magnetic fields generated by the AC current flowing through the primary wire to induce a secondary current. Current transformers are simple to use, a low-cost solution that provides also good isolation. However, the main drawbacks are large size, weight and ability to measure only AC signals [11][12].

Very attractive measurement equipment for railway applications is Hall effect transducers. They can be divided into two groups: open and closed loop transducers. Open loop Hall effect technology could be used for current measurement, while closed loop Hall effect transducers can measure both: voltage and current. The inherent advantages of Hall effect transducers are small weight and size, isolated output signal, high overload capability and high reliability. In addition, measurement of all waveforms, alternating, direct and impulse current is possible [13][14].

Open loop Hall effect transducers consist of a magnetic circuit with an air gap (Fig. 1.3). Magnetic flux (B) created by primary current (I_{pr}) is measured in the air gap by a Hall effect sensor (H). The output voltage (U_{out}) of the Hall device is an exact representation of the primary current and can be easily measured [13].

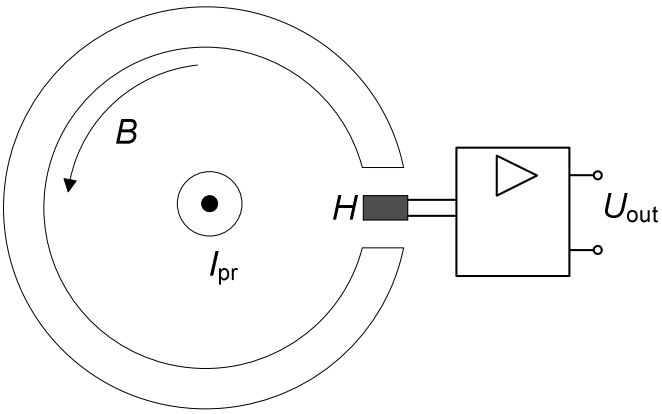


Fig. 1.3 Operation principle of an open loop Hall effect transducer

Closed loop Hall effect transducers consist of a magnetic circuit with an air gap and a secondary winding (Fig. 1.4). Primary current creates a magnetic flux (B) in the magnetic circuit. A Hall device and associated control electronic balances that flux with a complementary flux by driving current (I_{sec}) in the secondary winding. The secondary current is an exact representation of the primary current [13].

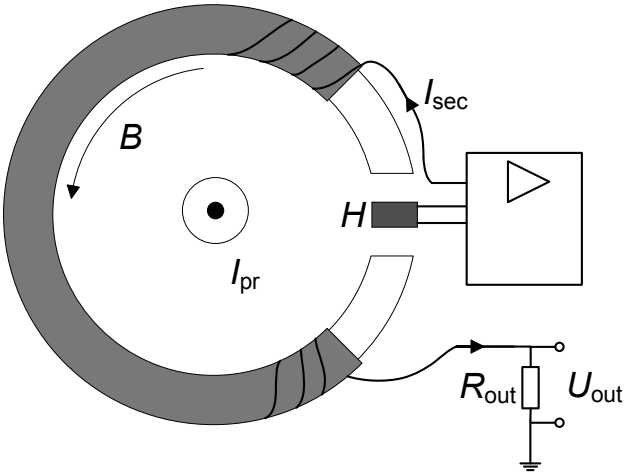


Fig. 1.4 Operation principle of a closed loop Hall effect transducer

Open loop Hall effect current transducers have low power consumption, and galvanically isolated output, they are cheaper and more compact than closed loop ones. However, the response time, frequency range and overall accuracy are smaller compared to closed loop Hall effect transducers. The benefits of closed-loop current transducers are a low temperature drift, excellent linearity, fast response time, good accuracy and wide band width [15].

An isolation amplifier could also be used for voltage measurement. The overall accuracy and linearity are slightly better compared to Hall effect transducers. They provide high immunity against electromagnetic interference (EMI) and galvanic isolation up to 15 kV. Until recently the maximal

measurement range reached only about 3.5 kV and isolation amplifiers were insufficient for many HV traction applications. However, the newest models of isolation amplifiers can measure voltages up to 6 kV, which makes them a good competitor for Hall effect transducers [14]. Isolation amplifiers can be divided into two groups (Fig. 1.2): electronically isolated and optically isolated. The main advantage of this technology is the small size and light weight. Similarly to closed loop Hall effect transducers, any kind of signal can be measured. The limitations compared to closed loop Hall effect transducers are: slower response time, higher power consumption, they are unsuitable for current measurement and have lower insulation capability [16]-[19].

Air-core (Rogowski effect) transducers have toroidal structure, but with a coil wrapped on a non-magnetic core (Rogowski coil) and its structure can be either rigid or flexible. The coil is magnetically coupled with the flux created by the current to be measured. A voltage is induced on the coil proportional to the derivative of flux and thus proportional to the derivative of the current to be measured. The main benefit of air-core transducers is lightweight measuring head, which can be positioned away from the measurement electronics. The main drawback is that it is only suitable for AC current measurement [15][20].

Fluxgate transducers can be used both: for current and voltage measurement. Any kind of signals (AC, DC, impulse, etc.) can be measured. The working principle and construction are similar to the closed loop Hall effect transducer. A magnetic circuit including a gap and secondary winding is used. The secondary winding is driven to balance the flux in the gap. The main difference between the closed loop Hall technology and the Fluxgate is on the way the air gap field is detected. Fluxgate technology uses a saturable inductor instead of Hall sensor. Benefits of fluxgate technology are: excellent accuracy, low offset, excellent overcurrent recovery, high bandwidth, large dynamic range allowing measurement of both small and large currents, and small size. Drawbacks are: large noise level at the excitation frequency, relatively complex technology, and price [21]-[23].

A comparison between most common and widely used current and voltage measurement methods is shown in Table 2. Considering the information given previously three measurement methods are most suitable for the current application: Hall effect transducer, isolation amplifier, and fluxgate transducer. Fluxgate transducers are extremely accurate and stable but also complex and expensive. In the current case, no high precision measurements are needed. Isolation amplifiers, except some new generation and expensive models on the market, are slow, have limited insulation and can not measure sufficiently high voltages. According to general demands for the measurement equipment to be used in the FEC for traction applications the closed loop Hall effect transducer is the most convenient solution.

Table 2 Comparison of current/voltage measurement methods

Parameter	Current transformer	Hall effect transducer	Isolation amplifier	Air-core transducer	Fluxgate transducer
AC/DC measure	AC	AC/DC	AC/DC	AC	AC/DC
Bandwidth	Low	Middle	Low	Middle	High
Isolation	Very high	High	Middle	Very High	High
Linearity	High	Middle	Middle	High	Very high
Accuracy	Middle	Middle	Middle	Middle	Very high
Offset	No	Yes	Yes	No	No
Response time	High	Middle	Low	Middle	Very high
Saturation effect	Yes	Yes	No	No	No
Temperature dependence	Low	High	High	Very low	Low
Power consumption	Low	Low	Middle	Low	Low
Weight	High	Middle	Small	Very small	Middle

Control Principles and Requirements for High Voltage IGBTs

The HV IGBTs have been established as dominant power semiconductors. In this work HV IGBT are defined as transistors with the collector-emitter voltage greater than 1.7 kV e.g. 2.5 kV, 3.3 kV, and 6.5 kV. Drivers for such IGBTs are subject of high requirements. The most important requirements to be fulfilled can be summarized briefly as follows [24]:

- properly selected gate resistor;
- galvanic isolation between IGBT and control electronics (at least 15 kV);
- isolated power supply;
- small signal propagation delay;
- appropriate output power level;
- short-circuit detection and protection;
- overcurrent protection;
- supply undervoltage protection;
- status and diagnostics functions;
- small size and weight.

An IGBT module is a sophisticated switching unit. Due to the high voltages and currents the IGBT must be isolated from the control system. It requires bipolar gate signal to properly switch between on and off states. The gate peak current can reach up to 20 A. Thus, IGBTs can not be directly driven with a microcontroller. A specially designed IGBT driver is needed. In addition, state of the art IGBT drivers also include several protection and status acknowledgment functions, which increase the overall reliability of a converter system. In general, drivers for high-voltage IGBTs are available in two realizations: driver cores and plug&play drivers. Driver cores are modules equipped with all essential functions of a driver, such as electrical separation, protective functions, DC/DC converters etc. The user can configure the driver according to the need using some external hardware. Plug&play drivers are fully adjusted to a specific IGBT module including all functions needed for proper operation. Thus, driver cores offer a great flexibility, while plug&play drivers considerably reduce development time and effort [25][26].

When developing a control program for an IGBT based converter the most important parameters to consider are IGBT switching time and control signal propagation delay. A fast driver with a short delay introduces significantly less phase lag into the converter control loop. The IGBT switching time is controlled by charging and discharging the gate capacitor of the IGBT. If the gate peak current is increased, the turn-on and turn-off time will be shorter and the switching losses reduced. This obviously has an impact on other switching parameters such as overvoltage stress, short-circuit safe operation area, EMI etc. The gate charge currents can be controlled by the gate resistor. Thus, the gate resistor must be chosen carefully and the resulting behaviour of the IGBT must be taken into account in the control program. Parameters that depend on the gate resistor are shown in Table 3 [27]-[30]. As can be seen, a rise of the gate resistance increases the turn-on time, turn-off time, switching energy per pulse, surge voltage sensitivity, and short-circuit withstand capability. At the same time it decreases turn-on and turn-off peak currents. Forward characteristics of the IGBT remain unchanged.

Table 3 IGBT parameters that are depending on gate resistor

Rating/characteristic	**Rise of gate resistance**
Turn-on time	Rises
Turn-on energy per pulse	Rises
Turn-off time	Rises
Turn-off energy per pulse	Rises
Turn-on peak current	Falls
Turn-off peak voltage	Falls
Surge voltage sensitivity for IGBTs	Rises
Short-circuits withstand capability	Rises
Forward characteristics	Remain

1.3 Signal Transmission Stage

The signal transmission stage is a link between control and communication stage and power interface stage, as shown in Fig. . It represents different signal transmission possibilities. Since the power interface stage includes components which deal with high voltages and currents and the control and communication stage includes only low voltage electronic components, it is vital to have good isolation between those two stages. The signals in the signal transmission stage can be divided into three groups: sensor, control and driver status feedback signals. It is also important to distinguish between digital and analog signals since they should be transmitted differently. Sensor signals are analog signals generated by current and voltage transducers. Control signals for the switches, usually pulse width modulated signals, are digital signals generated by the microcontroller. Driver status feedback signals are digital signals generated by the IGBT driver. The easiest and cheapest way to transmit any signal is through copper wires. However, it provides no isolation. There are several alternatives available for the potential isolation, as shown in Table 4 [30].

Table 4 Potential isolation techniques

	Inductive	**Optical**	
Device	Isolation transformer	Optocoupler	Fiber optic link
Insulation	>1700 V	<1700 V	>1700 V
Surge voltage immunity	High	Low	High
Cost	Medium	Low	Medium

In addition to insulation, electromagnetic compatibility aspects have to be taken into account especially for control of power switches. The overall performance of the converter depends on the switches (IGBTs, MOSFETs etc). Even a small fault in the control pulse can have catastrophic results. Using copper wires with an isolation transformer provides the needed isolation, but the length of transmission lines is strictly limited to 0.5 m due to the impact of EMI. Optocouplers and copper wires do not offer sufficient isolation and also suffer under strong EMI impact. A fiber optic cable is immune against EMI and has the desired isolation class, which makes it the best solution for digital signal transfer in the front-end converter for traction applications [31]. Unfortunately, it is not suitable for analogue signals since the optical transmitters and receivers are mostly designed for digital signals. Therefore sensor signals will be mostly transferred through copper wires. In the case of Hall effect transducers the isolation is not a problem since current and voltage transducers provide galvanic isolation between high power and low power part. However, all cables are subject to interference pickup. Basically there are four main types of interference coupling [32][33]:

1. capacitive coupling;
2. inductive coupling;

3. galvanic coupling;
4. electromagnetic radiation.

Typically an environment in traction applications includes HV and high current sources. Alternating HV sources emit electrostatic fields that cause capacitively coupled interferences. High current sources emit electromagnetic fields that interfere using inductive coupling. Major risks for sensor signals in traction applications are interferences with capacitive and inductive coupling. Capacitive coupling can be reduced by [34][35]:

- increasing distance between interfering circuits;
- keeping the wires as short as possible;
- avoiding parallel conduction of interfering signals;
- screening.

Inductive coupling can be reduced by:

- increasing the distance between conductors;
- mounting conductors close to conductive surfaces;
- keeping the wires as short as possible;
- avoiding parallel conduction of interfering signals;
- screening;
- using twisted pair cable, which effectively reduces the magnetic loop area.

Screening or shielding is helpful for both coupling types. In order to avoid ground loops commonly shielded cables will be grounded only on one end of the shield. The effectiveness of the shield depends on the surface transfer impedance (STI), which can be calculated as

$$Z_{\mathrm{T}} = \frac{dU}{dx} \cdot \frac{1}{I_{\mathrm{s}}}, \tag{2}$$

where dU/dx is the voltage drop cased by the shield current per shield unit length and I_{s} is the induced shield current. The smaller the STI the greater is the screening effect of the shield. STI depends on the following parameters [36]:

1. mutual inductance – shield to inner;
2. mutual capacitance – shield to inner;
3. leakage inductance – inner to external;
4. skin effect.

In general in the HP and HV DC/DC converters the signal cables of sensors should be kept as short as possible, preferable are twisted pair cables, and all cables should be shielded.

1.4 Control and Communication Stage

Control and communication stage (Fig. 3) is the brain of the control system. Physically it includes the control unit. In addition, this stage also deals with control algorithms, methods, diagnostic functions, and peripherals.

1.4.1 Main Trends in Control System Development

Twenty years ago analogue control circuits were dominant in power electronics. They remained cheap and simple compared to a digital controller required. Analogue circuits also give near infinite resolution, free parallel processing, and no computational time delay. However, with the technology developing rapidly, which are inevitably increasing requirements for a modern switching power supply. Reduced weight, volume, cost and increased reliability of circuitry are becoming increasingly important to DC/DC converter manufacturers. Corresponding analogue control circuits would be too complex and inflexible for such demanding requirements [37].

The past few years have seen substantial developments in the digital control of DC/DC converters. New low cost, high performance embedded digital signal processors (DSP) and microcontrollers (MC) are now available on the market. Digital controllers are provided with many integrated power electronic peripherals, such as analogue-to-digital converters (ADC), pulse width modulators (PWM), general purpose timers (GPT) etc. [38]-[40]. Therefore, digital control of switching power supplies is becoming more and more common in industry. Ultimately, the aim today is to apply a single chip digital controller that can fulfil all the requirements of a DC/DC converter. Main benefits of digital control compared to analogue are [41]-[45]:

- programmability;
- higher flexibility and modularity;
- fewer components;
- lower sensitivity to noise and environment conditions.

Main drawbacks of digital control that must be taken into account are:

- the time-consuming computations;
- A/D conversions slowing down the sampling rate of the controlled variable;
- limited resolution depending on the system clock frequency;
- finite lengths of variables resulting in a round off error.

1.4.2 Modular Embedded Control Units

Flexibility and reliability are the key issues in traction applications. Due to very rough environment conditions and performance requirements, a digital controller is advisable. Demands for the control unit are:

- high working frequency;
- operating temperature range -40 °C …+60 °C ;
- immunity against shock and vibration;
- reprogrammability ;
- flash memory for program code and data storage;
- real time clock module for long term measurements;
- GPT units;
- communication possibilities;
- PWM channels with timers;
- interrupt and trap functions including external interrupts;
- sufficient number of I/O lines;
- ADC;
- support of floating point calculations;
- optimal price.

Unfortunately, such high demands also require a powerful control unit, which can be quite expensive. Thus, the controller should be chosen carefully. In general, there are five types of digital control units that can be taken into consideration: field programmable gate array (FPGA), programmable logic controller (PLC), digital signal processor (DSP), microcontroller (MC), and digital signal controller (DSC). FPGAs are a form of highly configurable hardware. FPGAs contain thousands of programmable logic blocks, I/O modules and a hierarchy of reconfigurable interconnection network that allows the blocks to be connected together. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory. The main advantage of FPGAs is the support of parallel calculations. Therefore, the optimal applications for FPGAs are those that require high computational performance, e.g. telecommunication technology and audio technology. However, FPGAs have poor performance in handling sequential algorithms and floating point calculations. FPGAs are reprogrammable but it is quite a slow process and depends on the system complexity. Naturally FPGAs do not include any peripherals like Timers, PWM generators, ADC etc. That makes them unpractical for multilevel control systems where the controller also has to fulfil other higher level tasks besides

the main control algorithm, e.g. communicate with other devices, display sensor readouts etc. [46][47].

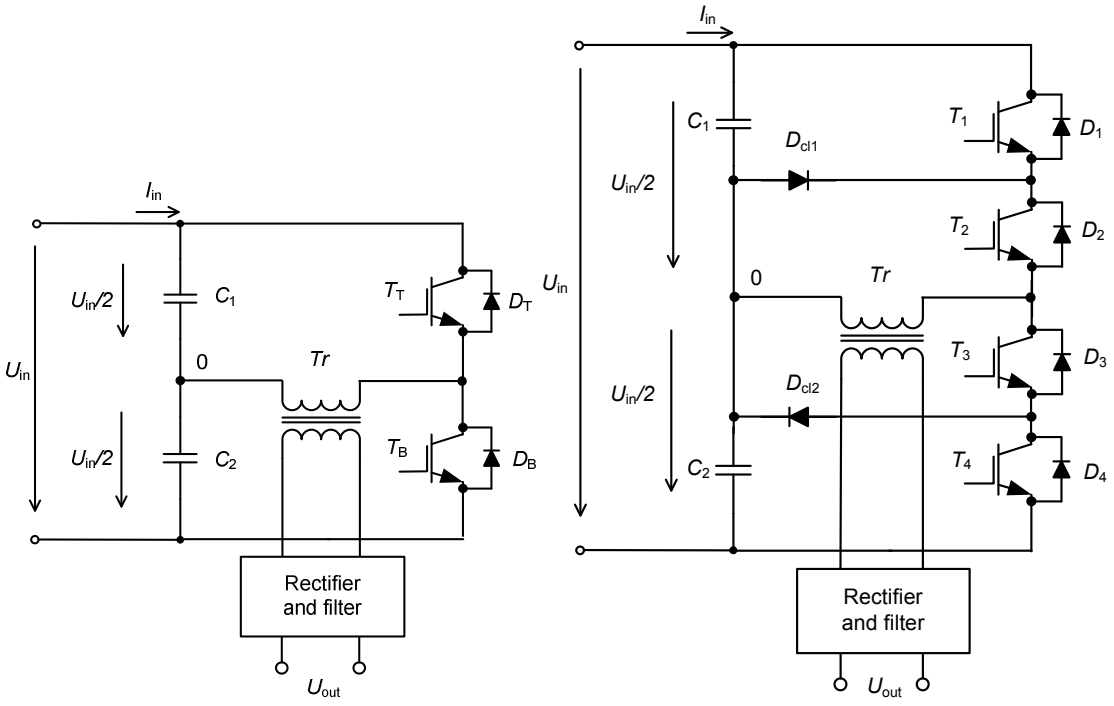
PLC is a digital controller specially developed for industrial applications. They are designed for multiple input and output arrangements, with extended temperature ranges, immune to electrical noise, and resistant to vibration and impact. Modern PLCs can be programmed in a variety of ways, from ladder logic to more traditional programming languages such as BASIC and C. However, the languages are simplified and have only limited functionality. PLCs have also their own operation system, which reduces the flexibility of the controller. In general, the emphasis lies more on speed and simplicity than on flexibility. PLCs are best suitable for standardized industrial processes, which are not very fast, nor complex and where changes to the system would be expected during its operational life.

DSPs are basically a specialized form of microcontrollers. DSPs are optimized for signal processing and computations, offering many architectural features to reduce the number of needed instructions. MCs, however, concentrate on performing control functions and handling algorithms. As such, a typical MC application involves many conditional operations, with frequent changes in the program flow. MC also has a larger variety of peripherals. In order to handle two tasks simultaneously, developers have tried to combine DSPs with MC technology. The most recent approach that has emerged incorporates MC functionality into a DSP. These new so-called digital signal controllers (DSC) exhibit a unified architecture and a flexible set of peripherals optimised not only for numeric computation, but also for control-oriented tasks [39][48][49]. For the current application, both: DSC and MC technologies are suitable. In order to find out the more optimal solution both digital control units should be tested and compared in more detail.

One possibility is also to combine several control units with each other. It is especially useful in complex control tasks where just one controller can not afford enough flexibility. Since this solution is also the most expensive one it should be avoided, if possible [50].

1.4.3 Modulation Methods and Control Algorithms

Two sub-topologies were considered, as shown in Fig. 1.5: two-level HB with 6.5 kV IGBTs and diode-clamped three-level HB with 3.3 kV IGBTs. The two-level HB is the simplest solution. It consists only of two transistors and input capacitors. One limitation of this topology is that the full input voltage is applied across each transistor. So the blocking capability of each IGBT must be greater than the input voltage.



(a) *(b)*

Fig. 1.5 Studied converter topologies: two-level half-bridge (a), three-level half-bridge (b)

The three-level topology can be easily derived from the two-level topology with four series connected transistors by the introduction of clamping diodes (D_{cl1}, D_{cl2}), which balance out voltage sharing between series connected top and bottom group transistors [51]. Here the required voltage blocking capability of each IGBT is only half of the input voltage.

Modulation Methods

Pulse width modulation (PWM) is the most common modulation method used to control switching-mode DC/DC converters. The output voltage is changed by varying the duty cycle.

$$D = \frac{t_{on}}{t_{off} + t_{on}} = \frac{t_{on}}{T_{pwm}}, \qquad (3)$$

where D is the duty cycle, t_{on} is the on-state time, t_{off} is off-state time, and T_{pwm} is the switching period.

In general, two PWM methods can be distinguished: fixed-frequency and variable-frequency PWM (Fig. 1.6). Fixed-frequency PWM is achieved by changing both t_{on} and t_{off} while maintaining a constant switching period, as shown in Fig. 1.6 (a).

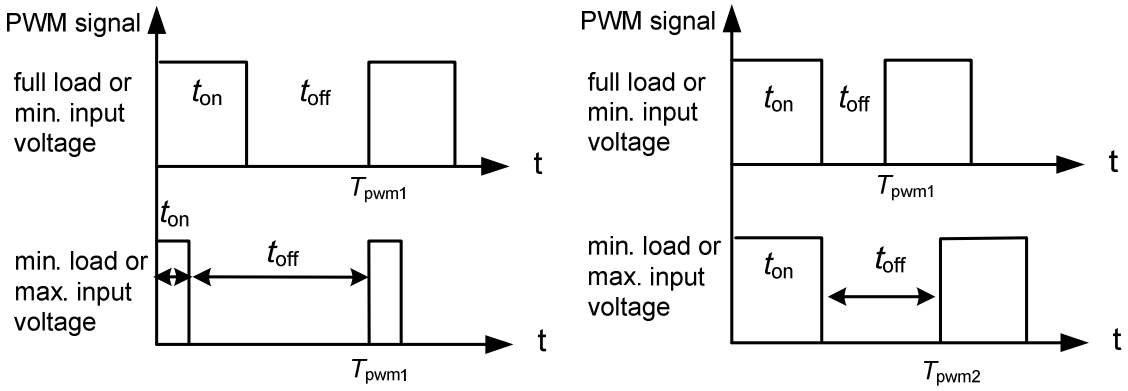


Fig. 1.6 PWM methods: fixed frequency (a) and variable frequency (b)

Variable-frequency PWM is achieved by changing t_{off} while keeping t_{on} constant or vice versa. The switching period is not fixed, thus the frequency is variable, as shown in Fig. 1.6 (b). An advantage of the variable frequency technique is that it reduces switching losses with the load-current increase. A major problem associated with the variable-frequency PWM is the unpredictable electromagnetic interference (EMI), which makes it unsuitable for demanding front-end converters of traction applications. The EMI of the fixed-frequency PWM can be easily filtered out [52][53].

Phase shift modulation (PSM) is a common modulation method for multilevel HB and full bridge DC/DC converters. The resulting output voltage is similar to PWM control but commutation timings of switches are different. The PSM modulation method can be also applied to three-level HB topology (Fig. 1.5). In PSM control, all switches operate with nearly 50% duty cycle, as shown in Fig. 1.7. The phase-shift between signals determines the operating duty cycle or the transformer voltage (U_{Tr}) of the converter. Here the frequency is always fixed [54]-[56].

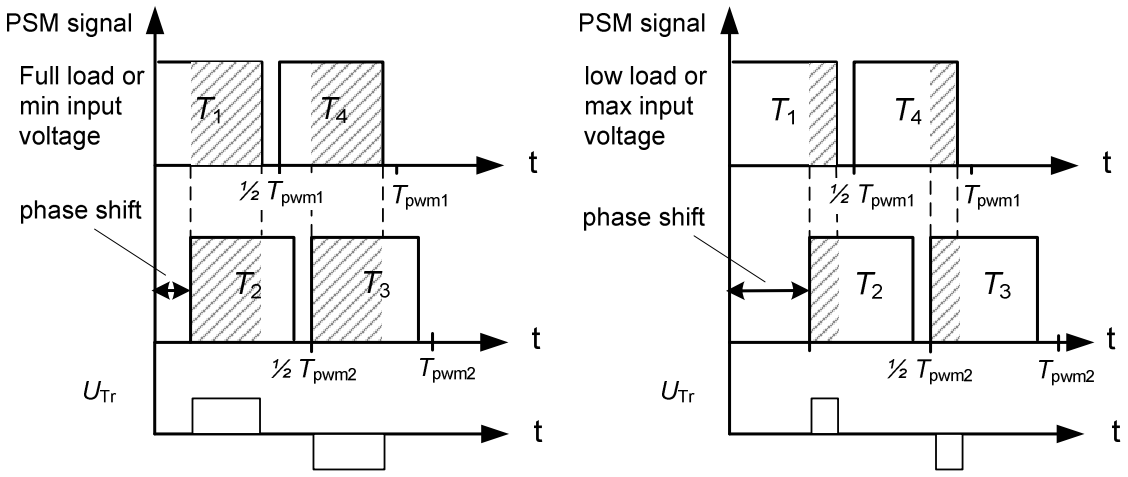


Fig. 1.7. PSM method for multilevel HB or full-bridge inverters: maximum duty cycle (a), minimum duty cycle (b)

Generally, for the two-level HB only the PWM method is applicable. In the case of three-level converter topology, both PSM and PWM can be applied. Both methods have benefits and drawbacks. Which of the methods to choose depends on many factors and will be discussed later in this work.

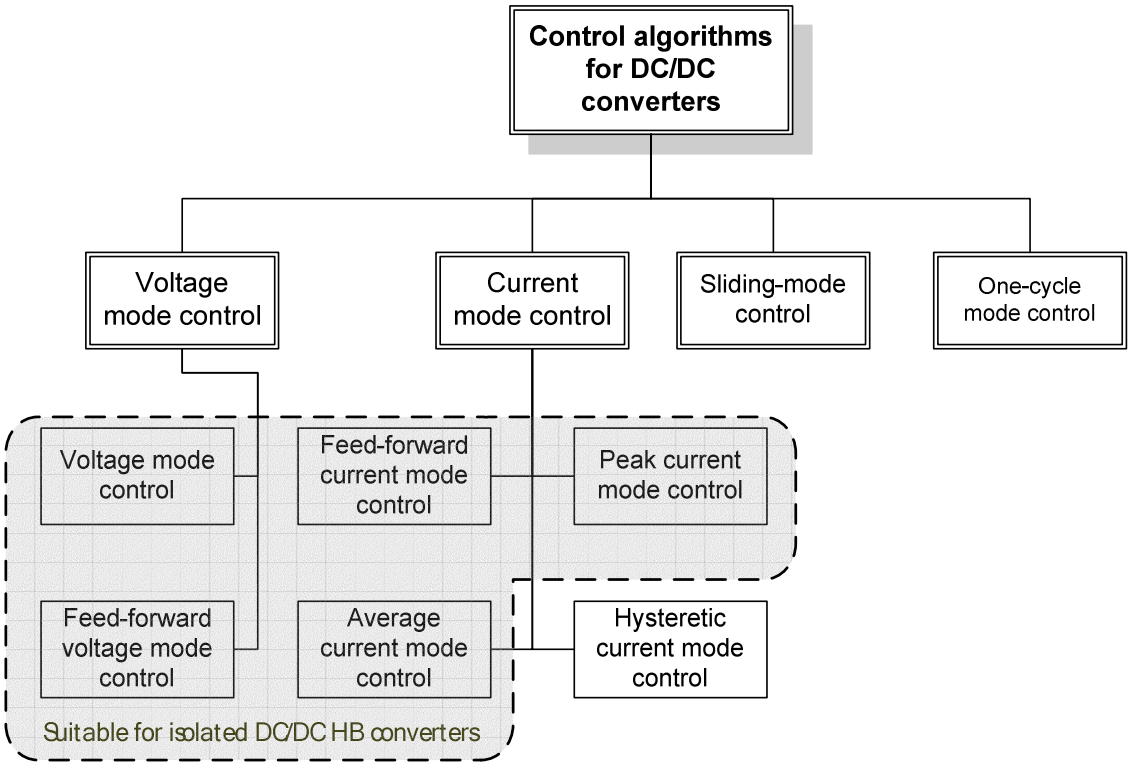


Fig. 1.8. Classification of control algorithms for DC/DC converters

Control algorithms

In general, control algorithms for isolated DC/DC converters can be divided into four main groups (Fig. 1.8): voltage mode control (VMC), current mode control (CMC), sliding-mode control, and one-cycle mode control. In order to find out, which algorithms of them are suitable for digitally controlled HB isolated DC/DC converters following comparative analysis was carried out.

VMC is a single loop control algorithm, mostly based on the fixed-frequency PWM control method although it is also used with PSM. A classical VMC algorithm consists of one voltage control loop, as shown in Fig. 1.9. The output voltage U_{out} is measured and compared to a reference value U_{ref}, the voltage error is sensed by the error amplifier (*EA*). The output of the regulator is coupled with the PWM stage. VMC is simple and can be easily implemented in a HB isolated DC/DC converter. However, suffers from poor line regulation and parallel operation [57]-[60].

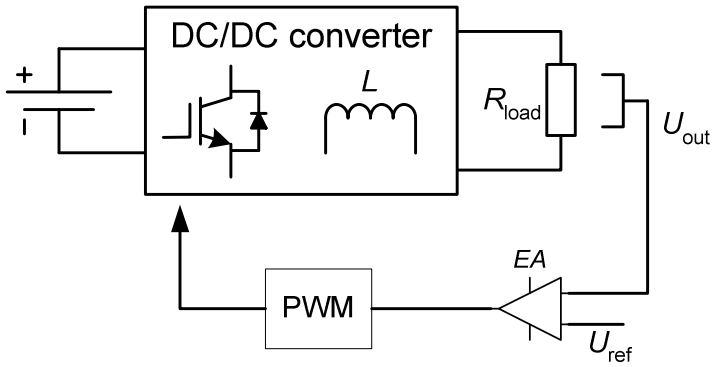


Fig. 1.9. Block diagram of the voltage mode control strategy

In the feed-forward voltage mode control, poor line regulation is somewhat improved, as shown in Fig. 1.10. The enhancement comes from the additional line voltage control loop. The ramp of the triangle waveform generator (G_1) will be changed proportional with the input voltage. The output voltage is sensed by an error amplifier *EA1*. The result is an instantaneous response to line voltage and load changes. Since it is difficult to change the ramp within a digital control unit, this method is less important for the digitally controlled HB. Another approach is to calculate the duty cycle in accordance with the input voltage. The transfer function of the converter is usually known. This algorithm is especially suitable for a digitally controlled HB. In general, feed-forward voltage mode control is inherently stable [61][62].

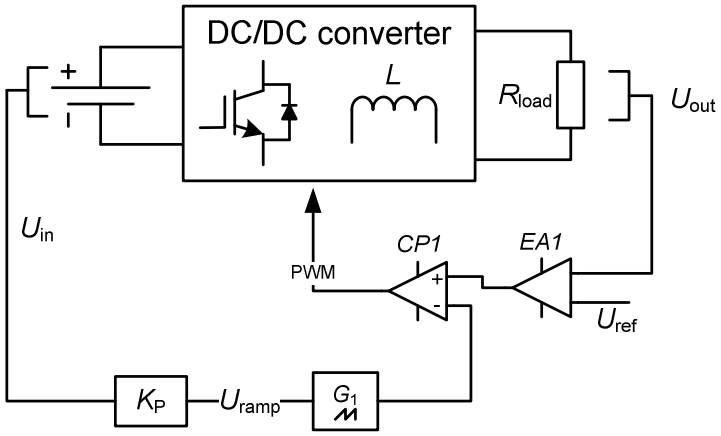


Fig. 1.10. Block diagram of the feed-forward voltage mode control strategy

CMC includes four sub-variations: peak, average, hysteretic, and feed-forward CMC, as indicated in Fig. 1.8. A simplified regulation loop of the peak current mode is presented in Fig. 1.11. It consists of two control loops, inner current and outer voltage control loop. The voltage control loop measures the output voltage (U_{out}) of the converter and an error amplifier *EA* programs the peak current value (I_{peak}) for the inner current loop. The inner current loop measures inductor or transformer current according to the topology used and compares it with the current program I_{peak}. Power switches of the DC/DC converter are turned on with a fixed-frequency clock signal and switched off by the comparator (*CP*) when the peak current value is reached. PWM output is

generated with a RS latch. The peak CMC algorithm can also be applied in HB isolated DC/DC converters. In that case transformer primary current is measured and two PWM signals are created. The peak current mode has a good input voltage response but suffers from pure noise immunity and volt-second unbalance problem, which aggravates its use in half-bridge PWM converters [43] [63]-[69].

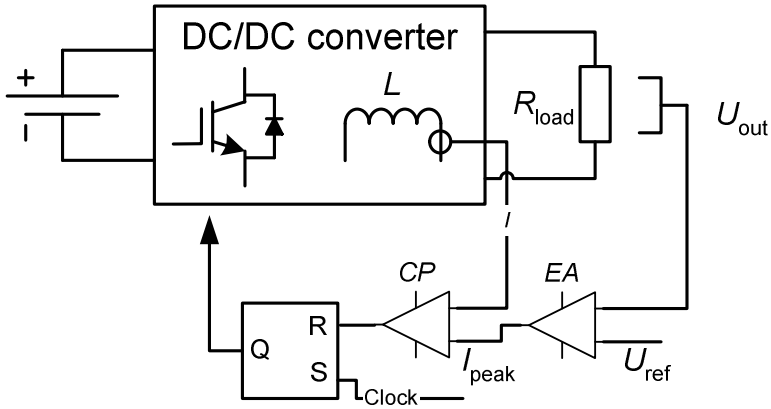


Fig. 1.11. Block diagram of the peak current mode control strategy

The average current mode control (AVCMC) overcomes most of the problems of the peak CMC. It consists of two control loops but instead of comparators a current error amplifier (*EA1*) is introduced, as shown in Fig. 1.12. Inductor or transformer current (*I*) is measured and integrated over the period. The average value then is compared to the current program (I_{av}), which is given by the outer voltage control loop. Instead of a RS latch that was used in peak CMC, here a PWM block is used to generate control signals for the transistors. The average CMC algorithm can be applied in HB isolated DC/DC converters. In that case the transformer primary current is rectified and passed through a low-pass filter. The average CMC has good noise immunity and high current loop gain due to the current error amplifier (Reg1) [42][70][71].

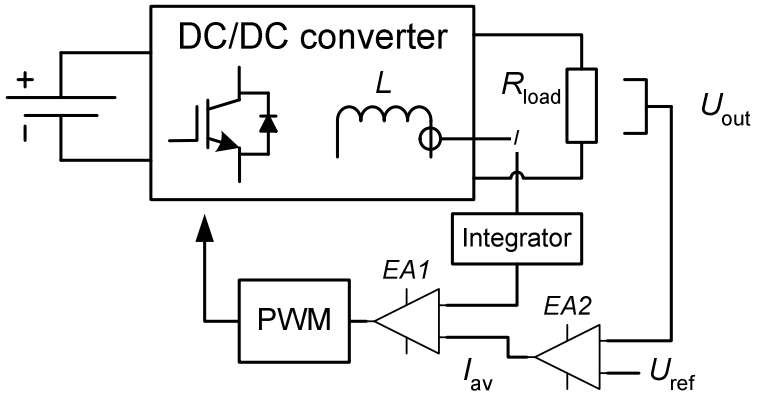


Fig. 1.12. Block diagram of the average current mode control strategy

Hysteretic CMC suits best for DC/DC converters with one switching element and continuous mode current. The inductor current waveform is used to control both the on-state and off-state time of the switch. The current is controlled between two limits. It is a variable frequency control algorithm, since the conducting and non-conducting periods of the power switch can change. Thus, also no-clock or timing function is needed [72]. Application of this algorithm in a half-bridge topology leads to some complications: the transformer primary current is AC and needs to be rectified, HB DC/DC converter is not working in a continuous conduction mode, instead of one switch there are two transistors, which drastically increase the complexity of the control loop. Therefore the application in HB isolated DC/DC converter is limited. A possible way of how to use it is presented in the patent [73]. In general, hysteretic CMC reacts fast to load and line transient, it is simple and it does not require loop compensation. The drawbacks are a wide operating frequency range and the requirement of high speed current measurements, which can cause difficulties especially in digital control systems [74].

Commonly the transfer function of a DC/DC converter is known. The output voltage can be calculated in terms of input voltage, duty cycle and transformer turns ratio. This idea is implemented in the feed-forward CMC. The voltage feed-forward can be added either to the current set point or in parallel with the current control loop. The feed-forward CMC can provide a faster transient response but needs higher calculation capability. Since CMC has inherently good input transient response then the feed-forward CMC is used rarely [75][76].

Sliding-mode control is a nonlinear control form of variable structure control. In nature it is very similar to the hysteretic CMC. The idea is to hold a controlled variable within two predefined boundaries called a sliding surface. The equilibrium point of the sliding surface is the desired operation point. Similar to hysteretic CMC, sliding-mode is a variable frequency control algorithm. However, unlike hysteretic CMC, sliding-mode control can also be implemented in a manner where there is a known upper limit on the switching frequency, as shown in Fig. 1.13. Inductor or transformer current (I) is measured and compared to the current program (I_{av}), which is given by the outer voltage control loop. A comparator with hysteresis (CP) is connected with D flip-flop, which is clocked with fixed frequency. The main benefits of sliding-mode control are stability, even for large supply and load variations, robustness, good dynamic response, and simple implementation in analogue electronics. Drawbacks are: variable switching frequency, high switching frequency requires very quick measurements, which makes it difficult to apply in the digital control. Sliding-mode control is best suitable for inverters with analogue control and sinusoidal output parameters. It is not an optimal solution for the HB isolated DC/DC converter where the voltages and currents are square wave shape [77]-[83].

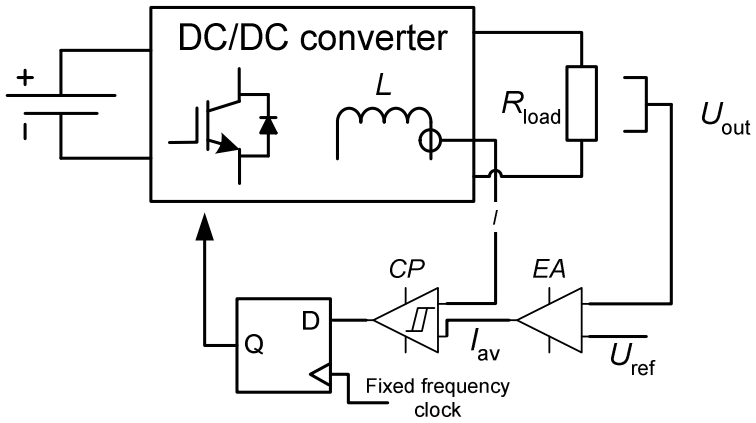


Fig. 1.13 Block diagram of the sliding-mode control strategy with the upper frequency limit

One-cycle mode control is a nonlinear control algorithm that is based on the integration of a switched variable (voltage or current) in order to force its average value to be equal to the control reference. The benefit of the one-cycle mode control is its ability to reject input disturbances in just one switching cycle. However, it is not easy to apply it in converters, which have more than one switch (e.g. converters based on HB topology) and it also suffers from poor dynamic behaviour in response to load variations. An external controller could solve the problem but the nonlinearity of the one-cycle mode control algorithm makes it quite difficult to design an external controller [84]-[86].

A classification of different control algorithms suitable for a multi-level HB isolated DC/DC converter is shown in Fig. 1.14. As it can be seen, control algorithms do not only depend on converter topology but also on the modulation method, chosen, e.g. peak CMC is not applicable in the case of PSM. On the other hand, if a variable frequency PWM control is required, the one-cycle mode control algorithm can not be applied. Therefore, the first step in control system design is to choose a converter topology and a modulation method and after that an appropriate control algorithm.

Many different integrated circuits are available to provide the current mode or VMC for switching-mode DC/DC converters. They are mostly used for such low power applications as power supplies for computers, monitors, printers, etc. [87]-[90]. The benefits of such integrated circuits are: easy to use, no development needed, and reduced costs. The main drawback is reduced flexibility. Thus, rigorous dynamic performance requirements and high level of complexity of the control system prevents the use of standardized integral circuits in the FEC for the rolling stock.

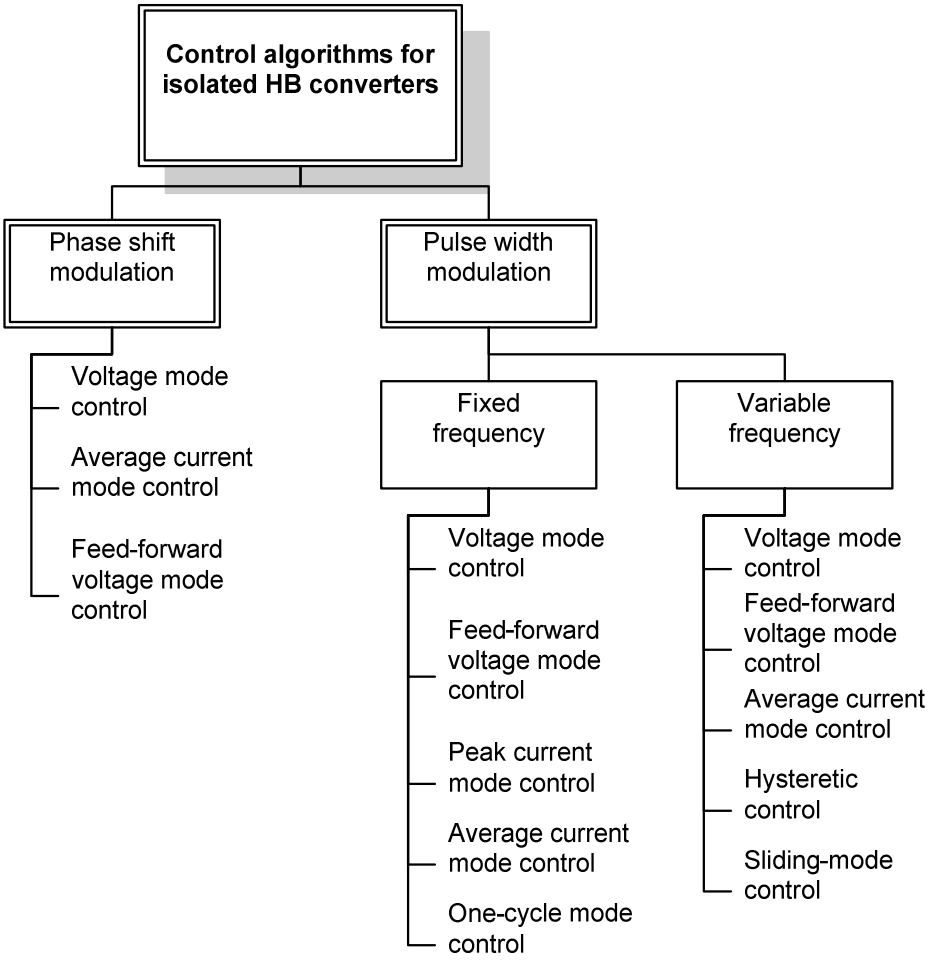


Fig. 1.14 Classification of control algorithms for two- or three-level half-bridge with respect to the chosen modulation method

The discussion above reveals that there are two main groups of control algorithms suitable for the FEC based on the isolated HB topology: VMC or CMC. It is also clear that there is no direct answer to the question which control algorithm is the best. It all depends on the application, control task, control environment etc. However, there are considerations which could point to one or the other as more optimum for each particular application [60]. CMC should be considered if:

1. the output of the converter is to be used as a current source;
2. fast dynamic response to input changes is needed;
3. a DC/DC converter where the input voltage variation is relatively constrained;
4. modular applications, where parallelability with load sharing is required.

VMC is to be considered if:

1. there are wide input line and/or output load variations possible;
2. particularly with low line - light load conditions, where the current ramp slope is too shallow for stable PWM operation;

3. high power and/or noisy applications, where noise on the current waveform would be difficult to control;
4. applications, where the complexities of dual feedback loops and/or slope compensation are to be avoided.

1.4.4 Communication and Diagnostics

According to standard EN50155 the traction equipment should be provided with built-in diagnostic and indication functions. Today's most advanced FEC systems are constantly monitoring and saving internal parameters. An important issue is communication with other on-vehicle devices. In order to exchange information between all kinds of on-board equipment a standardized train communication network (TCN) has been worked out. According to IEC61375 regulations the TCN is constituted by two buses Wire Train Bus (WTB) and Multifunctional Vehicle Bus (MVB). WTB is defined as the train bus that is used to connect multiple vehicles. MVB is defined as the vehicle bus that is used to connect equipment within a single vehicle. In general MVB is a field bus, which has been specially designed for railway vehicles. The main characteristics of the MVB are the high robustness achieved by redundant communication lines and extensive error checking, capability to handle real time communication, support of cyclic process data at fixed time intervals, and easy interfacing to other bus systems. MVB interface is recommended for all new generation converters used in traction applications [91]-[93].

Usually a serial communication technology RS-232 or Ethernet is used for service and diagnostics. The system can be easily monitored using a laptop or a personal computer. Both online and offline monitoring mode should be possible. Online mode allows real time measurements and status indications while working in the offline mode allows displaying and analyzing previously stored data. To fulfil the indication requirement of EN50155 some relay outputs should be added to the control system. One drawback of conventional control systems of FEC is the lack of manual adjustment possibilities. The users can only observe and analyze the operating data but cannot change the parameters. Adding adjustment functions to the control system, e.g. freely programmable functionality of the relay outputs, in real time adjustable regulator parameters etc. could improve the adaptability and general performance of the FEC for traction applications [94]-[96].

1.5 Generalizations

There are no benchmark solutions available for such a demanding application as the control system of the front-end converter for traction APS. The rugged railway standards combined with strict end user requirements make the design of a FEC for traction applications and its control system very challenging. Together with the technological progress also the demands are rapidly growing. Therefore a modern FEC for traction applications must be reliable, energy efficient and flexible. These goals can only be reached using the most recent

state of the art components, technologies and combining them with new software solutions. Based on the analysis of technological advancement of DC/DC converters and their control systems, the main trends in control systems for front-end converters can be summarized as follows:

1. The complexity of control systems of front-end converters for traction applications has been steadily growing over the last decade. A modern control system of FEC not only generates control pulses for IGBTs but also stores operating parameters and is able to communicate with other devices. A communication and diagnostic interface is becoming an indivisible part of the control system. Referred to HP and HV traction applications, the control system should also have a reliable protection system.
2. Digital control is replacing analogue control in front-end converters for traction applications. This has been a strong tendency over last decade. Modern front-end converters for traction applications are sophisticated systems where high flexibility and compactness is required. Digital control fulfils best those requirements.
3. As a central control unit in today's front-end converters for traction applications, a DSC or MC has the highest potential. PLCs lack flexibility although they are reprogrammable and easy to use. FPGAs will be most probably applied as auxiliary control units beside a MC or a DSC. FPGAs can handle non-sequential control operations, e.g. signal generation, mixing, logic operations (AND, OR, XOR etc) between control signals etc.
4. PWM is the most widely used modulation method in front-end converters for traction applications. However, the rapid development of power semiconductors allows the use of new converter topologies for which PSM may be more optimal modulation method.
5. Most widely used control algorithms are CMC and VMC. Naturally both algorithms were based on analogue control technology but nowadays also digital algorithms are available. Digital VMC has become a new trend in front-end converters for traction applications. It is simple, yet flexible and has good dynamic response to wide load variations. Due to complexity and poor response to load changes, digital CMC has remained on the background.
6. Classical soft switching is mostly not used in front-end converters for traction applications due to the external circuits, which increase complexity and implementation costs. An alternative to be researched is soft switching without additional components.
7. Most of today's front-end converters for traction applications are provided with communication and diagnostics functions. Often RS-232 interface is used for service and diagnostics.

2. ANALYTICAL STUDY OF HALF-BRIDGE ISOLATED DC/DC CONVERTERS

2.1 General Requirements for the Front-End Converter

One of the greatest challenges that designers of rolling stock power supplies have to face is the extremely wide input voltage range at the converter input terminals and the load step changes at the output. The converter must ensure stable output, i.e. in brief, dynamic performance that provides the basic properties of the power supply. The main functions of the converter's dynamic performance are line regulation, load regulation, and load transient response. Load transient response provides information on the reaction of the converter output to a rapidly changing load. Line regulation is defined as an ability of a converter to provide a stable output voltage under the conditions of changing input voltage. In the traction applications the output voltage should not change over the full range of the input voltage fluctuations. The second demanding item of the power supplies for traction application is load regulation, which defines the maximum deviation of the output voltage from its nominal value, with a variation of the load current within its specified limits. A typical front-end converter for traction APS has to fulfil combined regulation requirements, i.e. to provide a stable output voltage under the conditions of changing input voltage and load current.

2.2 Front-End Converter for Traction Applications Based on the Two-Level Half-Bridge Topology

Up to today, the HB isolated DC/DC converter has been generally referred as an attractive topology for different low-voltage middle-power applications with the power range up to 2 kW. The use of the HB topology was limited by the properties of inverter switches. Today's implementation of new generation high-voltage IGBTs (6.5 kV IGBTs) opens up a whole new area of possibilities in power electronics. The HB topology is suddenly an interesting alternative for high power (P>20 kW) and high voltage (U>2 kV) DC/DC converters. Main benefits of a two-level HB topology are: simplicity, small number of power switches, and reduced number of components. It all can sum up in greater reliability and efficiency. In this thesis the half-bridge isolated DC/DC converter was researched as a candidate topology for the front-end converter for traction applications. A simplified circuit diagram is shown in Fig. 2.1. It consists of two switches: top side IGBT T_T and bottom side IGBT T_B. Both switches are provided with freewheeling diodes. The isolation requirement is fulfilled by a transformer *Tr*. The input of the converter is to be directly feed form the catenary voltage (2200 V…4000 V). Secondary voltage of the

isolation transformer is rectified and filtered. Technical specifications of the investigated two-level HB isolated DC/DC converter are presented in Table 5.

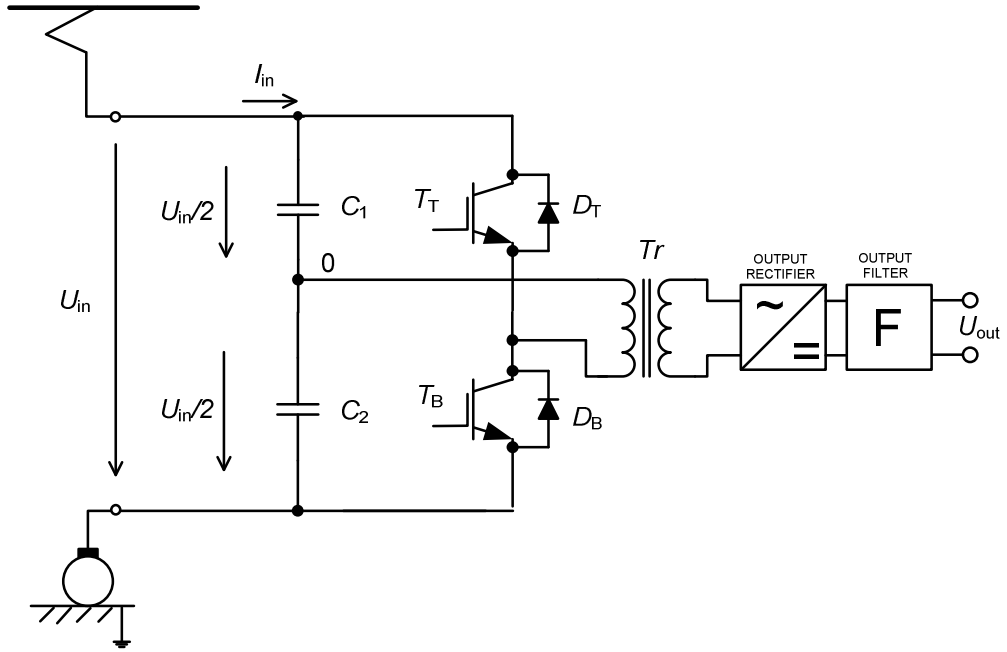


Fig. 2.1 Front-end converter based on the two-level half-bridge topology

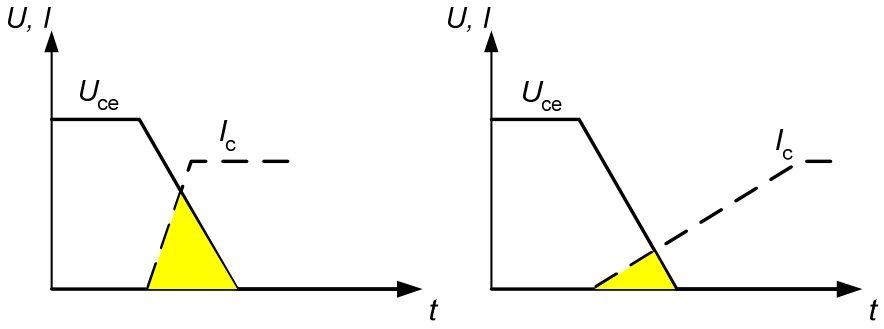
Table 5 Technical specifications of the front end converter for traction applications based on two-level half-bridge topology

Parameter	**Value**
Long-term minimal input voltage $U_{in\text{-}min}$, kV	2.2
Long-term maximal input voltage $U_{in\text{-}max}$, kV	4.0
Rated output power P_{out}, kW	50
Switching frequency f_{sw}, kHz	1
Converter output voltage U_{out}, kV	0.35 ±5%
HV IGBT modules	FZ200R65KF1

2.2.1 Comparative Analysis of Modulation Methods and Soft Switching Techniques for Two-Level Half-Bridge Inverters

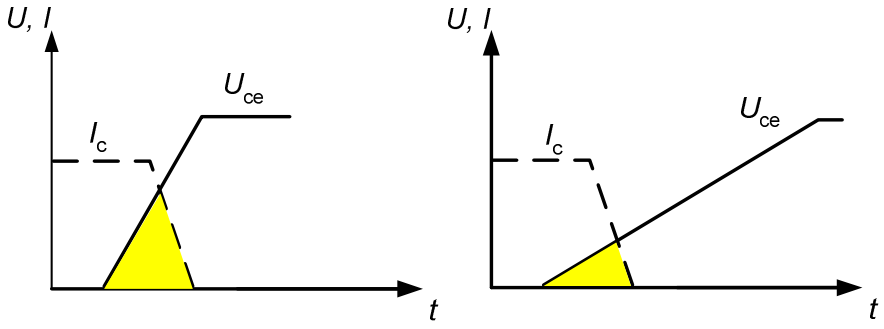
In order to efficiently process energy, modern DC/DC converters must provide high volumetric power density, low electromagnetic interference and low cost. One way to partly satisfy those requirements is to use higher switching frequency of DC/DC converters. The disadvantage of this is that increased switching frequency leads to higher switching losses. Resonant-mode converters offer some solutions to overcome those problems. Using additional reactive snubbers, switching losses can be decreased, as shown in Fig. 2.2. The commutation mode of semiconductor devices is usually classified as hard switched, snubbered or soft switched. In hard switching, there is a considerable area of overlap between the collector-emitter voltage (U_{CE}) and its commutated current (I_C), as indicated in Fig. 2.2 (a). The overlap area is proportional to

switching losses. An inductor-type snubber (L-type) in series with the transistor reduces the current's rate of change (dI_c/dt) and this helps to reduce the overlap area, as shown in Fig. 2.2 (b). A capacitance type snubber (C-type) connected in parallel to the transistor reduces the voltage change (dU_{ce}/dt) and this helps to reduce turn-off losses, as shown in Fig. 2.3 (b). The drawback of resonant-mode converters is that additional components are needed. In rolling stock HP and HV DC/DC front-end converters this can be a serious drawback [97][98].



(a) *(b)*

Fig. 2.2 Turn-on commutation mode: hard switched commutation (a), L-snubbered commutation (b)



(a) *(b)*

Fig. 2.3 Turn-off commutation mode: hard switched commutation (a), C-snubbered commutation (b)

Soft switching technique can also be a valuable option to enhance the converter's efficiency. Soft switching reduces turn-on and turn-off losses of transistors. In general, there are two soft switching techniques available: zero voltage switching (ZVS) and zero current switching (ZCS), as shown in Fig. 2.4. ZVS is always related to the turn-on process of an IGBT. The transistor does not start conducting until the voltage across its terminals has reached zero. Turn-on losses are thus eliminated. ZCS is comparable. It involves the turn-off process of the IGBT. Thus, turn-off losses are eliminated. A combination of ZCS and ZVS is also possible [99][100].

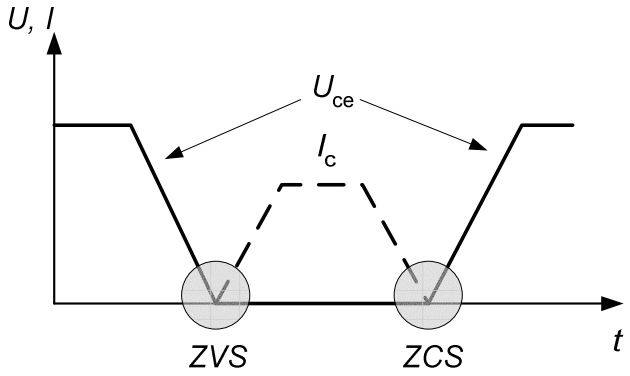


Fig. 2.4 Principle of ZVS and ZCS

Unlike the snubbered commutations, soft switching can also be achieved without additional components. Better performance is to be achieved by incorporating circuit parasitic elements, such as stray capacitances and stray inductances. However, only partial soft switching is achievable, i.e. ZVS or ZCS and not both at the same time. Two soft switching techniques are available for HB converters which do not require any additional components: asymmetric PWM (Fig. 2.5 (b)) and duty cycle shifted PWM (Fig. 2.5 (c)). In the classical symmetrical PWM (Fig. 2.5 (a)), transistors are working in the hard switching mode.

In the asymmetric PWM method, transistors are switched complementary, as shown in Fig. 2.5 (b). It means that the upper IGBT T_T, operates with a duty cycle $D<0.5$ while the bottom IGBT T_B operates with a duty cycle $1-D$. The output voltage regulation is attained by changing D. If T_T is turned off, then the leakage inductance of the transformer primary forces the current to flow through the parasitic capacitors of each transistor. The parasitic capacitor of the upper IGBT will be charged and the parasitic capacitor of the bottom IGBT discharged. After discharge the freewheeling diode D_B begins to conduct and guarantees zero voltage across T_B. The conduction time of the recovery diode depends on the energy stored in the leakage inductance of the transformer *Tr*. Thus, the bottom IGBT can be turned on lossless in zero voltage conditions. The same process repeats for the opposite IGBT T_T. In order to prevent cross conduction, a small dead time (t_d) will be introduced between the consecutive transitions, as indicated in Fig. 2.5. However, the timing must be accurate. Otherwise ZVS is not achievable. The dead time between the consecutive transitions must be shorter than the conduction time of the corresponding freewheeling diode. In general, ZVS conditions for an asymmetrical PWM converter depend on the following parameters: parasitic capacitances of IGBTs, leakage inductance of the transformer, load resistance, switching frequency, and dead time. The asymmetric PWM method has the following benefits and drawbacks [101]-[107].

Benefits:

- reduced switching losses;

- soft switching possible without any additional components.

Drawbacks:

- accurate timing required, increase in the complexity of the control system;
- ZVS depending on many parameters, which makes the design of the converter a complicated task and limits the application field;
- limited dead time, results in reduced protection capability of HV IGBT switches;
- unbalanced voltages of input capacitors (C_1, C_2), which can cause volt-second unbalance and saturation of the isolation transformer;
- uneven voltage and current components stresses;
- nonlinear DC gain ratio.

The asymmetric PWM method is not suitable for rolling stock power converters because of the wide input voltage range, load variations, relative low switching frequencies, and overall rugged environment conditions.

An alternative to the asymmetric PWM method is a duty cycle shifted PWM (DCS PWM) control scheme (Fig. 2.5 (c)). It achieves ZVS operation for one of the two switches without adding additional components by utilizing transformer leakage inductance and parasitic capacitances of the switches. The concept of this new control scheme is based on the asymmetric PWM method. One of the two symmetric PWM driving signals is shifted close to the other, such that ZVS may be achieved, as shown in Fig. 2.5. Unlike the asymmetric control, the pulse width is kept equal for both switches. Compared with the conventional symmetric PWM methods, DCS PWM controlled HB has the same voltage and current stresses in the primary switches, the same peak and root mean square values of transformer currents, identical volt-second value and magnetizing B-H loop of the transformer. DCS PWM has the following benefits and drawbacks [108].

Benefits:

- even voltage and current stresses of components;
- ZVS for one switch achievable without additional components.

Drawbacks:

- accurate timing required, increase in the complexity of the control system;
- implementation in a digital control system complicated due to variable phase shift between control signals;
- limited dead time results in reduced protection capability of HV IGBT switches;
- ZVS depending on many parameters and difficult to achieve at lower frequencies.

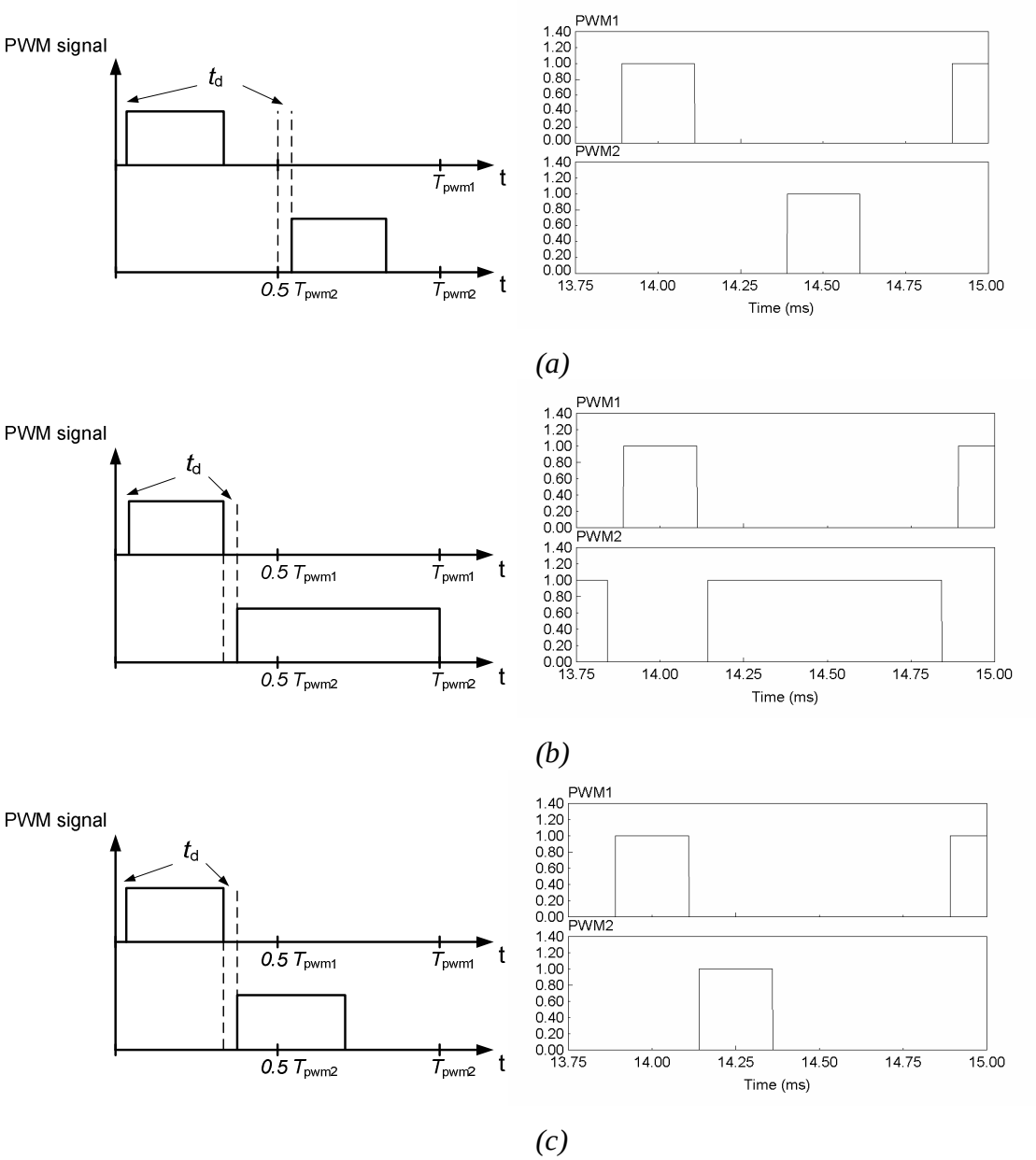


Fig. 2.5 Different PWM modulation methods: symmetrical PWM (a), asymmetric PWM (b), duty cycle shifted PWM (c)

In the traditional PWM method the transistors are working symmetrically. To ensure proper work of the inverter and to prevent cross conduction, the control signals of IGBTs must be phase shifted in 180°, as shown Fig. 2.5 (a). The main drawback of the symmetric PWM is that both primary switches operate in hard switching conditions. Moreover, the oscillation between the transformer leakage inductance and junction capacitance of the switches results in energy dissipation and increased EMI emissions. To suppress the so-called ringing, resistive snubbers are usually added, which increase losses. Therefore, the symmetric PWM is not a good candidate for high frequency HB converters [108]. In the case of HP and HV converters as the front-end converter for traction applications, usually switching frequencies are relatively low (1…3 kHz), which essentially reduces switching losses compared to IGBT conduction

losses. As a result, simplicity and reliability of the symmetrical PWM method will gain priority while asymmetric PWM and DCS PWM methods remain on the background. For such applications symmetrical PWM is the best suitable method. Symmetrical PWM has the following benefits and drawbacks.

Benefits:

- even voltage and current stresses of components;
- simple to imply in a digital control system;
- dead time length is not limited, which provides better protection of IGBTs.

Drawbacks:

- soft switching without additional components is not achievable;
- increased switching losses.

2.2.2 Selection of Operation Points and Duty Cycle Variation Range

The best modulation method for the FEC is symmetrical PWM. Before designing a control system for such a converter, the exact relation between input and output voltage needs to be found. In the case of switching mode HB isolated DC/DC converter the transformer primary winding is alternately connected with input capacitors C_1 and C_2, as shown in Fig. 2.15. Therefore, the voltage amplitude ($U_{\text{Tr-p}}$) over the transformer primary is twice lower than the input voltage. Then the output voltage of the isolated DC/DC half-bridge can be calculated

$$U_{\text{out}} = 2 \cdot D \cdot U_{\text{Tr-s}} = \frac{2 \cdot D \cdot U_{\text{Tr-p}}}{n} = \frac{D \cdot U_{\text{in}}}{n}, \tag{4}$$

where $U_{\text{Tr-s}}$ is the amplitude of the transformer secondary voltage, U_{in} is the input voltage of the converter and n is turn ratio of the transformer. As it can be seen, the output can be regulated simply by the duty cycle. As a next step the operation points and duty cycle range can be selected. The input side of the converter is assumed to be connected directly to the traction supply grid with the voltage tolerances from 2.2 kV DC up to 4.0 kV DC. The most demanding operation point is at the minimum input voltage (2.2 kV DC) and at the rated load conditions (i.e. maximum duty cycle operation). It is essential to prevent even short-time simultaneous conduction of IGBT transistors (Fig. 2.1) in these demanding conditions - it leads to the short circuit across the supply voltage and to the destruction of the converter. According to that, the maximal on-state time $t_{\text{on-max}}$ of each switch of a HB should be set at 80 % of the half period. The maximal duty cycle of the FEC for traction applications is then

$$D_{\max} = \frac{t_{\text{on}-\max}}{T_{\text{pwm}}} = 0.4 \,. \tag{5}$$

If the input voltage at the rated load conditions starts to increase, then in order to maintain stable output voltage, the on-state time must decrease. Thus, maximal input voltage means minimal on-state time ($t_{\text{on-min}}$) and it can be calculated as

$$t_{\text{on}-\min} = \frac{U_{\text{in}-\min}}{U_{\text{in}-\max}} t_{\text{on}-\max} = \frac{2200}{4000} \cdot \left[0.8 \cdot \left(\frac{T_{\text{pwm}}}{2} \right) \right] = 0.44 \left(\frac{T_{\text{pwm}}}{2} \right), \tag{6}$$

where $U_{\text{in-min}}$ is the minimum input voltage, $U_{\text{in-max}}$ is the maximum input voltage, and T_{pwm} is the PWM period. According to (6) minimal duty cycle of the FECis

$$D_{\min} = \frac{t_{\text{on}-\min}}{T_{\text{pwm}}} = 0.22 \,. \tag{7}$$

Operation voltage ranges and on-state times of the front-end converter switches are presented in Table 6. Simulated primary voltage waveforms of the isolation transformer with different input voltages (and the corresponding t_{on}) at the rated load are presented in Fig. 2.6.

Table 6 Operation voltage ranges vs. on-state times and duty cycles of inverter switches

Parameter	**Max. input voltage**	**Min. input voltage**
Converter input voltage U_{in}	2.2 kV DC	4.0 kV DC
on-state time t_{on}	$0.8(T_{\text{pwm}}/2)$	$0.44(T_{\text{pwm}}/2)$
Duty cycle D	0.4	0.22

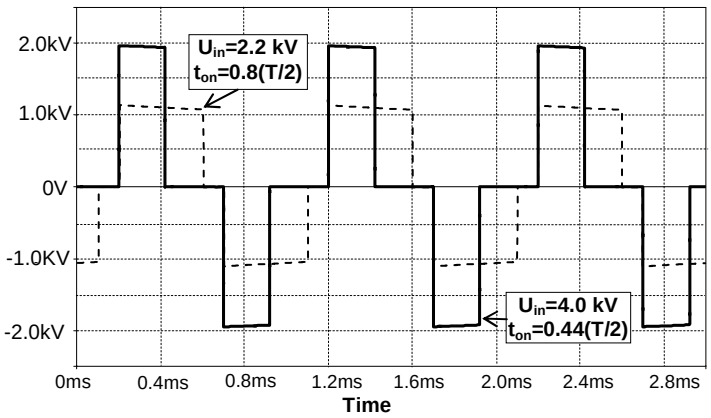


Fig. 2.6 Isolation transformer supply voltage waveforms at maximal and minimal input voltages

2.2.3 General Analysis of Capacitor-Related Volt-Second Unbalance Problems

The most widely discussed problem concerning HB inverters is volt-second unbalance of series connected input capacitors. Unbalanced capacitor voltages produce a DC component in the transformer primary which pushes the transformer core towards into saturation. Transformer saturation can have harmful consequences: increased conduction (or short circuit), EMI, higher switching losses, and decreased overall reliability. Generally, volt-second unbalance of a symmetrical half-bridge could be caused by: unsymmetrical duty cycles of the control signals, differences in the voltage drops of switches, secondary side diode parameters, varying loads, and input capacitor parameters [109]-[112].

The HB circuit (see Fig. 2.1) uses two switches (T_T and T_B) to produce a bidirectional current in the primary winding of the transformer *Tr*. The capacitor voltage divider biases one side of the primary winding at half the input voltage (U_{in}) so that the voltage imparted on the winding is one-half U_{in}. In the case of voltage unbalance, the average volt-seconds applied to the isolation transformer primary winding for the positive-going pulses will not exactly equal to that for negative-going pulses. The transformer flux density will increase with each cycle into saturation. Such staircase saturation effect of the transformer is one of the major HB topology related problems.

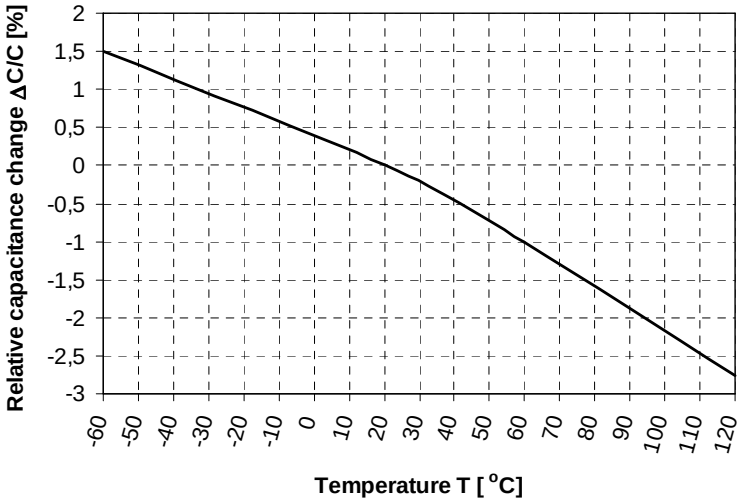
It is a well-known fact that power electronic converters developed for the rolling stock must be mechanically rugged for reliable operation under very harsh field conditions, with additional protection to ensure immunity to humidity (up to 95% relative humidity) and high operating temperature values (internal cubicle temperature is -25…+55 ºC according to EN50155). In such a demanding application, the DC-link capacitors have become the most critical element in the whole converter stack. The trend of the industrial and traction market for power conversion is to replace electrolytic capacitors by film technology. This trend is generated by many advantages that film technology is offering. The major benefit is high rated voltage (up to 10 kV and even more) and overvoltage withstanding up to two times the rated voltage. Thus, in the current case the advanced polypropylene capacitors ELCOD K75-80 (rated voltage/maximum peak voltage relation is 4000 V/6600 V, capacitance is 100 uF, capacitance tolerance is ± 10 %) were implemented on the primary side of the converter (C_1 and C_2 in Fig. 2.1). However, despite excellent electrostatic properties the new film capacitors still suffer from capacitance change related to temperature, humidity and lifetime [113].

Capacitance will undergo a reversible change within the range of temperatures between the upper and lower category temperatures. The gradient of the capacitance/temperature curve is given by the temperature coefficient α_C, which is defined as the average capacitance change in relation to the capacitance measured at (20±2) ºC, occurring within the temperature range T_1 to T_2.

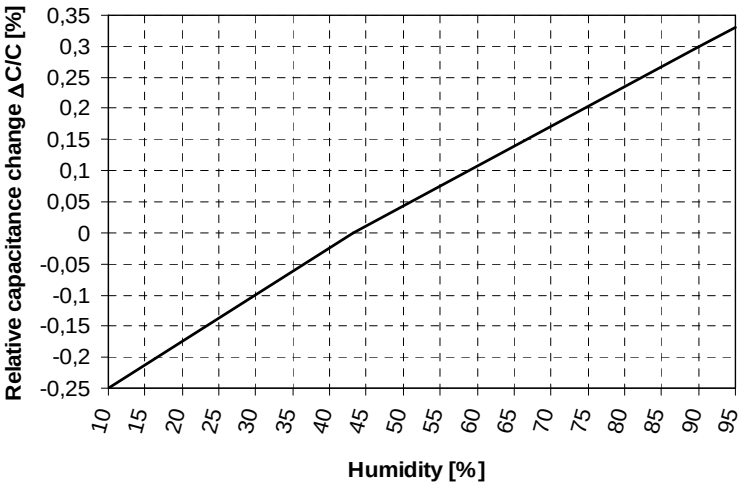
$$\alpha_c = \frac{C_2 - C_1}{C_3 \cdot (T_2 - T_1)}, \tag{8}$$

where C_1 is the capacitance measured at temperature T_1, C_2 is the capacitance measured at temperature T_2 and C_3 is the reference capacitance measured at (20±2) ºC.

The temperature coefficient is essentially determined by the properties of the dielectric, the capacitor construction and the manufacturing parameters. Polypropylene capacitors used in the project (ELCOD K75-80) have a negative temperature coefficient α_C = -250 (10^{-6}/K). The reversible change of capacitance with the temperature for the investigated capacitors is presented in Fig. 2.7 (a).



(a)



(b)

Fig. 2.7 Relative capacitance change vs. temperature (a) vs. humidity (b)

Another possible reason of the capacitance mismatch is related to a variation of capacitance with humidity. Depending on the type of capacitor design, both the dielectric and the effective air gap between the films will react to changes in the

ambient humidity, which will thus affect the measured capacitance. The humidity coefficient β_C is defined as the relative capacitance change determined for a 1 % change in humidity at constant temperature:

$$\beta_c = \frac{2 \cdot (C_2 - C_1)}{(C_2 + C_1) \cdot (F_2 - F_1)}, \tag{9}$$

where C_1 is the capacitance at relative humidity F_1 and C_2 is the capacitance at relative humidity F_2. High-voltage polypropylene capacitors used in the project (ELCOD K75-80) have a humidity coefficient β_C = 40…100 (10^{-6}/% r.h.). A typical capacitance/humidity characteristic of a selected capacitor type is shown in Fig. 2.7 (b). Wide variations of capacitance are to be expected at the relative humidity above 85 %.

In addition to the changes described, the capacitance of a DC-link capacitor is also subjected to irreversible changes known as drift $i_z = |\Delta C/C|$. The values stated for the capacitance drift are maximum values and refer to a two-year period and a temperature up to 40 ºC. Here the reversible effects of temperature changes (α_C) and changes in the relative humidity (β_C) are not taken into consideration. The drift is stabilized over time and thus provides a long-term stability of capacitance. For the polypropylene capacitors, the capacitance drift is about 2…3 %. However, it may exceed the specified values if a capacitor is subjected to frequent, large temperature changes in the vicinity of the upper category temperature and relative humidity limits.

Considering “the worst case” discussed above capacitance change could achieve about 4.5…5 %. But if the input capacitors are not properly matched during converter assembling, the total capacitance drift can even reach 12...15 %. The idea of the following analysis is to find out what the influence of the capacitance difference is on the volt-second unbalance [114].

Matlab Simulink together with Sim Power Systems toolbox was used to simulate the processes. The most interesting part of the HB isolated DC/DC converter in the current case is the input stage i.e. the HB inverter. Thus, the model could be simplified by leaving out the transformer and the output rectifier and replacing them with an equivalent resistor as shown in Fig. 2.8. The value of equivalent load resistance could be calculated as:

$$R_{equ} = \frac{U_{Tr-p-rms}^2}{P_{Tr}}, \tag{10}$$

where $U_{Tr\text{-}p\text{-}rms}$ is the transformer primary rms voltage and P_{Tr} is the active power of the isolation transformer (neglecting the losses). The transformer primary rms voltage is proportional to the converter input voltage [115]:

$$U_{Tr-p-rms} = \frac{U_{in}}{2} \cdot \sqrt{2 \cdot D}\,. \tag{11}$$

By substituting (11) into (10) the equivalent load resistor can be calculated as:

$$R_{\text{equ}} = \frac{U_{\text{in}}^2}{P_{\text{Tr}}} \cdot \frac{D}{2}, \tag{12}$$

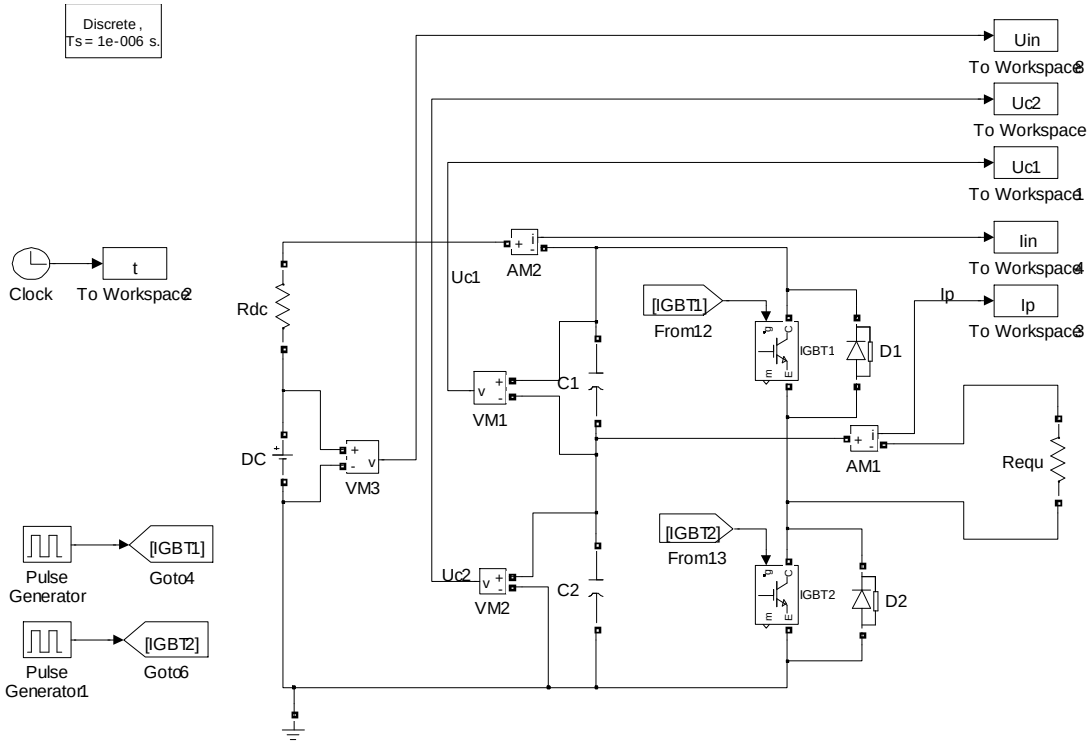


Fig. 2.8 Simplified simulation model of the HB isolated DC/DC converter in Matlab Simulink

The IGBTs are controlled with PWM. The switching frequency is 1 kHz. The converter is supplied with reduced input voltage 500 VDC.

First a normal situation was simulated: symmetrical duty cycles of IGBTs and symmetrical input capacitors each 300 μF. No voltage unbalance occurred as it can be seen in Fig. 2.9.

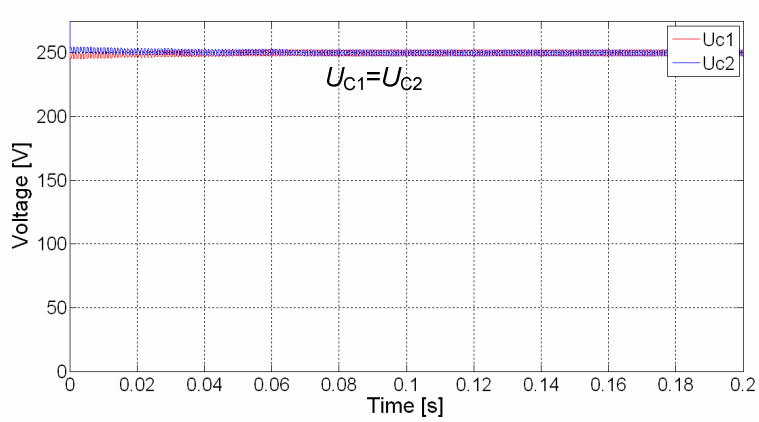


Fig. 2.9 Input capacitor voltages (equal capacitance and symmetrical PWM)

The situation is completely different in the case of unsymmetrical duty cycle, as shown in Fig. 2.10. Duty cycles of IGBTs differ from each other by 20 %. Capacitor voltages are strongly unbalanced although the capacitances are equal.

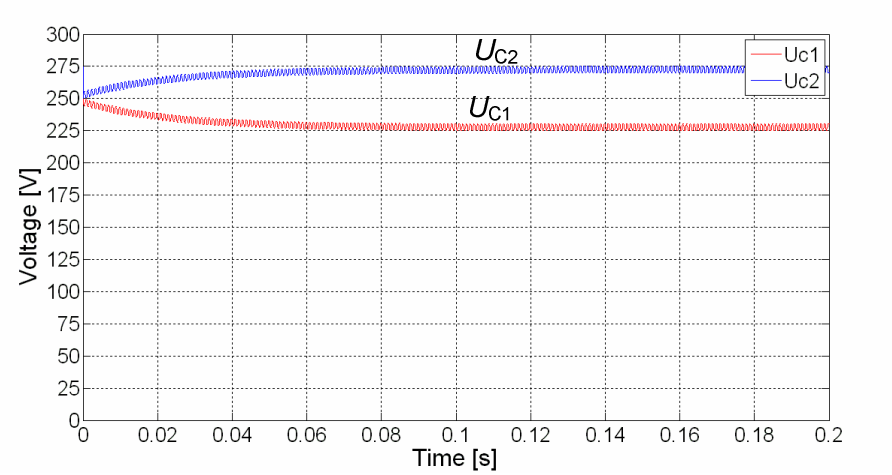


Fig. 2.10 Input capacitor voltages (equal capacitance and unsymmetrical duty cycles)

Let us consider the situation where the duty cycle is symmetrical but input capacitors have unequal capacitance. C_2 will be reduced to 200 µF and C_1 remains 300 µF. In that case the capacitor drift 33 %, which is more than two times higher than the worse case real life value (15 %). The difference in the capacitance has no effect on the voltage unbalance of input capacitors, as shown in Fig. 2.11. No distinct differences in voltage levels can be noticed.

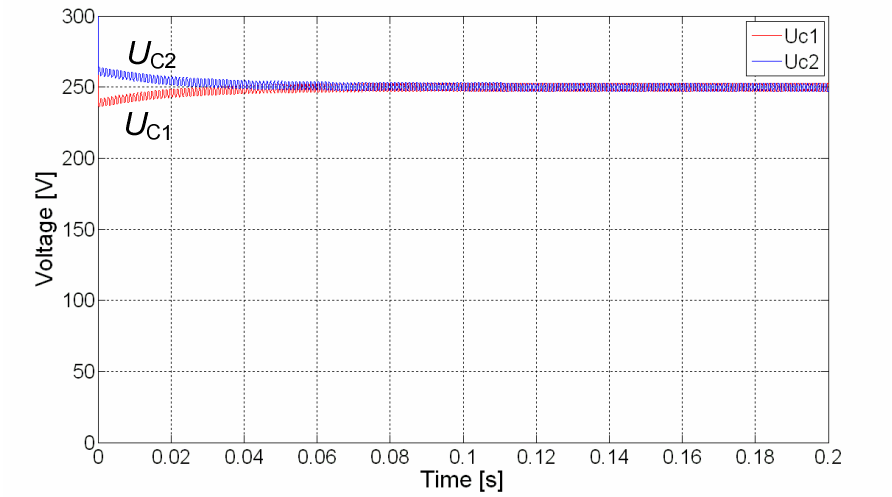


Fig. 2.11 Input capacitor voltages (unequal capacitance and symmetrical duty cycles)

In the following two simulations (Fig. 2.12 and Fig. 2.13), a situation with unequal capacitances (33 % capacitor drift) and unsymmetrical duty cycles (20 % duty cycle drift $D_{TT}>D_{TB}$) was studied. An unbalance in the voltages of input capacitors can be seen. The situation does not change by alternating duty cycles ($D_{TT}<D_{TB}$), as shown in Fig. 2.13. The simulations provide a clear indication that unequal capacitances do not have any effect on volt-second

unbalance, which mainly depends on the duty cycle symmetry. The practical results are analyzed in chapter 3.3.6.

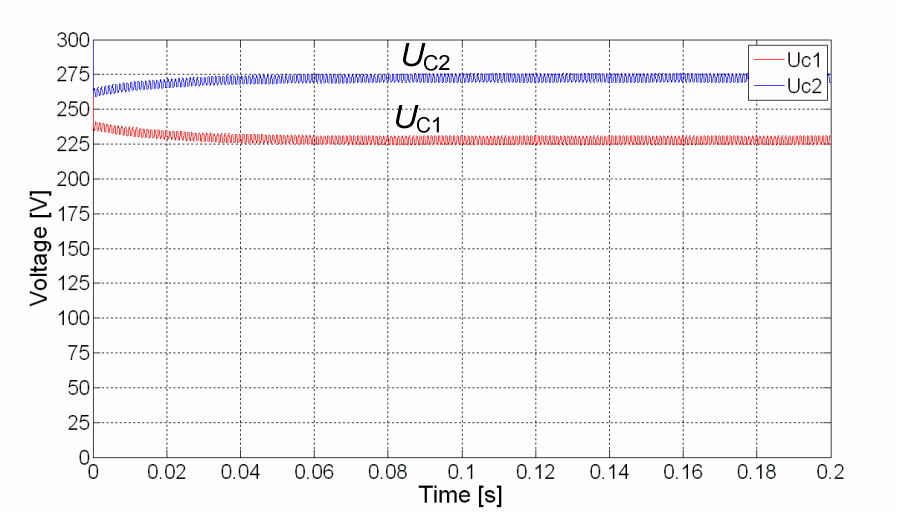


Fig. 2.12 Unequal input capacitors and unsymmetrical duty cycles ($D_{TT}>D_{TB}$)

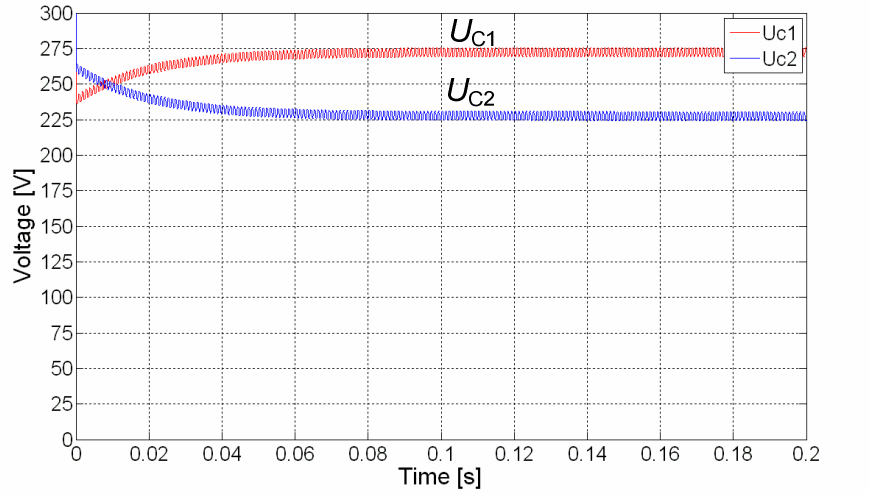


Fig. 2.13 Unequal input capacitors and unsymmetrical duty cycles ($D_{TT}<D_{TB}$)

2.2.4 Analysis and Simulation of Digital Control Algorithms for Two-Level Half-Bridge Converters

According to the diagram in Fig. 1.14, five control algorithms are available for a HB isolated DC/DC converter controlled by fixed frequency PWM: voltage mode control (VMC), feed forward VMC, peak current mode control (CMC), average CMC, and one-cycle mode control. Due to complexity and nonlinear nature, one-cycle mode control can be considered unsuitable for the current application. Therefore, only four control algorithms will be analyzed in more detail.

Peak Current Mode Control

A peak CMC regulation loop for the HB isolated DC/DC converter is shown in Fig. 2.14. It consists of two control loops, inner current and outer voltage control loop. The current peak value (I_{peak}) is adjusted by the outer voltage control loop, which starts with the output voltage (U_{out}) measurement. A regulator (*REG*) eliminates the regulation error and outputs peak current value. Since $I_{Tr\text{-}p}$ is alternating current, it is also required to define a negative I_{peak} value. That will be used to control the transistor T_B. The inner current control loop starts with the transformer primary current ($I_{Tr\text{-}p}$) measurement. Comparators (*CP1*, *CP2*) compare the primary current with I_{peak}. When both currents become equal, a RS-latch will be reset and the corresponding transistor (T_T or T_B) will be switched off. The RS-latches are clocked with phase shifted pulses that guarantees 180 º phase shift between control signals. The inner current control loop provides a very fast acting line regulation and overcurrent protection function. The voltage control loop is much slower, depending on the electrical circuit and the regulator time constants hence the response to load variations (which depends on the voltage control loop) will not be as fast as the inherent input voltage transient rejection performance. However, peak CMC cannot be directly applied on a DC-DC isolated HB converter topology due to the capacitor voltage unbalance issue.

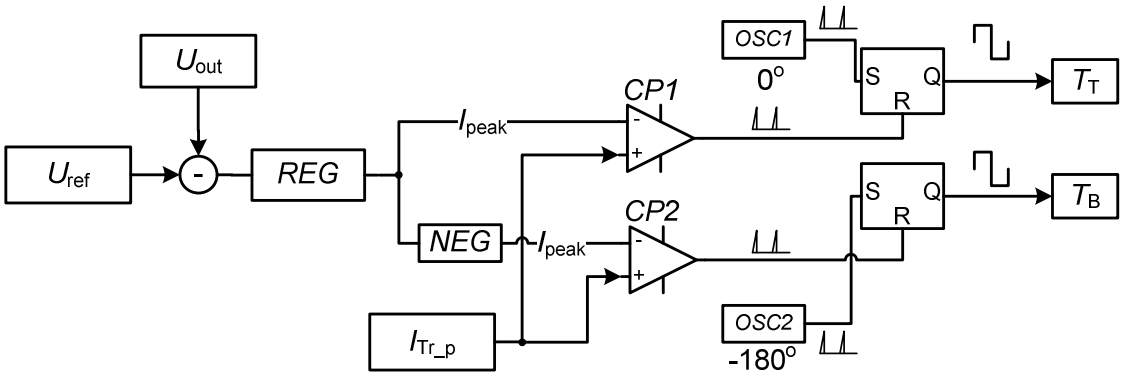


Fig. 2.14 Peak current mode control principle for the half-bridge isolated DC/DC converter

Peak Current Mode Control Related Volt-Second Unbalance Problem

In Fig. 2.15 (a) a simplified input stage of the HB isolated DC/DC converter is shown. The current path (I_{IGBT}) when the top transistor T_T is in on-state is shown in Fig. 2.15 (b) and current path when the bottom transistor T_B is conducting is shown in Fig. 2.15 (c). In the case of symmetrical PWM control switches have symmetrical on-state times and the currents are symmetrical and with equal on-state time.

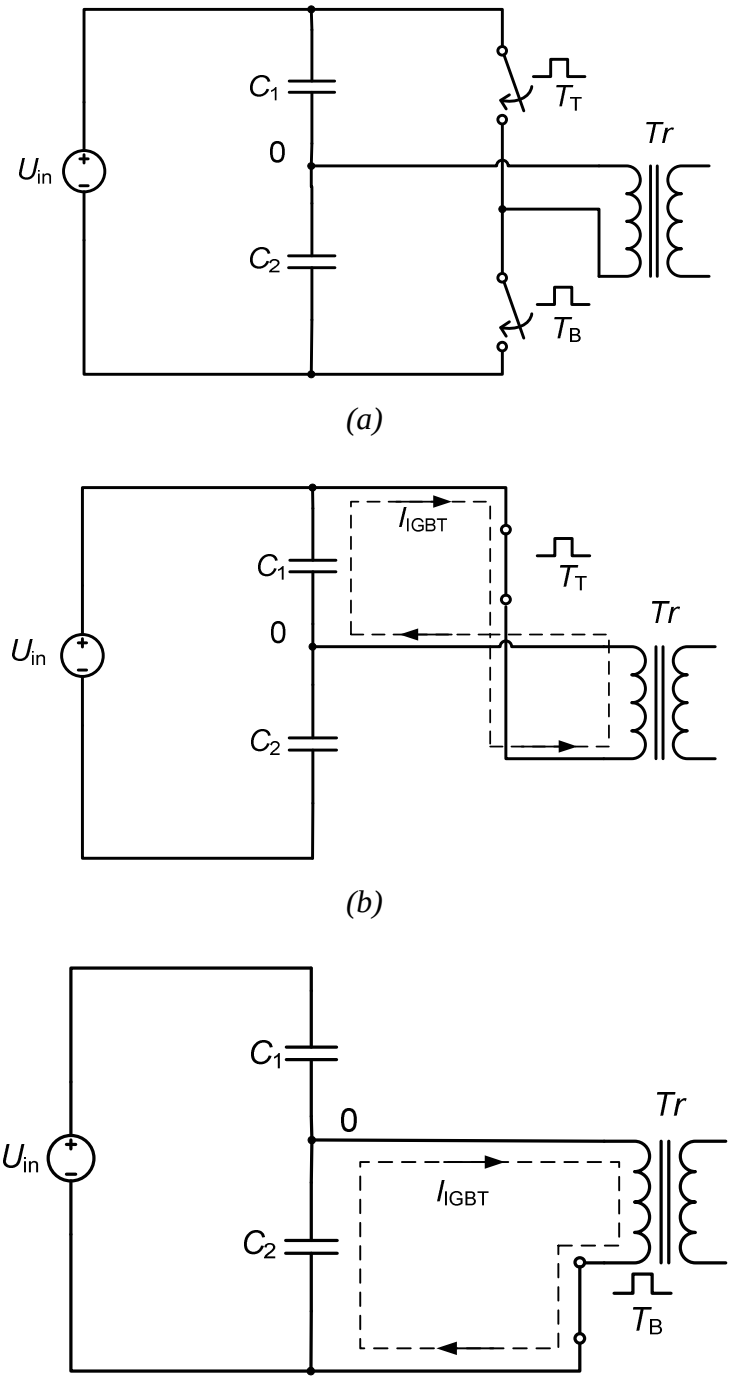


Fig. 2.15 Simplified circuit diagram of the half-bridge isolated DC/DC inverter (a), IGBT current path when T_T is conducting (b), IGBT current path when T_B is conducting (c)

As it can be seen, the transformer primary winding is alternately connected with input capacitors C_1 and C_2. Therefore, the voltage over the transformer primary can be calculated as follows:

$$U_{c2} = U_{\text{Tr-p}} = L \cdot \frac{dI_{\text{IGBT}}}{dt} \approx L \cdot \frac{\Delta I_{\text{IGBT}}}{t_{\text{on}}}, \tag{13}$$

where L is leakage inductance of the transformer primary, I_{IGBT} is transistor current, t_{on} is the on-state time of the IGBT, and U_{c2} is the voltage of the according capacitor. Rearranging (13) t_{on} for one transistor can be obtained:

$$t_{\text{on}} = L \cdot \frac{\Delta I_{\text{IGBT}}}{U_{c2}}. \tag{14}$$

In an ideal case, input capacitors C_1 and C_2 are equally charged with the half input voltage $U_{\text{in}}/2$ and no volt-second unbalance occurs. But in real conditions there is always a voltage difference due to parasitic parameters. Peak CMC introduces additional positive feedback, which will increase the voltage difference of the input capacitors. According to (14), reduced U_{c2} increases t_{on} and vice versa. As a result, duty cycles of the transistors will change until one switch has reached its maximum and the other its minimum duty cycle.

Second reason for the volt-second unbalance is poor noise immunity of the peak CMC, especially in the systems where the current slope is small. The typical shape of a IGBT current waveform of the HB isolated DC/DC converter is presented in Fig. 2.16. It can be seen that the slope of the current ramp is small and therefore quite susceptible to noise. The situation was simulated, as shown in Fig. 2.17. During the simulation, an artificial noise signal was added to the normal current signal. As a result, the modulation can be erratic, as shown in Fig. 2.17 (b).

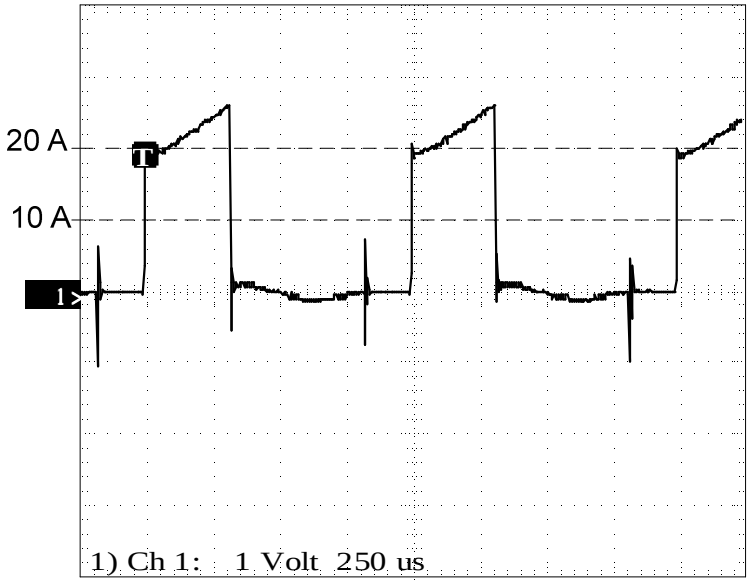
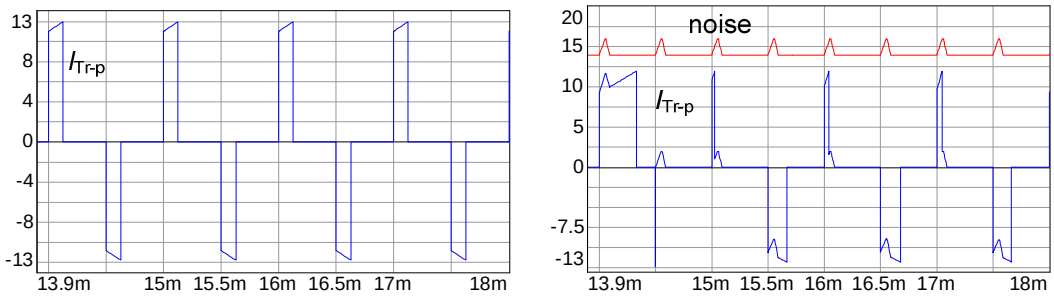


Fig. 2.16 Measured IGBT current waveform of the HB isolated DC/DC converter



(a) *(b)*

Fig. 2.17 Transformer primary current waveforms: ideal noise-free operation (a), with the noise impact (b)

In order study the influence of the volt-second unbalance on the HB isolated DC/DC converter output, a computer model was created, as shown in Fig. 2.18. State graphs were used to simulate the peak CMC algorithm. Since there are two transistors, there are also two identical state graphs. The idea of state graph modeling is to divide a process sequence into different states (round circles) and events (vertical bars). The current state is called active. At the beginning of the simulation, one state in the graph must be defined active (state 1 and state 3) Switching between states is called an event. Events occur if the transfer conditions are true. Let us consider the left state graph in Fig. 2.18. At the beginning, state 1 will be set active. Within that state, the duty cycle of transistor T_T will be set to its maximum (pwm1.dc:=0.4) and the time of the next activation will be calculated (pp1:=pp1+1m). The transistor is switched on and the current I_{Tr-p} starts to increase. Transfer to the second state occurs if the current reaches the peak value I_{peak}. The transistor will be switched off until the PWM1 period (pp1) has been reached and the program returns into state 1.

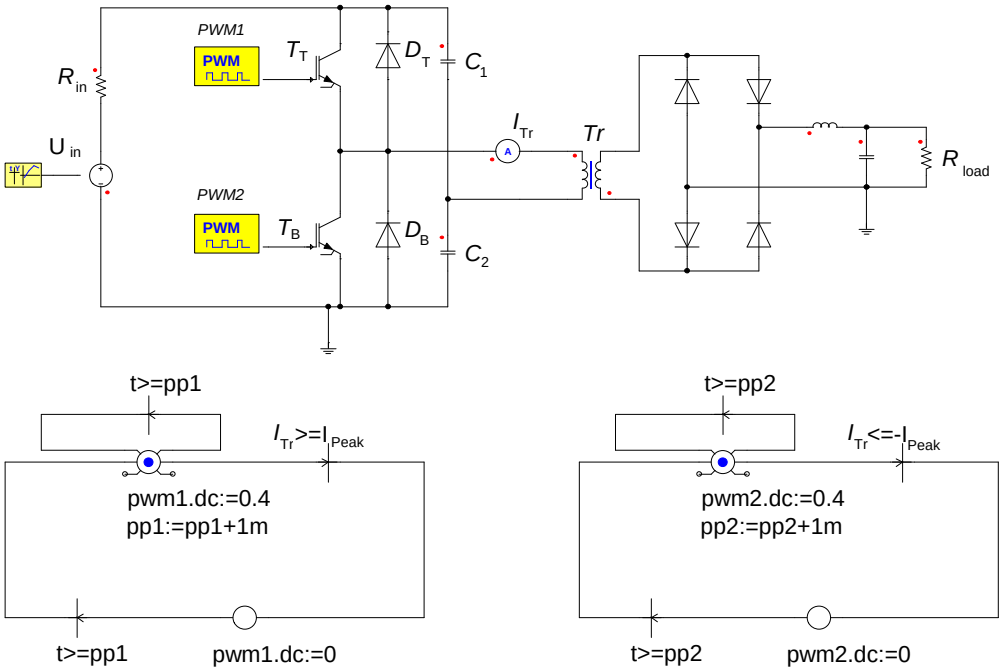
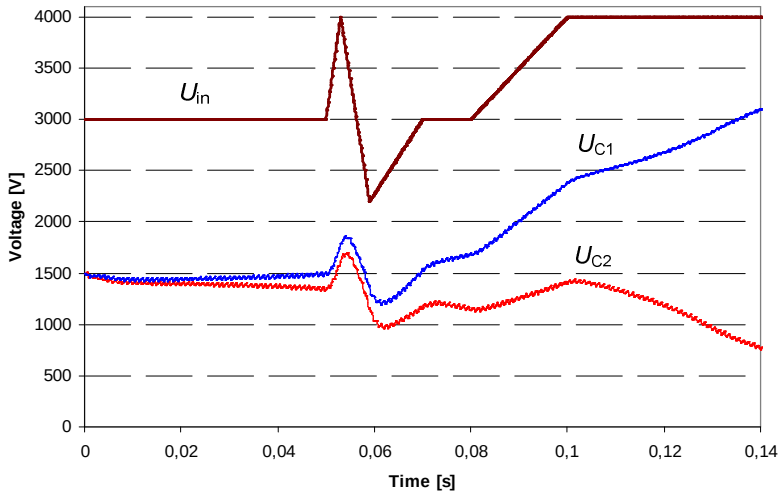
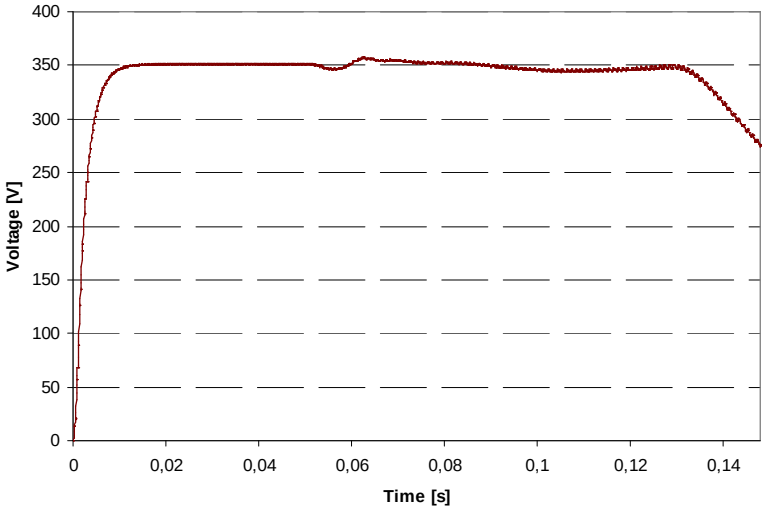


Fig. 2.18 Computer model of peak CMC without outer voltage control loop

Since peak CMC algorithm without output voltage compensation loop was applied, line regulation was chosen. This means that the input voltage will be changed, while the load remains constant. The results are presented in Fig. 2.19. At the beginning the input capacitors (C_1, C_2) are charged equally to the half of the input voltage. The voltage of C_1 gradually starts to increase, while the voltage of C_2 decreases. After 5 ms the input voltage of the converter starts to change, as indicated in Fig. 2.19 (a). It was found that variable input voltage speeds up the unbalance process and the voltage asymmetry will grow even faster. The load voltage remains stable at the beginning but later if the asymmetry has exceeded a certain limit, also the output voltage will collapse, as shown in Fig. 2.19 (b). According to (14) the duty cycle of T_T starts to decrease and the duty cycle of the opposite transistor T_B starts to increase. Finally, T_T reaches its minimum duty cycle and T_B the maximum duty cycle, as presented in Fig. 2.20.

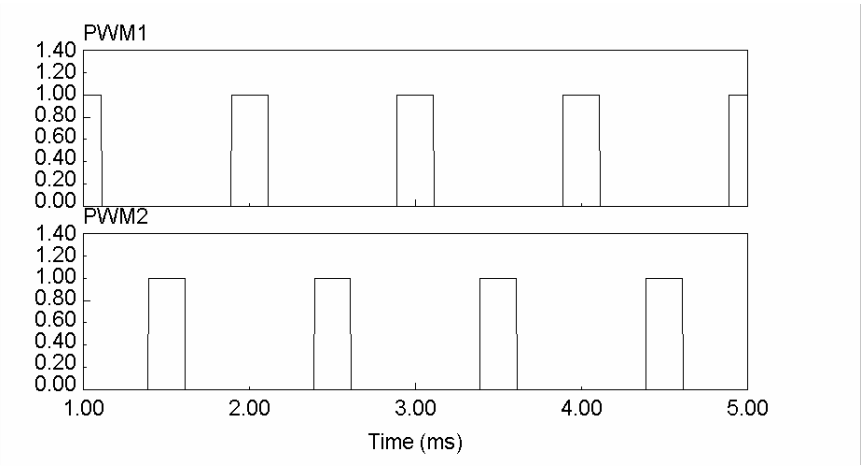


(a)

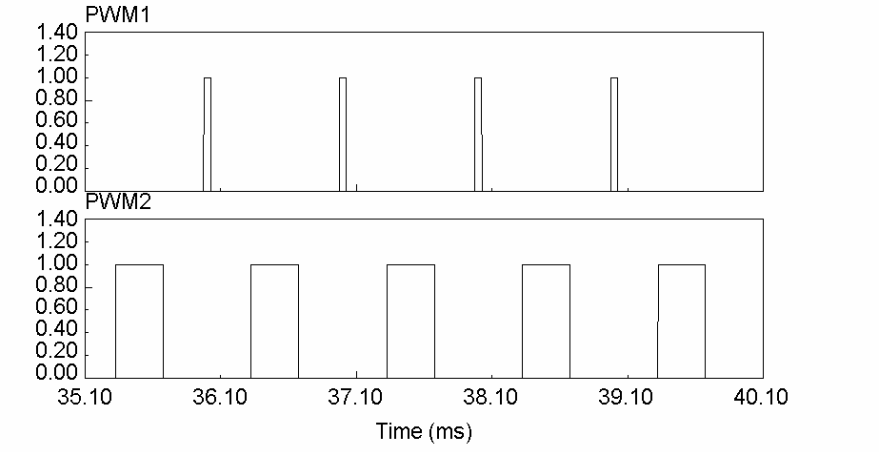


(b)

Fig. 2.19 Volt-second unbalance caused by peak CMC: input voltage and unbalanced input capacitors (a), output voltage (b)



(a)



(b)

Fig. 2.20 Pulse width signals: at the beginning of the simulation (a), at the end of the simulation (b)

There are several possibilities to solve the volt-second unbalance problem inherent to the peak CMC. The most common solution is to add a separate winding to the transformer and two catching diodes parallel to the input capacitors [1]. A very interesting method of balancing the input capacitor voltage with an additional voltage compensation loop was proposed in [64]. Although this method requires no additional hardware and can be implemented within the software, it still makes the software much more complicated. A similar method was discussed in [116]. The problem could be solved by adding a square wave compensating signal the amplitude of which is proportional to the voltage unbalance, to the peak current value.

In this thesis a new digital peak CMC algorithm is proposed by the author, which reduces needed current measurement cycles and eliminates volt-second unbalance problem.

An Improved Peak Current Mode Control Algorithm for Digitally Controlled Half-Bridge Isolated DC/DC Converters

The idea of the peak CMC for the HB isolated DC/DC converter is to measure both negative and positive transformer primary current values and according to that separately switch transistors T_T and T_B (Fig. 1). The proposed idea is to measure just the positive primary current values i.e. the current through the IGBT T_T. The on-state time of T_T will be measured and also used for T_B. That way symmetrical control of the HB would be guaranteed and also no voltage unbalance problem of input capacitors could occur since the duty cycle of both transistors is artificially kept equal.

Digital control is based on interrupts. Interrupts offer an excellent possibility to stop the main program at any time instant thus, time intervals between interrupts can be adjusted with timers and kept constant. This possibility is useful when applying a digital regulator. A properly programmed regulator must act on fixed time steps, easily achievable by using interrupts. Normally there are many interrupt sources that can also occur simultaneously. A prioritization scheme allows a user to specify the order in which multiple interrupt requests are to be handled. Carefully planning the timings and priorities of interrupts can avoid overlapping. An interrupt timing diagram is shown in Fig. 2.21.

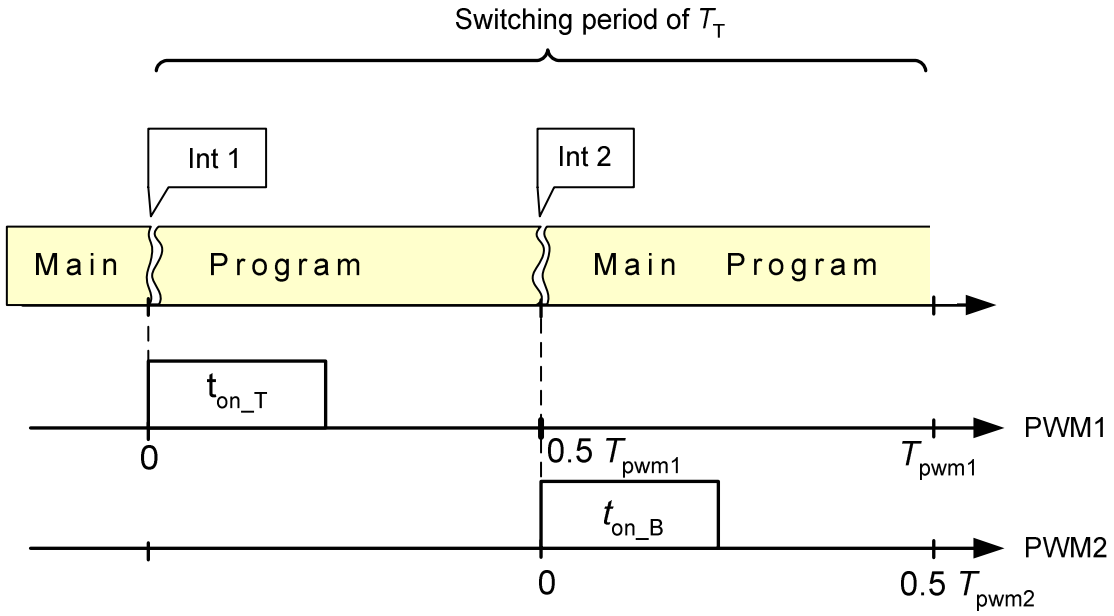


Fig. 2.21 Interrupt timings for improved peak CMC

Interrupts can suspend the main program at any instant. In the proposed improved peak CMC, two interrupts (Int 1 and Int 2) are used that are triggered by the period match of the corresponding PWM timer, as indicated in Fig. 2.21. The general control algorithm is shown in Fig. 2.22. The algorithm is simplified by omitting the outer voltage loop. When an interrupt occurs, the corresponding interrupt routine will be started. The interrupt routine switches on a general purpose timer (GPT), which is used to measure on-state time of the

corresponding IGBT. Then the transistor is turned on. The top transistor T_T remains conducting until one of the following conditions is fulfilled: $I_{Tr\text{-}p}$ has reached I_{peak} value or the on-state time ($t_{on\text{-}T}$) has exceeded the maximal allowed conduction time ($t_{on\text{-}max}$). If one of the two conditions is true, T_T is turned off and GPT_1 stopped. The resulting conduction time of T_T is stored for the following interrupt Int 2. The bottom transistor T_B remains conducting until its on-state time is equal to $t_{on\text{-}T}$.

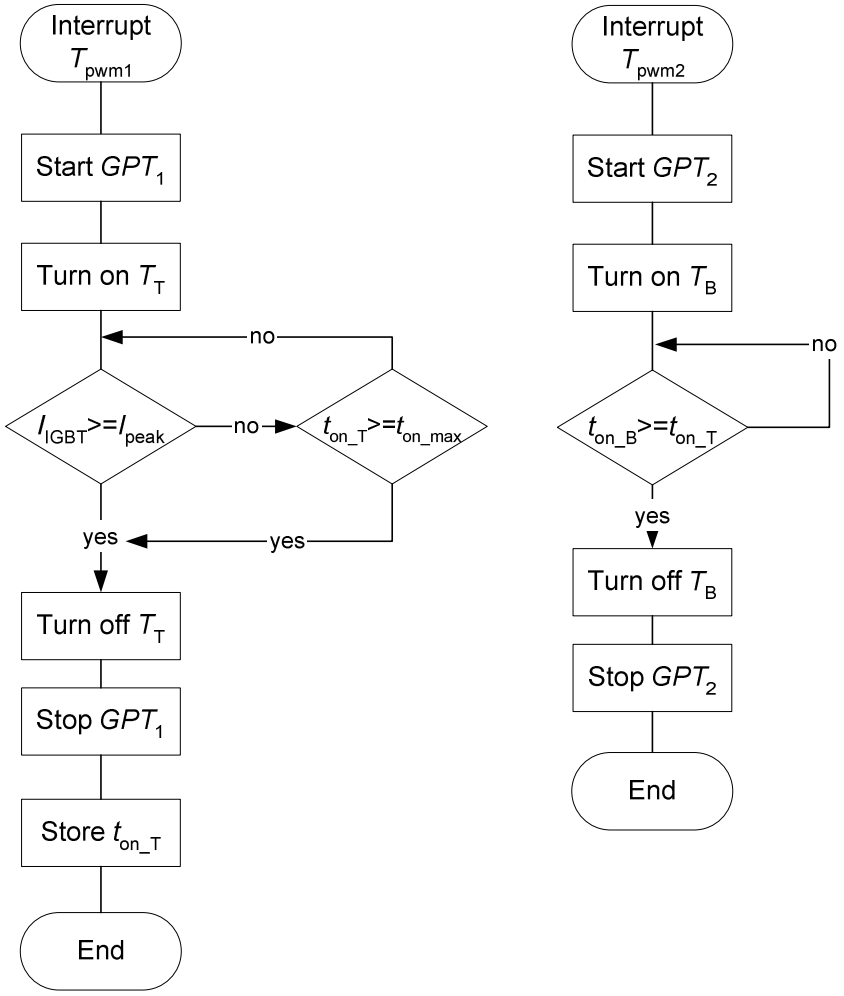
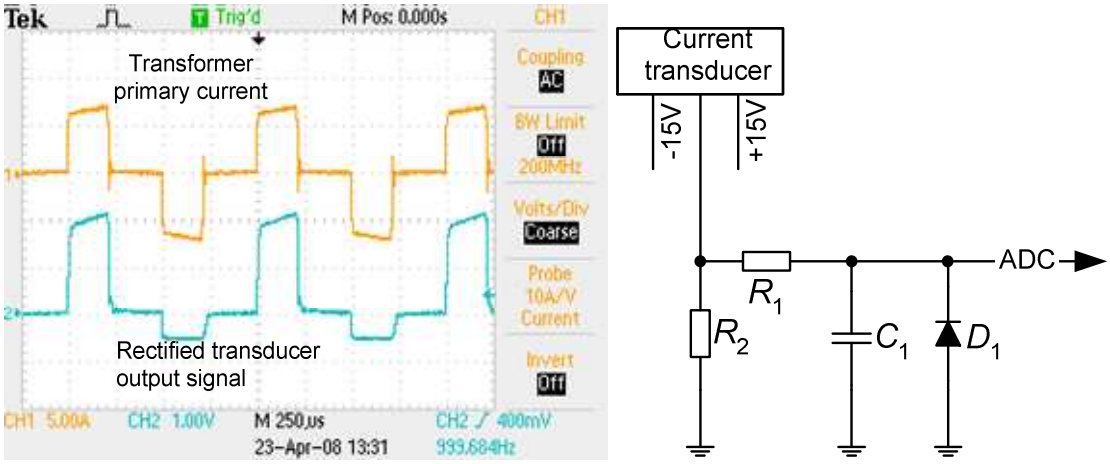


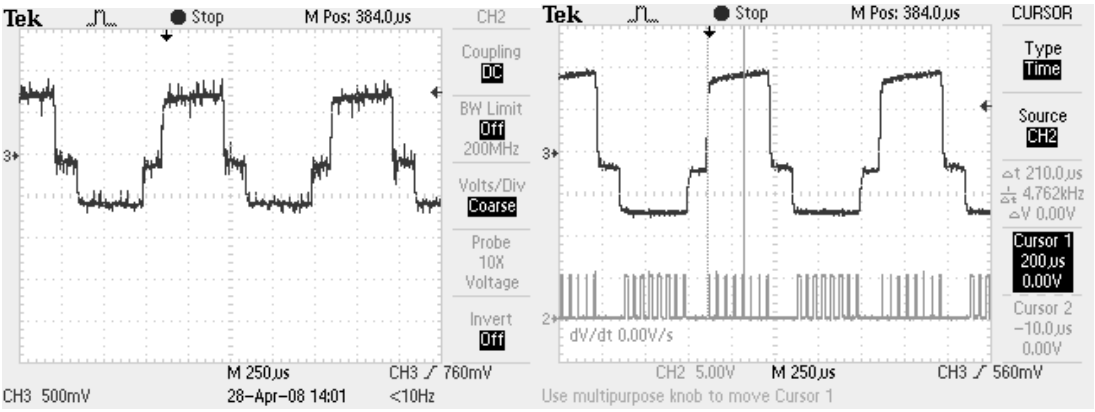
Fig. 2.22 Improved peak current mode control algorithm

The primary current of the transformer is an alternating current, as shown in Fig. 2.23 (a). According to the proposed control algorithm, only positive values of the transformer current should be measured. In the case of a current transducer a simple diode rectifier combined with a RC filter can be used, as shown in Fig. 2.23 (b). Peak CMC is highly sensitive to noise thus, correctly dimensioned filter is vital. In Fig. 2.24 the transducers output signal with and without RC filter are shown. As it can be seen, the filter substantially improves the signal quality.



(a) *(b)*

Fig. 2.23 Primary current and current transducer output signal (a), schematic of current transducer output signal rectifier and filter (b)



(a) *(b)*

Fig. 2.24 Output signal of the current transducer without the RC filter (a) output signal with filter (b)

Considering the facts that the voltage unbalance problem could be solved completely within the software without any additional hardware and the number of needed current measurement cycles was reduced, the proposed control method may look as a quite attractive solution for HP and HV applications. However, the resolution issue inherent to all digital control systems, still remains. The accuracy of the current measurement depends on the system clock frequency and A/D conversion speed. As a result also the maximal switching frequency of the converter will be limited. Moreover, high speed current measurement and A/D conversion essentially decrease the overall performance capability of a control unit. Considering the fact that modern HP and HV DC/DC converters have usually highly complicated control systems, where not only current needs to be measured, one may face the fact that one control unit is not enough to implement digital peak CMC.

Average Current Mode Control

The AVCMC is a typical two loop control algorithm (inner current loop, outer voltage loop). Most of the problems of the peak current mode control are solved in AVCMC. Since average current is measured, the control method is less susceptible against noise, the implementation of current error amplifier gives high current loop gain, in the output a regular pulse width modulator is used, which guaranties equal pulses for both transistors. This also eliminates volt-second unbalance problem.

Digital AVCMC can bring some more advantages. A control unit carries out the entire control method in software. Thus, the component number is considerably reduced, there is no ageing or drift of the components, the control system is reprogrammable, which makes the system more adaptable. Also, a variety of adaptive control schemes are possible. Digital AVCMC eliminates the gain restrictions of the current error amplifier and increases immunity against EMI. The biggest drawback of digital control is the need to sample and quantize parameters. It introduces a noticeable phase lag to the system and reduces measurement accuracy [41] [45][117]. In order to increase the accuracy, sample rate has to be increased. Sample rate is directly connected to the clock frequency of the control unit and cannot be increased endlessly. On the other hand, increasing the sampling rate can overload the control unit, which would reduce the overall performance of the system. In order to sustain the performance of a complex control system several control units may be necessary. Therefore classical approach of digital AVCMC is not an optimal solution for a modern HP and HV DC/DC converter.

An Improved Average Current Mode Control Algorithm for Digitally Controlled Half-Bridge Isolated DC/DC Converters

In the current thesis a new mathematical method for a digital AVCMC for HB isolated DC/DC converters was developed that allows reducing the sample rate of current measurement without resulting penalties in accuracy. The central idea is to exploit the linear nature of the current slopes. Instead of sampling and summing the inductor current over the switching period, the current is measured only twice per period. The method is based on the digital AVCMC described in [37]. The described method is applicable only for buck, boost and flyback topologies while the method proposed here can be applied on two level half-bridge and full-bridge converter topologies.

HB or full-bridge DC/DC converters have one distinctive difference from simple buck and boost topologies. They have an isolation transformer (Fig. 2.1) and instead of the inductor current the transformer primary current is measured. In order to calculate average value, the current must be rectified, which is not easy to do in high voltage and power applications [64]. Here another simpler method is proposed. Instead of primary current, the IGBT current (I_{IGBT}) is measured (Fig. 2.15). In the case of symmetrical PWM control the average

switch current is proportional to the rectified average primary current. The average current ($I_{IGBT-AV}$) through the respective inverter switch in the HB topology is

$$I_{IGBT-AV} = \frac{1}{T}\int_{t_1}^{t_2} I_{IGBT}(t)dt\,, \tag{15}$$

where T is the switching period, t_1 is the turn-on instant of a transistor, and t_2 is the turn-off instant of a transistor [118].

The rectified average current of the isolation transformer primary is

$$I_{Tr-p-AV} = \frac{2}{T}\int_{t_1}^{t_2} I_{IGBT}(t)dt\,, \tag{16}$$

As it can be seen, $I_{IGBT-AV}$ is twice lower than $I_{Tr-p-AV}$. Due to the symmetry it is irrelevant which current of both transistors will be measured.

The idea of the proposed digital AVCMC method is to measure I_{IGBT} only twice per switching period at the following instants: at the beginning of on-state time (I_1) and at the end of on-state time (I_2) of the IGBT, as shown in Fig. 2.25.

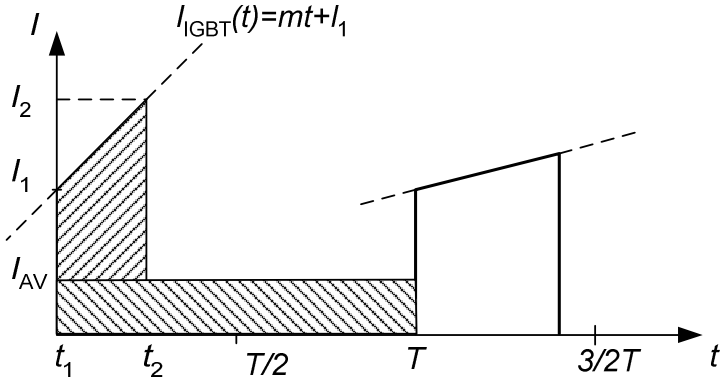


Fig. 2.25 Ideal IGBT current waveforms in a half-bridge or full-bridge converter

This control method assumes that the current slopes are linear. Then an average IGBT current can be easily calculated according to two measured current values. Since the current is always increasing linearly, the current function can be expressed with the linear equation as follows:

$$I_{IGBT}(t) = m \cdot t + I_1\,, \tag{17}$$

where m is the slope of the IGBT current $I_{IGBT}(t)$, t is time and I_1 is the IGBT current at the beginning of the on-state time. The current slope can be calculated as follows:

$$m = \frac{I_2 - I_1}{t_2 - t_1}, \tag{18}$$

where I_2 is the current value at the end of the on-state time, and I_1 is the current at the beginning of the on-state time. A change in the duty cycle results in a change in the current slope. However, the current retains its linearity. The average current can be found by solving the following integral:

$$I_{\text{IGBT}-\text{AV}} = \frac{1}{T_{\text{PWM}}} \int_{t_1}^{t_2} I_{\text{IGBT}}(t)dt = \frac{1}{T_{\text{PWM}}} \int_{t_1}^{t_2} (m \cdot t + I_1)dt =$$

$$= \frac{1}{T_{\text{PWM}}} \left[\int_{t_1}^{t_2} m \cdot t dt + \int_{t_1}^{t_2} I_1 dt \right] =$$

$$= \frac{1}{T_{\text{PWM}}} \left[\frac{m}{2}(t_2 - t_1)^2 + I_1 \cdot (t_2 - t_1) \right] =$$

$$= \frac{1}{2T_{\text{PWM}}} \left[\frac{I_2 - I_1}{t_2 - t_1} \cdot (t_2 - t_1)^2 + 2I_1 \cdot (t_2 - t_1) \right] =$$

$$= \frac{1}{2T_{\text{PWM}}} \cdot (t_2 - t_1) \cdot (I_2 + I_1), \tag{19}$$

where $I_{\text{IGBT-AV}}$ is the average IGBT current, T_{PWM} is the switching period of transistors. In the AVCMC, fixed frequency PWM control is used. Therefore the switching period and the duty cycle are known parameters. By measuring the current at the beginning and at the end of the IGBT on-state time, the average current can be calculated according to (19). However, one must consider that in Fig. 2.25 indicated current shape is ideal. The real current shape of a half-bridge converter includes overcurrent peaks at every turn-on instant and depending on the measurement equipment used, can have other abnormal components in the signal.

In order to achieve accurate timing of the digital regulator and synchronize it with other internal processes, interrupts were used. The interrupt timing diagram of the proposed digital AVCMC is shown in Fig. 2.26. The first interrupt (Int 1) is triggered by period match of the first PWM timer. The IGBT1 current I_1 is measured. The trigger sequence and duration of an interrupt routine are constant values. The duration of the interrupt routine depends on many factors like ADC speed, program structure etc. To avoid interrupt overlapping, the maximal duration of the first interrupt routine is limited with the minimum on-state time ($t_{\text{on-min}}$). The second interrupt (Int 2) will be triggered at the end of the duty cycle and the IGBT current I_2 will be measured. Since the duty cycle is changing ($t_{\text{on-min}}$ … $t_{\text{on-max}}$), the trigger sequence of the second interrupt is also variable, as shown in Fig. 2.26. The duration of the interrupt routine is limited and can be calculated as follows:

$$t_{\text{int}\,2} = \frac{T_{\text{PWM}}}{2} - t_{\text{on}-\max}\,, \tag{20}$$

where T_{PWM} is the switching period of IGBTs, $t_{\text{on-max}}$ is maximal on-state time of the IGBT. The third interrupt (Int 3), triggered by the period match T_{pwm2}, executes a regulator. Since the IGBTs of the opposite branches are switched symmetrically and with the same frequency, the trigger sequence of the Int 3 is constant and equals to the sequence of Int 1. The maximal duration of the third interrupt routine is limited with the half PWM period ($0.5T_{\text{PWM}}$).

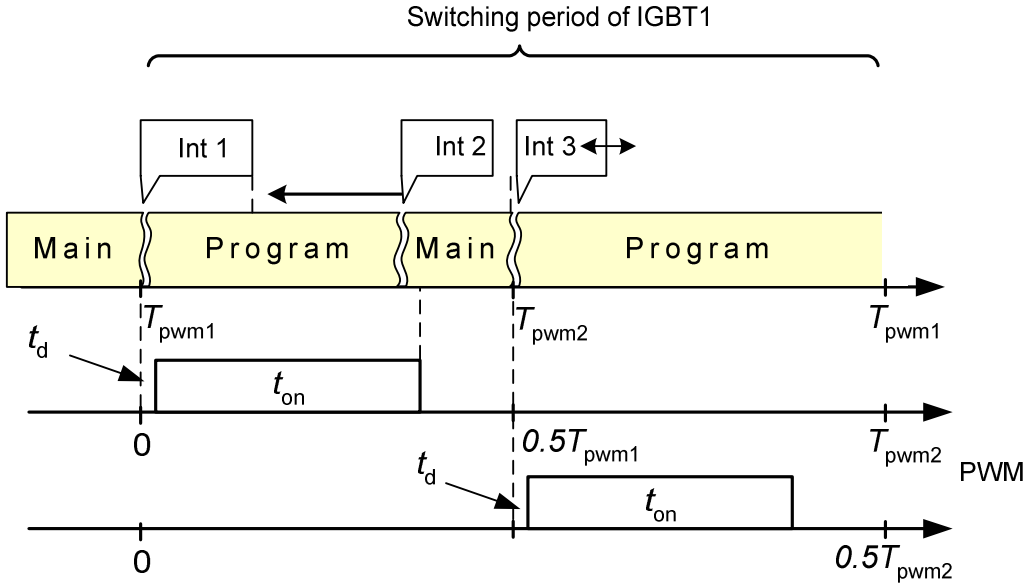


Fig. 2.26 Interrupt timings of the improved digital AVCMC

A general program structure is shown in Fig. 2.27. As it can be seen, the most vital functions of the converter (control of IGBTs and protection algorithms) are carried out within the main program. Interrupts are only used for processes that require precise timing. There are three interrupt sources: period match of the first PWM timer (T_{PWM1}), period match of the second PWM timer (T_{PWM2}), and period match of a GPT.

The first interrupt service routine (ISR) starts with calculating a new reload value for the GPT, as shown in Fig. 2.28. The reload value of the GPT is a variable that depends on the current duty cycle. The new value will be reloaded and the GPT started. As a next step, a small pause is generated to compensate the dead time (t_{d}) added to control signals and also possible current peaks occurring during turn-on. The software delay must be exactly as long as it is needed for the IGBT to fully open and start conducting. Accordingly, ADC is started and after completing the conversion of the IGBT current I_1, ISR returns to the main program.

The GPT will trigger the next interrupt (Int 2) slightly before turning off the IGBT, as shown in Fig. 2.26. This guarantees that the current peak is measured before the transistor is turned off and the current decreases to zero. Flowingly, ADC measures IGBT current I_2 and ISR returns to the main program.

The third ISR serves mainly to provide digital regulation and to calculate the new duty cycle for the switches. First, the outer voltage control loop provides a new current program for the inner current loop. The inner current control loop then calculates an average current according to (19). A digital current error amplifier compares the average current to the current program and on that basis calculates new duty cycles for the transistors. The HB is controlled symmetrically and the duty cycles are kept equal to each other.

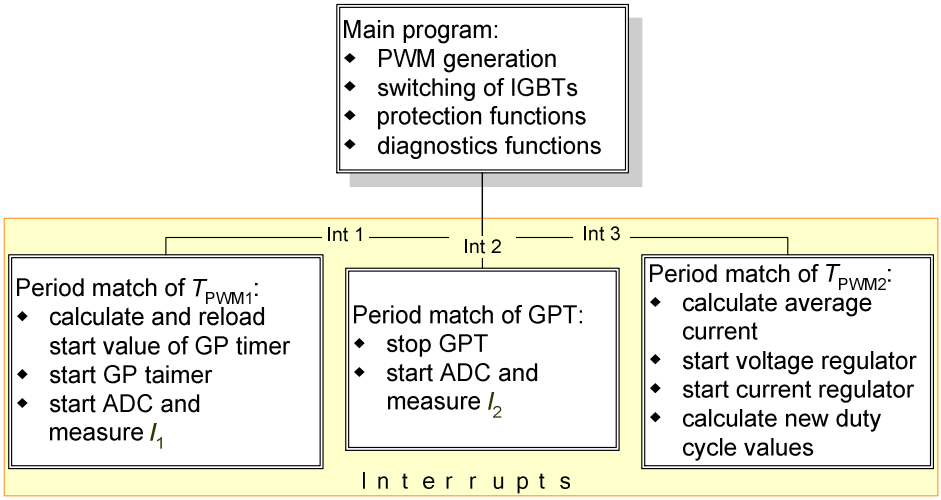


Fig. 2.27 Program structure diagram of a DC/DC half-bridge converter controlled with the improved AVCMC

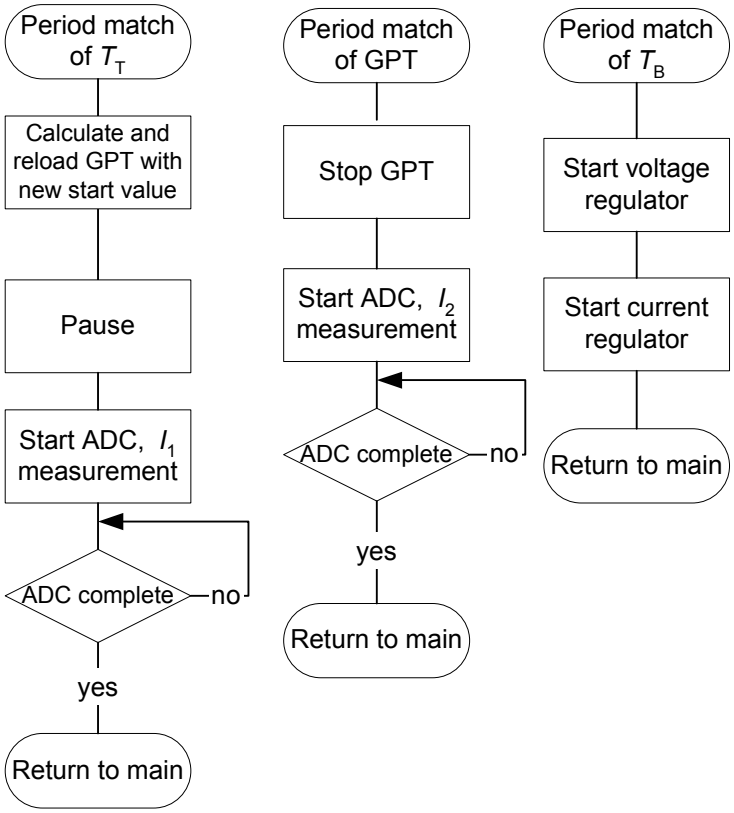


Fig. 2.28 Flow charts of interrupt service routines for improved AVCMC

A drawback of the proposed control method is that it is only suitable for converters where the current is growing linearly. This raises a question of how to build an appropriate converter. In order to answer that question, it is necessary to find out the parameters that the current depends on. In the CMC, the current is measured. Depending on the topology, it can be an inductor or a transformer primary current. The current slope though an inductor or a transformer primary can be calculated as follows:

$$\frac{di}{dt} = \frac{U}{L}, \tag{21}$$

where *di/dt* is the current slope, *U* is the voltage across the winding, and *L* is the inductance of the winding. The digital AVCMC proposed in this paper assumes that the current increases linearly over the on-state time. The term linearity refers to the constant current slope. According to (21), a constant slope is only achieved if the ratio U/L remains constant. The terminal voltage *U* of an inductor or a transformer primary depends on the input voltage and on the duty cycle of the converter. The duty cycle is constant over a switching period. The input voltage change during a switching period is usually small so that U can be considered as constant. Also, inductance must remain constant. The inductance of the winding can be calculated as follows:

$$L = \frac{n \cdot \Phi}{i}, \tag{22}$$

where Φ is the magnetic flux through the area spanned by the current loop, *n* is the number of wire turns, and *i* is the loop current. In order to keep the inductance constant, the ratio between the magnetic flux and the loop current (Φ/i) must remain constant. Transformers and inductors with ferromagnetic cores operate linearly as long as the current through them is not large enough to drive their core materials into saturation. Saturation destroys the balance between the flux and the current, resulting in an inductance change. It is clear that one key element to success is an optimally designed transformer or inductor. Main attention here must be paid to the selection of the proper material for the magnetic core and to define an optimal operating flux density to minimize the dimensions and to improve operability and efficiency of the transformer, respectively [115].

The simulations were carried out with the simulation software *Simplorer*. The model of the HB isolated DC/DC converter is shown in Fig. 2.29. In order to simplify the simulation, ideal semiconductor devices and a non-saturable isolation transformer were used. The IGBTs are controlled with PWM method. The switching frequency is 1 kHz. The input voltage U_{in} is 1 kV. The transformer has the following parameters: a saw tooth generator changes magnetizing inductance 12…100 mH, primary leakage inductance is 30 μH and secondary leakage inductance is 1 μH. The input capacitors C1 and C2 are identical. Since the leakage inductance of the primary is negligibly small

compared to the magnetizing inductance, it does not affect the current shape. However, increase in the magnetizing inductance decreases the current slope, as shown in Fig. 2.30. The magnetizing inductance is changing in saw tooth shape while the current increases exponentially.

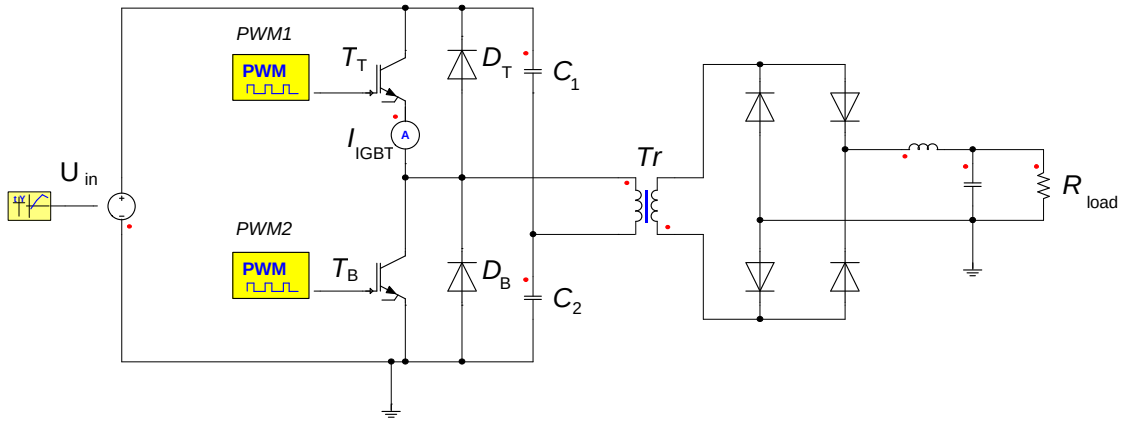


Fig. 2.29 Simulation model of the half-bridge DC/DC converter

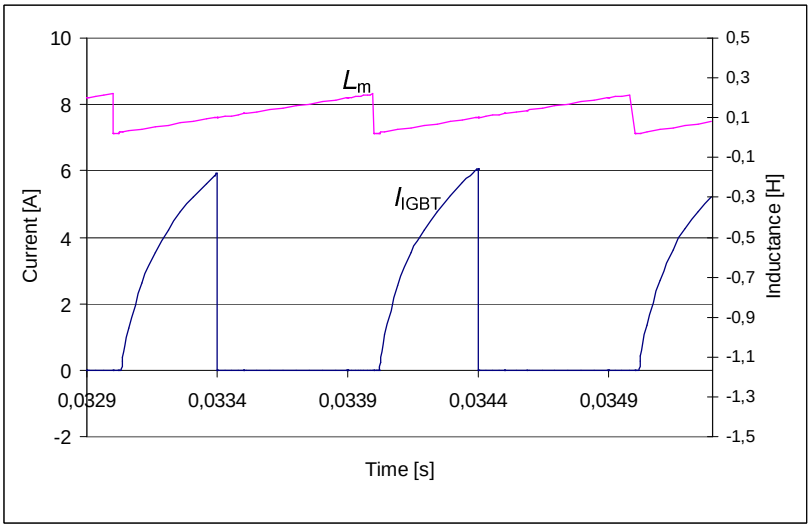
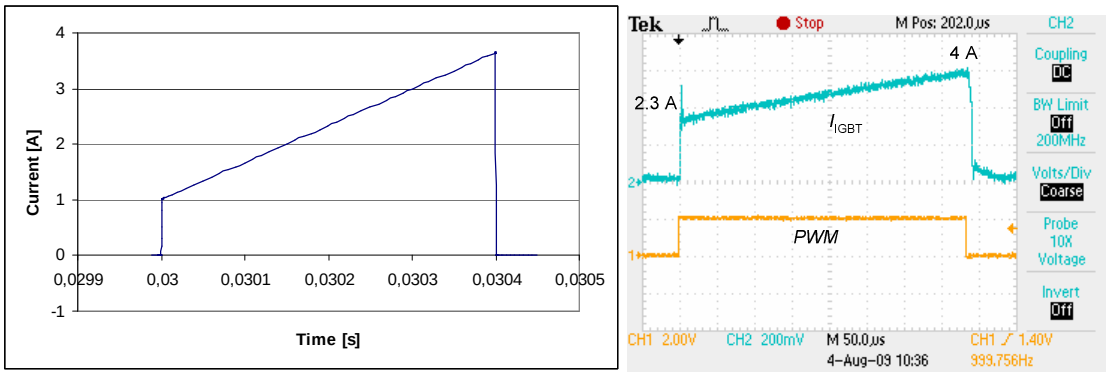
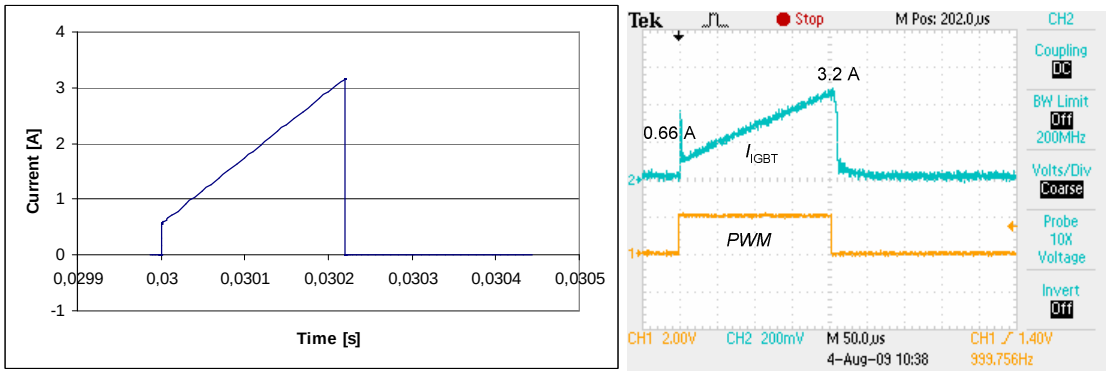


Fig. 2.30 Variable magnetizing inductance and IGBT current with non-linear slope

In order to demonstrate the influence of the duty cycle on the current shape, following simulations and tests were carried out: without changing any electrical parameters, the duty cycle was reduced from maximum 0.4 to minimum 0.2 resulting in an increase of the current slope, as shown in Fig. 2.31.



(a)



(b)

Fig. 2.31. IGBT current: duty cycle D=0.4 (a), duty cycle D=0.22 (b)

Since I_{IGBT} is measured only twice per period, it is vital to have a clear current signal. Secondly, the timing of interrupts should be accurate. In order to visualize trigger instants of interrupts, a general purpose digital output of the control unit was toggled synchronously to the interrupts. The resulting impulses are equal to a corresponding interrupt routine duration (Fig. 2.32). A period match of the PWM timer generates the first interrupt. The correct timing for current measurement can be seen in Fig. 2.32. Since the IGBT is turned on with a small delay then the first interrupt is generated before the current starts to grow. This delay and also the current peak at the beginning of turn-on are compensated with the pause function of the ISR (see Fig. 2.28). The second interrupt occurs slightly before turning off the transistor. The interrupt is triggered by a GPT.

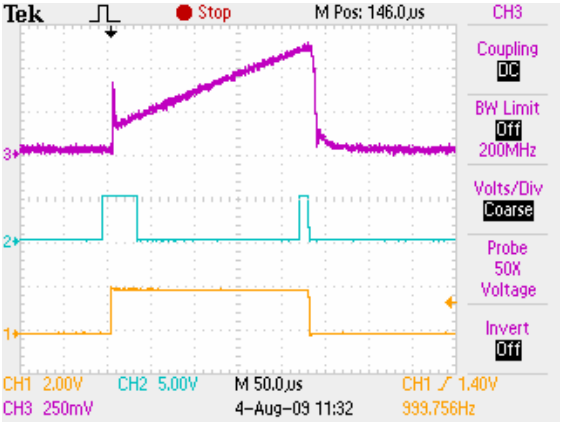


Fig. 2.32 Correct timing of interrupts: CH1 – PWM control signal, CH2 – interrupt service routine duration and trigger instants, CH3 – IGBT current

The accuracy of the proposed control method was verified by importing oscilloscope data into MS Excel where the average current could be calculated using classical integration methods. The current was also calculated using the proposed simplified digital AVCMC equation (19). Comparison of results is shown in Table 7. As it can be seen, in the case of maximal duty cycle the difference between Excel results and those that where obtained with improved AVCMC is only 0.002 A. In the case of minimum duty cycle the difference is slightly bigger 0.004 A.

Table 7 Comparison of results

Duty cycle	**0.4**	**0.22**
Average current with Excel	1.262 A	0.429 A
Average current with Eq. (19)	1.260 A	0.425 A

The proposed digital AVCMC has the following benefits:

- simple equation for average current calculations;
- reduced sample rate, i.e. only two current measurements per duty cycle are needed, resulting in a less loaded microcontroller;
- increased noise immunity due to the lower sampling rate.

Drawbacks are:

- high speed current measurements required;
- applicable only in the case of linear current slope.

Voltage Mode Control

VMC or direct duty cycle control is one of the simplest control algorithms. It is a single loop control method where only output voltage is measured. It can be easily implemented in a HB topology, as shown in Fig. 2.33. The regulator output is connected to the PWM blocks, which create two 180 degree phase shifted PWM signals. The duty cycle of both transistors (T_T and T_B) is kept equal to prevent volt-second unbalance in the transformer primary.

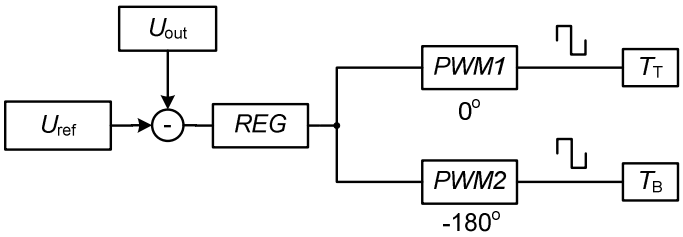


Fig. 2.33 Voltage mode control principle for the half-bridge isolated DC/DC converter

The main limitation of VMC is its slow response to sudden input changes. In some cases it can be compensated with higher loop gain but commonly VMC is best suitable for applications with no input changes. Unfortunately in the current case the converter has to work in combined regulation conditions where both input voltage and output load can change simultaneously. Therefore, the VMC suitability is questionable. However, VMC as one of the simplest control algorithms would be a good candidate for railway applications where simplicity and reliability are the major priorities.

A powerful method to test system dynamic behaviour and overall control loop response is the transient response analysis. In cases of combined regulation, two transient tests should be carried out: input voltage and load transient response.

First, open loop transient responses were considered. The computer model used in the simulations is shown in Fig. 2.34.

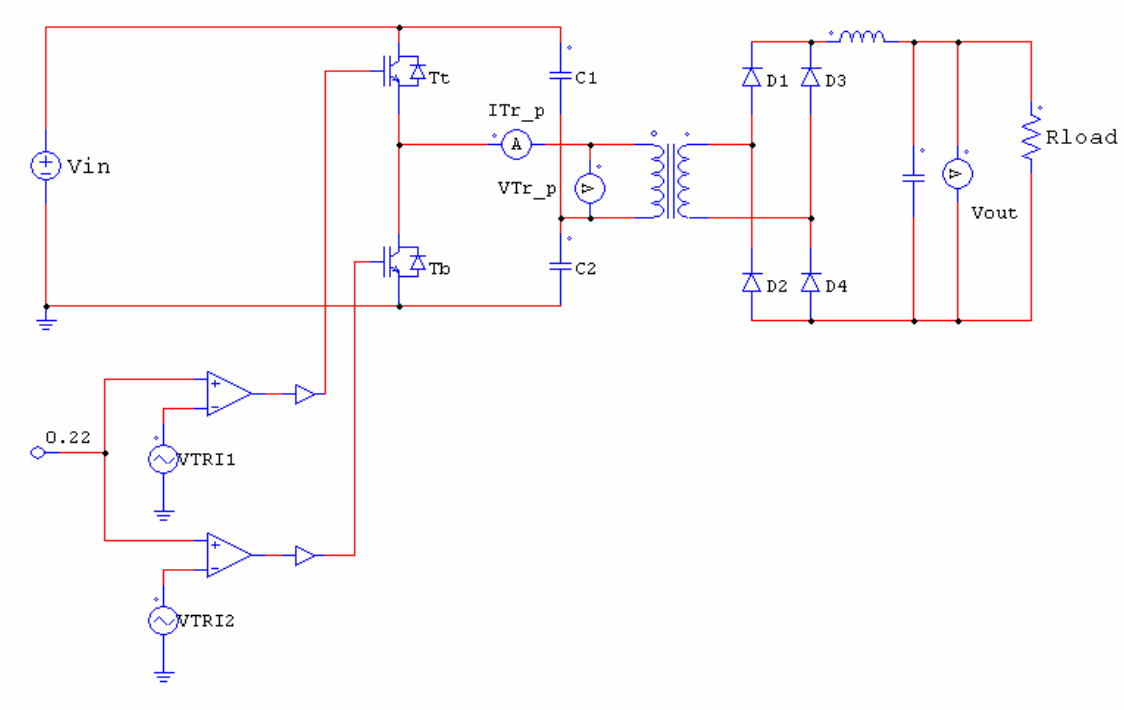


Fig. 2.34 Open loop model for transient response simulations

In order to obtain the open loop input voltage transient response, the following modifications to the model were made: the input of the converter (V_{in}) was

replaced with a square wave voltage source with the output voltage range 2200…4000 V, the duty cycle and load were chosen so that at maximal input voltage the nominal output voltage (350 V) in maximum load conditions (50 kW) could be achieved. The results are shown in Fig. 2.35. The output voltage waveform (V_{out}) shows a stable output with a good input damping, which is caused by the low pass output filter. According to that, good closed loop behaviour could be assumed.

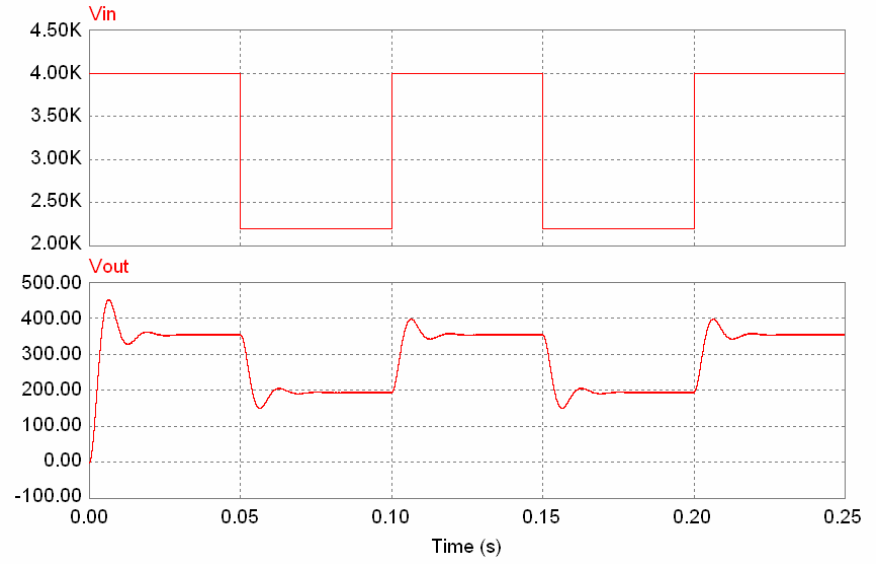


Fig. 2.35 Open loop response to input voltage transients

In order to obtain an open loop load transient response, the following modifications to the computer model (Fig. 2.34) were made: the input voltage was set to minimum 2200 V, the duty cycle was chosen so that nominal output voltage could be achieved, and the load was changed periodically between 10 % and 100 %. The results are shown in Fig. 2.36. The waveform shows somewhat overdamped response, which, although very stable, does not give the best transient recovery performance.

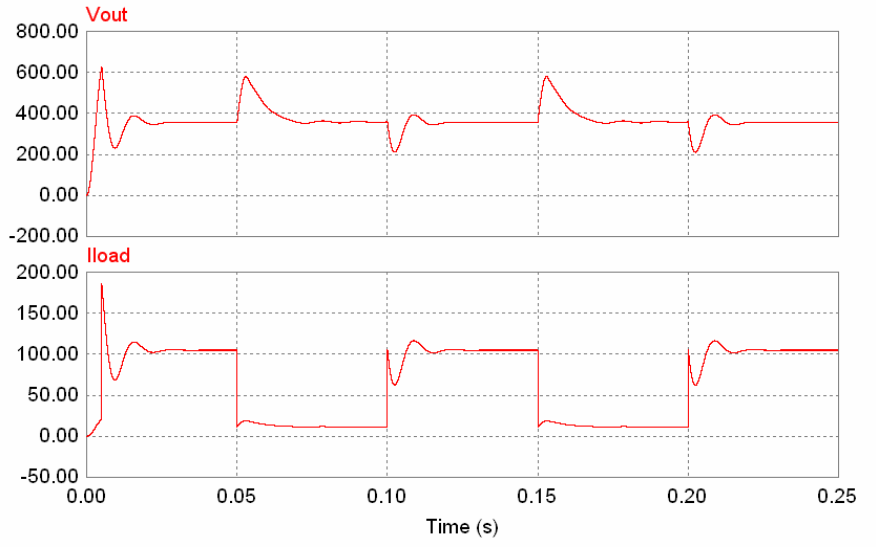


Fig. 2.36 Open loop response to load transients

Flowingly, the closed loop behaviour of the DC/DC converter will be examined. In this case the most important parameter to be estimated is the output voltage fluctuation, which must remain inside predefined limits (350 V±17.5 V). Type II compensation was used to regulate the output voltage. The computer model used for the simulations is shown in Fig. 2.37.

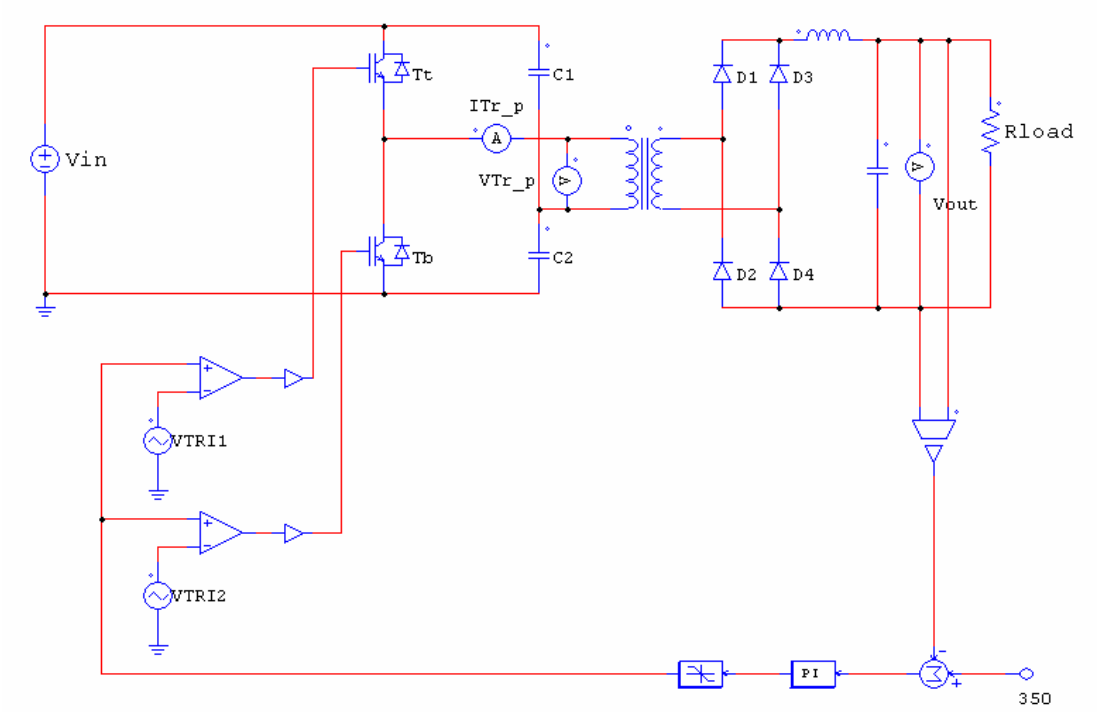


Fig. 2.37 Closed loop model for transient response simulations

In order to obtain the closed loop input voltage transient response, the following modifications to the model were made: the input voltage source (V_{in}) was changed to a square wave voltage source with the output voltage range 2200…4000 V, the fixed load resistor was chosen so that the full output power (50 kW) could be achieved. The results are shown in Fig. 2.38. As expected, the converter sustains very good and stable output voltage despite the input transients. Therefore, the pure input regulation inherent to VMC is not a problem in terms of the current hardware configuration. The output low pass filter damps fast input transients so that they can be easily compensated by the output voltage regulator.

In order to obtain the closed loop load transient response, the following modifications to the computer model (Fig. 2.37) were made: the input voltage was set to 3000 V, the load was increased in 30 % steps until the full load. The output voltage and the load current are shown in Fig. 2.39. The output voltage wave form shows some fluctuations caused by the steady state error but in general the output remains stable within allowed limits.

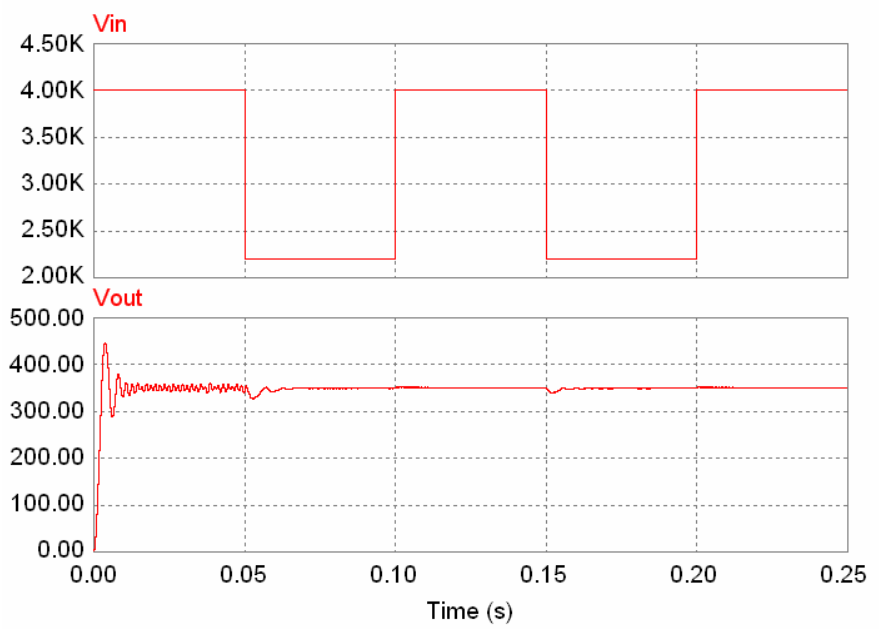


Fig. 2.38 Closed loop response to input voltage transients

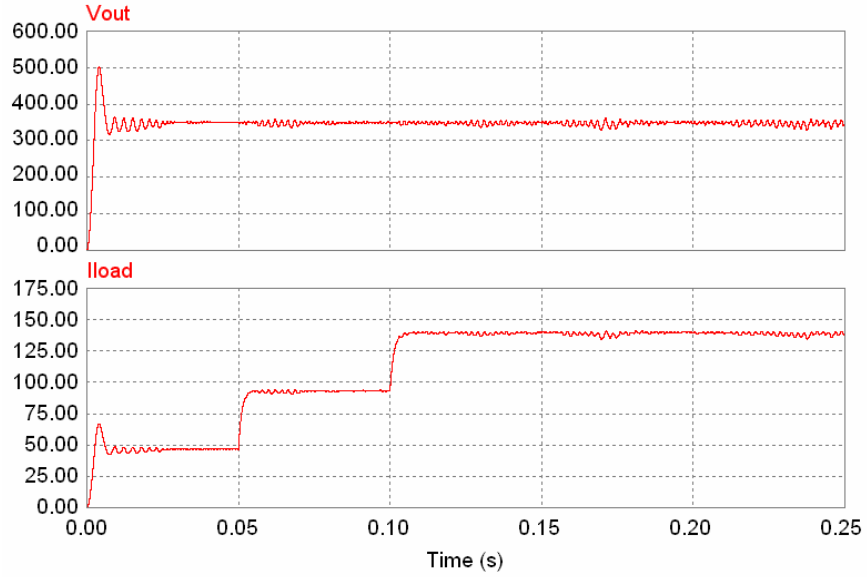


Fig. 2.39 Output voltage of the converter under pulse loading and closed loop conditions

There is another aspect that needs to be taken into account by VMC. The principle of PWM is shown in Fig. 2.40. A saw-tooth signal with fixed amplitude U_{ramp} was generated and compared to a compare value U_{cp}. The resulting duty cycle can be calculated as follows:

$$D = \frac{t_{\text{on}}}{T_{\text{PWM}}} = \frac{U_{\text{cp}}}{U_{\text{ramp}}}. \tag{23}$$

Substituting (23) into (4), the pulse width modulator gain of the converter can be calculated as

$$U_{\text{out}} = \frac{U_{\text{cp}}}{U_{\text{ramp}}} \cdot \frac{U_{\text{in}}}{n}$$

$$\frac{U_{\text{out}}}{U_{\text{cp}}} = \frac{1}{n} \cdot \frac{U_{\text{in}}}{U_{\text{ramp}}}. \tag{24}$$

The result is that in a fixed ramp PWM topology the modulator gain and therefore also the total gain of the control loop depends on the input voltage. The loop gain and bandwidth increase with the increase of the input voltage. This makes the loop compensation slightly more complicated.

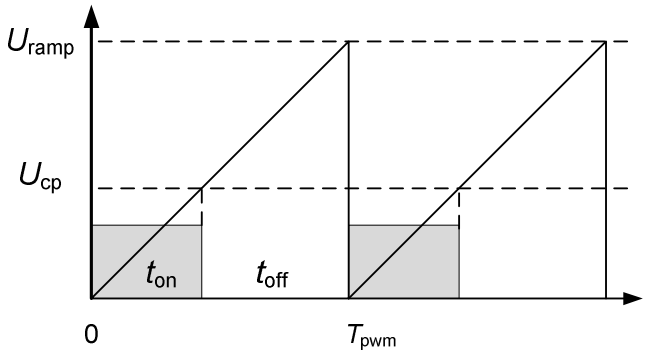


Fig. 2.40 The principle of the fixed ramp PWM generation

VMC has the following benefits:

- simple to implement, lower costs;
- voltage sensing is easier and more efficient than current sensing;
- smaller noise susceptibility compared to CMC;
- single feedback path is easier to design;
- increased reliability due to simplicity.

Some limitations are:

- poor input transient response;
- loop gain and bandwidth depend on the input voltage;
- it is difficult to optimize compensation loop gain over the entire input voltage range.

Feed-Forward Voltage Mode Control

Conventional voltage mode control uses a fixed ramp signal for PWM. Since the only feedback signal comes from the output, this results in inferior line regulation. In feed forward VMC the ramp of the triangle waveform changes with the input voltage, as shown in Fig. 2.41. Hence the regulator changes the

duty cycle before an error occurs at the output and the line transient response is improved.

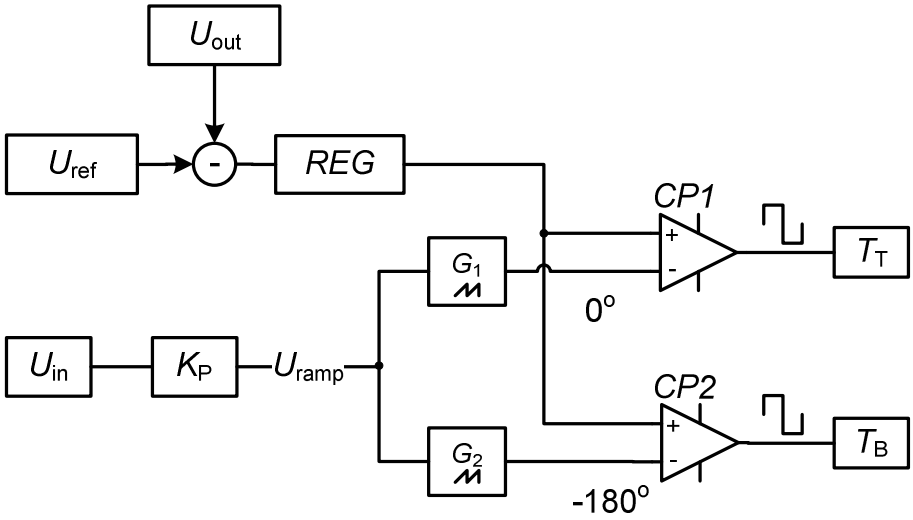


Fig. 2.41 Feed forward voltage mode control for the isolated DC/DC half-bridge converter

Usually the ramp is changed with a fixed gain (K_P), as shown in Fig. 2.41. The amplitude of the saw-tooth signal can be calculated as

$$U_{\text{ramp}} = K_P \cdot U_{\text{in}} . \tag{25}$$

Substituting (25) into (24), the feed forward gain of the modulator can be calculated as

$$\frac{U_{\text{out}}}{U_{\text{cp}}} = \frac{1}{n} \cdot \frac{U_{\text{in}}}{K_P \cdot U_{\text{in}}} = \frac{1}{n \cdot K_P} . \tag{26}$$

As it can be seen, feed forward VMC removes the variable loop gain and bandwidth of the control loop, which allows loop gain to be optimized over the entire input voltage range.

However, changing the ramp in cases of digital control is complicated. The saw-tooth signal in digital control systems is usually generated by PWM timers. The period of the timer determines U_{ramp} and compare registers are used for U_{cp} values. The problem is that the period register also determines the PWM period. In order to sustain a constant PWM period but change U_{ramp}, also the timer clock frequency must be changed in contrast to U_{ramp}. All microcontrollers have prescalers for such purposes but since the resolution usually remains under 3 bit, it does not provide enough bandwidth for the control loop.

There is another feed forward technique available, which is especially useful for digitally controlled DC/DC converters. It is based on the fact that commonly the transfer function of a DC/DC converter is known. Thus, the output voltage can be calculated in terms of input voltage, duty cycle and transformer turns

ratio. Rearranging (4), the duty cycle of the isolated DC/DC HB converter can be calculated as follows:

$$D = \frac{U_{\text{out}} \cdot n}{U_{\text{in}}}. \tag{27}$$

The output voltage and turns ratio of the transformer remain constant while the input voltage is changing. Input feed forward will be added parallel to the output voltage control loop, as shown in Fig. 2.42. The output control loop will compensate the load changes and the feed forward compensator (W_1) calculates the correct duty cycle with respect to the input voltage.

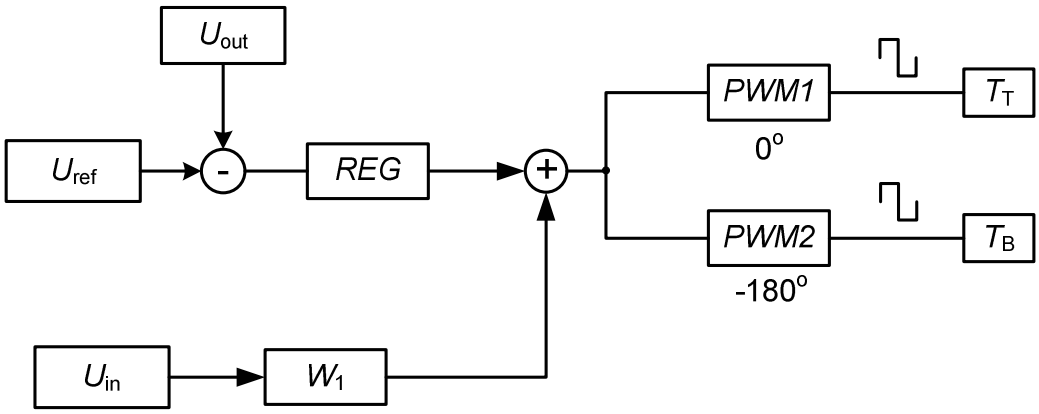


Fig. 2.42 Feed forward mode control scheme for the isolated DC/DC half-bridge

The effect of the feed forward regulator becomes clear when looking at the input voltage transient response. The simulation model is shown in Fig. 2.43.

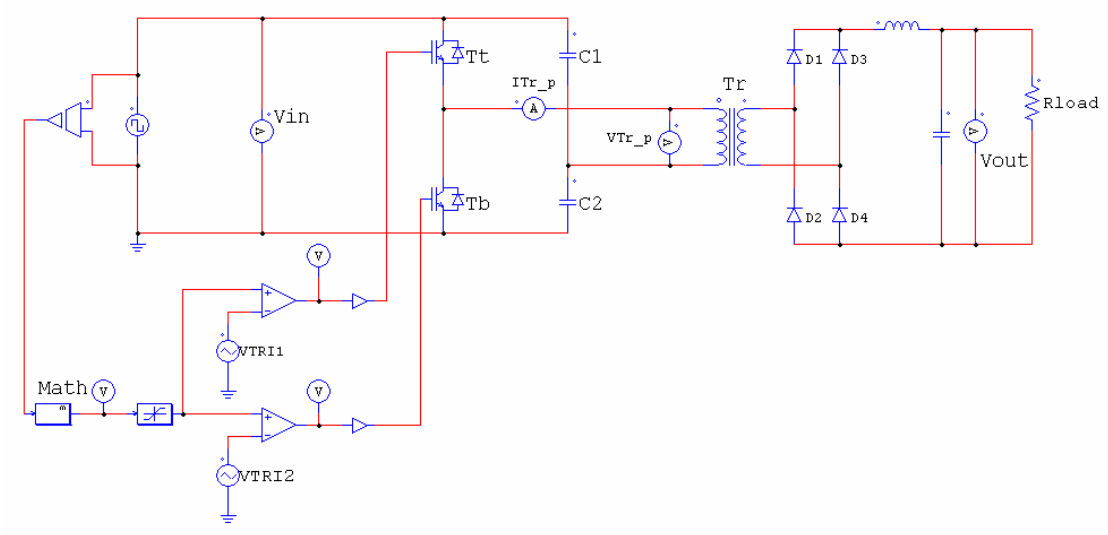


Fig. 2.43 Feed forward mode control model for the simulation of the input transient response ˇ

The input voltage source is a square wave signal generator with an output voltage range 2200…4000 V, the load was chosen so that at the nominal output

voltage (350 V), the maximum output power 50 kW could be achieved. The load remains constant, hence the output control loop is excluded from the simulation. Simulation results are shown in Fig. 2.44. Compared to the normal VMC (Fig. 2.38) some improvements can be noticed. The feed forward compensator lowers voltage peaks that are caused by input voltage transients and also reduces the overall voltage ripple. Whether to use this algorithm or not depends on the experimental results carried out with the normal VMC. If the results are satisfying, the VMC, which is simpler and requires fewer sensors, should be preferred.

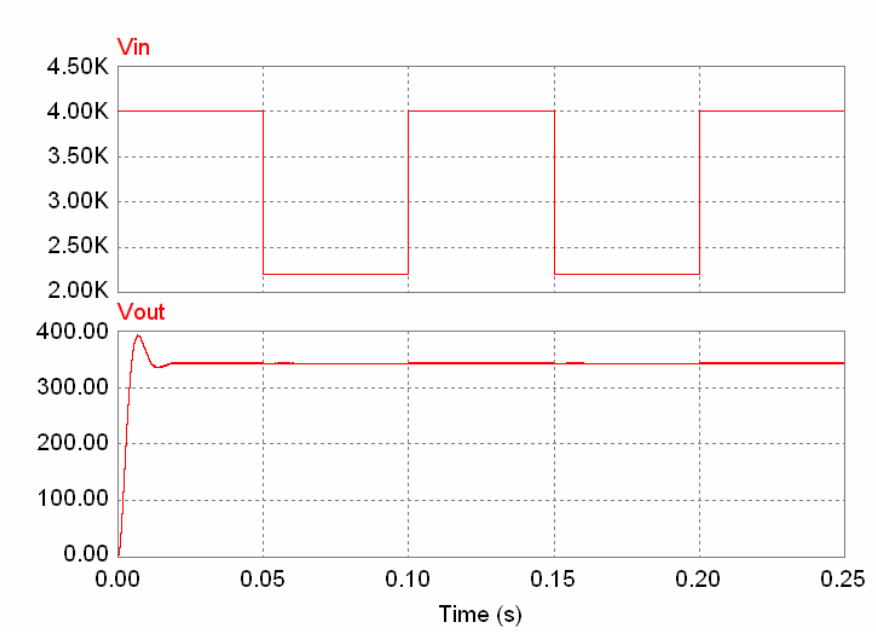


Fig. 2.44 Feed forward response to the input voltage transient

Feed forward VMC has the following benefit:

- improved line transient response.

Drawbacks:

- increased number of sensors;
- more calculation capability needed.

2.3 Front-End Converter for Traction Applications Based on the Three-Level Half-Bridge Topology

Implementation of 6.5 kV IGBT modules in two-level HB topology can give many advantages as reported in previous chapter. However, there are also some drawbacks. High price of the IGBTs and drastic switching losses reduce the benefits imposed by 6.5 kV IGBTs. An interesting alternative is a three-level isolated DC/DC HB converter, which has already demonstrated its obvious benefits in several low-voltage low-power applications [118]. It has some

important advantages over a traditional half-bridge: instead of two switches, a three-level isolated DC/DC HB uses four, i.e. the voltage stress of a switch is two times lower. Thus, two times lower blocking voltage capability is required and with the implementation of 3.3 kV IGBT modules, the switching frequency can be increased at least two times [120].

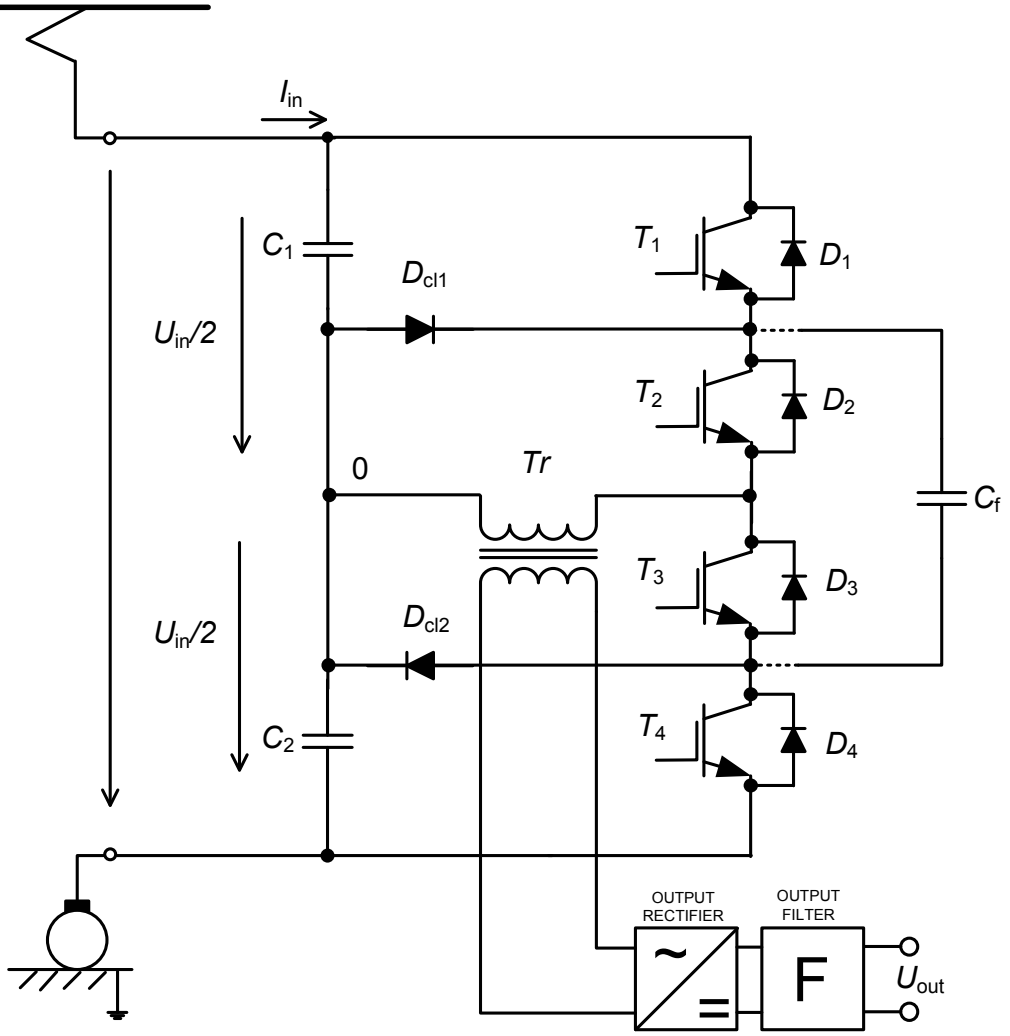


Fig. 2.45 Isolated DC/DC front-end converter for traction APS based on three-level half-bridge topology

A simplified circuit diagram of a rolling stock front-end converter based on the three-level isolated DC/DC HB topology is shown in Fig. 2.45. Instead of two switches four switches $T_1 \ldots T_4$ are used. The input capacitors C_1 and C_2 divide the input voltage U_{in}. The isolation requirement is fulfilled by a transformer *Tr*. The input of the converter is to be directly feed form the catenary voltage (2200 V…4000 V). The secondary voltage of the isolation transformer is rectified and filtered. Typical to a multilevel converter is increased number of clamping components: two clamping diodes D_{cl1}, D_{cl2} and a flying capacitor C_f (optional). In general there are three types of camping methods: diode clamping, capacitor clamping and combination of diode and capacitor clamping. The diode clamping is the most robust and reliable method. The capacitor clamping

method is seldom used due to the large current rating of the flying capacitor, the combination of the diode and flying capacitor clamping method combines the advantages of both methods but has increased component count. Usually the clamping method will be selected according to the control method of the converter [121]. Technical specification of the investigated three-level HB isolated DC/DC converter is presented in Table 8.

Table 8 Technical specifications of the front end converter based on three-level half-bridge topology

Parameter	**Value**
Long-term minimal input voltage $U_{\text{in-min}}$, kV	2.2
Long-term maximal input voltage $U_{\text{in-max}}$, kV	4.0
Rated output power P_{out}, kW	50
Switching frequency f_{sw}, kHz	4
Converter output voltage U_{out}, kV	0.35 ±5%
HV IGBT modules	Dual FF200R33KF2C

2.3.1 Comparative Analysis of Modulation Methods and Soft Switching Techniques for Three-Level Half-Bridge Inverters

There are several soft switching methods for multilevel HB topologies, which do not require any additional components. All those soft switching techniques depend on the modulation method. Hence, modulation methods are also connected to different switching losses. In order to find out optimal solution for current application, a detailed analyses was carried out.

At the rated load, a converter should perform regulation between two boundary points i.e. long term minimal and the long-term maximal input voltage values (Table 6). To maintain the constant output voltage at the rated load, the maximum duty cycle should always be associated with the minimum input voltage in normal steady-state operation, while the minimum duty cycle should correspond to the maximum input voltage. These two boundary operating points determine the regulation range of the converter and thus, will be used for further analysis and discussions.

In general, two modulation methods are available for multilevel HB converters: PWM and PSM. The principle PWM method for a three-level HB isolated DC/DC converter is shown in Fig. 2.46. A three-level HB inverter has two additional IGBTs, as compared to the two-level HB. However, this does not necessarily increase the complexity of the control system in terms of software. The two additional IGBT control signals can be derived within the hardware simply by inverting two PWM base signals, as shown in Fig. 2.46. Thus, the microcontroller only generates two 180 ° phase shifted PWM base signals (*PWM1* and *PWM4*). *PWM2* is derived by inverting *PWM4* and similarly *PWM3* is derived by inverting *PWM1*. Each PWM signal controls an individual switch. The IGBTs will be turned on and off one after the other. Since the IGBTs are

not ideal switches and have a certain turn-on and turn-off delay time, the situation can occur where three devices T_1, T_2, T_3 or T_2, T_3, T_4 are simultaneously conducting. Having three devices conducting at the same time would result in short circuit of the corresponding input capacitor C_1 or C_2 and the IGBTs would be destroyed. In order to prevent short circuit it is necessary to add a dead time t_d at the beginning of every signal, as shown in Fig. 2.46. The exact operational principle of a PWM controlled three level HB is described in [118].

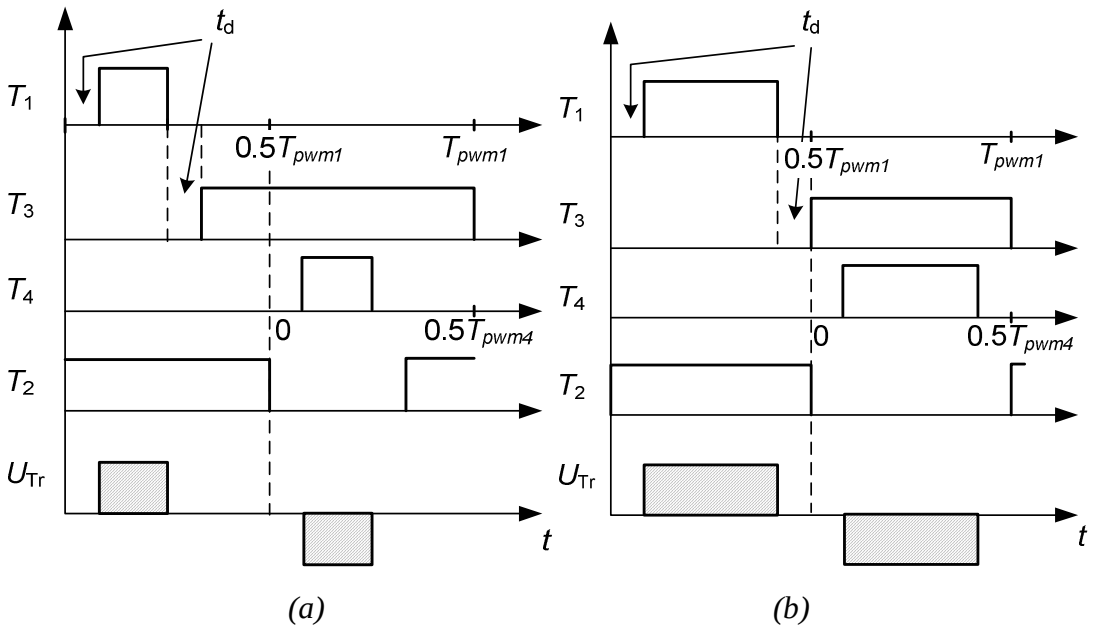


Fig. 2.46 PWM method for the three-level isolated DC/DC half-bridge converter: maximum input voltage (a) and minimum input voltage (b)

An alternative to PWM is the PSM method. In PSM all switches operate with duty cycle nearly 0.5. The phase-shift between signals *PWM1* and *PWM4* or *PWM2* and *PWM3* determines the operating duty cycle of the converter, as shown in Fig. 2.47. Theoretically only two independent PWM channels of the microcontroller are needed. Two additional channels can be derived within hardware by inverting the base PWM signals, e.g. T_4 can be seen as an inversion of T_1 and T_3 as an inversion of T_2. Each PWM signal controls an individual switch. In order to prevent cross conduction and overvoltages, a dead time t_d is added at the beginning of each control signal, as shown in Fig. 2.47. The exact operating principle is described in [54]-[56].

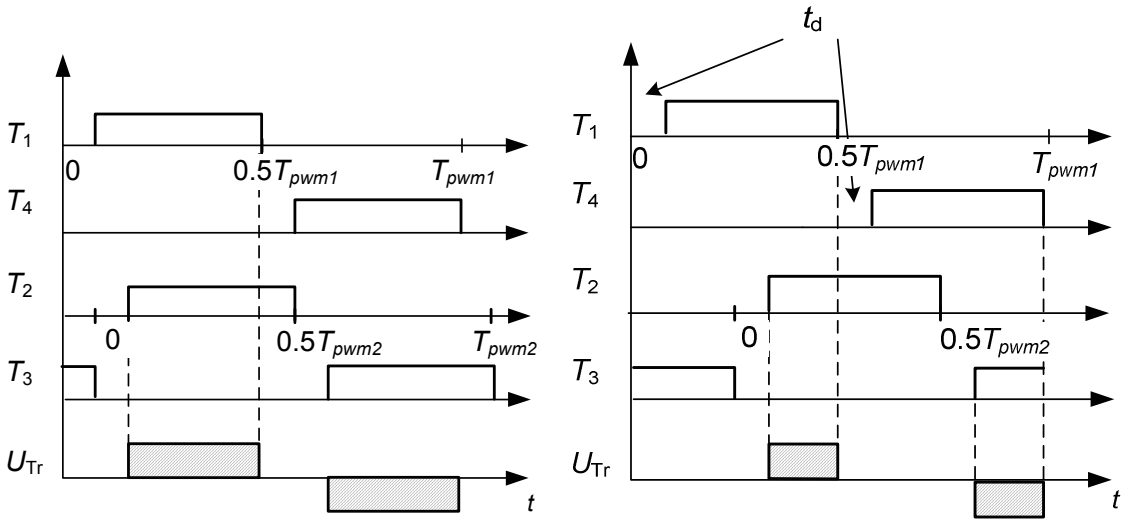


Fig. 2.47 PSM method for the three-level isolated DC/DC half-bridge converter: maximum input voltage (a) and minimum input voltage (b)

The computer model of the three-level isolated DC/DC HB converter that was used in the analysis is shown in Fig. 2.48. The same model was used for both control schemes: PWM and PSM. However, in the case of PWM control scheme, the flying capacitor (C_f) was excluded from the model. The IGBTs are controlled by four corresponding PWM signals. The switching frequency is 4 kHz. The input capacitors C_1 and C_2 are identical each 300 µF. In order to simplify the simulation, ideal semiconductor devices and a non-saturable isolation transformer were used. The simulations were performed at the rated load conditions (i.e. with the constant output power 50 kW) and in two boundary operating points described above.

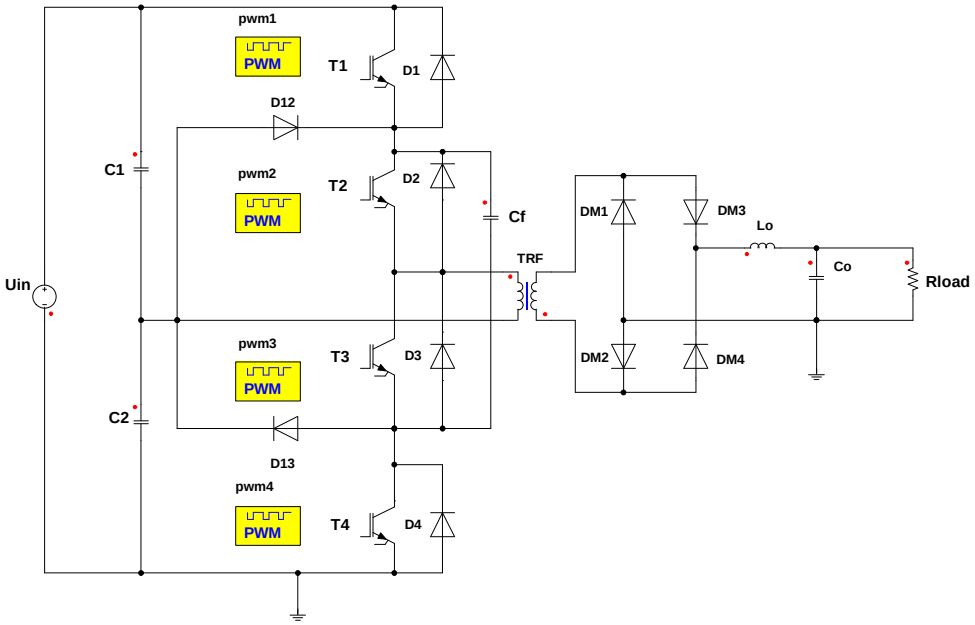
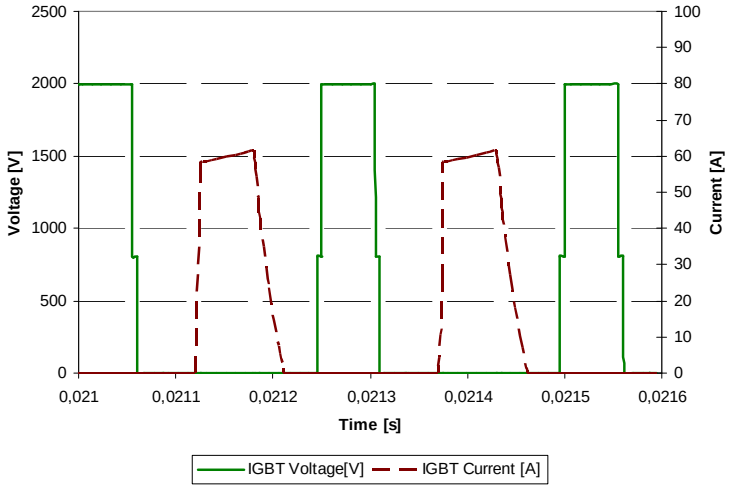


Fig. 2.48 Computer model of the three-level isolated DC/DC half-bridge converter

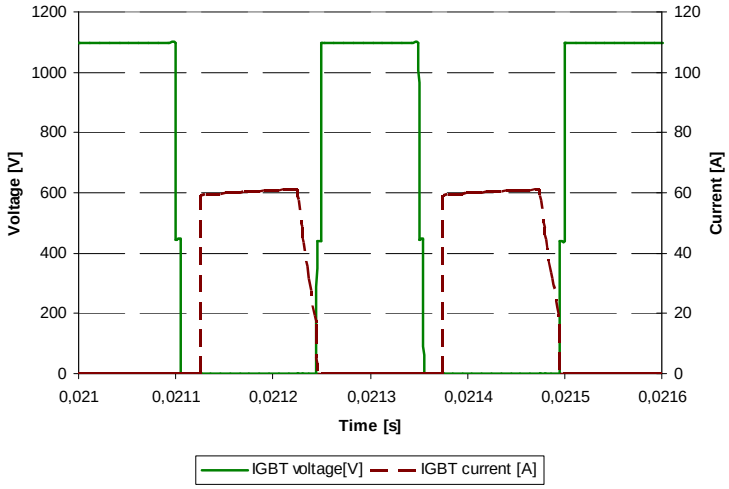
PWM method

The computer model is shown in Fig. 2.48 (excluding the flying capacitor C_f). The transistors are controlled according to timing diagrams, as shown in Fig. 2.46. Two independent PWM channels are required for the control scheme, as explained above. Two additional channels can be derived by inverting the base PWM channels.

If the leakage inductance of the isolation transformer is relatively small (1 µH …2 µH), ZVS and ZCS can be achieved for inner switches (T_2 and T_3) even at relatively low switching frequencies (4 kHz), as shown in Fig. 2.49. However, it can only be reached for a certain regulation range. Decreasing input voltage results in an increasing duty cycle at rated load conditions. ZCS is currently possible up to the input voltage value of 3100 V. In the case of input voltages below 3100 V only ZVS could be reached, as shown in Fig. 2.49 (b).



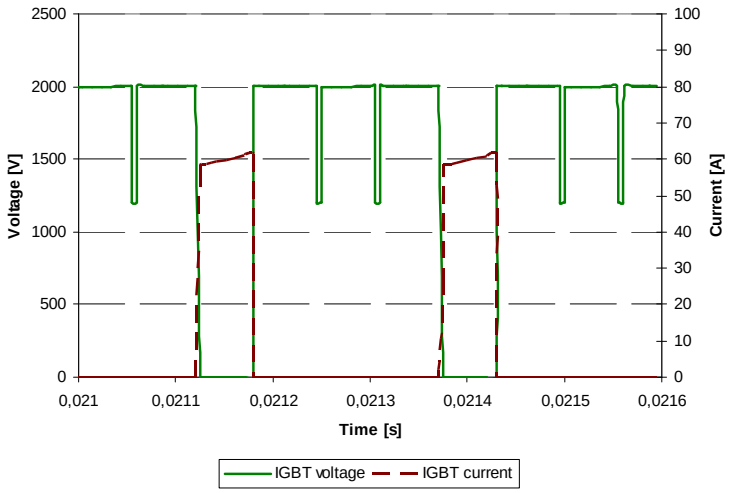
(a)



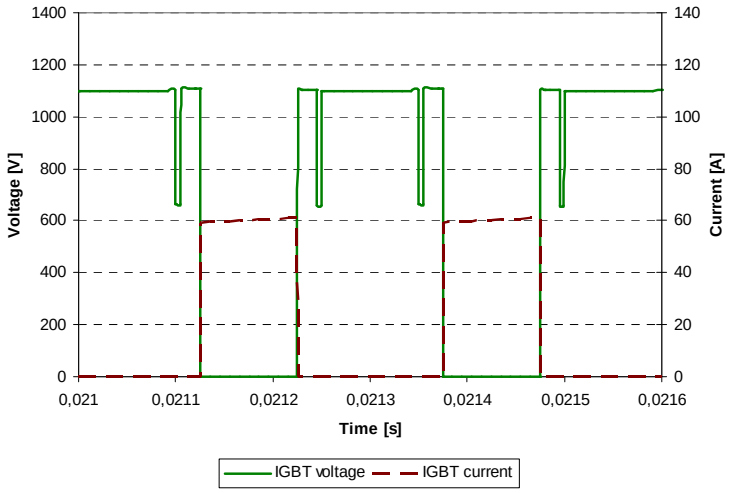
(b)

Fig. 2.49 Soft switching of inner IGBTs: maximal input voltage - ZVS and ZCS (a), minimal input voltage - ZVS (b)

It was noticed that during the whole input voltage range the outer switches T_1 and T_4 were hard switched, as shown in Fig. 2.50. There are several possibilities to increase the input voltage range for ZCS and even achieve ZVS for outer switches as described in [122][123][124]. However, these methods always require some additional components, which is a problematic issue in the case of HP and HV applications.



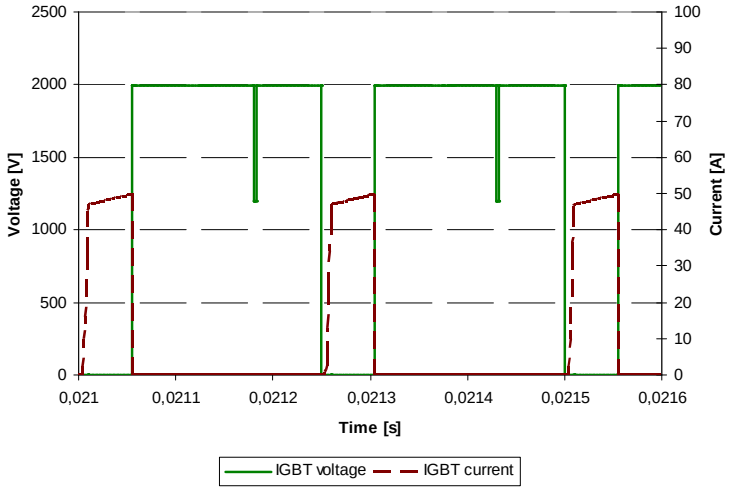
(a)



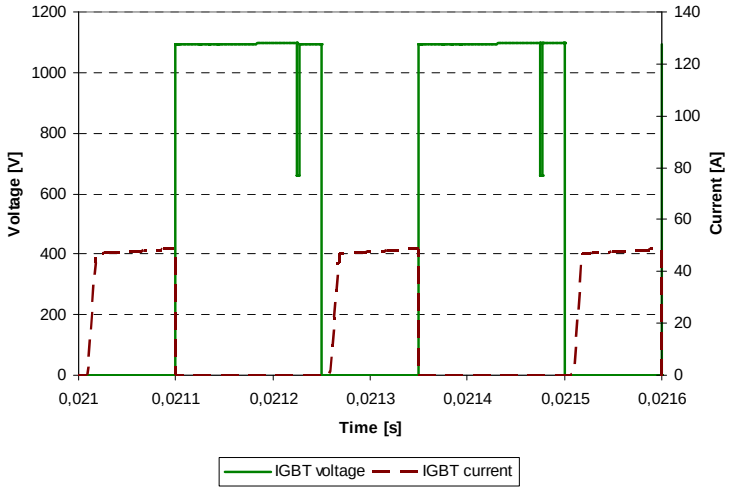
(b)

Fig. 2.50 Hard switching of outer switches: maximal input voltage (a), minimal input voltage (b)

In the case of higher leakage inductance (≥30 μH) of the transformer primary and secondary winding, ZVS for the outer switches over the full regulation range is possible, as shown in Fig. 2.51. The sufficient condition for ZVS is that the dead time should be smaller than the time needed to utilize the leakage energy. It should be noted that the possibility of ZCS for inner switches will be lost. As a result, all switches will work in ZVS operating mode.



(a)



(b)

Fig. 2.51 Soft switching of outer IGBTs: maximal input voltage - ZVS (a), minimal input voltage - ZVS (b)

The benefits of the PWM control scheme are as follows:

- only two PWM channels are required, which unload the control unit;
- ZCS is achievable for inner switches T_2 and T_3;
- ZVS for all switches over the whole regulation range is achievable;
- flying capacitor is not needed, thus space-weight constraints are fulfilled.

Drawbacks are:

- in the case of small leakage inductance no soft switching for outer switches T_1 and T_4 is possible;
- ZCS for inner switches T_2 and T_3 is achievable within the limited regulation range and in the case of small leakage inductance.

PSM method

The computer model of the PSM method is shown in Fig. 2.48. Here it is recommended to use the combination of the diode and flying capacitor clamping method [121]. The flying capacitor provides a mechanism to balance the charge of both input capacitors. However, it does not fully eliminate the volt-second unbalance problem. It merely suppresses the volt-second unbalance effect of the input capacitors, as shown in Fig. 2.52.

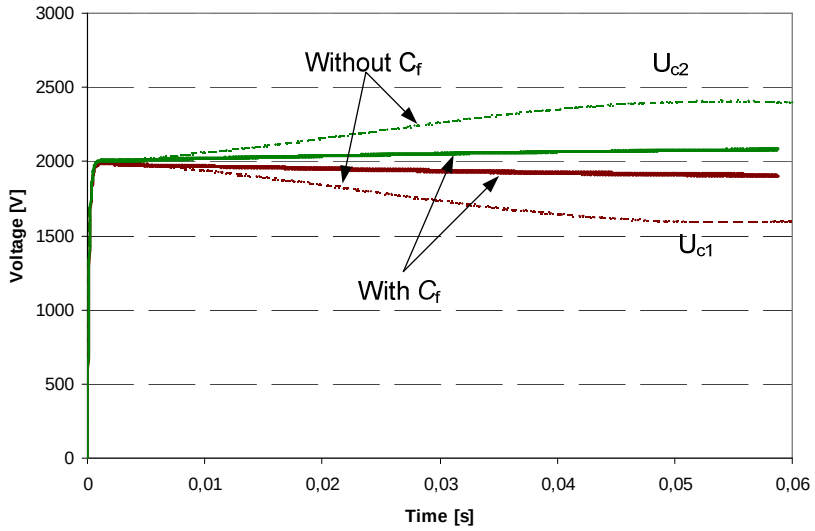
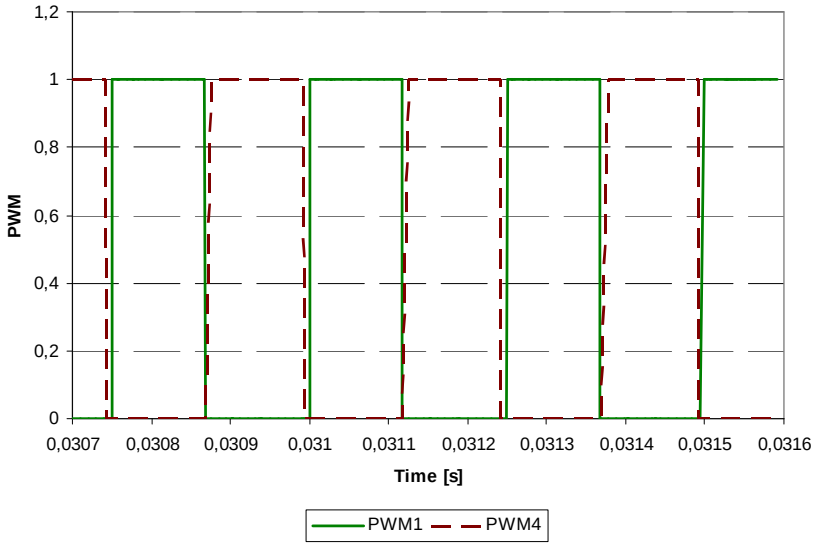


Fig. 2.52 Voltage unbalance of input capacitors with and without flying capacitor C_f

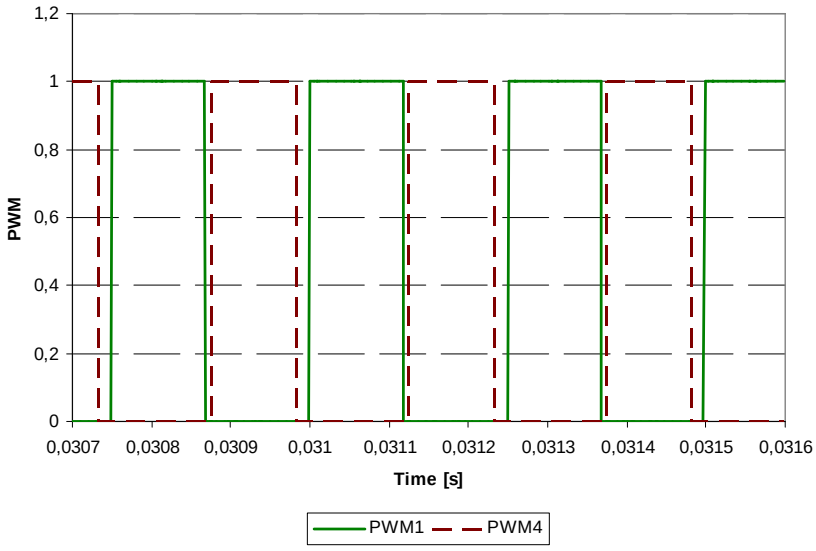
The switches are controlled exactly as if they were used in a phase shifted full-bridge, which gives several advantages of the full-bridge topology [121]. The corresponding timing diagrams are shown in Fig. 2.47. Theoretically two control signals are needed as explained above. However, it is critical to keep according control pulses exactly equal to one another. Any asymmetry in the control pulses will result in an unbalance of the input capacitor voltage, as shown in Fig. 2.53. If ZVS for inner switches is desired, then the dead time must be adjustable. The maximum dead time requirement to achieve ZVS operation can be determined as [54]:

$$t_{\mathrm{d\_max}} = \frac{\pi}{2}\sqrt{L_{\mathrm{lk}}\left(C_{\mathrm{IGBT}} + C_{\mathrm{tr}}\right)}, \tag{28}$$

where L_{lk} is the leakage inductance of the transformer primary, C_{IGBT} is the non-linear parasitic capacitance of the switch and C_{tr} is the transformer winding capacitance.



(a)



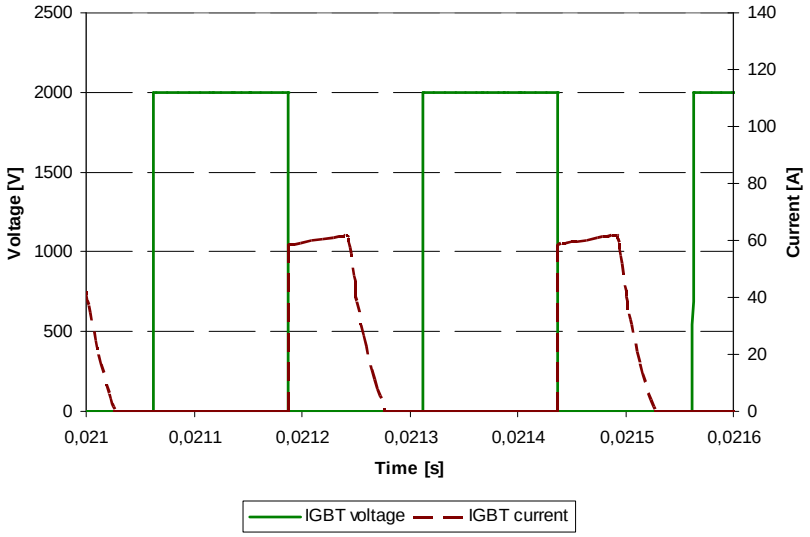
(b)

Fig. 2.53 Control signals of the half-bridge converter: symmetrical duty cycles of T_1 and T_4 (a), 4% difference in the duty cycles T_1>T_4 (b).

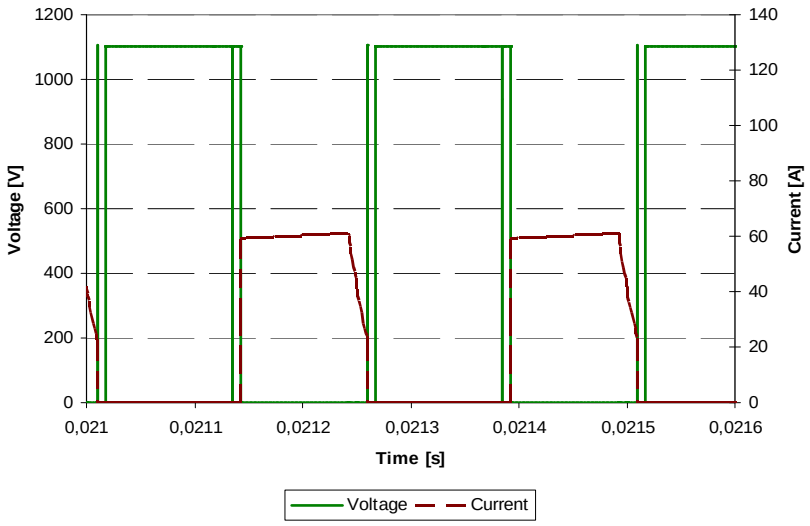
In case if the leakage inductance of the transformer primary and secondary is small (1 μH …2 μH), ZCS can be achieved for T_2 and T_3, as shown in Fig. 2.54 (a). It is achievable only within a small regulation range. Normally the inductance of the transformer primary is higher and ZCS is not possible. An alternative solution is to use the leakage inductance of the transformer primary for ZVS. This method is described in detail in [54]-[56],[125]. In order to achieve ZVS operation, the energy stored in the transformer primary should meet the following condition [54][126]:

$$\frac{1}{2}L_{\mathrm{lk}} \cdot {i_{\mathrm{Tr\text{-}p}}}^2 > \frac{4}{3}C_{\mathrm{IGBT}}\left(\frac{U_{\mathrm{in}}}{2}\right)^2 + \frac{1}{2}C_{\mathrm{tr}}\left(\frac{U_{\mathrm{in}}}{2}\right)^2, \tag{29}$$

where L_{lk} is the leakage inductance, $i_{\mathrm{Tr\text{-}p}}$ is the primary current, U_{in} is the input voltage of the converter.

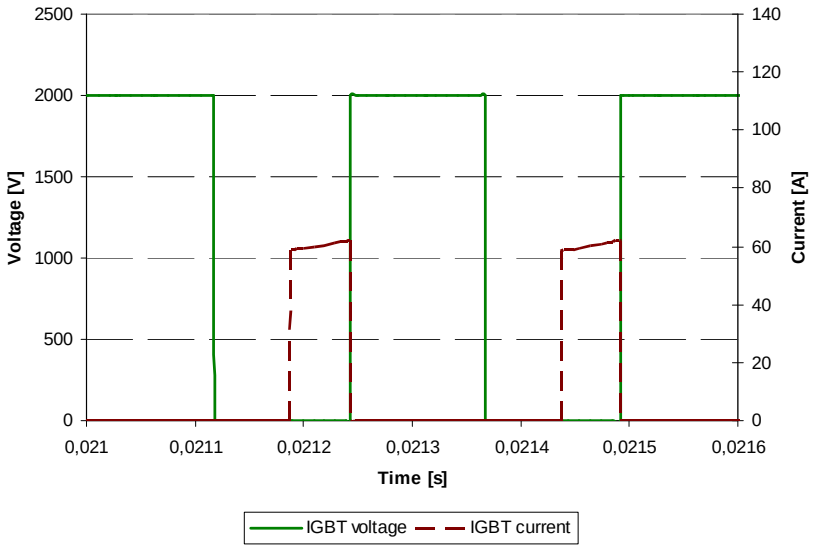


(a)

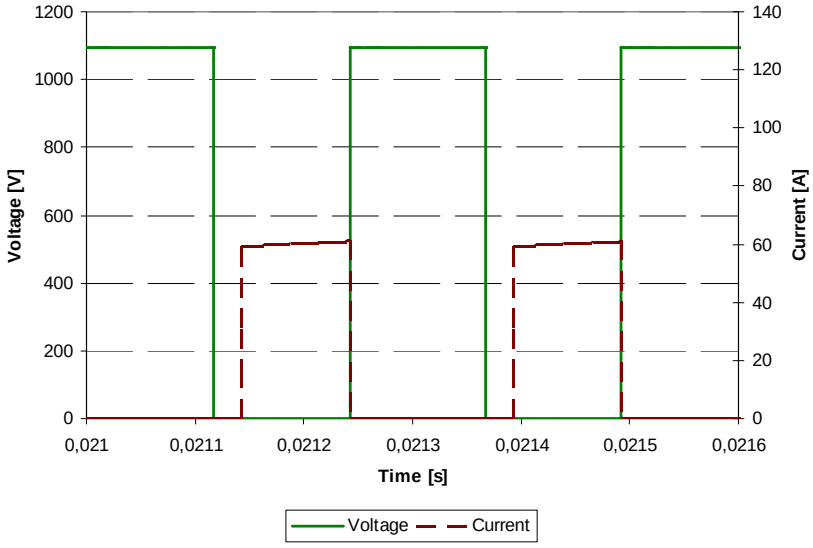


(b)

Fig. 2.54 Switching diagrams of the inner IGBTs at rated load conditions: maximal input voltage and minimum duty cycle ZCS is achievable (a), minimal input voltage and maximum duty cycle (b)



(a)



(b)

Fig. 2.55 Switching diagrams of the outer switches in rated load conditions: full input voltage and minimum duty cycle- ZVS achievable (a), minimum input voltage and maximum duty cycle- ZVS achievable (b)

ZVS over the full regulation range can be achieved for the outer switches without any additional components or efforts, as shown in Fig. 2.55.

Benefits of this control scheme are as follows:

- ZVS over the full regulation range can be achieved for T_1 and T_4;
- by increasing the leakage inductance of the transformer, ZVS over the full regulation range can be achieved for T_2 and T_3;
- in the case of a small leakage inductance ZCS of the inner switches in a limited regulation range can be achieved.

Drawbacks are:

- the leakage inductance of the transformer must be high enough to meet the condition (29);
- flying capacitor is recommended, thus increasing weight and price of the converter;
- ZCS of inner switches is achievable only for limited regulation range.

2.3.2 Analysis and Simulation of Digital Control Algorithms for Three-Level Half-Bridge Converters

The three-level HB is similar to the two-level HB topology. The only difference lies in the inverter where the three-level topology has two additional transistors and some clamping components. Since the input and output filter configurations do not change, also the converter stability criteria and transient response behaviour should not change considerably. The computer model used in the simulations is shown in Fig. 2.56. The conditions for open loop input voltage and load transient response were the same as in the case of two-level HB topology. The results of the open loop transient responses are shown in Fig. 2.57 and Fig. 2.58. As stated before, the three-level system acts similarly to the two-level system. Due to the low pass filter in the output, the open loop system has good input voltage and load damping. In general, the system is stable and with an appropriately designed compensator, good closed loop behaviour could be assumed.

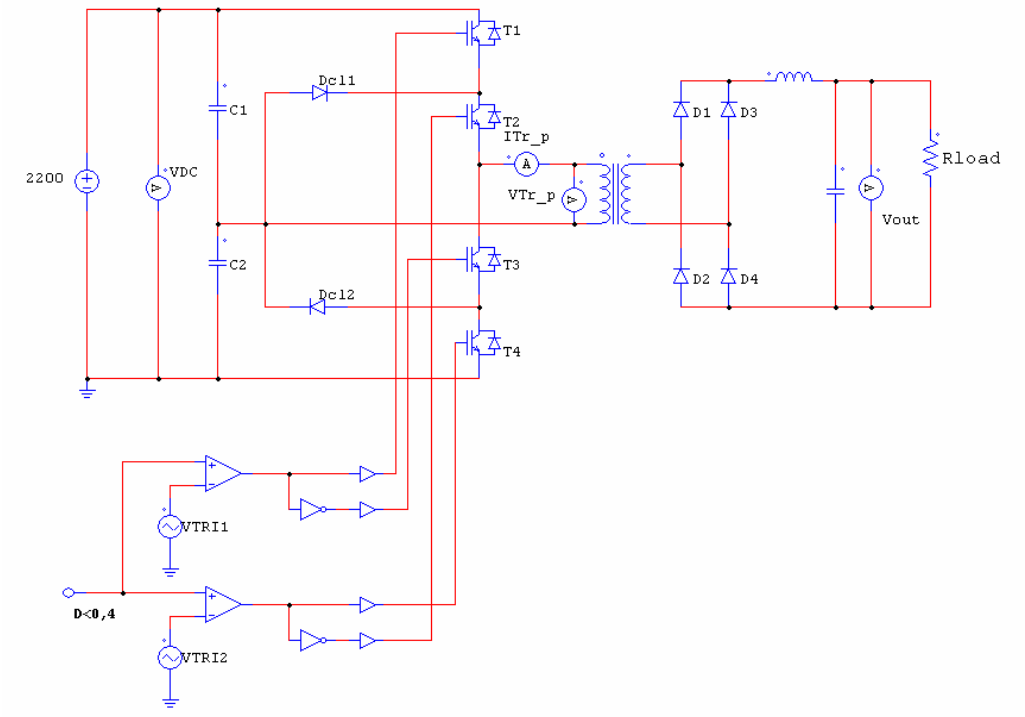


Fig. 2.56 Open loop model of the three-level half-bridge for transient response simulations

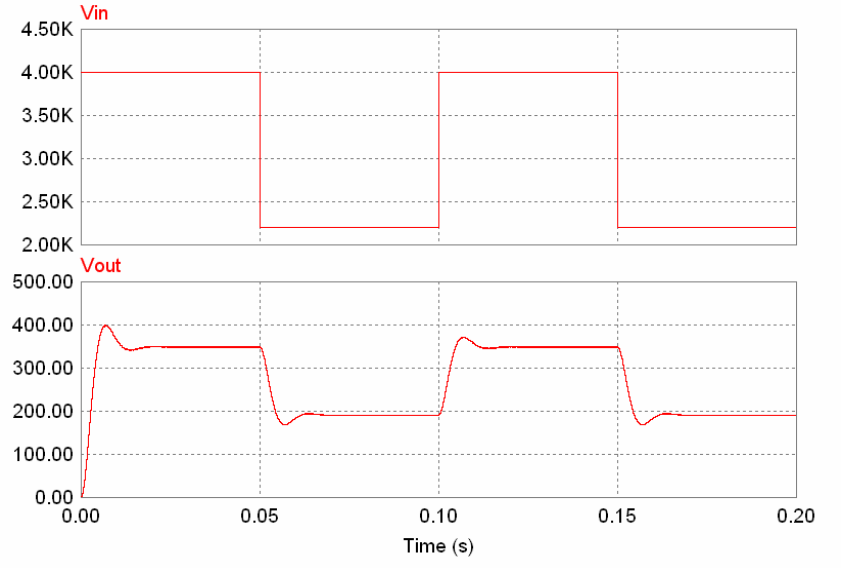


Fig. 2.57 Open loop response to input voltage transients

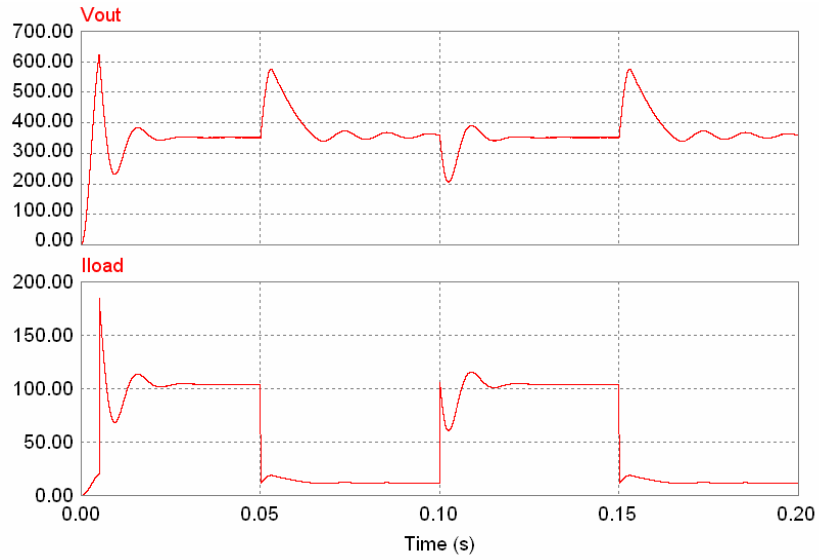


Fig. 2.58 Open loop response to load transients

In the case of PWM, all the algorithms suitable for two-level HB are also applicable for a three-level topology. In the case of PSM only three control algorithms are available (Fig. 1.14): VMC, feed forward VMC, average current mode control. All of these algorithms were analyzed and simulated in the previous chapter. In the same manner they can be applied in a three-level HB converter controlled by PSM. The only difference is that instead of a direct duty cycle control, phase shift between PWM signals is regulated.

Due to the excellent input voltage damping and good line regulation, VMC is quite an attractive control algorithm also for the isolated DC/DC front-end converter based on the three-level topology. In order to increase reliability, reduce weight and costs of the HP and HV isolated DC/DC converter it is recommended to use PWM method, which do not require flying capacitor. In principle ZVS for all switches is achievable, which can further reduce switching losses. The practical results are presented in Chapter 3.3.9.

3. PRACTICAL DESIGN ISSUES AND EXPERIMENTAL RESULTS

Based on the information and knowledge acquired from previous analyses and simulations, a state of the art test prototype of the front-end converter (FEC) for traction applications was built and tested. The first developed prototype is based on the two-level half-bridge topology (Fig. 3.1). In general, the isolated HB topology was implemented because of its simple construction and high overall reliability. The new 6.5 kV FZ200R65KF1 IGBT modules have made it possible for the first time to implement HB topology in such a high power (P>20 kW) and high voltage (U>2 kV) application as the FEC. Logical enhancement of the two-level topology would be the three-level HB topology (Fig. 3.2). Three-level topology does not differ much from the classical HB. Instead of two switches, the three-level HB uses four, which lowers the voltage stress of a switch and IGBTs with two times lower blocking voltage capability (3.3 kV IGBT modules) could be implemented. In addition, the switching frequency can be increased at least two times or even more when the soft switching effect (without additional components) is utilized. Also, the control system of the three-level HB does not differ much from the control system of the two-level converter. Due to the similarities between the two converter topologies the three-level HB isolated DC/DC converter could also be built and tested. The differences are presented in the practical part of the doctoral work.

A generalized scheme of the front-end converter for traction applications based on the two-level HB isolated DC/DC converter is shown in Fig. 3.1. It can be divided into four stages: power electronics stage, power interface stage, signal transmission stage, control and communication stage. The power electronics stage includes the main hardware of the front-end converter and does not concern the control system. The current doctoral work analyzes only the control system design that includes the following: power interface stage, signal transmission stage, and control and communication stage.

The control and communication stage receives feedback signals from ten sensors. The input current sensor is needed only for diagnostics. The output current is used to identify overload conditions. In order to detect volt-second unbalance of the transformer primary the capacitor voltage U_{C2} is measured. The input voltage U_{in} is sensed to detect over- and undervoltage situations. The output voltage is controlled with the classical voltage mode control algorithm. Thus, the output voltage is measured for the control loop feedback. In addition, transistor, transformer and output inductor temperatures are measured. This information is used by the protection and diagnostic system. Plug&play drivers were chosen for the control of the IGBTs. All sensor and driver signals are galvanically isolated from the power electronics stage. The converter is controlled by the control and communication stage, which includes a powerful DSC. The main functions of the DSC are output voltage stabilization, protection

against erroneous and faulty operation and communication with external devices.

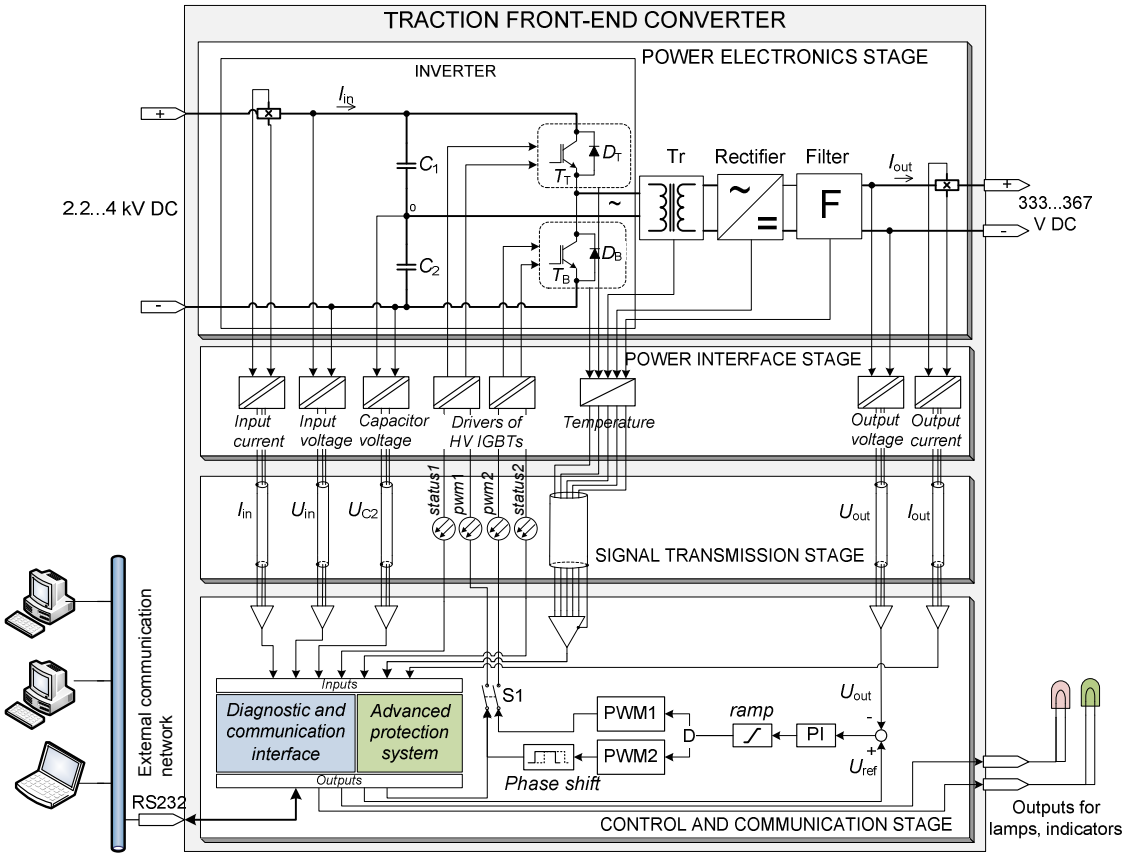


Fig. 3.1 A generalized block diagram of the front-end converter for traction applications based on the two-level HB isolated DC/DC converter

A generalized scheme of the FEC topology based on the three-level HB isolated DC/DC converter is shown in Fig. 3.2. The three-level topology has two additional transistors. Other components of the control system (the number and type of sensors, relay outputs for lamps or indicators, protection and communication functions) remain unchanged. The changes are shown in the simplified block diagram in Fig. 3.2. Redrawn were only the blocks that had changed.

Two additional transistors require two more control channels. This would normally complicate the control program and also increase the load of the microcontroller but in this doctoral project an innovative solution to the problem was introduced. A method was developed that derives additional channels within the hardware without any software interaction (Fig. 3.17). The controller can save its resources for other tasks. In general, assuming that voltage mode control and the PWM method is used, the control program also remains unchanged. As a result, the flexibility of the developed control system for the front-end converter increases, allowing its use for both two-level and three-level half-bridge converters without any changes.

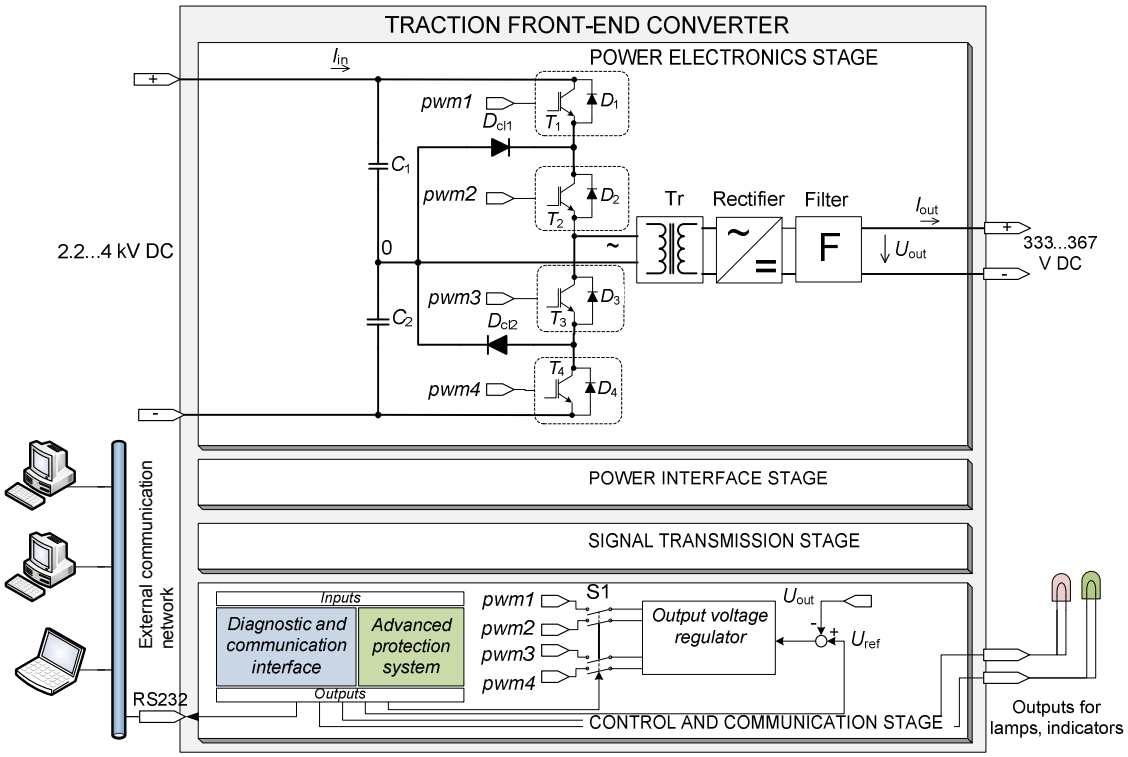
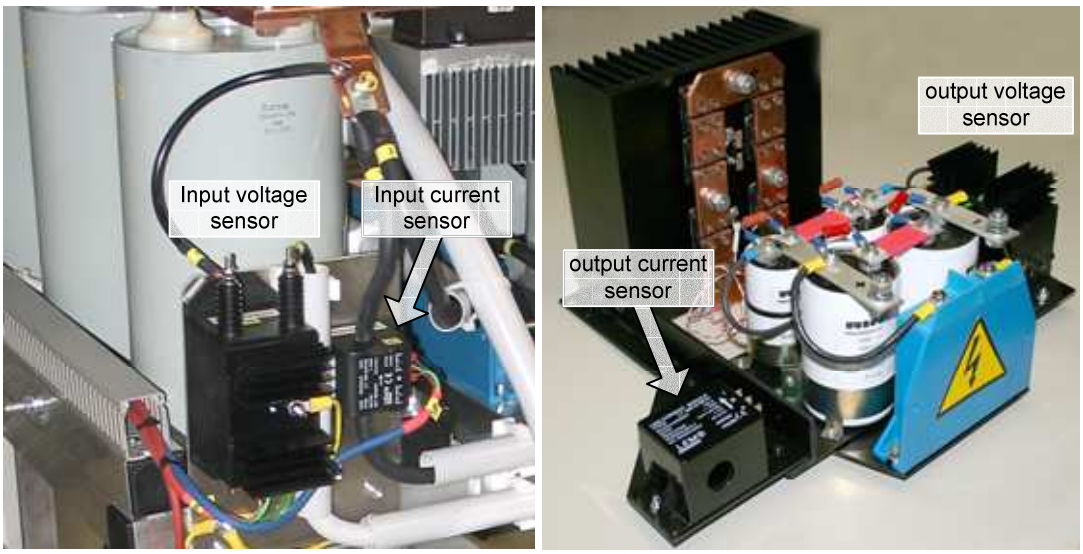


Fig. 3.2 A generalized block diagram of the front-end converter for traction applications based on the three-level HB isolated DC/DC converter

3.1 Power Interface Stage

This section mainly concentrates on IGBT drivers and different types of sensors. Important issues are isolation classes and suitability for HV applications. The FEC for traction applications consists of ten sensors (Fig. 3.1): two current (I_{in}, I_{out}), three voltage transducers (U_{in}, U_{C2}, U_{out}) and five temperature sensors. In general, closed loop Hall effect transducers were used for current and voltage measurement. The transducers were placed such that the length of power cables could be minimized. The input voltage and current transducers are placed close to the input capacitors and input terminals of the FEC, as indicated in Fig. 3.3 (a). The output voltage and current transducers are placed next to the output capacitors, as shown in Fig. 3.3 (b). The FEC is equipped with advanced protection and diagnostic functions. In addition, to the currents and voltages, the temperatures of the IGBTs, transformer and output inductor are measured. The temperature was measured with platinum (PT-100) resistance thermo sensors that offer excellent accuracy over a wide temperature range. The two IGBT temperature sensors are screwed on the inverter heat sink alongside each IGBT, as shown in Fig. 3.4. In order to measure transformer and output inductor temperature, two sensors were integrated into the windings.



(a) *(b)*

Fig. 3.3 Input voltage and current sensors (a), output rectifier-filter module with output current and voltage sensors (b)

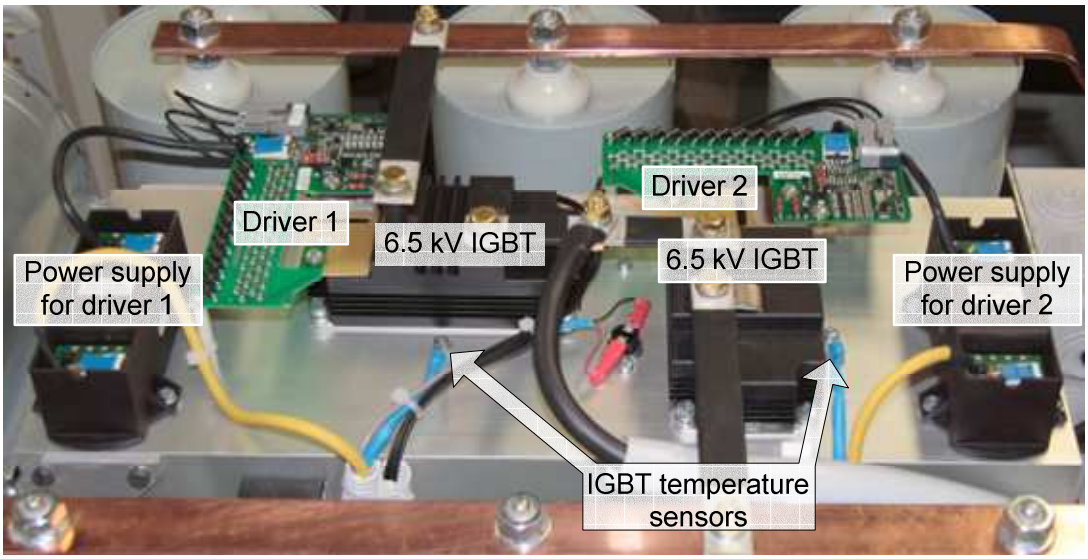


Fig. 3.4 Two-level half-bridge inverter of the FEC for traction applications

3.1.1 Current Measurement

In the current application, DC current needs to be measured. According to the performance requirements, all components in the HV input side of the FEC should have rated insulation of at least 15 kV. Since the current is only measured for diagnostics and converter protection, high accuracy current sensors are not obligatory. The input current was measured with a closed loop current transducer LEM LT 100-S/SP30 (Fig. 3.3 (a)) specially designed for traction applications. The main parameters are summarized in Table 9. The output current was measured with closed loop current transducer LEM LT 200-S/SP44 (Fig. 3.3 (b)) designed for industrial applications. The main parameters

are summarized in Table 9. Both transducers can be characterized by galvanic isolation between high power and electronic part, high accuracy, very good linearity, low temperature drift, high immunity to EMI, and current overload capability.

Table 9 Technical data of the input and output current transducers

Type	**LT 100-S/SP30**	**LT 200-S/SP44**
Current measuring range	-200…+200 A	-300…+300 A
Accuracy	±0.5 %	±0.5 %
Response time	< 1 μs	< 1 μs
Ambient operating temperature	-40…+70 ºC	-40…+85 ºC
Weight	184 g	230 g

3.1.2 Voltage Measurement

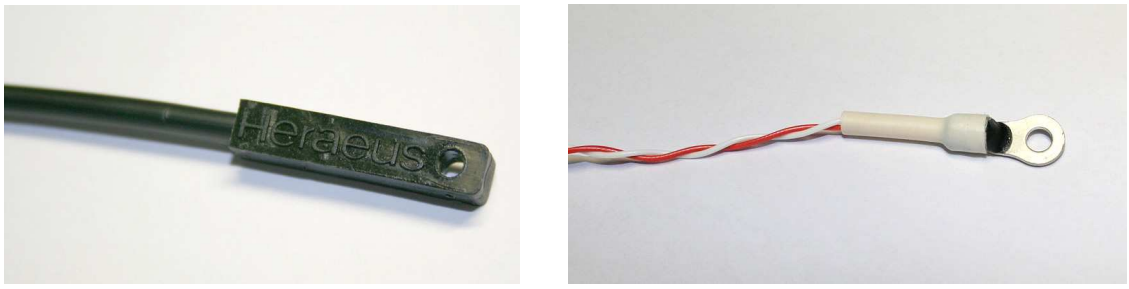
In the current application, DC and pulsed voltage needs to be measured. According to the performance requirements, all components in the HV input side of the FEC should have rated insulation of at least 15 kV. The most critical point is the output voltage where high measurement accuracy is needed (below one percent). The output voltage feedback is used by the regulator to compensate the load changes in the output. The input voltage was measured with a closed loop voltage transducer LEM LV 100-4000/SP6 (Fig. 3.3 (a)) specially designed for HV traction applications. The main parameters are summarized in Table 10. The capacitor voltage was measured with a closed loop voltage transducer LEM LV 100-2000/SP18 specially designed for HV traction applications. The main parameters are summarized in Table 10. The accuracy is from moderate to high. For output voltage measurement a LEM LV 100-300 closed loop voltage transducer (Fig. 3.3 (b)) designed for industrial applications was chosen. The main parameters are summarized in Table 10. As can be seen, the output voltage transducer exhibits the needed accuracy class. In addition, it has very good response time compared to the input or capacitor voltage transducers. In general, all voltage transducers are characterized by medium accuracy, very good linearity, low temperature drift, and high immunity to EMI.

Table 10 Technical data of the voltage transducers

Type	**LV 100-4000**	**LV 100-2000**	**LV 100-300**
Purpose	input voltage	capacitor voltage	output voltage
Measuring range	-6 kV…+6 kV	-3 kV…+3 kV	-450 V…+450 V
Accuracy	±0.7 %	± 1.2 %	± 0.7 %
Response time	200 μs	150 μs	80 μs
Ambient operating temperature	-25…+70 ºC	-40…+70 ºC	0…+70 ºC
Weight	850 g	850 g	850 g

3.1.3 Temperature Measurement

In general, five PT-100 temperature sensors are used. For transformer and output inductor special temperature sensor Heraeus SZK(0) was used, as shown in Fig. 3.5 (a). The technical specification is presented in Table 11. The temperature of IGBTs and the output rectifier is measured with Heraeus FK 422 (Fig. 3.5 (b) and Fig. 3.4) which are specially designed for surface montage. The technical specification is presented in Table 11. In order to convert nonlinear output of the sensors into a linear current signal the special signal converter SEM203P (Status Instruments) was used.



(a) *(b)*

Fig. 3.5 Temperature sensors PT-100 Heraeus: SZK(0) (a), FK 422 (b)

Table 11 Technical data of the temperature sensor PT-100 Heraeus SZK(0)

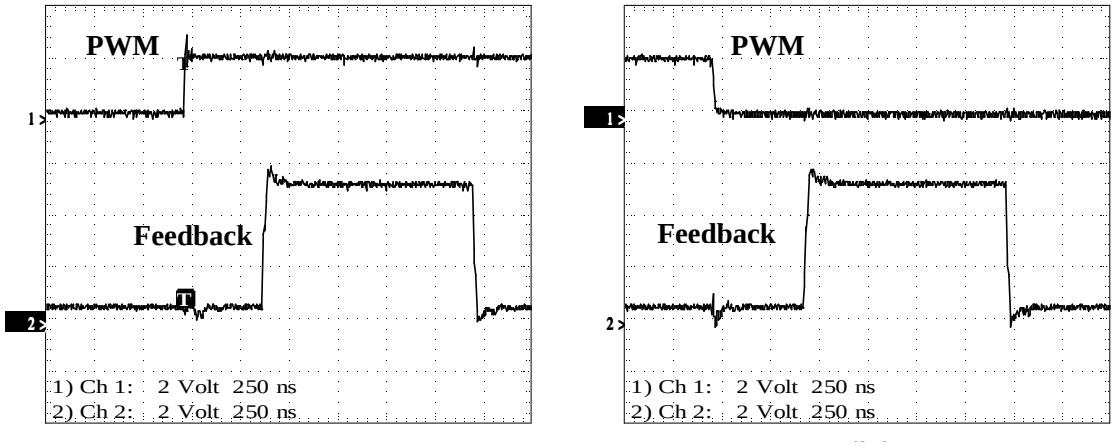
Type	**PT-100 SZK(0)**	**PT-100 FK 422**
Purpose	Transformer, inductor	IGBTs, rectifier
Measuring range:	−20 … +110 °C	0 … 250 °C
Accuracy	± 0.3 ºC at 0 ºC (class B)	± 0.3 ºC at 0 ºC

3.1.4 High Voltage IGBT Drivers

Two types of drivers are available for modern HV IGBTs: driver cores and plug&play drivers. In order to achieve the highest possible reliability with the shortest development time plug&play drivers were chosen. The Concept driver 1SD210F2 (Fig. 3.4) is compact, intelligent, high performance, single-channel plug&play driver for 6.5 kV IGBTs. It is equipped with several protection and diagnostics functions, e.g. collector-emitter voltage monitoring for the short-circuit detection, supply-undervoltage shut down and the status feedback. The driver must be electrically isolated from the control system. Each plug&play driver has a build-in optical interface with two channels: for IGBT control signal and for driver status feedback signal. Driver status feedback signals enable the main controller to monitor both the driver and the IGBT [127]. The errors that can be identified using driver status feedback signals are shown in Table 13

During normal operation (i.e., no fault) the driver status feedback is “light on” at the optical link. A malfunction is signalled by “light off”. Each edge of the

control signal is acknowledged by the driver via a short pulse (900 ns), as indicated in Fig. 3.6 [127].



(a) *(b)*

Fig. 3.6 Driver status feedback signals on the rising edge of the control signal (a), on the falling edge of the control signal (b)

3.2 Signal Transmission Stage

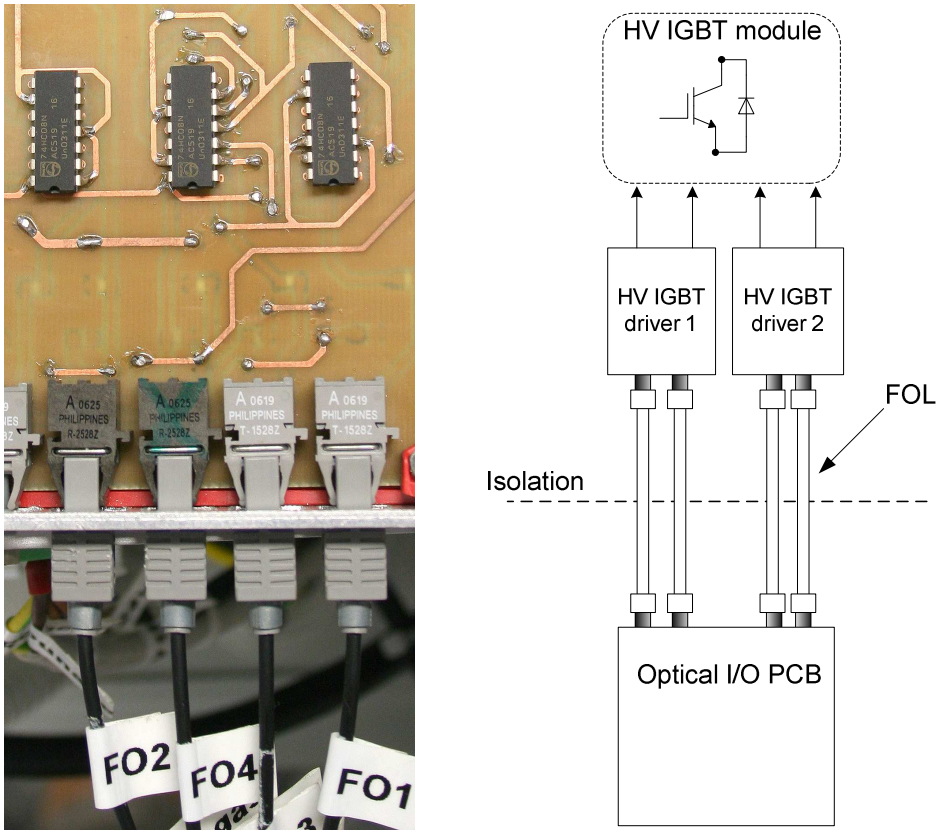
The signal transmission stage is a link between control and communication stage and power interface stage, as shown in Fig. 3.1. The main topics to be discussed here are EMC problems of the signals and isolation between HP and HV power electronics stage and the low voltage control and communication stage.

3.2.1 Sensor Signals

According to the performance requirements, the power electronics stage must be isolated from the control and communication stage. Closed loop voltage and current transducers used for measurements provide galvanic isolation between the high power and low power side. The temperature sensors are connected with the isolated parts of the converter. In addition, all current, voltage and temperature signal cables are shielded to decrease EMI impact.

3.2.2 Driver Signals

In order to provide sufficient isolation and protection against EMI digital signals like driver status feedback, control signals were transferred over a fiber optic link (FOL). The practical realization of FOL and the corresponding output logic in the optical I/O PCB are shown in Fig. 3.7. Four signals (pwm1, pwm2, status1, status2) are needed in the FEC based on the two-level HB topology. In the case of three-level topology, the number increases to six, i.e. four control signals for the IGBTs and two status feedback signals corresponding to the IGBT pairs.



(a) *(b)*

Fig. 3.7 Output logics and FOL in the developed optical I/O PCB (a), the FOL implementation principle in the FEC (b)

3.3 Control and Communication Stage

Control and communication stage (Fig. 3.1) is the control and processing centre of the FEC. The main topics discussed here are: components, their design and the general structure of the control and communication stage, practical realization of the advanced control and protection system and real life behaviour of the designed converter. As stated above, in general two-level and three-level HB topologies are quite similar to each other and most of the time they can be discussed jointly. Only in a few cases where there are essential differences in the three-level topology, it will be discussed separately.

3.3.1 Assembly and Components of the Control System

One goal of this doctoral project was to build a test prototype of the control system for FEC. In order to achieve flexibility the control system was assembled in a 19-inch rack module (Fig. 3.8) was used. The whole system consists of 7 printed circuit boards (PCB)(each 100x160 mm) developed during the project:

- Auxiliary power supply PCB– step down DC/DC voltage converter for driver power supply;

- relay PCB – solid-state relays outputs for external indicators or lamps;
- optical input and output (I/O) PCB:
    a. two inputs and two outputs for driver signals in the case of two-level HB topology;
    b. two inputs and four outputs for driver signals in the case of three-level HB topology;
- control unit PCB;
- current measurement PCB – transforms sensor signals into a suitable form for the A/D conversion;
- voltage measurement PCB – transforms sensor signals into a suitable form for the A/D conversion;
- temperature measurement PCB – transforms sensor signals into a suitable form for the A/D conversion.

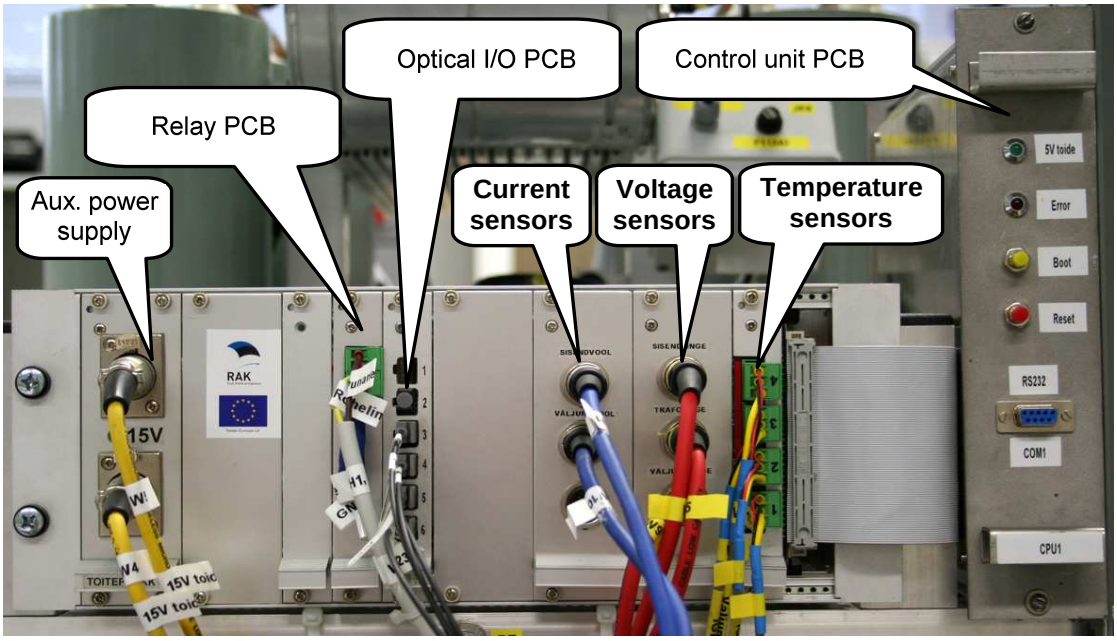


Fig. 3.8 The control system is built into a 19-inch rack module

The backplane of the rack module is a special bus system which provides power to the PCBs and interconnects all the boards with the control unit board. In general, an advantage of the rack module is its flexibility and adaptability, which makes it especially suitable for development. However, due to the high price it is not very practical for an end product.

Auxiliary power supply PCB

The HV IGBT drivers require a reliable and isolated supply voltage (±15 V), which is generated by the power supply CT-CONCEPT ISO3116I (Fig. 3.4). The auxiliary power supply PCB (Fig. 3.9) is used to generate stabilized supply voltage (+ 15 V) for CT-CONCEPT ISO3116I.

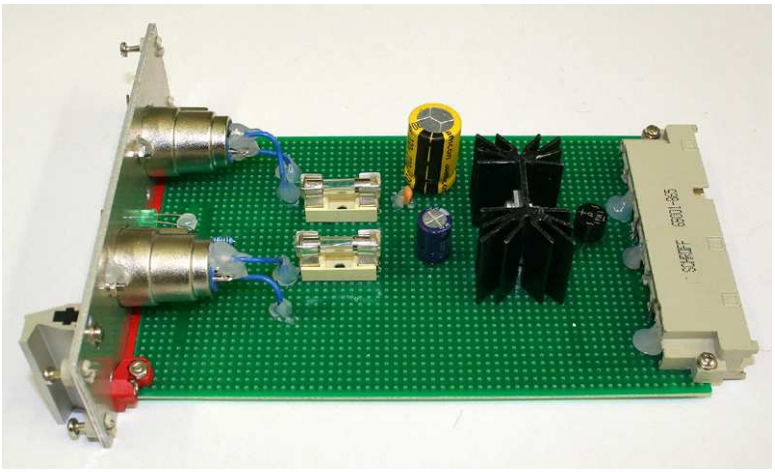


Fig. 3.9 Power supply PCB of IGBT drivers

Relay PCB

All converters for traction applications should have an acknowledgement or indication function (EN50155 requirement). The relay PCB (Fig. 3.10) includes two semiconductor relays to switch external lamps or indicators. In general, the PCB is designed for eight relays, thus the number of channels can be extended if necessary. In order to further increase the flexibility of the system the function of each relay output has been made programmable over the diagnostic and communication interface. So the user can freely choose events to be indicated.

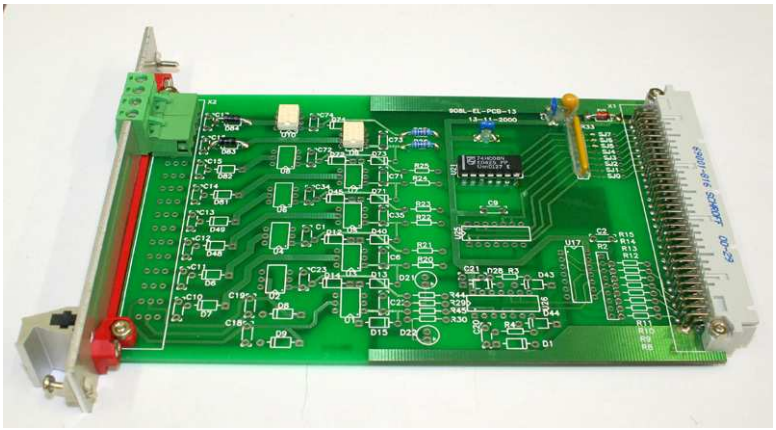


Fig. 3.10 Relay PCB with two outputs, extendable up to eight outputs

Optical input and output PCB

Optical I/O PCB (Fig. 3.11) for two-level HB topology includes two control outputs and two status feedback signal inputs. In addition, some hardware protection circuits are placed on this PCB, e.g. dead time circuit, common signal blocking circuit. The dead time is added at the beginning of each control signal. Thus, the dead time generation circuit has a direct impact on control signal shape and if designed incorrectly can have catastrophic results.

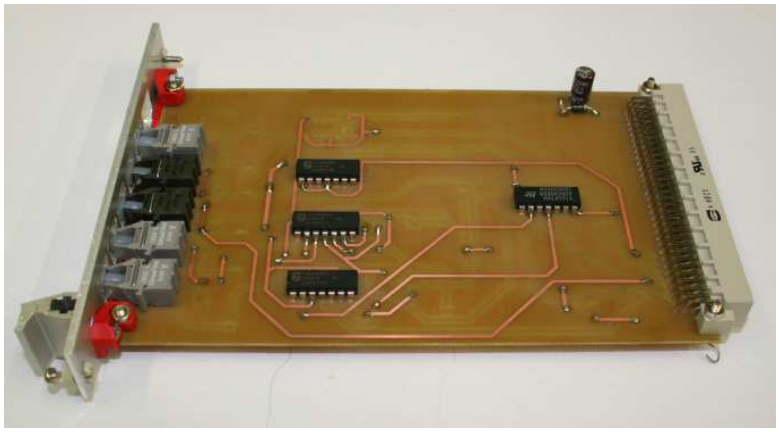
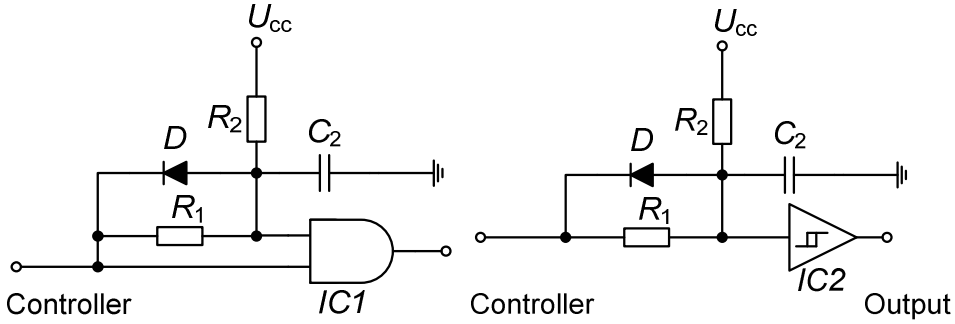


Fig. 3.11 Optical input and output PCB

Two circuit topologies were considered for dead time generation, as shown in Fig. 3.12. The first scheme consists of a simple RC circuit followed by a digital integrated circuit (IC). The RC circuit is responsible for the delay while the IC is used for the signal amplification and commutation. The dead time equals approximately to the time constant, which may be determined as:

$$\tau = \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C \text{ ,} \tag{30}$$

where τ is the time constant, R_1 and R_2 are the resistances of according resistors, C is the capacitance of the capacitor C_2.



(a) *(b)*

Fig. 3.12 Schematic of dead time circuit with the logic AND gate (a) and with Schmidt trigger (b)

In the first case, a logic AND gate (IC_1) is implemented as a commutating component. The circuit is simple and with low realization cost. However, all logic gates have two predefined voltage ranges, which correspond to logical one or zero. The area between those predefined voltage values is undefined as well as the gate output. Thus, the operations within that zone should be avoided. Due to the RC delay circuit, the input voltage of the gate crosses the undefined area relatively slowly (Fig. 3.13), which can lead to the output instabilities. Clearly the larger the time constant, the stronger the distortion will be [128].

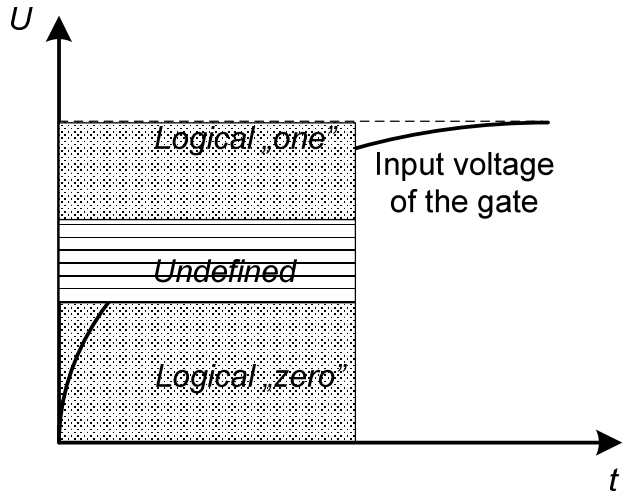
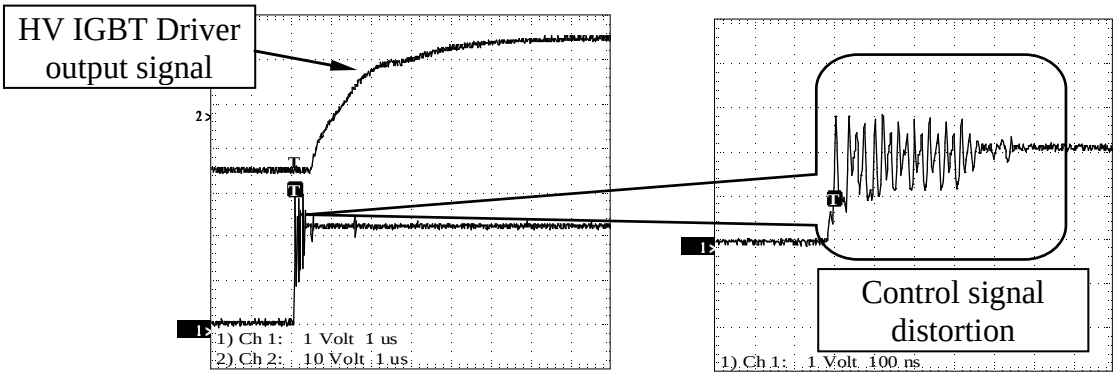
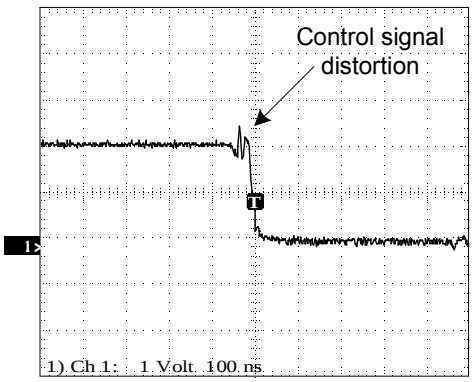


Fig. 3.13 Input voltage of the logic gate IC1

The impulse distortion on the rising front of the PWM signal can be seen in Fig. 3.14. It also occurs on the falling front. However, the distortion on the falling front can be somewhat reduced (Fig. 3.14 (b)) by reducing the capacitance *C* and choosing a fast acting discharge diode *D*. As result the discharge process of the capacitor speeds up and reduces the time spent in the undefined are of the logic component thus, less impulse distortion on the PWM falling front.



(a)



(b)

Fig. 3.14 Distortion of the PWM signal due to the dead time circuit: on the rising front (a), on the falling front (b)

Most of the modern IGBT drivers are capable of filtering out those distortions, as can be seen in Fig. 3.14. Nevertheless the distortion should be avoided. In the current thesis the problem could be solved by replacing AND gate with the Schmidt trigger (*IC2*), as shown in Fig. 3.12 (b). The Schmidt trigger has an input with hysteresis, which means that the turn on and off instants occur at different voltage levels. No undefined area exists and the signal distortion can be prevented, as indicated in Fig. 3.15. The delayed control signal shows distortion neither in the rising nor in the falling front. It should also be noted that the dead time is only added at the beginning of each control signal. The falling front of the control signal has no delay, as shown in Fig. 3.15.

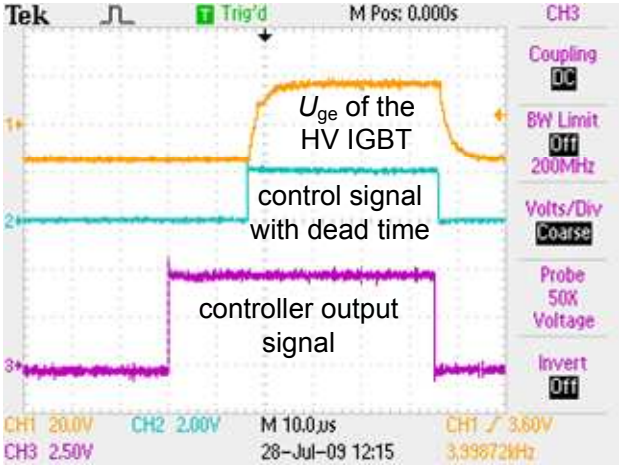


Fig. 3.15 Control signal delay created with Schmidt trigger

The dead time circuit provides no protection against common signals, which can be caused by some software error. An additional logic circuit is needed. The common signal blocking circuit is shown in Fig. 3.16. The negation gates (*Neg1*, *Neg2*) block the common signal while the "pull down" resistors (R_1, R_2) force the PWM outputs to zero during microcontroller reset or a failure situation.

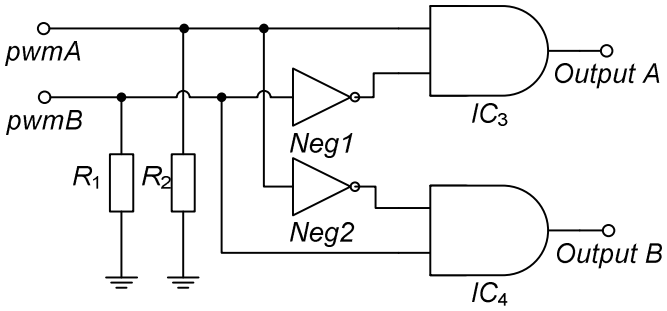


Fig. 3.16 Common signal blocking circuit

For the FEC based on the three-level HB a new optical I/O PCB with four control outputs and two status feedback signal inputs had to be designed. It results logically that four independent PWM channels are also required, which

increase the complexity of the control program and load the controller. A new concept that uses hardware based signal multiplication circuit is proposed in the current doctoral project. By use of this method, only two independent PWM channels (pwmA and pwmB) are needed. The missing channels can be derived by inverting those two PWM signals, as shown in Fig. 3.17. The detailed description in each case was given in the analytical chapter 2.3.1 on page 82. The resulting four control signals (ctr1, ctr2, ctr3, ctr4) are provided with a dead time that is generated by the RC delay circuit (Fig. 3.12 (b)) and transmitted via FOL to the HV IGBT drivers, as shown in Fig. 3.17. The resulting gate-emitter voltages of the IGBTS are indicated in Fig. 3.18. Although this optical I/O PCB was originally designed for three-level HB topology, it can be used also for two-level HB topology. In that case only two control signals (ctr2 and ctr4) are needed.

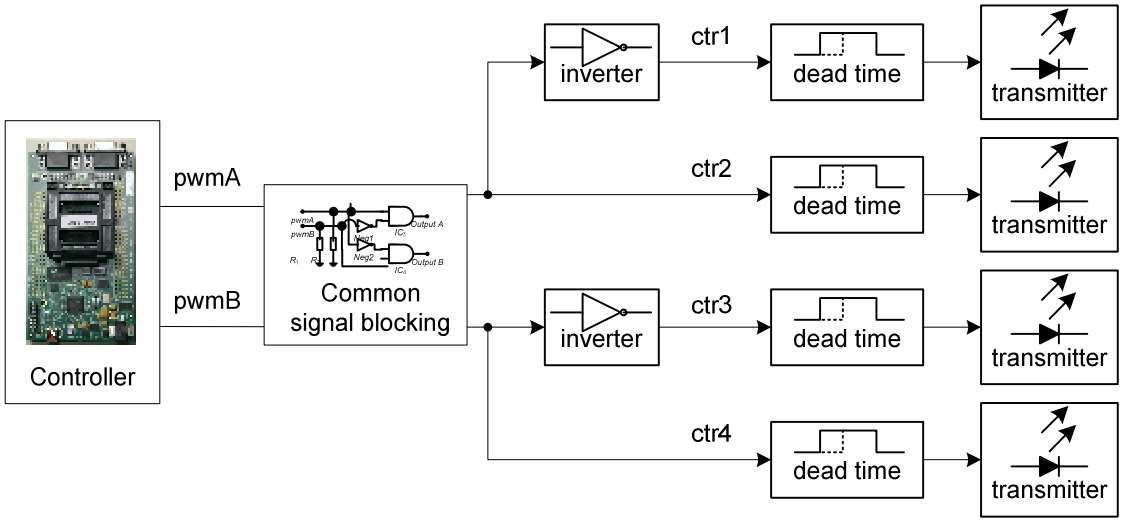
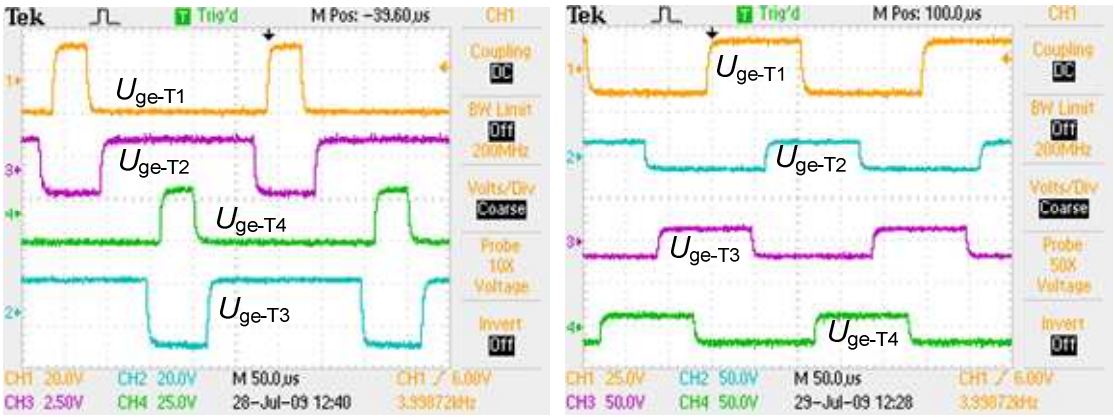


Fig. 3.17 Block diagram of control signal multiplication concept



(a) *(b)*

Fig. 3.18 Gate-emitter voltages of a three-level half-bridge controlled with PWM (a) and PSM (b)

Control unit PCB

Control unit PCB (Fig. 3.19) is the heart of the whole converter. This PCB connects the control unit to all peripherals and sensors. In addition to digital and analogue I/Os, it also has communication interface to communicate with external devices. Control unit PCB includes a precision voltage regulator to generate stable reference voltage for the ADC. The control unit is equipped with a real time clock module and a lithium battery that serves as a reserve power source for the real time clock module.

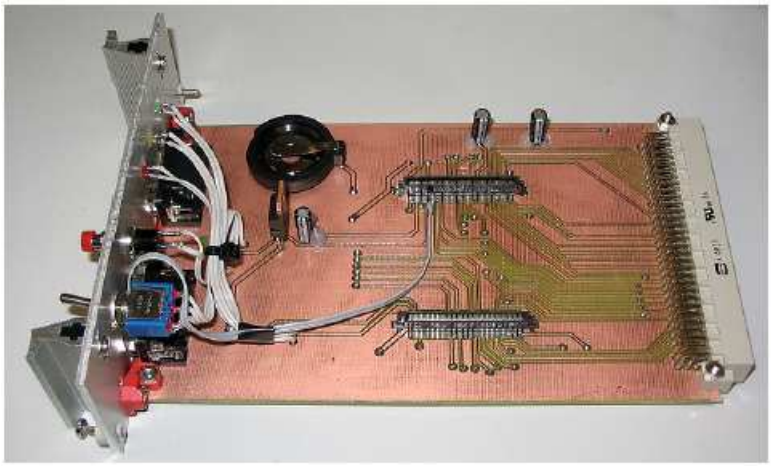


Fig. 3.19 Control unit PCB

Current measurement PCB

Current measurement PCB (Fig. 3.20) includes two analogue channels for input and load current measurement. The current transducers need stabilized bipolar supply voltage (± 15 V), which is generated on the current measurement PCB.

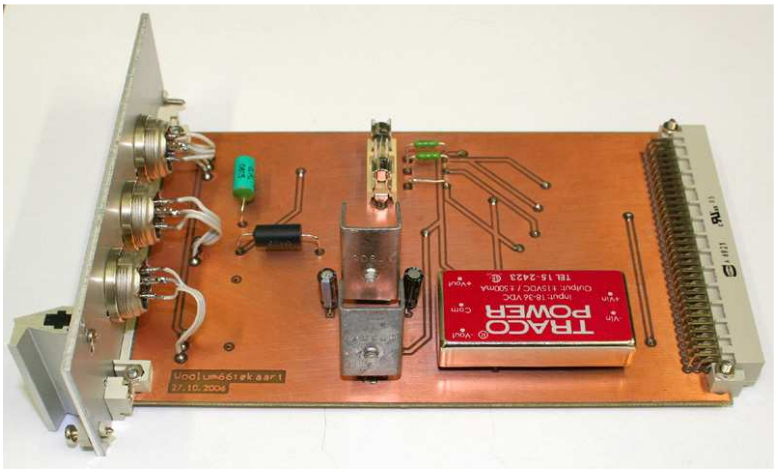


Fig. 3.20 Current measurement PCB

In general, transducers have current output. A wire wound precision measurement resistor (R_m) is used to convert the current signal of the transducer into a voltage signal, as shown in Fig. 3.21. The resistor R_m must be chosen so that no dangerous voltages can occur in the controller analogue input ANx. Analogue inputs of microcontrollers are especially sensitive against overvoltages. To provide sufficient protection usually a zener diode (D_z) and a current limiting resistor R_x are placed in the analogue input of the controller, as shown in Fig. 3.21.

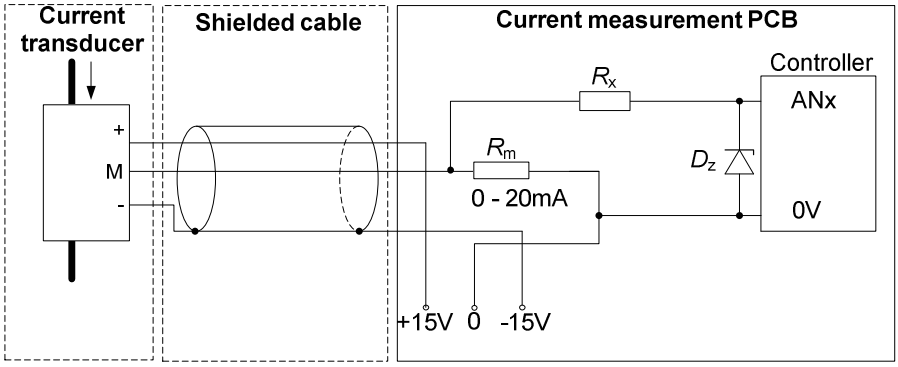


Fig. 3.21 Electrical connection diagram of the current transducers

Voltage measurement PCB

Voltage measurement PCB (Fig. 3.22) includes three analogue channels for input, output and capacitor voltage measurement. The general, implementation here is similar to the current transducers. The voltage measurement PCB includes a bipolar power supply, precision measurement resistors for transducer signal conversion and protection circuit against overvoltages, as shown in Fig. 3.23. The transducer output signal is converted to a voltage signal and measured by the controller.

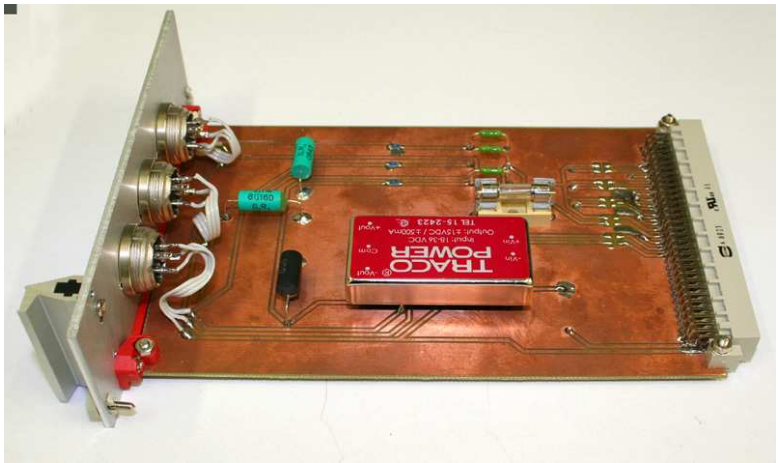


Fig. 3.22 Voltage measurement PCB

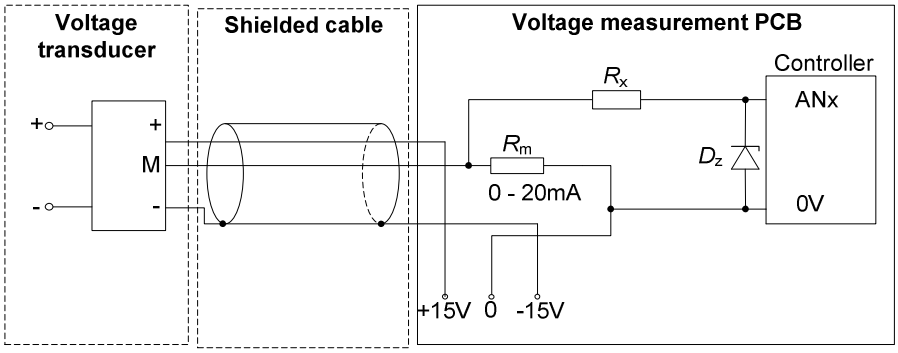


Fig. 3.23 Electrical connection diagram of the voltage transducers

Temperature measurement PCB

The temperature measurement PCB (Fig. 3.24) includes voltage dividers to convert sensor signals into suitable voltage signals that could be measured by the controller.

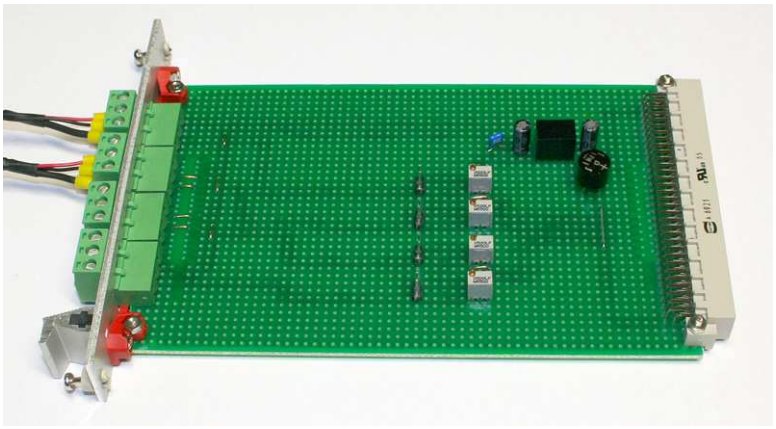


Fig. 3.24 Temperature measurement PCB

3.3.2 EMC Considerations in PCB Design

Electromagnetic compatibility (EMC) is a subject that most designers did not have to worry about ten years ago. Today's situation is different. Our surroundings are crowded with different kinds of electromagnetic devices. EMC and electromagnetic interference (EMI) are important issues in new electric device design. There are mainly two reasons for that, the electromagnetic environment is getting tougher and the devices are very complicated and sensitive to the interferences. In 1995 the EMC directive was introduced in Europe. The directive regulates both electromagnetic radiation and the immunity to the environmental interferences. Therefore, the designer must make sure that the new device will not affect others and can also resist the influences from outside.

The switching frequency of the current converter is relative low but due to the HP and HV signals the electromagnetic environment is still rugged. The most sensitive part of the converter to the EMI is the control system. The most

sensitive PCBs of the whole system are: control unit PCB, voltage and current measurement PCB). Hence, special attention to those three PCBs was paid.

In the development process, modern PCB design software was used. The whole process can be divided into two parts: schematic and layout design. First, the schematic was created. The circuit schematic serves as a basis for the layout design. It insures that the layout and design are consistent. Today's powerful tool of the PCB design software is an autorouter. It means that the software can route the whole PCB automatically, following the routing rules specified by the user. Autorouting has many advantages, e.g. it is much faster than manual routing, it takes EMC rules into account, autorouter always optimizes track lengths and avoids sharp windings. The disadvantages are that it takes some time to set up the routing rules and the expected result may not be ensured. Sometimes, when the PCB is too complicated, the autorouter is not able to route all the tracks. Thus, you still have to route some tracks manually. In the current project, a combination of manual routing and autorouter was applied [129].

The following EMC guidelines should be followed while designing a PCB [129]-[134]:

1. Identify the noise sources and eliminate them as close to the source as possible. Since the source of the received noise lies usually outside the system, the first possibility for the designer to handle noise is on the system inputs.
2. Control the path to the ground. Signals and noise will always take the shortest path to the ground. The task of the system designer is to make sure that noise will find a path to the ground before leaving the system or reaching sensitive signals. The best way to do so is to add a complete ground plane to the board.
3. Avoid large current loops. Current loops are acting like antennas, they emit and receive noise. The larger the loop, the more interference there can be. Loops should therefore be as small as possible. The best solution for high frequency signals is using a complete ground plain on one side of the PCB. The return path in the ground plane will be the track with the smallest impedance, i.e. the path exactly under the signal track. Thus, also the current loop is the smallest. In the case of low frequency signals, the return path will be the track with the smallest DC resistance, in other words the shortest route. One thing to bear in mind is that any slits or tracks in the ground plane could block the optimal return path and lead to undesired results. In case no ground or power plane can be made, the power and ground lines should always be drawn as close as possible to each other.
4. Keep the analogue tracks as short as possible. Analogue signals are the most sensitive signals to the disturbances.

5. Filter the power supply. Badly coupled power supply is one of the most common reasons for EMI problems. The current drawn by digital electronics consists of short spikes occurring on the clock edges. Those pulses in the power lines can interfere with other devices that are connected with the power supply. To filter these spikes, decoupling capacitors are placed as close to the component as possible.
6. Avoid 90 º corners and other abrupt transitions on traces. It is recommended to use 45 º angles instead of 90 º. All abrupt transitions on the traces increase the radiation.
7. Split the layout in zones. Sometimes if the PCB is very complicated, it might be impossible to handle every EMC problem at once. Therefore it might be a good idea to split the design into subparts and handle the EMC problems individual for every zone. The basic idea is to separate noisy parts and components from the sensitive ones. In general, the power supply and digital part should always be separated from the analog part.

Design and optimization of PCBs

All the PCBs are double sided with the dimensions of 160x100 mm, which makes them suitable for the rack system, as shown in Fig. 3.8. The PCBs are connected with each other through a bus system in the backside of the rack.

A. Voltage measurement PCB

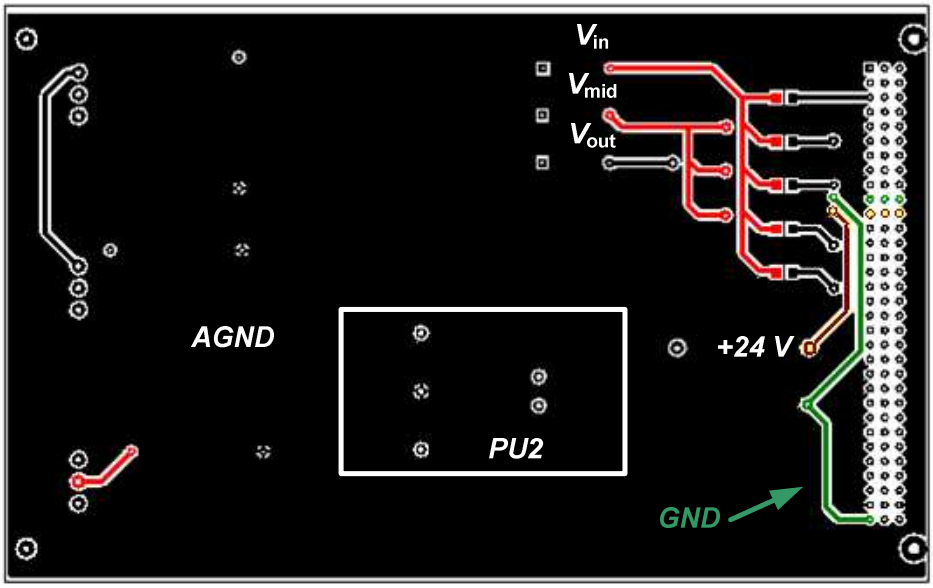
The top and bottom view of the layout of the voltage measurement PCB is shown in Fig. 3.25. It has three analogue channels V_{in}, V_{mid}, V_{out} and one switching mode power supply (*PU2*) for the sensors. The sensitive analogue signals should be kept away from digital power supply *PU2* and power lines (+/- 15 V, 24 V).

Optimized features of the board:

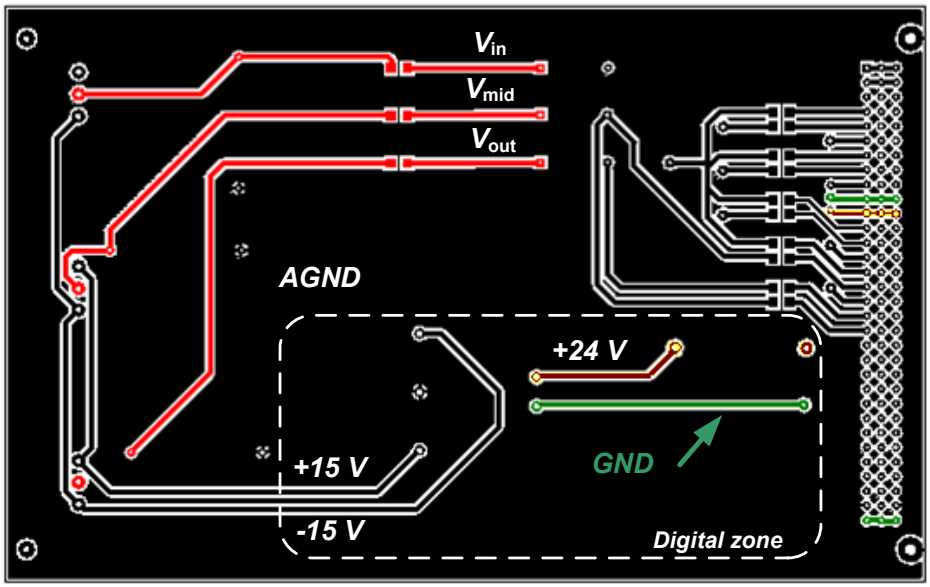
- track windings are mostly 45 degrees without sharp transitions, which reduces the radiation risk;
- the layout splitting principle has been used, the digital zone is kept away from analogue part, as shown in Fig. 3.25 (b);
- both, the bottom and top side of the PCB (Fig. 3.25) are covered with ground plane AGND;
- the analogue signal routes are optimized in length;
- minimized current loops (parallel routing of +/- 15 V and 24 V).

Potential weak-points:

- due to complexity there are tracks on both sides of the board thus, the ground planes are interrupted and it may disturbs the return paths of the signals;
- no digital ground plane under the digital zone (Fig. 3.25 (b));
- there are no decoupling capacitors on the +24 V power line, which may introduce disturbances in the analogue part.



(a)

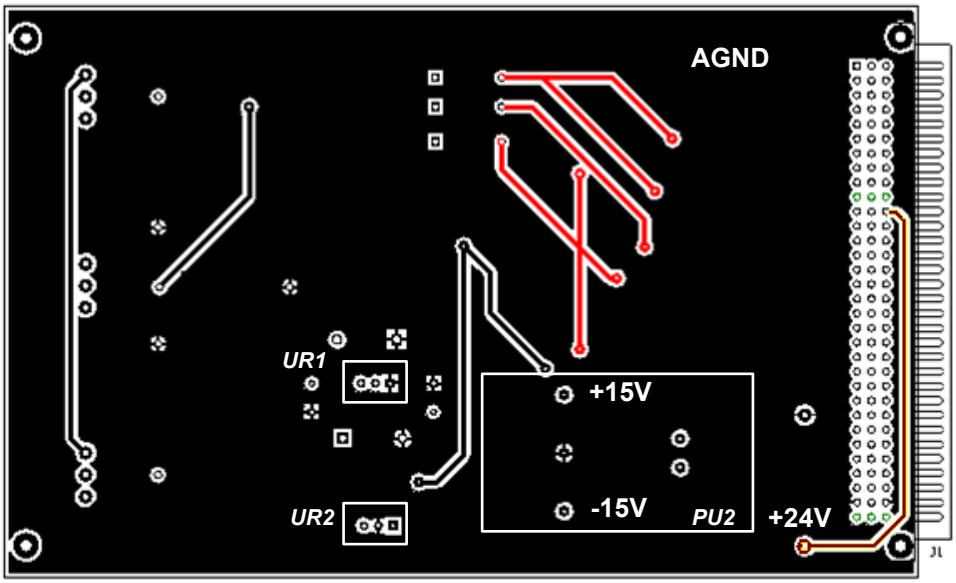


(b)

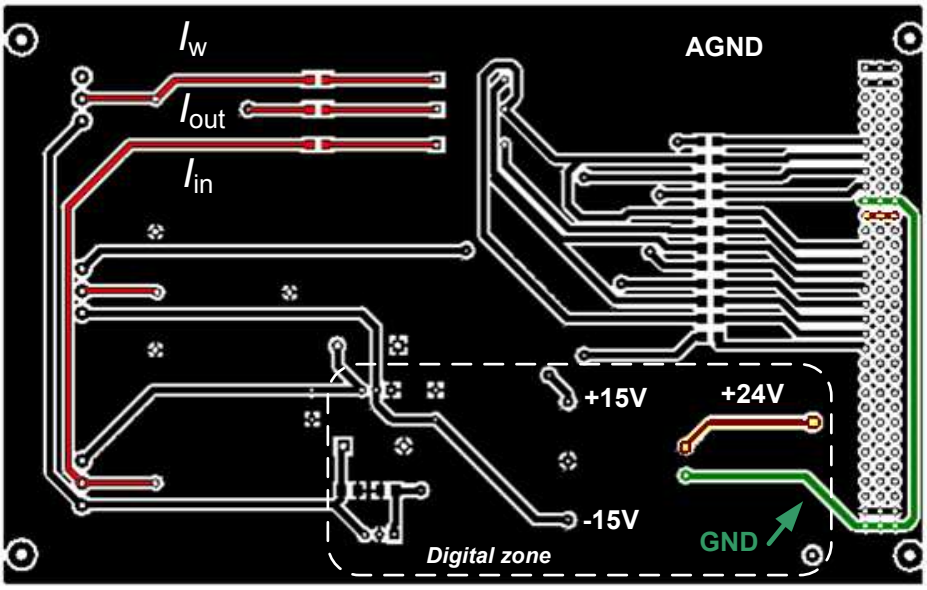
Fig. 3.25 Top (a) and bottom (b) view of the voltage measurement PCB layout

B. Current measurement PCB

The top and bottom view of the layout can be seen in Fig. 3.26. The analog part of the board consists of three analog channels I_w, I_{out}, I_{in}, the digital part contains one switching mode power supply (PU1) and two voltage regulators (*UR1*, *UR2*).



(a)



(b)

Fig. 3.26 Top (a) and bottom (b) view of the current measurement PCB layout

Optimized features of the board:

- track windings are mostly 45 degrees without sharp transitions, which reduces the radiation risk;

- the layout splitting principle has been used, the digital zone is kept away from analogue part, as shown in Fig. 3.26 (b);
- both, the bottom and top side of the PCB are covered with ground plane AGND;
- analogue tracks have optimized lengths;
- minimized current loops (parallel routing of +24 V power lines).

Potential weak-points:

- due to complexity there are tracks on both sides of the board, which may disturbs the return paths of the signals;
- no digital ground plane under the digital zone (Fig. 3.26(b));
- there are no decoupling capacitors on the +24 V power line, which may introduce disturbances in the analogue part.

C. Control unit PCB

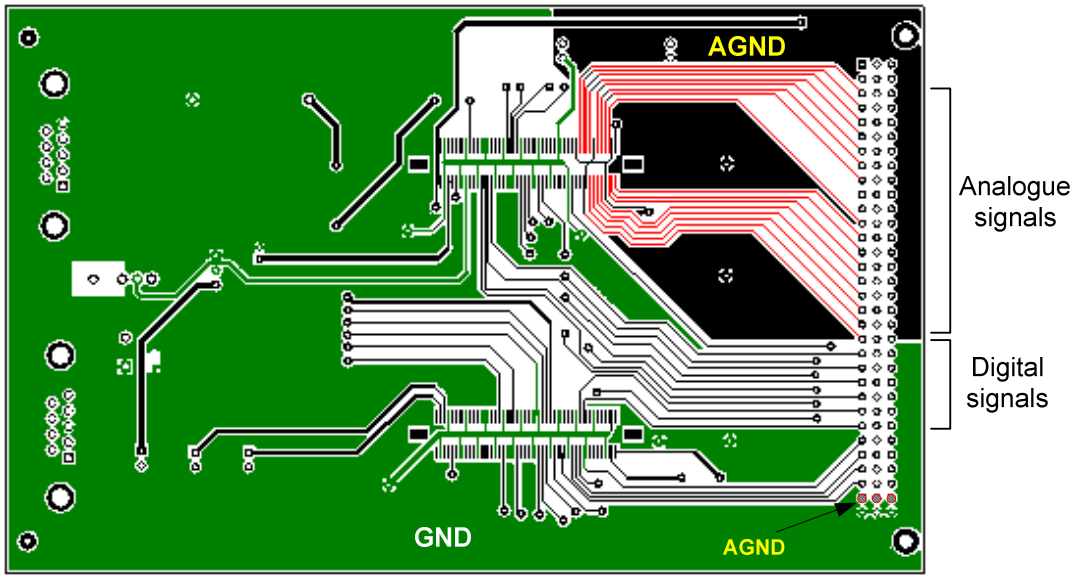
The control unit board layout is presented in Fig. 3.27. The control unit module (MODUL1) is an integrated system, including everything that is needed for a control system. The module works at the frequency of 40 MHz, which makes form it a potential EMI source.

Optimized features of the board:

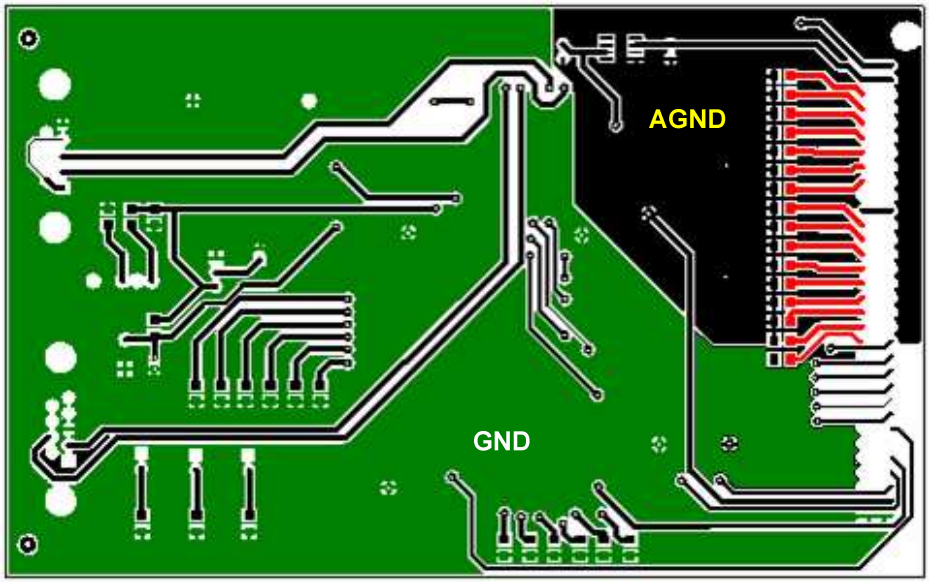
- track windings are mostly 45 degrees without sharp transitions, which reduces the radiation risk;
- the layout splitting principle has been used, the digital ground (GND) is separated from analogue ground (AGND), as shown in Fig. 3.27;
- analogue signals are kept a part from the digital signals;
- both, the bottom and top side of the PCB are covered with ground planes;
- the tracks have optimized lengths.

Potential weak-points:

- due to complexity there are tracks on both sides of the board, which may disturbs the return paths of the signals;



(a)



(b)

Fig. 3.27 Top (a) and bottom (b) view of the control unit PCB layout

3.3.3 Selection of the Digital Control Unit

The two best suitable types of controllers for FEC are: DSC or a general purpose MC. In order to find out the best control unit a comparative analysis was carried out. The following criteria for evaluation were established:

1. electrical and mechanical parameters;
2. features of the development software;
3. working frequency – the higher the frequency, the better performance can be achieved;

4. the number of peripherals including PWM timers, GPT, ADC, digital/analogue I/Os etc.;
5. structure of the interrupt handling system;
6. variety of interrupt sources;
7. integration readiness into a user specified application;
8. price.

According to those criteria, two widely used 16 bit digital control units (Infineon MC XC167 and Texas Instruments DSC TMS320F28335) specially designed for industrial applications were compared to each other. They have an extra wide ambient operating temperature range, reaching from -40 to +125 ºC (industrial temperature range), power optimized design and a rich peripheral set for numerous applications.

The comparative data of the two controllers is shown in Table 12. The DSC F28335 is optimized for industrial applications, such as digital motor control, digital power supplies and intelligent sensor applications. The first feature that distinguishes it from the microcontroller XC167 is nearly four times higher operating frequency, which improves the overall performance of the DSC. The 12 bit ADC in combination with the faster system clock of the F28335 allows much faster and more accurate measurements that can be achieved with 10 bit ADC of the XC167. XC167 has two more GPT than F28335. However, the lack of timers is compensated by a flexible peripheral synchronization system. In the control of a DC/DC converter based on the HB topology, a parameter of essential importance is the number of PWM timers. For HB topology at least two synchronized PWM timers are required. From this point of view both digital control units are suitable but as soon as the system exhibits higher complexity and more than two synchronized PWM timers are needed, the implementation of the XC167 appears more complicated. It has four PWM timers, which cannot be fully synchronized with each other. In addition, centre-aligned PWM mode is only possible with two timers. F28335's PWM generation module is of much higher flexibility, with six timers and numerous synchronization possibilities. The advantages of the MC XC167 are its higher amount of on-board program memory (flash) and twice lower power consumption in full power mode. However, in general, considering that the memory can be extended and power consumption optimized by switching off unneeded peripherals, the DSC is a better choice for the current application.

Table 12 Technical specifications of digital control units

	XC167	**F28335**
Operating frequency	40 MHz	150 MHz
ADC	10 bit, 16 channels	12 bit, 16 channels
GPT	five 16 bit timers	three 32 bit timers
PWM timers	four 16 bit timers	six 16 bit timers
Memory: RAM Flash	 64 KB 1 MB	 68 KB 512 KB
Supply voltage: device core	 5 V 2,5 V	 3.3 V 1.9 V
Operating temperature	-40 ºC…+125 ºC	-40 ºC…+125 ºC
Max power consumption	300 mW	600 mW
Power consumption in idle mode	245 mW	228 mW

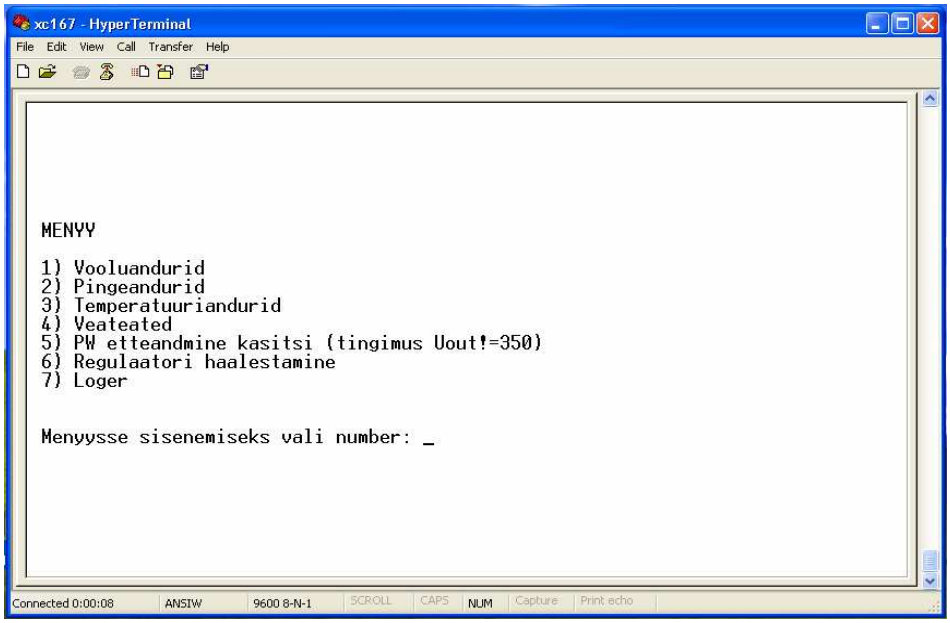
3.3.4 Diagnostic and Communication Interface

Although the front-end converter is able to work completely autonomously, it still has a built-in diagnostic and communication interface, which can be connected to other external devices. Data exchange between an external device and the FEC is currently realized via serial communication interface (RS-232), which is also supported by the MVB network protocol. With the standard Windows communication program HyperTerminal, the entire information from the FEC can be observed and also changed to some degree, as shown in Fig. 3.28. The diagnostic and communication interface includes the following functions:

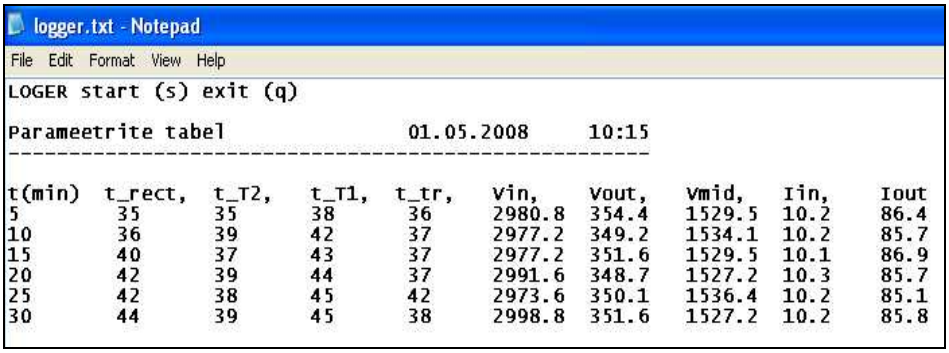
- display of sensor readouts;
- read the error code;
- programmable relay outputs, i.e. different events to be indicated can be chosen;
- real time adjustment of regulator parameters;
- manual pulse width adjustment in online or offline mode;
- real time log and display of sensor data and error code, possibility of data storage for offline analysis.

The sensor readouts are displayed only in the online mode while the error code can be also seen in the offline mode. The flexibility and functionality of the converter has been increased with several integrated adjustment functions, e.g. the user can manually adjust the duty cycle, regulator parameters and logger time step. Long term measurements can be done using the integrated logger. The logger stores readouts of all sensors. Recording of electrical and physical

parameters during test-operation allows the analysis of faults and malfunctioning modes of converter operation. Data is recorded to the PC hard disk in the tabular form, as indicated in Fig. 3.28 (b). The data could be later analyzed in the spreadsheet programs (e.g. MS. Excel) in the form of diagrams (Fig. 3.29) [9].



(a)



(b)

Fig. 3.28 Diagnostic and communication interface displayed in the HyperTerminal window (a), measurement data saved by the logger (b)

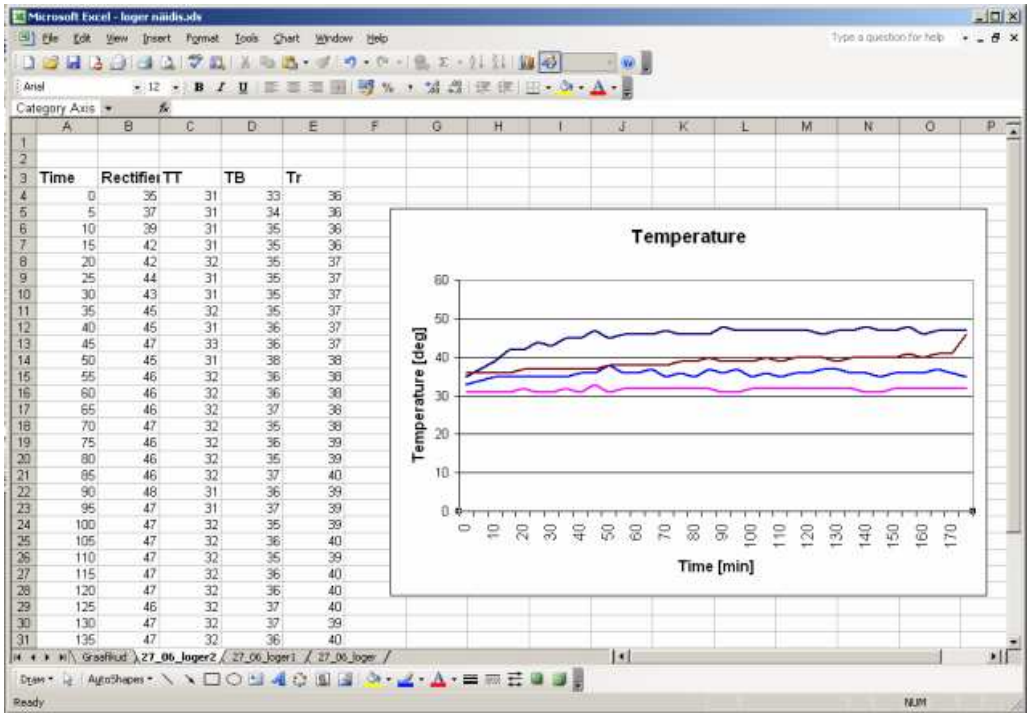


Fig. 3.29 Logger data analysis in Excel

In addition, the current FEC is provided with two relay outputs, which are connected with two lamps (red and green), as shown in Fig. 3.1. The user can choose which events are to be indicated by each lamp, e.g. nominal output voltage reached, maximal load in the output, dangerous voltages in the input, nominal operation range reached in the input. Each lamp can be connected with one event only.

3.3.5 Advanced Protection System

Although the HB isolated DC/DC converter topology seems to be a very attractive solution for the HP and HV electronic converters due to its overall simplicity, small component count and low realization costs, this converter also has to comply with numerous safety requirements in railway applications. Clearly, a robust protection and diagnostic system is essential. The protection system should minimize the risk of serious failures while diagnostic system helps to analyse the reasons of the faults and thus, improve the overall performance of the converter.

In principle, the protection system is divided into two parts: hardware and software based protections (Fig. 3.30). The software based protections are: output voltage observation, cross conduction prevention, volt-second unbalance detection, over- and undervoltage protection, overload protection, temperature check and soft start feature. The hardware based protections are (Fig. 3.30): dead time generation, common signal blocking, and automatic transistor blocking in the case of short circuit. In general, hardware serves as a second level protection against software errors, which means that some of the protection functions are duplicated.

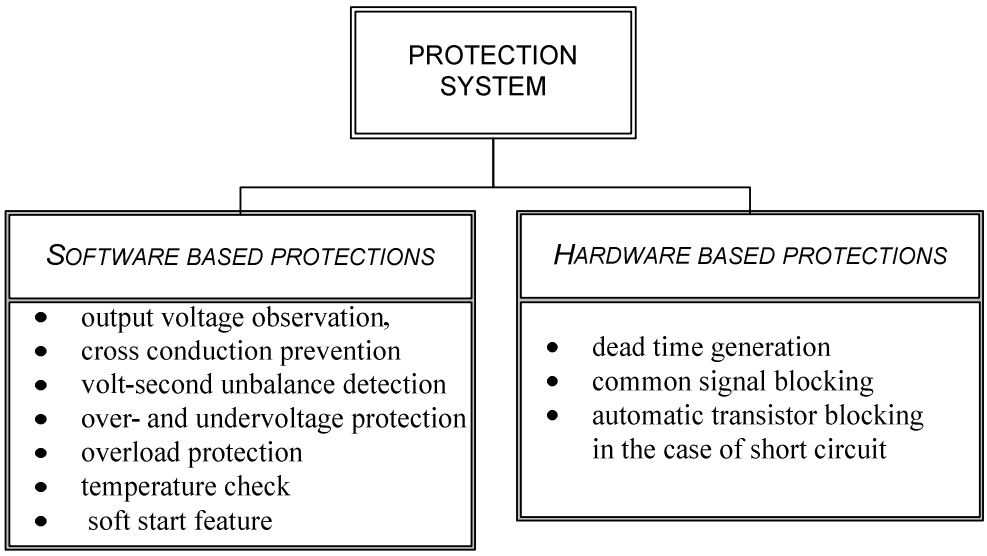


Fig. 3.30 Structure of the protection system

Software based protections

According to end-user requirements currently the output voltage range is 350 V ± 5 %. In order to guarantee the output stability it must be constantly observed and regulated.

Cross conduction means that both transistors of the HB are conducting simultaneously thus, causing a short circuit. In order to prevent cross conduction the PWM signals must be 180 º phase shifted (phase shift block in Fig. 3.1) and the theoretical maximal duty cycle may not exceed 0.5, as indicated in Fig. 3.31. The real maximum value depends on the circuit and transistor parameters. But if the parameters are not known, many handbooks recommend to choose the duty cycle value 0.4, which in the most cases provides sufficient safety margin and optimal control bandwidth.

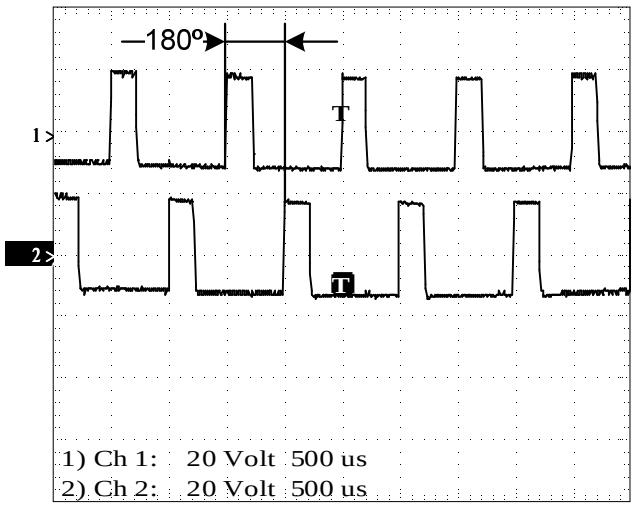


Fig. 3.31 Cross conduction prevention, 180° phase shifted PWM signals with the maximum duty cycle 0.4

In order to prevent volt-second unbalance of the isolation transformer the voltage of the input capacitor U_{C2} is measured and compared to the input voltage. Voltages of input the capacitors C_1 and C_2 are balanced if the following condition is fulfilled:

$$U_{C2} = \frac{U_{in}}{2}. \tag{31}$$

Over- and undervoltage protection is related to the input voltage, which is constantly observed. Any values outside the allowed voltage variation range result in an error message.

Load of the converter can be estimated by measuring the output current. In the current case the output current must not exceed 140 A.

The front-end converter is equipped with temperature sensors, which constantly measure the temperatures of all semiconductor devices, isolation transformer, and output choke.

Starting the front-end converter can be a problematic issue due to the discharged output capacitors. The dangerous current peaks occurring in the output can be avoided with a soft start algorithm that has been added to the control program. It gradually increases the duty cycle of the IGBT transistors until the nominal output voltage has been reached, as shown in Fig. 3.32. After that the system proceeds to the normal operating mode.

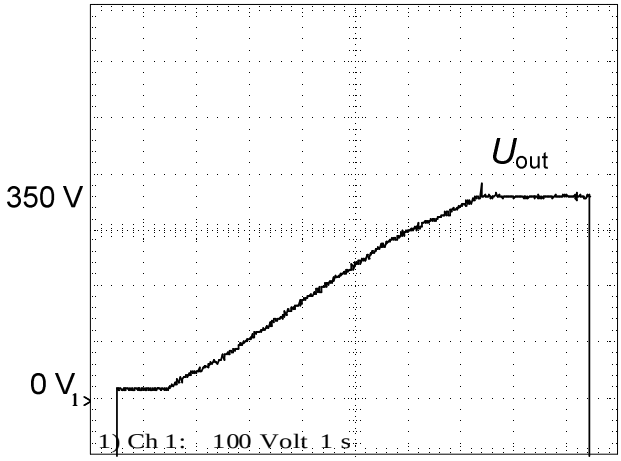


Fig. 3.32 Soft start algorithms gradually increases the output voltage

Hardware based protections

As discussed before, simultaneous conduction of transistors in the HB configuration creates a short circuit. Clearly, the transistors would not normally be driven such that they both are on at the same time. The cause of cross conduction lies usually in the overlap of turn-off and turn-on transients of switching transistors. Although the maximal duty cycle is limited within the software, a second level protection within hardware is recommended. That is realized by implementing a dead time to each positive signal front. The delay

must be of sufficient duration to ensure a safe operation. To calculate the right delay time we must know the signal propagation delay from the control unit to the IGBT. The minimum dead time requirement for HB converters can be calculated as follows:

$$t_{\mathrm{d}} = ((t_{\mathrm{off-max}} - t_{\mathrm{on-min}}) + (t_{\mathrm{PDD-max}} - t_{\mathrm{PDD-min}}) + \\ + (t_{\mathrm{PDD\_cs\_max}} - t_{\mathrm{PDD\_cs\_min}}) + (t_{\mathrm{d\_fall\_max}} - t_{\mathrm{d\_rise\_min}})) \cdot b\,, \qquad (32)$$

where $t_{\mathrm{off\text{-}max}}$ is the maximal turn-off time of the transistor, $t_{\mathrm{on\text{-}min}}$ is the minimal turn-on time of the transistor, $t_{\mathrm{PDD\text{-}max}}$ is the maximal propagation delay of the driver, $t_{\mathrm{PDD\text{-}min}}$ is the minimal propagation delay of the driver, $t_{\mathrm{PDD\text{-}cs\text{-}max}}$ is the maximal propagation delay of the control system, $t_{\mathrm{PDD\text{-}cs\text{-}min}}$ is the minimal propagation delay of the control system. The result is multiplied with the safety margin *b* obtained from field experience [135]. In the current case the minimum dead time requirement is 2.4 µs. The actual dead time must be chosen greater than $t_{\mathrm{d\text{-}min}}$. In the current case it is 8.3 µs. The measured signal before and after the dead time circuit is presented in Fig. 3.33.

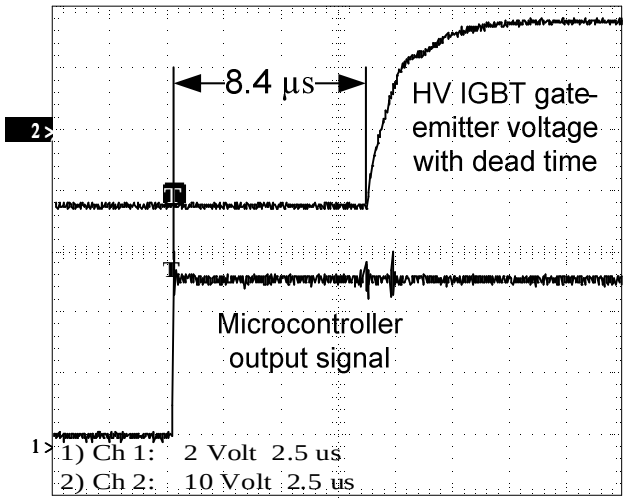
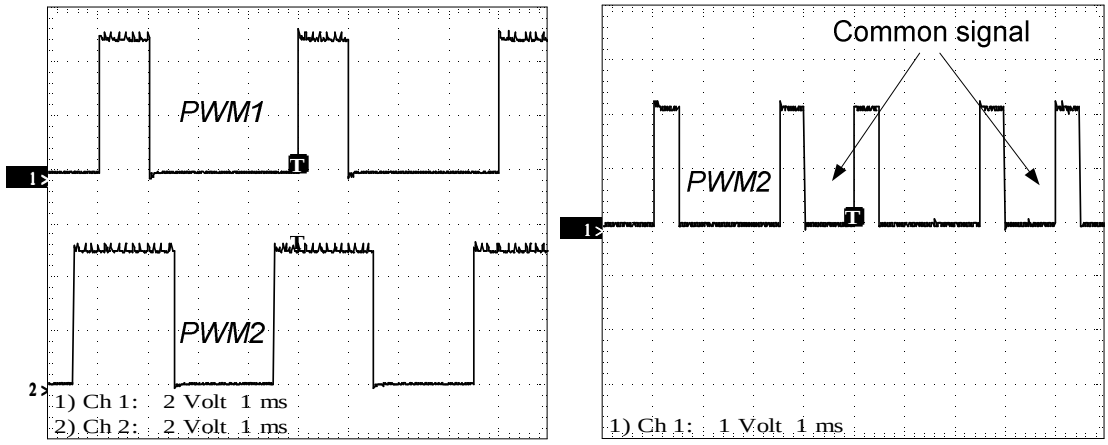


Fig. 3.33 Dead time generation

The control algorithm generates 180° phase shifted PWM signals. Even a small change in the phase shift can cause a short circuit. That can be avoided with the common signal blocking circuit, as illustrated in Fig. 3.16. The controller generates two PWM signals (Fig. 3.34(a)). In the output only *PWM2* will occur while *PWM1* is completely blocked due to overlapping. The resulting signal is shown in Fig. 3.34 (b).



(a) *(b)*

Fig. 3.34 Common signal blocking action: input signals (a), resulting output signal (b)

In general, all modern IGBT drivers are provided with integrated short circuit protection function. The short circuit detection is realized by monitoring the collector-emitter voltage. The circuit checks if during the first 10 µs after turn on the collector-emitter voltage has dropped below some pre-defined level that depends on the IGBT type. If the collector-emitter voltage does not shrink below that level, the short-circuit condition is assumed and the IGBT will be switched off immediately. After that a driver status feedback signal is sent to the main controller that will then switch off the rest of the control system.

The status feedback signals are checked by the control unit. An interrupt based method was proposed to measure the width of the status feedback pulses (Fig. 3.6). Both the rising and the falling edge create an external interrupt. Interrupt on the rising edge starts a timer and interrupt on the falling edge stops it. Thus, the status feedback pulse width can be measured and Table 13 shows possible errors that can be detected according to that information.

Table 13 Different errors according to the driver status feedback signals

Width	T_T	T_B	**Error message**
>10 µs	+	-	T_T not working properly or optical link interruption
>10 µs	-	+	T_B not working properly or optical link interruption
>10 µs	+	+	Short circuit
<2 µs	+	+	Normal work, no error

All three errors cause the inverter to shut down. If one of the first two errors occurs, then the inverter will be switched off by the main controller of the converter. In the case of short circuit, the driver automatically inhibits the control signal and the IGBTs will be switched off. After that the error signal will be sent to the main controller. Thus, the short circuit protection is independent of the main controller. However, if any of those errors occurs, no automatic start will be possible. The host controller needs to be reset manually before the inverter can be started again.

Fault detection and classification algorithm

In general, any failure or inadmissible operation conditions always create a warning and/or alarm message, which will be stored in the error code. The front-end converter is provided with various sensors (Fig. 3.1). The errors that can be detected are listed in Table 14.

Table 14 Classification of integrated protections

Condition	**Action**
Transistor malfunction	
driver status code	Terminate program, manual reset
Short circuit	
driver status code	Terminate program, manual reset
Input undervoltage	
U_{in} < 2200 V	Suspend program
U_{in} >= 2300 V	Automatic recovery
Input overvoltage	
U_{in} > 4000 V	Suspend program
U_{in} <= 3800 V	Automatic recovery
Overload	
I_{out} >140 A	Terminate program, manual reset
Short circuit	Terminate program, manual reset
Output overvoltage	
U_{out}>368 V	Terminate program, manual reset
Output undervoltage	
U_{out}<333 V	Terminate program, manual reset
Prevention of the transformer saturation	
U_{C2} shift >5%	Terminate program, manual reset
Overheating of the transistors	
T_T>=60º	Terminate program, manual reset
Overheating of the rectifier	
T_{rect}>=50º	Terminate program, manual reset
Overheating of the transformer and/or output inductor	
T_{trafo}>=60º	Terminate program, manual reset

Errors are divided into two groups. The faults in the first group terminate the control program. For recovery, manual reset of the controller is needed. The second group errors do not terminate the program and automatic recovery is possible after the error has been eliminated. The general algorithm for fault detection prioritization is shown in Fig. 3.35.

According to Table 13, three hardware errors can be read from the driver status code. A transistor malfunction creates a first group error and the program will be terminated. Thus, automatic recovery is not possible. Short circuit protection is independent of the main controller which receives accordingly the

error message after the IGBTs are already blocked by the driver. Short circuit creates the first group error.

The input and output voltage is sensed to discover over- or undervoltages. In the case of an over- or undervoltage in the input, a second group error will be created, the system will be switched off and automatically restored after the voltage has returned in the nominal area. Similarly, the output voltage is regulated but once the output is switched off, no automatic recovery is possible (Fig. 3.35).

In order to prevent volt-second unbalance of the transformer primary the condition (31) must be fulfilled. Any difference greater than 5 % results in an immediate blocking of IGBTs. The recovery is only possible after manual reset of the control system.

The capacitor voltage check is followed by the temperature measurement in transistors, the rectifier and the transformer. An overheated system will be automatically switched off and also needs manual reset.

The output current is measured to determine the overload situation. In the case of overload, the system will be switched off and manual reset is required for recovery.

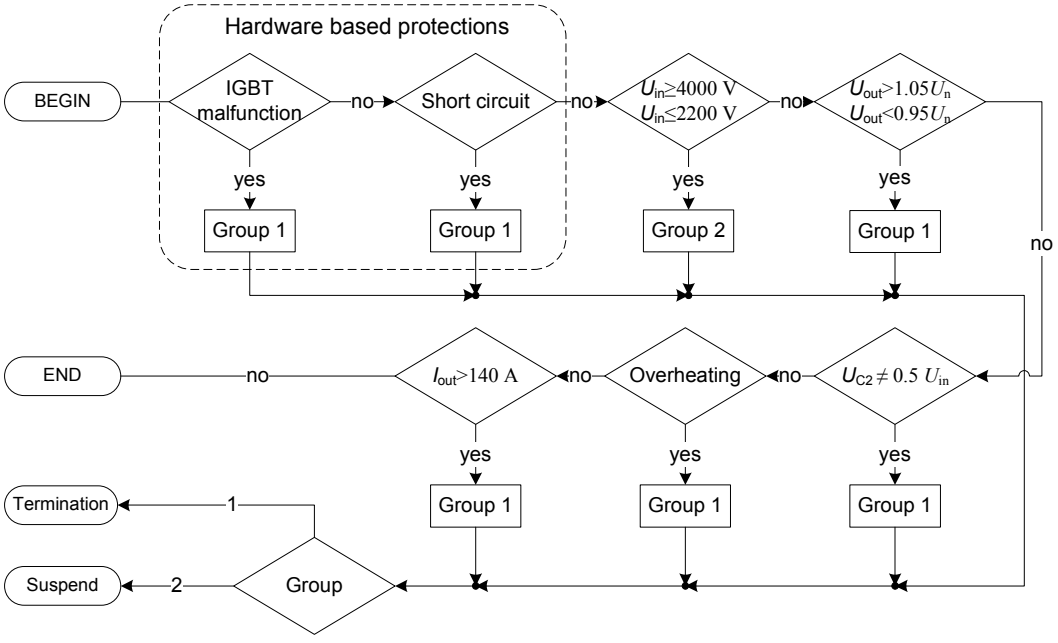


Fig. 3.35 Flow chart of the fault detection and classification algorithm

The practical evaluation of the input undervoltage protection function is shown in Fig. 3.36. Undervoltage (U_{in} < 2200 V) in the input creates a group 2 error and the output is blocked. The output voltage is automatically recovered if the input voltage exceeds the value 2300 V. The output voltage increases with the ramp due to the soft start system.

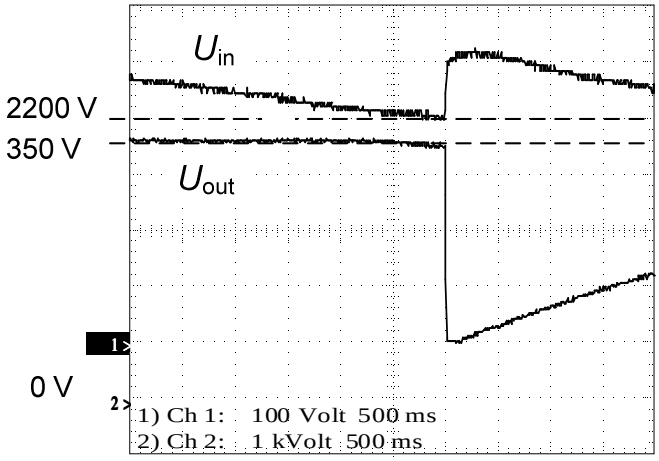


Fig. 3.36 Input undervoltage protection and soft start system

3.3.6 Capacitor-Related Volt-Second Unbalance Problems

In order to verify modelled results in chapter 2.2.3, experiments were carried out. The experiments were performed with the following parameters: input voltage 500 VDC, input capacitors C_1=300 µF, C_2= 200 µF, and switching frequency 1 kHz. Fig. 3.37 shows the performance of the symmetrical duty cycle and unsymmetrical input capacitors. Comparison of these results to those of the simulation (Fig. 2.11) reveals the similarities. No voltage unbalance occurred.

Fig. 3.38 and Fig. 3.39 show experimental results for the unsymmetrical duty cycle and unequal input capacitors. Depending on the duty cycle, two cases were considered: $D_{TT}>D_{TB}$ and $D_{TT}<D_{TB}$. Comparing these results with those of the simulation (Fig. 2.12 and Fig. 2.13), similarities can be seen. Voltage difference 50 V appears in both simulation and experiments.

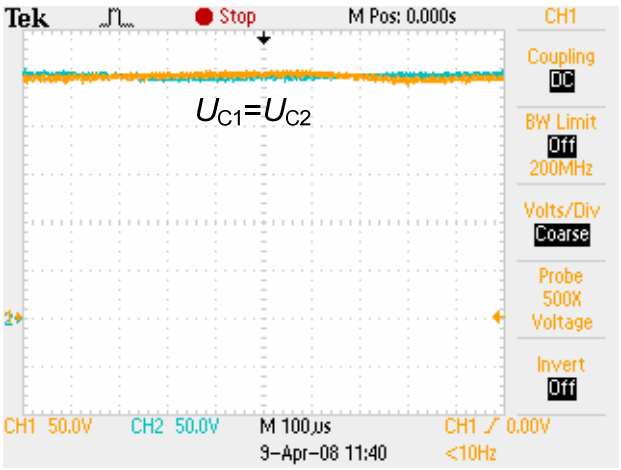


Fig. 3.37 Unequal capacitances and symmetrical duty cycle

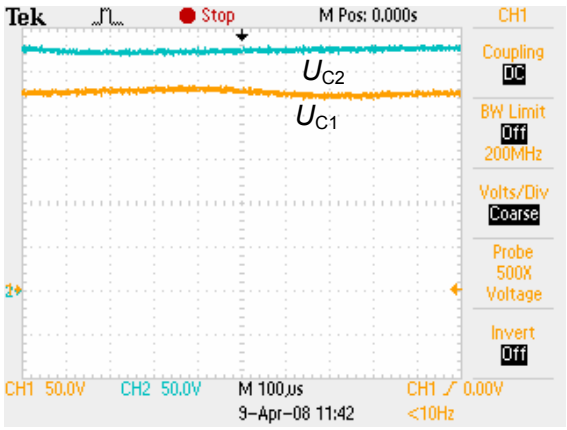


Fig. 3.38 Unequal capacitances and unsymmetrical duty cycle (D_{TT}>D_{TB})

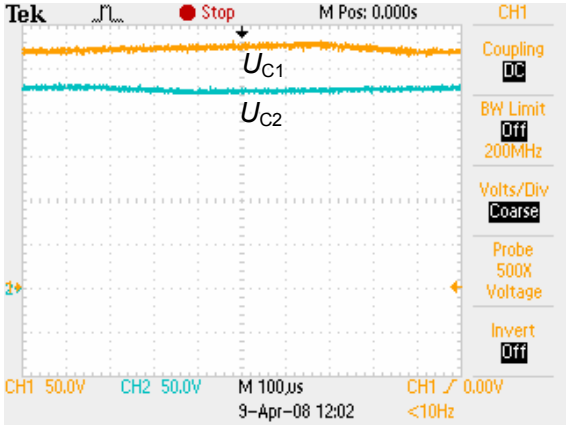


Fig. 3.39 Unequal capacitances and unsymmetrical duty cycle, (D_{TT}<D_{TB})

The simulations and experiments prove that unequal capacitors do not deteriorate the volt-second unbalance issue even in the case of unsymmetrical duty cycles. Thus, the role of input capacitors mismatch in the HB converter is not significant and the capacitance change due to rugged environmental conditions can be neglected.

3.3.7 Mathematical Representation of the Digital Type II Compensator

Resulting from the simulations and previous analyses the best control algorithm for the FEC based on two- or three-level HB topology is digital VMC with the type II compensator. The classical mathematical form of a digital type II compensator is:

$$y_k = K_P \cdot e_k + K_I \cdot \sum_{i=1}^{k} e_i \cdot T_A \,, \tag{33}$$

where y_k is controlled variable at the present moment, K_P is proportional gain constant, K_I is integral gain constant, T_A is integration time step, e_i is the sum of all errors in the regulator input. The disadvantage of this equation is the summation of the errors. In microcontrollers all the data is stored in variables, which size must be defined before compiling and running the program. Since

the values and the number of errors in the regulator input are unknown, it is difficult to estimate the needed memory size. This can lead to unknown errors if the summation variable exceeds the predefined memory space. The controlled variable of the previous cycle can be calculated as:

$$y_{k-1} = K_P \cdot e_{k-1} + K_I \cdot T_A \cdot \sum_{i=1}^{k-1} e_i \,. \tag{34}$$

By subtracting (34) from (33) we will get the change of the controlled variable

$$\Delta y = K_P \cdot (e_k - e_{k-1}) + K_I \cdot T_A \cdot e_k \,. \tag{35}$$

By summing (35) and (33) we get new a regulator output

$$y_k = y_{k-1} + \Delta y$$

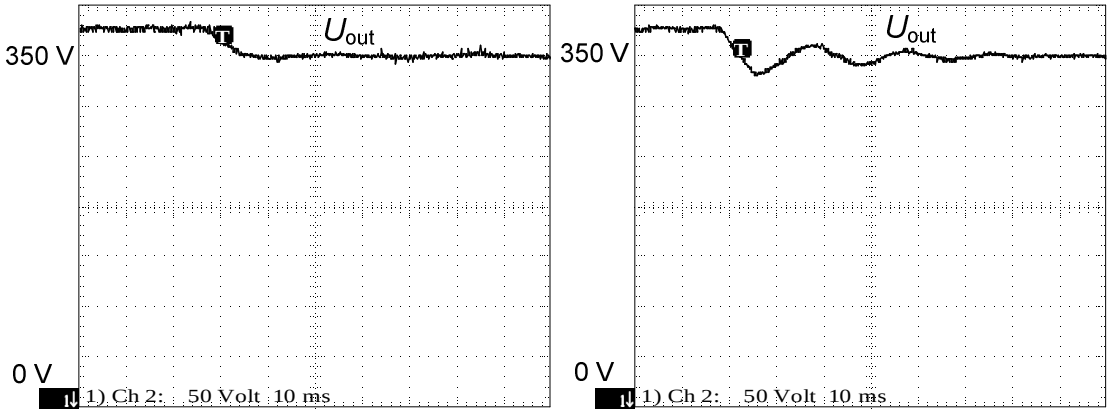
$$y_k = y_{k-1} + K_P \cdot (e_k - e_{k-1}) + K_I \cdot T_A \cdot e_k \,, \tag{36}$$

where y_{k-1} is the previous value of the controlled variable, e_k is the error at the present moment, e_{k-1} is previous error. It results that the regulator output can be calculated based on just two subsequent errors and the previous controlled variable value. There is no need to sum all the errors. This algorithm is more reliable and simple than the classic equation of digital type II compensator. Thus, (36) was also implemented in the current front-end converter.

3.3.8 Practical Tests of the Voltage Mode Control Algorithm

All test conditions comply with the simulations. The same loads and overall conditions were used. The test prototype was loaded with a resistor network. The load changes were emulated with a conductor that connected/disconnected parallel branches of a resistor network. Input voltage was changed with an autotransformer. Thus, the load could be changed only in steps while the input voltage could be changed also gradually.

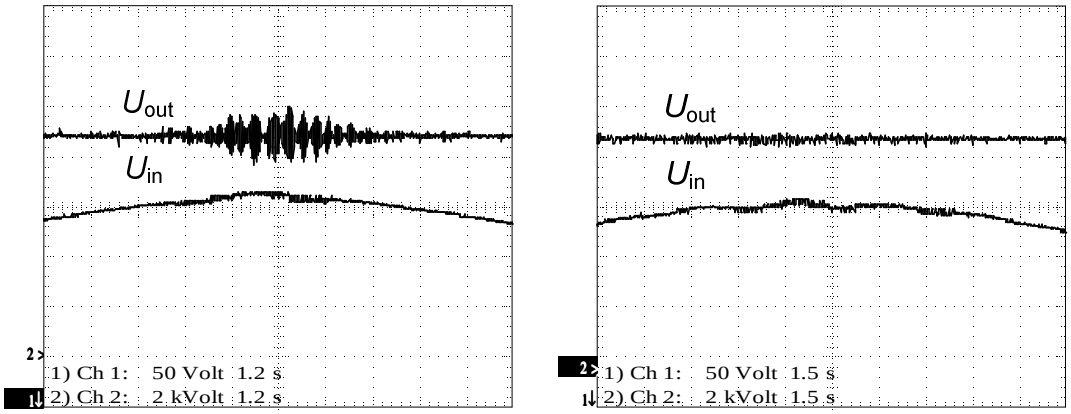
Regulator parameters can be adjusted by the user whether in online or offline operating mode. The offline adjustments are useful for transient response tests and stability studies. The term offline here is oriented to the regulator and means an operation without a regulator, i.e. the converter works with a predefined duty cycle. The user can change the regulator parameters while the output is not affected. If the regulator is turned on again, then a transient process caused by the output voltage step change occurs in the output. The regulator behavior and stability with the new parameters can be estimated from the resulting output transient response. Fig. 3.40 (a) shows somewhat overdamped response, which has excellent stability but average transient recovery performance. By optimizing regulator parameters, the transient recovery performance could be improved, as shown Fig. 3.40 (b).



(a) *(b)*

Fig. 3.40 Converter output response to output voltage step: overdamped (a), optimized (b)

The parameters acquired with the transient response evaluation do not guarantee a stable output in real operating conditions. Currently the output instabilities are caused by the changing input voltage, as shown in Fig. 3.41 (a). The parameters of the regulator need small adjustments, which can be done in the online operating mode. In the online operating mode, the effect of parameter adjustments appears instantaneously in the output. After small optimizations stable parameters for the regulator could be found (Fig. 3.41 (b)).



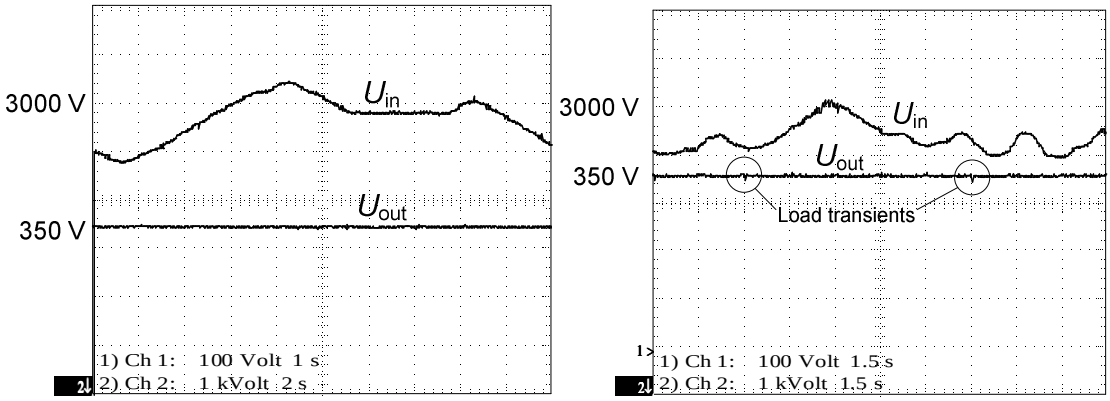
(a) *(b)*

Fig. 3.41 Output instabilities caused by the changing input voltage (a), the system response with optimized regulator parameters (b)

According to simulations (Fig. 1.41), the front-end converter in the current configuration has a good closed loop response to input voltage transients. That can be also seen from the experiment results (Fig. 3.42 (a)) where the output voltage shows very stable behaviour in the conditions of varying input voltage (2400 V…3300 V).

In the real operating conditions, both input voltage and output load can change simultaneously. The corresponding experiment results are shown in Fig. 3.42 (b). The experiment was carried out under the following conditions: input

voltage 2500 V…3100 V, load 4.7 Ω…7.5 Ω. Small spikes occurred due to rapidly changing load, however, the output voltage remained stable.



(a) *(b)*

Fig. 3.42 Closed loop response of the front-end converter to input voltage variation (a), in the conditions of changing input voltage and load (b)

In order to estimate the quality of the output voltage the voltage ripple was measured in pulse loading conditions, as shown in Fig. 3.43. In general, voltage spikes remain under 10 V, which is in accordance with the user requirements. It was noticed that by a decreasing load (from 5 Ω to 8 Ω) the steady state pulsation of the output voltage increased, as shown in Fig. 3.43.

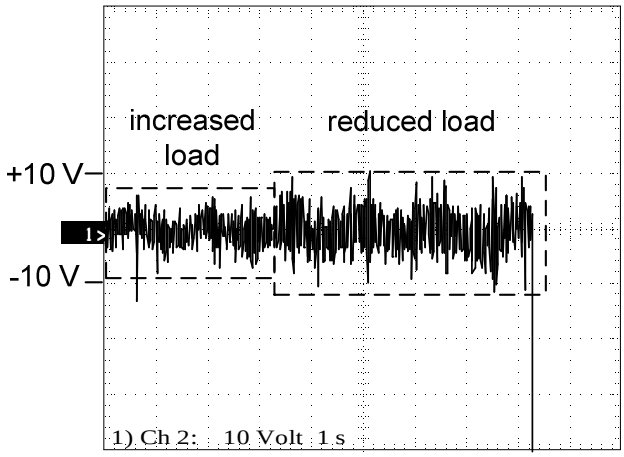


Fig. 3.43 Output voltage ripple in pulse loading conditions

In general, the results of simulations and experiments matched the expectations. The digital VMC with the digital type II compensator fulfilled all the requirements and can be effectively implemented in the proposed front-end converter for traction applications.

3.3.9 Optimization of Switching Losses in the Front-End Converter Based on the Three-Level Half-Bridge Topology

Logically, if the number of switches is increased, the switching losses will also increase. At the same time, the complexity of the topology grows, which on the other hand, allows use of new modulation strategies and soft switching

methods. In this work only soft switching techniques without additional components are studied. The simulation and partly also analyses carried out are described in the chapter 2.3.1, with the test result analyzed and compared to the simulation results.

PWM method

The test prototype had the same configuration as the simulation model in Fig. 2.48 (excluding the flying capacitor C_f). The leakage inductance of the transformer is relative high $\geq$ 30 µH. In Fig. 3.44 the voltages of the top side transistors T_1 and T_2 are shown. Following events can be distinguished:

1. The transistor T_2 is turned off, the leakage inductance of the transformer primary draws the current through freewheeling diodes D3 and D4. Full input voltage is applied across transistors T_1 and T_2 and a voltage peak occurs on the transistor T2. The pulse width of the peak depends on the primary leakage inductance. If the leakage inductance energy has been utilized, the voltage across T2 drops to zero and remains unchanged until to the end of dead time.
2. The bottom side transistors are conducting and full input voltage is evenly distributed across the upper leg transistors T1 and T2.
3. The outer transistor T4 is turned off and clamping diode Dcl2 starts to conduct. Instead of full input voltage now only half of the value is applied on the top side transistors. The voltage distribution can be seen in Fig. 3.44.
4. After a dead time T2 is turned on and the voltage drops to zero. The voltage across T1 increases to half of the input voltage.
5. T3 is turned off and the leakage inductance of the transformer primary pushes the current through freewheeling diodes D2 and D1. The voltage across T1 drops to zero. After the transformer leakage energy has been utilized the voltage across T1 increases to its previous value. The width of this narrow voltage pulse is equal to the dead time. Theoretically by increasing the leakage inductance of the transformer and/or decreasing the dead time ZVS for outer transistors can be achieved.

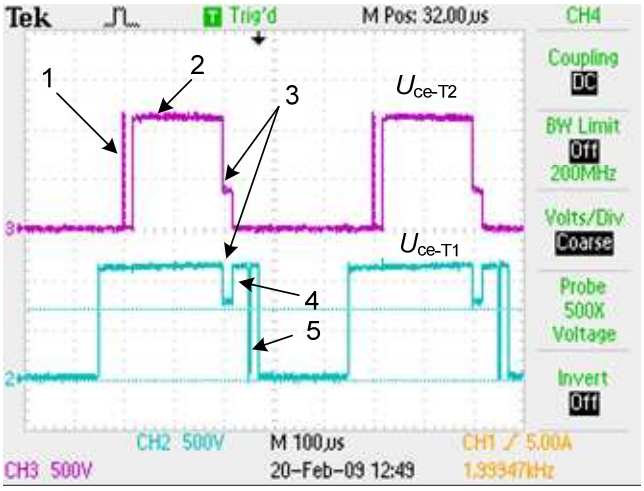


Fig. 3.44 Collector-emitter voltage of the top side transistors in the case of PWM

Voltage and current shape of the transformer primary are shown in Fig. 3.45. Following events can be distinguished:

1. Both top side transistors are conducting.
2. The outer transistor T_1 is turned off. Leakage inductance draws current through clamping diode D_{cl1}. The transformer voltage drops to zero.
3. The inner transistor T_2 is turned off. The leakage inductance draws current through freewheeling diodes D_3 and D_4 and a negative voltage impulse occurs on the transformer primary. If the leakage energy is utilized the transformer voltage and current drop to zero. Then T_3 will be turned on and current together with the voltage change direction.

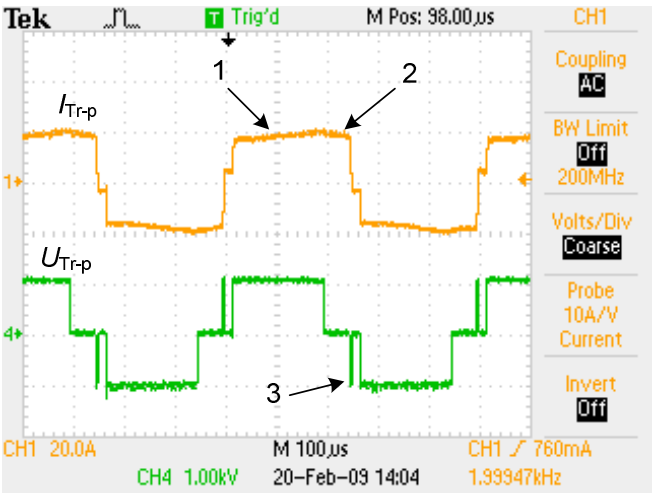
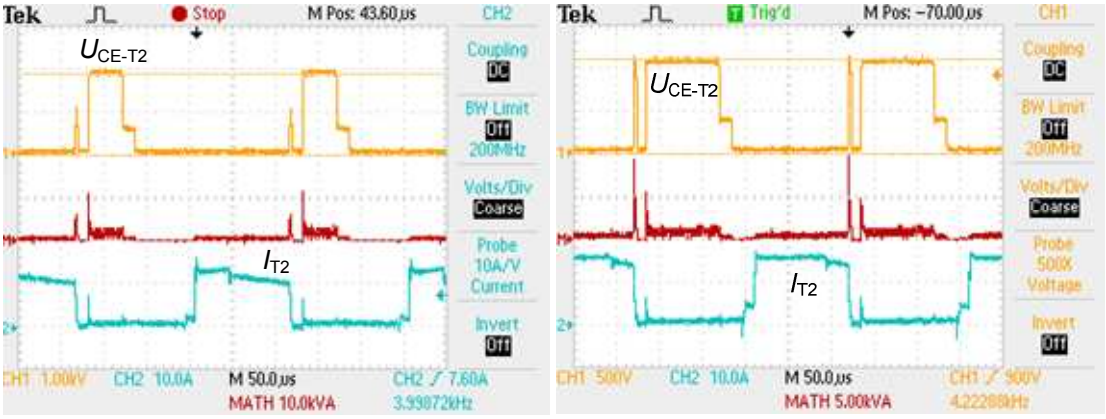


Fig. 3.45 Voltage and current of the transformer primary in the case of PWM

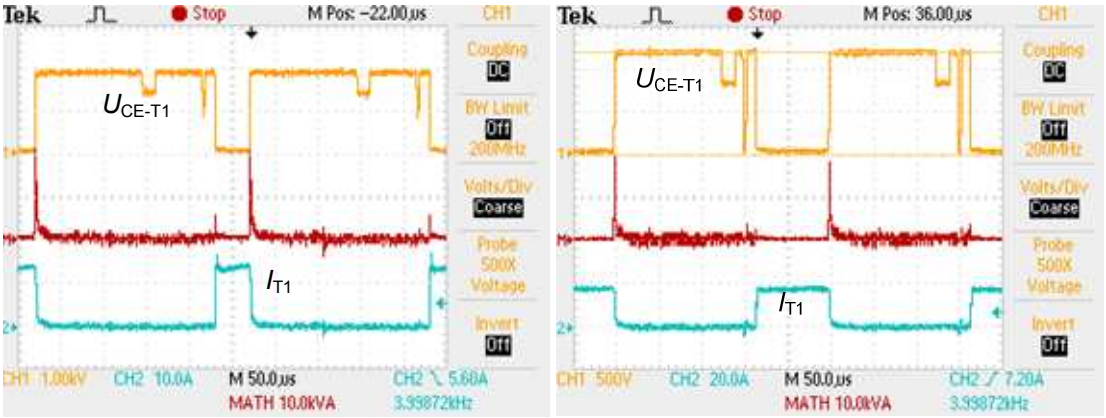
Due to the relative high leakage inductance ZCS for the inner switches is impossible. However, ZVS is achieved over the full regulation range of the

converter as shown in Fig. 3.46. The outer switches are operating in the hard switching mode, as shown in Fig. 3.47. Theoretically by increasing the leakage inductance and decreasing the dead time ZVS should be possible (as explained above).



(a) *(b)*

Fig. 3.46 ZVS of inner IGBTs: maximal input voltage (a), minimal input voltage (b)

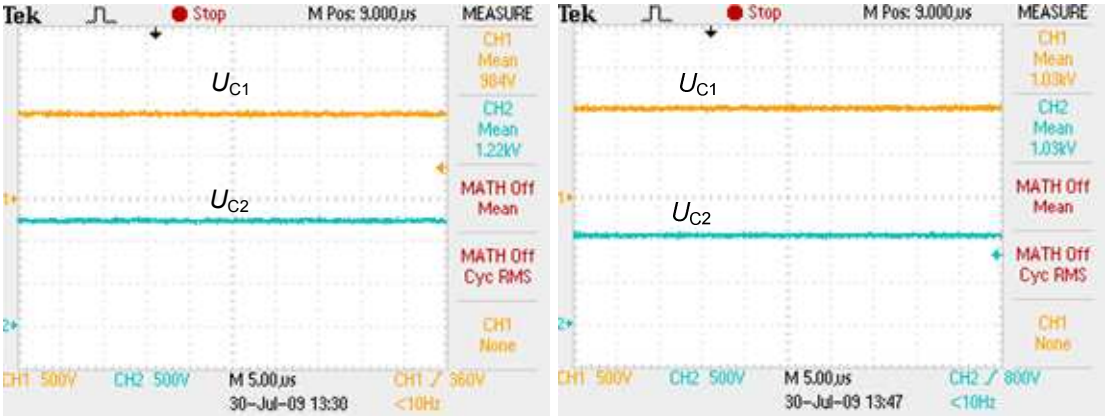


(a) *(b)*

Fig. 3.47 Hard switching of outer IGBTs: maximal input voltage (a), minimal input voltage (b)

PSM method

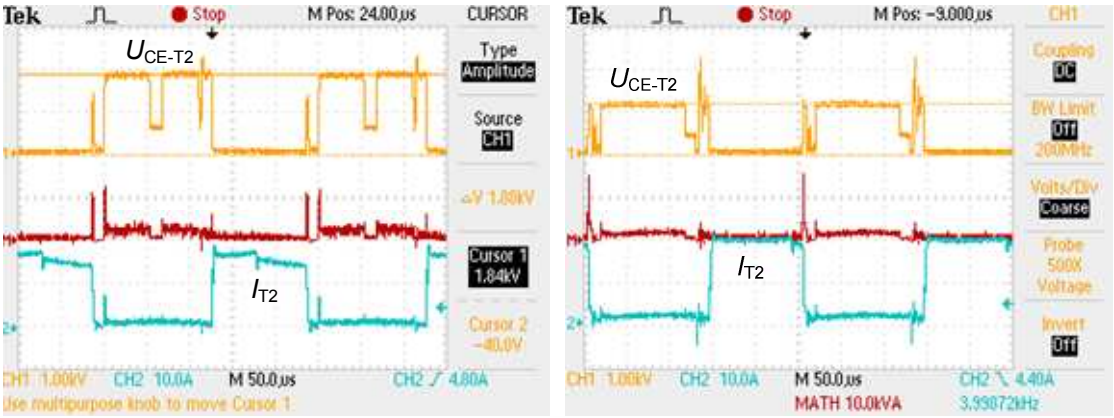
Also here the tests are based on the simulations and the same converter configuration was used, as shown in Fig. 2.48. It is recommended to use the flying capacitor since it improves the voltage balance between input capacitors, as indicated in Fig. 3.48. In order to see the effect 10 % difference was added to the duty cycles. As a result the input capacitors charged unevenly: U_{C1}=984 V, U_{C2}=1003 V. Adding the flying capacitor the voltage imbalance could be eliminated, as indicated in Fig. 3.48 (b).



(a) *(b)*

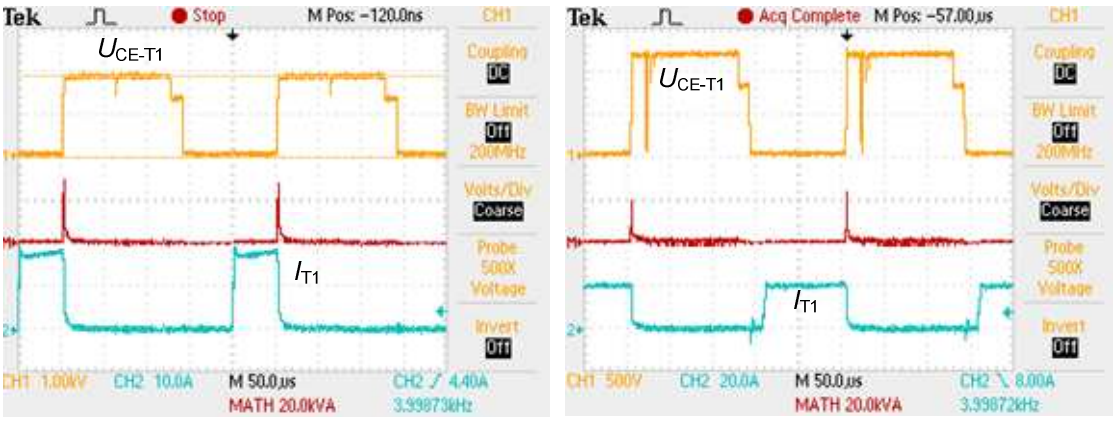
Fig. 3.48 Voltage imbalance of input capacitors due to unsymmetrical duty cycles (10 % difference): without flying capacitor (a), with flying capacitor (b)

Due to relative high leakage inductance (≥ 30 µH) ZCS for inner switches is not achievable. Both inner switches T_2 and T_3 are working in hard switching mode as shown in Fig. 3.49. In principle also ZVS can be achieved by increasing the leakage inductance and decreasing dead time. For the outer transistors T_1 and T_4 ZVS is achieved over the full regulation range, as shown in Fig. 3.50.



(a) *(b)*

Fig. 3.49 Hard switching of inner transistors maximal input voltage (a), minimal input voltage (b)



(a) *(b)*

Fig. 3.50 ZVS of outer IGBTs: maximal input voltage (a), minimal input voltage (b)

3.3.10 Generalizations

The most sensitive part of the converter against EMI is the control system. Hence, special attention to the PCB design must be paid. General guideline and recommendations are presented in chapter 3.3.2.

High voltage and high power applications must be well protected against possible errors. Not only external factors like overvoltage, overload, undervoltage, etc. but also against software and controller errors. This can be achieved by implementing two-level protection system. The most of the threats are handled within software while special hardware circuits provide protection against software errors (chapter 3.3.5).

Due to soft switching effects switching losses can be reduced in three-level HB topology. The practical tests (chapter 3.3.9) showed the same results as the simulations (chapter 2.3.1). In general ZVS for one pair of switches is always possible, no matter what modulation method is used. In order to achieve ZVS for all IGBTs the leakage inductance should be increased and dead time of corresponding IGBTs decreased. However, this cannot be done without a deeper analysis of the resulting effects and risks on the IGBTs. One should also take into account that increased leakage inductance reduces the efficiency of the transformer and the dead time can only be reduced until to a certain limit to sustain sufficient protection of the converter. Although there is no difference between PWM and PSM considering switching losses, PWM has still one advantage especially for HP and HV applications. The omitted flying capacitor decreases overall weight, and costs of the converter, thus PWM is recommended modulation method also for the FEC based on the three-level HB.

Comparing two-level and three-level HB topologies on the basis of practical results, the advantages of the three-level topology become clear. Transistors with smaller blocking voltage capability allow the switching frequency to be

increased at least twice (2 kHz). Taking also soft switching effects into account the frequency could be increased up to four times (4 kHz). However, currently ZVS only for one pair of switches was achieved, which leads to the logical assumption that if ZVS for all switches will be achieved then the switching losses will be reduced even more. The detailed analysis and evaluation of switching losses of the FEC for traction applications will be published in the doctoral work of T. Jalakas.

4. FUTURE RESEARCH AND DEVELOPMENT

The current thesis was concentrated on the control system development for a special purpose DC/DC converter for traction applications. The next challenge for the author is to use the acquired knowledge and experience in the field of renewable energy power converters. In general, the problem statement remains unchanged: control system and algorithm development for special purpose DC/DC converters. However, instead of a high voltage DC/DC converter, the new control object is a low voltage step-up DC/DC converter based on the full-bridge topology. The full-bridge topology combined with a special input filter (impedance or Z-source network) results in a totally new converter concept that is called quasi-Z-source-based isolated DC/DC converter. The most critical part of the new converter is the control system. The efficiency and overall performance depend directly on the chosen control algorithm. The modulation method in general is of higher complexity than the PWM used for traditional full-bridge converters. The new converter concept is suitable for many renewable power sources due to its high boost factor, efficiency and compact design. The quasi-Z-source inverter with a continuous input current on the primary side makes it especially suitable for fuel cells.

A fuel cell (FC) is potentially the most efficient modern approach to distributed power generation. The efficiency of the conversion, i.e., the ratio of the electrical output to the heat content of the fuel, could be as high as 65-70% [136]. In fact, its electrical efficiency could be greater than 70% in theory. Current technologies have only been capable of reaching efficiencies of around 45%. Combined cycles are intended to raise electrical efficiency up to 60% for plants based on high temperature cells [137].

To interconnect a low DC voltage producing fuel cell (typically, 40...80 V DC) to the residential loads (typically, 230 V AC single phase or 3x400 V AC), a special voltage matching converter with large voltage boost factor is required. A typical structure of the two-stage interface converter is presented in Fig. 4.1.

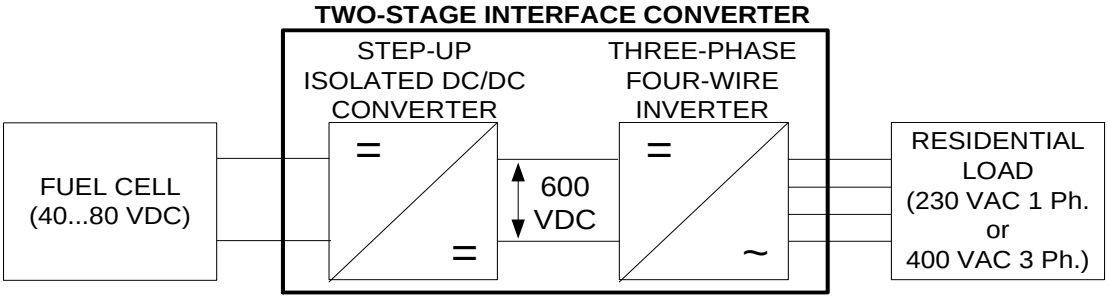


Fig. 4.1 Typical structure of the interface converter for the residential fuel cell powered systems

Due to safety and dynamic performance requirements, the interface converter should be realized within the DC/DC/AC concept. This means that low voltage

from the fuel cell first passes through the front-end step-up DC/DC converter with the galvanic isolation; subsequently the output DC voltage is inverted in the three-phase inverter and filtered to comply with the imposed standards and requirements (second DC/AC stage).

The design of the front-end isolated DC/DC converter is most challenging because this stage is the main contributor of an interface converter efficiency, weight and overall dimensions. The low-voltage provided by the fuel cell is always associated with the high currents in the primary part of the DC/DC converter (switching transistors and primary winding of the isolation transformer). These high currents lead to high conduction and switching losses in the semiconductors, and therefore reduce the efficiency. Moreover, the large voltage boost factor requirement presents a unique challenge to the DC/DC converter design [137]. This specific requirement could be fulfilled in different ways: by use of an auxiliary boost converter before the isolated DC/DC converter [138]- [141]or by use of an isolation transformer with a large turns ratio [142]- [144] for effective voltage step-up.

In this thesis a new approach to the step-up DC/DC converters with high voltage gain is presented. The topology proposed (Fig. 4.2) utilizes the voltage-fed quasi-Z-source inverter (qZSI) with a continuous input current on the converter input side, a high-frequency step-up isolation transformer and a voltage doubler rectifier (VDR). As compared to traditional topologies [138]-[144], the proposed converter has the following key features:

- the qZSI implemented on the primary side of the converter could provide both the voltage boost and buck functions with no additional switches, merely by use of a special control algorithm;
- the qZSI has an excellent immunity against the cross conduction of top- and bottom-side inverter switches. The qZSI implemented can boost the input voltage by introducing a shoot-through operation mode, which is forbidden in traditional voltage source inverters;
- the qZSI implemented has the continuous input current (input current never drops to zero) during the shoot-through operating mode;
- the high-frequency step-up isolation transformer provides the required voltage gain as well as input-output galvanic isolation demanded in several applications;
- voltage doubler rectifier implemented on the converter secondary side has improved rectification efficiency due to reduced voltage drop (twice reduced number of rectifying diodes and full elimination of the smoothing inductor);
- in contrast to the converter with full-bridge rectifiers, the turns number of the secondary winding of the isolation transformer could be reduced by 62% for the same operating conditions due to the voltage doubling effect available with the VDR.

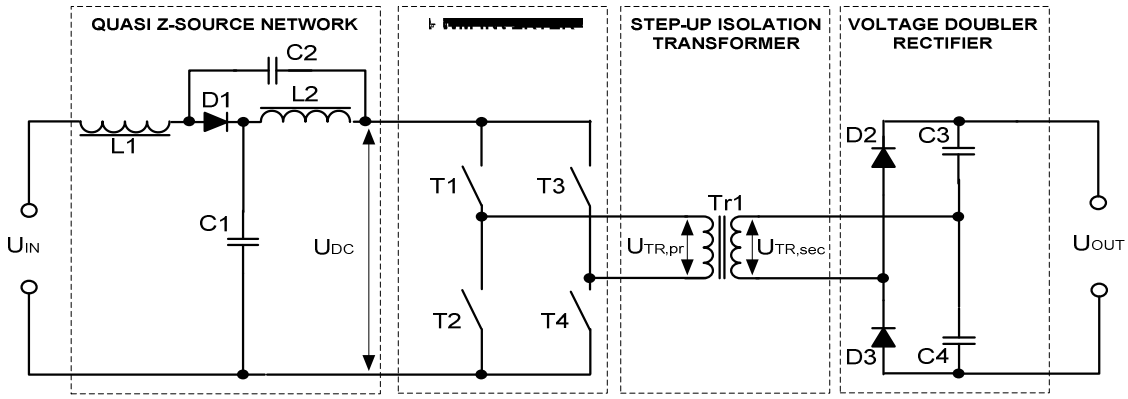


Fig. 4.2 Simplified power circuit diagram of the quasi-Z-source based isolated DC/DC converter

The voltage-fed qZSI with a continuous input current implemented on the converter input side (Fig. 4.2) has a unique feature: it can boost the input voltage by introducing special shoot-through switching states, which is the simultaneous conduction (cross conduction) of both switches of the same phase leg of the inverter. This switching state is forbidden for the traditional voltage source converters (VSI) because of the short circuit of the dc link capacitors. In the discussed qZSI, the shoot-through states are used to boost the magnetic energy stored on the dc side inductors without short-circuiting the dc capacitors. This increase in inductive energy, in turn, provides voltage boost seen on the transformer primary winding during the traditional operating states of the inverter. Thus, the varying input voltage is first preregulated by adjusting the shoot-through duty cycle. Afterwards the isolation transformer is being supplied with a voltage having constant amplitude.

If the input voltage is sufficiently high, the shoot-through mode is eliminated and the converter starts to operate as a traditional VSI. Although the control principle of the qZSI is more complicated than the traditional VSI, it provides a potentially cheaper and more reliable and efficient approach to step-up conversion techniques.

The voltage-fed qZSI with a continuous input current was first reported in [146] as a modification of a currently popular voltage-fed Z-source inverter (ZSI) [147]. The conventional ZSI suffers from a significant drawback of discontinuous input current during the boost conversion mode. In contrast to the traditional ZSI topology, the discussed qZSI shown in Fig. 4.2 features a continuous input current as well as lower operating voltage of the capacitor C2.

4.1 Shoot-Through Control Methods

Two shoot-through control methods for the qZSI based DC/DC converter are proposed (Fig. 4.3): pulse width modulation (PWM) control and phase shift modulation (PSM) control. In both cases shoot-through is generated during zero states. The shoot-through states are evenly spread over the switching period so that the number of higher harmonics in the transformer primary could be

reduced. In order to reduce switching losses of the transistors, the number of shoot-through states per period was limited by two. Moreover, to decrease the conduction losses of the transistors, the shoot-through current is distributed between both inverter legs.

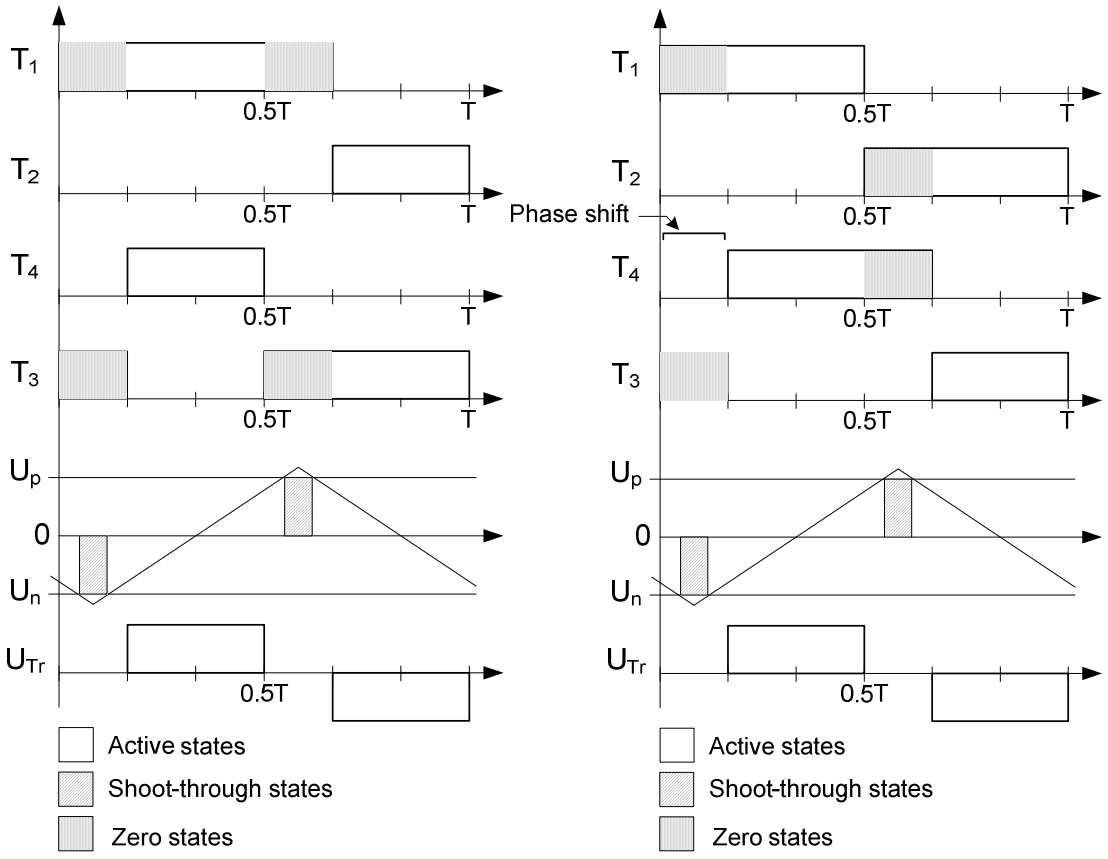


Fig. 4.3 Shoot-through modulation methods: PWM method (a), PSM method (b)

The shoot-through states are created during the zero states of the full-bridge inverter. To provide a sufficient regulation margin, the zero state time t_Z should always exceed the maximum duration of the shoot-through states per one switching period. In general, each operating period of the qZSI during the shoot-through mode always consists of an active state t_A, shoot-through state t_S and zero state t_Z:

$$T = t_A + t_S + t_Z . \tag{37}$$

4.1.1 PWM Control with Shoot-Through During Zero States

Fig. 4.3 (a) presents the PWM control of the single-phase qZSI where shoot-through is generated during zero states. Zero states are the states when the primary winding of the isolation transformer is shorted through either the top (T1 and T3) or bottom (T2 and T4) inverter switches. In order to generate the shoot-through states, two compare values (U_p and U_n) were introduced (Fig. 4.3

(a)). If the triangle waveform is greater than U_p or lower than U_n, the inverter switches turn into the shoot-through state. During this operating mode the current through inverter switches reaches its maximum. The voltage across the inverter bridge (U_{DC}) during shoot-through states drops to zero; the resulting primary winding voltage waveform (U_{Tr}) of the isolation transformer is indicated in Fig. 4.3 (a)

The block-diagram of the gating signal generation principle for the PWM control method is shown in Fig. 4.4. The transistors are controlled by the separate signals. During zero states only top transistors (T1 and T3) are turned on while in the case of shoot-through both inverter legs are conducting.

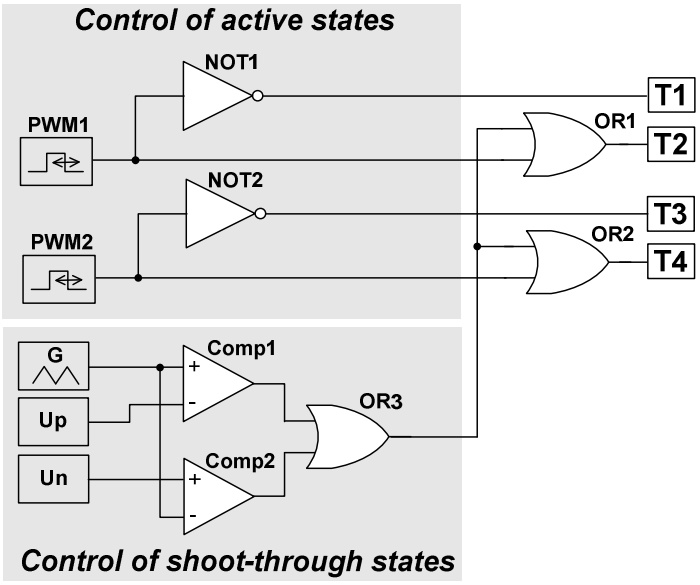


Fig. 4.4 Generalized block diagram of a gating signal generator for PWM

Regarding to this methodology, the switching states sequence is shown in Table 15. The states are shown for one operating period of the isolation transformer. As it can be seen, the transistors work with different switching frequencies, thus have unequal switching losses. T1 and T3 are working with the frequency of the isolation transformer, while T2 and T4 have three time higher operating frequency. The resulting gate signals are shown in Fig. 4.5.

Table 15 PWM switching states sequence per one period

	T1	T2	T3	T4
zero state	1	0	1	0
shoot-through	**1**	**1**	**1**	**1**
zero state	1	0	1	0
active state	1	0	0	1
zero state	1	0	1	0
shoot-through	**1**	**1**	**1**	**1**
zero state	1	0	1	0
active state	0	1	1	0

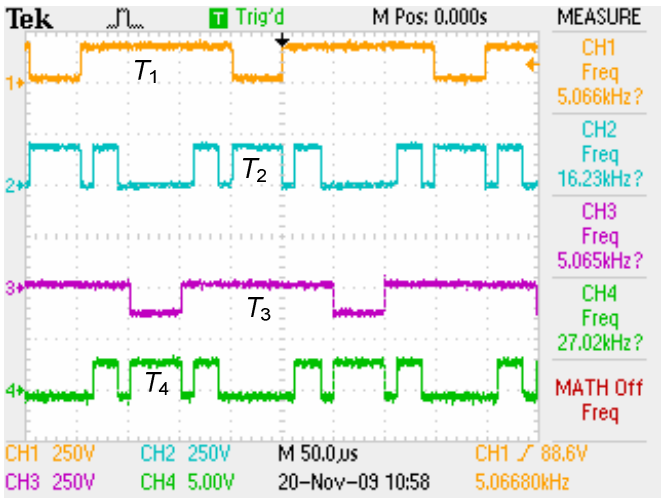


Fig. 4.5 Gate signals of the transistors in PWM control

4.1.2 PSM Control with Shoot-Through During Zero States

An alternative to PWM control is the PSM control where the active states are controlled with phase shift between signals. Duty cycle is kept constant (nearly 0.5) and only the phase is shifted, as shown in Fig. 4.3 (b). Unlike in the PWM control where zero states were always generated by the same pair of transistors (T1/T3 or T2/T4), here the pairs are alternating over each period. As a result, the transistors are equally loaded. The shoot-through states are created similarly to PWM control.

The block-diagram of the gating signal generation principle for the PSM control method is shown in Fig. 4.6. The transistors are controlled by separate signals. During zero alternatively top and bottom transistor pairs (T1/T3 or T2/T4) are turned on. In the case of shoot-through both inverter legs are conducting.

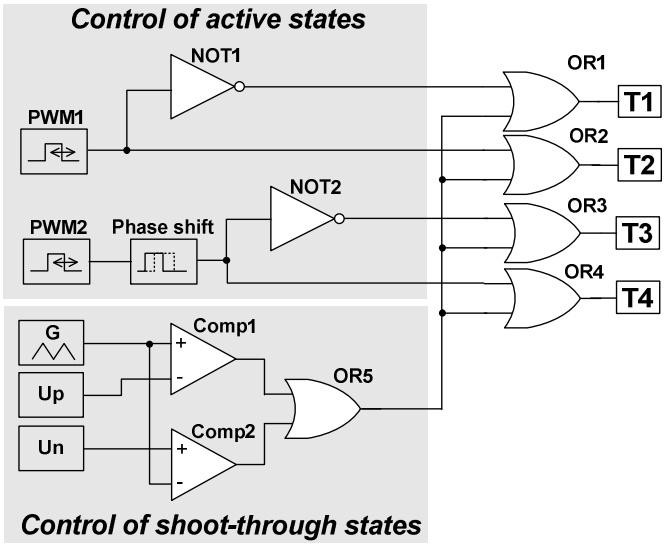


Fig. 4.6 Generalized block diagram of a gating signal generator for PSM

The switching states sequence of the transistors in Table 16 reveals the differences in the comparison with the PWM method. All transistors work with the same frequency, which is twice the transformer operating frequency. Thus, the transistors have also balanced switching losses. The resulting gate signals are shown in Fig. 4.7

Table 16 PSM switching states sequence per one period

	T1	T2	T3	T4
zero state	1	0	1	0
shoot-through	**1**	**1**	**1**	**1**
zero state	1	0	1	0
active state	1	0	0	1
zero state	0	1	0	1
shoot-through	**1**	**1**	**1**	**1**
zero state	0	1	0	1
active state	0	1	1	0

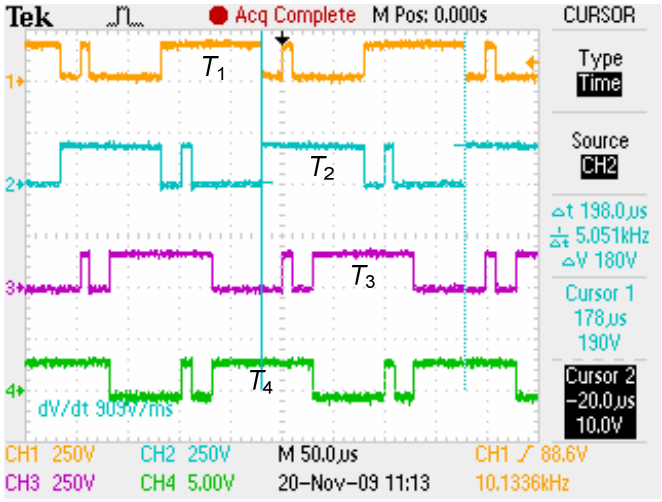


Fig. 4.7 Gate signals of the transistors in PSM control

4.2 Generalizations and Future Research

Generally, the qZSI based isolated DC/DC converters are very prospective and advantageous energy conversion technologies, suitable for applications with wide input voltage range and where the isolation between input and output is required. To optimize efficiency and flexibility of these converters main research efforts should be concentrated on control methods. The proposed shoot-through generation method during zero states seems to be a good control method for many applications due to its flexibility and reduced number of harmonics in the transformer primary voltage. Currently main efforts are focused on:

- the optimization of switching strategies of power transistors;
- parameter measurement accuracy in high EMI environment;
- development of fast protection and diagnostic algorithms;
- development of converter control algorithms with special attention to operation conditions and service life of the fuel cell.

Thus, it is a perspective topic for the postdoctoral studies of the author. The results will be reported in the scientific papers and future doctoral theses of the Department of Electrical Drives and Power Electronics.

CONCLUSIONS

In the current doctoral work digital control systems and algorithms for high power (P>20 kW) and high voltage (U>2 kV) isolated DC/DC converters were studied and analyzed. That knowledge was used to design and assemble a flexible control system for a novel front-end converter to be used in traction applications. Since the developed control system has been built and optimized according to the most recent development trends and design requirements of power electronics together with novel design proposals from the author, the doctoral work has a great practical value for the industry.

In general, the doctoral work has following results:

1. based on the valuable information that was gathered from the analysis of recent technologies and development trends, a state of the art control system with advanced protection functions was built and tested;
2. systematization and comparison of conventional control algorithms for DC/DC converters allowed to select suitable algorithms for the FEC based on half-bridge topology. The resulting classification (Fig. 1.14) served as a basis for the further work;
3. two- and three-level HB topologies were analyzed and tested. It was stated that two-level HB topology should be used when the main emphases lies on robustness and simplicity. In case if lower switching losses and systems costs are desired the three-level topology should be considered;
4. capacitor-related volt-second unbalance problem, which is well known and typical problem for low power (P=0…500 W) HB converters, was analyzed and researched. It was stated that the problem is not depending on the input capacitors. Mostly the problem lies in the unsymmetrical control pulses. A new control algorithm (improved digital peak current mode control, page 61) was proposed by the author to solve the problem;
5. during the analytical part of the thesis computer models of the converter with corresponding control algorithms were developed. The models were improved later during practical tests, thus they create an excellent basis for further development and research;
6. optimal control algorithm for the FEC to stabilize output voltage was found based on simulations and practical test results;
7. general design guidelines and recommendations including EMC aspects, PCB design guidelines, recommendations for sensors and control unit selection etc. were elaborated;
8. using the proposed control signal multiplication concept a flexible and optimized control system could be designed, which can be used for both

two- or three-level HB topology without any changes either in the hardware nor in the software;

The current doctoral work involved both theoretical and practical investigations. The control system was built in accordance with all user requirements and corresponding norms. Recent technologies and components were combined with several improvements proposed by the author. As a result, a flexible, multifunctional and novel control system for the FEC for traction applications was designed. Novelty and profitability of the work have been confirmed by the registered Estonian utility model certificates (EE00824U1 and EE00687U1).

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ABSTRACT

This thesis is devoted to design and development of a state of the art control system for a half-bridge (HB) isolated DC/DC converter. The HB topology is first examined as a candidate topology for the front-end converter (FEC) of the rolling stock auxiliary power supply (APS). The new converter topology improves power density and reliability of the FEC, reduces component number and system volume.

In order to define exact tasks of the control system, user requirements and railway norms are specified. To meet the demanding railway conditions and provide effective and reliable operation of the FEC, the recent trends and technologies of analogues applications were studied in detail.

In the analytical part of the thesis general requirements, topology and working conditions of the FEC are specified. First, different modulation methods and soft switching techniques are analyzed, compared and simulated. It is shown which of the methods are suitable and an optimal solution for the FEC is selected. Based on the selected modulation method (pulse width or phase shift modulation) corresponding control algorithms are analyzed. Also, several new algorithms have been developed by the author of the thesis to solve some control issues typical of a digitally controlled HB. In order to find out the best and optimal algorithms for the current converter, the complete system is simulated and its stability is estimated. The analytical results are verified in the practical part of the thesis.

As a practical output of the thesis, an advanced control system for FEC for traction applications was developed and tested. The assembly, components and functions of the control system are described in detail. The control system was designed so that it is applicable for two- or three-level HB topology without any changes. As a logical enhancement of the two-level HB, the three-level HB topology with 3.3 kV IGBTs is proposed and also implemented in the current doctoral project. Practical recommendations and general guidelines to design such HP and HV isolated DC/DC converter for traction applications are given. Finally, test and simulation results are compared and analyzed.

In the fourth part of the thesis, postdoctoral research topics of the author are covered. The future research and development involves the field of renewable power converters. Two control methods for the quasi-Z-source-based isolated DC/DC converter are studied and explained.

Novelty and profitability of the work have been confirmed by the registered Estonian Utility Model certificates (EE00824U1 and EE00687U1).

KOKKUVÕTE

Doktoritöö eesmärgiks oli uurida ning välja töötada arukas juhtimissüsteem rööbastranspordi abitoitemuunduri sisendastmele. Kõrgete pingete (U>2 kV) ja suurtele võimsuste (P>20 kW) tõttu on antud valdkonnas senini olnud suureks probleemiks pooljuhtkomponentide suhteliselt madal pingetaluvus. Doktoritöös rakendatakse uudseid kõrgepingelisi IGBTsid, tänu millele oli võimalik kasutada lihtsa struktuuriga poolsildtopoloogiat. Väljapakutud muunduri topoloogia võimaldab suurendada muunduri energiatihedust, kasutegurit ning töökindlust.

Ülesande lahendamiseks uuriti ning klassifitseeriti antud valdkonna tehnilised nõuded ja kasutaja soovid. Juhtimissüsteemi ehitamisel lähtuti teaduse ja tehnoloogia viimase aja trendidest, et tagada muunduri efektiivne töö ning kõrge kasutegur.

Töö analüütilises osas kirjeldatakse muunduri topoloogiat, töövahemikku ning tehnilisi parameetreid. Esmalt uuritakse topoloogiale sobivaid modulatsioonimeetodeid ja pehme lülituse võimalusi. Analüüsi ja simulatsiooni tulemuste põhjal leitakse optimaalseim modulatsiooni meetod (pulsilaius või faasinihke modulatsioon), millest lähtudes uuritakse sobivaid juhtimisalgoritme. Käsitletakse ka autori poolt loodud täiesti uusi algoritme, mis lahendavad mitu digitaalselt juhitud poolsildtopoloogiale omast tüüpprobleemi. Optimaalseim juhtimisalgoritm selgitatakse välja süsteemi kui terviku simuleerimise ja stabiilsuse uurimise läbi. Simuleerimistulemused kontrollitakse katseliselt töö praktilises osas.

Doktoritöö praktilise tulemusena töötati välja ning katsetati arukas juhtimissüsteem rööbastranspordi abitoitemuunduritele, mis vastab kaasaegsetele nõuetele ja normidele. Juhtimissüsteemi paindlikkust tõestab asjaolu, et teda on võimalik rakendada nii kahe- kui ka kolmetasandilise poolsildtopoloogiaga muundurile ilma lisakomponentideta. Mõlemat topoloogiat on töös ka käsitletud. Lisaks kirjeldatakse töö praktilises osas põhjalikult juhtimissüsteemi ehitust, tema komponente ning funktsioone. Peatükis antud praktilised nõuanded ja soovitused analoogse juhtimissüsteemi ehitamiseks lisavad tööle praktilist väärtust.

Töö tulemustele on Eestis välja antud kaks kasuliku mudeli tunnistust (EE00824U1 ja EE00687U1), mis tõestavad tehtud töö uudsust ja vajalikkust.

AUTHOR'S MAIN PUBLICATIONS

1. Vinnikov, D.; Roasto, I.; Jalakas, T. (2009). Design and Development of 3.3 kV IGBT Based Three-Level DC/DC Converter. Scientific Journal Electrical Engineering Research Report, pp. 1 - 6.
2. Vinnikov, D.; Jalakas, T.; Roasto, I. (2009). Analysis and Design of 3.3 kV IGBT Based Three-Level DC/DC Converter with High-Frequency Isolation and Current Doubler Rectifier. Power and Electrical Engineering. Scientific Journal of Riga Technical University, pp. 97 - 102.
3. Vinnikov, D.; Roasto, I.; Jalakas, T. (2009). An Improved High-Power DC/DC Converter for Distributed Power Generation , 10th International Conference on "Electrical Power Quality and Utilisation", September 15-17, 2009, Lodz, Poland, pp. 1 - 6.
4. Roasto, I.; Vinnikov, D. (2009). Simplified Digital Average Current Mode Control Algorithm for Half- or Full-Bridge Isolated DC/DC Converters, 35th Annual Conference of the IEEE Industrial Electronics Society, Alfândega Congress Center, Porto, Portugal, 3-5 November 2009. pp. 1744 - 1749.
5. Vinnikov, D.; Roasto, I.; Jalakas, T. (2009). New Step-Up DC/DC Converter with High-Frequency Isolation . In: Proceedings of: 35th Annual Conference of the IEEE Industrial Electronics Society, Alfândega Congress Center, Porto, Portugal, 3-5 November 2009, pp. 667 - 672.
6. Vinnikov, D.; Hõimoja, H.; Andrijanovitš, A.; Roasto, I.; Lehtla, T.; Klytta, M. (2009). An Improved Interface Converter for a Medium-Power Wind-Hydrogen System. In: Proceedings of 2nd IEEE International Conference on Clean Electrical Power: Renewable Energy Resources Impact (ICCEP'2009). June 9-11, 2009, Capri, Italy: IEEE Publishing, pp. 426 - 432.
7. Roasto, I.; Vinnikov, D.; Galkin, I. (2009). Comparison of Control Methods for High-Voltage High-Power Three-Level Half-Bridge DC/DC Converters. In: Proceedings of: 6th IEEE Conference-Workshop "Compatibility and Power Electronics CPE'2009". 20.05.-22.05.2009, Badajoz, Spain. 2009, pp. 258 - 264.
8. Vinnikov, D.; Jalakas, T.; Roasto, I. (2009). Analysis of Implementation Possibilities and Benefits of Three-Level Half-Bridge NPC Topology in Static Auxiliary Converters for Rolling Stock. Proceedings of Second International Conference on Power Engineering, Energy and Electrical Drives, POWERENG; Lisbon, Portugal, March 18-20, 2009. pp. 587 - 592.

9. Roasto, I.; Vinnikov, D.; Vodovozov, V. (2009). Simulation and Evaluation of Control Methods for the Rolling Stock Static Auxiliary Converter Based on Three-Level NPC Inverter Topology. In: Conference proceedings of IEEE Second International Conference on Power Engineering, Energy and Electrical Drives, POWERENG; Lisbon, Portugal, March 18-20, 2009, pp. 593 - 598.

10. Jalakas, T.; Vinnikov, D.; Roasto, I. (2009). Design and Development of Three-Level Half-Bridge NPC Converter with Dual 3.3 kV IGBT Modules. In: 6th International Symposium "Topical Problems in the Field of Electrical and Power Engineering", Doctoral School of Energy and Geotechnology. Kuressaare, Estonia, Tallinn 12-17 Jan. 2009, pp. 43 - 48.

11. Roasto, I.; Vinnikov, D.; Lehtla, T. (2009). State of the Art and Development Trends of Smart Control Systems for High-Voltage DC/DC Converters. In: 6th International Symposium "Topical Problems in the Field of Electrical and Power Engineering", Doctoral School of Energy and Geotechnology. Kuressaare, Estonia, 12-17 Jan. 2009 pp. 36 - 42.

12. Vinnikov, D.; Roasto, I.; Vodovozov, V. (2009). Design Issues of Redundant Protection and Supervision System for the Special Purpose Power Converters . In: Proceedings of: International Conference on Renewable Energy and Power Quality (ICREPQ´09), April 15-17, 2009, Valencia, Spain. pp. 2009, 1 - 6.

13. Vinnikov, D.; Roasto, I.; Jalakas, T. (2009). Selection of the Duty Cycle Variation Range and Its Influence on the Efficiency and Operability of High-Power Converters Operating at Wide Input Voltage Swing. R. Lahtmets (Toim.). 7th International Symposium "Topical Problems in the Field of Electrical and Power Engineering", Doctoral School of Energy and Geotechnology. Narva-Jõesuu, Estonia, 16-19 Jun. 2009.

14. Vinnikov, D.; Jalakas, T.; Roasto, I. (2009). A New High-Power DC/DC Converter for Residential Fuel Cell Power Systems. In: Proceedings of: 11th Spanish-Portuguese Congress on Electrical Engineering (11CHLIE), July 1-4, 2009, Zaragoza, Spain, 2009, pp. 1 - 6.

15. Roasto, I.; Vinnikov, D.; Lehtla, T.; Auväärt, A. (2008). A Simplified Peak Current Mode Control Algorithm for Special Purpose High Voltage IGBT Converters. In: BEC 2008 : 2008 International Biennial Baltic Electronics Conference : Proceedings: 11th Biennial Baltic Electronics Conference, Tallinn University of Technology, 6-8 Oct. 2008, pp 305 - 308.

16. Jalakas, T.; Vinnikov, D.; Roasto, I.; Raud, Z.; Egorov, M. (2008). Versatile Laboratory Tools for Advanced Course of Power Electronics.

In: BEC 2008 : 2008 International Biennial Baltic Electronics Conference : Proceedings: 11th Biennial Baltic Electronics Conference, Tallinn University of Technology, 6-8 Oct. 2008, pp. 277 - 280.

17. Vinnikov, D.; Roasto, I.; Lehtla, T. (2008). Fault Detection and Protection System for the Power Converters with High-Voltage IGBTs. In: Proceedings of 15th IEEE International Conference on Electronics, Circuits and Systems ICECS 2008, August 31 – September 3, 2008, Malta, pp. 922 - 925.

18. Roasto, I.; Vinnikov, D.; Lehtla, T. (2008). Laboratory Setup for Studying Ultracapacitors in Industrial Applications. In: Proceedings of 13th International Power Electronics and Motion Control Conference EPE-PEMC 2008, 13th International Power Electronics and Motion Control Conference EPE-PEMC, 1-3 Sept. 2008, Poznan, Poland, pp. 2034 - 2037.

19. Roasto, I.; Vinnikov, D.; Lehtla, T. (2008). Analysis of Capacitor-Related Mid-Voltage Point Shift Problems in High-Voltage Half-Bridge DC/DC Converters. In: Proceedings of 2008 IEEE 39th Annual Power Electronics Specialists Conference PESC 2008, June 15-19, 2008. Greece, pp. 3619 - 3622.

20. Roasto, I.; Vinnikov, D.; Lehtla, T. (2008). Ultracapacitors as an Innovative Teaching Topic in Tallinn University of Technology. International Symposium on Power Electronics, Electrical Drives, Automation and Motion SPEEDAM 2008, June 11-13, 2008, Ischia, Italy, pp. 475 - 480.

21. Roasto, I.; Vinnikov, D.; Lehtla, T. (2008). Comparison of Different Microcontroller Development Boards for Power Electronics Applications. 5th International Symposium "Topical problems in the field of electrical and power engineering" doctoral school of energy and geotechnology, Kuressaare, Estonia, January 14-19, 2008 pp. 103 - 107.

22. Roasto, I.; Vinnikov, D.; Vodovozov, V. (2008). Development and Verification of Control and Protection Algorithms for the Special Purpose High Power Converters. In: Proceedings of the 3rd International Workshop: Intelligent Technologies in Logistics and Mechatronics Systems ITELMS'2008, Panevezys, Lithuania., May 22-23, 2008, pp. 23 - 27.

23. Roasto, I.; Vinnikov, D.; Klytta, M. (2007). EMC Considerations on PCB Design for a High-Power Converter Control System. In: 5th International Conference-Workshop on Compatibility in Power Electronics CPE'2007: 5th International Conference-Workshop on Compatibility in Power Electronics CPE'2007, May 29 - June 1, 2007, Gdańsk, Poland, 2007, 4 Pages.

24. Roasto, I., Vinnikov, D. (2007). Control System Simulation of a 40 kW Half-Bridge Isolated DC-DC Converter. In 12th European Conference on Power Electronics and Applications, EPE'2007. Sept. 2 - 5, 2007, Aalborg (Denmark), 2007.

25. Roasto, I.; Vinnikov, D.; Klytta, M. (2007). Control and Protection of a High-Voltage IGBT-Based Half-Bridge Inverter. Scientific proceedings of Riga Technical University. Power and Electrical Engineering, Riga, Latvia, pp. 75 - 83

26. Roasto, I.; Vinnikov, D. (2007). Control Methodology of the Rolling Stock Auxiliary Power Supply. 4th International Symposium "Topical problems of education in the field of electrical and power engineering". Doctoral school of energy and geotechnology, Kuressaare, Estonia, January 15-20, 2007, pp. 122 - 125.

27. Jalakas, T.; Roasto, I.; Müür, M.; Vinnikov, D.; Laugis, J. (2007). Research and Development of Voltage Converters Based on 6.5 kV IGBTs. In: International Youth Conference on Energetics IYCE-2007, 31.05.-02.06.2007, Budapest, Hungary, pp. 153 - 154.

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29. Roasto, I.; Lehtla, T. Rosin, A. (2006). Control Strategies of Ultracapacitors. In: 3rd International Symposium "Topical problems of education in the field of electrical and power engineering": doctoral school of energy and geotechnology : Kuressaare, Estonia, January 16-21, 2006 pp. 85 - 88.

30. Jalakas, T.; Möller, T.; Roasto, I. (2006). PIC microcontroller learning system. In: 3rd International Symposium "Topical problems of education in the field of electrical and power engineering": doctoral school of energy and geotechnology, 16-21 Jan. 2006 Kuressaare, Estonia, pp. 99 - 101.

31. Roasto, Indrek (2006). Programmeeritavad loogikaelemendid. Elektriala 1, pp. 24 - 26.

32. Roasto, I. (2005). Ultrakondensatoren– Energiespeicher für Schienenfahrzeuge. 2nd International Symposium "Topical Problems of Education in the Field of Electrical and Power Engineering", 17-22 Jan. 2005, Kuressaare, Estonia, pp. 119 - 122.

LISA 1 / ANNEX 1

Intellectual Properties

1. Registered Estonian Utility Model Certificate “Rolling stock HV APS”; Estonian Patent Office, reg. nr. EE00687U1. Applicant: Tallinn University of Technology. Authors: D. Vinnikov, J. Laugis, T. Jalakas, I. Roasto, J. Matvejev, S. Frolov, N. Samsonov. Date of issue: 15.10.2007.

EESTI VABARIIK

KASULIKU MUDELI TUNNISTUS

NR 00687

TUNNISTUS ON VÄLJA ANTUD KASULIKU MUDELI SEADUSE § 32 JÄRGI.

TUNNISTUS TÕENDAB REGISTREERINGUT JA KASULIKU MUDELI OMANIKU AINUÕIGUST KASULIKU MUDELI KIRJELDUSES TOODUD LEIUTISELE. REGISTREERING KEHTIB NELI AASTAT REGISTREERIMISTAOTLUSE ESITAMISE KUUPÄEVAST ARVATES. REGISTREERINGU KEHTIVUST VÕIB PIKENDADA RIIGILÕIVU TASUMISEL ESMALT NELJAKS JA HILJEM VEEL KAHEKS AASTAKS.

PATENDIAMET

PEADIREKTOR

TALLINNAS 16. [illegible] 2007

EE 00687 U1

(19) EESTI VABARIIK
PATENDIAMET

(11) EE 00687 U1

(51) Int.Cl.
B60L 9/30 (2007.01)
H02M 5/42 (2007.01)

(12) KASULIKU MUDELI KIRJELDUS

(21) Registreerimistaotluse number: **U200700077**

(22) Registreerimistaotluse esitamise kuupäev: **25.06.2007**

(24) Registreeringu kehtivuse alguse kuupäev: **25.06.2007**

(45) Kasuliku mudeli kirjelduse avaldamise kuupäev: **15.10.2007**

(73) Kasuliku mudeli omanikud:

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Sergei Frolov
Koidu 122-43, 10139 Tallinn, EE
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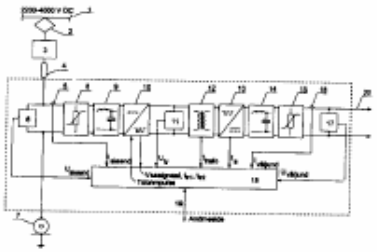
Narva mnt 17-8, 10120 Tallinn, EE

(74) Ühine esindaja:

Tallinna Tehnikaülikool

(54) Rööbastranspordi kõrgepingeline abitoiteallikas

(57) Uutel IGBT (6,5 kV) transistoridel põhinev staatiline abitoiteallikas elektritranspordi rakendustele, mis on ette nähtud alalisvoolu kontaktliini toitega elektrisõiduki, näiteks elektrirongi abiseadmete toiteks. Abitoiteallikas sisaldab sisendfiltrit (9), täis- või poolsillana realiseeritud sisendvaheldit (10), eraldustransformaatorit (12) ning kiiretoimeliste dioodidega väljundaladit (13) koos LC-tüüpi väljundfiltriga (14). Abitoiteallika väljundpinged on sisendpingest galvaaniliselt isoleeritud kõrgsageduseraldustransformaatoriga (12).



2. Registered Estonian Utility Model Certificate “Rolling stock HV APS with improved power density”; Estonian Patent Office, reg. nr. EE00824U1. Applicant: Tallinn University of Technology. Authors: D. Vinnikov, T. Jalakas, I. Roasto, J. Laugis. Date of issue: 15.04.2009.

EESTI VABARIIK

KASULIKU MUDELI TUNNISTUS

NR 00824

TUNNISTUS ON VÄLJA ANTUD KASULIKU MUDELI SEADUSE § 32 JÄRGI.

TUNNISTUS TÕENDAB REGISTREERINGUT JA KASULIKU MUDELI OMANIKU AINUÕIGUST KASULIKU MUDELI KIRJELDUSES TOODUD LEIUTISELE. REGISTREERING KEHTIB NELI AASTAT REGISTREERIMISTAOTLUSE ESITAMISE KUUPÄEVAST ARVATES. REGISTREERINGU KEHTIVUST VÕIB PIKENDADA RIIGILÕIVU TASUMISEL ESMALT NELJAKS JA HILJEM VEEL KAHEKS AASTAKS.

PATENDIAMET

PEADIREKTOR

TALLINNAS 15. -4- 2009

EE 00824 U1

(19) EESTI VABARIIK
PATENDIAMET

(11) EE 00824 U1

(51) Int.Cl.
H02M 5/42 (2009.01)
B60L 9/28 (2009.01)

(12) KASULIKU MUDELI KIRJELDUS

(21) Registreerimistaotluse number: **U200800134**

(22) Registreerimistaotluse esitamise kuupäev: **16.12.2008**

(24) Registreeringu kehtivuse alguse kuupäev: **16.12.2008**

(45) Kasuliku mudeli kirjelduse avaldamise kuupäev: **15.04.2009**

(73) Kasuliku mudeli omanik:

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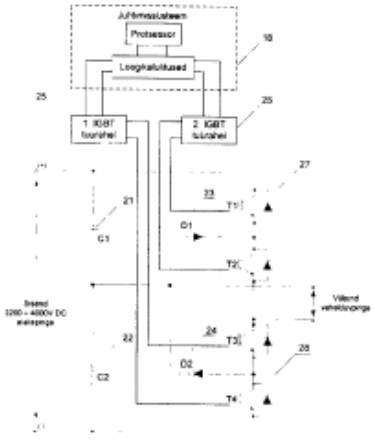
Indrek Roasto
Ehitajate tee 5, 19086 Tallinn, EE

Juhan Laugis
Ehitajate tee 5, 19086 Tallinn, EE

(54) Rööbastranspordi kõrgepingeline suure võimsustihedusega staatiline abitoitemuundur

(57) Leiutis käsitleb 3,3 kV IGBT-del põhinevat kõrgepingelist staatilist suure võimsustihedusega abitoitemuundurit rööbastranspordi rakendustele, mis on ette nähtud alalisvoolu kontaktliini toitega elektrisõiduki, näiteks elektrirongi abiseadmete toiteks. Abitoitemuundur sisaldab sisendfiltrit, poolsillana realiseeritud kolmetasandilise topoloogiaga sisendvaheldit, eraldustransformaatorit ning kiiretoimeliste dioodidega väljundalaldit koos LC filtriga. Väljundalaldi võib olla realiseeritud kas täissildalaldina, voolu kahekordistava topoloogiaga alaldina või kahe paralleelühenduses oleva voolu kahekordistava topoloogiaga alaldina. Abitoitemuunduri väljundpinged on sisendpingest galvaaniliselt isoleeritud eraldustransformaatoriga, millel võib olla üks sekundaarmähis koos selle külge ühendatud sildalaldiga või voolu kahekordistava alaldiga. Eraldustransformaatoril võib olla ka kaks sekundaarmähist, mille külge on ühendatud omavahel paralleelühenduses olevad voolu kahekordistava topoloogiaga alaldid. Ühe eraldustransformaatori asemel võib kasutada kahte jadaühenduses oleva primaarmähisega eraldustransformaatorit.



LISA 2 / ANNEX 2

ELULOOKIRJELDUS

1. Isikuandmed

Ees- ja perekonnanimi: Indrek Roasto
Sünniaeg ja -koht: 02.07.1980, Tallinn
Kodakondsus: Eesti
Perekonnaseis: vallaline
Lapsed: -

2. Kontaktandmed

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3. Hariduskäik

Õppeasutus (nimetus lõpetamise ajal)	**Lõpetamise aeg**	**Haridus (eriala/kraad)**
Tallinna Tehnikaülikool	2005	tehnikateaduste magister
Saksamaa Giessen-Friedbergi rakendusteaduste ülikool (FH)	2005	diplomeeritud insener
Tallinna Tehnikaülikool	2003	tehnikateaduste bakalaureus
Tallinna Kadrioru Saksagümnaasium	1999	keskharidus

4. Keelteoskus (alg-, kesk- või kõrgtase)

Keel	**Tase**
eesti	emakeel
inglise	kesktase
saksa	kõrgtase
vene	algtase

5. Teenistuskäik

Töötamise aeg	**Ülikooli, teadusasutuse või muu organisatsiooni nimetus**	**Ametikoht**
2009	Gdynia Maritime ülikool, Poola	erakorraline teadur
2005 -	Tallinna Tehnikaülikool	teadur

2005	Lust Antriebstechnik GmbH, Saksamaa	insener
2004	Siemens AG Erlangen, Saksamaa	insener
2003 - 2005	Tallinna Tehnikaülikool	insener
2002	Lust Antriebstechnik GmbH, Saksamaa	insener

6. Teadustegevus

2009	BF113 Z-tüüpi sisendvaheldiga ja mitmefaasiline neutraaljuhi väljundiga muunduri katseseade taastuvenergeetika rakendusteks
2008	F7114 Kahesuunalist juhitavat energiavahetust võimaldavad muundurid elektrienergia salvestamiseks
2008-2011	ETF7572 Võimsad kõrgsagedusliku vahelüliga alalispingemuundurid
2008-2010	ETF7425 Kõrgepingeliste IGBT transistoride lülitusomaduste uurimine
2008	BF110 Kõrgepingelistel IGBT transistoridel põhineva kolmetasandilise vaheldi katseseade
2008	SF0140009s08 Säästev ja jätkusuutlik elektroenergeetika
2007-2008	IN7061 Välisõppejõu kutsumine TTÜ elektriajamite ja jõuelektroonika instituuti eesmärgiga välja arendada kaasaegne jõuelektroonika labor
2007	BF-54 Energiasalvestitel ja pooljuhtmuunduritel põhinevate elektritoitesüsteemide uurimine, väljatöötamine ning rakendamine
2006-2007	631F Energiasalvestid ja nende kasutusvõimaluste uurimine Eestis
2006-2007	656F Elektertranspordi pardaseadmete toitemuundurid
2005-2007	ETF6175 Ülikondensaatorsalvestiga elektriajami energiavahetuse uurimine
2005-2006	BF15 Energiasalvestitel põhinevate elektritoitesüsteemide ja ajamite uurimine, väljatöötamine ning rakendamine
2005-2006	AA7 Energeetikamaja energiabilanss
2003-2007	SF0142513s03 Energiamuundus- ja -vahetusprotsesside uurimine elektriajamite ja pooljuhtmuundurite jõuvõrkudes
2003-2004	358L Elektriajamite jõumuundurite katsepartii madalapõhjalise keskosa ja rekonstrueeritud infosüsteemidega trammidele
2002-2004	245F Elektertranspordi veoajamid, automaatika ja infosüsteemid

7. Kaitstud lõputööd

- „Ülikondensaator-energiasalvestit teenindav muundur” (Bakalaureusetöö, 2003)
- „Ülikondensaator-energiasalvesti juhtimismudeli väljatöötamine rööbassõidukile” (magistritöö, 2005)

8. Teadustöö põhisuunad

- Z-tüüpi sisendvaheldiga ja mitmefaasiline neutraaljuhi väljundiga muunduri katseseade taastuvenergeetika rakendusteks

Kuupäev: 2.12.09.

LISA 3 / ANNEX 3

CURRICULUM VITAE

1. Personal information

Name: Indrek Roasto
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Citizenship: Estonian
Marital status: single
Children: no

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3. Education

Institution	Graduation year	Education
Tallinn University of Technology	2005	M.Sc., Electrical Drives and Power Electronics
Germany Giessen-Friedberg University of Applied Science	2005	Dipl. Eng.
Tallinn University of Technology	2003	Bachelor
Germany Gymnasium of Kadriorg	1999	Basic

4. Languages

Language	Level
English	Middle
Estonian	Native
Germany	Excellent
Russian	Basic

5. Professional Employment

Date	Organization	Position
2009	Gdynia Maritime University, Poland	extraordinary researcher
2005 -	Tallinn University of Technology	researcher

2005	Lust Antriebstechnik GmbH, Germany	engineer
2004	Siemens AG Erlangen, Germany	engineer
2003 - 2005	Tallinn University of Technology	engineer
2002	Lust Antriebstechnik GmbH, Germany	engineer

6. Scientific work

2009	BF113 Experimental Setup of Power Conditioning Unit for Fuel Cell Applications Utilizing Z-Source-based Frond-End Converter and 4-Wire Inverter
2008	F7114 Bidirectional interface converters for energy storage
2008-2011	ETF7572 High power DC voltage converters with high frequency transformer link
2008-2010	ETF7425 Research of Dynamic Performance of High-Voltage IGBTs
2008	BF110 Experimental setup of a high-voltage IGBT-based three-level inverter
2008	SF0140009s08 Energy saving and sustainable electrical power engineering
2007	BF-54 Research, development and implementation of electrical supply systems based on energy storage devices and semiconductors
2006-2007	F656 Power converters for onboard equipment of electrical transport
2005-2007	ETF6175 Research of energy change in electrical drive with supercapacitor
2005-2006	BF15 Development and application of electrical supply systems and drives based on energy storage devices
2005-2006	AA7 Energy balance of the building of Power Engineering
2003-2007	SF0142513s03 Energy saving and sustainable electrical power engineering
2003-2004	Pilot series of power converters of electrical drives for trams with low-floor middle part and modernized communication systems
2002-2004	245F Traction drives, automation and information systems

7. Defended theses

- “Energy Interface Converter for Ultracapacitors Bank” (Dipl. Eng, 2003)
- “Development of the Control-Module for the Rail Vehicle Ultracapacitor Energy Storage Device” (M.Sc, 2005)

8. Main areas of scientific work

- Experimental Setup of Power Conditioning Unit for Fuel Cell Applications Utilizing Z-Source-based Frond-End Converter and 4-Wire Inverter

Date: 2.12.09.