TALLINN UNIVERSITY OF TECHNOLOGY
SCHOOL OF ENGINEERING
Department of Electrical Power Engineering and Mechatronics

DEPARTMENT OF ELECTRICAL POWER ENGINEERING AND MECHATRONICS

PRODUCT QUALITY IMPROVEMENT THROUGH TESTING PROCEDURES

TESTIMISPROTSEDUURIDE ABIL TOOTEKVALITEEDI PARANDAMINE

MASTER THESIS

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Tallinn, 2023

(*On the reverse side of title page*)

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ABSTRACT

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Abstract:

The purpose of the thesis is to research cases that can help to improve overall product quality in the manufacturing field. This research is a study based, where information is collected on historically available data, and based on that researcher has provided the available options for further implementation to improve the available processes in the manufacturing field. In this thesis, the author has used the six-sigma approach which is a study on defining; measuring; analysing; improving; controlling cases while handling process improvement management and project management skills. The conclusion of the study has been written in the thesis with the available options in the market. The improvements described in the thesis can be used by any of the manufacturing companies for future implementation to make improvements in their products. Obviously, improvements/processes can be modified according to the manufacturing company.

Keywords: Quality, Improvements, Master Thesis, PCB, Programming, Gage R&R.

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Märksõnad: Kvaliteet, täiustused, magistritöö, PCB, programmeerimine, Gage R&R.

THESIS TASK

Thesis title in English:	**Product Quality Improvement Through Testing Procedures**
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Submission deadline of the thesis:	21.12.2022

___________________ ___________________ _____________________

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____

Co-supervisor (signature)

1. Reasons for choosing the topic

Author selected this topic *Improvements in product quality* to research because our company's main target is to provide quality products to our customers. Compromising the quality means compromising the growth of the company. Our Products have specified criteria and requirements for testing [1]. Usually, companies have different ways to check quality Like Functional checks by equipment, tests by creating a field environment, Inspections by an external inspector in the factory, final inspections on a platform, piece-by-piece inspections in the factory, training & auditing internal inspector in the factory

The author's main contribution to this task is to study/research different cases that are part and linked somehow with testing the products.

2. Thesis objective

The thesis objective is to have researched existing techniques and documents for improving product quality using different approaches along the manufacturing cycle as introducing Product Control Board (PCB) level into the flow; preprograming at the component level to check on the final test only; checking how formal verification can help in quality; stressing the product under different ground/usability condition as high/low temperature and stressing the product in Stress TEST HW and SW solution for automating looping without forgetting improvements a right Not Fault Found (NFF) process and Gage R&R techniques[2]. This research is a compendium study to understand how important these are and to be aware of what could happen if they are not implemented and the cost related to it. To do it, readers have the luxury opportunity to check on a real supply innovative site in Estonia. Because some information is sensitive for the company some real values only have only available for internal company-related persons, and this is the reason that some references are not public.

3. List of sub-questions

Test Steps that will be part of the Thesis:

- Chip/component quality test
- Programming at chip/component level
- Formal verification of SW
- PCB level test
- No-fault found (NFF)
- Gage R&R
- Stressing the product under different temperature
- Stress the product in looping to secure the stability of the test system

4. Basic data

The author will use data analytics, test analytical, process improvement management, and project management skills to write the thesis and make research on the cases such as NFF, Gage R&R, PCB level test, stressing products under different environmental conditions, Pre-programming electronics components, and stressing test HW and SW solution in order to improve product quality. The author will get the data from the manufacturing companies and follow the generic processes. The data source will be

existing data sources in companies and the google search engine. The company sources are not available for external references, even those are not accessible.

5. Research methods

To finalize the thesis author will use the DMAIC process– A Six Sigma Process Improvement Methodology. DMAIC steps are DEFINE, MEASURE, ANALYZE, IMPROVE and CONTROL. Here researcher has used the DMAIC process in the sense that the author will write the definition/introduction, measurements, analysis, and improvements for the specific case written as per the study performed[3]. Different tasks will be done like; problem statement specifically on the test step, goal statement, project scope, team and responsibilities, time plan, estimated project benefits, etc. MINITAB, companies database will be used.

6. Graphical material

Drawings, tables, and graphs will be part of the main work and will be presented once data will be analyzed.

7. Thesis structure

Some chapter names are mentioned below, and sub-items will be added during thesis writing.

- Preface
- List of abbreviations and symbols
- Introduction
- List of figures
- Introduction
- Chip/component quality test
- Programming at chip/component level
- Formal verification of SW
- PCB level test
- Test based on no-fault found (NFF)
- Gage R&R
- Stressing the product under different temperature
- Stress the product in looping to secure the stability of the test system
- Summary
- List of references

- Appendix

8. References

Companies' references are difficult to share, the author will use study sources from the companies, and because of confidentiality, it is not allowed to share. However, the author has added some external references related to product quality improvements. All the references are at the last of the thesis, I am using references in order to support processes written in the thesis. Some of the references are not my work.

9. Thesis consultants

NA.

10. Work stages and schedule

No.	Task	Time plan
1.	Collecting basic data	Wk45, 2022
2.	Verification and validate the product and the test quality system before its execution	Wk46, 2022
3.	Verification and validation of the test quality result after execution	Wk48, 2022
4.	Completing the first version of the work	Wk50, 2022
5.	Writing theoretical part	Wk50, 2022
6.	Compiling a summary	Wk51, 2022
7.	Sending to the supervisor (first reading)	Wk52, 2022
8.	Final submission	Wk02, 2023
9.	Finalize presentation	17.01.2023

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PREFACE

The idea of this thesis is to study the test steps to improve production quality using different techniques. Quality improvement topic is a general topic in each and every organization and company. The author analysed that quality is the best key to make our customers happy. In that sense, the author thought to perform the investigation using different references and databases and identify the existing areas where some improvement and implementation can be made in the manufacturing companies.

In this topic, the author researched the gage R&R technique, the no-fault found process, the STRESS TEST HW and SW solution process where companies can improve the quality by stressing the product in loops, the technique to stress product in different environmental conditions, finding the way how to pre-program electronics component in respect to programming when assembled, and how to test the product at PCB level, etc. Different techniques are used, and different proposals are provided to the team for further study and implementation.

The author would like to express his gratitude to the supervisor of the thesis, Even Sekhri from Tallinn University of Technology, and Salvador Gonzalez Perez, the line manager of Test Data Analyses working for a telecom company in Estonia for assisting and supporting me in finalizing my thesis.

LIST OF ABBREVIATIONS AND SYMBOLS

BW Bandwidth

CL Clock Loop

DA Data Analyst

DA Data analyst

DFM Design for manufacturing

DT Development team

DU Design unit

FNF Fault not found

FRAG Fault rate analysis group

HALT Highly accelerated life test

HAST Highly accelerated stress test HAST

HS Hansoft

HW Hardware

LA Line manager

LT Leaders team

MP Measurement point

mPjM Maintenance project manager

NFF No fault found

NOK Not Ok

PCB Printed circuit board

PM Program manager

PTDT product test development team

PVT Production verification test

QE Quality engineer

R&R Repeatability + Reproducibility

RCA Root Cause analysis

Re-HALT Retest of Highly accelerated life test

RF Radio frequency

RM Resource management

RTC Rapid thermal cycling

SW Software

TDE	Test development engineers
TDT	Test development team
TE	Technical engineers
TOR	Transmission observation receiver
TX	Transmitter
YWoR	Yield without repair

INTRODUCTION

Overview

In this competitive environment, every company/field would like to provide their products with better quality to their customer to maintain the standard in the market. To beat the competitors, the key is delivering the best quality of products. In the existing telecommunication field, the companies those are competing are Intel, Taiwan semiconductors, Qualcomm, Micron, Ericsson Broadcom, and AMT, etc. Compromising with the quality means compromising the growth of the company. Every company is interested in maintaining the standards and values of its brands. Cost-efficiency and quality are the main factors and biggest challenges for a company to be achieved. However, to stay in this competition it should be maintained. In leading industrialized countries, a high-quality degree is necessary to remain competitive. For production, checking the quality of each product is challenging.

Human handling can cause defects in the products which could be at any stage during the production of the product. It does not matter which kind of product, but the quality check is important for every product, Software, or Hardware. Testing is the main factor to check the quality of the system. Testing is to determine whether the product meets the expected requirements or not. The main motive to test the product is to find errors, issues, bugs, and if the products match with the actual requirements or not, etc before sending the product to the customer. If in the case of the bug, an issue is found during the testing then it is easier to fix the issue in the early phase. It helps to save money if the bug or issue is reported during the testing then the products are found faulty at the customer end. It increases the return or claim rate. Testing helps to secure our internal information which can go out if having any bugs in the product. Checking the quality during production gives the best satisfaction of the customer which is the main objective of the company.

The quality function deployment method is an effective method of managing product quality and reliability improvement[4]. The main failure modes and causes can be obtained from the quality guarantee data statistical analysis and translated into customer requirements. The purpose of the thesis is to Study the different test steps which will be added to the existing generic processes to minimize the quality issues and improve yield. The study will be based on different failures and test steps.

Background

The processes are already existing in our manufacturing companies however this research is based on the improvement of the existing processes [5]. Products have specified criteria and requirements for testing. Usually, companies have different ways to do quality checks like Functional checks by equipment, tests by creating a field environment, inspections by an external inspector in the factory, final inspections on a platform, piece-by-piece inspections in the factory, and training & auditing internal inspectors in the factory, etc.

Here the target is mainly on the test systems which help to provide better quality, and in that sense, testing will contribute to the overall projects differently. As the researcher has selected quality so here test is the area where to prove the quality of the products, in this study the techniques are to research.

- Chip/component quality test
- Introducing pre-programming chips.
- Formal verification of SW
- PCB level test
- No-fault found (NFF)
- Gage R&R,
- Stressing product under environmental conditions,
- STRESS Test HW and SW solution

The idea to perform or make a setup for Testing is to identify failures/defects, reduce the bugs/flaws in the system/product, and improve the overall quality. Improvement of quality plays the biggest role in capacity calculation as well. Testing makes sure the product is reliable to use and works perfectly at the customer end[6].

The generic process for producing a product is in figure 1, the author has explained his proposal for the process flow by marking the cases which he will introduce later in the thesis. This flow shows the manufacturing steps where cases for the quality check can be performed, this is prepared by the author by generalizing available data in manufacturing companies.

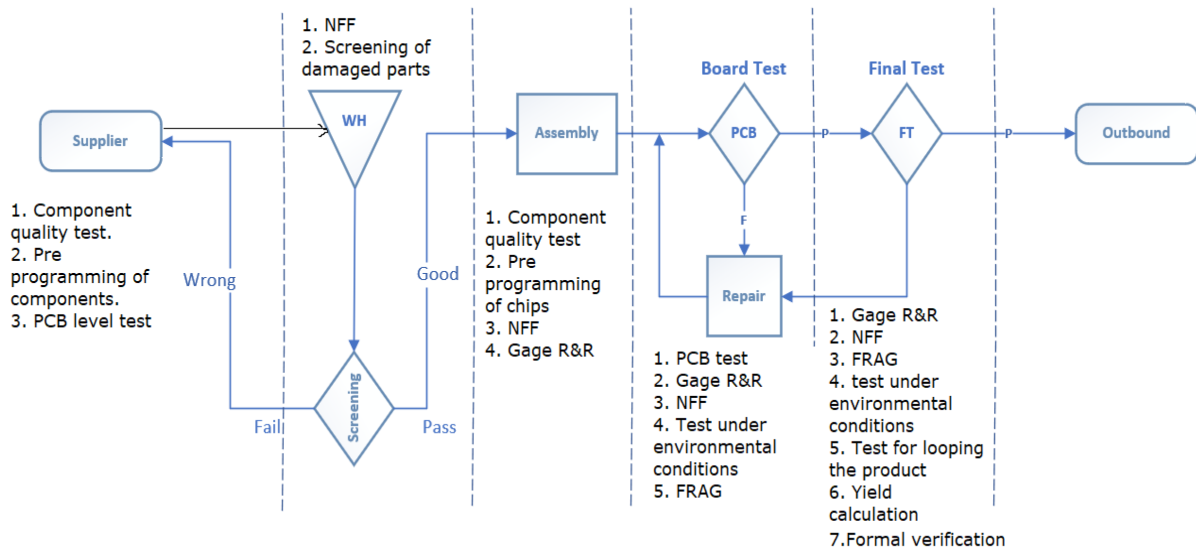

Figure 0 Generic process with the cases which will be discussed

Problem Statement

Test setup already exists in the company to check the quality of products. In every step/field, humans are involved, and the defect can occur due to human errors and HW/SW issues which affect the quality of the product. It sometimes effects the capacity of the production because the production capacity is based on the quality and availability of test equipments[7].

To make sure 100% qualified products, companies need to add some more steps in the testing or inspection. However, every company always looks to have more qualified products to make our customers satisfied. Companies main target is to have a zero-return rate and zero claim rate. In one of the research projects, it is mentioned that for quality and testing inspection overall cost for new product development is [2]5000 to 50000 Euros. To have qualified products, companies need extra manpower, techniques, time to spend, and cost to focus only on quality to reach a 100% level of the quality.

The test flow usually in manufacturing companies are well stable to check the functionality of the product according to specific requirements however companies still have some failures which are found at the functional test and some of them are reported with the claim and return products. The issues which are found at functional test increase the disassembly and assemble time of the product and the quality issue

[2] *The values mentioned are just for analysis, values are valid for generic products for inspection of quality and for new product development. There is no connection between these numbers to any company relevant data or product*

reported by the claim or return product increases the overall cost to the company[8]. In one of the research projects, it is mentioned that only 2:1 revenue will be acceptable for the manufacturing companies by the of the product is acceptable. Usually, zero is the ideal failure rate however it is not possible because of invisible bugs the acceptable return rate is [3]0% to 15% for the manufacturers[9].

[3] *Return rate percentage is calculated on a generic level for research purposes.*

Different techniques to be discussed

Chip/component quality test: Introduction; Advantages to implement chip level test; Observations and suggestions, Check components at supplier end, Test and verify components just before assembly; and Overall conclusion.

Programming at chip/component level: Introduction; Analysis and options, Program components at vendor end, Programming system in factory; and Conclusion.

Formal verification of SW: Introductions, Performed verification on Output power for Tx test case, Performed verification on Delay for Rx test case; and Conclusion.

PCB level test: Introduction; Advantages; Facts and risks; Option; and Conclusion.

No-fault found (NFF): Introduction; Author contribution to NFF investigation; Proposal on the NFF process, Information Flow, NFF impacting with solution flow, Project Updates; and Conclusion.

Gage R&R: Introduction; and Conclusion.

Stressing product under environmental conditions: Introduction; HALT; HAST; Measurements for the thermal chamber; and Conclusion.

STRESS Test HW and SW solution: Introduction; Problem addressed; Process for Clock-test loop; and Conclusion.

1. CHIP/COMPONENT QUALITY TEST

1.1 Introduction

Chip/component test can be used to check the standalone electronics components at the beginning before assembly to any final product. Some of the electronic components are very expensive and some electronic components can not repair once install in a printed circuit board(PCB)[10]. Because of not having to repair properties for those electronic components it ends up in scrapping the whole printed circuit board. So in this research author is looking for an option to test electronic components in advance before assembly to minimize repair and scrap tasks. In research of chip/component level testers, the author will analyze what testers can improve the quality of the final product with help of checking to unassemble electronic components where the issues can be detected in advance. The author has gone through difficult conversations and situations as one of the most difficult tasks was to figure out what components to consider for the analysis. In the final, he decided to choose the components which are difficult to repair after assembling like BGA components (like Snowridge, Wolverine, and Grand Ridge, etc), and the components that can be received faulty batches from the supplier[11].

1.2 Advantages to implement chip level test

- Save disassemble time if chip issue can be detected in the early phase.
- Fewer products will go to scrap.
- Save manpower for repairing and assemble.
- Electronics components can be sent back to the supplier if found faulty batch.
- Check defective electronic chips in advance.

1.3 Observations and suggestions

1.3.1 Check components at the supplier end

The author of the research analyzed that some expensive components can be tested and verified at the supplier's end just after the production of electronics components which is possible at the supplier’s house. During the research[12], the author has been in the contact with the supplier to investigate how to move forward.

During the conversations with the supplier Author's observations/risks

- Mode of conversation: Online meetings, Emails, etc.
- Who will own the cost of development and implementation (Supplier or factory)?
- At the supplier end, what will be the frequency level to test the components (100% or less)?
- How components will be isolated for tested and untested components if not tested at 100% level?
- How tested/not tested components will be identified if failed after assembly at the final production?
- Difficult to convince the supplier that their components are faulty.
- Difficult to make an agreement with the supplier as it is an extra step for them to implement in their production.

With the discussions/investigation with the supplier, the researcher has concluded that it is ok to make the development of such testers that can test at the component level at the supplier end. However, it will be only for components that have more failures. The cost of development and implementation can be discussed and depending on the factory it can be decided. One good thing one of the suppliers shared a possible board (Lake board tester) tester can be developed to verify their components. If the supplier agrees to make this development at their end it will help to improve [4]2 to 6 % of yield rate which is basically cost saving of retesting and repairing a product by approximately [5]10 to 70 euros. It is not finally decided how to isolate the tested and untested components however there are a few suggestions like the tested components can have an extra level with the mark but it is not easy to implement. The discussions are still ongoing to finalize component verification at the supplier end. Here new investigation will come into the picture to find the solution to segregate the tested and untested electronic components, Author will not talk about that here.

1.3.2 Test and verify components just before assembly

During the analysis of chip-level testing, the author of the research analyzed the existing option where the author can verify electronic components just before assembly at final production house[13]. For this investigation, the author has been in referring the

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[4] *Values are calculated based on generic processes, the percentage has not any linked with any specific company.*

[5] *This value is calculated by plotting different companies costs for repairing and repairing per product. The number can vary depending on the products and processes of the manufacturing company.*

available data for the manufacturing companies to analyze the current situation. During the conversations with the internal stakeholders author's observations and open questions

- Mode of conversations: Online meetings, Emails, and offline discussions, etc.
- Who will be developing such tester (HW+SW)?
- Same chips/components will be used in different products, how to segregate?
- What will be the frequency level to test the components (100% or less)?
- How components will be segregated between tested and untested components?
- How components will be identified if failed after assembly at final production?
- What will be done with the component if tested component failed at final assembly test? Etc.

During theinternal discussion, the researcher has lots of open questions the biggest one is thatthe components company received for further use are produced by the supplier so theresponsibility for the quality of the component should also be of the supplier. Whichis a valid point. However, the Author analyzed that company might need atester/fixture which can be developed by one of the suppliers(Lake board tester) foranalysis purposes in the troubleshooting area or repair area.

1.4 Overall conclusion

The author has analyzed that both the given options to verify electronics components as per the requirement before they assemble to any PCB are for now NOK means conditionally acceptable where the conditions are already written in the above clauses. The author's next task will be to resolve the open question so that the development of electronic components can be started quickly. Overall for chip level quality check, it is under discussion to finalize it[14]. The conclusion for the research on chip-level tests is that the author has made a study as an electronics/technical engineer to minimize failures because of BGA components and improve the overall yield at the production. With overall calculation, the Authors receive the pre-qualified and verified electronics components for the assembly on PCB, which will save the cost of [6]10 to 120 USD per

[6] *The cost mentioned is calculated for the general technique used to test electronic components for quality, it is calculated by plotting different processes at manufacturers.*

product which is basically a saving of 2% to 7% of yield improvement. The future trend to have testers for electronics components will obviously rise based on investigations.

2. PROGRAMMING AT CHIP/COMPONENT LEVEL

2.1 Introduction

During the research to improve the overall quality of the production, the researcher found that programming of electronics programmable component level is another option to save the overall test time and improve quality with the precheck. The idea came into the picture when the researcher analyzed that overall test time is high and one part of the final test is the programming of electronics components. Usually, programming takes 3-6 mins on the electronics components depending on what components are to be programmed. With this level, companies can have the chance to secure preprogrammed chips/components for the final assembly and testing[15]. Preprogram is to configure chips used in the products in advance and then assemble them on the specific product/PCB to reduce the over testing time and check in advance if the chip has some programming issue.

Overall test time with programmed chips can be reduced at the final functional test because at the functional test then no need to perform programming of the components which is approx from 3 to 6 mins. On the other hand, preprogrammed chips will help in improving quality by checking the functional chips in advance.

Advantages

- Reduce overall testing time at the final level
- Less products will go to scrap by verifying the programming issue.

Disadvantages

- Without some electronics around is not possible to pre-program

2.2 Analysis and options

2.2.1 Program components at vendor end

The researcher has analyzed that it would be good if the author can have discussions with the supplier who supplies the programmable components. The author's idea behind having conversations with the supplier is to get preprogrammed components from the supplier itself to minimize extra handling time in final product production[16].

During the conversations with the vendor researcher observations/risks

- Mode of conversations: Online meetings, emails, etc.
- Who will own the cost of development and implementation of the programming tester/system?
- How components/chips will be segregated if programmed/calibrated/data or not programmed?
- Difficult to convince the supplier to make them agree to implement programming system at their production.
- How to track which chips are delivered for which product with what programming?

With the discussions with vendors, the researcher has concluded that it is ok to make the development/implementation of such a programming system which can provide preprogrammed to save overall testing time at the final stage. However, it will be difficult to segregate the programmed and not programmed chips as the vendor delivers the components in batches with not any marks and it would be difficult to isolate them. The components are recognized by their specific number or name so all particular chips will have specific product numbers. The author is keeping this topic for further investigation to finalize programming at the supplier end. This is difficult at the component vendor end as well as it is an additional requirement from manufacturing companies.

2.2.2 Programming system in at the final factory

During the analysis of pre-programmable system implementation, the author of the research analyzed that usually companies have an option where they can implement/develop a programming system of programmable components before assembly in-house as well[17]. For system implementation in-house, the researcher has gone through discussions with the internal stakeholders to analyze the existing situations and risks. Author's conversation and analyzed risks with internal stakeholders

- Mode of conversations: Online meetings, emails, and offline discussions, etc.
- The biggest considerable risk that mixing chips/components with the different SW which will be used in different products.
- What will be done with the component if having a programming issue before the final assembly? etc.

The researcher has summarised the overall discussion with the internal stakeholders. Usually, programmable chips can be used in different products with a different configurations. if the author agrees to do programming at our factory, it seems that it will lose the flexibility to use programmable chips. In-house companies usually have a high chance to mix up the programmed chips which can lead to more scraps of the final products because the same programmable chips can be used in different products which means that those chips will have the same Product number. The researcher analyzed that in generic when the same component is usable in different products it is hard to decide what programming has been added to the particular component [18]. However, the author investigated the available testers/systems in the market which can be used for the in-house programming of chips. Below are the two options for automatic production programming systems which are investigated by the author.

BPM 4910 Automatic Production Programming System

- Faster and Easier
- Up to 1,708 Devices per Hour
- Component Handling Range: 0402 to 240-pin QF
- Architecture: 9TH Gen Concurrent Programming System with Vector Engine Co-Processor

Figure 2.2.2(a) BPM 4910 Automatic Production Programming System

BPM 4910 Proposed Configuration

- FP4910 – Programming System (1 to 12 Pgm/site, 1-4 sockets/site, 48 sockets)
- 3 x X900 – Auto Programming Site, (1 to 4 sockets/site, 12 sockets) [18]
- Assembly, monitor arm, auto
- 1-Tray Assembly
- FSW49 – BP4900 Software Support
- FSWAPI49 – API Software Feature 49x0
- TM-50 Tape output Loader
- Safety door, 4xside
- Xstream tape input & take up 4x
- Xstream series tape FDR 16mm
- Xstream series tape FDR 12mm
- Standard spare parts kit, 4910
- Installation & Education, 3 days onsite or web-based
- Proposed BPM 4910 System Price: € 335,000.00

BPM 3928 Programming System:

- Award-winning BPW TM Software
- Handler Throughput: Up to 1,432 Devices per Hour
- Component Handling Range: 0402 to 240-pin QFP
- 9TH Gen Concurrent Programming System with Vector Engine coprocessor

Figure 2.2.2(b) BPM 3928 Automatic Production Programming System

2.3 Conclusion

The researcher concluded from the overall investigation that both the options programming at factories or programming at the vendor end are fittable. However, for further research, the author will find the solution to open question the one is how to segregate the programmed and unprogrammed components to make an accurate final assembly. To implement a programming system author need to set up effortless sorting of programmed chips according to their configuration where the author can decide with some label or automatic which configured chip has which program and to which product it will assemble. Both options available for programming systems BPM 4910 and BPM 3928 are acceptable depending on in-house requirements. With this implementation, overall [7]3 to 7 mins and 1 to 2% of yield will improve on functional tests at the manufacturing site.

[7] *This data is for research purposes only and it is calculated based on common processes and available options, there is no direct link of this data to any of the companies.*

3. FORMAL VERIFICATION OF SW

3.1 Introductions

The researcher has studied that companies formal verification of SW s done to verify if the prepared SW for the product is according to the test requirement of the product and fittable for the produced product[19]. This verification will check if the SW is correct or not, if the procedure or steps of the SW are correct, if is it according to the product specifications or not, if the SW is stable or not, etc. This procedure of verifying each and every step of the test case of SW is done by the SWverify tool. Once the complete SW is ready and 100% implemented according to the test requirement of the product, the author analyzed few weeks are needed to verify each and every step of the SW. Once formal verification is done for the SW, the product can be produced for customer orders. If the product gives deviation in the result, the information with isolation values will be sent to the design unit(DU)[20] or to the test SW development team(TDT) to check the test requirement again and align it according to the deviation values. The author has approached responsible stakeholders to understand and study how to perform formal verification of SW, which will be explained in 3.1.1.

3.1.1 Performed verification on Output power for Tx test case

For the research, the author has chosen a simulated case for experimenting with TX output power on mid-power, high power, and low power. The experiment consists of a circuit with a power amplifier with which TOR will be calculated. In this experiment, some power is injected and then output power will be calculated. The verification process consists of 10 samples on different BW on 32 test points. This data is just for experiment purposes, nothing related to the real product, and try to find what is the deviation with help of the transmission observation receiver(TOR). For the below measurements, there is an approximately [8]0.4 - 0.5 dB difference between production results for the verified product and P values, obtained on the verification setup. Data from the verification setup corresponds with general distribution from the database tool with verification product results in production being the outliers. Data from the verification setup also corresponds with data from the same product, when measurements were performed on Station X.

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[8] *This value is calculated based on values measured and generic values available for the output power for the TX test, it is an estimation, not a real value.*

The conclusion for the below measurements is that the result is passed because in measurements, there is an approximately 0.4 - 0.5 dB difference between product results for the verification unit and the peak values, obtained on verification setup. The difference in the expected value is only with marginal value and it will be investigated further to see why this happens. A few experimental measurements are mentioned below.

Table 1 Measurement for TX output power on mid, high, and low power

Test Point Code	Test Point Name	TC 1 Test Point Limit Low	TC 1 Test Point Limit High	#Sample	Measured Average	Standard Deviation	Min	Max	TC 1	TC 2	TC 3	TC 4	TC 5	TC 6	TC 7	TC 8	TC 9	TC 10
1.11.10.0.0	TX Output Power_mid Pwr: [0] dB branch D (A)	-0.30	0.30	10.00	-0.11	0.01	-0.12	-0.09	-0.09	-0.10	-0.11	-0.11	-0.11	-0.09	-0.09	-0.10	-0.11	-0.11
1.11.10.0.1	TX Output Power_mid Pwr: [0] dB branch C (B)	-0.30	0.30	10.00	-0.12	0.01	-0.14	-0.10	-0.11	-0.11	-0.12	-0.13	-0.11	-0.11	-0.10	-0.11	-0.13	-0.12
1.11.10.0.2	TX Output Power_mid Pwr: [0] dB branch B (C)	-0.30	0.30	10.00	-0.13	0.02	-0.15	-0.10	-0.11	-0.12	-0.13	-0.15	-0.13	-0.10	-0.11	-0.13	-0.14	-0.14
1.11.10.0.3	TX Output Power_high Pwr: [-3] dB branch D (A)	-0.30	0.30	10.00	-0.08	0.01	-0.09	-0.05	-0.08	-0.08	-0.08	-0.09	-0.08	-0.05	-0.05	-0.09	-0.09	-0.09
1.11.10.0.4	TX Output Power_high Pwr: [-3] dB branch C (B)	-0.30	0.30	10.00	-0.08	0.01	-0.09	-0.05	-0.08	-0.08	-0.08	-0.09	-0.09	-0.05	-0.06	-0.08	-0.09	-0.09
1.11.10.0.5	TX Output Power_high Pwr: [-3] dB branch B (C)	-0.30	0.30	10.00	-0.08	0.02	-0.10	-0.04	-0.08	-0.08	-0.09	-0.10	-0.10	-0.04	-0.06	-0.08	-0.09	-0.09
1.11.10.0.6	TX Output Power_low Pwr: [-3] dB branch D (A)	-0.30	0.30	10.00	-0.05	0.02	-0.07	0.00	-0.04	-0.03	-0.05	-0.06	-0.05	0.00	-0.02	-0.05	-0.04	-0.06
1.11.10.0.7	TX Output Power_low Pwr: [-3] dB branch C (B)	-0.30	0.30	10.00	-0.06	0.02	-0.08	-0.02	-0.05	-0.05	-0.06	-0.07	-0.07	-0.02	-0.04	-0.06	-0.05	-0.07
1.11.10.0.8	TX Output Power_low Pwr: [-3] dB branch B (C)	-0.30	0.30	10.00	-0.06	0.02	-0.09	-0.02	-0.06	-0.06	-0.07	-0.07	-0.07	-0.02	-0.04	-0.06	-0.05	-0.07
1.11.10.0.9	TX Output Power_mid Pwr: [-3] dB branch D (A)	-0.30	0.30	10.00	-0.09	0.01	-0.10	-0.06	-0.09	-0.09	-0.09	-0.10	-0.09	-0.06	-0.07	-0.09	-0.09	-0.10
1.11.10.0.10	TX Output Power_mid Pwr: [-3] dB branch C (B)	-0.30	0.30	10.00	-0.09	0.01	-0.10	-0.06	-0.09	-0.09	-0.09	-0.10	-0.09	-0.06	-0.08	-0.09	-0.09	-0.10
1.11.10.0.11	TX Output Power_mid Pwr: [-3] dB branch B (C)	-0.30	0.30	10.00	-0.10	0.02	-0.12	-0.05	-0.10	-0.11	-0.11	-0.11	-0.11	-0.05	-0.08	-0.09	-0.10	-0.11
1.11.10.0.12	TX Output Power_high Pwr: [0] dB branch E (E)	-0.70	0.30	10.00	-0.10	0.02	-0.12	-0.06	-0.10	-0.11	-0.09	-0.09	-0.09	-0.06	-0.10	-0.09	-0.10	-0.12
1.11.10.0.13	TX Output Power_high Pwr: [0] dB branch F (F)	-0.70	0.30	10.00	-0.08	0.01	-0.10	-0.06	-0.08	-0.09	-0.07	-0.07	-0.06	-0.06	-0.08	-0.07	-0.08	-0.09
1.11.10.0.14	TX Output Power_high Pwr: [0] dB branch G (G)	-0.70	0.30	10.00	-0.10	0.01	-0.11	-0.07	-0.10	-0.10	-0.09	-0.09	-0.08	-0.07	-0.10	-0.09	-0.11	-0.11
1.11.10.0.15	TX Output Power_low Pwr: [0] dB branch E (E)	-0.70	0.30	10.00	-0.08	0.01	-0.10	-0.05	-0.08	-0.09	-0.09	-0.09	-0.08	-0.05	-0.08	-0.07	-0.09	-0.10
1.11.10.0.16	TX Output Power_low Pwr: [0] dB branch F (F)	-0.70	0.30	10.00	-0.07	0.01	-0.08	-0.05	-0.07	-0.07	-0.07	-0.08	-0.06	-0.05	-0.07	-0.06	-0.08	-0.08
1.11.10.0.17	TX Output Power_low Pwr: [0] dB branch G (G)	-0.70	0.30	10.00	-0.07	0.01	-0.08	-0.05	-0.06	-0.07	-0.07	-0.08	-0.06	-0.05	-0.07	-0.05	-0.08	-0.07

[9]

Explanation on terms used in the experiment

- Test point code: It is the code to identify what test point has what number.
- Test point name: It is the name of the test performed.
- TC 1, Test Point Limit Low: Test case 1 measurement for low limit
- TC 1, Test Point Limit high: Test case 1 measurement for high limit
- #Sample: The samples on what measurements have taken.
- Measured Average: Average measured values
- Standard Deviation: Deviation calculated on measured values
- Min: Minimum measured values at production.
- Max: Maximum measured values at production
- TC1 to TC10 is the measurement value for test cases 1 to 10 with 10 units.

[9] *The measured values are just for experiment, no relation of these values with any real measurements.*

3.1.2 Performed verification on Delay for Rx test case

For further studies of formal verification of SW, the author has chosen another parameter for an experiment which is output power for Rx with delay. This is an experiment on a product that differs from the real implementation. The author has chosen a simulated case for experimenting with TX output power on mid-power, high power, and low power for one of our products. The author has taken verified the case with 1 sample on different BW on 32 test points, this data is just for the experiment nothing related to the real product. For this verification the sample rate is 1 product of different BW, this data is just for experiment purposes with this data nothing to do with the real product. According to the test requirement, the pass criteria are defined for Rx AGC phase delay and Rx delay frequency response.

Explanation on terms used in the experiment

- Test point code: It is the code to identify what test point has what number.
- Test point name: It is the name of the test performed.
- TC 1, Test Point Limit Low: Test case 1 measurement for low limit
- TC 1, Test Point Limit high: Test case 1 measurement for high limit
- #Sample: The samples on what measurements has taken.
- Measured Average: Average measured values
- Measurement done: Value for measurements done
- diff PROD-performed: Is the difference in production and values measured

Table 2 Measurement for output power for Rx with delay and delay phase

Test Point Code	Test Point Name	TC 1 Test Point Limit Low	TC 1 Test Point Limit High	#Sample	Measured Average	Measurements done	diff PROD-Performed
1.11.1.00	RX_AGC_DELAY agc Port: 0	-10.00	-1.00	1.00	-6.09	-8.03	1.94
1.11.1.01	RX_AGC_DELAY agc Port: 1	-10.00	-1.00	1.00	-5.35	-8.5	3.15
1.11.1.02	RX_AGC_DELAY agc Port: 2	-10.00	-1.00	1.00	-7.36	-8.54	1.18
1.11.1.03	RX_AGC_DELAY agc Port: 3	-10.00	-1.00	1.00	-5.87	-8.81	2.94
1.11.1.04	RX_AGC_DELAY agc Port: 4	-10.00	-1.00	1.00	-6.99	-8.84	1.85
1.11.1.05	RX_AGC_DELAY delay port: 0	600.00	700.00	1.00	634.00	659.84	-25.84
1.11.1.06	RX_AGC_DELAY delay port: 1	600.00	700.00	1.00	661.00	653.61	7.39
1.11.1.07	RX_AGC_DELAY delay port: 2	600.00	700.00	1.00	614.00	653.96	-39.96
1.11.1.08	RX_AGC_DELAY delay port: 3	600.00	700.00	1.00	632.00	661.08	-29.08
1.11.1.09	RX_AGC_DELAY delay port: 4	600.00	700.00	1.00	645.00	662.64	-17.64
1.11.1.10	RX_AGC_DELAY delay3port: 0	525.00	625.00	1.00	581.00	572.13	8.87
1.11.1.11	RX_AGC_DELAY delay3port: 1	525.00	625.00	1.00	579.00	566.27	12.73
1.11.1.12	RX_AGC_DELAY delay3port: 2	525.00	625.00	1.00	580.00	567.96	12.04
1.11.1.13	RX_AGC_DELAY delay3port: 3	525.00	625.00	1.00	567.00	570.14	-3.14
1.11.1.14	RX_AGC_DELAY delay3port: 4	525.00	625.00	1.00	568.00	570.65	-2.65
1.11.1.15	RX_AGC_DELAY phase port: 0	-3.00	6.00	1.00	-1.10	4.27	-5.37
1.11.1.16	RX_AGC_DELAY phase port: 1	-3.00	6.00	1.00	-0.10	4.99	-5.09
1.11.1.17	RX_AGC_DELAY phase port: 2	-3.00	6.00	1.00	0.40	4.77	-4.37
1.11.1.18	RX_AGC_DELAY phase port: 3	-3.00	6.00	1.00	0.40	4.22	-3.82
1.11.1.19	RX_AGC_DELAY phase port: 4	-3.00	6.00	1.00	0.10	3.82	-3.72

[10]

[10] *The measured values are just for experiment, no relation of these values with any real measurements.*

In the above snip, the Author has reported only a few values. Here researcher has some reverse values which are not according to the test requirements. The Delay limit is lying between D 600 to 700, Φdiff , 0->1: -4~7, Φdiff , 1->9: -11~1. However, delay limits are different which the author will not mention as per the confidentiality of the test requirement. One example from the above snip: {"value": 653.65, "unit": "ns", "limType": 3, "lim1": 600.00, "lim2": 700.00}. The above logs used for experimenting have been taken from the log file of the test, and it clearly shows that due to the wrong limits defined in the test requirement it failed. These all values are for experimental purpose only, it has no any relation with the real life products.

3.2 Conclusion

With the above performances, the Author concluded that verification of SW with the verified products should be necessary for the quality. For formal verification of SW, a 100% verified, tested and calibrated product should be used to get accurate results. Values which was measured will be considered reference value and can be used in the future for tester verification[21]. Another point is that the same product can be used as a reference product to measure with other faulty products to match product quality and to find issues in the faulty products. The first experiment result for verification on Output power for the Tx test case is passed and it is as per the test requirement. Another test performed for verification on output power for the Rx test case failed and it has reverse values and the result is not according to the test requirement defined by the design unit(DU). The instruction can be shared with the design unit for updating the test requirement and software package for further verifications. If the product does not pass this formal verification of SW, that means that the product does not match the actual values of the hardware and the requirement which shows that the hardware product has some issues. The efforts made to make this experiement takes usually [11]1-2 days and the cost for performing one experiment will be approximately 100 to 250 USD.

[11] *Estimations are based on calculations for the generic process.*

4. PCB LEVEL TEST

4.1 Introduction

During the research to improve product quality, the idea of testing the PCB board came into the picture. The researcher has observed a test can be performed after the assembly of all the electronic components. So basically with some investigation, the author has found that through stressing PCB board testing can be performed before mechanical parts assembly to the printed circuit board. With PCB testing, the issues on the electronic components can be detected in advance. As PCB level test will help to improve the overall testing yield, which is usually measured by the software which measures first pass and overall yield [22]. Yield is measured by the proportion of correct/passed products in comparison to the overall products you put in. Please refer below image(In this case yield will be: 356/361 = 0.98%)

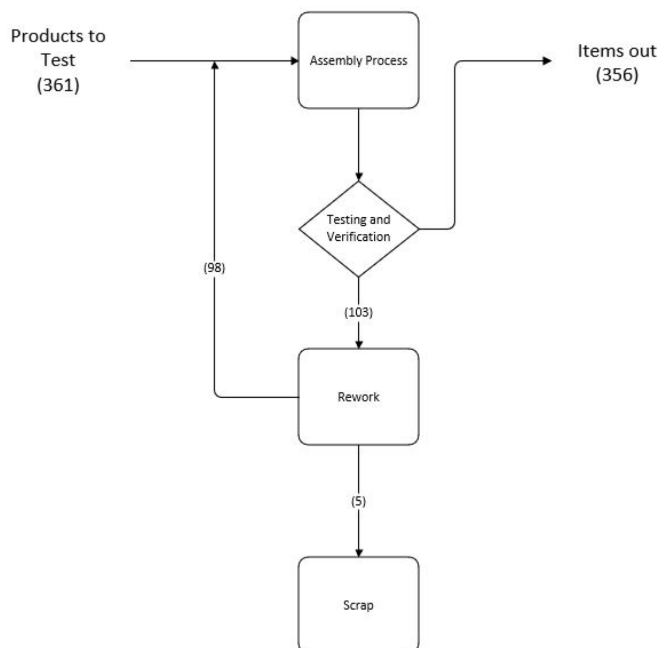

Figure 4.1 Yield process

4.2 Advantages

- Avoid to mount faulty PCBs in final products.
- PCB level tester could be cheaper than the final functional test after assembly.
- Saves disassembly and re-assembly time for faulty products.

- Overall Testing yield = PCB-level yield * functional-level yield
- PCB level tester might help to reduce testing time at the functional level as some of the test steps can be skipped from the final functional test which is also passed at the PCB level.
- According to the investigated results it will help to improve functional level yield.

4.3 Facts and risks

If test all mass products on the PCB level with an automatic PCB tester

- At the PCB level tester, it has a high chance to damage the components, as the PCB board has all the electronics open components without any mechanical protection which will be easily damaged and will lead to more scrapping cost [23]
- If the author makes an agreement, it should be aligned with all production sites, as well as author's opinion is to pay more for the equipments.

If test all volumes on the PCB level with a manual PCB tester

- With manual tester it has even more chances to damage the components because the tester will be handled manually, and still open components will exist which will take to more scrap cost.
- Suggestion to have only on premature builds or in early phase builds to verify product requirements.
- More manual work however, companies are moving towards automation.
- Need experts to work on Mass production testing, difficult to be handled by production operators.

4.3 Option

During the investigation, the researcher found a company named Columbia a Swedish brand, those works on electronics fixtures including HW and SW. Columbia gives the chance to the customers to get customized fixtures according to customers requirements. The researcher also found an available fixture that can be customized according to the requirement of the product [24]. Below is the picture of Columbia’s existing tester which can be modified in different sizes and requirements based on the

product. For this option, the companies can provide the product specifications to make modifications to the existing testers [25]. To find

Figure 4.3(a) Columbia PCB test tester

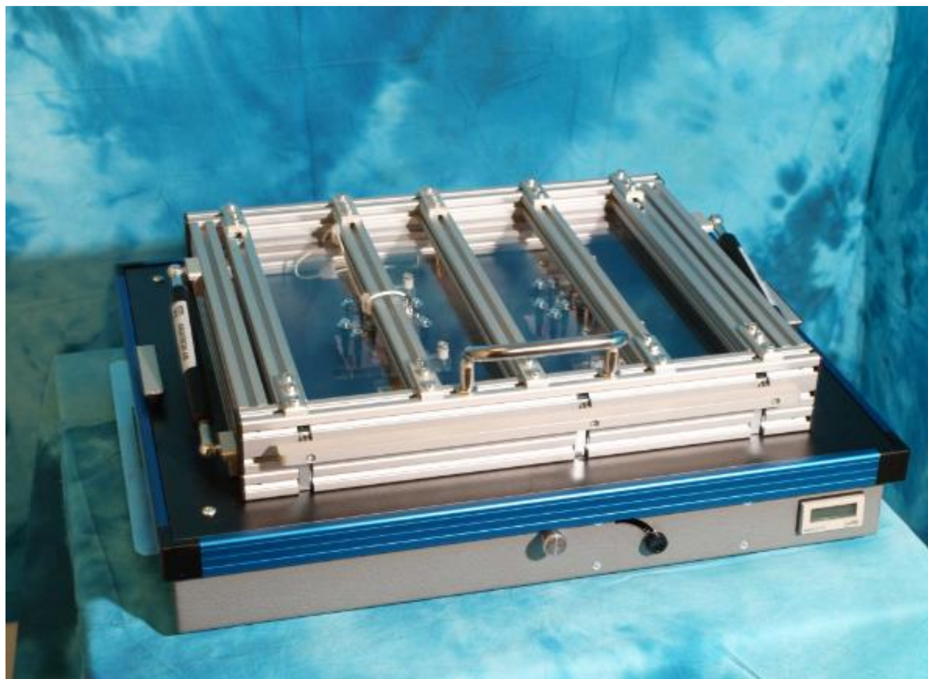

Figure 4.3(b) Columbia PCB test palette

4.4 Conclusion

In the study of the PCB level testing, the author analyzed that author needs to ask Columbia to customize the PCB fixture according to companies products with different sizes and functions. On the other way, such testers can be developed at the production factories as usually NPI sites have HW and SW development teams that can develop such testers as well. The research is made only on the existing product which is open on the search engines and can be purchased by anyone according to the requirement. It is good that Columbia provides the full package including hardware and software so for customers, it is easy to just implement. With the PCB tester for the research data, it is calculated that approximately [12]50 to 450 USD cost can be saved only by saving disassembly and assembly time. Yield without repair can be improved by [13]1% to 6% on the overall yield. will On the other side, scrapping costs might increase with [14]1 to 4% of overall scraps, Columbia company has also its products specification on its website as well so can be followed easily. Overall PCB level testing will help to find the issues of assembling electronic components on a printed circuit board. However, in the investigation, it has been noted that the PCB fixture will be complex HW as high-quality requirements of the products towards handling PCB board and overall automation strategy will make it more complex.

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[12] *Estimated disassembly and assembly time is calculated based on product assembly time including handling time with respect to products available globally in telecom industries, this value is not based on real product.*

[13] *Yield without repair is calculated by plotting different data from already research done.*

[14] *Estimated scrapping cost is measurement done based on the research data, no link to real data.*

5. TEST BASED ON NO-FAULT FOUND(NFF)

5.1 Introduction

NFF is introduced as no-fault found. This is considered when the author has a fault but can not decide the cause of the fault in the product. The cause in NFF can be anything, product issue, test HW issue, test SW issue, component issue, stability issue, and environmental issues, etc. When it is difficult to know the reason for the fault, it is hard to implement the improvement or diagnose the fault. During the research to improve product quality, the researcher summarized that if author can reduce the NFF level that will ensure yield improvement or product quality in any of the production factories. [26]. In a generic way, NFF depends on different conditions like SW, HW instability, shift change, the person with more experience, etc. As we discussed in the previous chapter that first pass yield and yield without repair(YwoR) are two different measurement terms, which is another way to introduce that NFF exists.

5.2 Author contribution to NFF investigation

- The NFF process must be implemented when the product is ready for customer delivery and finished its NPI phase and moved to the maintenance phase. However, in some cases, NPI phase can also have NFF.
- NFF investigations start when it is highlighted by the Quality engineer during development activities or monitoring activities.
- At the first, test data analysis must discover fluctuations in test results and pre-categorize the root cause. After that the Quality department performs the sorting and initial evaluation of test cases of NFF impact, then the Fault analysis group will decide to discuss the impact and cause with different functions of the product development.
- Apply the NFF process during the new product development (NPD) phase is complicated because the product itself is not mature and usually the main focus of production in the NPI phase of the product is on making product with important quality issues. Another issue in the manufacturing field is that the quality of the resources needed to perform RCA and time to volume made it difficult for companies to deal with it from priorities and cost points of view besides new products development.

Proposal on resource requirements: The author just proposed only one new process, however, for NFF there can be different proposals one of them is explained in detail:
NFF Coordinator: The NFF coordinator should be responsible to care about the needed processes to solve NFF and increase the stability of Hardware/Software.

NFF Coordinator: will participate actively in the meetings to advise regarding resource estimation and assignment according to the priority of the test case which has NFF. This role will be almost like a project manager who will consider a single NFF as a project by aligning resources, priorities, risks, effects, timeframe, etc.

Technical Resources/Engineers: The technical resources will be working on a test case which will be shared by the NFF coordinator to find the cause of the NFF. Technical resources will be responsible to obtain the technical solution for each NFF. Technical resources should give the ideas to resolve the NFF that occurred on the products to make it stable including HW and SW. NFFs are usually complex in nature and only experienced engineers who have a deep understanding of product systems, test systems, internal processes, and knowledge of historical issues should handle the NFFs.

Other active roles: A quality Engineer (QE) can be appointed as a quality inspector to perform inspection virtually and onsite to evaluate the NFF impact, and impact on product quality, and production capacity and to check what products are affected. QE will be the person who will create the backlog and continuously monitor the solutions.

5.3 Proposal on the NFF process

Companies usually have existing processes to resolve NFFs however in some generic existing processes this is the proposal from author's side. The researcher has studied an NFF process to implement in production to track and work on NFF cases that occurred in the production site. The process will start by evaluating the NFF impact and production capacity of the quality engineer and information will be sent to the NFF coordinator to create resource estimation and bring the responsible technical resources into the picture. Then NFF coordinator will create the priority of the task and schedule a discussion to discuss the NFF with the technical engineer and accordingly assign the task to the responsible engineer. Technical engineers will create a Root cause analysis (RCA). Once TEs find the root cause they will implement the solution and send the

solution to production for trial and monitoring[27]. The QE will be monitoring and tracking the results of implemented solution on the case.

If QE will notice that issue has been resolved and no further issues have occurred, then the particular NFF case will be closed. If during the monitoring phase, QE finds that the NFF percentage for the case is decreased or no positive result then he should inform it back again to technical engineers to work again on the case. Below is the drafted process.

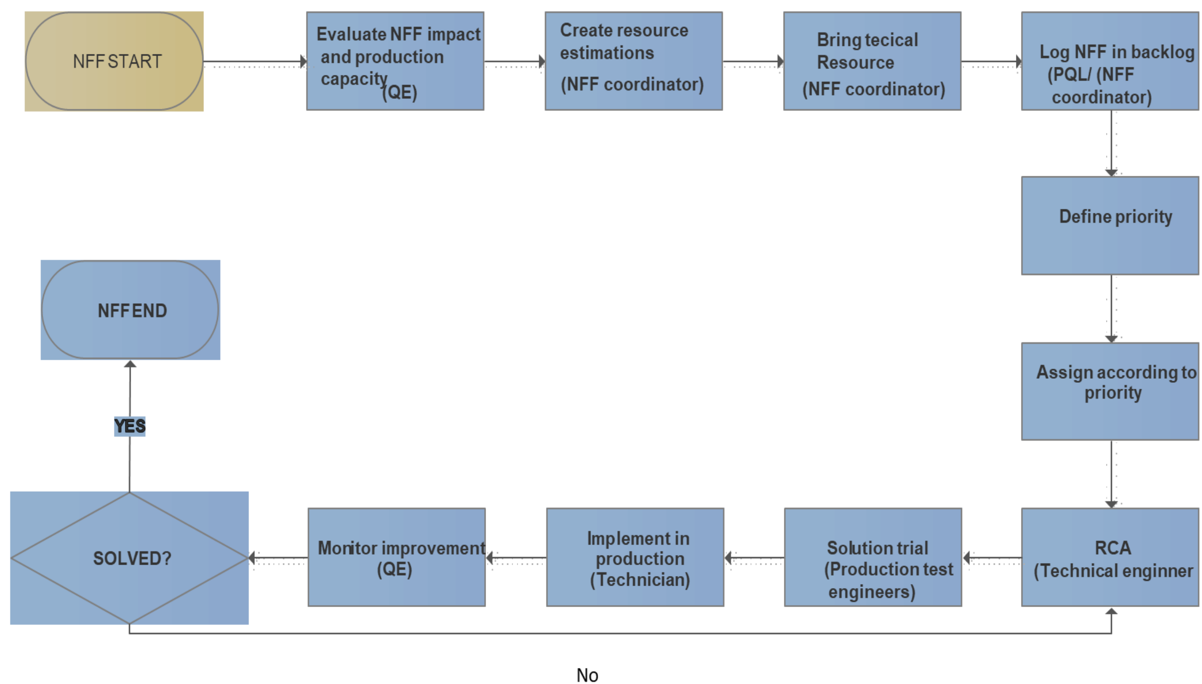

Figure 5.3(a) Draft version of wanted NFF process

The author has put NFF's difficult situation in a process or complex structure below. The researcher has considered that in production sites, not only product and test sites are responsible for disasters to produce NFFs. Other factors like HW stability, noise, design, and shift change are also responsible to decrease overall production yield[28].

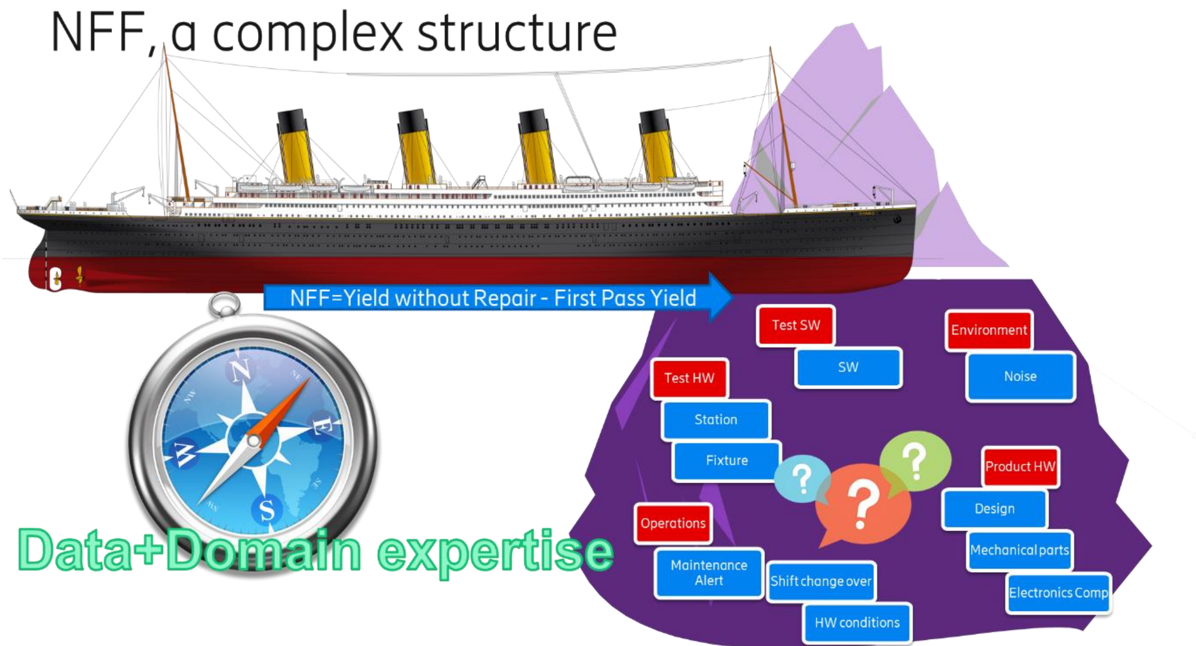

Figure 5.3(b) Complex structure of NFF process

Existing challenges to implementing the NFF process which need to be solved

- Researcher noticed that a responsible driver should be assigned.
- Dedicated team should be appointed.
- NFF case causes are hard to find.
- Difficult to track progress or implementing solutions.
- Need good collaboration with QE and NFF coordinator and use the same source data and angle of visualization.
- It is hard to provide the solution by the technical team as the reason behind failure is not defined.
- Challenge on Categorization NFF, Hard to do without expertise in the discussions.
- Challenge to assign tasks and define priorities.
- Author observed that the NFF rate must be on the scorecard.
- Setting up good visualization Per project, Program, Shift, and Testers. The team should use a systematic approach
- Evaluate the possibility to receive subscription DF dashboards.
- Evaluating the new criteria for analysis that if the product failed once should consider it into account for quality checking.
- Evaluating process to add tester's info with classification per segment, yield, test time, and including a ranking formula to help technical engineers and the NFF coordinator.

5.3.1 Information Flow

- NFF issues are not related specifically for a week, however, the process in detail is prepared by the author to report weekly.
- NFF coordinator will be suggested according to the program for each NFF. A responsible NFF coordinator should be appointed to delegate, follow up and implement the solution.
- Resource management (RM) is only on a needed basis: To participate in weekly NFF business reports, supporting the priorities, and Allocation of resources.
- Test data analyses (DA) should be responsible to facilitate and automate complex reports from different angles into simpler reports. Keeper of "NFF scorecards", "NFF improvement monitor" dashboard, and "On radar" dashboards.
- Product Quality engineers (QE) will check with the responsible NFF coordinator the status of the NFF solution proposed and implemented based on technical engineers (TE).
- Plan to have a tracking tool for checking the progress for NFF solutions with transparency.

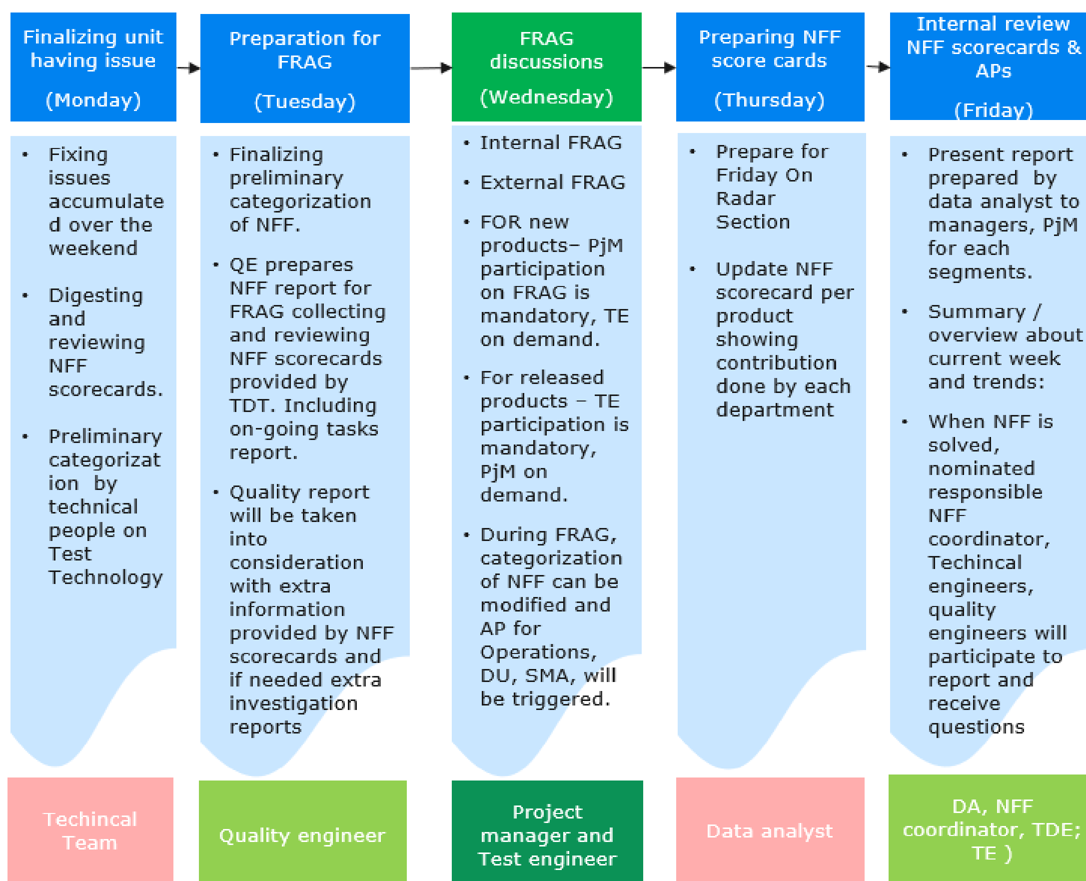

Figure 5.3.1 Draft version of wanted information flow for the week

Wanted position for information sharing that presentation from data analyst and NFF coordinator to be shared with all internal stakeholders like higher managements (LTs), Line managers (LMs), program managers (PMs), and project managers (PjM), etc [29]. Each segment/ program will define criteria for being on the radar. NFF (YwoR) will be on the project scorecard. The NFF coordinator will explain in detail all ongoing activities. On Friday, elaborated a top list with proposed high-level tasks to solve each NFF found should be present.

From the data point of view, TDT will prepare NFF scorecards as per the project and will classify preliminary NFF measurement points (MP) which should be described into 5 categories: Test SW, Test HW, Product HW, Operations, Environment, and Others. With the task planning tool (HS), it will be possible to observe weak cooperation between test departments and escalation will be considered in operations.

If any of the NFF will be solved, the responsible Quality engineer will participate to listen and comment on the root cause analysis done and its future impact. This is the suggested process.

5.3.2 NFF impacting with solution flow

The author has explained the weekly NFF process in detail for more clarification. The NFF process in detail. Please refer image below. The process is detailed and has been summarized by the author by selecting TOP NFF to solve it [30].

- Author has understood that to resolve issues where No fault-found case has been reported, RCA and transparency is a key to success.
- Independently of WoW adopted to solve the issue and the resources needed to be allocated, RCA (Root cause Analysis) is important to achieve success on it.
- A live template (one-pager) can be prepared to document conclusions and to create a database to help DAs/QEs to screen future NFFs
- It is concluded that from the priority perspective, first should be selected from the TOP, then define priority and the responsible person will be in a meeting with the program manager (PM) that can be held Monday or Tuesday, with the support of DA from the NFF Friday report.
- Invention of the task will be by mPjM and transparency with Hansoft is needed
- Implemented solutions will be stored for consultancy future.

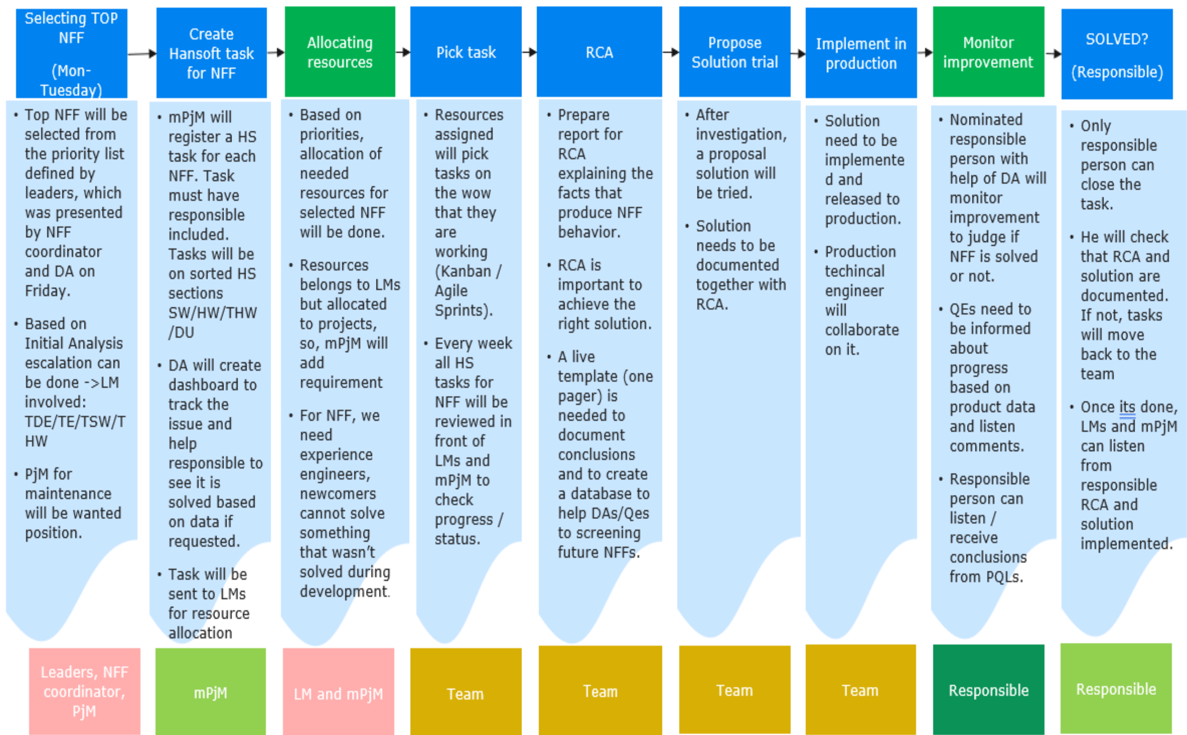

Figure 5.3.2(a) Detailed version of NFF process with responsibilities.

FRAG readiness; FRAG is introduced as a Fault rate analysis group, it is basically a group where the participants join to discuss the reason for faults. This group basically exists in manufacturing companies. Here author wants to put detail to explain what should be ready for the FRAG analysis, please refer to below image [31]

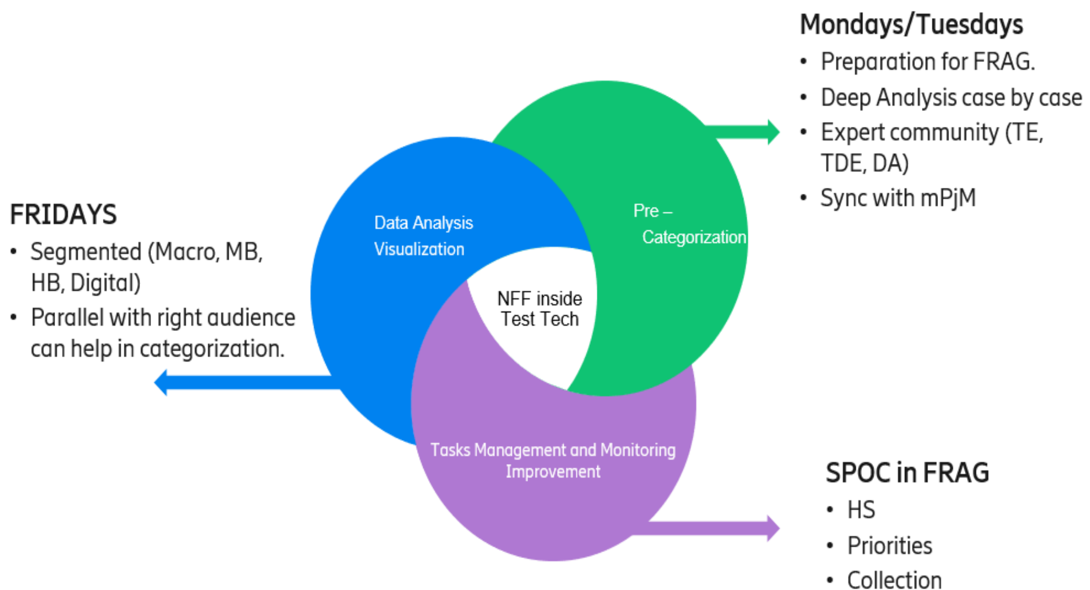

Figure 5.3.2(b) FRAG readiness

5.3.3 Project Updates

Decided

- Implemented Pre-FRAG discussions on the first two day of the week
- New Dashboards to help with Pre-FRAG based on PowerBI
- Set of Dashboards based on Tableau to track NFF and projects
- Draft of process.
- Positive feedback about participants on Pre-Frag.

Ongoing

- Author has investigated that generic quality report should have all clear information to use in FRAGs with info from PRE-FRAG/Categorization meeting
- Present the outputs to the leaders to visualize top-level NFF% trend, top 5 NFFs, attendance on Pre-FRAG, and project management tool metrics (tasks received, assigned, and done)
- Implementation of test station analysis tool
- Correlation related to components and multiple port NFF.
- Correlation between SW release and multiple port NFFs.

Facts and Risks

- Author analyzed that working on NFF is basically easy when the product is at a mature state however it is challenging to take NFF which is for unmatured products.
- Another challenge that the author wants to highlight is that it has challenged to consider NFF tasks with respect to new product development tasks. Usually, manufacturing companies have priority on NPIs
- During the investigation author noticed that a company should have a maintenance organization (Leaders and dedicated Res) to consider issues that occurred in matured products like NFFs.

5.4 Conclusion

During the research for NFF issues, the author has drafted a process which is further explained in detail version with the requirement. Overall the wanted position in the manufacturing companies is to have fix process to analyze the NFF issues. Another wanted position in companies is that root cause analysis solutions should be presented

in fix manner to track the issues to all stakeholders and the results need to be monitored to declare that the NFF case for the particular issue has been resolved or not resolved. If the above-mentioned process can be implemented in any of the manufacturing companies, overall [15]1 to 2% issues can be resolved every week and by tracking/implementing root cause analysis solution overall [16]2 to 10% yield will improve in next 3 to 6 month which will help to increase first pass yield and save retest time as well.

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[15] *The value mentioned is just estimation for the issues which can resolve with the suggested process, There is no any connection between these numbers to any company relevant data or product*

[16] *This percentage is calculated based on the value of clause 15.*

6. GAGE R&R

6.1 Introduction

The author thought to choose another topic to make the test system more stable and verified so that company can deliver the best quality to the customer. The Gage R&R process is to reveal the relative amount of variation that might be due to the manufacturing or testing system. According to the author, it is used to validate the measurement system concerning testing requirements. During the investigation, the author found that the gage R&R task is performed before releasing the system or for an immature product to make it ready for maturity. Gage R&R is basically performing the verification with Repeatability and Reproducibility.

One of the fundamental principles of Six Sigma is to reduce variation. As soon as variation is observed that causes some disturbance in a process, the root of the issue should be found and eliminate them.

"Is this variation due to actual flaws within processes, and products, or irregularities can be suspected in the way of measures, regardless of what tools are used?"

Gage R&R is a tool that examines what the variation consists of. It estimates how much is caused by the measurement system itself and what is due to the measured parts.

Some important terms for Gauge R&R studies

- Repeatability - variation within the instruments
- Reproducibility - variation between instrument
- Repeatability + Reproducibility = Total Gage R&R
- Total Gage R&R and Part-to-part sum up to 100%.
- For a good Measurement System and well-done Gauge R&R, the variance should be ≤ 10%, and part-to-part ≥ 90%.

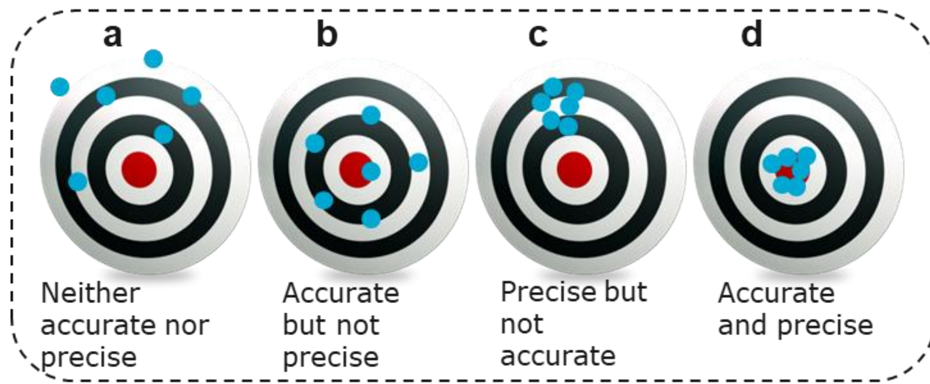

Figure 6.1 Gage R&R measurements

6.1.1 Measurement system and its terms

MSA stands for measurement [32] system analysis which is defined in two measurement terms, Accuracy and Precision. It analyzed that Gauge R&R is a part of MSA, where Gage R&R checks how consistent repeated measurements are, within each tool that is used for the measurement. The author asks you to remember one thing, Gauge R&R is all about variation. The tool doesn't say anything about how accurate your equipments are. For accuracy, you have to check outside the Gauge R&R process. With the Gage R&R process author wants to tell the difference between a/c or b/d (changes in variation), but not what's right between a/b or c/d (off position). A, b, c, and d are just terms to denote the object.

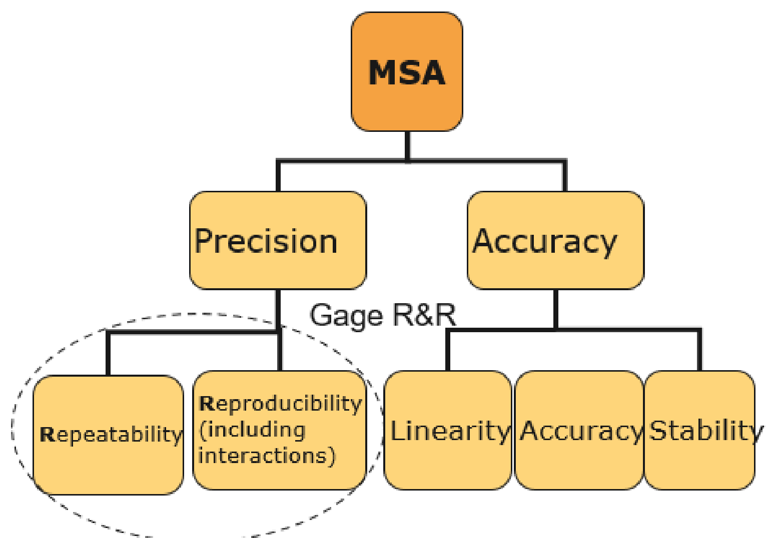

Figure 6.1.1 Types of Gage R&R measurement system

Here the author has explained the MSA terms with accuracy[33].

- Linearity checks during measurement analysis if deviations from true values are larger at one end of the scale than at the other end. A system without linearity problems can measure small and large values with the same accuracy.
- Accuracy is simply a measurement of how "correct" the system is. The difference between a true value and a measured value is an accuracy problem.
- Stability tells how well the system performs over time. Does the system have an issue when performing the same test on the same tool for the same functional test? To have a stable system, it should give the same accuracy tomorrow as it is today.

6.1.2 Analysis done by the author based on historical data

The study of Gage R&R measurements is done by tools that contain raw data, where is possible to see CPK analysis and Gauge Analysis per measurement point (MP) and the tool that can generate excel and graphs using the Mathematical suite. This is an example summary of the Gauge R&R study in the session window. Data from this window will be described in the graph. Typically, several test parameters are measured in parallel. They are evaluated one by one.

Table 3 Gauge R&R study

Source	**VarComp**	**%Contribution (of VarComp)**
Total Gage R&R	14.4545	87.04
Repeatability	11.3125	74.52
Reproducibility	1.4283	5.1
Instrument	1.7137	7.42
Part-To-Part	2.6330	11.59
Total Variation	17.088	98.63

For a good Measurement System, the "Total Gage R&R" variance should be ≤ 10%, and with a well-done Gauge R&R, the Part-To-Part portion should be ≥ 90%. General criteria

Table 4 General criteria

		Legend		
%Contribution	< 5	>=5 ... <= 20	....	> 20
%StudyVar	< 10	>= 10 ... <= 30	....	> 30
%Tolerance	< 10	>= 10 ... <= 40	....	> 40
Number of Distinct Categories	> 10	>= 4 ... <= 10	....	< 4

<10% - Acceptable

10% <= … <= 30% - Acceptable depending on the application, cost, etc.

30% < … Not Acceptable (should be improved)

In one of the research, it is evaluated that the above values are assigned to check if the measurement system is suitable to evaluate and if the parameter is lying between the limits and compared to Total Gage R&R contribution in %Tolerance. This evaluation is not fixed it is depending on the manufacturing company.
In the research, author find to explain that if you would like to check that the measurement system is suitable to evaluate your process variation, compare the total Gage R&R contribution in %StudyVar.

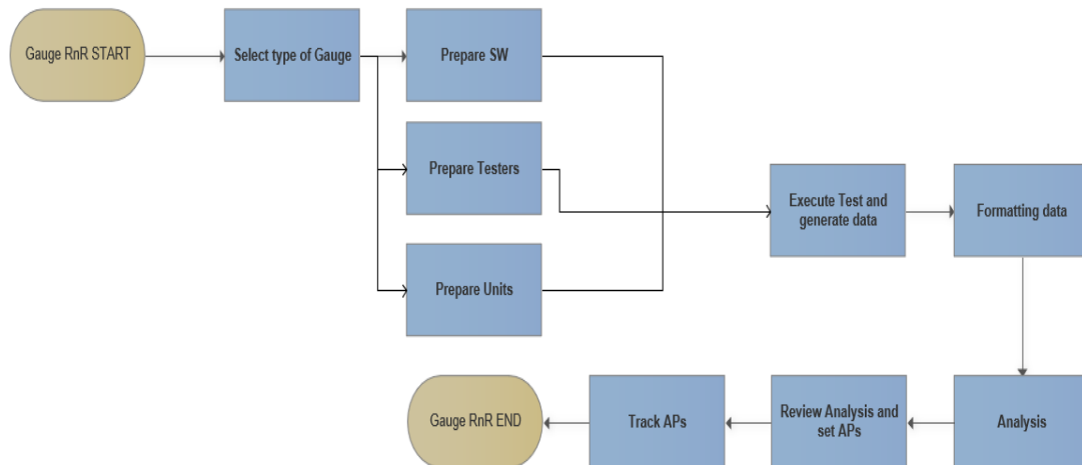

Figure 6.1.2(a) Author's wanted process for Gage R&R

Gage RnR is basically performed to check the variations [34] of the test. In the above process, the author tried to prepare the gage R&R process. Researchers analyzed that it is important to analyze what type of gage Author need to prepare and accordingly Software, testers, and a minimum of 10 products to perform repeatability tests. The author also wants to highlight that additionally, the repeatability test should not be performed by the same individual because some of the variations in results can be due to handling the product and testing system. Once preparation is done, testing will be performed with repetition and data will be formulated. The researcher has concluded that the test system will pass the gage RnR if the measurement data will lying between the test requirement, if in case the data will have different values and lying outside the product quality requirement that means that either SW is not stable or the tester is not the stable or worst case if the product is not stable. In such cases, further RCA will be performed. Below is the detailed version of the Gage RnR process.

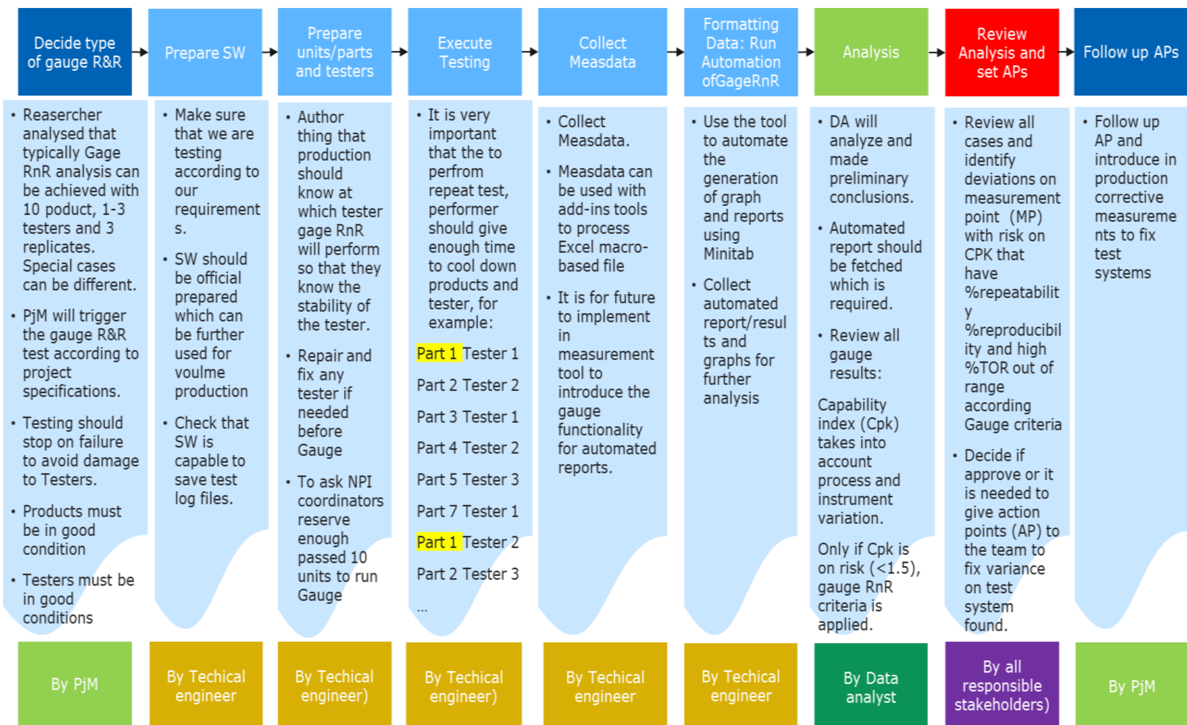

Figure 6.1.2(b) Gage R&R process with detailed responsibilities

Here author would like to write detail for stakeholder and governance according to his observations

- Gage R&R (GR&R) process owner – Line manager of process [35]
- GR&R measurement execution organization – Project managers
- GR&R measurement protocol preparation (SW, products, and Testers) - Technical Engineer
- GR&R measurement conduct - Technical Engineer
- GR&R measurement visualization/formatting (preparation for analyses:) - Technical Engineer
- GR&R analysing - Data Analyst
- GR&R approval will be handled by the team in the meeting, stakeholders are Data Analysts, Technical Engineers, Test Developers, Quality Engineers, Product Engineers, PDU, and PjM (depending on the project
- Result storing will be done
- Action point follow will be done after the result of the gage R&R will be presented, PjM task will be to follow up the results for future.

6.1.3 Analysis performed with help of technical engineers on Gage R&R

- The first graph (figure 17) is checking % StudyVar (SV) and %Tolerance and Part to Part. The measurement system should be ≤ 10%, and part-to-part ≥ 90% and %Contribution is reflecting STdev
- Analysis for graph 2, Range is the distance between the smallest and largest value. The author should get a range value for each part–tool combination

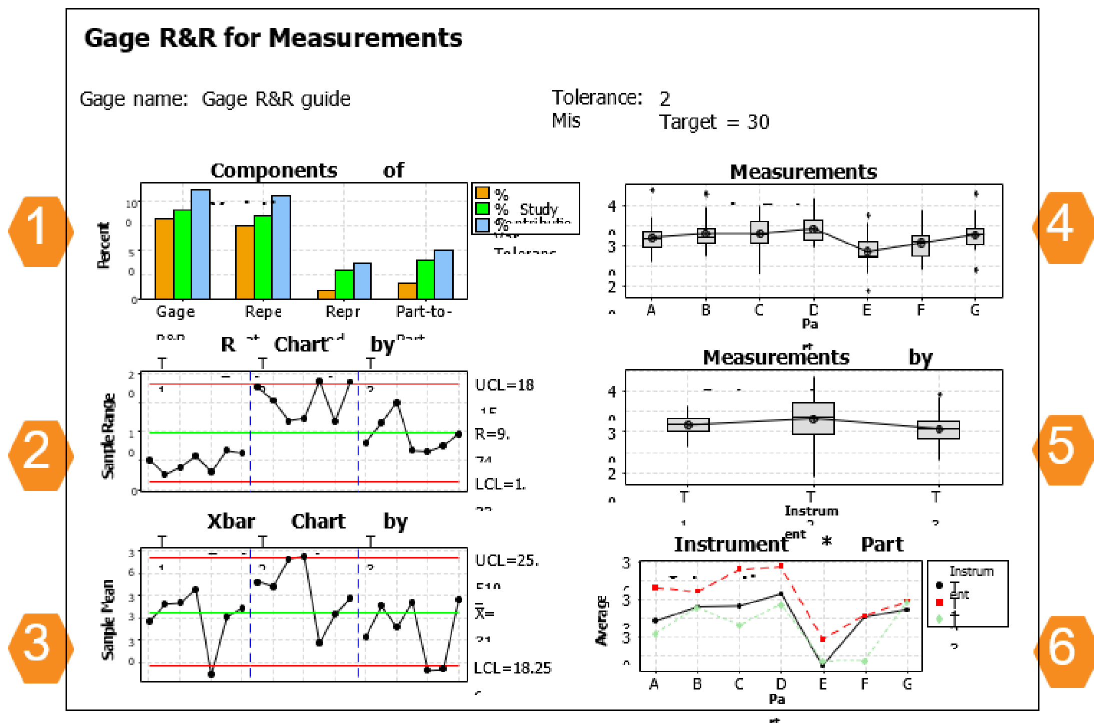

Figure 6.1.3 Measured values for Gage R&R

- For graph 3, as in the above subgraph here, the values are mean values. Check if some Instrument has strange behaviour [35].
- For graph 4, check if some part has strange behaviour.
- Graph 5 tells that the horizontal line should be as flat as possible (equal mean values), otherwise there's some problem with reproducibility.
- Graph 6, the different levels are not important. It should consider from deviating patterns.

IMPORTANT, In gage R&R variation exists but can be acceptable!

- Cpk takes into account process and instrument variation.
- Only if Cpk is on risk <1.5, gauge RnR criteria is applied

6.2 Conclusion

The researcher has studied the gage R&R process and analyzed the missing factors in the existing process. The author has shared the draft version of the process for further implementation. According to one of the investigations that if gage R&R will be performed it will reduce the faults which will occur due to instability of the test and production system which will be approx 1 to 4%(data is calculated by plotting results from different companies already added to the research papers). It is also that we gage R&R is not performed on any product which will lead to more faults in mass production. Here are a few important points which researcher wants to highlight in this research

- Analysis must consider variation and CPK. Designers' units and NPD organization must be reported.
- It is important to secure the condition of Testers/Nodes before expending too much production precious time.
- Test domain must be known and informed to the technical engineer because some variables present variance.
- Precision cannot be guaranteed with a gauge analysis.
- Why does the author want the parts to have "high" variation? The answer is the key to understanding what Gage R&R is. A perfect system has no variation. So, if you can measure all small variations with high accuracy between the items you have an adequate system. Also, "high" variation between parts is only relatively speaking. You may have excellent parts, but the system should be better and be able to tell them apart [36].
- Author's suggestion, in order to avoid inaccurate product variation, pick tested and verified items/products randomly, 10 or more, and tester 1-3 as per preferences (This number is depending on the company to company based on products they produced).
- Author's point of view on this is to make the evaluation work you need to pick items that represent the normal spread amongst your produced items. You cannot hand pick the most perfect and equal items to be part of the Gage R&R, otherwise, you falsely accuse the system of having larger variation than it has. Gage R&R isn't about absolute values, but relative values, i.e., system variation relative to part variation.

7. STRESSING THE PRODUCT UNDER DIFFERENT TEMPERATURE

7.1 Introduction

The author analyzed that to improve product quality different stress can be given to the product to verify its capability in a field where the product must work in environmental conditions like temperature, wind, rain, etc. With this analysis, the author thought to investigate the condition and requirements of the products that will be stressed under high and low temperatures. In this investigation, idea is to implement temperature on the product to detect components' stability and quality in production to check if the product is able to qualify for temperature conditions or not. According to the author if the product can pass the condition at production before delivering to the customer it will reduce the risk of product failure and the customer would be satisfied with our deliveries as he will receive a more qualified product. Basically, in short, it will be the reliability test of the product where the product should perform a required function successfully under specified environmental conditions for a specific period of time. The purpose of the reliability test is

- Identify product weaknesses.
- Reduce the likelihood problem
- Ensure customer satisfaction
- Improve product quality

In this study, the author will bring the conditions and options available globally to stress the product under high and low temperatures. Considering the factors, here the main analysis will be on stressing the product at highly accelerated stress test, HAST and highly accelerated life test, HALT. Which will monitor manufacturing and prevent any defects from being introduced during the process. Based on the product functionality limits determined from (HALT) and a discovery test as opposed to a compliance test to reveal the weakness in the system/product design and manufacturing in a relatively short time by subjecting test products beyond their specification limits.

7.1.1 Reliability introduction

In the reliability process, we have 4 main areas where reliability tests can be performed.

- Component reliability performed at supplier: This reliability test is performed on the component level which will be able to find black boxes, issues in small mechanical, batch problems and specification ambiguity, etc.
- Reliability test performed at the factory: This reliability test is performed on the final product level which will be able to find the issues that occurred because of production process changes, HW/SW updates, workmanship, test instability, and product process capability, etc.
- Reliability at design end: This reliability test is performed at the design level which is to find the issues at the DFM level, when design/release changes, and design margin, etc.
- Reliability test performed at the customer: This reliability test is performed at the customer level which will consider the issues that occurred by capability, competence NFF, claim/repair data accuracy and site environment, etc [37].

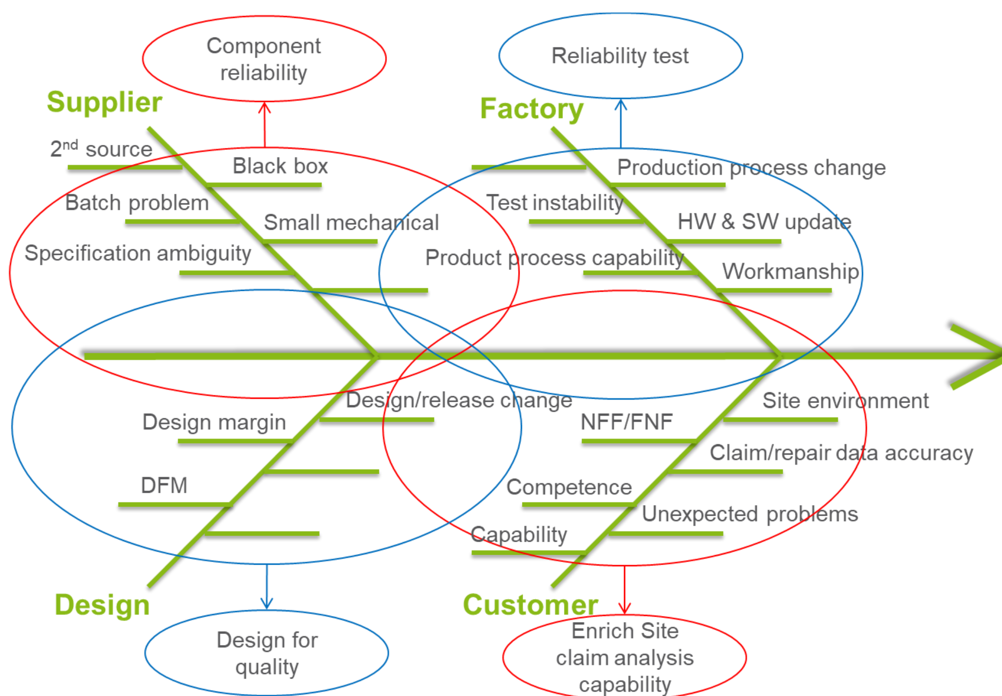

Figure 7.1.1 Reliability introduction

7.2 HALT

According to author's analysis, the HALT test will be stressing the product under high and low temperatures and can also include a rapid thermal cycling test. It will be to find

our potential weakness of the product during the new product development and once all RCA has done on the weakness found, the best product will be delivered to the customers. The test will be followed by these steps

HALT → Failure → Analysis → Improve → Re-HALT → Product limitation

Steps performed for the HALT test

- Step 1: Cold test
- Step 2: Hot test
- Step 3: RTC (Rapid thermal cycling) test
- Step 4: Vibration test
- Step 5: Combined (RTC + Vibration) test

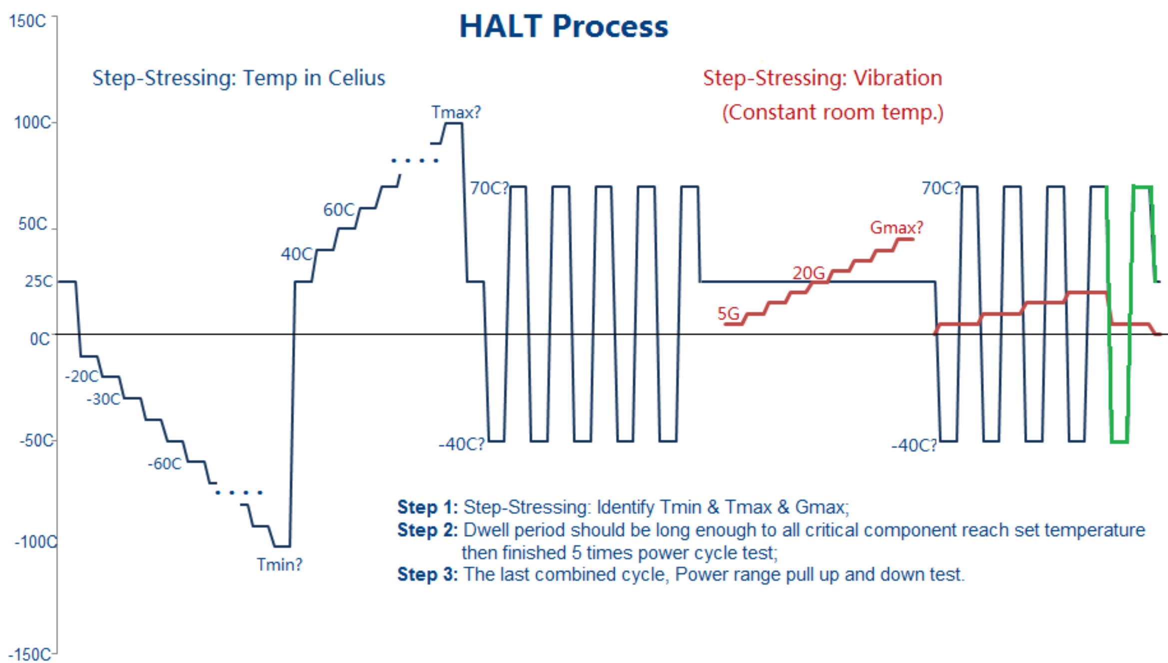

Figure 7.2 HALT process

7.2.1 HALT; Stimulation vs. Simulation

Stimulation

- Qualitative Highly Accelerated Life Testing [38]
- Identify failure modes
- If tests are not designed properly, the product could fail due to modes never encountered in real operation

Simulation

- Quantitative Highly Accelerated Life Testing
- Quantify product life under normal use conditions
- Consider frequency and duration of operation, extreme conditions, and transient operation
- Simulate the entire product lifetime in a short period of time.

7.3 HAST

Now, the author would like to put focus on the HAST test which is based on the sample and should be performed when production produces high volumes to check potential failure which was limited by HALT. In another investigation, it is found that HASS can also be used for volume production to check 100% screening tests.

The below process for the HAST shows the steps after the test for the first HAST failed. It shows what resources are needed at what steps, for more detailed explanation please follow the below process for the HAST [39].

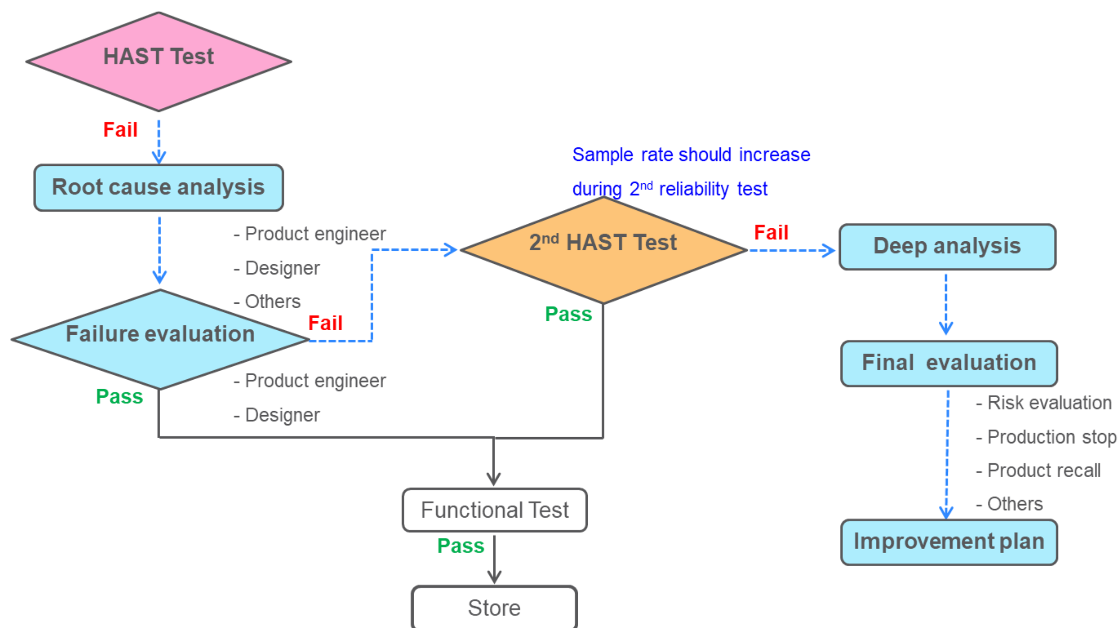

Figure 7.3 HAST process

7.4 Motivation to have HAST and HALT

- Reduce claims, failure rates, and NFF.
- Predict and eliminate modes of failure and identify problems at an early stage.
- Analysis for intelligent adjustment of product parameters (such as calibration curves) and test cases.
- Investigate claims and support root cause analyses.
- Reduce time to market.
- Quick testing and verification of failure modes and design changes.
- Capability to support PDU and PTDT with testing, design, and analysis.
- Increasing internal and external (customer) demand for more rigorous and advanced testing and analysis[40].

7.5 Measurements for the thermal chamber

Here below is the information for high accelerated chamber combining temperature and vibration to keep product for a day in high temperature (Dry heat normal condition+5x℃) [37].

Figure 7.5 Thermal chamber

- Use a walk-in chamber.
- Board temperature: 3~5°C below Normal High temperature
- Module environment with product
- Sample size should be defined
- Temperature range: -100 ~ +200 °C
- Temperature change speed: 60 °C /minute
- Vibration: 6 Degrees of Freedom, Random,5~60 Grms (10~5000Hz)
- Size: 1.65 M3 (W: 1.366, H: 0.879, D: 1.372m)
- Table capacity: Recommended 600 lbs (272.16kg)
- Application: Component, PCBA board, Module, etc.

Table 5 Cost/Expense

Equipment	Description	Quantity	Unit Price with tax(SEK)	Price with tax(SEK)
Chamber	16m3 walk-in chamber, W2.6m×D2.8m×H2.2m	1	1,267,200	1,267,200
Rack	W600mm*D800mm*H1500mm	4	990	3,960
Testbed shelf	W600mm*D800mm*H1500mm	1	990	990

7.6 Conclusion

The reliability test is a process where issues can be found at any stage of the product. Here in this chapter author has studied HALT and HAST reliability tests which are performed by stressing the products under high-low temperature conditions. Overall product quality will be improved from 1 to 3% by HALT and 1 to 3% by the HAST test. In the above investigation author mentioned about thermal chamber specification, it is only for study purposes to present what the thermal champer used for HALT and HAST looks like. The total budget to implement HALT and HAST is raised by 25 to 40% of the overall cost of the project, including all the following equipment and materials.

8. STRESSING TEST BY LOOPING PRODUCT TO SECURE STABILITY OF THE TEST SYSTEM

8.1 Introduction

The researcher has analyzed a tool or software that automates the looping of tests. Its main function is to perform a complete test and cool down the product. The SW will be able to loop it continuously or a certain number of loops defined by the user. It can loop test during day shifts, night shifts, or weekends depending on the user. This tool does not need any manpower to stress and retest the product. This is basically to launch a machine/SW which start the test automatically and repeat until the predefined condition or it will be stopped by an engineer if required, additionally, it will be giving the flexibility to define time interval to cool products between testing loops.
The author would like to give the name of the tool *CLOCK LOOP test which is also called STRESS TEST HW and SW solution loop*. This loop concept will help in the following

- Find issues in HW/SW with the continuous test.
- Automate verifications for SW.
- Identify issues in certain Test Measurement point if it has good Repeatability and Standard Deviation.
- Reproduce issues/problems that only occur in production scenarios and resolve/fix them before releasing the Test Solution to Production
- Make the testers automatically ready for testing in software terms.

8.1.1 How STRESS TEST HW and SW solution works

- Configure the test with what serial, test type, and a number of loops to use.
- Run the SW and leave it running.
- Wait for it to end or you can abort the test loop.
- After ending the loop, the test has been performed and a lot of data to analyse further, debug, and resolve for better release of a stable test solution will be produced.

8.1.2 Tactic with Stress test HW and SW solution/clock-loop

- Guarantee quality of Test SW solution to identify instabilities.
- Stress test HW and SW solution can run in any tester on having a test manager.
- It can run on all products.
- It can primarily be used for further investigations of instabilities identifications.
- During analysis, it will be possible to identify products and/or test cases that it wants to test more, and these products will be brought to stress test HW/SW solution. Test data will be available in the test record database, so it expects these data to be further analysed by engineers.
- It will be generating an action point and set responsible engineer to make sure that the efforts are not wasted. Stressing the product can be stopped for specific cases when an engineer will say so, after that the next case will be selected, and so on.

8.1.3 Advantages for stressing test HW/SW solution in tester inside test SW release

- Find issues in HW/SW with the continuous test.
- Stress Test to secure the stability of Test Solution and yield.
- Automate verifications for SW and HW.
- This solution is a part of the release test software process to guarantee quality test software, here is the process for putting the product to check stability into the loop [41].

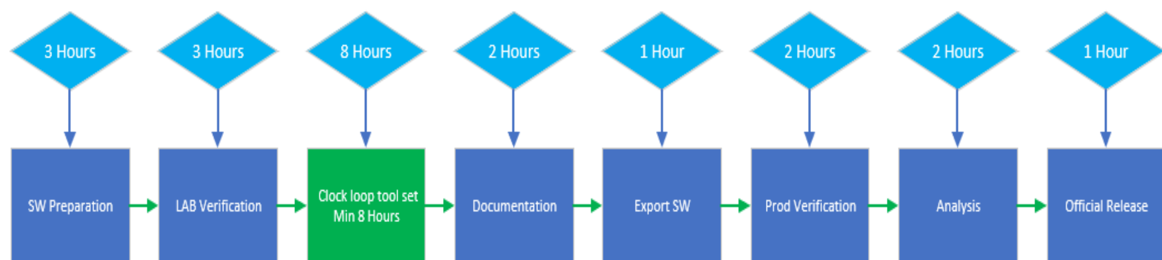

Figure 8.1.3(a) Process of stressing test HW/SW solution

This process is the detailed version of the stressing test HW/SW solution/CL test with continuous integration [41] is below

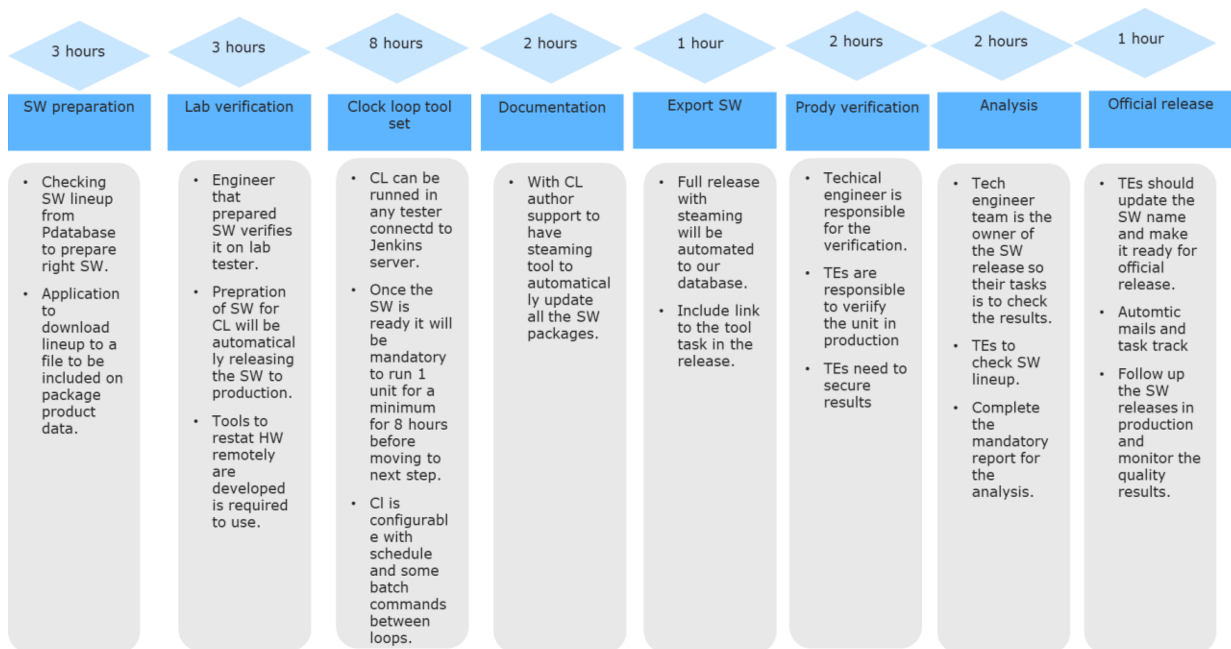

Figure 8.1.3(b) Process of Clock Loop with detailed responsibilities

8.2 Problem addressed

The clockloop machine's main target is to stress the unit to check hardware and software issues by loop test of the product. The researcher analyzed the wanted position from Clock-Loop Tool.

- Operations with CL must be easy for engineers.
- Test Cases for CL should be prepared automatically based on an existing test case to be released.
- Possibility to program scheduled time (nights and specific days).
- Possible to receive automatic emails related to your CL job programmed.
- With CL you can leave the product connected with the tester, program it and forget. You will receive an email that your job was finished.
- Clock-Loop tool can be used here to get data for Gage R&R to check the stability of the test system.
- The CL tool will continuously be finding the issue in HW and SW.
- Reduce time if not eliminated for TDE in setting up and performing loop testing manually.
- Improve SW Quality by catching intermittent failures that is currently hard to reproduce in lab setup.

The following shows how engineers can let the machine does its job unattended in a (24 Hrs) day scenario.

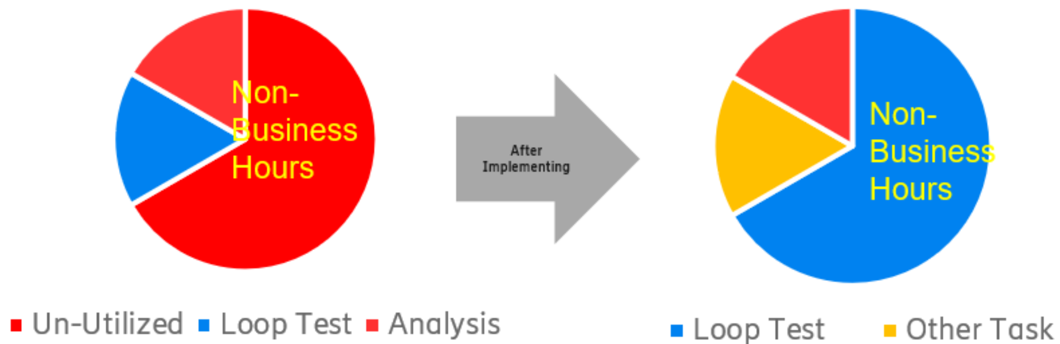

Figure 8.2 Measurement of machine performance in 24 hours

8.3 Process for Clock-test loop

The Clock loop machine performs a complete platform Test with a cooldown process by stressing the product in a loop and is able to loop it continuously or a certain number of loops defined by the user. The CL can manually start when the user decides to. It can also start automatically by schedule as defined by the user.

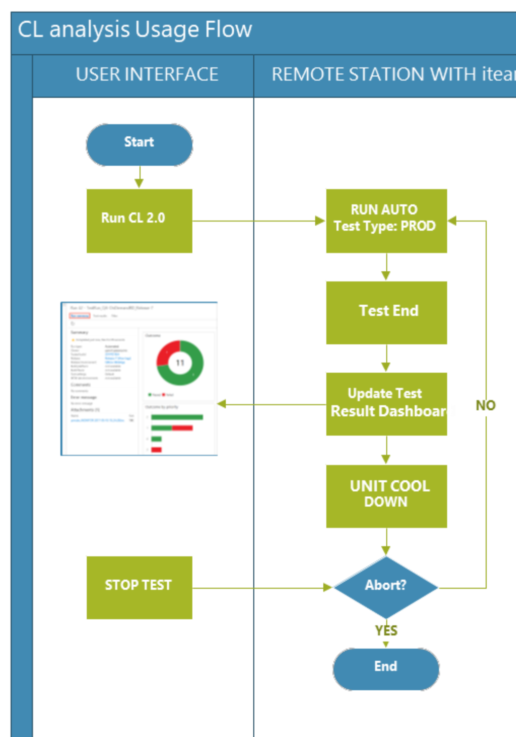

Figure 8.3 CL analysis user flow

While it is running, a dashboard is available that monitors it in real-time. The Dashboard shall consist at least of Test Times and Pass/Fail Results. The Test ends when the user aborts it while it is running or when it reaches it loop limit. Finally, an alert email is sent to the user that CL has ended with a summary of the Test Results.[42]. KPIs are written down below

- Reduce technical engineers' loop-testing tasks. This will further convert to cost reduction.
- Improve yield by addressing captured potential intermittent failures.
- Reduce return rate failures.

8.3 Conclusion

The author has concluded that the clock loop machine is the best improvement activity which will be done by stressing the product multiple times to check its functionality. Automating the clock loop will reduce the manual testing performed by the engineers and which will lead to less manpower requirement. The author investigated that by stressing the products in the loop, potential intermittent failures will be captured and sent for root cause analysis before moving the product to a mature state. Once the product quality will be improved, it will lead to the reduction of failed returns from the customer.

SUMMARY

In the summary of the thesis, the author would like to mainly point out the areas where research has been done and improvement has been analyzed. In the summary, improvements/observations/proposals have been briefly written down. Note that all the numbers mentioned are estimations.[17]

Chip/component quality test In this test overall result, if the authors received prequalified and verified electronics components before assembly, they will save 10 to 120 USD per product, which represents a cost reduction of 2% to 7%.

Programming at chip/component level In this case, the author has analyzed two options available for programming systems which are BPM 4910 and BPM 3928 from one of the manufacturing companies. As a result of this implementation, functional tests at the manufacturing site will take 3 to 7 minutes longer and yield will increase by 1 to 2%.

Formal verification of SW Main investigation done by the author on this case is to conclude why formal verification of SW is important. According to the author, this verification is critical to make a stable SW that means that the measured values of the produced product on the SW should meet the test requirement. If in SW verification, the values are not according to the test requirement of the product it means that the either produced product has an issue or the test requirements are not clear.

PCB level test The author has concluded that with PCB tester implementation in the manufacturing site, approximately 50 to 450 USD cost can be saved only by saving disassembly and assembly time. There is a potential to improve overall yield by 1% to 6% without repairing. Alternatively, scrapping costs might increase by one to four percent of the total scrap. The author has concluded that a manufacturing company named Columbia made the best proposal for PCB testers.

No-fault found (NFF) The author concluded that if the proposed process in the NFF section will be implemented in any of the manufacturing companies, with a weekly resolution rate of 1 to 2%, implementing root cause analysis solutions will lead to an

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[17] *All the numbers mentioned in the thesis are for research purposes only. The values do not have any link to real data or any specific manufacturing company. The numbers are calculated by plotting different data from different references and mean values is considered in this thesis.*

overall improvement of 2 to 10% yield in the next 3 to 6 months, thereby increasing first pass yield and decreasing retest time.

Gage R&R As a result of one of the investigations in the Gage R&R study, the author concluded that if gage R&R is performed, the number of faults caused by unstable test and production systems will decrease by approximately 1 to 4% (data derived from plotting results from different companies already included in the research papers)

Stressing products under environmental conditions In this study, the author investigated the reliability tests known as HALT and HAST, which stress the products under conditions of high-low temperature. By using HALT and HAST tests, overall product quality will be improved by 1 to 3%. All equipment and materials necessary for the implementation of HALT and HAST are raised by 25 to 40% of the overall project budget.

STRESS Test HW and SW solution As a result of stressing the product multiple times to check its functionality, the author recommends upgrading to a clock loop machine as the best improvement activity. A clock loop that is automated will reduce the need for manual testing by engineers, thereby requiring less manpower.

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APPENDICES

The Appendices and supporting information for the Six sigma approach of using DMAIC can be followed by below link https://asq.org/quality-resources/dmaic

The Columbia webpage can be followed by https://www.columbia.se/