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# **FORMULA STUDENT GROUND SPEED RADAR**

Master's thesis

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TALLINNA TEHNIKAÜLIKOOL  
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# **TUDENGIVORMELI KIIRUSRADAR**

Magistritöö

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doktorikraad

Tallinn 2018

## **Author's declaration of originality**

I hereby certify that I am the sole author of this thesis. All the used materials, references to the literature and the work of others have been referred to. This thesis has not been presented for examination anywhere else.

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06.05.2018

## **Abstract**

In this thesis, a ground speed radar was developed for use in a Formula Student race car. The radar was required to measure car speed at frequency of at least 100 Hz, with 1 km/h resolution, up to 120 km/h maximum speed, in both longitudinal and lateral axes. A device was developed that went under the car. It featured 2 24 GHz continuous-wave Doppler radars based on BGT24MTR11. The radars measure speed in both axes by measuring Doppler frequency shift in radio waves reflected from the road surface. A high gain microstrip patch antenna array was developed and simulated in HFSS. The doppler radars are assisted by inertial measurement unit. The radar and the inertial measurement unit data is gathered by STM32F767 microcontroller. From it, the vehicle speed is calculated and broadcasted via CAN bus.

This thesis is written in English and is 48 pages long, including 5 chapters, 43 figures and 11 tables.

## Annotatsioon

### Tudengivormeli kiirusradar

Käesoleva magistritöö eesmärk on arendada radar, mis mõõdaks tudengivormeli auto kiirust. Radar asub autos ja peab olema võimeline mõõtma kiirust sagedusega vähemalt 100 Hz, resolutsiooniga 1 km/h ja kuni 120 km/h kiiruseni nii piki- kui ka külgsuunas. Lõputöö käigus arendati välja nõuetele vastav seade. Seade põhineb kahel 24 GHz pidevlainelise Doppleri radaril. Radarid on paigaldatud nii, et nende vaheline nurk on 90 kraadi, kuna selline asend lubab mõõta kiirust mõlemas suunas. Kõrge 24 GHz sagedus on valitud, et vähendada antennide suurust ja suurendada Doppleri sageduse muutust. Lisaks arendati radaritega kasutamiseks eraldi *Microstrip patch* antennivõre. Võre koosneb neljast elemendist ja iga radar kasutab 2 sellist antenni, üht signaali saatmiseks ja teist signaali vastuvõtmiseks. Väljaarendatud antenn on 77% efektiivsusega, tema tippvõimendus on 12.82 dB ja *S11* kesksagedusel -14.33 dB. Arvutused näitasid, et ainult radarist ei piisa 100 Hz sagedusega kiiruse mõõtmiseks. Võendamissageduse tingimuse täitmiseks kasutab seade lisaks radaritele ka inertsiaalandurit, mis koosneb neljast MEMS kiirendusandurist/güroskoobist. Andurid mõõdavad sõiduki kiirendusi erinevate telgede suhtes, mille järgi sõiduki kiirus on hinnatud radarite mõõtmiste vahel. Radarite andmetöötluse funktsioone täidavad kaks BGT42MTR11 mikroskeemi. Kogu kõrgsageduslik signaalitöötlus toimub nende sees. Doppleri sagedust võimendatakse kesksageduse võimendi abil ja pärast seda mõõdetakse signaali STM32F767 mikrokontrolleri abil. Mikrokontroller arvutab välja auto kiiruse kasutades infot radaritest ja MEMS sensoritest. Kiirus on saadetud 100 Hz sagedusega auto CAN bus võrku ja salvestatud ka SD kaardile. Seadme mõõdud on 86.4 mm x 68.4 mm x 20.2 mm ja ta kinnitub auto alla kerekonstruktsioonide külge võimalikult auto massikeskme lähedale.

Lõputöö on kirjutatud inglise keeles ning sisaldab teksti 48 leheküljel, 5 peatükki, 43 joonist, 11 tabelit.

## List of abbreviations and terms

ADC	Analog-to-digital converter
BOM	Bill of materials
CAN	Controller Area Network
DC	Direct current
EIRP	Effective isotropic radiated power
ESD	Electrostatic discharge
FFT	Fast Fourier transform
FIFO	First in, first out
FM	Frequency modulation
GPS	Global positioning system
HFSS	High frequency structure simulator
IF	Intermediate frequency
IMU	Inertial measurement unit
ISM	Industrial, scientific and medical
LED	Light-emitting diode
LNA	Low-noise amplifier
LO	Local oscillator
MEMS	Microelectromechanical system
PCB	Printed circuit board
PLL	Phase-locked loop
RC	Resistor-capacitor
RX	Receive
SD	Secure Digital
SPI	Serial peripheral interface
SRAM	Static random-access memory
SWD	Serial wire debug
TX	Transmit
UART	Universal asynchronous receiver transmitter

VCO

Voltage-controlled oscillator

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# 1 Introduction

The purpose of this project is to create a precise and quick ground speed sensor for Formula Student Team Tallinn.

Formula Student is an international engineering competition where each year students must assemble a team, design and construct a racing car and compete with other teams.

Traditionally cars use wheel speed encoders to measure speed. This approach works well in a situation where some of the wheels are not driven, such as the common rear-wheel drive. To accelerate with maximum efficiency, driven wheels must rotate at speed approximately 9% higher than vehicle's ground speed. Our team's car has all-wheel drive which means that there is no way to reliably measure ground speed.

Several solutions were evaluated previously. GPS has low precision and update rate. Several accelerometers were installed on a car. They proved to be good, but they accumulated error with time. Ground-tracking camera was tested and showed excellent performance but was very sensitive to weather conditions. Finally, ground speed radar was proposed, and it is the topic of this thesis.

The ground speed radar must meet the specifications listed below.

- Determine vehicle speed in both lateral and longitudinal axis.
- Have speed resolution of at least 1 km/h.
- Have a top speed limit of at least 120km/h.
- Transmit speed readings via CAN bus every 10ms.
- Be as lightweight as possible.

Determining speed in longitudinal axis is the most important function of the sensor. It is used to control wheel slip. Lateral speed is currently not used, but there are plans to implement stability assist in the future and then it will be useful.

Speed resolution and limit come from the nature of the competition. Top speeds are limited by track design.

On-board computer's control loop runs at 100Hz frequency, this sets the 10ms speed reading update rate requirement.

The project involves designing and manufacturing the radar ground speed sensor, as well as writing software for it. This thesis focuses on the hardware design only.

The thesis consists of 3 chapters. "Theoretical background" provides essential information on measuring speed with radar. "Architecture" provides a high-level hardware overview and explains main components choice. "Hardware design" provides detailed description of a hardware design procedure.

## 2 Theoretical background

Radar works by sending radio waves towards an object and measuring the reflected waves. When an electromagnetic wave reflects off a moving object its frequency is shifted according to equation (1) [1]

$$f_d = \frac{2 \cdot f \cdot v_r}{c} \quad (1)$$

where  $f_d$  is the doppler frequency shift,  $f$  is the initial frequency,  $v_r$  is the radial speed of a moving object and  $c$  is a velocity of propagation (light speed).

This effect can be utilized to measure the speed of a moving vehicle by solving the above equation for the speed; other parameters are either constant or can be measured.

There are several types of radars that can be used for measuring speed. This project uses continuous wave Doppler radar because it has very simple concept. Basic Doppler radar circuit is shown in figure 1.

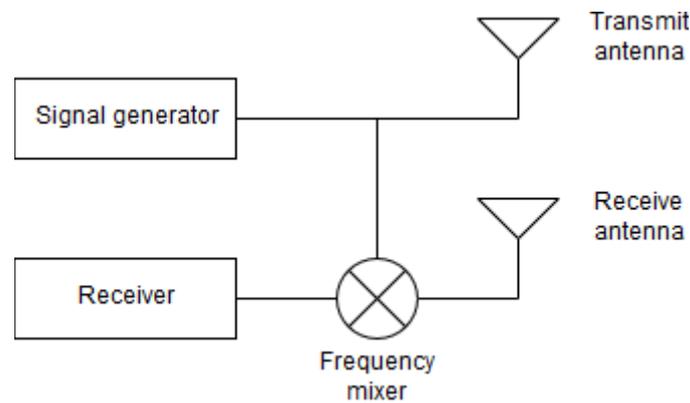


Figure 1. Basic doppler radar.

In Doppler radar, signal generator generates harmonic signal with frequency  $f$  which is then radiated into space from a transmit antenna. Once transmitted signal is reflected by some distant object, it is picked up by receive antenna. If the distant object is moving, the frequency will be shifted by a Doppler frequency  $f_d$ , so that the resulting frequency will be  $(f + f_d)$ . Both  $f$  and  $f_d$  are multiplied in a frequency mixer, resulting in two output frequencies:  $|f - (f + f_d)| = f_d$  and  $|f + (f + f_d)| = 2f + f_d$ . As can be seen, first

frequency equals Doppler shift frequency. Second output frequency is useless and can be easily filtered out because in a practical application  $2f$  term will be large. [2]

Higher operating frequency is preferred for 2 reasons. First, high frequency antennas are small, which is a definite advantage in a racing car where weight is important. Second, higher transmit frequency results in a higher Doppler frequency. This allows higher update rate because multiple signal periods needed to measure the frequency reliably fit in smaller time frame.

If the velocity is low, Doppler frequency will be low too. This limits the update rate at lower speeds. Due to that, additional speed measurement technique must be used in addition to the radar. In this project, radar is assisted by accelerometer data.

## 3 System architecture

### 3.1 Device location and orientation

Typically, car radars are installed in front or rear bumpers. For speed-only measurement, these locations are good when only longitudinal velocity is needed and the car has a large turning radius. Due to specifics of the Formula Student competition, cars have short wheel base with nose protruding almost 1 meter in front of wheels. This creates high lateral velocity for objects mounted on the nose when the car is turning. If a speed-measuring radar is placed in the nose, the high lateral velocity, even when compensated mathematically, may cause a significant error.

Back of the car does not have this issue but mounting the radar there was not considered because the back plate is detachable on most Formula Student cars to allow battery pack removal, and there are other components mounted there already.

Since lateral velocity measurement is needed, good location for a radar would be below the car near the center of mass.

To keep the project simple, no electronic or mechanical beam steering is used. To get both longitudinal and lateral velocities, 2 separate radars are used, mounted  $90^\circ$  relative to each other.

Figure 2 shows the radar location on the car model as well as beam directions for both radars.

Each radar antenna is mounted  $45^\circ$  relative to longitudinal axis. This is done to improve lateral velocity measurement. Since lateral velocity is most often expected to have small numerical value, Doppler frequency will be small too, requiring long time window to measure it. When both radars are mounted at  $45^\circ$  angle, some frequency is always present on both radars and time window for the frequency measurement can be small.

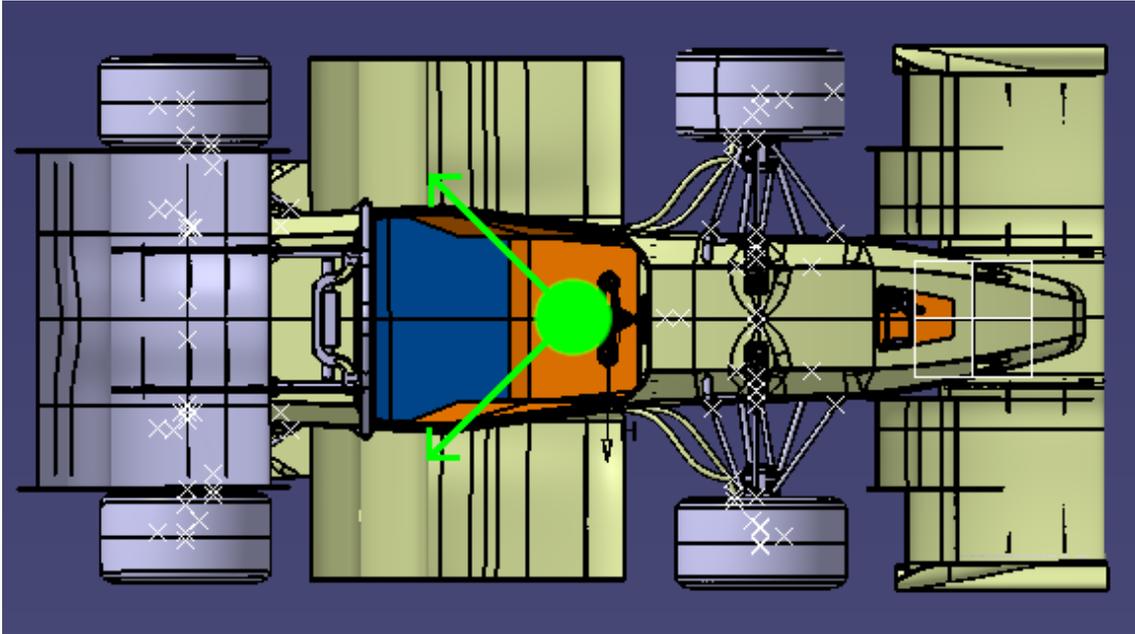


Figure 2. Radar position in the car (green dot) and beam directions (green arrows)

### 3.2 Radar

Several companies provide solutions for automotive and industrial radars. Notable products are 77GHz mmWave Sensors from Texas Instruments such as AWR1642, TEF810X from NXP and 24GHz BGT24 series from Infineon.

BGT24MTR11 from Infineon was chosen because it was widely available at the time this project was developed. It has all building blocks necessary for a Doppler radar – signal generator, mixer, LNA - in a single chip which will significantly simplify development. Its internal structure is shown in figure 3.



$$f_{d\ 1km/h} = f_{d\ max} \cdot \frac{1\ km/h}{120\ km/h} = 22.47\ Hz \quad (4)$$

Minimum FFT length  $N$  rounded to nearest  $2^n$  integer necessary to give such resolution at a sampling frequency  $f_s = 2f_{d\ max}$  will be

$$N = \frac{f_s}{f_{d\ 1km/h}} = 240 \approx 256\ points \quad (5)$$

At the sampling frequency  $f_s = 2f_{d\ max}$ , such measurement will require to sample signal for time  $t$  equal to at least

$$t = \frac{N}{f_s} = \frac{256}{2 \cdot 2.70\ kHz} \approx 47\ ms \quad (6)$$

Of course, in real life the sampling frequency and FFT resolution must be higher to reliably provide 1 km/h resolution. With  $f_s = 8f_{d\ max}$  and four times the FFT resolution, the FFT length will be

$$N = \frac{8 \cdot f_{d\ max}}{0.25 \cdot f_{d\ 1km/h}} = 3840 \approx 4096\ points \quad (7)$$

And the time needed for signal sampling will be

$$t = \frac{N}{f_s} = \frac{4096}{8 \cdot 2.70\ kHz} \approx 190\ ms \quad (8)$$

These numbers show that to achieve 10m/s speed update rate, radar alone can not be used and must be assisted by other device such as an inertial measurement unit.

Another important radar parameter is its maximum working range. The range is set by equation

$$R_{max} = \left[ \frac{P_t G A_e \sigma}{(4\pi)^2 S_{min}} \right]^{1/4} \quad (9)$$

Where  $P_t$  is transmitted power,  $G$  is transmitting antenna gain,  $A_e$  is the effective area of the receiving antenna,  $\sigma$  is target cross section and  $S_{min}$  is minimum detectable signal. All these parameters except for the target cross section can be chosen by a radar engineer. In this project, speed is determined from the radio waves reflected off road surface. Target cross section is dependent on how different road surfaces reflect radio waves. Since finding this out seems to be complicated task, a different approach is taken.

Instead of determining target cross section, we look at available products to estimate if 11dBm of power radiated by the BGT24MTR11 is enough to perform the task.

Infineon's Distance2Go radar demo kit based on BGT24MTR11 is a good example. Its transmitter has EIRP of 21 [4], which consists of 11dBm transmitter power, 2dB of cable loss and a high gain 12dBi antenna. Receiver, in addition to the LNA inside the BGT24MTR11, has an additional IF amplifier which provides either 34dB or 64dB gain, depending on configuration. Receiver uses high-gain 12dBi antenna, same as the transmitter. According to the datasheet [5], the demo kit with 34dB IF amplifier can resolve targets with 1m radar cross section at up to 16m range. Considering this information, it can be assumed that if a system with similar characteristics is designed then it should get decent signal from a close-range target (10-30cm).

### **3.3 Processor**

The purpose of this component is to sample analog radar signals, determine their frequency, calculate the car speed and transmit it via CAN bus.

The preferred choice is STM32F 32-bit microcontroller series because this series is used by our Formula team in other projects. Thus, development time and risks can be reduced by having same software libraries and development toolchain as other projects.

Project author has previously used 1024-point 16-bit FFT on a STM32F429 chip running on maximum 180MHz frequency; execution times were approximately 1.2ms, which seems fast enough for processing 2 radars every 10ms.

Fastest available microcontroller from the same series at the time the project was developed was STM32F767VIT6. It has 216MHz clock, 2MB of flash and 512kBytes of SRAM. This should be enough to handle 2 radars, IMU and a CAN communication.

### **3.4 Inertial measurement unit**

Inertial measurement unit, or IMU, is composed of 4 Bosch BMI160 MEMS sensors. 4 of them are used to make system more noise proof – single accelerometer can be quite noisy.

The IMU purpose is to provide speed estimation at a high frequency. As mentioned before, FFT needs some time window to determine the speed. At low speed, it may be very long. The accelerometer, on the other hand, supports sampling frequencies up to 6400Hz. Because of that, speed will be measured by integrating accelerometer data and accumulated error will be eliminated with the help low-frequency speed estimates from the radar.

### 3.5 Memory

Since two radars are can provide up to 5.4kHz signal, the real sampling frequency must be several times that to make a reliable frequency estimation. To make a rough estimation, let's assume that each radar signal is sampled at 8 times higher frequency, that makes

$$f_{sample} = 5.4kHz \cdot 8 = 43.2kHz \quad (10)$$

The microcontroller features 12bit ADC. For simplicity it is assumed that the measurements are stored as a 16-bit integer. If both I and Q channels are sampled for each radar, and each sample is 16-bit (2 byte), then total data rate will be

$$data\ rate = 4\ channels \cdot 2\ bytes \cdot 43.2kHz = 345600\ bytes/second \quad (11)$$

The data rate can be reduced by using 8-bit ADC mode and a lossless compression algorithm.

Ability to analyse this data afterwards will be of great help in developing and improving the radar software. The car has a data logger which logs CAN bus communication but streaming the unprocessed radar signal will be impossible due to limited effective data rate of a CAN bus. It will be useful if the radar has a memory to log the signal for further analysis.

Longest ride a car can have during a competition is during an endurance event, in which car must pass 21km. Such ride together with preparations and obligatory pit stop lasts approximately 30 minutes. Amount of data generated during the event will then be

$$amount\ of\ data = data\ rate \cdot 30\ min \approx 622\ megabytes \quad (12)$$

A perfect solution would be a SD card. They are cheap, provide several gigabytes of non-volatile storage and use a common SPI protocol.

### 3.6 Intermediate frequency amplifier

Like in the demo kit, an intermediate frequency (IF) amplifier is used.

The amplifier is based on LTC6912-2. The component is chosen because it features 35dB gain, same operating 3.3V supply as BGT24MTR11 and the microcontroller, and the gain is programmable via SPI, which is useful because signal strength will vary depending on road type and may need on-the-fly adjustment. The amplifier supports up to 100kHz frequency operation at maximum gain.

### 3.7 Power budget

This chapter briefly estimates voltage and power requirements.

In the car, a regulated 24V 1kW power supply is available.

Table 1 lists all components mentioned above and their voltage and power requirements. This gives an overview of needed voltage regulators and their current limits [6]-[11]

Table 1. Input voltage ranges and absolute maximum current consumption for major components.

Component	Input voltage, V	Maximum input current, mA
BGT24MTR11	3.14-3.46	190
LTC6912	2.7-10.5	7.5
STM32F767	1.7-3.6	279
SD Card	3.3	24
BMI160	1.71-3.6	0.99
TCAN1042HDRQ1	4.5-5.5	180

As can be seen, all components except the TCAN1042HDRQ1 CAN transceiver allow 3.3V operation. Additionally, many of them deal with analog signals and therefore require clean analog supply.

It makes sense to have a single switching regulator that will convert input 24V to 5V. 5V will be consumed by the CAN transceiver and will go to other components where it will be converted to 3.3V by local linear regulators. To simplify BOM, all 3.3V regulators can be the same.

NCP705MT33TCG 3.3V linear regulator will be used. It can provide up to 500mA of current, which is enough for each of the main components and their possible periphery.

Current capability of a 5V line can be estimated by adding together all current consumption numbers:

$$I_{5V\ max} = 2 \cdot I_{BGT24} + 2 \cdot I_{LTC} + I_{STM32} + I_{SD} + 4 \cdot I_{BMI} + I_{CAN} = 2 \cdot 190mA + 2 \cdot 7.5mA + 275mA + 24mA + 4 \cdot 0.99mA + 180mA = 881.96mA \quad (13)$$

LTM8073 is chosen to handle the 24V to 5V conversion. Its 60V input rating will help in harsh automotive environment, and 3A output current will handle the demand.

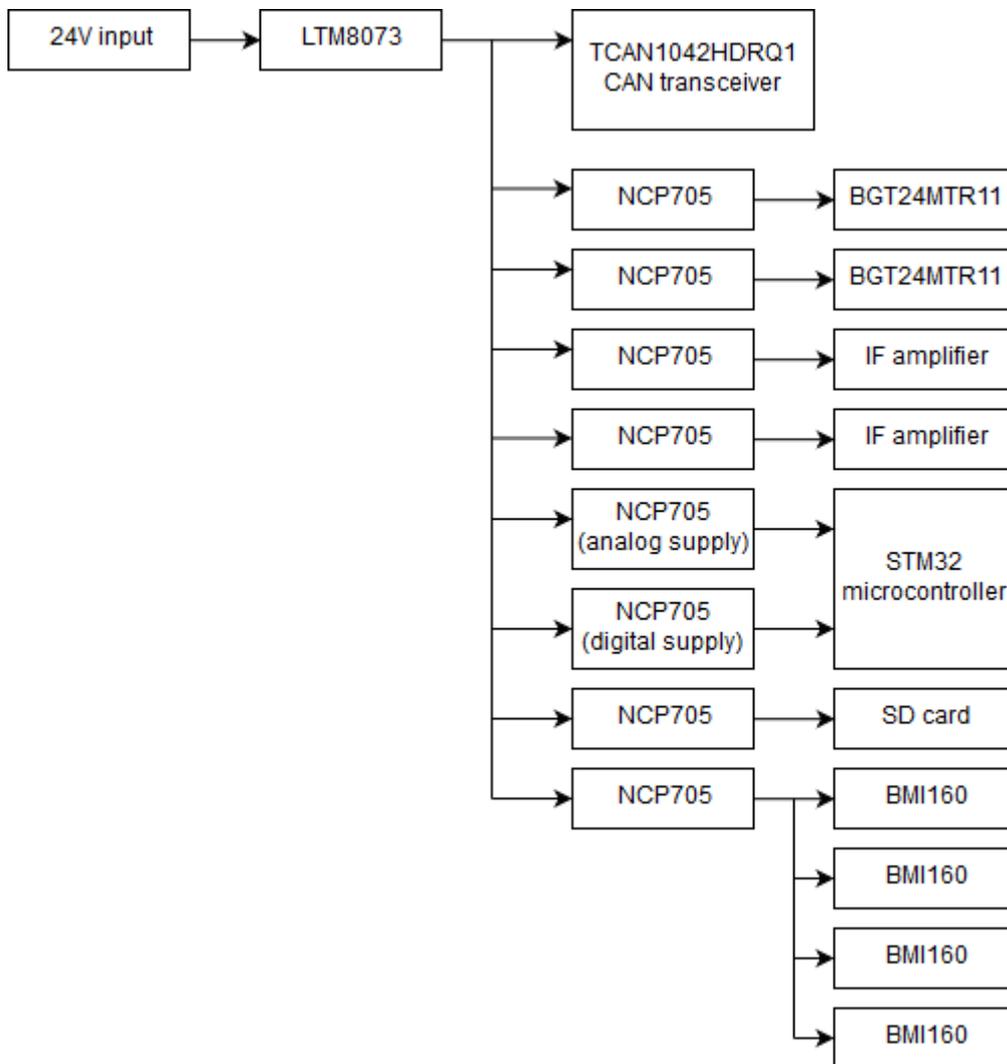


Figure 4. Power tree.

## **4 Hardware design**

This section provides detailed hardware design description. It starts with a radar PCB, which handles all radio and high frequency functions. Then a processor PCB is developed to digitize the radar signals coming from the radar PCBs. Finally, an enclosure is created to house all the components.

### **4.1 Radar PCB**

The radar PCB handles all radio and high frequency functions. Two such PCBs are used in a final product, each facing in its own direction.

Design process starts with the antenna. Once its dimensions are known, the rest of the PCB is done.

#### **4.1.1 Antenna choice**

Considering the application requirements, radar antenna must have the following parameters:

- High gain. Since velocity reading depends on reflection angle, antenna beam should be narrow to reduce ambiguity regarding reflection angle.
- Small size. Good antenna can easily be the largest component in a product. Radar should be as flat as possible because it is located under car very close to the road surface.

Many high gain antenna types are suitable for a radar. These include patch, Yagi, horn and other antennas, both single and in array configurations. Microstrip antennas are preferred in this project because PCBs are manufactured anyway, and no additional manufacturing process is required if microstrip antenna is chosen.

BGT24MTR11 has pins for both transmit and receive antennas. Same antenna can be used as either receive or transmit antenna, which simplifies the design.

Patch antenna is a very common high gain antenna type. It can be manufactured easily, takes little space and can be easily combined into arrays to further increase gain. Since it is so popular, there are many reference materials available which describe the design steps in detail. Considering this, microstrip patch antenna is chosen.

Ansys HFSS simulation software is used to simulate and optimize the antenna.

#### 4.1.2 Single patch antenna design

Antenna is designed using [12] as a guide.

We start by calculating antenna dimensions. Based on them, Ansys HFSS model is constructed, simulated and optimized.

First, some input parameters are defined. Resonant frequency  $f_r$  is 24.125GHz.  $\epsilon_r$  and  $h$  depend on PCB material. PCB manufacturer has Rogers RO4003C material available with thicknesses of 0.203, 0.508 and 0.813mm. 0.203mm thick material is selected. Its dielectric constant is 3.38 [13].

Antenna width is determined using equation (14):

$$W = \frac{v_0}{2f_r} \sqrt{\frac{2}{\epsilon_r+1}} = \frac{299792458 \text{ m/s}}{2 \cdot 24.125 \text{ GHz}} \sqrt{\frac{2}{3.38+1}} \approx 4.199 \text{ mm} \quad (14)$$

where  $v_0$  is a free-space velocity of light,  $f_r$  is resonant frequency and  $\epsilon_r$  is substrate dielectric constant [14].

Next, effective dielectric constant is determined using equation [15] (15):

$$\epsilon_{reff} = \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2} \left(1 + \frac{12h}{W}\right)^{-\frac{1}{2}} = \frac{3.38+1}{2} + \frac{3.38-1}{2} \left(1 + \frac{12 \cdot 0.203 \text{ mm}}{4.99 \text{ mm}}\right)^{-\frac{1}{2}} \approx 3.14 \quad (15)$$

Condition  $\frac{W}{h} > 1 \approx 20.68$  is satisfied.

Then, extension of length is calculated using equation (16)

$$\begin{aligned} \Delta L &= 0.412h \frac{(\epsilon_{reff}+0.3)\left(\frac{W}{h}+0.264\right)}{(\epsilon_{reff}-0.258)\left(\frac{W}{h}+0.8\right)} = \\ &= 0.412 \cdot 0.208 \text{ mm} \cdot \frac{(3.14+0.3)(20.68+0.264)}{(3.14-0.258)(20.68+0.8)} \approx 97.36 \mu\text{m} \end{aligned} \quad (16)$$

Finally, actual length of the patch is calculated

$$L = \frac{v_0}{2f_r\sqrt{\epsilon_{reff}}} - 2\Delta L = \frac{299792458 \frac{m}{s}}{2 \cdot 24.125 \text{ GHz} \sqrt{3.14}} - 2 \cdot 97.36 \mu\text{m} \approx 3.314 \text{ mm} \quad (17)$$

Based on the above width and length, Ansys HFSS model is constructed.

There are several feed types commonly used with patch antennas. These include inset, quarter-wave transformer, probe, coupled or aperture feeds [16]. Inset feed is preferred because it allows for more compact feed network design compared to quarter-wave transformer feed, and it only requires two copper layers, which means that all high-frequency circuitry stays on one side of the board.

Final HFSS model is displayed below.

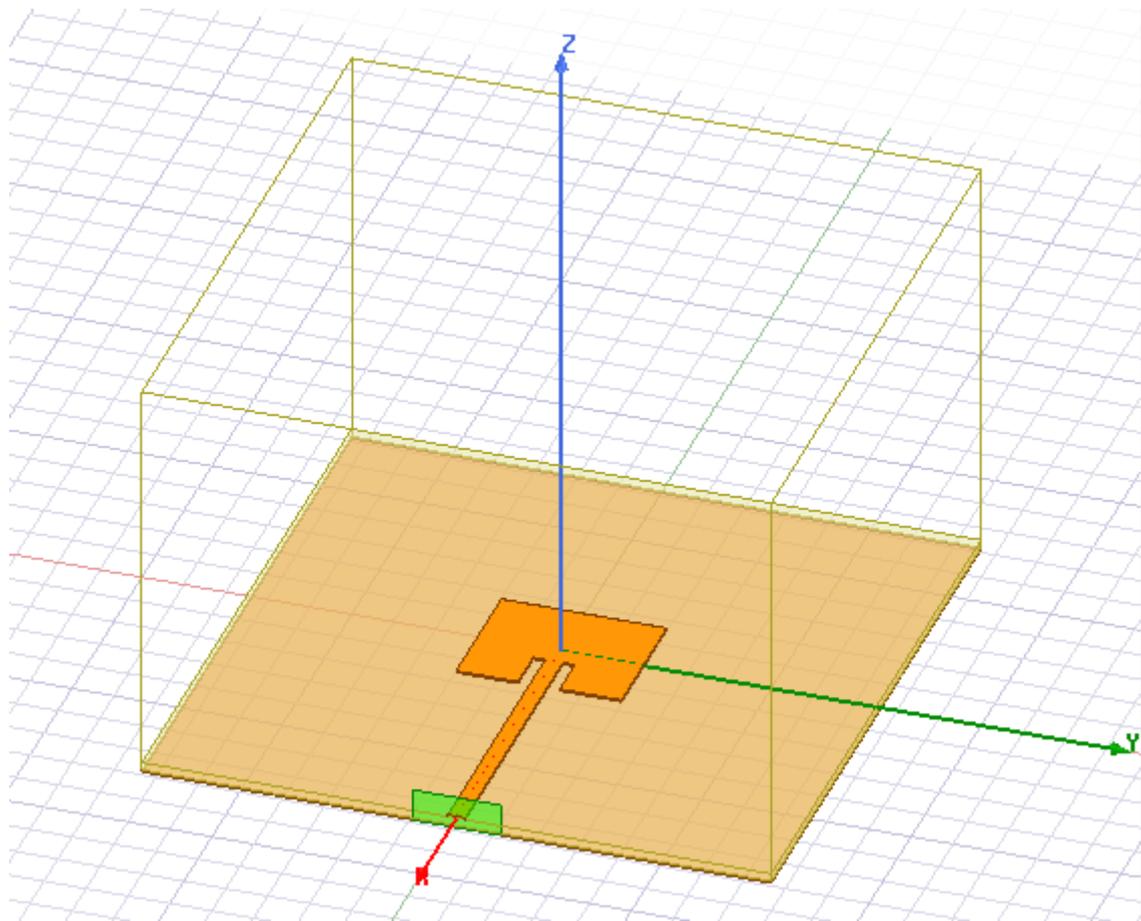


Figure 5. HFSS model of a 24GHz microstrip patch antenna.

The model is optimized using HFSS's built-in functions to find the optimal dimensions of the patch. The dimensions optimized are patch width and length, gap width and length,

and feed width. Initial patch width and length are chosen from the values calculated above. Starting gap dimensions are chosen arbitrarily, 1mm width and 1mm length.

Feed is a  $50\Omega$  trace. Its width is calculated using PCB toolkit V7.05. Following parameters were entered: microstrip, 24.125GHz center frequency, RO4003 material,  $18\mu\text{m}+35\mu\text{m}$  copper, 0.203mm substrate thickness. With these parameters, 0.46mm wide conductor achieves  $50\Omega$  impedance.

Sequential Nonlinear Programming algorithm was used to optimize antenna dimensions. It's initial values, as well as minimum and maximum given in a table below.

Table 2. Antenna dimensions before optimization.

Parameter	Starting value, mm	Min value, mm	Max value, mm
Patch width	4.199	3.149	5.249
Patch length	3.314	2.486	4.143
Gap width	1.000	0.750	1.250
Gap length	1.000	0.750	1.250
Feed width	0.460	0.345	0.575

In the HFSS model, antenna is driven by a single wave port. Maximum  $\Delta S$  is 0.02. Optimization goal is to minimize  $S_{11}$ . Optimized dimensions are shown in table 3 and in figure 6.

Table 3. Antenna dimensions after optimization.

Parameter	Value after optimization, mm
Patch width	3.936
Patch length	3.226
Gap width	0.995
Gap length	1.091
Feed width	0.420

According to the simulation, antenna efficiency is 81% and maximum gain is 6.68dB. Figure 7 shows  $S_{11}$ . Figures 8 and 9 show the radiation pattern.

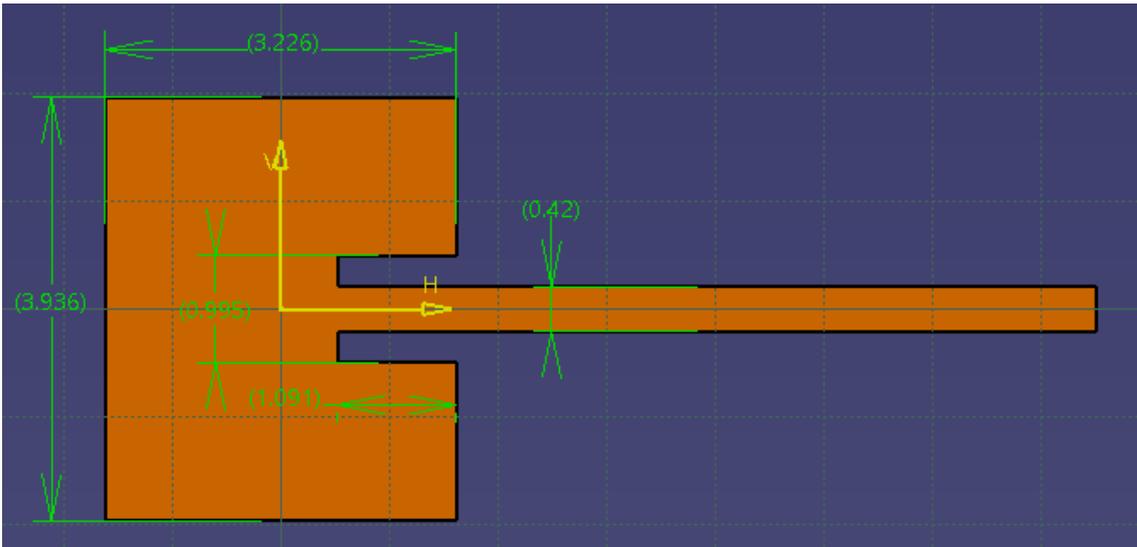


Figure 6. Patch drawing showing optimized dimensions, in mm.

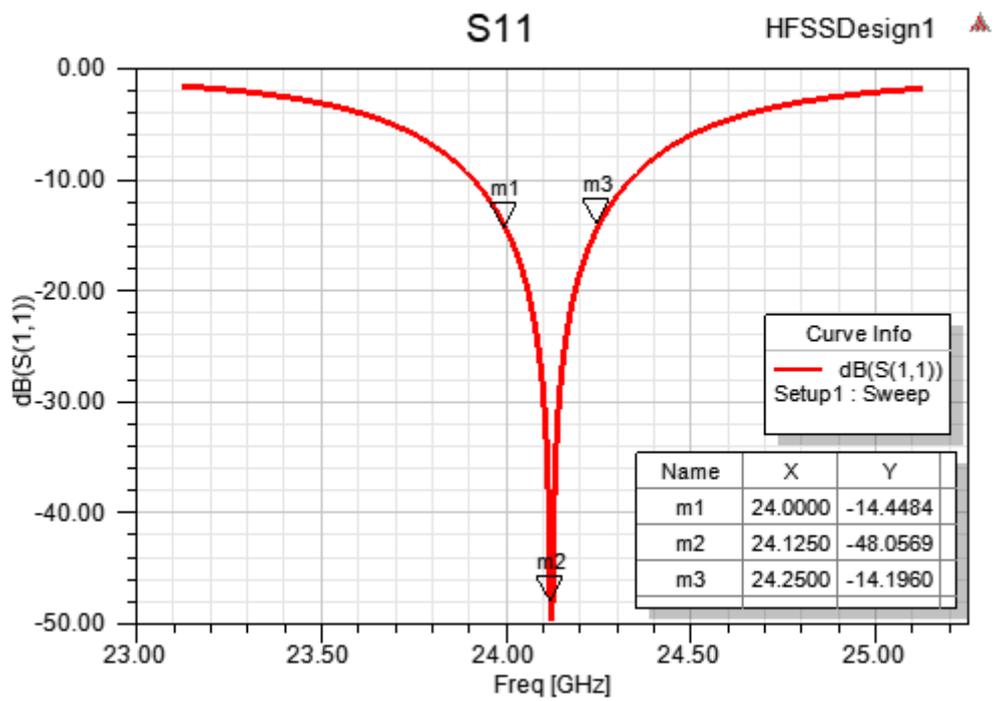


Figure 7. Optimized path  $S_{11}$ .

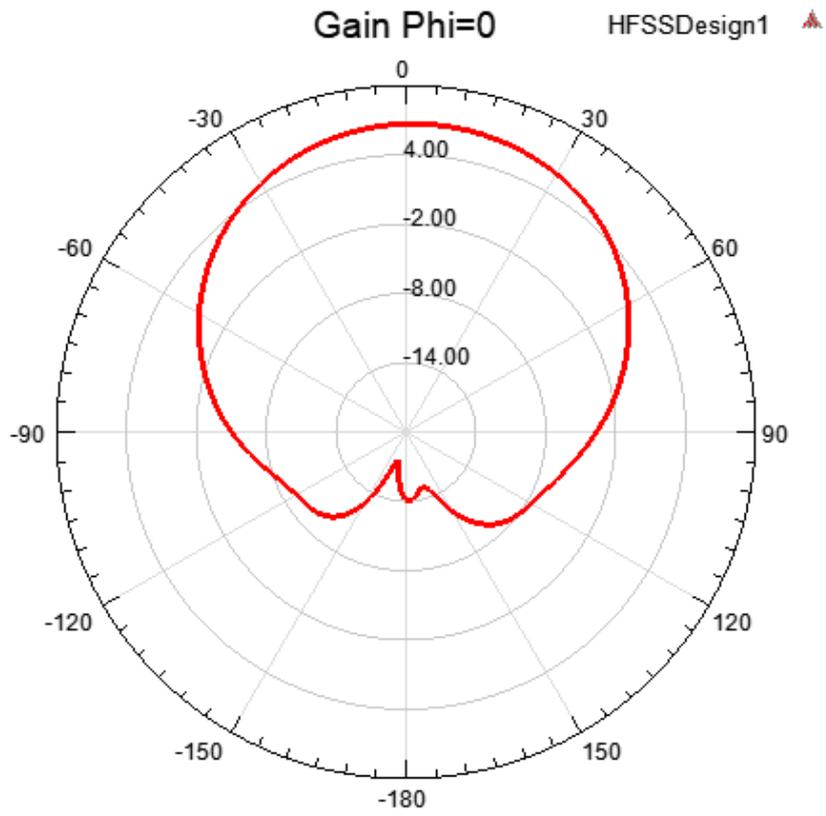


Figure 8. Patch radiation pattern at  $\phi=0^\circ$ .

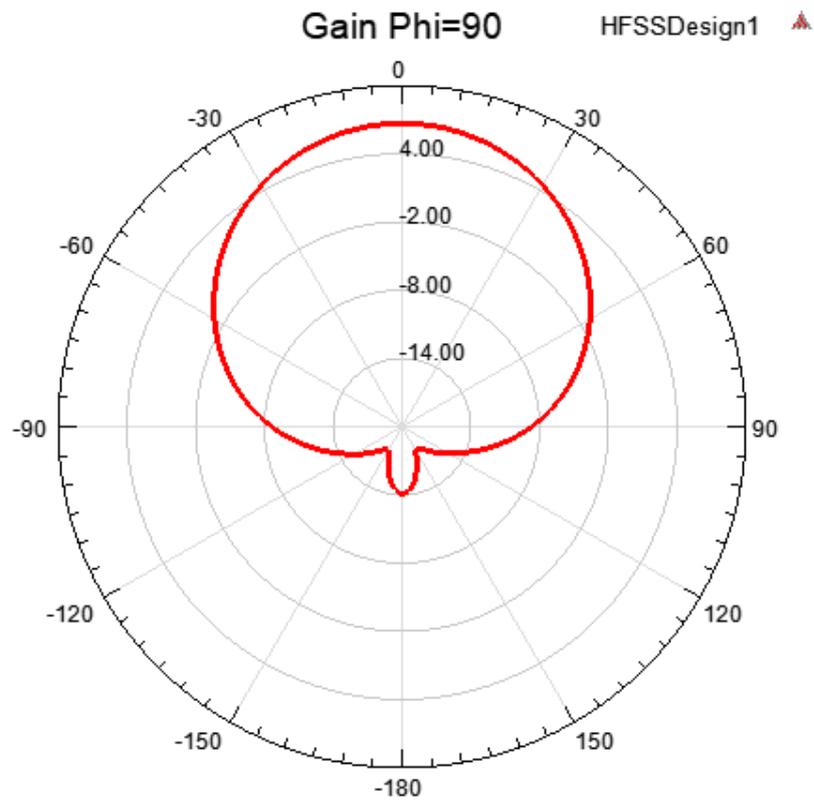


Figure 9. Patch radiation pattern at  $\phi=90^\circ$ .

Table 4 sums up the patch parameters.

Table 4. Summary of patch parameters.

Parameter	Value
Maximum gain, dB	6.68
Efficiency	82%
<i>S11</i> at 24.000GHz, dB	-14.45
<i>S11</i> at 24.125GHz, dB	-48.06
<i>S11</i> at 24.250GHz, dB	-14.20

It should be noted that optimized antenna length is close to that initially calculated, but width is slightly smaller. According to the simulation, 50  $\Omega$  feed should be 0.42mm wide, which contradicts with 0.46mm width obtained from PCB Toolkit software. Due to this, additional simulation of a 50 $\Omega$  stripline from figure 10 was performed to find out correct trace width.

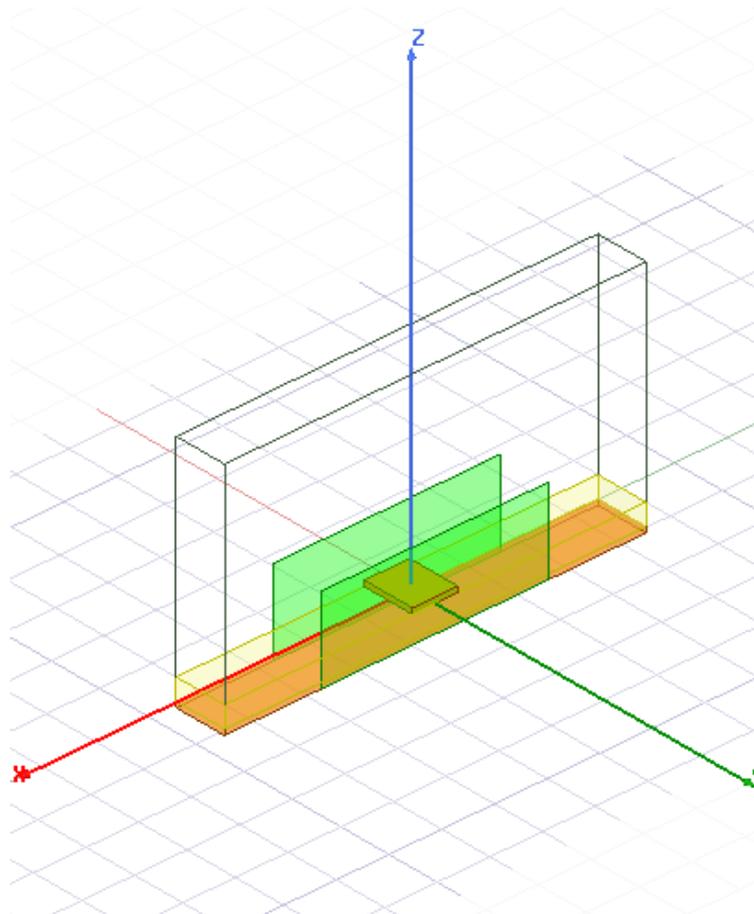


Figure 10. HFSS 50 $\Omega$  stripline simulation model.

In the model, 0.5mm long stripline is constructed on RO4003 substrate. Two ports are present, port 1 is input and port 2 is output. *S11* is measured.

Using parametric sweep, stripline width was varied from 0.4mm to 0.48mm using 0.01mm step. Results are provided in table 5.

Table 5. *S11* for a stripline with different widths.

Trace width, mm	<i>S11</i> , dB
0.40	-40.790
0.41	-48.100
0.42	-37.720
0.43	-34.040
0.44	-32.730
0.45	-30.470
0.46	-28.810
0.47	-27.690
0.48	-26.220

Although 0.41mm stripline is a clear winner, all candidates are very good. Even worst of them, 0.48mm, has very good *S11* of -26.22dB, which is more than enough for the job. Thus, 50Ω stripline will be 0.42mm as it came out in patch simulation.

#### 4.1.3 Antenna array design and simulation

As mentioned before, high gain is important to achieve better radar performance. To further increase gain, microstrip patches are placed in an array. More elements in the array, higher the gain. Number of elements is, however, limited by height available under the car.

Distance from the car's lowest point to the road surface is approximately 33mm. Center of mass is approximately 10cm behind the lowest point. This is illustrated in figure 11.

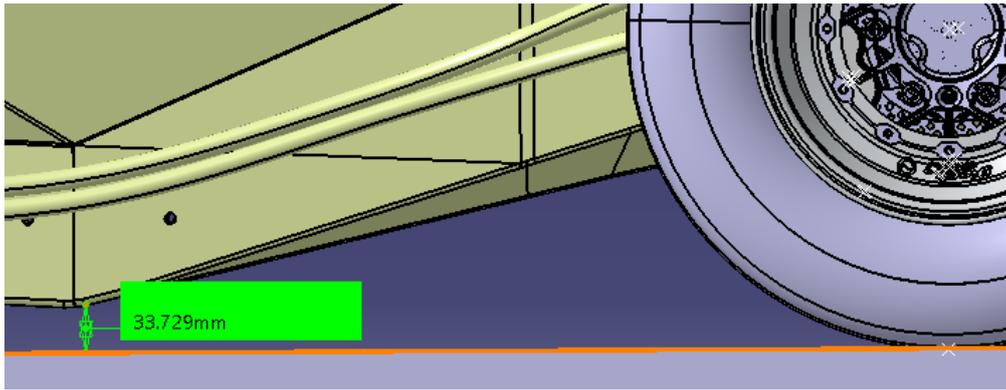


Figure 11. Distance from the car's lowest point to road surface.

To get the radar as close to the center of mass as possible, it should be very close to the lowest point, which means large antenna array will not fit in. Because of that, array configuration of 2x2 is chosen.

To maximize the power radiated in a single direction, feed network is constructed in such a manner that all elements have same phase excitation.

According to [17], element spacing should not be multiple of wavelength to prevent grating lobes. This, however, has little effect on patch antenna array because separate elements have high gain and grating lobes will have very little gain.

Figure 12 shows what final version of the antenna array looks like. Detailed explanation of a feed network structure, its elements and simulation procedures are given below. Different elements are analyzed and simulated separately to simplify the job, then combined.

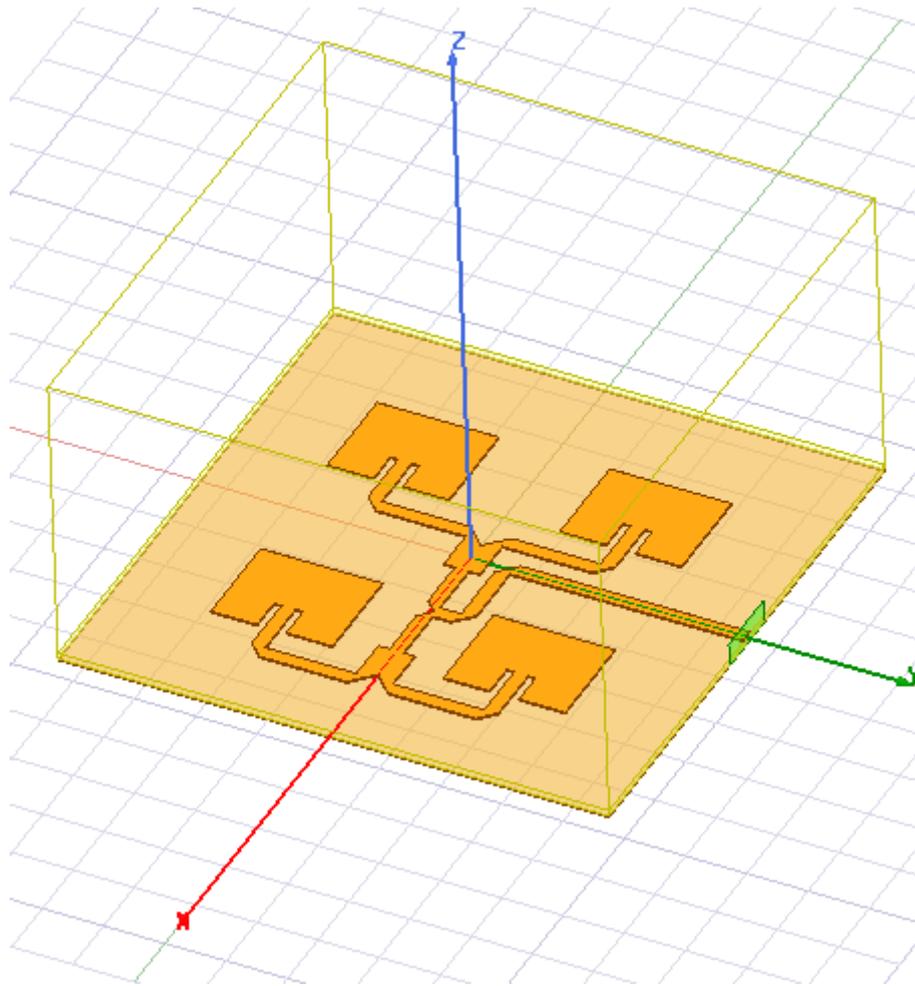


Figure 12. Simulated HFSS model of a 2x2 patch antenna array.

Array design is started from a feed network. To minimize distance between antenna elements, feed network should contain as little fixed-dimension components as possible. One such component is quarter wave transformer. It can be bent to fit in a small space, but it requires an additional effort to design and simulate such element. Figure 13 shows feed network structure containing only 2 quarter wave transformers in total.



Figure 13. Feed network structure.

From PCB component point of view, antenna is ‘seen’ as a single 50Ω feed. This feed then splits into 2 100Ω feeds. These 2 100Ω feeds are in parallel, so their total impedance is 50Ω, and no quarter-wave transformer is needed to match them.

‘Looking’ from antenna side, each patch element is 50Ω. Two patches are combined in parallel, their total impedance is 25Ω.

Both 100Ω and 25Ω traces meet in the middle of the figure 13 and are matched via a quarter-wave transformer. Its impedance is

$$Z_{\frac{\lambda}{4}} = \sqrt{Z_{in}Z_{out}} = \sqrt{100\Omega \cdot 25\Omega} = 50\Omega, \quad (18)$$

Apart from requiring only 2 quarter-wave transformers, 1 for each branch, this feed network has an additional benefit: it only requires only 2 different impedance microstrips, 50Ω and 25Ω. 100Ω trace can be omitted because there is no specific length requirement, and we can simply set its length to 0. This simplifies PCB design and manufacturing because 100Ω trace would be approximately 0.08mm wide, which is very thin compared to the other elements of the array.

According to the PCB Toolkit software, 25Ω trace should be 1.3mm thick. Like the 50Ω trace, it is simulated in HFSS and the results are compared. Trace width was varied from 1.1mm to 1.4mm with 0.05mm step. The model is shown in figure 14 and the simulation results are presented in table 6.

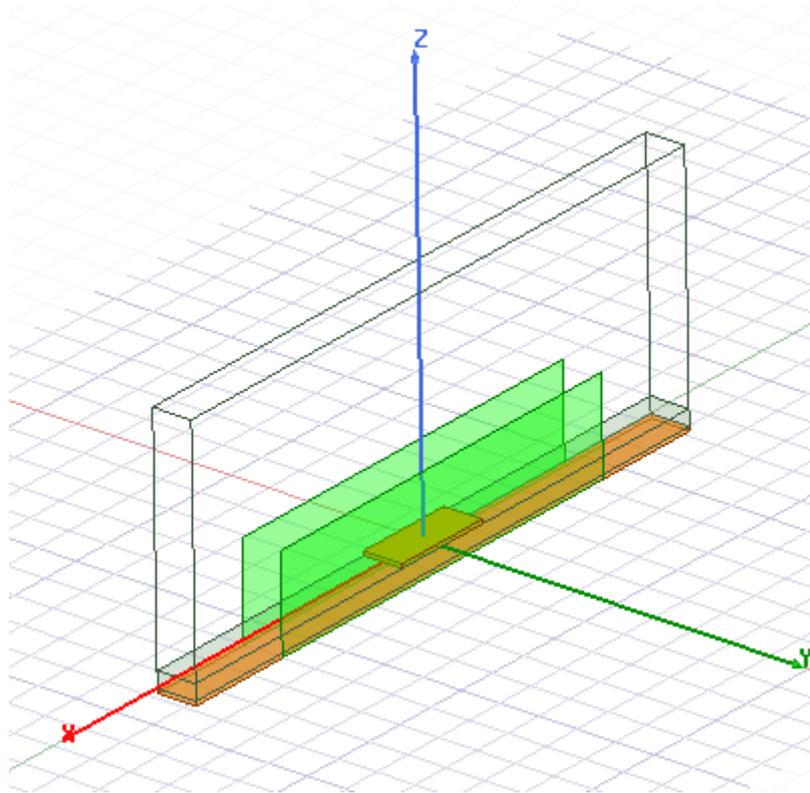


Figure 14. HFSS model of a 25Ω trace.

Table 6. Simulation results for 25Ω traces.

Trace width, mm	<i>S<sub>11</sub></i> , dB
1.1	-35.76
1.15	-51.51
1.2	-36.21
1.25	-30.81
1.3	-26.95
1.35	-25.11
1.4	-23.25

1.15mm wide trace is shows the best performance, but again, just like in case of the 50Ω trace, all widths provide very good result.

With trace widths in place it is time improve trace corner performance. According to [18], sharp 90° angles add shunt capacitance to the traces due to impedance mismatch. HFSS model is constructed to simulate this effect. The model is shown in figure 15.

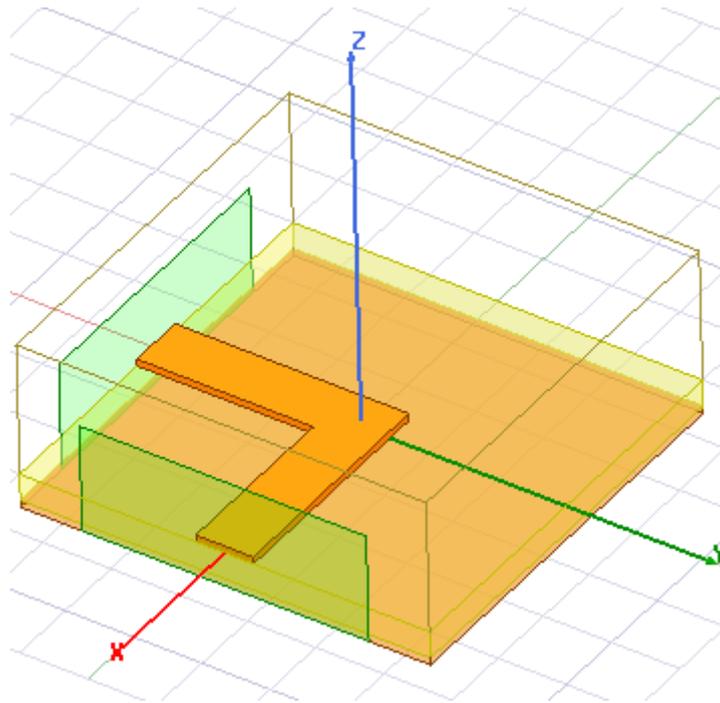


Figure 15. HFSS model of a 90° bend in 50Ω trace.

Once simulated, unmodified 90° bend  $S_{11}$  is -14.83dB. Not that bad, but can this be improved?

In a new model, miter is introduced as shown in figure 16. Its offset is changed by 0.1mm using parametric sweep.  $S_{11}$  is measured. Results are given in table 7.

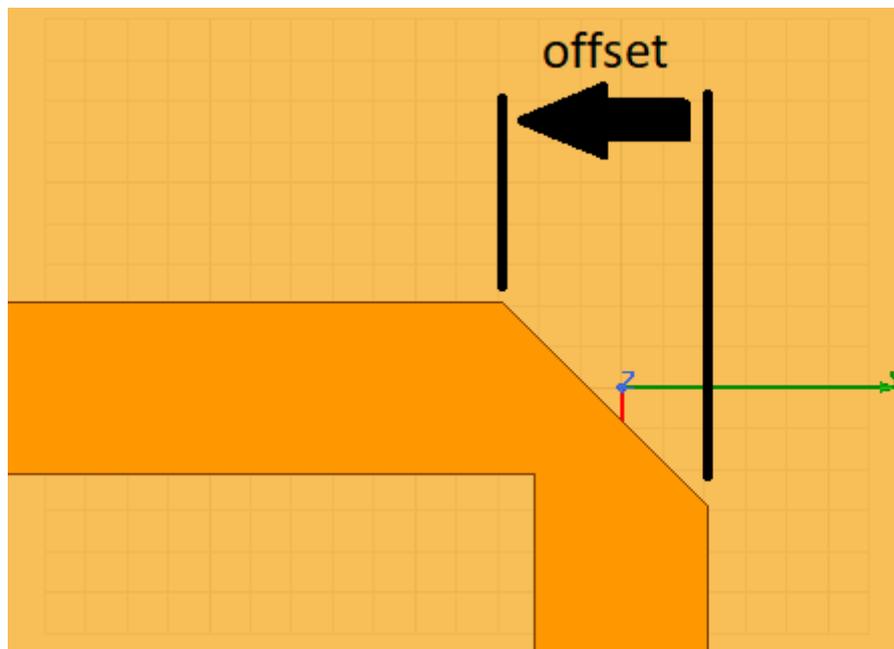


Figure 16. Offset direction in a mitered bend.

Table 7. 50Ω trace mitered bend simulation result.

Offset, mm	<i>S11</i> , dB
0.0	-14.83
0.1	-15.37
0.2	-16.03
0.3	-17.33
0.4	-20.33
0.5	-25.17
0.6	-40.32
0.7	-21.06

As can be seen, the best result is achieved by applying 0.6mm offset to the 0.42mm trace. Values from 0.4mm to 0.7mm can also be safely used due to their low *S11*.

Next simulated element is first split in a feed network which splits 50Ω antenna feed to 2 x 50Ω quarter wave transformers. It is displayed on figure 17.

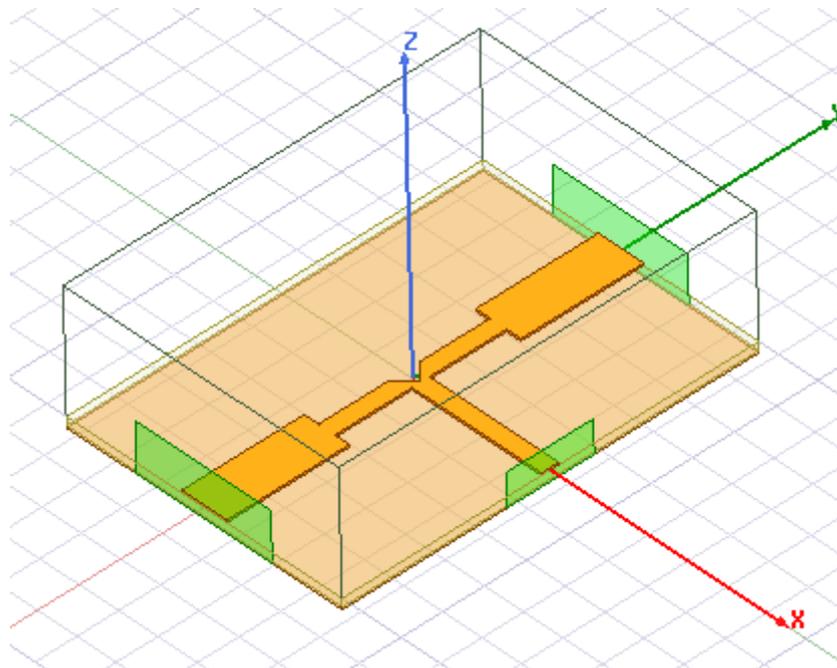


Figure 17. HFSS model of a first split in feedline.

Here, 50Ω port 1 in the middle sends signal down 50Ω line. Line is split into 2 branches which start with 50Ω quarter-wave transformers that transition into 25Ω traces. These end with ports 2 and 3, both normalized to 25Ω.

Optimization job is set up in HFSS to modify 2 parameters: cutout depth and quarter-wave transformer length to minimize  $S_{11}$ . According to the PCB toolkit software quarter-wave is approximately 2mm on the substrate used in this project. However, quarter-wave transformer length may vary slightly depending on the surrounding elements, therefore its length is subject to the optimization. Elements optimized are shown in figure 18.

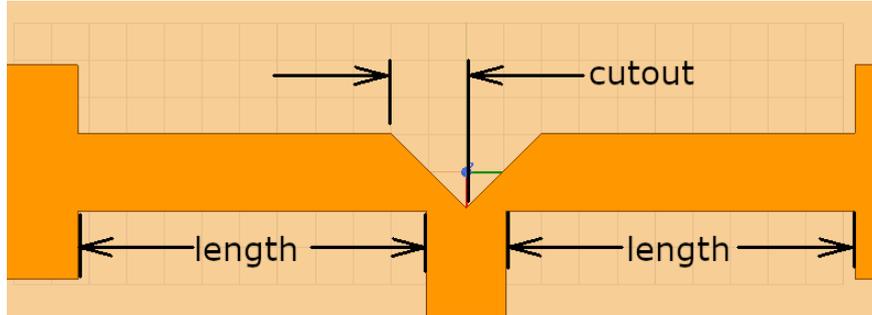


Figure 18. Dimensions varied in the optimization.

Sequential Nonlinear Optimization algorithm was used for the optimization. Cutout range was limited from 0.2mm to 0.7mm, and quarter wave transformer length range was limited from 1.5mm to 2.5mm. Optimization results are given in a table below.

Table 8. Optimization result

Parameter	Value
Cutout depth, mm	0.40
Quarter-wave transformer length, mm	1.85
$S_{11}$ at 24.125GHz, dB	-21.98
$S_{21}$ at 24.125GHz, dB	-3.45
$S_{31}$ at 24.250GHz, dB	-3.24

As can be seen, this structure nicely splits signal into two almost equal parts while providing little reflection.

Finally, the split from  $25\Omega$  to 2  $50\Omega$  traces is analyzed. The model simulating it is shown in figure 19.

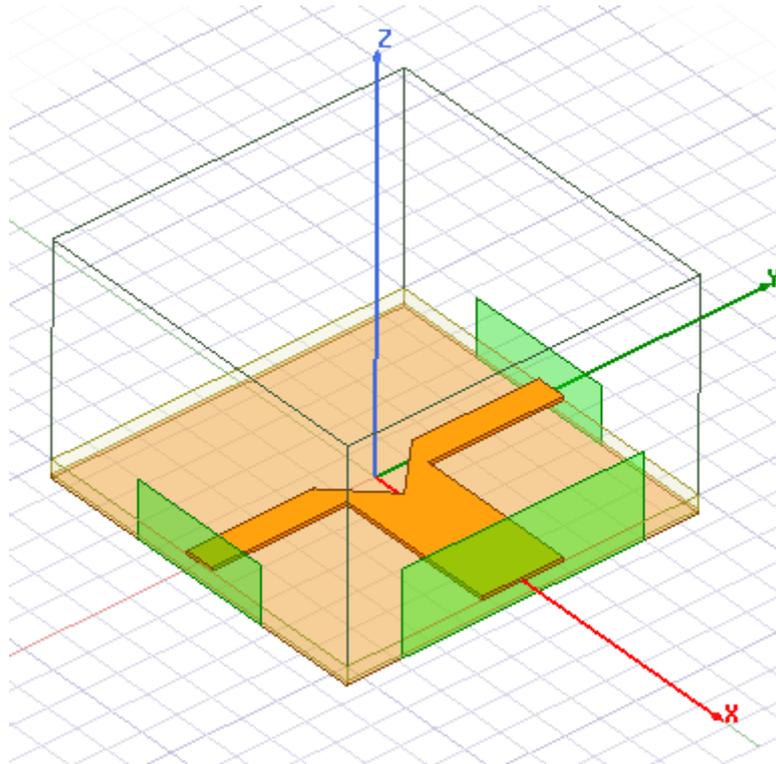


Figure 19. HFSS model of the split from  $25\Omega$  to  $2 \times 50\Omega$  traces.

Since there is only one parameter to analyze, the cutout depth, a simple parametric sweep is executed which varies the cutout depth from 0.2mm to 0.8mm.  $S_{11}$  is measured. Result is given in table 9.

Table 9.  $25\Omega$  to  $2 \times 50\Omega$  split simulation results.

Depth, mm	$S_{11}$ , dB
0.2	-16.16
0.3	-16.58
0.4	-18.71
0.5	-19.32
0.6	-22.40
0.7	-30.80
0.8	-22.43

Based on the results, 0.7mm cutout depth is chosen.

Now everything is ready to create the antenna array. The array model is demonstrated in figure 20.

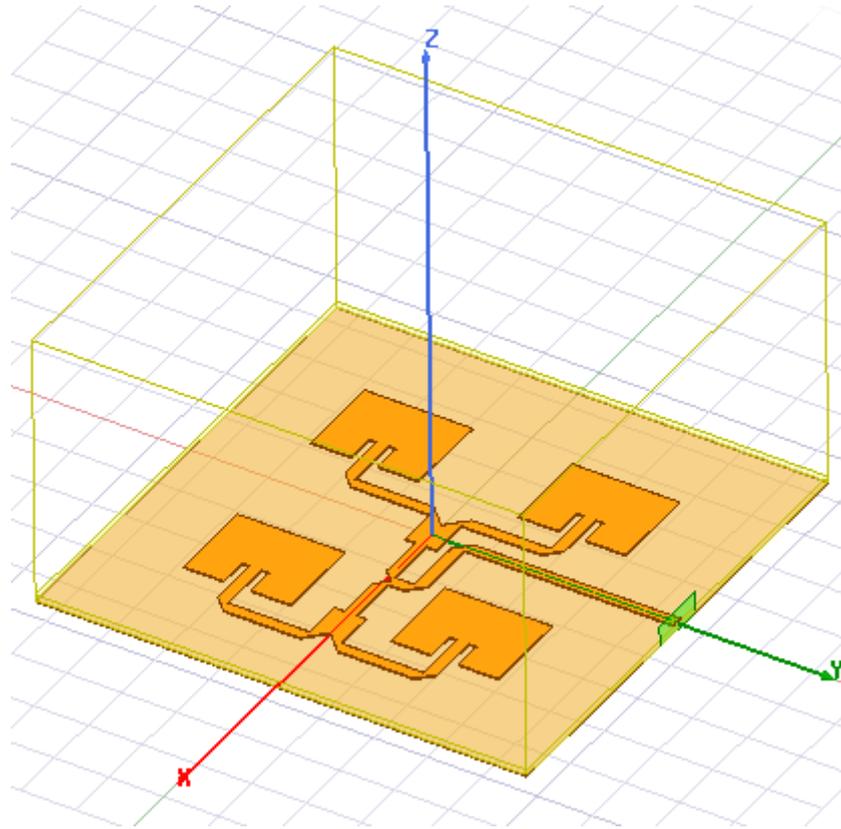


Figure 20. HFSS model of the antenna array.

The model was simulated to see the total system performance. Important antenna parameters such as  $S_{11}$ , radiation efficiency and a radiation pattern were measured. The parameters are presented in table 10 and in figures 21-24.

Table 10. 2x2 patch array parameters.

Parameter	Value
Maximum gain, dB	12.82
Efficiency	77%
$S_{11}$ at 24.000GHz, dB	-13.92
$S_{11}$ at 24.125GHz, dB	-14.33
$S_{11}$ at 24.250GHz, dB	-11.85

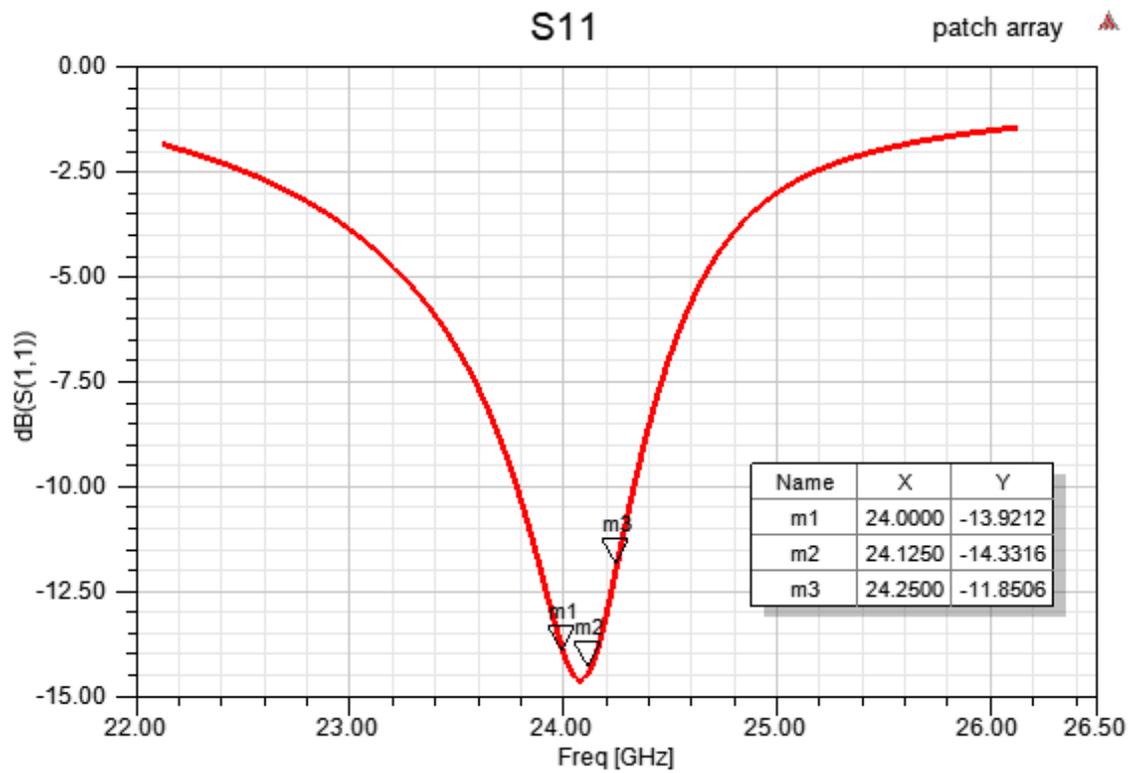


Figure 21. Antenna array  $S_{11}$ .

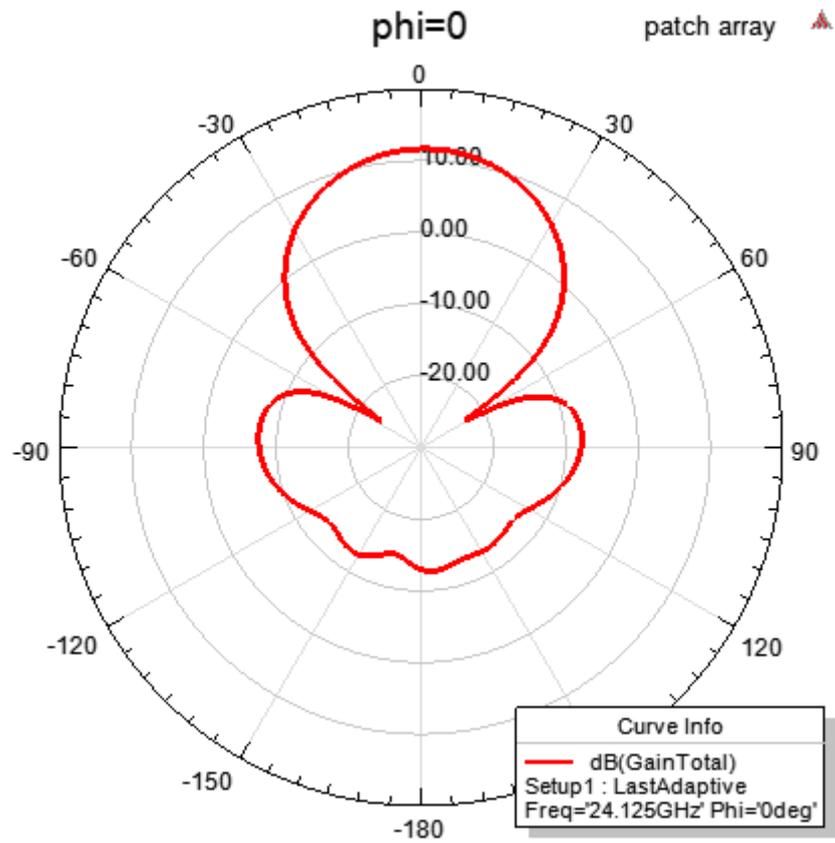


Figure 22. Radiation pattern for  $\phi=0^\circ$ .

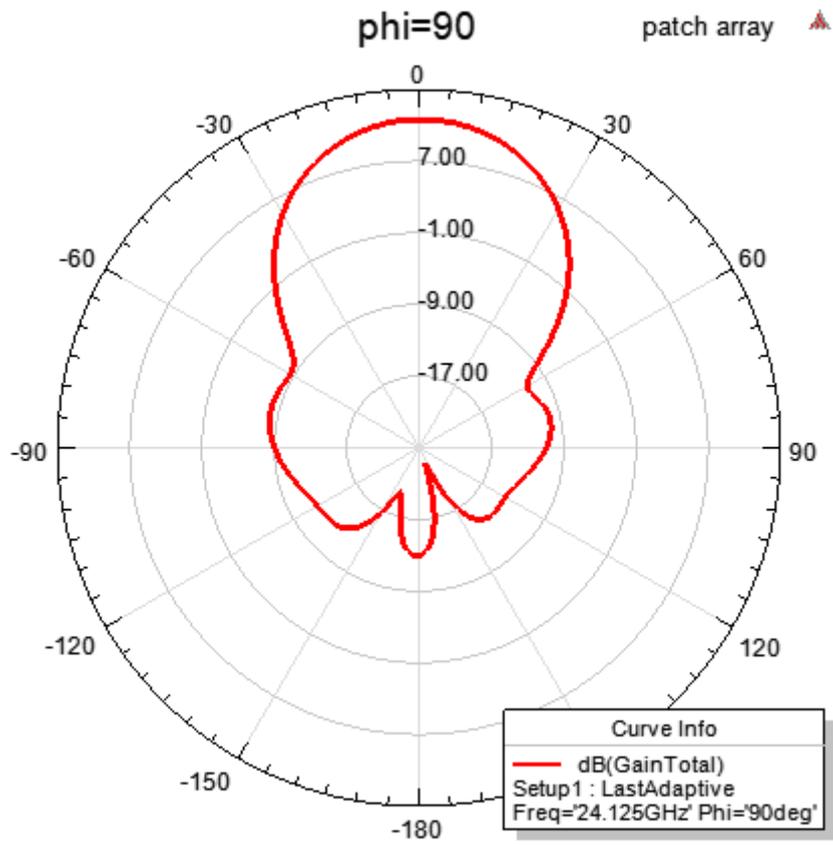


Figure 23. Radiation pattern for  $\phi=90^\circ$ .

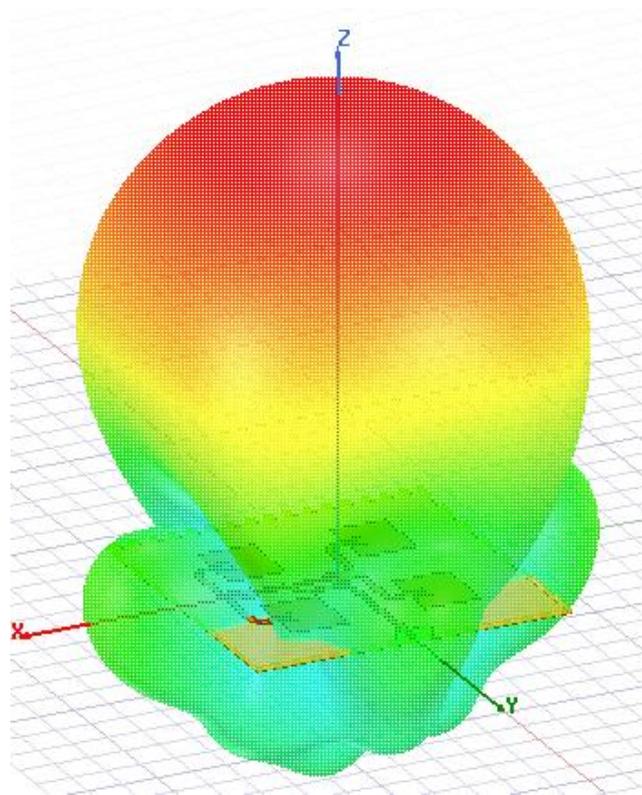


Figure 24. 3D radiation pattern displayed on the antenna model.

Radiating array elements are placed in a 7.6mm grid. The dimension is chosen empirically. This dimension reduces antenna size while feed elements are still separated from the radiating elements.

Figure 25 demonstrates all important dimensions. Since many elements are symmetrical, dimensions are shown only once for every unique element. Microstrip thickness,  $53\mu m$ , is not shown.

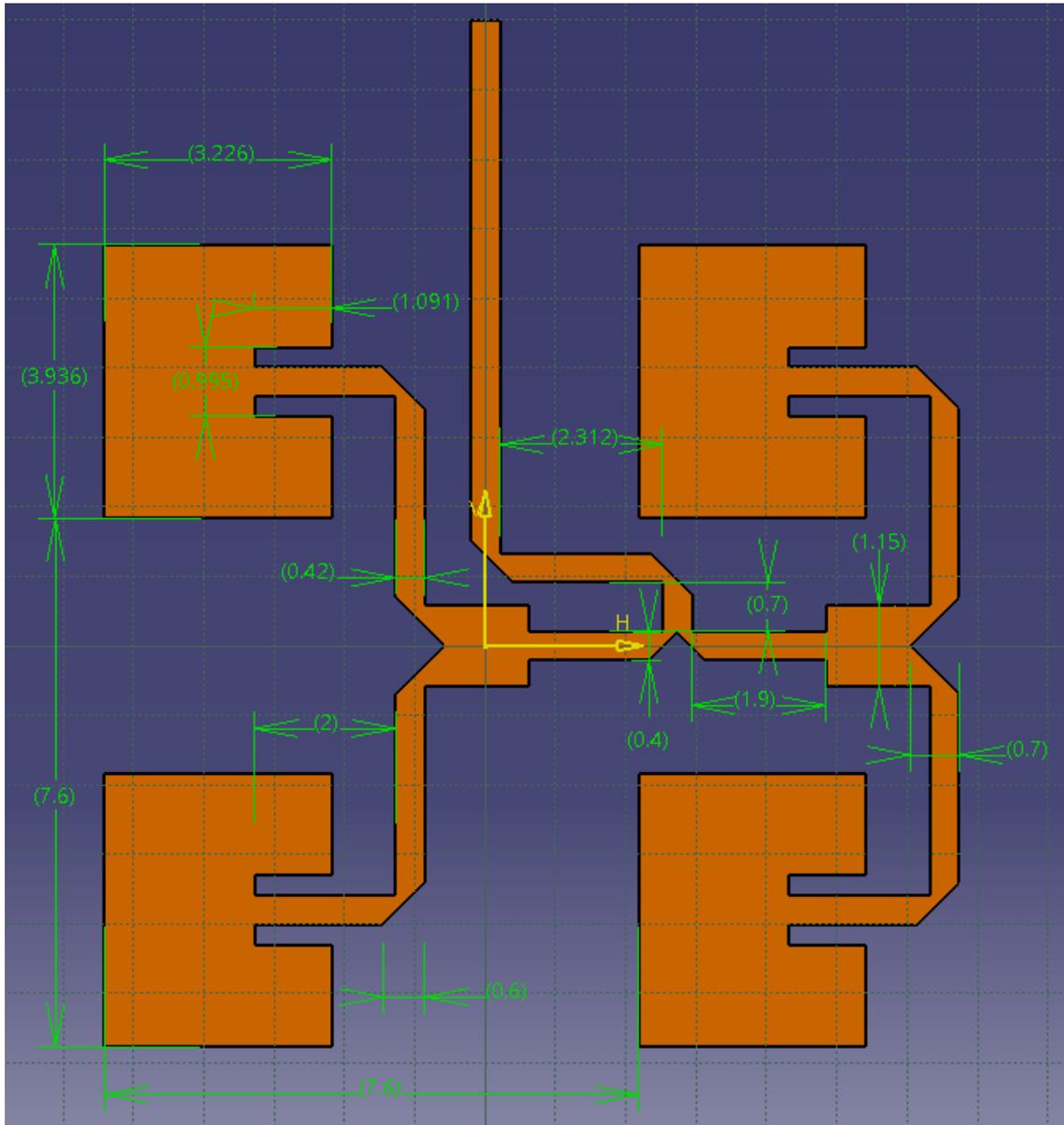


Figure 25. Important dimensions, in mm.

#### 4.1.4 Radar PCB design

With main components and the antenna figured out, the PCB can now be designed. Altium Designer software is used to design all PCBs in this project.

Radar PCB has all components dealing with high frequency, that includes BGT24MTR11 and the antennas. As soon as high frequency signal is converted to IF by the BGT24MTR11, it leaves the board. IF amplifier is located on the processor board due to space constraints. No blind vias are used. Because of that, components cannot be placed on the opposite board side beneath antennas, limiting the component area to small square between the antennas.

BGT24MTR11 has a local 3.3V regulator. Power pins are bypassed by 1 $\mu$ F ceramic capacitors as suggested in the datasheet [19]. Since the datasheet does not mention smaller picofarad bypass capacitors it is assumed that the necessary amount of high frequency bypass capacitance is already built into the silicon.

Since noise may be an issue, all signal lines leaving the board have RC low-pass filters on them. Due to space limit on the radar PCB, RC filter components are split between the boards. The resistors are located near the signal source to limit the instantaneous currents going down the line. The capacitors are placed near receiving pins to bypass high frequency noise more effectively. To simplify the BOM, RC filters are implemented with common components, namely 1nF capacitors and 1k $\Omega$  resistors. Such filters have a cutoff frequency of

$$f_c = \frac{1}{2 \cdot \pi \cdot C \cdot R} = \frac{1}{2 \cdot \pi \cdot 1nF \cdot 1k\Omega} \approx 159.16 \text{ kHz} \quad (19)$$

The filters are placed on a SPI lines, VCO, ANA and Q2 signal pins.

IF signals use 100 $\Omega$  and 100nF capacitors which give lower cutoff frequency

$$f_c = \frac{1}{2 \cdot \pi \cdot C \cdot R} = \frac{1}{2 \cdot \pi \cdot 100nF \cdot 100\Omega} \approx 15.92 \text{ kHz} \quad (20)$$

VCO and Q2 pins go to the microcontroller. Together, they give the ability to control the radar frequency by measuring the feedback frequency on a Q2 and setting oscillator frequency by applying analog signal to the VCO pin. This is important for two reasons: first, two radars may interfere with each other if operating frequencies get too close; second, oscillator frequency will drift with temperature and corrections will be necessary. Additionally, it allows using the PCB as an FM radar in the future, however, in this case a proper PLL chip would have enabled much more precise frequency sweep.

TXOFF pin is shorted to ground via  $0\Omega$  resistor because TXOFF function can be controlled via the SPI.

ANA pin voltage is measured by the microcontroller to get a feedback on TX power and the chip temperature.

Divide-by-16 prescaler is not used. Its pins Q1 and Q1N are terminated by  $49.9\Omega$  resistors. According to the application note [20], there is DC bias present on the pins and DC blocking capacitors must be used. 47pF Murata GRM0335C1E470JA01D is chosen because this model has ESR curve minimum at 1.5GHz, the frequency of the divide-by-16 prescaler.

High frequency TX, LO and RX pins have complex impedance. The datasheet suggests using the compensation structures shown in figure 26 [21]. The compensation structure geometry resembles quarter-wave transformers, which simply convert the real part of the impedance while ignoring small complex component.

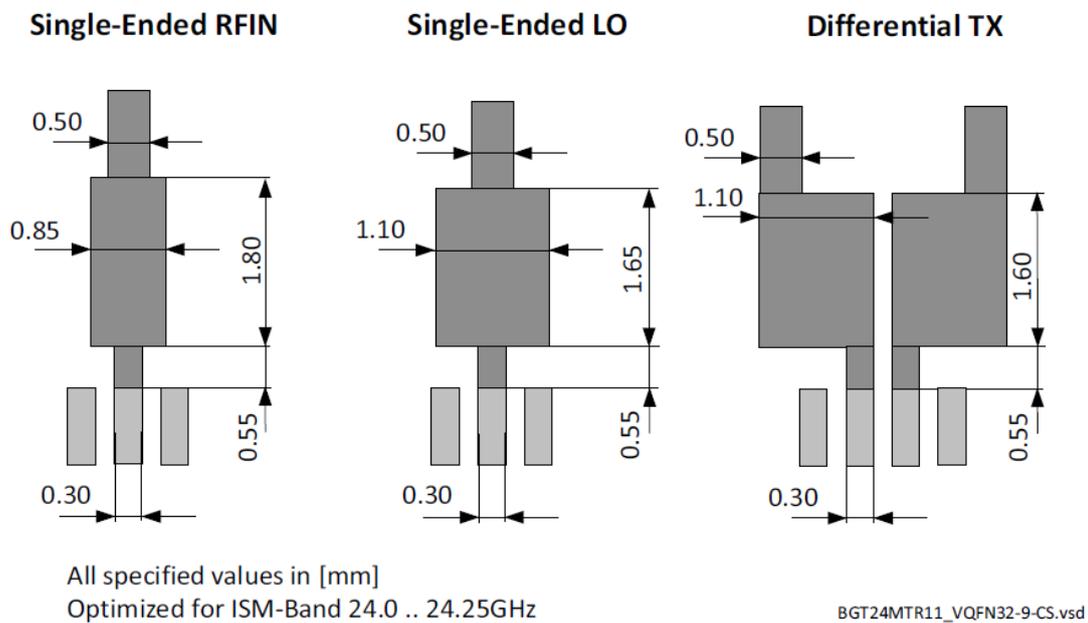


Figure 26. Compensation structures given by the BGT24MTR11 datasheet.

The problem is, however, that the structures provided in the datasheet use 0.254mm thick RO4350B substrate. Thus, the copper geometry must be different. A HFSS simulation was performed to analyze the structure performance on different substrates.

RFIN compensation structure model was created in HFSS with dimensions equal to those given in the datasheet. It is shown on figure 27. Port 1 simulates the antenna and has  $50\Omega$

impedance. Port 2 simulates the chip's input pin and has  $22.9-j14.9\Omega$  impedance. 3 variations were simulated. First simulated the structure with the exact parameters given in the datasheet. Second changed substrate to RO4003C while keeping the same copper geometry. Third changed  $50\Omega$  feedline thickness to 0.42mm instead of 0.5mm. Simulation results are given in table 11.

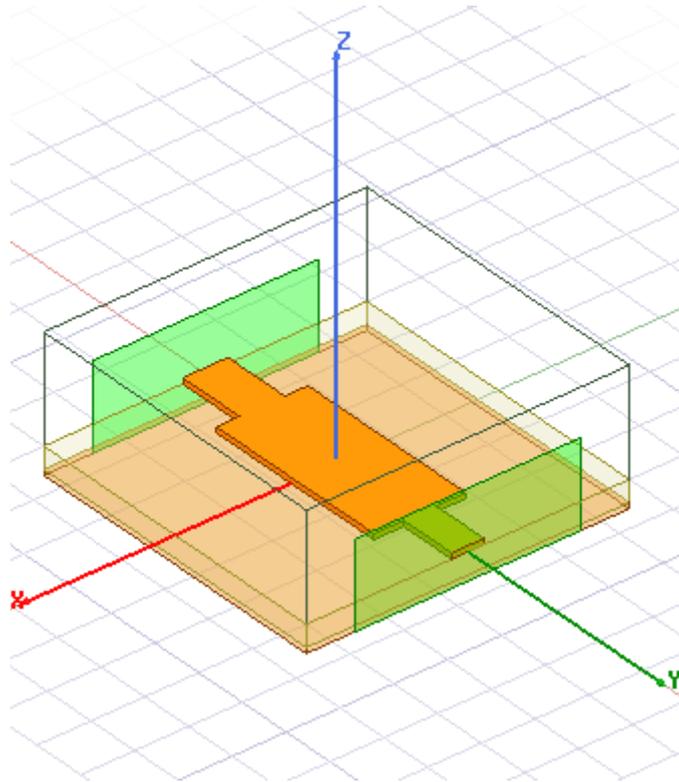


Figure 27. HFSS model of RFIN compensation structure.

Table 11. RFIN compensation structure simulation results.

<b>Variation</b>	<b>0.254mm thick RO4350B substrate with copper dimensions provided in the datasheet</b>	<b>0.203mm thick RO4003C substrate with copper dimensions provided in the datasheet</b>	<b>0.203mm thick RO4003C substrate with <math>50\Omega</math> trace thickness 0.42mm instead of 0.5mm. Other dimensions same as in previous tests.</b>
<i>S11</i> at 24.000GHz, dB	-11.06	-10.10	-11.62
<i>S11</i> at 24.125GHz, dB	-10.92	-9.97	-11.45
<i>S11</i> at 24.250GHz, dB	-10.77	-9.84	-11.28

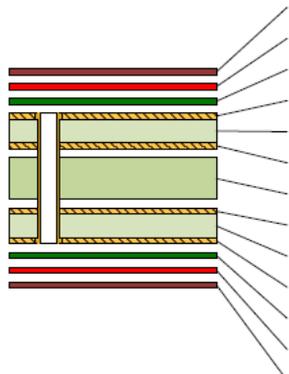
The simulation has shown that using different substrate has very little effect on the  $S_{11}$ . Maximum difference does not exceed 1dB. Because of that, the compensation structures on the manufactured PCB will have the same dimensions as in the datasheet.

LO pin is not used and is terminated with a  $49.9\Omega$  resistor.

TX pin is used in single-ended mode instead of the default differential. TXX pin is terminated with  $49.9\Omega$  resistor according to the application note instructions [page 9]. This reduces maximum TX power by 3dB.

The PCB has four layers. Top 2 layers contain high frequency circuitry and use the RO4003C dielectric between them. Layer 2 is a solid ground plane. Layers 3 and 4 only contain traces for slow signals. Layer stack is demonstrated in figure 28.

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Paste			Paste Mask	GTP
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.020mm	Solder Resist	Solder Mask	GTS
<b>Copper</b>	<b>Top Layer</b>	<b>0.053mm</b>		<b>Signal</b>	<b>GTL</b>
Core		0.203mm	RO4003C	Dielectric	
<b>Copper</b>	<b>Signal Layer 1</b>	<b>0.018mm</b>		<b>Signal</b>	<b>G1</b>
Prepreg		0.360mm	FR4	Dielectric	
<b>Copper</b>	<b>Signal Layer 2</b>	<b>0.018mm</b>		<b>Signal</b>	<b>G2</b>
Core		0.200mm	FR4	Dielectric	
<b>Copper</b>	<b>Bottom Layer</b>	<b>0.053mm</b>		<b>Signal</b>	<b>GBL</b>
Surface Material	Bottom Solder	0.020mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
	Bottom Paste			Paste Mask	GBP

Total thickness: 0.945mm

Figure 28. Radar PCB layer stack.

The PCB dimensions are 58mm by 18mm. Antennas occupy the left and right sides. Electronic components are in the middle. Figures 29 and 30 show the PCB from the top and bottom sides.

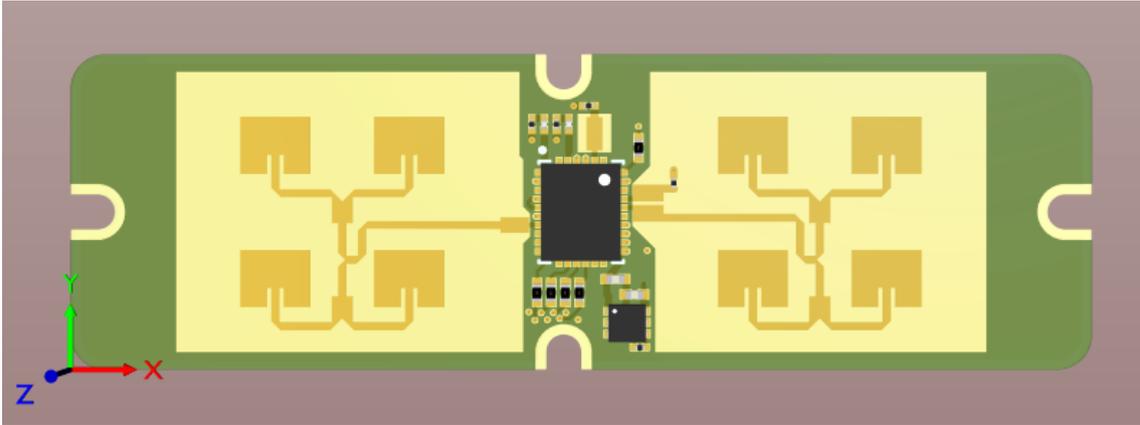


Figure 29. Radar PCB, top side.

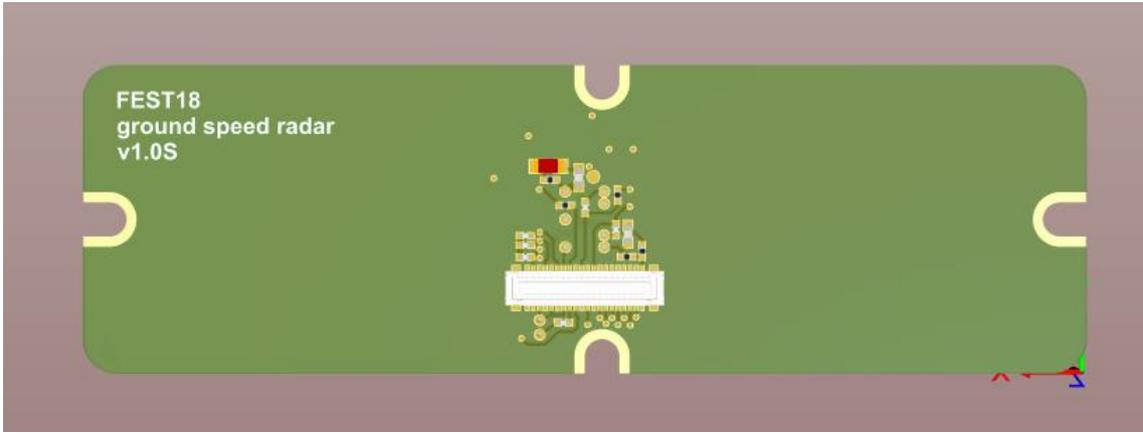


Figure 30. Radar PCB, bottom side.

## 4.2 Processor PCB design

This section addresses schematic design and PCB layout for a processor PCB.

### 4.2.1 Microcontroller

STM32F767 microcontroller was chosen in one of the previous sections. As often happens with digital components, circuit implementation consists mainly of copying example schematics from the datasheet.

Power supply decoupling closely follows the datasheet recommendations [22]. Every power pin is bypassed by a 100nF ceramic capacitor close to the pin. Further away, larger capacitor is present. Two 3.3V power supplies are used, one for analog circuits and other for digital. Separate analog supply will reduce high frequency noise component from ADC measurements. Figure 31 shows the microcontroller power supply schematic: both voltage regulators, decoupling capacitors and pins they are connected to.

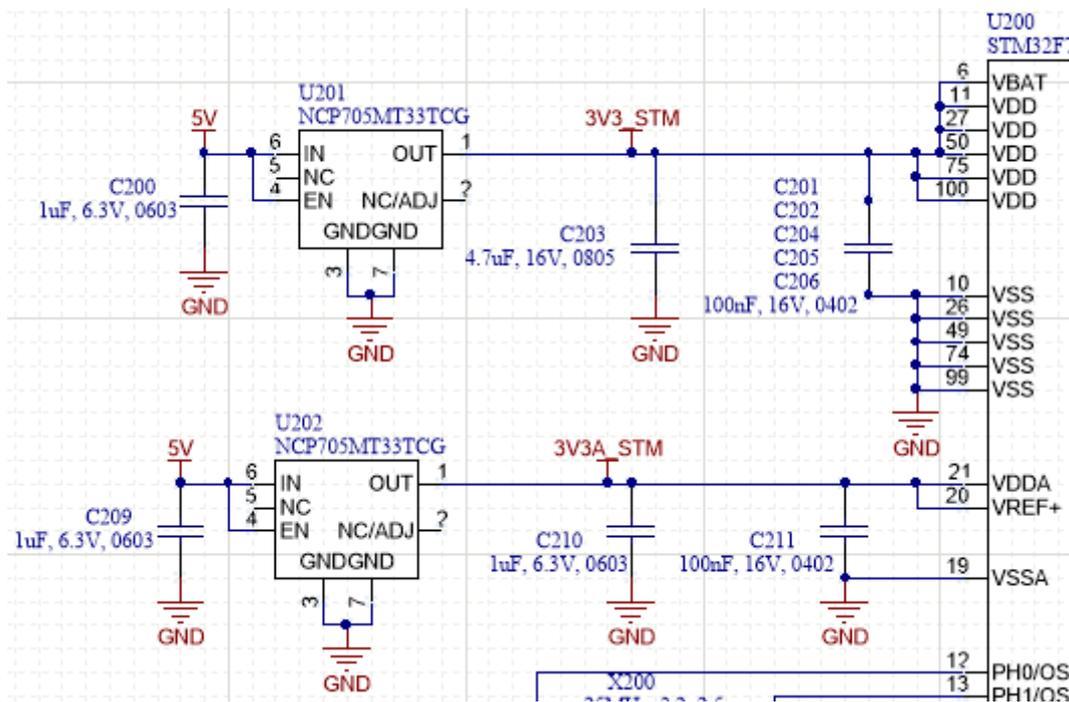


Figure 31. Schematic showing power supply of STM32F767.

25MHz crystal is chosen as a clock source. Internal PLL will increase the operating frequency to a maximum of 216MHz. Crystal load capacitance is 10pF, knowing that we can calculate the value of the capacitors needed using equation 21:

$$C = 2 \cdot C_{load} - 2 \cdot C_{stray} = 2 \cdot 10pF - 2 \cdot 1pF = 18pF \quad (21)$$

Here  $C$  is the capacitance of both capacitors and  $C_{stray}$  is estimated stray capacitance of the trace.

SWD is used for programming and debug. 5 signals are brought to a 2.54mm pin header: 3.3V, SWCLK, GND, NRST and SWDIO. BOOT0 pin functionality is not used and it is pulled to ground via 1k $\Omega$  resistor.

To assist development, UART is brought out to a separate header. It can be used to provide some debug information during development.

Two green LEDs are controlled directly by the microcontroller. STATUS LED's intended purpose is to indicate program execution status by blinking a different pattern. BUSY LED is lit up only when some function is executed to get an estimate of how much time the function takes. To assist precise time measurement with the oscilloscope a test point is added. Both LEDs are expected to be used during software development only and are contained within sealed enclosure rendering them invisible during normal use of a product.

Signals related to the radar have RC filters for noise reduction. Their values are discussed in previous sections.

Four SPI peripherals are used. Although SPI protocol supports putting several devices on a single line it is avoided here. First, separate point-to-point lines are easier to route and protect from noise. Second, timing requirements are different. Where radar SPI used for automatic gain control may require strict real-time performance at random times, memory operations will transfer large chunks of data at once. Developing software that can prioritize transmissions adds additional unnecessary development effort.

For better overview, figure 32 shows all SPI connections.

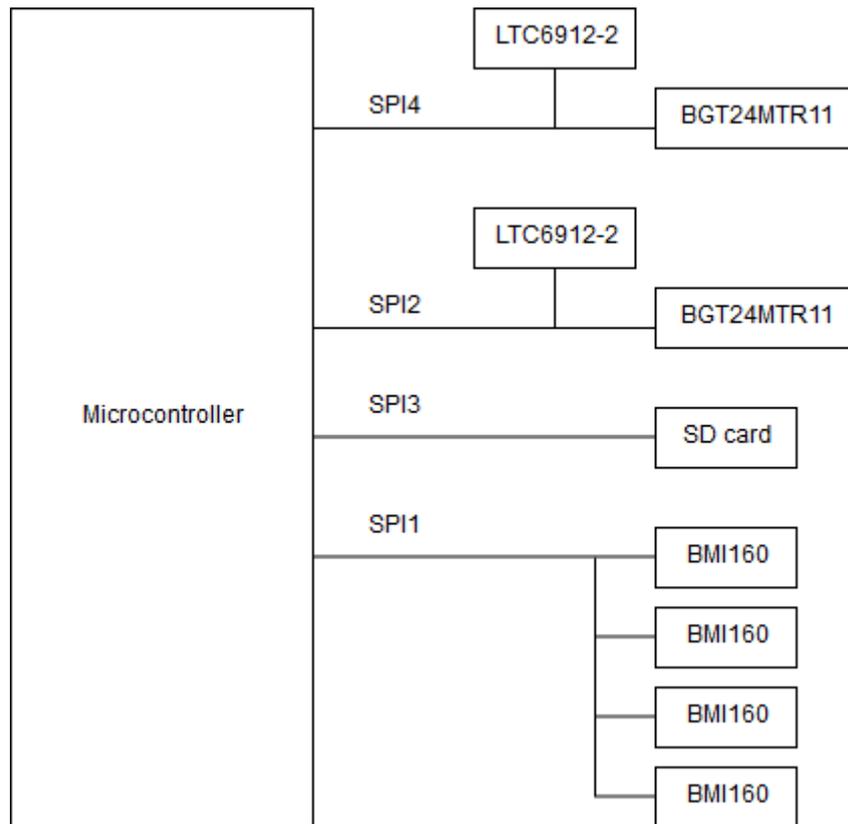


Figure 32. SPI connections overview.

The microcontroller features 3 ADCs, each having multiple channels. Since both radar signals must be measured at a strict frequency, ADC1 and ADC2 peripherals are dedicated to radar signal measurement only. All other analog signals which do not have strict timing requirements are tied to ADC3. These include temperature and RF power sensors for radar ICs as well as power rail voltage feedback signals. Voltage is measured for the following power rails: both BGT24MTR11 3.3V supplies, both LTC6912-2 3.3V supplies, SD card and BMI160 3.3V supplies. Microcontroller power supply voltage can be measured via separate internal channel. 24V and 5V rails are not measured due to lack of free ADC3 channels. Being able to remotely measure supply voltages allows quick checking is something is wrong.

#### 4.2.2 IF amplifier

Before the radar analog signals are measured by the microcontroller, some additional signal conditioning is needed.

Low pass RC filter was discussed previously.

According to the BGT24MTR11's application note [23], IF output has DC bias of 2.3V with variable  $\pm 0.2V$  offset. AC-swing may reach 1V peak-to-peak in deep saturation. Additionally, output is differential.

On the microcontroller side, ADC has working input range of 0-3.3V. To prevent clipping of an amplified signal, LTC6912-2 amplifier input signal must be biased to

$$V_{ref} = \frac{3.3V}{2} = 1.65V \quad (22)$$

A differential amplifier is used to provide the biasing and in addition to convert the differential signal to a single-ended. Block diagram of the whole analog signal path is shown in figure 33.



Figure 33. Analog signal path from radar to microcontroller

The schematic of the differential amplifier is given in figure 34.

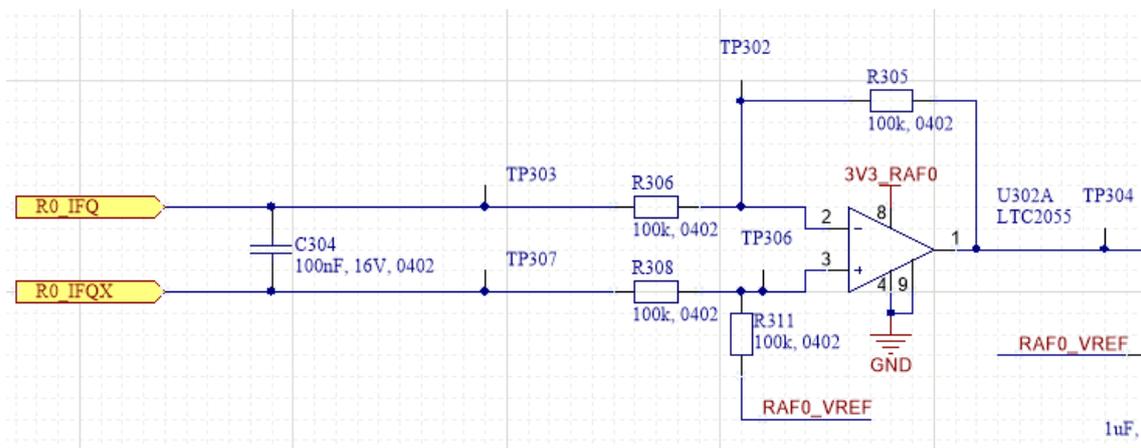


Figure 34. Differential amplifier.

The figure shows the amplifier for Q channel of one of the two radars. 4 such amplifiers are used in total.

Since all four resistors on the schematic are equal ( $R305 = R306 = R308 = R311 = 100k\Omega$ ), gain set by  $\frac{R305}{R306}$  becomes 1, and output voltage is

$$V_{out} = V_{ref} + V_2 - V_1 \quad (23)$$

where  $V_{out}$  is the output voltage,  $V_{ref}$  is the 1.65V reference from RAF0\_VREF node,  $V_2$  is voltage of a R0\_IFQX node and  $V_1$  is a voltage of a R0\_IFQ node.

The differential amplifier is built using LTC2055 operational amplifier. The LTC2055 was chosen because of compatible voltage range, rail-to-rail operation and compatible frequency bandwidth.

1.65V reference is generated by a simple voltage divider circuit as shown in figure 35. Due to low resistance values of 100Ω the voltage divider's impedance is low compared to that of the differential amplifier and thus is not affected by it in any noticeable manner.

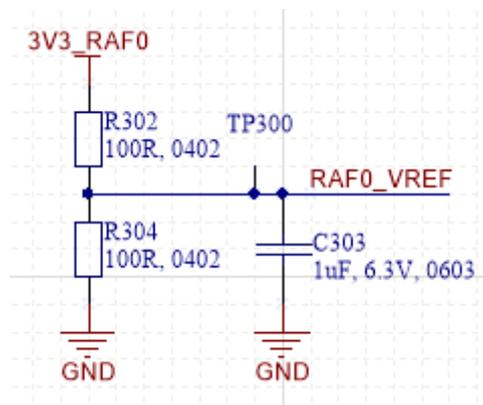


Figure 35. 1.65V reference circuit.

Same reference circuit node provides reference to the LTC6912-2.

#### 4.2.3 BMI160 inertial measurement unit

As mentioned previously, 4 BMI160 MEMS accelerometer/gyroscope components are used to assist the radar.

All 4 sensors share the same 3.3V analog supply. Each component has 2 100nF decoupling capacitors for VDD and VDDIO lines.

Additionally, all 4 sensors share same SPI line. To reduce noise, 100Ω slew rate limiting resistors are used.

INT1 pins have a test points to make them accessible in a case they are needed, however no such need is expected.

The sensors will work at a maximum frequency and store the measurement results in an internal FIFO buffer. The buffer will be read out periodically.

## 4.2.4 SD card

The schematic is simple and is shown in figure 36.

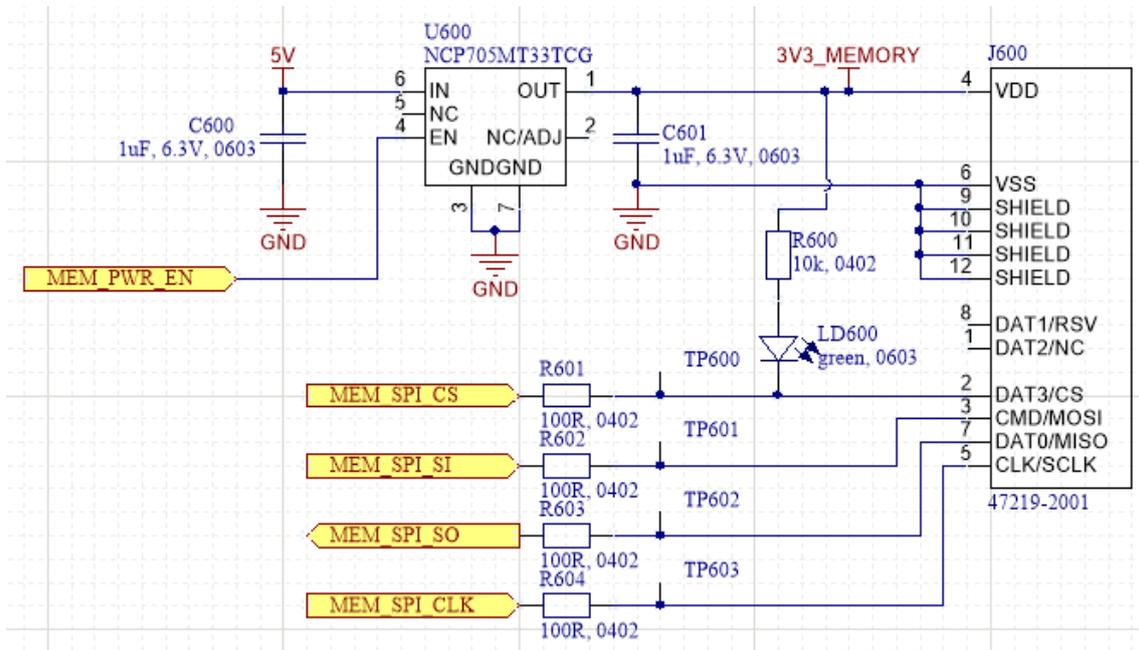


Figure 36. SD card connector schematic.

As with other components, separate 3.3V power supply is provided.

SPI lines have series 100Ω resistors that limit the slew rate and provide some ESD protection (in addition to STM32F767's built in protection). SD card is not supposed to be changed often because the radar is location is hard to access.

## 4.2.5 CAN bus

STM32F767 microcontroller has CAN peripheral which manages data link layer. For a physical layer, an external transceiver must be used. The schematic is shown in figure 37.

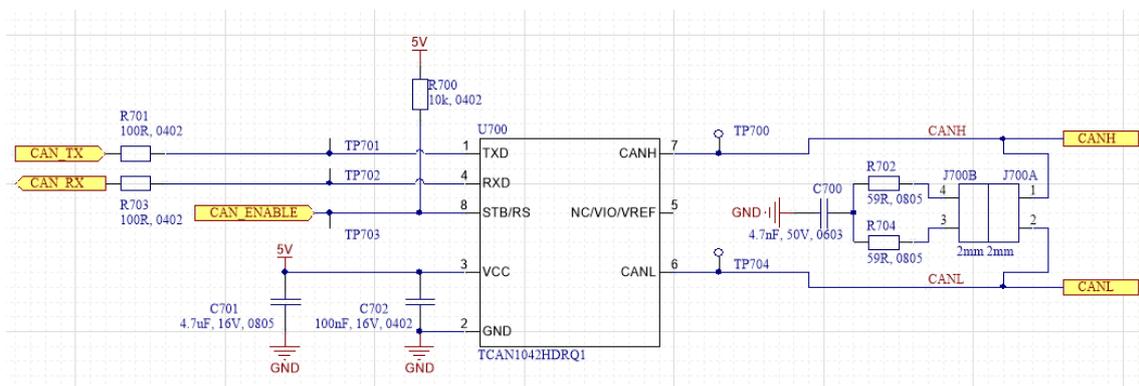


Figure 37. CAN transceiver.

Automotive grade TCAN1042HDRQ1 CAN transceiver from Texas Instruments is used. It can withstand up to  $\pm 70V$  [24], which, as discovered by our team in previous seasons, is important. Powerful cooling systems and electrical motors induce a lot of noise in a wiring which destroys less robust CAN transceivers.

The circuit has an optional split terminator which can be connected by placing jumpers on *J700* connector.

#### 4.2.6 24V to 5V step down regulator

To simplify the design effort, LTM8073 module was used. The datasheet [25] provides suggested component values for different use cases. Use case for 7-60V input and 5V output was implemented. The schematic is shown below.

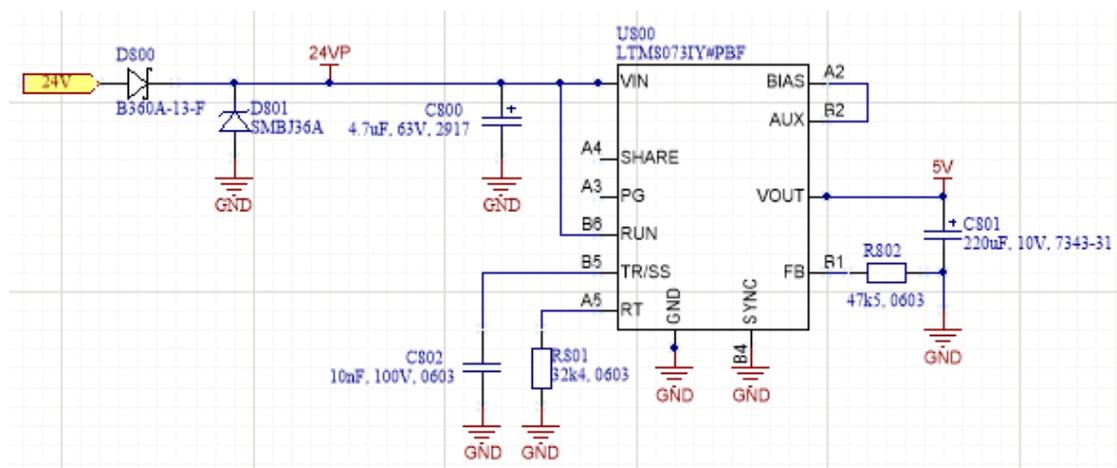


Figure 38. 24V to 5V step down converter schematic

Input is protected against reverse voltage by diode *D800*. Excessive voltage spikes are absorbed by 36V TVS *D801*. Low ESR tantalum capacitors are used for both input and output.

#### 4.2.7 PCB layout

The PCB has 4 copper layers. Top and bottom are used for signals, and two layers in the middle are solid ground planes. Power is routed as traces. All power supplies are located close to their loads so current loop areas are minimized.

Since there is no high frequency circuitry, usual FR4 stack-up is used. It is shown in figure 39.

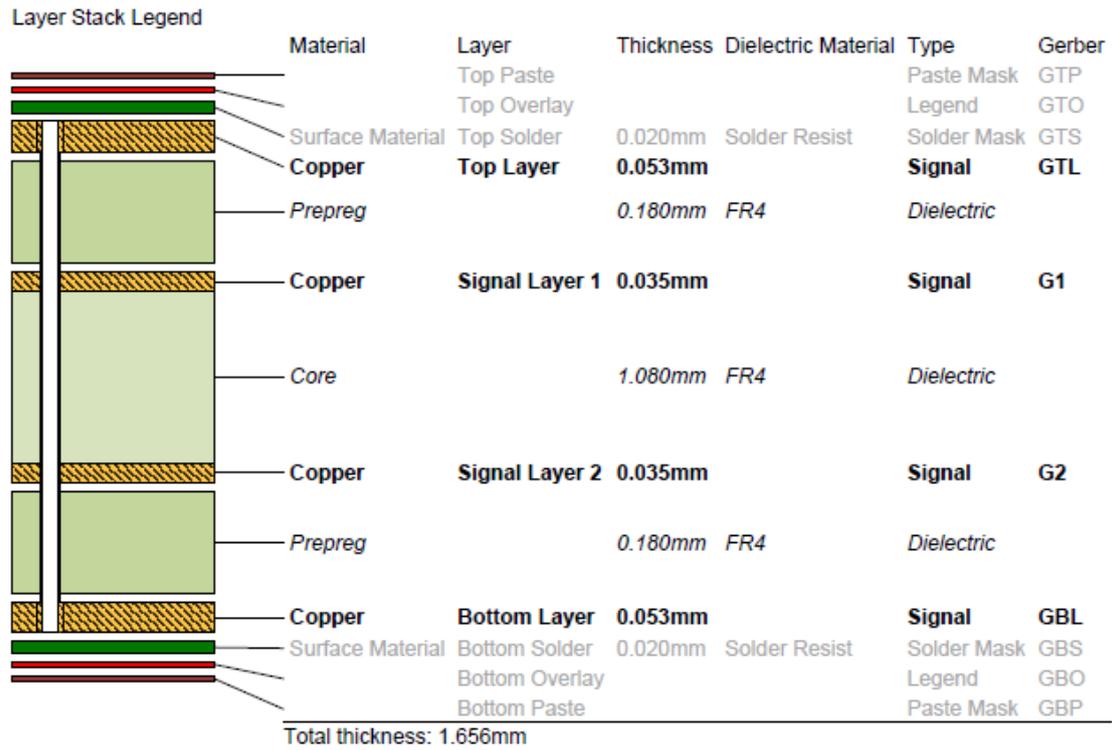


Figure 39. Processor PCB stack-up.

Figures 40 and 41 show locations of components on the PCB.

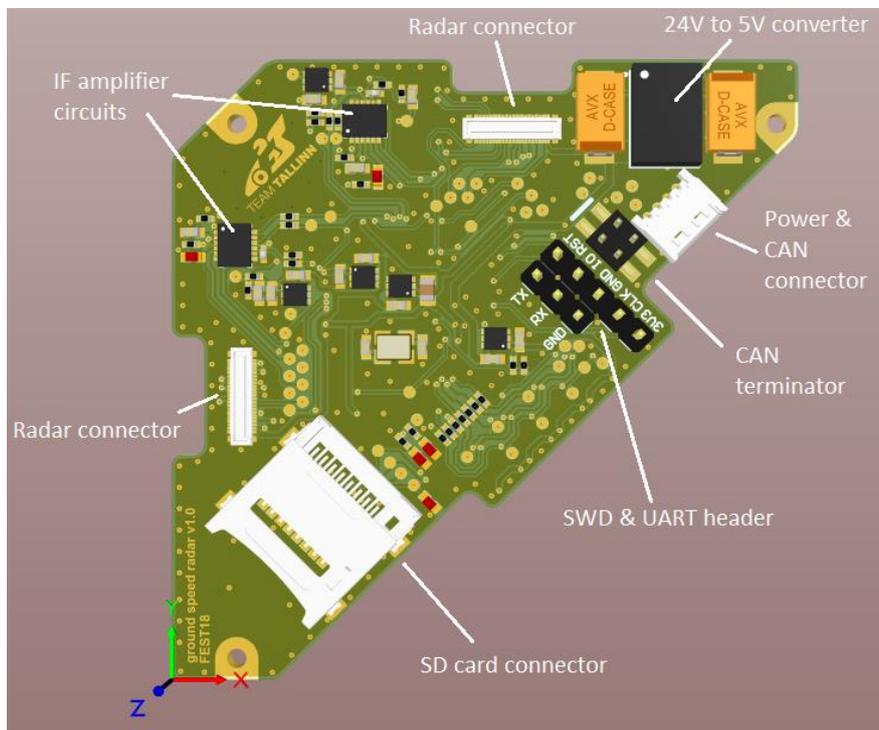


Figure 40. Processor PCB component locations, top side.

Power and CAN signals enter the PCB via a 4-pin Molex PicoBlade connector. Short 5cm wires from that connector go to the enclosure wall, which has proper automotive grade connector mounted.

Analog radar circuitry is in a corner where no high frequency signals are present. Each of the 2 radars has 14 unique signals going to the processor PCB. To fit them and provide appropriate amount of ground return paths, a single-layer flexible PCB was designed and manufactured. It uses 20-pin 0.35mm pitch Molex SlimStack series board to board connectors. Figure 42 shows the flex PCB.

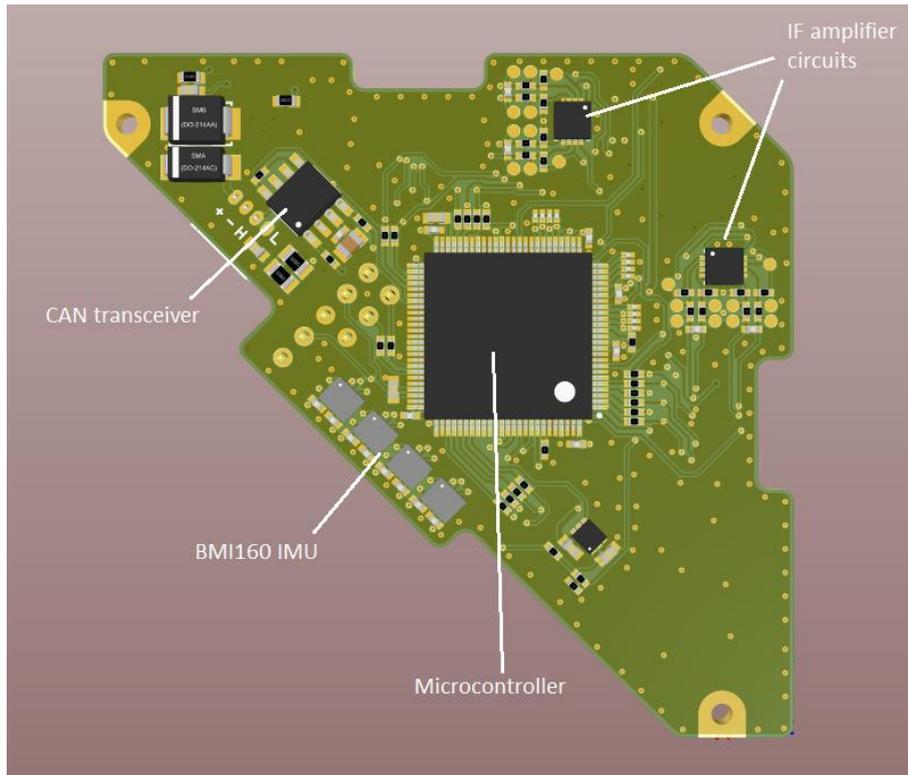


Figure 41. Processor PCB component locations, bottom side.

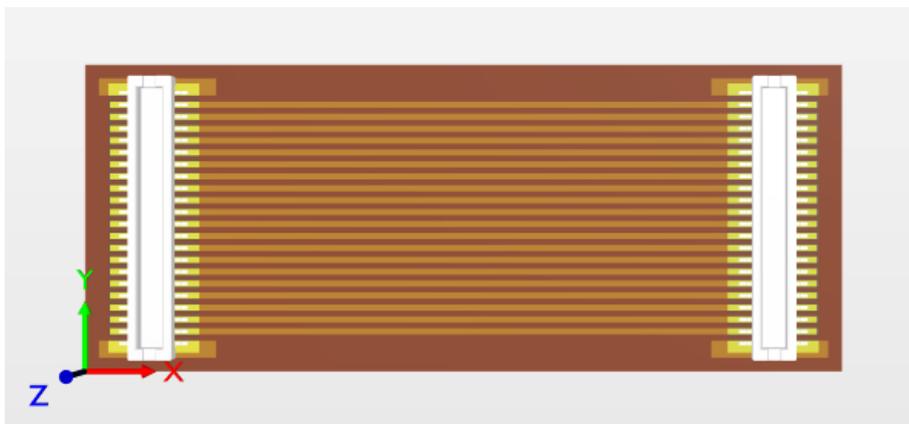


Figure 42. Flex PCB used to connect radar to the processor PCB.

The processor PCB is triangular, has dimensions on 58x58mm, and is supposed to be mounted by three M1.6 screws.

### 4.3 Enclosure

Bottom of a car is a harsh environment. A plastic enclosure was designed to protect the electronics. Its components are shown in figure 43.

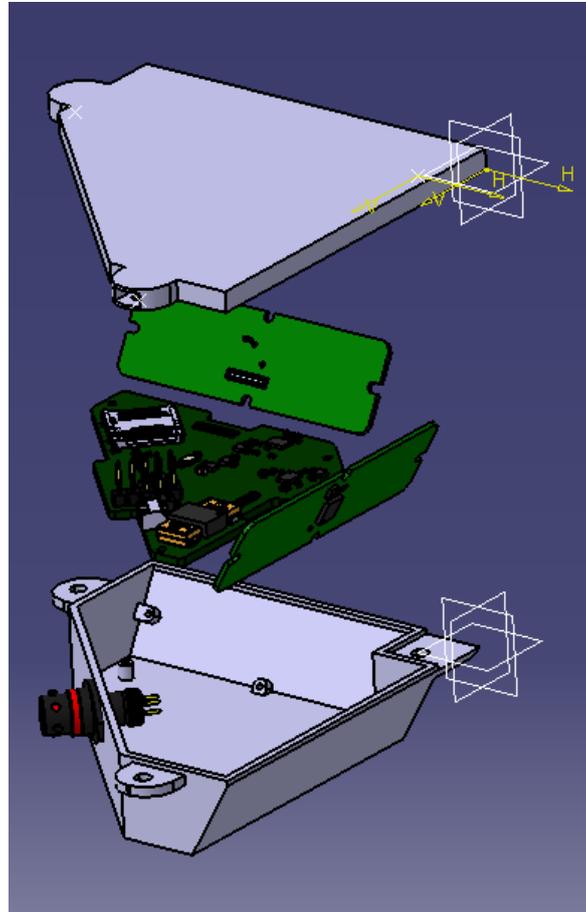


Figure 43. Radar enclosure

The enclosure consists of two parts, top and bottom. The bottom part has connection points for the PCBs, as well as mounting holes for panel mount ASX202-05SN-HE connector. This connector allows connecting the radar to the vehicle power and CAN wiring. Inside the enclosure, wires connect the ASX202-05SN-HE connector to the PicoBlade connector on the processor PCB.

Top and bottom parts are attached together with M3 bolts. 3 mounting holes are provided. A gasket can be inserted into slot between the enclosure parts. The top part of the enclosure is glued permanently to the bottom of the car.

The enclosure has dimensions of 86.4mm by 86.4mm by 20.2mm. It is manufactured using 3D printing technology. The total weight of both plastic parts is estimated to be 28 grams.

## 5 Summary

The goal of the thesis was to develop hardware for a ground speed radar for use in a Formula Student race car. The radar was required to measure car speed at frequency of at least 100Hz, with 1km/h resolution, up to 120km/h maximum speed. The radar had to determine the speed in both longitudinal and lateral axes.

Such device was developed. It is based 2 24GHz continuous wave Doppler radars, placed 90° relative to each other. Such configuration allows measuring the speed in both axes. 24GHz frequency was selected to reduce antenna size and increase Doppler frequency shift.

According to the calculations, measuring the speed at the required update rate will take at least 200ms or more. To improve that and reach the 10ms speed update rate goal, the radars are assisted by the inertial measurement unit consisting of 4 MEMS accelerometers/gyroscopes. They can measure vehicle acceleration which, after integration, can be used to estimate vehicle speed between radar measurements.

A microstrip patch antenna array was designed and simulated using Ansys HFSS. It consists of four rectangular patches with inset feed. Two such antennas are used per radar, one to transmit and another to receive the signal. The antenna is 77% efficient, has peak gain of 12.82dB and S11 at the center frequency reaches -14.33dB.

Main components in the device are 2 BTG24MTR11 radar transceiver IC's which are responsible for high frequency signal operations. After the signal is downconverted to a low frequency, it passes through an intermediate frequency amplifier. This circuitry amplifies the signal and conditions it before it gets digitized by STM32F767. The latter calculates the velocity of the car based on the radar and accelerometer data. The velocity is then transmitted via the CAN bus. The device features SD card, which allows logging the signal for further analysis.

With compact dimensions of 86.4mm by 86.4mm by 20.2mm, it is designed to be mounted under the car, near the center of mass.

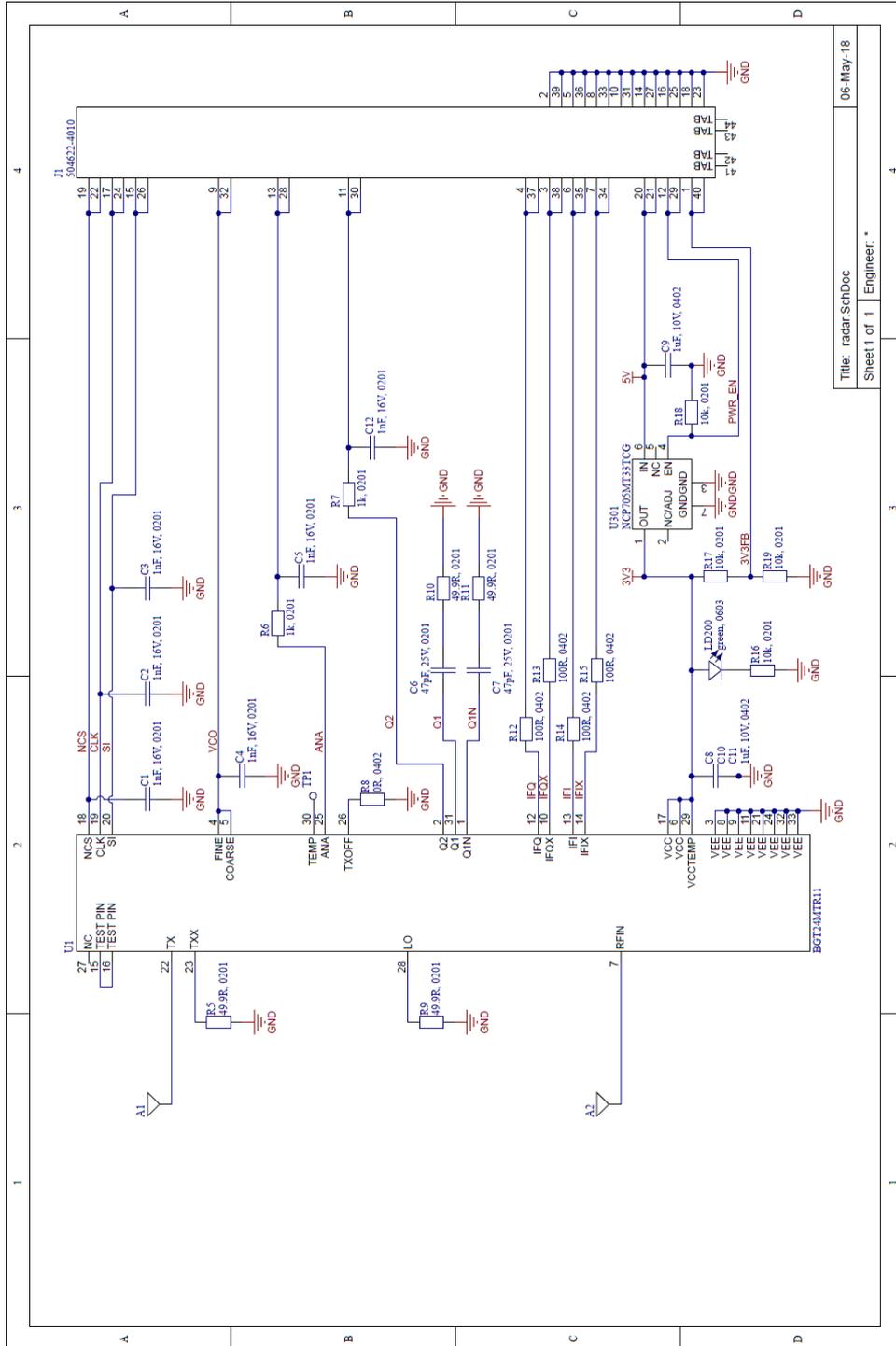
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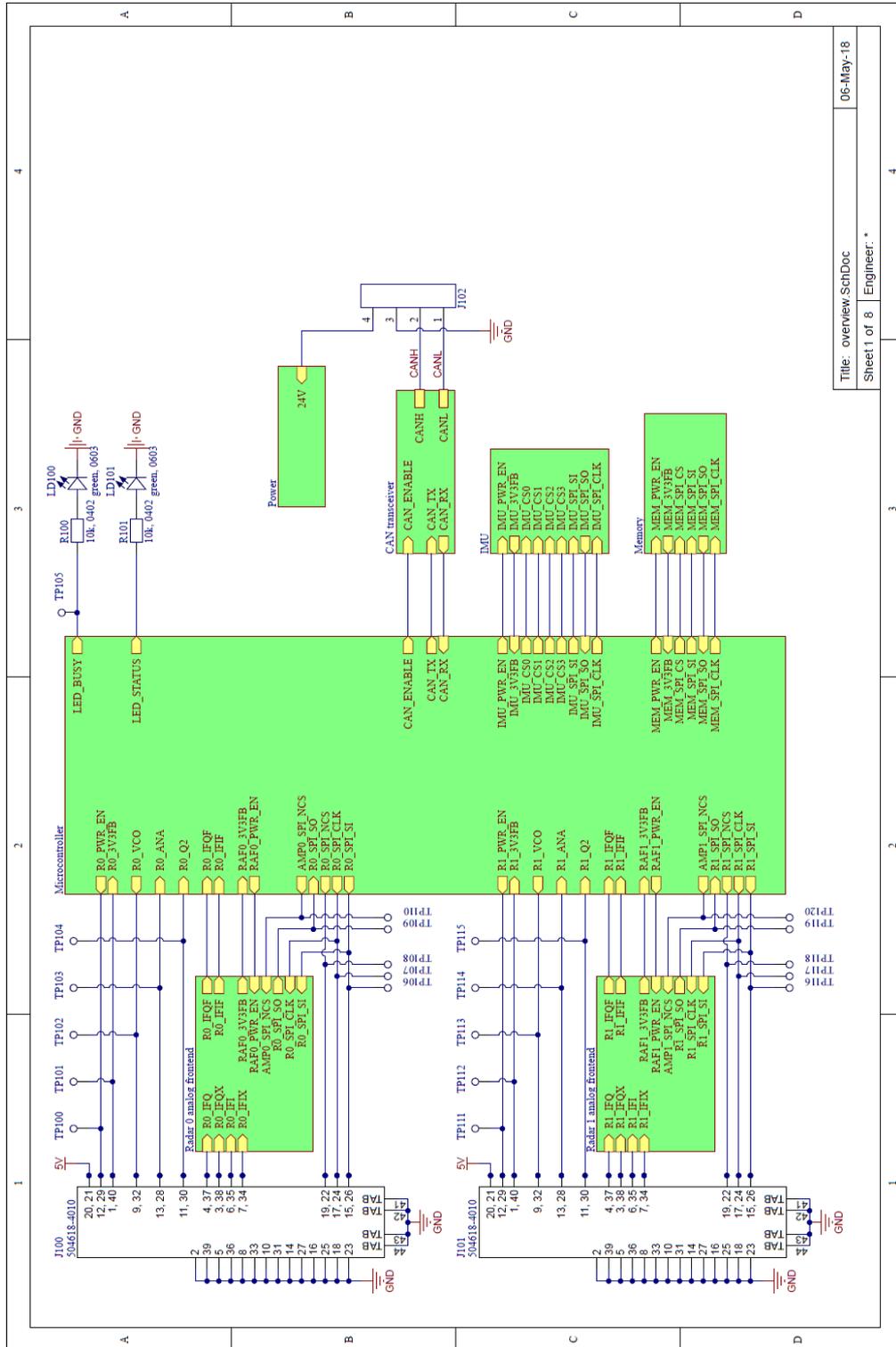
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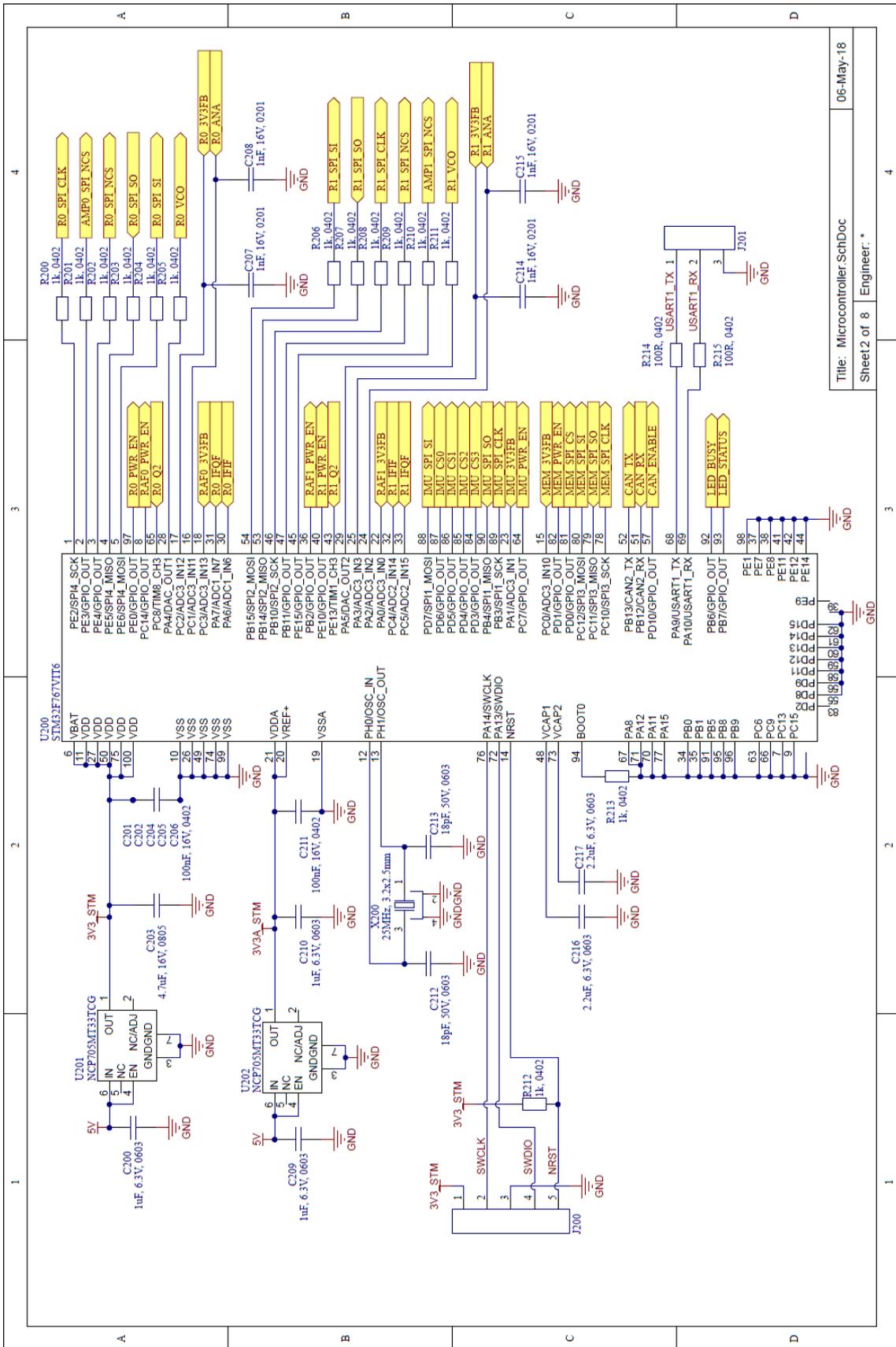
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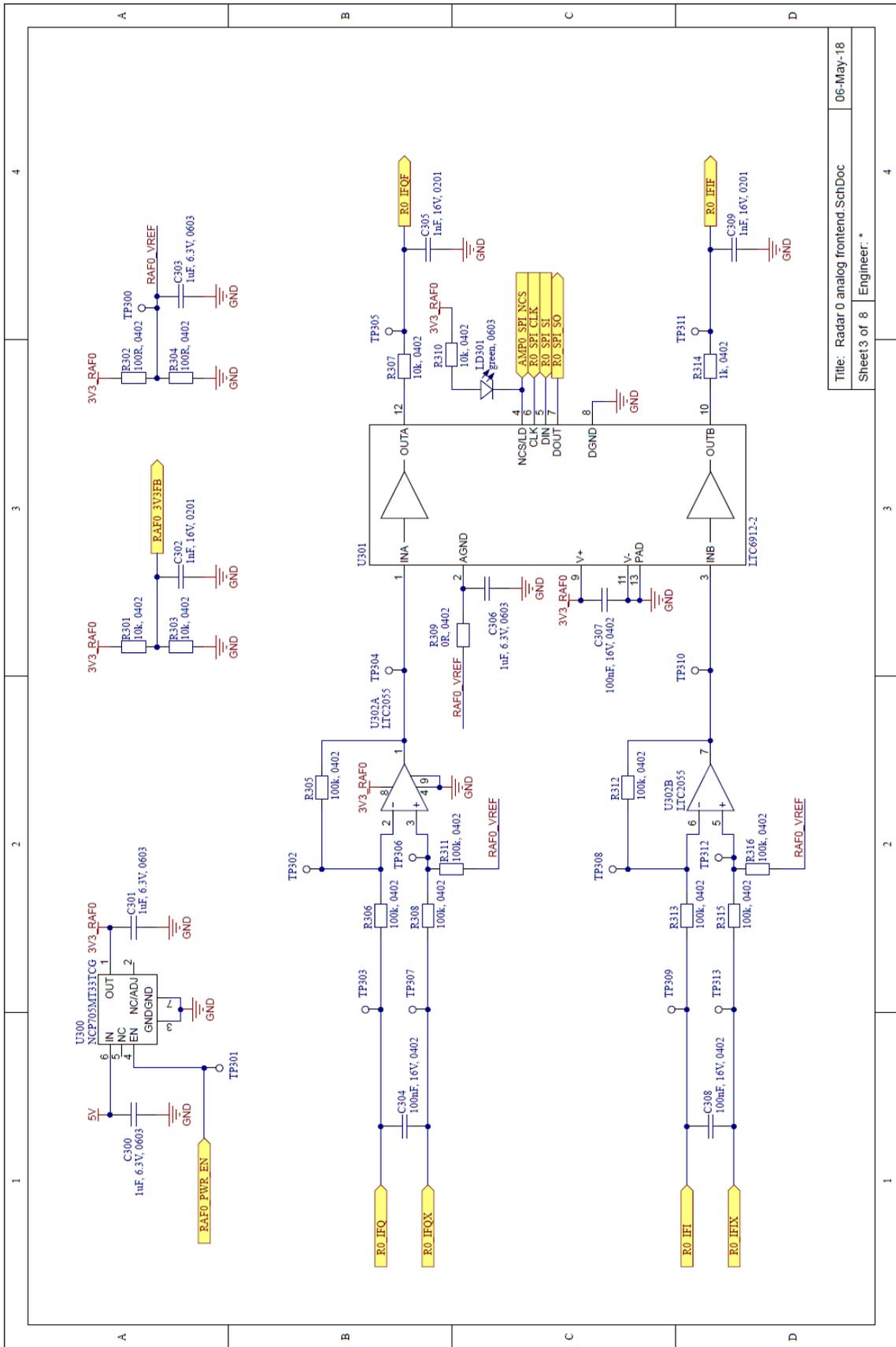
# Appendix 1 – Radar PCB schematics



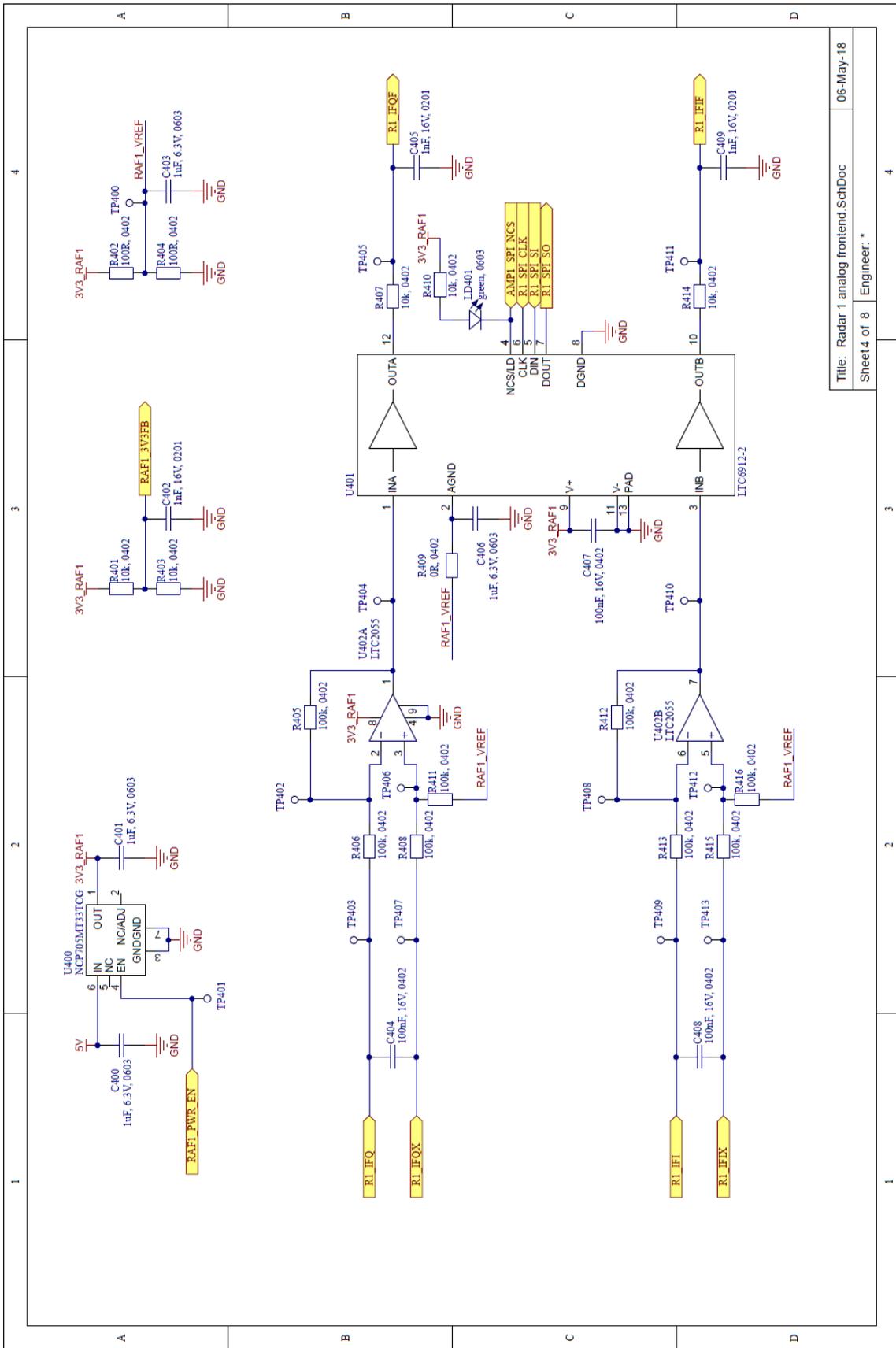
# Appendix 2 – Processor PCB schematics



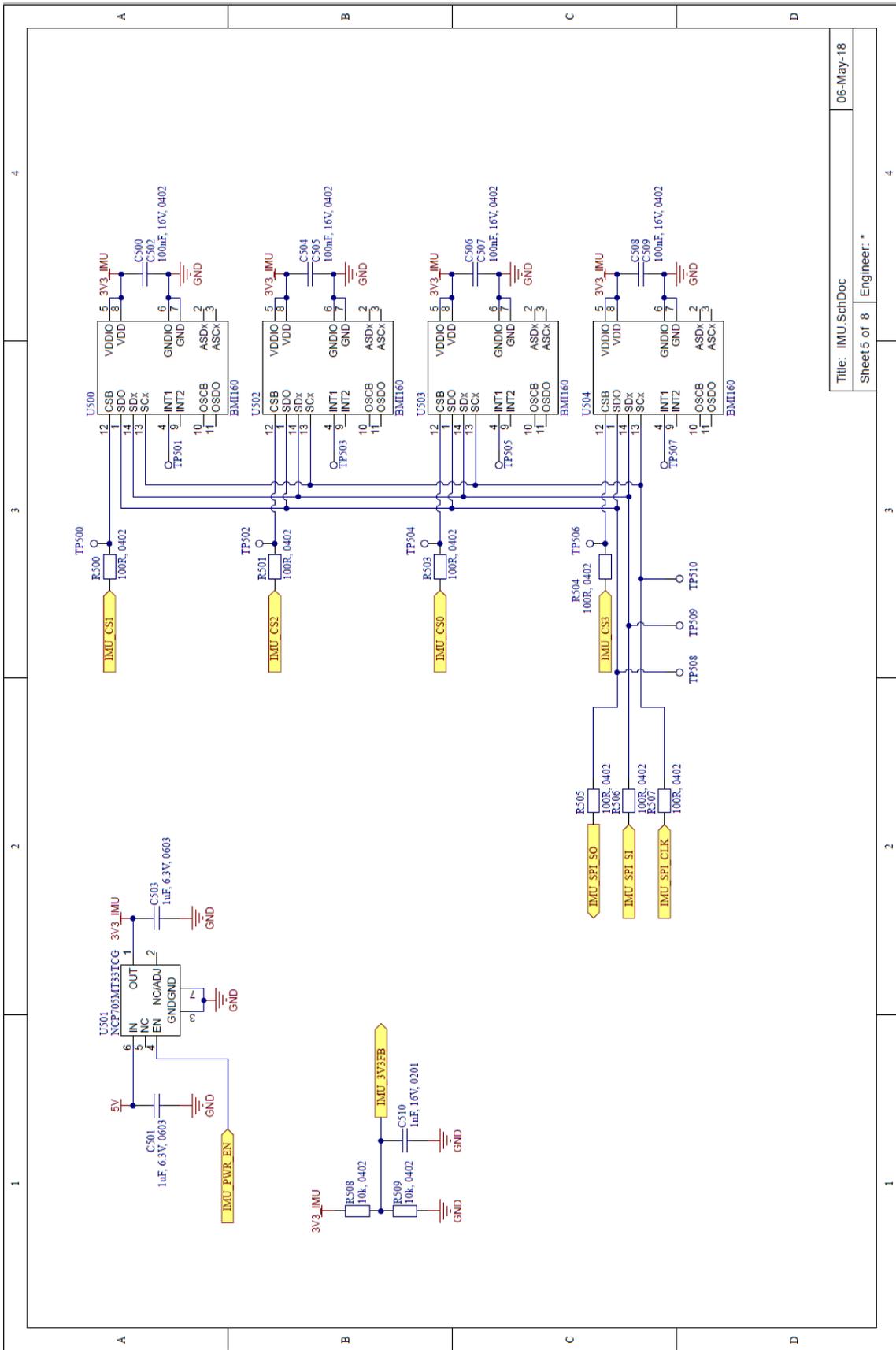




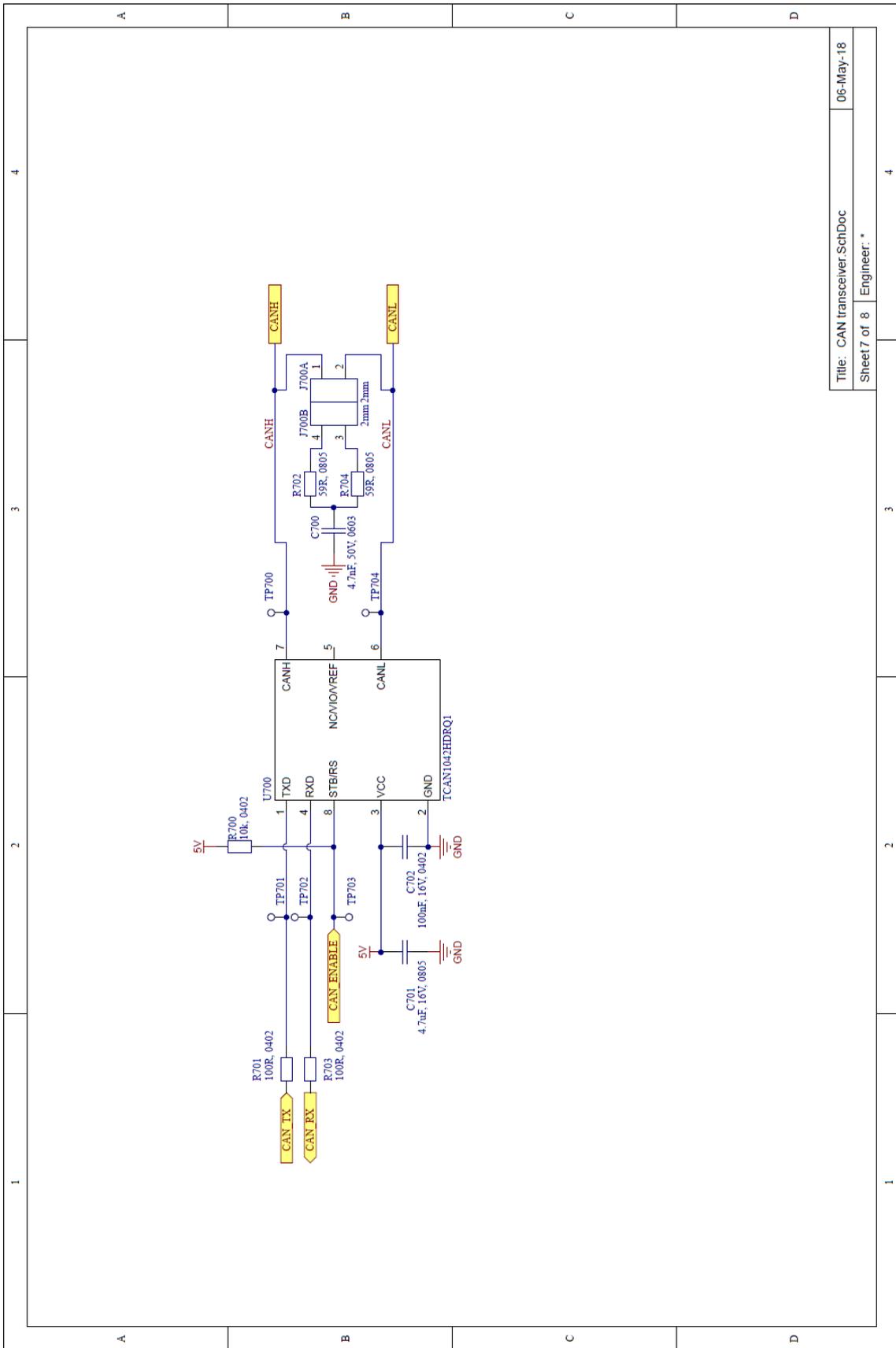
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 Engineer: \*



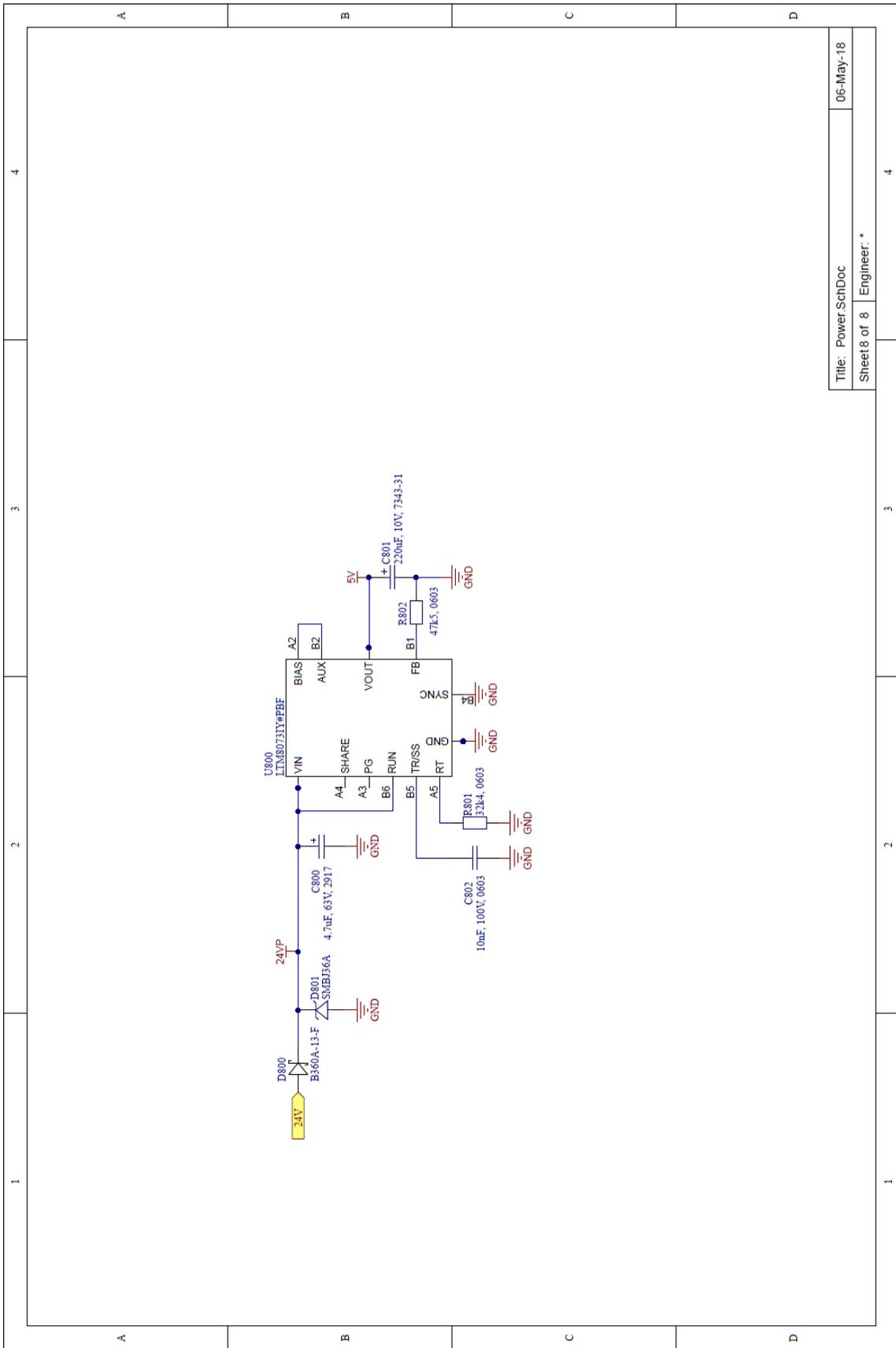
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 Engineer: \*







Title: CAN transceiver.SchDoc  
 Sheet 7 of 8  
 Engineer: \*



Title: Power.SchDoc  
 Sheet 8 of 8  
 Engineer: \*

## Appendix 3 – Radar PCB layer prints

