Investigation of Avalanche Transistor Sub-nanosecond Transient Processes in Ultra-fast Pulse Generators Using 2D Simulations of the Semiconductor Structure

Master's Thesis

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ÜLIKIIRETE IMPULSSGENERAATORITE LAVIINTRANSISTORITE SUBNANOSEKUNDILISTE SIIRDEPROTSESSIDE UURIMINE POOLJUHTSTRUKTUURI 2D SIMULATSIOONIDE ABIL

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Author’s Declaration of Originality

I hereby declare that I have written this thesis independently and the thesis has not previously been submitted for defense. All works and major viewpoints of the other authors, data from sources of literature and elsewhere used for writing this paper have been properly cited.

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Introduction

Fast electric pulse generation has been applied in a variety of different fields, including: signal processing, telecommunications and radar technology. Electric pulse generation process can generally be described as a transformation of slow or constant low-power electric input into a very short high-power output. This process is separable into two main tasks: the energy storage for further release during the pulse itself, and the switching mechanism that initiates the energy release. Over the years, there has been many approaches to these two tasks. [1, 2]

The problem of energy storage can be solved by either using capacitive storage (where energy is stored in electric field in capacitors), or using inductive storage (where energy is stored in magnetic field of inductive coils). Multiple approaches to the switching mechanism are possible: reed switch (which uses magnetic field to attract electrodes, and electric field for eventual breakdown of the medium between the electrodes), spark gap (which relies exclusively on the ionization of the medium between the electrodes due to electric field) and semiconductor based switches. Recently, due to advances in semiconductor fabrication technology, fast electric pulse generation relies more and more on the semiconductor based switching mechanisms due to their relative compactness and higher reliability, as well as better general performance. [1, 2]

On of the more popular topologies of a fast electric pulse generator is a *Marx* bank circuit. This device is able to convert a constant voltage into a short ($t < 1\,\mathrm{ns}$) high voltage ($V > 1\,\mathrm{kV}$) pulse. The working principle is as follows (see Figure 1): capacitors fulfill the energy storage task, they are charged up to some input voltage, which is slightly below the voltage required to open the switches; after the charging is complete, this static voltage is applied to every switch; slow pulse generator is used to momentarily increase voltage on the first

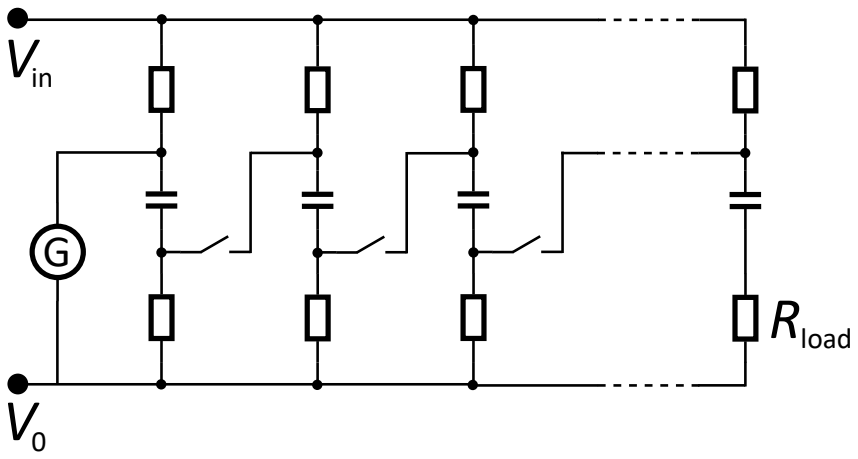

Figure 1. Circuit diagram of a Marx generator.

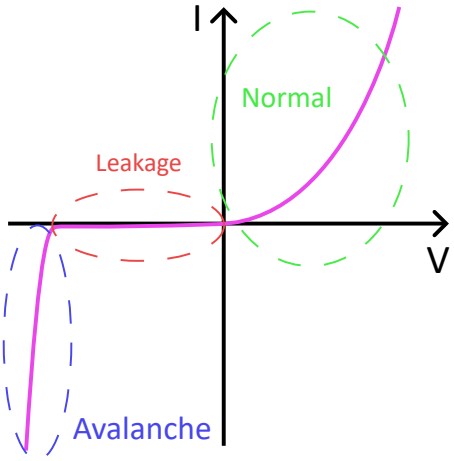

Figure 2. IV-curve of a typical diode (or a transistor in certain cases, depending on base electrode connections).

switch, thus opening it; once the first switch is open, a cascading process of switches opening occurs due to voltages on capacitors adding up; once all switches are open, a circuit with low resistance forms that passes through all switches, all capacitors, slow pulse generator and load resistance (load resistance is much smaller than all other resistances present in the circuit); thus, in case of ideal capacitors and switches, the input voltage is multiplied by the number of switches used in the circuit, and fast high voltage pulse is achieved. Traditionally, a system of spark gaps was used as switches in *Marx* bank circuits. This method, however, proved to be insufficient for extremely fast pulses due to physical size, low repetition rate and switch opening inefficiencies. Therefore, semiconductor switching mechanisms have become dominant in *Marx* bank circuits. [3, 4, 5, 6]

Semiconductor devices are generally considered to be the fundamental building block of modern electronics. The working principle of a given semiconductor depends heavily on its structure; if one has to describe it generally in a single sentence, it would be a complex motion of electrons and electron holes in silicon (or electrically similar) medium with carefully measured amounts of impurities and additives, that direct said motion. The use cases vary a lot, ranging from light generation and current direction control to complex switching mechanism of different power tolerances. In the context of fast pulse generation, the switching behavior of transistors is the most feasible approach. [7]

While transistors can be used as switches, their opening speed is relatively slow in normal operation mode, when current rises gradually with voltage. However, an interesting phenomenon is observed when a diode (or a transistor in some cases) is biased in the opposite direction: current rises extremely rapidly after passing a certain reverse voltage level. While this process is destructive for most semiconductor devices, some are designed to operate in this so called avalanche mode. Here, current stays negligible up to an avalanche breakdown voltage, at which point the current increases dramatically due to controlled ionization of the

semiconductor structure (see Figure 2). [8]

This phenomenon is extremely useful for fast electric pulse generation: an avalanche transistor or avalanche diode can be used as an extremely fast switch ($t < 200\,\mathrm{ps}$), that is able to reliably control high voltages $V > 1\,\mathrm{kV}$, thus achieving a high voltage ramp $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)$ for every pulse. [2, 4, 5, 6]

Usage of avalanche transistors as fast switches, while theoretically sound, has problems. It has been observed, that in certain conditions avalanche transistors deteriorate at an accelerated rate, or fail unexpectedly. The failure is heavily tied to improper triggering of the avalanche process: instead of electrons being injected into the structure over the whole available area, at lower voltage ramps a hot spot appears, and a current channel forms, which contributes to overheating and further deterioration. It has been shown, that this type of failure is directly tied to the geometry of a semiconductor device. [8, 9]

In this thesis, structure of an avalanche transistor **FMMT417** is investigated in the context of fast transient processes using *Silvaco TCAD*. This includes: recreation of the semiconductor structure in two dimensions, investigation of macroscopic parameters and microscopic transient behaviors of the structure in different conditions, investigation of behavior of multiple transistors in a simulated *Marx* bank circuit. [10]

1. Theoretical Framework

In this chapter, the governing equations of the simulations are presented and their choice is justified; many of the presented equations are well known in semiconductor physics, and are taken (and simplified where possible) from *Silvaco TCAD* modeling software user manuals. Next, used numerical methods are briefly mentioned. Finally, transistor internal processes are discussed. [11]

1.1 Basic Equations

Since the simulation of transient electric processes in semiconductors is almost entirely defined by movement of free charge carriers in electric field, the *Maxwell* equations cannot be avoided. In differential form, they can be written as:

$$\begin{aligned} \nabla \cdot \vec{E} &= \frac{\rho}{\varepsilon}; \\ \nabla \cdot \vec{B} &= 0; \\ \nabla \times \vec{E} &= -\frac{\partial \vec{B}}{\partial t}; \\ \nabla \times \vec{B} &= \mu\left(\vec{J} + \varepsilon \frac{\partial \vec{E}}{\partial t}\right); \end{aligned} \tag{1.1}$$

where $\vec{E}$ is electric field vector, $\vec{B}$ is magnetic field vector, ρ is electric charge density, $\vec{J}$ is electric current density, μ is magnetic permeability, and ε is electric permittivity.

For the purposes of this thesis, the impact of magnetic field inside the semiconductor structure is assumed to be negligible in comparison to the effects of the electric field. Therefore, the magnetic field is not simulated, and the structure can be reduced to two dimensions. Then (assuming, that electric field $\vec{E}$ can be expressed in terms of electrostatic potential ψ as $\vec{E} = \nabla\psi$), the only *Maxwell* equation that remains is:

$$\nabla \cdot (\nabla\psi) = \frac{\rho}{\varepsilon}. \tag{1.2}$$

Next, it is important to define charge carrier continuity equations. In semiconductor physics, the following form is often used:

$$\begin{aligned} \frac{\partial n}{\partial t} &= \frac{1}{q}\nabla \cdot \vec{J_n} + G_n - R_n; \\ \frac{\partial p}{\partial t} &= -\frac{1}{q}\nabla \cdot \vec{J_p} + G_p - R_p; \end{aligned} \tag{1.3}$$

where n is free electron concentration, p is positively charged electron hole concentration, q is the elementary charge, $\vec{J}$ is electric current density of the corresponding charge carrier, G is generation rate of the corresponding charge carrier, and R is recombination rate of the corresponding charge carrier. [7]

Finally, charge carrier transport equations have to be defined. These equations consist of two parts: carrier transport due to effective (accounts for both electric field and charge carrier statistics) electric field, and carrier diffusion. In semiconductor physics, they are often written as follows:

$$\begin{aligned} \vec{J_n} &= qn\mu_n \nabla\phi_n + qD_n \nabla n; \\ \vec{J_p} &= qp\mu_p \nabla\phi_p - qD_p \nabla p; \end{aligned} \tag{1.4}$$

where μ is mobility of the corresponding charge carrier, ϕ is quasi-Fermi potentials of the corresponding charge carriers, and D is diffusion coefficient of the corresponding charge carriers. [7, 11]

The quasi-Fermi potentials and diffusion coefficients can be expressed (using *Maxwell-Boltzmann* statistics) as follows:

$$\begin{aligned} \phi_n &= \psi - \frac{k_\mathrm{B}T}{q} \ln \frac{n}{n_{ie}}; \\ \phi_p &= \psi - \frac{k_\mathrm{B}T}{q} \ln \frac{p}{n_{ie}}; \\ D_n &= \frac{k_\mathrm{B}T}{q} \mu_n; \\ D_p &= \frac{k_\mathrm{B}T}{q} \mu_p; \end{aligned} \tag{1.5}$$

where ψ is electrostatic potential, k_B is *Boltzmann* constant, T is temperature (set to $300\,\mathrm{K}$ for all simulations), n_{ie} is effective intrinsic carrier concentrations of charge carriers, and μ is respective charge carrier mobility. [11]

Thus, the main equations used in the simulation are equations 1.2, 1.3, 1.4 and 1.5. Additional models are required to define carrier generation rate, carrier recombination rate, carrier mobility and carrier intrinsic concentrations[1]. For these purposes, predefined in *Silvaco TCAD* models are used; these models are discussed in detail in the following sections. [10]

[1] It should be noted here, that all numerical coefficients presented further in this chapter are true for silicon, which is the material used in the simulations. Said numerical coefficients may be different for other materials.

1.2 Mobility Models

Mobility μ describes how easy it is for charge carriers to move inside the semiconductor lattice, and is present in equations 1.4 and 1.5. Charge carriers move[2] due to gradient of potential, but their movement is slowed down due to a number of different effects and scattering mechanisms. Thus, mobility depends on many parameters, including: electric field strength, temperature, charge carrier concentration. [11]

A distinction is made between low electric field mobility (mobility depends mostly on lattice structure, temperature and carrier concentrations) and high electric field mobility (higher energies result in increased significance of some scattering mechanism, thus reducing mobility). [11]

Low electric field carrier mobility is often written as μ_{n0} for electrons, and μ_{p0} for electron holes. Since temperature is assumed to be constant, doping concentration[3] dependent model is used. In *Silvaco TCAD*, empirical measurements of low electric field carrier mobility at temperature $T = 300\,\mathrm{K}$ are provided for some values of doping concentration, linear interpolation is used for intermediate values. This data is presented in Table 1. [11]

An important parameter for high electric field carrier mobility is the saturation velocity. As carrier velocity increases with increasing electric field strength, mobility decreases due to stronger scattering effects; thus, velocity approaches the saturation velocity – maximum velocity achievable by a charge carrier. A simplified temperature dependent model is used, so the saturation velocities are constant: $v_{sat,n} = v_{sat,p} = 1.035 \times 10^7\,\mathrm{cm \cdot s^{-1}}$. [11, 12]

Finally, field dependent mobility model at constant temperature can be defined:[4]

$$\begin{aligned} \mu_n &= \mu_{n0}\left(1 + \left(\frac{\mu_{n0}E_\parallel}{v_{sat,n}}\right)^{1.109}\right)^{-0.9017}; \\ \mu_p &= \mu_{p0}\left(1 + \left(\frac{\mu_{p0}E_\parallel}{v_{sat,p}}\right)^{1.213}\right)^{-0.8244}; \end{aligned} \tag{1.6}$$

where $E_\parallel$ is electric field magnitude in the direction of carrier motion, v_{sat} are saturation velocities of the respective charge carriers, and μ_0 are low electric field mobilities of the respective charge carriers. [11, 13, 14]

[2] Inertialess carrier velocity depends on electric field and mobility as: $\vec{v} = \pm\mu\vec{E}$, depending on the carrier charge.

[3] Doping is an impurity added to semiconductors, typically boron as electron acceptor and phosphorus as electron donor (or chemically similar elements); doping concentration is usually measured in number of atoms per volume.

[4] This model provides a smooth transition between constant mobility at low electric fields, and constant carrier velocity at high electric fields.

Table 1. Empirical mobility values at temperature $T = 300\,\mathrm{K}$ used in *Silvaco TCAD*.

Doping concentration (cm^{-3})	Electron mobility ($\mathrm{cm}^2{\cdot}\mathrm{V}^{-1}{\cdot}\mathrm{s}^{-1}$)	Hole mobility ($\mathrm{cm}^2{\cdot}\mathrm{V}^{-1}{\cdot}\mathrm{s}^{-1}$)
1.0×10^{14}	1350.0	495.0
2.0×10^{14}	1345.0	495.0
4.0×10^{14}	1335.0	495.0
6.0×10^{14}	1320.0	495.0
8.0×10^{14}	1310.0	495.0
1.0×10^{15}	1300.0	491.1
2.0×10^{15}	1248.0	487.3
4.0×10^{15}	1200.0	480.1
6.0×10^{15}	1156.0	473.3
8.0×10^{15}	1115.0	466.9
1.0×10^{16}	1076.0	460.9
2.0×10^{16}	960.0	434.8
4.0×10^{16}	845.0	396.5
6.0×10^{16}	760.0	369.2
8.0×10^{16}	720.0	348.3
1.0×10^{17}	675.0	331.5
2.0×10^{17}	524.0	279.0
4.0×10^{17}	385.0	229.8
6.0×10^{17}	321.0	213.8
8.0×10^{17}	279.0	186.9
1.0×10^{18}	252.0	178.0
2.0×10^{18}	182.5	130.0
4.0×10^{18}	140.6	90.0
6.0×10^{18}	113.6	74.5
8.0×10^{18}	99.5	66.6
1.0×10^{19}	90.5	61.0
2.0×10^{19}	86.9	55.0
4.0×10^{19}	83.4	53.7
6.0×10^{19}	78.8	52.9
8.0×10^{19}	71.6	52.4
1.0×10^{20}	67.8	52.0
2.0×10^{20}	52.0	50.8
4.0×10^{20}	35.5	49.6
6.0×10^{20}	23.6	48.9
8.0×10^{20}	19.0	48.4
1.0×10^{21}	17.8	48.0

1.3 Generation Models

Charge carrier generation process is the ionization of atoms in the semiconductor structure, which results in release of a free electron, and a free electron hole. Generation rate of electrons G_n and generation rate of electron holes G_p is present in equations 1.3. There are many

generation models available in *Silvaco TCAD*. While it is technically possible to include all of them in the simulation process, it is beneficial for the purposes of numerical stability and calculation time reduction to select the most significant generation models. [11]

The first (and, probably, the most important of all used models) selected generation model is the impact ionization model. Impact ionization process is widely considered to be the main mechanism behind avalanche operation mode of semiconductor devices. The process can be described as follows: a small number of charge carriers starts moving in high electric field, thus attaining high velocity and high energy; the charge carriers collide with bound electrons; collision results in ionization of additional charge carries; rapid multiplication of charge carriers creates a sudden increase in current in the semiconductor structure. Impact ionization rate can be expressed as:

$$G_I = \alpha_n \frac{J_n}{q} + \alpha_p \frac{J_p}{q}; \tag{1.7}$$

where α are ionization coefficients for respective charge carriers (number of carrier pairs generated per unit of distance traveled), J are current densities of respective charge carriers, and q is the elementary charge. [8, 11]

Ionization coefficients α depend on electric field, so additional model is required to define them. For this purpose, *Selberherr* impact ionization model is used (again, since temperature is assumed to be constant, some simplifications can be made):

$$\begin{aligned} \alpha_n &= A_n \mathrm{e}^{-\frac{B_n}{E_{n\parallel}}}; \\ \alpha_p &= A_p \mathrm{e}^{-\frac{B_p}{E_{p\parallel}}}; \end{aligned} \tag{1.8}$$

where $E_{n\parallel}$ is the magnitude of electric field parallel to the electron motion direction, $E_{p\parallel}$ is the magnitude of electric field parallel to the electron hole motion direction, $A_n = 7.03 \times 10^5\,\mathrm{cm}^{-1}$, $B_n = 1.231 \times 10^6\,\mathrm{V \cdot cm}^{-1}$, and A_p and B_p are parameters that depend on electric field: if $E_{p\parallel} > 4 \times 10^5\,\mathrm{V \cdot cm}^{-1}$, then $A_p = 6.71 \times 10^5\,\mathrm{cm}^{-1}$ and $B_p = 1.693 \times 10^6\,\mathrm{V \cdot cm}^{-1}$; otherwise $A_p = 1.582 \times 10^6\,\mathrm{cm}^{-1}$ and $B_p = 2.036 \times 10^6\,\mathrm{V \cdot cm}^{-1}$ (for silicon-based semiconductors). [11, 15]

The second important generation model is the band-to-band tunneling model. At very high electric fields (in avalanche semiconductors, voltage reaches hundreds of volts over sub-millimeter distances), band bending allows for direct transition of electrons from from the valence band to the conduction band, which releases a charge carrier pair. [11]

Standard band-to-band tunneling model is used:

$$G_{BBT} = A\left(\frac{E}{E_0}\right)^2 \mathrm{e}^{-\frac{B}{E}}; \tag{1.9}$$

where E is electric field magnitude, $E_0 = 1\,\mathrm{V}\cdot\mathrm{cm}^{-1}$ is a normalizing constant, $A = 9.6615 \times 10^{18}\,\mathrm{cm}^{-3}\cdot\mathrm{s}^{-1}$, and $B = 3.0 \times 10^7\,\mathrm{V}\cdot\mathrm{cm}^{-1}$. [11, 16, 17, 18, 19]

Combining these two models, we get total charge carrier generation rate: $G = G_I + G_{BBT}$.

In some cases, usually involving deep impurity levels, other quantum effects, and process speeds below $t \approx 1\,\mathrm{ps}$, generation rates of electrons G_n and electron holes G_p may differ. For the purposes of this thesis, however, such unpaired charge carrier generation effects are not simulated as they add much more complexity for insignificant benefits. Therefore, generation rates are assumed to be equal in equations 1.3: $G_n = G_p = G$.

1.4 Recombination Models

Charge carrier recombination is the process, which is essentially opposite to charge carrier generation, and charge carrier recombination rates are present in equations 1.3. For the purposes of this thesis, both used recombination models can be thought of as springs that return carrier concentration inside the semiconductor to the equilibrium (intrinsic) concentration. Intrinsic concentration calculation methods are presented later in this chapter. [11]

First used recombination model is the *Shockley-Read-Hall* trap-assisted recombination model (this is a well-known, classical recombination model)[5]:

$$R_{SRH} = \frac{np - n_{ie}^2}{\tau_p(n + n_{ie}) + \tau_n(p + n_{ie})}; \tag{1.10}$$

where n and p are respective charge carrier concentrations, n_{ie} is is effective intrinsic charge carrier concentration, and τ is respective charge carrier lifetimes (for constant temperature: $\tau_n = \tau_p = 1.0 \times 10^{-7}\,\mathrm{s}$). [11, 20, 21]

Second recombination model is used to simulate the *Auger* transitions. This transition involves interaction of multiple bound and free electrons, where energy is redistributed so to release or absorb charge carriers; the phenomenon is inherently quantum-mechanical. This recombination mechanism dominates at higher charge carrier concentrations, as well as higher electric fields; these conditions are common in semiconductors operating in avalanche mode.

[5] In trap-assisted recombination models, it is assumed that charged particle transfers from conductive band to valence band in two steps, utilizing a trap or defect within the forbidden gap of the semiconductor.

The following model is used in the simulations to quantitatively describe the effect:

$$R_A = C_n n(np - n_{ie}^2) + C_p p(np - n_{ie}^2) \tag{1.11}$$

where n and p are respective charge carrier concentrations, n_{ie} is effective intrinsic charge carrier concentration, and constants $C_n = 2.8 \times 10^{-31}\,\mathrm{cm^6 \cdot s^{-1}}$ and $C_p = 9.9 \times 10^{-32}\,\mathrm{cm^6 \cdot s^{-1}}$. [11, 15, 22, 23]

One could notice, that recombination equations allow for both negative and positive values, thus representing both recombination and generation in some cases.

Combining these two models, we get total recombination rate: $R = R_{SRH} + R_A$.

As with generation rates, effects that may create unpaired charge carriers are assumed to be negligible, so recombination rates in equations 1.3 are assumed to be equal: $R_n = R_p = R$.

1.5 Additional Models

Of the variables required for the governing equations 1.2, 1.3 and 1.4 only effective intrinsic charge carrier concentration remains undefined.

Intrinsic charge carries concentration is number of charge carriers per, typically, unit of volume when no external conditions affect the semiconductor. Intrinsic concentration depends on material type and temperature, as it is heavily related to electron state statistics. In *Silvaco TCAD*, the following model is used[6]:

$$n_{ie} = \sqrt{N_C N_V}\mathrm{e}^{-\frac{E_G}{2k_\mathrm{B}T}}; \tag{1.12}$$

where k_B is *Boltzmann* constant, $T = 300\,\mathrm{K}$ is temperature, E_G is band gap energy, $N_C = 2.752 \times 10^{19}\,\mathrm{cm^{-3}}$ is effective density of electrons in conductive state, and $N_V = 1.021 \times 10^{19}\,\mathrm{cm^{-3}}$ is effective density of electrons in valence state (in silicon at specified temperature). [11]

Band gap energy E_G in general case depends on material, temperature and doping concentration. Since temperature is assumed to be constant, $E_{G0} = 1.08\,\mathrm{eV}$ is band gap energy for silicon at low doping concentration. At high doping concentrations ($N > 1.0 \times 10^{18}\,\mathrm{cm^{-3}}$) the effect of band gap narrowing is observed. This effect can be approximated using equation:

$$\Delta E_G = E_0 \left(\ln \frac{N}{N_0} + \sqrt{\left(\ln \frac{N}{N_0} \right)^2 + \frac{1}{2}} \right); \tag{1.13}$$

[6]This model is easy to derive using *Maxwell-Boltzmann* statistics.

where N is doping concentration, and constants $N_0 = 1.0 \times 10^{17}\,\mathrm{cm}^{-3}$ and $E_0 = 9.0 \times 10^{-3}\,\mathrm{eV}$. Then modified band gap energy is $E_G = E_{G0} - \Delta E_G$. [11, 24, 25]

Spacial charge density, used in equation 1.2, is defined as: $\rho = q(p - n + N_D^+ - N_A^-)$, where q is the elementary charge, n and p are respective charge carrier densities, N_D^+ is ionized electron donor concentration, and N_A^- is ionized electron acceptor concentration. The simplest model assumes, that all impurities are fully ionized, so N_D^+ and N_A^- are equal to the doping concentrations. [11]

Final parameter used in equation 1.2 is dielectric permeability $\varepsilon = \varepsilon_r \varepsilon_0$. For silicon, relative electric permittivity $\varepsilon_r = 11.8$. [11, 26]

Finally, fundamental constant are to be given numerical values: elementary charge $q = 1.6 \times 10^{-19}\,\mathrm{C}$, electric permittivity of vacuum $\varepsilon_0 = 8.85 \times 10^{-12}\,\mathrm{F \cdot m^{-1}}$, and *Boltzmann* constant $k_\mathbf{B} = 1.38 \times 10^{-23}\,\mathrm{J \cdot K^{-1}}$. [11, 26]

Thus, every equation required for semiconductor structure modeling for the observed case (*Marx* bank circuit based on silicon bipolar junction transistors at constant temperature) has been described.

Additionally, in *Silvaco TCAD* a semiconductor structure can be connected to a simplified electric circuit consisting of linear elements. The simulation of such circuit is trivial in comparison to semiconductor structure modeling, therefore only the most basic ideas are introduced. Voltage sources have no internal resistance; resistors are ideal: $I = \frac{V}{R}$; capacitors are ideal: $Q = CV$; connections between elements have no resistance and no inductance; using $I = \frac{\mathrm{d}Q}{\mathrm{d}t}$ and *Kirchhoff* laws it is possible to construct a system of differential equations and attach it to the system of semiconductor equations. [11]

1.6 Numerical Methods

While it is possible to modify numerical methods used in simulation by *Silvaco TCAD*, the default settings proved sufficient for the purposes of this thesis. This section provides a brief overview of numerical techniques, mostly for the sake of completeness.

By combining all theoretical models, a system of nonlinear partial differential equations for every semiconductor structure point and every external simplified device is constructed. While it is possible to iterate over different parameters, such as input voltage, this approach is less numerically stable and provides limited insight into the ultra-fast transient behavior of the semiconductor. Therefore, all simulations presented in this thesis involve integration over time. [11]

A numerical solution cannot be found for a continuous semiconductor structure, thus it has to

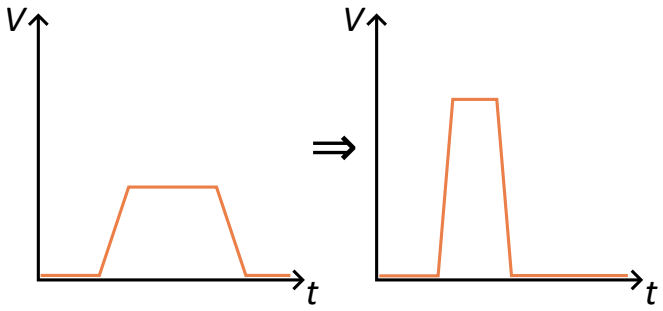

Figure 3. General principle of pulse transformation.

be discretized and later be solved using finite element method. These processes are handled internally by *Silvaco TCAD*, so practical applications of discretization techniques will be discussed in the next chapter. [11]

To acquire a unique solution, boundary conditions have to be defined. In case of semiconductor structure, in simulations completed for this thesis, boundary condition on electrodes connected to the semiconductor are defined manually; for non-electrode boundaries insulating boundary conditions are applied. [11]

In order to find solutions to the system of partial differential equations, iterative methods are used. In most cases, first-order backwards difference formula is used; for transport equations, second-order backwards difference formula is used; in both cases trapezoidal rule implementation increases accuracy. [11, 27, 28, 29, 30]

As mentioned before, almost all numerical processes are handled by *Silvaco TCAD* software. Two parameters that occasionally required modifications are: initial time step (since backwards differentiation formula allows fo adaptive time step, only reasonable initial guess was required), and relative tolerance (set to 1×10^{-6} for most simulations).

1.7 Task Overview

In modern *Marx* bank circuits (see Figure 1) avalanche transistors are often used as switches. One of the more popular avalanche transistors used in fast pulse generation applications is **FMMT417** *npn* bipolar junction transistor, as it is able to withstand high rate of ultra-fast pulse repetition without significant degradation. [9, 8, 4, 5, 6]

The purpose of an avalanche transistor in a *Marx* bank circuit can generally be described as pulse transformation: a slow low voltage pulse is compressed into a fast high voltage pulse (see Figure 3). The tail end of the pulse is mostly dependent on energy storage part of the *Marx* bank circuit, and on additional trimming processes that are beyond the scope of this thesis. The front end of the pulse depends on switching mechanism and input voltage ramp;

some of the more important parameters characterizing the output pulse front end are: pulse maximum voltage V_{max}, pulse rise time Δt, and output voltage ramp $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{out}}$.

Existing research has shown that it is possible, utilizing multiple stages of the *Marx* bank circuit, to achieve pulse maximum voltage on the order of magnitude of multiple kilovolts, and pulse rise time below $100\,\mathrm{ps}$. [4, 5, 6]

However, avalanche transistors **FMMT417** have been observed to have a tendency to degrade at accelerated rate or fail unexpectedly. Existing research suggests, that the reason is too slow input voltage ramp, which results in avalanche process not triggering properly (over the whole transistor junction area), but in weak spots, thus overheating said weak spots and damaging the semiconductor. [9]

The main aim of the simulations conducted for this thesis is to recreate previously observed phenomena in *Silvaco TCAD*, investigate semiconductor structure behavior in different conditions, and implement a comprehensive model of the whole multi-stage *Marx* bank circuit.

There are multiple mechanisms hypothesized that result in transistor opening, they are discussed below and schematically shown in Figure 4. Transistor opening in the context of this thesis means sudden voltage drop on the transistor and dramatic increase in electric current through the structure. Detailed description of the transistor structure follows in the next chapter.

First opening mechanism is standard opening with base[7]. Here, voltage on the base electrode is over the inbuilt potential of the emitter-base junction (over $0.7\,\mathrm{V}$ for silicon), which allows charge carriers to flow through the transistor by electron injection into the base and later diffusion towards the collector. This opening mechanism is slow. One way to avoid this opening mechanism is to connect emitter and base electrodes so that their voltage is always the same. However, even if emitter and base electrodes are connected, when sufficiently large voltage is applied to the collector electrode, base zone effectively behaves like a resistor between base junctions and emitter zone (see green paths in Figure 4, top), thus pushing base voltage slightly above that of emitter and creating lateral currents; since voltage of the base is then somewhere slightly above the voltage of the emitter, transistor opens in the center (red path in Figure 4, top) where voltage difference is the highest (current through blue path in Figure 4, top is negligible). This process is slow and has to be avoided: increasing base thickness w_{b} or its doping concentration is one way to decrease resistance of base zone, thus decreasing voltage difference between emitter and base. [9]

Second much faster opening mechanism is static avalanche. Avalanche opening process

[7] It should be noted that standard opening mechanism may still involve high rates of impact ionization, thus it may be classified as an avalanche process as well; the difference between the three opening mechanism is qualitative – based on speed and transistor damage likelihood.

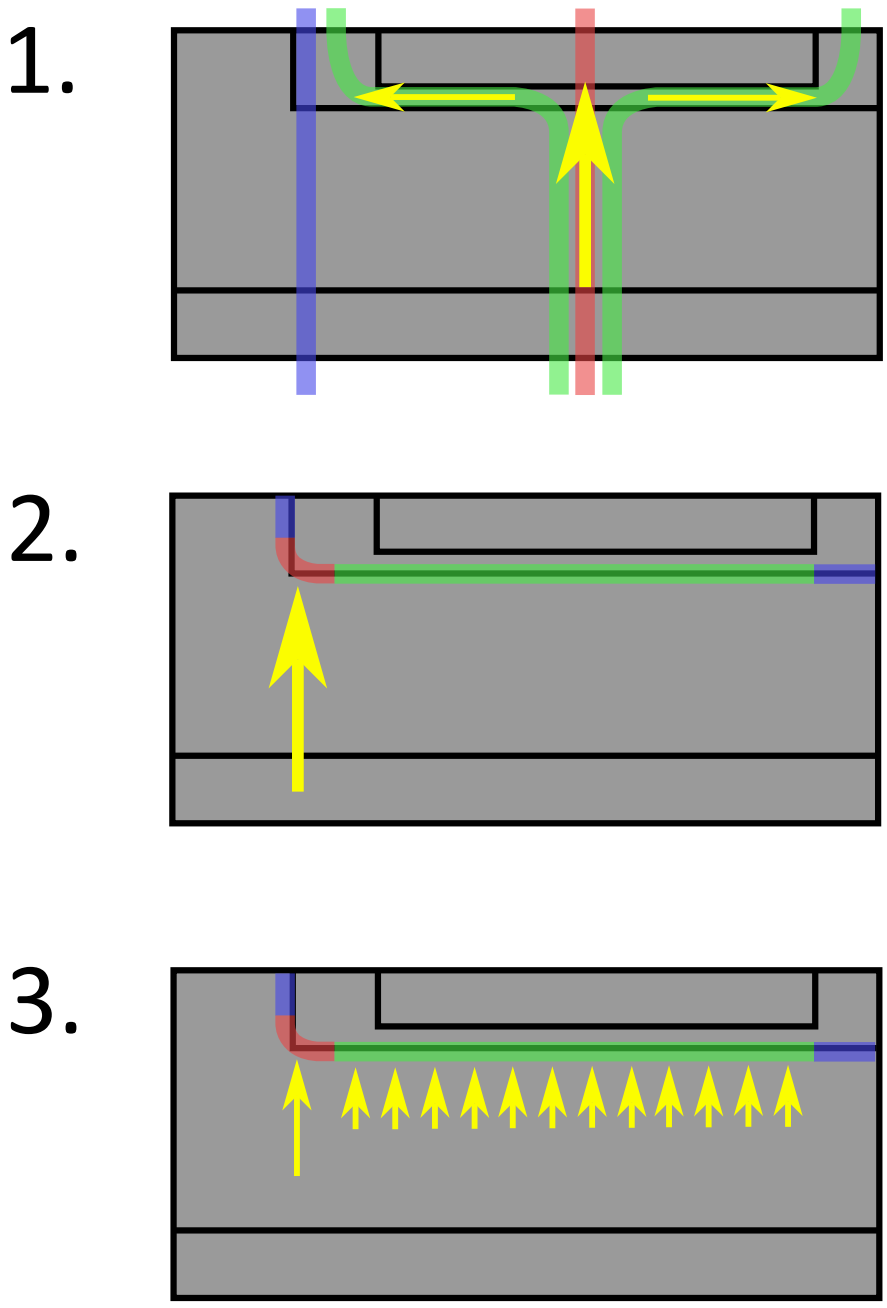

Figure 4. Standard opening mechanism (top); static avalanche opening mechanism (center); dynamic avalanche opening mechanism (bottom).

starts when a charge carrier in a sufficiently strong electric field is accelerated, colliding with electrons bound to atom orbitals, giving them enough energy to leave and thus effectively ionizing additional charge carriers which causes a chain reaction. This process is most likely to start at a point with strongest electric field, which is usually the corner of base-collector junction (red zone in Figure 4, center). In static case, avalanche starts in one spot only (current trough green and blue zones in Figure 4, center is negligible), thus creating voltage drop and reducing probability of another avalanche triggering in any other spot. Therefore, all current flows through a thin avalanche path resulting in overheating and damage. This process is to be avoided due to potential damage to the transistor. [8]

Third opening mechanism is dynamic avalanche. Here, voltage increases quickly enough to a point, where avalanches are very likely to start. First avalanche is likely to start in red zone in Figure 4, bottom. However, due to fast increase, no single avalanche has time to develop fully, thus no voltage drop is observed initially. Therefore, avalanches can start in many spot simultaneously (green zone in Figure 4, bottom), resulting in much wider current path through the transistor[8]. This is a very fast process that avoids extreme current densities, thus it is preferable in the context of *Marx* bank circuit. [8]

Existing research suggests, that processes in the transistor could be considered static when input voltage ramp $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}}$ is below $100\,\mathrm{V}\cdot\mathrm{ns}^{-1}$. Dynamic processes begin somewhere between $100\,\mathrm{V}\cdot\mathrm{ns}^{-1}$ and $2000\,\mathrm{V}\cdot\mathrm{ns}^{-1}$. Therefore, range of input voltage ramps to be explored is quite large. [9]

[8] Essentially, the difference between the second and the third mechanisms is voltage rise time: it is slower than avalanche development speed in the second mechanism, and faster than avalanche development speed in the third mechanism.

2. Modeling Process

In this chapter, the simulation parameters are presented and their choice is justified. Additionally, the simulation process is discussed in detail.

2.1 Transistor Structure

Firstly, a semiconductor structure has to be defined.

A top-down schematic of **FMMT417** avalanche transistor is presented in Figure 5 on the left. Emitter and base electrodes (**E** and **B**) are on the top of the transistor, while collector electrode (**C**) is on the bottom; an orange spot represents one of the possible points of failure. [9]

In order to construct a 2D model of the transistor, a representative slice has to be taken; this slice has to include parts of emitter, base and collector, as well as weak spots. Chosen slice is marked with a green dashed line on Figure 5 on the left; similar slice was used in preexisting research on the transistor properties. [9]

A 2D structure of the slice is shown in Figure 5 on the right. Since total area of the transistor surface is measured to be about $0.1\,\mathrm{mm}^2$, total width of the slice should be about $350\,\mu\mathrm{m}$. The structure consists of rectangular areas of different doping concentrations. Since **FMMT417** is a *npn* transistor, both emitter and collector are doped with electron donors at high concentrations (n^+, $1 \times 10^{20}\,\mathrm{cm}^{-3}$)[1], base is doped with electron acceptor at intermediate concentration (p, $1 \times 10^{17}\,\mathrm{cm}^{-3}$ or $1 \times 10^{18}\,\mathrm{cm}^{-3}$), additionally zone between collector and base is doped at

[1] In fact, this concentration is so high that emitter and collector areas can be effectively handled as conductors.

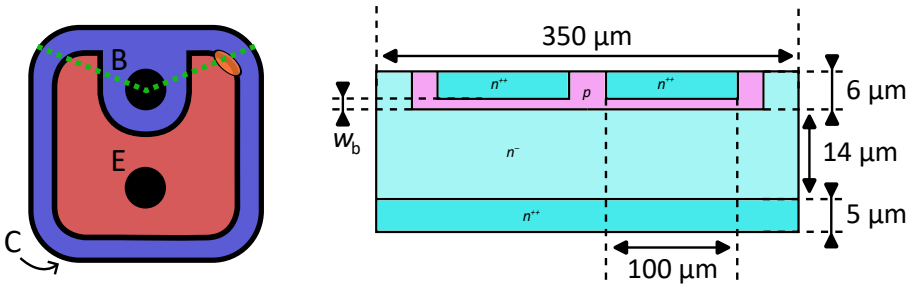

Figure 5. Top-down view of **FMMT417** avalanche transistor (left); simulated transistor slice schematic (right).

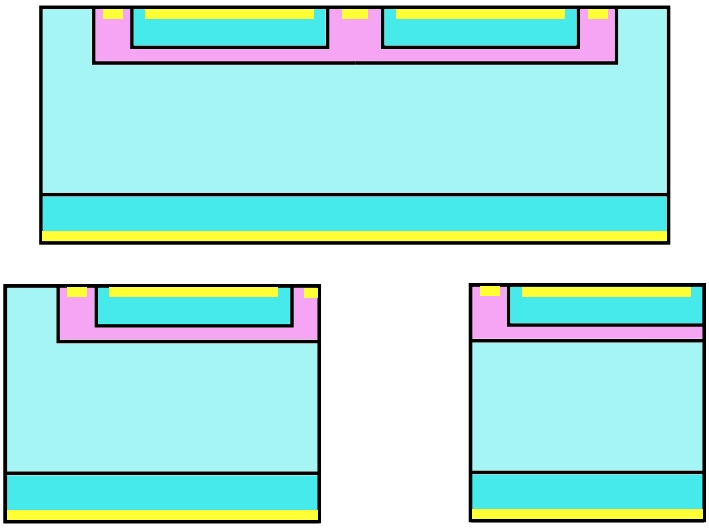

Figure 6. Full structure (top); half-structure (bottom-left); simplified structure (bottom-right).

low concentration (n^-, $1 \times 10^{14}\,\mathrm{cm}^{-3}$)[2]; the measurements (both sizes[3] and concentrations[4]) are taken from preexisting research. [9]

In reality, semiconductor devices are produced by implanting doping atoms into silicon and promoting diffusion. This process inevitably results in fuzzy boundaries between zones, and rounded corners. For the purposes of this thesis, it is assumed that non-fuzzy semiconductor structure can be used to provide meaningful insight into transient behavior of the transistor, as it is a first order 2D approximation of the internal processes[5]. This approximation can be used as a starting point in development of more accurate transistor models in the future.

While symmetric structure presented in Figure 5 can be useful for symmetry analysis and exploration of current path bifurcation, not all simulations benefit from using this structure due to increased computation time. Additionally, sharp corners between p and n^- zones may result in numerical instabilities or unrealistic results. Due to these reasons, two additional structures were defined. In Figure 6, at the top the original structure is shown, at the bottom-left the half structure is shown, at the bottom-right the simplified structure is shown; all of these were constructed by trimming down the unnecessary parts of the full structure. Additionally, yellow parts represent areas, directly on top of which electrodes are attached; notice that electrodes

[2]This low doping concentration ensures, that the main barrier on the path of the current is this central zone.

[3]Sizes not shown in Figure 5 (right): n^- zone width on the top is $30\,\mu\mathrm{m}$, p zone width on the sides is $20\,\mu\mathrm{m}$, p zone width in the center is $50\,\mu\mathrm{m}$.

[4]In semiconductor physics, doping concentration is marked with symbols n and p, sometimes with superscripts; "$++$" means borderline conductor level doping concentration, "$+$" means high doping concentration, no superscript means intermediate doping concentration, "$-$" means low doping concentration, and "$--$" means borderline isolator level doping concentration.

[5]More realistic semiconductor structure could be created in *Silvaco TCAD* using transistor production specifications; unfortunately, this data is not public for **FMMT417**.

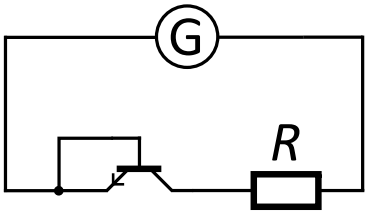

Figure 7. Circuit diagram for normal mode simulations of the transistor structure, $R = 10\,\Omega$.

do not cover the whole size of the respective semiconductor zones[6]; the contact between the semiconductor structure and electrode is assumed to be ohmic.

2.2 Simulation Tasks

Software used for simulation purposes is installed and run on a remote server. Multiple applications are included in *Silvaco TCAD*; *DeckBuild* is used to connect those applications, as well as construct, test and run simulations. [31]

The transient simulations are run using *Victory Device*. Additionally, *Victory Device* is used to define initial semiconductor structure and mesh (see Figure 6), changing the base width when needed. The structure generated in *Victory Device* is a pseudo-2D structure: its depth is assigned to $1\,\mu\mathrm{m}$. Thus, to get realistic external resistance and output current, both have to be multiplied by some value to get total top surface of the device to be equal to $0.1\,\mathrm{mm}^2$, this value is 285 for full structure and 570 for half and simplified structures. [11]

Meshes created in *Victory Device* are generally simple and overloaded with unnecessary points. The structure can be remeshed using *Victory Mesh*. Two types of meshes were tested: conformal mesh (rectangles split up into triangles by their diagonals), and *Delaunay* mesh (based on *Voronoi* diagram). In both cases, mesh cell side length is limited to $1\,\mu\mathrm{m}$ globally, as well as to $0.5\,\mu\mathrm{m}$ at semiconductor junctions, with linear change between the two. [32]

Thus, the semiconductor structure and its mesh are fully defined. Firstly, it is tested in standard mode of *Victory Device*: here, a specified voltage is applied to the electrodes of the structure and a resistor connected in series (see Figure 7). For all following simulations, all emitter and base electrodes are connected, positive voltage is applied from the collector electrode side. For all standard mode simulations, emitter-base side is held at $0\,\mathrm{V}$, collector voltage is changing in time. Firstly, collector voltage rises to $250\,\mathrm{V}$ during time of $90\,\mathrm{ns}$[7],

[6] Collector electrode covers the whole bottom part ($350\,\mu\mathrm{m}$ in the original structure); emitter electrodes are both $80\,\mu\mathrm{m}$ long, base electrodes on the sides are $10\,\mu\mathrm{m}$ wide, base electrode in the center is $30\,\mu\mathrm{m}$ long; all electrodes are centered on the respective semiconductor zones; both electrodes and isolative oxide zones are $1\,\mu\mathrm{m}$ wide.

[7] Real **FMMT417** transistor opens statically at about $300\,\mathrm{V}$, so the initial voltage is to be held slightly below that.

then additional $10\,\mathrm{ns}$ are given for the structure carrier distributions to stabilize. Then, a rapid rise to collector voltage of $550\,\mathrm{V}$ occurs (so, a total increase of $300\,\mathrm{V}$), with a specified linear voltage ramp $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}}$. Afterwards, a couple of nanoseconds are simulated in case if additional effects can be found after the ramp. In total, nine voltage ramps were defined[8], parameters of said voltage ramp simulations can be seen in Table 2. An ohmic resistor is attached to the collector electrode, its value is found by multiplying total resistance R by structure true width (either 285 or 570, depending on the structure); resistance value R is set to $10\,\Omega$. It also should be noted here, that voltage ramps are measured in $\mathrm{V}\cdot\mathrm{ns}^{-1}$ for the purposes of this thesis; due to file naming restrictions and general ease of use, a unit of $\mathrm{Vns} = \mathrm{V}\cdot\mathrm{ns}^{-1}$ is used in some cases interchangeably with the conventional unit. [11]

Table 2. Standard simulation mode conditions.

Short name	Input voltage ramp ($\mathrm{V}\cdot\mathrm{ns}^{-1}$)	Total simulation time (s)	Ramp rise time (s)
static	6	1.6×10^{-7}	5×10^{-8}
slow	100	1.06×10^{-7}	3×10^{-9}
medium	200	1.04×10^{-7}	1.5×10^{-9}
fast	400	1.02×10^{-7}	7.5×10^{-10}
faster	800	1.015×10^{-7}	3.75×10^{-10}
fastest	1600	1.015×10^{-7}	1.975×10^{-10}
rapid	4800	1.015×10^{-7}	6.25×10^{-11}
blitz	19 200	1.015×10^{-7}	1.5625×10^{-11}
bullet	96 000	1.015×10^{-7}	3.125×10^{-12}

Additionally, the semiconductor structure is to be tested in a full *Marx* bank circuit. For this purpose, the so called *Mixed Mode* is used: transient simulation of the semiconductor structure is combined with simplified models for circuit components; this functionality is included in *Victory Device*. In Figure 8, three tested circuits are presented. In all cases, $R_{\mathrm{load}} = 50\,\Omega$, R_{charge} is variable (see its transient behavior below), all other resistors $R = 10\,\mathrm{k}\Omega$, all capacitors $C = 100\,\mathrm{pF}$, generator is ideal, and all transistors are replaced with semiconductor structure models. [11]

Transient processes in the circuits are described using Figure 9; transistors are simulated fully using previously defined semiconductor structure, for all other elements simplified models are used. Firstly, capacitors have to be charged; blue charging circuit in Figure 9 shows current paths during this phase; all transistors are closed. Then, a sudden drop in voltage on the generator occurs, which causes transistors to open one by one due to charged capacitor voltages adding up[9]; the stored charge on the capacitors discharges through the discharge circuit on Figure 9; since all capacitors are connected in series in this circuit, their voltages

[8] Of the nine defined input voltage ramps, last three can be considered unrealistic or inapplicable; the simulations are still run in case if it provides additional insight into semiconductor transient processes.

[9] Since the process is extremely fast, $10\,\mathrm{k}\Omega$ resistors are effectively isolators during the discharge process.

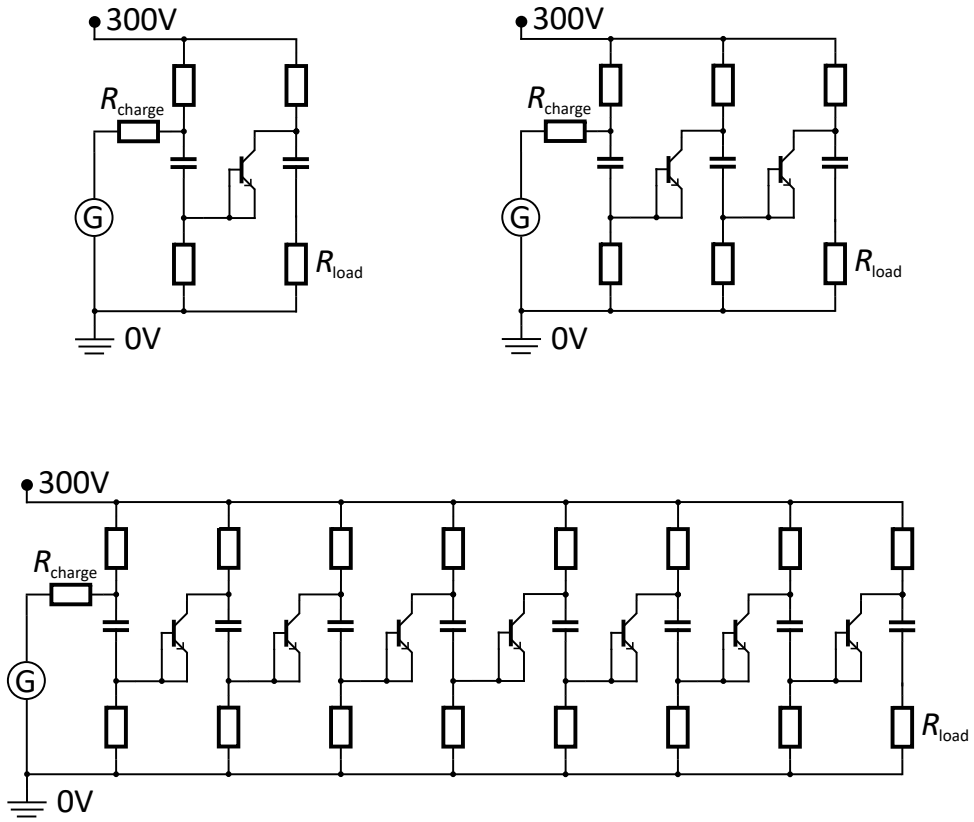

Figure 8. One transistor circuit (top-left); two transistor circuit (top-right); seven transistor circuit (bottom); $R_{\mathrm{load}} = 50\,\Omega$, R_{charge} is variable, all other resistors $R = 10\,\mathrm{k}\Omega$, all capacitors $C = 100\,\mathrm{pF}$.

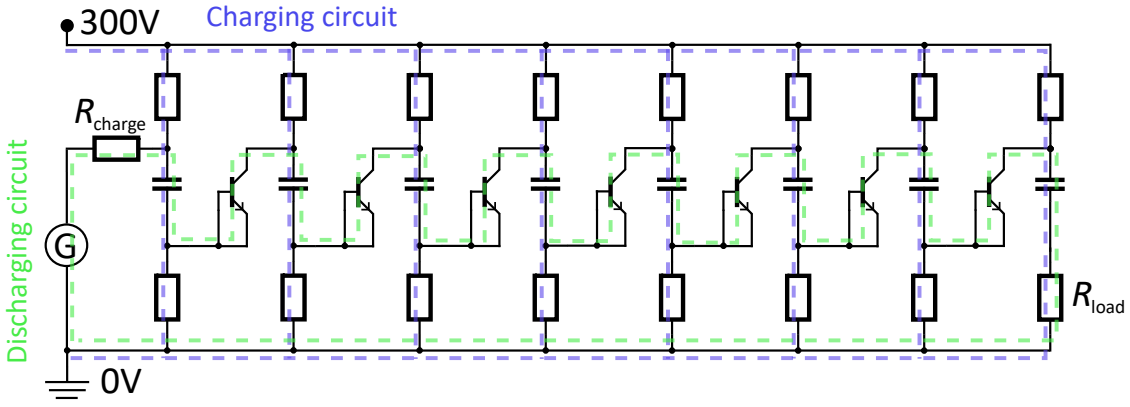

Figure 9. Charging and discharging current paths in seven transistor *Marx* bank circuit.

add up, so each next transistor experiences a faster voltage ramp; the load resistance in the end experiences a fast high-voltage pulse. Once the capacitors are discharged, transistors close and the charging process begins anew; this part is not simulated.

Generator in circuit diagram in Figures 8, 9 is meant to represent some initial slow pulse generation circuit, it can be replaced by an additional transistor (not necessarily **FMMT417**) operating in standard mode. Its maximum voltage ramp is assumed to be $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 150\,\mathrm{Vns}$, however it can be increased above that for simulation testing purposes.

Transient behavior of voltage sources and charging resistor have to be defined. Initially, all voltages are set to zero, and all capacitors are empty. To prepare the circuit for discharge, voltages on generator and positive electrode are increased linearly up to $300\,\mathrm{V}$ during $100\,\mu\mathrm{s}$; positive electrode voltage stays at $300\,\mathrm{V}$ until the end of the simulation. Additional $10\,\mathrm{ns}$ at constant voltages and resistances are given for numerical stability purposes. Charge resistor R_{charge} is put between the generator and first capacitor for numerical stability; its resistance is initially $R_{\mathrm{charge}} = 10\,\mathrm{M}\Omega$; after voltage has reached its maximal value and additional $10\,\mathrm{M}\Omega$ have passed, the resistance decreases linearly for $10\,\mathrm{ns}$ to $1\,\mathrm{m}\Omega$ and stays there until the end of the simulation; additional $10\,\mathrm{ns}$ are given for numerical stability purposes. Then, the discharge process begins: voltage on the generator drops to $-300\,\mathrm{V}$ (so a total drop of $600\,\mathrm{V}$), with a specified voltage ramp; the generator voltage stays at $-300\,\mathrm{V}$ until $110\,\mathrm{ns}$ have passed since the start of the discharge process. Then, it rises back to $300\,\mathrm{V}$ with the same voltage ramp and stays there until the end of the simulation, which occurs $130\,\mathrm{ns}$ after the start of the discharge process.

3. Simulation Results

In this chapter, simulation results are presented and discussed. Additional data analysis is done using *Python* coding language and its packages (*NumPy* for data operations, *SciPy* for interpolation, and *Matplotlib* for plotting). [33, 34, 35, 36]

Since the simulated processes are transient, it makes sense to combine multiple frames of the semiconductor structure into an animation. Full animations of results presented in this chapter can be found according to Appendix 2.

3.1 Structure Optimization

Firstly, structure mesh has to be chosen. As described in the previous chapter, the options are: conformal and *Delaunay* (see examples in Figure 10, top row).

Unfortunately, simulations of same structures in same conditions with different reasonably fine meshes yield noticeably different results[1]. Thus, the choice between the two is more significant than one would want it to be. It has been observed, that *Delaunay* mesh simulations often produce physically unexplainable artifacts (see example in Figure 10, bottom-left); similar problems have not been encountered in conformal mesh simulations (see Figure 10, bottom-right)[2]. Additionally, the structure consists of exclusively rectangular regions, so conformal mesh is expected to yield plausible results. Due to these reasons, all further simulations are made using conformal mesh structures.

Before moving on to simulation results, it is worth discussing variables that are to be extracted and analyzed. It is possible to extract macroscopic parameters saved over the whole duration of the simulation, as well as save structure files that contain parameter values at all mesh points. From the latter, electric current density $\vec{J}$, electric potential ψ, electric field $\vec{E}$, and electron density n are the main parameters to be extracted. From the former, transient time t, total electric current through the semiconductor I, voltage applied to the whole device V, and voltage applied to the semiconductor structure V_{in} are extracted; additionally, maximum output voltage ramp $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{out}}$ is calculated by taking a numerical derivative of voltage. Voltage applied to the whole device is the external voltage, it is part of the boundary conditions. On the other hand, voltage applied to the semiconductor structure, or **internal voltage**, is part of the external voltage that is *not* on the ohmic resistor ($10\,\Omega$) or other circuit elements. Initially internal and external voltages are close to equal since the transistor is closed. Once transistor

[1] In addition to artifacts, macroscopic physical parameters seem to suggest, that *Delaunay* mesh structures are more prone to avalanche opening mechanisms.

[2] In both cases in Figure 10, half-structure at $1600\,\mathrm{V ns}$ input voltage ramp was tested; artifacts and macroscopic differences have also been observed in other conditions.

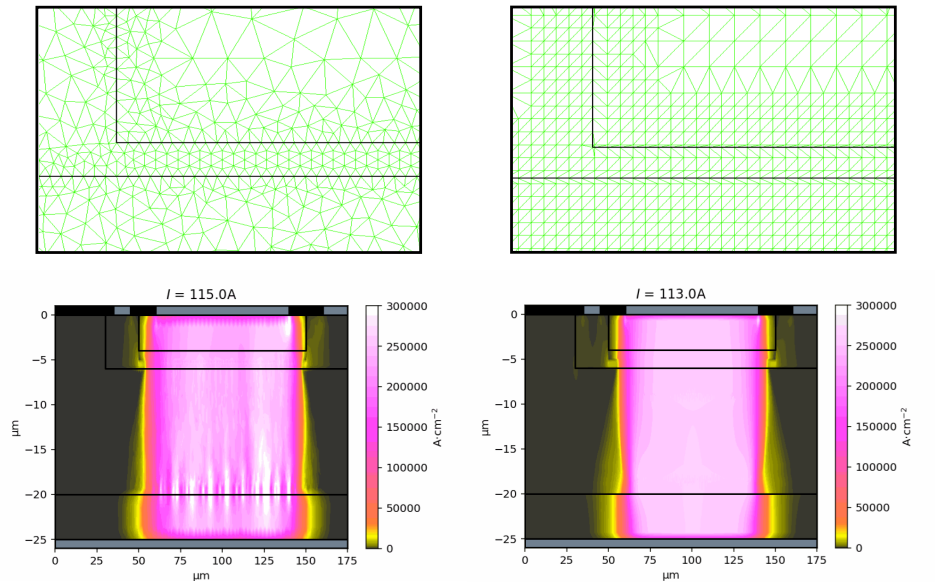

Figure 10. *Delaunay* mesh example (top-left); conformal mesh example (top-right); *Delaunay* mesh artifacts (bottom-left); lack of artifacts in case of conformal mesh (bottom-right).

opens, the ohmic resistance attached to the collector electrode becomes significant, and the internal voltage falls below the external voltage. Similar processes occur in case of circuit simulation.

While it is convenient in many cases to plot macroscopic parameters of the transistor against transient simulation time t, comparison of different input voltage ramps is difficult due to differences of orders of magnitude between voltage ramp speeds. Therefore, **normalized time scale** V_t is introduced. This scale is calculated by multiplying transient simulation time by input voltage ramp: $V_t = t\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}}$, and is measured in volts[3].

Firstly, it is important to test, which base width allows for best transistor performance, as it affects base lateral resistance, thus affecting standard opening mechanism (see previous chapter) opening voltage. Simplified structure is sufficient for this purpose. Two values are tested: $1\,\mu\mathrm{m}$ and $2\,\mu\mathrm{m}$ with constant doping concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$, nine simulations per structure are completed, according to previously presented normal mode simulation conditions. The most important results are presented in Figure 11. It can be seen that wider base structure consistently requires higher voltages for the opening process to begin, as well as in every case the opening happens in two stages: fast stage and slow stage; faster first part allows for higher output voltage ramps. Both effects can be explained by a delayed standard opening mechanism, as higher voltages are achieved and faster opening mechanism can activate. This is supported by voltage differences within the base: it is $0.5\,\mathrm{V}$ for thin base

[3]Normalized time scale can be thought of as voltage change that would occur by this point, if it was changing with input ramp speed.

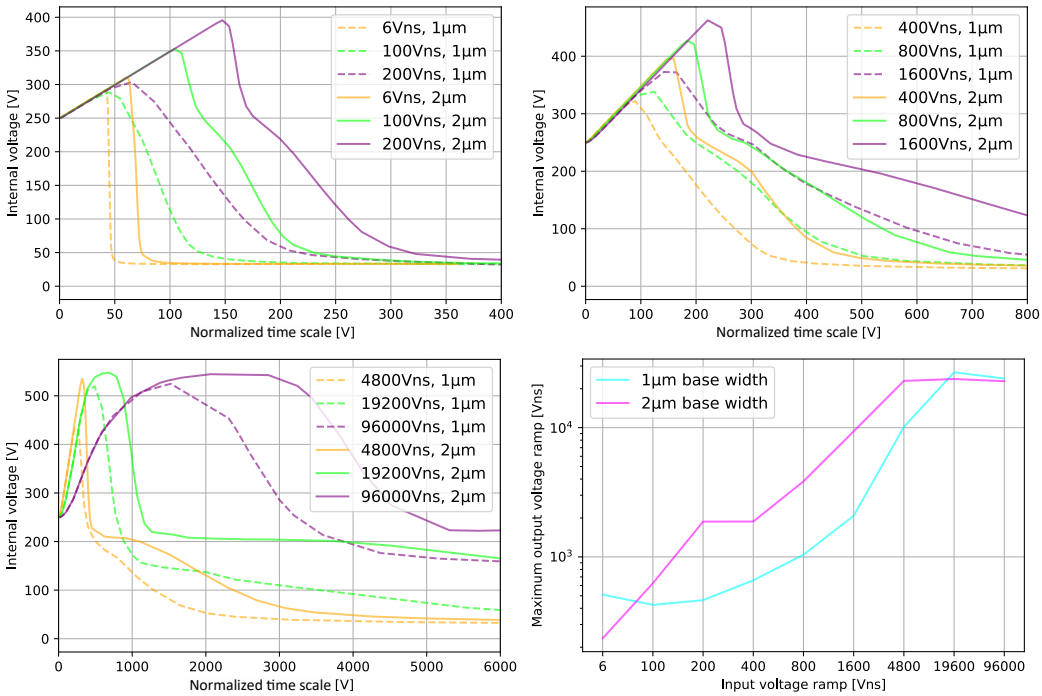

Figure 11. Comparison of main macroscopic parameters of semiconductor structures with different base widths ($1\,\mu m$ and $2\,\mu m$): internal voltage at slower input ramps (top-left), internal voltage at intermediate input ramps (top-right), internal voltage at extreme input ramps (bottom-left), output voltage ramps against input voltage ramps (bottom-right).

and $0.3\,V$ for wide base right before the opening begins[4].

From electric current distribution plots (see Figure 13, left and middle columns) it can be seen, that in static case thinner base opens near the boundary of the simulated region; this is the spot where voltage drop due to base zone resistance would be the highest – this must be standard (slow) opening process. Wider base reduces base resistance, so (presumably) avalanche opening mechanism can activate in some other spot, in this case close to the center; standard opening mechanism is still present. At higher voltage ramps the mechanisms become less distinguishable, however, at extreme voltage ramps in case of a wider base a channel appears near the corner of the structure. Previous research suggests, that this too is an avalanche. [9]

Next, different base doping concentrations are tested in same conditions. Two tested doping concentrations are: $1 \times 10^{17}\,cm^{-3}$ and $1 \times 10^{18}\,cm^{-3}$, both with base width of $1\,\mu m$[5]. Main results can be seen in Figure 12. Similarly, base resistance decrease results in a delayed opening of the transistor with a high doping concentration base. However, output voltage ramp increase is marginal compared to the previous set of simulations, and separation between two opening stages is more noticeable and bumpy, which in real devices may cause unwanted

[4]Standard opening mechanism usually activates at voltage difference between base and emitter around or slightly below $0.7\,V$

[5]Since for one of the cases base parameters are the same as for the previous set, only nine additional simulations have to be done.

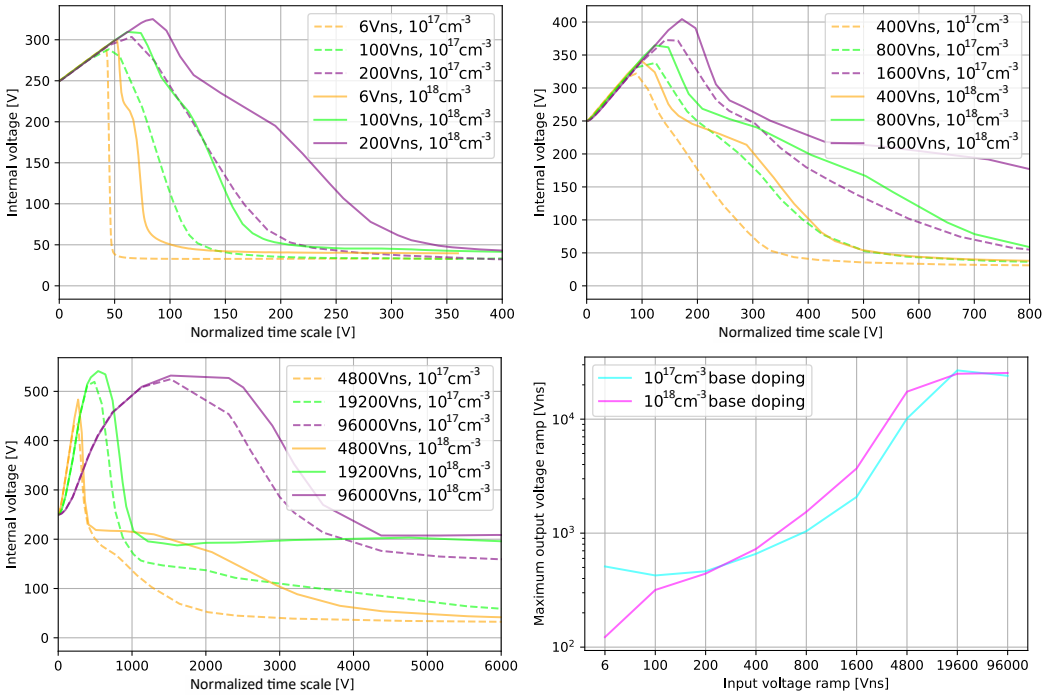

Figure 12. Comparison of main macroscopic parameters of semiconductor structures with different base doping concentrations ($1 \times 10^{17}\,\mathrm{cm}^{-3}$ and $1 \times 10^{18}\,\mathrm{cm}^{-3}$): voltage on the semiconductor at slower input ramps (top-left), voltage on the semiconductor at intermediate input ramps (top-right), voltage on the semiconductor at extreme input ramps (bottom-left), output voltage ramps against input voltage ramps (bottom-right).

oscillations. Voltage difference within base is: $0.5\,\mathrm{V}$ for low doping concentration base, and $0.7\,\mathrm{V}$ for high doping concentration base, which suggests standard opening mechanism has become stronger in the latter case.

Additionally, it can be seen in Figure 13 (comparing now middle and right columns), that highly doped base promotes avalanche in the corner in static case, and delays the electric current channel widening process (which increases current density in some regions). At higher input voltage ramps it is hard to make a distinction between opening mechanisms.

These results suggest, that while both increasing base doping concentration and increasing base width improve transistor performance in avalanche mode, width increase has more noticeable benefits and does not cause unwanted side effects. In all simulated cases, macroscopic parameters do not deviate much from realistic ones: static opening voltage is $295\,\mathrm{V}$ for thin base with low doping concentration, $310\,\mathrm{V}$ for wide base, and $300\,\mathrm{V}$ for high doping concentration base; and residual voltage (voltage that remains on the semiconductor structure after a long time[6]) is $34\,\mathrm{V}$ for thin base with low doping concentration, $33\,\mathrm{V}$ for wide base, and $40\,\mathrm{V}$ for high doping concentration base. All these parameters are realistic for **FMMT417** avalanche transistor. [37]

[6]This tail part does not fit on the graphs in case of extreme voltage ramps.

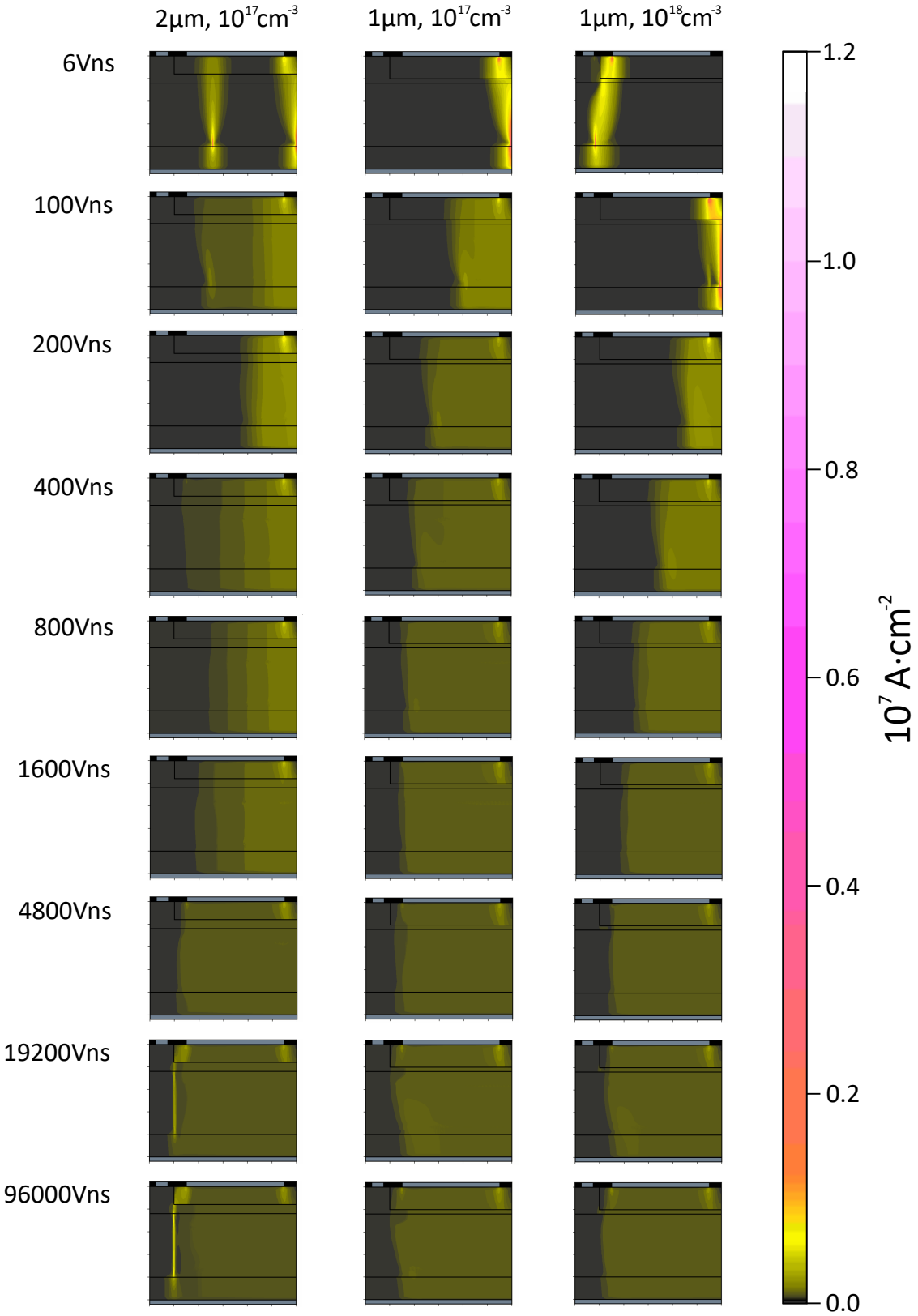

Figure 13. Electric current density distributions in three structures with different base parameters (base width and base doping concentration) in nine different input voltage ramp conditions at the moment of transistor opening (at about 30 A total current through the transistor); each structure dimensions are 120 µm on horizontal axis, and 27 µm on vertical axis.

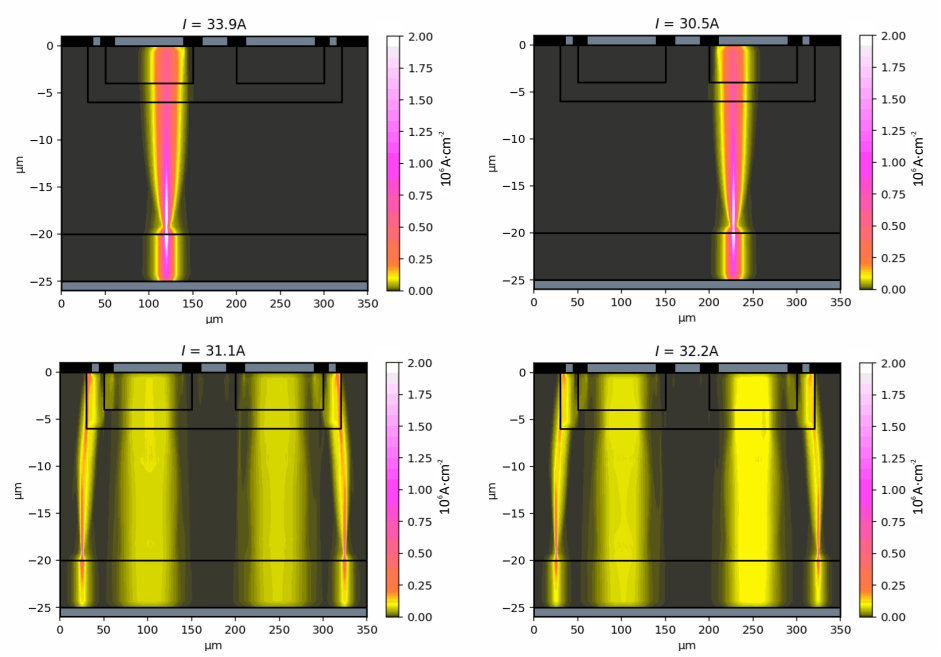

Figure 14. Electric current density distributions in two marginally different structures at two voltage ramps: static voltage ramp with left bias (top-left); static voltage ramp with right bias (top-right); faster voltage ramp with left bias (bottom-left); faster voltage ramp with right bias (bottom-right).

Secondly, it is worth investigating symmetric structure behavior. It has been observed that at lower voltage ramps current paths may open on one side of the symmetric structure, but not the other. It can be hypothesized, that due to numerical imprecisions one path is more favorable than the other and bifurcation occurs. This hypothesis can be tested by intentionally adding bias into the structure, which directs current towards one of the possible paths. For this purpose, full structure (see previous chapter) is modified by increasing low doping concentration collector zone doping by $5\,\%$ on one transistor side, and decreasing it by $5\,\%$ on the other side (biasing the doping concentration towards one side or the other). It is expected that in static case transistor will open in the higher doping concentration areas, but in dynamic case opening will be more or less evenly distributed. The results are presented in Figure 14, tests were conducted at $6\,\mathrm{Vns}$ and $800\,\mathrm{Vns}$ input voltage ramps. It can be seen that, indeed, in static case current path forms exclusively on the biased side, the standard opening mechanism probably dominates, but static avalanche mechanism still may play a role. In faster input voltage ramp case, bias influence is not significant. In both faster voltage ramps cases there are four current path: the central ones are probably tied to the standard opening mechanisms, as the voltage drop in the base zone would be the largest there; the side paths are likely formed due to the dynamic avalanche process, as electric field strength would be the highest near the corners of the structure. The fact that avalanche occurs in both corners suggests that at high input voltage ramps current would become more spread out over the transistor cross section as opposed to triggering in one single spot, which supports separation between the two

avalanche mechanisms. Lack of avalanche process activating over the whole transistor area can be explained by insufficiently fine geometry definition, which always pushes avalanches to start near the corner (area with by far the strongest electric field).

Based on results presented in this section, transistor structure used in all the following simulations can be specified:

- Conformal mesh is to be used, as *Delaunay* (triangular) mesh structures seem to be numerically unstable, more computationally demanding, or produce unexplainable artifacts;
- Base width of $2\,\mu\mathrm{m}$ is to be used, as thinner base seems to promote slower opening mechanism;
- Base doping concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ is to be used, as higher concentrations seem to promote destructive opening processes and does not significantly increase opening speed;
- Half structure (see previous chapter) is to be used, as it is more realistic than simplified structure and less computationally demanding than full structure, and tests with slightly asymmetric full structure have yielded expected results, so there is no need to simulate the full structure.

Additionally, some preliminary conclusions can be made:

- Standard opening mechanism has been observed to activate at low voltage ramps;
- Static avalanche opening mechanism is either hard to be differentiated from the standard opening mechanism, or has not been observed yet;
- Dynamic avalanche opening mechanism seems to be partially confirmed by symmetry tests, as two separate avalanche processes in two different spots were active despite bias towards one of the sides of the structure.

3.2 Transistor Simulation

With the simulated transistor structure fully defined, it is possible to move on to thorough examination of its behavior.

Internal voltage and electric current curves of the half structure transistor in nine different conditions (see previous chapter) are presented in Figure 15, normalized time scale $V_t = t\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}}$ is used, here t is true time, and $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}}$ is input voltage ramp. Internal voltages and electric currents are also presented separately with true time on the horizontal axis in Figures 16 and 17 respectively. From the static case it is possible to extract some important parameters: static opening of the transistor occurs at about $310\,\mathrm{V}$, voltage that remains on the fully open transistor is about $34\,\mathrm{V}$. Both these parameters are realistic for **FMMT417**

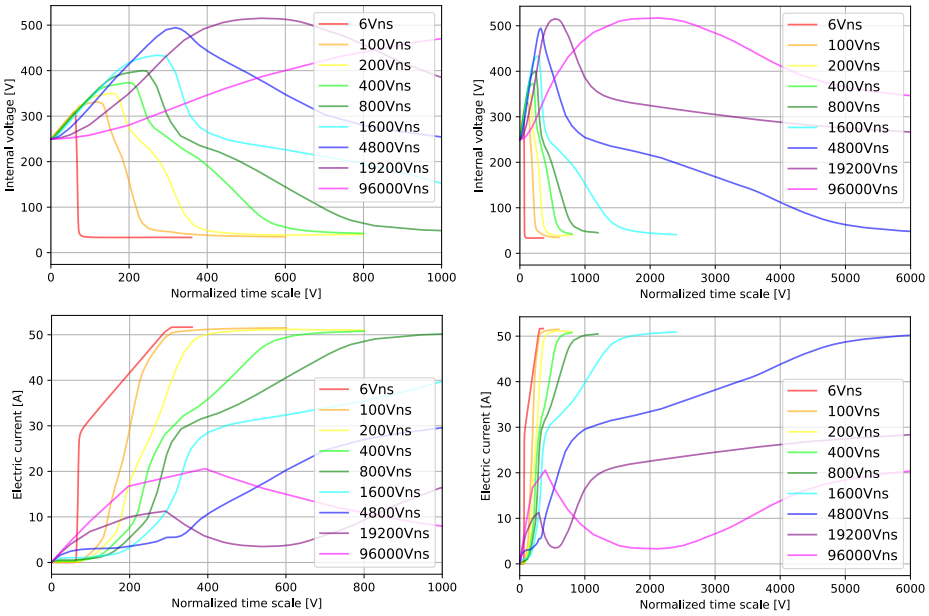

Figure 15. Internal voltage curves (top-left); internal voltage curves with extended horizontal axis (top-right); electric current curves (bottom-left); electric current curves with extended horizontal axis (bottom-right).

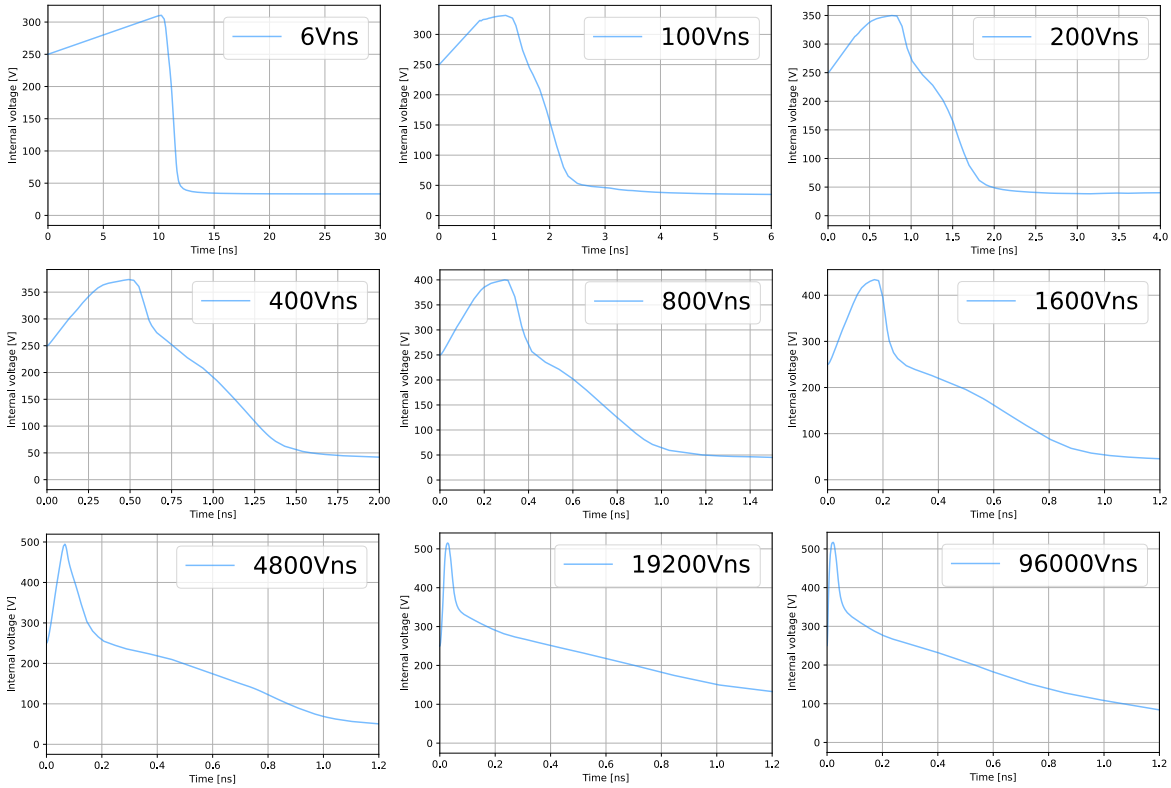

Figure 16. Internal voltages in nine different simulation cases against true time.

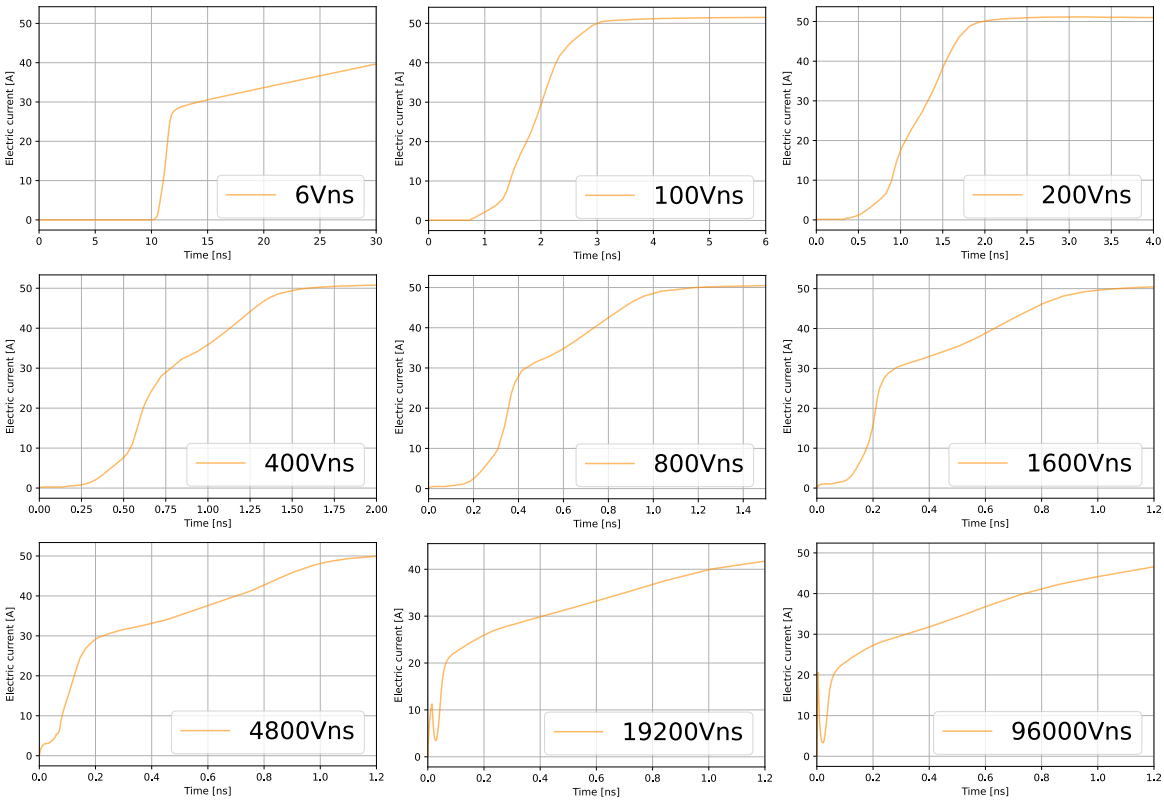

Figure 17. Electric currents in nine different simulation cases against true time.

transistor. [37]

Graphs in Figure 15 can be conveniently used to compare the transistor behavior at different input voltage ramps. Static case $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 6\,\mathrm{Vns}$ can be used as a baseline; the opening process begins at the lowest voltage, and the curves can be visually separated into three straight sections: before opening, opening process, open state; the most important part for the purposes of this thesis is the opening process part – nothing conclusive can be said about it in static case. In case of faster input voltage ramps $200\,\mathrm{Vns} \leq \left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} \leq 1600\,\mathrm{Vns}$ the opening process can be additionally separated into two distinct sections: fast and slow. In the context of *Marx* bank circuit, the faster part of the opening process is most interesting. One could also notice, that fast opening stage occurs when internal voltage drops from excess voltage to the static opening voltage ($310\,\mathrm{V}$). The faster the ramp, the more excess voltage will accumulate before the opening process begins. The opening stages and voltages are presented schematically in Figure 18. At extreme voltage ramps $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} \geq 4800\,\mathrm{Vns}$, the section before opening contains electric current spikes – those are explained by strong displacement currents due to extremely fast voltage changes; additionally, internal voltage rise is delayed due to these currents, and plateaus at about $510\,\mathrm{V}$ of internal voltage. Otherwise, the opening process seems to follow the same stages.

One of the most important parameters to be visualized from single transistor structure simula-

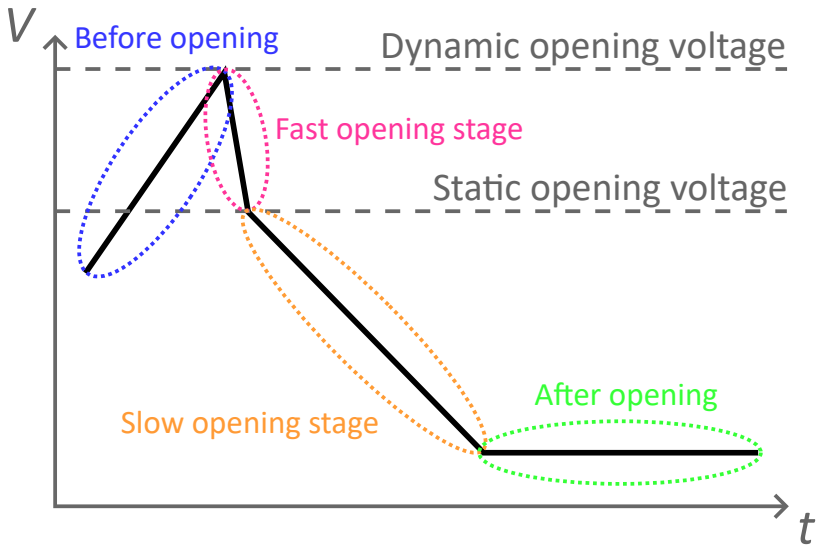

Figure 18. Schematic representation of different stages of the opening process.

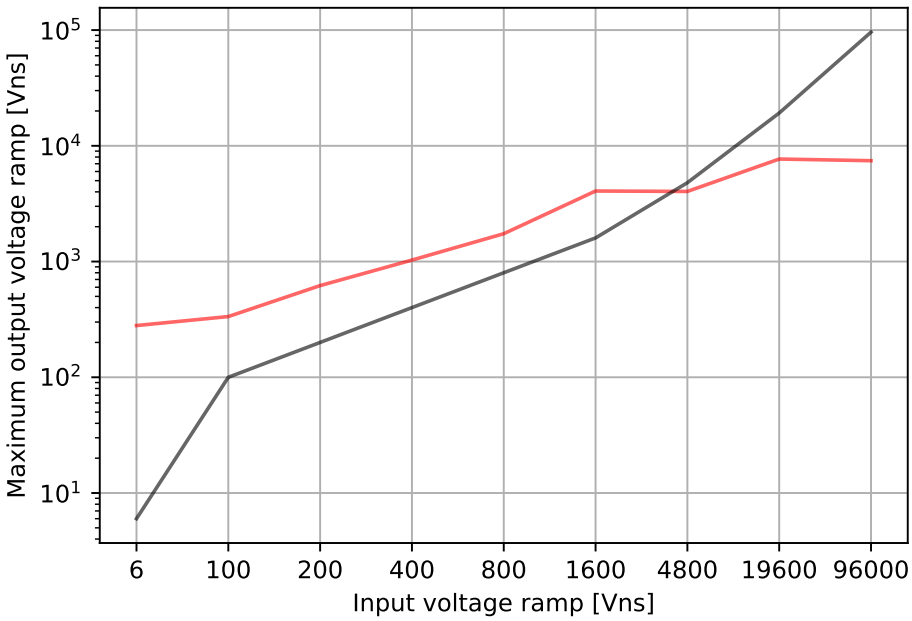

Figure 19. Maximum output voltage ramps against input voltage ramps, black line represents input voltage ramps for comparison purposes.

tions is output voltage ramp. In *Marx* bank circuit, this output voltage ramp is almost directly passed to the next transistor. Thus, if output voltage ramp is higher than the input voltage ramp, pulse speed is expected to increase. In Figure 19, output voltage ramps are plotted in red, input voltage ramps are plotted in black for reference. It can be seen that output voltage ramp is consistently higher than the input one (about 50 times in static case, and about double in the following cases) up until $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$, where it falls below the input ramp. Additionally, at extreme input ramps, output ramp does not rise above about $7500\,\mathrm{Vns}$, which could be hypothesized to be the physical limit for the output voltage ramp. In *Marx* bank circuit, however, output voltage ramp is not expected to even rise above about $4500\,\mathrm{Vns}$ due to lack of speed increase at this point.

Another important parameter is pulse rise time[7], it is easiest to measure from Figure 17. In case of $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 6\,\mathrm{Vns}$ it is hard to separate fast and slow parts; pulse rise time is measured to be about $1\,\mathrm{ns}$. In case of $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 100\,\mathrm{Vns}$ no significant change is seen, pulse rise time is still about $1\,\mathrm{ns}$. At $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 200\,\mathrm{Vns}$ fast stage becomes more visible, however it is still hard to argue that the pulse rise time should be measured on it exclusively, pulse rise time has somewhat decreased to about $0.9\,\mathrm{ns}$. At $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 400\,\mathrm{Vns}$ total pulse rise time has fallen to about $0.8\,\mathrm{ns}$; this seems to be the physical limit for the standard opening mechanism. Input voltage ramp $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 800\,\mathrm{Vns}$ is the first case where fast and slow parts are different enough to assume that slow part is no longer important[8], so it is reasonable to measure pulse rise time on the fast part: it is about $200\,\mathrm{ps}$. For $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 1600\,\mathrm{Vns}$ even lower rise time is reached: about $150\,\mathrm{ps}$. At $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ (which is likely to be around the fastest input voltage ramp that can be achieved by *Marx* bank circuit) pulse rise time is about $100\,\mathrm{ps}$. Extreme input voltage ramps $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 19\,200\,\mathrm{Vns}$ and $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 96\,000\,\mathrm{Vns}$ are already on the physical limit and look similar, here pulse rise time has reached values below $50\,\mathrm{ps}$.

Electric current distributions at the moment of opening are presented in Figure 20. It can be seen that at slower ramps current path in the central part of the transistor is stronger, in case of faster ramps side path through the corner becomes more dominant. To understand the dynamics of the current distribution, it is worth looking at multiple animation frames in a row. Simulation with input voltage ramp $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ has been chosen for this purpose as it shows all interesting effects and can be considered a limit for *Marx* bank circuit.

Selected frames form $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ simulation are presented in Figure 21. First row is a good visualization of the avalanche forming: electrons gather near the corner until electric

[7] In electronics, it is usually defined as time difference between $10\,\%$ and $90\,\%$ of total pulse magnitude on the left side; since we are mostly interested in the order of magnitude, more precise measuring methods are not required.

[8] In practice, slow part will either be slow enough so that capacitors are discharged and pulse stops after the fast part exclusively, next transistor is triggered by the fast part exclusively, or the slow tail part will be cut off using additional pulse shape manipulation techniques.

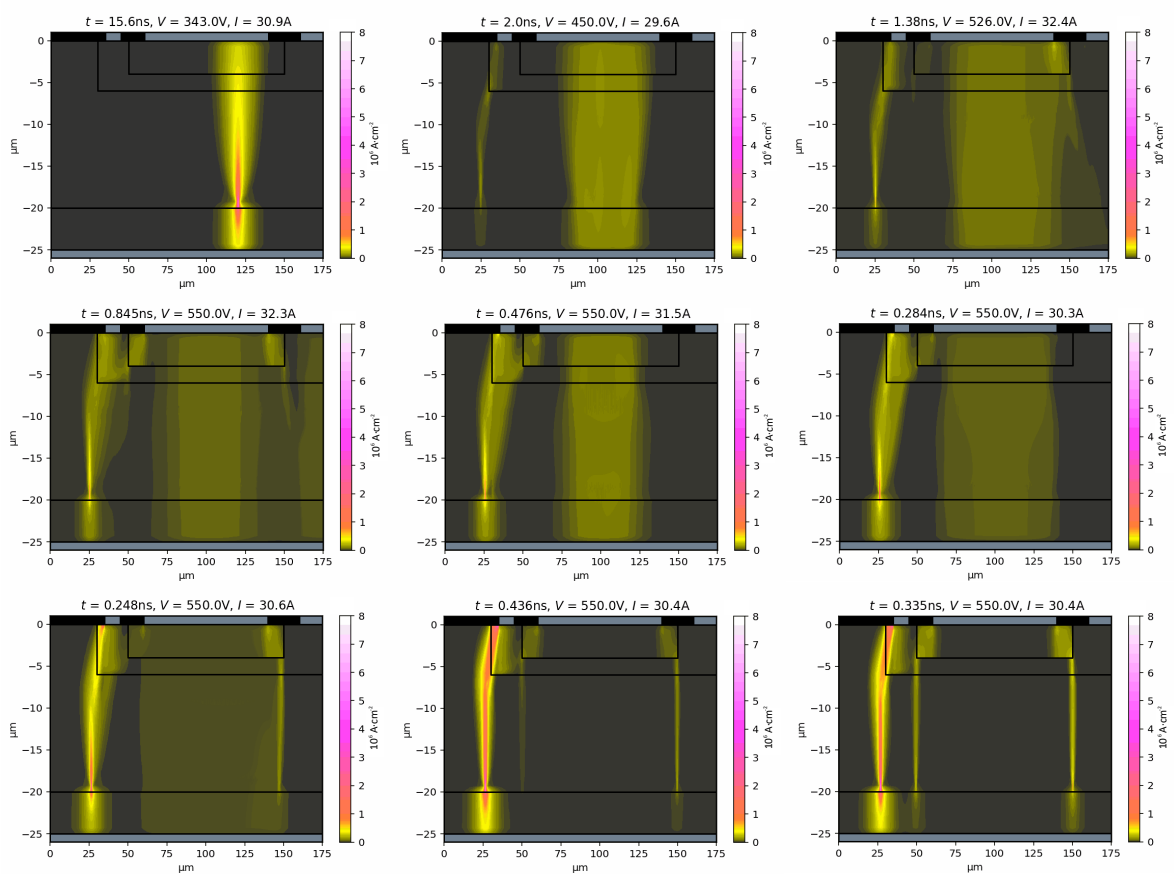

Figure 20. Electric current density distributions in nine different simulation cases at the moment of transistor opening (order: left to right, top to bottom, from $6\,\mathrm{Vns}$ to $96\,000\,\mathrm{Vns}$).

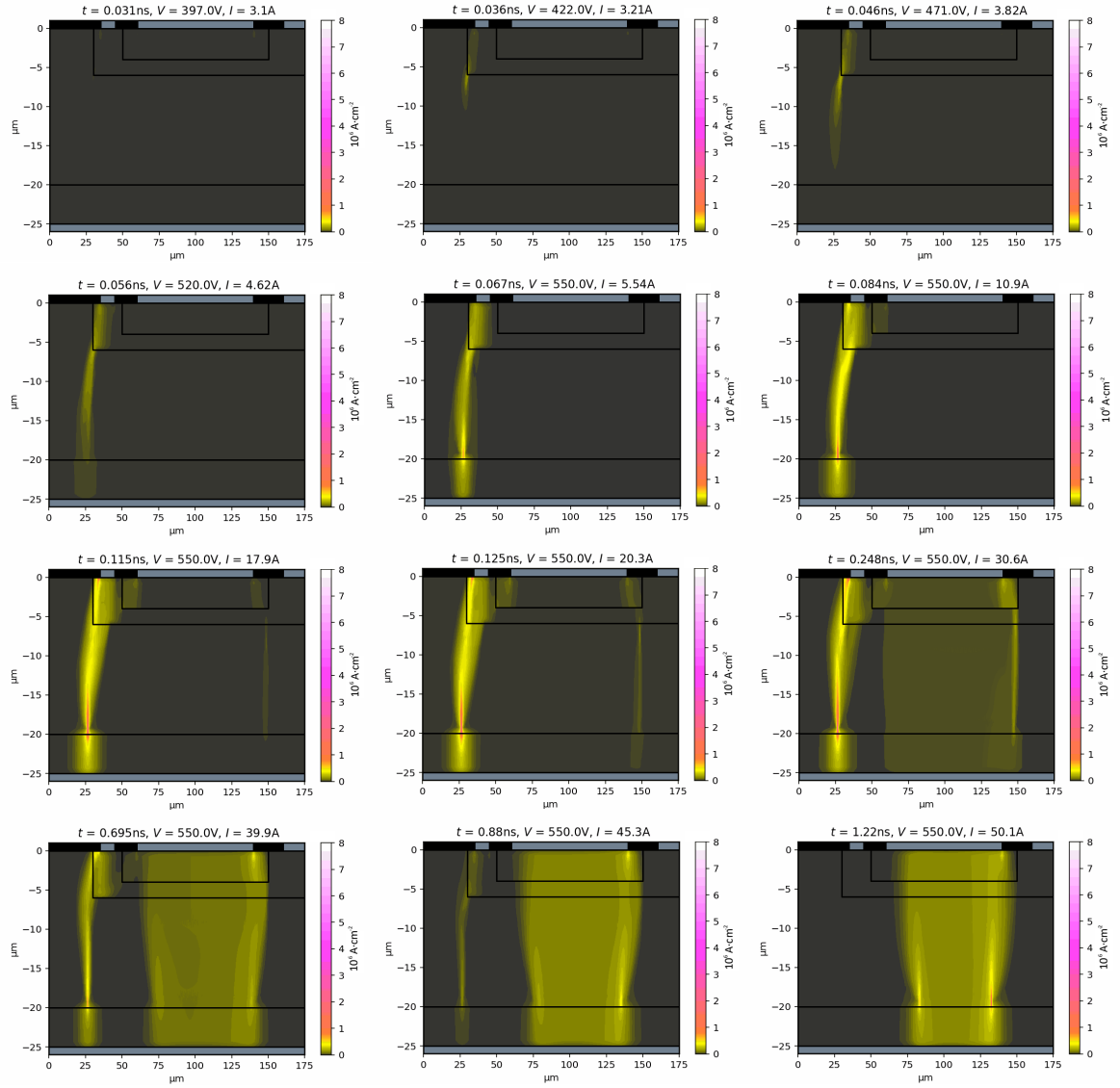

Figure 21. Electric current density distributions in multiple frames of $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ simulation (order: left to right, top to bottom).

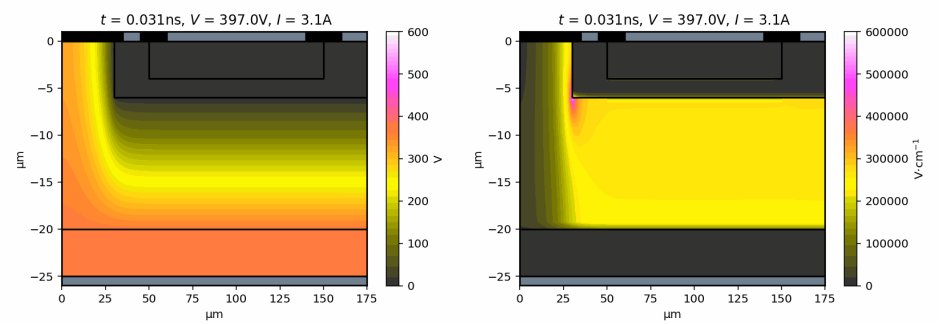

Figure 22. Electric potential (left) and electric field strength (right) right before opening moment of the $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ simulation.

field strength reaches some critical value, then the discharge through the semiconductor structure begins whereby electrons move at saturation velocity until this wave reaches the other side of the low doping concentration collector zone. In the second row the corner avalanche reaches its maximum strength, additionally the second avalanche seem to form on the other side of the structure (in Figure 20, in the last picture three avalanches can be seen in three different geometrically favorable spots). These avalanches are responsible for the fast opening stage, as current reaches $20\,\mathrm{A}$. Then, the slow opening stage begins as a current channel opens in the center of the structure according to the standard opening mechanism. As more current flows through this central channel, voltage drops and avalanche processes deactivate. The central channel has been observed to become thinner with time, therefore very thin central channel seen in first picture of Figure 20 can be considered a fully evolved standard opening mechanism channel; at higher voltage ramps it is much wider initially. It is also worth noting, that multiple avalanche processes starting suggests the dynamic avalanche opening mechanism during the fast opening stage. It seems that in so far completed simulations the static avalanche opening mechanism has not been observed.

It is also worth investigating electric potential and electric field strength in the semiconductor structure. Again, frames from simulation with $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ are taken as it seems to showcase most of the important effects, they are presented in Figure 22. Right before the avalanche opening process begins the electric field is the strongest in the corner. Right below the emitter zone electric field is weaker, which pushes additional avalanches to form below the emitter zone corners. As the transistor opens (not shown here), electric potential and electric field distributions become less orderly, drop in potential can be seen in areas where electric current channels form.

Another important quantity is charge carrier concentration, specifically electron density. By looking at electron density one can clearly see the difference between opening mechanisms. A number of consecutive frames of the $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ simulation are presented in Figure 23. Here, initially electron density is low in base zone and low doping concentration collector

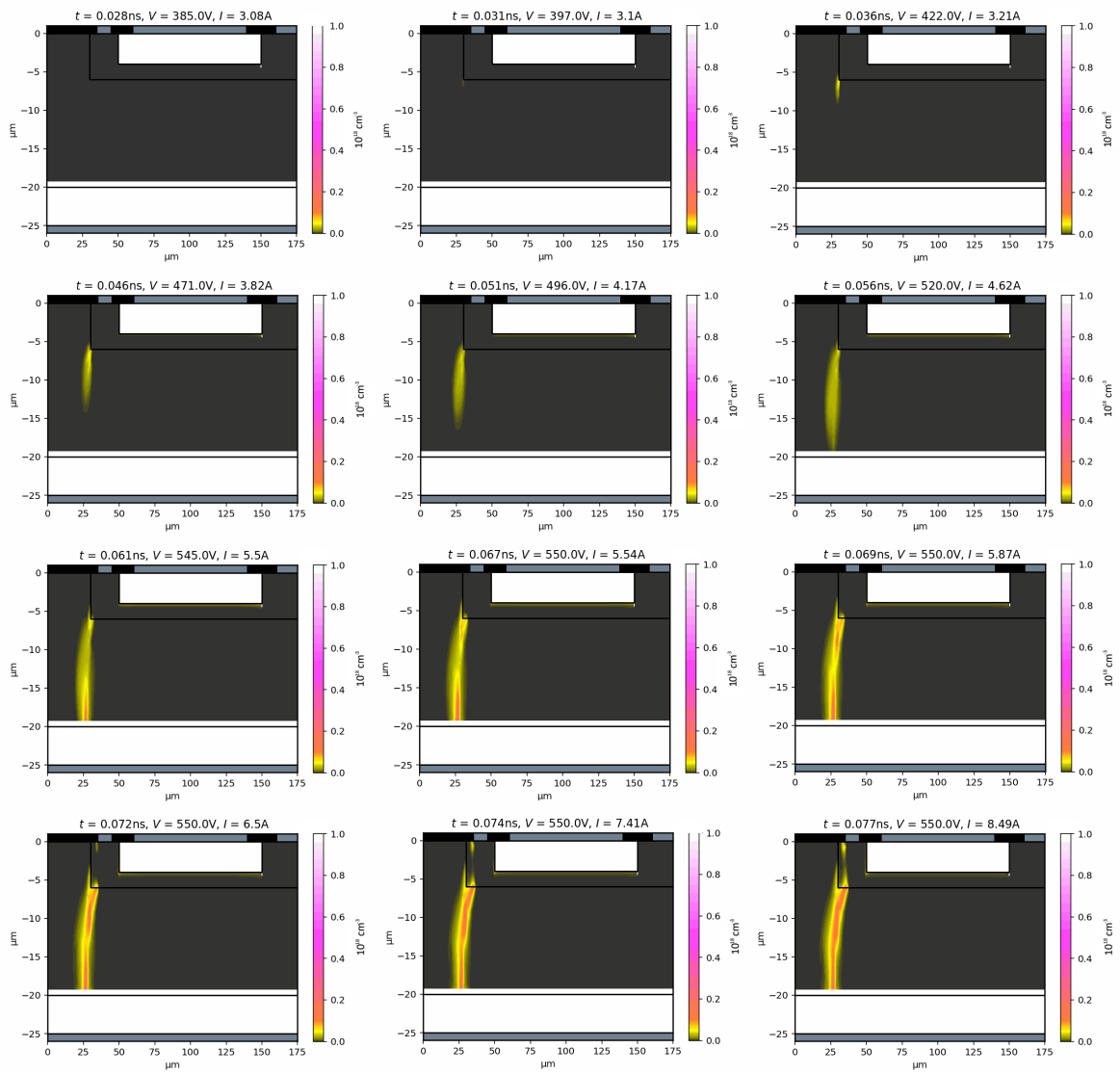

Figure 23. Electron volumetric concentration for $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ simulation (order: left to right, top to bottom), avalanche opening mechanism.

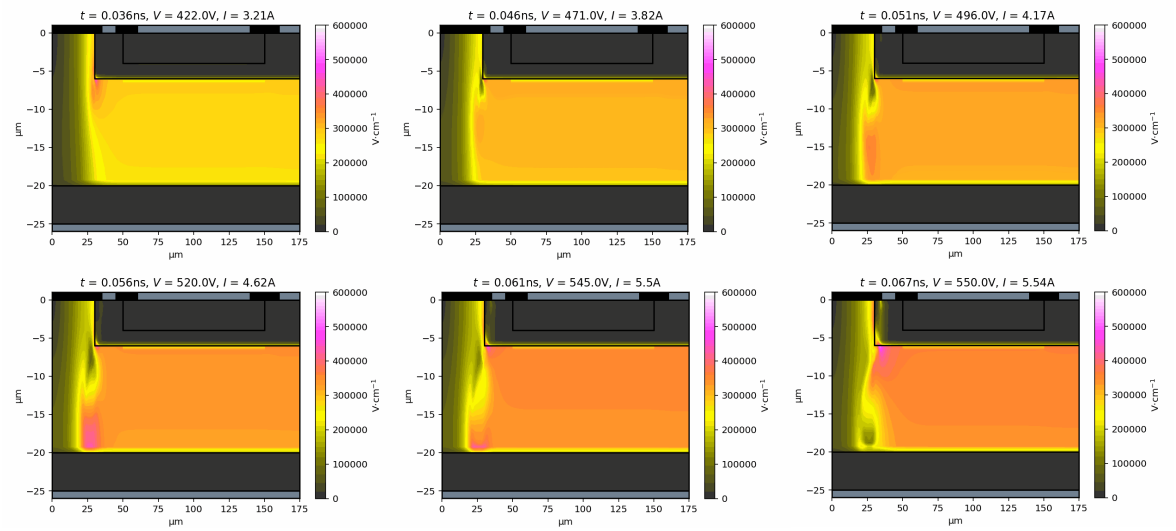

Figure 24. Electric field strength for $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ simulation (order: left to right, top to bottom), avalanche opening mechanism.

zone. In emitter zone and high doping concentration collector zone electron densities are around doping concentration levels. Additionally, some electrons diffuse into low doping concentration collector zone from high doping concentration collector zone. Once electric field strength reaches critical value, the avalanche starts in the corner and moves towards the collector electrode. Sudden increase in electron density in the avalanche increases electric field strength (see Figure 24, bottom row). Thus, the avalanche can propagate through the transistor structure even faster than the saturation velocity (maximum velocity of individual charge carriers). The electric field strength drop in Figure 24, (top row) moves at about the electron saturation velocity ($v_{sat,n} = 1.035 \times 10^7\,\mathrm{cm \cdot s^{-1}}$).

Standard opening process involves injection of electrons from emitter to base and later diffusion from base to collector. This process can be seen in Figure 25; the injection and diffusion takes a lot of time in comparison to the avalanche process. Once the electrons have reached the other side of the base zone, strong electric field in the low doping concentration collector zone facilitates quick transfer of charge carriers. Once the central channel is open, voltage on the semiconductor structure drops and avalanche process becomes unsustainable. Thus, in the end all current flows through the central channel.

Some preliminary conclusions can be made based on the transistor structure simulations analyzed in this section:

- At pseudo-static voltage ramp transistor opens at static opening voltage of about $310\,\mathrm{V}$, since static opening voltage is this high, $300\,\mathrm{V}$ static voltage can be used in further circuit simulations;
- At higher voltage ramps transistor opens at higher voltage – dynamic opening voltage;

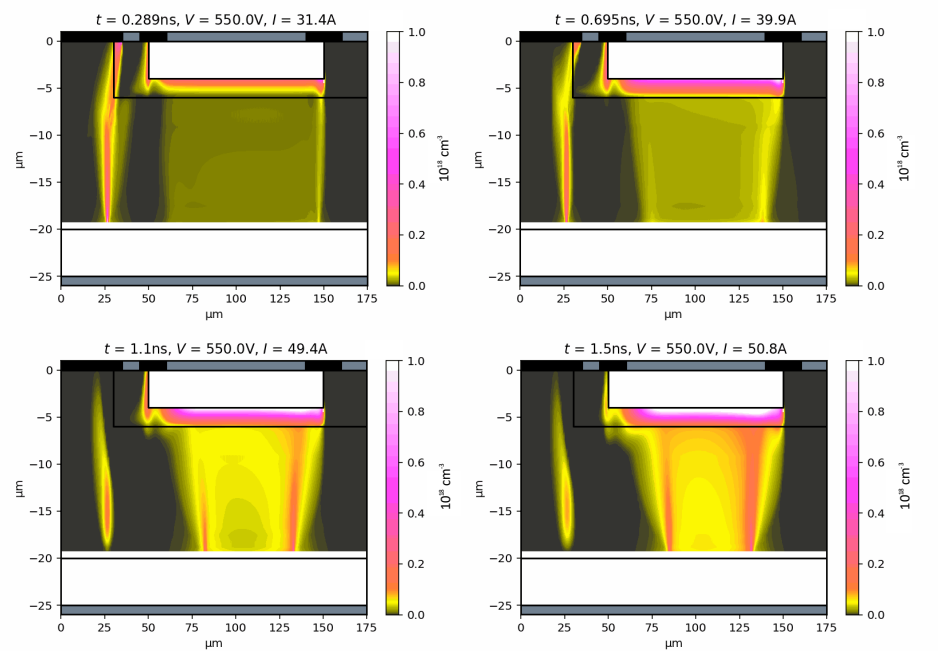

Figure 25. Electron volumetric concentration for $\left(\frac{\mathrm{d}V}{\mathrm{d}t}\right)_{\mathrm{in}} = 4800\,\mathrm{Vns}$ simulation (order: left to right, top to bottom), standard opening mechanism.

- In all cases about $34\,\mathrm{V}$ stays on the semiconductor structure in open state – residual voltage;
- Transistor opening process consists of two stages: fast (voltage drop from dynamic opening voltage to static opening voltage) and slow (voltage drop from static opening voltage to residual voltage);
- Physical limit for transistor output voltage ramp is about $7500\,\mathrm{Vns}$ (assuming even faster input voltage ramp), physical limit for output pulse voltage ramp in the context of *Marx* bank circuit is about $4500\,\mathrm{Vns}$;
- Pulse rise time, in case if slower part is neglected, can realistically reach values around $100\,\mathrm{ps}$.
- Fast opening stage is directly tied to avalanche opening mechanism, the electric current channels appear in the weakest spots (usually due to geometry), opening time physical limit in case of this mechanism is around $100\,\mathrm{ps}$;
- Slow opening stage is directly tied to standard opening mechanism, electric current channel form in the center and is wider when input voltage ramps are higher, it becomes thinner with time, opening time physical limit in case of this mechanism is around $1\,\mathrm{ns}$;
- Avalanche opening process has been observed, its velocity seems to be realistic (around saturation velocity);
- Standard opening process with electron injection from the emitter has been observed.

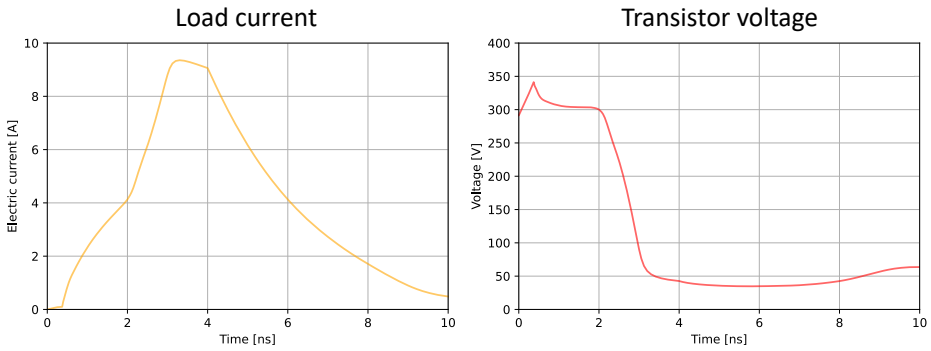

Figure 26. Current through the load resistor (left) and voltage on the transistor (right) in one transistor circuit; time $t = 0$ corresponds to the beginning of the voltage drop on the generator.

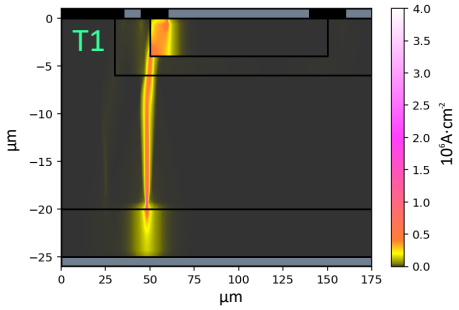

Figure 27. Current density in transistor at time $t = 2\,\mathrm{ns}$.

3.3 Circuit Simulation

Finally, full circuit simulations according to Figure 8 are done. Here, all transistors are simulated fully using previously defined and optimized structure, all other elements are simulated using simplified models.

Two most important parameters from the one transistor circuit simulation are presented in Figure 26: electric current through the load resistor, and voltage applied to the transistor structure. It can be seen that the opening stage consists of two stages with similar voltage ramps. First stage corresponds to transistor voltage staying at about the static opening voltage, while total voltage on the system increases, thus increasing current on the load. Second stage corresponds to the voltage drop on the transistor to its residual voltage, this stage is significantly delayed in comparison to transistor simulations. Current through the load resistor reaches $9\,\mathrm{A}$, which corresponds to voltage of $450\,\mathrm{V}$ – a significant increase from $300\,\mathrm{V}$ using only one transistor. Current pulse rise time is about $2.5\,\mathrm{ns}$, which is considered slow. One transistor *Marx* bank circuit output voltage ramp is, therefore, about $180\,\mathrm{Vns}$ – a marginal increase from the input voltage ramps of $150\,\mathrm{Vns}$.

A plot of electric current density in one transistor circuit simulation is presented in Figure 27.

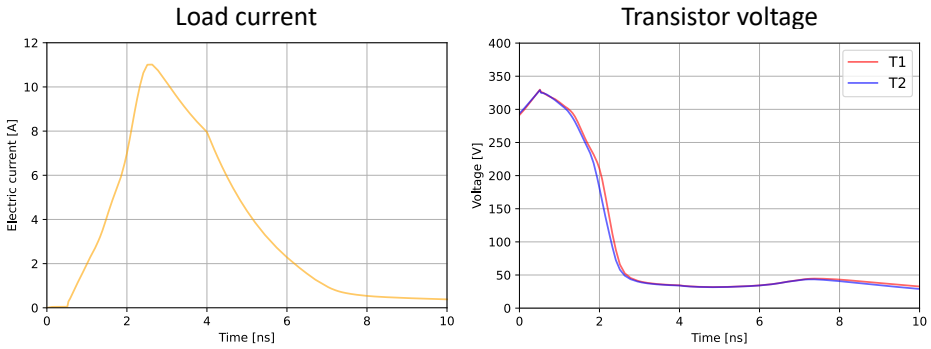

Figure 28. Current through the load resistor (left) and voltage on the transistors (right) in two transistor circuit (order: transistor **T1** is the closest to the generator); time $t = 0$ corresponds to the beginning of the voltage drop on the generator.

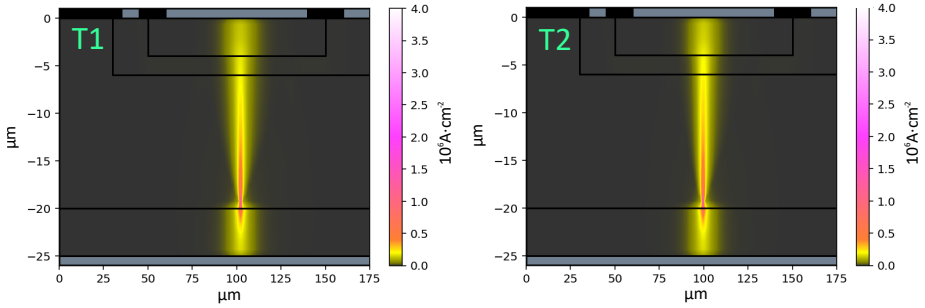

Figure 29. Current densities in transistors at time $t = 2\,\mathrm{ns}$ in two transistor circuit (order: transistor **T1** is the closest to the generator).

At time $t = 2\,\mathrm{ns}$ transistor is about to enter second opening stage, it can be seen that current flow shifts towards the center of the structure. However, the avalanche process in the corner still dominates. In fact, at a slightly earlier moment current was flowing through the corner exclusively, and at a slightly later moment the current channel moves further right and flow through the corner disappears. Thus, this plot confirms that two separate mechanism were active during the opening process. Additionally, due to relatively low input voltage ramp this may be the first time a static avalanche process has been observed; a further study is needed to either confirm or deny this hypothesis[9].

Results of the two transistor circuit simulation are presented in Figure 28. It can be seen that opening stages are much harder to separate now, as the voltage drop on the transistors seems to follow a smooth curve. Electric current through the load resistor has reached its maximum earlier, as well as the pulse magnitude is larger: rise time is about $2\,\mathrm{ns}$, maximum current is about $11\,\mathrm{A}$, which corresponds to $550\,\mathrm{V}$, thus the output voltage ramps is about $275\,\mathrm{V ns}$ – a noticeable increase.

Plots of electric current density in two transistor circuit simulation at time $t = 2\,\mathrm{ns}$ are

[9] A simulation with full symmetric structure may be sufficient, however circuit simulations are already computationally intensive and doubling the structure size makes it unfeasible for the purposes of this thesis.

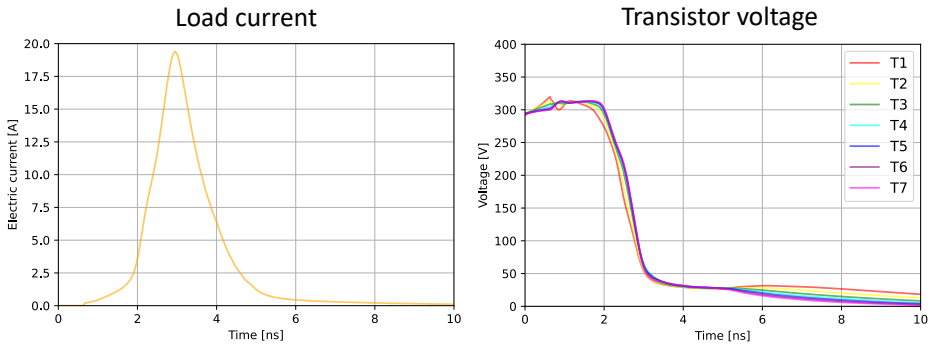

Figure 30. Current through the load resistor (left) and voltage on the transistors (right) in seven transistor circuit (order: transistor **T1** is the closest to the generator); time $t = 0$ corresponds to the beginning of the voltage drop on the generator.

presented in Figure 27. It can be seen that the process progresses faster: at the same moment as in one transistor circuit simulation most of the current flows through the central channel. This suggests, that standard opening mechanism activated earlier in this simulation. Additionally, it can be seen from Figure 28 that standard opening process seems to be slightly more developed in the second transistor. This may be the effect of current flowing through the corner in the first transistor in the chain, thus damaging it – it is well described in existing research. [9]

Results of the seven transistor *Marx* bank circuit simulation are presented in Figure 30. Again, two opening stages are visible: voltage drop to the static opening voltage level, and further voltage drop to the residual voltage level; avalanche opening mechanism is responsible for the former, standard opening process is responsible for the latter. An initial jump in voltage can be seen on the first transistor in the chain, it is not transferred to the following transistors. Maximum current of about $19\,\mathrm{A}$ is reached (from the beginning of the fast phase) in about $1\,\mathrm{ns}$, which is around the limit for standard opening mechanism; output voltage ramp (with maximum voltage being $950\,\mathrm{V}$) is around $950\,\mathrm{Vns}$. Also it can be seen from voltage graphs that transistors later in the chain seem to open slightly later.

Plots of electric current density distributions at time $t = 2\,\mathrm{ns}$ of the seven transistor circuit simulation are presented in Figure 31. It can be seen that, again, current flow transitions from the corner channel to the central channel during the second part of the opening stage. Additionally, the first transistor in the chain has stronger currents in the central part and weaker currents in the corner part, which suggests that, indeed, transistors further along the chain open with a barely noticeable delay. The effect of central path being more developed seems to go against the conclusions of the existing research. It can be theorized, that there are two competing effects: stronger central channel current due to increased voltage ramp, and delay in each next transistor opening process (the second effect can be accounted for by slightly adjusting the horizontal axis). [9]

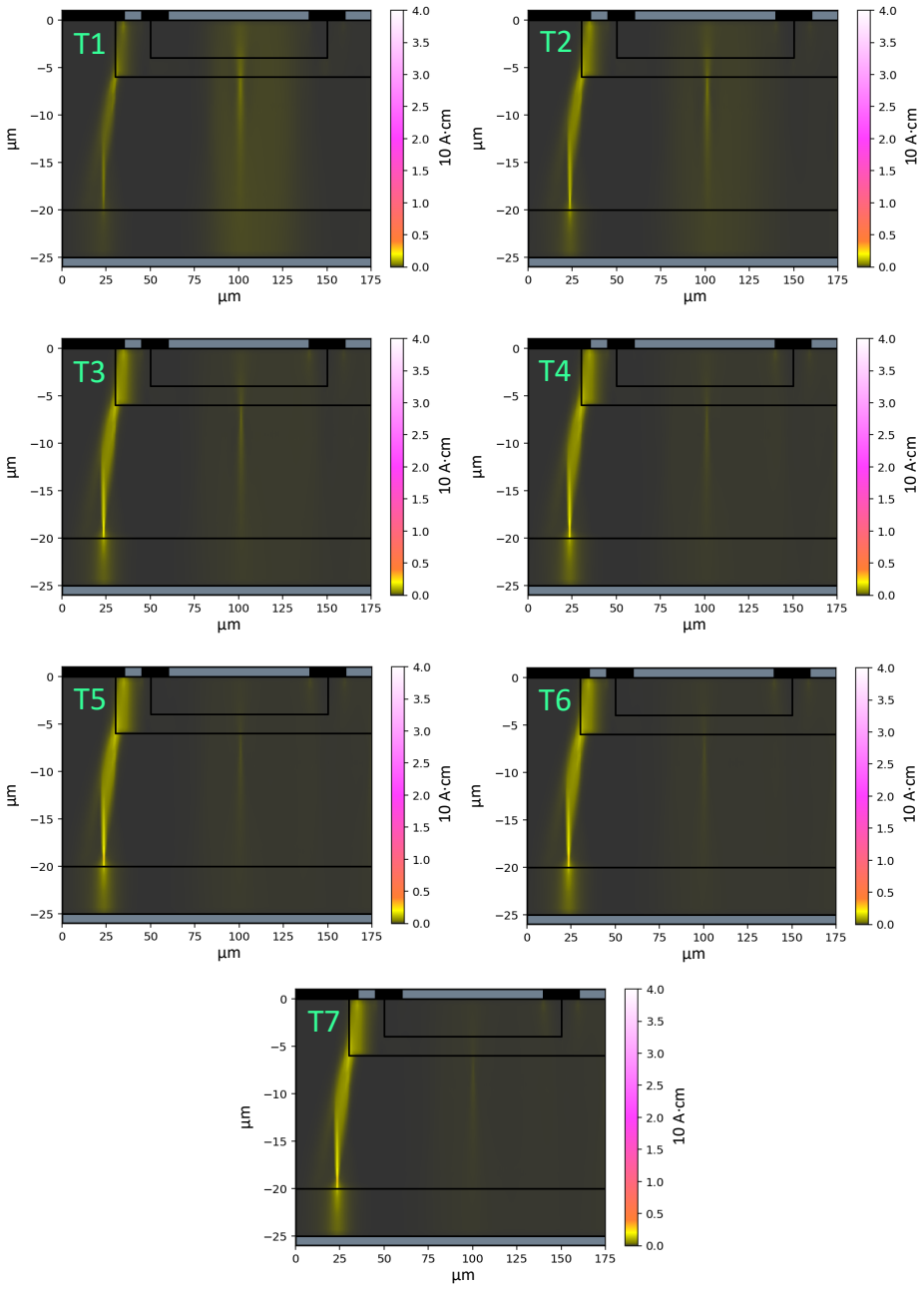

Figure 31. Current densities in transistors at time $t = 2\,\mathrm{ns}$ in seven transistor circuit (order: transistor **T1** is the closest to the generator)

From all three circuit simulations it can be seen, that an increased number of *Marx* bank circuit stages results in faster and stronger pulses. This effect can clearly be seen by comparing Figures 26, 28, 30.

4. Conclusions

In this chapter, all conclusions of the conducted study are presented and discussed, and further research directions are suggested.

4.1 Transistor Conclusions

It has been hypothesized that there are three mechanism that can be responsible for the opening of the avalanche transistor: standard (electron injection into the base and later diffusion toward the collector), static avalanche (sudden increase of charge carrier concentration in one spot due to runaway impact ionization), and dynamic avalanche (sudden increase of charge carrier concentration due to runaway impact ionization that occurs in many spots at once); distinction between the avalanche mechanisms is qualitative, as static avalanche is very likely to damage the transistor due to creation of a hot spot, while dynamic avalanche results in electric current being more evenly distributed over the whole transistor area. Standard opening mechanism behavior has been clearly observed as it is responsible for the opening of the central current channel; it is the slowest of the three proposed mechanism, with opening time physical limit around $1\,\mathrm{ns}$. Avalanche mechanisms were observed, but it is hard to separate static avalanche mechanism from the dynamic one; symmetry tests and ridiculously high input voltage ramp tests suggests that dynamic avalanche mechanism exists as described.

Avalanche mechanisms have been observed to be responsible for the voltage drop to the static opening voltage (around $310\,\mathrm{V}$), thus it can only occur when input voltage ramp is fast enough to momentarily exceed the static opening voltage. Standard mechanism activates later and allows for voltage drop to the residual voltage level (around $34\,\mathrm{V}$). These values are in agreement with measurements of **FMMT417** avalanche transistor. [37]

One of the most important regions in an avalanche transistor is the base zone. Multiple base zone parameters were tested: thin base (width of $1\,\mu\mathrm{m}$), wide base (width of $2\,\mu\mathrm{m}$); doping concentration of $1 \times 10^{17}\,\mathrm{cm}^{-3}$ and $1 \times 10^{18}\,\mathrm{cm}^{-3}$. Base parameters affect static opening voltage, which decreases in case of base with lower lateral resistance (so wider base or base with higher doping concentration). More importantly, base parameters influence opening mechanisms: base with higher lateral resistance is more likely to open with standard opening mechanism; thus, it can be theorized, that lower lateral resistance is beneficial for avalanche opening mechanism. However, increased base doping may be directing avalanches to start in the structure corner, which may damage the structure. Therefore, a structure with wide lower doping concentration base was chosen as the most optimal for further simulations.

One of the tested structures was a slightly asymmetric structure. The tests have revealed that

at lower input voltage ramps electric current channels open only in the most favorable spot; at higher voltage ramps the electric current channels are more evenly distributed over the whole structure area. These results suggests that there is, indeed, some qualitative difference between static avalanche and dynamic avalanche opening mechanisms: over some critical input voltage ramp avalanches are more evenly distributed and no single hot spot is observed, thus damage to the transistor is less likely.

In existing research, a distinction between standard opening mechanism and avalanche opening mechanism is made. This paradigm implies a tradeoff between transistor lifespan and reliability, and maximum pulse speed. Simulations done for this thesis support this distinction; additionally, separation of avalanche mechanism into static and dynamic is proposed. Notably, dynamic avalanche mechanism has lower maximum current densities than static avalanche mechanism, thus it is more reliable. Therefore, an avalanche semiconductor device design that relies on the dynamic avalanche mechanism may have acceptable reliability without sacrificing the maximum pulse speed. [9]

Transistor structure simulations have shown, that physical limit for output voltage ramp with the defined structure is around $7500\,\mathrm{Vns}$. However, this level cannot be achieved using *Marx* bank circuit, as the output voltage ramp becomes comparable to the input voltage ramp at around $4500\,\mathrm{Vns}$. This value is, therefore, the maximum voltage ramp achievable by a *Marx* bank circuit with modeled semiconductor structure used as switches.

It should be noted, that simulations done for this thesis use geometrically simplified structure, that may not reflect real device behavior on the level required to conclusively declare full understanding of the internal processes. Therefore, the simulated structure has to be redesigned with real semiconductor device manufacturing processes in mind[1]. Additionally, it is worth investigating internal processes using either a three-dimensional model, or introducing a replacement of the third dimension by using a fully symmetric two-dimensional structure. For the purposes of this thesis, influence of magnetic field on the semiconductor structure was assumed to be negligible; due to large current densities within the structure, this assumption may be wrong, and an introduction of magnetic field effects into the simulation may be necessary.

4.2 Circuit Conclusions

Circuit simulations made for this thesis include one transistor, two transistor, and seven transistor *Marx* bank circuit simulations; where each transistor structure is fully simulated using semiconductor physics equations. Introduction of multiple transistor simulation and

[1]While *Silvaco TCAD* can simulate the device manufacturing process, thus may theoretically produce geometrically perfect semiconductor model, the manufacturing methods are often considered a trade secret and are not publicly available.

simplified circuit element models has revealed additional effects not seen in the transistor simulations.

Firstly, in transistor simulations static avalanche opening mechanism has not been definitively observed; in circuit simulation it is likely to be present in the initial stages of the first transistor opening process. Secondly, initial avalanche opening voltage drop seems to be immediately transferred to the next transistors, causing it to partially open in avalanche mode, which prevents further voltage buildup and fast opening stage activation. Additionally, the slow opening stage (standard opening mechanism) is significantly delayed. Therefore, now fast opening stage is not present at all, and slow opening stage is preceded by even slower leakage stage; pulse rise time cannot go below $1\,\mathrm{ns}$ due to standard opening mechanism being the dominating one – significantly slower than realistically achievable opening speeds of about $100\,\mathrm{ps}$ with a similar circuit configuration.

Main reason for slower than expected processes seems to be the lack of avalanche activating properly on transistors after the first one. The avalanche process keeps voltage at about $310\,\mathrm{V}$ – the static opening voltage – until standard opening mechanism activates; standard opening mechanism on the first transistor seems to fail to activate avalanches on the following transistors. Additionally, barely any delay between transistors is observed, which prevents voltage from building up on every next stage.

Possible solutions to these problems can be categorized into transistor level, and circuit level.

Transistor level solutions include change of base parameters so that standard opening mechanism is not delayed that much, allowing for initial fast opening stage to directly transition into the slow one, thus successfully increasing voltage on the next transistor in the chain. Another approach could be to attempt to eliminate standard opening mechanism, forcing all processes to involve exclusively avalanche mechanisms; this however, will dramatically increase residual voltage and reduce output pulse magnitude, unless a total redesign of the transistor is undertaken. Since it is known to be possible to achieve higher speeds with *Marx* bank circuit topology discussed in this thesis, structure optimizations and improvement may resolve the problem of slow opening speed as well. [4, 5, 6]

Circuit level solutions include change of circuit element parameters, or introduction of additional circuit elements. Since the transistor simulations yielded high output voltage ramps, and circuit simulations did not with the same transistors, it may be possible to recreate the conditions required for the fast opening stage to dominate. However, changes of the circuit topology should not be necessary, as high speeds are known to be achievable with the presented circuit. [4, 5, 6]

Otherwise, the transistor behavior agrees with existing research: two electric current channel

are clearly visible, one of which is tied to the destructive avalanche mechanism, the other – to the standard (injection) mechanism. On the first transistor, avalanche channel is stronger, which causes it to be the first transistor to fail due to increased current density. Additionally, an decrease of pulse rise time is observed when increasing the number of *Marx* bank circuit stages. [9, 4, 5, 6]

Based on the results of all simulations, some suggestions can be made. It can be confidently stated, that static avalanche process is to be avoided as it is known to be responsible for low transistor reliability. Standard opening process is reliable, but slow, thus it cannot be used in the later stages on the *Marx* bank circuit. Dynamic avalanche process requires a fast input voltage ramp to activate safely, so it cannot be used in the earlier stages of the *Marx* bank circuit. Therefore, it should be possible to combine two types of transistors in one circuit: the first group increases voltage ramp from the initial (slow) one to some critical value by opening using the standard opening mechanism; the second group takes the output of the first group and transforms already reasonably fast pulse into even faster one using the dynamic avalanche mechanism. Transistors in the first group have to be biased towards opening in the standard mode, by increasing base lateral resistance. Transistors in the second group have to be biased towards opening in the avalanche mode, by reducing base lateral resistance and allowing for avalanche activation in many spots at once. Static opening voltage for both groups can be additionally tuned by changing the low doping concentration collector zone width.

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Abstract

Fast electric pulse generation is a process with many applications. Nowadays, ultra-fast pulses are commonly generated using *Marx* bank circuits with avalanche transistors as switches. In this thesis, a model of **FMMT417** *npn* bipolar junction avalanche transistor is defined and tested in a set of conditions using *Silvaco TCAD* modeling software.

Transistors used in *Marx* bank circuits are known to deteriorate at an accelerated rate or fail in some cases, this behavior is tied to local overheating due to high current density. One of the main tasks of the transistor simulations is to determine the reason behind this undesirable behavior, and suggest possible improvements. For this purpose, a mathematical model is constructed based on main equations of semiconductor physics and transistor real geometric structure. Next, the resulting differential equations are solved numerically, using *Silvaco TCAD* software. Multiple simulations were completed. The first group provided some initial insight into the transistor behavior and allowed for some semiconductor structure optimizations. The second group explored transistor behavior in isolation from other elements. The third group explored whole *Marx* bank circuit behavior, with multiple transistors and other simplified circuit elements.

Multiple transistor opening mechanisms were observed. The standard opening mechanism, which is activated by electron injection into the base due to small potential difference caused by lateral currents, and their slow diffusion toward the collector, is responsible for the slow opening stage; it is possible to achieve pulse rise times of about $1\,\mathrm{ns}$ with this mechanism. The static avalanche opening mechanism, which involves a runaway process of impact ionization in the collector zone, is often damaging due to high electric current densities. The dynamic avalanche opening mechanism, which involves many runaway impact ionization waves forming in the structure, is more reliable than the static one due to more even electric current density distribution. Both avalanche mechanism can achieve pulse rise times of about $100\,\mathrm{ps}$. Using this classification of processes in the transistor structure, it is possible to explain its behavior and construct a pulse generation device, that is both fast and reliable.

The model presented in this thesis can be further improved by: implementing a more realistic geometry of the transistor, inclusion of thermodynamic models, and inclusion of magnetic field models. The results of the thesis can be used to adjust avalanche transistor designs to better suit ultra-fast electric pulse generation use cases.

Keywords: avalanche transistor, numerical simulation, *Marx* generator, *Silvaco TCAD*.

Annotatsioon

Ülikiirete elektriimpulsside genereerimine on protsess, millel on palju rakendusi. Tänapäeval genereeritakse ülikiireid impulsse tavaliselt *Marxi* generaatori astmeliste ahelate abil, mille lülititena kasutatakse laviintransistore. Käesolevas lõputöös defineeritakse **FMMT417** *npn* bipolaarse laviintransistori mudelit ning testitakse seda mudelit erinevates tingimustes, kasutades *Silvaco TCAD* modelleerimistarkvara.

Marxi generaatori ahelates kasutatavad transistorid on teadaolevalt mõnel juhul kiirenenud tempos kahjustunud või riknenud, seda seostatakse lokaalse ülekuumenemistega suure voolutiheduse tõttu. Transistori simulatsioonide üks peamisi eesmärke on selle soovimatu käitumise põhjuse kindlakstegemine ja võimalike parenduste pakkumine. Selleks konstrueeritakse pooljuhtfüüsika põhivõrranditel põhinev matemaatiline mudel, arvestades transistorstruktuuri reaalset geomeetriat. Seejärel lahendatakse saadud diferentsiaalvõrrandid numbriliselt, kasutades *Silvaco TCAD* võimalusi. Teostati mitmeid simulatsioone. Esimene rühm andis esialgse ülevaate transistori käitumisest ning võimaldas teha mõningaid pooljuhtstruktuuri optimeerimisi. Teine rühm uuris transistori käitumist teistest elementidest eraldatuna. Kolmas rühm uuris terve *Marx* generaatori ahela käitumist, hõlmates mitut transistorit ja teisi lihtsustatud vooluahela elemente.

Täheldati mitut transistori avanemismehhanismi. Standardne avanemismehhanism, mis aktiveerub elektronide süstimisel baasi väikese lateraalsete voolude põhjustatud potentsiaalierinevuse tõttu ning nende aeglases difusioonis kollektori suunas, vastutab aeglase avanemisetapi eest; selle mehhanismi korral on võimalik saavutada impulsi tõusuaeg ligikaudu $1\,\mathrm{ns}$. Staatiline laviiniavanemismehhanism, mis hõlmab kollektori piirkonnas toimuvat löögiionisatsiooni ahelreaktsiooni, on sageli kahjulik suure voolutiheduse tõttu. Dünaamiline laviiniavanemismehhanism, mille korral tekib struktuuris mitmeid löögiionisatsioonilaineid, on ühtlasema voolutiheduse jaotuse tõttu töökindlam kui staatiline mehhanism. Mõlemad laviinmehhanismid võimaldavad saavutada impulsi tõusuaegu suurusjärgus $100\,\mathrm{ps}$. Selline transistori sees toimuvate protsesside klassifikatsioon võimaldab selgitada nende käitumist ning kavandada impulssgeneraatorit, mis on ühtaegu kiire ja töökindel.

Lõputöös esitatud mudelit saab edasi täiustada, rakendades realistlikumat transistori geomeetriat ning kaasates termodünaamilised ja magnetvälja mudelid. Töö tulemusi saab kasutada laviintransistoride konstruktsioonide kohandamiseks, et need sobiksid paremini ülikiirete elektriimpulsside genereerimiseks.

Märksõnad: laviintransistor, numbriline simulatsioon, *Marxi* generaator, *Silvaco TCAD*.

Appendices

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Appendix 2 – Simulation Animated Results

Animations, produced from results of the simulations done for this thesis are submitted alongside with the thesis text and additional documents as *appendix.zip* archive, or available online at: *https://github.com/MikeKerman/transitor_modeling_animated_results*. Note that in some animations the first frame may not be representative of the real values due to the specifics of data structure extraction methods for these animations.