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Investigation of the Intermediate Layer in the Metal-Silicon Carbide Contact Obtained by Diffusion Welding

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Declaration:

Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for any degree or examination.

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INFORMAATIKA JA SÜSTEEMITEHNIKA C61

Difusioonkeevitusega valmistatud metalli ja ränikarbiidi vahelise üleminekuala vahekihi uurimine

NATALJA SLEPŠTUK

TTÜ
KIRJASTUS

Abstract

Metal-semiconductor contacts are an obvious component of semiconductor device. The current-voltage characteristics of actual metal-semiconductor Schottky-barrier contacts are known to differ from the ideal ones. Considerable scientific interest has been devoted to this situation since the last century. One of the most probable reasons of this deviation is the presence of an intermediate layer between the metal and semiconductor. The presence of interface layer may lead to such effects as the potential drop at the interface layer and barrier lowering, reduction of space charge region, the tunnelling of the electrons through the barrier, and all this, in turn, may be the reason of strong discrepancy in real electrical characteristics of metal-semiconductor contacts.
The theme of this thesis is devoted to investigation of the intermediate layer in the metal-semiconductor contact obtained by diffusion welding (DW).
In Chapter 1, are given a previous history of the issue to justify the research subject and problem statement.
In Chapter 2, from the current-voltage and capacitance-voltage characteristics are analyzed possible reasons for the deviation of electrical parameters of the DW contacts on the parameters of an ideal model.
In Chapter 3 electron microscopy study of subcontact layer in SiC after the diffusion welding has been made. Electron-microscopy studies showed the presence of destructed layer of ~ 25 nm thick of strip character with a structure similar to the amorphous state.
In Chapter 4 are shown the results of the investigation of additional states introduced into the semiconductor surface layer during the diffusion welding by use of deep level transient microscopy (DLTS).
Chapter 5 shows the investigation of the surface of the semiconductor after the DW process by the method of vibrating capacitor. An increase in surface charge density after diffusion welding is shown. In addition, in the last Chapter 6 by AFM and SEM microscopy are shown the variation of surface topography and changes in the elemental composition of the surface after diffusion welding.
Each chapter is taken separately on the conditions of full value investigations. Although the aims of this research have been reached, it is too early to draw the final conclusions as I consider the work being far from completed, but the main target – to show the presence of an intermediate layer on the semiconductor surface– has been reached.

Kokkuvõte

Metall-pooljuht (M-P) kontakte kohtame igas pooljuhtseadises. On tuntud tõsiasi, et reaalsete Schottky dioodide voolu-pinge karakteristikud erinevad ideaalse Schottky siirde omast. Nimetatud eripära on uuritud kaua ja ainsat ning ühest põhjust sellele seni ei ole leitud. Üheks tõenäoliseks põhjuseks on asjaolu, et metalli ja pooljuhi vahele võib kontakti valmistamisel tekkida nn vahekiht. Sellise vahekihi olemasolu põhjustab mitmeid anaomaaliaid tuues kaasa näiteks potentsiaali hüpe ning barjääri kõrguse alanemise, ruumlaengu piirkonna kitsenemise, elektronide tunneleerumise läbi barjääri, jne. Kõik nimetatud nähtused mõjutavad otseselt reaalsete M-P kontaktide elektrilisi karakteristikuid, mis võivadki põhjustada reaalsete ja ideaalse karakteristiku tugevat lahknevust. Siit tuleneb ka põhjendus tegelemaks uurmistööga, mis on seotud difusioonkeevituse (DW) abil valmistatud M-P vahelise üleminekuala vahekihi uurimisele.

Esimeses peatükis käsitletakse Schottky strukturide ajaloolist tausta ning põhjendatakse uurimiteema valikut.

Teises peatükis analüüsitakse voolu-pinge ja mahtuvuse-pinge karakteristikuid eesmärgiga selgitada välja DW abil valmistatud Schottky kontaktide elektriliste karakteristikute suurt erinevust ideaalse Schottky siirde karakteristikuga võrreldes.

Kolmandas peatükis uuritakse DW tehnoloogias valmistatud SiC Schottky siiretel tekkiva vahekihi teket elektronmikroskoobi abil. Uurimine näitas, et vahekihi paksuseks kujuneb orienteeruvalt ~ 25 nm. Vahekihi struktuur on aga lähedane SiC amorfsele olekule.

Neljandas peatükis käsitletakse sügavate lisandivoode uurimist kasutades sügavate nivoode spektroskoopiat (DLTS). Uurimistöö tulemusena selgitatid välja täiendavate lõksude tekkimise peamised põhjused tingituna DW metalliseerimistehnoloogiast.

Viiendas peatükis uuriti SiC pooljuhi pinnaolekuid, mis tekivad peale DW metalliseerimist, kasutades selleks muutuva mahtuvuse (vibreeriv kondensaator) mõõtmisi. Uurimine näitab pinnaolekute tiheduse suurenemist peale difusioon keevitust.

Kuuendas peatükis uuritakse pinna topograafia variatsioone peale DW protsessi kasutades AFM ning SEM mikroskoopiat.

Vaadates iga peatüki teoreetilisi tagamaid, võib julgelt väita, et enamus peatükke võiksid olla iseseisvad süvauuringud, millest mõne maht küüniks eraldi doktori dissertatsiooni mahuni. Vaatamata asjaolule, et mitmed järeldused ei ole lõplikud ja vajavad täiendavaid uuringuid, suutsin käesoleva uuringu alguses püstitatud sihi – näidata ära metalli ja ränikarbiide vahelise vahekihi tekkimise ja tema olemasolu mõju elektrilistele karakteristikutele - täita.

God made the bulk;

the surface was invented by the devil

------Wolfgang Pauli

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List of symbols

A –area
A^* – Richardson's constant
a – lattice space in plane of slip
b – the Burgers vector
C – capacitance
c – distance between two adjacent slip planes
D_S – surface state density
d_{ox} – oxide thickness
e_n – electron emission rate
E – Young's modulus
E_a – activation energy
E_c – bottom of conduction band
E_F – Fermi energy level
E_{Fn} – Fermi level in metal
E_g – bandgap of the semiconductor
E_v – top of valence band
f_d – quantum-mechanical reflection of electrons
f_p – Peierls force
G – shear modulus
h – Planck's constant
J – the current density
k – Boltzmann constant
L_D –intrinsic debye length
m_0 – electron rest mass
m^* – electron effective mass
Nc – the effective density of states in the conduction band of the semiconductor
N_D – doping concentration
n – density of free electrons
n_i –intrinsic charge carrier concentration
Q – surface charge
Q_{SS} – interface charge
q – magnitude of electronic charge
R_s – series resistance
T – absolute temperature
U_T –thermal voltage
V – voltage
V_B – built-in potential

V_{FB} – oxide surface potential
V_{do} – diffusion potential
V_R – reverse bias
$\bar{\upsilon}_{th}$ – the average thermal velocity of electrons
w – space charge region width
γ – carrier injection coefficient
δ – the thickness of the oxide layer
$\mathcal{E}_{max}$ – the maximum electric field
ε –dielectric constant
ε_0 – vacuum dielectric constant
ε_{0X} – oxide permittivity
ε_i – total permittivity
ε_{rel} – relative dielectric constant
η – ideality coefficient
μ_n – the electron mobility
ν – Poisson coefficient
σ_n – capture cross section
τ_p – the minimum tangential stress needed for dislocation slip in ideal crystal
Φ_0 – "neutral level"
Φ_b – barrier height
Φ_{bb} – distance between the middle of the bandgap and Fermi level
Φ_m – work function of the metal
Φ_{ms} – metal-semiconductor work function
Φ_s – work function of the semiconductor
χ_s – electron affinity
Ψ – surface potential barrier

Contents

INTRODUCTION

The study of metal-semiconductor contacts goes back to 1874, when Braun has discovered the rectification property of metal-semiconductor contacts using mercury metal contacted with copper and iron sulphide semiconductors. Although, the founder of contact phenomenon can be considered Thomas Johann Seebeck, who has discovered thermoelectricity effect in 1820 [1]. The application of metal-semiconductor contacts as radio-frequency detectors is almost as old as wireless telegraphy itself, and in 1906 G.W. Pickard took out a patent for a point-contact rectifier using silicon. In late 1906, General Henry Harrison Chase Dunwoody (1842-1933) obtained the patent [2] for wireless telegraph system with carborundum crystal (called by the inventor as a wave-responsive device) used to detect radio waves (Fig.1).

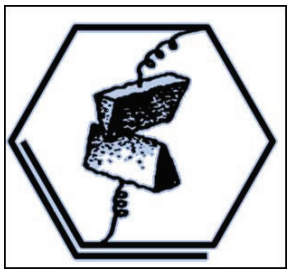


Fig. 1. Some kind of the carborundum wave-responsive devices patented by General H.H.C. Dunwoody [2]

In 1907, Pierce published a paper in Physical Review showing rectification properties of diodes made by sputtering many metals on many semiconductors. The electroluminescence phenomenon (for the light-emitting diode) was discovered by Round in 1907, who observed the generation of yellowish light from crystal of carborundum when he applied a potential between two points on the crystal. In 1938, German physicist Walter H. Schottky suggested that the potential barrier in a metal-semiconductor contact could arise from stable space charge region in the semiconductor alone without the presence of a chemical layer; the potential barrier is known as the Schottky barrier. The Schottky diode (named after German physicist Walter H. Schottky; also known as hot carrier diode) is a semiconductor diode with a low forward voltage drop and a very fast switching action.

The earliest metal-semiconductor M/S diodes in electronics application occurred in the early 1920's when the cat's whisker rectifiers were used in broadcast receivers. The point-contact rectifier or cat's-whisker was used extensively in the early days of radio. The cat's-whisker detectors used in the early days of wireless can be considered as primitive Schottky diodes. But the first real scientific study of the device (and indeed the beginning of semiconductor physics) was stimulated by the wartime use of silicon and germanium point-contact rectifiers as microwave detectors. Point-contact

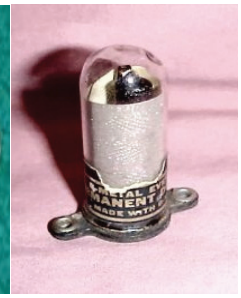
rectifiers were very variable and unreliable in their characteristics, and on that time the present understanding of contact behavior has come with the realization that metal films evaporated onto single-crystal semiconductor surfaces under conditions of high cleanliness can show almost ideal rectification characteristics. The intensive study of contacts in the 1960s and 1970s was largely stimulated by their importance in semiconductor technology, both as rectifying elements and as low resistance or 'ohmic' contacts.

The Schottky diode on Si has been still widely used in the electronics industry finding many uses as a general-purpose rectifier. However, it has come into its own for radio frequency applications because of its high switching speed and high frequency capability. In view of this it is used in many high performance diode ring mixers. In addition, their low turn on voltage and high frequency capability and low capacitance make them ideal as RF detectors. Schottky diodes are also used in high power applications, as rectifiers. The Schottky diode may also be used as a clamp diode in a transistor circuit to speed the operation when used as a switch.

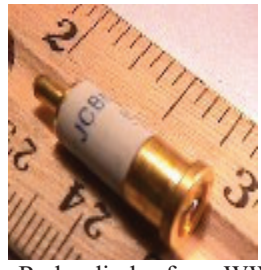
The most evident limitations of Schottky diodes are the relatively low reverse voltage rating for silicon-metal Schottky diodes, 50 V and below, and a relatively high reverse leakage current. Diode designs have been improving over time. Voltage ratings now can reach 200 V. Reverse leakage current, because it increases with temperature, leads to a thermal instability issue. This often limits the useful reverse voltage to well below the actual rating. Therefore, in the past sixty years another way from silicon has been looked for. A significant interest in the development of using of III-V and II-VI compound semiconductors with wide bandgap for high power, high temperature and high frequency applications. The high breakdown voltage of wide bandgap semiconductors is a useful property in high power applications that require large electric fields. Devices for high power and high temperature applications have been developed. Aluminium nitride (AlN) can be used to fabricate ultraviolet light-emitting diode LEDs with wavelengths down to 200-250 nm. Gallium nitride (GaN) is used to make blue LEDs and lasers. The only high bandgap materials in group IV are diamond and silicon carbide (SiC). Silicon carbide is a robust material well suited for such applications. As a wide bandgap semiconductor, the potential advantages of SiC include higher junction temperatures and narrow drift regions (due to a high critical electrical breakdown field value ten times higher than Si) that can result in much lower device on-resistance than is possible in Si. Another important advantage of SiC as a power electronic device material is that its coefficient of thermal expansion (CTE) is better suited to the ceramics used today in packaging technology.

Since 2001 a silicon carbide (SiC) Schottky diode was presented by Siemens Semiconductor (now Infineon): SiC Schottky diodes have about 40 times lower reverse leakage current compared to silicon Schottky diodes and are available in 300 V and 600 V variants. As of 2007 a new 1200 volt 7.5 A variant was sold as 2x2 mm chip for power inverter manufacturers.

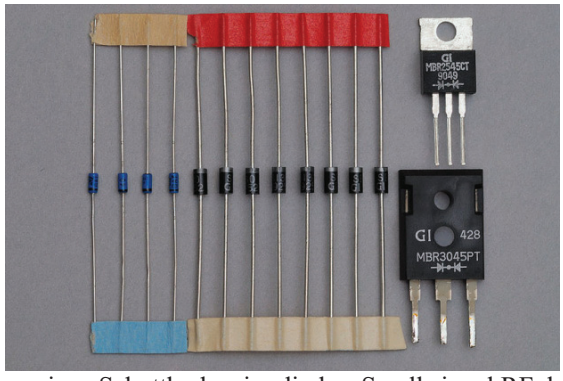
The evolution of the diodes used from the beginning of 1900-s to nowadays are shown on the next pictures (Fig.2).



The Carborundum Company Niagra Falls, New York (~1930) Eveready Co.



Philmore Westfield Machine Company Radar diodes from WWII



The modern various Schottky barrier diodes: Small signal RF devices (left), medium and high power Schottky rectifying diodes (middle and right).

Fig.2. The evolution of Schottky diodes [3]

Chapter 1. Metal-semiconductor contacts

1.1. Theoretical basis of the metal-semiconductor contact

Schottky-Mott model. The rectifying properties of a metal-semiconductor contact arise from the presence of an electrostatic barrier between the metal and the semiconductor. This barrier is due to the difference in work functions of the two materials. If the work function of the metal Φ_m exceeds that of the semiconductor Φ_s, electrons pass from the semiconductor into the metal to equalize the Fermi levels, leaving behind a depletion region in the semiconductor in which the bands are bent upwards (Fig. 3a for the case of an n-type semiconductor).

Assuming that the region of the semiconductor, where the bands are bent upwards is completely devoid of conduction electrons (the so-called depletion approximation), the space charge is due entirely to the uncompensated donor ions. If these are uniformly distributed, there will be a uniform space charge in the depletion region, and the electric field strength will increase linearly with distance from the edge of the depletion region as the metal is approached, in accordance with Gauss's theorem. The magnitude of the electrostatic potential will increase quadratically, and the resulting potential barrier will be parabolic in shape. This is known as a *Schottky barrier*.

It can be shown by a straightforward argument [4] that the amount by which the bands are bent upwards (the so-called diffusion potential V_{do}) is given by

$$V_{d0} = \Phi_m - \Phi_s \, . \tag{1.1}$$

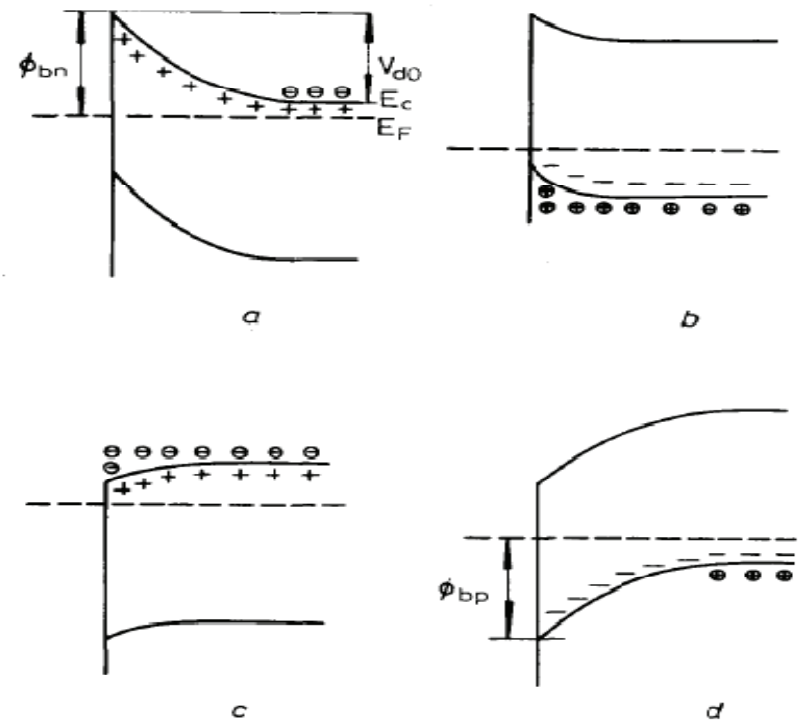


Fig. 3. *Schottky barriers for semiconductors of different types and work functions a)* $\Phi_m > \Phi_s$*, n-type; b)* $\Phi_m > \Phi_s$*, p-type; c)* $\Phi_m < \Phi_s$*, n-type; d)* $\Phi_m < \Phi_s$*, p-type;* [4]

All energies are measured in electron-volts, and so the energy of an electron due to its electrostatic potential is equal to the magnitude of the potential expressed in volts. If $\Phi_m > \Phi_s$, V_{do} is positive and the bands are bent upwards; for the case of an n-type semiconductor this produces a barrier which the electrons have to surmount in order to pass from the semiconductor into the metal, as in Fig. 3a, which, we shall see, leads to rectifying properties. On the other hand, for p-type semiconductor (Fig. 3b), the band-bending causes no impediment to the motion of holes, and no rectification takes place, giving an ohmic contact.

If $\Phi_m < \Phi_s$, the bands are bent downwards. This gives an ohmic contact for an n-type semiconductor (Fig. 3c) and, since holes have difficulty in passing underneath a barrier, a rectifying contact for a p-type semiconductor (Fig. 3d). In nearly all cases $\Phi_m > \Phi_s$ for n-type semiconductors, but $\Phi_m < \Phi_s$ for p-type semiconductors, and so most metal-semiconductor combinations form rectifying contacts. Unless the contrary is clearly stated, all subsequent discussions will centre round the case of *n* -type semiconductors with $\Phi_m > \Phi_s$, which is the most important case in practice.

What is usually quoted is not the diffusion potential but the barrier height Φ_b as viewed from the metal (Fig. 3). For an n-type semiconductor, this is given by

$$\Phi_{bn} = V_{d0} + (E_C - E_F) = \Phi_m - \chi_s \,, \tag{1.2}$$

where $\chi_s = \Phi_s$ — $(Ec - E_F)$ is the electron affinity of the semiconductor, i.e. the difference in energy between the vacuum level and the bottom of the conduction band. Although usually attributed to Schottky [5], Eq. 1.2 was first stated implicitly by Mott [6], and will be referred to as the *Schottky-Mott approximation*. In obtaining it, the assumption is made that the surface dipole contributions to Φ_m and χ_s do not change when the metal and semiconductor come into contact.

The main way in which current can be through a metal-semiconductor contact under forward bias by Schottky-Mott model is the emission of electrons from the semiconductor over the top of the barrier into the metal. Before an electron can be emitted over the barrier into the metal, it must first be transported through the depletion region of the semiconductor. In the latter process its motion is determined by the usual mechanisms of diffusion and drift, while the emission process is controlled by the number of electrons that impinge on unit area of the metal per second. These two processes are essentially in series, and the current is determined predominantly by whichever causes the larger impediment to the flow of electrons.

Historically, the first theory of conduction in Schottky diodes was the diffusion theory of Wagner [7] and Schottky and Spenke [8]. According to this theory, the current is limited by diffusion and drift in the depletion region, and the assumption is made that the conduction electrons in the semiconductor immediately adjacent to the metal are in thermal equilibrium with those in the metal. In contrast, the thermionic-emission theory or diode theory proposed by Bethe [9] assumes that the current is limited by the emission process, and that the quasi-Fermi level for electrons remains horizontal throughout the depletion region, as in a *p-n* junction (see Fig. 3). One can avoid the necessity of postulating a discontinuity in the quasi-Fermi level at the metal-semiconductor interface by regarding the electrons emitted into the metal as "hot" electrons with their own quasi-Fermi level [10].

For an n-type semiconductor, the *J/V* relationship predicted by the diffusion theory can be shown [11] to be

$$J = qN_c\mu_n\mathcal{E}_{max} exp\,(-\tfrac{\Phi_{bn}}{kT})\left[exp\left(\tfrac{qV}{kT}\right) - 1\right], \tag{1.3}$$

where J is the current density per unit area, Nc the effective density of states in the conduction band of the semiconductor, μ_n the electron mobility, $\mathcal{E}_{max}$ the maximum electric field, and Φ_{bn} the barrier height. This is not quite of the form of the ideal rectifier equation $J= J_0$ [$exp(qV/kT$ — 1] because $\mathcal{E}_{max}$ is voltage dependent.

The *J/V* characteristic for the case of the thermionic-emission theory or diode theory can easily be derived if one realizes that, under the application of a

forward bias *V,* a flat quasi-Fermi level implies that the electron concentration in the semiconductor just inside the interface is given by

$$n = N_c exp[-(\Phi_{bn} - qV)/kT] \tag{1.4}$$

(see Fig. 4). The flux of these electrons across the interface into the metal can be shown by elementary kinetic theory to be $n\bar{v}_{th}/4$, where $\bar{v}_{th}$ is the average thermal velocity of electrons in the semiconductor. The flux in the reverse direction, which is independent of voltage *V,* must exactly balance the flux of electrons from semiconductor to metal when no bias is applied, and so the net current density is given by

$$\begin{aligned} J &= \frac{qN_c\bar{v}_{th}}{4} ex\,p\left(-\frac{\Phi_{bn}}{kT}\right)\left[exp\left(\frac{qV}{kT}\right) - 1\right] \\ &= A^*T^2 ex\,p\left(-\frac{\Phi_{bn}}{kT}\right)\left[exp\left(\frac{qV}{kT}\right) - 1\right], \end{aligned} \tag{1.5}$$

where $A^*=(4\pi m^* qk^2)/h^3$ is the Richardson's constant corresponding to the effective mass of electron in the semiconductor.

Modifications to Schottky-Mott theory. The Schottky-Mott approximation (Eq. 1.2) assumes that the surface dipole contributions to Φ_m and χ_s do not change when the metal and the semiconductor is brought into contact. These surface dipole layers arise because at the surface of a solid the atoms have neighbors on one side only. This causes a distortion of the electron cloud belonging to the surface atoms, so that the centers of the positive and negative charge distributions do not coincide. It was soon discovered that the linear dependence of Φ_{bn} on Φ_m predicted by Eq. 1.2 does not occur in practice, and so the assumption of constancy of the surface dipole layers cannot be true.

One of the first explanations for the departures of the experimental data from Eq. 1.2 was given by Bardeen [12], who pointed out the importance of localised surface states. For our present purpose it is sufficiently accurate to regard surface states as unsatisfied bonds on the surface of the semiconductor. At the surface, the atoms have neighbours on one side only, and on the vacuum side the valence electrons have no partners with which to form covalent bonds. Each surface atom, therefore, has associated with it an unpaired electron in a localized orbital, directed away from the surface. Such an orbital is often spoken of as a dangling bond. It can either give up its electron, acting as a donor, or accept another acting as an acceptor. The surface states are usually continuously distributed in energy within the forbidden gap, and are characterized by a neutral level Φ_0 such that, if the surface states are occupied up to Φ_0 and empty above Φ_0, the surface is electrically neutral. In general, the Fermi level does not coincide with the neutral level, and in this case there will be a net charge in the surface states.

In most practical metal-semiconductor contacts the ideal situation shown in Fig. 3a is never reached, because there is usually a thin supplementary intermediate layer of different composition of nanometers thick on the surface of

the semiconductor. Such film is referred to as an interfacial layer. A practical contact is, therefore, more like Fig. 4.

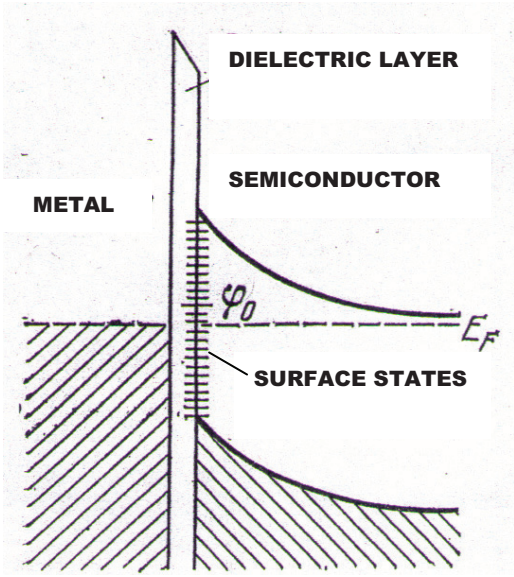


Fig.4. Metal-semiconductor contact with the surface states [4]

The presence of such a dielectric layer leads to the effect of tunneling of the electrons through the barrier under the forward bias.

If, in addition, there is a thin oxide layer between the metal and the semiconductor, as will happen if the surface of the latter has been prepared by chemical polishing, the charge in the surface states together with its image charge on the surface of the metal will constitute a dipole layer. This dipole layer will alter the potential difference between the semiconductor and the metal and will upset Eq. 1.2. It was shown by Cowley and Sze [13] that, according to the Bardeen model, the barrier height is given approximately by

$$\Phi_{bn} = \gamma(\Phi_m - \chi_s) + (1 - \gamma)(E_g - \Phi_0), \tag{1.6}$$

where

$$\gamma = \frac{\varepsilon_i}{\varepsilon_i + q\delta D_S}\ , \tag{1.7}$$

E_g is the bandgap of the semiconductor, δ the thickness of the oxide layer, and ε_i its total permittivity. The surface states are assumed to be uniformly distributed in energy within the bandgap, with a density D_S per electron-volt per unit area. The position of the neutral level Φ_0 is measured from the top of the valence band.

If there are no surface states, $D_S = 0$ and $\gamma = 1$, and so Eq. 1.3 gives $\Phi_{bn} = \Phi_m - \chi_s$, which is the Schottky-Mott approximation. If the density of states is very high, γ becomes very small and Φ_{bn} approaches the value $E_g — \Phi_0$. This is because a very small deviation of the Fermi level from the neutral level can produce a large dipole moment, which stabilises the barrier height by a sort of negative feedback effect. The Fermi level is said to be 'pinned' relative to the bandedges by the surface states.

A similar analysis for the case of a p-type semiconductor shows that Φ_{bp} is approximately given by

$$\Phi_{bp} = \gamma\left(E_g - \Phi_m + \chi_s\right) + (1-\gamma)\Phi_0 \ . \tag{1.8}$$

Hence, if Φ_{bn} and Φ_{bp} refer to the same metal on n- and p-type specimens of the same semiconductor, we should have

$$\Phi_{bn} + \Phi_{bp} \cong E_g, \tag{1.9}$$

if the semiconductor surface is prepared in the same way in both cases, so that δ, ε_i, D_s, and Φ_0 are the same. This relationship holds quite well in practice [14]. It is usually true that $\Phi_{bn} > E_g/2$, and so $\Phi_{bn} > \Phi_{bp}$.

Intimate contacts

The Bardeen model assumes the existence of an insulating layer between the metal and semiconductor, as evidenced by the occurrence of δ and ε_i in the expression for γ (Eq. 1.3). This corresponds quite closely to the majority of practical contacts, which are fabricated in such a way that there is a thin oxide layer on the surface of the semiconductor. Occasionally, for research purposes, contacts are made by cleaving a crystal of the semiconductor in an ultra-high vacuum system and then evaporating a metal film before there is time for an oxide layer to form on the freshly created surface. Such a contact is known as an intimate contact, and is devoid of any interfacial layer. We must now ask, whether Bardeen's model of the effect of surface states can be applied to such an intimate contact.

In Bardeen's analysis, the interface states are regarded as point charges, and the term $q\delta$ in the expression for γ is simply the dipole moment of a charged interface state together with its balancing charge on the surface of the metal. But the interface states actually extend into the semiconductor to a distance of about 1 nm, and even if there is no interfacial layer there is still a dipole between a charged interface state and the surface of the metal. This point of view has been developed by Heine [15], who regards the interface states as the exponentially decaying tails of the wave functions of the conduction electrons in the metal, which can penetrate into the bandgap of the semiconductor by tunneling. The situation is much more difficult to analyse theoretically than when there is an interfacial layer present, because the density of the interface states and the position of the neutral level Φ_0 both depend on the metal as well as on the semiconductor [16].

Rhoderick's [4] present ideas of barrier formation at intimate metal-semiconductor contacts are influenced very largely by three recent pieces of experimental evidence:

(a) It is now well established (e.g. from the work of Thanailakis and co-workers [17, 18] that Φ_{bn} is not a monotonically increasing function of Φ_m. Indeed, there is some group of metals, for which Φ_{bn} actually decreases as Φ_m increases.

(b) It has recently been discovered that the nature of the barrier produced when a particular metal makes contact with a semiconductor can be correlated with the chemical properties of the metal, i.e. with whether or not a chemical reaction takes place at the interface [19].

(c) It is now recognised that ideally sharp boundaries at metal-semiconductor junctions hardly ever occur in practice, even if the metal is deposited at room temperature on a cleaved semiconductor in an ultra-high-vacuum. There may be an alloy phase at the interface, or there may be a gradual transition from metal to semiconductor over a distance of 10 Å or more due to interdiffusion effects [20].

1.2. Metal-semiconductor interface

The real situation on the metal-semiconductor interface is even more complicated. Most contacts used in semiconductor devices are subjected to heat treatment, for instance, the annealing process in the sputtering deposition technology (usually at the temperatures above 950 ^{0}C). This may be deliberate, to promote adhesion of the metal to the semiconductor, or unavoidable, because high temperatures are needed for other processing stages which occur after the metal is deposited. It is important to avoid the melting of rectifying contacts, because if this happens the interface may become markedly nonplanar, with sharp metallic spikes projecting into the semiconductor. When this occurs, tunnelling through the high-field region at the tip of the spike may severely degrade the electrical characteristics [21]. Unless alloying of the contact is desired (e.g. in the formation of ohmic contacts), it is necessary to keep the temperatures to which contacts are subjected below the eutectic temperature of the metal-semiconductor system. The other problem is that on the metal-semiconductor interfaces different kinds of interfacial phases can take place. Two possible mechanisms of forming an interfacial amorphous phase are:

1. Solid-state reaction (SSR);
2. Freezing of an eutectic liquid.

Even at the temperatures substantially below the euthetic temperature, migration of the semiconductor through the metal may occur. As a result of the migration, the electrical characteristics become nonideal. The change in *I-V* characteristics cannot normally be explained simply in terms of a change in barrier height, but as a rule the whole shape of the characteristic alters to such an extent that it is clear that we no longer have a simple Schottky barrier.

The study of metal-semiconductor interface formed without extensive chemical reaction is particularly interesting due to the abrupt change in the lattice bonding and electron structure across the interface. SiC becomes chemically reactive with most metals at elevated temperatures, and many metals react with SiC at relatively low temperatures to form silicides and carbon or carbides. Some metals only react with Si to form metal silicides not with carbon at elevated temperatures. One example is Pd which reacts with SiC to form Pd silicides and carbon at temperatures as low as 300 ^{0}C [22]. Kurimoto et al. [23]. reported that the Ni silicides, composed of Ni_2Si, NiSi, and $NiSi_2$, are formed at 500 °C, and the composition does not vary in the temperature region of 500–1100 °C. However, the effects of the carbon phase and its structural changes after annealing on electrical contact properties have not received adequate attention. In addition, from the standpoint of surface structures, SiC graphitizes due to the preferential volatility of silicon, when the annealing temperature is above 900 °C [24]. A graphitic carbon phase is found in Ni/SiC after annealing above 1000 °C [25]. The ability of some metals mostly used for metallization to form carbides and/or silicides in contact with silicon is shown in Table 1.

Table 1. The interaction of carbon and silicon in various metals

metals	***carbides***	***silicides***
Al	Al_4C_3	
Au	AuC	
Co	Co_2C	
Cr	Cr_3C_2	
Mo	Mo_2C	
Ni	Ni_2C	Ni_2Si, NiSi, $NiSi_2$
Ti	TiC	Ti_5Si_3, $TiSi_2$
W	WC, W_2C	W_2Si, W_5Si_3,

Aluminum is a metal that forms Al_4C_3 only and no aluminum silicides. Aluminum-based ohmic contacts are commonly used on p-type SiC and have been described by many research groups.

It is worth to notice that all the intermetallics formed at the metal/semiconductor interface can have *ordered* (interfacial layers) or *disordered* (small-grained) structure. These disordered structures can lead to more complicated picture of the interface between metal and semiconductor. In other words, a metal-semiconductor contact can be considered as consisting of two successive junctions between metal and semiconductor: metal/interfacial layer junction and interfacial layer/semiconductor junction that in turns leads to distortion in the current-voltage characteristics.

Tanimoto et al. [25] have examined the microstructure at the interface between the Ti/Al contacts and SiC by using Auger electron spectroscopy and found that carbides containing Ti and Si were formed at the interface. Recently,

[26] suggested that aluminum carbide and Al-doped Si formed at the interface might be the primary current-transport paths in the Ti/Al contacts to p-type SiC.

Tsukimoto et al. [27] have investigated and compared the electrical properties and microstructure of Ti/Al and Ni/Ti/Al ohmic contacts evaporated using electron beam evaporation on p-type 4H-SiC by using the *I-V* measurements, x-ray diffraction microscope (XRD) and transmission electron microscope (TEM). The TEM observation revealed that the interfacial Ti_3SiC_2 carbide layers were formed directly on the SiC surface in both the Ti/Al and Ni/Ti/Al contacts. Fig. 5 shows a cross-sectional bright-field TEM micrograph of a typical region in the Ti/Al ohmic contact formed on the 4H-SiC.

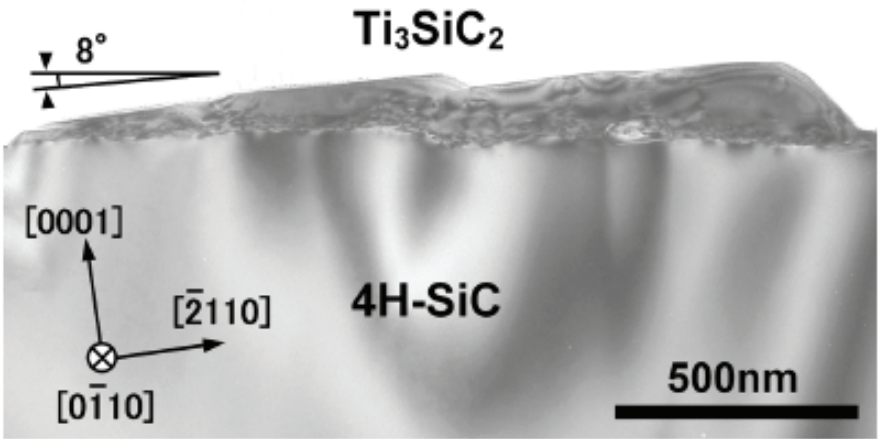


Fig. 5. A cross-sectional bright-field TEM micrograph at the interface between a Ti/Al contact and 4H-SiC annealed at 1000^0C for 2 min. [27]

The Ti/Al contact forms a plate-shaped layer directly on the SiC substrate. The plate-shaped layer was identified as a ternary Ti_3SiC_2 compound by indexing the diffraction patterns. The thickness of the Ti_3SiC_2 layer is not uniform and ranges from 30nm to 300nm. The total area of the SiC substrate surface is covered by the Ti_3SiC_2 layers, meaning that no other compounds make direct contact with the SiC surface. From the present TEM observations, Tsukimoto has concluded that the rough interface formed after annealing the Ti/Al contacts exclusively consists of Ti_3SiC_2 in contact with SiC. Several pits (~200 nm in depth in the substrate) were observed at the surface. A typical cross-sectional bright-field TEM micrograph of the interface between the Ni/Ti/Al contact and 4H-SiC is shown in Fig. 6

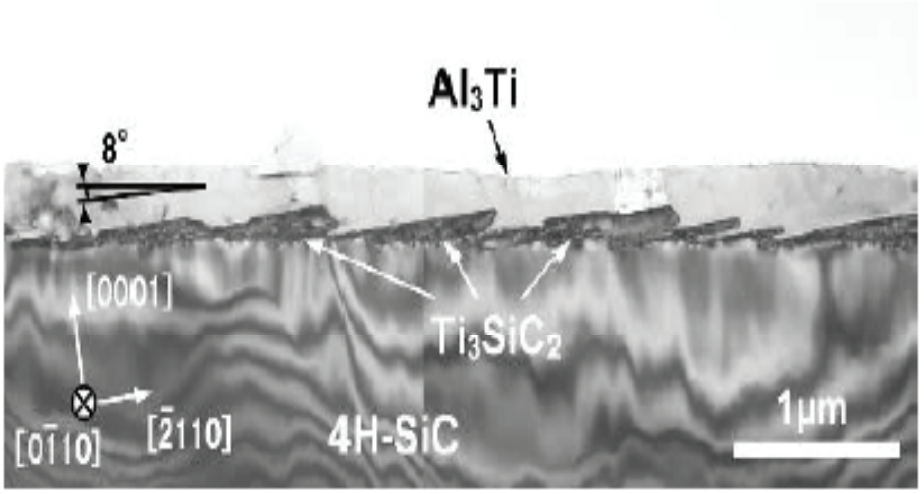


Fig. 6. A cross-sectional bright-field TEM micrograph at the interface between Ni/Ti/Al contact and 4H-SiC [27]

The microstructure of the Ni/Ti/Al ohmic contact is similar to that of the Ti/Al ohmic contact. The ternary Ti_3SiC_2 and the binary Al_3Ti compound layers are the major compounds as observed in this TEM micrograph. The plate-shaped Ti_3SiC_2 layers make direct contact with the SiC surface. The thickness of the Ti_3SiC_2 layers is not uniform and the thickest layer is approximately 200nm. The coverage of Ti_3SiC_2 layers on the SiC surface was estimated to be close to 90% from the present TEM micrograph. In contrast, in the Ti/Al contacts, the Ti_3SiC_2 layers had 100% coverage on the SiC surface.

Fig. 7 a and b illustrate the cross section of the microstructures, and the corresponding energy band diagrams at the TiAl-based contact/p-type SiC interface before and after annealing, respectively.

From the high-resolution transmission electron microscope (HRTEM) observation, the interfaces between the epitaxial Ti_3SiC_2 layers and 4H-SiC were found to be atomically flat without any contamination layers.

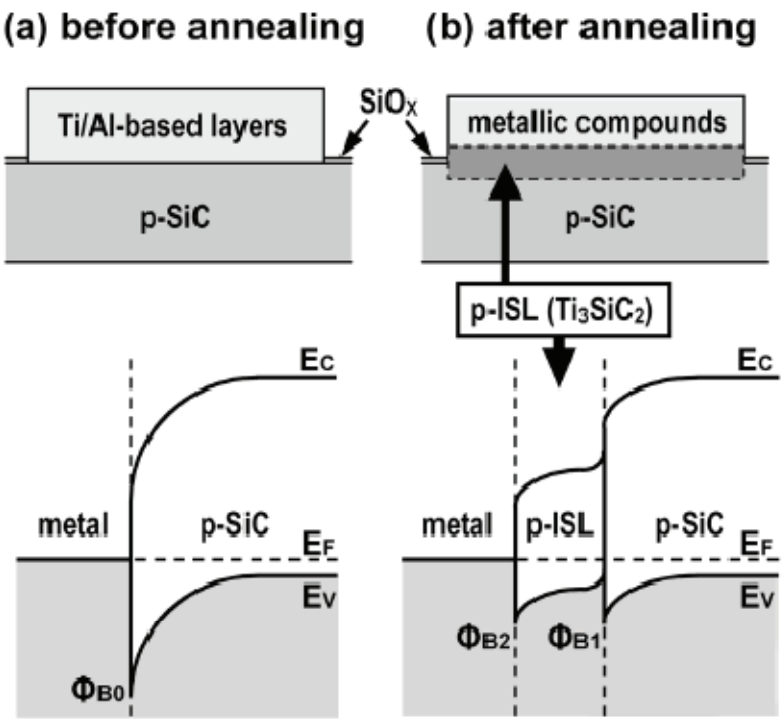


Fig. 7. Schematic illustrations of cross-sectional microstructures and energy band diagrams at the interface between the Ti/Al-based contact and p-type SiC (a) before annealing and (b) after annealing [27]

Before annealing, a large barrier height (Φ_{b0}) is formed at the metallic layer/p-type SiC interface [28] Recently, Lee et al. [29] measured the barrier heights at the interfaces between metal layers and p-type 4H-SiC using *I-V* and *C-V* methods. They reported that the Φ_{b0} values were 1.96eV and 1.41eV for Ti and Ni layers, respectively. These vales would be too large to obtain ohmic behavior for p-type SiC with Al concentration of $4.5 \times 10^{18} cm^{-3}$. Thus, the current transport through the metal/SiC interface would be hindered by this high barrier existing before annealing (Fig.7a). The carbide layers formed after annealing may divide the high barrier height Φ_{b0} into two barriers of Φ_{b1} and Φ_{b2}, as shown in Fig. 7b.

In addition to the microstructure, the morphology at the interface between the intermediate semiconductor layers (ISL) and p-SiC may also be important for the ohmic contact formation. Aboelfotoh et al. [30] suggested that Schottky barrier heights on covalent semiconductors such as SiC depended weaky on the metal work function; thus, the partial Fermi level pinning would be caused by the interface states. They also pointed out that the chemical bonding at the interface played an important role in determinining the barrier height. Their suggestion implies that the Fermi level at the ISL/SiC interface may be unpinned by controlling the chemical bonding and interfacial morphology.

Teraji et al. [31] also pointed out that an atomically flat and clean interface was needed to reduce the interface state density.

Masakatsu et al. [32] haveinvestigated the microstructure of TiAl/SiC interface formed by solid-state diffusion bonding, where a TiAl foil was inserted between two SiC specimen and set in a high-frequency induction-heating vacuum furnace in a temperature ranges between 1573 K and 1673 K under the uniaxial pressure of 126 MPa between the time ranges of 15 min and 54 min. The interface microstructure and growth behavior of the reaction products were analyzed by means of scanning electron microscope (SEM), Electron Probe Microanalysis (EPMA) and XRD and considered on the basis of the Ti-Al-Si-C quaternary chemical potential diagram. Four layers of reaction products are formed at the interface by diffusion bonding: a layer of TiC adjacent to SiC followed by a diphase layer of TiC+Ti_2AlC, a layer of $Ti_5Si_3C_X$ containing Ti_2AlC particles and a layer of $TiAl_2$. However, the $TiAl_2$ layer was formed during cooling.

The presence of the interfacial layer may lead to the following effects:

1. May lead to the potential drop at the interfacial layer. Therefore, the barrier height under zero bias is less than for an ideal diode (the barrier height here is the maximum distance between the bottom of conduction band in semiconductor and Fermi level in metal. This barrier height differs from the barrier height between the metal and the dielectric layer).
2. The electrons can tunnel through the barrier formed by interfacial layer and that, in turns, changes current-voltage characteristic at a given bias. The probability of tunnelling through an interfacial layer at low voltages associated with the overlap of electron clouds on either side of the barrier. This probability arises because of the presence of a large number of free electron states in the interfacial layer.
3. At the applied bias some part of it drops on the interfacial layer, therefore, the barrier height depends on voltage bias. That, in turns, leads to the distortion of the current-voltage characteristics and can be described by the increasing of the ideality factor.

1.3. Diffusion-welded Al/SiC contacts

During the diffusion welding of Al to SiC the possibility of intermetals formation is quite small due to the low process temperatures. Anyway, the process of diffusion welding has its own peculiar properties. The processes of solid state bonding of metal and semiconductor can be subdivided into three stages: [33, 34]

1) Intimate closing of materials (creation of physical contact);
2) Contact area activation (generation of active centers);
3) Development of bulk interaction.

At the first stage, the materials are closing together to a distance where van der Waals forces are acting and where slight chemical interaction is taking place. This is possible only due the microplastic deformation of, at least, one of the materials going to be bonded. At this time, the contact surfaces of the material being under plastic deformation are activated due to the dislocations outlet. This creates the conditions for slight chemical coupling of materials being in contact. In solid-state welding of dissimilar materials, for example, metals and semiconductors, the first stage is completed with a slight chemical interaction.

At the second stage, active centers are formed on surface of the harder material, e.g. semiconductor. The duration of this period is conditioned by specifics of plastic microdeformation as well as by incubation period for creation of the centers [35, 36].

The third stage begins from the moment, when the active centers are already formed. During this stage, the interactions of bonding materials are developed both in interface and bulk zones. This process is running on the active centers that are, in particular, the dislocations with surrounding stress fields. In the interface, this process ends with conjunction of interaction centers.

Therefore, the interaction of semiconductor and metal is in the places where dislocations are present. This fact allows concluding that during diffusion welding under loading and heating, the microplastic deformation of semiconductor layer is taking place and this process is dominant in the interaction. Besides that, in the surface layer of semiconductor the process of stress relaxation was found at elevated temperature that can be explained by dislocation motion. The dislocation motion in covalent crystals needs electron transmission from one linkage to another, i.e. destruction and translation of the linkages. So during diffusion welding process broken links are generated in semiconductor surface layer due to dislocation motion. The broken links serve as active centers for topochemical reaction between metal and semiconductor. In addition, the dislocation motion is accompanied by wake of point defects (vacancies) that in turn supply the surface with supplementary centers of interaction. The micro plastic deformation of surface layer was studied by the so-called soft prick method [37, 38] and by normal axial loading [39, 40]. The fact of generation and motion of dislocations in the surface layer of semiconductor was established.

Dr. Korolkov in his work [41] has made an attempt to calculate the minimum shear stress necessary to displace an atom between two adjacent position for hexagonal SiC. To overcome the potential barrier between two adjacent positions of dislocation a force must be applied. This force named as Peierls force or Peierls barrier and it is equal to

$$f_p = b\tau_p, \tag{1.10}$$

where b is the Burgers vector, and τ_p is the minimum tangential stress needed for dislocation slip in ideal crystal. The calculation of Peierls force is a very difficult and not completely solved problem. The analytical method of Peierls

for sinusoidal law of interaction force between two adjacent planes of atoms gives the expression for Peierls stress

$$\tau_p = \frac{2G}{1-\nu} e^{-\frac{2\pi}{1-\nu}\frac{c}{a}} , \quad (1.11)$$

where, G – the shear modulus, ν – the Poisson coefficient, c – the distance between two adjacent slip planes, and a – the lattice space in plane of slip.
The greater is interatomic bond force, which is expressed by shear modulus G, the greater is τ_p.

The critical tangential stress strongly depends on $\frac{c}{a}$ ratio and sharply decreases with an increase of $\frac{c}{a}$. For the planes of atoms with close-packed lattice this ratio usually is the greatest and that is why the slip more easily proceeds in closed-packed planes (for hexagonal SiC it is (0001) plane).

In elasticity theory [42] the basic elastic parameters of the crystal are bound with each other by the ratio

$$E = 2G(1+\nu), \quad (1.12)$$

where E is the Young's modulus. Then

$$\nu = \frac{E}{2G} - 1 . \quad (1.13)$$

By use of crystal elastic coefficients the basic elastic parameters can be described as

$$G = C_{44} , \; E = \frac{C_{44}(3C_{12}+2C_{44})}{C_{12}+C_{44}}, \quad \nu = \frac{C_{12}}{2\,(C_{12}+C_{44})} . \quad (1.14)$$

The ratios $\frac{c}{a}$ are 3.27 for 4H-SiC and 4.91 for 6H-SiC (the values of c and a for 4H-SiC and 6H-SiC are taken from [43]).

In that way, by use of quantitative values of elastic coefficients from [43] and neglecting the orientation factors the rough preliminary estimate gives $\tau_p \sim 10^{-5}$ Pa for 6H-SiC and $\tau_p \sim 10^{-1}$ Pa for 4H-SiC. Proceeding from the Prandtl solution for the model of pressing of the plastic layer between two rough plates the tangential stresses on the contacts may reach the yield stress of plastic material [44]. In this case, the yield stress of aluminum at welding temperature equal to 2–3 MPa is the tangential stress on Al/SiC contact and exceeds the critical Peierls stress τ_p by many orders of magnitude. It is the matter of fact that this problem is far more complicated.

On the other hand, the theoretical preconditions do not turn down the possibility of plastic deformation in the surface layer of SiC under DW

condition. And as the evidence of this fact the microscope pictures of the 6H-SiC areas before and after diffusion welding are illustrated in the Ph.D. thesis of Dr. Oleg Korolkov [41]. On these pictures the fact of dislocation motion was shown that, in turn, is the evidance of microplastic surface deformation in the formation of DW contact for SiC, so as it was established earlier to Si. It must be noted that after removal of Al from SiC surface by etching in hydrochloric acid no typical marks of surface interaction could be found. The local pits of solid state etching, typical for diffusion welding of Si, were not found on the SiC surface. Apparently, in the process of solid state solving of SiC in Al only the silicon atoms of silicon carbide take part leaving unreacted carbon atoms behind. Such separate solving destroys the surface crystal structure and is equal to the process of isotropic etching after which the surface remains smooth and polished.

The problem statement:

Thus, as seen from above, the actual metal-semiconductor contacts may differ significantly from the model proposed by Schottky-Mott. In the metal-semiconductor contacts are always present an intermediate layer, the structure and properties of which depend on the method and conditions of contact preparation. Therefore, the real Schottky parameters may differ significantly from the calculated and mathematical tools can be used with certain assumptions, as a preliminary estimate of real output parameters of the model.

At the present time can be viewed two parallel paths of development of the situation.

- Path number one. Improving the conditions for obtaining metal-semiconductor contact in order to better fit his ideal model of the Schottky-Mott. Modern technical conditions give such a possibility just now, eg. the use of outer space for the manufacture of Schottky contacts. But keep in mind that the cost of such devices will also be out of space height.
- Another way is more practical. It is the way of operating with real contacts obtained in our earthly environment. The way that makes it possible to produce the necessary devices by commercially acceptable prices. But in this way you need to know what we are dealing with. In other words, you need to study the characteristic features of contacts depending on the method of metallization and try to control their properties.

Being a practical /wo/man, I choose the second path, which defines the problem statement of my doctoral thesis: ***"Investigation of the intermediate layer in the metal-silicon carbide contact obtained by diffusion welding".***

Chapter 2. *I-V* characteristics and Schottky parameters of DW contacts

As a first step of the experimental part of the thesis was to measure the forward current-voltage characteristics of the diffusion welded metal-semiconductor contact.

For this purpose were used the silicon carbide wafers specially prepared for Schottky contacts: n^0 – n^- 4H-SiC epi-structure from Cree Research Inc., thickness 0.35 mm., epi-layer thickness 5μm. Net nitrogen doping density in epi-layer $N_d \sim 1x10^{15}$ cm^{-3}. Substrate orientation: (0001), Si, 8º off.

Double oxide layer consisting of naturally grown and (CVD) deposited SiO_2 oxide layers with a thickness of ~ 1 μm were grown/deposited on epi-layer. After oxidation, a nickel contact was performed on the heavily doped backside substrate and annealed at 1100 ºC. To obtain a thicker ohmic contact, the gold layer of 1 μm thickness was further sputtered over annealed nickel. Then the plate was cut into chips of size 5x5 mm^2. Prior to Schottky contact fabrication circular contact windows of 1 mm diameter had been opened in the oxide layer by the lithography technique. All of the above preparations were carried out in collaboration with the Technologies and Devices International Inc. (TDI Inc.,USA).

An aluminum foil of 30 μm thick was welded over the entire surface of epi-layer of the chips. Diffusion welding was carried out in vacuum not worse than 10^{-4} torr at a temperature of ~ 600 ºC and a pressure of 30 MPa. Thus, the metal contact of 1 mm diameter was formed to low doped epi-layer of silicon carbide structure. The cross-section scheme of the experimental specimen is shown in Fig. 8.

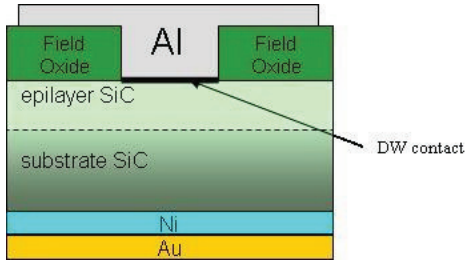


Fig. 8. Schematical cross-sectional picture of the experimental specimen

On the fabricated samples the forward current-voltage characteristics were measured. The measurements were carried out on Agilent Technologies Analyzer B 1500A (USA) applying DC voltage/current mode. The typical view of *J-V* characteristics at room temperature for the diffusion welded Al/SiC contacts are shown in Fig.9.

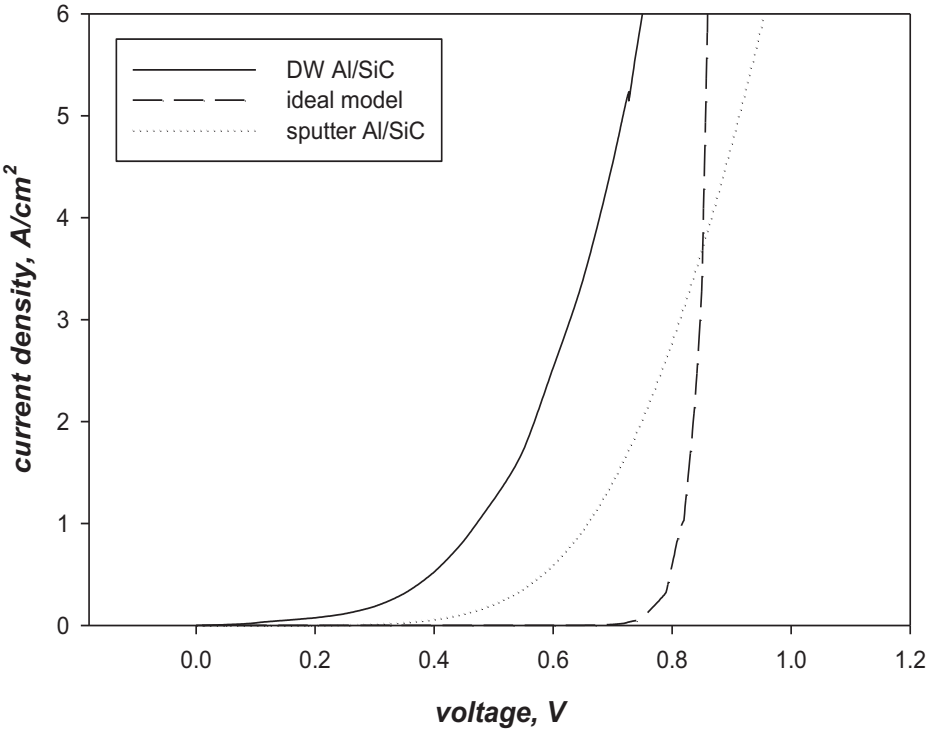


Fig.9. *J-V* characteristics for Al/SiC contacts

For comparison, Fig. 9 also shows the current-voltage characteristics for sputtered aluminium contact to SiC, kindly provided by William R. Harrell, who is one of the authors of [45] (marked as *sputter Al/SiC*). As a reference also presents the *J-V* characteristic, which corresponds to the ideal Schottky-Mott model calculated for an ideality coefficient η=1, barrier height for Al/SiC Φ_b=0.6 eV, T=293 K, Richardson's constant A^*=120 $Acm^{-2}K^{-2}$ [46] and for series resistance R_s =0 (marked as *ideal model*).

As seen from Fig. 9 for the relatively small voltages, in sputtered and diffusion-welded contacts current is growing significantly faster (lower threshold) than in the ideal model. Externally, this looks like as the barrier height is reduced, and/or in addition to the thermionic current another current appears. Semilogarithmic representation of the *J-V* characteristics in Fig. 10 supplements the above picture.

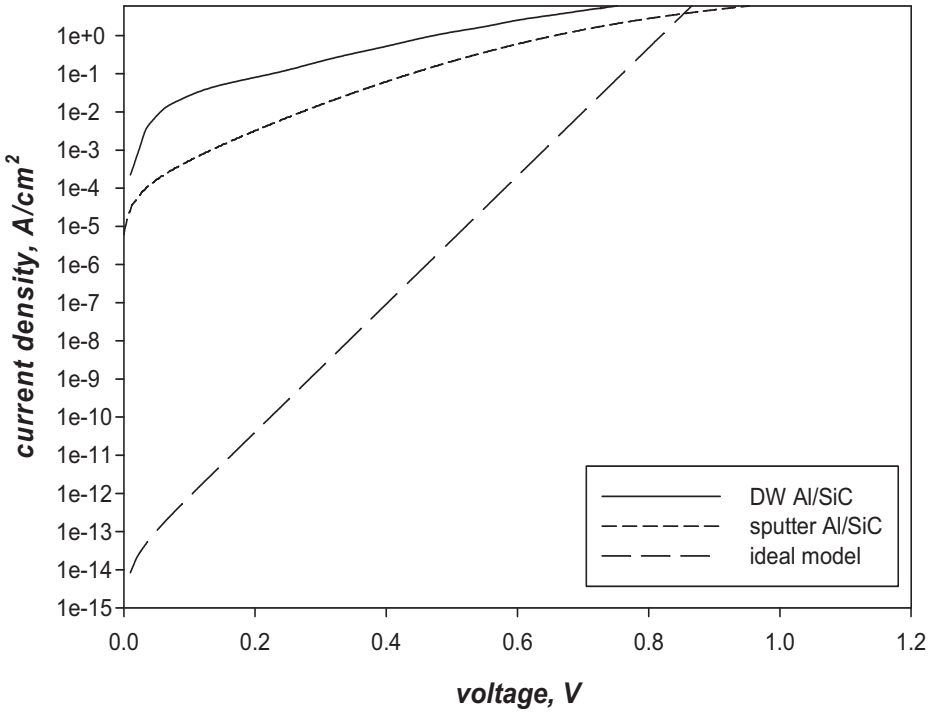


Fig. 10. Semilogarithmic representation of the *J-V* characteristics for Al/SiC contacts

This view clearly shows how much is the difference between the experimental *J-V* curves and calculated theoretical exponent of the ideal Schottky-Mott model. Higher current density at the same voltages in the DW contacts in comparison with evaporated contacts, apparently, can be explained, by a decrease of the parasitic spreading resistance in thick aluminum foil welded to the contacts surface.

Current flow through metal-semiconductor contact is possible by the following mechanisms:

- the emission of electrons from the semiconductor over the barrier into the metal (thermionic emission);
- quantum mechanical tunnelling through the barrier;
- recombination in the space charge region and in the neutral region.

Last two of these mechanisms the most probably can cause additional to the thermionic current and this is going to be clarified in the further analysis.

For this purpose, on the diffusion-welded contacts were measured direct *J-V* characteristics in the temperature range of 20÷500 ºC (Fig. 11).

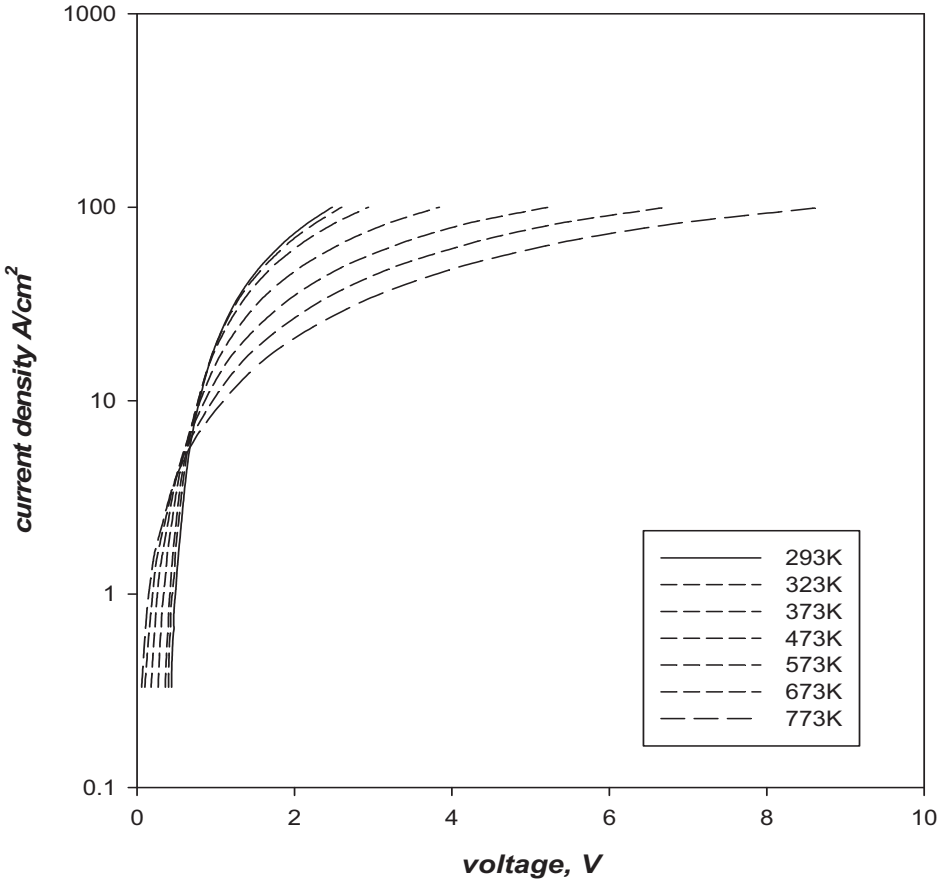


Fig. 11. *J-V* characteristics for DW contacts in temperature range of 293 ÷773 K

Applying known techniques, well described in the work by Cheung [47], we can calculate the basic parameters of the Schottky DW contact. The *J-V* relationship under thermionic emission theory is given by

$$J = J_s \left[exp\left(\frac{qV}{\eta kT}\right) - 1 \right], \tag{2.1}$$

where

$$J_s = A^{**}T^2 exp\left[-\frac{\Phi_b}{kT}\right]. \tag{2.2}$$

If $V>3kT/q$, then the exponential term in the Eq. 2.2 dominates, and J can be approximated as

$$J = J_s \exp\left(\frac{qV}{nkT}\right), \tag{2.3}$$

J_S and η can, thus, be determined from the experimentally obtained forward current density-voltage (J-V) characteristics at a given temperature. J_S can be measured by extrapolating the linear region of the $ln\ J$ versus V plot to V=0, and η can be determined by modifying Eq. 2.3 as

$$\eta \equiv \frac{q}{kT}\frac{dV}{d\ln J}. \tag{2.4}$$

High-temperature forward J-V data was utilized to obtain the Richardson's constant. The quantity can be found from the y-intercept obtained from the following equation:

$$\ln\left(\frac{J_S}{T^2}\right) = -\frac{\Phi_b}{k}\left(\frac{1}{T}\right) + \ln(A^{**}). \tag{2.5}$$

By use of Arrhenius curves (Fig. 12) the Richardson's constant was determined.

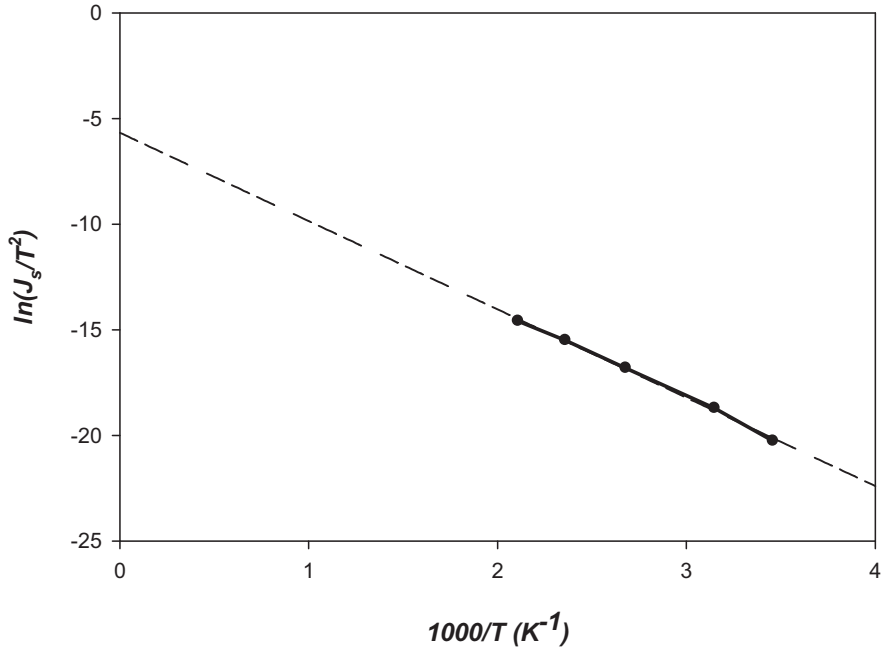


Fig. 12. Arrhenius plot for DW contact

The Schottky barrier height was evaluated by defining a function *H(J)* given by [47]

$$H(J) \equiv V - \left(\frac{\eta kT}{q}\right) ln\left(\frac{J}{A^{**}T^2}\right). \quad (2.6)$$

Applying the equation

$$J = J_S \exp\left[\frac{q(V-IR_S)}{\eta kT}\right], \quad (2.7)$$

H(J) can be deduced as

$$H(J) = R_S J + \eta\Phi_b. \quad (2.8)$$

The plot of *H(J)* vs. *J* gives a straight line which intercepts the *y* axis at $\eta\Phi_b$. Using the ideality factor value extracted from the *d(V)/d(lnJ)* vs. *J* plot, the barrier height can be determined. The obtained key Schottky parameters are J_S=1.0x10^{-6} A/cm^2, Φ_b=0.27 eV, η=1.65 and A^{**}=6.2x10^{-7} A/cm^{2}K^2.

In a rigorous approach, the use of purely thermionic theory for the extraction of Schottky parameters in case of significant deviations from the ideal model is not quite correct. However, since our aim is to obtain the analytical material for building our own version of the reasons for the deviation of the DW contact from the ideal model, the use of this approach can be considered as legitimate.

As was predicted on the basis of *J-V* characteristics (Fig. 9) DW contact parameters disagree with theoretical values in Schottky-Mott limitation condition. For example, in ideal Schottky-Mott model valid in the absence of significant density of interface states, the barrier height in electron-volts is given by

$$\Phi_b = \Phi_m - \chi, \quad (2.9)$$

where Φ_m is the metal work function.

Work function for many metals are readily obtained from many references and the work function for Al averaged from many experimental results can be taken as 4.20 eV [48]. Using this value for Φ_m along with χ = 3.6 eV in Eq. 2.9 the theoretical barrier height is Φ_b = 0.6 eV. As it seen, the theoretical result is more than two times over the experimental result Φ_b = 0.27 eV for DW Al contact to n-type 4H-SiC at room temperature. Strong difference is observed for saturation current J_s and ideality factor η, compared with the ideal model. But the most significant difference is observed for the Richardson's constant.

The experimental Richardson's constants for DW contacts are nine orders of magnitude lower than theoretical value.

The Richardson's constant for electron rest mass is found to be $A = 120$ Acm^{-2}K^{-2}.

Thus, originating from universal Richardson's constant formula

$$A = \frac{4\pi m_0 q k^2}{h^3}, \tag{2.10}$$

the ratio between effective and rest mass of electron must be: $\frac{m^*}{m_0} = \frac{A^*}{A} = \frac{146}{120} = 1.22.$

Taking into account the probabilities of electron scattering on low-frequency phonons (f_{ph}) and quantum-mechanical reflection of electrons (f_d), $A^{**} = f_{ph} f_d A^*$ may be not less than 50 % of A^* [4]. In this case the mass ratio can be $\frac{m^*}{m_0} = 0.61.$

The Richardson's constants extracted from experimental *J-V* characteristics of DW contacts give the effective and rest mass ratio 6.2×10^{-9}.

Saxena with co-authors in their work [49] also have obtained very small values of Richardson's constants for sputtered Ni and Pt (1.39×10^{-3} and 3.85×10^{-3} Acm^{-2}K^{-2}, respectively). The smaller experimentally determined values of Richardson's constants are explained by them so that either the effective active area is in fact smaller than the device area, or the effects of quantum-mechanical reflection of electrons from the barrier and tunnelling of electrons through the barrier must be included in the calculation for A^{**}. Such explanation does not seem to be persuasive. If electron scattering on phonons or quantum-mechanical reflection come into effect the effective Richardson's constant (A^{**}) can be only two times lower than theoretic A^*. Thus, the effective active area becomes the only and cardinal reason for constant A^{**} lowering.

But that means that dimensions of active area must be of somewhat interatomic space and even smaller if the device area is of 30–240 μm diameter. Such situation seems to be unbelievable.

As for DW Al contacts, the discrepancy between the experimental Richardson's constant and theoretical value is much more serious and the experimental constant is lower than theoretical value for nine orders of magnitude. The effective mass for DW contact turns out to be billion (10^9) times less than the electron rest mass. In other words, from classic theory point such values of parameters are ***incredible*** and ***absurd.***

If in the law of free electron dispersion

$$E(\vec{k}) = \frac{\hbar^2 \vec{k}^2}{2m}, \tag{2.11}$$

experimental effective mass is substituted for electron rest mass the dispersion grows nine orders of magnitude. Such a dramatic rise of dispersion is the evidence of distortion in lattice periodicity. As appears from above it may be supposed that during welding process because of micro plastic deformation an amorphous layer appears in subcontact layer of SiC. The supposed amorphous layer may be of 10 – 500 nm thick. The lower value of the thickness is determined by electron wavelength. The higher level is limited by the possibilities of heterodiffusion in conditions of thermal-deformation cycle of diffusion welding. The amorphous layer brings the distortions into the physical model of Schottky diode and causes the discrepancy between theoretical and experimental results.

The supposed intermediate amorphous layer between metal and semiconductor may be the reason of two effects inherent in DW Schottky contacts.

1. The potential drop on intermediate layer causes the barrier lowering at zero bias and, therefore, the real barrier height becomes lower than in ideal diode.

2. The electrons can tunnel through the barrier formed by intermediate layer. This fact results in the appearance of tunnel current in addition to the thermionic current at given bias, and changes the form of *I-V* characteristic. Besides that the tunneling makes its own contribution to A^{**} lowering.

Chapter 3. Electron microscopy study of subcontact layers in SiC after diffusion welding

Logical continuation of the work is the direct investigation of the subcontact surface layers in silicon carbide after diffusion welding. The most suitable method for this is the study by transmission electron microscopy (TEM).

TEM is a universal classical method to study the structural defects of crystals and is directly used for the analysis of morphological features of the crystal lattice. To work on a transmission electron microscope requires specially prepared thin specimens that are transparent to electrons. The most common electron microscopes have an accelerating voltage from 100 to 400 kV. Naturally, the samples must have appropriate thickness depending on the accelerating voltage of the microscope. The studies of crystals defects are carried out on the foils - thin films, which is produced from bulk samples of the crystal. Naturally thinning of the sample is necessary to conduct such a way that does not bring in additional distortions in studied area. In the study of thin crystal films in the defect regions should be observed change in intensity of contrast because of the distortions in crystal lattice or there is an elastic stress field around dislocations, or implementation defects.

For experimental studies has been chosen the same material that was used for the analysis of the current-voltage characteristics presented in the chapter 2: 4H-SiC $n^0 – n^-$ structure, 350 μm of thickness with 5 μm epilayer and (0001) Si orientation. After the proper chemical treatment the aluminum foil of 30 μm thick was welded to the episurface of the sample in vacuum not worse than 10^{-4} torr at 600 ºC under the pressure of 30 MPa. The schematic picture of the sample after diffusion welding that was prepared for the TEM investigations, is shown in Fig. 13.

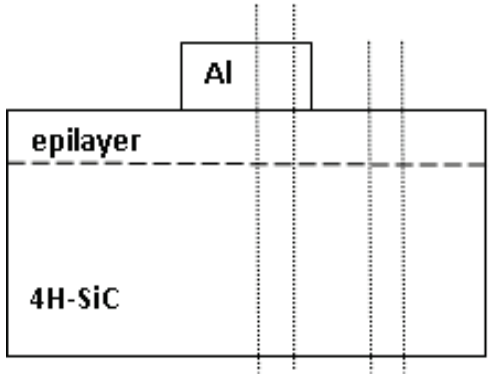


Fig.13. The scheme of the sample cross-sectioning after diffusion welding

After the diffusion welding from SiC plate were cut out two samples of 3x3 mm^2. One sample was cut out from the area, to which aluminum foil was

welded. Another chip was cut out from peripheral area, which was not under thermo-deformations impact during DW process.

The interface was examined in cross-section of the chips. The specimen preparation before TEM analysis has been made in conventional standard way by two steps. First step was mechanical pre-thinning to near electron transparency by dimple grinding and subsequent polishing by use of dimple grinder (model 656) of Gatan, Inc. tools line. The finish thinning was performed in DuoMill 600 – ion beam etching apparatus of Gatan, Inc. Schematic view of the samples prepared for TEM study is shown in Fig. 14.

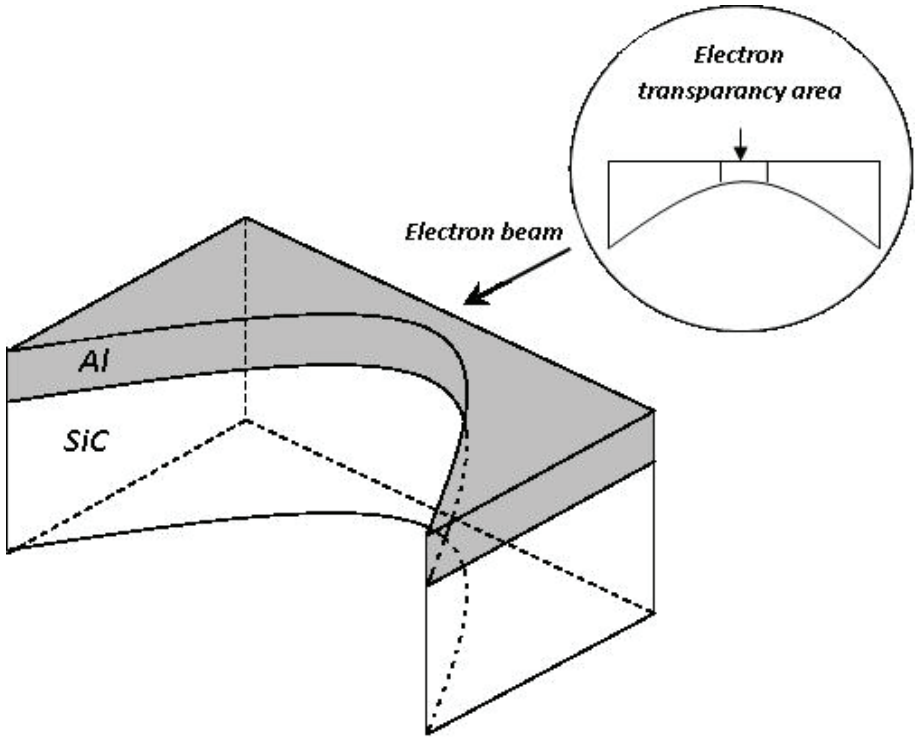
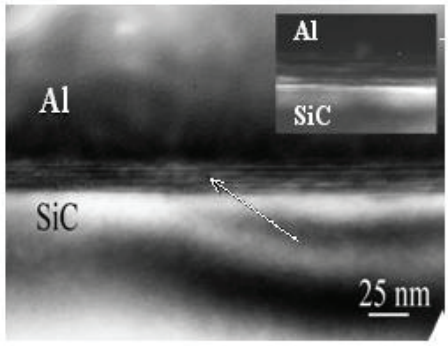


Fig.14. Schematic view of the samples for TEM study

The TEM interface examination was made in JRM (JEOL) 2100F microscope at an accelerating voltage of 200 kV.



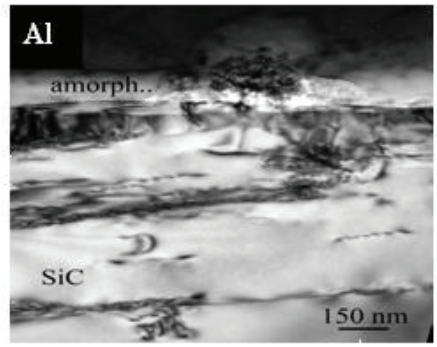


Fig.15. TEM image of boundary contact zone

Fig.16. Contrast TEM image of boundary zone in diffracted SiC rays

In Fig.15 is shown the TEM image of interface boundary between aluminum and silicon carbide. The thickness of interface layer is ~ 25 nm and the layer (marked by arrow) is of strip character. The strip subcontact surface zone is the evidence that during diffusion welding in subcontact surface layer perpendicularly to C-axis of SiC the shear micro deformations have been taking place and due to this process the plane inclusions of small-grained phase have been appeared. In right upper corner of the picture, the image of the same contact area obtained in diffracted SiC rays (dark field) is shown. Apparently, the stripy zone belongs to silicon carbide because the aluminium (black zone) fell out of contrast.

The residual disturbances of crystalline structure in bulk SiC zone have local character (Fig.16). They look like separated, mainly horizontal, shear deformation zones in basic planes of silicon carbide and are the sources of dislocations. But the diffraction picture obtained from bulk zone of silicon carbide (plane $(01\bar{1}0)$ looks like monocrystalline (Fig. 17). The position of major spot is determined by the position of the trap.

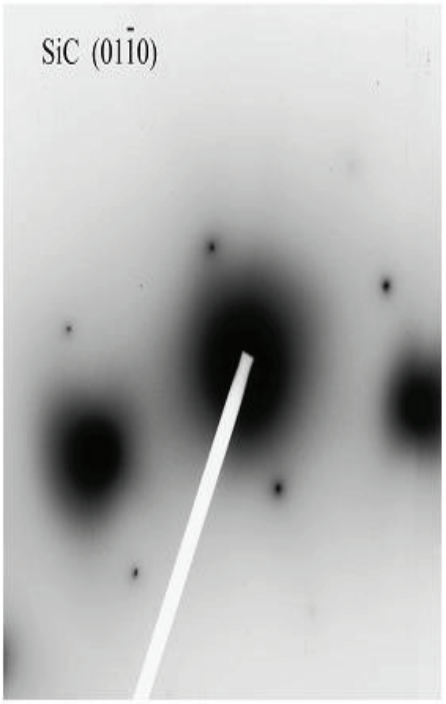


Fig.17 Electron-diffraction pattern of bulk zone of silicon carbide

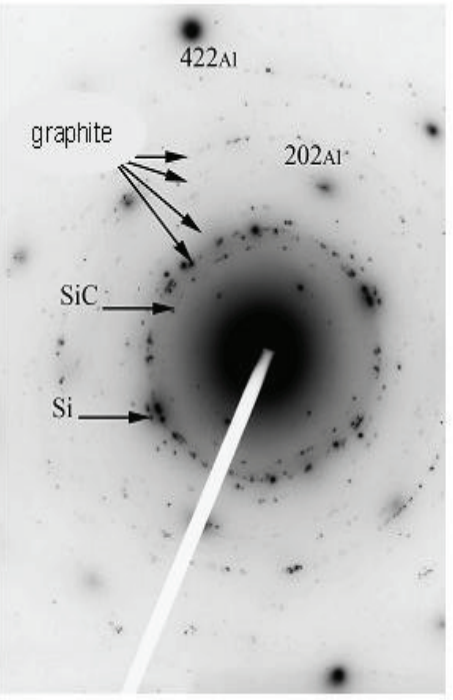
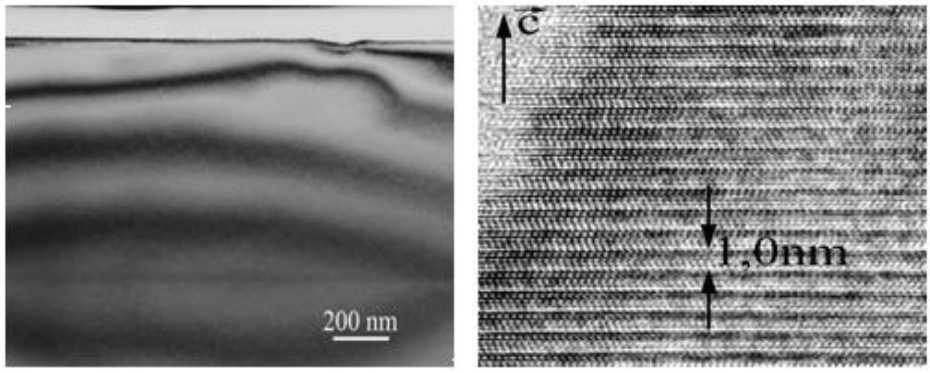


Fig.18 Electron-diffraction picture of subcontact zone in silicon carbide

At the same time on the microdiffraction picture obtained from the subcontact layer (stripy zone), many concentric circles are to be observed (Fig. 18). That makes evidential the fact of existence of small-grained phase. Deciphering of this electron diffraction pattern gives the following range of interplanar atomic distances in Angstroms (Å): 3.35, 2.55, 2.15, 1.94, 1.84 and 1.24. The ring with d=2.55 Å belongs to residue silicon carbide, the ring with d=1.94 Å to silicon. All the rest are in good accordance with interatomic distances for graphite: d (0002) = 3.35 Å, d (10$\bar{1}$0)= 2.13 Å, d (10$\bar{1}$1)= 2.03 Å, d (10$\bar{1}$2)= 1.8 Å and d (11$\bar{2}$0)= 1.23 Å. The point reflexes in diffraction pattern belong to aluminium (plane (111); the experimental values (Å): 1.44, 1.25, and 0.79 are in good confirmation with the table data: d (022) = 1.43 Å, d (113) = 1.22 Å, and d (224) = 0.8 Å.

To evaluate the initial crystal situation and the contribution of specimen preparation treatment in crystal surface distortions the part of 4H-SiC structure free of DW contacts (see Fig. 19) was examined in the same way as the specimens with Al DW contacts.



a) b)

Fig.19. The cross-section image of the SiC surface layer before diffusion welding in diffraction (a) and phase (b) contrast

As it is seen from Fig. 19, the TEM image shows the perfect crystalline structure of 4H-SiC polytype. The concentration threshold, from which the structural defects become visible, is equal to 10^6 cm^{-3}. So, it can be concluded that the surface layers of initial SiC structure are practically free of defects. That is confirmed by diffraction contrast image (Fig. 19,a), where only the extinction contours are visible. The phase contrast vision of the same region of the specimen (Fig. 19,b) demonstrates the ideal interchange of atomic planes.

Thus, the main goal in these studies has been achieved. TEM investigations have shown significant distortions of the crystal structure in the surface contact layer of silicon carbide after diffusion welding.

At the same time, the initial surface of SiC before diffusion welding had the crystal structure near ideal and free of characteristic defects. We consider this fact as the evidence that during DW at elevated temperature and under tangential forces the shear microdeformations have been taking place in subcontact surface of SiC that, in turns, led to the destruction of the crystal lattice and the formation of quasi-amorphous layer. This basic message may be the evidence that strong disparity between the experimental electrical parameters of DW contacts and parameters predicted by ideal Schottky-Mott model may be attributed to the specific of the interface between the metal and silicon carbide. The direct contribution of thermal-deformation during DW and the process control may be the subject of our future detail studies.

Note. *All electron microscopic studies were carried out at the Center for collective use in Ioffe Institute of RAS.*

Chapter 4. Investigation of additional states in the semiconductor surface after diffusion welding

Thus, as it was established in the chapter 3, in the surface layer of the semiconductor during diffusion welding with the metal the defect surface layer of ~ 25 nm thickness is formed. The formation of numerous crystalline defects in subcontact layer leads to the distortion of the electronic spectrum of the crystal. This means that, in the band gap of the defect zone appear numerous additional states, so-called deep centers. The presence of deep centers can give the semiconductors both useful and undesirable properties. Therefore, the investigation of deep levels is a necessary part of modern semiconductor physics. Moreover, this must be done because the fact of the defect zone was observed experimentally by TEM investigations.

4.1. Method of relaxation spectroscopy of deep levels

The most spread method of determining the parameters of deep levels is currently the method of relaxation spectroscopy of deep levels - Deep Level Transient Spectroscopy (DLTS). The advantages of this method are the high sensitivity, the ability to determine the parameters of deep levels by changing their occupation, both by majority and by minority carriers, the ability to study deep levels in semiconductor devices, as well as in the original semiconductor.

DLTS was first introduced by D.V. Lang [50] in 1974 and has evolved into a routine characterization technique for semiconductor materials and devices. The DLTS method is based on the concept of relaxation of capacitance in the structure with a potential barrier, e.g. Schottky barrier or an asymmetric *p-n* junction. The relaxation of capacity is due to a change in the charge state of the traps in semiconductor space charge region under the applied bias voltage. As a result, the occupancy of electron traps becomes different from the equilibrium value. In the process of returning the occupied traps to the equilibrium value of capacitance is also returned to its equilibrium value.

In order to describe this section of the study more clear, it is appropriate to give a schematic interpretation of the method.

4.2. The principle of the DLTS measurement

The detector in the DLTS measurement is actually the space-charge region (SCR).

As an example, we take n-type metal-semiconductor junction, in which there are two levels, the shallow donor level and a deep level (electron trap). At reverse biased condition, there is a relatively wide SCR in the semiconductor near the surface (Fig. 20). The width of this region is determined by the charge on the metal contact as well as the shallow level concentration because the whole system should be neutral. It means that the negative charge on the metal is

completely compensated by the positive charge of the localized donor ions in the SCR. Supposing that the concentration distribution of the donor level is homogenous:

$$w = \sqrt{\frac{2\varepsilon}{qN_D}}\sqrt{V_R + V_B} \ , \tag{4.1}$$

where V_R is the reverse bias and V_B is the built-in potential of junction (barrier).

At the beginning the junction is reverse biased (Fig. 20, a), so deep level below the Fermi level ($x>L_R$) is completely filled and it is practically empty above the Fermi level ($x<L_R$). Then, a positive pulse reduces the reverse bias, which results in a decreased SCR width (Fig. 20, b). This excitation pulse is the so called *filling pulse* because during it the part of the deep level which got below the Fermi level ($L_1<x<L_R$) is filled by electrons from the conductive band (capture process). After the filling pulse the applied reverse bias is the same as the one before the pulse but the width of the SCR is larger because of the filled trap (Fig. 20,c). The negative charge of the captured electrons is compensated by the positive charge of the localized donor ions in the $L(t)$-L_R region of the SCR. While the deep level is emitting the electrons to the conductive band ($L_1<x<L(t)$), the width of the SCR is going back to its original value (emission process).

The deep level transient can be monitored as a capacitance transient. Since the capacitance of the Schottky diode is proportional to the reciprocal value of the SCR width,

$$C(t) = \frac{\varepsilon A}{w(t)} \ , \tag{4.2}$$

the transient of the width can be measured as capacitance transient.

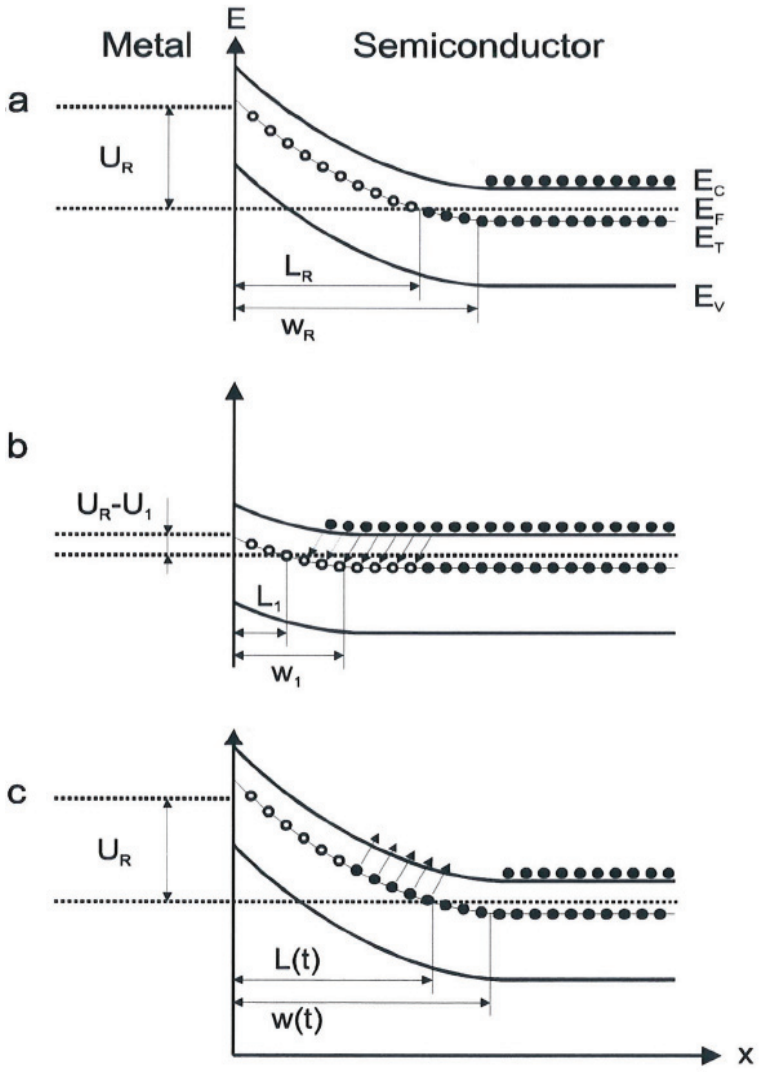


Fig. 20. Energy band diagrams of the metal-semiconductor junctions
Before the filling impulse (a), during the filling impulse (b),
just after the filling impulse (c) (U_r=V_r) [50]

4.3. Preparation of experimental samples

For studying the deep levels in diode structures before and after the diffusion welding Schottky diode chips of Cree Research Inc. were used. For the manufacture was used epitaxial 4H-SiC structure of thickness 0.35 mm, net nitrogen doping density in epi-layer $N_d \sim 1x10^{15}$ cm^{-3} and epi-layer thickness of 6 μm. Overall size of the chips – 1.4x1.4 mm^2, contact diode area was 1x1 mm^2.

The sputtered aluminium was used as a contact metal, and peripheral protection – silica (SiO_2).

The capacitance–voltage *(C–V)* characteristics and DLTS spectra measurements were performed with a computer-controlled deep-level spectrometer DLS-83D (Semilab, Semiconductor Physics laboratory, Inc., Hungary)

Initially, all the necessary measurements were made on the original chip, and then evaporated aluminum was removed by etching and to the contact surface was welded aluminum foil of 30 μm thickness (the welding modes are described in Chapter 2). Then the same measurements were repeated on a chip with a diffusion-welded contact.

4.4. Capacitance-voltage characteristics

Below are shown the capacitance-voltage characteristics in the images C-V_r and $1/C^2$-V_r for diode structures before and after the diffusion welding (Fig. 21, 22).

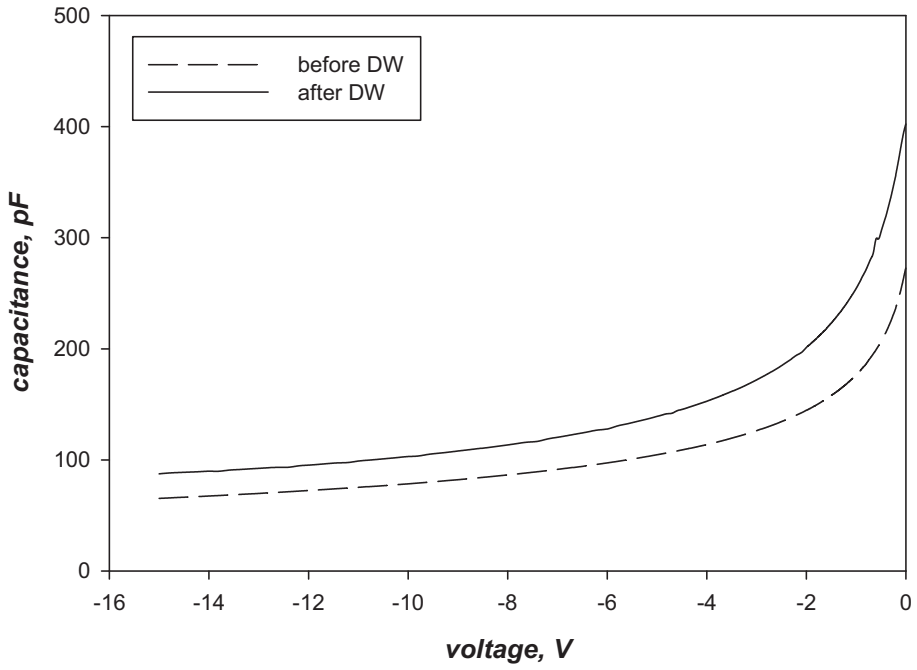


Fig. 21.Capacitance-voltage characteristic for a Schottky diode before and after DW

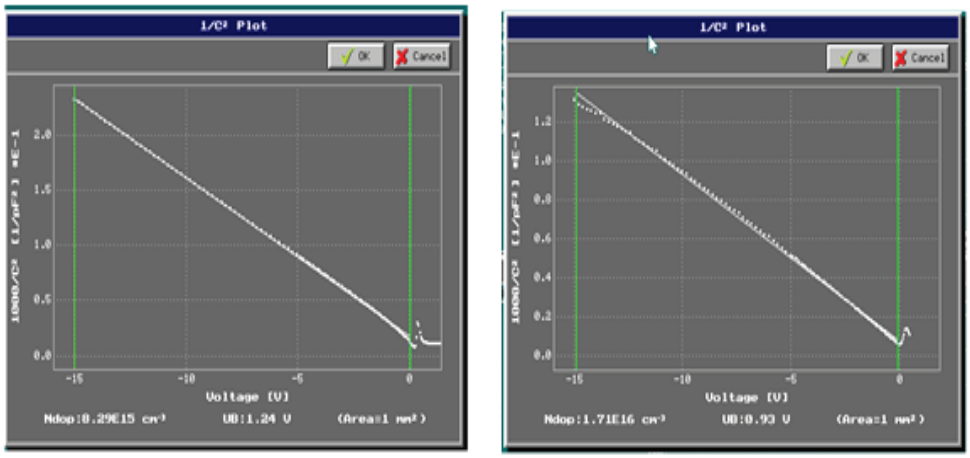


Fig. 22.The dependence of C^{-2} on V_r for a Schottky diode before (left) and after (right) DW

As seen in Fig. 21 the diode after DW has some increased level of barrier capacity compared with the initial Schottky diode before DW. At the same time, the built-in voltage obtained by extrapolated intersection of $1/C^2$ line and voltage axis for DW diode is less than for the sputter contact (compare 0.93 V and 1.24 V, respectively). Based on the following set of formulas can be clearly seen that the increase of the barrier capacitance is associated with a decrease of built-in voltage.

For the semiconductor width homogenous doping profile the differential capacitance $C=dQ/dV$ can be interpreted as:

$$C = \frac{C_0}{\sqrt{V_B - V_R}} \quad , \tag{4.3}$$

where $C_0 = A\sqrt{\frac{\varepsilon q N_D}{2}}$, $\varepsilon=\varepsilon_0\varepsilon_{rel}$.

Under zero reverse bias ($V_R=0$), the capacitance depends on doping density (N_D) and built-in voltage, which, in turns (excluding the effect of image force), can be represented as:

$$V_B = \Phi_b - \left(E_C - E_{F_n}\right) - \frac{kT}{q} \quad . \tag{4.4}$$

Thus, theoretically, for the diode with one and the same initial epitaxial structure (hence, at one and the same doping density N_D) the value of built-in voltage depends only on the barrier height. So, increase of the barrier capacitance in the diffusion-welded contact is due to the decrease in the height of the barrier and may serve as indirect confirmation of the existence of the intermediate layer (reduction of the barrier height is one of the effects of an intermediate layer between metal and semiconductor (see chapter 3).

4.5. Comparison of deep level situation by transient spectroscopy

It is well known that the distortions of the crystal lattice are accompanied by the formation of various defects, which, in turn, may result the deep levels in the bandgap of semiconductor if it is an electrically active defect. Based on previous TEM studies the distortions in subcontact zone of the crystal structure that occurred during the process of diffusion welding can be considered as reliably established fact. Therefore, it would be logical to expect changes in the spectrum of deep levels before and after diffusion bonding. For this purpose, on the samples described in the paragraph 4.3 were measured DLTS spectra, or in other words DLTS signal as a function of temperature (so called temperature scan) and as a function of frequency (so called frequency scan). The appearance of temperature and frequency scans before and after the diffusion welding in form of the specific relation $\Delta C/C$ is shown in Fig. 23 and Fig. 24.

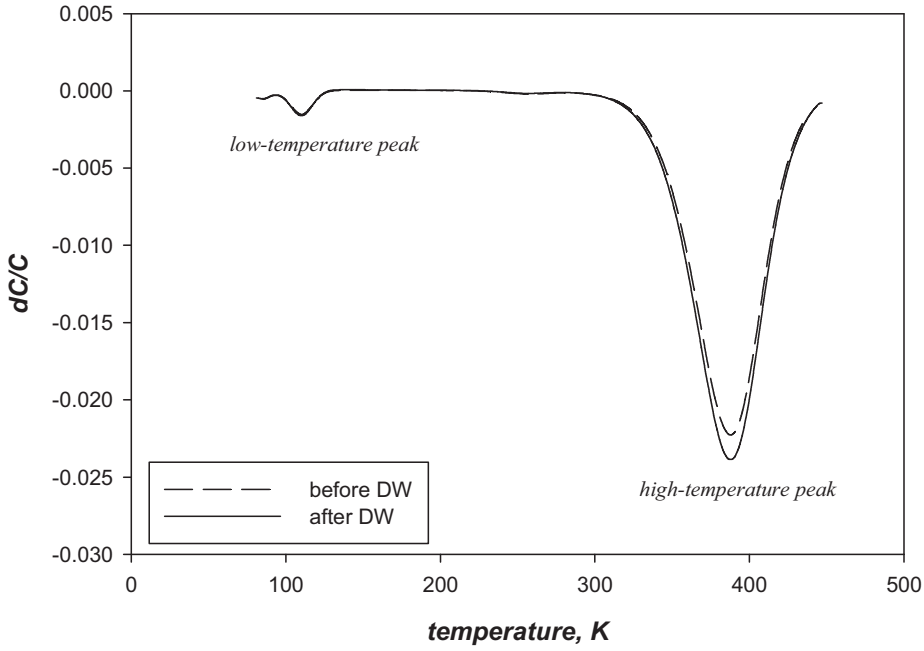


Fig. 23. Temperature scans for Schottky diode before and after DW (f=2000Hz)

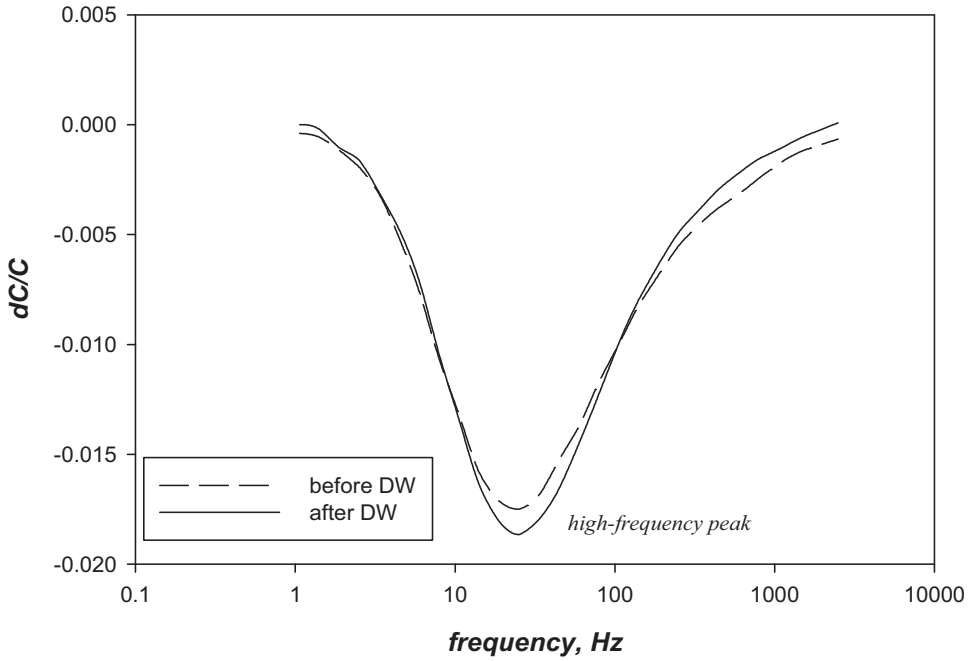
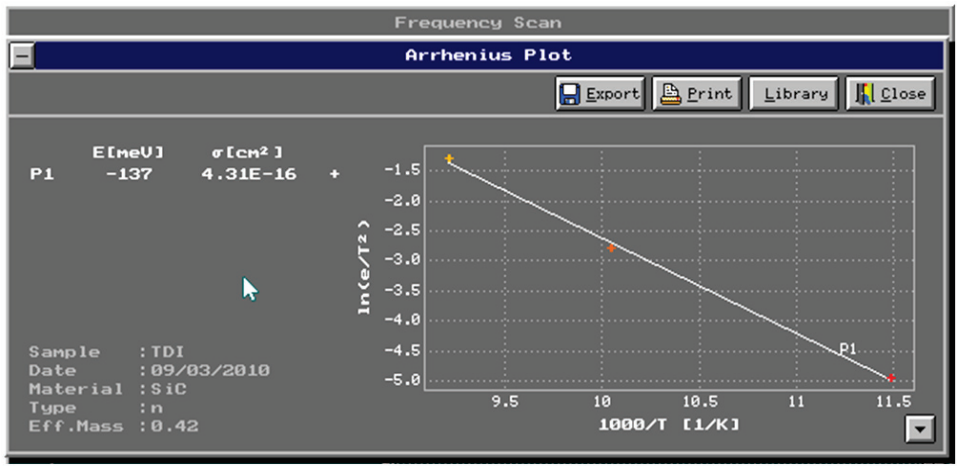


Fig. 24. Frequency scans for Schottky diode before and after DW (T=320K)

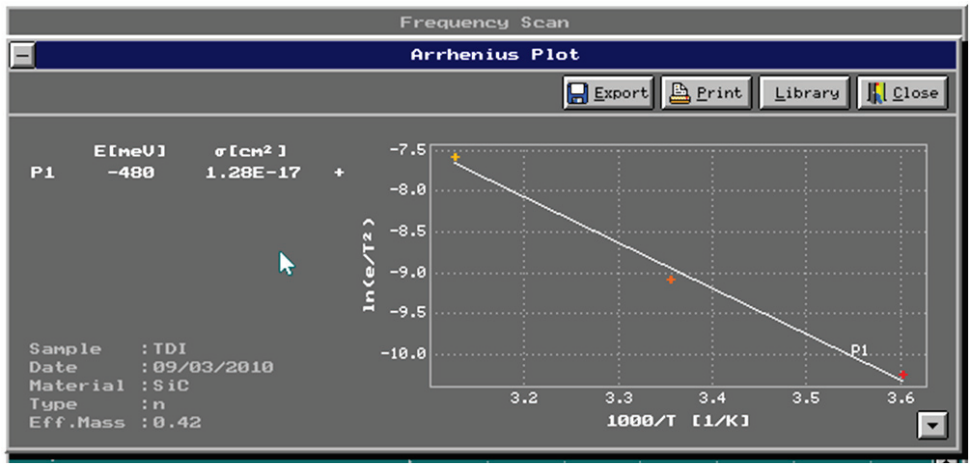
First of all, it should be noted that after the thermal deformation during diffusion welding the pattern of DLTS spectra is not changed. The negative amplitude of transient capacitance indicates that this are a majority carrier (*id est* electron) traps. The spectra shows that the positions of negative peaks before and after diffusion welding coincide both in temperature and frequency in the corresponding temperature and frequency scans. Somewhat lower value of $\Delta C/C$ for scans after diffusion welding is associated with an increase in capacity due to lowering of built-in voltage, as was shown above. The deep levels can be described by their activation energy and the capture cross section. These parameters can be calculated from the *Arrhenius Plot*. After performing and evaluating several measurements with different frequencies (for T-scans) and at different temperatures (for F-scans) there are frequency-temperature data pairs belonging to each peak. The obtained f-T i.e. (e_n-T) data pairs can be illustrated according to the following equation, which is the logarithmic form of the expression of the emission rate. The left side is on the Y axis, $1/T$ is on the X axis (K is a constant).

$$\ln\left(\frac{e_n}{T^2}\right) = \ln(K\sigma_n) - \frac{E_a}{kT} \tag{4.5}$$

where $K = 2k^2m^*\left(\frac{2\pi}{h^2}\right)^{3/2}(3)^{1/2}$ and E_a-activation energy, σ_n-capture cross section, e_n- electron thermal emission rate from deep state.
Below in Fig. 25 and Fig. 26 are shown the *Arrhenius Plots* for temperature and frequency scans for the Schottky diode before diffusion welding (since the positions of peaks before and after diffusion welding are completely coincide, I show the performance of *Arrhenius Plots* only for one of the two cases).

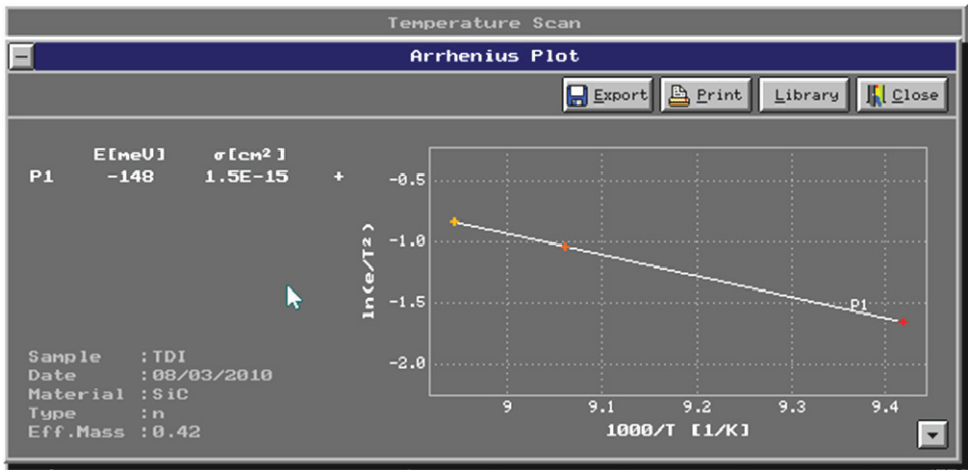


a)

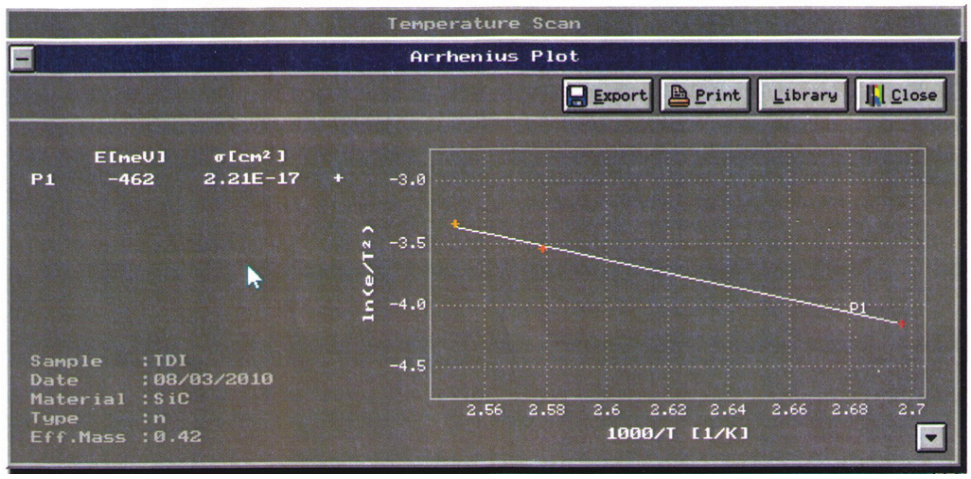


b)

Fig. 25. *Arrhenius plot* of frequency scans for (a) low-frequency and (b) high-frequency peaks



a)



b)

Fig.26. *Arrhenius plot* of temperature scans for (a) low-temperature and (b) high-temperature peaks

The points obtained on *Arrhenius plot* field are fitted by straight line (least square method). The slope of the line determines the activation energy. The intersection of the plot and *Y* axis gives the capture cross section.

The obtained activation energies for low-temperature peak is (E_a= – 0.148 eV, *T*-scan) and (E_a= – 0.137 eV, *F*-scan) and for high-temperature peak the activation energies are, respectively, (E_a= – 0.46 eV) and (E_a= – 0.48 eV). Based on the literature data the deep levels with the corresponding activation energies

are most likely the *S* centers. The first is a defect of S_0 type, which can be associated with defects such as nitrogen impurities substituting at lattice sites [51-54]. Another, deeper *S* center can be related to the higher concentration of oxygen-related defects near the surface [55] in different configurations and complexes [56]. Both the first and another type of defects are characteristic of the epitaxial layer and, therefore, they are not brought in by the diffusion welding. The absence of newly formed deep centers after diffusion welding seems to be the disagreement with the fact of the existence of the damaged layer observed in TEM studies. But in reality it is not so. If we turn to the scheme shown in Fig. 20, we see that after applying the filling pulse, there is a zone L_1, adjacent to the contact, in which deep levels always remain above the quasi-Fermi level. These levels save ionized state and do not participate in the recharge process during DLTS measurements. Residual disturbances of crystalline structure after DW propagate into the bulk SiC for a depth of 25 nm (compare the width of SCR calculated by the Eq. 4.1 and having value of 1 μm at zero bias). Of course, it would be wrong to expect the appearance of exponential relaxation of capacitance in such a narrow zone using the DLTS method. In addition, it should be noted that since for the detection of deep levels is used a Schottky barrier, it is impossible to observe the traps of minority carriers (i.e. donor center) because direct current do not inject the minority carries. Moreover, the use of special measurement modes, such as higher temperatures or/and a combination of DLTS and photocapacitance cannot in principle identify the deep levels in semiconductor surface under DW contact. Keep in mind that diffusion welding process was accompanied by numerous microplastic shifts of the crystal lattice in this narrow surface area. As a result, the considered region is overcrowded by every possible defect (point defects - vacancies, interstitial atoms, linear - dislocations, volume - clusters). It is well known that the lattice defects entail the appearance of additional electronic states in the band gap. On the physical nature, these states can be divided into four main types.

- Tamm states
- Shockley states
- Crystalline defect states
- Impurity states

Tamm states are caused by breakage of the crystal lattice periodicity. Shockley states are, thus, states that arise due to the change in the electron potential associated solely with the crystal termination. There is no real physical distinction between the two terms, only the mathematical approach in describing surface states is different. The nature of defect and impurity states in the crystal lattice is similar to the local levels.

For more visual understanding, are given the diagrams of the electronic states near the metallurgical metal - semiconductor boundary by Tamm and Bardeen (Fig. 4) and Shockley (Fig. 27).

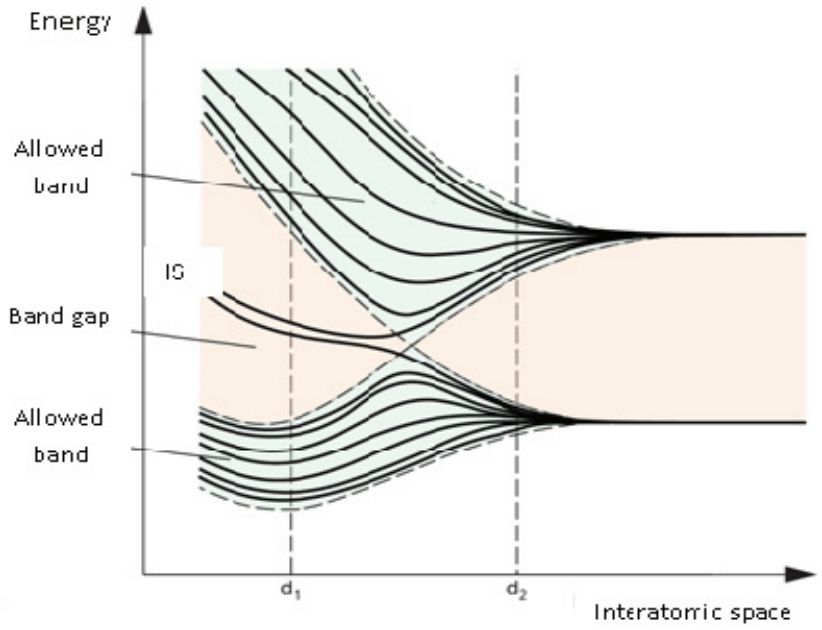


Fig. 27. Splitting of energy levels in interfacial zone (IS denotes interface states) [57]

As seen from the diagram in Fig. 4 in the presence of numerous states the Fermi level will be "pinned" at a certain level (so-called neutral Φ_0 level) above the top of valence band.

Under the Shockley scheme (Fig. 27) from two allowed bands is split off one bulk state, and that leads to additional states in the bandgap. Thus, the destruction of the band structure in the interfacial layer of semiconductor makes it impossible to use the Lang method for fixing the deeper levels. Hence, it is necessary to use other approaches to identify the contribution of diffusion welding in the electronic states of the subcontact area of semiconductor. One should try to approach to contact area not from the bulk of semiconductor but from the surface. One of such methods in available is *vibrating capacitor method.*

Resume

The real situation makes it impossible to use as the primary any of the existing physical metal-semiconductor models. At the same time, following each model separately, we should expect multiple deviations from the ideal: the displacement of the barrier from the interface into bulk semiconductor, the barrier lowering, the appearance of local regions with metallic conductivity, the appearance of the intermediate zones with modified crystal structure and, consequently, the splitting of the barrier.

Regarding to the current flow through the barrier, none of the mechanisms cannot be preferred (at least until the electric field becomes sufficient for the dominant thermionic emission over the barrier). And at the same time each mechanism may be partially implemented, thus, creating the effect of additional current to the initial part of the forward I-V characteristics.
It's interesting that the similar summary expresses S.M. Sze in its latest edition [46].
Quote: "An exact calculation of Schottky-barrier height requires detailed information on the distribution of the interface states and on other properties of the interfacial layer. Since such information is not usually available, the Schottky-barrier height is normally determined from experimental current-voltage and capacitance-voltage characteristics".

Chapter 5. Vibrating capacitor (VC) and surface photo voltage (SPV) method

5.1. The basic principle of vibrating capacitor measurements

The vibrating capacitor (in other words, the *Kelvin Probe*) is quite an old method and thanks to this is well-developed and adapted for the surface investigations. The basis of this method was firstly postulated by the renowned Scottish scientist Lord Kelvin, in 1861. Modern implementation of this method is illustrated in Fig. 28.

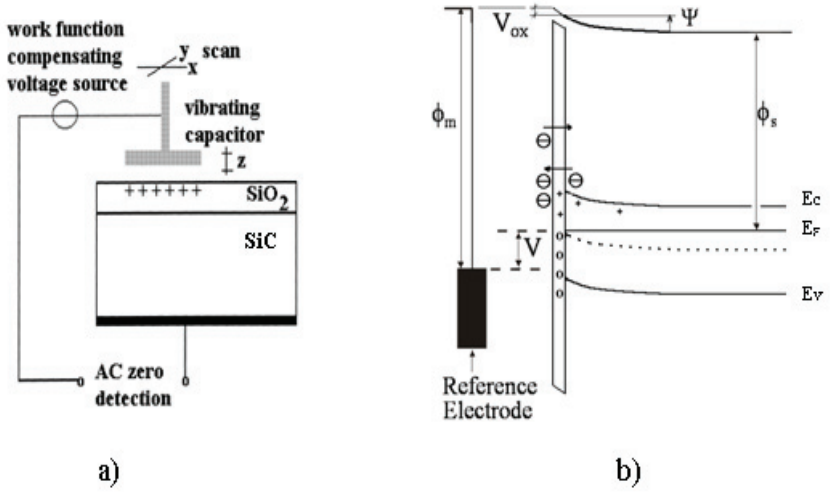


Fig. 28. The principle of vibrating capacitor method (a) and band diagram of semiconductor surface (b)

The method is based on the compensation of the electric field between a vibrating (reference) electrode and the surface to be investigated (Fig. 28).

The vibration of electrode (cantilever) is excited mechanically. Simultaneously to the electrode the compensating potential V is applied. Thus, the surface of the semiconductor and the electrode form a capacitor, and the effect of movement of the conductor in electric field is realized. As the electrode is vibrating, the exited alternating electric charge is pushed around the external detection circuit. The feedback system changes the compensating potential until the alternating current induced by vibrating electrode is near zero. Then the compensating voltage becomes equal to the total surface potential. Assuming zero electric field above the surface, the surface potential depends on the surface charge (Q) according to

$$V = \frac{Qd_{ox}}{\varepsilon_{ox}} + \Psi(Q + Q_{ss}) + \Phi_{ms} \,, \tag{5.1}$$

i.e. the total potential V is the sum of the voltage drop in the oxide, ($V_{ox} = Qd_{ox}/\varepsilon_{ox}$), the voltage drop in the semiconductor (Ψ, surface potential barrier), and the work function difference between the reference electrode and the semiconductor (Φ_{ms}) (Fig.28). In Eq. (5.1) d_{ox} is the oxide thickness, $\varepsilon_{ox} = \varepsilon\varepsilon_0$ is the oxide permittivity.

Combining the Kelvin probe and Einstein Photoelectric effect the next step of measurement can be realized (Fig.29).

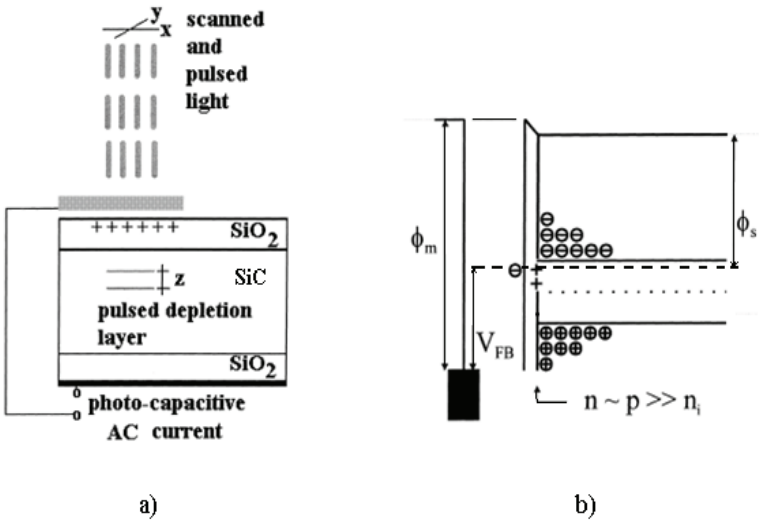


Fig. 29. The physical arrangement for the surface potential measurement by coupling VC and SPV methods (a) and band diagram in presence of high intensity light excitation (b)

In the presence of high intensity light excitation, due to high carrier concentrations the band bending disappears (also disappears the second term in Eq. 5.1). The oxide surface potential V_{FB} can be measured by the photo-capacitive current generated by light pulses:

$$V_{FB} = V_{ox} + \Phi_{ms} = \frac{Qd_{ox}}{\varepsilon_{ox}} + \Phi_{ms} \ . \tag{5.2}$$

Thus, the vibrating capacitor measurement in dark combined with light excitation measurement, gives a surface potential barrier as:

$$\Psi = V - V_{FB} \,, \tag{5.3}$$

where the surface potential barrier is the difference between the dark and light values of the measured oxide surface potential. The (static) surface charge, Q, is assumed to be constant during illumination. This assumption is reasonable,

as the oxide surface is isolated from the environment. (The basic principles of the VC and SPV method as applied to semiconductors are presented in [58-59]).

5.2. Material, sample preparation and experimental results

For test measurements were used the chips of 5x5 mm^2. Chips were cut out from n^0 – n^- 4H-SiC epi-structure of thickness 0.35 mm, epi-layer thickness 5μm. Net nitrogen doping density in epi-layer $N_d \sim 1x10^{15}$ cm^{-3}.
First, the sample epi-surface was tested in the initial state, just after cutting. Then to the epi-surface of the same sample was welded the aluminium foil of 30 μm thickness at 640 ºC temperature under 30 MPa pressure. After welding, the aluminum foil was removed from the surface by etching in hot dilute hydrochloric acid. Then on the same sample was repeated the surface potential measurement "in darkness" and under illumination.

The surface potential barrier measurements were performed using the Kelvin probe Trek model 320 c type equipped with a 4mm x 4mm reference electrode made of glass, covered by transparent and conductive tin-oxide thin film. A standard 36 W microscope bulb was used to excite the surface by focused light. The light power intensity is estimated 1-2 W/cm^2, which is usually enough for the saturated SPV test, i. e. the measured surface photovoltage does not depend strongly on the light intensity.

The measured surface potential barrier was ~600 mV (+/- 30 mV) before diffusion welding and ~750 mV (+/- 30 mV) after the diffusion welding, respectively. The direction of the potential shift showed upward bending bands, which proves the depletion condition for n-type semiconductors.

5.3. Analytical proceeding of the results

Before analytical proceeding of the results, it should be emphasized that the measurements were performed on one and the same sample in one and the same conditions. That means that in the first and the second measurements the semiconductor surface was covered by an ultra-thin native oxide with the thickness of about 2 - 3 nm, because the conditions for oxide formation were the same. So the first term of Eq. 5.1 for both cases of measurement should have the same value close to zero because of the very small thickness of the oxide and, hence, it can be neglected. It is clear that the third term of Eq. 5.1 (reference electrode-semiconductor contact potential) also remains the same in both cases the measurements. Thus, the difference between the values of the surface potentials resulting from the two measurements is determined only by the second term, namely by $\Psi (Q + Q_{ss})$.

The second term of Eq. 5.1 is the surface potential barrier (Ψ). It is known in implicit form, using $F(\Psi;\Phi_{bb})$ as the solution of the Poisson equation:

$$Q + Q_{SS} = 2qn_iL_D\mathrm{sgn}(\Psi)F(\Psi;\Phi_{bb})\,. \qquad (5.4)$$

Eq. 5.4 states that the sum of the surface charge (Q) and the interface charge (Q_{ss}) is equal to that of the total semiconductor space charge. In this equation q, n_i, L_D are the electron charge, intrinsic charge carrier concentration, intrinsic Debye length, Φ_{bb} is the distance between the middle of the bandgap and Fermi level.

$$F(\Psi;\Phi_{bb}) = \mathrm{sgn}(\Psi)\sqrt{2}\sqrt{\mathrm{ch}\frac{\Phi_{bb}-\Psi}{U_T} - \mathrm{ch}\frac{\Phi_{bb}}{U_T} + \frac{\Psi}{U_T}\mathrm{sh}\frac{\Phi_{bb}}{U_T}}, \qquad (5.5)$$

where U_T is the thermal voltage. The Eq. 5.4 has a high importance, because the surface potential barrier (Ψ) can directly be calculated as the difference between the equilibrium and non-equilibrium (photo-saturated) value of the surface voltage measured by the vibrating capacitor method (Eq. 5.3). Thus, knowing Ψ, the total surface and interface charge can be calculated from the Eqs. (5.4-5.5). Initial data and calculated values obtained from Eqs. 5.4 and 5.5 are given in Table 2.

Table 2. The results of the calculation of surface charges

DATA			
Initial	*Eg,* eV *(bandgap)*	3.23	
	T, K *(temperature)*	300	
	n_i, cm^{-3} *(intrinsic carrier concentration)*	10^{-7}	
	L_D, cm *(intrinsic Debye length)*	$9.3x10^4$	
Calculated		**Before DW**	**After DW**
	Ψ, mV *(surface potential)*	-600	-750
	$F(\Psi;\Phi_{bb})$	$1.1x10^{15}$	$1{,}99x10^{16}$
	$N=Q/q$, cm^{-2} *(number of surface charges density)*	$-2x10^{15}$	$-3.5x10^{16}$

As seen from the results presented in Table 2, after DW was detected an increase in surface potential as well as increase of more than order of the surface charge density. Taking into account the principle of thermodynamic equilibrium, the surface potential must be compensated by the corresponding potential in the surface region of the semiconductor. The increase in surface potential can be either by increase in surface barrier and due to the appearance of additional positively charged states in the surface region of the semiconductor. Based on the experimental conditions, we have no physical reason to explain the increase in surface potential after DW by increasing the surface barrier.

Thus, increase in the surface potential should be due to the positive charge on the additional states arising after diffusion welding because of lattice distortions in the surface layer of the semiconductor. Thus, the real surface that separates the metal and the semiconductor is a thin (nanometers), but still a three-dimensional buffer area. This area contains high number of structural defects, which are the main sources of surface states. Attributed to these states the name of *surface states* is quite arbitrary. And the density of these states in some cases may exceed the possible density of Tamm states ($\sim 10^{15}$ cm^{-2}). Using a more sophisticated methodological scheme of the *VC-SPV* experiment [59] can determine the density of deep traps in the total surface charge, but it is beyond the scope of this work.

Note. *The experimental studies were carried out at the Department of Electron Devices of Budapest Technical University using the method of Professor János Mizsei. The results will be published in a separate paper in the near future (joint publication in the framework of cooperation agreement between the Academies of Sciences of both countries).*

Chapter 6. Solid-state etching of silicon carbide during diffusion welding

In earlier studies on DW applied to SiC [41] it was found that after removal of Al from SiC surface by etching in hydrochloric acid no typical marks of surface interaction could be found. The local pits of solid state etching, typical for diffusion welding of Si, have not been found on the SiC surface. Since the process occurs at a temperature below the melting point of aluminum (below 650 ^{0}C), carbon has extremely low solubility in solid aluminum. Apparently, only the silicon atoms of silicon carbide take part in the process of solid state solving in Al leaving behind unreacted carbon atoms. Such separate solving destroys the crystal surface and is equal to the process of isotropic etching, after which the surface remains smooth and polished. Besides that, it would be expected the precipitation of carbon at interface during cooling after DW.

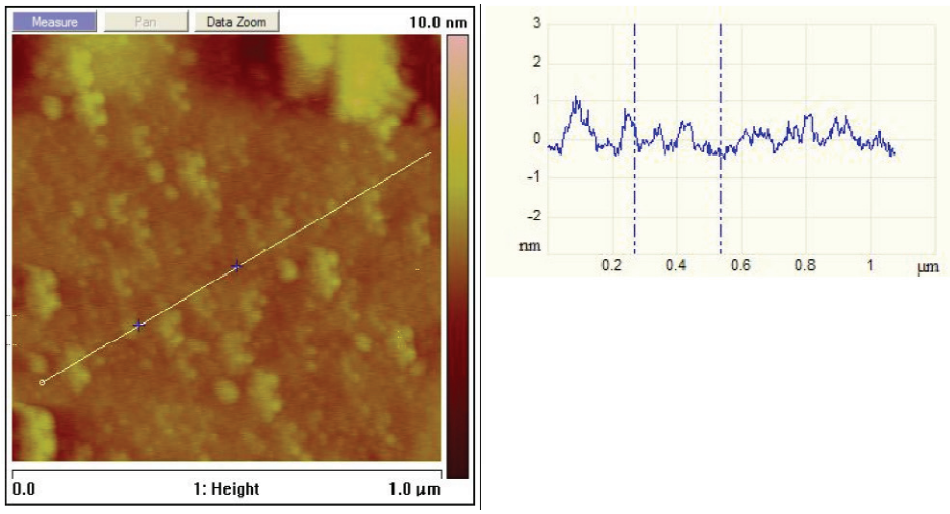
To confirm the stated assumption, below are described the results of two indirect and direct experiments. The results of these investigations should be important in developing predictive models of interfacial structure.

6.1. Investigating of the surface topography by AFM microscopy

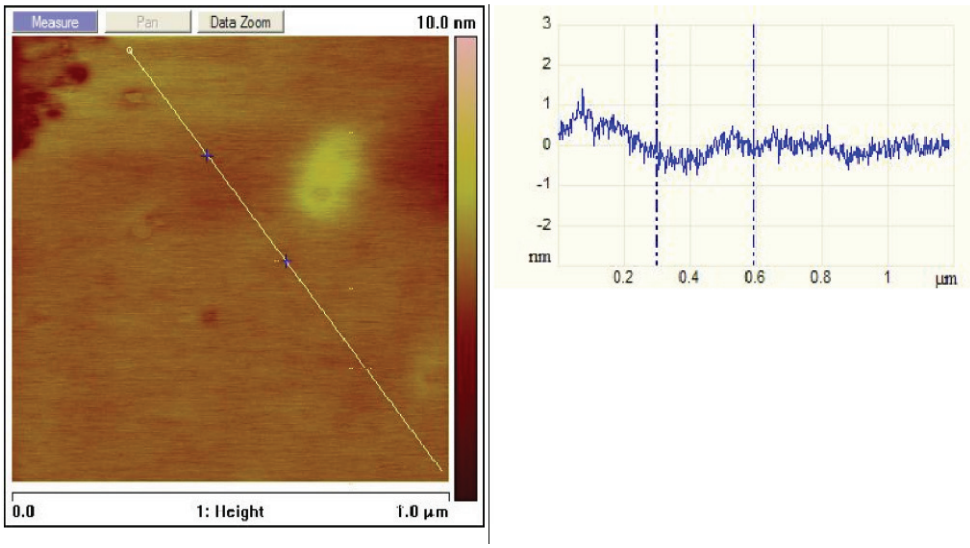
For the experiment was used the chip of 4H-SiC substrate, 350 μm thickness, 5x5 mm^2 area, with polished surfaces, prepared for epitaxy.

The topography of the sample was investigated in the soft tapping mode by Atomic Force Microscope (AFM) Veeco NanoScope IIIa with cantilever MikroMasch NSC15/AlBs.

First, the sample was scanned in initial state and then, the sample was scanned again after diffusion welding and subsequent etching removal of the 30 μm aluminum foil from the surface. All together there were traced about 20 scan lines. The typical pictures of the surface topography before and after DW are shown in Fig. 30.



a)



b)

Fig. 30. AFM images (left) and cross-sectional profiles (right)
before (a) and after diffusion welding (b)

As is evident from Fig .30 the height irregularities in plan and profile changed after the interaction of the silicon carbide with aluminum foil during diffusion welding. The peaks regularity caused by mechanical polishing disappears and the surface becomes smoother. It is the effect that was expected to see, but the change of the surface roughness is only indirect evidence of interaction of Al and SiC. If this is true, then we should expect the precipitation

of unreacted carbon at interface after DW. To detect the precipitated carbon the next step of the experiment was taken.

6.2. The SEM scanning of the surface

For an investigation SEM model ZEISS EVO MA-15 and energy Dispersive X-ray microanalysis (EDS) analyser Oxford Instruments INCA Energy system have been used. The SiC chip of 5x5 mm^2 was welded by 100 μm aluminum foil to the ground tungsten electrode. Then, after etching in hot hydrochloric acid the SiC chip was separated from the tungsten. Thus, on the surface of the tungsten under side lighting can be seen the place, where the chip was welded (see Fig.31).

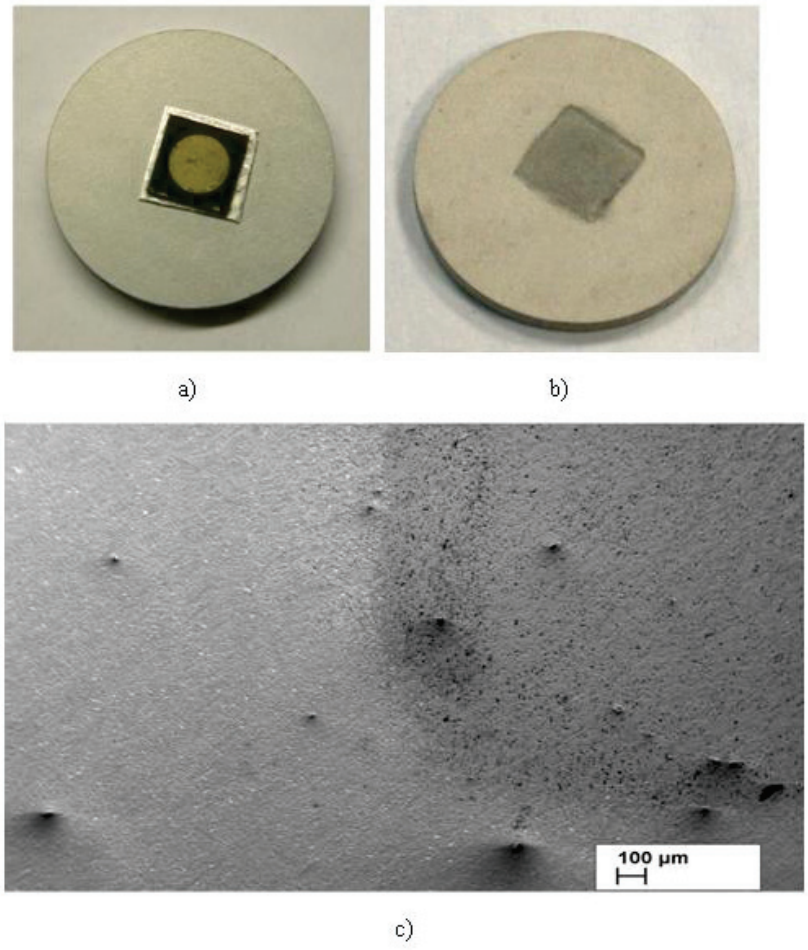


Fig.31 The view of the welded chip (a), tungsten electrode after etching (b) and tungsten electrode surface under the great magnification (c) (secondary electron image)

Spectral analysis has not revealed the presence of carbon on the surface of silicon carbide, as might be expected in view of the polished surface. Spectrum taken from ground surfaces of tungsten is shown in Fig.32.

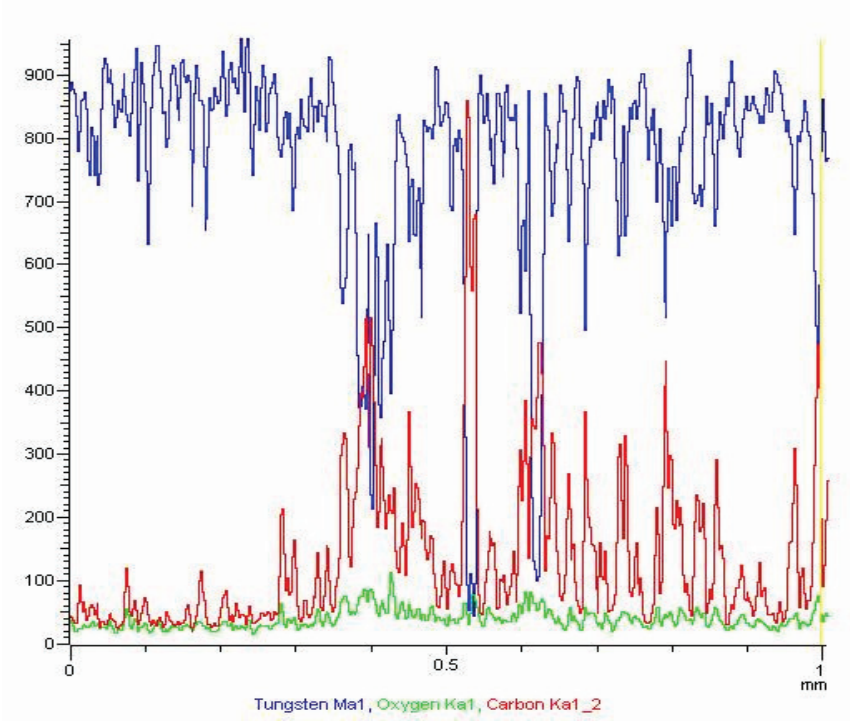


Fig. 32 The spectral distribution of elements on the surface of tungsten in welding area.

As seen from Fig .32 presence of the precipitated carbon in welding place is not in doubt.
Unfortunately, the study was carried out on a single sample and requires statistical testing; however, I found it possible to put the results for discussion in this thesis.

Note. *Topography measurements on AFM were carried out at MicroMasch Company, Tallinn.*
The SEM spectrographs were carried out at the Centre for Materials Research, Tallinn University of Technology.

SUMMARY

Diffusion welding as an alternative method of metallization applied for semiconductor devices has been known for over 30 years. The method has been used mainly for the manufacturing of power silicon devices with various combinations of *p-n* junctions located in relatively deep from the contact surfaces. Obviously, the contacts in such devices perform support but not device forming functions. However, there was a completely different situation when the experiments on the diffusion welding of Al to the SiC have begun. The thing is that the Schottky diode was chosen as the basic instrument for study the properties of DW contact. Contacts in the Schottky diode are of particular importance and are the device forming element. The first models of the DW contacts have shown the differences in the main Schottky parameters from the corresponding parameters of the devices with sputtered contacts. The analysis of the DW contacts characteristics has lead to the assumption about the appearance of a thin subcontact layer with destruction of the structure close to amorphous state. However, the suggested assumption needed a proof. Hence, arose the need for a detailed study of the electrical-physical contact properties after diffusion welding. Since no one before had not investigated the SiC surface after the diffusion welding, then the summarised results of the present work have formed the scientific novelty.

Scientific novelty:

1. ***It was found that diffusion-welded Schottky contacts have "soft" forward current-voltage characteristics. I-V and C-V analysis shown that due to the reduction of space charge region, the built-in potential in DW Schottky diodes usually is 0.5 V lower than for the ideal model and ~0.3 V lower than for real sputtered Schottky contacts.***

2. ***The observation of DW contact in transmission electron microscope (TEM) has revealed a thin ~25 nm subcontact area of silicon carbide with a strong distortion of the crystal structure. The microdiffraction picture of this subcontact layer indicates the presence of the small-grained phase, close to amorphous state.***

3. ***Using of combined method of vibrating capacitor & surface photo voltage was established the appearance of the additional charged states at the semiconductor surface after the diffusion welding. An increased density of such states, obviously, explains the reducing of space charge region in the semiconductor bulk.***

4. ***AFM study of the surface topography and SEM analysis before and after DW confirms the assumption of a possible solid-state etching of silicon carbide by aluminum during diffusion welding.***

The investigation results have been reported on numerous international conferences and were the base of 8 published works. To date the most in powerful commercial Schottky diodes with thin sputtered contacts are of ~3.5 mm^2 contact area with forward current up to 10 A. An increasing demand for high power devices will cause to search for new technological solutions in the contacts and packaging of SiC Schottky devices. Diffusion welding is ready to be an alternative way of metallization, especially because this method was successfully tested in commercial production of power silicon devices.

Therefore, the work on the investigation of DW contacts should be continued and the next nearest problems that I see is the identification and differentiation of the states associated with surface defects and the investigation of the DW contact properties in reverse branch of current-voltage characteristics.

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1. Korolkov, Oleg; Rang, Toomas; **Kuznetsova, N**; Ruut, J (2002). Preliminary investigation of diffusion welded contacts to p-type 6H-SiC. BEC 2002: proceedings of the 8th Biennial Baltic Electronics Conference: October 6-9, 2002, Tallinn, Estonia, pp. 55 - 56. **(classification number: 3.1)**
2. Korolkov, O.; Ruut, J.; **Kuznetsova, N**.; Rang, T. (2004). The Basic Parameters of Diffusion Welded Al Schottky Contacts to p- and n- SiC. R. Madar, J. Camassel, E. Blanquet (Toim.). Silicon Carbide and Related Materials 2003 pp. 857 - 860. Trans Tech Publications Ltd. **(classification number: 1.1)**
3. Korolkov, O.; Ljutov, J.; **Kuznetsova, N**.; Ruut, J.; Rang, T. (2004). Analysis of the basic Schottky parameters for diffusion-welded aluminium contacts to p- and n-type SiC. In: BEC 2004: proceedings of the 9th Biennial Baltic Electronics Conference: October 3-6, 2004, Tallinn, Estonia: (Toim.) Rang, T. Tallinn: Tallinn University of Technology, 2004, pp. 51 - 53. **(classification number: 3.1)**
4. Korolkov, O.; **Kuznetsova, N**.; Rang, T. (2006). Clamp mode package diffusion welded power SiC Schottky diodes. In: Proceedings of the 10th Biennial Baltic Electronics Conference BEC2006: 2006 International Baltic Electronics Conference, Tallinn, Oct. 2-4, 2006. (Toim.) T.Rang. Tallinn: IEEE Operations Center, 2006, pp. 55 - 58. **(classification number: 3.1)**
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COPIES OF SELECTED PAPERS

I. Korolkov, Oleg; Rang, Toomas; **Kuznetsova, N**; Ruut, J (2002). Preliminary investigation of diffusion welded contacts to p-type 6H-SiC. BEC 2002: proceedings of the 8th Biennial Baltic Electronics Conference: October 6-9, 2002, Tallinn, Estonia, pp. 55 - 56. **(classification number: 3.1)**

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Preliminary Investigation of Diffusion Welded Contacts to p-type 6H-SiC

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ABSTRACT: The first experimental results on diffusion welding (DW) applied to p-type 6H-SiC are described. Using the extrapolation method and available measurement apparatus the specific on-resistance and current-voltage characteristic of Schottky contacts in comparison with the n-type Schottky contacts were obtained.

1. Introduction

In all our early papers about DW contacts to SiC substrates and epilayers only n-type 6H- and 4H-polytypes were investigated [1]. In the same time, very few works are reported on p-type SiC Schottky diodes, e.g. [2], where some unique characteristics of diodes fabricated on p-type SiC are pointed out, which could make p-SiC very promising for high current density and high temperature applications. Comparison of forward and reverse characteristics of identical n- and p- type Schottky diodes clearly indicates that the p-type Schottky diodes could have advantages over n-type diodes at very high current densities (when self heating comes important), as well as at high temperatures. In turn, in his review paper [3], Madsen noted that the formation of p-type ohmic contact is even more difficult than formation of ohmic contacts to n-type SiC and the favored approach is to use Al or aluminium alloys, where post-annealing enables Al to diffuse into SiC thus resulting the ohmic properties of the conatct. The properties of metallic Al complicate the process of making ohmic contacts: Al easily oxides and it tends to volatilize during annealing act, but it still seems to support the formation of ohmic contacts. Unfortunately the mechanism by which it happens is not well understood. Since the process of diffusion welding is quite different from the conventional methods of metallization the characteristics of DW contacts to p-type SiC have a special interest.

2. Contact fabrication

In the experiments the n- and p-type "research grade" 6H-SiC wafers purchased from Cree Research Inc with epilayers from TDI Inc (USA) were used. The wafers were of following specification.

p^0 6H-SiC substrate pieces, average areas of 350mm^2 with thickness of 0.35mm. Net Al doping density - N_a~5×10^{17} cm^{-3}. Substrate orientation: (0001) Si, 3.5° off. Without epilayers. Surface treatment: Si-face sublimation etched.

p^0 – p^+ 6H-SiC structure with TDI p^+ epilayer. Structure size: 35mm diameter, 0.35mm thickness; epilayer thickness 0.3μm. p^+-epilayer net Al doping N_a ~ 1×10^{18} cm^{-3}. Substrate orientation: (0001) Si, 3.5° off. Substrate treatment: Si-face, p^+-epilayer as grown.

n^+ - p^{++} 6H-SiC structure piece with TDI p^{++} epilayer. Structure piece area of 260mm^2, thickness 0.35mm, epilayer thickness 1-3μm. p^{++} epilayer net Al doping N_a ~ 1×10^{19} cm^{-3}. Substrate orientation (0001) Si, 3.5° off. Surface treatment: Si-face, p^{++}-epilayer as grown.

n^0 6H-SiC substrate. Substrate size: diameter - 35mm, thickness – 0.35mm. Net nitrogen doping density N_d ~ 1×10^{18} cm^{-3}. Substrate orientation: (0001) Si, 3.5° off. Surface treatment: C-face polished.

All the wafers were qualified as "research grade", which means that the wafers have increased concentrations and densities of defects.

The commercial aluminium foil of 99.99% purity and the thickness of 0.03mm (operating contact) and 0.1mm (backside contact) was used for the contacting. After proper chemical treatment the aluminium foil was welded to the both sides of the silicon carbide samples in the special diffusion welding equipment UDS-6 in vacuum not worse than 10^{-4} torr at 600° C under the pressure of 15 MPa. Using chemical etching the Schottky contacts of 5mm diameter (Fig. 1) were formed. Further, using the extrapolation method [4] and available measurement apparatus the specific on-resistance and current-voltage characteristics of Schottky contacts were obtained.

3. Results and discussion

Fig 2. shows the variation of the specific on-resistance - $\frac{V}{I}A_c$, (A_c is the contact area) versus measurement current. As seen from Fig.2, the specific on-resistance for p-type 6H-SiC substrate is 5 times greater than the same one for n-type 6H-SiC substrate with the same doping concentration. Non-linear character of the specific on-resistance value for p- and n-type silicon carbide has the same nature, but with increase of the measurement current, the specific on-resistance for p-type SiC drops more sharply, and there is trend that at high currents the specific on-resistance for

p-type Schottky contacts will become lower than that of the n-type Schottky contacts.

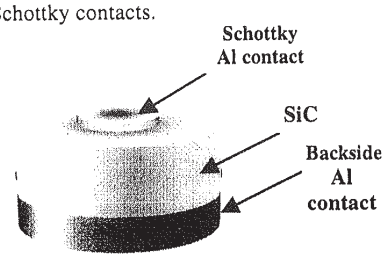

Fig.1. Schematic picture of the experimental specimen

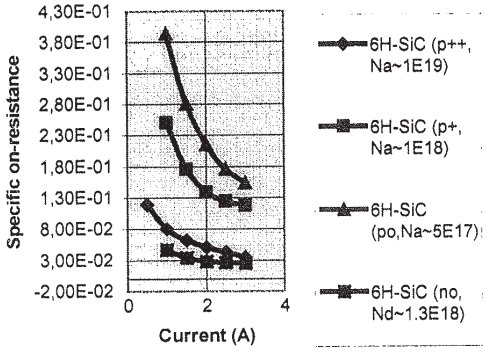

Fig. 2. Specific on-resistance vs current for p- and n-type SiC.

This trend has increasing character with the rise of doping concentration in p-type silicon carbide

Forward and reverse current-voltage characteristics of Schottky contacts, both for p-and n-type silicon carbide are shown in Fig.3.

Non-linearity of characteristics is more evident for p-type SiC substrate, than for the substrate of n-type and become more visible for p-type SiC structures with p^+-epilayer. The forward branches of characteristics are in a good agreement with the measured specific on-resistance values. So, at room temperature, the forward voltage drop is greater for p-type SiC Schottky contacts than for n-type SiC and decrease with increasing the doping concentration in silicon carbide.

4. Conclusions

Comparison of forward and reverse characteristics of Schottky contacts to n- and p-type 6H-SiC substrates gives the clear evidence that the diffusion welding contacts generally are in good conformity with the same characteristics of Schottky contacts obtained by conventional methods of metallization [2]

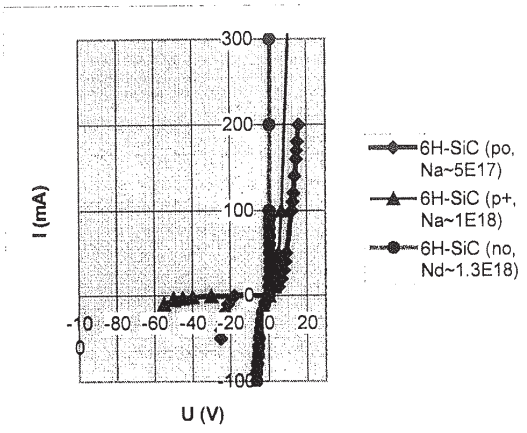

Fig. 3. Comparative I-V characteristics for p-and n-type SiC.

At the same time, since the mechanism of interaction between metal and semiconductor is too different for DW and, for example, for sputtering, it should be expected the quantitative distinction between their characteristics of contacts.

The direct comparison of the results for the conventional methods of metallization and diffusion welding can hardly be fulfilled now, because of the great difference between the thicknesses, contact area and so the current densities in both cases.

Never the less, the predicted optimal operating regimes for p-type SiC Schottky diodes seems to be more easily achievable for the thick and large DW contacts.

Acknowledgement

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G2815

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The Basic Parameters of Diffusion Welded Al Schottky Contacts to p- and n-SiC

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Keywords: Diffusion welding, Al p- and n-type Schottky contacts, Schottky parameters.

Abstract. Aluminium Schottky contacts to n- and p-type SiC were fabricated by diffusion welding. Forward current-voltage measurements were made in a temperature range of 300÷773°K. The basic Schottky parameters, such as saturation current (J_S), barrier height (Φ_B), the ideality factor (η), the effective Richardson's constant (A^{**}) and the series on-resistance (R_{sp}) were obtained from *U-I* curves at different temperatures. The comparative analysis of temperature variations of these parameters is presented.

Introduction

In our previous report [1] on the diffusion welded aluminium contacts to p-type SiC the first results of current-voltage and on-resistance measurements were presented. All the results were in good qualitative accordance with the same characteristics of Ni-Schottky contacts obtained by sputtering [2]. The direct quantative comparison was not possible because of the difference in Schottky contact metal. The results on electrical measurements for sputtered Al contact to n-type 4H-SiC were reported in [3] where the authors referred to our work [4], while no analysis of Schottky parameters was performed. To bridge the gap we present the basic parameters of diffusion welded Al Schottky contacts to p- and n-SiC obtained from the current-voltage (*U-I*) temperature characteristics.

Materials and sample preparation

The silicon carbide wafers used in experiments were form Cree Research Inc. and Sterling Semiconductor Inc. with the following specification:
p^0 6H-SiC substrate pieces from Cree with an average area of 350 mm^2, thickness - 0.35 mm. Net Al doping density $N_a \sim 5\times10^{17}$ cm^{-3}. Substrate orientation: (0001) Si, 3.5° off.
n^0-n^- 6H-SiC epi-structure from Sterling. Substrate size: diameter - 50.8 mm, thickness - 0.35 mm, epilayer thickness - 6 μm. Net nitrogen doping density in epilayer $N_d \sim 1\times10^{15}$ cm^{-3}. Substrate orientation: (0001) Si, 8° off.

The commercial aluminium foil of 99,99% purity and the thickness of 0.03 mm (operating contact) and 0.1 mm (backside contact) was used for the contact. After proper chemical treatment the aluminium foil was welded to the both sides of the silicon carbide samples in the special diffusion welding equipment UDS-6 in vacuum not less than 10^{-4} torr at 600°C under the pressure of 15 MPa. The Schottky square shaped (2×2 mm^2) contacts were formed on the samples by chemical etching.

Results and Discussion

The forward current-voltage (*U-I*) characteristics measured in the temperature range of 300÷773°K shown in Fig. 1 allow the quantitative determination of Schottky diode parameters such as the Schottky barrier height (Φ_B), the ideality factor (η), the effective Richardson's constant (A^{**}), and the series resistance (R_{sp}) of the diodes.

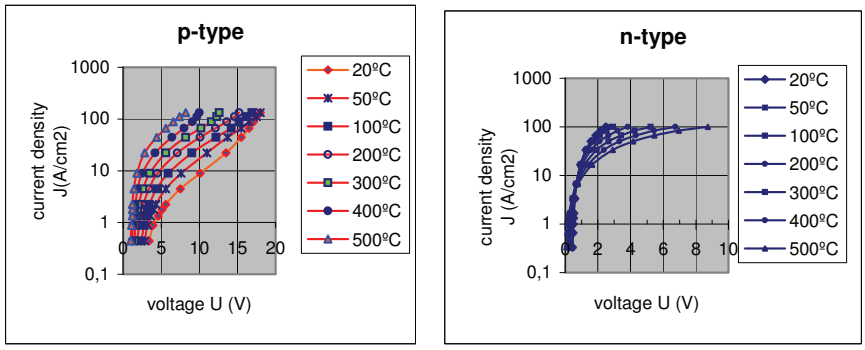

Fig. 1. Forward *U-I* characteristics of n- and p-type Schottky contacts.

The thermionic emission theory based *U-I* relationship taken from [5] suggests that if the applied voltage V is much larger than kT/q, then J can be approximated as

$$J = J_S \exp\left(\frac{qV}{\eta kT}\right). \quad (1)$$

The method given in [5] was used to determine J_S and Richardson constant (A^{**}). J_S can thus be determined from experimentally obtained forward density-voltage (U-I) characteristics at a given temperature by extrapolating the linear region of the lg$J$ versus V plot to $V = 0$ (Fig. 1).

High-temperature forward *U-I* data was utilized to obtain the Richardson constant. These quantities can be found from the y-intercept and the slope of the $\ln(J_S/T^2)$ vs. $1000/T$ plot.

The value of the active-area Richardson constant for n- and p-type diodes was found to be 6.2×10^{-7} and SiC and 9.6×10^{-8} A cm^{-2} K^{-2} respectively.

The temperature variation of saturation current (J_S) for p-and n-SiC contacts is shown in Fig. 2.

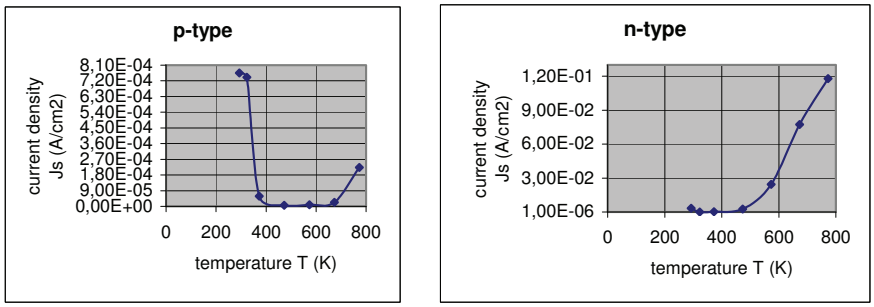

Fig.2. Temperature variation of saturation current (J_S) for p- and n-SiC Schottky contacts.

For the determination of the ideality factor (η), the Schottky barrier height (Φ_B), and the series on-resistance (R_{sp}) the Cheung's [6] suggested method was used. The idea of the method is that the voltage V_D across the diode can be expressed in terms of the total voltage drop V across the series combination of the diode and the resistor ($V_D = V - IR$).

Plotting $d(V)/d(\ln J)$ versus J, the slope of the straight line gives the specific series resistance, (R_{sp}), and the y-axis intercept gives the ideality factor (η). The Schottky barrier height is evaluated by defining a function $H(J)$ given as: $H(J) = R_{sp}J + \eta\Phi_b$.

The plot of $H(J)$ versus J thus gives a straight line that intercepts the y-axis at $\eta\Phi_B$, so if η is already known the barrier height can be determined.

The ideality factor, barrier height, and series on-resistance are shown in Fig. 3÷5 respectively.

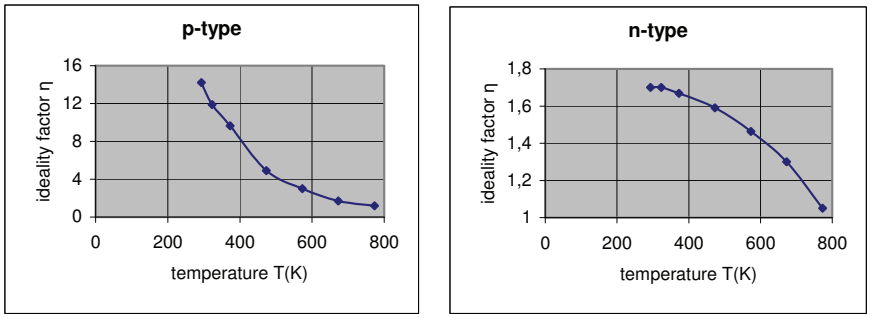

Fig.3. The temperature variation of ideality factor (η) for p- and n-SiC Schottky contacts.

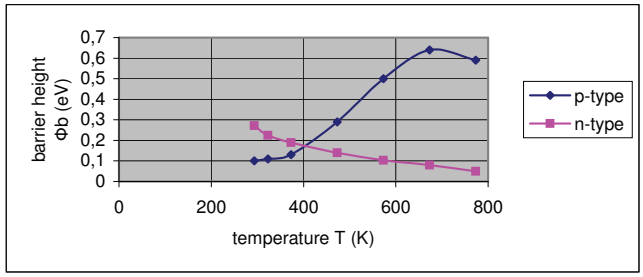

Fig.4. The temperature variation of barrier height (Φ_B) for p- and n-SiC Schottky contacts.

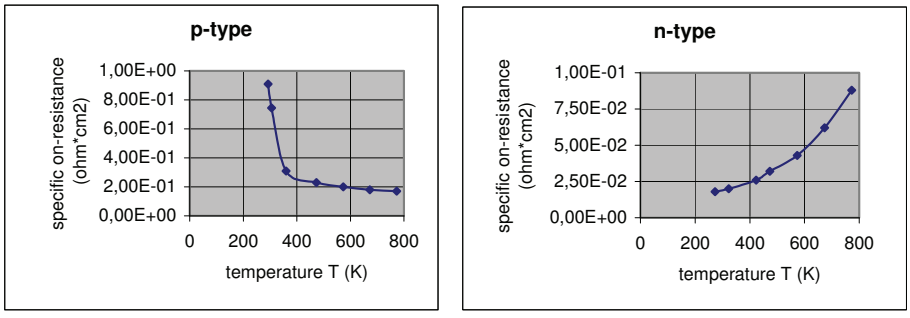

Fig. 5. The temperature variation of series on-resistance for p- and n-SiC Schottky contacts.

The comparison of the temperature dependence of Schottky parameters such as saturation current (J_S), barrier height (Φ_B), series on-resistance (R_{sp}) gives the evidence that for p- and n-SiC they appear to be opposed. The character of J_S temperature variation is in a good agreement with the temperature dependence of barrier height (Fig. 4). The barrier height for n-SiC decreases with the temperature and for p-SiC Φ_B increases. The slight lowering of Φ_B for p-SiC in temperature range of 673÷773°K results in saturation current rise in the same temperature range.

The ideality factors for all of the investigated wafers decreased with the temperature and are close to unity for n-SiC near 773°K (Fig. 3). As the elevated value of η for n-SiC at room

temperature (η = 1.65) can be explained by structure imperfection of intermediate layer of Al-SiC or by oxide, the enormous value of ideality factor for p-SiC in the temperature range of 300÷573°K cannot be explained only by surface states.

The value of Richardson's constant (A^{**}) obtained form *U-I* characteristics at different temperatures for diffusion welded Schottky contacts has been found to be several orders of magnitude lower than theoretically predicted (146 A cm^{-2} K^{-2}) [7]. That indicates that the effective active area may be in fact much smaller that the Schottky contact area. Besides that, the great contribution in A^{**} lowering bring the effects of quantum-mechanical reflection of electrons from the barrier and tunneling of electrons through the barrier.

The extraordinary experimental values of A^{**} used for barrier height calculation are the partial reason of drop in Φ_B values obtained in our experiments.

The temperature variations of series on-resistance (R_{sp}) for p- and n-SiC wafers are also significantly different. For p-type wafer R_{sp} decrease with the temperature rise and for n-type wafer R_{sp} linearly increase in temperature. The rise of n-type Schottky contact resistance is apparently connected with electron mobility lowering at elevated temperature and for p-type contacts the priority is the process of fractional ionization of impurities with the temperature rise and so the R_{sp} lowering.

The results obtained in our investigations are in good qualitative accordance with the results presented in the paper [2], but the direct comparison with literary data is a difficult problem. We have not found the necessary information about aluminium Schottky contacts to p-type SiC.

Comparatively little information on aluminium contacts to n-SiC is available. Their values vary in a wide range. For the barrier height the results are reported form 0.2÷0.3 eV up to 1.45÷1.7 eV and the ideality factor range from the value close to unity up to 13.3. The closer analogy with our results is presented in the recent paper [3], where Φ_B at room temperature is 0.67 eV and ideality factor η~1.66.

Conclusions

All the results on the electrical characteristics and Schottky parameters of aluminium diffusion welded contacts to p- and n-type silicon carbide obtained in our investigations give the apparent evidence that p-type contacts differ so much form their n-type analogy that p-type Schottky diodes can be marked out as individual group of devices. It exposes its own advantages at elevated temperatures and high current density.

The operation of Schottky structures under such extreme conditions needs the special metallization properties, which can be ensured by diffusion welding technology. More detailed measurements and modeling may provide deeper assurance about these phenomena and further studies are under way.

Acknowledgement

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Clamp mode package diffusion welded power SiC Schottky diodes

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Abstract. This paper is devoted to the results of a diffusion welding technique applied to solve the problem of packaging for large area SiC Schottky diodes. The forward current-voltage characteristics measured at 75 A measured for packaged diodes yields 250 A/cm2 (70A) at 1.9 V forward voltage. Reverse recovery time for packaged diodes was in the range of 29-36 ns.

1 Introduction

As is generally known the main obstacle for manufacturing power SiC power Schottky diodes with large area contacts is the high density of micropipes and screw dislocations in commercial substrates. During the last few years the research team of TDI, Inc. has developed defect-reduced techniques to increase the yield of SiC power diodes. Such technology prevents propagation of micropipes and screw dislocations from SiC substrate into active device area defined by the epitaxial layers and potentially increases the operating area of Schottky contact. In paper [1] 1 cm^2 300V Schottky diodes and high yield 0.03 cm^2 600V Schottky diodes were demonstrated using substrates with reduced defect density. At the same time, increase of Schottky contact area leads to problems in of power takeoff from large operating area, or in other words to the problem of external connections and proper device packaging. The problem is the current spreading resistance for large area Schottky contacts with submicron sputter metallization makes appreciable contribution to the total device resistance, limiting the forward operating current. The spot contact bonds for external connections, which can be made by thermal compressing, ultrasonic welding or impulse welding, can't solve the problem. Conductive glues or soft solders are not always suitable for large area sputter layers and they limit the operating temperature of device, preventing the realization of the full potential of SiC. In paper [1] several 2 mm diameter diode chips packaged in high frequency metal-ceramic packages and bonded to package terminal by golden ribbon were presented. This paper is devoted to the results of diffusion welding technique [2,3] applied to solve the problem of packaging for large area SiC Schottky diodes.

2 Diode Fabrication and Testing

To supply low defect density substrates for fabrication of 0.3 cm^2 Schottky diodes TDI's defect-reducing technology was used. 4H-SiC 2-inch diameter substrates with "standard" micropipe density were purchased from a commercial vendor. Defect density reduction in these substrates was done at TDI [4], and included, micropipe filling, porous SiC buffer formation, and combinations of the above. These substrates were delivered for CVD growth of thick undoped voltage blocking layers at TDI to form large area Schottky diodes. Diodes were fabricated on CVD grown low-doped epitaxial layer without edge termination. Double layer Ni-Au and triple layer Ti-Ni-Au sputter metallization were used for Schottky contacts fabrication. Non-rectifying backside contacts were provided by Ni-Au metallization. Diodes were tested on-wafer and delivered for dicing, and packaging. To decrease the parasitic spreading resistance the thickness of the initial sputter metallization was increased by diffusion welded 30 μm metal foil. The welding was made using three methods presented in Fig. 1.

To realize schemes 2 and 3 the initial sputter metallization was successively removed from the surfaces of the chips by chemical etching. Then over the top and the bottom faces of the chips simultaneously was welded 30 μm aluminium foil. Such method combine thick and plane metal foil with the chip making possible to perform the clamp mode package in cases used in power electronics (Fig. 2). This scheme of packaging ensures current takeoff from the whole contact area and increases maximum operating temperature to 600°C.

The forward current-voltage measurements to a maximum of 75 A were performed on the diodes fabricated by the schemes shown in Fig. 1. Comparative semilogarithmic J-V dependences for different methods are given in Fig. 3.

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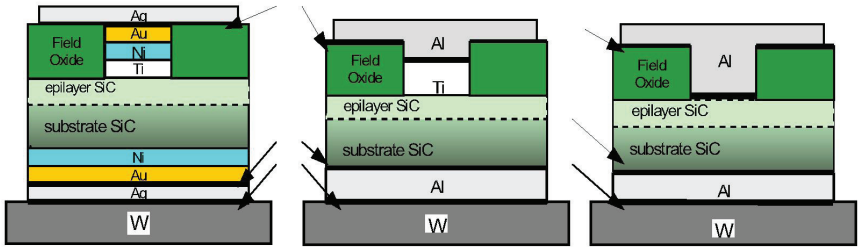


Fig. 1. Methods of chip metallization (diffusion welded contacts are shown by arrows).

Fig. 2. Diode clamp mode package.

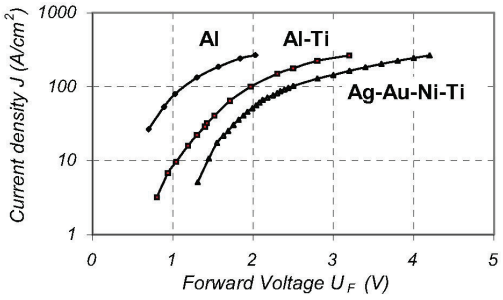


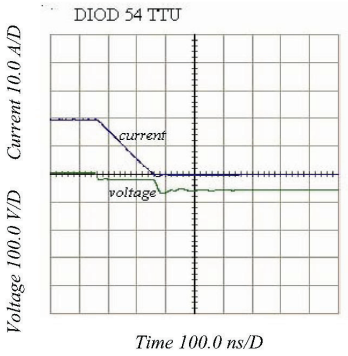
Fig. 3. Forward I-V characteristics for different methods of metallization.

The best results are attributed to the devices made using method 3, where the sputter metallization was fully removed from the surface and replaced by diffusion welded aluminium foil, 30 μm thick. This method gives a 250 A/cm^2 current density at less then 1.9 V of forward voltage, that corresponds to the results [1] received on the diodes with a 0.03 cm^2 area contact, at 8 A of forward current. The first method of fabrication, based on the simple approach to enlarge the thickness of contact by welding of thick (30 μm) silver foil over initial sandwich of sputter metallization, yielded the worst results. The values of specific on-resistance calculated using the method in [5], are as follows: method 1 – 3.95×10^{-3}, method 2 – 2.07×10^{-2}, method 3 – 3.55×10^{-2} ohm cm^2. The character of J-V curves shown in Fig. 3, confirms such conformity. This fact serves as confirmation that diffusion welding is not a simple mechanical thickening of metallization by bonding of thick metal foil, but causes a reformation of the metal-semiconductor interlayer. This changes the basic Schottky parameters, like barrier height and on-resistance.

The reverse recovery time (τ_{rr}) was measured on the first method of packaged diodes, since they most fully meet the requirements of reverse voltage, necessary for these measurements. The results and conditions of measurements are presented graphically and by the tables in Fig. 4.

In estimating the magnitude of reverse recovery time, the contribution of the package case capacitance to the total device capacitance must be taken into account. The package of the diodes was made in the available standard cases predestinated for silicon diodes of 20 mm diameter. So, the dimensions and mass of the cases was deliberately greater and do not conform to SiC Schottky chips of 7×7 mm^2 area. The reverse recovery time measurements carried out on the non-packaged chips under the same conditions gave $\tau_{rr} \sim 10$ ns (Fig. 5).

Hence, the contribution of package case in reverse recovery time of device makes up ~ 20 ns. So, bringing the dimensions of package case in accordance with the dimensions of SiC Schottky chips we may expect considerable reduction in value of reverse recovery time.



Test Conditions		Electrical Characteristics	
I_F	= 20 A	V_F	= 1,95 V
V_R	= 60 V	t_{rr}	= 29,0 ns
di/dt	= 100 A/μs	I_{RRM}	= 0,61 A
T_J	= 25 °C	FRRS	= 1,70
		Q_{rr}	= 8,85 nK
		E_{rec}	= 0,10 μJ

Fig. 4. Reverse recovery characteristic of packaged diode.
I_F – initial forward current; V_R – switching reverse bias; di/dt – rate of change of forward current;
Tj – junction temperature; V_F – forward voltage; t_{rr} – reverse recovery time; I_{RRM} – maximum reverse recovery current;
FRRS – factor of reverse recovery softens; Q_{rr} – total reverse recovery charge;
E_{rec} – recovery energy.

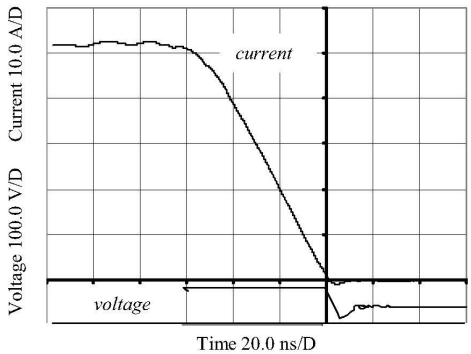


Fig. 5. Reverse recovery characteristic of non-packaged chip.

3 Conclusions

Defect density reduction techniques coupled with diffusion welded contacts have the potential for providing more effective use of large area Schottky by increasing the forward current takeoff through reductions in overall resistance.

Since the diffusion welding changes the structure of intermediate metal-semiconductor layer the basic Schottky parameters are also changed. To understand these changes the additional investigations on the optimum combination of the contact metals must be done.

Use of clamp mode cases for heavy current Schottky diodes provides a commercially suitable package method. This method of packaging ensures effective current takeoff from large area contacts and the absence of solder connections provides the potential to raise the operating temperatures up to melting point of contact metals.

Acknowledgements

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The Schottky Parameter Test for Combined Diffusion Welded and Sputter Large Area Contacts

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Keywords: Diffusion welded contacts, Large area diodes, Schottky parameters, Long-term stability

Abstract. For more authentic comparison of Schottky parameters between combined sputter (Ti/Ni/Au) and diffusion welded (DW) Al contact and direct DW Al contact to SiC the forward current-voltage characteristics were measured at the temperature range 293-473 K on full-packed 0.3 cm^2 Schottky diodes. Surprising fact was discovered that the temperature behaviour of parameters remains of the same character for both kind of contacts but for the combined sputter-DW samples the values of parameters is much closer in magnitude to sputter contacts. Apparently, chemical treatment before the DW process preserves untouched the contact surface layer formed by annealing of initial sputter metallization of the chips (e.g. Ni_2Si, Ti_3SiC_2), and this layer serves as barrier during diffusion welding. In the second part of the work we give the results on long-term reliability testing where through the SiC Schottky diode with the DW Al contacts during 300 hr has been passed constant forward stabilized current of 100 A/cm^2 density. The primary and final values of U_f for DW Schottky contact have not changed during the test.

Introduction

In our previous paper [1] a diffusion welding technique was applied to solve the problem of packaging for large area SiC Schottky diodes. The triple layer Ti-Ni-Au sputter metallization were used for Schottky contacts fabrication. Non-rectifying backside contacts were provided by Ni-Au metallization. To decrease the parasitic spreading resistance the initial sputter metallization was increased by diffusion welded 30 μm thick metal foil. Combined thick and plane metal layers make it possible to perform the clamp mode package used in power electronics. This scheme of packaging ensures current takeoff from the whole contact area and allows operating temperatures up to 600°C. The forward current-voltage characteristics at measured for packaged diodes yields 250 A/cm^2 (70 A) at 1.9 V forward voltages.

Since the diffusion welding can change the structure of intermediate metal-semiconductor layer the basic Schottky parameters also can be changed. To understand these changes the additional investigations on the optimum combination of the contact metals must be done. The forward current-voltage characteristics measured at different temperatures allow for quantative determination of Schottky contact parameters such as the effective-area Richardson constant A^{**}, Schottky barrier height Φ_b, ideality factor η, and the specific on-resistance R_{sp} of diodes using the method given in [2]. To verify the previous results [3] and for the more authentic comparison of Schottky parameters between sputtered and diffusion welded contact, in present work full-packed models of Schottky diodes were used for experiments.

Materials and sample preparation

The n-type 4H-SiC wafers with substrate nitrogen doping concentration of 2.5×10^{18} cm^{-3} and with 5 μm thick epilayer of 1×10^{15} cm^{-3} doping concentration were purchased from Cree Inc. (USA). On the opposite sides of the structure was sputter deposited Ni and after annealing at 1000 ºC for 3 min.

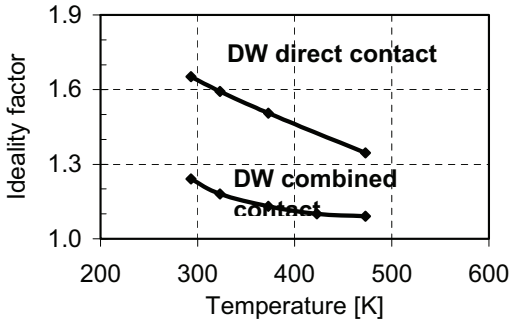

Fig. 1. Ideality factor η as a function of temperature.

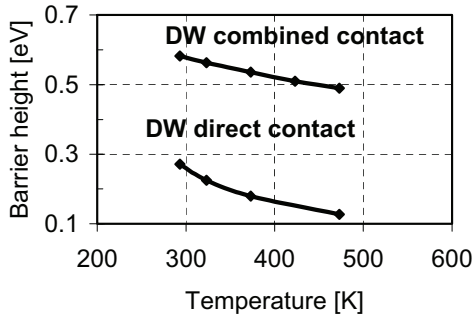

Fig. 2. Schottky barrier height as a function of temperature.

0.5 μm thick gold layer was deposited over the nickel contact. Sputter metallization and following thermal treatment of the chips were realized in TDI Inc. (USA). Afterwards, the 35 mm diameter wafer was cut into 6×6 mm^2 pieces.

Before diffusion welding the previous sputter metallization was chemically removed from both sides of the chips. For the fabrication of DW contacts to SiC commercial aluminium foil A99 with the thickness of 0.03 mm was used. The Al foil was welded to both faces of silicon carbide samples in the special diffusion welding unite UDS-6 in vacuum not worse than 10^{-4} torr at 600 ºC under the pressure of 30 MPa.

After diffusion welding the Schottky diode chips were packed in clamp-package cases and were marked as “DW combined contacts”.

Results and discussion

The temperature dependences of the basic Schottky diode parameters extracted from I-V characteristics by methods given in the [2] for “DW combined contacts” diodes compared to the earlier obtained results [3] where the direct diffusion welded Al contacts to 4H-SiC chips were used are presented in Figs. 1-3.

The mean value of the active-area Richardson constant for “combined contacts” diodes was found to be $A^{**}=4.0\times10^{-4}$ A·$cm^{-2}K^{-2}$. It is important to note that the extracted values of the active-area effective Richardson constants have been found to be several orders of magnitude lower than the theoretically predicted value (146 A·$cm^{-2}K^{-2}$). Such results are not unusual for sputter contacts too. For example, Saxena et al., [4] using the same method as we have used, have obtained the Richardson constants for sputtered Ni and Pt as 1.39×10^{-3} and 3.83×10^{-3} A·$cm^{-2}K^{-2}$, respectively. These results are close to ours, but we have the different conceptions of such low values of constants. The authors try to explain this by the fact that actually active area is smaller than the device area, or by effects of quantum-mechanical reflection of electrons from barrier and tunnelling of electrons through the barrier.

Our position lies in the fact that situation is more complicated and connected with structural specifics of the intermediate layer between metal and silicon carbide [5]. The process of extraction for Φ_b in this work was naturally preceded with attraction of experimental value of Richardson constants. The direct comparison of barrier height Φ_b, ideality factor η, the specific on-resistance R_{sp} between diffusion welded and sputter deposited Al contacts turned out to be rather difficult thing, because there are very few results on Al/4H-SiC contacts. Thus, in resent work [6] Harrell with co-authors gives for sputtered Al contacts to 4H-SiC the values of η ranged from 1.57 to 1.66 and Φ_b of 0.58 - 0.69 eV. The results are close to ours, but it must be noted that for calculation of barrier height the authors used the Richardson's constant as 146 A$cm^{-2}K^{-2}$.

The results for specific on-resistance R_{sp} at room temperature obtained in this work was found to be $R_{sp}=2.07\times10^{-2}$ Ohm·cm^2. These results seem to be an order higher than the results reported for sputter contacts in most of the works.

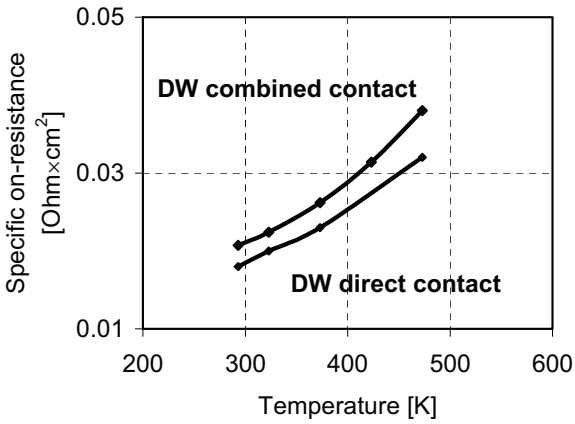

Fig. 3. Specific on-resistance as a function of temperature.

Thus, as seen from above the key Schottky parameters Φ_b, η, and R_{sp} for DW contacts lie in the range of the corresponding data for sputter contacts or differ not dramatically.

The more informative data may be obtained from the comparison of temperature behavior of basic Schottky parameters for sputter and diffusion welded contacts. The results obtained in this work demonstrate evident temperature dependence of key Schottky parameters as it seen from diagrams in Figs. 1-3. As seen from Fig. 1 the ideality factors for DW contacts were found to decrease with the temperature, and ranged from η =1.24 to 1.09. But decrease is not so dramatic as presented in the work [7] where the ideality factor was found to decrease with temperature from 3.2 to 1.6 for Pt/4H-SiC n-type sample in temperature range 25 - 425 ºC. The series on-state resistance in many works e.g. [8,9] is given as increasing with the temperature.

Thus, the comparative review of the temperature behaviour of basic Schottky parameters permits for conclusion that DW contacts have their own specifics but they are not too distant from the sputter contacts. Much more surprising thing was discovered in comparison of DW Schottky parameters obtained for package diodes with “combined DW contacts” and parameters for the direct DW Al contacts to SiC obtained earlier [3]. The temperature behaviour of parameters remains of the same character, but for “combined contact diodes” the values of parameters are much closer in magnitude to sputter contacts. The point of this concludes in previous treatment of the specimens before diffusion welding. Apparently, chemical treatment preserved untouched the contact surface layer formed by annealing after previous sputter metallization of the chips, (e.g. Ni_2Si, Ti_3SiC_2) and this layer serves as barrier during diffusion welding. This fact may be significant for structural composition of intermediate layer being formed during welding process and finally may change the contact properties.

As a remark, it must be noted that on-state resistance remains practically of the same value for both types of the chips. It means that intermediate layer has weak influence on R_{sp} and temperature behaviour of resistance is determined by electron mobility and donor fractional ionisation ratio.

The comparison of thermal stability of sputter and DW contacts is given in the second part of this work. This comparison was based on the results obtained during the experiment where through the SiC Schottky diode with the DW Al contacts during 300 hr has been passed constant forward stabilized current of 100 A/cm^2 density. Periodically, at 6 - 8 hr intervals was registered the forward voltage (U_f). The temperature was held relatively constant 50±1ºC.

The long-term stability for DW Schottky contacts shows the advantage over the sputter contacts [10] because after 300 hr test the primary and final values of U_f for DW contacts have not changed (Fig 4). Singh et al. [10] have tested their device with Ti/Pt/Au sputter contacts in the same condition and after 130 hr test the forward voltage of the device increased from 4.11 V to 4.19 V. Schottky diode with DW contacts showed slight instability in forward voltage during first 100 hr. of experiment, but primary and final values of U_f for DW Schottky contact have not changed after the test. This comparison is not fully correct because in Singh’s work was tested p-i-n rectifier with soldered output wire. In our test were used the clamp electrodes. That's why the increase in U_f in work [10] may be connected with the structural reconstruction of sputtered metal layer. In our case the slight instability of U_f in initial stage are determined by the processes on the clamp surfaces of the contacts.

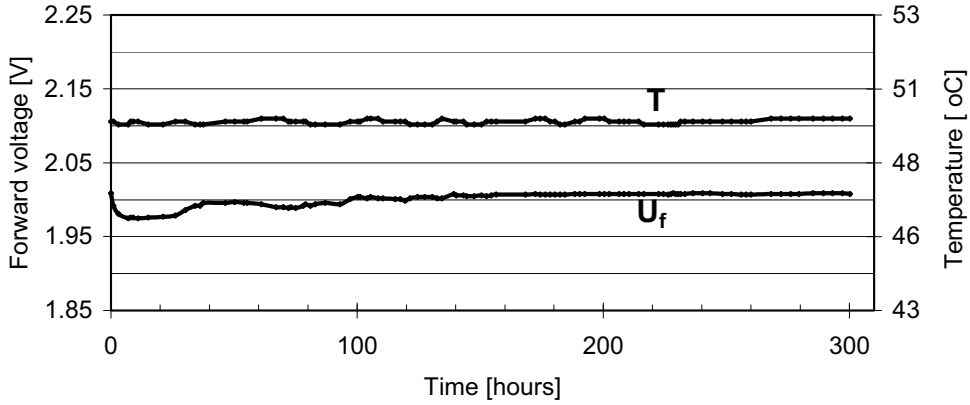

Fig. 4. U_f drift during long-term testing for devices with DW contacts.

Summary

Comparative review of the temperature behaviour of basic Schottky parameters permits to make the conclusion the DW contacts have their own specifics, but the properties of DW contacts are not so much distinct from the properties of sputter contacts. The difference in Schottky parameters for the direct DW Al contact and for combined sputter and DW contacts makes it possible to suppose an existence of barrier layer between Al foil and SiC in combined sputter and DW contacts. The weak difference of on-state resistance for direct and combined DW contacts means that intermediate layer has not strong influence on R_{sp} and temperature behaviour of resistance is determined by electron mobility and donor fractional ionisation ratio. The long-term stability for DW contacts shows the advantage over the sputter contacts.

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The Schottky Parameter Test for Combined Diffusion Welded and Sputter Large Area Contacts

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Investigation of Subcontact Layers in SiC After Diffusion Welding

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Keywords: Diffusion Welding; Metal Contacts; Interface Layer; Transmission Electron Microscopy; Diffraction Investigations.

Abstract. In our early analytic reports [1,2] has been made the supposition that during the diffusion welding *(DW)* in subcontact area of SiC is formed the intermediate amorphous layer. In the present work are given the first results of transmission electron microscopy (*TEM*) and electron diffraction investigations of subcontact layers in n^0-n^- 4H-SiC. *TEM* examinations show that the boundary between aluminium and silicon carbide looks like stripy interface layer of ~ 25 nm thickness. This is the evidence that during diffusion welding in subcontact surface layer of SiC the shear micro deformations have been taking place and due to this process the plane inclusions of small-grained phase have been appeared. The image of contact area obtained in diffracted SiC rays (dark field) apparently confirms that stripy zone belongs to silicon carbide because the aluminium (black zone) fell out of contrast. Diffraction picture obtained from bulk zone of silicon carbide looks like monocrystallin, but the micro diffraction pattern obtained from the subcontact (stripy zone) gives a lot of concentric rings, that makes evidential the fact of existence of small-grained inclusions. Deciphering of this electron-diffraction pattern reveals the presence of such elements as residue SiC, Al, Si, as well as inclusions of graphite.

Introduction

In our previous reports [1,2] were presented the basic parameters of diffusion welded Al contacts to p- and n-type SiC, extracted from the experimental current-voltage (I-V) characteristics. The results were in qualitative accordance with the same characteristics of Schottky contacts obtained by sputtering e.g. [3], but the quantative comparison shows the strong disparity between practical results and parameters predicted by ideal Schottky-Mott physical model.

Low barrier heights both for p- and n-type contacts obviously are conditioned by quite low values of effective Richardson constants (A**), $6.2\text{x}10^{-7}$ $\text{Acm}^{-2}\text{K}^{-2}$ for n-type and $9.8\text{x}10^{-8}$ $\text{Acm}^{-2}\text{K}^{-2}$ for p-type wafer. Such extremely low values of (A**) can be attributed to the specific of *DW* Schottky interface.

For ideal Schottky barrier, the effective Richardson constant calculated with regard to effective mass of electron, and neglecting the effects of optical photon scattering and quantum mechanical reflection is found to be A* = 146 $\text{Acm}^{-2}\text{K}^{-2}$ [4]. For free electrons the Richardson constant A is 120 $\text{Acm}^{-2}\text{K}^{-2}$. Thus, issuing from universal Richardson constant formula:

$$A = \frac{4\pi m_0 q k^2}{h^3}, \qquad (1)$$

the ratio between effective and rest mass of electron must be: $\frac{m^*}{m_0} = \frac{A^*}{A} = \frac{146}{120} = 1.22$.

Taking into account the probabilities of electron scattering on low-frequency phonons (f_{ph}) and quantum-mechanical reflection of electrons (f_d), the effective Richardson constant ($A^{**} = f_{ph} f_d A^*$) cannot be less than 50 % of A^* [5]. In this case the minimum mass ratio can be: $\frac{m^*}{m_0} = 0.61$.

The Richardson constants extracted from experimental I-V characteristics of DW contacts give the effective and rest mass ratios 8×10^{-10} for p-type wafer and 6.2×10^{-9} for n-type.

The small values of Richardson constants for sputter metallization given in any works (e.g. [6]) are explained by the authors so, that either the effective active area is in the fact smaller than the device area, or by the fact that effects of quantum-mechanical reflection of electrons from the barrier and tunnelling of electrons through the barrier are not included in the calculation for A^{**}. Such explanation does not seem to be persuasive. If electron scattering on phonons and quantum-mechanical reflection come into effect the effective Richardson constant (A^{**}) can be only two times lower than theoretic A^*. Thus, the real effective active area becomes the only and cardinal reason for constant A^{**} lowering. That means that dimensions of active area must be of somewhat interatomic space and even smaller if the device area is of 30–240 μm diameter. Such situation seems to be unbelievable.

As for *DW* Al contacts, the discrepancy between the experimental Richardson constant and theoretical value for ideal Schottky contact is much more serious and the experimental constant is lower than theoretical value for ten orders of magnitude. The effective mass for *DW* contact turns out to be billion (10^9) times less than the electron rest mass. In other words, from the point of classic theory such values of parameters are *incredible*.

If in the law of free electron dispersion:

$$E_{(\bar{k})} = \frac{\hbar^2 \bar{k}^2}{2m}, \qquad (2)$$

the experimental effective mass is substituted for electron rest mass, the dispersion grows nine orders of magnitude. Such a dramatic rise of dispersion is the evidence of distortion in lattice periodicity. As appears from above it may be supposed that during welding process as a result of shear micro deformations and heterodiffusion an amorphous layer appears between Al and SiC. The supposed amorphous layer may be up to ~ 500 nm thick. The thickness is limited by the possibilities of heterodiffusion in conditions of thermal-deformation cycle of diffusion welding. The amorphous layer brings the distortions in physical model of Schottky diode and causes the discrepancy between theoretical and experimental results.

In confirmation of our theoretical supposition this paper presents the first series of electron microscopy study of subcontact layer in 4H-SiC after *DW* metallization.

Materials and specimen preparation

For electron microscopy examination was chosen 4H-SiC $n^0 - n^-$ structure, 350 μm of thickness with 6 μm epilayer and (0001) Si orientation. After proper chemical treatment the aluminium foil of 30 μm thick was welded to the both sides of the sample in the special diffusion welded machine UDS-6 in vacuum not worse than 10^{-4} torr at 600ºC under the pressure of 20MPa. (More detailed information about DW technology can be found in our early papers (e.g. [7]). The interface was examined in cross-section by transmission electron microscopy. The specimen preparation before *TEM* analysis has been made in standard conventional way: mechanical grinding and polishing by use of Gatan, Inc. tools line. The finish thinning was performed in DuoMill 600 – ion beam etching

apparatus of Gatan, Inc. The *TEM* interface examination was made in JRM (JEOL) 2100F microscope at an accelerating voltage of 200 kV.

Results and Discussion

In Fig.1, is shown the *TEM* image of interface boundary between aluminium and silicon carbide. The thickness of interface layer is ~ 25 nm and the layer (marked by arrow) is of stripy character. This is the evidence that during diffusion welding in subcontact surface layer perpendicularly to C-axis of SiC the shear micro deformations have been taking place and due to this process the plane inclusions of small-grained phase have been appeared. In left upper corner of the picture is shown the image of the same contact area obtained in diffracted SiC rays (dark field). Apparently the stripy zone belongs to silicon carbide because the aluminium (black zone) fell out of contrast.

Residual disturbances of crystalline structure in bulk SiC zone have local character (Fig. 2). They look like separated, mainly horizontal, shear deformation zones in basic planes of silicon carbide and are the sources of dislocations. But the diffraction picture obtained from bulk zone of silicon

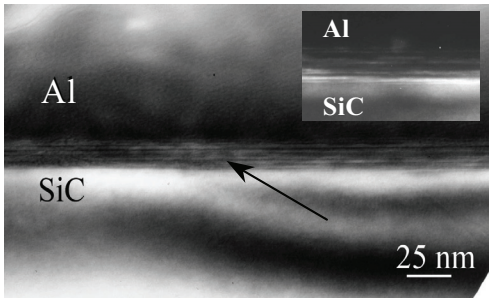

Fig. 1. TEM image of boundary contract zone

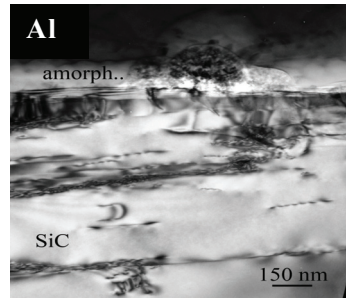

Fig. 2. Residual disturbances of crystalline structure in bulk SiC.

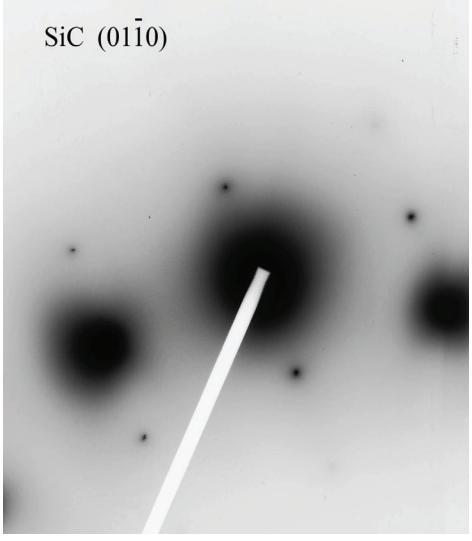

Fig. 3. Electron-diffraction pattern of bulk zone of silicon carbide

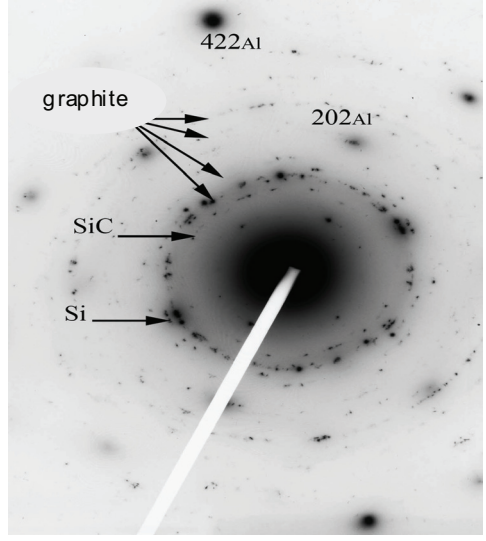

Fig. 4. Electron-diffraction picture of subcontact zone in silicon carbide

carbide (plane $01\bar{1}0$) looks like monocrystallin (Fig. 3). The position of major spot is determined by the position of the trap.
At the same time on the microdiffraction obtained from the subcontact layer (stripy zone) a lot of concentric circles are to be observed (Fig. 4). That makes evidential the fact of existence of small-grained phase. Decipherment of this electron diffraction pattern gives the following range of interplanar atomic distances in Angströms (Å): 3.35, 2.55, 2.15, 1.94, 1.84 and 1.24. The ring with d=2.55 belongs to residue silicon carbide, the ring with d=1.94 to silicon. All the rest are in good accordance with interatomic distances for graphite: d (0002) = 3.35, d $(10\bar{1}0)$ = 2.13, d $(10\bar{1}1)$= 2.03, d $(10\bar{1}2)$= 1.8 and d $(11\bar{2}0)$ = 1.23. The point reflexes in diffraction pattern belong to aluminium (plane (111); the experimental values: 1.44, 1.25, and 0.79 are in good confirmation with the table data: d (022) = 1.43, d (113) = 1.22, and d (224) = 0.8.

Summary

The basic message of this paper is to show that strong disparity between the experimental electrical parameters of DW contacts and parameters predicted by ideal Schottky-Mott model must be attributed to specific of the interface between metal and silicon carbide. The TEM examination revealed that the stripy interface layer of ~25 nm was formed directly on SiC surface after diffusion welding. We consider this fact as evidence that during DW at elevated temperature and under tangential forces the shear microdeformations have been taking place in subcontact surface of SiC. The direct contribution of DW thermal-deformation parameters to this process is the subject of our future detail studies, which are now under the way.

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