INFOTEHNOLOOGIA TEADUSKONNA ARVUTITEHNIKA INSTITUUDI TEADUS- JA ARENDUSTEGEVUSE AASTAARUANNE 2011

1. Instituudi struktuur

Instituudi direktor Margus Kruus

- Arvutitehnika ja -diagnostika õppetool, Chair of Computer Engineering and Diagnostics, Ubar Raimund-Johannes
- Digitaaltehnika õppetool, Chair of Digital Systems Design, Margus Kruus
- Süsteemitarkvara õppetool, Chair of Systems Programming, Ahto Kalja

2. Instituudi teadus- ja arendustegevuse (edaspidi T&A) iseloomustus

2.1. Struktuuriüksuse koosseisu kuuluvate uurimisgruppide teadustöö kirjeldus ja tulemused

2.1.1. Teadustöö kirjeldus

The research is carried out in three fields: digital systems and design, digital test and diagnostics, and system software.

In the field of system hardware design and test, the following topics are covered:

(1) Diagnostic modeling of digital systems,

(2) Fault simulation algorithms and methods,

(3) Hardware verification,

(4) Test pattern generation,

(5) Processor-centric board testing,

(6) Built-in self-test in digital systems,

(7) Development of FPGA-based computing methods,

(8) System-Wide Fault Management for Failure Resilience,

(9) Design for Dependability, and

(10) Development of experimental research environment.

The research activities of the system software group includes the topics:

(11) web based systems, e-Government, information systems and CAD.

Scientific work in the department is coordinated mainly by the research plans of the Excellence Centre CEBE funded by EU structural funds, where the institute is the leading partner of the centre, Target financing project SF0140041s08 “Design of Reliable Embedded Systems”, and two EU FP7 projects CREDES and DIAMOND.

In frame of CEBE, the institute is coordinating and leading the research in three cooperation projects: P1: Application Specific Processors for Signal Processing in Biomedicine, P2: Verification, test generation and fault diagnosis, and P4: Evaluation of mental disorders using EEG analyser.

2.1.2. Teadustöö tulemused

(1) Several new results have been achieved in extending the theory of decision diagrams (DD). Extension of the Structurally Synthesized Binary DDs to the SSBDDs with multiple inputs (SSMIBDD) allows to reduce the complexity of the previous model, to speed up simulation, and to minimize the complexity of fault modeling. The High Level DDs (HLDD) was proved to be the first canonical representation of digital systems as a generalization of logic level BDDs. The main impact

is the possibility of translation logic level algorithms of diagnosis to higher system levels with reduced complexity. New methods for high-level verification and test generation were developed which provide more accurate results than traditional VHDL code coverage based methods.

(2) New fault simulation methods were developed and implemented. For logic level, a new parallel critical path tracing method was invented, which the first time allows exact calculation of faults in the nested fanout-free regions in parallel for many test patterns simultaneously. In average about 10 times higher speed was achieved than with commercial simulators in use. For higher functional levels, a novel deductive fault simulator was developed with a speed of up to two orders of magnitude higher than with traditional, logic-level methods.

(3) A new verification method based on mutation testing using transaction level modeling at SystemC was developed. An open-source platform for advanced hardware design, verification and debug zamiaCAD was proposed in cooperation with IBM, Germany.

(4) A constraint-driven high-level test pattern generation method was developed based on HLDDs and on a combination of hierarchical, functional and mixed fault models. The first time, proofs were developed for high-level untestable faults, and the methods were developed for proving gate-level untestability on higher levels. The novelty of the results is in the hierarchical fault analysis which allows to cope with the high number of faults.

(5) We proposed a general modeling methodology for automated test path synthesis for microprocessor SoC-based systems, that drastically reduces the cost of test programs. The new automation methodology forms a complementary solution to traditional boundary scan that allows to overcome it's weaknesses at no investment into system design process.

(6) Multi-dimensional optimization methods at given constraints have been developed for Hybrid BIST and BIST with reseeding in single core designs. A novel reseeding optimization algorithm based on test compaction techniques for sequential designs is proposed. Experiments showed that applied heuristics can yield optimal or quasi-optimal solutions in polynomial time. The solutions outperform previously published reseeding and hybrid BIST results. A novel more general hierarchical approach was proposed as an upper level optimization strategy. The main contribution and novelty is in representing search space as a function of some parameters of BIST for finding the best solution in a very fast way. No methods for optimization of multi-core BIST processes have been proposed so far.

Most results of this field is presented in the PhD thesis of Helena Kruus, defended in 2011.

(7) Methods were developed for accelerating of recursive data sorting over tree-based structures using different FPGA-based computing platforms. Comparably with other techniques our approach allows very fast rearranging of newly arriving items that is an important feature for data processing in stream applications. The results of experiments clearly demonstrate applicability and high efficiency of the proposed methods, which can easily be implemented not only in advanced, but also in low cost widely available FPGAs.

The research in this field is carried out in a very close cooperation with University of Aveiro in Portugal.

(8) Fault tolerance and fault management mechanisms are necessary means to reduce the impact of soft errors and wear out in electronic devices. Typically, fault tolerance techniques assume certain limits in error rates when they are still applicable. Failure resilience goes beyond that by localizing and classifying faults into e.g. transient vs. permanent and critical vs. low-priority ones. We have proposed a new general scalable fault management architecture based on the latest upcoming DFT standard IEEE P1687 IJTAG. The standard allows to create an efficient and regular network for handling fault detection information as well as to manage test and system resources as a system-wide background process during system operation.

(9) We have developed a system-level model and design space exploration environment for designing dynamically reconfigurable NoC-based systems with real-time constraints. Proposed approach can be used for communication modeling and synthesis to calculate communication hard

deadlines that are represented by communication delay and guide the scheduling and (re-)mapping processes to take into account possible network conflicts. The work can be used in various contexts. For example, the presented approach can be enhanced such, that communication and computation slack can be optimized for enabling different SW based fault tolerance methods.

The research is carried out in close cooperation with TU Darmstadt as the produced schedules are verified with cycle-accurate XHiNoC simulator, developed at TUD and is currently being integrated with the TUD lower level NoC design flow.

(10) A prototype software environment for modeling the functionalities of JTAG and Boundary Scan standards in testing ofdigital systems. The tools include goJTAG and Trainer 1149 software, and BIST Analyzer for synthesis and optimization of BIST. The tool set represents a unique environment for teaching digital design and lab research. The tools have been regularly used in teaching at U Aveiro in Portugal, TU Darmstadt and TU Ilmenau in Germany and at TU Tallinn.

(11) Several new e-Government services for X-Road platform were devewloped. We have proposed a novel approach to integrating asynchronous communication into OSGi service platform and we have proposed an intelligent learning object as a tool for teaching the basics of digital logic in which students learn by exploring and investigating the elements. The novelty of the tool relies in the use of specially designed ontology to capture domain knowledge of microelectronics.

Cooperation results in CEBE:

1. CEBE Project P1. Based on two biomedical signal processing units, bioimpedance and EEG analyzers, a concept of digital signal processing modular platform has been developed. The platform will essentially consist of three parts - communication network, input sensors and output actuators, and signal processing units. While the sensors and actuators can be seen as more-or-less standard ADC-s and DAC-s, the other parts must be configurable to allow to make trade-offs depending on the design constraints like performance, energy consumption, etc. Future research will focus onto analyzing the requirements of different signal processing applications to identify the needs for parameterization and developing parameterizable network and processing modules.
2. CEBE Project P2. The goal of the project is to verify the designs of signal processors developed in CEBE and carry out the testability analysis, fault simulation and test generation. A converter was developed for creating SSBDD based diagnostic models of the processor architectures developed in P1. The VHDL designs of 8 signal processors developed in P1 were converted into the diagnostic models. The testability of the processors and the potential quality of testing the processors by traditional BIST methods was analyzed and suggestions worked out. A useful synergy was achieved here with creating a biosignal processors which will have practical use in medical field and simultaneously were used as a family of bechmark circuits to prove the unique properties of new test algorithms in the field of electronics.
3. A device for determining human depression by measuring EEG signals of the brain and using a special SASI algorithm developed in Technomedicum was developed. In cooperation with Technomedicum, the algorithm was implemented as a FPGA-based prototype of an EEG Analyzer device. The analyzer is aimed at early detection of brain disorders and can be used for preventing screening of people or monitoring special groups of high-risk or high-stress workers (military personnel, police, rescue workers). Compared to existing EEG analyzers, the developed one has advantages in high detectability of disorders and simplicity of implementation (one EEG channel, quick noninvasive method). The proposed portable EEG analyzer device will be evaluated in the North Estonia Medical Center.

2.2 Uurimisgrupi kuni 5 olulisemat publikatsiooni läinud aastal.

1. Sagahyroon, F. A. Aloul, A. Sudnitson, "Using SAT-Based Techniques in Low Power State Assignment" Journal of Circuits, Systems, and Computers (JCSC), Vol. 20, No. 8, 2011, p. 14, World Scientific Publishing Company, ISSN: 0218-1266. (1.1)
2. D.Mihhailov, V. Sklyarov, I. Skliarova, A. Sudnitson. Acceleration of Recursive Data Sorting over Tree-based Structures. J. of Electronics and Electrical Engineering, 2011, No. 7(113), pp. 51-56. (1.1)
3. M.Tagel, P.Ellervee, T.Hollstein, G.Jervan. System-level optimization of NoC-based timing sensitive systems. Estonian Journal of Engineering, 17(2), pp.158 – 168, 2011. (1.2)
4. R.Ubar, J.Raik, H.-T.Vierhaus (Eds.). Design and Test Technology for Dependable Systems-on-Chip. Information Science Reference, Hershey - New York, *IGI Global,* 2011, 550 p. (2.1)
5. J.Raik, A.Rannaste, M.Jenihhin, T.Viilukas, H.Fujiwara, R.Ubar. Constraint-Based Hierarchical Untestability Identification for Synchronous Sequential Circuits. Proc. of European Test Symposium, Trondheim, Norway, May 23-27, 2011, pp. 1-6. (3.1)

2.3 Loetelu struktuuriüksuse töötajate rahvusvahelistest tegevustest.

1. Raimund Ubar
    - IEEE East-West Design & Test Symposium (EWDTS) – aseesimees
    - IEEE Latin American Test Workshop (LATW) – Ida-Euroopa regiooni koordinaator
    - EU programmi ARTEMIS JU evaluaator
    - Reed-Muller 2011 Workshop, Finland – Keynote speech
2. Peeter Ellervee
    - Baltic Electronics Conference (BEC) – aseesimees
    - NORCHIP Conference – juhtkomitee liige
    - FPGAworld Conference 2011 – sektsiooni juhatamine
    - 10. SoC Symposium 2011 – sektsiooni juhatamine
3. Ahto Kalja
    - PICMET11(USA) – riikide esinduskomitee liige
    - Acta Universitatis Latviensis seeria Informatics toimetuse liige
4. Jaan Raik
    - IEEE Design and Diagnostics of Electronics Circuits and Systems (DDECS'12) – esimees
    - IEEE European Test Symposium (ETS'2012) – tutoorialide sessiooni esimees
    - IEEE European Dependable Computing Conference (EDCC) – juhtkomitee liige
    - Baltic Electronics Conference (BEC) – juhtkomitee liige
    - IEEE 12th Workshop on RTL and High Level Testing 2011 – ümarlaua sektsiooni juhatamine
    - FP7 Raamprogrammi Europrojekt DIAMOND – Projekti üldkoordinaator
5. Gert Jervan
    - European Association for Education in Electrical and Information Engineering (EAEEIE) – juhtkomitee liige
    - IEEE International Workshop on Impact of Low Power Design on Test and Reliability (ReCoSoC) – erisessiooni organisaator ja juht
    - FP7 Raamprogrammi Europrojekt CREDES – Projekti üldkoordinaator
    - FP7 Raamprogrammi INCO projekt KhAI-ERA – Eesti poolne koordinaator
6. Thomas Hollstein
    - Baltic Electronics Conference (BEC) – juhtkomitee liige
7. Maksim Jenihin
    - COST European Network of Competence. Manufacturable and Dependable Multicore Architectures at Nanoscale – Eesti poolne koordinaator

- IBM Faculty Award (2011-2012): ZamiaCAD Framework for Hardware Design, Debug, and Research

8. Artur Jutman
    - EUROSTARS: COMBOARD - FPGA-Based Test Acceleration Methodology for Complex Electronic Boards projekt – Eesti poolne koordinaator

2.4 Loetelu struktuuriüksuse töötajatest, kes on välisakadeemiate või muude oluliste T&A-ga seotud välisorganisatsioonide liikmed

2.5 Aruandeaasta tähtsamad T&A finantseerimise allikad.

1. SA Archimedesega sõlmitud lepingud infrastruktuur:
    - AP041, Töökindlate sardsüsteemide disain, Ubar Raimund
    - ÜLTAP61, Integreeritud elektroonsed süsteemid ja komponendid (SARS2), koordineerib elektroonikainstituut
    - ÜLTAP15-3, Mikro- ja nanostruktuursed sardsüsteemid ja komponendid (SARS3), koordineerib elektroonikainstituut
    - Magistriõppekava "Arvutisüsteemid" arendamine – COMPSYS, Ellervee, Peeter
2. Eesti tippkeskused:
    - TAR8077, Integreeritud elektroonikasüsteemide ja biomeditsiinitehnika tippkeskus, Raimund Ubar
    - Koostöö Eesti Arvutiteaduse tippkeskusega EXCS (tarkvara grupp)
3. EL Raamprogrammi projektid:
    - VFP382, Centre of research excellence in dependable embedded systems, Jervan Gert
    - VFP443, European Union's 7th Framework Programme IST collaborative project DIAMOND, Diagnosis, Error Modelling and Correction for Reliable Systems Design, Raik Jaan
4. Välisriiklikud lepingud:
    - VERT403, European Thematic Network for Teaching, Research and Innovations in Computing Education(ETN TRICE), Sudnitsõn, Aleksander
    - VERT422, Enhancing Lifelong Learning for the Electrical and Information Engineering Community - ELLEIEC, Jervan, Gert
    - Adaptiivne rikete diagnostika struktuurse multituumalise emuleerimise baasil – ERADOS, Jutman, Artur
    - COMBOARD: FPGA põhine keeruliste elektroonikaskeemide testimise kiirendamise metodoloogia, Jutman, Artur
5. SA Eesti Teadusfond grandid:
    - ETF8478, Riistvara funktsionaalne verifitseerimine ja silumine, Jenihhin, Maksim
    - ETF7894, Süsteemitesti meetodid keerukatele trükkplaatidele, Jutman, Artur
    - ETF7483, Isediagnoosivad digitaalsüsteemid, Ubar, Raimund
6. Haridus- ja Teadusministeeriumi sihtfinantseeritav teema:
    - SF0140041s08, Töökindlate sardsüsteemide disain , Ubar, Raimund

2.6 Hinnang oma teadustulemustele.

1. Uurimisgrupp on Eestis valdkonna juhtpositsioonil, omab 16 projekti: 3 ETF granti, on 2 FP7 raamprogrammi projekti koordinaator, käivitati 5 uut rahvusvahelist projekti: COST, ZUSYS, IBM Faculty Award, projektide COMBOARD, ROBSY initsiaatoriks on instituudist välja kasvanud spin-off firma Testonica Lab.

2. Instituut koordineerib Eesti Teadustippkeskust CEBE, kus koos partneritega Elektroonika instituudist ja Tehnomeedikumist on 3-aastase eksisteerimise vältel saadud märkimisväärseid tulemusi, mille tunnistuseks on 2011. a. lõpul toimunud rahvusvahelisel evalveerimisel kõikide kriteeriumite järgi saadud hinded "väljapaistev".

3. Instituudi vanemteadurile Maksim Jenihhinile omistati märkimist vääriv rahvusvaheline auhind: IBM Faculty Award for "ZamiaCAD Framework for Hardware Design, Debug and Research"

4. Instituudi 2011. aasta tähtsamateks tulemusteks on:

- digitaalsüsteemide kõrgtaseme kanooniline graafmudel, meetod nende ekvivalentsuse tõestamiseks (3 publikatsiooni);
- uut tüüpi otsustusdiagrammide mudelid, nende korrektsuse tõestus ja neil põhinevad simuleerimismeetodid (4 publikatsiooni);
- meetodid rikete analüüsi kiirendamiseks (3 publikatsiooni);
- hierarhiline rikete diagnoosimeetod (2 publikatsiooni);
- uus efektiivsem hierarhiline testide genereerimise meetod (2 publikatsiooni);
- automatiseeritud testprogrammide süntesaator trükkplaatidele (1 publikatsioon);
- meetodid andmete rekursiivse sorteerimise kiirendamiseks erinevatel FPGA tehnoloogia platformidel (7 publikatsiooni);
- koostööna tippkeskuse CEBE partneritega eriprotsessor signaalitöötluseks biomeditsiinis ning digitaalse signaalitöötluse modulaarplatvormi kontseptsioon projekteerimise efektiivsuse tõstmiseks (2 publikatsiooni).

5. Kaitsti 1 doktoritöö (H.Kruus), kuid 2012.aasta esimeses pooles on kaitsmisele tulemas 5 doktoritööd, neist 2 doktoritöö kaitsmine (D.Mihhailov, A.Tšertov) on käesoleva aruande esitamise hetkeks juba toimunud.

6. Avaldati monograafia USA-s ja 35 artiklit (s.h. 1.1 - 1, 1.2 - 4, 3.1 - 24).

7. Kokkuvõttes oli päris edukas aasta.

2.7 Instituudi teadus- ja arendustegevuse teemade ja projektide nimetused *(Eesti Teadusinfosüsteemi, edaspidi ETIS, andmetel)*

- Haridus- ja Teadusministeeriumi sihtfinantseeritavad teemad:
  - T041, Töökindlate sardsüsteemide disain , Ubar,Raimund

- SA Eesti Teadusfondi grandid:
  - ETF8478, Riistvara funktsionaalne verifitseerimine ja silumine, Jenihhin Maksim
  - ETF7894, Süsteemitesti meetodid keerukatele trükkplaatidele, Jutman Artur
  - ETF7483, Isediagnoosivad digitaalsüsteemid, Ubar Raimund

- Ettevõtluse Arendamise SA eeluuringud:

- F11007, EAS eeluuring - Eeluuring mikroelektroonika kiipide tõrkekindlate 3D-arhitektuuride rakendusuuringule 7. raamprogrammi raames (3D-CHIP), Raik Jaan

- SA Archimedesega sõlmitud lepingud infrastruktuur:
- AP041,Töökindlate sardsüsteemide disain, Ubar Raimund
- ÜLTAP61, Integreeritud elektroonsed süsteemid ja komponendid (SARS2), koordineerib elektroonikainstituut
- ÜLTAP15-3, Mikro- ja nanostruktuursed sardsüsteemid ja komponendid (SARS3), koordineerib elektroonikainstituut

- Eesti tippkeskused:
- TAR8077, Integreeritud elektroonikasüsteemide ja biomeditsiinitehnika tippkeskus, Raimund Ubar

- EL Raamprogrammi projektid:
- VFP382, Centre of research excellence in dependable embedded systems, Jervan Gert
- VFP443, European Union's 7th Framework Programme IST collaborative project DIAMOND, Diagnosis, Error Modelling and Correction for Reliable Systems Design, Raik Jaan

- Välisriiklikud lepingud:
- VERT403, European Thematic Network for Teaching, Research and Innovations in Computing Education (ETN TRICE), Sudnitsõn Aleksander
- VERT422, Enhancing Lifelong Learning for the Electrical and Information Engineering Community - ELLEIEC, Jervan Gert

2.8 Struktuuriüksuse töötajate poolt avaldatud sihtfinantseeritava teadusteema taotlemisel arvestatavad eelretsenseeritavad teaduspublikatsioonid *(ETIS klassifikaatori alusel 1.1, 1.2, 1.3, 2.1, 2.2, 3.1, 3.2, 3.3, 4.1 ja 5.1).*

1.1

Mihhailov, D.; Sklyarov, V.; Skliarova, I.; Sudnitson, A. (2011). Acceleration of Recursive Data Sorting over Tree-based Structures. Electronics and Electrical Engineering, 7(113), 51 - 56.

Sagahyroon, F.; Aloul, A.; Sudnitson, A. (2011). Using SAT-Based Techniques in Low Power State Assignment. Journal of Circuits Systems and Computers, 20(8), 1 - 14. [ilmumas]

1.2

Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund; Viilukas, Taavi; Fujiwara, Hideo (2011). An Approach for Verification Assertions Reuse in RTL Test Pattern Generation. J. of Shanghai Normal University (Natural Sciences), Vol. 39(No 5), 441 - 447.

Ivask, Eero; Devadze, Sergei; Ubar, Raimund. (2011). Distributed Fault Simulation with Collaborative Load Balancing for VLSI Circuits. Scalable Computing: Practice and Experience, Vol 12(No 1), 153-163

Kostin, Sergei; Ubar, Raimund; Raik, Jaan; Brik, Marina (2011). Hierarchical Physical Defect Reasoning in Digital Circuits. Estonian Journal of Engineering, 17(3), 1 - 15.

Tagel, M.; Ellervee, P.; Hollstein, T.; Jervan, G. (2011). System-level optimization of NoC-based timing sensitive systems. Estonian Journal of Engineering, 17(2), 158 - 168.

2.2

Ubar, Raimund; Vierhaus, Theo; Raik, Jaan (2011). Design and Test Technology for Dependable Embedded Systems. USA: IGI Global [ilmumas]

Ubar, Raimund; Raik, Jaan; Vierhaus, Heinrich Theodor (2011). Design and Test Technology for Dependable Systems-on-Chip. USA, Hershey - New York: Information Science Reference, IGI Global

3.1

Viilukas, Taavi; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund; Baranov, Samary (2011). Automated Test Bench Generation for High-Level Synthesis flow ABELITE. Proceedings of IEEE East-West Design & Test Symposium 2011 (1 - 6). Sevastopol, Ukraine: IEEE Computer Society

Tsertov, Anton; Jurman, Artur; Ubar, Raimund; Devadze, Sergei (2011). Board-Level Modeling for PCB Testing. Proceedings of 14th Euromicro Conference on Digital System Design (1 - 6). Oulu, Finland: IEEE Computer Society

Tagel, M.; Ellervee, P.; Hollstein, T.; Jervan, G. (2011). Communication modelling and synthesis for NoC-based systems with real-time constraints . IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems 2011 (237 - 242).IEEE

Raik, J; Rannaste, A; Jenihhin, M; Viilukas, T; Fujiwara, H; Ubar, R (2011). Constraint-Based Hierarchical Untestability Identification for Synchronous Sequential Circuits. Proceedings of IEEE European Test Symposium, (1 - 6).IEEE Computer Society Press

Ubar, Raimund; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim (2011). Diagnostic Modeling of Digital Systems with Multi-Level Decision Diagrams. Design and Test Technology for Dependable Systems-on-chip (92 - 118). USA, Hershey - New York: IGI Publishing

Ubar, Raimund; Devadze, Sergei (2011). Fast Parallel Fault Reasoning in Digital Circuits. Design and Test Technology for Dependable Systems-on-chip (310 - 335). USA, Hershey - New York: IGI Publishing

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund; Ellervee, Peeter (2011). Fast RTL Fault Simulation Using Decision Diagrams and Bitwise Set Operations. Proceedings of 26th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (1 - 6). Vancouver, Canada: IEEE Computer Society

Ubar, Raimund (2011). Fault Simulation and Fault Injection. Design and Test Technology for Dependable Systems-on-chip (266 - 267). USA, Hershey - Nerw York: IGI Publishing

Jutman, Artur; Devadze, Sergei; Aleksejev, Jevgeni (2011). Invited paper: System-Wide Fault Management based on IEEE P1687 IJTAG. 6th IEEE Workshop on Reconfigurable Communication-centric Systems-on-Chip, Montpellier, France, June 20-22, 2011 (1 - 6).IEEE Computer Society

Hinrikus, H.; Bachmann, M.; Lass, J.; Tuulik, V.; Ubar, R. (2011). Method for Testing the Brain . Jobbagy, Akos (Toim.). 5th European Conference of the International Federation for Medical and Biological Engineering 14 - 18 September 2011, Budapest, Hungary (1198 - 1201).Springer

Guarnieri, V; Hantson, H; Raik, J; Jenihhin, M; Bombieri, N; Pravadelli, G; Fummi, F; Ubar, R (2011). Mutation Analysis for SystemC Designs at TLM. 12th IEEE Latin-American Test Workshop Proceedings (1 - 6). Porto de Galinhas, Brasiilia: IEEE Computer Society Press

Ubar, Raimund; Raik, Jaan; Vierhaus, Theo (2011). Preface. Design and Test Technology for Dependable Systems-on-chip. Design and Test Technology for Dependable Systems-on-chip (XX - XXVI). USA, Hershey - New York: IGI Publishing

Jutman, Artur; Aleksejev, Igor; Raik, Jaan (2011). Sequential Test Set Compaction in LFSR Reseeding. Design and Test Technology for Dependable Systems-on-Chip (476 - 493). Hershey - New York: Information Science Reference IGI Global

Jutman, A; Ubar, R; Devadze, S; Shibin, K; Rosin, V (2011). Trainer 1149: a Boundary Scan Simulation Bundle for Labs (Best Paper). Proceedings of 18th International Conference Mixed Design of Integrated Circuits and Systems - MIXDES (1 - 6).TU Gliwice

Jenihhin, M.; Raik, J.; Fujiwara, H.; Ubar, R.; Viilukas, T. (2011). An Approach for Verification Assertions Reuse in RTL Test Pattern Generation. In: Proceedings of the IEEE 11th Workshop on RTL and High Level Testing (WRTLT'10) : IEEE 11th Workshop on RTL and High Level Testing (WRTLT'10), Shanghai, China, December 5-6, 2010,. , 2011, 1 - 6. [ilmumas]

Robal, T.; Kann, T.; Kalja, A. (2011). An ontology-based intelligent learning object for teaching the basics of digital logic. In: 2011 IEEE International Conference on Microelectronic Systems Education (MSE): Microelectronic Systems Education (MSE) Conference, 5-6 June 2011, San Diego, CA, USA. [Los Alamitos, CA]: IEEE Computer Society, 2011, 106 - 107.

Mihhailov, D.; Sklyarov, V.; Skliarova, J.; Sudnitson, A. (2011). Application-specific hardware accelerator for implementing recursive sorting algorithms. The 2010 International Conference on Field-Programmable Technology (FPT'10), Beijing, China, Dec. 8-10, 2010. IEEE, 2011, 269.

Tagel, Mihkel; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert (2011). Contention aware scheduling for NoC-based real-time systems. Norchip 2011. IEEE Computer Society, 2011, 1 - 4.

Ubar, Raimund; Kostin, Sergei; Raik, Jaan (2011). Defect-Oriented Module-Level Fault Diagnosis in Digital Circuits. 14th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, April 13-15, 2011, Cottbus, Germany. IEEE Computer Society Press, 2011, 81 - 86.

Ubar, Raimund; Mironov, Dmitri; Devadze, Sergei; Raik, Jaan; Jutman, Artur (2011). Digital Logic Simulation with Compressed BDDs. In: Proceedings of 2011 IEEE International Conference on Computer Science and Automation Engineering (CSAE) : 2011 IEEE International Conference on Computer Science and Automation Engineering, Shanghai, China, 10 - 12 Jun, 2011. IEEE Computer Society, 2011, 105 - 109.

Jenihhin, Maksim; Gorev, Maksim; Pesonen, Vadim; Mihhailov, Dmitri; Ellervee, Peeter; Hinrikus, Hiie; Bachmann, Maie; Lass, Jaanus. (2011). EEG Analyzer Prototype Based on FPGA. In: Poceedings of IEEE 7th International Symposium on Image and Signal Processing and Analysis (ISPA): IEEE 7th International Symposium on Image and Signal Processing and Analysis (ISPA 2011), Dubrovnik, Croatia, September 4-6, 2011. IEEE, 2011, 101 - 106.

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2.9 Struktuuriüksuses kaitstud doktoriväitekirjade loetelu *(NB! struktuuriüksus lisab struktuuriüksuse töötaja juhendamisel mujal kaitstud doktoriväitekirjade loetelu)*

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