

DOCTORAL THESIS

Concept of Isolated Universal Bidirectional Converters for Electric Vehicle Applications with Improved Power Density

Parham Mohseni Dash Agholi

TALLINN UNIVERSITY OF TECHNOLOGY
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Declaration:

Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for doctoral or equivalent academic degree.

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TALLINNA TEHNIKAÜLIKOO
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**Parendatud võimsustihedusega
isoleeritud universaalsete kahe-suunaliste
muundurite kontseptsioon elektriautode
rakendustele**

PARHAM MOHSENI DASH AGHOLI



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List of Publications

The list of author's publications, on the basis of which the thesis has been prepared:

- [PAPER-I] P. Mohseni, O. Husev, D. Vinnikov, R. Strzelecki, E. Romero-Cadaval and I. Tokarski, "Battery Technologies in Electric Vehicles: Improvements in Electric Battery Packs," in *IEEE Industrial Electronics Magazine*, vol. 17, no. 4, pp. 55-65, Dec. 2023, doi: 10.1109/MIE.2023.3252265.
- [PAPER-II] P. Mohseni, O. Husev, M. Kasper and G. Deboy, "Design Optimization for Enhancing the Power Density and Efficiency for GaN-Based DC-DC Converter," in *IEEE Transactions on Industrial Electronics*, doi: 10.1109/TIE.2025.3552273.
- [PAPER-III] P. Mohseni, S. Pourjafar, O. Matiushkin, O. Husev and D. Vinnikov, "Isolated High Step-Up Current-Fed DC-DC Converter With Low Input Current Ripple and Wide Full-Soft-Switching Capability," in *IEEE Transactions on Industry Applications*, vol. 61, no. 4, pp. 6499-6510, July-Aug. 2025, doi: 10.1109/TIA.2025.3544985.
- [PAPER-IV] S. Pourjafar, H. Afshari, P. Mohseni, O. Husev, O. Matiushkin and N. Shabbir, "Comprehensive Comparison of Isolated High Step-up DC-DC Converters for Low Power Application," *IEEE Open Journal of Power Electronics*, vol. 5, pp. 1149-1161, 2024, doi: 10.1109/OJPEL.2024.3433554.
- [PAPER-V] P. Mohseni, O. Husev, D. Vinnikov, M. Kasper, and G. Deboy, "Novel Concept of Universal AC/DC-DC Onboard Battery Charger for Electric Vehicles," *2025 IEEE 7th International Conference on DC Microgrids (ICDCM 2025)*, Tallinn, Estonia, 2025.
- [PAPER-VI] P. Mohseni, O. Husev, D. Vinnikov, O. Matiushkin and N. V. Kurdkandi, "A Three-Phase Unfolding-Based PFC Topology with Two Inductors for Electric Vehicles Battery Charging," *2023 IEEE 64th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, Riga, Latvia, 2023, pp. 1-6, doi: 10.1109/RTUCON60080.2023.10413182.
- [PAPER-VII] P. Mohseni, O. Husev, D. Vinnikov, M. Kasper, G. Deboy, and N. V. Kurdkandi, "FCB-MPC-Based Cycle Skipping Control For Soft-Switched Isolated AC-DC Converter With Reduced Inductors In PFC Stage," *Proc. IEEE IECON – 51st Annual Conference of the IEEE Industrial Electronics Society, Madrid, Spain*, Oct. 2025.

Author's Contribution to the Publications

Contribution to the papers in this thesis are:

- [PAPER-I] Parham Mohseni, as the main author, reviewed and investigated references on state-of-the-art battery technologies utilized in EV applications, authored the paper, responded to reviewers' comments, and managed correspondence with the journal.
- [PAPER-II] Parham Mohseni, as the main author, carried out all design, calculation, and optimization processes, including PCB design, assembly, and laboratory tests. He also wrote the paper, responded to reviewers' comments, and handled correspondence with the journal.
- [PAPER-III] Parham Mohseni, as the main author, proposed the approach and completed theoretical calculations, PCB design, and laboratory work support, while also writing the paper, responding to reviewers' comments, managing correspondence, and organizing the paper for publication.
- [PAPER-IV] Parham Mohseni, as a coauthor, reviewed and provided comparison results while supporting PCB design and experimental validation.
- [PAPER-V] Parham Mohseni, as the main author, carried out theoretical calculations, design, optimization, PCB design and assembly, and laboratory testing for the proposed configuration. He also wrote the paper, presented it orally at the conference, and managed correspondence.
- [PAPER-VI] Parham Mohseni, as the main author, developed the proposed design, performed theoretical calculations, PCB design, coding and AC grid control, PCB assembly, and all laboratory tests. He also wrote the paper, managed correspondence, and presented it orally at the conference.
- [PAPER-VII] Parham Mohseni, as the main author, developed the proposed control design and simulations, performed theoretical calculations, and organized the paper for publication. He also wrote the paper, managed correspondence, and presented it orally at the conference.

1 Introduction

The landscape of electrical power distribution is undergoing a major transformation. For over a century, Alternating Current (AC) has been the dominant choice for grids, largely because its voltage can be easily stepped up or down through transformers, making long-distance transmission practical and cost-effective. However, with the rise of new technologies and energy needs, Direct Current (DC) is emerging as a strong competitor. High-voltage DC distribution has shown the potential to surpass AC systems in efficiency, particularly when dealing with modern energy applications and long-distance transmission.

A significant driver of this shift is the rapid expansion of renewable energy generation and large-scale energy storage. Most renewable sources—such as solar photovoltaics and batteries—are inherently DC in nature. Similarly, many of today’s end-use devices, from data centers to Electric Vehicles (EVs), also rely on DC operation. Feeding these systems through conventional AC networks often requires multiple conversion stages, which reduces efficiency and increases system complexity. By contrast, low-voltage DC distribution provides a more direct and efficient pathway, enabling better integration of renewables and storage while reducing unnecessary energy conversions [1]–[3].

Despite these advantages, a full-scale transition from AC to DC infrastructure is unlikely to happen in the immediate future. The global power grid is heavily dependent on existing AC networks, and replacing this infrastructure outright would be neither practical nor economically feasible. Instead, what is more realistic is the emergence of hybrid AC-DC systems, where both grid types coexist and complement one another. Over the next decade, such hybrid networks are expected to play a central role in meeting growing power demands and integrating renewable energy more effectively [4].

This convergence of AC and DC introduces new technical challenges. Systems and devices connected to the grid—particularly EV chargers—must be designed to function reliably in both environments. EV users already face inconveniences due to varying standards, connector types, and voltage levels across regions. As it is shown simply in Figure 1.1, depending on the location, charging may involve either a three-phase AC source or a DC supply, often requiring additional adapters or infrastructure-specific hardware. This not only complicates the charging process but also undermines the scalability and convenience of EV adoption.

1.1 Motivation of the Thesis

To address these challenges, there is a strong need for a Universal Onboard Charger (UOBC) capable of interfacing seamlessly with both AC and DC grids. Unlike traditional chargers, which are typically limited to a single input type, a UOBC would provide EVs with the flexibility to connect to any available power source without reconfiguration or external conversion equipment. Such versatility would greatly simplify the charging process, improve user convenience, and support broader adoption of electric vehicles across global markets.

Beyond convenience, technical performance requirements also motivate the development of UOBCs. Modern chargers must achieve high power density to fit within the constrained space of vehicles, while ensuring galvanic isolation for safety [5]–[8]. They must be adaptable to a wide range of battery voltages and support bidirectional power flow—allowing not only Grid-to-Vehicle (G2V) charging but also Vehicle-to-Grid

(V2G) energy transfer. This bidirectional capability positions EVs as active participants in the energy ecosystem, where they can provide grid support and enhance renewable energy utilization.

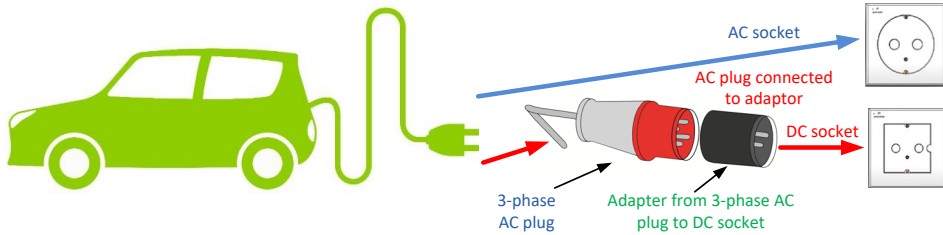


Figure 1.1 A streamlined representation of the suggested UOBC design.

Conventional Onboard Chargers (OBC), with their rigid designs and limited input compatibility, cannot meet these evolving demands. By contrast, UOBCs represent a forward-looking solution that bridges the gap between today's AC-dominant grids and tomorrow's DC-enabled infrastructure. Their adoption will be crucial for enabling the smooth coexistence of hybrid power networks, supporting renewable integration, and advancing the role of EVs in the broader transition toward sustainable energy systems.

1.2 Voltage and Power level of Battery Packs of EV Manufacturers

0 outlines the battery pack specifications of leading EV manufacturers. Recent advances have enabled packs delivering 50–150 kW, while Tesla achieves 200–250 kW fast charging with a 400 V pack. Most other manufacturers increase charging power by raising pack voltages to 600–800 V [PAPER-I].

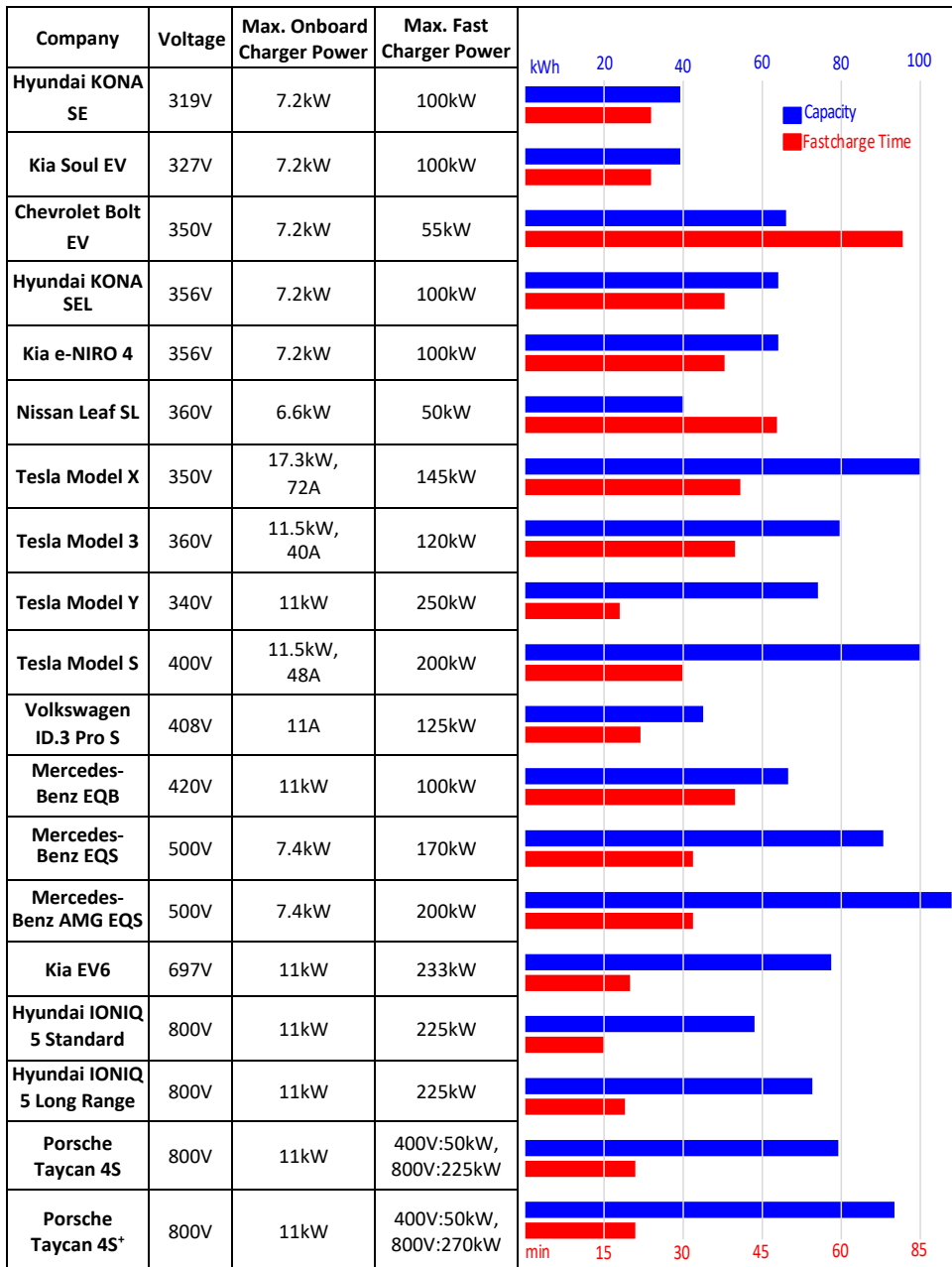
Since cable and busbar sizes cannot be scaled indefinitely, the most practical way to boost charging power without excessive heat is to raise voltage [9]–[10]. As shown in Figure 1.2, doubling pack voltage demonstrates this benefit. A 400 V pack (100 series $\times$ 4 parallel) is limited to 350 A by the CCS connector, while an 800 V pack (200 series $\times$ 2 parallel) remains at 300 A, still under the CCS limit. Thus, increasing voltage from 400 V to 800 V boosts charging power by about 71% without adding cells or capacity.

Higher voltage increases battery management system complexity, as 800 V systems require monitoring 200 cells instead of 100, but manufacturers such as Porsche, Hyundai, Kia, and Mercedes-Benz have adopted them for ultra-fast charging. The trade-off is higher per-cell current (150 A vs. 87.5 A at 400 V), which raises heat generation and potential degradation, necessitating stronger thermal management.

A major advantage of higher voltage is reduced conductor size and weight [11]–[12]. For example, a 350 kW charger at 350 V requires 1000 A and a 300 mm² cable weighing 16.1 kg for 5 m. At 800 V, only 438 A is needed, allowing a 125 mm² cable weighing $\sim$ 7 kg. While higher voltages require thicker insulation, the added material is negligible compared to copper mass.

Voltage increases, however, cannot continue indefinitely. Moving from 400 V to 800 V requires redesigning motors, converters, and inverters with higher-rated semiconductors (1.2–1.7 kV), adding size and cost. Still, even with $\sim$ 10% larger chargers or inverters, the overall impact is small since battery packs are 20–40 times larger, and system-level savings from higher voltage outweigh these increases.

Table 1.1 Voltage and Power Ratings of Onboard Battery Packs Across Leading EV Manufacturers [PAPER-I].



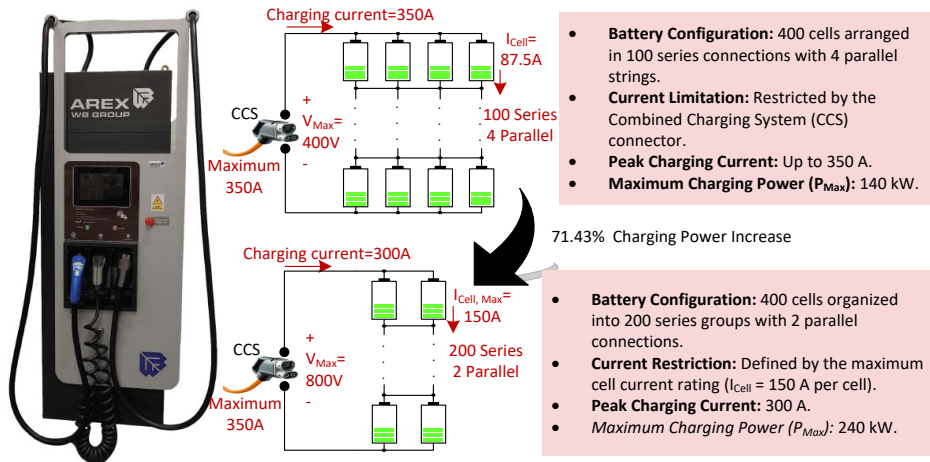


Figure 1.2 Enhancing the battery charging performance by raising the battery pack voltage from 400V to 800V [PAPER-I].

Table 1.2 Key Challenges and Solutions in Raising EV Battery Pack Voltage [PAPER-I].

Aspect	Challenge	Proposed Solution
Elevated voltage levels pose a higher risk of electrical arcing and potential electrocution.	Increasing the voltage of the battery pack may reduce passenger safety, particularly in the event of a crash.	✓ Enhance insulation thickness and increase spacing between conductors to minimize the associated risks.
The overall capacity of batteries connected in series is determined by the weakest individual cell.	When more cells are added in series, the performance of the weakest cell becomes increasingly influential.	✓ Parallel connection of low-capacity cells before series connection can reduce this issue, although not entirely. ✓ Implement an effective BMS to monitor and control each cell, ensuring balanced charge and discharge. ✓ Conduct predictive testing of battery cells before assembly into the pack. ✓ Regular inspection and replacement of weak cells are essential to sustain battery pack efficiency.
Increasing the voltage of the battery pack necessitates adjustments in circuits, parameters, and components used in EV power electronics such as the inverter, OBC, and DC-DC converter.	Capacitors in the DC voltage link must be able to withstand the elevated voltage levels, whereas most commonly used capacitors are rated for a maximum of 450 V.	✓ Series connection of specific capacitors may help, though this may lead to leakage currents. ✓ Use of film and ceramic capacitors can provide high capacitance but may increase system cost.
Higher battery voltage allows for increased switching frequency, which helps in reducing the size of magnetic components.	• Increased voltage can lead to higher dv/dt and more severe Electromagnetic Interference (EMI) problems. • The ability of semiconductors to handle high switching frequencies should also be considered.	✓ Apply proper shielding and fully resonant, soft-switching power conversion methods to mitigate EMI issues. ✓ SiC semiconductors, with their high-frequency switching capability, offer an effective solution. ✓ Adopting GaN devices for applications above 650 V is difficult, as such components are not widely available and would necessitate a complete redesign of the power electronic converters.

Table 1.2 lists the main challenges associated with raising battery pack voltage to 800 V and proposes potential solutions for each issue.

While some EV makers are pursuing breakthroughs in battery chemistry, others take a more practical route by reconfiguring cells in series and parallel to raise pack voltage. This approach addresses the key limitation of conductor sizing, since enlarging cable diameters would only increase heat during high-power charging.

The shift from 350 V to 800 V packs highlights a balance of benefits and trade-offs—enabling faster charging and better thermal performance. Overall, EV progress reflects steady, incremental advancements rather than disruptive leaps.

1.3 Aims, Hypothesis and Research Tasks

The main aim of this PhD research project is to develop and experimentally validate a universal, bidirectional onboard charging system for electric vehicles that supports seamless operation across various global AC and DC grid standards—including single-phase AC, three-phase AC, two-wire DC, and three-wire DC systems—without requiring hardware replacing. The proposed solution is intended to accelerate the transition from conventional AC infrastructures to hybrid AC/DC systems. The project focuses on achieving compactness and high-power density by employing wide-bandgap GaN transistors, enabling high-frequency operation and significantly reducing the size of magnetic components, especially the isolation transformer. A key goal is to reach acceptable efficiency and competitive power density compared to existing mainstream solutions. The final objective is to validate the proposed architecture through an 11 kVA hardware prototype, demonstrating stable operation with battery voltage of up to 800 V and achieving an efficiency above 95% with a power density of 4.3 kW/L (6.7 kW/L excluding the heatsink).

Hypothesis:

1. A reconfigurable bidirectional AC/DC-DC interface enables a UOBC compatible with single-phase AC, three-phase AC, and DC grids, supporting both V2G and G2V power transfer.
2. The limited availability of high-frequency ferrite core materials makes ferrite core transformers impractical in terms of power density for multi-kilowatt applications operating above 500 kHz.
3. Air-core transformers, by eliminating core losses, present a viable solution for multi-kilowatt, high-frequency applications beyond 500 kHz.
4. Cycle-skipping control enables high-frequency switching (above 500 kHz) with lower-frequency control (about 50 kHz), making high-frequency EV charging feasible.

Research tasks:

1. Review of existing battery technologies used in electric vehicles with a focus on voltage ranges along with existing onboard battery charger solutions and their comparative analysis in terms of universal applicability.
2. Propose the optimal power electronics topology that can link onboard batteries (300 V–800 V) with DC (350 V–700 V) or AC grid (single-phase and three-phase).
3. Design optimization of GaN-based converters in terms of thermal management, PCB layout, efficiency, and power density for several-kilowatt power levels and switching frequencies above 200 kHz.
4. Design and development of an isolated DC-DC stage operating above 500 kHz with a power density over 10 kW/L.
5. Overview, research, and development of the novel (if needed) control algorithms.

6. Design of the experimental setup and validation of the 11 kVA bidirectional UOBC, achieving over 95% efficiency and competitive power density, compatible with both AC (single-phase and three-phase) and DC (350 V–700 V) grids.

1.4 Research Methods

The methodology adopted in this thesis combines theoretical modeling, numerical simulations, and practical experiments. Theoretical analysis is conducted in the time domain using volt-second and ampere-second balance to describe converter operation. Simulation studies are performed in PSIM and MATLAB, which are both available at Tallinn University of Technology (TalTech University). Circuit and PCB design are carried out in Altium Designer, while DSP-based control coding is implemented using Code Composer Studio. Loss estimation is performed in two stages: first, by calculating conduction and switching losses from semiconductor datasheets, and second, by verifying these predictions with experimental measurements. A thermal imaging camera is used to capture device heating and validate real loss distribution, while overall efficiency is measured using a power quality and efficiency analyzer. Experimental validation is conducted on laboratory prototypes to confirm theoretical analysis and simulation results. These prototypes serve to test new converter topologies, control strategies, and unconventional circuit arrangements. The Power Electronics Research Laboratory at TalTech University provides modern infrastructure for this work, including digital oscilloscopes, function generators, power quality analyzers, microcontroller development platforms, and PCB prototyping and assembly tools, enabling full hardware and software realization of the proposed designs.

1.5 Contributions and Disseminations

The outcomes of the research have been disseminated through various academic and professional channels, including journal articles, conferences, oral presentations, symposiums, seminars, and doctoral schools. Throughout the course of the PhD, the author actively contributed to a total of 14 scientific publications. This includes four articles featured in reputable peer-reviewed international journals and one invention granted as a European patent. The other contributions were shared at internationally recognized IEEE conferences. The core content of the dissertation is built upon seven primary publications—comprising four papers published in leading IEEE journals and three presented at different IEEE international conferences.

Scientific novelties:

1. A novel interface suitable for universal applications with both AC (single-phase and three-phase) and DC (350 V–700 V) grids for EV battery charging application.
2. Comparative analysis in case of state of the art battery technologies for electric vehicles.
3. Definition of requirements for the optimization of ultra-high-frequency GaN-based DC-DC converters.
4. Definition of requirements for the optimization of ultra-high-frequency isolation transformers.
5. Synthesis and control of OBCs based on cycle skipping control for ultra-high switching frequency in the DC-DC stage.

Practical novelties:

1. Thermal management of GaN-based converters operating at ultra-high switching frequencies and multi-kilowatt power levels, while achieving high power densities.
2. Elimination of magnetic cores in the isolation transformer and GaN-based DC-DC converters by increasing the switching frequency, achieving power density and efficiency comparable to those using ferrite cores.
3. Inferior performance of available ultra-high-frequency ferrite cores compared to air-core transformers and inductors when operating at ultra-high frequencies and multi-kilowatt power levels.
4. Grid connection of an unfolding-based three-phase Power Factor Corrector (PFC) rectifier using only two inductors, as opposed to the conventional design requiring three inductors.

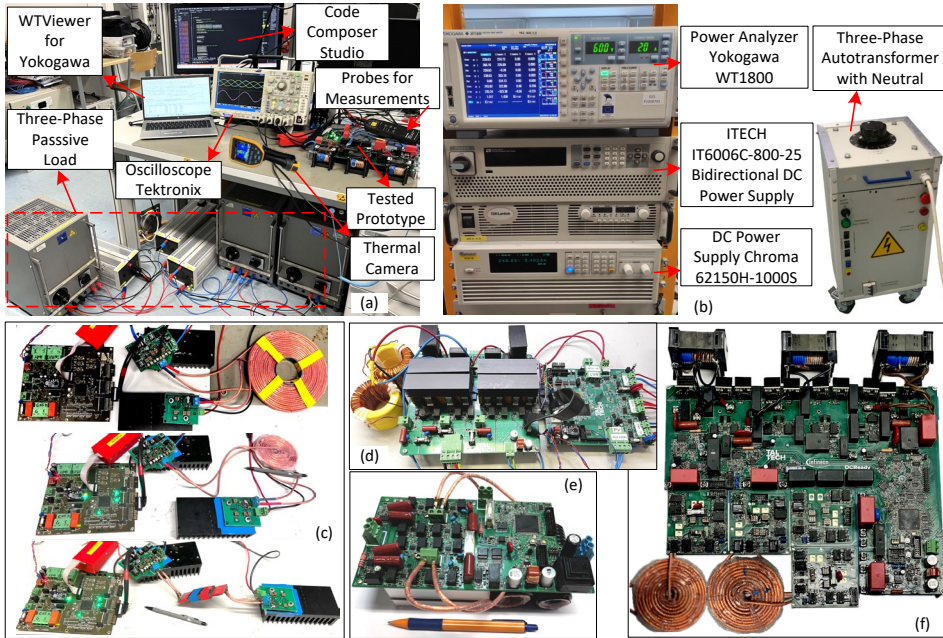


Figure 1.3 (a) Laboratory power electronics workspace, (b) power analyzer with DC sources for experiments (Unidirectional for input sources, bidirectional for battery) and autotransformer for grid connection, (c) GaN-based Isolated resonant converters for DC-DC stage optimization, (d) proposed unfolding based two inductor power factor corrector, (e) GaN-based Buck-Boost converter for GaN-based converters optimization, and (f) proposed bidirectional UOBC for single/three-phase AC and two/three-wire DC.

1.6 Experimental Setup and Instruments

The experimental work was carried out in the Power Electronics Laboratory of Tallinn University of Technology, where the test environment is illustrated in Figure 1.3a. A Tektronix MDO4034B-3 oscilloscope was employed to capture voltage and current waveforms of the passive components, using Tektronix P5205A high-voltage probes and Tektronix TCP0030A current probes for accurate measurements. The control software for the MCU (Texas Instruments TMS320F28379DPTPT) was developed in Code Composer Studio.

System efficiency was measured with a Yokogawa WT1800 power analyzer, supported by WTVIEWER software for remote monitoring. For input sources, a Chroma 62150H-1000S DC supply was used, while an IT6000C bidirectional programmable DC source emulated the battery system. In open-loop tests, a three-phase passive load was applied, whereas for grid-connected validation, an autotransformer provided the grid interface, as shown in Figure 1.3b.

Over the course of the PhD research, four experimental prototypes were designed, implemented, and tested, illustrated in Figure 1.3c–Figure 1.3f. The prototypes in Figure 1.3c and Figure 1.3e were developed to optimize GaN-based isolated DC-DC stage. Meanwhile, the setups in Figure 1.3d and Figure 1.3f represent the proposed universal onboard charger prototypes, validated for EV charging applications in terms of efficiency, power density, and practical feasibility.

1.7 Thesis Outline

Chapter 2 reviewed state-of-the-art OBC and isolated DC-DC designs, focusing on architectures that improve efficiency, power density, and enable universal hybrid AC/DC operation with bidirectional capability.

Chapter 3 presents two complementary OBC solutions for EVs: a cost-effective three-phase unfolding PFC rectifier that reduces inductors and sensors while maintaining grid performance, and a bidirectional UOBC supporting multiple AC/DC inputs with high-frequency SiC/GaN-based soft-switched DC-DC conversion for compact, efficient, and globally adaptable charging.

Chapter 4 explores methods to boost efficiency and power density in GaN-based converters. A top-side cooling strategy is validated, while interleaved with air-core inductors achieves soft-switching, and eliminates core losses. For isolated stages, resonant DC-DC topologies above 1 MHz are studied with ferrite and air-core transformers. Experimental results highlight trade-offs in loss, thermal behavior, and soft switching, offering practical design guidelines for compact, high-frequency, GaN based multi-kilowatt systems.

In Chapter 5, a feasible control approach based on cycle-skipping is proposed to enable MHz operation of the isolated DC-DC stage, ensuring soft switching and fine power regulation. Also, in this chapter, experimental validation was carried out on two prototypes: a 3.6 kW setup with the unfolding-based PFC and a 11 kW UOBC, achieving over 95% efficiency and 4.3 kW/L power density.

2 State of Art Onboard Battery Chargers and Isolated DC-DC Stages

The accelerating growth of EVs has underscored the limitations of conventional OBCs, which are typically designed for AC-only grids and struggle to accommodate today's diverse charging standards, connectors, and grid types. With AC infrastructure remaining dominant but low-voltage DC networks steadily expanding through integration of renewable energy, storage, and DC-native loads, future charging systems must be designed for hybrid AC and DC environments. This transition necessitates UOBCs capable of seamless operation across both grid types without external adapters or reconfiguration.

In addition to universality, state-of-the-art OBCs must satisfy stringent technical demands: galvanic isolation for safety and compliance, high power density to fit within limited vehicle space, and wide voltage adaptability to support the variety of EV battery systems now entering the market. Furthermore, bidirectional capability—enabling G2V charging and V2G energy return—is becoming essential, positioning EVs as active elements in the power system. Meeting these requirements has driven advances in isolated DC-DC converter stages, where modern soft-switching and high-frequency designs enable compactness, efficiency, and bidirectional operation.

This section reviews the state of the art in OBCs and isolated DC-DC converters, with emphasis on architectures and design strategies that support universality, high performance, and adaptability in hybrid AC and DC grid environments.

2.1 OBC Review

Research efforts reported in [13]–[17] (with [17] presented by Delta Electronics) have introduced advanced battery charging architectures often referred to as “universal” chargers. This designation primarily stems from their capability to handle a broad spectrum of battery voltage ranges, an increasingly important feature given the growing diversity of EV models and their powertrain requirements. These studies emphasize enhancing charging efficiency, incorporating soft-switching techniques, and ensuring compatibility with various battery voltages to meet the needs of different vehicle manufacturers.

However, this definition of universality remains mostly confined to the battery interface. Many of these solutions are developed as standalone or externally mounted chargers rather than as fully integrated onboard systems. Consequently, they lack the inherent capability to provide seamless bidirectional functionality with both AC and DC grids. Furthermore, they are not inherently designed to adapt to hybrid AC/DC charging environments without requiring hardware changes. In contrast, for onboard implementations—where each vehicle generally operates with a fixed battery voltage—the ability to connect efficiently to single-phase, three-phase, and DC power sources becomes a critical factor in achieving truly universal charging functionality.

OBCs for EVs can be classified by their underlying architecture. Single-stage designs (shown in Figure 2.1a) [18] (ETH Zürich) and [19] (Toyota) combine the AC-DC and DC-DC conversion stages into one step, reducing cost and saving space but increasing control complexity.

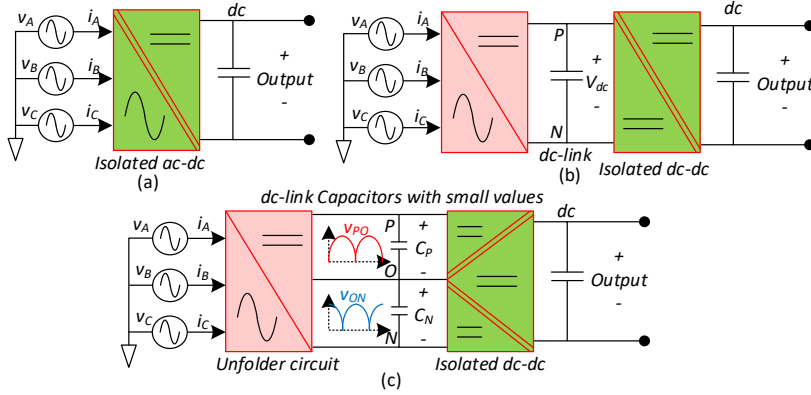


Figure 2.1 (a) Single-step AC-DC power conversion, (b) two-step AC-DC power conversion system, and (c) quasi-single stage unfolding system [20].

In these topologies, matrix-type PFC rectifiers are often used. They directly convert the low-frequency line-to-line AC input into High-Frequency (HF) AC, which is then applied to an isolation transformer. The transformer's secondary side subsequently rectifies this HF AC into a regulated DC output. These systems typically employ two series-connected switches configured as four-quadrant devices operating at high switching frequencies.

The main advantage of this approach is its single-stage power conversion, which allows for high efficiency and excellent power density. However, there are several challenges:

- Conduction losses: Each current path passes through two devices, requiring a trade-off between conduction losses and switching performance.
- Parasitic inductance: The back-to-back switch configuration increases loop inductance, which limits switching speed and demands careful design to prevent short circuits on the grid side or an open HF-link inductor during transitions.
- Output ripple: Without a large intermediate DC-link capacitor, these converters are more susceptible to low-frequency ripple, especially under unbalanced grid conditions.

Conversely, two-stage OBC architectures Figure 2.1b [21]–[22] separate the AC-DC and DC-DC conversion processes. While this approach generally increases size and conduction losses, it significantly simplifies control and remains the predominant structure for conventional AC-DC conversion systems. In a two-stage OBC architecture, the AC-DC stage employs a non-isolated PFC rectifier to convert grid AC to DC, which is then stabilized by an intermediate DC-link capacitor acting as an energy buffer. This buffered DC is subsequently processed by an isolated DC-DC converter to deliver a regulated output, while an LCL filter is typically incorporated at the input to minimize harmonic distortion and ensure compliance with emission standards. Key characteristics of this architecture include:

- Simplified control: The DC-link capacitor provides effective decoupling between stages, reducing control complexity.
- Stable output performance: The intermediate energy buffer enables consistent DC output, even during grid imbalances.
- Switching frequency limitations: High reverse-recovery and switching losses limit operation to below ~ 20 kHz, necessitating large magnetic components for filtering, which increases size and cost.

- Increased component count: Separate stage control and additional filter components add to implementation complexity.

Another technique, referred to as the Quasi-Single-Stage Unfolding method (illustrated in Figure 2.1c), enables the rectifier stage to function at the grid frequency without relying on high-frequency switching or Pulse-Width Modulation (PWM). Instead, it transfers the AC voltage to a gradually varying DC link. In this approach, all high-frequency switching tasks—such as PFC and power regulation—are carried out exclusively by the isolated DC-DC converter stage. This clear separation minimizes the filtering requirements on the AC side and streamlines the design of the rectifier front end [23].

OBCs can also be grouped into integrated [24]–[25] and non-integrated designs. Integrated OBCs reuse components from other vehicle subsystems, such as traction inverters or auxiliary DC-DC converters. This strategy improves overall efficiency and reduces component duplication but comes with the drawback of more challenging thermal management. In contrast, non-integrated OBCs operate as independent units, which simplifies design and maintenance at the expense of some efficiency advantages.

A further category is modular OBCs [25]–[28], which split power conversion across several smaller modules. This modularization enhances scalability, increases system reliability, and spreads thermal loads more evenly. It also provides the flexibility to adapt to various grid standards, including both single-phase and three-phase systems, making this approach attractive for EVs designed for global deployment. However, this flexibility often comes with higher control complexity and a larger component count. For example, [25] (Silicon Austria Labs) presents a compact bidirectional modular OBC based on a multiport series-resonant topology that supports single- and three-phase inputs as well as an integrated low-voltage output. A key feature of this converter is its ability to integrate both the Onboard charger (OBC), responsible for charging the high-voltage (HV) battery, and the low-voltage DC charger, which supplies 12 V auxiliary loads such as electric windows. The modular architecture consists of one or three interleaved single-phase totem-pole PFC stages paired with the primary side of a CLLC resonant converter, where the number of modules scales with the required power level. On the secondary side, the multi-winding transformer of the CLLC converter connects to the HV battery, while an additional secondary winding links to an interleaved buck stage that supplies the LVDC converter. Likewise, [26] (ETH Zürich) introduces a modular three-phase isolated rectifier built using matrix converters that can operate in either star (Y) or delta (Δ) configurations. This design supports a wide input voltage range, achieves Zero Voltage Switching (ZVS), and uses third-harmonic injection to increase output voltage in Δ -mode while optimizing device stresses for 650 V Si or GaN devices. These modular isolated matrix-based PFC rectifiers provide a single-stage isolated power conversion path from the three-phase grid to the DC bus, offering a compelling alternative to conventional phase-integrated rectifier architectures.

On the other hand, [27] describes a simplified single-stage electrolytic capacitor-free OBC aimed at achieving high efficiency and power density. Despite being marketed as “universal input,” it is limited to single-phase AC (100–240 V) and does not accommodate three-phase AC or DC connections. To overcome this limitation, [28] proposes a modular single-stage OBC that eliminates electrolytic capacitors and supports both single- and three-phase AC operation. In three-phase mode, it inherently enables DC charging, whereas in single-phase mode, one module is dedicated to power decoupling. However, this solution still lacks direct support for DC grid charging.

2.1.1 State of Art Isolated Single-Stage Onboard Chargers

For single-stage onboard chargers (OBCs), [31] (Infineon Technologies) (see Figure 2.2a) [29] introduces the isolated Y-Rectifier with series-resonant operation, a next-generation OBC architecture that unifies high-frequency isolation and supports both single- and three-phase AC inputs within a single bidirectional conversion stage. By utilizing 600 V GaN monolithic bidirectional switches, the isolated Y-Rectifier achieves a wide input-to-output voltage range and enables seamless bidirectional power transfer.

In another work, [26] (Seoul Tech and Hyundai) proposes a 3.7 kW single-stage AC-DC charger that incorporates an integrated magnetic structure, combining grid inductors and the transformer into a single magnetic core. This design reduces material costs, cuts core losses—particularly at lighter loads—improves efficiency by approximately 0.9%, and enhances power density by 11.1%. The approach also includes carefully optimized PCB winding arrangements to minimize AC losses and parasitic capacitances.

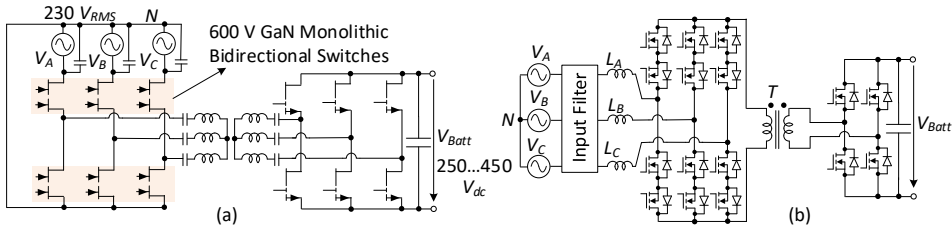


Figure 2.2 State of art isolated single-stage onboard chargers, (a) bidirectional single-stage EV onboard charger utilizing GaN monolithic bidirectional switches [31] (Infineon Technologies), (b) isolated high-efficiency matrix-based Dual Active Bridge (DAB) buck-boost rectifier [18] (ETH Zürich).

Similarly, [30] (GaN Systems) presents a compact 7.2 kW single-phase charger that leverages enhancement-mode GaN HEMTs for high efficiency and power density. The system is modular and can be scaled up to a 22 kW three-phase version by combining multiple units. Its DC-DC stage is designed to handle both power transfer and PFC, eliminating the need for bulky DC-link capacitors. Furthermore, the charger employs advanced modulation methods—such as dual and triple phase-shift control—to ensure soft switching while maintaining robust performance across a broad input voltage range (80–260 Vac) and output range (200–450 VDC).

In addition, [18] (ETH Zürich) (see Figure 2.2b) develops an 8 kW isolated matrix-type dual-active-bridge three-phase rectifier that delivers outstanding efficiency, with a peak of 99% and 98.7% efficiency even at 10% of the rated input voltage. The topology connects the high-frequency transformer directly to the three-phase grid in a matrix arrangement and uses 900 V SiC MOSFETs operating at 31 kHz with forced-air cooling. By integrating the series inductor into the transformer and applying an optimized soft-switching modulation strategy—analytical for Discontinuous Conduction Mode (DCM) and numerical for Continuous Conduction Mode (CCM)—the system achieves minimal Total Harmonic Distortion (THD) in grid currents.

2.1.2 State of Art Two-Stage Onboard Chargers

When examining state of art two-stage onboard charger (OBC) designs, [32]–[33] from Virginia Tech detail a 6.6 kW solution (see Figure 2.3a) specifically developed for 400 V battery systems. The first stage features a high-frequency interleaved totem-pole PFC circuit operating in critical conduction mode (CRM) at over 300 kHz, followed by a CLLC

resonant converter switching at 500 kHz. By implementing a variable DC link (500–850 V), the design improves efficiency by up to 1.3% and maintains a stable efficiency profile across different operating ranges compared to conventional fixed-voltage systems. This approach utilizes 1.2 kV SiC MOSFETs in the PFC and primary side, while the secondary employs 650 V GaN devices. Additional advancements include PI-based DC-link voltage control—maintaining the link at approximately twice the battery voltage—and PCB-based matrix transformers with integrated resonant inductors, which minimize size and losses. Further refinements in transformer materials, winding configurations, and layout increased the power density from 2.3 kW/L to 2.7 kW/L.

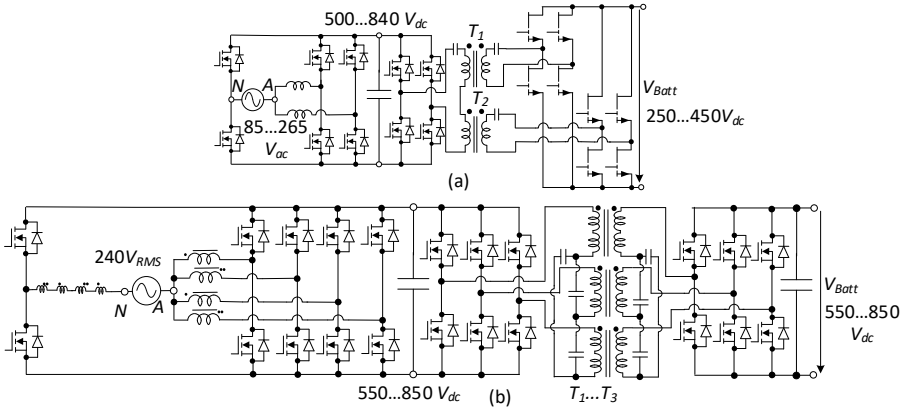


Figure 2.3 Isolated two-stage OBCs proposed by Virginia Tech, (a) Wide-bandgap-enabled high-efficiency, high-power-density bidirectional OBC [32]–[33], and (b) 11 kW high-frequency bidirectional OBC featuring integrated PCB-based magnetic components [34].

Virginia Tech later expanded this concept with an 11 kW charger optimized for 800 V batteries [34], which is shown in Figure 2.3b. This version incorporates a four-phase interleaved totem-pole PFC in CRM, where return path windings are combined with boost inductors, reducing the number of magnetic cores from eight to two while mitigating common-mode noise. The second stage consists of a three-phase CLLC resonant converter with a delta-connected primary for balanced current sharing and rapid startup. A variable DC link aligned with the battery voltage ensures that the CLLC stage runs precisely at resonance, maximizing conversion efficiency. Both stages use 1.2 kV SiC devices, operating at 350 kHz for the PFC stage and 500 kHz for the DC-DC stage. The DC-DC stage combines the transformer and resonant inductors into a single matrix transformer, reducing size and losses. This design achieves 98% efficiency per stage, 96% peak overall efficiency, and 3.2 kW/L power density.

In parallel, researchers from Nanjing developed bidirectional LLC-based solutions [35] (see Figure 2.4a) and [36] (see Figure 2.4b) to overcome the inherent limitation of conventional LLC topologies, where reverse power transfer is constrained due to the voltage gain dropping below unity. Their approach employs a variable DC link (400–700 V) alongside a dedicated gain-control method and digital regulation to manage high dv/dt oscillations, allowing reliable operation at high voltage and frequency. The design uses SiC MOSFETs switching at 300 kHz while simplifying the resonant network by removing one capacitor and one inductor compared to a CLLC stage, while adding parallel SiC devices to the totem-pole PFC. Their prototype demonstrated 95.6% efficiency and a power density of 3.4 kW/L [35]. A subsequent version [36] integrates a relay-based

mode-switching mechanism: during charging, the system functions as a standard two-stage converter, while during discharging, an auxiliary boost stage is added to elevate voltage for grid-tied operation. Although this slightly reduces efficiency and density, it enables full bidirectional power flow.

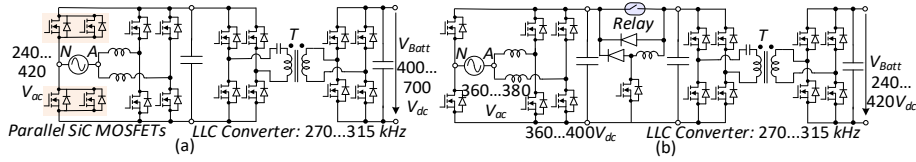


Figure 2.4 Isolated two-stage OBCs proposed by Nanjing, 6.6 kW SiC-driven bidirectional LLC charger operating at 300 kHz [35], (b) [36].

Texas Instruments developed a compact 6.6–7.4 kW bidirectional OBC [37]–[38] (see Figure 2.5a) featuring a two-phase totem-pole PFC paired with a full-bridge CLLC converter built around high-speed GaN devices. This design employs frequency and phase modulation for wide-range voltage regulation and uses advanced controllers with integrated Rogowski coil sensing for precise management of both stages, including synchronous rectification. With PFC operating at 120 kHz and the CLLC stage at up to 800 kHz, the design integrates the transformer and resonant inductors to save space. Combined with liquid cooling, this results in a power density of approximately 3.8 kW/L and a peak efficiency of around 96.5%.

Wolfspeed introduced a 22 kW bidirectional OBC [39]–[40] (see Figure 2.5b) using 1200 V SiC MOSFETs to achieve high efficiency and support a broad battery voltage range for both charging and discharging. The CLLC stage operates at 140–250 kHz, while the Active Front End (AFE) runs at 45 kHz, delivering over 97% efficiency in both power flow directions and accommodating both single-phase and three-phase inputs.

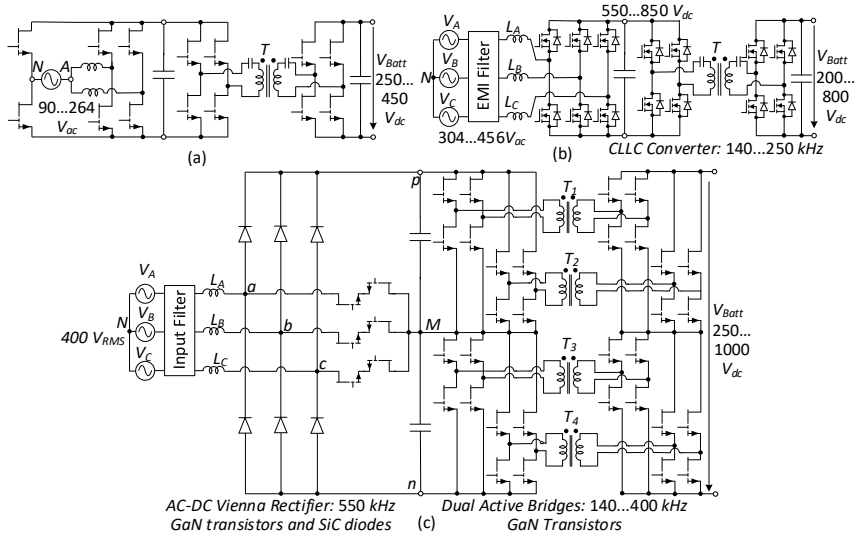


Figure 2.5 State of Art Isolated two-stage OBCs, (a) GaN-powered bidirectional onboard charger [37]–[38] (Texas Instruments), (b) SiC-enabled bidirectional EV charger [39]–[40] (Wolfspeed), and (c) advanced GaN-based onboard charger featuring ultra-high power density and broad output voltage capability [41] (Infineon) and [42] (ETH Zürich).

Finally, Infineon [38] and ETH Zürich [42] unveiled a 10 kW three-phase GaN-based OBC (see Figure 2.5c) offering a power density of 10 kW/L (9 kW/L reported by ETH Zürich). It supports output voltages from 250–1000 V and currents up to 25 A by combining a Vienna rectifier PFC with four DAB converters operating at 560 kHz and 140–400 kHz, respectively. Using GaN GIT HEMTs, SiC diodes, and isolated gate drivers, it achieves soft-switching operation with high efficiency.

However, although these solutions accommodate multiple voltage ranges and both single- and three-phase AC inputs, they remain limited to AC grid connectivity. None of these designs directly interface with DC distribution systems or renewable energy sources. As hybrid AC/DC grids continue to emerge, this shortcoming highlights the need for truly universal OBCs capable of seamless operation across both grid types, supporting bidirectional energy transfer and fully integrated onboard functionality.

2.2 Comparative Analysis of Conventional Three-Phase Two-Stage AC-DC Converter and Single-Stage Matrix Converter Architectures

This subsection presents a comparison between the conventional two-stage OBC architecture and the well-established single-stage matrix converter, which is recognized for achieving superior power density and efficiency. The comparison focuses on key parameters such as size, efficiency, and overall suitability for high-performance applications. The calculation methods and analysis for the comparison are detailed in [20].

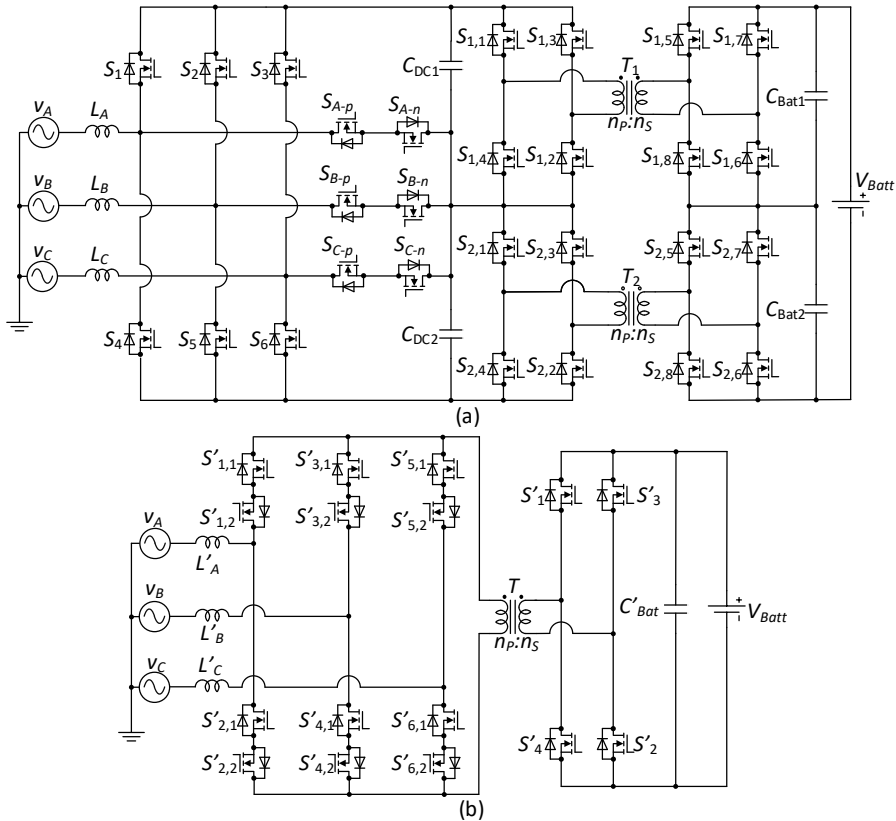


Figure 2.6 (a) Selected topology for the two-stage AC-DC architecture, and (b) Selected topology for the single-stage AC-DC architecture [20].

2.2.1 Definition of the Compared Structures

The conventional two-stage AC-DC OBC consists of a PFC rectifier followed by an isolated DC-DC converter. Three-level AC-DC rectifiers are widely used in high-power systems for lower switching losses, reduced voltage stress, and smaller grid filters. In the isolated bidirectional DC-DC stage, phase-shifted full-bridge and CLLC resonant converters are common, with CLLC preferred for operating at resonant frequency, enabling full soft-switching and lower losses. Full-bridge LLC designs suit higher power levels by reducing current stress and improving transformer use. For comparison, the reference system uses a three-level Vienna rectifier with two series-connected full-bridge CLLC converters (Figure 2.6a). Figure 2.6b shows the alternative single-stage three-phase high-frequency link matrix rectifier [18] and [43]–[47]. This design includes a grid filter, 3×1 matrix converter, isolation transformer, secondary full-bridge rectifier, and output capacitor. The matrix converter's six bidirectional switches directly convert low-frequency AC to high-frequency AC for the transformer primary.

2.2.2 Comparison Results

Figure 2.7 compares the performance of the traditional three-phase two-stage AC-DC converter and the single-stage matrix converter for EV OBC. Both topologies have similar physical volume and power density. However, conduction losses in the single-stage system are nearly double those of the two-stage design, while the two-stage incurs about four times higher switching losses.

Voltage stress analysis—under both ideal (calculated) and practical (device-rated) conditions—shows that the single-stage design experiences higher switch voltage stress in all cases. This directly impacts device selection for high-frequency operation. GaN transistors, with typical voltage ratings of 650 V or 900 V, are well-suited for the two-stage design, enabling higher switching frequencies, smaller passive components, and improved power density. The single-stage topology, however, exceeds these voltage limits, making GaN integration impractical and restricting its miniaturization potential.

Functionally, both converters can process three-phase AC into an 800 V DC output for EV battery charging while maintaining a high Power Factor (PF). Yet, the control complexity differs—the two-stage design primarily regulates power in the AC-DC stage, offering a simpler control strategy, whereas the single-stage matrix converter requires more complex modulation and control to manage power flow effectively.

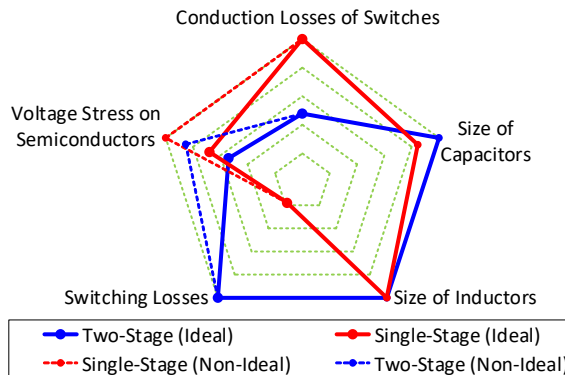


Figure 2.7 Comparative spider chart illustrating the key performance metrics of the two-stage versus single-stage converter topologies [20].

2.3 State of Art Isolated DC-DC Converters

Galvanically isolated DC-DC converters are highly advantageous since they ensure electrical separation between the source and load while accommodating large voltage variations. Established isolated designs are generally classified into two groups: voltage-fed and current-fed topologies.

Current-fed DC-DC converters offer several advantages, including lower input current ripple, smaller transformer turns ratio, improved efficiency, reduced voltage stress on output semiconductors, and immunity to shoot-through faults in switching devices. Another option is the impedance source converter, which blends the features of both voltage-fed and current-fed designs, thereby inheriting the strengths of each. For clarity, the characteristics of voltage-fed, current-fed and impedance source converters are compared in Table 2.1.

Table 2.1 Key characteristics comparison of Voltage-Fed, Current-Fed, and Impedance Source converters [PAPER-IV].

Feature	Voltage-Fed	Current-Fed	Impedance Source
Voltage step-up	No	Yes	Yes
Voltage step-down	Yes	No	Yes
Short-circuit exemption	No	Yes	Yes
Open-circuit exemption	Yes	No	Yes
Element for storing energy	One capacitor	One inductor	Minimum one capacitor and one inductor
Cascading capability of energy elements	No	No	Yes
Simplicity in control	Simple	Complex	Moderate

2.3.1 Current-Fed Isolated DC-DC Converters

Isolated DC-DC converters can be categorized into passive and active clamp types. Passive clamp converters require fewer switches but are limited by hard-switching losses. Active clamp versions—such as push-pull, half-bridge, and full-bridge—achieve ZVS turn-on and suppress voltage overshoot but are less attractive in low-power ranges due to higher cost and circuit complexity. Resonant bridge converters exploit parasitic elements to realize soft switching without clamp networks; however, they are prone to transformer DC bias, which increases the size requirement. 0 outlines the strengths and weaknesses of established isolated DC-DC converter designs.

Table 2.2 Advantages and drawbacks of conventional isolated DC-DC converters [PAPER-IV].

Topology	Advantages	Disadvantages
Flyback	✓ Simple design and low cost. ✓ Suitable for low to moderate power applications	• Limited power handling capability. • High peak currents and voltage stresses.
Isolated SEPIC	✓ Dual regulation: step-up & step-down. ✓ Reduced input current ripple.	• Complex control, higher components. • Limited for high power applications.
Forward	✓ High efficiency. ✓ Good for high power applications	• Limited voltage regulation range. • Needs tight control for reliability.
Push-Pull	✓ High-frequency operation capability. ✓ Good for high power applications.	• Complex control, higher components. • Transformer design can be challenging.
Half-Bridge	✓ Moderate complexity. ✓ Suitable for a wide range of power applications.	• Needs careful control to prevent spikes. • Limited for very low or very high power.
Full-Bridge	✓ High efficiency. ✓ Suitable for high-power applications	• Complex control, higher components. • Not ideal for low-power applications.
Resonant	✓ Reduced electromagnetic interference. ✓ Improved reliability due to soft switching.	• Complex control and higher cost. • High current stress on semiconductors.

Figure 2.8 presents the individual performance comparison of each converter. This analysis was conducted under specific operating conditions: an output power of 400 W, input voltage range of 20–50 V, fixed switching frequency of 50 kHz, and constant output voltage of 350 V. To maintain comparability, all converters were evaluated with identical output power and consistent dynamic switch configurations. [PAPER-IV] provides an in-depth analysis of isolated DC-DC converter topologies.

An isolated current-fed DC-DC converter with low voltage stress on the switches is presented in [PAPER-III]. Transformer leakage inductance enables soft switching for the all semiconductors over a wide range. The converter supports both resonant and non-resonant modulation. In the non-resonant case, phase-shift modulation reduces switch stress and only ZVS turn-on, while combining it with pulse-frequency modulation—or using resonant control—achieves full soft switching, enabling higher frequency operation, smaller passive components, and greater power density.

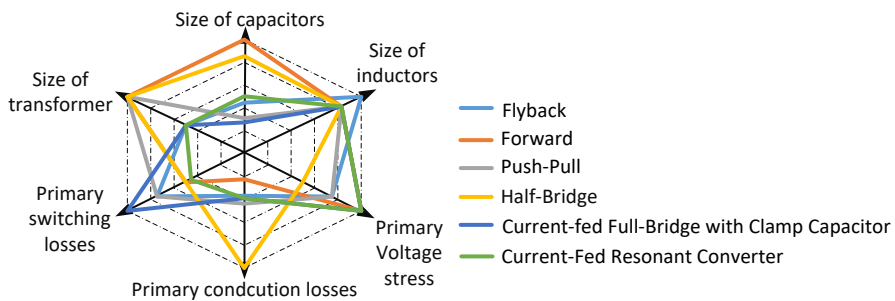


Figure 2.8 Overall comparison of isolated converter families based on key parameters [PAPER-IV].

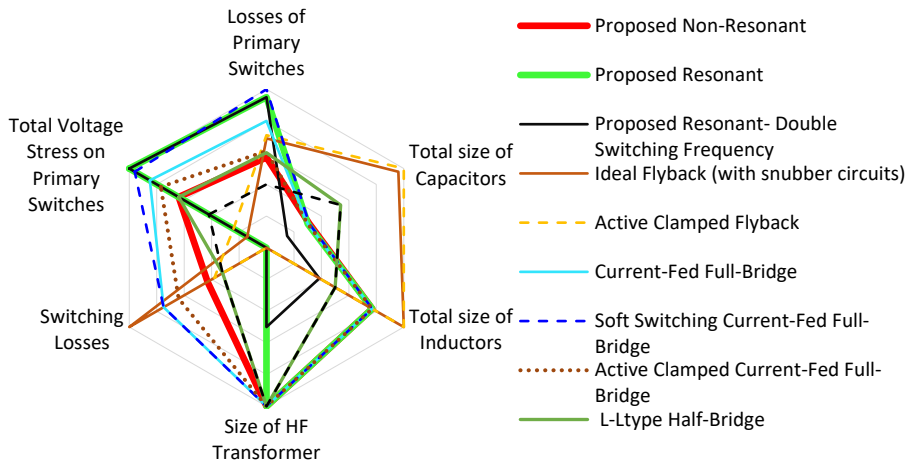


Figure 2.9 Comparison results between the proposed soft-switching current-fed design in [PAPER-III] and other current-fed isolated DC-DC structures.

The full soft-switching scheme provides ZVS turn-on and soft turn-off for the primary switches, eliminating switching losses. The modulation also doubles the effective frequency of the input inductor, halving its size, while an auxiliary circuit suppresses voltage overshoots caused by mismatch between the input inductor and transformer leakage inductance.

The design was validated with Si MOSFETs at 100–280 kHz, confirming feasibility, with strong potential for ultra-high-frequency operation using GaN. Comparative evaluation with Flyback, Current-Fed Full-Bridge, and L-L type Half-Bridge converters (Figure 2.9) considered passive component sizes, conduction and switching losses, and voltage stress. Results show that the non-resonant scheme excels in reducing switching losses and passive volume but is limited by turn-off losses at higher frequencies. In contrast, the resonant scheme supports full soft switching at elevated frequencies, allowing further downsizing and higher power density. Performance under doubled switching frequency (Figure 2.9) confirms these benefits in the resonant configuration.

2.3.2 Voltage-Fed Isolated DC-DC Converters

Research conducted at Virginia Tech has produced several high-frequency CLLC-based solutions operating around 500 kHz using SiC MOSFETs. One design in [48] introduced a single-phase 11 kW CLLC converter employing a three-core integrated matrix transformer to charge 800 V battery systems. By distributing the magnetic flux across three EI-cores instead of one, core losses were greatly reduced. These cores were combined with the resonant inductors into a six-leg matrix configuration, achieving 97.9% peak efficiency and a power density of 14.6 kW/L. In another study [49], a three-phase CLLC was followed by a four-channel interleaved buck stage to extend the output range from 200 V to 800 V. Although versatile, this addition lowered the prototype's efficiency by nearly 1% and reduced its power density to 6.1 kW/L.

Wolfsped reported a 22 kW CLLC resonant converter designed for 200–800 V outputs [50]. By coordinating with a variable DC-link PFC, the CLLC operated consistently near resonance across 135–250 kHz. Using 1.2 kV SiC MOSFETs in TO-247 packaging, the prototype achieved 98.5% peak efficiency and 8.0 kW/L.

Delta Electronics focused on universal charger concepts that accommodate a broad spectrum of EV powertrain requirements [17]. Their design combined an LCL-T resonant stage with a multilevel stacked half-bridge DC-DC structure. The stacked half-bridge was chosen to minimize capacitor current stress, particularly when using GaN devices at ≥ 800 V. Two secondary-side options were presented: a full-bridge rectifier with paralleled GaN switches for 400 V batteries, and a stacked half-bridge voltage doubler for 800 V systems. The 6.6 kW prototype achieved 98.2% peak efficiency and 7.3 kW/L power density.

2.4 Summary

In recent years, OBC research has made big strides in improving efficiency, power density, and flexibility, thanks to SiC and GaN devices, smarter modulation methods, and new integrated or modular designs. Many of these so-called “universal” chargers can already handle a wide battery voltage range and work with both single- and three-phase AC inputs, while also benefiting from soft-switching at high frequencies and compact magnetics. These advances mark an important step toward smaller, more efficient chargers that can meet the growing demands of modern EVs.

That said, most of today's OBCs are still heavily tied to AC grids. They rarely support direct connection to DC distribution networks that are becoming more common with renewables, storage, and DC-native loads. On top of that, many are built as external or add-on units rather than being fully integrated onboard. As a result, the idea of a truly universal charger—one that can seamlessly connect to both AC and DC grids, operate bidirectionally for V2G and G2V, and consolidate all conversion and control functions into

a single compact system—remains out of reach. Bridging this gap calls for the next generation of UOBCs, designed to meet both the technical and integration challenges of hybrid AC and DC infrastructures.

Moreover, Both single-stage and two-stage OBCs are similar in size and achieve high PF for 800 V EV batteries, but the two-stage offers higher efficiency and simpler control. With GaN at higher frequencies, the single-stage suffers from excessive voltage stress, while the two-stage benefits from smaller passives and better performance.

3 Proposed Unfolding-Based PFC Rectifier and UOBC

This section introduces two high-performance solutions for OBC applications in EVs, each targeting high efficiency, compact size, and cost reduction.

The first solution is an advanced three-phase unfolding-based PFC rectifier tailored for EV charging systems. It retains the same grid-side PFC performance as conventional three-phase designs but reduces the magnetic component count by using only two filter inductors instead of three, lowering cost and size. Grid current regulation is achieved by measuring the two inductor currents, removing the need for an additional current sensor found in traditional topologies. To validate its advantages, the proposed design is benchmarked against a conventional three-phase T-type configuration.

The second solution is a versatile, bidirectional UOBC capable of operating efficiently with various AC and DC grid configurations, including single-phase or three-phase AC inputs and two- or three-wire DC sources, without requiring hardware modifications. Leveraging SiC and GaN switches, the system operates at 100 kHz in the rectifier stage and 1 MHz in the isolated DC-DC stage, enabling significant downsizing of magnetic components—especially the isolation transformer—and improving thermal management. The DC-DC stage employs air-core transformers to handle high ripple currents without core losses or saturation, while soft-switching techniques minimize switching losses. This bidirectional capability supports both G2V and V2G operation.

Together, these two approaches offer complementary pathways for next-generation OBCs: the first focuses on simplifying and cost-optimizing the PFC stage, while the second delivers a globally adaptable, high-frequency, soft-switched, and magnetically optimized bidirectional charging system.

3.1 Three-Phase Unfolding-Based PFC Rectifier with Two Inductors

3.1.1 Fundamental Principles of Low-Frequency Unfolding Method

Figure 3.1 illustrates the concept of this method. In the configuration shown in figure, switches S_A , S_B , and S_C function as bidirectional switches. Before examining the requirements imposed on the DC–DC conversion stage, it is helpful to understand the working principle of the three-phase unfolding-based converter. As illustrated in Figure 3.1a, the initial stage—referred to as the *unfolder*—performs a straightforward rectification of the incoming three-phase AC voltages. Unlike a conventional active rectifier, this stage neither regulates the DC-link voltage nor shapes the input current waveform. It operates without PWM or any high-frequency switching, and the resulting DC-link is soft or floating, with its voltage naturally varying over time rather than remaining rigidly fixed.

A specific implementation of this concept, applied to electric vehicle battery charging with only two inductors for the PFC function, has been detailed in [PAPER-VI]. In this architecture, depicted in Figure 3.1b, a pair of filter inductors connects the unfolding stage to a 3-Level Asymmetrical CLLC Full-Bridge Inductive Power Transformer (3LA-CLLC-FB-IPT) isolated DC-DC converter, which processes power to the load. Figure 3.2 presents the idealized voltage and current waveforms corresponding to different intervals of operation, offering a clear illustration of the unfolding process.

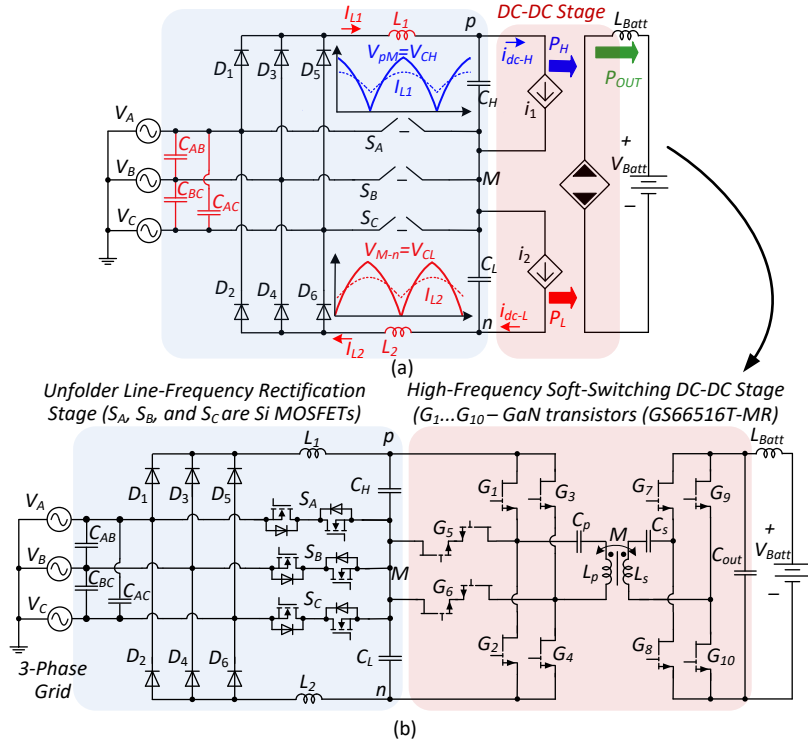


Figure 3.1 (a) Functional diagram of the proposed two-inductor three-phase rectifier topology employing an unfolded soft DC-link method, and (b) the 3LA-CLLC-FB-IPT converter as the DC-DC stage, integrated with the two-inductor three-phase unfolding PFC system [PAPER-VII].

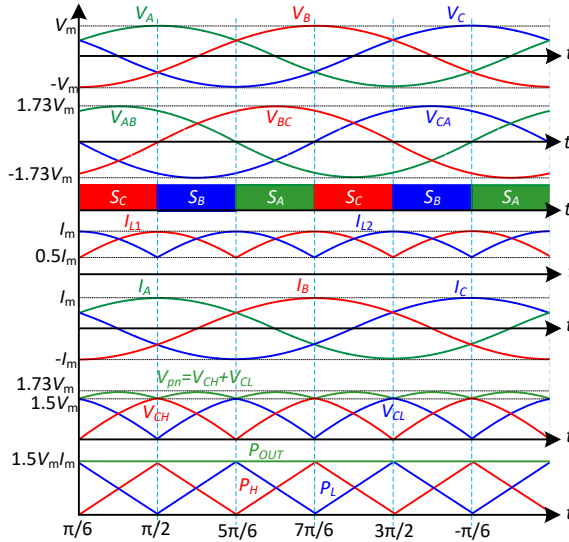


Figure 3.2 Main operating waveforms of the proposed unfolding structure [PAPER-VII].

The proposed three-phase unfolding rectifier, shown in Figure 3.1b, transforms the AC inputs V_A , V_B , and V_C into two floating DC-link voltages, V_{CH} and V_{CL} , across decoupling capacitors C_H and C_L . These capacitors not only smooth the high-frequency ripple from the isolated DC-DC converter, ensuring that the unfolding stage handles only low-frequency current, but they also draw reactive current from the AC source to maintain phase current balance.

From a control perspective, the rectifier operates as a current-source converter with six distinct operating regions, each defined by the instantaneous order of the three-phase voltages over a full grid cycle, as indicated and discussed in detail in [PAPER-VI]. The proposed three-phase, two-inductor unfolding-based rectifier uses inductors L_1 and L_2 as input current filters—replacing the three inductors found in conventional unfolding-based rectifiers. By regulating the current flow through L_1 and L_2 , as illustrated in Figure 3.2, the three-phase grid currents i_A , i_B , and i_C can be balanced with their respective phase voltages. This balance is achieved by independently managing the power transferred through two high-frequency DC-DC converters connected to the DC-link capacitors C_H and C_L .

3.1.2 Comparison Results of the Unfolding Rectifier Stage

To evaluate the effectiveness of the proposed converter, its performance was compared against the conventional three-inductor-based T-type three-phase unfolding structures [51]–[56], with respect to both physical size and efficiency. The comparison results are presented in the spider diagram of Figure 3.3.

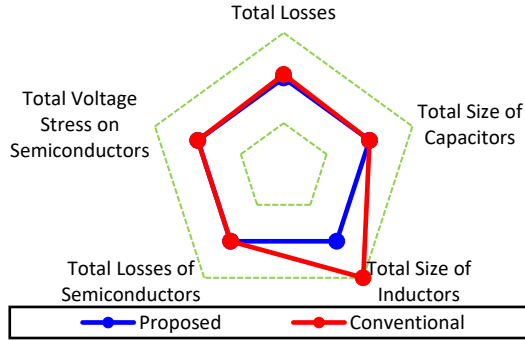


Figure 3.3 Spider chart comparing the performance metrics of the proposed structure with those of the conventional three-phase T-type unfolding structure [PAPER-VI].

A primary advantage of the proposed approach is its ability to deliver the same operational performance as the conventional three-inductor designs while requiring only two inductors. The maximum stored energy in each inductor, for both the conventional and proposed configurations, can be expressed as $E_L = 0.5LI_m^2$, where L denotes the inductance value of the filter inductors. Since in both topologies the peak inductor currents are equal to the maximum input current drawn from the grid, the maximum stored energy per inductor is identical. Consequently, the physical size of each individual inductor remains the same for both designs. However, because the proposed topology uses only two inductors instead of three, the total inductor volume is reduced to approximately 67% of that required by the conventional T-type structure.

Additionally, the proposed design achieves power PFC using only two current sensors to measure the currents through inductors L_1 and L_2 . In contrast, the conventional design requires three sensors—one for each inductor. This reduction in components not only increases the power density but also significantly lowers the overall system cost, further enhancing the appeal of the proposed converter compared to its conventional counterpart.

3.2 Architecture of the Proposed UOBC System

The proposed system, illustrated in Figure 3.4, presents a fully UOBC architecture with a bidirectional power converter that supports energy transfer in both charging and discharging directions. It is designed to interface with four types of inputs—three-phase AC, single-phase AC, two-wire DC, and three-wire DC—making it compatible with a wide range of charging infrastructures worldwide. The design is built around two main functional blocks: a front-end PFC or rectification stage, and a high-frequency isolated DC-DC conversion stage.

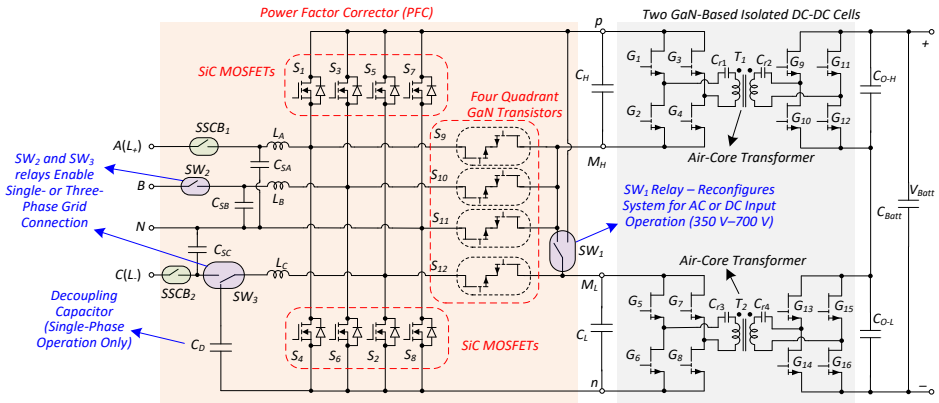


Figure 3.4 Configuration of the UOBC capable of handling both three- or single-phase AC and two- or three-wire DC inputs for electric vehicle applications [PAPER-V] and [55].

In the DC-DC section, high-speed GaN devices are used along with ZVS switching, enabling efficient operation at very high switching frequencies [57]–[59]. Unlike traditional ferrite-core magnetic components that limit frequency scaling and add core losses ([60], [PAPER-II], [61], and [62]), this system employs coreless magnetic elements, reducing losses and component volume while boosting power density.

The DC-DC modules can be dynamically configured in series or parallel to suit the target battery voltage. For lower voltage levels, the modules run in parallel to share current evenly, whereas for higher voltage needs, they are switched into a series arrangement. This flexibility is achieved without altering the connection between the rectifier and DC-DC stages.

Input-dependent configurations are handled automatically. For three-phase AC, the rectifier output is connected in series to the downstream modules. With single-phase AC, the modules are set in parallel for optimal current distribution. For DC inputs, the Configuration depends on voltage—350–380 V DC sources are paired with a parallel setup, while inputs between 700–750 V DC use a series arrangement. In the case of three-wire DC, the series configuration is always used. A smart control system monitors

input voltage and rectifier parameters to switch configurations seamlessly, requiring no user interaction.

The rectifier employs a T-type topology featuring switches S_1 – S_{12} and input filter inductors L_A , L_B , and L_C [63]. Switches S_1 – S_8 operate as bidirectional current controllers, while switches S_9 – S_{12} are GaN-based four-quadrant devices that enable true bidirectional operation. For safe DC grid interfacing, the design integrates Solid-State Circuit Breakers ($SSCB_1$ and $SSCB_2$) and suppression capacitors (C_{SA} , C_{SB} , C_{SC}), which protect against transients and stabilize operation.

An optional decoupling capacitor, C_D , is included for single-phase AC mode. This element balances power flow and suppresses ripple, making it possible to use long-life, high-reliability film or ceramic capacitors instead of electrolytic types, which benefits both durability and power density in compact designs [64]–[66].

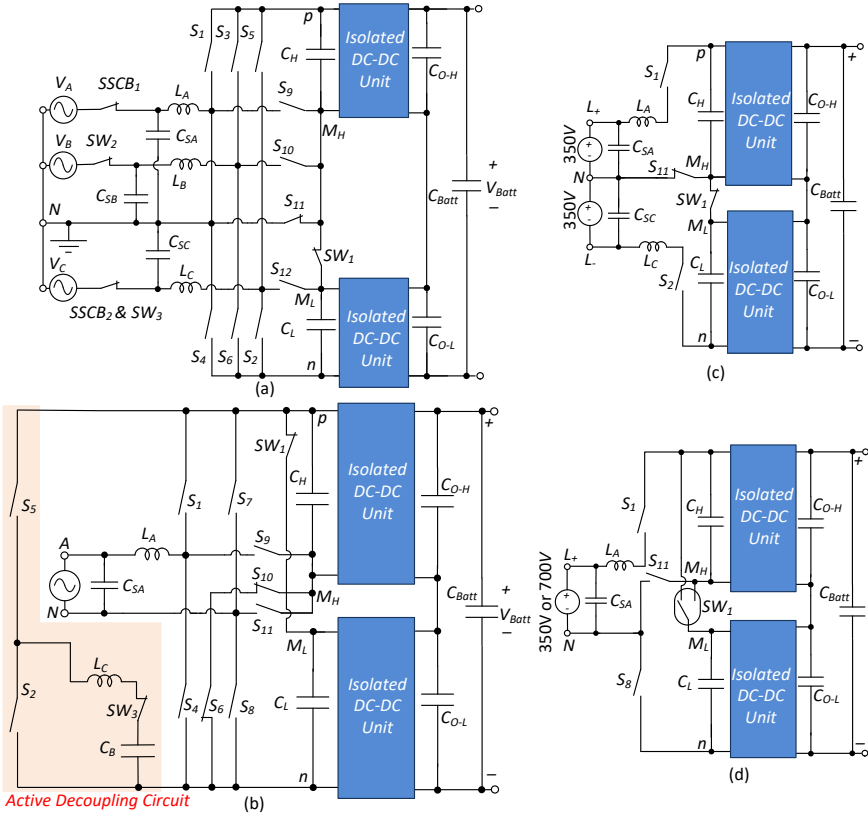


Figure 3.5 Equivalent circuit representations of the UOBC under various operating modes: (a) three-phase AC input, (b) single-phase AC input, (c) three-wire DC input, and (d) two-wire DC input. In the two-wire DC case, the DC-DC modules operate in parallel for input voltages of 350–380 V, and in series for input voltages of 700–750 V [PAPER-V] and [55].

The control framework supports various operating modes. In one mode—Vienna rectifier mode—the four-quadrant GaN devices perform high-frequency switching, while the rest operate at grid frequency to minimize switching losses.

A notable feature of the system is its use of reconfigurable electromechanical switches (SW_1 – SW_3), which adjust the power stage connections depending on the input source

and desired output voltage. SW_1 selects series or parallel operation of the DC-DC modules by linking capacitor terminals accordingly. SW_2 and SW_3 handle input source routing, enabling automatic transitions between three-phase AC, single-phase AC, and DC inputs. The rectifier's control unit governs these switches, ensuring smooth, efficient, and fully automated reconfiguration.

3.2.1 System Configurations and Operation Under Different Input Conditions

Three-Phase AC Input Mode

When the charger is connected to a three-phase AC supply—either with or without a neutral wire—it operates as shown in Figure 3.5a. In this setup, SW_2 engages to connect to phase B , while SW_3 disconnects the Active Power Decoupling (APD) capacitor and links phase C to the input. Each phase (A, B, C) is routed to its designated terminal, and if a neutral conductor is available, it may be connected to one of these points as needed.

Input inductors L_A, L_B , and L_C act as line filters to smooth current and meet grid harmonic standards. The main switching devices adjust their function based on power flow direction. Switches S_1 – S_6 serve as freewheeling paths (like diodes) during G2V charging, and act as actively controlled switches during V2G discharge, both under high-frequency modulation. Meanwhile, GaN-based four-quadrant switches S_9 – S_{12} (with S_{11} having a unique role) switch between primary high-frequency operation in rectification mode and auxiliary support in inversion mode.

Switch S_{11} specifically connects the neutral line to the midpoint of the DC link capacitors (M_H, M_L , or M), which helps maintain equal voltage sharing and reduces stress on the power stage.

The PWM control strategy—Under three phase AC operation is fully discussed in [PAPER-V].

Single-Phase AC Input Mode

When powered from a single-phase AC source, the charger operates as illustrated in Figure 3.5b. In this configuration, S_6 and S_{10} are turned on to connect the negative terminals of C_H and C_L , linking midpoint M_H to terminal n . At the same time, SW_1 is engaged to reconfigure the DC-link capacitors in parallel and connect them to the active power decoupling network. This setup helps counteract the inherent power pulsations present in single-phase inputs.

To further smooth power flow, SW_3 brings the decoupling capacitor C_D into the circuit. Switches S_2 and S_5 then operate at high switching frequency, working with inductor L_C to form a buck-type balancing stage [64], which actively regulates the energy exchange between the AC side and the DC-link, keeping the capacitor voltages stable.

The AC-DC conversion is handled by S_1, S_4, S_7 – S_9 , and S_{11} , which operate under high-frequency PWM to either rectify power during G2V charging or invert it during vehicle- V2G operation. This arrangement supports efficient bidirectional transfer under varying loads and input conditions.

The PWM switching strategy for the single-phase AC input operation is fully discussed in [PAPER-V].

Active Power Decoupling in Single-Phase AC Operation

In single-phase mode, when connected to the AC grid as illustrated in Figure 3.6a and Figure 3.6b, the system is assumed to operate with both voltage and current as clean sinusoids, achieving an ideal unity PF. Under these conditions, the instantaneous grid voltage $v_{AN}(t)$ and current $i_A(t)$ can be described by sinusoidal waveforms, with both

signals in phase due to the near-perfect PF. In the following equation, V_m and I_m denote the peak amplitudes of the voltage and current, and $\omega = 2\pi f$ is the angular frequency of the supply.

$$P_{AN}(t) = v_{AN}(t)i_A(t) = \underbrace{\frac{V_m I_m}{2}}_{P_{avg} = P_{Batt}} - \underbrace{\frac{V_m I_m}{2} \cos(2\omega t)}_{P_{Ripple}(t)} \quad (3-1)$$

The instantaneous power drawn from the grid, given by equation (3-1), consists of two components: P_{avg} – the constant average power transferred to the load and $P_{Ripple}(t)$ – a double-frequency oscillating term (twice the grid frequency) caused by the nature of single-phase power transfer, as shown in Figure 3.6a.

While the rectifier's DC output should ideally remain constant, this oscillating power term creates a mismatch between the instantaneous input and output power. The result is a second-harmonic ripple in the DC-link voltage.

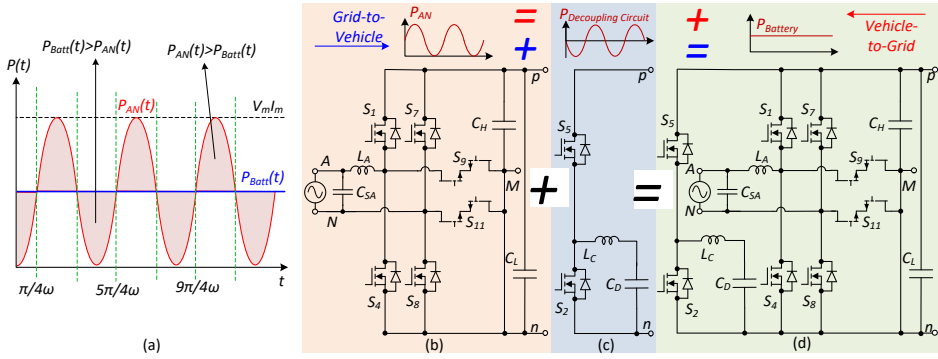


Figure 3.6 Simplified diagram of the single-phase AC configuration with parallel DC-link capacitors C_H and C_L : (a) power flow from the single-phase AC grid to C_H and C_L for battery charging, (b) single-phase rectifier stage, (c) decoupling circuit, and (d) complete single-phase system integrating the decoupling stage with DC-link capacitors C_H and C_L [PAPER-V].

To counteract this, the system employs an APD circuit across the midpoint of the DC-link capacitors (C_H and C_L). This APD stage either stores or releases energy in real time to neutralize the ripple component $P_{Ripple}(t)$, ensuring that only the constant power component reaches the load. By doing so, it prevents double-frequency voltage fluctuations on the DC-link that could otherwise degrade power quality, introduce harmonics, and disrupt control accuracy. The instantaneous power handled by the decoupling stage, $P_{Decoupling}(t)$, is depicted in Figure 3.6c and defined in equation (3-2).

$$P_{Decoupling}(t) = -P_{Ripple}(t) = -\frac{V_m I_m}{2} \cos(2\omega t). \quad (3-2)$$

When the decoupling capacitor C_D is engaged in this role Figure 3.6d, it acts as a high-speed energy buffer, dynamically compensating for power imbalances and maintaining the condition stated in equation (3-3). This ensures stable DC output voltage even during large power oscillations inherent to single-phase AC operation.

$$P_{AN}(t) = P_{Batt}(t) + P_{Decoupling}(t) \text{ for V2G; } P_{Batt}(t) = P_{AN}(t) + P_{Decoupling}(t) \text{ for G2V.} \quad (3-3)$$

Three-Wire DC Input Mode

As shown in Figure 3.5c, the charger can be directly linked to a three-wire DC distribution system by connecting the positive, neutral, and negative terminals to L^+ , N , and L^- , respectively. In this configuration, the system's control logic automatically sets the isolated DC-DC modules into a series arrangement, achieved via switches S_1 , S_6 , S_{11} , and SW_1 . This series setup provides balanced voltage distribution, maintains galvanic isolation, and preserves the bidirectional power flow capability, ensuring proper operation in both G2V and V2G modes.

Two-Wire DC Input Mode

When connected to a two-wire DC supply, as illustrated in Figure 3.5d, the charger adjusts its internal configuration according to the input voltage range. For lower voltages (around 350–380 V), the DC-DC modules are connected in parallel to increase current capability. For higher voltages (700–750 V), they are switched in series to handle the voltage level efficiently. This reconfiguration is managed by S_{11} and SW_1 , which control how the DC-link capacitors are interconnected.

In this mode, S_1 and S_8 remain continuously on to provide a direct path from the DC input to the power conversion stage, while all other switches remain off during steady operation. This minimizes unnecessary switching events, reducing losses and simplifying control requirements for constant-voltage DC input operation.

3.2.2 Isolated DC-DC Unit Analysis

Based on the discussion in Subsection 4.2.1, to reduce switching losses at a 1 MHz switching frequency, the isolated DC-DC stage is implemented as a conventional CLLC resonant converter. To mitigate high-frequency losses, the CLLC operates above its resonant frequency (Buck mode [67]: $f_s > f_r$) to ensure ZVS turn-on, rather than relying on $f_s > f_r$ for ZCS, based on Subsection 4.1.1.1 and [PAPER-II]. This approach addresses a key feature of GaN devices—significant capacitance energy remains even at zero current during turn-on, causing losses unless the voltage is also zero. Prior studies [68]–[70] show that GaN switches experience minimal turn-off loss but substantial turn-on loss, making ZVS far more valuable for efficiency. By enabling the resonant inductor current to fully discharge the switch capacitance before conduction begins, ZVS reduces switching losses and improves thermal performance at high operating frequencies.

The CLLC converter operates in two main intervals per half-cycle (with the second half repeating on complementary switches):

Power Transfer Mode (Figure 3.7b): Primary switches G_1 and G_4 conduct, delivering energy through the air-core transformer to the secondary side, where G_9 and G_{12} rectify. The magnetizing inductance L_m stores energy linearly and does not participate in the resonant exchange. Power transfer occurs when the primary resonant current exceeds the magnetizing current, with the secondary resonant current equal to their difference.

Dead Time Interval (Figure 3.7c): All primary switches are turned off to prevent shoot-through. During this phase, device output capacitances either charge or discharge naturally. G_1 and G_4 see voltage rise across their terminals, while G_2 and G_3 discharge toward zero volts—setting up ZVS for the next switching transition.

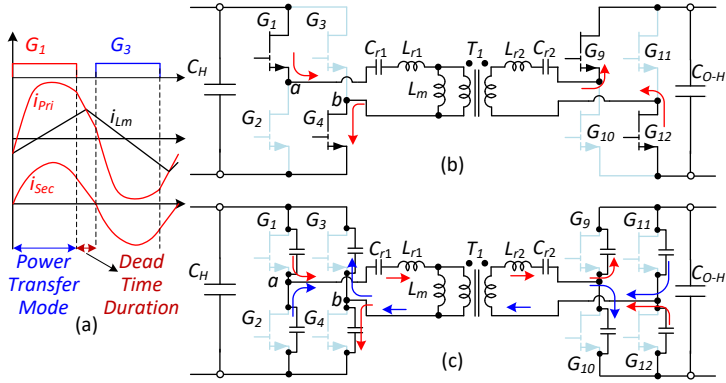


Figure 3.7 (a) Gate drive waveforms along with the primary current, magnetizing inductance current, and secondary current of the CLLC resonant tank, (b) operating power transfer mode of the CLLC resonant converter, and (c) dead-time period of the CLLC resonant converter.

3.2.3 Design Considerations of The Proposed System

Rectifier or PFC Stage Design

While optimized for three-phase AC input, the rectifier can also be configured for single-phase AC operation with minimal changes. The sizing of the input filter inductors (L_A , L_B , L_C) is based on the maximum allowable line current ripple ($\Delta i_{Lx,Max}$), with the minimum inductance calculated using (3-4).

$$L_x \geq \frac{V_{CH}}{4 f_{SW_PFC} \cdot \Delta i_{Lx,Max}} . \quad (3-4)$$

The peak input line current, needed for inductor and device selection, is obtained from (3-5) as a function of the battery charge/discharge power (P_{Batt}) and input PF:

$$I_{Lx,Peak} = 0.67 \times P_{Batt} / PF \times V_{AN,Peak} . \quad (3-5)$$

The modulation index (M), given by (3-6), defines the proportion of the available DC-link voltage utilized to produce the required AC waveform:

$$M = \frac{V_{CH} + V_{CL}}{\sqrt{3} V_{AN,Peak}} . \quad (3-6)$$

To choose suitable SiC MOSFETs and GaN transistors and estimate conduction losses, both average and RMS device currents are calculated via (3-7) and (3-8):

$$I_{S1-S6}^{Avg} = \frac{I_{Lx,Peak}}{2\sqrt{3}M}; I_{S9,S10,S12}^{Avg} = I_{Lx,Peak} \left(\frac{2}{\pi} - \frac{1}{\sqrt{3}M} \right) , \quad (3-7)$$

$$I_{S1-S6}^{RMS} = I_{Lx,Peak} \sqrt{\frac{4}{3\sqrt{3}\pi M}}; I_{S9,S10,S12}^{RMS} = I_{Lx,Peak} \sqrt{\frac{1}{2} - \frac{8}{3\sqrt{3}\pi M}} . \quad (3-8)$$

Switching losses for GaN devices (S_9, S_{10}, S_{12}) and SiC devices (S_1-S_6) are evaluated using (3-9), where rise/fall times for voltage (t_{rv} , t_{fv}) and current (t_{ri} , t_{fi}) are taken from device datasheets [71].

$$P_{SW} = \frac{1}{2} V_{CH} \times I_S^{Avg} \times f_{SW_PFC} \times (t_{rv} + t_{fi} + t_{ri} + t_{fv}) + \frac{1}{2} C_{d,eq} (V_{CH}) \cdot V_{CH}^2 \cdot f_{SW} \quad (3-9)$$

Finally, the RMS current stress on the DC-link capacitors (C_H and C_L) is calculated using (3-10), ensuring proper capacitor sizing for thermal and lifetime performance:

$$I_{CH}^{RMS} = I_{CL}^{RMS} = I_{Lx,Peak} \sqrt{\frac{5}{2 \times \pi \times M} - \frac{8}{4 \times M^2}}. \quad (3-10)$$

APD Stage Design

In this system, the decoupling capacitor (C_D) functions as an active element rather than a passive storage component. Working in conjunction with a controlled switching network, it compensates for the double-line-frequency (2ω) power oscillations by alternately absorbing and releasing energy in real time, as shown in Figure 3.6a.

Although actively controlled, its sizing still depends on parameters such as the system's power rating, allowable ripple voltage, and switching behavior. The peak ripple voltage across C_D can be estimated using (3-11) [72]:

$$\Delta V_{C_D,Max} = V_m I_m / 2\omega C_D V_{C_D}. \quad (3-11)$$

For a buck-type active decoupling configuration, the allowable ripple is constrained by $\Delta V_{C_D,Max} \leq 2V_{C_D}$, and the corresponding minimum capacitance required to maintain stable operation is given by (3-12):

$$C_D \geq V_m I_m / 4\omega V_{C_D}^2. \quad (3-12)$$

Losses in the decoupling stage arise from three main sources of conduction and switching losses in the semiconductor devices, resistive losses from the buffer inductor's Equivalent Series Resistance (ESR), and capacitor ESR-related losses. To evaluate these losses, key time-varying parameters are derived: the duty cycle of S_5 , $d_5(t)$, the voltage across C_D , $v_{CD}(t)$, and the current through the inductor L_C , $i_{LC}(t)$, as expressed in (3-13):

$$v_{CD}(t) \approx V_{C_D} - \frac{V_m I_m}{4\omega C_D V_{C_D}} \sin(2\omega t); \quad i_{LC}(t) = \frac{V_m I_m \cos(2\omega t)}{2v_{CD}(t)}; \quad d_5(t) = \frac{v_{CD}(t)}{V_{CH}}. \quad (3-13)$$

The RMS current ratings for L_C and C_D , necessary for conduction loss calculation, are determined using (3-14):

$$I_{LC}^{RMS} = I_{C_D}^{RMS} = V_m I_m / 2\sqrt{2} V_{C_D} \quad (3-14)$$

Similarly, RMS and average conduction currents for switches S_5 and S_2 are calculated via (3-15) and (3-16), which are then substituted into (12) to estimate their switching losses:

$$I_{S5}^{Avg} = V_m I_m / 2\pi V_{CH}; \quad I_{S5}^{RMS} = V_m I_m \sqrt{V_{C_D} V_{CH}} / 4V_{C_D} V_{CH}, \quad (3-15)$$

$$I_{S2}^{Avg} \approx \frac{V_m I_m}{\pi V_{CD} \sqrt{1 - \left(\frac{V_m I_m}{4\omega C_D V_{CD}^2}\right)^2}} - \frac{V_m I_m}{2\pi V_{CH}}; \quad I_{S2}^{RMS} \approx \frac{V_m I_m}{2V_{CD} \sqrt{1 - \left(\frac{V_m I_m}{4\omega C_D V_{CD}^2}\right)^2}} - \frac{V_m I_m}{4V_{CH}}. \quad (3-16)$$

DC-DC Stage Design Considerations

Achieving ZVS during turn-on requires that the active switch's drain-source capacitance is fully discharged, while the opposite leg's capacitance is charged up to the blocking voltage (V_S or V_{CH}). This transition relies on the energy stored in the primary or secondary inductances, with the turn-off current $I_{Turn-OFF}$ playing a decisive role.

As shown in Figure 3.7c, the charge redistribution process can be described using (3-17), which accounts for the device's equivalent output capacitance $C_{Q,eq}$ and any parasitic capacitances (C_{Par}).

$$0.5(L_m + L_{r1}) \cdot I_{Turn-OFF}^2 \geq 2C_{Q,eq}(V_S) \cdot V_S^2 + 0.5C_{Par} \cdot V_S^2, \quad (3-17)$$

The latter part of the equation (3-17), which originate from PCB layout and transformer geometry, are minimized in this design through careful high-frequency optimization and are therefore neglected.

At MHz-level switching frequencies, the air-core transformer's inductances are very small (on the order of μH), meaning $I_{Turn-OFF}$ must be relatively high to ensure complete discharge of the transistor capacitance.

To maintain ZVS, the dead time T_d between complementary switch transitions must be longer than the capacitor's charging/discharging interval $\Delta T_{SW-Transient}$. Assuming $I_{Turn-OFF}$ remains nearly constant over this brief period, (3-18) can be used to approximate the required timing:

$$\Delta T_{SW-Transient} \approx 4V_S C_{Q,eq}(V_S) / I_{Turn-OFF} \leq T_d. \quad (3-18)$$

this relationship emphasizes the balance between $I_{Turn-OFF}$, $C_{Q,eq}$, and T_d . The same conditions apply to the secondary side and must be satisfied for proper ZVS operation there as well.

For resonant analysis, the first harmonic approximation method is used, focusing only on the fundamental voltage and current components. The primary-referred output resistance is given by (3-19):

$$R_{eq} = \frac{4}{\pi^2} \cdot \frac{N_p^2}{N_s^2} \cdot \frac{V_{Batt}^2}{P_{Batt}}. \quad (3-19)$$

In a symmetrical CLLC converter, the voltage gain is expressed by (3-20), with parameters such as normalized frequency F_x , resonant frequency f_r , quality factor Q , and inductance ratio K defined in (3-21):

$$G(Q, K, F_x) = \frac{1}{\sqrt{\left(1 + \frac{1}{K} - \frac{1}{K \times F_x^2}\right)^2 + \left(Q \times F_x \left(2 + \frac{1}{K}\right) - \frac{Q}{F_x} \left(2 + \frac{2}{K}\right) + \frac{Q}{K \times F_x^3}\right)^2}}, \quad (3-20)$$

$$F_x = \frac{f_{SW-DC-DC}}{f_r}; \quad f_r = \frac{1}{2\pi \sqrt{L_{r1} C_p}} = \frac{1}{2\pi \sqrt{L_{r2} C_s}}; \quad Q = \frac{\sqrt{L_{r1}/C_p}}{R_{eq}}; \quad K = \frac{L_m}{L_{r1}}. \quad (3-21)$$

Figure 3.8 illustrates the gain variation versus normalized frequency for different Q values, using $K = 1.95$ from the prototype transformer.

Conduction losses for the GaN transistors, air-core transformer, and resonant capacitors are calculated using the RMS currents in (3-22) and (3-23):

$$I_{G9-G16}^{Avg} = I_{G1-G8}^{Avg} = P_{Batt} / 2V_{Batt}; \quad I_{G9-G16}^{RMS} = I_{G1-G8}^{RMS} = \pi P_{Batt} / 4\sqrt{2}V_{Batt}, \quad (3-22)$$

$$I_{Sec}^{Avg} = I_{Pri}^{Avg} = I_{Cr}^{Avg} = P_{Batt} / V_{Batt}; \quad I_{Sec}^{RMS} = I_{Pri}^{RMS} = I_{Cr}^{RMS} = \pi P_{Batt} / 2\sqrt{2}V_{Batt}. \quad (3-23)$$

Since the GaN devices achieve ZVS at turn-on but hard-switch at turn-off, only turn-off losses are considered. A strong gate drive shortens the saturation interval, ensuring the device turns off before the drain–source voltage rises significantly. The output capacitance C_{OSS} is charged by the device current, which limits overlap between voltage and current and reduces losses compared to standard MOSFETs [73]. The loss calculation for these conditions is given by (3-24):

$$P_{G1-G16}^{SW} = (I_{Turn-OFF} \times t_{fi})^2 f_{SW_DC-DC} / 12 [C_{OSS}(0) + C_{OSS}(V_{Batt}/2)] \quad (3-24)$$

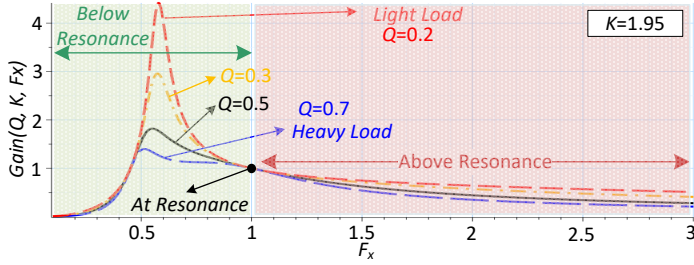


Figure 3.8 Voltage gain curve of the CLLC resonant converter for $K = 1.95$ with different Q values.

3.3 Summary

This section introduces two innovative OBC solutions for EVs, each addressing efficiency and power density in next generation charging systems.

The first solution is a three-phase unfolding-based PFC rectifier designed to simplify hardware while maintaining grid-side performance comparable to conventional topologies. By employing only two filter inductors instead of three, it reduces magnetic component count, cost, and size. Grid current control is achieved using the two inductor current measurements, eliminating the need for additional sensors. Comparative analysis with a traditional T-type rectifier shows clear improvements in cost-effectiveness and power density. The concept is validated through theoretical analysis, simulations at 7.2 kW, and a 3.6 kW experimental prototype, which are presented in [PAPER-VI] and Section 5, all confirming its practical viability.

The second solution is a UOBC capable of seamless operation with diverse input conditions, including single- or three-phase AC and both two- and three-wire DC grids, without hardware reconfiguration. Leveraging SiC and GaN devices, the rectifier stage operates at 100 kHz and the isolated DC-DC stage at 1 MHz, enabling significant downsizing of magnetic elements, particularly the isolation transformer. Air-core transformers are adopted to handle high ripple currents without saturation, while soft-switching minimizes losses and improves thermal management. An 11 kW prototype, which is analyzed in Section 5, validates the design, demonstrating stable and efficient operation across multiple modes, including bidirectional G2V and V2G functions.

Together, these approaches present complementary pathways for advancing OBC technology: the unfolding-based rectifier emphasizes cost and component reduction, while the UOBC highlights global adaptability, high-frequency operation, and bidirectional capability, establishing a foundation for compact, efficient, and versatile EV charging systems.

4 Design Optimization of GaN-based Converters for Enhancing the Efficiency and Power Density

4.1 Design Optimization in GaN-Based DC-DC Converter for Solar String Applications

This study examines thermal management for GaN-based power converters, focusing on a top-side cooling approach. It presents a design methodology covering heatsink configuration, TIM selection, and a thermal model for an interleaved Buck-Boost GaN DC-DC converter with a heatsink. A laboratory prototype is tested using two different TIMs, confirming the model's accuracy and real-world effectiveness.

Beyond thermal aspects, the work develops a high-power, high-efficiency, high-power-density DC-DC converter for solar string applications in DC microgrids. Negative Valley Current Mode (NVCM), or Critical Current Mode (CRM), is used for zero-voltage turn-on under wide range load. To counter CRM's large inductor ripple, multiple phases are interleaved, cancelling ripple at the switching frequency to reduce EMI filter size and boost efficiency. Recognizing ferrite-core limitations under high current and frequency, air-core inductors are adopted to eliminate core loss and saturation, improving power handling and density. The combination of NVCM and air-core inductors yields favourable trade-offs in switching loss, magnetic performance, and operating frequency.

Experimentally, the prototype demonstrates a peak efficiency of 99% and power densities exceeding 17.5 kW/L (50 kW/L without heatsink) and 6 kW/kg at 9 kW output using a natural convection heatsink—substantially outperforming prior work, which achieved 6.6–8.7 kW/L and efficiencies of 96–98.5% at significantly lower power levels. These results underscore the combined benefits of advanced thermal management, optimized circuit operation, and innovative magnetic design, providing a practical pathway toward more compact, efficient, and reliable GaN-based converters for renewable energy and other high-power applications. This part of this section is covered by [PAPER-II] and [74].

4.1.1 Operation Principle of the GaN-Based DC-DC Converter

The configuration in Figure 3.4a uses a modular interleaved 4-switch non-inverting buck-boost converter, where each phase is a non-isolated DC-DC cell referenced to the negative DC terminal. The module count N_{Module} balances cost, PCB area, inductive energy, and efficiency—more modules raise cost and area but reduce required inductive energy, allowing smaller inductors. Following [75] and based on analysis provided in [PAPER-II], two modules were selected, as shown in Figure 3.4b.

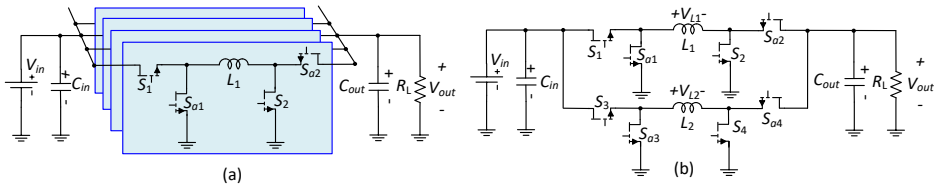


Figure 4.1 Schematic diagram of the modular interleaved DC-DC converter with a voltage source configuration, b) schematic of the two-phase voltage source interleaved DC-DC converter [PAPER-II].

Each module has two half-bridges—one for buck, one for boost—across inductor L . For $V_{in} > V_{out}$, only the buck half-bridge switches, and for $V_{in} < V_{out}$, only the boost half-bridge switches operate actively. The two modules run 180° phase-shift, shaping interleaved operation and combined behaviour.

4.1.1.1 Zero-Voltage Turn-On with Variable Frequency

A variable switching frequency control strategy is used to maintain ZVS turn-ON across the full operating range, eliminating turn-ON and C_{OSS} losses—critical for high-frequency converters. During each switching event, the inductor current I_L charges and discharges GaN-transistors drain–source capacitances. Therefore, ZVS operation requires full discharge of the main transistor’s drain–source capacitor, and full charge of the auxiliary transistor’s capacitor to V_S (V_S is equal to the output voltage in boost mode, and input voltage in buck mode). Achieving zero-voltage turn-on for the main transistor S requires precise control of the energy stored in inductor L during its turn-on transition. This control allows the parallel capacitors to fully discharge or charge as necessary, and the process can be accurately represented by the following model [57]:

$$0.5L \cdot I_{L-Valley}^2 \geq C_{Q,eq}(V_S) \cdot V_S^2 + 0.5C_{Par} \cdot V_S^2, \quad (4-1)$$

where $C_{Q,eq}$ is the main transistor’s charge-equivalent capacitance and C_{Par} is parasitic capacitance, here neglected via optimized PCB design. $I_{L-Valley}$ is the minimum negative inductor current. For reliable ZVS, dead time T_d must exceed $\Delta T_{SW-Transient}$ [57], estimated as:

$$\Delta T_{SW-Transient} \approx V_S (C_{Q,eq}(V_S) + C_{Q,eq,a}(V_S)) / I_{L-Valley} \leq T_d, \quad (4-2)$$

where $C_{Q,eq,a}$ is the auxiliary transistor capacitance.

The Variable Frequency Zero Voltage Turn-ON (VFZVTO) method adjusts switching frequency to set ripple in L_1 and L_2 so $I_{L-Valley}$ meets ZVS conditions. Total capacitance ($C_{Q,eq} + C_{Q,eq,a}$) defines $\Delta T_{SW-Transient}$, so T_d must be larger to avoid partial hard turn-ON.

Boundary Conduction Mode (BCM) achieves ZCS for main devices but retains C_{OSS} losses, given by:

$$P_{SW}^{C_{OSS} Loss} = Q_{OSS}(V_S) \cdot V_S \cdot f_{SW} = C_{Q,eq}(V_S) \cdot V_S^2 \cdot f_{SW}, \quad (4-3)$$

where f_{SW} is switching frequency and Q_{OSS} is stored C_{OSS} charge. Full elimination requires negative $I_{L-Valley}$. If average inductor current is positive, ripple must drive the valley below $-I_{L-Valley}$ to discharge capacitance during auxiliary turn-off. Excessively negative valley current, however, increases auxiliary turn-off and main switch turn-off losses.

To demonstrate this, Figure 4.2 presents the theoretical switching losses of the interleaved DC-DC converter for operating conditions of 20 A input current, 350 V output voltage, 450 V input voltage, and a switching frequency of 218 kHz. The converter uses GaN devices GS66516T for (S_{a1} – S_{a4}) and GaN devices GS66508T for (S_1 – S_4). As shown in the figure, with inductors above 14 μ H, the system operates under full hard-switching with high switching losses. At around 14 μ H (BCM), ZCS is achieved, but C_{OSS} losses remain. For inductor values between 12 μ H and 14 μ H, partial C_{OSS} reduction is achieved without full ZVS. Below 12 μ H, C_{OSS} losses are completely eliminated and full ZVS is achieved, but auxiliary turn-off losses increase sharply.

Reducing main switch losses lowers heat generation—critical for GaN devices due to limited thermal dissipation—so the trade-off between main and auxiliary switch losses should be assessed using datasheets. The variable switching frequency calculation for a target $I_{L-Valley}$ is completely discussed in [PAPER-II].

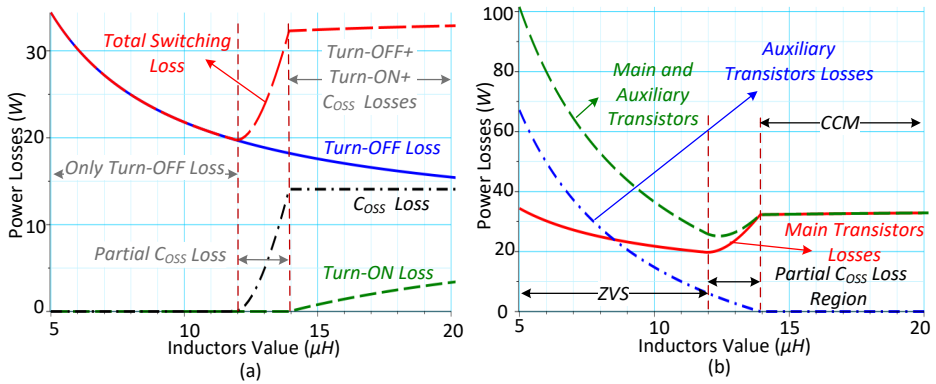


Figure 4.2 Calculated switching losses of the interleaved DC-DC converter evaluated over inductor values ranging from 5 μH to 20 μH across three operating regions. (a) Breakdown of the main switches' losses, including turn-on loss, turn-off loss, C_{oss} loss, and the total switching losses in the three regions. (b) Comparison of switching losses for the main transistors, auxiliary transistors, and the overall total switching losses [PAPER-II].

Low-inductance air-core inductors are preferred to improve efficiency, minimize conduction losses, avoid saturation at peak current, and eliminate ferrite core losses at variable frequencies. Accurate inductance measurement allows the controller for real-time frequency adjustment to maintain ZVS. For example, with $L = 12 \mu\text{H}$, $I_{L-\text{Valley}} = -2\text{A}$, $I_{\text{in}} = 20\text{A}$, and $V_{\text{out}} = 350\text{V}$, the optimal switching frequency over the input voltage range of 110–450 V is 18–304 kHz. Using GaN devices with air-core inductors eliminates core losses, removes frequency limitations, and maintains high efficiency across the entire range.

4.1.2 Appropriate Thermal Management Strategy Based on Power Level

The converter's power density depends on inductor size and heatsink selection, with effective heat dissipation essential for performance and reliability. Heatsink sizing is based on total transistor losses—conduction plus switching. The design uses eight transistors: S_1 – S_4 (main) and S_{a1} – S_{a4} (auxiliary). Main switches require high-speed switching, while auxiliary switches prioritize low conduction losses (low R_{DS}), so different transistor types are chosen. Accurate heatsink and TIM selection require each device's thermal resistance ($R_{\theta\text{JC}}$) and maximum power loss.

A top-side cooling approach with validated thermal modeling for the interleaved buck-boost GaN converter is detailed in [74]. The model accounts for losses from main, auxiliary, and continuously conducting transistors. In boost mode, conduction losses are constant for a given input current; in buck mode, they rise linearly with input voltage. Worst-case occurs at 450 V in buck mode, where S_1 and S_3 are main, S_{a1} and S_{a3} are auxiliary, S_{a2} and S_{a4} conduct continuously, and S_2 and S_4 remain OFF.

The one-phase thermal model in Figure 2 of [74] considers three top-side cooled GaN transistors sharing a natural convection heatsink; two-phase operation doubles losses and parallels resistances. For GaN transistors, the relatively small thermal pad area on the top surface makes the choice of thermal TIM critical for effective heat removal. Even with a well-designed heatsink, the overall cooling performance can be limited if the TIM is not appropriately selected. An unsuitable interface can prevent efficient heat transfer, meaning that high-performance heatsinks or active cooling systems may not deliver their full potential.

The thermal resistance of a TIM, measured from the transistor's top surface to the heatsink, can be easily estimated by considering the device's thermal pad area. Using the thermal impedance values provided in the transistor datasheets, the corresponding TIM thermal resistances for each device type can then be calculated by

$$R_{Thermal}^{TIM} (^{\circ}C / W) = \frac{\text{Thermal Impedance } (^{\circ}C \cdot \text{inch}^2 / W)}{\text{Thermal Pad Area } (\text{inch}^2)} \quad (4-4)$$

Considering the thermal network shown in Figure 2(b) of [74] and including the junction-to-case resistance of the transistors $R_{\theta JC}$ and the case-to-sink resistance of the TIMs $R_{\theta CS}$, the required heatsink thermal resistance for each device category—continuously conducting, main, and auxiliary transistors—can be determined using the expression provided in [74].

4.1.3 Power Density and Efficiency Optimization

Figure 4.3a shows transistors switching and conduction losses, inductor conduction losses, and total losses in buck mode for 220 kHz switching, 20 A input current, and 450 V input voltage (GS66516T for S_{a1} – S_{a4} , GS66508T for S_1 – S_4) versus the inductor value. At 14 μH , the converter operates in BCM (main transistors ZCS). Reducing inductor value increases negative $I_{L-Valley}$, lowering C_{OSS} losses and enabling ZVS, but also raising auxiliary transistors turn-off losses. Minimum main transistors switching losses occur at $\sim 12 \mu\text{H}$, with minimum total transistors switching losses at $\sim 12.5 \mu\text{H}$.

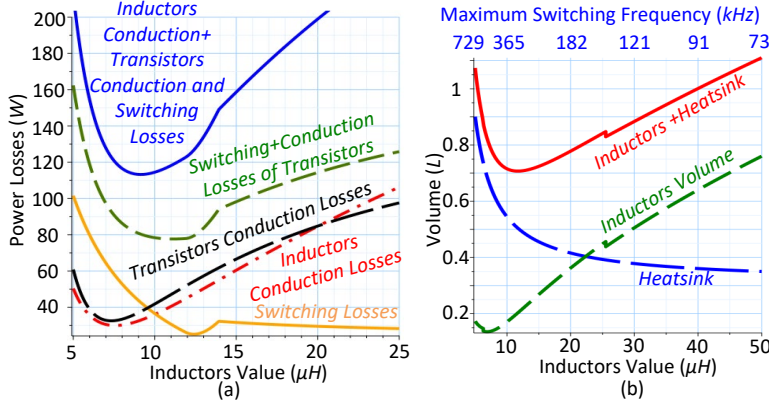


Figure 4.3 Impact of inductor value on losses and volumes, (a) Buck-mode losses at 220 kHz, $I_{in} = 20 \text{ A}$, $V_{in} = 450 \text{ V}$, (b) Inductor, heatsink, and total volumes [PAPER-II].

Transistors conduction losses are lowest near 7.5 μH but remain close to this minimum up to 12 μH , while switching losses rise sharply below 10 μH . Thus, $\sim 12 \mu\text{H}$ offers the best trade-off between switching and conduction losses, supporting both efficiency and thermal management for GaN devices. Inductor conduction losses are lowest near 8 μH and show minimal change up to 12 μH .

Figure 4.3b indicates that minimum inductor volume occurs at 7–8 μH , but the higher switching frequency at low inductance increases transistor losses and heatsink size. The lowest combined volume of inductors and heatsink is achieved at $\sim 12 \mu\text{H}$.

Figure 4.4 shows the converter's theoretical power density and maximum switching frequency plotted against efficiency. The peak power density of 12.2 kW/L, using a natural convection heatsink, occurs at an inductor value of 12 μH with a theoretical efficiency of 98.42%. While actual power density depends on heatsink design, airflow,

and environmental conditions, the results show that 12 μH provides the best trade-off between high efficiency and compact size [76]. Overall, larger inductors slightly improve efficiency, but 12 μH yields the best balance of high power density, acceptable efficiency, and manageable thermal requirements for GaN-based converters.

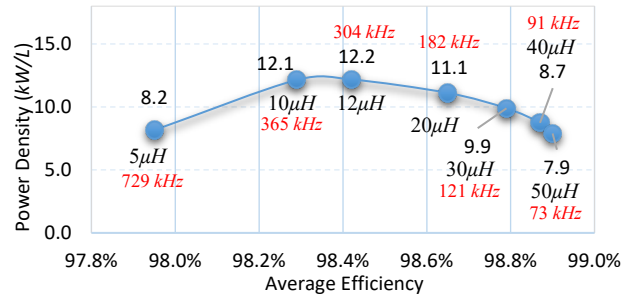


Figure 4.4 Theoretical power density and maximum switching frequency against the converter's average efficiency [PAPER-II].

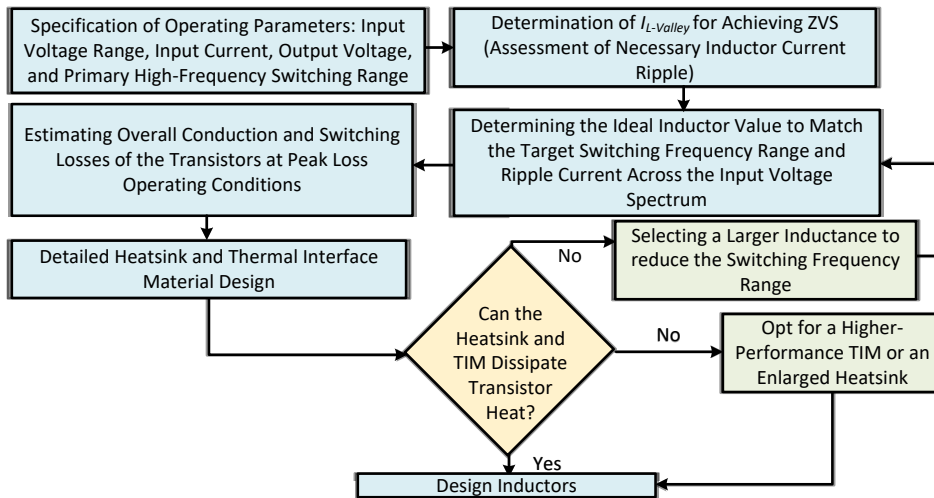


Figure 4.5 Methodology for the GaN-Based DC-DC Converter Optimization [PAPER-II].

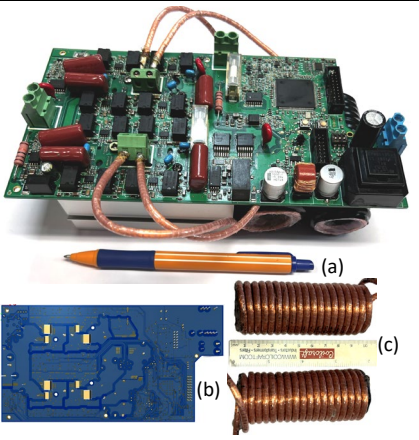
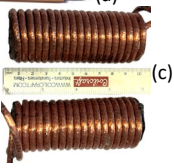
Figure 4.5 presents the design optimization strategy for a GaN-based DC-DC converters aimed at achieving maximum efficiency and high power density. At high power levels, the main priority is managing heat dissipation from the transistors' limited-size cooling pads [PAPER-II] and [74]. After ensuring effective thermal management and minimizing losses at the highest feasible switching frequency and power, attention shifts to inductor design. Under high-power operation, the switching frequency should be high enough to allow the use of low-value air-core inductors, which reduce core losses in conditions of hard-switching and high current ripple.

4.1.4 Experimental Results of the GaN-Based DC-DC Converter for Solar String Applications

A laboratory prototype of the GaN-based interleaved DC-DC converter with air-core inductors was built and tested to confirm the theoretical analysis. The prototype specifications are listed in Table 4.1. Its total volume is 0.51 L, composed of the PCB and

components (0.08 L), two air-core inductors (0.1 L total), and a natural convection heatsink (0.325 L, no airflow). The overall mass is 1.5 kg, giving a power density of 17.65 kW/L (50 kW/L without heatsink) and 6 kW/kg. The converter was tested over the input voltage range of 110–450 V while maintaining a constant 350 V output. Photos of the prototype, air-core inductors, and PCB layout showing the GaN transistor placement are provided in Table 4.1.

Table 4.1 Characteristics of the laboratory prototype of the GaN-based air-core DC-DC interleaved converter, with (a) photograph of the laboratory prototype, (b) PCB bottom side designed in Altium Designer, and (c) photograph of the air-core inductors [PAPER-II].

Components Characteristics		
Air-Core Inductors L_1 and L_2	12 μ H	
Inductors L_1 and L_2 Wire	3000 litz wires with 50 μ m diameter	
Input Capacitor C_{in}	7.4 μ F / 630 V	
Output Capacitor C_{out}	4 μ F / 630 V	
Natural Convection (without airflow) Heatsink	LAM5D1005V, 100×100.5×50 mm ³	
Thermal Interface Material	TG-A1780- 150-150-0.8	
Semiconductor Elements		
Main GaN Transistors ($S_1, \dots, S_4$)	GS66508T-TR, 30A, 650V	
Auxiliary GaN Transistors ($S_{a1}, \dots, S_{a4}$)	GS66516T-TR, 60A, 650V	
Solid State Circuit Breaker SiC MOSFETs	IMZA120R007M1HXKSA1, 225A, 1200V	
Operating Point		
Input voltage range (V_{in})	110 V–450 V	
Output voltage (V_{out})	350 V	
Maximum rated power (P_{out})	2.2 kW–9 kW	
Switching frequency (f_s)	18 kHz–304 kHz	

Comparison of ZCS and ZVS operation

Experimental results in Figure 4.6 compare BCM with negative $I_{L-Valley}$ operation (ZVS) at 2 kW output, 200 V output voltage, and 340 V input voltage. In BCM (ZCS turn-ON, 300 kHz), the junction temperature of S_3 reached 97 °C, while in ZVS mode (250 kHz) it dropped to 67 °C—a 30 °C reduction. This improvement comes from eliminating C_{oss} losses in the main transistors, even with only a modest reduction in switching frequency. Auxiliary transistor S_{a3} ran slightly hotter in ZVS mode due to increased turn-OFF losses, but overall efficiency improved from 97.8% to 98.2%.

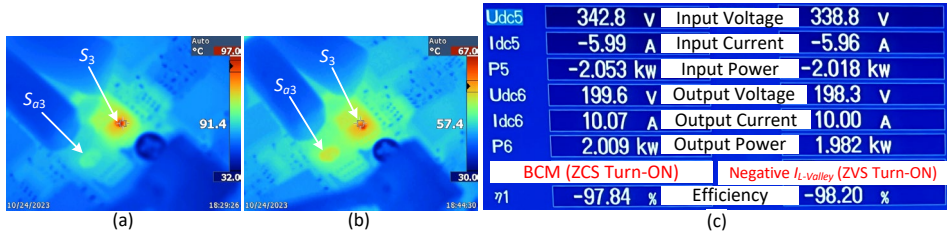


Figure 4.6 Experimental comparison of converter performance in BCM and negative $I_{L-Valley}$ operation at 2 kW, 200 V output, and 340 V input: (a) junction temperatures of S_3 and S_{a3} in BCM (300 kHz), (b) in negative $I_{L-Valley}$ (250 kHz), (c) efficiency in both modes [PAPER-II].

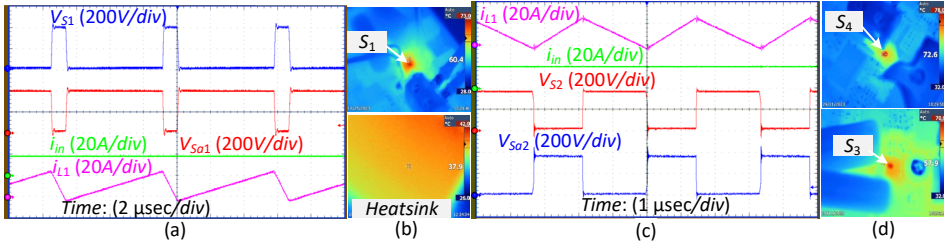


Figure 4.7 Buck mode ($f_s = 150$ kHz, $V_{in} = 400$ V, $V_{out} = 350$ V, $P_{out} = 7.8$ kW): (a) V_{DS} of S_1 , V_{DS} of S_{a1} , i_{L1} , and i_{in} waveforms, (b) thermal images of S_1 and heatsink; Boost mode ($f_s = 300$ kHz, $V_{in} = 200$ V, $V_{out} = 350$ V, $P_{out} = 4$ kW): (c) V_{DS} of S_2 , V_{DS} of S_{a2} , i_{L1} , and i_{in} waveforms, (d) thermal images of S_3 and S_4 [PAPER-II].

Buck and Boost mode operations

Figure 4.7a and Figure 4.7b show buck-mode results at 150 kHz, 400 V input, 350 V output, and 7.8 kW output power. The inductor valley current was set to -3 A to achieve ZVS, requiring a ripple of 28.3 A. Measured waveforms match theoretical predictions, with 400 V across the switches and minimal overshoot. Thermal imaging confirmed calculated junction temperatures for S_1 (73 °C measured vs. 75 °C predicted). Measured efficiency, including SSCB losses (3.48 W), was 98.91%, close to the calculated 99.2%.

Figure 4.7c and Figure 4.7d present boost-mode testing at 300 kHz, 200 V input, 350 V output, and 4 kW output power. ZVS was achieved with an $I_{L-Valley}$ of -3 A and a 26 A ripple current. Voltage stress matched the output voltage with no significant spikes. With the heatsink at 52 °C, the estimated junction temperatures for S_4 and S_3 are 78 °C and 69 °C, matching closely with the measured values of 78 °C and 70 °C. The measured efficiency of 98.1% aligns well with the calculated 98.4%, confirming the theoretical predictions.

Loss breakdown and Efficiency

Figure 4.8a plots measured and calculated efficiencies across the input voltage range using a YOKOGAWA WT1800 power analyzer. Maximum measured efficiency, including SSCB losses (2.8 W at 7 kW), was 99% at 7 kW, compared to a calculated 99.3%.

The loss breakdown in Figure 4.8b shows that transistor conduction and switching losses dominate total losses, with inductor and SSCB conduction losses making smaller contributions. Thermal images from Figure 4.7b and Figure 4.7d confirm the predicted device loss distribution. A distinct step in conduction losses occurs at 350 V input due to the converter switching between boost and buck operation.

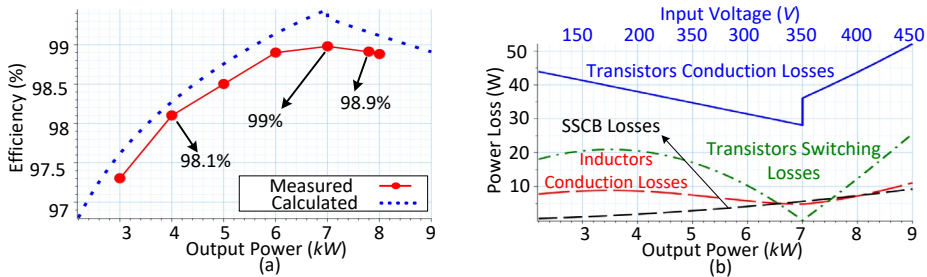


Figure 4.8 Theoretical and experimental efficiencies, along with the theoretical power loss breakdown of the converter: (a) efficiency, (b) loss breakdown [PAPER-II].

4.2 High-Frequency Isolated DC-DC Stage Optimization

It is widely recognized that advancements in Wide Band Gap (WBG) semiconductor technology serve as a major driving force in the progression of power electronics, particularly in enhancing efficiency and reducing system size [77]–[78]. One of the key advantages of these modern devices is their capability to operate at higher switching frequencies, which not only supports an increase in power density but also contributes to reducing future electronic waste.

While numerous studies have explored high switching frequency applications, there is still a lack of clear, structured guidelines for designing isolated DC-DC converters that fully consider the necessity of maintaining ZVS operation.

Within this framework, this subsection focuses on assessing different circuit approaches for isolated DC-DC converters intended to operate at switching frequencies of 1 MHz and above, with an emphasis on establishing a design methodology that sustains ZVS conditions. The primary objective is to develop practical design recommendations that ensure reliable ZVS operation at such high frequencies.

This study examines both the design process and performance of isolated DC-DC converters operating beyond 1 MHz, concentrating on ZVS achievement. It presents a comparative analysis of multiple resonant isolated converter topologies—namely conventional LLC, conventional CLLC, Capacitive Coupling Isolation (CCI), and asymmetrical CLLC—alongside an evaluation of air-core and ferrite-core transformers with respect to efficiency, loss mechanisms, thermal performance, and implementation constraints.

The investigation begins by reviewing several high-frequency-capable converter architectures, including Dual Active Bridge (DAB), LLC, CLLC, CI, and asymmetrical CLLC, while outlining the specific ZVS requirements for each. This is followed by a detailed examination of ZVS conditions across the selected topologies. Transformer designs are then compared, highlighting the trade-offs in losses and volume between standard ferrite cores available commercially and custom air-core transformers optimized for MHz-level operation.

Experimental validation is performed to benchmark the performance of both ferrite-core and air-core transformer designs in LLC, CLLC, CI, and asymmetrical CLLC configurations under 1 MHz switching frequency, power levels between 3.5 kW and 6 kW, and an input voltage of 350 V. The experimental analysis covers efficiency, thermal behavior, limitations in practical implementation, and ZVS performance.

The findings emphasize the crucial role of optimized transformer geometry, accurate selection of components, and appropriate circuit configuration to minimize parasitic effects while preserving ZVS. The outcome of this work delivers concrete, application-oriented guidelines for the design of high-frequency resonant converters, ensuring both high performance and technical feasibility in MHz-range, multi-kilowatt applications.

4.2.1 High-Frequency Bidirectional Isolated DC-DC Converter Topologies

The isolated DC-DC stage of the proposed system can be implemented using several bidirectional converter architectures, as shown in Figure 4.9. Four configurations are considered in this study: Dual Active Bridge (DAB) with ZVS turn-on and hard turn-off switching behavior; Conventional LLC and CLLC resonant converter with standard compensation; Modified CLLC resonant converter adapted from Inductive Power Transfer (IPT) concepts; and CCI topology that replaces magnetic coupling with capacitive elements.

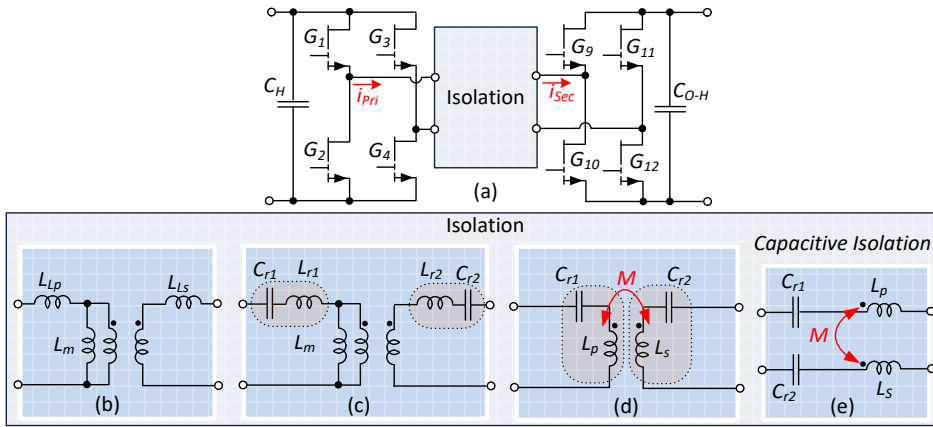


Figure 4.9 Bidirectional isolated DC-DC interface for 1 MHz operation accommodating multiple isolation methods: (b) DAB converter with ZVS turn-on and hard turn-off [79], (c) conventional CLLC resonant converter with traditional compensation [80]–[81], (d) modified CLLC design inspired by IPT systems [61], (e) CCI approach [62].

For demonstration, Figure 4.9a shows the upper DC-DC module in the proposed UOBC in section 3, which mirrors the operation of the lower module. The two can be connected in either series or parallel depending on the battery voltage requirement. Each module uses a full-bridge on both the primary (G_1 – G_4) and secondary (G_9 – G_{12}) sides.

The DAB (Figure 4.9b) is a well-known choice for wide output regulation and high efficiency [79], but most reported performance data comes from relatively low-frequency operation. Although it achieves ZVS turn-on over a wide range, it suffers from hard turn-off losses—especially at peak currents—which worsen as switching frequency rises, making it less favorable for MHz-level applications.

Resonant converters like LLC and CLLC (Figure 4.9c) offer soft-switching for both turn-on and turn-off, reducing switching losses and improving efficiency [80]–[81]. They have been applied successfully in DC transformer systems and other high-performance power electronics. While high-frequency operation under large load variation is less documented, recent studies [82]–[83] show strong potential. However, these converters require sufficient magnetizing inductance to offset leakage effects, which is harder to achieve at ultra-high frequencies without ferrite cores.

A modified CLLC design inspired by IPT [61] (Figure 4.9(d)) minimizes inductance and runs at resonance with ZCS at rated load. By applying asymmetrical compensation which is completely discussed in [61], it can also achieve ZVS without large magnetics—ideal for MHz switching with WBG devices. Unlike traditional resonant converters, its transformer design avoids complex tuning since winding coupling is fixed. However, at high power and MHz operation, reducing the compensation capacitor to enhance performance raises voltage stress. The large, high-voltage capacitors required in this case often have high ESR, leading to excessive conduction losses and heating, which limits practicality without significant redesign.

Table 4.1 compares the passive component requirements of these topologies under equal conditions: 350 V input and output, 5 kW, and 1 MHz switching. The DAB has the largest magnetic size, making it unsuitable without ferrite cores. The modified CLLC has the smallest inductance and maintains ZVS over a good voltage range [61], but strong

coupling can cause frequency splitting and increase conduction losses. Standard LLC and conventional CLLC remain practical due to their moderate magnetic requirements, though they demand larger series capacitors.

Table 4.1 Passive components values required for resonant isolated DC-DC converters.

Symbol	Values			
	DAB	LLC	CLLC	CLLC [61]
C_{r1}	-	55 nF	55 nF	8 nF
L_{r1}	6 μ H	0.45 μ H	0.45 μ H	0.3 μ H
L_m	60 μ H	4.5 μ H	4.5 μ H	3.2 μ H
L_{r2}	-	-	0.45 μ H	0.3 μ H
C_{r2}	-	-	55 nF	4 nF

CCI (Figure 4.9e) eliminates the transformer, reducing size, cost, and magnetic complexity [62]. While switching performance can match inductive systems, this method does not provide inherent galvanic isolation, which is required by most safety standards for shock protection—usually achieved with transformers.

Figure 4.10 presents a simplified loss comparison for several isolated converter topologies in a 5 kW system, evaluated across various switching frequencies using GaN-based GS66516T devices. The study accounts for conduction losses P_{CON} , turn-off switching losses P_{SW-OFF} , and losses from the output capacitance P_{COSS} . The DAB is modeled under ZVS turn-on, while the LLC and CLLC are assessed assuming ideal ZCS with high enough magnetizing inductance to maintain soft current transitions.

At lower switching frequencies, LLC and CLLC converters show slightly higher conduction losses compared to the DAB. However, once frequencies exceed ~ 200 kHz, switching-related losses—particularly those linked to device output capacitance—become the dominant factor. In the DAB, turn-off losses rise sharply with frequency despite ZVS turn-on, limiting its effectiveness for MHz-class operation. While LLC and CLLC avoid hard turn-off losses due to ZCS, they still suffer from P_{COSS} because the stored energy in the transistor's output capacitance is dissipated during turn-on. This becomes a major efficiency penalty at higher frequencies.

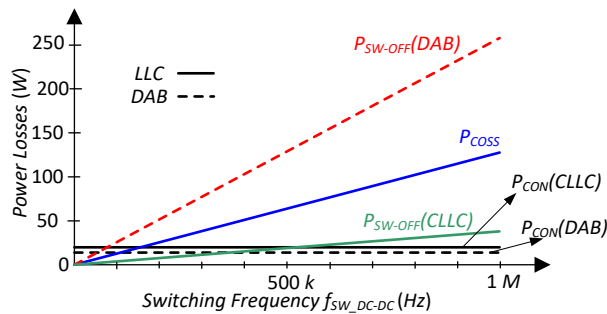


Figure 4.10 Loss distribution of the evaluated solutions versus switching frequency using GaN transistors [61].

4.2.2 Theoretical Comparison of Ferrite and Air-Core Transformers at 1 MHz

At megahertz-range switching frequencies, three widely used planar ferrite core materials—PC200, ML91S, and 3F4—are favoured for their comparatively low core losses under such conditions. Manufacturers supply loss characteristics for different frequencies and flux densities, which can be modelled using the relationship:

$$P_{cv} (kW / m^3) = K_c f_s^\alpha B_m^\beta. \quad (4-5)$$

By applying provided data points to this formula, it becomes possible to determine the frequency exponent α , flux density exponent β , and loss coefficient K_c for each material. These constants, derived from datasheet specifications, are summarized in Table 4.2. The peak flux density B_m for (4-6) is given by:

$$B_m = V_{in} / 4Nf_s A_e, \quad (4-6)$$

where N is the number of turns in the winding and A_e is the core's effective cross-sectional area.

Table 4.2 Values of core loss coefficients for PC200, ML91S, and 3F4 core materials.

Symbol	Values for temperature of 100 °C and $f_s = 500\text{kHz}-1\text{MHz}$		
	K_c	α	β
PC200	0.00023671	1.518	2.497
ML91S	2.024×10^{-11}	2.784	3.077
3F4	0.000034620	1.856	2.994

Using the dataset provided in Table 4.2, the trends in relative core losses across different magnetic flux densities for switching frequencies of 500 kHz, 700 kHz, and 1 MHz—under the condition of a 100 °C core temperature—are illustrated in Figure 4.11. Within this operating band, ML91S ferrite consistently demonstrates the lowest losses, with PC200 delivering similar results. In contrast, the 3F4 material exhibits the highest loss values, approximately five to ten times greater than the other two. For high power density designs, the restricted physical size of available ferrite cores often necessitates connecting multiple cores in parallel to share the thermal load and prevent excessive heating. However, increasing the winding turns to satisfy flux density constraints amplifies proximity effects and AC resistance, thereby elevating copper losses and enlarging the transformer's physical dimensions. While paralleling cores offers improved thermal performance, it also increases overall transformer volume.

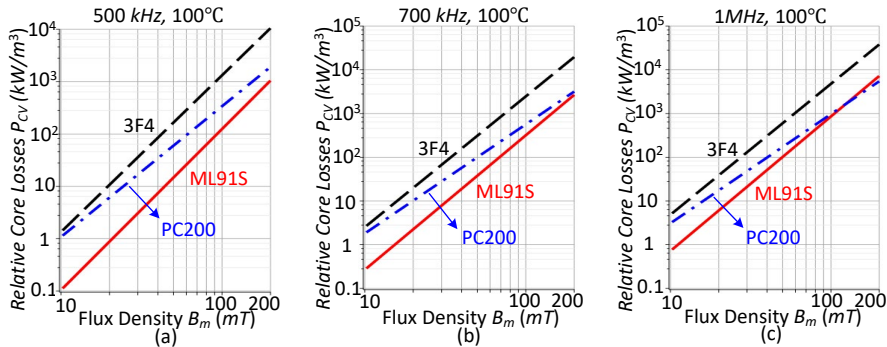


Figure 4.11 Relative core losses versus magnetic flux density for (a) $f = 500 \text{ kHz}$, $T = 100 \text{ }^\circ\text{C}$, (b) $f = 700 \text{ kHz}$, $T = 100 \text{ }^\circ\text{C}$, and (c) $f = 1 \text{ MHz}$, $T = 100 \text{ }^\circ\text{C}$.

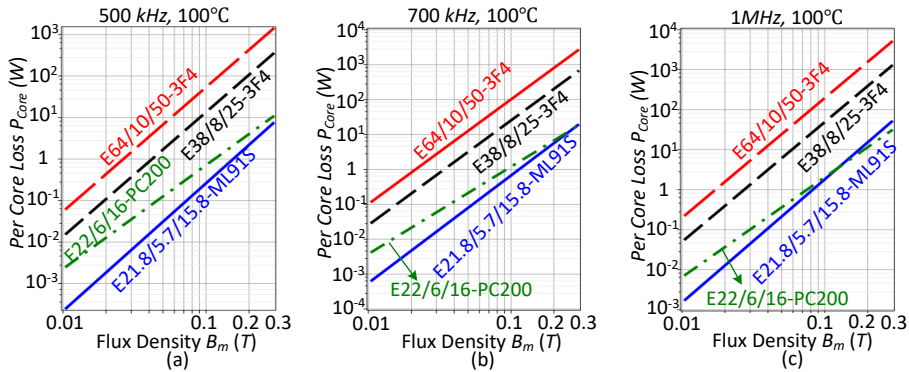


Figure 4.12 Relative Per-core losses for the largest available cores of the three materials versus maximum flux density for (a) $f = 500$ kHz, $T = 100$ °C, (b) $f = 700$ kHz, $T = 100$ °C, and (c) $f = 1$ MHz, $T = 100$ °C.

Table 4.3 Units for magnetic properties.

Core material	B_{sat} (mT)	Commercially biggest available core size	A_e (mm ²)	Possible parallel cores ($N_{Parallel}$) and winding turns (N)	Total min. needed footprint (mm ²)	Max. output voltage at 100 °C core ($\Delta T = 60$ °C) for $f_s = 1$ MHz (V)	Total core losses (W) at max output voltage for 100 °C core ($\Delta T = 60$ °C) at $f_s = 1$ MHz	Thermal resistance of each core (°C/W)	Required max. flux density for 100 °C core ($\Delta T = 60$ °C) at $f_s = 1$ MHz (mT)
PC200	410	E22/6/16	78.3	$N_{Parallel} = 12, N = 1$	5114.3	387	$12 \times 1.7W = 20.4$	35.5	100
ML91S	430	E21.8/5.7/15.8	78.3	$N_{Parallel} = 12, N = 1$	5114.3	409	$12 \times 1.7W = 20.4$	35.5	100
3F4	430	E 64/10/50	519	$N_{Parallel} = 3, N = 2$	14361.6	476	$3 \times 8.4W = 25.2$	7.163	35
				$N_{Parallel} = 3, N = 3$		714	$3 \times 8.4W = 25.2$		
				$N_{Parallel} = 3, N = 4$		953	$3 \times 8.4W = 25.2$		
				$N_{Parallel} = 2, N = 3$	11110.4	476	$2 \times 8.4W = 16.8$		
				$N_{Parallel} = 2, N = 4$		635	$2 \times 8.4W = 16.8$		
				$N_{Parallel} = 1, N = 4$		318	$1 \times 8.4W = 8.4$		
				$N_{Parallel} = 1, N = 5$	7859.2	397	$1 \times 8.4W = 8.4$		
		E 38/8/25	194	$N_{Parallel} = 5, N = 2$	6843.9	373	$5 \times 4W = 20$	15.12	45
				$N_{Parallel} = 4, N = 2$	5876.2	298	$4 \times 4W = 16$		
				$N_{Parallel} = 3, N = 2$	4908.4	224	$3 \times 4W = 12$		
				$N_{Parallel} = 2, N = 2$	3940.7	149	$2 \times 4W = 8$		
Air core	-	-	-	$N = 11$	6647.6	-	-	-	-

For winding construction, a common method is a vertically stacked, interleaved arrangement of primary and secondary layers. This configuration provides strong flux cancellation, effectively lowering leakage inductance and associated AC losses. However, it tends to raise interwinding capacitance [84]. To counter this drawback, advanced winding geometries are recommended to limit capacitance without significantly increasing AC resistance. Because winding topology directly affects key transformer parameters—such as leakage inductance, stray capacitance, AC losses, and heat dissipation—optimization must be carried out jointly with core selection and physical layout.

The largest commercially available planar ferrite cores and their feasible winding arrangements are outlined in Table 4.3, while Figure 4.12 presents the per-core loss characteristics of these cores for three ferrite materials over different maximum flux densities. Although ML91S and PC200 offer favorable loss performance, their relatively small form factors restrict their suitability for higher power levels. Conversely, 3F4,

despite its higher core loss values, is often preferred in multi-kilowatt designs because it is available in larger core sizes capable of handling greater throughput.

In MHz-frequency planar transformer design, mitigating core losses along with proximity and skin effects is critical to maintaining low AC resistance. One effective strategy to lower stray capacitance is reducing the overlap area between adjacent turns or increasing the physical spacing. A horizontal routing approach—where adjacent turns are laid side-by-side instead of stacked—can achieve this, as demonstrated in Figure 9(a) of [84]. In such a layout, the overlap is governed by the conductor length and thickness, with PCB copper thickness being much smaller than its width. Although this arrangement increases the footprint by limiting vertical PCB stacking, it reduces AC resistance, enhances leakage inductance, and is well suited for LLC and CLLC applications. Additionally, because of the limited core dimensions and the properties of available ferrite materials, the number of winding turns is kept minimal in both primary and secondary to avoid excessive AC resistance from skin and proximity effects.

Thermal performance also becomes a deciding factor in core selection. From Table 4.3, PC200 and ML91S possess relatively high thermal resistance due to their compact dimensions, which demands operation with lower allowable losses for safe thermal margins. At an ambient temperature of 40 °C and an allowable temperature rise of 60 °C (resulting in a core temperature of approximately 100 °C), their maximum operating flux density should be restricted to around 100 mT. Larger-sized 3F4 cores, with lower thermal resistance, can accommodate higher power levels but at the cost of increased core losses. To limit the temperature rise to 60 °C, Figure 4.12 shows that the E64/10/50 core should operate at a maximum flux density of 35 mT, while the E38/8/25 core should not exceed 45 mT.

For LLC and CLLC converters running at 1 MHz, the required number of parallel cores N_{Parallel} and winding turns N —to keep core temperature under 100 °C without using an air gap—are provided in Table 4.3. While adding parallel cores reduces flux density and core losses, keeping temperature rise under control, it increases the transformer's volume. At multi-MHz frequencies, hysteresis and eddy-current losses also become more prominent, limiting the practicality of excessive core parallelism.

In horizontal winding layouts, the number of turns is dictated by the output power and the available core window area. With a PCB trace current density limit of 15 A/mm² and an output current of 10 A (11.11 A RMS per winding [81]), the transformer requires a minimum routing cross-sectional area of 0.74 mm². At frequencies above 1 MHz, copper thickness should not exceed 2 oz/ft² (0.07 mm) to keep skin and proximity effects in check, leading to a minimum trace width of 10.58 mm. Under these constraints, the E22/6/16 core cannot accommodate the required conductor width, making it unsuitable for such current levels in a horizontal routing design. By comparison, the E38/8/25 and E64/10/50 cores allow a maximum of one and two turns per winding, respectively, without exceeding the thermal and geometric constraints.

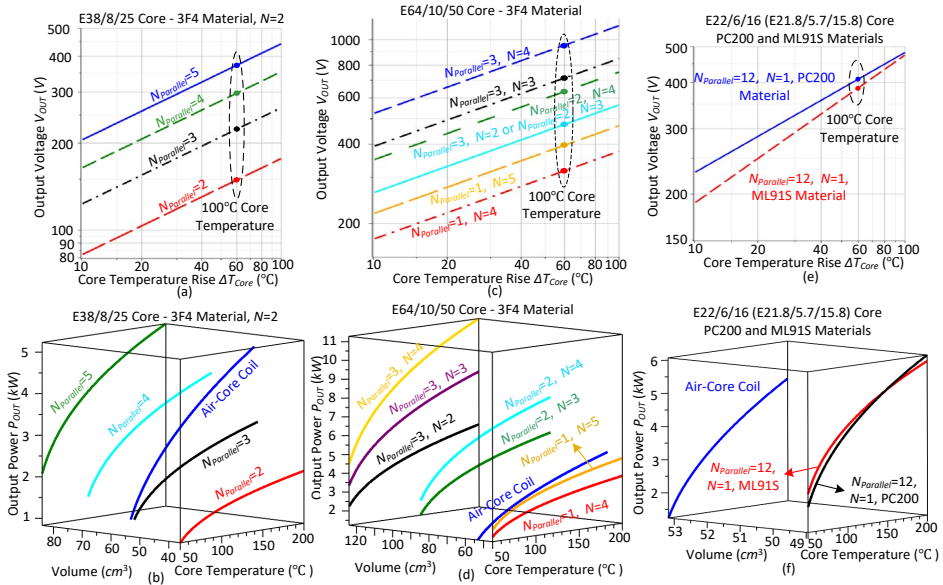


Figure 4.13 Maximum output voltage and power in LLC converters (1 MHz, 10 A) versus core temperature rise (ΔT_{Core}) and volume, for various turns, parallel cores, and materials: (a,b) E38/8/25, 3F4, $N = 2$; (c,d) E64/10/50, 3F4; (e,f) E22/6/16, PC200 and ML91S, including air-core and ferrite-core transformer comparison.

While PC200 and ML91S remain advantageous in loss performance for MHz-range operation, their smaller size limits practical deployment in kW-scale systems. In contrast, larger 3F4 cores can meet these power demands either by increasing the number of turns or by paralleling two or three E64/10/50 units.

Figure 4.13 maps the maximum output voltage against the number of turns N , parallel cores $N_{Parallel}$, and core material type for LLC and CLLC converters at 1 MHz and 10 A output, factoring in core temperature rise ΔT_{Core} . Air-core transformers are also included in the comparison, with evaluations covering maximum output power, winding count, parallel core count, and volume for equivalent designs.

For the E38/8/25-3F4 core (Figure 4.13a), horizontal routing limits the design to one turn per winding, but employing top and bottom PCB layers for the primary and secondary enables two turns without raising AC resistance or capacitance [85]. Under a 60 °C maximum rise (ambient = 40 °C), the achievable output voltages are 149 V, 224 V, 298 V, and 373 V for $N_{Parallel}$ values of 2, 3, 4, and 5, respectively. Thus, obtaining 350 V output requires five parallel E38/8/25-3F4 cores with two turns each. In Figure 4.13b, when compared to an air-core transformer of similar design, the air-core unit surpasses configurations of 2–4 parallel cores in kW power capability and occupies less volume than the 4-core and 5-core versions.

The E64/10/50-3F4 case (Figure 4.13c) allows two turns in horizontal routing, but planar transformer techniques enable up to four turns with separate PCBs for each winding layer, thereby keeping AC resistance and stray capacitance under control [85]. For a 100 °C limit, Table 4.3 lists the output voltages achievable for various $N_{Parallel}$ and N combinations, showing that most configurations can meet a 350 V target except for $N_{Parallel} = 1$, $N = 4$. Adding a fifth turn with standard routing increases AC losses, while vertical layouts worsen skin and proximity effects and boost capacitance. As shown in Figure 4.13d, the air-core transformer again outperforms single-core designs in both

density and efficiency and maintains a smaller footprint than configurations using two or three parallel E64/10/50-3F4 cores.

For the E22/5/16 core (Figure 4.13e), PC200 shows slightly better voltage handling than ML91S for a given temperature rise, with achievable voltages of 387 V and 409 V, respectively, under a 100 °C core temperature limit. Meeting a 350 V target requires twelve parallel cores in either material, but the limited window area prevents proper routing for 10 A currents without severe AC copper loss. In Figure 4.13f, the air-core coil again demonstrates superior practicality by avoiding the physical and thermal constraints associated with heavy parallelism in small ferrite cores.

For resonant LLC/CLLC designs, achieving proper leakage inductance is challenging in PCB-embedded ferrite transformers, often requiring air gaps or auxiliary inductors. Air-core coils wound with litz wire naturally meet leakage needs while removing core loss entirely, providing a compact, high-density option for multi-megahertz kW designs.

Data in Table 4.3 show that for 350 V, 5 kW, and ~1 MHz, air-core designs can rival ferrite-core transformers in size. As illustrated in Figure 4.15, an air-core transformer and a ferrite transformer built from two E38/8/25-3F4 cores have nearly identical volume and power density. While ferrite designs excel at lower frequencies due to lower copper loss, air-core coils dominate above 1 MHz by removing core losses, leaving only conduction effects to be managed.

4.2.3 Performance Comparison of Inductive VS Capacitive Isolations

The configurations of both capacitive-coupling and inductive-coupling-based converter structures used for comparison are shown in Figure 4.9, while their performance evaluation is presented in Figure 4.14, both converters operating under soft-switching conditions. To ensure a fair and consistent evaluation, all other dynamic switching configurations are kept identical between the two designs.

From the results in Figure 4.14, it is evident that both converter types exhibit nearly identical performance in terms of switching voltage stress, conduction losses, and switching losses. However, CCI offers a distinct advantage in size and volume due to the absence of bulky transformers and the use of smaller inductive elements. This translates into a higher achievable power density and reduced manufacturing cost. Consequently, based on this analysis, CCI converters present a more compact, cost-effective solution with higher power density compared to their inductive-isolated counterparts [62].

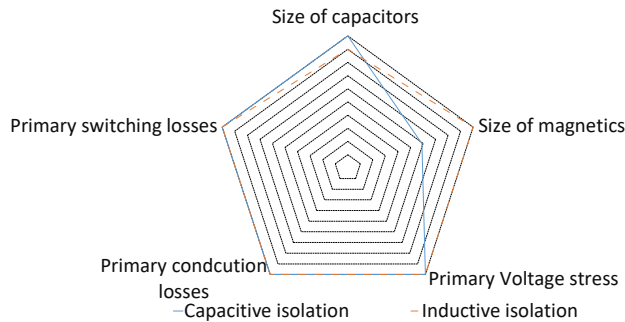


Figure 4.14 Overall performance comparison between converters using CCI and those employing inductive isolation [62].

Table 4.4 Prototype specifications and component details.

Components Characteristics	
Input Capacitor C_1	7 μF , 630 V
Output Capacitor C_2	7 μF , 630 V
Capacitor C_p	1 nF to 50 nF
Capacitor C_s	0 nF to 50 nF
1 st air-core transformer (L_p , L_s , M)	0.05 mm $\times$ 3000 strands litz wire ($N_p = N_s = 15$) 26 μH /26 μH /21.2 μH
2 nd air-core transformer (L_p , L_s , M)	0.05 mm $\times$ 3000 strands litz wire ($N_p = N_s = 11$) 5.85 μH /5.9 μH /3.5 μH
CCI air-core transformer (L_p , L_s , M)	0.05 mm $\times$ 3000 strands litz wire ($N_p = N_s = 7$) 2.9 μH /3 μH /1.3 μH
Ferrite core transformer (L_p , L_s , M)	Two parallel E38/8/25-3F4 Ferrite Cores 5 μH (with adding 1.2 μH external inductor)/3.8 μH /3.6 μH
Semiconductor Elements	
GaN transistors S_1 - S_4	GS66516T-TR, 60A, 650V, Thermal resistance $R_{\theta JC} = 0.5$ $^{\circ}C/W$
Secondary side diodes D_1 - D_4	SCS230AE2HRC11, Thermal resistance $R_{\theta JC} = 0.55$ $^{\circ}C/W$
Operating Point	
Input voltage range V_{in}	350 V
Output voltage V_{out}	300-400 V
Input power P_{out}	3.5 kW- 6 kW
Input Current I_{in}	10-12 A
Switching frequency f_s	1 MHz-1.5 MHz
Thermal Cooling System Characteristics with TG-A1780- 150-150-0.8 TIM [74]	
Thermal film for GaN	1.38 $^{\circ}C/W$
Thermal film for SiC diode	0.26 $^{\circ}C/W$

4.2.4 Experimental Verifications in Case of High-Frequency Isolated DC-DC Stage Optimization

As outlined in [61], the experimental setup featured separate primary and secondary PCBs with dedicated heatsinks, an interchangeable air-core or ferrite-core transformer, and a TMS32028379DPTPT-based control board for high-frequency operation. The primary heatsink cooled the GaN switches, gate drivers, isolated DC-DC supplies, and DC-link capacitors, while the secondary heatsink served the rectifier diodes, capacitors, and output filter. Measurement equipment included Tektronix voltage and current probes, a Tektronix MDO4034B-3 oscilloscope, a Chroma 62150H-1000S power supply, and a bidirectional DC source with an electronic load. Efficiency was recorded using a YOKOGAWA WT1800 power analyzer.

The objective was to validate the proposed CLLC converter operation in at a switching frequency of 1 MHz, extending earlier tests performed at 500 kHz. The evaluation used an air-core transformer coil with half the physical size of the ferrite-core transformer in [61], with its dimensions illustrated in Figure 4.15a. The analysis included a comparative study between LLC and CLLC converters (each tested with both air-core and ferrite-core transformers) and CCI converters focusing on performance under similar operating conditions. Given the high efficiency achievable at MHz switching frequencies [86], efficiency testing was a central part of the investigation.

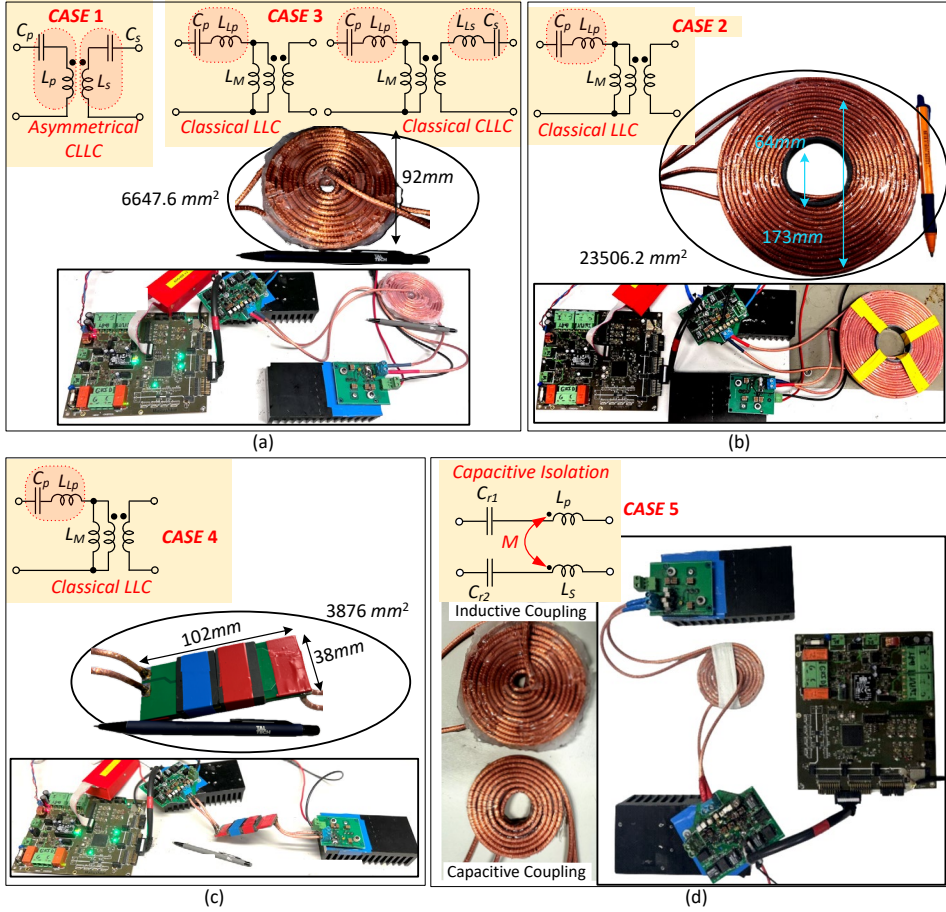


Figure 4.15 (a) Second air-core coil for CASE 1: asymmetrical CLLC (half-size core from [61]) and CASE 3: classical LLC/CLLC; (b) first air-core coil for CASE 2: classical LLC; (c) ferrite transformer, two parallel E38/8/25-3F4 cores for CASE 4: classical LLC; (d) capacitive coupling with air-core coupled inductor.

CASE 1: Asymmetrical CLLC as in [61]

Initial experiments focused on understanding the impact of the asymmetrical CLLC configuration. The baseline test used a symmetrical setup, with 4.33 nF series capacitors placed on both the primary and secondary sides, tuned to resonate at 1 MHz with the coil inductance. Since GaN transistors suffer significant C_{oss} -related losses at high frequencies [32], the target was toward ZVS at turn-on, thereby eliminating these losses by adjusting the secondary-side series capacitor C_s .

In the second test, C_s was reduced to 3 nF (Figure 4.16a), allowing complete charging and discharging of the devices' drain-source capacitances, which successfully enabled ZVS turn-on at 100 V with a turn-off current of 6 A. Under these conditions, the measured efficiency was 90.3% at 330 W. However, operation at higher voltage and power levels was still necessary to meet the intended design targets.

The next test pushed the input voltage to 150 V, with C_s further reduced to 2.66 nF. As depicted in Figure 4.16b, this configuration led to pronounced voltage oscillations across C_s under high-power operation. At 150 V input and 800 W output, the capacitor voltage swung between approximately -500 V and +500 V—approaching its 630 V

rating—creating instability in the converter. Moreover, the drain–source capacitance of switch S_1 remained partially charged despite an 8 A turn-off current, preventing full elimination of C_{oss} losses and resulting in only partial ZVS turn-on. Under these operating conditions, the peak efficiency achieved was 91.3 %.

CASE 2: First Air-Core Coil in Classical LLC Operation

To evaluate the capability of an air-core transformer under high-frequency, high-power conditions, tests were performed at 1 MHz, 3–4 kW input power, and a 350 V input voltage using a classical LLC resonant configuration. The test arrangement, shown in Figure 4.15b, operated at 4 kW input power, delivering 300 V output from a 350 V input at 1 MHz switching frequency. As shown in Figure 4.16c, ZVS at 350 V was achieved through the use of an 8 nF primary-side series capacitor C_p . Approximately 16 A of current was required to store enough energy in the equivalent series inductance to fully charge and discharge the drain–source capacitances of the transistors during switching events.

Thermal imaging after one hour of continuous operation (Figure 4.16d) indicated the air-core coil reached a steady-state temperature of 104 °C while carrying 13.6 A RMS at 1 MHz. Given the coil’s thermal resistance of 1 °C/W per winding and an ambient temperature of 30 °C, total coil losses were estimated at 148 W, corresponding to an AC resistance of 0.4 Ω per winding. At such high switching frequencies and power levels, GaN devices face significant thermal dissipation challenges, which necessitate not only large heatsinks but also the use of high-quality thermal TIM for effective heat transfer.

The thermal profile in Figure 4.16d also includes both the primary-side PCB hosting the GaN transistors and the secondary-side PCB with SiC diodes. For the GaN switches, a measured junction-to-heatsink temperature difference of 13 °C, combined with a thermal resistance of 1.88 °C/W (from Table 4.4), corresponds to a power loss of 6.9 W per device—totaling 27.7 W for four transistors. On the secondary side, the SiC diodes exhibited a 10 °C temperature difference with a thermal resistance of 0.81 °C/W, leading to losses of 12.4 W per diode, or 49.4 W in total. This gives a combined semiconductor loss of approximately 77 W, with the SiC diodes dissipating nearly double the heat of the GaN switches.

These findings confirm that the thermal management strategy implemented was effective for maintaining stable operation, and they also indicate headroom for either increasing output power or pushing the switching frequency beyond 1 MHz without surpassing safe operating temperatures.

CASE 3: Second Air-Core Coil in Classical LLC and CLLC Operation

To further improve efficiency and reduce losses in air-core transformer applications, a smaller coil was tested. The evaluation was carried out at 1 MHz switching frequency, 350 V input, and a 3.5–4.5 kW power range, with both LLC and CLLC configurations examined for their ZVS performance, as shown in Figure 4.15a.

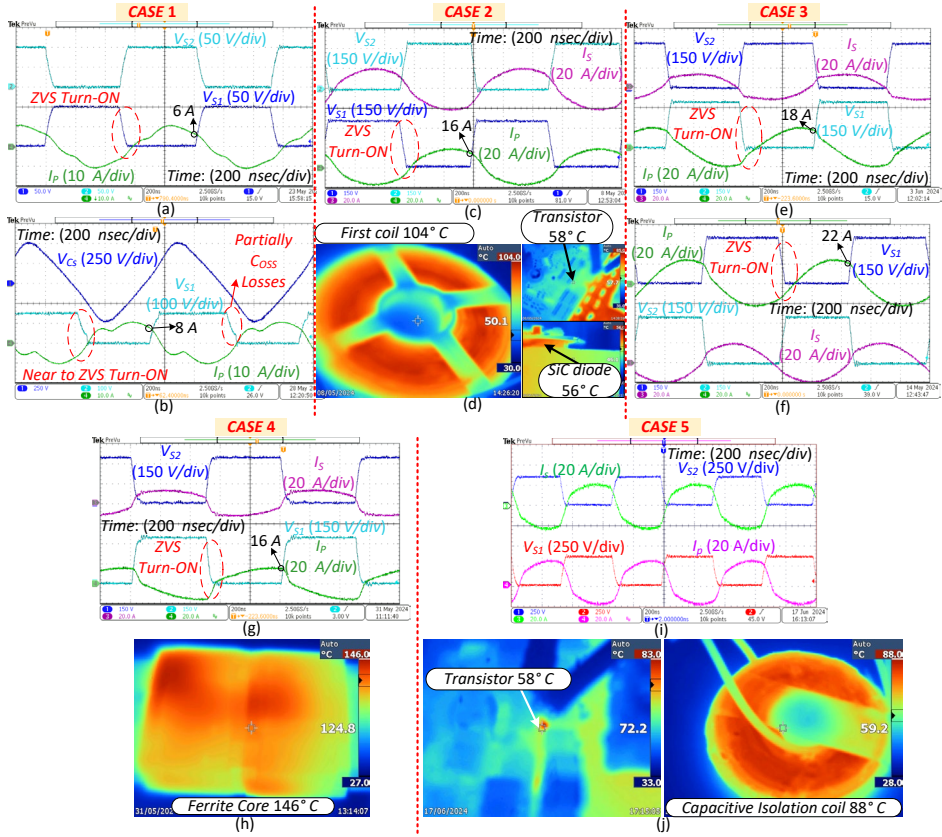


Figure 4.16 Key waveforms and thermal images for four cases — (a,b) CASE 1: Asymmetrical setup with reduced CS; (c,d) CASE 2: First air-core coil at 4 kW and thermal image; (e,f) CASE 3: Second air-core coil in LLC and CLLC modes; (g,h) CASE 4: Ferrite-core transformer waveforms and thermal image at full load; (i,j) CASE 5: Capacitive coupling isolation coil at 6 kW and 1.5 MHz switching frequency and thermal image.

In the LLC setup, Figure 4.16e illustrates the primary and secondary currents alongside the drain–source voltages of switches S_1 and S_2 . A 15 nF primary-side series capacitor C_P was used to achieve resonance and enable ZVS at 350 V. Achieving full charging and discharging of the transistor drain–source capacitances required approximately 18 A of current in the equivalent series inductance.

For the symmetrical CLLC configuration, shown in Figure 4.16f, both the primary and secondary sides used 22 nF series capacitors (C_P and C_S), providing resonance for ZVS at 350 V. In this case, around 22 A was needed to store enough energy in the series inductance for full ZVS turn-on.

Thermal performance was assessed after one hour of operation at 4.2 kW, 350 V input, and 1 MHz switching. The second air-core coil reached 101 °C while conducting 13.4 A RMS. Given a thermal resistance of 2.6 °C/W per winding and an ambient temperature of 30 °C, total coil losses were calculated at 54.6 W, corresponding to an AC resistance of 0.15 Ω per winding.

For the GaN transistors, a junction-to- heatsink temperature difference of 16 °C combined with a thermal resistance of 1.88 °C/W indicated losses of 8.5 W per device, or 34 W for four transistors. The SiC diodes showed a 12 °C temperature difference and

0.81 °C/W thermal resistance, equating to 14.8 W per diode, or 59.3 W total for four devices. Overall semiconductor losses summed to approximately 93.3 W, with diode losses being nearly double those of the transistors.

CASE 4: Two-Parallel E38/8/25-3F4 Ferrite Cores in Classical LLC Operation

To evaluate ferrite core behavior at high-frequency operation, a test was conducted using two parallel E38/8/25-3F4 ferrite cores under 1 MHz switching, 350 V input, and 3.5 kW power. The total core volume was 36 cm³, which is smaller than the second air-core coil (53 cm³). The experimental arrangement and transformer are shown in Figure 4.15c, while Figure 4.16g displays the primary and secondary winding currents alongside the drain–source voltages of switches S_1 and S_2 during LLC operation. To achieve ZVS at 350 V, a 1.2 µH external inductor was connected in series, forming a resonant tank with a 50 nF primary-side capacitor C_p . Achieving full drain–source capacitance charging and discharging for ZVS turn-on required approximately 16 A flowing through the equivalent series inductance.

Thermal imaging results, presented in Figure 4.16h, show that the ferrite cores experienced rapid heating at 350 V, 3.5 kW, and 1 MHz switching. The core temperature reached 146 °C within seconds of startup, significantly impacting performance and reducing efficiency to 86.1%. Semiconductor device temperatures remained stable, indicating that the primary loss source was the ferrite core itself.

This case highlights the challenge of managing excessive core losses in ferrite materials at MHz-level switching, even when parallel cores are used, and underlines the importance of material and geometry selection in high-frequency, high-power transformer designs.

CASE 5: Capacitive Coupling Isolation

Figure 4.16i illustrates the key operating waveforms of the converter under an output power of approximately 6 kW and 1.5 MHz switching frequency, including the drain-source voltages of switches S_1 and S_2 , along with the primary and secondary currents of the coupled inductor. The waveforms clearly indicate ZVS for both turn-on and turn-off events, with the transistors experiencing only minimal voltage stress during switching transitions. Operating in ZVS mode allows the switches to transition at zero voltage, effectively eliminating C_{oss} losses and reducing heat generation. The observed primary and secondary currents follow the expected resonant patterns, confirming that the resonant network successfully shapes both current and voltage profiles for efficient power transfer.

Figure 4.16j presents the measured operating temperatures of the main switch S_1 and the air-core coupled inductor, respectively, under an output power of approximately 6 kW and 1.5 MHz switching frequency. The temperature of S_1 remains comfortably within safe limits, indicating that the applied thermal management strategy ensures adequate heat dissipation. Likewise, the air-core coupled inductor maintains a stable temperature profile without signs of excessive thermal stress, highlighting the design’s robustness for high-power operation. These results collectively verify that the thermal characteristics of both the switching devices and the magnetic components do not impose any negative impact on the converter’s overall efficiency and stability, even under heavy-load conditions.

Feasibility and Efficiency Analysis

The findings from CASE 1 indicate that while lowering the secondary series capacitance C_s can improve performance by enabling ZVS turn-on, it also substantially raises voltage stress, risking capacitor reliability. In high-power, high-voltage operation at 1 MHz,

capacitors with higher voltage ratings would be required; however, such components typically exhibit higher ESR, which in turn increases conduction losses and thermal stress in the capacitor. As a result, the isolation method proposed in [61] is not practical for these conditions without significant redesign.

Efficiency Overview – Figure 4.17a: Across all cases, the second air-core coil in CLLC mode (CASE 3) demonstrated the highest performance. At 3.5 kW, 350 V, and 1 MHz, the LLC configuration achieved 95.9%, while the CLLC improved slightly to 96%. At 4.2 kW, the CLLC peaked at 96.2%, confirming its suitability for high-power MHz switching applications. In contrast, the ferrite-core design in CASE 4—despite having a similar physical volume—showed the lowest efficiency (86.1%) due to severe core heating. CASE 1’s voltage ripple issues limited testing to 800 W, where it reached 91.3%.

Loss Breakdown – (Figure 4.17b):

- CASE 2 – First air-core coil (LLC): At 4 kW, efficiency reached 94%. Of the total 239 W losses, the air-core coil contributed 148 W (AC resistance $\sim 0.4 \Omega$ per winding). Subtracting coil losses leaves 91 W from conduction and switching, which closely matches the 77 W from thermal measurements—an error margin of $\sim 7\%$. Loss distribution: 62% transformer, 19% SiC diodes, 12% GaN transistors.
- CASE 3 – Second air-core coil (CLLC): At 4.2 kW, efficiency reached 96.2%. Coil losses totaled 55 W; subtracting this from the total 160 W losses leaves 105 W for conduction and switching, closely matching the 93.3 W thermal estimate (error $\sim 8\%$). Transformer loss reduction (34% of total) boosted CLLC efficiency by $\sim 2.2\%$ over LLC. Loss distribution: 37% SiC diodes, 21% GaN transistors. This suggests replacing SiC diodes with GaN switches could further raise efficiency.
- CASE 4 – Ferrite core (LLC): At 3.5 kW and 350 V, excessive core losses caused rapid overheating, lowering efficiency to 86.1%. While lowering power or using more parallel cores could reduce core heating, both approaches increase size. Ferrite designs also require additional inductors for resonance, and introducing an air gap to boost leakage inductance demands more turns—raising AC resistance and further increasing volume.

Spider Chart Comparison – Figure 4.17c: The spider diagram compares all four cases based on transformer type (air-core or ferrite) and topology (LLC or CLLC).

- CASE 1 had the lowest semiconductor losses but suffered from largest volume per kW due to long conductor lengths and high AC resistance at 1 MHz.
- CASE 3 offered the lowest transformer volume per kW, minimal transformer losses, and only a slight increase in semiconductor losses compared to CASE 1—thanks to ZVS and GaN’s low turn-off losses.
- CASE 4’s ferrite-based design had the highest volume per kW when evaluated at its thermally stable operating point (200 V, 2 kW). Despite a smaller core volume (36 cm^3 vs. 53 cm^3 in CASE 3), its losses were higher and efficiency lower, confirming its inferiority for compact MHz designs.

These results clearly demonstrate that air-core transformers, particularly the second design in CLLC operation, deliver superior efficiency, lower thermal stress, and better power density than ferrite-core transformers for compact, high-power isolated DC-DC converters at MHz switching frequencies.

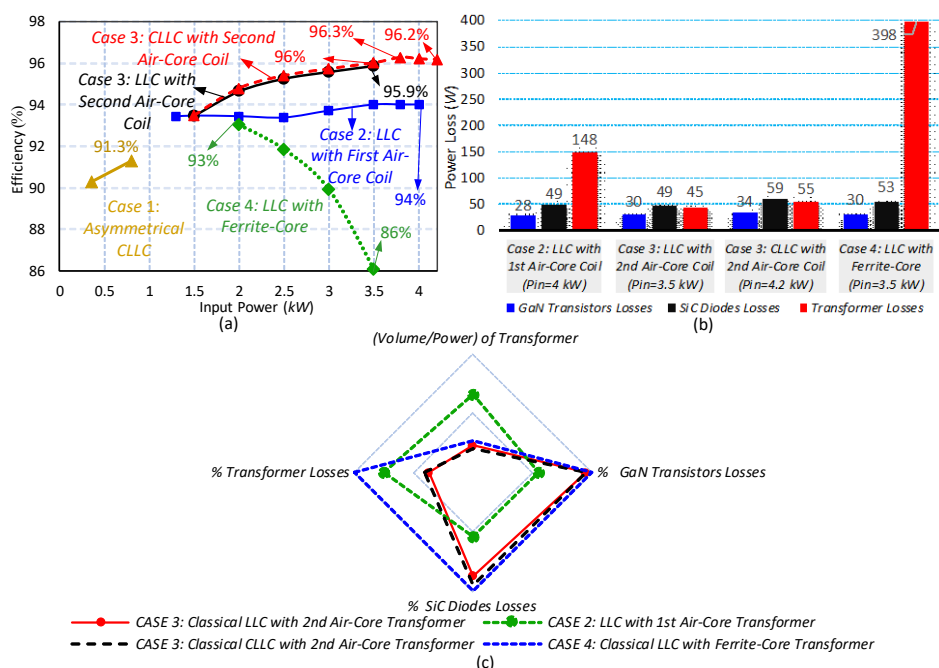


Figure 4.17 (a) Efficiency comparison of four test cases versus input power, (b) measured and calculated loss breakdown for all cases except CASE 1 at maximum tested power, and (c) performance comparison between air-core and ferrite-core transformers.

With the capacitive isolation, at an output power of 5 kW, the converter reaches an efficiency of 95%, and at 5.46 kW, it maintains a high efficiency of 94.55%. These results demonstrate the converter's ability to keep losses minimal across its entire operating range. This performance is primarily attributed to the ZVS switching operation and the integration of low-loss devices such as GaN transistors and SiC diodes. The minimal variation in efficiency between different load levels further confirms the robustness of the design in sustaining high performance.

Figure 4.15d compares the coupled inductor sizes used in magnetic coupling versus capacitive coupling-based converters. Under equivalent testing conditions, the inductive element in the capacitive coupling design is notably smaller, contributing to higher power density and lower overall system cost, while still meeting the same operational requirements. However, capacitors do not provide inherent galvanic isolation, and most safety standards mandate galvanic isolation to protect against electric shock. This requirement is more reliably met using magnetic isolation methods, such as transformers.

4.3 Summary

This section presents a comprehensive investigation into GaN-based DC-DC converter optimization, covering both wide-input non-isolated architectures and high-frequency isolated resonant designs, with an emphasis on achieving maximum efficiency, high power density, and effective thermal management.

For the non-isolated GaN-based DC-DC converter, a 9 kW GaN prototype reached 99% peak efficiency and power densities of 17.7 kW/L (50 kW/L excluding the heatsink) and 6 kW/kg by implementing four key strategies:

1. Utilizing GaN transistors with air-core inductors to eliminate switching frequency constraints and avoid magnetic core saturation.
2. Applying variable switching frequency control to generate negative inductor valley current, enabling full ZVS.
3. Using a suitable TIM to efficiently transfer heat from the GaN transistor junction, especially given the small cooling pad area, ensuring effective thermal management without relying solely on oversized heatsinks.
4. Removing core losses entirely through the use of air-core designs instead of ferrite inductors.
5. Employing a systematic design optimization framework for practical replication.

For the isolated DC-DC converter, experimental evaluation of LLC, CLLC, CI, and asymmetrical CLLC topologies operating above 1 MHz confirmed that ZVS can be sustained at very high frequencies with proper control, though magnetic design remains the dominant loss contributor. Air-core transformers outperformed ferrite designs, achieving up to 96.2% efficiency at 4.2 kW without core loss constraints. In contrast, ferrite cores required flux derating or parallel core arrangements to control heating—both of which increased size and reduced compactness.

A CI-based resonant converter operating at 1.5 MHz and 6 kW demonstrated high efficiency, stable thermal performance, and reduced size by minimizing magnetic volume. Capacitors inherently lack galvanic isolation, and since most safety regulations require it to protect against electric shock, magnetic isolation—typically achieved through transformers—remains the more dependable solution.

Additionally, when designing GaN-based converters, TIM selection is critical. The relatively small top-side thermal pad area of GaN devices can limit heat removal, meaning even high-performance heatsinks or active cooling solutions may underperform if the TIM is poorly chosen. Ensuring optimal thermal transfer between device and heatsink is therefore essential for sustaining high efficiency and reliability.

In summary, combining GaN transistors with air-core magnetics and optimized control strategies enables exceptional performance in both isolated and non-isolated systems. For MHz-range isolated designs, air-core transformers deliver the best efficiency–size trade-off, while capacitive coupling offers superior compactness and cost advantages in applications where safety-compliant galvanic isolation is not required.

5 Control Strategy for Ultra-High-Frequency Operation and Experimental Results of the Proposed OBC Systems

This section presents a control framework and experimental validation for the proposed OBC systems introduced in Section 3. Two OBC configurations are considered: (i) a three-phase unfolding-based PFC employing two inductors, and (ii) a UOBC capable of charging an EV battery from single-/three-phase AC as well as two-/three-wire DC grids.

To enable ultra-high-frequency operation, a Finite Cycle-Based Model Predictive Control (FCB-MPC) based cycle-skipping control strategy is developed as a feasible solution for the isolated DC-DC stage. The approach integrates a soft-switched resonant converter into the charging architecture and employs a finite cycle-based model predictive control scheme that allocates discrete switching cycles among different energy transfer paths. Operating at a 25 kHz sampling rate, with 40 switching cycles per interval (corresponding to a 1 MHz switching frequency), the method achieves fine-grained 2.5% power regulation while maintaining sinusoidal grid currents and a high PF. This control method completely is discussed in [PAPER-VII].

Unlike conventional chargers that rely on three inductors and a separate low-frequency PFC stage, the proposed architecture embeds PFC functionality directly into the high-frequency DC-DC stage. This integration significantly increases power density and reduces system size. A soft-switching modulation scheme ensures ZVS across all GaN transistors even in the hundreds of kilohertz to megahertz range, thereby minimizing switching losses.

Experimental validation was performed on two prototypes. The first is a 3.6 kW laboratory setup demonstrating the unfolding-based PFC with a high-frequency DC-DC stage. The second is an 11 kW UOBC prototype, verified up to 800 V battery voltage and 8 kW transfer, achieving over 95% efficiency and 4.3 kW/L (6.7 kW/L excluding the heatsink) power density. GaN devices with high-frequency operation (100 kHz rectifier, 1 MHz DC-DC stage) reduce magnetic size, improve thermal performance, and increase density. Air-core transformers remove core losses and handle high currents, while soft-switching further minimizes switching losses.

5.1 FCB-MPC-Based Cycle-Skipping Control Method

As shown in Figure 3.1, the three-phase unfolding-based PFC system employs two inductors connected to a 3LA-CLLC-FB-IPT converter serving as the DC-DC stage. This stage shapes the currents in L_1 and L_2 to match the AC input currents and regulates the output voltage, while also providing galvanic isolation through a high-frequency transformer. Operating in the several-hundred-kilohertz to megahertz range, it manages both energy conversion and control.

5.1.1 3LA-CLLC-FB-IPT DC-DC Stage Description

The CLLC full-bridge converter is widely used in medium- and high-power isolated DC-DC applications due to its capability for soft-switching, making it ideal for systems such as battery chargers. In this work, a modified variant—referred to as the 3LA-CLLC-FB-IPT—is adopted for the DC-DC stage, as shown in Figure 3.1 and Figure 5.1. This design differs from a conventional three-level bridge in that the DC-link is asymmetrically split, which enables a specialized cycle-skipping modulation method rather than standard CLLC leg-to-leg control.

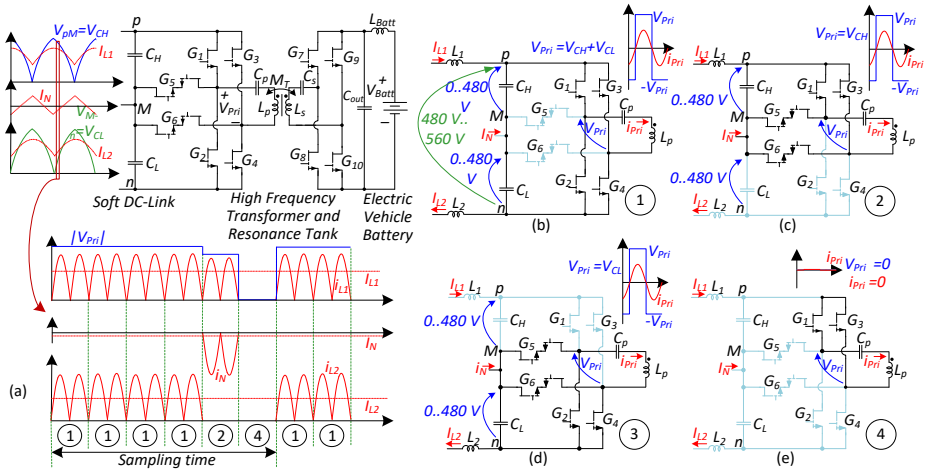


Figure 5.1 Equivalent circuits of the 3LA-CLLC-FB-IPT DC-DC stage operating under ZCS, plus a conceptual diagram of the cycle-skipping control used to regulate input current [PAPER-VII].

The converter can be modeled as a three-port system: two series-connected input ports, each tied to a different half of the soft DC-link, and a single output port. Operating close to its resonant frequency (hundreds of kHz up to several MHz) allows all GaN switches to achieve ZVS turn-on, effectively removing C_{OSS} and turn-on losses while minimizing turn-off losses. The switching frequency $f_{SW,DC-DC}$ is defined as $N_R \times f_{sampling}$, where N_R determines both the number of high-frequency cycles executed per sampling interval and the achievable control resolution. Higher N_R values yield finer control of inductor currents i_{L1} and i_{L2} , as well as the input grid current.

Both input sections contribute to a three-level primary voltage waveform V_{pri} (Figure 5.1a). Within each sampling period, four switching states are available: Full-state (Figure 5.1b): draws power from both DC-link sections, controlling both inductors; Up-state (Figure 5.1c): draws from the upper DC-link, mainly controlling i_{L1} ; Down-state (Figure 5.1d): draws from the lower DC-link, mainly controlling i_{L2} ; and Zero-state (Figure 5.1e): no power transfer, freewheeling mode. The number of each state's cycles—denoted n_{Full} , n_{Up} , n_{Down} , and n_{Zero} —determines how energy is shared between inductors and must satisfy:

$$N_R = n_{Full} + n_{Up} + n_{Down} + n_{Zero} \quad (5-2)$$

This control method allows precise shaping of inductor currents while maintaining high efficiency and compact magnetics, supporting a lightweight and space-efficient EV charger architecture.

5.1.2 Modulation Scheme of the Cycle Skipping Control

The three-level converter legs can connect the bridge input to the positive (p), midpoint (M), or negative (n) terminals of the DC-link. Unequal DC-link voltages expand the available unique states to seven, as summarized in Table 5.1. Among these, the zero-voltage state can be achieved through three redundant switching combinations.

The cycle counts n_{Full} , n_{Up} , n_{Down} , and n_{Zero} are adjusted to keep the grid currents sinusoidal for PFC, while the absolute sum of these cycles sets the delivered power.

The average inductor currents I_{L1} and I_{L2} over a sampling period are related to the full/up/down states by:

$$I_{L1} = \left(\frac{n_{Full}}{N_R} + \frac{n_{Up}}{N_R} \right) \frac{8}{\pi^2} \frac{V_{Batt}}{\omega_0 M_T}; \quad I_{L2} = \left(\frac{n_{Full}}{N_R} + \frac{n_{Down}}{N_R} \right) \frac{8}{\pi^2} \frac{V_{Batt}}{\omega_0 M_T}, \quad (5-3)$$

where ω_0 is the angular resonant frequency and M_T is the transformer's mutual inductance.

As shown in Figure 4, the controller distributes cycles according to the relationship between I_{L1} and I_{L2} . If I_{L1} exceeds I_{L2} , shared full cycles n_{Full} follow I_{L2} and the surplus of I_{L1} is managed with n_{Up} , while n_{Down} is unused. Conversely, when I_{L2} is higher, n_{Full} follows I_{L1} and the excess is assigned to n_{Down} , leaving n_{Up} at zero. In the balanced case ($I_{L1} = I_{L2}$), all current is handled by n_{Full} , with no need for n_{Up} or n_{Down} . The DC-DC stage runs at a fixed frequency near to the primary tank resonance, as in conventional CLLC converters. To maintain ZVS at every transition, the resonant capacitors are intentionally made asymmetrical—specifically, which is discussed in [61], the secondary-side capacitor is reduced—introducing a slight inductive load characteristic that keeps current flowing at turn-on. Table 5.1 The asymmetrical capacitor arrangement ensures that primary current is sufficient to discharge C_{OSS} before turn-on, improving efficiency.

Table 5.1 Switching states of the 3-level leg and their corresponding primary-side voltages [PAPER-VII].

Cycle Name	Positive Leg of Primary	Negative Leg of Primary	Primary Side Voltage V_{Pri}	Voltage Range (V)	Related Figure
Full-Cycle	$G_1: \text{ON}, G_2: \text{OFF}$	$G_4: \text{ON}, G_3: \text{OFF}$	$V_{pn} = V_{CH} + V_{CL}$	480... 560	Figure 5.1b
	$G_1: \text{OFF}, G_2: \text{ON}$	$G_4: \text{OFF}, G_3: \text{ON}$	$V_{np} = -(V_{CH} + V_{CL})$	-560... -480	
Up-Cycle	$G_1: \text{ON}, G_5: \text{OFF}$	$G_6: \text{ON}, G_3: \text{OFF}$	$V_{pM} = V_{CH}$	0... 480	Figure 5.1c
	$G_1: \text{OFF}, G_5: \text{ON}$	$G_6: \text{OFF}, G_3: \text{ON}$	$V_{Mp} = -V_{CH}$	-480... 0	
Down-Cycle	$G_5: \text{ON}, G_2: \text{OFF}$	$G_4: \text{ON}, G_6: \text{OFF}$	$V_{Mn} = V_{CL}$	0... 480	Figure 5.1d
	$G_5: \text{OFF}, G_2: \text{ON}$	$G_4: \text{OFF}, G_6: \text{ON}$	$V_{nM} = -V_{CL}$	-480... 0	
Zero-State Cycle	$G_1: \text{ON}, G_2: \text{OFF}, G_5: \text{OFF}$	$G_3: \text{ON}, G_4: \text{OFF}, G_6: \text{OFF}$	0	0	Figure 5.1e
	$G_2: \text{ON}, G_1: \text{OFF}, G_5: \text{OFF}$	$G_4: \text{ON}, G_3: \text{OFF}, G_6: \text{OFF}$			
	$G_5: \text{ON}, G_1: \text{OFF}, G_2: \text{OFF}$	$G_6: \text{ON}, G_3: \text{OFF}, G_4: \text{OFF}$			

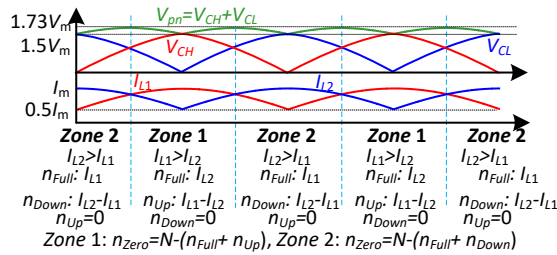


Figure 5.2 Dynamic cycle allocation method that adjusts for inductor current imbalance to achieve optimal power sharing and precise current shaping [PAPER-VII].

5.1.3 FCB-MPC-Based Cycle Skipping Control System

Figure 5.3 illustrates the complete control architecture of the proposed system. The front-end, consisting of the three-phase unfolding stage, operates at twice the mains frequency (as shown earlier in Figure 3.2) and is directly coupled to the high-frequency 3LA-CLLC-FB-IPT DC-DC stage. This DC-DC stage is tasked with regulating power transfer

and shaping the grid-side inductor currents. Control is performed using an independently tuned FCB-MPC algorithm, chosen for its straightforward implementation and fast dynamic response.

For clarity, consider a control algorithm with a 25 kHz sampling rate. In this setup, the controller can handle 40 high-frequency cycles within each sampling interval, giving an effective switching frequency of 1 MHz. These cycles are allocated across three energy transfer modes: Full-path (n_{Full}), which transfers energy from both capacitors simultaneously; Upper v-path (n_{Up}), which draws current only from the upper capacitor; and Lower-path (n_{Down}), which draws current only from the lower capacitor.

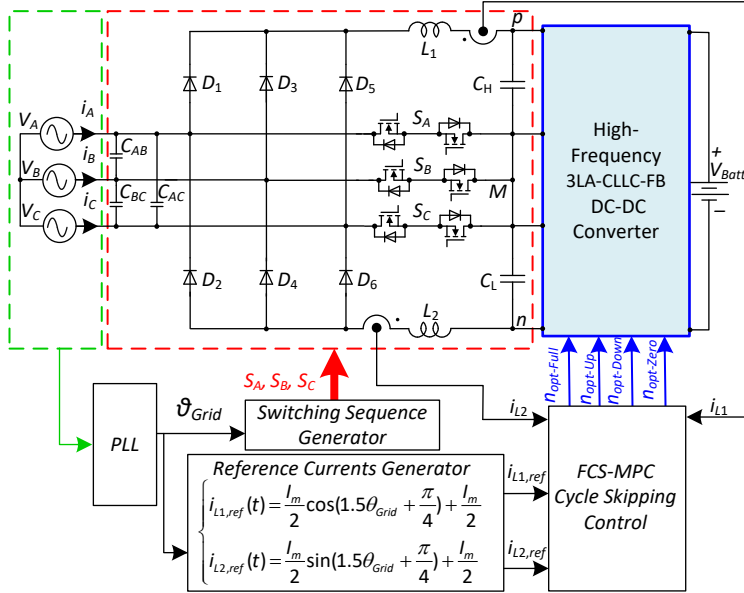


Figure 5.3 Overall control framework combining the three-phase unfolding rectifier with the high-frequency 3LA-CLLC-FB IPT DC-DC converter to regulate power and shape grid currents [PAPER-VII].

This cycle-allocation method enables precise shaping of inductor currents while preserving soft-switching operation and minimizing switching losses. The controller uses a simplified linear prediction model to estimate the change in inductor current over a given number of switching cycles:

$$\Delta i_L(n) = \frac{n_{Cycle}}{N_R} \frac{8}{\pi^2} \frac{V_{Batt}}{\omega_0 M_T}. \quad (5-4)$$

Here, $\Delta i_L(n)$ denotes the expected change in current over n_{Cycle} cycles.

At each sampling instant, the algorithm determines the optimal values of n_{Full} , n_{Up} , and n_{Down} by minimizing a cost function based on the absolute tracking error between the measured inductor currents and their references:

$$\begin{aligned} i_{L1,ref} > i_{L2,ref} &\rightarrow g_{Full} = |i_{L2,ref} - \Delta i_{L,Full}(n_{opt-Full})|; g_{Up} = |(i_{L1,ref} - i_{L2,ref}) - \Delta i_{L,Up}(n_{opt-Up})| \\ i_{L2,ref} > i_{L1,ref} &\rightarrow g_{Full} = |i_{L1,ref} - \Delta i_{L,Full}(n_{opt-Full})|; g_{Up} = |(i_{L2,ref} - i_{L1,ref}) - \Delta i_{L,Down}(n_{opt-Down})| \\ i_{L2,ref} = i_{L1,ref} &\rightarrow g_{Full} = |i_{L1,ref} - \Delta i_{L,Full}(n_{opt-Full})| \end{aligned} \quad (5-5)$$

A brute-force search evaluates all permissible integer combinations of n_{Full} , n_{Up} , and n_{Down} under the constraint $N_R \geq n_{Opt-Full} + n_{Opt-Up} + n_{Opt-Down}$. The combination yielding the smallest overall tracking error is selected for implementation.

Once determined, these cycle counts directly set the gating patterns of the 3LA-CLLC-FB-IPT converter. Any remaining cycles are unused switching cycles $n_{Opt-Zero} = N_R - n_{Opt-Full} + n_{Opt-Up} + n_{Opt-Down}$.

The simulation waveforms and analysis of the proposed FCB-MPC control method are provided in [PAPER-VII]. Furthermore, in [61], the cycle-skipping approach for voltage and current regulation was experimentally verified in a high-frequency CLLC-FB-IPT DC-DC stage operating at a 500 kHz switching frequency and 5 kW nominal power, where cycle skipping of up to 90% was demonstrated and validated.

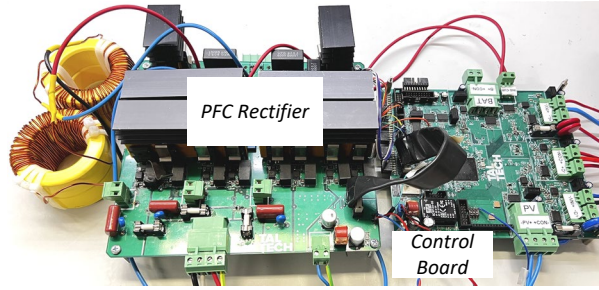


Figure 5.4 Laboratory prototype of the proposed Unfolding-Based PFC [PAPER-VI].

5.2 Experimental Results the Proposed Three-Phase Unfolding-Based PFC Connecting to Grid

To verify the performance of the proposed two inductor three-phase unfolding-based PFC topology, the theoretical analysis presented in section 3 and [PAPER-VI] was complemented with experimental validation using a laboratory-built prototype. A photograph of the constructed prototype is shown in Figure 5.4.

The grid connected experimental tests were conducted at an output power level of 3.6 kW, with the three-phase grid voltages set to 50% of their nominal values. In this setup, two independent conventional high-frequency buck-boost converters were connected to the DC-link capacitors C_H and C_L , each supplying a separate load. These converters acted in place of the high-frequency DC-DC converters illustrated in Figure 3.1, serving as the interface between the loads and the proposed PFC stage.

In the implemented system, the reference currents i_{L1} and i_{L2} for the filter inductors L_1 and L_2 were regulated independently by adjusting the duty cycles of the buck-boost converters. This allowed precise control of the inductor currents, thereby enabling the desired PFC functionality.

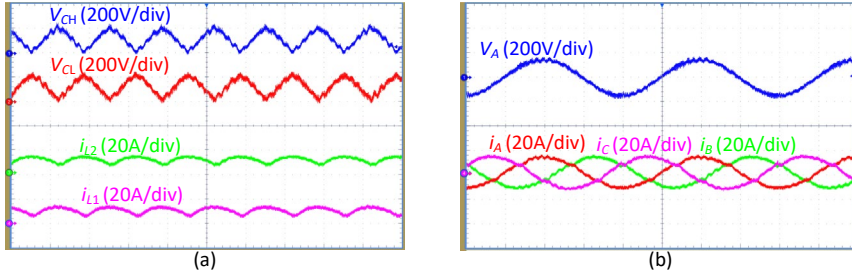


Figure 5.5 Laboratory Experimental waveforms of the proposed three-phase unfold: (a) DC-link capacitor voltages (V_{CH} , V_{CL}) and inductor currents (i_{L1} , i_{L2}); (b) grid phase-to-phase voltage (V_A) and grid phase currents (i_A , i_B , i_C) [PAPER-VI].

The measured experimental waveforms are presented in Figure 5.5. As shown in Figure 5.5a, the currents through inductors L_1 and L_2 are effectively regulated, with peak values reaching 15 A, confirming the accuracy and stability of the control strategy presented in [PAPER-VI]. The figure also includes the voltage profiles of the DC-link capacitors, further validating the correct operation of the proposed structure. Figure 5.5b shows the grid currents and voltage V_A , confirming that power factor correction is achieved by regulating inductor currents L_1 and L_2 using only two current sensors.

5.3 Experimental Results of the Proposed UOBC

A laboratory prototype of the proposed 11 kW system (Figure 5.6) was constructed to validate performance. The rectifier stage operates at 100 kHz, while the isolated DC-DC stage runs at 1 MHz, supporting battery voltages up to 800 V. Key electrical and mechanical parameters for all active and passive elements are summarized in Table 5.2, with control implemented on a TMS320F28379DPTPT digital controller.

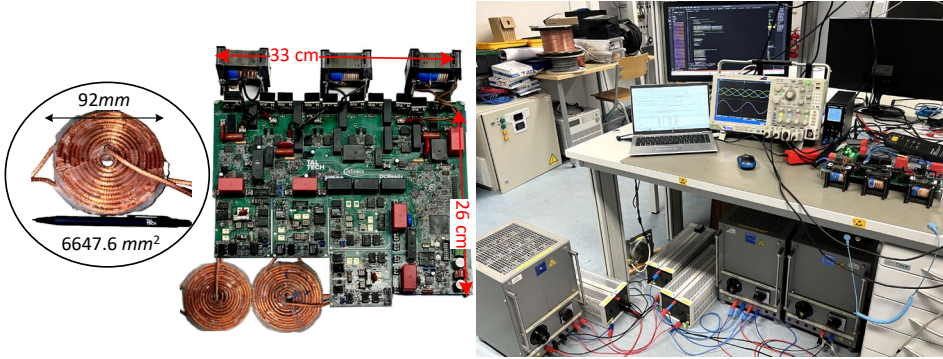


Figure 5.6 Photographs of the laboratory prototype and experimental test setup of the UOBC.

With passive cooling, the charger achieves a power density of 4.3 kW/L (6.7 kW/L excluding the heatsink), based on a 2.57 L total volume including magnetics, capacitors, and thermal hardware. The DC-DC stage employs air-core transformers to avoid core losses at high frequency and high power. Most components are PCB top-mounted, except for GaN devices (optimized for top-side heat extraction), SiC MOSFETs, and certain decoupling capacitors, which are mounted on the underside. All semiconductors share a single 2.5 cm-thick heatsink beneath the PCB, spanning most of the board for uniform heat removal.

5.3.1 Experimental Waveforms of the UOBC Laboratory Test

The DC-DC stage was tested with each CLLC converter running at 1 MHz, supplied with 360 V (equivalent to a 720 V battery) and delivering 1.5 kW to 4.5 kW. Under these conditions, ZVS was achieved for all switches. As shown in Figure 5.7a, the transformer's primary/secondary currents and the drain–source voltages of switches G_9 and G_{10} were recorded during battery discharge. ZVS was facilitated by 15 nF resonant capacitors (C_{r1} , C_{r2}) on both transformer sides, requiring roughly 18 A turn-off current to fully charge/discharge the device output capacitances each cycle.

Table 5.2 Specifications of the proposed UOBC Prototype.

Components Specifications	
Suppression Capacitors (C_{SA} , C_{SB} and C_{SC})	Ceramic Type, 1.8 μF , 630 V
Resonant Capacitors C_{r1} and C_{r2}	Ceramic Type, 15 nF, 650 V
DC-Link and DC-DC Output Capacitors (C_H , C_L , C_{O-H} and C_{O-L})	Film Type, 42 μF , 500 V
Battery Capacitor C_S	Film Type, 9 μF , 1000 V
Decoupling Capacitor C_D	Film Type, 195 μF , 500 V
Filtering Inductors (L_A , L_B and L_C)	ETD 59/31/22-N97, 4 $^{\circ}C/W$ Thermal Resistance, 260 μH , 20 m Ω
Air-core transformer(L_P , L_S , M_T)	Wound with 3000 Strands of 0.05 mm Litz Wire, Turns Ratio $N_P = N_S = 11$, 5.9 $\mu H/5.9 \mu H/3.9 \mu H$
Semiconductor Devices	
SiC MOSFETs of Rectifier Stage ($S_1 - S_8$)	Infineon Technologies, IMZA120R014M1HXKSA1, 1200 V, 14 m Ω
GaN Transistors of Rectifier and DC-DC stages ($S_9 - S_{12}$) and ($G_1 - G_{16}$)	Infineon Technologies, GaN FETs Automotive GS-065-060-5-T-A-MR, 60A, 650V
Solid-State Circuit Breakers SiC MOSFETs ($SSCB_1$ and $SSCB_2$)	Infineon Technologies, IMZA120R007M1HXKSA1, 1200 V, 7 m Ω
Solid State Relay SW_1	ADJH21112, 50 A
Solid State Relays SW_2 and SW_3	T9GV5L14-12, 30 A
Operating Parameters	
Peak AC Three/Single Phase Voltages	320 V
Maximum Battery voltage V_{Batt}	800 V
Maximum Battery Charging Power P_{Batt}	11 kW
Switching frequency	PFC Stage f_{SW_PFC} : 100 kHz, DC-DC Stage f_{SW_DC-DC} : 1 MHz
Thermal Management [74]	
TIM for GaN Transistors, $R_{\theta JC} = 0.5 \text{ }^{\circ}C/W$	TG-A1780- 150-150-0.8 TIM 1.38 $^{\circ}C/W$
TIM for SiC MOSFETs, $R_{\theta JC-PFC} = 0.51 \text{ }^{\circ}C/W$	SP1500ST0.008-02-1012 TIM 0.67 $^{\circ}C/W$

Figure 5.7b depicts transistor voltage, input current, and output current waveforms, showing minimal current ripple. After half hour of continuous operation at these settings, thermal imaging (Figure 5.7c and Figure 5.7d) showed the air-core transformer reaching about 101 $^{\circ}C$ at 13.4 A RMS (calculated by equation (3-23)). With a winding thermal resistance of 2.7 $^{\circ}C/W$ and 30 $^{\circ}C$ ambient, losses per winding were estimated at 22.6 W, totaling 45.2 W per coil, corresponding to an AC resistance of $\sim 0.126 \Omega$ at 1 MHz.

The GaN switches exhibited a 22 $^{\circ}C$ temperature rise between junction (63.3 $^{\circ}C$) and heatsink (41 $^{\circ}C$), implying about 11.7 W dissipation per device. With four transistors per side of each module, semiconductor losses totaled 46.8 W for the primary and the same for the secondary, giving 93.6 W overall. While ZVS reduced C_{OSS} -related turn-on losses, the large transformer current of the air-core design increased turn-off losses. Nonetheless, thermal margins remained safe, leaving headroom for higher power or frequency operation.

At 4.3 kW per module, the converter's efficiency was 96.7%. Deducting the 45 W coil losses from the measured 142 W total system loss leaves 97 W attributable to switching and conduction—closely matching the 93.6 W estimated from thermal analysis, confirming strong agreement between electrical and thermal performance data.

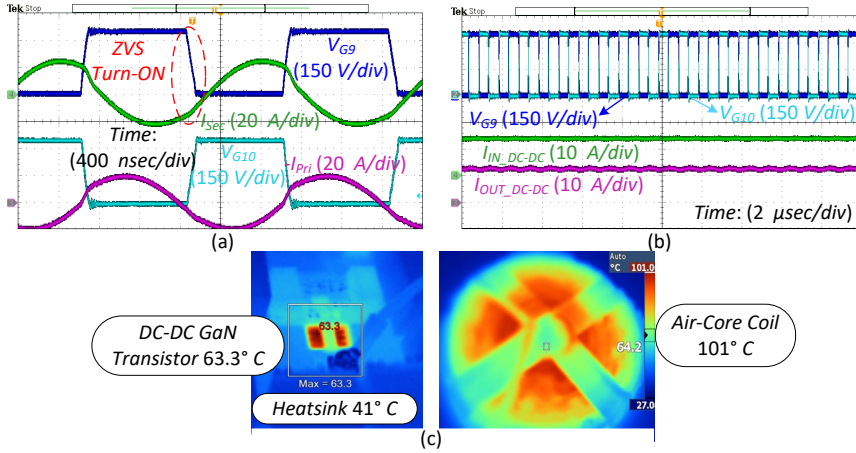


Figure 5.7 Experimental waveforms and thermal images of the DC-DC stage at 8.6 kW discharge, 720 V battery voltage, and 1 MHz switching: (a) primary/secondary currents (I_{Pri} , I_{Sec}) with drain-source voltages of G_9 and G_{10} ; (b) drain-source voltages of G_9 and G_{10} with module input/output currents; (c) thermal image of GaN transistors; (d) thermal image of the air-core transformer.

Figure 5.8 presents a set of significant experimental findings that demonstrate the performance of the proposed system when functioning in inverter mode during battery discharge operation. In Figure 5.8a, the test case corresponds to three-phase inverter operation where the system delivers 8 kW of output power from a 730 V battery pack to the three-phase AC output. The measured waveforms include the voltages of all three phases (V_A , V_B , and V_C) as well as the current flowing through phase A. Under these conditions, each phase voltage reached a peak value of approximately 325 V, while the peak phase current was measured at around 16 A. These measurements confirm the system's ability to generate balanced three-phase output voltages and currents under high-power operation, maintaining waveform integrity while operating from a high-voltage DC source.

In Figure 5.8b, the system is operated in single-phase inverter mode with a load power of 3 kW, still using a 730 V battery as the DC source. The recorded traces capture the voltage across phase A (V_A), the corresponding current (i_A), the voltage measured across the power decoupling capacitor (V_{CD}), and the current through the decoupling inductor (L_C). In this configuration, the phase A voltage reaches a peak of about 315 V, while the current peaks at roughly 19 A. The decoupling capacitor voltage exhibits a clear 100 Hz ripple, corresponding to twice the mains frequency, with a peak-to-peak swing of approximately 230 V centered around a mean value of 215 V. Simultaneously, the current through the decoupling inductor peaks at around 14 A. These results align with the theoretical prediction of equation (3-13) and demonstrate that the active power decoupling stage effectively compensates for the double-frequency power oscillations in both single-phase charging G2V and discharging V2G modes.

Following a 30-minute operation in three-phase inverter mode at 8 kW output power, a series of thermal measurements was carried out to assess the temperature rise of the

key components, namely the filter inductors, GaN transistors, and SiC MOSFETs in the PFC section. In Figure 5.8c, the thermal image of inductor L_A is shown. Each input inductor was measured to have a winding resistance of 20 m Ω , and with an RMS current of 11.3 A, the conduction loss per inductor was calculated to be approximately 2.6 W. Therefore, the combined conduction loss for all three inductors is about 7.8 W. The inductor core temperature was recorded at 32.2 $^{\circ}\text{C}$. Considering an ambient temperature of 30 $^{\circ}\text{C}$ and a thermal resistance of 4 $^{\circ}\text{C}/\text{W}$ for the ETD59/31/22 core, the core losses for each inductor were estimated at 0.6 W, resulting in a total of 1.8 W for all phases. This brings the total losses associated with the inductors (conduction plus core) to roughly 9.6 W.

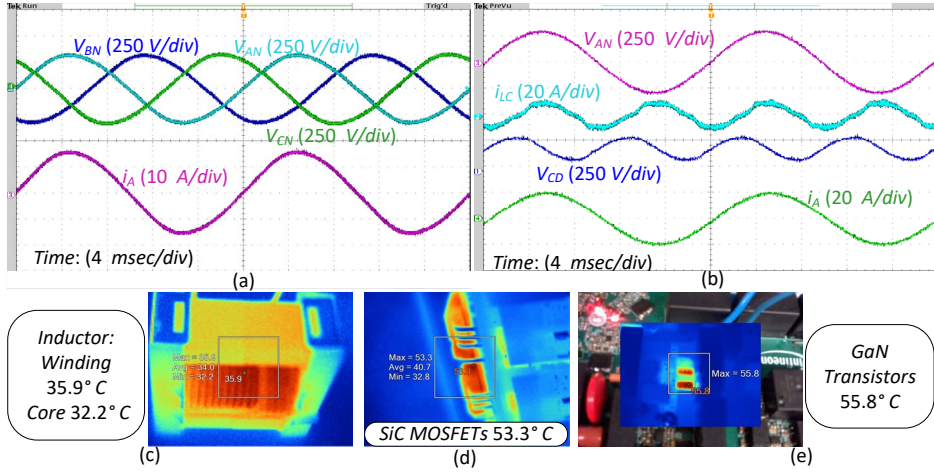


Figure 5.8 Experimental waveforms and thermal images of the DC-AC stage in battery discharge mode for three-phase and single-phase operation: (a) three-phase voltages (V_{AN} , V_{BN} , V_{CN}) with phase current i_A at 8 kW, 720 V; (b) single-phase operation showing V_A , i_A , decoupling inductor current i_{LC} , and capacitor voltage V_{CD} at 3.2 kW, 720 V; (c) thermal image of filter inductor L_A at 8 kW three-phase; (d) thermal image of SiC MOSFETs S_1 , S_2 at 8 kW three-phase; (e) thermal image of GaN switches S_{12} at 8 kW three-phase.

Thermal pictures for the semiconductor devices are illustrated in Figure 5.8d and Figure 5.8e. The SiC MOSFETs S_3 and S_4 exhibited a maximum recorded temperature of 53.3 $^{\circ}\text{C}$, while the GaN transistors S_{12} reached 55.8 $^{\circ}\text{C}$, with the shared heatsink maintained at 39 $^{\circ}\text{C}$. From these readings, the estimated conduction and switching losses for each SiC MOSFET were about 12.1 W, whereas each individual GaN transistor dissipated around 8.9 W. It should be noted that the S_{12} switch is implemented as a four-quadrant configuration composed of two GaN devices; therefore, the total power loss per S_{12} switch is approximately 17.8 W. The SSCB MOSFETs, on the other hand, displayed only a minor temperature increase during operation. By analytical estimation, considering their 7 m Ω on-resistance and an RMS current of 11.3 A, the conduction loss for each SSCB device was calculated to be roughly 1.8 W, resulting in a combined loss of 3.6 W across all three phases. When summing the losses from inductors, semiconductors, and SSCBs, the inverter stage was determined to dissipate approximately 139.2 W at the 8 kW operating point. This yields a calculated efficiency of 98.3%, which is in very close agreement with the 98.2% efficiency measured directly using a power analyzer.

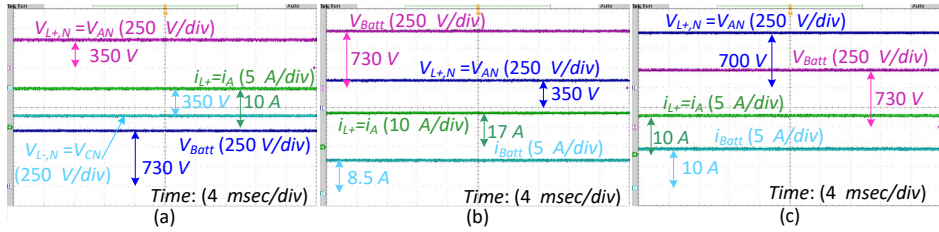


Figure 5.9 UOBC waveforms in battery discharge mode: (a) three-wire 350 V DC grid at 7 kW, (b) two-wire 350 V DC grid at 6 kW, (c) two-wire 700 V DC grid at 7 kW.

Figure 5.9 shifts focus to the operation of the system in battery discharging mode when connected to various DC grid configurations, representing the DC-DC operating stage of the converter. In Figure 5.9, the system is connected to a three-wire DC grid configuration, delivering a total output power of 7 kW. The input battery voltage during the test was 730 V. The DC load voltages were regulated to +350 V and -350 V, each supplying 10 A of load current. The recorded waveforms include V_{AN} (measured as $V_{L+,N}$), V_{CN} (measured as $V_{L-,N}$), the current through inductor L_A , and the battery voltage V_{Batt} .

In Figure 5.9b, the configuration changes to a two-wire 350 V DC grid scenario, with the system delivering 6 kW of output power. The battery voltage was again 730 V, while the output current to the DC load reached 17 A. The measured waveforms here include V_{AN} , i_{LA} , and V_{Batt} , confirming stable operation under this configuration.

Figure 5.9c presents the test results for a two-wire 700 V DC grid connection. In this case, the output power was 7 kW, with the DC output voltage $V_{L+,N}$ regulated at 700 V and an output current of 10 A. The battery voltage was held at 730 V during the test.

Across all DC grid configurations tested—three-wire at ± 350 V, two-wire at 350 V, and two-wire at 700 V—the system maintained stable performance, validating that the proposed battery discharging stage can interface seamlessly with multiple DC grid architectures while delivering consistent power levels.

5.3.2 Efficiency Analysis of the Proposed UOBC

The efficiency performance of the proposed universal onboard charger was assessed through both analytical loss calculations and experimental measurements, providing a detailed understanding of its operation under various conditions.

Figure 5.10a presents the calculated loss distribution of the PFC stage during three-phase AC operation over an output power range from 2 kW to 11 kW. The results indicate that the dominant loss sources are the SiC MOSFETs and GaN transistors, with switching losses contributing more significantly than conduction losses due to the hard-switching nature at 100 kHz. At an output power of 8 kW, the analytical loss breakdown shows 68.7 W for the SiC MOSFETs, 47.2 W for the GaN transistors, 8.1 W for the input inductors, and 3 W for the SSCB devices. These values closely correspond to thermal-imaging measurements, which recorded losses of 72.6 W, 53.4 W, 7.8 W, and 3.6 W, respectively, confirming the accuracy of the loss model.

Figure 5.10b illustrates the theoretical loss breakdown in the DC-DC stage, operating at a switching frequency of 1 MHz. Losses are predominantly attributed to the GaN devices—particularly turn-off switching losses—and the conduction losses in the air-core transformer windings. Even though skin effect is mitigated through the use of 3,000 strands of 0.05 mm Litz wire, the proximity effect remains significant, increasing the AC

resistance to approximately 0.126Ω at 1 MHz. At 8 kW output power, calculated losses are 170 W for the GaN transistors and 76.8 W for the transformer, which closely match measured values of 187.2 W and 90.4 W at 8.6 kW input power.

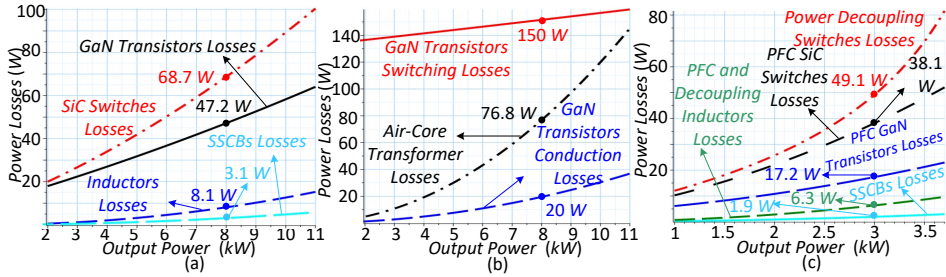


Figure 5.10 Loss breakdown of charger stages: (a) PFC losses under three-phase AC (2–11 kW), (b) 1 MHz DC-DC stage losses highlighting GaN switching and transformer conduction, (c) PFC losses under single-phase AC (1–3.7 kW) including active decoupling losses.

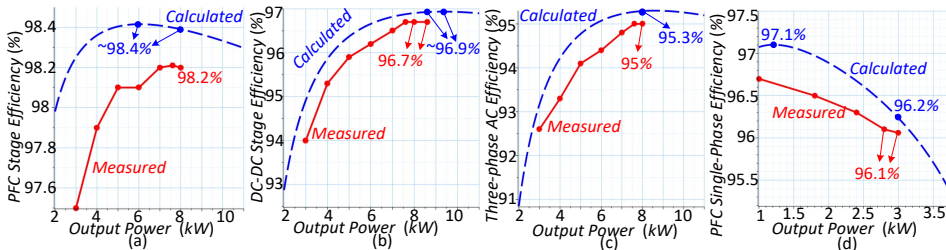


Figure 5.11 Theoretical and experimental efficiency results: (a) PFC stage in three-phase AC mode, (b) 1 MHz CLLC resonant DC-DC stage, (c) overall system efficiency in three-phase AC, and (d) PFC stage efficiency in single-phase AC.

Figure 5.10c shows the PFC stage loss profile under single-phase AC operation for output power levels ranging from 1 kW to 3.7 kW. In this case, the active power decoupling circuit contributes almost as much to total losses as the single-phase inverter or rectifier section. At 3 kW, analytical results show that the active decoupling stage dissipates 49.1 W in the switches and 2.9 W in its inductor, totaling 52 W. The inverter/rectifier stage, in comparison, exhibits 38.1 W in SiC MOSFETs, 17.2 W in GaN transistors, 3.4 W in the filter inductor, and 1.9 W in the SSCBs—summing to 60.6 W. This leads to a combined loss of 112.6 W at 3 kW, slightly lowering the overall efficiency in single-phase mode.

The combined efficiency results for the PFC stage, DC-DC stage, and the complete charger system under various operating modes are presented in Figure 5.11.

- Figure 5.11a: For the PFC stage under three-phase AC operation, the highest theoretical efficiency is achieved at 6 kW and remains nearly constant up to 8 kW, reaching about 98.4%. The measured efficiency at 8 kW is 98.2%, closely aligning with analytical predictions.
- Figure 5.11b: In the DC-DC stage operating at 1 MHz, peak measured efficiency reaches 96.7% between 8 kW and 8.6 kW, in close agreement with the calculated value of 96.9% for the same range.
- Figure 5.11c: For the complete UOBC under three-phase AC input, the measured efficiency is 95%, which closely matches the theoretical prediction of 95.3%.

- Figure 5.11d: Under single-phase AC operation, the active decoupling circuit introduces additional losses that slightly lower efficiency. The highest theoretical efficiency, 97.1%, occurs at approximately 1.2 kW, dropping to 96.2% at 3 kW. Experimental measurements at 3 kW yield 96.1%, again demonstrating strong agreement with theory.

Overall, the close correlation between theoretical predictions, thermal loss estimations, and experimental measurements across all modes confirms both the robustness of the analytical models and the design accuracy of the proposed UOBC.

5.4 Summary

This section introduced an FCB-MPC control strategy for GaN-based OBC systems, validated for two configurations: (i) a three-phase unfolding-based PFC rectifier using only two inductors, and (ii) a UOBC compatible with single-/three-phase AC inputs and two-/three-wire DC grids. These architectures target compact, efficient, and flexible EV charging solutions.

The proposed cycle-skipping FCB-MPC was applied to the isolated DC-DC stage, allocating MHz-range switching cycles among multiple energy paths. This enabled fine power regulation, sinusoidal grid currents, unity power factor, and ZVS for all GaN switches. Operating with kHz-rate sampling and MHz switching, the method ensured reliable soft-switching and high-frequency operation in both OBC configurations.

Compared to conventional chargers requiring three inductors and low-frequency PFC, the unfolding-based PFC embeds current shaping directly into the high-frequency DC-DC stage, reducing magnetic count, improving power density, and simplifying sensing. Air-core magnetics eliminated core losses and supported high-current handling, while soft-switching minimized losses at MHz frequencies.

Experimental validation confirmed these benefits. A 3.6-kW prototype achieved correct DC-link balancing on the three-phase grid, sinusoidal currents with <3% THD, and reliable PFC using only two inductors. The 11-kW UOBC prototype demonstrated charging up to 8 kW at 800 V, > 95% efficiency, and 4.3 kW/L power density under passive cooling (6.7 kW/L excluding the heatsink), with verified universal compatibility across AC and DC grid connections. Thermal imaging showed uniform device cooling, oscilloscope waveforms confirmed ZVS, and loss analysis identified GaN switching and transformer conduction as the main losses, effectively reduced by soft-switching and air-core design.

In conclusion, combining GaN devices, air-core magnetics, and FCB-MPC control establishes a scalable and globally adaptable OBC platform, delivering compactness, high efficiency, and reliable performance for both G2V and V2G applications.

6 Conclusions and Future Work

This thesis has presented a comprehensive study of next-generation OBC technologies for EVs, focusing on three aspects: advanced OBC architectures, GaN-based high-efficiency DC-DC converters, and model predictive control strategies designed for MHz-range operation. Together, these contributions build a scalable foundation for compact, efficient, and globally adaptable EV charging systems.

As the results of thesis, the author can claim the following:

- The first contribution introduced two OBC solutions. The three-phase unfolding-based PFC rectifier achieves grid-side PFC with only two inductors instead of three, lowering magnetic count, cost, and current sensor requirements while maintaining performance. Its effectiveness was confirmed through theoretical analysis and a 3.6 kW prototype. The second solution, a UOBC, operates seamlessly with single-/three-phase AC and two-/three-wire DC grids without hardware changes. Using SiC and GaN switches at 100 kHz (rectifier) and 1 MHz (DC-DC), it minimizes magnetic size, employs air-core transformers to handle ripple without saturation, and supports bidirectional G2V and V2G operation. An 11 kW prototype, achieving 4.3 kW/L (6.7 kW/L excluding the heatsink) power density and 95% efficiency, validated these features, showing stable operation and broad compatibility.
- The second contribution focused on GaN-based DC-DC converter optimization, covering non-isolated and isolated topologies. A 9 kW non-isolated GaN prototype reached 99% peak efficiency and outstanding power density (17.7 kW/L—or 50 kW/L without a heatsink—and 6 kW/kg) by integrating air-core inductors, ZVS-enabled variable-frequency control, and optimized TIM. For isolated converters above 1 MHz, experimental evaluation of LLC, CLLC, CI, and asymmetrical CLLC confirmed that conventional CLLC or LLC remain the most practical for OBCs, consistently achieving ZVS at very high frequencies. Air-core transformers outperformed ferrite designs, delivering higher efficiency and power density in the multi-kilowatt range. These findings emphasize the importance of air-core magnetics, ZVS turn-on over ZCS switching, and proper TIM selection as enablers of high-efficiency GaN systems.
- The third contribution developed an FCB-MPC control strategy for GaN-based OBCs, applicable to both the two-inductor unfolding rectifier and the UOBC. The thesis showed its flexibility in distributing MHz switching cycles across multiple energy paths, ensuring sinusoidal grid currents, unity PF, and ZVS for all GaN switches. This demonstrates that the control technique can be effectively applied to both proposed OBC designs.

In conclusion, the thesis shows that combining simplified magnetics, GaN-based high-frequency converters, and advanced predictive control strategies enables a new class of OBCs that are compact, efficient, bidirectional, and universally compatible. These innovations address the challenges of EV charging while paving the way toward sustainable, high-performance, and globally deployable solutions.

Looking ahead, although the current UOBC integrates control, measurement, and rectifier PFC circuits on a single PCB, future work will focus on further readiness level increasing by adding the DC-DC stage and unifying all subsystems—including PFC, DC-DC, control, and measurement—onto one board.

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On a more personal note, I dedicate this thesis to the memory of my beloved parents, Fariba and Siroos, whom I tragically lost to COVID-19. They were my greatest supporters, my strength, and my inspiration. Whatever I have achieved in life is built upon the foundation of their love, sacrifices, and unwavering faith in me. You will always remain my real Superman and Wonder Woman. I love you deeply, and you will forever live in my heart.

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To all of you—my supervisors, mentors, funding organizations, colleagues, friends, and family—thank you. This work is as much yours as it is mine.

Abstract

Concept of Isolated Universal Bidirectional Converters for Electric Vehicle Applications with Improved Power Density

This thesis presents a comprehensive investigation into next-generation onboard battery chargers for electric vehicles, with a focus on universality, high efficiency, and enhanced power density. The research brings together three key areas: advanced onboard battery charging architectures capable of seamless operation across AC and DC grids, GaN-based converter optimization for ultra-high-frequency operation, and predictive control strategies tailored for MHz-range isolated converters. By addressing both technical challenges and system-level integration, the work lays the foundation for a new class of compact, efficient, and globally adaptable electric vehicle charging systems.

The first contribution introduces two onboard charger architectures. A three-phase unfolding-based power factor corrector is proposed, which achieves grid compliance using only two inductors instead of three, thereby reducing cost, magnetic count, and sensor requirements. Its effectiveness was verified with theoretical analysis and a 3.6 kW prototype. In parallel, a universal bidirectional OBC was developed that operates with single/three-phase AC inputs as well as two/three-wire DC grids without hardware changes. Leveraging SiC and GaN devices switching at 100 kHz in the rectifier and 1 MHz in the isolated DC-DC stage, this prototype achieved 95% efficiency and 4.3 kW/L (6.7 kW/L without heatsink) power density at 11 kW, while demonstrating bidirectional Grid-to-Vehicle and Vehicle-to-Grid operation.

The second contribution advances GaN-based converter design, addressing both non-isolated and isolated topologies. A 9 kW non-isolated prototype reached 99% efficiency and record power densities of 17.7 kW/L (50 kW/L without heatsink) and 6 kW/kg by combining interleaved operation, ZVS control, air-core inductors, and optimized thermal management. For isolated MHz-range converters, experimental evaluation of LLC, CLLC, capacitive-isolation, and asymmetrical CLLC topologies confirmed that conventional LLC/CLLC remain the most practical choices for onboard chargers, consistently achieving ZVS. Comparative transformer studies demonstrated that air-core designs outperform ferrite cores at multi-kilowatt, high-frequency operation, eliminating core loss while maintaining compact size.

The third contribution is the development of a finite-cycle-based model predictive control strategy that enables MHz-range switching with lower-frequency control effort. This method allocates discrete switching cycles among energy paths, ensuring sinusoidal grid currents, unity power factor, and ZVS for all GaN transistors. Its applicability was validated by simulation results. It will be practically tested connecting to the AC on both the two-inductor unfolding rectifier and the universal onboard charging prototype as the future work, proving the control scheme's flexibility and robustness.

Overall, the thesis demonstrates that the combination of simplified magnetic structures, GaN-based ultra-high-frequency converters, and advanced predictive control strategies enables onboard chargers that are compact, efficient, bidirectional, and compatible with both AC- and DC-dominated grids. These contributions not only address today's electric vehicle charging challenges but also provide a scalable pathway toward sustainable, high-performance, and universally deployable charging solutions.

Lühikokkuvõte

Parendatud võimsustihedusega isoleeritud universaalsete kahesuunaliste muundurite kontseptsioon elektriautode rakendustele

Käesolev doktoritöö käsitleb uue põlvkonna elektrisõidukite pardalaadijad (PRL), keskendudes universaalsusele, suurele kasutegurile ja parendatud võimsustihedusele. Uurimistöö seob kolm põhivaldkonda: topoloogiade arendus, uue põlvkonna transistoride rakendamine ja prognoosivad juhtimisalgoritmid. Uued täiustatud topoloogiad võimaldavad laadijal töötada korraga nii vahelduv- kui alalisvooluvõrkudes. GaN transistoridel põhinevad muundurid on optimeeritud ultra-kõrgsageduslikuks tööks ning prognoosiv juhtimisstrateegia sobib hästi MHz-tasemel isoleeritud muunduritele. Nende tehniliste ja süsteemsete väljakutsete lahendamine loob aluse uuele PRL klassile, mis on kompaktsed, tõhusad ja globaalselt kohandatavad elektrisõidukitele.

Esmalt pakuti välja kaks PRL arhitektuuri. Kolmefaasiline pingeformeerimispõhine võimsusteguri korrigeerija vastab võrgu nõuetele ja kasutab vaid kahte induktiivpooli (kolme asemel), vähendades seeläbi kulusid, magnetkomponentide hulka ja andurite vajadust. Lahenduse toimivus tõestati nii teoreetilise analüüsi kui ka 3,6 kW prototüübi abil. Paralleelselt töötati välja universaalne kahesuunaline PRL, mis suudab töötada nii ühe- kui kolmefaasilise vahelduvvooluga kui ka kahe- või kolmejuhtmeliste alalisvooluga. Kasutades SiC ja GaN pooljuhte, tõsteti sagedust alaldis (100 kHz) ja isoleeritud alalispingemuunduris (1 MHz), mis läbi saavutati 11 kW prototüübil 95% kasutegur ja võimsustihedus 4,3 kW/L ning tõestati kahesuunaline töö (G2V ja V2G).

Teiseks arendati edasi nii isoleeritud kui ka mitteisoleeritud GaN põhiseid muundureid. Kombineerides omavahel kaskaadjuhtimise, pehmelülitusega modulatsiooni, õhusüdamikuga drosselid ja optimeeritud soojusjuhtimise, saavutati 9 kW mitteisoleeritud muunduri prototüübiga kasutegur 99% ja rekordiline võimsustihedus 17,7 kW/L (6 kW/kg). Katsed MHz-tasemel isoleeritud muundurtopoloogiatega nagu LLC-, CLLC-, mahtuvuslikisolatsioon ja asümmeetrilise CLLC kinnitasid, et traditsioonilised LLC/CLLC topoloogiad on PRL-de jaoks kõige praktilisemaks lahenduseks, võimaldades pidevat talitlust pehmelülitusega. Rakendades õhksüdamikuga trafosid kõrgsagedusmuundurites võimaldas tõsta võimsust mitmeid kilovatte vähendades sealjuures kadusid ja säilitades kompaktsuse.

Kolmandaks töötati välja tsükliline mudelipõhine prognoosiv juhtimine (FCB-MPC), mis võimaldab MHz-tasemel lülitamist madalama juhtimissageduse juures. Meetod jaotab juhtimistsükleid süsteemi olekute vahel nii, et tagada siinuseline võrguvool, ühe lähedane võimsustegur ning pehmelülitus kõigil GaN transistoridel. Selle rakendatavust testiti kahe induktiivpooliga formeerimisahelaga alaldis ja universaalses PRL prototüübis. Tulemused kinnitasid juhtimisstrateegia paindlikkust ja töökindlust.

Kokkuvõttes näitab töö, et kombinatsioon lihtsustatud magnetlahendustest, GaN-põhistest ultra-kõrgsageduslikest muunduritest ja täiustatud prognoosivatest juhtimisstrateegiatest võimaldab välja töötada PRL-d, mis on kompaktsed, tõhusad, kahesuunalised ja sobivad nii vahelduv- kui alalisvooluvõrkudega. Need uuendused lahendavad elektrisõidukite laadimisega seotud tänased kitsaskohad ning loovad skalleeritava tee jätkusuutlike, suure jõudlusega ja globaalselt rakendatavate laadimislahendusteni.

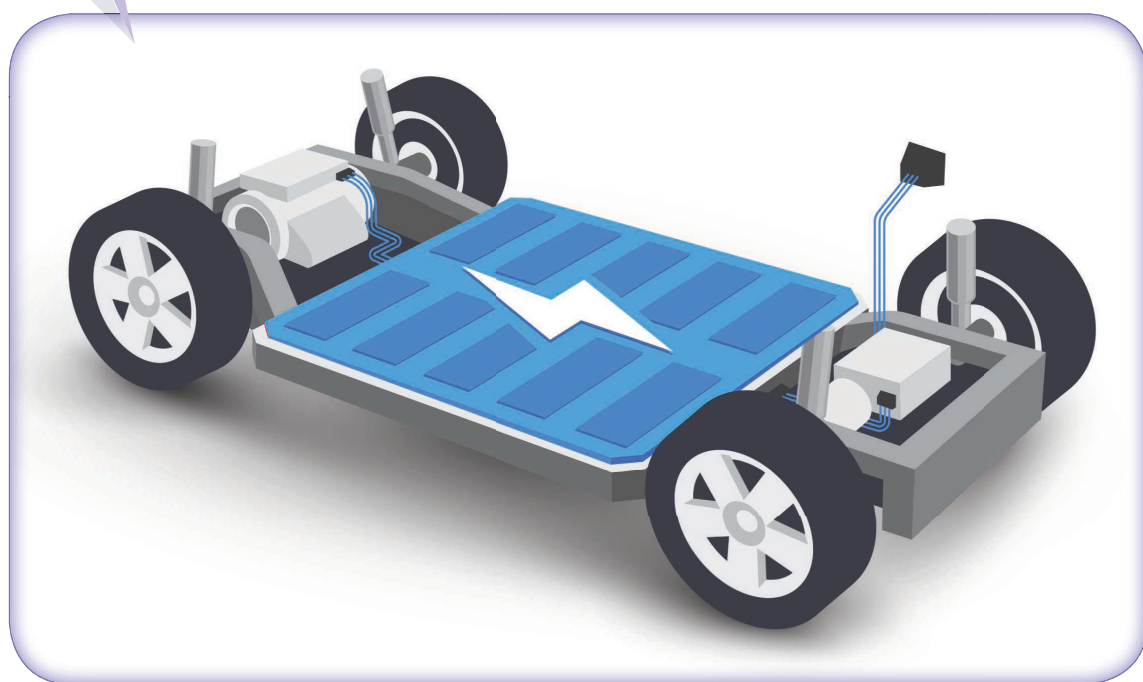
Appendix

Paper I

P. Mohseni, O. Husev, D. Vinnikov, R. Strzelecki, E. Romero-Cadaval and I. Tokarski, "Battery Technologies in Electric Vehicles: Improvements in Electric Battery Packs," in *IEEE Industrial Electronics Magazine*, vol. 17, no. 4, pp. 55–65, Dec. 2023, doi: 10.1109/MIE.2023.3252265.

Battery Technologies in Electric Vehicles

Improvements in Electric Battery Packs



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Restrictions on fossil fuels and related environmental pollution issues motivate many organizations and countries to set their focus on electric vehicles (EVs) rather than conventional internal combustion engine vehicles [1], [2]. EVs require an energy storage system to store converted electric power in another form of energy and then reconvert the stored energy to electric

power whenever it is required. The energy stored can be converted to electric energy for various uses, such as movement, lighting, and heating (although accessories are supplied by a 12-V auxiliary battery; the auxiliary battery is supplied by the main battery pack or by recuperative energy). Fortunately, many electrical energy storage technologies are available, with some offered commercially while others are in the research and development stage

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Ongoing research of battery technologies for EVs focuses on some promising next-generation battery technologies for EV applications.

[3], [4]. Electrochemical energy storage systems use various technologies [5], [6]. Energy storage systems, the heart of EVs, are composed of battery cells, battery modules, and a battery pack. Researchers work on various sections of battery packs to improve their performance [7]. These sections are illustrated in Figure 1. As shown in the figure, some EV battery technology developers are studying chemical materials to increase the capacity, power, energy density, safety, and cell voltage. In the past century, the most common batteries for EV applications were Pb–acid and Ni-based batteries [8]. In current use, Li-ion-based batteries are at the top.

Ongoing research of battery technologies for EVs focuses on some promising next-generation battery technologies for EV applications, such as solid electrolyte or aqueous, Li-oxygen (O₂), and Li-S, along with solid-state batteries [9], [10]. Also, research efforts concentrate on the cell components to decrease the internal resistance of cells, provide thermal management conditions, improve performance, reduce the production cost, facilitate fabrication, and support the stable operation of batteries [11], [12]. Eventually, the required high energy and voltage for EVs are obtained by connecting the selected cells in series

and parallel [13]. Consequently, novel cell materials, cell components, and techniques of connecting cells can improve the voltage, capacity, weight, size, cost, thermal management, and safety of onboard battery packs, which are all required to upgrade the performance of EVs [14]. As a result, there are many fields involved in the movement toward improved EV battery pack technologies. Also, many different parameters should be considered during the design of battery packs. In this design, it is necessary to determine strategies for combining these parameters. In addition to choosing the proper cell chemistry and type in the battery pack design, some other parameters, shown in Figure 2, should be considered [7].

This article addresses the various technologies utilized by well-known EV manufacturers. We discuss the different approaches of various EV manufacturers to improve the performance

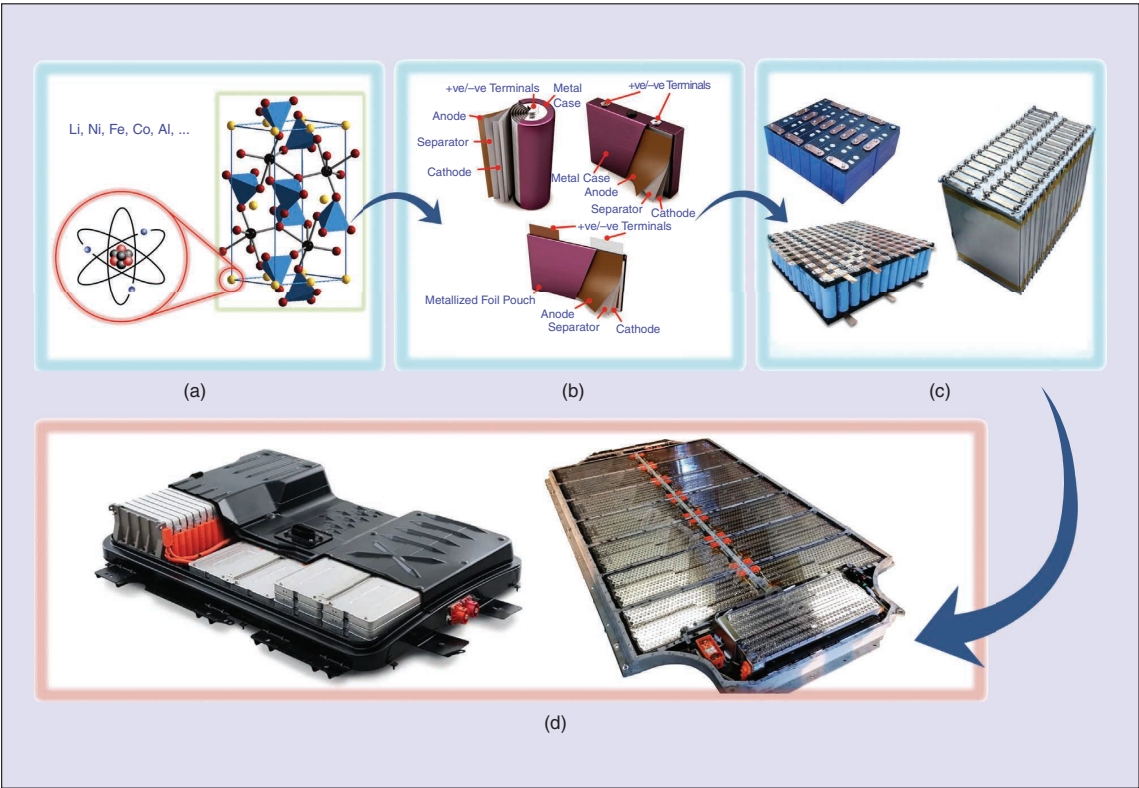


FIGURE 1 – The production structure of an onboard battery pack for EVs. The (a) chemical materials, (b) cell components, (c) series- and parallel-connected cells, and (d) battery pack. +ve: positive; –ve: negative.

of their battery packs. The advantages and disadvantages of the approaches are pointed out to enable better analysis of the performance of the EV battery technologies.

Basic Types of Battery Storage Technologies Used in EVs and Their Comparison

The chemistry of batteries distinguishes them in terms of their specific power rate, specific energy rate, lifecycle, cost, performance, and safety. In the early decades of the 20th century, Pb-acid and Ni-based batteries were utilized to power most automobiles. The oldest rechargeable battery technology is Pb-acid-based batteries. Ni-based batteries can provide better electrochemical characteristics, and they are lighter than lead-acid or Pb-acid batteries; on the other hand, their cost is approximately 10 times higher than that of lead-acid or Pb-acid batteries.

The chemistry of batteries distinguishes them in terms of their specific power rate, specific energy rate, lifecycle, cost, performance, and safety.

In many applications, Li-ion-based batteries are being replaced with lead and Ni-based batteries. Li-ion-based batteries are more expensive, but their low maintenance and high cycle count reduce their per-cycle costs. The main Li-ion-based battery types, based on their chemical composition, are LiCoO₂, LiMn₂ oxide (LMO), LiNiMnCoO₂ (NMC), LiFe phosphate (LFP), LiNiCoAl oxide (NCA), and Li titanate (LTO) [17]. Li-ion battery cells used onboard EV energy storage systems are also categorized into three types, as listed in Table 1: prismatic cell, cylindrical cell, and pouch

cell [18]. The specific energy rate of Li-ion-based batteries, Pb-acid batteries, and Ni-based batteries are compared in Figure 3. It can be concluded that the energy rates of Li-ion-based batteries are higher compared to Pb-acid and Ni-based batteries. The advantages, disadvantages, and applications of the battery storage technologies are presented in Table 2. Li-based battery technologies have been dominating the EV onboard storage systems market, due to the features given in the table. But these batteries have some limitations and challenges, and to solve

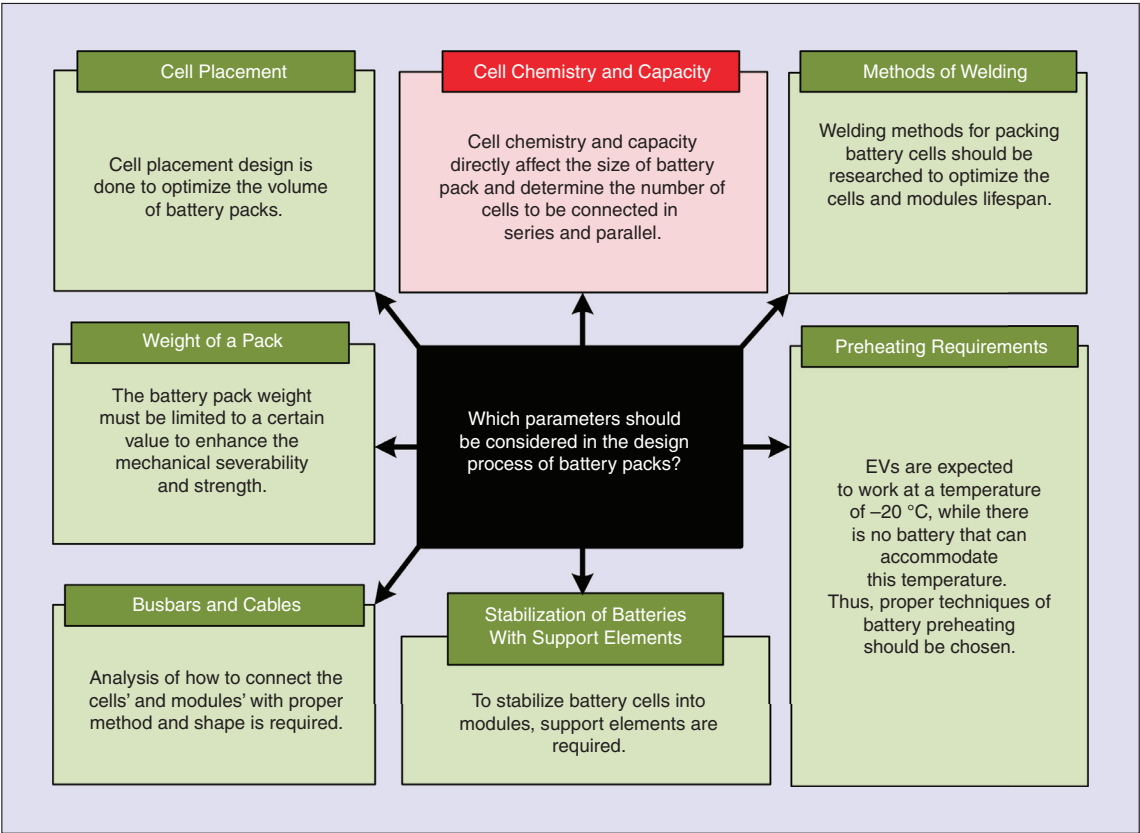


FIGURE 2 – The parameters to be considered in the battery pack design.

TABLE 1 – THE THREE TYPES OF LI-ION-BASED BATTERIES.

CELL TYPE	CYLINDRICAL CELL	PRISMATIC CELL	POUCH CELL
			
Produced by	Li-NMC, Li-NCA, and Li-LMO	Li-LFP	Li-LFP, Li-NMC, and Li-LTO
Features	✓ Proper cost performance and high manufacturability	✓ Better thermal management performance ✓ Easy heat exchange between the inside of the cells and the cooling system ✓ Easier design of cooling system [7], [19]	✓ Accidental swelling and bulging produces major safety concerns ✓ Being gradually marginalized due to safety problems [20]
Attractive among EV manufacturers	Tesla	Toyota, Volkswagen, and BYD	Chevrolet, Nisan, Hyundai, BAIC, Mazda, and General Motors [13]

them requires better technologies. Battery technologies are advancing, and batteries under research have the potential to be the future large-scale commercial batteries for EV applications [13]. Future batteries theoretically work amazingly, but most of them do not meet the basic eight requirements, including high specific energy, high specific power, safety, a reasonable price, toxicity, long life, fast charging, and a wide function range, for an ideal battery. A limited load current and short cycle life often prevent them from being commercialized. Besides the eight

requirements, a battery should have a low self-discharge, long shelf-life, and capability of providing instant start-up whenever required. Meeting all the basic requirements is not easy, but researchers have not given up. Some of the future batteries may find specific markets, but some may not come out of laboratories. Therefore, the advantages, disadvantages, and applications of the most promising experimental batteries are also mentioned in Table 2.

Si anodes are a promising technology for Li-ion batteries, due to their considerably high capacity for storing

Li. But Si anodes tend to shrink and expand during charging and discharging, which makes the system unstable. To reduce the amount of shrinkage and expansion, it is proposed to make batteries from a composite of Si and graphite to maintain their theoretical high capacity. However, the cycle life is still limited due to some problems in the structure [13], [25]. Therefore, more research and development are needed to make Si-based anode batteries commercialize to meet the market demand.

Figure 4 gives a performance summary of the five main battery chemistries through a hexagonal spider graphic of the onboard battery storage system of EVs. Also, Table 3 summarizes the performance of the five battery technologies for EVs. Although the power rate of the Li-LFP chemistry is the highest, there are no significant differences among the five chemistries. In the terms of safety, Li-NCA takes the lowest place. The safety of Li-NMC and Li-LMO is lower than that of Li-LFP and Li-LTO. In terms of performance, since Li-LTO is in the lead, it shows the best performance. In terms of the cycle life count, Li-LTO has the highest cycle life count, but it is the most expensive battery chemistry. Therefore, it cannot be added considerable things about the cycle life count and cost. Although Li-NCA has the highest capacity in EV applications, the cycle count and safety will gain more attraction compared to capacity.

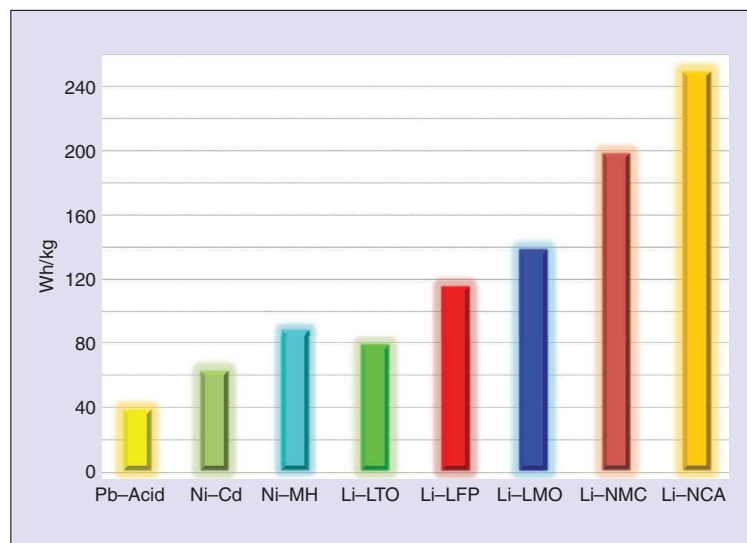


FIGURE 3 – A comparison of Li-ion-based batteries with Pb-acid and Ni-based batteries in terms of specific energy. MH: metal hydride.

Battery Technology Comparison of EV Manufacturers

Table 4 summarizes the characteristics of the utilized battery cell technologies of four well-known EV manufacturers (Tesla, Nissan, Chevrolet, and Kia). The table clearly shows that Tesla has elevated the power

density of its battery cells while providing a 20% higher energy density by increasing the battery size (utilizing 21,700 cells instead of 18,650 cells) in its Model Y and Model 3. As a result, it can be concluded that Tesla attempts to increase the size of the batteries to increase the power, capacity, and

control of heat generation over the previous ones. This results in higher power and capacity per pack, with fewer cells in the same pack size utilized for the previous cell generations.

While cylindrical batteries are attractive for Tesla, other large car companies, such as Chevrolet,

TABLE 2 – THE ADVANTAGES, DISADVANTAGES, AND APPLICATIONS OF THE BATTERY STORAGE TECHNOLOGIES [8], [10], [13], [15], [16].				
CELL CHEMISTRY		ADVANTAGE	DISADVANTAGE	APPLICATION
Pb–acid		Economically acceptable due to low price	- Low cycle count - Limited energy - Pb is toxic	- Lighting and starting in internal combustion engine vehicles - Golf carts - Wheelchairs - UPS
Ni based	Ni–Cd	- Ultrafast charging without considerable stress - High discharge current - Long service life - Work at high temperatures	- Cd is a toxic element - Memory effect; needs periodic full discharges	- UPS - Medical instruments
	Ni–MH	Replacement for Ni–Cd batteries: provide higher energy	- Composed of mildly toxic metals - Slight memory effect	- Hybrid cars - Medical instruments - Industrial applications
Li-ion based	Li–NMC	- Can be designed based on application in terms of needed energy or power per cell - Increasing market due to high energy and power	Expensive	- E-bikes - Medical devices - EVs
	Li–LFP	- High electrochemical performance with low resistance - Safe even when fully charged - Can tolerate high-voltage conditions for a long time with less stress - High thermal stability, cycle count, and current performance	- Low temperature reduces performance - High storage temperature reduces lifecycle - Highest discharge rate among Li-ion batteries (makes balancing problem with aging) - Low cell voltage reduces the battery energy	EVs and so on
	Li–LTO	- Fast charging - High discharge current - Highest cycle count and best thermal stability among Li-ion batteries - Excellent low-temperature performance (80% capacity at –30 °C)	- Low capacity - Expensive - Low charging and discharging voltage range	- UPS - Electric powertrains - Street lighting
	Li–LMO	- Low internal resistance (proper for high-current discharging and fast charging conditions) - Design flexibility for maximum delivered power, high lifecycle, and high capacity	Expensive	- Electric powertrains - Medical devices
	Li–NCA	Highest specific energy, high power, and high lifecycle count	Lowest safety among Li-ion-based batteries	- Electric powertrains - Medical devices
	Future batteries	Li–air	Theoretical specific energy density is up to 2,000–3,000 Wh/kg, which is a high value	- Poor loading - Short life - Need to breathe clean air [21]
	Li–S	- High specific energy density of $\geq 2,500$ Wh/kg - Wide operating temperatures - Good safety - Low production cost	Poor loading and cycle life [22]	
	Li–metal	- Good loading capability - High specific energy - Rapid charging	Lithium deposition is uncontrolled, which makes safety hazards	- Portable and industrial applications - EVs
	Solid-state Li-ion	- Wonderful specific energy density and safety - High potential for large-scale manufacturing and high lifecycle - Possibility of producing in a single large plate piece - Increasing the driving mileage significantly - Solving safety problems by reducing heat generation [23]		- Talked about for EVs - Wheeled mobility - Electrical energy storage - Under investigation by BMW, Hyundai, and Volkswagen
UPS: uninterruptable power supply; MH: metal hydride.				

The charging power can be increased significantly by increasing the voltage without changing the conductor size and increasing the generation of heat.

Nissan, and Kia, have chosen a different laminated battery type. At present, the provided battery technology by Tesla has reached a high rate of production automation, lighter weight, and higher security and compliance, which is proper for mass production of batteries. Using this battery cell type by Tesla is the best choice. But many smaller batteries provided by Tesla must be wired in parallel and in series to provide the required power, energy, and voltage. This high number of battery cells in the pack requires a complicated battery management system (BMS), which has been acquired only by Tesla. The sheet shape of the laminated batteries makes them more suitable to conduct heat to the cooling system outside the batteries. Thus, they do not need a complicated cooling system and a complex BMS. But generally, the thin aluminum plastic film packing of the laminated batteries makes them more vulnerable to mechanical damage. Therefore, the batteries are prone to major damage

in the case of critical circumstances and car accidents, which is the main defect of the cars.

Voltage and Power Level of Battery Packs of EV Manufacturers

The specifications of some onboard battery pack technologies used by some reputable EV manufacturers are provided in Table 5. This table shows that battery technology has been improving and helped with the advent of large battery packs with 50–150 kW. Although Tesla achieved ultrafast charging powers of 200–250 kW in models Y and S, with a 400-V pack voltage, the other EV manufacturers have been able to improve their power only by increasing the battery pack voltages to 600–800 V. The charging cables and busbars of the battery packs are large enough, and it is not possible to enlarge them. The charging power can be increased significantly by increasing the voltage without changing the conductor size and increasing the generation of heat [2], [26].

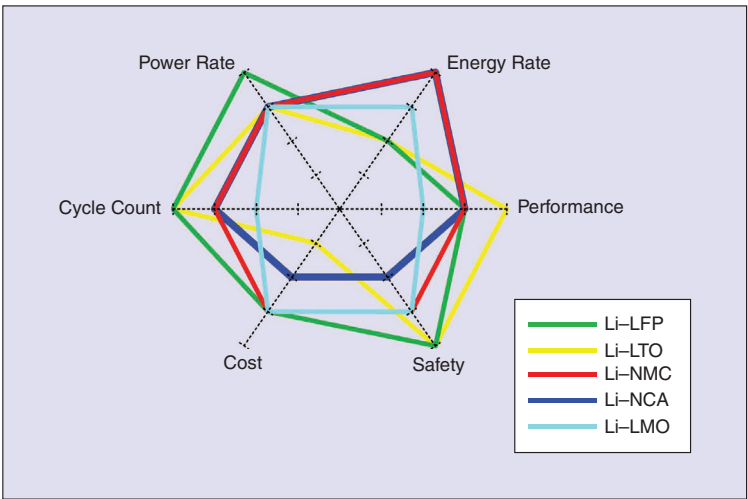


FIGURE 4 – A performance comparison of the five main Li-ion-based battery chemistries utilized in EVs.

An example of an improved battery charging profile by increasing the battery pack voltage is given in Figure 5. In the first configuration, the 400-V battery pack system is obtained from 100 series- and four parallel-connected battery cells. The 100 series-connected battery cells make the battery pack voltage around 400 V. Although the maximum conduction current of each cell is around 150 A, the charging current of the four parallel-connected battery cells is limited by the maximum current of the combined charging system (CCS) connector: 350 A. The increased-voltage battery pack 800-V system is composed of 200 series- and two parallel-connected battery cells. The charging current of this system is limited by the total maximum charging current of two cells, $2I_{\text{Cell,max}} = 300$ A, which is lower than the maximum current of the CCS, at 350 A. As a result, the maximum charging power of the standard battery pack system is increased by 71.43% by increasing its voltage to 800 V, without increasing the number of battery cells and the battery pack capacity. But on the other hand, it should be considered that the charging current of the batteries in the 800-V system is 150 A versus 87.5 A in the 400-V system. This maximum charging current increases the heat generation and thermal loss in the batteries, which can also reduce the lifetime of the batteries. Therefore, this thermal loss in the batteries should be managed by a well-designed thermal cooling system of the vehicle or a thermal capacity. However, increasing the voltage rate of the battery pack increases the number of battery channels in the BMS. For instance, in Figure 5, in the 800-V system, 200 voltage levels should be controlled and monitored, versus 100 voltage levels in the 400-V system. As can be seen in Table 5, some of the EV manufacturers, including Porsche, Hyundai, Kia, and Mercedes-Benz, increased their battery pack voltages to provide ultrafast battery charging stations. Increasing the voltage can provide many benefits, such as a significant reduction in the cross-sectional area and weight of busbars

and cables to handle the same amount of power [27], [28]. For example, a cable to handle the 350-kW fast-charging power with a 350-V battery pack voltage should conduct a 1,000-A current with a reasonable temperature rise. A proper cable for this current should have a 300-mm² cross-sectional area, which will weigh 3.22 kg/m. Therefore, 5 m of the cable would have a 16.1-kg weight. While this high conducting current can be reduced, with an 800-V battery pack voltage, to 438 A, this requires a 125-mm² cross-sectional area, which weighs 1.4 kg/m, and its 5-m cable would have a 7-kg weight. Increasing the voltage to increase the power requires more thickness for the insulators of cables and busbars, but the relative impact is not considerable because the needed extra insulation is just a few millimeters in thickness, and its materials have about a 12.5% density compared to copper. Moreover, increasing the fast-charging power by increasing the voltage rather than the current would allow the same cooling system to be used without significant changes and save a significant portion of the conducting losses.

It should be considered that the battery pack voltage cannot be increased arbitrarily. By increasing the voltage from 300–400 V to 600–800 V, designers should modify all the devices utilized in the EV system: the conductors need more insulation, motors need more turn, dc–dc converters and the inverter need to be redesigned or use semiconductors with 1.2–1.7-kV blocking voltage rates, and so on. This will impact all components in different ways. For example, the volume of the onboard charger (Figure 6) or inverter will increase by 10% by increasing the voltage range. This 10% is a significant increment in the power electronics range, but it should be considered that the volume of the battery pack is 20–40 times more than the power electronics size, and this volume increment can be compensated easily by the saving in the battery pack voltage increase. In addition, the voltage level elevation can affect the structure of fuses and requires putting some insulators between fuses and

TABLE 3 – A PERFORMANCE COMPARISON OF THE FIVE WELL-KNOWN BATTERY CHEMISTRIES FOR THE ONBOARD STORAGE SYSTEM OF EVs.

	BATTERY MANUFACTURERS [7], [13]	NOMINAL VOLTAGE (PER CELL)	TYPICAL OPERATING VOLTAGE RANGE (PER CELL)	SPECIFIC ENERGY (Wh/kg)	CHARGE (C RATE)	DISCHARGE (C RATE)	CYCLE LIFE COUNT	COST (\$/kWh) [24], [25]	THERMAL RUNAWAY	OPERATING TEMPERATURE (°C)
Li-LFP	BYD, Valence, Lishen, and GS Yuasa	3.2 and 3.3 V	2.5–3.65 V	90–120	1C	1C; 25C in some cells	2,000 and higher	~580	270 °C; very safe even when fully charged	0–40
Li-LTO	IEC, EnerDel, CATL, Valence, Hitachi, Toshiba, and SAFT	2.4 V	1.8–2.85 V	50–80	1C; 2.8C maximum	10C; 30C for 5-s pulses	3,000–7,000	~1,005	One of the safest	–30–45
Li-LMO	Panasonic, Sony, Sanyo, LG Chem, Samsung SDI, CATL, BYD, and Lishen	3.7 and 3.8 V	3–4.2 V	100–150	0.7–1C; 3C maximum	1C; 10C possible for some cells; 30C for 5-s pulses	300–700	~360	250 °C; high charge increases it	–
Li-NMC	CATL, SK Innovation, Panasonic, Samsung SDI, LG Chem, and Hitachi	3.6 and 3.7 V	3–4.2 V or higher	150–220	0.7–1C (<1C shortens battery life)	1C; 2C possible for some cells	1,000–2,000	~420	210 °C; high charge increases it	0–40
Li-NCA	Panasonic, Tesla, CATL, and LG Chem	3.6 V	3–4.2 V	200–260	0.7C; fast charging possible	1C; high discharge reduces battery life	500	~350	150 °C; high charge increases it	–

TABLE 4 – THE SPECIFICATIONS OF THE BATTERY CELL TECHNOLOGIES UTILIZED IN SOME RECENT WELL-KNOWN EVs.

	TESLA		2018 NISSAN LEAF ZE1	CHEVROLET BOLT	KIA e-NIRO
	MODELS S AND X	MODELS Y AND 3			
Cell type	Panasonic cylindrical 18650	Tesla and Panasonic or LG Chem Cylindrical 21700	AESC Pouch Sheet shaped 261 × 216 mm	LG Chem Ni-rich sheet shaped 300 × 110 mm	SK Innovations Sheet shaped 300.5 × 108.5 mm
Nominal voltage	3.8 V	3.6 and 3.7 V	3.65 V	3.75 V	3.75 V
Capacity	3.4 Ah	5 and 4 Ah	56.3 Ah	60 Ah	60 Ah
Voltage range	2.5–4.2 V	2.5–4.2 V	2.5–4.2 V	2.75–4.2 V	2.5–4.2 V
Discharging current	Continuous 5.5 A	Continuous 15 and 12 A	–	Continuous 120 A	Continuous 120 A
Weight (maximum)	48 g	69 g	914 g	850 g	899.3 g
Temperature range	–20~+60 °C	–20~+60 °C	–35~+45 °C	–10~+60 °C	–20~+60 °C
Dimensions	18.25 × 65.1 mm	21 × 70 mm	261 × 216 × 7.9 mm	300 × 110 × 15 mm	300.5 × 108.5 × 15 mm
Energy density (volumetric)	675 Wh/L	689 and 707 Wh/L	460 Wh/L	614 Wh/L	607 Wh/L
Energy density (gravimetric)	250 Wh/kg	300 Wh/kg	224 Wh/kg	243 Wh/kg	257 Wh/kg
Cost	US\$185/kWh	US\$170/kWh	US\$236/kWh	–	–
Number of cells	S: 7,104 X: 8,256	4,416	192	288	294

TABLE 5 – A COMPARISON OF THE VOLTAGE AND POWER LEVEL OF THE ONBOARD BATTERY PACKS OF SOME WELL-KNOWN EV MANUFACTURERS.

	VOLTAGE	MAXIMUM ONBOARD CHARGER POWER	MAXIMUM FAST CHARGER POWER	Capacity						Fastcharge Time		
				kWh min	20 15	40 30	60 45	80 60	100 85			
Hyundai Kona SE	319 V	7.2 kW	100 kW									
Kia Soul EV	327 V	7.2 kW	100 kW									
Chevrolet Bolt EV	350 V	7.2 kW	55 kW									
Hyundai Kona SEL	356 V	7.2 kW	100 kW									
Kia e-NIRO 4	356 V	7.2 kW	100 kW									
Nissan Leaf SL	360 V	6.6 kW	50 kW									
Tesla Model X	350 V	17.3 kW, 72 A	145 kW									
Tesla Model 3	360 V	11.5 kW, 40 A	120 kW									
Tesla Model Y	340 V	11 kW	250 kW									
Tesla Model S	400 V	11.5 kW, 48 A	200 kW									
Volkswagen ID.3 Pro S	408 V	11 A	125 kW									
Mercedes-Benz EQB	420 V	11 kW	100 kW									
Mercedes-Benz EQS	500 V	7.4 kW	170 kW									
Mercedes-Benz AMG EQS	500 V	7.4 kW	200 kW									
Kia EV6	697 V	11 kW	233 kW									
Hyundai Ioniq 5 Standard	800 V	11 kW	225 kW									
Hyundai Ioniq 5 Long Range	800 V	11 kW	225 kW									
Porsche Taycan 4S	800 V	11 kW	400 V:50 kW; 800 V:225 kW									
Porsche Taycan 4S+	800 V	11 kW	400 V:50 kW; 800 V:270 kW									

increasing the separation distance between them, which increases the cost of the fuses. The major challenges of increasing the battery pack voltage to 800 V and the recommended solutions are presented in Table 6.

Conclusion

This article compared various types of previous, contemporary, and future battery technologies for EVs and presented their advantages and disadvantages. A battery pack designer should consider all aspects of the design. Currently, Li-ion-based batteries are the best selection for EV battery packs. But battery pack technology is improving, and next-generation

The reasonable progress achieved in EV technology is an evolutionary rather than a revolutionary step forward.

battery technologies will be commercially available. Although some EV manufacturers have invested much in battery cell technologies, others do not rely on any revolutionary battery technology. They are trying only to rearrange the series and parallel connections of battery cells to increase the total voltage of their battery packs. The only reason is that they cannot increase the diameter of

the conductor, which gets hot during fast charging. Considering all the discussed advantages and disadvantages of increasing the battery pack voltage from 350 to 800 V for reducing the charging time and managing the generated heat during battery charging, we can conclude that the reasonable progress achieved in EV technology is an evolutionary rather than a revolutionary step forward.

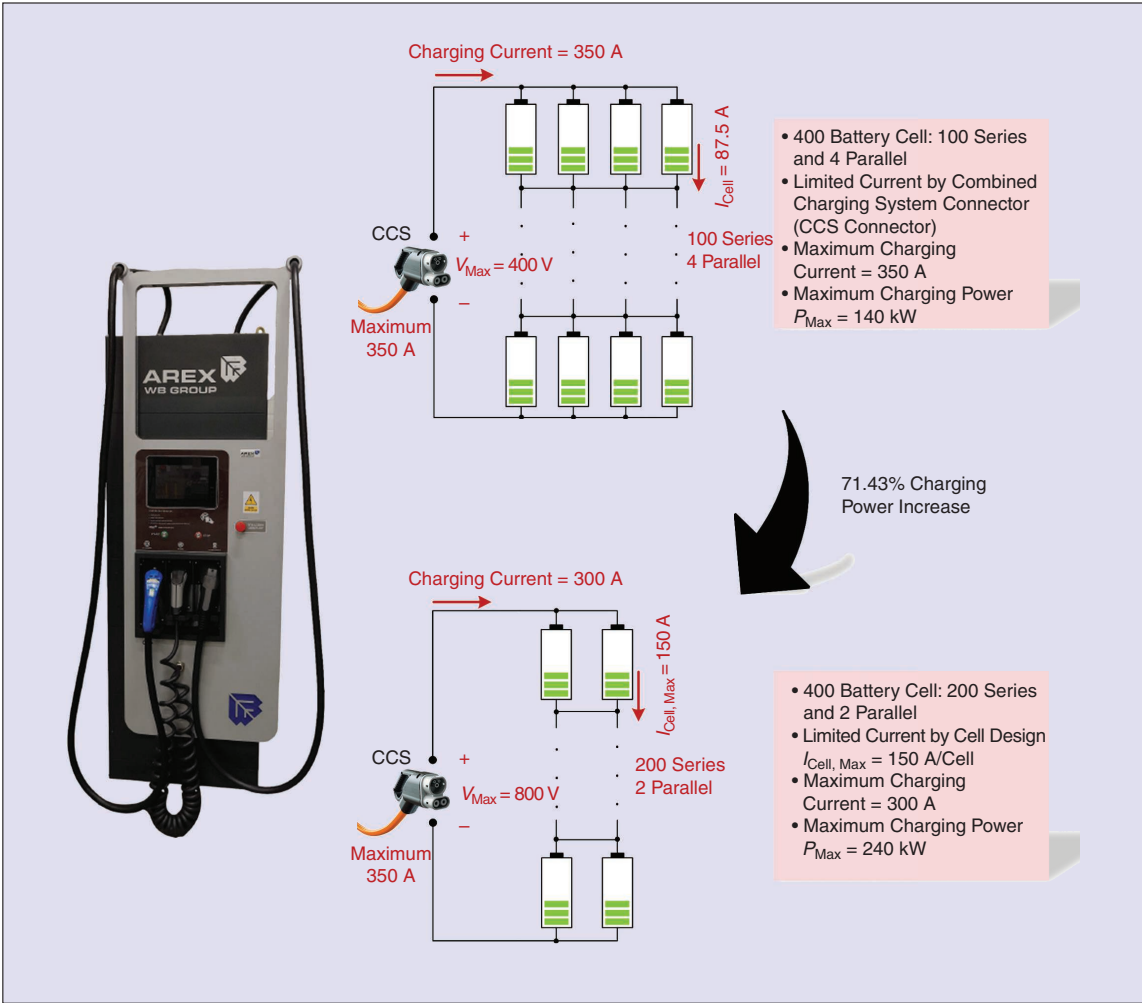


FIGURE 5 – The improved battery charging profile by increasing the battery pack voltage from 400 to 800 V. CCS: combined charging system.

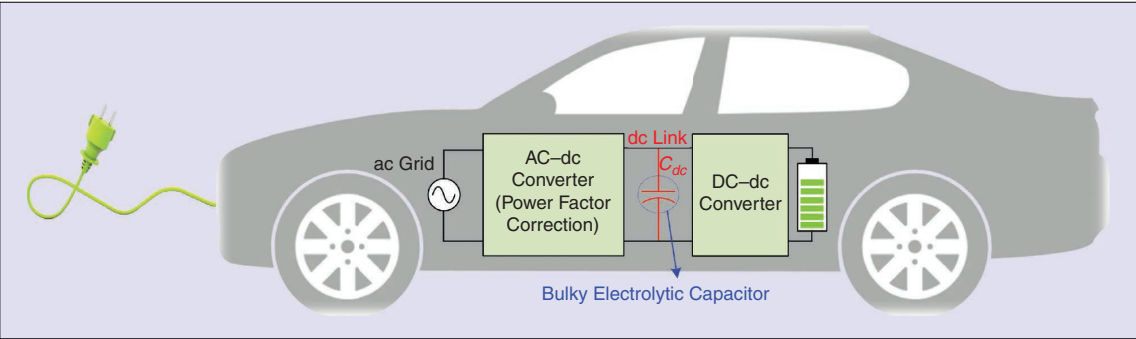


FIGURE 6 – The onboard EV charger.

TABLE 6 – THE MAJOR CHALLENGES OF INCREASING THE BATTERY PACK VOLTAGE OF EVs.		
POINT	CHALLENGE	SOLUTION
High voltages are more likely to make an arc and electrocution menace.	Increasing the battery pack voltage decreases the safety of passengers, especially in car accidents.	Increase the thickness of the insulators and the separation distance between conductors.
The total capacity of the series-connected batteries depends on the capacity of the weakest battery.	Increasing the number of series-connected batteries increases the impact of the weakest battery.	✓ Parallel connecting low-capacity batteries and then connecting in series can help to reduce the impact, but it still cannot solve the issue. ✓ Use a proper BMS, which monitors and manages the individual cells and regulates the charge and discharge of each cell to keep all cells at an equal state of charge and avoid overworking weaker cells. ✓ Perform a diagnostic battery cell test before inserting a cell in the battery pack. ✓ Additionally, it is important to have a regular checkup of the battery pack and replace weaker battery cells with new ones to maintain the high performance of the battery pack.
A little increase in the battery pack voltage requires modifying the circuit, parameters, and utilized components in the power electronics elements of the inverter, onboard charger, and dc-dc converter of the EV.	DC voltage link capacitors (shown in Figure 6) should tolerate the high voltage, while 450 V is the highest rate for commonly used capacitors.	✓ Connect some specific capacitors in series, but this would provide some leakage current issues. ✓ Use film and ceramic capacitors, but utilizing them to provide the high capacitance for the dc link will increase the cost of the power electronics circuits.
The switching frequency can be increased significantly to decrease the size of the magnetic components.	• The higher voltage could lead to higher dv/dt and higher electromagnetic interference problems compared to lower voltages. • The high switching capability of the utilized semiconductors should be considered.	✓ The electromagnetic interference issues can be solved with a proper shield and by providing fully resonant and soft-switching operations in power electronics converters [29], [30], [31]. ✓ The high-voltage-range Si carbide semiconductors, which have high-frequency switching capability, can be a proper choice. ✓ Using gallium nitride semiconductors for their uncommon availability for higher-than-650-V blocking voltage ranges would be challenging and require redesigning the power electronics converters.

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Paper II

P. Mohseni, O. Husev, M. Kasper and G. Deboy, "Design Optimization for Enhancing the Power Density and Efficiency for GaN-Based DC–DC Converter," in *IEEE Transactions on Industrial Electronics*, doi: 10.1109/TIE.2025.3552273.

Design Optimization for Enhancing the Power Density and Efficiency for GaN-Based DC–DC Converter

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Abstract—This article presents an optimization strategy for enhancing the efficiency and power density of a GaN-based dc–dc converter, tailored for different applications with a wide input voltage range regulation. The optimization employs air-core inductors and implements a variable switching frequency modulation method to enable zero voltage switching turn-on for GaN transistors, facilitating greater flexibility in frequency adjustment and improved thermal management. Additionally, a specialized thermal model is introduced for the interleaved Buck-Boost GaN transistor-based dc–dc converter, accounting for the presence of a natural convection heatsink. In the conclusion, theoretical discussions transition to practical implementation through the testing of a laboratory prototype. This prototype achieves high efficiency (around 99%), along with power densities of >17.5 kW/L and 6 kW/kg when equipped with a natural convection (without air-flow) heatsink. It features a wide input voltage range (110–450 V), a constant output voltage of 350 V, variable switching frequency (18–304 kHz) and supports up to 9 kW output power.

Index Terms—GaN-based dc–dc converter, high efficiency, high power density, zero-voltage turn-on.

I. INTRODUCTION

THE growing demand for electricity is driving a transition from traditional power grids to dc microgrids (DCMG), which provide better power management and simpler control, thus enhancing reliability. This shift is particularly accelerated by the increasing use of renewable energy sources, contributing to a sustainable energy future [1], [2]. Power electronics are vital

for integrating renewable sources like solar panels and battery storage into microgrids. Key advancements in power converter technology focus on efficiency and compactness, which can reduce installation and labor costs for PV inverters, making photovoltaic (PV) energy more affordable [3]. The Department of Energy emphasizes maximizing efficiency in PV microconverters to minimize energy losses and effectively manage heat [4].

Another obvious field where buck-boost dc–dc solution with superior power density can be required is an electric vertical take-off and landing (eVTOL) aircraft [5].

Wide band-gap (WBG) devices, such as gallium nitride (GaN) and silicon carbide (SiC), are increasingly utilized for higher power density in applications like dc–dc converters. GaN devices, in particular, provide significant advantages, including higher switching frequencies compared to traditional silicon MOSFETs, which leads to faster switching, enhanced efficiency, and smaller passive components that increase power density and reduce costs. Additionally, GaN transistors do not have a body diode with substantial reverse recovery charge, minimizing switching losses during hard-switching. Their low gate charge further decreases gate-drive losses, making them highly efficient for high-frequency applications [6].

GaN-based dc–dc converters for high-power applications require careful design considerations, focusing on enhanced power density, efficiency, low parasitic inductance, and effective thermal management, especially in dc microgrids and renewable energy systems. GaN semiconductors are pivotal in technological advancements due to their high breakdown voltages, low conduction resistances, and compact sizes. Their ability to minimize switching losses is crucial for improving power density [7], [8], as seen in automotive converter systems [9], [10], [11]. Additionally, GaN technology has significantly enhanced efficiency and power density in induction power transfer [12], railway, and photovoltaic applications [13].

In high-frequency operation of dc–dc converters, while size reduction is achieved, switching losses tend to increase, adversely affecting efficiency and generating excess heat in GaN-based converters. To optimize efficiency while controlling costs and size, it is essential to reduce these switching losses. Soft-switching techniques have proven effective in minimizing switching losses, allowing for higher frequencies and reduced passive filter volume, thereby improving efficiency and power density [14], [15]. Huang et al. [16], [17], [18] have investigated switching loss mechanisms in high-voltage Cascode GaN

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transistors, identifying that turn-on losses are significant due to charge stored in the junction capacitor of the freewheeling diode during hard switching, while turn-off losses are minimal due to the Cascode configuration's intrinsic current source behavior. Their research emphasizes the importance of zero-voltage switching (ZVS) for GaN devices at high frequencies, with less concern regarding turn-off current in Cascode GaN transistors. Additionally, Huang et al. [17], [18] compare the efficiency and loss distribution between Cascode GaN switches and Silicon MOSFETs under both hard and soft-switching conditions, demonstrating the performance advantages of GaN devices. Thus, achieving zero-voltage turn-on is particularly advantageous for GaN transistors, given their low turn-off losses and high turn-on losses, indicating significant optimization potential.

In high-power applications, effectively dissipating heat from GaN-based semiconductor devices is challenging due to the limited space of the thermal pad. This increases the risk of surpassing the maximum junction temperature [19], [20]. However, achieving peak performance and power density requires careful consideration of thermal design to address these concerns [21]. Proper heat management is crucial for the reliable operation of GaN-based PV string dc-dc converters, especially in microgrid setups with high power densities [22]. Efficient cooling systems, including optimized heatsinks and thermal interface materials (TIMs), are necessary to dissipate heat effectively and maintain optimal temperatures. Selecting the right TIMs, whether adhesive or non-adhesive, is essential for balancing thermal performance and ease of assembly [23].

The high switching speed of GaN transistors can be compromised by parasitic inductances and capacitances from PCB tracks, which increase switching losses and generate voltage overshoots and ringing on the transistor's drain-source voltage waveforms. To mitigate these effects, a low-inductance layout for both power and gate circuits is crucial, and transistors with Kelvin-source connections should be used when possible. Internal capacitances combined with PCB-induced parasitic contribute to switching losses, but careful placement of tracks and ground planes can reduce their impact [24].

The focus should be on the essential regulation across a broad input voltage range, necessitating an alternative approach, particularly in PV applications. Research indicates that a conventional noninverting buck-boost converter is highly suitable for these scenarios [25], [26]. The article delves into the utilization of PV string converters as a case study example for DCMG applications. It outlines an approach centered around interleaved buck-boost nonisolated dc-dc converters, which form the fundamental components of a previously introduced universal solar dc-dc/ac converter by a research team [27]. A thorough comparison of the modular buck-boost converter against other options highlights its superior efficiency and power density for both dc and ac grid applications. The article confirms that the modular buck-boost converter excels in dc-dc operation, making it an optimal choice. Also, approach used in [1] was very similar to the approach used in [28]. It is assumed that the converter's fundamental waveforms are dictated by the modulation scheme, independent of components or electrical parameters, which aids

in component sizing and ensures consistent current and voltage ripple. Ultimately, the conventional buck-boost topology was found to be the best for wide input voltage regulation. Consequently, optimizing the phase-modular buck-boost PV string dc-dc converter for DCMG applications, particularly in terms of power density and efficiency, is a significant approach for high-power systems (several kW).

Agrawal et al. [29] and Antivachis et al. [32] explore GaN-based buck/boost and buck-boost dc-dc converters for various applications, highlighting advancements in power density and efficiency. In [29], a converter achieves 1 kW output with 96% efficiency and a power density of 7.8 kW/L with forced air-cooling system. In [30], a 1 kW GaN-based interleaved bidirectional buck/boost converter with inverse coupled inductor reaches 98.5% efficiency. Li et al. [31] presents a 3.5 kW bidirectional GaN-based converter with six-phase interleaving, delivering 97.5% efficiency with 8.7 kW/L power density. Meanwhile, Antivachis et al. [32] describes a fuel-cell supplied motor drive system using an interleaved four-switch buck-boost converter, achieving 1 kW output power, 98.3% efficiency, and 6.6 kW/L power density. Although these studies demonstrate excellent performance within their specific applications, they are limited in addressing the requirements of high-power, high-switching-frequency, and high-power-density scenarios. While the reported power densities, efficiencies, and power ranges are adequate for their intended applications, they are primarily focused on low-power designs. These studies do not fully address the challenges encountered in high-power applications (several kilowatts), such as effective thermal management, achieving optimized soft-switching techniques, and mitigating core losses under high inductor current ripple conditions. There is significant potential for further advancements in these areas to meet the demands of high-power, high-frequency, and high-density operations.

This article presents significant contributions to the design and optimization of high-power, high power density, and high-efficiency dc-dc converters, particularly for solar string applications within dc microgrids (DCMG). The article introduces negative valley current mode (NVCM), also known as critical current mode (CRM), as an effective method for achieving zero-voltage turn-on in low-power applications [17]. Although CRM generates substantial current ripple, which can exceed twice the inductor current, the article addresses this challenge by interleaving multiple module cells to cancel the ripple at the switching frequency. This approach helps reduce the size of the EMI filter, a critical factor in maintaining system efficiency. The article explores the optimal number of interleaved cells required to maximize both efficiency and power density, while discussing the limitations of simply increasing the number of cells in high-power scenarios.

Moreover, the article identifies that the significant current ripple in high-power converters contributes to increased core losses in ferrite inductors, especially under high input currents and switching frequencies. To overcome this, air-core inductors are employed in PV string applications, effectively mitigating core losses and saturation currents. This not only enhances the power output but also improves the converter's power density. By combining NVCM operation with air-core inductors, the research

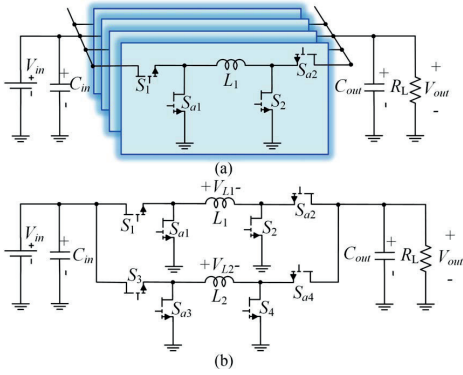


Fig. 1. (a) Voltage source modular interleaved dc-dc converter schematic. (b) Two-phase voltage source interleaved dc-dc converter schematic.

optimizes switching losses, inductor performance, and switching frequency, ensuring optimal efficiency.

Thermal management plays a crucial role in the performance of GaN-based converters, and this article provides an in-depth analysis of thermal strategies, including a tailored top-side cooling design, selection of heatsinks, and thermal interface materials (TIMs). The experimental findings demonstrate that the proposed design reaches an outstanding 99% efficiency, with power densities surpassing 17.5 kW/L and 6 kW/kg under high power conditions of 9 kW using natural convection heatsink. In contrast, previous studies [29], [30], [31], [32] reported power densities of 6.6–8.7 kW/L and maximum efficiencies of 96%–98.5% for output powers ranging from 1 kW to 3.5 kW. These findings highlight the substantial improvements in power density, efficiency, and thermal management for GaN-based dc-dc converters in high-power applications. Overall, this article offers valuable insights and practical guidelines for advancing power electronics in DCMG systems, renewable energy integration, and other high-power applications, providing a pathway to more efficient, compact, and reliable energy solutions.

II. OPERATION PRINCIPLE

A. Topology

The interleaved approach under examination, depicted in Fig. 1(a), derives from the established concept of modular interleaved 4-switch noninverting buck-boost converters interconnected at a shared ground point. In this configuration, each module represents a nonisolated buck-boost dc-dc converter cells connected to the negative dc terminal (ground). The optimal number of module cells N_{Module} depends on factors such as the converter's cost, the power board's area, the overall energy stored in the inductances, and efficiency. The findings reveal a linear increase in both cost and power board area with the addition of an extra buck-boost cell. Simultaneously, the energy stored in the inductances exhibits a linear decrease, allowing for a reduction in inductance size with a higher number of cells. The following study in the article (Section III-B)

identifies two module cells N_{Module} as the optimal number for this investigation which is done based on [33]. Fig. 1(b) depicts the interleaved converter with two identical dc-dc converter cells explored in this article. The PMC introduces several key advantages:

- 1) *Buck-boost capability*: Leveraging the inherent buck-boost characteristics of each phase-module, the interleaving allows for the regulation of the output voltage to the dc-link, which can be either higher or lower than the dc input voltage.
- 2) *High operational efficiency*: In the interleaved configuration, the input current divides among cells, leading to the distribution of total losses by the number of phases. Additionally, typically, only one out of the two half-bridges of each phase is actively switched at any given time. This approach effectively minimizes switching losses, resulting in a substantial improvement in the overall efficiency of the converter.
- 3) *Low input current ripple*: In the interleaved approach, the implementation of a phase shift operation between cells ensures minimal input current ripple and output voltage ripple. This, in turn, leads to the compensation of both output voltage and input current ripples, facilitated by the phase shift operation. This flexibility in managing both inductor current ripple and phase output voltage ripple reduces the necessity for high-value passive components in the converter design.
- 4) *Streamlined control strategy*: Each individual module within operates independently of the other module, adopting a straightforward control configuration reminiscent of traditional dc-dc converters. This simplicity not only improves overall system manageability but also enhances control efficiency.

Each individual module comprises two half-bridges: the buck half-bridge and the boost half-bridge. These are connected to opposite terminals of an inductor L . During the operational phase in which the converter's input voltage exceeds the output voltage ($V_{in} > V_{out}$), the converter operates in the buck mode, as illustrated in Fig. 2(a). In this configuration, only the buck half-bridge is activated. Conversely, when the converter's input voltage is lower than the output voltage ($V_{in} < V_{out}$), the converter shifts into boost mode, depicted in Fig. 2(b), where only the boost half-bridge is activated.

It is crucial to acknowledge that the operating point of each cell experiences a 180-degree phase shift in comparison to the other phase. This consideration is vital for a comprehensive understanding of the converter's behavior, especially with regard to the relative phase shifts between the two buck-boost converters.

A. Variable Frequency Zero-Voltage Turn-on

Employing a variable switching frequency scheme is essential to uphold zero voltage switching (ZVS) turn-on across the entire operational range of the converter. Maintaining ZVS turn-on and emphasizing the necessity to steer clear of hard-switching are critical for the converter's functionality for high switching conditions. This approach leads to a substantial reduction in switching

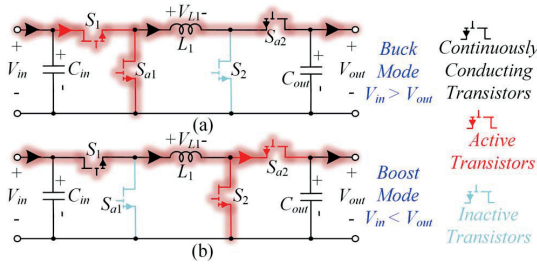


Fig. 2. Two operational modes of the dc-dc PMC: (a) buck mode, when the input voltage surpasses the output dc-link voltage ($V_{in} > V_{out}$); and (b) boost mode, when the output voltage is greater than the input voltage ($V_{in} < V_{out}$).

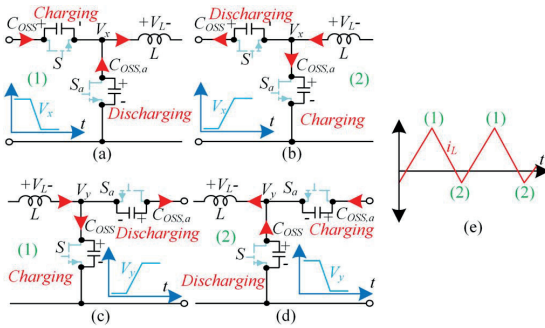


Fig. 3. Current paths involved in charging and discharging the drain-source capacitance during switching transients for both buck and boost operation modes. The diagram distinguishes between two scenarios for each mode: (a) upper turn-off and lower turn-on transient in buck mode; (b) upper turn-on and lower turn-off transient in buck mode; (c) lower turn-off and upper turn-on transient in boost mode; (d) lower turn-on and upper turn-off transient in boost mode; and (e) current flows through the inductor L (either L_1 or L_2) related to both buck and boost modes, demonstrating the peak and valley of the inductor current.

losses by not only eliminating the turn-on losses of the transistors but also eliminating their C_{OSS} losses.

In the switching transient, the inductor current I_L charges and discharges the drain-source capacitances, as illustrated in Fig. 3 outlining the current paths. Examining Fig. 3(b) and 3(d) for both boost and buck modes, ensuring zero-voltage turn-on for the main transistors and preventing the discharge of stored energy in the drain-source capacitors during transistors turn-on (to eliminate C_{OSS} losses) requires specific conditions.

It involves completely discharging the drain-source capacitor of the main transistor, to zero, and fully charging the drain-source capacitor of the auxiliary transistor to V_S (V_S is the blocking voltage across the transistors which is equal to the output voltage in the boost mode or input voltage in the buck mode) [34], [35]. Achieving zero-voltage turn-on for the transistor S necessitates the careful management of the stored energy in the inductor L during the turn-on transient of the transistor. This ensures that the parallel capacitors can discharge, or charge as needed, and this behavior can be effectively modeled as follows [14]:

$$0.5L \cdot I_{L-\text{Valley}}^2 \geq C_{Q,\text{eq}}(V_S) \cdot V_S^2 + 0.5C_{\text{Par}} \cdot V_S^2 \quad (1)$$

where $C_{Q,\text{eq}}$ and C_{Par} are the charge-equivalent capacitance of the main transistor and the parasitic capacitances at the switching node, including those from the PCB and the inductor's inherent capacitance, respectively. Also, $I_{L-\text{Valley}}$ is the minimum negative current through the inductor L . In this article, the parasitic capacitance C_{Par} is neglected due to the careful design of the PCB for high switching frequency conditions.

To ensure smooth ZVS completion before activating the auxiliary (S_a) transistor, the dead time T_d must be configured to exceed this transition time $\Delta T_{\text{SW-Transient}}$ [14], [36], [37]. By straightforwardly analyzing the circuits in Fig. 3 and approximating that the inductor current remains constant during the switching transient, the switching transient time $\Delta T_{\text{SW-Transient}}$ is determined as follows:

$$\Delta T_{\text{SW-Transient}} \approx V_S(C_{Q,\text{eq}}(V_S) + C_{Q,\text{eq},a}(V_S))/I_{L-\text{Valley}} \leq T_d. \quad (2)$$

In (2), $C_{Q,\text{eq},a}$ is the charge-equivalent capacitance of the auxiliary transistor. This analysis provides insights into the crucial interplay of inductor current, drain-source capacitance, and dead time in facilitating ZVS during the turn-on transient.

The variable frequency zero voltage turn-on (VFZVTO) scheme utilizes the switching frequency to regulate the ripple current in the inductors L_1 and L_2 . Achieving ZVS involves ensuring that the peaks and valleys of inductors L_1 and L_2 currents meet the ZVS boundary condition of dead time (T_d) and peak/valley inductor currents. Precisely controlling the switching frequency enables the strategic placement of peaks and valleys to consistently satisfy this boundary condition. Determining the desired placement of these inductors L_1 and L_2 current points involves setting the valley point to a predetermined value known as the inductor threshold current ($I_{L-\text{Valley}}$). $I_{L-\text{Valley}}$ is established based on the boundary condition derived from the transistors total output capacitance ($C_{Q,\text{eq}} + C_{Q,\text{eq},a}$). The value of $C_{Q,\text{eq}} + C_{Q,\text{eq},a}$ affects the switching transient time $\Delta T_{\text{SW-Transient}}$, and the dead time must surpass $\Delta T_{\text{SW-Transient}}$ to facilitate ZVS before activating the auxiliary transistor. Failure to achieve this sequence may lead to partial hard turn-on losses, compromising the maintenance of soft-switching. It is noteworthy to mention that while attempting to regulate the frequency for boundary conduction mode (BCM) of the dc-dc converter can achieve zero-current switching (ZCS) turn-on to eliminate turn-on switching losses of the main transistors, it does not address the C_{OSS} losses. These losses persist and contribute significantly to switching losses, particularly in high switching frequency conditions. The C_{OSS} losses, as computable in (3), can only be mitigated by ensuring a negative and appropriate inductor threshold current $I_{L-\text{Valley}}$.

$$P_{\text{SW}}^{\text{Loss}} = Q_{\text{OSS}}(V_S) \cdot V_S f_{\text{SW}} = C_{Q,\text{eq}}(V_S) \cdot V_S^2 f_{\text{SW}}. \quad (3)$$

In (3), f_{SW} is the switching frequency of the transistors and Q_{OSS} is the charge storing in C_{OSS} of the main transistors.

When dealing with positive average L inductor current, it is essential to establish the current ripple at a level where the valley point is situated below the negative threshold current level ($-I_{L-\text{Valley}}$). This arrangement ensures that the negative inductor

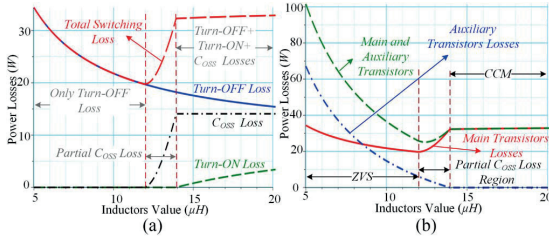


Fig. 4. Calculated switching losses for the interleaved dc-dc converter with 20 A input current, 350 V output voltage, 450 V input voltage, 217 kHz switching frequency versus various inductor values 5–20 μH (under three operation regions): (a) breakdown of switching losses for the main switches' turn-on loss, turn-off loss, C_{OSS} loss and total switching losses under three operation regions; and (b) switching losses of the main transistors, auxiliary transistors, and the total switching losses.

current effectively discharges the main transistor output capacitance during the turn-off transient of the auxiliary transistor. Soft-switching for the main transistors is attained when the negative inductor current ($-I_{L-\text{Valley}}$) completely discharges the main transistor output capacitances in the turn-off transient period of the auxiliary transistors. However, it is important to note that supplying a substantial negative valley current ($-I_{L-\text{Valley}}$) leads to significant turn-off losses for the auxiliary transistors, which is undesirable. Additionally, creating a high current ripple in the inductors to achieve a large negative valley current increases the turn-off current, leading to higher turn-off losses for the main transistors, which is also not recommended. To illustrate these, Fig. 4 depicts the theoretical switching losses of the interleaved dc-dc converter under specific operating parameters: 20 A input current, 350 V output voltage, 450 V input voltage, and a 218 kHz switching frequency. The theoretical breakdown of the main switches' switching losses, including the main switches' turn-on loss, turn-off loss, and C_{OSS} loss are shown Fig. 4(a). Since the auxiliary switches turn-on under ZVS conditions, only their turn-off losses are shown in Fig. 4(b). Fig. 4(b) displays the total switching losses for both the main and auxiliary transistors, as well as the combined overall switching losses. The analysis considers the use of GS66516T GaN transistors for S_{a1} – S_{a4} and GS66508T GaN transistors for S_1 – S_4 . For inductor values exceeding 14 μH , the converter operates under fully hard switching conditions, leading to significantly high switching losses. The converter operates in BCM when the inductor value is approximately 14 μH . Even though the main transistors switch on under ZCS, some C_{OSS} losses persist. When the inductor value ranges between 12 μH and 14 μH , C_{OSS} losses are partially mitigated, but the complete zero-voltage turn-on cannot be realized. For inductor values below 12 μH , C_{OSS} losses are entirely eliminated, enabling the main transistors to switch on entirely under ZVS conditions. However, lowering the inductor value below 14 μH increases turn-off losses for the auxiliary transistors, highlighting the need to avoid reducing the inductor value significantly below 12 μH . Additionally, enabling ZVS turn-on for the main transistors, reduces their switching losses and the resultant heat generation, significantly. This approach is particularly beneficial in GaN transistors, where managing heat dissipation presents a significant

challenge due to limitations in their cooling pad size. This reduction in heat production plays a crucial role in effectively managing the thermal conditions of GaN transistors, thereby enhancing the reliability and performance of the interleaved dc-dc converter. This fact is empirically demonstrated in Section IV of the article. However, designers should carefully navigate the tradeoff between the turn-off losses of the main transistors and the auxiliary transistors, taking into account the specifications provided in the datasheets for both main and auxiliary transistors. The determination of the switching frequency required to achieve the desired current ripple for any given $I_{L-\text{Valley}}$ value can be computed as follows:

$$f_{\text{SW}} = \begin{cases} (V_{\text{in}} - V_{\text{out}})d / 2L(I_{L-\text{AVG}} + |I_{L-\text{Valley}}|) & V_{\text{in}} > V_{\text{out}}, \text{Buck} \\ V_{\text{in}}d / 2L(I_{L-\text{AVG}} + |I_{L-\text{Valley}}|) & V_{\text{in}} < V_{\text{out}}, \text{Boost.} \end{cases} \quad (4)$$

In the given equation, V_{in} , $I_{L-\text{AVG}}$, V_{out} , and d represent the input voltage, average of each inductor current, output voltage, and the converter duty cycle, respectively, the values of the duty cycle d can be derived from the regulated output voltage and the obtained input voltage using the following equation:

$$d = \begin{cases} V_{\text{out}} / V_{\text{in}} & V_{\text{in}} > V_{\text{out}}, \text{Buck} \\ (V_{\text{out}} - V_{\text{in}}) / V_{\text{out}} & V_{\text{in}} < V_{\text{out}}, \text{Boost.} \end{cases} \quad (5)$$

To enhance efficiency, minimize conduction losses, and eliminate core losses, it is advisable to use low inductance values, allowing for the implementation of the air-core inductors. This approach eliminates the risk of core saturation at the peak inductor current point and completely eradicates core losses. Also, the ferrite cores exhibit frequency-dependent behavior, making them unsuitable for variable switching frequency conditions. However, practical implementations necessitate a relatively precise measurement of the inductance, denoted as L . The controller iteratively calculates (4) to determine the correct switching frequency required for achieving critical zero voltage turn-on. This iterative process ensures that the switching frequency is dynamically adjusted to maintain optimal zero voltage turn-on conditions in the system. As an example, utilizing (4) and (5) with inductors value $L = 12 \mu\text{H}$, the optimal switching frequency is presented in Fig. 5 for a scenario involving a 20 A input current, $I_{L-\text{Valley}}$ of -2 A , and a 350 V output voltage, across an input voltage range of 110–450 V.

At 350 V input voltage, the calculated frequency reaches zero. However, in practical terms, a switching frequency is zero for only one point particular. Therefore, in practical implementation, the minimum switching frequency is determined to be 18 kHz for input voltage ranges between 345 V and 355 V, which closely aligns with the output voltage of 350 V. Moreover, recognizing the need for the converter to operate within the range of 18–304 kHz, and to overcome limitations associated with switching frequency and eliminate core losses, adopting a GaN transistor-based converter with air-core inductors is deemed a suitable choice. This technology choice addresses the practical constraints and enables the converter to operate efficiently within the desired frequency range.

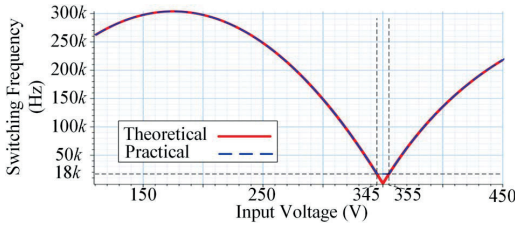


Fig. 5. Calculated optimal switching frequency for an interleaved dc-dc converter with inductors value (L) of 12 μ H, a 20 A input current, an inductor valley current ($I_{L\text{-Valley}}$) of -2 A, and a 350 V output voltage which covers a range of input voltages from 110 to 450 V, corresponding to input power levels of 2.2 to 9 kW.

III. DESIGN CONSIDERATIONS

A. Power Losses Analysis

In the realm of efficiency analysis and loss calculations, it is beneficial to consider this converter topology as comprising two distinct buck-boost converters, with each one dedicated to serving a single phase. This perspective enables the independent calculation of losses for each phase, and the efficiency of each phase provides a representative measure of the overall converter performance. It's essential to highlight that each individual buck-boost converter generates a dc output voltage of 350 V, introducing variations in its operating point relative to the input voltage.

The total converter loss can be dissected into three distinct components: transistors conduction loss, transistors switching loss, and inductor winding loss. In this analysis, capacitor losses are deemed negligible. As mentioned earlier, in this converter design, all transistors are configured to turn on under ZVS conditions. Consequently, the analysis neglects both the turn-on losses and C_{OSS} losses of all transistors. In the context of switching losses, the focus is solely on turn-off losses. The transistors switching losses can be computed using the following equation:

$$P_{SW} = \begin{cases} \begin{matrix} (+) I_{L\text{-Peak}} \text{ for Main transistor} \\ (-) I_{L\text{-Valley}} \text{ for Auxiliary transistor} \end{matrix} \\ \frac{1}{2} V_{in} \left(\frac{I_{in} \pm \frac{(V_{in}-V_{out})V_{out}}{2f_{SW}V_{in}L}}{2} \right) f_{SW}(t_{rv} + t_{fi}) & V_{in} > V_{out} \\ \frac{1}{2} V_{out} \left(\frac{I_{in} \pm \frac{V_{in}(V_{out}-V_{in})}{2f_{SW}V_{out}L}}{2} \right) f_{SW}(t_{rv} + t_{fi}) & V_{in} < V_{out} \end{cases} \quad (6)$$

In the provided equations, t_{rv} and t_{fi} represents the drain-source voltage rise time and current fall time during the turn-off period for each transistor which can be obtained from the

datasheets of the transistors. Equation (6) is thoroughly explained in [38], [39], [40], including the calculations for the t_{rv} and t_{fi} values from the parameters presented in transistors datasheets. The conduction losses of the transistors can be calculated using formula $P_{S}^{Cond.} = R_{DS\text{-Main}} \cdot I_{DS\text{-rms}}^2$, which involves determining the root-mean-square (rms) current flowing through the transistors as follows:

$$P_{Main}^{Cond.} = \begin{cases} R_{DS\text{-Main}} \cdot f_{SW} \int_0^{d/f_{SW}} \left(I_{L\text{-Valley}} + \frac{V_{in}-V_{out}}{L} t \right)^2 dt & V_{in} > V_{out} \\ R_{DS\text{-Main}} \cdot f_{SW} \int_0^{d/f_{SW}} \left(I_{L\text{-Valley}} + \frac{V_{in}}{L} t \right)^2 dt & V_{in} < V_{out} \end{cases} \quad (7)$$

$$P_{Auxiliary}^{Cond.} = \begin{cases} R_{DS\text{-Aux}} \cdot f_{SW} \int_0^{(1-d)/f_{SW}} \left(I_{L\text{-Peak}} - \frac{V_{out}}{L} t \right)^2 dt & V_{in} > V_{out} \\ R_{DS\text{-Aux}} \cdot f_{SW} \int_0^{(1-d)/f_{SW}} \left(I_{L\text{-Peak}} + \frac{V_{in}-V_{out}}{L} t \right)^2 dt & V_{in} < V_{out} \end{cases} \quad (8)$$

In (7) and (8), R_{DS} is the drain-source conducting resistance of the main and auxiliary transistors. Lastly, the winding losses of each inductor can be calculated by determining the rms current flowing through the inductors as follow to as shown in (9), at the bottom of this page.

In (9), R_{dc}^L represents the dc resistance of each inductor. It is important to note that, given the variable switching frequency range of the converter (18–304 kHz), the conducting resistance of the inductors is subject to change due to the skin effect. Also, in (9), F_r is a factor that links the dc resistance to the ac resistance, which takes into account all winding losses when an ac current with an rms value is applied. If the conductor's diameter is less than the skin depth and there are many strands ($n_{Litz} > 25$), F_r can be approximated using an approach provided in [43] and is shown in the following equation:

$$F_r = 1 + (ml \times \pi \times \mu_0 \times K_{Layer} \times f_s / 12 \rho_w)^2 \times n_{Litz} \times d_s^4 \quad (10)$$

where ρ_w represents the resistivity of copper, d_s is the diameter of the copper conductor, K_{Layer} denotes the layer utilization factor (discussed in detail in [43]), and m_l refers to the number of layers in the winding.

B. Selection Between Air-Core and Magnetic-Core Inductors

To demonstrate the advantages of air-core inductors, we designed and compared air-core inductors with ferrite-core

$$P_L^{Cond.} = \begin{cases} F_r R_{dc}^L f_{SW} \int_0^{d/f_{SW}} \left(I_{L\text{-Valley}} + \frac{V_{in}-V_{out}}{L} t \right)^2 dt + \int_0^{(1-d)/f_{SW}} \left(I_{L\text{-Peak}} - \frac{V_{out}}{L} t \right)^2 dt & V_{in} > V_{out} \\ F_r R_{dc}^L f_{SW} \int_0^{d/f_{SW}} \left(I_{L\text{-Valley}} + \frac{V_{in}}{L} t \right)^2 dt + \int_0^{(1-d)/f_{SW}} \left(I_{L\text{-Peak}} + \frac{V_{in}-V_{out}}{L} t \right)^2 dt & V_{in} < V_{out} \end{cases} \quad (9)$$

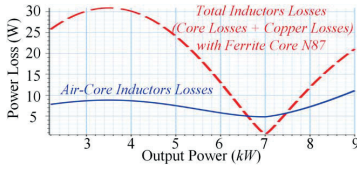


Fig. 6. Comparison of total inductors losses with ferrite core N87 and air-core versus the output power.

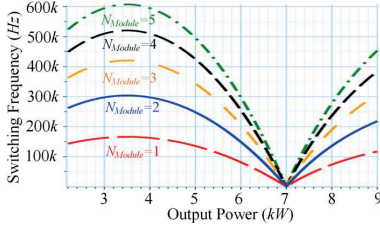


Fig. 7. Calculated optimal switching frequency for a modular dc-dc converter with various number of module cells N_{Module} .

inductors, using the EPCOS N87 Mn-Zn ferrite material, which is suitable for the converter's operating frequency range. Fig. 6 illustrates the comparison of total losses (both core and copper losses) between ferrite-core inductors and air-core inductors across varying output power levels. The results clearly indicate that air-core inductors exhibit much lower losses than N87 ferrite-core inductors, particularly at high switching frequencies and in conditions with large inductor current ripples. Therefore, utilizing air-core inductors in the proposed design optimization significantly reduces power losses and enhances the converter's overall efficiency.

C. Determining the Optimum Number of Module Cells N_{Module}

The operating conditions for the converter are as follows: the input voltage range is 110–450 V, the input current is 20 A, the output voltage is 350 V, and the output power range is 2.2–9 kW. As discussed in the main manuscript, to ensure ZVS operation for the transistors, the $I_{L-Valley}$ current should be -2 A. Based on these conditions, the optimal variable switching frequency for different numbers of cells is shown in Fig. 7. It should be mentioned that, increasing the number of module cells (N_{Module}) causes the current through each inductor to be distributed among the cells, thereby reducing the average current through each inductor. As the average current per cell decreases, the required current ripple for ZVS operation also diminishes. As a result, the switching frequency increases [because of reduction of current ripple, also considering (4)] with a higher number of module cells. Therefore, while increasing the number of module cells N_{Module} reduces the RMS current through the transistors and inductors, it significantly increases the required switching frequency. The calculated switching and conduction losses for the transistors with varying numbers of module cells (N_{Module}) are shown in Fig. 8(a) and 8(b). From these figures, it can be concluded that It should be noted that although increasing the

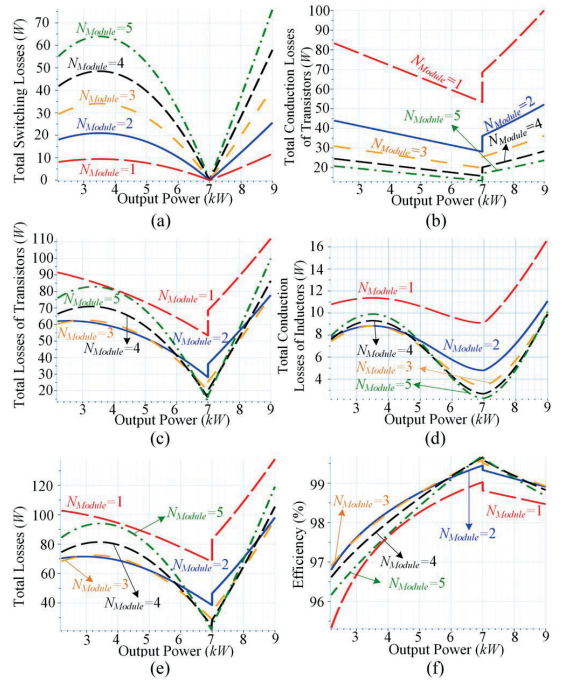


Fig. 8. Theoretical losses and efficiency for an interleaved dc-dc converter with various number of module cells N_{Module} : (a) total conduction and switching losses of transistors; (b) total inductors losses; (c) total losses versus output power; and (d) efficiency versus output power.

number of module cells reduces conduction losses through the transistors, it also significantly increases the switching losses (turn-off losses) due to increasing the required switching frequency. Furthermore, increasing the number of module cells beyond $N_{Module} = 2$ does not result in a substantial reduction in the transistors' conduction losses.

The total transistor losses, accounting for both conduction and switching losses, are presented in Fig. 8(c). It is evident that increasing the number of module cells from $N_{Module} = 1$ to $N_{Module} = 2$ significantly reduces total transistor losses, but further increases in the number of module cells not only add more components but also raise the total transistor losses. Additionally, it should be noted that higher transistor losses lead to increased heatsink requirements, which, in turn, raise the total volume and weight of the converter. This also complicates thermal management, requiring higher-quality thermal interface materials to effectively transfer heat from the transistors to the heatsink. Moreover, it should be noted that, based on this figure, while the total transistor losses for $N_{Module} = 2$ are slightly higher than those for higher N_{Module} in some power ranges, the total losses for $N_{Module} = 2$ are lower in the critical power ranges where transistor losses are at their peak (at $P_{out} = 9$ kW). Since thermal management is designed around these critical points, using $N_{Module} = 2$ would result in a smaller heatsink volume compared to higher N_{Module} , leading to a reduced overall converter volume, number of components and increased power density.

The total conduction losses of the inductors for various N_{Module} values are also shown in Fig. 8(d). It should be noted that, although the average and rms currents through the inductors decrease as the number of module cells increases, the required switching frequency to achieve ZVS also rises with the number of module cells. Considering (10), it can be concluded that an increase in switching frequency leads to higher ac resistance in the inductors, which prevents the inductor conduction losses from decreasing when the number of module cells exceeds $N_{\text{Module}} = 2$ under high-frequency conditions.

Fig. 8(e) and 8(f) present the calculated total losses and efficiency of the interleaved dc-dc converter with varying numbers of module cells (N_{Module}) under the mentioned operation conditions. Based on these figures, it can be asserted that with $N_{\text{Module}} = 2$, the converter achieves the lowest total losses and the highest efficiency. Therefore, it can be concluded that $N_{\text{Module}} = 2$ not only allows for the design of an optimal heatsink size, contributing to the highest power density, but also enables the converter to achieve optimal efficiency.

D. Appropriate Thermal Management Strategy Based on Power Level

The power density of the converter relies on the inductors size and the chosen heatsink. Proper heat dissipation from the transistors to the ambient is crucial for efficient operation. The size of the heatsink is determined by the power losses (conduction and switching losses) through the transistors. The converter comprises eight transistors S_1 – S_4 and S_{a1} – S_{a4} . Main transistors require high switching performance, while auxiliary transistors should have low conduction losses (low R_{DS}). Therefore, different transistors are chosen for the main and auxiliary roles. To guide heatsink and TIM selection, understanding the thermal resistance ($R_{\theta JC}$) and maximum power loss of each transistor is essential.

The thermal design approach for top-side cooling, including details on the selection of TIM and heatsink, is thoroughly discussed and supported by experimental validation in [23]. Furthermore, the article presents a detailed thermal model tailored to the interleaved Buck-Boost GaN transistor-based dc-dc converter, addressing key aspects of thermal management with the inclusion of a heatsink. This comprehensive analysis offers important contributions to the understanding of thermal management in GaN-based converter systems.

With an equal input current, conduction losses remain constant in boost mode across all input voltages. However, in buck mode, these losses increase linearly with the input voltage. On the other hand, switching losses (turn-off losses) depend on the switching frequency and voltage stress across the transistors. Considering the worst-case scenario at 450 V input voltage (which has the highest conduction and switching losses for transistors, highest switching frequency in Buck mode, and highest voltage stress across the transistors), the heatsink design should focus on dissipating maximum heat. In the buck mode, S_1 and S_3 serve as main transistors, while S_{a1} and S_{a3} act as auxiliary transistors. S_{a2} and S_{a4} conduct continuously, and S_2 and S_4 remain off. The thermal equivalent circuit for one phase of the

interleaved GaN-based dc-dc converter involves three discrete top-side-cooling GaN transistors responsible for dissipating power losses is provided in Fig. 2 of reference [23]. The thermal modeling is conducted for one phase and can be extended to two phases by doubling losses and paralleling the thermal resistances. The model represents the interleaved Buck-boost dc-dc power converter, considering a shared natural convection heatsink for all top-side cooling transistors. This model incorporates parameters reflecting major heat transfer pathways within the converter, with power losses stemming from main, auxiliary, and continuously conducting transistors.

In GaN transistors, the restricted size of the thermal pad on their top highlights the importance of the TIM in facilitating efficient heat transfer. While the choice of an appropriate heatsink is vital, the effectiveness of heat transfer hinges significantly on the selection of an appropriate thermal interface. Without a carefully chosen thermal interface, optimal heat dissipation efficiency may not be achieved, even with the use of a large heatsink or an active cooling system.

Calculating the thermal resistance of a TIM from the top side of the transistor to the heatsink can be done straightforwardly by taking into account the thermal pad area of the transistor. The thermal resistances of the TIMs for each type of transistor can be determined using the thermal impedance value provided in their datasheet, utilizing the following equation [23]:

$$R_{\text{Thermal}}^{\text{TIM}} (^{\circ}\text{C}/\text{W}) = \frac{\text{Thermal impedance } (^{\circ}\text{C} \cdot \text{inch}^2/\text{W})}{\text{Thermal pad area } (\text{inch}^2)}. \quad (11)$$

The total maximum power losses for each continuously conducting transistor, main transistor, and auxiliary transistor within the 2.2–9 kW output power range are identified as 7.64 W, 26.58 W, and 4.64 W, respectively. When taking into account the thermal equivalent circuit for the converter [depicted in Fig. 2(b)] and thermal resistances of the transistors $R_{\theta JC}$ and TIMs $R_{\theta CS}$, thermal resistance of heatsink for each continuously conducting transistor, main transistor, and auxiliary transistor, can be calculated using the expression [23]

$$R_{\theta SA} = [(T_{\text{Junction}} - T_{\text{Ambient}})/2Q_{\text{Loss}}] - (R_{\theta JC} + R_{\theta CS})/2. \quad (12)$$

In this equation, T_{Junction} , T_{Ambient} , $R_{\theta SA}$, and Q_{Loss} denote the target junction temperature, ambient temperature which is considered 30°C, thermal resistance of the heatsink, and maximum power loss of the transistor, respectively. Typically, the maximum specified operating junction temperature in the transistor datasheet is utilized for T_{Junction} .

Determining the volume of a heatsink, considering its obtained thermal resistance, involves accounting for various additional factors. These factors encompass specific dimensions of the heatsink, the type of heatsink utilized, flow configuration, orientation, surface finish, altitude, and other pertinent parameters [41].

E. Efficiency and Power Density Optimization

When dealing with air core inductors, the calculation of their volume becomes simpler compared to inductors with a ferrite core. Since air core inductors typically have a coil wound

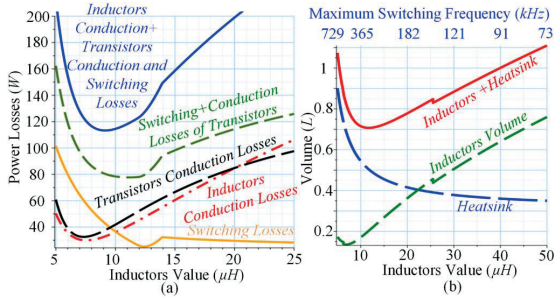


Fig. 9. Calculated switching and conduction losses of the transistors, conduction losses of the inductors, total losses, inductors volume, required heatsink volume, and total volume of heatsink and inductors versus the inductor values: (a) calculated losses for buck operation mode considering a constant 220 kHz switching frequency, 20 A input current, and 450 V input voltage; and (b) inductors, heatsink and inductors + heatsink volumes.

around a nonmagnetic form, the volume calculation can be approximated by considering the physical dimensions of the coil. Understanding the volume of air core inductors remains crucial for design considerations, particularly when assessing the overall physical layout, space constraints, and thermal aspects of the electronic system or circuit. Accurate volume calculations contribute to efficient system integration and optimization of the overall design. The volume of the inductors can be calculated as follows [42], [43]:

$$L = \frac{\mu_0 \pi n^2 a^2}{h + 0.9a + (0.32hc/a) + 0.84c}, a = \frac{r_1 + r_2}{2}, c = (r_2 - r_1) \quad (13)$$

where the symbols L , n , h , r_1 , and r_2 represent the inductance value, total number of turns, coil length in meters, coil inside radius in meters, and coil outside radius in meters, respectively. The suggested design for the solenoid inductor is rooted in the Brooks inductor geometry [42]. This geometry addresses the challenge of maximizing inductance with a given length of wire. Through research, it has been determined that among all possible rectangular sections, the optimal shape is a square, where the coil length (h) equals the coil thickness ($r_2 - r_1$). Additionally, it has been established that the coil outside radius should be approximately two times the coil inside radius, with the relationship $r_2 = 2r_1$. Therefore, (12) can be rewritten as $L = 2.029\mu_0(r_2 - r_1)n^2$. Utilizing the design procedures outlined in references [42] and [43], it is possible to determine the dimensions of the air-core inductors.

Fig. 9(a) illustrates the calculated switching and conduction losses of the transistors, as well as the conduction losses of the inductors, and the total losses in buck operation mode. These calculations are based on a fixed 220 kHz switching frequency, with a 20 A input current and a 450 V input voltage, considering the use of GS66516T GaN transistors for S_{a1} – S_{a4} , and GS66508T GaN transistors for S_1 – S_4 .

In this operational scenario, using a 14 μH inductor value leads the converter to operate in BCM, where the main transistors turn on under ZCS conditions. Decreasing the inductor value induces negative inductor valley current $I_{L-\text{Valley}}$, which

reduces the C_{OSS} losses of the main transistors. Sufficient negative $I_{L-\text{Valley}}$ can eliminate C_{OSS} losses and enable the main transistors to turn on under ZVS conditions. However, providing significant negative inductor valley current increases the turn-off losses of the auxiliary transistors, thereby increasing the total switching losses of the converter. Although the switching losses of the main transistors reach a minimum around a 12 μH inductor value, the minimum total switching losses occur at around 12.5 μH. Hence, reducing the inductor value significantly after reaching a sufficient negative valley current may not be advisable.

The minimum conduction losses for all transistors occur when the inductor value is approximately 7.5 μH. Conduction losses do not increase significantly when the inductor value increases to 12 μH, compared to the increase in total switching losses when decreasing the inductor value to around 10 μH. Therefore, the minimum total losses (conduction losses + switching losses) of the transistors are achieved at an inductor value of around 12 μH. Due to the mentioned thermal management challenge on GaN transistors, although maximizing power density is the design's primary goal, the generalized optimization strategy focuses on minimizing total transistor losses. Operating the converter at this point not only increases efficiency but also aids in thermal management for the GaN transistors, a critical consideration. Additionally, designing the converter to minimize transistor losses allows for the selection of a smaller heatsink volume to dissipate generated heat.

Furthermore, the minimum conduction losses of the inductors are observed at an inductor value of approximately 8 μH, attributed to the minimal value of conducting rms current through the inductors and low inductor resistance. However, the conduction losses of the inductors do not exhibit a significant increase for inductor values ranging from 8 μH to 12 μH. Consequently, the minimum total losses (comprising conduction losses of inductors and total losses of transistors) are recorded at an inductor value of approximately 9 μH. Nevertheless, there is no notable difference in losses (less than 10 W) for inductor values between 9 μH and 12 μH.

As depicted in Fig. 9(b), the graph illustrates theoretical correlation between the inductors value L and various parameters such as their volume, required heatsink volume, total volume of heatsink and inductors, and maximum switching frequency $f_{\text{SW-Max}}$ for specific operating conditions. Considering (4) and Fig. 5, the maximum switching frequency obtains at 175 V input voltage in boost mode. These conditions include a 20 A input current, an inductor valley current $I_{L-\text{Valley}}$ of -2 A, and a 350 V output voltage, spanning an input voltage range of 110–450 V. The analysis utilizes TG-A1780-150-150-0.8 thermal interface material, GS66516T GaN transistors for S_{a1} – S_{a4} , and GS66508T GaN transistors for S_1 – S_4 . It is evident from the figure that the minimum volume of the inductors can be attained within for 7–8 μH inductor values. Notably, there is no substantial increase in the volume of the inductors for inductor values ranging from 7 μH to 12 μH compared to their minimum volume. It is noteworthy that while reducing the inductor value leads to a decrease in the conducting resistance of the inductors R_L and the physical volume of the inductors, it also results in an increase in

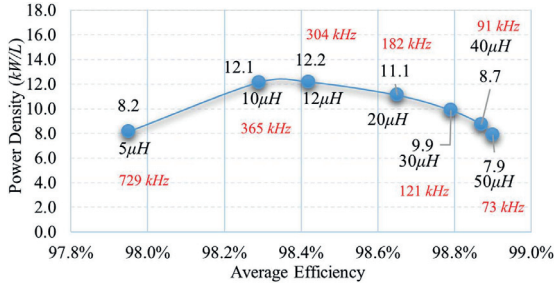


Fig. 10. Theoretical power density and maximum switching frequency [obtained from (4)] of the converter versus its average efficiency.

the switching frequency f_{SW} for the same operating conditions. This increase in switching frequency, in turn, raises the switching losses of the transistors. Higher switching losses necessitate a larger volume of heatsink to effectively dissipate the heat from the top side of the GaN transistors to the ambient. Consequently, decreasing the inductor value results in an increased volume of the heatsink. Given the emphasis on thermal management due to the use of GaN transistors, selecting the point of minimum losses for the transistors, particularly for the main transistors, is crucial. Operating the converter at the point of minimum losses for the transistors (around 12 μH inductor value) not only increases power density but also aids in transistor thermal management. It is evident from the figure that decreasing the volume of the inductors leads to an increase in the volume of the heatsink. While the volume of the inductors is at its minimum for a 7 μH value, there exists a significant difference in the heatsink volume between 5 μH and 10 μH inductors values due to the significant switching frequency and switching losses increase for the reduced inductors value. However, the difference in heatsink volume between 10 μH and 15 μH inductor values is not notably significant compared to the volume increase of the inductors, and any difference in the heatsink volume can potentially be mitigated by employing other techniques such as airflow configuration or surface finish. Therefore, the minimum total volume of the inductors and the heatsink is achieved with a 12 μH inductor value.

In Fig. 10, the theoretical power density and maximum switching frequency [obtained from (4)] of the converter is plotted against its efficiency. Notably, the maximum power density (with natural convection heatsink), reaching 12.2 kW/L, is achieved when the inductor value is set at 12 μH , accompanied by a theoretical average efficiency of 98.42%. The obtained efficiencies include solid-state circuit breaker (SSCB) losses ($P_{\text{Loss-SSCB}} = 2R_{\text{DS-SSCB}}I_{\text{out}}^2$), totaling 0.55–9.26 W for output powers ranging from 2.2 kW to 9 kW, where $R_{\text{DS-SSCB}}$ represents the conducting resistance of the SSCB switches and I_{out} is the output current. It's important to highlight that real power densities may increase with the utilization of particular dimensions of the heat sink, type of heat sink, flow configuration, orientation, surface finish, altitude, and other pertinent factors. Nonetheless, these results indicate that while larger inductor values can lead to higher efficiencies, for achieving optimal power density, a 12 μH inductor stands out as the most appropriate selection, providing both high efficiency and acceptability.

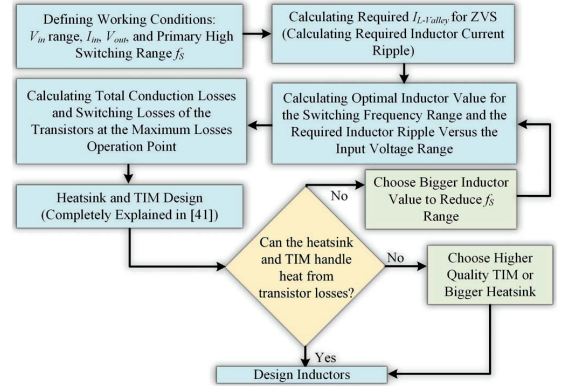


Fig. 11. Design optimization strategy for the GaN-based dc-dc converter.

TABLE I
CHARACTERISTICS OF THE LABORATORY PROTOTYPE OF THE GAN-BASED AIR-CORE DC-DC INTERLEAVED CONVERTER

Components Characteristics	
Air-core inductors L_1 and L_2	12 μH
Inductors L_1 and L_2 wire	3000 litz wires with 50 μm diameter
Input capacitor C_{in}	7.4 $\mu\text{F}/630\text{ V}$
Output capacitor C_{out}	4 $\mu\text{F}/630\text{ V}$
Natural convection (without airflow) heatsink	LAM5D1005 V, 100 $\times$ 100.5 $\times$ 50 mm ³
Thermal interface material	TG-A1780-150-150-0.8
Semiconductor elements	
Main GaN transistors ($S_1, \dots, S_4$)	GS66508T-TR, 30 A, 650 V
Auxiliary GaN transistors ($S_{a1}, \dots, S_{a4}$)	GS66516T-TR, 60 A, 650 V
Solid state circuit breaker SiC MOSFETs	IMZA120R007M1HXKSA1, 225 A, 1200 V
Operating point	
Input voltage range (V_{in})	110 V–450 V
Output voltage (V_{out})	350 V
Maximum rated power (P_{out})	2.2 kW–9 kW
Maximum input current (I_{in})	20 A
Switching frequency (f_s)	18 kHz–304 kHz

Fig. 11 outlines the design optimization strategy for a GaN-based dc-dc converter to achieve maximum efficiency and high-power density. For high power ranges, managing heat dissipation from the transistors' cooling pads—due to their limited surface area—is the primary concern [23]. Once effective thermal dissipation and minimum losses is ensured at the highest possible switching frequency and power, the next focus is inductor design. The switching frequency under high-power conditions should be sufficiently high to enable the use of low-value air-core inductors, which helps mitigate core losses under hard-switching and high current ripple conditions.

IV. EXPERIMENTAL RESULTS

A laboratory prototype of the GaN-based interleaved dc-dc converter with air-core inductors has been implemented and tested to validate the theoretical analysis. The specifications of the laboratory prototype are presented in Table I. The prototype

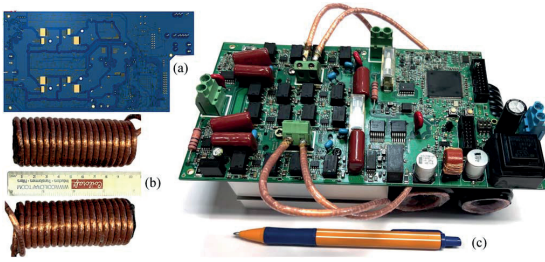


Fig. 12. (a) Designed PCB bottom side in altium designer. (b) Air-core inductors photo. (c) Laboratory prototype photo of the GaN based air-core interleaved dc-dc converter.

has a total volume of 0.51 L, which is determined by summing the volumes of the PCB and components (0.08 L), the inductors (0.1 L for two air-core inductors), and the heatsink (0.325 L for a natural convection heatsink without airflow). The total mass of the prototype is 1.5 kg. With both the mass and volume factoring in the inductors, heatsink and PCB, the resultant power density is calculated 17.65 kW/L and 6 kW/kg. Experimental results have been obtained for wide range of the input voltage ranging from 110 V to 450 V, while maintaining a constant output voltage of 350 V. The laboratory prototype of the converter and the air core inductors photos, along with its Altium PCB 3-D view of its bottom to show the location of GaN transistors at the bottom, has been depicted in Fig. 12.

The laboratory prototype comprises several parts, including a Texas Instruments DSP microcontroller TMS320F28379D, transistor driver circuits with gate driver ICs SI8271AB-IS, voltage and current sensors for the input and output ports, power circuit, and protection mechanisms such as solid-state circuit breaker, varistors, and fuses.

The thermal resistance for dissipating heat from the top surface to the surrounding environment for the heatsink (in the absence of airflow) ranges from 0.6°C/W to 1°C/W, as indicated in the heatsink datasheet. Additionally, the converter features two air-core inductors, each possessing a value of 12 μ H. These inductors are engineered to handle currents greater than 50 A and operate at a frequency of 6 MHz.

The experimental results comparing the performance of the converter under continuous conduction mode (CCM) with negative $I_{L-Valley}$ operation conditions with a 2 kW output power, 200 V output voltage, and 340 V input voltage are presented in Fig. 13. The junction temperature of the main transistor S_3 is measured 97°C for BCM operation (ZCS turn-on and 300 kHz switching frequency), whereas it is measured 67°C for negative $I_{L-Valley}$ operation conditions (ZVS turn-on and 250 kHz switching frequency). Although reducing the switching frequency from 300 kHz to 250 kHz (an 83% frequency reduction) to achieve ZVS turn-on and eliminate C_{OSS} losses in the main transistors, the temperature difference in the main transistor S_3 junction is significantly reduced. However, as observed in Fig. 13(a) and 13(b), the temperature of the auxiliary transistor S_{a3} increases slightly with negative $I_{L-Valley}$ operation, indicating the presence of turn-off losses on the auxiliary transistors due to negative $I_{L-Valley}$ operation. Nevertheless, as shown in Fig. 13(c),

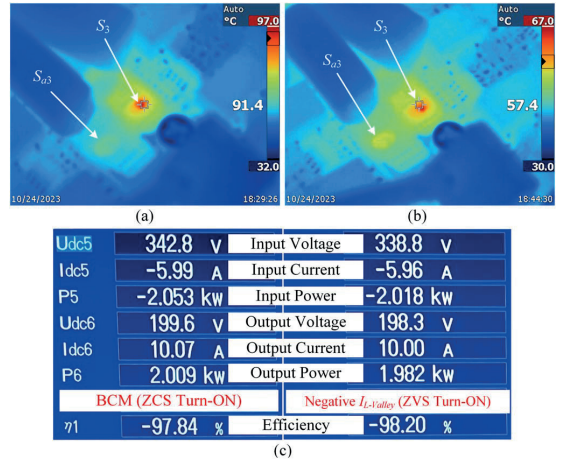


Fig. 13. Experimental results: comparison of the converter performance under CCM and negative $I_{L-Valley}$ operation conditions with 2 kW output power, 200 V output voltage, and 340 V input voltage. (a) Thermal camera photo of the junction temperature of the main transistor S_3 and auxiliary transistor S_{a3} in CCM with 300 kHz switching frequency. (b) Thermal camera photo of the junction temperature of the main transistor S_3 and auxiliary transistor S_{a3} in negative $I_{L-Valley}$ condition with 250 kHz switching frequency. (c) Measured efficiency of the converter under CCM (300 kHz switching frequency) and negative $I_{L-Valley}$ operation (250 kHz switching frequency) condition.

which demonstrates the measured efficiency by a power analyzer in both conditions, it can be concluded that the converter's efficiency increases from 97.84% to 98.2% (a 0.36% efficiency increase) by simply operating in the ZVS turn-on switching condition instead of the ZCS turn-on condition for the main transistors. These significant differences in the temperature of the main transistor S_3 and the overall converter efficiency highlight the importance of eliminating C_{OSS} losses in enhancing the performance of high-frequency GaN-based converter.

Fig. 14 presents experimental results of the converter in buck operating mode under specific conditions: 150 kHz switching frequency, 400 V input voltage and output voltage of 350 V with output power of 7.8 kW. In Fig. 14(a), waveforms of the drain-source voltage of the main transistor S_1 , the auxiliary transistor S_{a1} , inductor L_1 current, and input current (i_{in}) are shown. The average input current is approximately 19 A with very low ripple. The goal was to achieve the inductor valley current $I_{L-Valley}$ of -3 A to provide zero-voltage turn-on of the main transistors S_1 and S_2 , based on (1). This required an inductor current ripple of 28.3 A [based on (4)], which is provided in the experimental results and shown in the figure (inductor L_1 current). The voltage stress across the transistors equals the input voltage of 400 V without significant spikes, validating theoretical predictions.

In Fig. 14(b), thermal images from the thermal camera depict the junction temperature of the main transistor S_1 , the temperature of inductor L_1 , and the heatsink temperature. Utilizing a TG-A1780-150-150-0.8 TIM provides the thermal resistance of 1.34°C/W for the main transistor S_1 . The thermal junction-case resistance of the main transistor is $R_{\theta JC} = 0.5^\circ\text{C/W}$, which is provided in its datasheet. The theoretical temperature difference

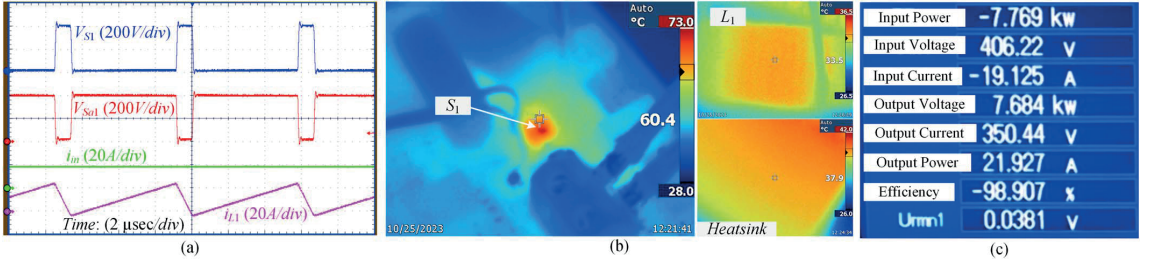


Fig. 14. Experimental results for buck operation mode of the converter with $f_S = 150$ kHz, $V_{in} = 400$ V, $V_{out} = 350$ V, $P_{out} = 7.8$ kW: (a) drain-source voltage of the main transistor S_1 , drain-source voltage the auxiliary transistor S_{a1} , inductor L_1 current, and input current (i_{in}) waveforms; (b) thermal camera pictures of the main transistor S_1 , inductor L_1 , and heatsink; and (c) power analyzer's measured efficiency.

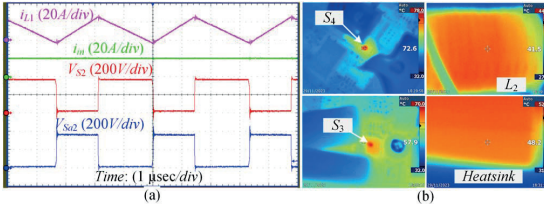


Fig. 15. Experimental results for boost operation mode of the converter with $f_S = 300$ kHz, $V_{in} = 200$ V, $V_{out} = 350$ V, $P_{out} = 4$ kW: (a) drain-source voltage of the main transistor S_2 , drain-source voltage the auxiliary transistor S_{a2} , inductor L_1 current, and input current (i_{in}) waveforms; and (b) thermal camera pictures of the main transistor S_4 , the main transistor S_3 , inductor L_2 , and heatsink.

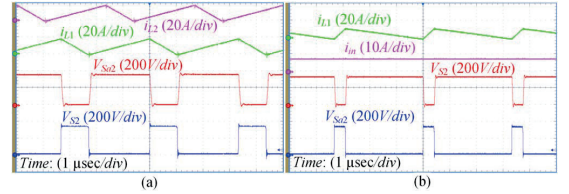


Fig. 16. Experimental waveforms for boost operation mode of the converter: (a) drain-source voltage of the main transistor S_2 , drain-source voltage the auxiliary transistor S_{a2} , inductors L_1 and L_2 currents waveforms with $V_{in} = 110$ V, $P_{out} = 1.9$ kW, $f_S = 300$ kHz, and $V_{out} = 350$ V; and (b) drain-source voltage of the main and auxiliary transistors S_2 and S_{a2} , inductor L_1 current, and input current (i_{in}) waveforms, $V_{in} = 300$ V, $P_{out} = 2.4$ kW, $f_S = 300$ kHz, and $V_{out} = 350$ V.

between the heatsink and junction of the main transistor with 18.14 W transistor total losses is calculated as 33°C. With a measured heatsink temperature of 42°C, the junction temperature is estimated to be 75°C, which corresponds closely to the measured temperature of 73°C for transistor S_1 . Fig. 14(c) illustrates the measured efficiency of the converter in the Buck operation mode, considering losses from the SSCB circuit, which amount to 3.48 W under the specified conditions. The measured efficiency via a power analyzer is 98.91%, confirming the calculated efficiency of 99.17%, validating theoretical predictions.

Fig. 15 showcases the experimental results of the dc-dc converter operating in the boost mode under the specific conditions: 300 kHz switching frequency, 200 V input voltage, 350 V output voltage and output power of 4 kW. In Fig. 15(a), waveforms of the drain-source voltage of the main transistor S_2 , the auxiliary transistor S_{a2} , inductor L_2 current, and input current (i_{in}) are presented. The average input current measured around 20 A with very low current ripple. To achieve the target inductor valley current $I_{L-valley}$ of -3 A to provide ZVS and eliminate C_{OSS} losses for the main transistors in boost mode, an inductor current ripple of 26 A is required. As it is indicated in the figure, this value is provided in the experiment. The voltage stress across the transistors conforms to the output voltage of 350 V without notable spikes, confirming theoretical expectations.

In Fig. 15(b), thermal images taken by a thermal camera display the junction temperature of the main transistor S_4 , the junction temperature of the continuously conducting transistor in

Boost mode S_3 , the temperature of inductor L_2 , and the heatsink temperature. The calculated theoretical temperature differences between the heatsink and junctions of the main transistor S_4 and the continuously conducting transistor S_3 , with total losses of 14.28 W and 9.3 W, respectively, yield estimations of 26°C and 17°C. With a recorded heatsink temperature of 52°C, the estimated junction temperatures for S_4 and S_3 are 78°C and 69°C, respectively, closely resembling the measured temperatures of 78°C and 70°C for transistors S_4 and S_3 . The efficiency measured in this mode using the power analyzer is 98.1%, closely aligning with the calculated efficiency of 98.35% and thereby validating the theoretical predictions.

Additionally, the experimental waveforms of the input and inductor currents, along with the drain-source voltages of the transistors, were presented for two critical operating conditions: low input voltage with high switching frequency at $f_S = 300$ kHz, $V_{in} = 110$ V, $V_{out} = 350$ V, $P_{out} = 1.9$ kW (Fig. 16(a)), and low input current with high switching frequency at $f_S = 300$ kHz, $V_{in} = 300$ V, $V_{out} = 350$ V, $P_{out} = 2.4$ kW (Fig. 16(b)). These waveforms confirm the converter's capability to achieve soft switching (ZVS) under challenging scenarios. Consequently, by properly controlling the switching frequency and duty cycle, ZVS can be achieved for all transistors, thereby reducing switching losses and improving overall efficiency across diverse voltage and load conditions. This function is essential for ensuring thermal stability and enhancing the converter's performance in high-power, high-frequency applications.

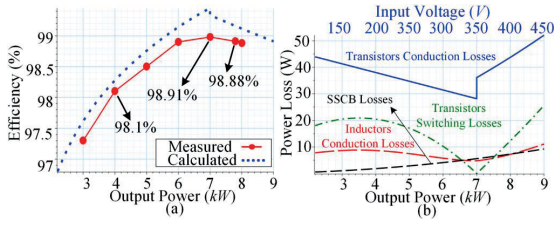


Fig. 17. Theoretical and experimental efficiencies and the theoretical power loss breakdown of the converter: (a) efficiency; and (b) loss breakdown.

Fig. 17(a) illustrates the efficiency curve of the converter for varying output power, adjusted with input voltages ranging from 110 V to 450 V. The efficiency measurement was conducted using the YOKOGAWA WT1800 precision power analyzer. Both experimental and theoretical efficiencies are provided, considering the SSCB circuit in the converter output port. Consequently, the efficiency of the converter without considering the SSCB losses is higher than the measured one. The maximum experimental efficiency, considering the SSCB losses (2.8 W at 7 kW output power, equivalent to 0.04% efficiency), is achieved 98.98% at 7 kW output power, while the theoretical efficiency is calculated 99.34% at the same power level. The minor difference between the theoretical and experimental efficiencies, possibly due to the conduction losses of the PCB or other components like *Coss* hysteresis losses, validates the calculations.

In Fig. 17(b), the theoretical power losses breakdown of the components for output power levels ranging from 2.2 kW to 9 kW (corresponding to input voltages of 110 V to 450 V and 20 A input current) is depicted. Transistor switching and conduction losses are calculated using (6)–(8) and transistor datasheet parameters, while inductor conduction losses are determined using (9) with ac resistance calculation based on variable frequencies provided in (10). The conduction losses of the solid-state circuit breaker are detailed in Section III-C. Additionally, the thermal camera images in Figs. 14(b) and 15(b) further validate the calculated transistor losses. These figures reveal that the major portion of the losses is attributed to the transistors' conduction and switching losses.

The noticeable step power loss difference in the transistors' conduction losses at 350 V input voltage arises due to changes in the configuration of the converter between boost and buck operation.

V. CONCLUSION

This article focuses on the developing dc–dc converter with wide input regulation range and outstanding performance metrics: achieving high efficiency (99%) and high-power density (17.7 kW/L and 6 kW/kg). These accomplishments are enabled by the integration of four key technologies. First, by employing GaN transistors and air-core inductors, the converter is free from limitations in switching frequency and core saturation current. Second, the variable frequency method facilitates the

generation of negative valley current for the inductors, enabling ZVS of the transistors. Thirdly, the use of air-core inductors eliminates the core losses associated with traditional core-based inductors, particularly advantageous in high switching frequency conditions. Lastly, two interleaved module cells configuration, provides very low input current and output voltage ripples along with optimization of all losses, especially the transistors losses. These key technologies are supported by comprehensive optimization analysis which can be used as the guidelines for design of similar converters. Experimental results with 9 kW prototype confirm all theoretical findings and feasibility of GaN semiconductors for industrial implementation.

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Paper III

P. Mohseni, S. Pourjafar, O. Matiushkin, O. Husev and D. Vinnikov, "Isolated High Step-Up Current-Fed DC-DC Converter With Low Input Current Ripple and Wide Full-Soft-Switching Capability," in *IEEE Transactions on Industry Applications*, vol. 61, no. 4, pp. 6499–6510, July-Aug. 2025, doi: 10.1109/TIA.2025.3544985.

Isolated High Step-Up Current-Fed DC-DC Converter With Low Input Current Ripple and Wide Full-Soft-Switching Capability

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Abstract—This paper presents a current-fed isolated, high step-up dc-dc converter that has the low voltage stress on the power switches. The suggested configuration achieves isolation between the input and output using a High-Frequency (HF) transformer. The leakage inductance of the transformer is harnessed to achieve Zero Voltage Switching (ZVS) during power switch turn-on and Zero Current Switching (ZCS) for power diodes across a broad range of operation. Furthermore, within this configuration, proper modulation (Phase Shift Modulation (PSM) or PSM with Pulse Frequency Modulation (PFM) combined with PSM) between the power switches enables the primary power switches to have soft turn-off conditions. Additionally, through this modulation technique, the input inductor experiences an effective frequency that is twice that of the power switches' switching frequency, leading to a reduction in the required size of the input inductor to half. Also, the auxiliary circuit eliminates the voltage spikes across the switches significantly, which occur due to the current difference between the input inductor and the leakage inductance of the transformer. To demonstrate the performance of the converter, the theoretical analysis along with comparisons to other converters are presented. Finally, to validate the theoretical analysis, the proposed converter is constructed to handle input voltages ranging from 20–50 V and operating at constant/variable switching frequency of 100–280 kHz,

resulting in an output voltage of 360 V, and a maximum output power of 400 W.

Index Terms—Current-fed converter, full soft switching, isolated boost converter.

I. INTRODUCTION

THE use of dc-dc converters has surged due to renewable energy growth, including solar, fuel cells, electric vehicles, and DC microgrids. Various configurations of dc-dc step-up systems have been suggested for transferring power from low to high voltage, encompassing both non-isolated and isolated design approaches [1]. Isolated converters utilize a magnetic coupling mechanism to transfer power from the input side to the output side without any direct electrical connection. This isolation feature reduces component stress but requires additional components, leading to increased power losses, weight, and costs due to the larger size of magnetic components such as transformers and inductors compared to other structures.

Bidirectional structures use power switches instead of diodes, as in unidirectional structures, and a control circuit is added to manage the turn-ON/OFF of these switches. These structures are suitable for onboard charging applications such as electric vehicles [2]. In renewable energy setups, the unidirectional isolated boost dc-dc converter can be classified as either a voltage-fed type or a current-fed type. In isolated converters, the most common topologies are the forward, flyback [3], push-pull, interleaved isolated [4], L-Ltype half-bridge [5], [6], [7], and full/half-bridge converter [8].

Current-fed isolated dc-dc converters offer advantages over voltage-fed isolated counterparts, including reduced input current ripples, inherent short-circuit protection, lower transformer turns ratio, high step-up ratios, wide voltage range regulation (allowing power to be drawn across a broad input voltage range), and improved current control. Moreover, they outshine their voltage-fed counterparts with a more reliable input-side inductor, which surpasses the lifespan of electrolytic capacitors used in the input. However, current-fed-isolated dc-dc converters are not without their challenges. They face significant challenges, including the need to charge the inductor at startup and the

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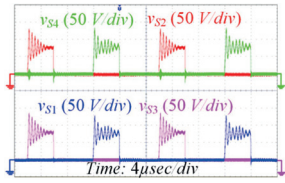


Fig. 1. Experimental voltage stress waveforms in isolated current-fed converters across switches in the absence of any voltage spike suppression method.

presence of voltage spikes across the OFF switches due to mismatches in current between the input boost inductor and the leakage inductance of a high-frequency transformer [2]. This causes elevated voltage stresses around two times more on primary-side switches. Fig. 1 illustrates the voltage stress waveforms across the switches which is taken in the laboratory in the absence of any voltage spike suppression method. It is evident from the figure that the voltage spikes across the switches, without employing voltage spike suppression, reaches approximately 80% (resulting in a 60 V spike for a 75 V voltage stress). Due to this provided voltage spikes power switches with two times more voltage blocking rate need to be utilized leading to increased conduction losses and reduced efficiency [9], [10], [11]. Researchers have made significant efforts to address these challenges through innovative circuit design modifications, novel modulation strategies, and the incorporation of soft-switching techniques. This proactive research approach often explores inventive modulation methods and the introduction of additional components or circuitry to effectively enhance the performance of these converter topologies for specific applications [12], [13], [14], [15], [16], [17], [18], [19]. The choice of the clamping circuit is aligned with the ZVS-PWM (Pulse Width Modulation) commutation cell used in a boost converter, as referenced in [14], [15]. However, the chosen clamping circuit is consistent with the ZVS-PWM commutation cell discussed in [16] but for a half-bridge converter. The same clamping circuit has also been employed in a current-fed half-bridge converter, as mentioned in another reference [17]. A simple clamping circuit with a single switch has been presented in a current-fed ZVS active clamping full-bridge converter, which is described in another references [18], [19].

Although the provided clamping circuits are simple, their effectiveness has not been fully demonstrated in practical results, as voltage spikes of 40% to 50% are still present in their experimental waveforms. Moreover, the auxiliary switch must operate at twice the switching frequency of the main switches, which can limit the structure's ability to function at higher frequencies.

This paper builds upon the findings presented in the conference paper [26] and has been developed to delve deeper into a current-fed isolated, high step-up dc-dc converter topology. The primary emphasis is on minimizing voltage stress on power switches and enhancing soft switching capability. Utilizing a high-frequency transformer and exploiting its leakage inductance enables ZVS during power switch turn-on, effectively eliminating associated losses. Moreover, ZCS for power diodes eliminates reverse recovery losses. The converter supports both resonant and non-resonant soft-switching approaches. While the non-resonant approach or PSM reduces voltage stresses on switches, PFM combined with PSM or resonant modulation enables full soft switching, leading to increased switching frequency, reduced passive component volume, and enhanced

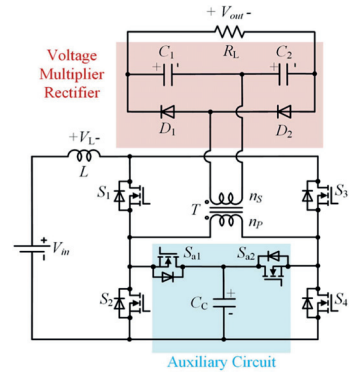


Fig. 2. The proposed isolated current-fed structure.

power density. Both strategies result in halving the required size of the input inductor by doubling its effective frequency. Additionally, the auxiliary circuit effectively mitigates voltage spikes across switches. These attributes render the converter topology suitable for photovoltaic applications, onboard or off-board chargers for electric vehicles, especially with a wide battery voltage regulation range.

II. PROPOSED STRUCTURE AND OPERATION MODES

A. Proposed Structure

The structure of the proposed soft-switched isolated current-fed structure is illustrated in Fig. 2. The proposed structure is composed of four main switches (S_1 - S_4), two auxiliary switches (S_{a1} and S_{a2}), one input inductor (L), one clamp capacitor (C_C), one High-Frequency (HF) transformer (T), two Voltage Multiplier (VM) diodes (D_1 and D_2), and two VM capacitors (C_1 and C_2). The output and input voltages and output load are named V_{out} , V_{in} , and R_L , respectively.

This structure can accommodate two types of soft-switching approaches: resonant and non-resonant. In the non-resonant approach, the clamp capacitor C_C is selected to maintain a constant voltage across it, thereby limiting the voltage stress across the transistors to the voltage of the clamp capacitor, V_{C_C} . In this method, the switching frequency remains constant across various operating conditions, including different input voltages. In this approach the modulation is only PSM (PSM involves shifting the phase angle of the gate signals of the switches S_1 - S_4 , S_{a1} and S_{a2} relative to the reference signal). On the other hand, in the resonant approach, the clamp capacitor's value is configured to resonate with the leakage inductance of the HF transformer. This resonance creates a half-sinusoidal voltage across the clamp capacitor, resulting in soft voltage increases and decreases during the turn-off and turn-on transients of the switches. This contrasts with the rapid voltage transients observed during these transitions in the non-resonant approach. In this approach, the switching frequency would be variable to provide the soft rising and falling voltages across the transistors. In this approach PSM modulation combined with PFM (PFM involves varying the frequency of the pulses while keeping the pulse width constant) is utilized. Fig. 3 illustrates the key waveforms of the proposed isolated current-fed structure in two operation approaches.

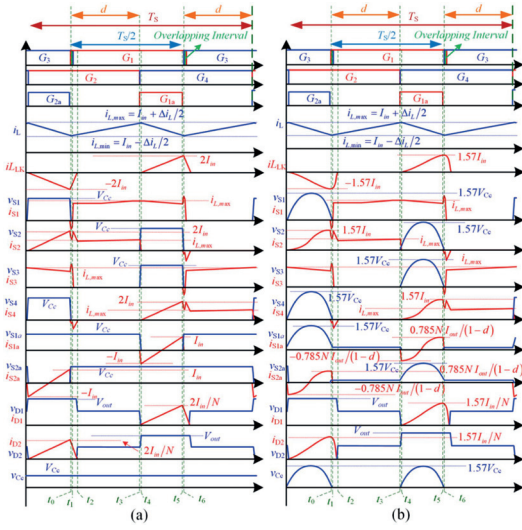


Fig. 3. Key waveforms of the proposed structure. (G_1 - G_4 , and G_{a1} and G_{a2} are the gate signals of switches S_1 - S_4 , and S_{a1} and S_{a2} , respectively.), (a) non-resonant approach, (b) resonant approach.

The operation modes of the proposed structure are divided into 12 operation modes. Due to the similarity of the modes to each other, only 6 modes of the one-half cycle are explained in this paper. As assumptions, the passive and active elements are considered ideal. The inductor L value, the magnetizing inductance value of the HF transformer T , and the values of the capacitors are high enough. Therefore, the current ripples of the inductor L , the magnetizing inductance of the HF transformer, and the voltage ripple of the capacitors are neglected during the switching period.

B. Operation Modes

Mode I [t_0 - t_1] (Fig. 4(a)): At t_0 , the voltages across power switches S_1 and S_4 drop to zero, their reverse body diodes begin to conduct. The current flowing through the secondary side winding and diode D_2 gradually diminishes to zero. To perform a turn-on with zero voltage switching for S_1 , the gate signal must be initiated during this stage. Moreover, the inductor L starts to charge by input voltage V_{in} , through switches S_1 and S_2 .

Mode II [t_1 - t_2] (Fig. 4(b)): At t_1 , the S_1 power switch can turn on under ZVS conditions due to the prior conduction of its anti-parallel body diode. When switch S_1 turns on, the current passing through switch S_3 drops to zero without any rise in the voltage across it. The inductor L continues to charge by input voltage, through switches S_1 and S_2 . The currents in both the primary and secondary side windings, as well as diode D_2 , steadily decrease until they reach zero through switch S_2 and the reverse body diode of S_4 .

Mode III [t_2 - t_3] (Fig. 4(c)): At t_2 , the currents through the primary and secondary side windings and VM diode D_2 reach zero, and the diode turns off under the ZCS condition. The inductor L continues to charge by input voltage, through switches S_1 and S_2 . Also, all other semiconductors are inactive or turned off.

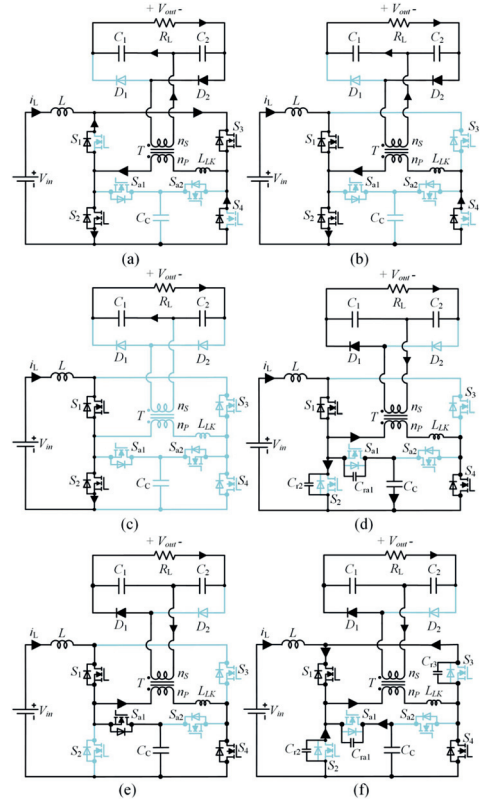


Fig. 4. Various operation modes of the presented structure, (a) Mode I, (b) Mode II, (c) Mode III, (d) Mode IV, (e) Mode V, and (f) Mode VI.

Mode IV [t_3 - t_4] (Fig. 4(d)): When power switch S_4 is turned on and power switch S_2 is turned off at time t_3 , using only the PSM method results in a rapid increase in voltage across switch S_2 , characterized by a hard turn-off condition. Conversely, employing both PSM and PFM leads to a gradual rise in voltage across switch S_2 from zero, with a minimal slope. Consequently, with the combined PSM and PFM approach, transistor S_2 switches off under nearly zero-voltage switching (ZVS) conditions.

Furthermore, the current through the inductor L begins to charge and discharge the parasitic capacitances of the auxiliary switch S_{a1} and the main switch S_2 . Furthermore, the voltage across switch S_3 begins to rise towards the clamping capacitor C_C voltage. Since its current had already reached zero in mode II, it turns off under ZCS conditions.

The values of capacitances C_{r2} and C_{ra1} (which correspond to the charge-equivalent capacitances of the main and auxiliary MOSFETs) are small, therefore, the time it takes to charge and discharge them is very short and it can be defined as follows:

$$t_4 - t_3 \approx (C_{r2} + C_{ra1}) (V_{Cc}) / i_L(t_3) \\ = (C_{Q,eq}(V_{Cc}) + C_{Q,eq,a}(V_{Cc})) (V_{Cc}) / i_L(t_3) \quad (1)$$

where $C_{Q,eq}$ and $C_{Q,eq,a}$ are the charge-equivalent capacitances of the main and the auxiliary MOSFETs, respectively. The parasitic capacitances at the switching node, including those from the inductor's inherent capacitance and the PCB, are disregarded due to the meticulous PCB design optimized for high switching frequency conditions.

Mode V [t_4 - t_5] (Fig. 4(e)): When the voltage across the main switch S_2 reaches V_{Cc} , the auxiliary switch S_{a1} 's reverse body diode begins conducting. The gate-source signal is then applied to the MOSFET S_{a1} , resulting in it commencing conduction as the current direction transitions from negative to positive. It should be considered that the gate-source signal must be applied to the auxiliary switch with a certain delay. This delay duration should exceed the time calculated in (1). Typically, this delay should be greater than 50 ns. This results in power switch S_{a1} turning on under zero voltage conditions. The disparity in current between inductor L and the leakage inductance L_{LK} charges and discharges the clamp capacitor C_C through auxiliary switch S_{a1} . The transformer secondary winding current starts to charge the VM capacitor C_1 through VM diode D_1 . In that condition, diode D_1 turns on under the ZCS condition. The leakage inductance L_{LK} (primary winding) current can be determined as:

$$i_{L_{LK}} = N i_{D1}. \quad (2)$$

Mode VI [t_5 - t_6] (Fig. 4(f)): At t_5 , S_{a1} , the auxiliary switch, turns off. As a result, the current through the HF transformer's secondary winding starts to decrease to zero. The difference in current between inductor L and the leakage inductance L_{LK} charges S_{a1} 's parasitic parallel capacitance to the voltage across the clamp capacitor C_C while discharging the parasitic capacitances of S_2 and S_3 down to zero. In the non-resonant approach, characterized by a nearly constant voltage across the clamp capacitor, it can be observed that the auxiliary switch S_{a1} turns off under hard switching conditions.

In contrast, in the resonant approach, where the voltage across the clamp capacitor is still near to zero, it can be asserted that the auxiliary switch S_{a1} turns off under conditions close to zero voltage switching (ZVS).

Because the values of capacitances C_{r2} , C_{r3} , and C_{ra1} (which correspond to the charge-equivalent capacitances of the main and auxiliary MOSFETs) are small, the time it takes to discharge and charge them is very short. This short time interval can be calculated as follows:

$$\begin{aligned} t_6 - t_5 &\approx (C_{r2} + C_{ra1} + C_{r3}) (V_{Cc}) / i_{L_{LK}}(t_5) - i_L(t_5) \\ &= (2C_{Q,eq}(V_{Cc}) + C_{Q,eq,a}(V_{Cc})) (V_{Cc}) / i_{L_{LK}}(t_5) - i_L(t_5) \end{aligned} \quad (3)$$

It should be considered that the gate-source signal must be applied to the main switch S_3 with a certain delay after the turn off moment of the auxiliary switch S_{a1} . This delay duration should exceed the time calculated in (3). Typically, this delay should be greater than 50 ns.

After this stage, the following half-cycle will be repeated, completing the full cycle of the converter in repetition.

III. STEADY STATE OF THE PROPOSED STRUCTURE

As steady-state assumptions, the intervals t_1 - t_3 and t_4 - t_5 (operation modes II, III, and V) are considerably longer than the other intervals. Consequently, in steady-state analysis, we do not consider short intervals.

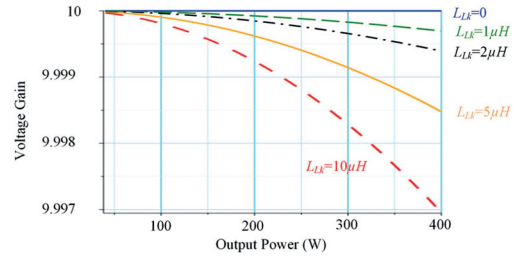


Fig. 5. Voltage gain graph versus output power (40 W-400 W) for various leakage inductance values considering the switching frequency of $f_S = 100$ kHz, overlapping interval of $d = 0.6$, and turns ratio $N = 2$.

A. Voltage Gain and Voltage Stress Calculations

By implementing the volt-second balance law to inductor L , the voltages of the capacitors C_C , C_1 , and C_2 are obtained as:

$$V_{Cc} = V_{in} / (1 - d) \quad (4)$$

$$V_{C1} = V_{C2} = NV_{Cc} = NV_{in} / (1 - d). \quad (5)$$

In (4)–(5), d is the overlapping intervals of the gate signals G_1 and G_2 , or G_3 and G_4 , and N is the turns ratio of the HF transformer n_s/n_p . The output voltage is equal to $V_{C1} + V_{C2}$.

Therefore, considering (5), the output voltage of the proposed converter is obtained as follows:

$$V_{out} = 2NV_{in} / (1 - d). \quad (6)$$

Regarding (6), it can be concluded that the voltage gain of the proposed structure depends on d and turns ratio N values.

Equation (6) provides the ideal output voltage without considering the leakage inductance effect of the HF transformer, which slightly reduces the voltage gain. To account for this effect, the voltage gain of the proposed structure is calculated as follows:

$$M = \frac{V_{out}}{V_{in}} = \frac{2N / (1 - d)}{1 + L_{LK} 8N^2 f_S / ((1 - d)^2 R_L)}. \quad (7)$$

As illustrated in (7), the gain depends not only on the parasitic leakage inductance L_{LK} but also on the load R_L and switching frequency f_S . Fig. 5 presents a graph of voltage gain versus load conditions for different leakage inductance values considering a high switching frequency of 100 kHz. It is observed that (7) converges to (6) as L_{LK} and f_S decrease. Conversely, as R_L increases (output power decreases), (7) simplifies to (6), indicating that the impact of leakage inductance becomes more effective at high power levels. However, based on Fig. 5, the effect of the leakage inductance within the 40 W- 400 W output power range in this converter is very low (maximum 0.03%) and can be considered negligible.

The voltage stress across all switches S_1 - S_4 and S_{a1} - S_{a2} are equal to the voltage across the clamp capacitor V_{Cc} . Considering (4), the voltage stresses across the power switches are written as follows:

$$V_{S1} = \dots = V_{S4} = V_{Sa1} = V_{Sa2} = V_{Cc} = V_{in} / (1 - d) = V_{out} / 2N. \quad (8)$$

The average conduction current through the main power switches S_1 - S_4 and VM diodes are obtained as follows:

$$I_{S1}^{Avg} = \dots = I_{S4}^{Avg} = N \cdot I_{out} / (1 - d) \quad (9)$$

$$I_{D1}^{Avg} = I_{D2}^{Avg} = 2I_{out}. \quad (10)$$

The voltage stress across the VM power diodes is equal to the output voltage V_{out} .

B. Passive Elements Design

The values of capacitors can be established according to their required ripple. Hence, the capacitance of capacitors are established by considering the voltage ripple as follows:

$$C_1 = C_2 = (1 + d)V_{out}/2\Delta V_C R_L f_S \quad (11)$$

In the above equations, f_S and ΔV_C are the switching frequency and voltage ripple of the VM capacitors, respectively. Inductor L value can be determined based on its designed input current ripple. Considering the designed input current ripple, the inductance value of inductor L can be calculated as:

$$L \geq dV_{in}/2f_S \Delta i_L \quad (12)$$

In (12), Δi_L is the current ripple of inductor L . According to (12), the effective switching frequency on inductor L is twice that of other current-fed converters, leading to half the current ripple compared to other structures. For example, if the switch frequency is set at 100 kHz, the effective inductor frequency is 200 kHz. Hence, a major advantage of this current-fed isolated structure is its smaller inductor size compared to other current-fed designs.

In the fourth mode of operation, the voltage applied to the primary winding of the high-frequency transformer is represented by (13):

$$V_{primary} = V_{in}/(1 - d) = 2n_p \times f_S \times \Delta B \times A_e/(1 - d). \quad (13)$$

This equation considers magnetic flux density (ΔB) and equivalent core area (A_e). The number of turns in primary and secondary windings (n_p and n_s) follows standard transformer design principles. Secondary winding current results from combined currents in the VM diodes. As a result, the RMS current value for the secondary winding can be obtained as follows:

$$I_{Secondary}^{RMS} = 2I_{out}\sqrt{(1 - d)}/(1 - d). \quad (14)$$

The root mean square (RMS) value of the current in the primary winding is equal to $N \times I_{Secondary}^{RMS}$. By using (14), the primary and secondary windings diameters of the high-frequency transformer can be determined.

Furthermore, (15) represents the RMS voltage across the primary winding of the transformer:

$$V_{Primary}^{RMS} = V_{in}\sqrt{(1 - d)}/(1 - d). \quad (15)$$

The high-frequency transformer's apparent power can be calculated by multiplying the RMS current and voltage of its primary winding.

N can be determined by calculating V_{out} and optimizing the power switch duty cycle. Increasing N reduces switch voltage stress. The HF transformer's turn ratio can be found using (16) derived from the peak inverse voltage of the chosen MOSFETs.

$$N \geq V_{out}/2V_{DS\max}. \quad (16)$$

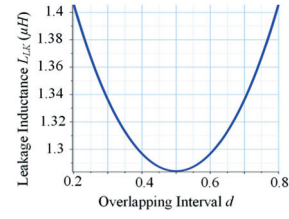


Fig. 6. The required leakage inductance relative to the converter's overlapping interval d , and considering the converter's minimum input current of 4 A.

C. Clamp Capacitor C_C Design and ZVS Realization

The value of the clamp capacitor can be established according to its required ripple. Therefore, the capacitance of the clamping capacitor is established by considering its voltage ripple as follows:

$$C_C = NV_{out}/2\Delta V_{Cc} R_L f_r. \quad (17)$$

In the equation provided, f_r represents the resonant frequency, which will be elaborated upon later, and ΔV_{Cc} signifies the voltage ripple of the clamp capacitor. By focusing on the time interval t_3 - t_6 in Fig. 3, the voltage variations across switches S_3 and S_2 , as well as the clamping capacitor C_C for both resonant and non-resonant approaches are clear. As it is obviously shown in the figure, in case of employing a non-resonant approach, it is crucial to maintain a low voltage ripple, typically around 10% of the voltage across the clamping capacitor $\Delta V_{Cc} = 0.1V_{Cc}$. However, when opting for a resonant approach, it is necessary to account for a voltage ripple approximately $\pi/2$ times the clamping voltage, $\Delta V_{Cc} \leq 1.57V_{Cc}$, to provide near ZCS turn off for all switches.

The auxiliary switches S_{a1} and S_{a2} achieve ZVS turn-on naturally due to their reverse body diodes. To guarantee ZVS during the turn-on of the main power switches S_1 - S_4 in non-resonant approach, the energy in leakage inductance L_{LK} must surpass the energy in parallel parasitic capacitances C_{r2} , C_{r3} , and C_{ra1} (which correspond to the charge-equivalent capacitances of the main and auxiliary MOSFETs $C_{Q,eq}$ and $C_{Q,eq,a}$) in Mode VI, as expressed by the following equation:

$$L_{LK} \geq \frac{(2C_{Q,eq}(V_{Cc}) + C_{Q,eq,a}(V_{Cc})) V_{out}^2}{4N^2 \left(\frac{2NP_{out}}{V_{out}(1-d)} - \frac{d(1-d)V_{out}}{8Nf_S L} \right)}. \quad (18)$$

The converter's minimum output power is set at 20% of its nominal capacity (400 W), equating to 80 W. Notably, the lowest output power from PV panels is reached when the panel voltage is at the lower limit of its operating range. Therefore, at an output power of 80 W, the converter's input voltage is considered in its minimum of 20 V, leading to a minimum input current of 4 A. Fig. 6 demonstrates the necessary leakage inductance to ensure ZVS operation of the converter in a non-resonant approach concerning the converter's overlapping interval d . Based on the minimum input current of 4 A (as derived from (18)), it is determined that a leakage inductance of 1.5 μH is adequate to achieve ZVS for the switches.

In the resonant approach, since the voltage across the MOSFETs reaches to nearly zero before they turn ON, the parallel parasitic capacitors are already discharged before the MOSFETs are turned-ON. Therefore, in the resonant approach, (18) is not necessary for ensuring ZVS turn-ON of the MOSFETs.

Furthermore, in order to achieve zero voltage turn-on for the main switches S_1 - S_4 , the duration during which the auxiliary switches S_{a1} and S_{a2} conduct, equal to $(1-d)T_S/2$ (where T_S is the switching period), should be shorter than the resonance period T_r provided by the clamp capacitor C_C and the leakage inductance L_{Lk} of the HF transformer in mode V. The resonant frequency f_r and period T_r can be calculated using (19).

$$f_r = 1/T_r = 1 / \left(2\pi \sqrt{L_{Lk} C_C} \right). \quad (19)$$

In the only PSM approach, where the clamping capacitor has a large value (several micro-farads), the resonant period is significantly longer than $(1-d)T_S/2$. Consequently, in this approach, the switching frequency can remain constant and equal to $f_s = f_r(1-d)/2$. In contrast, in the PSM along with PFM approach, the clamping capacitor is chosen much smaller values (several nano-farads) to resonate with the leakage inductance within the switching frequency range. As a result, the switching frequency must be regulated to ensure that $(1-d)T_S/2$ is shorter than the resonant period T_r . Hence, in this approach, the switching frequency varies according to the resonance frequency f_r and the overlapping interval d as follows:

$$f_s > f_r(1-d)/2 = (1 / (2\pi \sqrt{L_{Lk} C_C})) (1-d)/2. \quad (20)$$

IV. EFFICIENCY ANALYSIS

In the presented configuration, all power switches achieve ZVS during turn-on, with switches S_1 and S_3 additionally achieving ZCS during turn-off. The resonant approach offers the advantage of nearly achieving ZCS during turn-off for the remaining power switches, a feature not available in the non-resonant approach. Although the resonant approach provides full soft-switching conditions (ZVS turn-on, and ZCS or near ZVS turn-off) for all power switches, it's important to note that the voltage stress across the switches should be considered 1.57 times more than the value obtained in (8). Consequently, while the resonant approach effectively eliminates significant switching losses, unlike the non-resonant approach where only turn-off losses of switches S_2 , S_4 , S_{a1} , and S_{a2} are taken into account, the doubled voltage stress across the switches necessitates the use of power switches with higher conducting resistance, leading to increased conduction losses compared to the non-resonant approach. Therefore, when considering conduction losses and switching losses, the designer must carefully weigh the trade-offs to determine the optimal approach. Moreover, in the proposed structure, VM diodes switch on and off under zero-current conditions. Thus, although it is low, switching losses in this structure for the non-resonant approach pertain solely to the turn-off losses of switches S_2 , S_4 , S_{a1} , and S_{a2} , which are equal and calculated as follows:

$$P_{S2} = P_{S4} = P_{SWa1} = P_{SWa2} = \frac{P_{out} f_s (t_{rv} + t_{fi})}{2(1-d)} \quad (21)$$

In (21), P_{out} and $f_s = 100$ kHz are the converter output power, the turn-off time utilized power MOSFETs, and switching frequency, respectively. The parameters t_{rv} and t_{fi} denote the rise time of the drain-source voltage and the fall time of the current during the turn-off for each MOSFET. These values can be derived from the MOSFET datasheets. Equation (21) is

TABLE I
RMS CURRENTS EQUATIONS OF THE COMPONENTS

Component	RMS current
Main power switches (S_1 - S_4)	$\sqrt{2}N V_{out} / R_L (1-d) = 7.07 \text{ A}$
Auxiliary power switches (S_{a1} & S_{a2})	$\sqrt{2}N V_{out} \sqrt{(1-d)} / (2(1-d)R_L) = 2.36 \text{ A}$
VM power diodes (D_1 & D_2)	$V_{out} \sqrt{2(1-d)} / R_L (1-d) = 2.36 \text{ A}$
Inductor L	$2N V_{out} / R_L (1-d) = 10 \text{ A}$
Primary of the HF transformer	$2N V_{out} \sqrt{(1-d)} / R_L (1-d) = 6.67 \text{ A}$
Secondary of the HF transformer	$2V_{out} \sqrt{(1-d)} / R_L (1-d) = 3.33 \text{ A}$
Clamp capacitor C_C	$N V_{out} \sqrt{(1-d)} / (1-d) R_L = 3.33 \text{ A}$
VM capacitors (C_1 & C_2)	$V_{out} \sqrt{1+d^2} / R_L (1-d) = 2.94 \text{ A}$

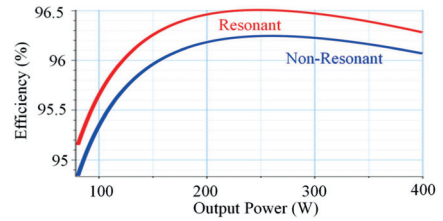


Fig. 7. Theoretical efficiency of the proposed converter in both resonant and non-resonant approaches considering 40 V input voltage.

comprehensively detailed in [27], where the process for calculating t_{rv} and t_{fi} based on the parameters found in the MOSFET datasheets is fully explained.

To compute conduction losses in the proposed structure, it is necessary to calculate the RMS currents of the components using the equations provided in Table I.

Fig. 7 illustrates the theoretical efficiency diagrams of the proposed converter for both resonant and non-resonant approaches. The maximum theoretical efficiencies achieved are 96.51% for the resonant approach and 96.25% for the non-resonant approach, both at an output power of 250 W. The resonant approach yields higher efficiency because it eliminates switching losses entirely, unlike the non-resonant approach. However, this advantage comes despite the resonant approach imposing 1.57 times higher voltage stress on the switches. Consequently, designers must select switches with approximately 1.57 times higher voltage ratings, which also have around 1.57 times higher conduction resistance.

V. CONTROL SYSTEM EXPLANATION

The simplified configuration of the control system, which utilizes a proportional-integral (PI) controller, is depicted in Fig. 8. This system incorporates a phase shift and switching calculation block, a pulse width modulation (PWM) block, and a PI regulator. To facilitate practical implementation using a microcontroller, a digital PI controller is employed. The conventional PI regulator's gain curve or transfer function is represented in the Laplace domain, but by applying a bilinear transform, the continuous PI controller can be converted into its digital form in the z-domain [28]. The digital PI controller comprises associated coefficients, sample delay blocks, and summation. A constant voltage reference of 360 V is fed into the regulator. The difference between this reference voltage and the

TABLE II
 COMPARISON OF THE PROPOSED CONVERTER WITH OTHER ISOLATED DC-DC CONVERTERS

Converter	Number of components						Normalized Voltage Stress on Switches	Soft switching of switches	Soft switching of diodes	Voltage spike on primary switches
	Switch	Inductor	Capacitor	Diode	Transformer	Total				
Ideal Flyback (with snubber circuits) [30]	1	1 (coupled Inductor)	1	1	0	4	K_r/ND^*	Hard	Hard	Low, $K_r=1.2 \sim 1.3^{**}$
Active Clamped Flyback [31]	2	1 (coupled Inductor)	2	1	0	6	K_r/ND	ZVS Turn-on	ZCS	Very low, $K_r=1$
Current-Fed Full-Bridge [20]-[23]	6 or 8	1	1 or 2	0 or 2	1	10-14	$K_r/2N$ or K_r/N	Primary full ZCS (C_{OSS} Loss is not solved), Secondary ZVS Turn-on	-	High, $K_r=1.5 \sim 2$
Active Clamped Current-Fed Full-Bridge [19]	5	1	2	4	1	13	K_r/N	ZVS Turn ON	ZCS	High, $K_r=1.5$
Full Soft Switching Current-Fed Full-Bridge [11]	8	1	2	0	1	12	$K_r/2N$	Primary full ZCS (C_{OSS} Loss is not solved), Secondary ZVS Turn-on and near-ZCS Turn-off	-	High, $K_r=1.5$
L-Ltype Half-Bridge [5]	4	2	2	4	1	13	K_r/N	ZVS Turn-on	ZCS	Very low, $K_r=1$
L-Ltype Half-Bridge [6], [7]	4	2	2	4	1	13	K_r/N	ZVS Turn-on	ZCS	High, $K_r=1.5$
Proposed	Non-resonant	6	1	3	2	13	$K_r/2N$	ZVS Turn-on, Partially ZCS Turn-off	ZCS	Very low, $K_r=1$
	Resonant	6	1	2 + 1 small	2	13	$\pi K_r/4N$	ZVS turn-on and ZCS or near ZVS turn-off	ZCS	Very low, $K_r=1$

* D is the duty cycle of the power switches in the Flyback converter. For the comparison analysis the duty cycle $D=d$ is considered.

** The variable " K_r " represents peak voltage overshoot which is within the range of 1 to 2. This overshoot in voltage occurs due to the disparity between the transformer's leakage inductance current and the input inductor current.

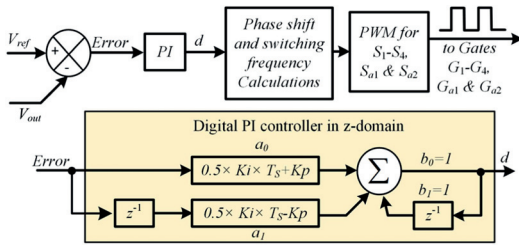


Fig. 8. Control system block diagram.

measured output voltage is supplied to the PI regulator's input. The PI regulator then computes the current sample modulation signal, denoted as d , for use in the phase shift and switching frequency calculation block. At the conclusion of each sampling period, overlapping intervals for gate signals G_1 and G_2 , or G_3 and G_4 , are determined, which are critical for phase shift calculation between gate signals and switching frequency calculation (using for the resonant approach), as described by (20). The computed values for phase shift and switching frequency are sent to the PWM block, which then generates gate signals for switches S_1 - S_4 , S_{a1} and S_{a2} , to regulate the desired output voltage.

VI. RESULTS OF COMPARISON

The proposed structure is compared to other well-known state-of-the-art isolated configurations (Flyback, Current-Fed Full-Bridge, and L-Ltype Half-Bridge converters) in terms of parameters like capacitor, inductor, and HF transformer sizes, primary side semiconductor conduction losses, switching losses, and primary side switch voltage stress. The comparison results are presented in Table II and Fig. 9. Fig. 9 shows the proportional values for conduction losses, switching losses, and total voltage stress experienced by the semiconductors. Additionally, the figure illustrates the relative sizes of the inductors and capacitors. All measurements are presented in a comparative format and

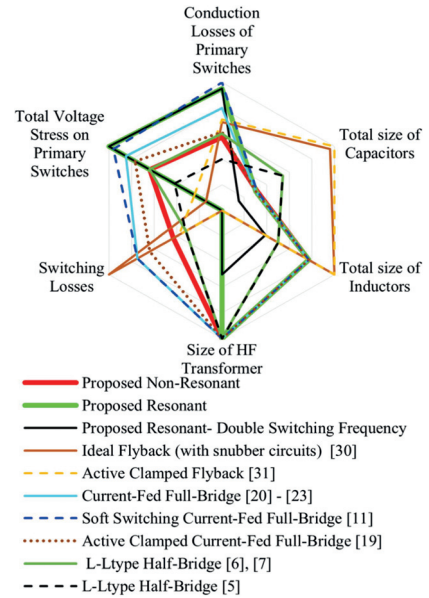


Fig. 9. Performance results of comparison of the proposed structure with other already presented structures.

normalized to their highest values (1 p.u.). Based on the parameters presented in the figure, we cannot definitively assert that the proposed converter excels in every aspect. However, it highlights the advantages and disadvantages of our design in comparison to other alternatives.

When comparing passive component volumes, consider that specific component values must ensure consistent maximum current ripple across the inductor and maximum voltage ripple across the capacitor at a given operating point. Since the input voltage varies between 20-50 V in these converters, the values

and sizes of the passive components should be calculated and compared in the worst condition of each structure. The size of capacitors and inductors is proportional to their stored energy. Therefore, the size of inductors and capacitors can be estimated and compared by obtaining the maximum conducting currents of the inductors and maximum voltages across the capacitors. In terms of inductor size, the proposed structure's inductor size is equivalent to current-fed full-bridge configurations, smaller than flyback topologies, and larger than L-L-type structures under similar conditions.

Moreover, in this proposed converter (for both resonant and non-resonant approach), the overall capacitor size is minimal compared to alternative configurations. However, it's worth noting that, in the proposed converter, although the inductor size is smaller than that of Flyback converters, it includes a high-frequency transformer that increases its size in comparison to Flyback structures. The size of high-frequency transformers in all other compared configurations with the proposed structure is the same.

The total voltage stress on the primary side switches is determined by considering the peak voltage overshoot values denoted as $K_r = 1 \sim 2$ in Table II for each type of converter. This voltage overshoot, which is shown in Fig. 1 and explained in the introduction, arises due to the difference in current between the transformer's leakage inductance and the input inductor. In the proposed converter, an active clamp circuit is employed to limit this overshoot, reducing it to a minimum value of 1, whereas it remains higher in other configurations except the converter in [5] and active clamped Flyback. In a conventional flyback converter without any snubber circuit, this overshoot typically ranges from 1.5 to 2 [29]. The use of RC or RCD snubber circuits in the ideal Flyback structure can reduce it to approximately 1.2 to 1.3 [30], and it can be further reduced to 1 in an active-clamped Flyback structure [31]. Consequently, when considering the voltage overshoot values, even though the proposed structure incorporates six power switches on its primary side, the total voltage stress experienced by these switches in the proposed converter with non-resonant approach is the lowest compared to other current-fed isolated structures (excluding the L-L-type Half-Bridge structure in [5]). It should be noted that in the resonant approach of the proposed converter, the voltage stress across the switches is 1.57 times higher compared to its non-resonant counterpart, owing to the resonant voltage of the clamping capacitor as opposed to the constant voltage in the non-resonant approach. Consequently, the total voltage stress on the switches in the resonant approach is 1.57 times greater than in the non-resonant approach.

In terms of switching power losses, the proposed structure utilizing a resonant approach stands out for its ability to minimize switching losses, as all switches operate under soft-switching conditions. This advantage holds true even when compared to the full soft-switching current-fed full-bridge converter outlined in reference [11] and converters in [20], [21], [22], [23]. While these converters feature soft switching on the primary side switches, employing ZCS for turn-on and turn-off, it's widely recognized that even with GaN semiconductors, ZCS alone may not suffice at high switching frequencies due to the remained C_{OSS} losses of the switches in ZCS switching, where switching losses tend to dominate over conduction losses. This underscores the importance of ZVS conditions, especially at very high switching frequencies [32]. Consequently, even the proposed converter employing the non-resonant approach exhibits lower

switching losses when compared to the converters proposed in [11], [19], [20], [21], [22], [23], and [30].

To evaluate and contrast the conduction losses in the primary switches of the proposed converter against those in other configurations, a linear relationship is assumed between the on-resistance $R_{DS(ON)}$ of the switches and the voltage stress across them. This on-resistance is presumed to vary proportionally, increases, or decreases linearly as the voltage stress across the MOSFETs is raised or lowered, respectively. Despite comprising six power switches, the proposed structure effectively addresses voltage spike concerns across these switches. This enables the proposed structure with non-resonant approach to opt for power MOSFETs with a lower blocking voltage range (lower $R_{DS(ON)}$), resulting in lower conduction losses when compared to other analyzed structures, except for the L-L-type Half-Bridge structure in [5]. In the case of ideal and active clamped Flyback structures, although they resolve voltage spike issues and feature a significantly lower quantity of power switches, their power switches experience higher conduction losses compared to the proposed structure with non-resonant approach due to the elevated RMS value of the conducting current.

As a result, in the proposed converter employing the non-resonant approach, while it demonstrates better performance in terms of switching losses and volume of passive components compared to most of the compared structures, it does have limitations when it comes to increasing the switching frequency to reduce the volume of passive components for compactness and enhanced power density due to turn-off losses. However, this approach outperforms many of the compared converters, including the proposed converter using the resonant approach, in terms of power switch conduction losses. It's noteworthy that in the resonant approach, due to the possibility of full soft switching, there are no limitations regarding switching losses when increasing the switching frequency to minimize passive component volume, resulting in a more compact converter with increased power density. The performance results of the proposed converter under double switching frequency in Fig. 6 clearly demonstrate the advantage of the converter when doubling the switching frequency.

Moreover, a detailed comparison of our proposed converter, which builds on the findings from our previous conference work [26], is provided in [33]. This comparison examines various isolated high step-up DC-DC converters for low-power applications. The analysis covers key circuit parameters such as voltage conversion ratio, voltage stress on semiconductor elements, component size, and both conduction and switching losses. The selected configurations are also assessed for cost and financial viability. Additionally, the paper outlines the design procedures and experimental prototypes of the solutions, presenting the main results.

VII. EXPERIMENTAL RESULTS

A laboratory scale sample of the converter is implemented and tested to validate the theoretical analysis according to Table III. With these specifications, the experimental results are presented for the two resonant and non-resonant approaches by just changing the clamping capacitor and the switching frequency. Considering the similar behavior of the main and auxiliary switches, this section highlights the current and the voltage waveforms of two main switches, an auxiliary switch, and

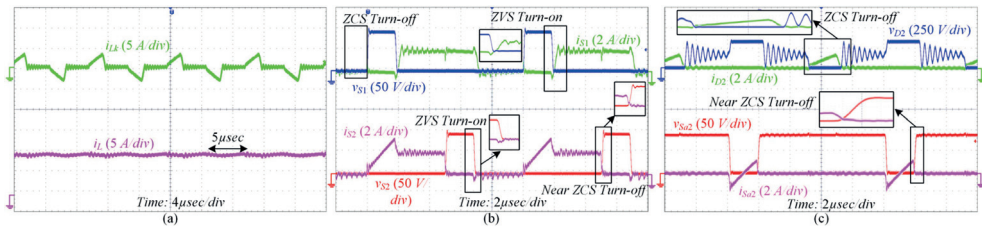


Fig. 10. The experimental results of the proposed converter operating in non-resonant mode at a switching frequency of 100 kHz under V_{in} = 37 V and d = 0.6, (a) input current and the leakage inductance of the transformer current, (b) Current and voltage waveforms of switches S_1 and S_2 , (c) Current and voltage waveforms of switch S_{a2} and diode D_2 .

TABLE III
CHARACTERISTICS OF THE PROPOSED CONVERTER AND COMPONENTS

Components characteristics		
Input inductor L		180 μH
Transformer leakage inductance (L_{lk})		1.8 μH
Turn's ratio of transformer (N)		2
Transformer and inductor cores		ETD54/28/19
Core Material		N97
Number of turns (Primary) N_p		12
Number of turns (Secondary) N_s		24
Capacitor C_c	Non-resonant	10 μF / 250 V
	Resonant	15 nF / 600 V
Capacitor C_1, C_2		3.3 μF / 600 V
Switches $S_{11} \dots, S_4, S_{a1}$ and S_{a2}		IPB048N15N5LFATMA1
Diodes D_{11}, D_2		C6D08065G
Operating point		
Input voltage range (V_{in})		20–50 V
Output voltage (V_{out})		360 V
Maximum rated power (P_{out})		400 W
Maximum Input Current (I_{in})		10 A
Switching frequency (f_s)	Non-resonant	100 kHz
	Resonant	100-280 kHz

an output diode in various operational conditions to avoid excessive figures.

The experimental waveforms of the proposed converter with non-resonant operation under 100 kHz switching frequency, and 400 W output power are shown in Fig. 10. Fig. 10 shows the experimental results for input voltage V_{in} = 37 V and output voltage V_{out} = 360 V, which causes the overlapping interval of the gate signals to be d = 0.6. In this condition, based on Fig. 10(a), the input current (i_{in}) is a continuous current with an average value of 11 A. The peak-to-peak ripple amount of the input current is nearly 0.6 A and the current ripple percent is almost 5.4%, which proves the validity of design consideration for the input inductor (L). Hence, it is clear that the effective frequency on the input inductor is twice the switching frequency (200 kHz), thereby prolonging the power source's lifespan with making very low input current ripple. The voltage and current waveforms of switches S_1 and S_2 are shown in Fig. 10(b). As shown in this figure, both switches turn on under ZVS condition, switch S_1 turns off under ZCS condition, and switch S_2 turns off by charging the parasitic capacitance of the utilized MOSFETs, which helps mitigate switching losses when the switch is turned off, as explained in Section II. Moreover, the voltage stress of these switches is about 90 V, which proves the correctness of the obtained (8). As seen in Fig. 10(c), switch S_{a2} turns on under ZVS condition. Also, based on this figure, it is evident that the switch (S_{a2}) is turned off by charging its parasitic capacitance condition. Additionally, diode D_2 turns off under the ZCS condition, which has been shown in Fig. 10(c). Furthermore, the

maximum voltage on S_{a2} and D_2 is about 90 V and 358 V, respectively that shows the correctness of theoretical results.

The experimental waveforms of the proposed converter operating in resonant mode at a switching frequency of 200 kHz and an output power of 360 W are depicted in Fig. 9. The figure illustrates the experimental results for an input voltage of 30 V and an output voltage of 260 V, with an overlapping interval of 0.6. Based on the data presented in Fig. 11(a), the input current exhibits a continuous flow with an average value of 12 A. The peak-to-peak ripple in the input current is approximately 0.25 A, translating to a current ripple percentage close to 2%, aligning with theoretical predictions. Consequently, it is evident that the effective frequency on the input inductor is twice the switching frequency (400 kHz), allowing for the selection of a lower-value inductor. Moreover, the voltage across the clamping capacitor oscillates between 1.57 times V_{Cc} (which is calculated by (4)) and zero.

The sinusoidal enhancing voltage across the clamp capacitor C_c makes the turn-off of primary switches under near-ZVS conditions. In Fig. 11(b), the voltage, and current waveforms of switches S_1 and S_2 are displayed, illustrating their turn-on under ZVS conditions, turn-off of S_1 under ZCS or near-ZVS conditions, and turn-off of S_2 under near-ZVS conditions due to the sinusoidal voltage increase. The voltage stress on these switches is approximately 120 V, consistent with theoretical expectations. In Fig. 11(c), switch S_{a2} is observed to turn on under ZVS conditions and turn off under near-ZVS conditions, while diode D_2 operates under ZCS conditions. Furthermore, the maximum voltages observed on S_{a2} and D_2 are approximately 120 V and 260 V, respectively, validating the theoretical predictions.

To demonstrate the soft-switching performance of the converter, Fig. 11 presents the voltage and current waveforms of the main switches, S_1 and S_2 , under two conditions: 20% of full load (80 W) for non-resonant operation and 10% of full load (40 W) for resonant operation. In Fig. 12(a), for the non-resonant approach, both switches turn on with ZVS. Switch S_1 turns off with ZCS, while switch S_2 turns off by charging the parasitic capacitance of the MOSFETs, which helps reduce switching losses. This confirms that the leakage inductance design, as described in (18), supports effective soft switching performance at 20% full load. Fig. 12(b) shows the waveforms for the resonant approach, where both switches turn on under ZVS conditions. Switch S_1 turns off under ZCS or near-ZVS conditions, while switch S_2 turns off under near-ZVS conditions due to the sinusoidal increase in voltage. This figure demonstrates that the converter achieves full soft switching performance even under very low load conditions (10% of full load).

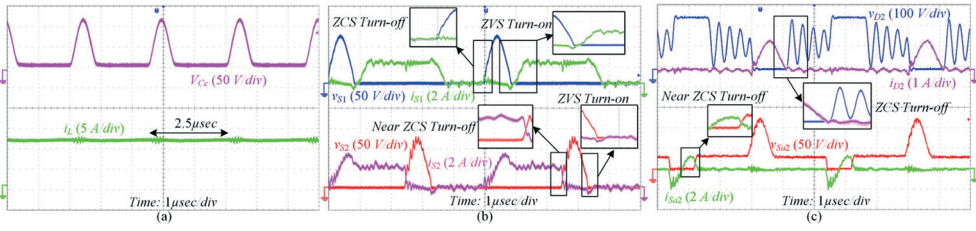


Fig. 11. The experimental results of the proposed converter operating in resonant mode at a switching frequency of 200 kHz under $V_{in} = 30$ V and $d = 0.6$, (a) input current and the voltage across the clamping capacitor V_{C_c} , (b) Current and voltage waveforms of switches S_1 and S_2 , (c) Current and voltage waveforms of switch S_{2a} and diode D_2 .

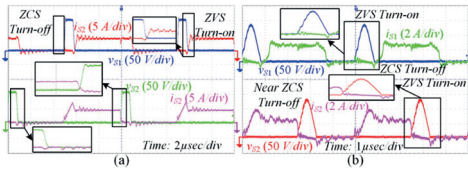


Fig. 12. Experimental results of the proposed converter operating in non-resonant and resonant modes under low load conditions: (a) Current and voltage waveforms of switches S_1 and S_2 operating in non-resonant mode with $V_{in} = 20$ V, $d = 0.8$, and 20% of full load (80 W); (b) Current and voltage waveforms of switches S_1 and S_2 operating in resonant mode under 10% of full load (40 W) condition.

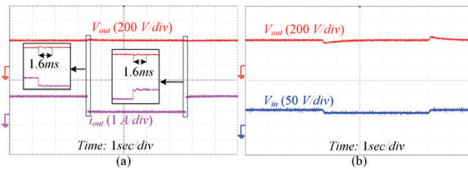


Fig. 13. Transient response of the proposed configuration in non-resonance approach: (a) load step alteration (full load to 20% load), and (b) input voltage step variation (50 V to 40 V).

The transient response of the proposed converter under load and input voltage step changes in the non-resonant approach is depicted in Fig. 12. In Fig. 13(a), the transient response illustrates how the converter reacts to load step changes from 20% to 100% and vice versa. As shown, the converter effectively adjusts to the load step changes and stabilizes the output voltage at 360 V within 1.6 milliseconds after the load change.

Fig. 13(b) presents the transient response of the converter to input voltage step changes from 40 V to 50 V and vice versa. It is evident from the figure that the converter responds appropriately to the input voltage step changes, stabilizing the output voltage at 360 V within 500 milliseconds, with approximately 10% overshoot during a 20% input voltage step change.

The converter's efficiency curve for resonant and non-resonant approach for varying output power, adjusted with input voltages from 40 V to 50 V, is shown in Fig. 14(a). Utilizing the YOKOGAWA WT1800 precision power analyzer, the efficiency estimation was conducted. Regarding this figure, an efficiency of 96.2% for the non-resonant approach and 96.28% for the resonant approach can be achieved at a 400 W output power for the proposed converter. The power losses curve of each component for the non-resonant and resonant approaches at 400

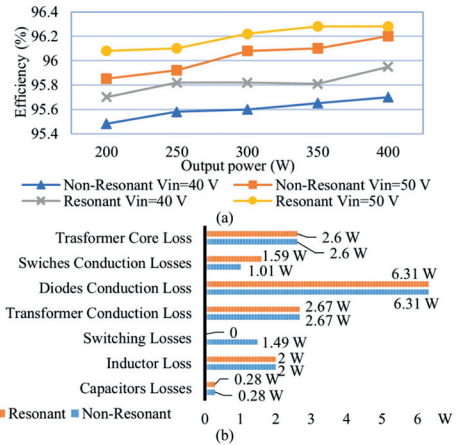


Fig. 14. (a) Efficiency curve for resonant and non-resonant approaches versus varying output power, (b) Total losses breakdown of the components for both non-resonant and resonant operations under a 40 V input voltage and 400 W output power is presented.

W output power level are depicted in Fig. 14(b). This figure clearly indicates that the major sources of loss in the converter are the diodes conduction losses and the conduction and core losses of the transformer and input inductor. These losses are mainly influenced by material engineering. Optimizing magnetic cores for high switching frequencies (100-280 kHz) and selecting diodes with lower forward voltage drops can reduce these losses. Achieving over 95.5% efficiency across the entire 100 W to 400 W power range under all operating conditions at these frequencies is sufficient for this application. However, further improvements in efficiency could be achieved with advancements in ferrite core materials.

VIII. CONCLUSION

This paper presents a current-fed isolated, high step-up dc-dc converter designed to minimize voltage stress on the power switches. Utilizing a HF transformer, the proposed configuration achieves effective isolation between input and output. By exploiting the leakage inductance of the transformer, ZVS during power switch turn-on is achieved, effectively eliminating turn-on and C_{OSS} losses of the primary switches. Additionally, ZCS for power diodes is enabled, eliminating reverse recovery losses

across a broad operational range. This structure can accommodate two types of resonant and non-resonant soft-switching approaches. Although the non-resonant approach or the PSM modulation does not entirely solve turn-off losses of the primary switches, it significantly reduces voltage stresses across the switches, making it advantageous in terms of conduction losses compared to previously established state-of-the-art structures or the resonant approach. However, the PFM combined with PSM modulation or resonant provides full soft switching operation, facilitating the use of GaN transistors to increase switching frequency, reduce passive component volume, and enhance power density. Both approaches result in the input inductor experiencing an effective frequency twice that of the power switches' switching frequency, halving the required size of the input inductor. Furthermore, the auxiliary circuit effectively mitigates voltage spikes across the switches arising from the current difference between the input inductor and the transformer's leakage inductance. Theoretical analysis, along with comparisons with other converters, highlights the performance of the proposed converter. Experimental validation demonstrates its ability to handle input voltages ranging from 20–50 V, operating at a constant/variable switching frequency of 100–280 kHz, yielding an output voltage of 360 V and a maximum output power of 400 W.

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Paper IV

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Comprehensive Comparison of Isolated High Step-up DC-DC Converters for Low Power Application

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ABSTRACT In this paper comprehensive evaluations of isolated high step-up dc-dc topologies have been investigated. These converters are especially well suited for distributed generation systems utilizing renewable or alternative energy sources that need a wide input voltage range with load regulation. With this in mind, this work primarily concentrates on comparative analysis of various isolated configurations employed in possible industry applications. Consequently, several isolated structures, including flyback, forward, push-pull, and full bridge and other similar solutions have been carried out in the literature. For the purpose of comparative and theoretical analysis, some of the circuit parameters are considered, which include voltage conversion ratio, semiconductor element voltage stress, component size, and conduction and switching losses. Furthermore, the selected configurations have been discussed in terms of cost estimation and financial feasibility. In addition, the design procedure and experimental prototypes of the available solutions with the main results are presented. Derived from this investigation, the authors provide a guide to help researchers to identify different isolated topologies with wide input voltage range and galvanic isolation for prospective research directions within this area.

INDEX TERMS Isolated high step-up converter, distributed generation systems, wide input voltage range.

I. INTRODUCTION

Environmental concerns, including issues like global warming, the limited availability of fossil fuels, and the need to decrease carbon dioxide emissions, have motivated the research for cleaner and more sustainable energy sources [1]. Simultaneously, there has been a growing demand for renewable energy systems such as solar panels, fuel cells, and wind turbines in recent years. This increased demand for cleaner energy options has led to a shift in thinking about operating grid-connected systems, necessitating the development of innovative strategies [2], [3]. In essence, the challenges posed by environmental issues and the push for renewable energy are reshaping the energy landscape and how power is generated and distributed [4], [5].

In recent times, microgrids have gained considerable attention due to the substantial benefits they offer to both electricity consumers and power grid operators. Microgrid deployments are seen as a means to enhance power quality, lower emissions, ease network congestion, reduce power losses, improve energy efficiency, and potentially enhance the overall economic performance of the system [6]. Furthermore, over the past decade, dc microgrids have garnered significant interest from both academia and industry. These dc microgrids have proven to be superior to ac microgrids in terms of reliability, efficiency, ease of control, integration of renewable energy sources, and connecting dc loads [7]. The architecture of a simple dc microgrid with a various power conversion section is depicted in Fig. 1.

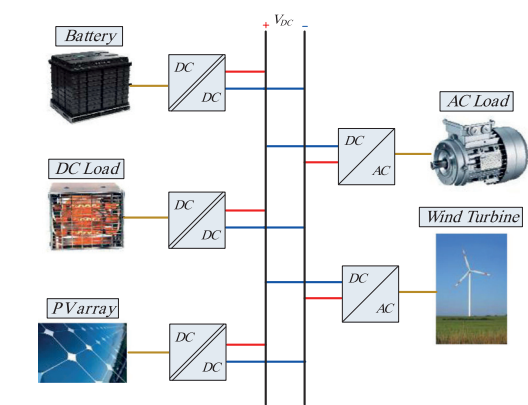


FIGURE 1. A simple architecture of DC Microgrid.

The primary challenge in implementing a dc grid is the lack of a viable business model. Hence, the power electronic converters need to be versatile and compatible with both dc and ac applications [8], [9]. Power electronic structures play a crucial role in incorporating renewable energy generation into the power grid, meanwhile their usage is widespread and expanding rapidly [10].

Solar Photovoltaic (PV) energy is a highly significant global energy source and is projected to be the leading contributor to electricity generation among all renewable options by 2040. This is due to its renewable nature, absence of harmful emissions, and high efficiency. PV power plants are an effective means of harnessing energy from the sun and directly converting it into electricity [11] and [12]. However, PV panels produce very low voltage, and for applications requiring high voltage, these panels must be connected in series and parallel configurations. Unfortunately, this approach increases the overall cost of PV power systems. To address the issue of low voltage output from PV panels, a high step-up dc-dc converter is needed to boost the low voltages (typically 20–30 V) to align with the voltage level for distribution of a dc microgrid (usually 350–400 V) [13], [14].

Lately, there have been numerous advancements in high step-up dc-dc converters designed to achieve high voltage gains in both isolated and non-isolated configurations [15], [16]. In non-isolated setups, where galvanic isolation is not present, various methods have been employed to enhance the dc-dc conversion process. These methods include using coupled inductors, cascading techniques, switched capacitors, switched inductors, and voltage multiplier cells [17]. They are used to achieve a substantial voltage boost in a cascade setup without the need for a transformer, all while maintaining high efficiency and high-power density [18]. To link energy sources with lower input voltages to a higher-voltage dc bus, galvanically isolated dc-dc converters are among the most promising solutions.

These converters provide isolation to shield the energy source from significant voltage fluctuations at the load. They

TABLE 1. Main Features Comparison of VF, CI and IS Converters

Feature	VF	CF	IS
Voltage step-up	No	Yes	Yes
Voltage step-down	Yes	No	Yes
Short-circuit exemption	No	Yes	Yes
Open-circuit exemption	Yes	No	Yes
Element for storing energy	One capacitor	One inductor	At a minimum, one capacitor and one inductor.
Cascading capability of energy elements	No	No	Yes
Simplicity in control	Simple	Complex	Moderate

are efficient in utilizing the energy source, offer more flexibility in handling varying load conditions, and are capable of working with a wider range of input voltages [19], [20], [21], [22], [23]. Various established isolated dc-dc converters can be broadly categorized as Voltage-Fed (VF) and Current-Fed (CF) converters. Current-fed converters primarily function by reducing the input voltage through the adjustment of switch duty cycles [24], [25]. They typically incorporate an output LC filter, which smoothens the pulsating voltage. To operate as boost isolated dc-dc converters, current-fed dc-dc converters offer several advantages, including reduced input current ripple, a lower transformer turns ratio, improved efficiency, lower voltage requirements for rectifier diodes, and the absence of shoot-through faults in power switches [26]. Moreover, there is another isolated converter called Impedance Source (IS) converter, which is a combination of VF and CF converters, and it can have the characteristics of both of them [19], [27], [28], [29]. To better understanding, the specifications of these three types of converters been compared with each other and illustrated in Table 1 [30]. Alternatively, in different scenarios, isolated converters can be classified into three primary types: those based on full or half-bridge switching (BS), single or two-switch PWM, and resonant designs. Full-BS converters offer high voltage step-up ratios and efficiency but are better suited for high-power applications due to their numerous switches [31]. For low-power applications PWM, half-BS, and resonant converters are more practical [32]. In PWM DC-DC converters, standard configurations such as Cuk, SEPIC, and Zeta, incorporating galvanic isolation, as well as Forward, Flyback, and Push-Pull designs, are simple yet may exhibit certain constraints such as reduced static voltage step-up ratios, high input current ripple, and the need for high-breakdown voltage diodes [33]. Isolated High step-up dc-dc converters also can be divided into two types: passive clamp and active clamp converters.

Passive clamp converters have a simple structure and few switches but suffer from power losses due to hard switching of the main switch [34]. Active clamp converters, based on push-pull, half-bridge, and full-bridge topologies, achieve zero-voltage switching (ZVS) for switch turn-on and eliminate voltage spikes. However, they may not be highly efficient or cost-effective in low-power applications due to increased switch count and complex driving circuits [35].

Resonant bridge isolated high step-up dc-dc converters address issues with soft switching, using parasitic elements for resonance and featuring a simple structure without clamp circuits. However, they may cause a significant dc-offset current in the transformer, increasing its size [36].

This paper presents a comprehensive evaluation of isolated high step-up DC-DC converter topologies for distributed generation systems using renewable energy sources. Unlike existing reviews that focus on individual converter types, this paper conducts a thorough comparative analysis across multiple configurations, including flyback, forward, push-pull, and full-bridge converters. The evaluation considers critical parameters such as capacitor and magnetic sizes, primary side switch voltage stress, semiconductor conduction losses, and switching losses, standardized for a fair comparison under identical conditions of 400 W output power, 20–50 V input voltage range, and 50 kHz switching frequency, maintaining a constant 350 V output voltage. The main contributions of the paper include:

- 1) *Component Sizing Analysis*: Introducing a quantitative approach to compare capacitor and magnetic sizes based on accumulated energy calculations, aiding in optimizing component selection.
- 2) *Voltage Stress and Losses Comparison*: Utilizing normalized parameters like Voltage Stress Ratio (VSR) and Conduction Loss Ratio (CLR) to evaluate primary side switch voltage stress and semiconductor conduction losses.
- 3) *Switching Losses Assessment*: Employing a Switching Loss Ratio (SLR) to assess the efficiency of switching losses management across different converter types.

To validate the comparative methodology, a series of experiments were conducted under controlled laboratory conditions. Representative converters, one using coupled inductors (flyback) and another using a transformer (full-bridge), were selected for direct performance comparison. This setup ensured a fair and equitable comparison of efficiency, losses, thermal characteristics, and cost-effectiveness under similar operating conditions.

By evaluating key performance indicators crucial for real-world applications, such as efficiency under varying loads, detailed losses analysis, thermal behavior, and cost considerations, this paper provides practical insights into the strengths and weaknesses of each converter type. Unlike many theoretical studies, this paper bridges theory with practice by incorporating experimental validation. The classification of converters into coupled inductor-based and transformer-based categories, based on their operational principles, aligns with the distinctions made in the introduction and the main body of the paper. This classification is essential for understanding the different converter types and their applications in renewable energy systems. The paper is structured as follows:

- 1) Section II provides an overview of the competitive solutions.
- 2) Section III delves into the methodology for comparative evaluation and offers guidelines for component design.

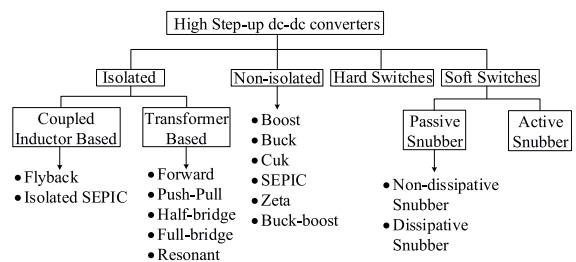


FIGURE 2. Classification of high step-up DC-DC converters.

- 3) Section IV offers experimental evaluation of the proposed solutions.
- 4) Finally, Section V presents the conclusions drawn from this study.

Overall, this paper aims to guide engineers and researchers in selecting optimal DC-DC converter topologies for diverse renewable energy applications, contributing significantly to the field by combining theoretical insights with practical validation.

II. OVERVIEW OF COMPETITIVE SOLUTIONS

The concise summary of the categorization of high step-up DC-DC converters for both isolated and non-isolated types is illustrated in Fig. 2. This paper primarily concentrates on isolated dc-dc converter topologies. Several isolated high step-up dc-dc converters have gained prominence in the industry due to their efficiency, capability, and suitability for applications such as single-phase PV application. The conventional isolated converters, as shown in Fig. 2, include coupled-inductor based converters like Flyback, isolated SEPIC, and transformer-based converters consisting of various topologies such as forward, Push-pull, voltage-fed half-bridge, voltage-fed full-bridge, current-fed half-bridge, current-fed full-bridge, resonant half-bridge, and resonant full-bridge. These converters are widely used based on their inherent characteristics, performance metrics, and suitability for specific applications. Table 2 provides a concise merits and demerits of main features among the conventional isolated high step-up dc-dc converters. In next sub-sections, a set of these solutions has been explained and discussed.

A. COUPLED INDUCTOR BASED ISOLATED SOLUTIONS

The isolated SEPIC, is one of the coupled inductor based isolated converter, commonly used in renewable application, which has advantages like low-input current ripples, minimal EMI, and versatile outputs. These converters possess a fundamental flaw, experiencing notable voltage stress on switch devices that is on par with the combined magnitude of both output and input voltages [37], [38], [39].

Flyback based converter, with its coupled-inductor based isolation, is known for its simplicity and cost-effectiveness. It is suitable for low to moderate power applications [40],

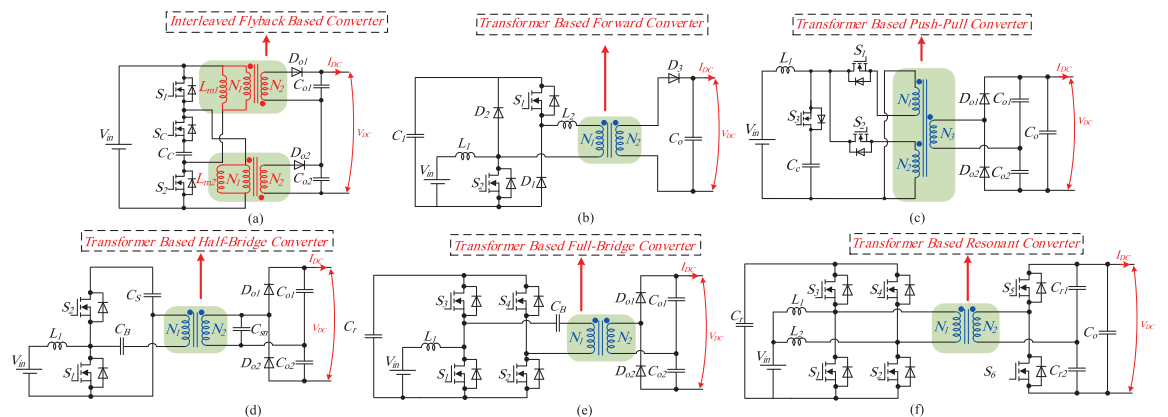


FIGURE 3. Several isolated high step-up DC-DC converters for dc-microgrid applications, (a) Flyback based converter [47], (b) Forward based converter [52], (c) Push-pull based converter [54], (d) Half-bridge based converter [56], (e) Current-fed FB with clamp capacitor [58], and (f) Current-fed resonant converter [67].

TABLE 2. Comparison of Conventional Isolated Converters

Topology	Advantages	Disadvantages
Flyback	• Simple design and low cost. • Suitable for low to moderate power applications	• Limited power handling capability • High peak currents and voltage stresses
Isolated SEPIC	• Dual voltage regulation: step-up and step-down capabilities. • Reduced input current ripple	• Complex control and higher component count • Limited for high power applications.
Forward	• High efficiency • Good for high power applications	• Limited voltage regulation range. • Requires tight control for reliable operation
Push-pull	• High-frequency operation capability • Good for high power applications.	• Complex control and higher component count • Transformer design can be challenging
Half-bridge	• Moderate complexity. • Suitable for a wide range of power applications.	• Requires careful control to avoid voltage spikes • Limited for very low or very high power
Full-bridge	• High efficiency. • Suitable for high-power applications	• Complex control and higher component count • Not ideal for low-power applications.
Resonant	• Reduced electromagnetic interference (EMI) • Improved reliability due to soft switching	• Complex control and higher cost • High current stress through the semiconductor devices

[41], [42], [43], [44], [45]. The conventional flyback converter topology has drawbacks that limit its performance in some applications. Some issues include high voltage spikes and oscillations caused by leakage inductance in the main transformer, reducing efficiency and risking switch and diode damage. Furthermore, the main switch requires a high voltage rating due to the summation of input and reflected output voltages [46]. Fig. 3(a) depicts a two-switch flyback PWM dc–dc converter with active snubber [47]. The proposed converter introduces a dual-flyback high step-up, enhancing voltage gain while minimizing turn ratios. Increasing voltage gain and

reducing switching losses are achieved by coupling two series secondary inductors.

To minimize input current ripple, the two primary sides are interconnected in a parallel configuration.

B. TRANSFORMER BASED ISOLATED SOLUTIONS

The forward converter is one of transformer based isolated solutions that extensively employed in applications requiring low to medium power supplies, primarily owing to its straightforward design and cost-effectiveness. Nonetheless, it possesses two primary disadvantages: When the switch is deactivated, the energy confined in the magnetizing inductance within the core results in transformer saturation, and the transformer’s leakage inductance subjects the switch to substantial voltage stress [48], [49], [50], [51]. Ref. [52] introduces an innovative Active-Clamp Forward Converter (ACFC) incorporating a lossless snubber on the secondary side to mitigate voltage spikes on the free-wheeling diode and forward-rectifier diode. Fig. 3(b) depicts the circuit configuration of the suggested converter.

The Push-Pull based converter is other transformer based isolated solution, which utilized in single phase PV applications. This converter is known for its simplicity and reduced component count, is often chosen for applications where isolation and high step-up ratios are essential. While cost-effective and efficient, it may face challenges in EMI [53]. One push pull based converter with Three Winding Transformer (3WT) has been illustrated in Fig. 3(c) [54]. This configuration’s primary benefit lies in its capacity for achieving a high voltage gain, operating with ZVS, and offering a wide operational range suitable for applications like PV microconverters.

A half-bridge converter finds wide application in motor drives, power supplies, battery chargers, and renewable energy systems. Similar to forward and push-pull converters, it can generate variable output voltages and offer electrical isolation. Despite its more intricate design compared to

forward or push-pull converters, the half-bridge converter delivers greater output power using fewer and cost-effective components [55]. Ref. [56] (Fig. 3(d)) explored an efficient quasi-resonant boost half-bridge dc-dc converter for PV micro-inverters, with a wide input voltage range. The design optimized conversion using a voltage doubler and snubber capacitor, eliminating DC-magnetizing currents in transformers. Employing quasi-resonance in switches and diodes achieved ZVS, minimizing turn-off losses.

The isolated Full-Bridge (FB) converters, which is another transformer based solution, offers improved efficiency and reduced stress on components compared to its half-bridge counterpart. Its full-bridge configuration allows bidirectional power flow, making it suitable for applications demanding higher power density [57]. In [58], which demonstrated in Fig. 3(e), a current fed FB with wide input voltage range has been presented. The voltage spike throughout this converter has been decreased because of using clamp capacitor.

Resonant converters, notably the LLC type, are gaining attention for their outstanding performance [59], [60], [61], [62], [63], [64]. Their benefits and drawbacks vary based on application needs like power density, efficiency, cost, complexity, and reliability [65]. The LLC converter, with low EMI, high power density, and ZVS capability in switches, is particularly favored. In high-step-up PV applications, LLC resonant converters operating at resonant frequencies are preferred for efficient power conversion [66]. Nevertheless, integrating additional components leads to increased magnetic loss, costs, and complexity within these converters. In [67] (Fig. 3(f)), a resonant dc-dc converter was created with the aim of attaining input currents devoid of ripples. Through the maintenance of a consistent duty cycle and the incorporation of a resonant circuit on the secondary side, this converter reduces turn-off currents and minimizes switching losses, ultimately enhancing efficiency.

III. COMPARISON METHODOLOGY OF ISOLATED SOLUTIONS

In this section, a comprehensive comparison of solutions depicted in Fig. 2 is conducted using a methodology that considers key parameters such as follows:

- 1) Capacitor size
- 2) Magnetic size
- 3) Primary side switch voltage stress
- 4) Primary side semiconductor conduction losses
- 5) Switching losses

The design parameter of comparison for all converters has been indicated in Table 3.

Capacitor size impacts energy efficiency, inductor size influences energy transfer, and high frequency transformer dimensions, which are magnetic elements, affect overall system size and efficiency. Analysis of relative conduction and switching losses of semiconductors provides insights into system efficiency and control mechanisms. Additionally, evaluating primary side switch voltage stress informs about component reliability. In a very general case, the fundamental

TABLE 3. Design Parameter of Comparison for All Converters

Parameters	Value
Input voltage range (V_{in})	20 V – 60 V
Output voltage (V_o)	350 V
Maximum rated power (P_o)	400 W
Switching frequency	50 kHz
Maximum input current	10 A
Maximum input current ripple	15 %
Maximum voltage ripple of capacitors	3 %

waveforms of a converter are independent of the selection of components and electric parameters (e.g., switching frequency, selected semiconductors) and result from the basic modulation scheme, yielding some general requirements for the dimensioning of the components [68]. This approach offers a nuanced understanding of the strengths and weaknesses of each solution, aiding engineers and researchers in optimizing these converters for diverse applications. It was applied in some other research works [69], [70].

A. MAGNETIC AND CAPACITORS SIZE COMPARISON

For comparing capacitor and magnetic sizes among the solutions, a methodology relies on calculating the total accumulated energy in these elements. This quantitative approach evaluates their energy storage capacities, providing insights into efficiency. The analysis also considers total conduction power loss, offering a holistic perspective on how effectively each solution manages power flow through these components. Therefore, the following equations has been utilized:

$$\sum_{i=1}^n E_{C_i} = \frac{1}{2} C_i V_{C_i}^2, \quad (1)$$

$$\sum_{j=1}^m E_{L_j} = \frac{1}{2} L_j I_{L_j}^2. \quad (2)$$

In the above equations, E_C , E_L , V_C , I_L , n and m are respectively the accumulated energy in capacitors and inductors, the voltage across the capacitors, the current through the inductors, number of capacitors and number of inductors.

B. PRIMARY SIDE SWITCH VOLTAGE STRESS COMPARISON

To compare the primary side switch voltage stress (V_{stress}) of switches, a normalized parameter called the Voltage Stress Ratio (VSR) can be used as follows:

$$VSR = \frac{V_{stress}}{V_{out}}. \quad (3)$$

This ratio provides a comparative measure that considers the impact of the voltage stress relative to the output voltage. A lower VSR indicates that the primary side switch voltage stress is a smaller proportion of the output voltage, which can be useful for evaluating the stress level on the switch in relation to the desired output voltage.

C. PRIMARY SIDE SEMICONDUCTOR CONDUCTION LOSSES COMPARISON

The primary side semiconductor conduction losses in mentioned converters are compared based on normalized parameter known as the Conduction Loss Ratio (*CLR*). The *CLR* is expressed as the ratio of the conduction losses to the total power:

$$CLR = \frac{P_{Conduction}}{P_{out}}. \quad (4)$$

In (4) P_{out} is the total power of the converter and $P_{conduction}$ represents the total conduction losses in the primary side semiconductor devices that define as follows:

$$P_{conduction} = \sum_{i=1}^N R_{on} I_{RMSi}^2. \quad (5)$$

I_{RMS} is the Root Mean Square (RMS) current flowing through the semiconductor device during conduction, and R_{on} is the ON-state resistance of the semiconductor device.

D. SWITCHING LOSSES COMPARISON

The switching loss ratio (*SLR*) is defined as the ratio of the switching losses to the total power for this comparison as follows:

$$SLR = \frac{P_{switching}}{P_{out}}. \quad (6)$$

The switching losses ($P_{switching}$) occur during both turn-on and turn-off events are influenced by semiconductor parameters such as the switching frequency, device capacitances that we assume to be similar to all compared solutions, while the voltage and current waveforms during switching are define by the selected topology and are expressed as follows:

$$SL \cong \sum_{i=1}^{N_s} \left[\hat{i}_{Si} \cdot \hat{v}_{Si} \right]_T. \quad (7)$$

In (7), the average of the product v_{Si} and i_{Si} throughout a fundamental period T serves as an appropriate indicator for assessing switching losses. Besides, *SLR* provides a comparative measure for evaluating how efficiently the converter handles switching losses relative to the total power. Based on the mentioned specification for methodology of comparison, the converters presented in Fig. 3 from each family of isolated converter has been compared with each other that is indicated in Fig. 4.

The comparison performance of each converter separately has been illustrated in Fig. 5. It is essential to emphasize that this comparative analysis is specifically implemented with an output power set at 400 W. The input voltage ranges between 20 V and 50 V, with a consistent switching frequency of 50 kHz, while the output voltage is maintained at a constant 350 V. To ensure a comprehensive and fair comparison, not only is the output power standardized, but the duty cycle and other dynamic switch configurations are also kept consistent

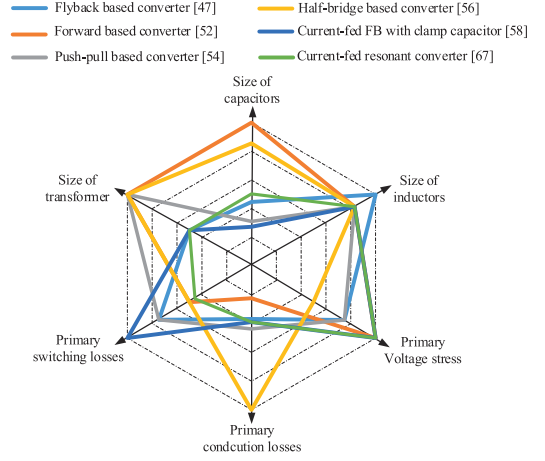


FIGURE 4. Overall comparison of the isolated converters from each family based on key parameters.

across all converters. It's worth noting that isolated high-step-up converters typically incorporate a voltage multiplier rectifier on their secondary side, a common feature among most isolated converters.

As a result, specifications related to the secondary side, such as the voltage stress of diodes and conduction losses, have been omitted from this comparison. This intentional exclusion allows us to focus specifically on the primary aspects influencing performance, providing a standardized basis for evaluating the efficiency and effectiveness of the converters. This meticulous approach ensures that the comparison is not only fair but also comprehensive, enabling a detailed examination of the converters' performance under consistent conditions.

In general isolated converters have been extensively employed across different power levels, frequently as adaptations of non-isolated converters [71] and [72]. As previously noted, DC-DC converters featuring galvanic isolation can be classified based on the energy transmission element as either transformers or coupled inductors [26]. Even though both transformers and coupled inductors share the commonality of having multiple windings on a magnetic core, their operational principles and roles in switching converters exhibit significant variations [73]. Transformers are the favored option for achieving galvanic isolation due to their noteworthy power density, making them a popular choice for high-power applications. Conversely, converters based on coupled inductors present a more efficient solution characterized by a smaller size and weight. Moreover, they find common use in applications with lower power requirements [74].

IV. EXPERIMENTAL EXAMPLE OF ISOLATED DC-DC CONVERTERS

To validate the comparison methodology, a series of experiments with various configurations was conducted in the

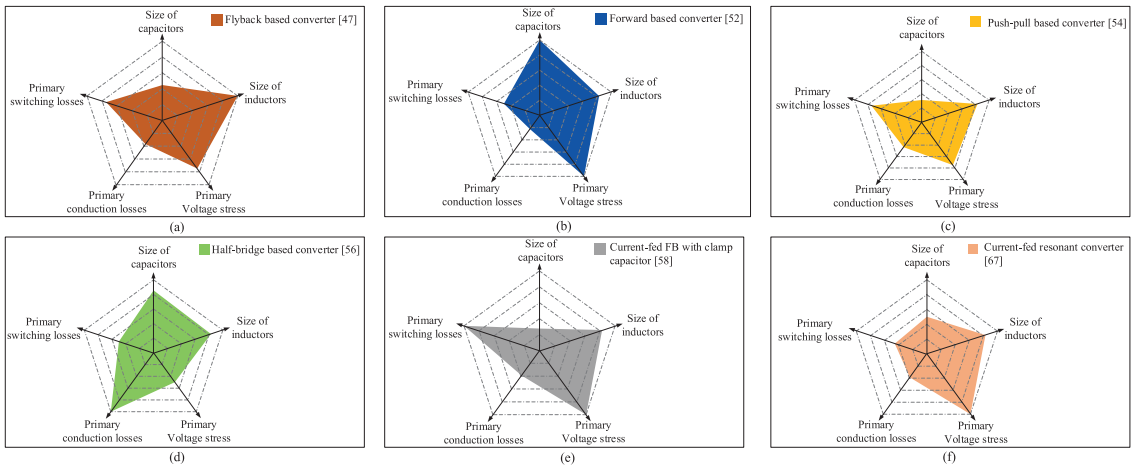


FIGURE 5. Performance Comparison of the isolated converters, (a) Flyback based converter [47], (b) Forward based converter [52], (c) Push-pull based converter [54], (d) Half-bridge based converter [56], (e) Current-fed FB with clamp capacitor [58], and (f) Current-fed resonant converter [67].

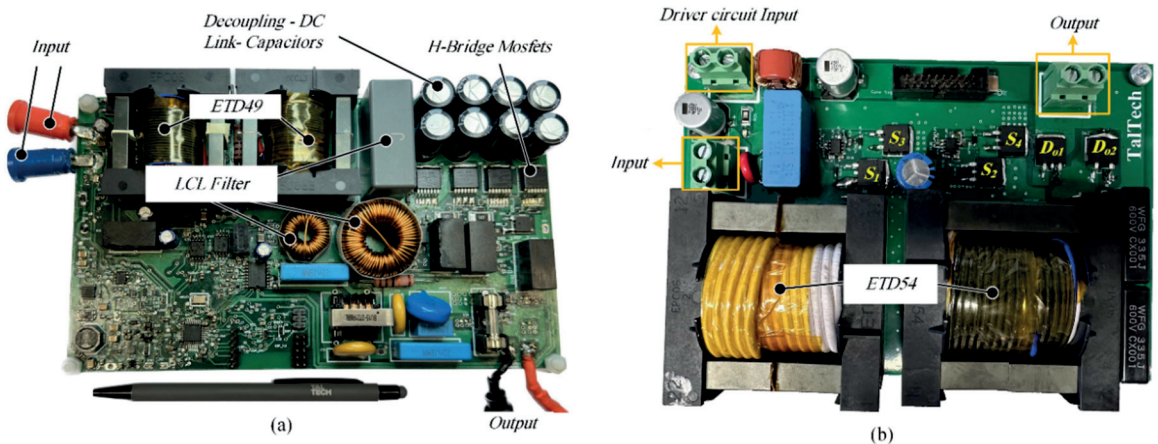


FIGURE 6. The experimental prototype of the isolated converters, (a) Flyback based converter, (b) FB based converter.

laboratory. In this specific comparison, the flyback converter was chosen from the family of isolated converters due to its reliance on the coupling inductor. Similarly, the full-bridge converter, selected from the same family of isolated converters, was chosen based on its use of a transformer. Moreover, Fig. 6 illustrates the experimental prototypes of each converter.

It's crucial to emphasize that the flyback converter showcased in this study was meticulously designed for PV microinverter applications and includes additional components because of its performance [45]. However, for a fair and focused comparison, only the DC portion of the flyback converter was considered. This deliberate choice enables a comprehensive and equitable evaluation of the essential

aspects pertinent to the comparison. The parameter specifications for both converters are provided in Table 4. Both converters underwent testing with an input voltage range of 20–60 V and a power rating of 400 W. The experimental waveforms for both the flyback-based high step-up converter and the full-bridge (FB) based converter are presented in Fig. 6. It is crucial to note that these waveforms were obtained with an input voltage fixed at 40 V and a constant output voltage of 350 V. In Fig. 7(a), the waveforms for input voltage (V_{in}), output voltage (V_{out}), and input current of the FB-based converter are displayed. Notably, the input current ripple content is approximately 20 %, indicating an acceptable level for this type of converter. Fig. 7(b) depicts the voltage and current waveforms of the main switches of the FB-based

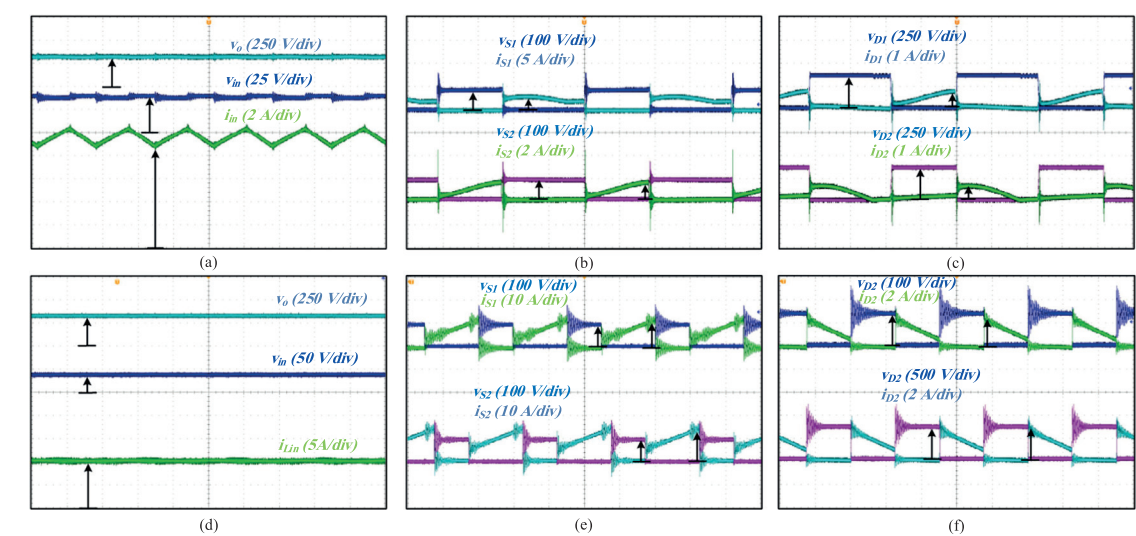


FIGURE 7. Experimental measurement of the isolated dc-dc converters, (a) Input voltage (V_{in}), output voltage (V_{out}) and input current of FB based converter, (i_{in}) waveforms, (b) current and voltage waveforms of switches S_1 and S_2 of FB based converter, (c) current and voltage waveforms of diode D_1 and D_2 of FB based converter, (d) Input voltage (V_{in}), output voltage (V_{out}) and input current (i_{in}) of flyback based converter, (e) current and voltage waveforms of switches S_1 and S_2 of flyback based converter, (f) current and voltage waveforms diodes D_1 and D_2 of flyback based converter.

TABLE 4. Specification of the Isolated Converters

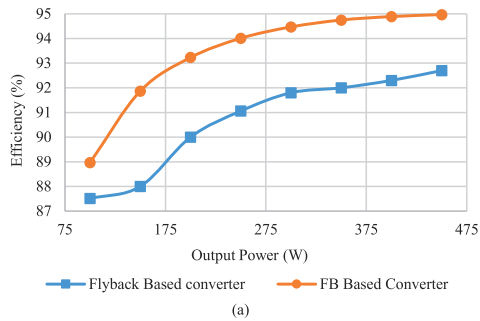
Parameters	Value/Type	
	Flyback based	FB based
Transformer core	ETD49	ETD54
Input inductor	-	220 μ H
Magnetic inductance	60 μ H	870 μ H
Leakage inductance	450 nH	1.7 μ H
Decoupling capacitor	$8 \times 22 \mu$ F	-
Capacitors C_b, C_r	-	22 μ F, 10 μ F
Semiconductor elements		
Switches S_1, S_2	-	IPB048N15N5LFATMA1
Diodes D_{o1}, D_{o2}	IDM05G120C5XTMA1	C6D08065G
Flyback switches	IPB044N15N5ATMA1	IPB044N15N5ATMA1
Operating point		
Input voltage range (V_{in})	20 V – 60 V	20 V – 60 V
Output voltage (V_o)	350 V	350 V
Maximum rated power (P_o)	400 W	400 W
Switching frequency	60 kHz	60 kHz

converter. From this figure, it is observed that the voltage stress on the two main switches is around 90 V, which is four times smaller than the output voltage. Moving to Fig. 7(c), the voltage and current waveforms of the voltage multiplier rectifier diodes (D_1 and D_2) are illustrated. The voltage stress on the output diode matches the output voltage, a typical characteristic in converters of this kind. Switching our attention to the isolated flyback converter, Fig. 7(d) showcases the input voltage, output voltage, and magnetizing current waveforms. A comparison with the FB-based converter reveals that the input current ripple of the flyback-based converter is generally higher. In Fig. 7(e), the voltage and current of switches S_1

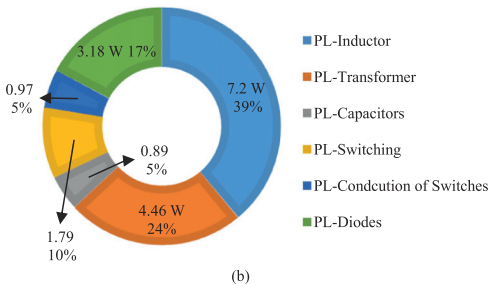
and S_2 are presented, indicating a maximum switch voltage of around 120 V. In terms of voltage stress evaluation, although each switch’s voltage stress in the FB-based converter is lower than that of the flyback-based converter, the total voltage stress in the FB-based converter is higher when compared to the flyback-based converter. Finally, Fig. 7(f) exhibits the voltage and current waveforms of the output diodes, revealing that their voltage stress is twice as high as the output voltage. While this may suggest high stress on the output diodes, it is noteworthy that there are also flyback-based converters mentioned in previous studies [45], where the output diode voltage stress aligns with the output voltage. In summary, the waveforms analysis indicates distinct performance characteristics between the flyback-based high step-up converter and the FB-based converter. The FB-based converter demonstrates lower voltage stress on individual switches but higher total voltage stress. The output diodes in the FB-based converter exhibit higher stress, yet it’s important to recognize that similar stress levels have been reported in certain flyback-based converters according to prior studies [45]. Choosing between the two converters depends on the specific application requirements and observed waveform characteristics

In order to provide a thorough comparison between coupled inductor-based and transformer-based structures, various key performance aspects have been analyzed and presented in Fig. 8(a)–(e) for both converters. These figures offer insights into the efficiency curve, losses breakdown of the power circuit, and thermal characteristics of the main switches for both FB based and flyback based converters.

In Fig. 8(a), the efficiency curve shows the performance of the proposed converters across a range of output power



Power Losses Breakdown of FB Based Converter



Power Losses Breakdown of Flyback Based Converter

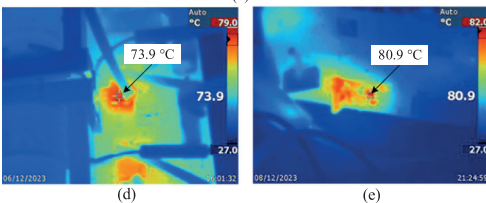
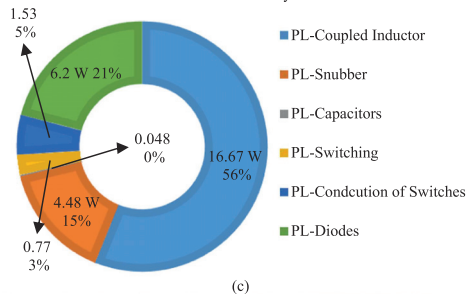


FIGURE 8. Efficiency, power loss curve and thermal image flyback based and FB based converters, (a) Efficiency curve versus output power, (b) Total losses breakdown of the components in FB based converter, (c) Total losses breakdown of the components in flyback based converter, (d) Thermal image of the main switch in FB based converter, (e) Thermal image of the main switch in flyback based converter.

levels, differing from light load to full load conditions. It is evident from this figure that the FB based converter exhibits a notably higher efficiency when compared to the flyback based converter. Fig. 8(b) and (c) present a detailed breakdown of losses within the power circuit for both converter types. The analysis reveals that the predominant source of losses in both converters is attributed to magnetic elements.

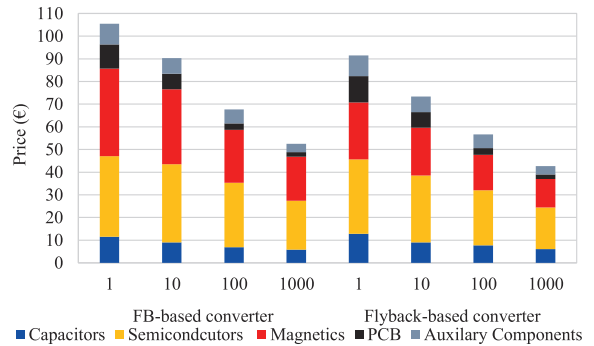


FIGURE 9. The cost graph of the image flyback based and FB based converters for different numbers of assemblies.

This commonality underscores the intrinsic nature of losses associated with these components. Notably, the Flyback converter introduces additional losses in the form of snubber circuit losses, which are conspicuously significant.

This observation raises considerations for optimizing the snubber circuit design to mitigate its impact on overall efficiency. Furthermore, the temperature curves of the main switches for each converter, as depicted in Fig. 8(d) and (e), highlight the thermal characteristics under the specified operating conditions. Based on this Figs, both converters demonstrate satisfactory thermal performance in this scenario, indicating that neither converter is adversely affected by excessive heating issues. In Fig. 9, the cost comparison between full-bridge and flyback converters reveals an interesting insight. Despite the full-bridge converter showing higher efficiency, the overall cost of the flyback converter is significantly lower. In essence, while efficiency is undoubtedly a critical factor in converter selection, the general consideration of cost-effectiveness, proves the practical appeal and widespread utilization of flyback-based converters across various industrial sectors.

This cost advantage is a key reason why flyback converters are commonly preferred in various industrial applications. The simplicity of the flyback topology, requiring fewer components and offering straightforward implementation, contributes to its cost-effectiveness. This economic advantage makes flyback converters a widely adopted and practical solution in the industry for low power applications

A comprehensive evaluation has been conducted to compare the flyback-based converter [45] with the FB-based converter across various crucial parameters such as total voltage stress on primary switches, component count, volume, size, power density, full load efficiency, and cost. The detailed findings are summarized in Table 4, providing an insightful overview of the performance characteristics of the two converters. Fig. 10 further elucidates the comparison by presenting the specifications of the Flyback-based and FB-based prototypes. Upon careful examination of both the Table 5 and the graphical representation in Fig. 10, it becomes evident

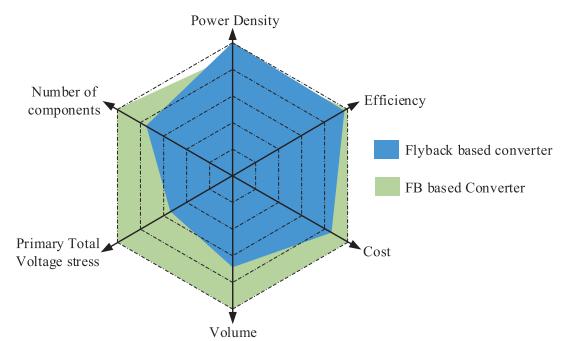


FIGURE 10. The specification of the comparison between the Flyback based and FB based prototypes.

TABLE 5. Specification of the Two Converter Comparison

Topologies	Flyback based converter	FB Based Converter
Power Density	1.97 kw/dm ³	1.78 kw/dm ³
Efficiency	92.3 %	94.89 %
Cost	91 €	105 €
Volume	188*111*28 mm ³	165*111*46 mm ³
Total Voltage stress of primary side	197 V	360 V
Number of main components	9	12

that the flyback-based converter exhibits superiority in several aspects when compared to the FB-based converter. Despite the high efficiency of the FB-based converter, it is noteworthy that it incurs elevated costs and experiences increased total voltage stress across the switches, unlike the flyback-based counterpart. Notably, the flyback-based converter demonstrates a favorable combination of high power density and a reduced number of components, contributing to an overall cost reduction in the converter assembly.

In a comparative analysis between the flyback based converter and the FB based converter, it is initially observed that the flyback converter imposes a higher voltage stress on a switch than the FB counterpart. However, considering the number of switches, the overall voltage stress of the full-bridge converter surpasses that of the flyback converter. Additionally, alternative flyback converters, such as the one presented in [47], demonstrate parity in voltage stress with the full-bridge converter for individual switches.

Based on comprehensive theoretical analysis and the practical results showcased for converters within the transformer and coupled inductor family, it is evident that several key parameters must be considered for the effective deployment of these converters in industrial applications. These crucial parameters include, but are not limited to, the number of elements, efficiency, and notably the cost. In the realm of industrial applications, the selection of an appropriate converter structure demands a precise evaluation, taking into account the complicated balance between these fundamental criteria. Efficiency, cost-effectiveness, and the specific requirements

of the intended application all play fundamental roles in determining the optimal choice. This consideration is superior in achieving not only optimal performance but also cost-efficient and sustainable solutions for different industrial applications.

V. CONCLUSION

This paper presented a comprehensive evaluation of isolated high step-up dc-dc converters, emphasizing their applicability in distributed generation systems powered by renewable energy sources. The overview of competitive solutions highlights the importance of power electronic structures in incorporating renewable energy into the power grid, emphasizing their widespread and rapidly expanding usage. Through a comparative analysis, key parameters such as voltage conversion ratio, semiconductor element voltage stress, component size, and conduction and switching losses are considered. The selected configurations are also assessed in terms of cost estimation and financial feasibility. The investigation aims to guide researchers in identifying suitable isolated topologies with wide input voltage ranges and galvanic isolation for future research directions.

The comparison methodology is provided as systematic approach, considering capacitor and magnetic sizes, primary side switch voltage stress, primary side semiconductor conduction losses, and switching losses. The experimental examples of isolated dc-dc converters, specifically the flyback-based and full-bridge-based converters, validate the methodology and showcase distinct performance characteristics between the two.

The efficiency curve, losses breakdown, thermal characteristics, and cost comparison provide a comprehensive understanding of the trade-offs between the flyback and FB converters. Despite the higher efficiency of the FB converter, the cost-effectiveness of the flyback converter, attributed to its simplicity and fewer components, demonstrates its practical appeal in various industrial applications.

In conclusion, based on the comparative analysis and experimental validation, the paper recommends considering specific application requirements when choosing isolated high step-up dc-dc converters. The findings emphasize the importance of balancing efficiency and cost-effectiveness for practical implementation in distributed generation systems using renewable energy sources.

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Paper V

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Novel Concept of Universal AC/DC-DC Onboard Battery Charger for Electric Vehicles

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Abstract— In this paper, a universal bidirectional ac/dc-dc power electronic converter is introduced to enable power transfer between input and output in both directions. This converter is particularly suited for onboard battery charging systems, offering vehicle-to-grid and grid-to-vehicle functionality. The proposed system serves as a versatile and universal interface for connecting ac or dc grids and facilitating efficient power transfer. The system supports three-phase and single-phase ac, as well as two-wire and three-wire dc sources, without altering input wiring. Enhanced safety is provided through input-output isolation, and the use of active diodes at higher frequencies improves overall efficiency compared to traditional passive diodes. An 11 kW prototype was developed to validate the proposed converter. It operated successfully at up to 800 V battery voltage, with 100 kHz and 700 kHz switching frequencies for the rectifier and dc-dc stages. Proper functionality was demonstrated in both single-phase and three-phase inverter modes under 5 kW testing.

Keywords— ac/dc-dc power converter, grid-to-vehicle (G2V), onboard battery charger, universal bidirectional converter, vehicle-to-grid (V2G).

I. INTRODUCTION

Electric Vehicles (EVs), especially plug-in EVs (PEVs), are quickly becoming a viable alternative to traditional internal combustion engine vehicles due to their numerous advantage. Concurrently, the energy grid is evolving, with a growing focus on direct current (dc) systems. While alternating current (ac) grids have been favored for their voltage modification capabilities, recent studies indicate that dc systems may offer greater efficiency [1]-[3]. However, a complete shift from ac to dc is not imminent, as the existing ac infrastructure is well-established and remains functional. Instead, the future will likely feature a hybrid system where ac and dc coexist, requiring advancements in power electronics to ensure compatibility with both grid types [4]. EV charging systems must consider key factors such as isolation, power density, and the ability to handle various battery voltages [5]-[8]. Power Factor Correction (PFC) rectifiers are crucial for efficient power transfer and energy efficiency. For EV owners, the capability to charge using both ac and dc inputs is vital. Charging solutions should evolve to support both types, allowing vehicles to use standard ac plugs and specialized dc adapters. A universal onboard charger that connects to both

grids would streamline this process, enhancing the transition from ac to dc infrastructure and providing a competitive edge for EVs with this technology. This hybrid approach promotes efficient energy distribution while ensuring convenience for EV users.

II. DESCRIPTION OF THE PROPOSED STRUCTURE

The proposed system, illustrated in Fig. 1, features a universal onboard charger with a bidirectional converter that enables power flow in both directions. It has four input terminals accommodating three-phase ac, single-phase ac, two-wire dc, and three-wire dc. The architecture includes several functional modules: the first is PFC stage, and the second comprises isolated dc-dc converters operating at high switching frequencies. The use of Zero Voltage Switching (ZVS) and GaN transistors allows for very high switching frequencies, resulting in low inductance without the need for a ferrite core [9]-[11]. This approach contrasts with previous methods, as magnetics, particularly ferrite cores, are significant sources of losses and limit switching frequency increases [12]-[14]. The configuration of the dc-dc modules can be either parallel or series, depending on the battery voltage requirements. Parallel connections are suitable for lower battery voltages, whereas series connections are used for higher voltages. Notably, the relationship between the rectifier module and the dc-dc converters remains unaffected by the output-side configuration. The system offers flexibility; for three-phase ac input, the rectifier connects to the converters in series, while for single-phase ac, they are connected in parallel. For dc input, the configuration depends on the voltage level: a parallel arrangement is used for 350-380 V, and a series arrangement for 700-750 V in a two-wire system. In a three-wire dc input, the modules are always in series. This setup is controlled by a system that monitors input terminal voltage and the rectifier's internal design.

The rectifier module employs a T-type topology, implemented using semiconductor switches (S_1 - S_{12}) and filtering inductors (L_A , L_B , L_C) [15]. Among these, S_1 - S_8 function as two-quadrant switches, and S_9 - S_{12} are GaN transistors operate as four-quadrant switches. Additionally, the module incorporates Solid-State Circuit Breakers (SSCB₁ and SSCB₂) and suppression capacitors (C_{SA} , C_{SB} , C_{SC}) to enable efficient dc grid connection and disconnection.

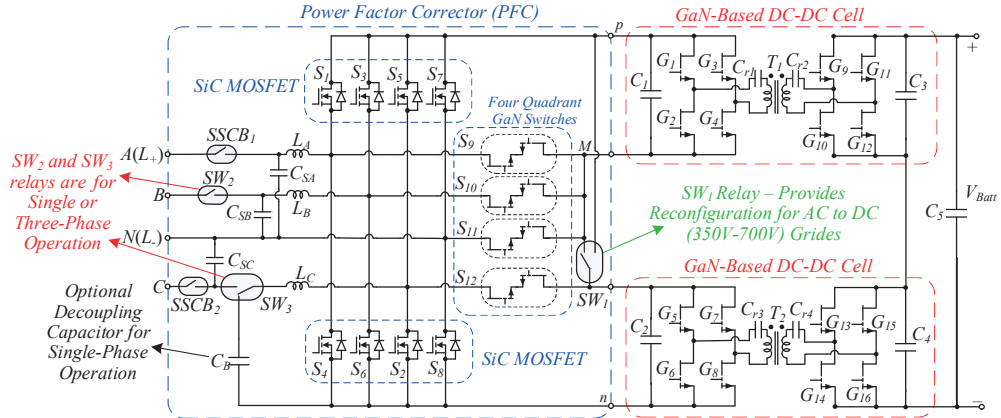


Fig. 1. The proposed universal ac/dc-onboard battery charger for electric vehicles.

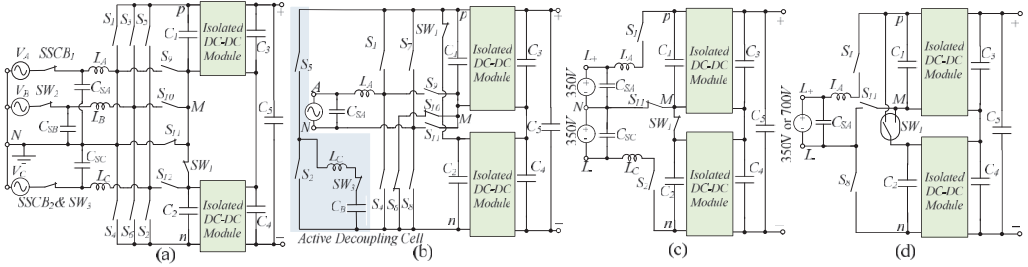


Fig. 2. Equivalent circuits of the universal onboard charger in different configurations: a) Three-phase ac input, b) Single-phase ac input, c) Three-wire dc input, and d) Two-wire dc input (with a parallel configuration for the dc-dc modules for 350-380 V dc input, and a series configuration for the dc-dc modules for 700-750 V dc input).

The structure includes an optional decoupling capacitor, C_B , designed to function as an active decoupling capacitor when the system is connected to a single-phase input. The active power decoupling circuit enables to have high power density and the use of film or ceramic capacitors (long lifetime capacitors rather than electrolytic capacitors) in the single-phase operation of the structure [16]-[18]. The control strategy for this system can include several methods, such as operating in Vienna rectifier mode, where only the four-quadrant switches perform high-frequency switching while the remaining switches operate at line frequency.

A key innovation in this system is the integration of a reconfigurable switches, denoted SW_1 - SW_3 . These switches are Electromechanical Relays (EMR). The series or parallel configuration of the inputs for isolated dc-dc modules is determined by the rectifier module. When the isolated dc-dc modules are connected in series, the positive terminal of capacitor C_2 is linked to the negative terminal of capacitor C_1 via switch SW_1 .

Conversely, if the modules are to be connected in parallel, the positive terminal of capacitor C_2 is connected to the positive terminal of capacitor C_1 through switch SW_1 . Switches SW_2 and SW_3 are used to change the converter's configuration between three-phase ac, single-phase ac, or dc inputs.

III. CONFIGURATIONS OF THE PROPOSED SYSTEM

The equivalent circuits of the universal onboard charger in different configurations are shown in Fig. 2.

A. Three-Phase AC Inputs

For three-phase ac inputs with or without neutral wire (which is shown in Fig. 2(a)), SW_2 is turned on to connect the converter to phase B, while SW_3 isolates the decoupling capacitor from the system and connects the system to phase C. The three phases are connected to their respective input terminals, with the neutral wire optionally connected to one of the input terminals. To regulate the current in each phase, inductor filters L_A , L_B and L_C are employed. Two-quadrant switches S_1 - S_6 operate as auxiliary switches (replacing diodes) in rectifier (grid-to-vehicle) mode, and as main switches in inverter (vehicle-to-grid) mode, handling high-frequency modulation. Four-quadrant switches S_9 - S_{12} (excluding S_{11}) serve as main switches in rectifier mode and as auxiliary switches in inverter mode, also operating under high-frequency modulation. In this configuration, S_{11} connects the neutral (N) to the midpoint (M) of the dc-link capacitors to balance the capacitors voltages.

B. Single-Phase AC Input

Fig. 2(b) illustrates the connection of the single-phase ac grid to the battery charger. In this setup, switches S_6 and S_{10} , operating in static conduction mode, connect the negative terminals of capacitors C_1 and C_2 (i.e., connecting node M to node n), thereby configuring the capacitors in parallel through switch SW_1 to the active decoupling cell. This configuration helps mitigate the power imbalance caused by the pulsating nature of the single-phase ac input. The

decoupling capacitor C_B is integrated into the system through switch SW_3 , while switches S_5 and S_2 operate at high frequency to balance power delivery to the dc-link capacitors (or draw from the dc-link capacitors in vehicle-to-grid mode), utilizing the L_C inductor filter as an active buck converter cell.

Additionally, switches S_1, S_4, S_7, S_8, S_9 , and S_{11} handle high-frequency modulation to perform single-phase ac-dc rectification (grid-to-vehicle) mode or dc-ac inversion in (vehicle-to-grid) mode.

C. Three-wire dc input

Fig. 2(c) depicts the connection of a three-wire dc grid to the battery charger. The universal onboard charger operates correctly with a three-wire dc grid by connecting the wires to terminals L_+, N , and L_- , with the dc-dc modules configured in series through switches SW_1, S_1, S_6 , and S_{11} .

D. Two-wire dc input

Fig. 2(d) illustrates the connection of a two-wire dc grid to the battery charger. In this configuration, switches SW_1 and S_{11} are used to set the dc-dc modules in either a parallel or series arrangement. Switches S_1 and S_8 operate in static conduction mode, connecting the dc-link capacitors to the two-wire dc input (ranging from 350-380 V or 700-750 V). All other switches remain in a static off state.

IV. SYSTEM OPERATION IN FOUR CONFIGURATIONS

A. Three-Phase ac Inputs

Fig. 3 illustrates the PWM (Pulse Width Modulation) gating logic and corresponding conduction states for a single phase-leg of the bidirectional Vienna rectifier. The control method uses three switches S_{x1}, S_{x2} , and S_{x3} to shape the input current i_{Lx} sinusoidally and regulate the dc-link capacitor voltages C_1 and C_2 . In the PWM scheme, the reference signal is compared against triangular carrier signal. This comparison determines the switching states to produce the required voltage levels across the inductor and ultimately shape the input current i_{Lx} sinusoidally (depicted in Figs. 3(a) and 3(d)). The triangular carrier signals serve as high-frequency waveforms (typically several kHz). The reference signal (e.g., a 50/60 Hz sinusoid) is compared against these carriers. Whenever the reference is lower than the carrier, S_{x1} is turned on (depicted in Figs. 3(c) and 3(f)). When the reference is greater than the carrier, S_{x2} is turned on during the positive half-cycle (depicted in Fig. 3(b)), and S_{x3} is turned on during the negative half-cycle in rectifier mode (depicted in Fig. 3(e)). Conversely, in inverter mode, when the reference signal is less than the carrier, S_{x3} is turned on during the positive half-cycle, and S_{x2} is turned on during the negative half-cycle.

In other words, the high-frequency PWM logic operates as follows: when the duty cycle $D=1$, switch S_{x1} remains off, while either S_{x2} or S_{x3} remains on, depending on the current polarity. In this case, V_y is connected directly to the dc-link via the corresponding switch, resulting in the maximum voltage applied to the inductor. Conversely, when the duty cycle $D=0$, switch S_{x1} is turned on, effectively clamping V_y to the midpoint M , which yields the minimum voltage level (0 V relative to the midpoint). As a result, the following equation can be written for V_y :

$$V_y = \begin{cases} D \times V_{C1} & \text{Positive Half Cycle} \\ -D \times V_{C2} & \text{Negative Half Cycle} \end{cases} \quad (1)$$

By appropriately modulating the switching states, the converter synthesizes a three-level voltage waveform, which enables unity power factor operation, sinusoidal current shaping, and balanced dc-link capacitor voltages. This PWM strategy supports a smooth transition between power flow directions while maintaining control stability and system efficiency. The four distinct switching states implement the three-level PWM operation, ensuring effective current regulation and voltage balancing across the dc-link. Although the described modulation is presented for rectifier mode, the same strategy is readily applicable to inverter mode through a suitable reversal of current direction and corresponding adjustments in the switching logic.

B. Single-Phase ac Input

Fig. 4 presents the PWM-based switching strategy and corresponding conduction states for one phase of the bidirectional Vienna rectifier. In this configuration, six switches— S_1, S_4, S_7, S_8, S_9 , and S_{11} —are used to control the input current i_{Lx} , shaping it into a sinusoidal waveform while simultaneously regulating the voltages across the two dc-link capacitors, C_1 and C_2 , which are arranged in parallel configuration.

It worth to note that, although, switches S_6 and S_{10} are connecting the negative terminals of capacitors C_1 and C_2 (connecting node M to node n) it is optional to constantly turn on switches S_8 and S_{11} during the positive cycle, and turn on switches S_4 and S_9 during the negative cycle.

Similar to the three-phase case, the control scheme uses a pulse-width modulation (PWM) approach, where a reference signal is continuously compared with a triangular carrier waveform. The outcome of this comparison determines which switches are turned on and off, thereby generating the voltage across the input inductor needed to form a sinusoidal current profile, as illustrated in Figs. 4(a) and 4(d).

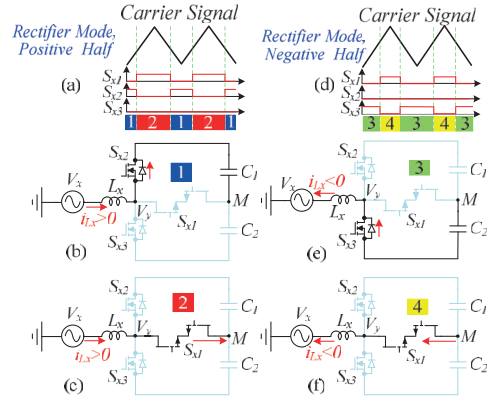


Fig. 3. PWM gating logic and conduction states for a single phase-leg of the bidirectional Vienna rectifier: (a) PWM gating logic for positive half cycle, (b) conduction state when the reference is greater than the carrier in positive half cycle, (c) conduction state when the reference is lower than the carrier in positive half cycle, (d) PWM gating logic for negative half cycle, (e) conduction state when the reference is greater than the carrier in negative half cycle, (f) conduction state when the reference is lower than the carrier in negative half cycle.

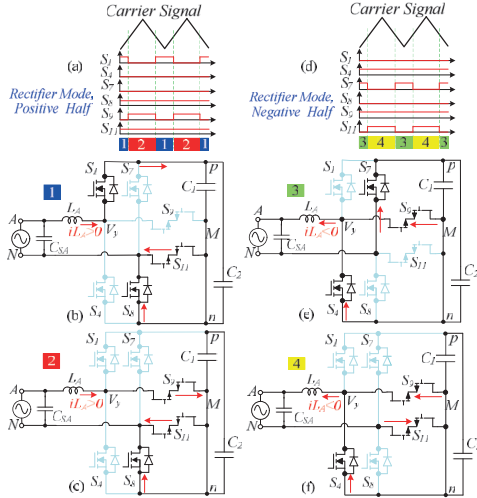


Fig. 4. PWM gating logic and conduction states for a single-phase implementation of the bidirectional Vienna rectifier: (a) PWM gating logic for the positive half-cycle, (b) conduction state when the reference is greater than the carrier in the positive half-cycle, (c) conduction state when the reference is lower than the carrier in the positive half-cycle, (d) PWM gating logic for the negative half-cycle, (e) conduction state when the reference is greater than the carrier in the negative half-cycle, (f) conduction state when the reference is lower than the carrier in the negative half-cycle.

During the positive half-cycle in rectifier operation, if the reference signal is higher than the carrier, switch S_1 is activated (Fig. 4(a)). Conversely, during the negative half-cycle, switch S_7 is turned on (Fig. 4(e)). If the reference signal falls below the carrier value, then S_9 is used in the positive half-cycle (Fig. 4(c)), and S_{11} in the negative half-cycle (Fig. 4(f)). In inverter mode, the logic is reversed.

To put it more simply, the PWM operates at high frequency using the duty cycle D as a key control parameter. When $D=1$, S_1 or S_7 stays on (depending on current direction), while S_9 and S_{11} remains off. This configuration allows the full dc-link voltage (represented by V_j in Fig. 4) to be applied directly to the inductor, enabling maximum voltage transfer. On the other hand, when $D=0$, switches S_9 or S_{11} are turned on, effectively connecting the voltage point V_j to the midpoint (M), which also ties to the ac neutral (N), clamping the inductor voltage to zero. As a result, the voltage equation described earlier for V_j as equation (1) remains valid.

By modulating the switching states, the converter generates a three-level voltage waveform that enables unity power factor, sinusoidal input current, and balanced parallel dc-link capacitor voltage. This PWM method ensures stable and efficient operation, supports bidirectional power flow, and uses four distinct switching states for effective current and voltage control. Though described for rectifier mode, the same approach applies to inverter mode with reversed current and adjusted switching logic.

C. Active Decoupling Operation in Single-Phase ac Input

In the single-phase rectifier connected to the ac grid (considering Fig.5(a)), where the input voltage and current are sinusoidal, and the power factor is ideally unity. The instantaneous grid voltage $v_{AN}(t)$ and input current $i_A(t)$ can be expressed as:

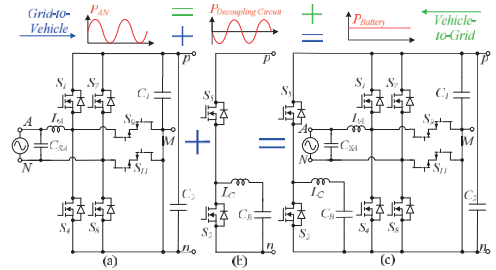


Fig. 5. Simplified circuit of the single-phase ac configuration with paralleled dc-link capacitors C_1 and C_2 , (a) single phase-rectifier, (b) decoupling cell, and (c) single-phase with paralleled decoupling cell with dc-link capacitors C_1 and C_2 .

$$\begin{cases} v_{AN}(t) = V_m \sin(\omega t) \\ i_A(t) = I_m \sin(\omega t) \end{cases} \quad (2)$$

Where, V_m and I_m are the peak values of the grid voltage and injected current, respectively, and $\omega=2\pi f$ is the angular frequency of the ac grid. The instantaneous input power drawn from the grid is given by:

$$P_{AN}(t) = v_{AN}(t)i_A(t) = V_m I_m \sin^2(\omega t) = \frac{V_m I_m}{2} [1 - \cos(2\omega t)] \quad (3)$$

This shows the power consists of a constant (average) power component P_{avg} and a time-varying (ripple) component $P_{Ripple}(t)$ at twice the grid frequency, which are defined as below:

$$\begin{cases} P_{avg} = \frac{V_m I_m}{2} = P_{Batt} \\ P_{Ripple}(t) = -\frac{V_m I_m}{2} \cos(2\omega t) \end{cases} \quad (4)$$

In the rectifier, the dc output must be steady. However, due to the presence of $P_{Ripple}(t)$, the power balance between the ac input and dc output fluctuates, introducing a double-frequency ripple on the dc-link. To mitigate this, an active decoupling circuit is integrated across the midpoint of the dc-link capacitors. This module dynamically handles the pulsating portion of the input power, temporarily storing or supplying energy to maintain a constant dc output. It effectively absorbs $P_{Ripple}(t)$ and prevents it from reaching the dc load. This energy balancing is essential because a large ripple in the power leads to voltage ripple across dc-link capacitors and it may compromise power quality, introduce distortion, or reduce control accuracy.

The decoupling circuit power $P_{Decoupling}(t)$ (shown Fig.5(b)) handled by the active module is:

$$P_{Decoupling}(t) = -P_{Ripple}(t) = \frac{V_m I_m}{2} \cos(2\omega t) \quad (5)$$

Thus, by utilizing capacitor C_B with active decoupling operation (shown Fig.5(c)), the active decoupling circuit acts like a dynamic energy buffer, ensuring that:

$$\begin{cases} P_{AN}(t) = P_{Batt}(t) + P_{Decoupling}(t) & \text{Vehicle-to-Grid} \\ P_{Batt}(t) = P_{AN}(t) + P_{Decoupling}(t) & \text{Grid-to-Vehicle} \end{cases} \quad (6)$$

In active decoupling, the capacitor C_B is not solely responsible for energy storage as in passive methods, but works with a controlled circuit to dynamically absorb and release the pulsating power (at 2ω) from the ac side.

TABLE I. PROTOTYPE PARAMETERS AND COMPONENTS

Components Characteristics	
Suppression Capacitors (C_{SA} , C_{SB} and C_{SC})	Ceramic Capacitor, 1.8 μF , 630 V
DC-Link Capacitors (C_1 and C_2)	Film Capacitor, 35 μF , 500 V
DC-DC Output Capacitors (C_3 and C_4)	Film Capacitor, 15 μF , 600 V
Battery Capacitor C_5	Film Capacitor, 9 μF , 1000 V
Filtering Inductors (L_A , L_B and L_C)	ETD 59/31/22-N97, 4 $^{\circ}C/W$ Thermal Resistance, 260 μH , 20 $m\Omega$
Semiconductor Elements	
Rectifier Stage SiC MOSFETs ($S_1 - S_6$)	Infineon Technologies, IMZA120R014M1HXKSA1, 1200 V , 14 $m\Omega$
Rectifier and DC-DC stages GaN Transistors ($S_7 - S_{12}$) and ($G_1 - G_{16}$)	Infineon Technologies, GaN FETs Automotive GS-065-060-5-T-A-MR, 60A, 650V
Solid-State Circuit Breakers SiC MOSFETs ($SSCB_1$ and $SSCB_2$)	Infineon Technologies, IMZA120R007M1HXKSA1, 1200 V , 7 $m\Omega$
Solid State Relays	SW_1 ADJH21112, 50 A
	SW_2 and SW_3 T9GVSL14-12, 30 A
Operating Point in Inverter Mode	
Peak AC Three/Single Phase Voltages	320 V
Maximum Battery voltage V_{Batt}	800 V
Maximum Output Power P_{out}	11 kW
Switching frequency f_s	PFC Stage 100 kHz
	DC-DC Stage 700 kHz
Thermal Cooling System Characteristics	
Thermal Film for GaN Transistors with Thermal Resistance $R_{aBt} = 0.5^{\circ}C/W$	TG-A1780- 150-150-0.8 TIM 1.38 $^{\circ}C/W$
Thermal Film for SiC MOSFETs with Thermal Resistances $R_{aDC-PFC} = 0.51^{\circ}C/W$	SP1500ST0.008-02-1012 TIM 0.67 $^{\circ}C/W$

However, its design still depends on key system parameters like power level, voltage ripple, and switching behavior. From the power ripple behavior, the maximum ripple voltage of the decoupling capacitor can be expressed as [19]:

$$\Delta V_{C_B, Max} = \frac{V_m I_m}{2\omega C_B V_{C_B}}. \quad (7)$$

To ensure continuous voltage behavior and reliable control, the ripple voltage must remain within a bound. The bound for the Buck active decoupling circuit is:

$$\Delta V_{C_B, Max} \leq 2V_{C_B}. \quad (8)$$

By combining equations (7) and (8), the effective condition for minimum required capacitance is derived as:

$$C_B \geq \frac{V_m I_m}{4\omega V_{C_B}^2}. \quad (9)$$

V. EXPERIMENTAL PROTOTYPE

To validate the operation of the proposed structure, an 11 kW laboratory prototype is designed. The rectifier switches operate at a switching frequency of 100 kHz , while the dc-dc stage operates at 700 kHz , with a maximum battery charging voltage of 800 V . The characteristics of the active and passive components of the prototype are given in Table I. The converter was operated under the control of PWM signals produced by the TMS320F28379DPTPT microcontroller.

The power density of the onboard charger, under these operating conditions with passive cooling, is around 4.3 kW/L , based on a total volume of 2.57 L , which includes the volumes of the magnetic components, capacitors and heatsink. In the dc-dc stage, the transformers are designed using air-core coils instead of ferrite cores to eliminate core losses under high-

frequency and that high-power conditions. The operation of the dc-dc stage and the transformer design is out of scope of this work.

The built system laboratory prototype photograph is shown in Fig. 6. Fig. 6(a) illustrates the top side of the prototype (PFC stage), showing that all components are mounted on the top side of the PCB. Exceptions include the GaN transistors (designed for topside cooling in this application), SiC MOSFETs, and a portion of the decoupling capacitors, which are located on the underside beside the heatsink. A single heatsink, with 2.5 cm thickness, is designed to cool all semiconductors. It is positioned beneath the PCB, covering most of PCB surface to ensure effective thermal management.

The experimental waveforms are shown in Fig. 7. Fig. 7(a) presents the three-phase voltages V_A , V_B , and V_C , along with the phase C current i_C , measured under 5 kW output power and a 700 V battery voltage during three-phase inverter mode operation. The maximum measured voltage and current for each phase are 320 V and 11 A , respectively. Fig. 7(b) displays the phase voltage V_A , its corresponding current i_A , and the battery voltage V_{Batt} under 1.7 kW output power and 700 V battery voltage during single-phase inverter mode operation. The measured peak voltage and current for phase A are also 320 V and 11 A .

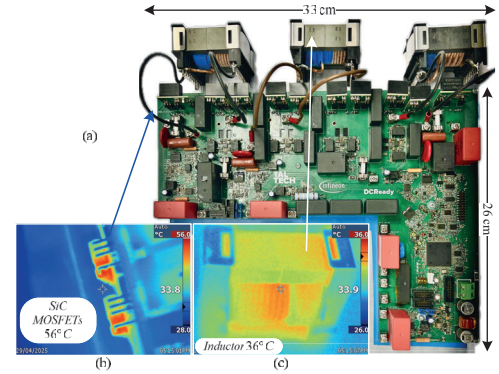


Fig. 6. (a) Photograph of the laboratory prototype (PFC Stage), (b) thermal camera picture of the SiC MOSFETs S_1 and S_2 under 5kW three-phase operation, and (c) thermal camera picture of the Filtering Inductor L_B under 5 kW three-phase operation.

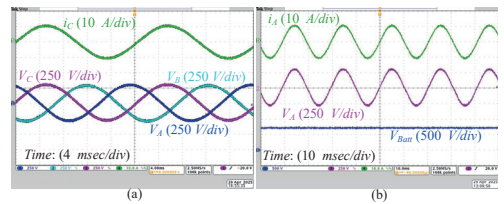


Fig. 7. Experimental waveforms of the proposed AC/DC-DC interface in inverter mode: (a) Three-phase voltages V_A , V_B , and V_C , and phase current i_C at 5 kW output power with 700 V battery voltage during three-phase operation, (b) Phase voltage V_A , current i_A , and battery voltage V_{Batt} at 1.7 kW output power and 700 V battery voltage during single-phase operation.

These results confirm that the proposed ac/dc-dc power electronic interface enables seamless power transfer for onboard battery charging systems across all grid types—three-phase ac, single-phase ac, two-wire dc, and three-wire dc—without requiring a change in the charging plug.

After stable operation at 5.1 kW output power and 700 V battery voltage, the temperature of the SiC MOSFETs—operating at a 100 kHz switching frequency—was measured at 56 °C, as shown in Fig. 6(b). Using thermal method for losses measuring and parameters given in Table I, the total losses was around 38 W for all active MOSFETs.

The resistance of the filtering inductors' winding was measured to be 20 mΩ using an RLC meter. With an RMS current of 7.8 A per inductor, the conduction losses per inductor are calculated as 1.2 W, totaling 3.5 W for all three inductors. Core losses were estimated based on thermal imaging, which showed the inductor cores reaching approximately 35 °C (Fig. 6(c)). Assuming an ambient temperature of 30 °C and a core thermal resistance of 4 °C/W, each core's loss is estimated at 1.5 W, giving a total of 4.5 W for all three inductors. Therefore, the total losses of the inductors are approximately 8.1 W.

Since the SSCB MOSFETs exhibited minimal temperature rise, their losses were calculated theoretically. With a conduction resistance of 7 mΩ and an RMS current of 7.8 A per phase, each SSCB dissipates approximately 0.85 W, totaling 1.7 W for the entire SSCB section.

In total, the estimated losses of the system amount to 50 W, indicating an overall efficiency of around 99 % for the PFC stage at a 5.1 kW output in the onboard battery charging system.

VI. CONCLUSIONS

The suggested ac/dc-dc power electronic interface facilitates bidirectional power transfer for onboard battery charging systems. It is compatible with single-phase ac, three-phase ac (both with and without a neutral wire), as well as two-wire dc and three-wire dc grids, achieving a power density of 4.3 kW/L. By utilizing a rectifier module, two isolated dc-dc modules with configurable series or parallel outputs, and a control system equipped with sensors, the interface achieves flexible operation through internal reconfiguration and adaptive control strategies. The system ensures proper grid integration by dynamically controlling switches SW_1 – SW_3 , S_1 – S_{12} , and the dc-dc modules based on the input grid type, providing an efficient, universal solution for diverse charging scenarios, which is validated by experimental results.

Based on experimental evaluation, the PFC stage of the interface achieves a final efficiency of 99% at a 5 kW output power, validating the effectiveness of the design for high-efficiency onboard charging applications.

ACKNOWLEDGMENT

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Paper VI

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A Three-Phase Unfolding-Based PFC Topology with Two Inductors for Electric Vehicles Battery Charging

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Abstract— This paper introduces a three-phase unfolding-based Power Factor Correction (PFC) rectifier design for electric vehicle charging systems, utilizing two filter inductors. The proposed structure achieves PFC action on the system grid side, similar to conventional three-phase PFC setups, but with only two filter inductors. Furthermore, the PFC functionality on the grid side requires only two current sensors (instead of three in the conventional ones) to measure the currents of the two filter inductors to control the current. This innovative approach results in a PFC-enabled electric vehicle battery charging system with significantly improved power density and reduced cost. To assess the advantages of the proposed design, a comparison is made with the conventional three-phase T-type structure. Theoretical analysis is performed, and simulations are carried to validate the proposed design versus the conventional T-type structure. Additionally, a 3.6 kW laboratory prototype of the proposed structure is constructed, and experimental results are presented for idea verification.

Keywords— Three-phase, power factor correction, unfolding-control, electric vehicle battery charger.

I. INTRODUCTION

This The pursuit of energy-efficient and environmentally friendly power conversion technologies has become a focal point in the modern era, driven by the escalating adoption of electric vehicles (EVs) and renewable energy sources [1]. In the case of EV power electronics chargers, several critical parameters have to be addressed, such as isolation and power density requirements along with a wide range of battery voltage regulation [2].

Among the critical components of these systems, PFC rectifiers play an important role in ensuring optimal power transfer and improved energy utilization. In response to this pressing need, researchers and engineers have been driven to explore novel topologies and innovative techniques to achieve high-performance battery charging systems.

In the pursuit of enhancing the efficiency and power density of three-phase ac-dc converters, soft dc-link-based topologies have been proposed in the existing articles [3]-[18]. Among these, the three-phase unfolding-based converters stand out as a class of soft dc-link converters capable of boosting power density and system efficiency [5]. Fig. 1a shows this solution. The soft dc-link topology offers notable advantages in terms of improved energy conversion and reduced losses, making it an attractive option for more efficient and compact ac/dc conversion systems. Various three-phase converter

topologies have been reported in the papers, falling under the category of this rectification approach [6] - [9]. These structures are part of unfolding-based converters utilizing the soft dc-link concept. They offer different design choices and advantages to achieve efficient three-phase rectification, catering to diverse application requirements in ac-dc conversion systems. For example, [6] presents a novel approach for isolated bidirectional power conversion between three-phase ac and dc systems. The proposed system utilizes series-resonant converter modules in combination with a three-phase unfolder to achieve efficient and reliable power conversion. This topology utilizes three-level legs with neutral point clamping for the unfolding stage and incorporates two separate isolated dc-dc converters for each of the soft dc-links. The combination of these components enables efficient power conversion and bidirectional energy flow between the ac and dc systems.

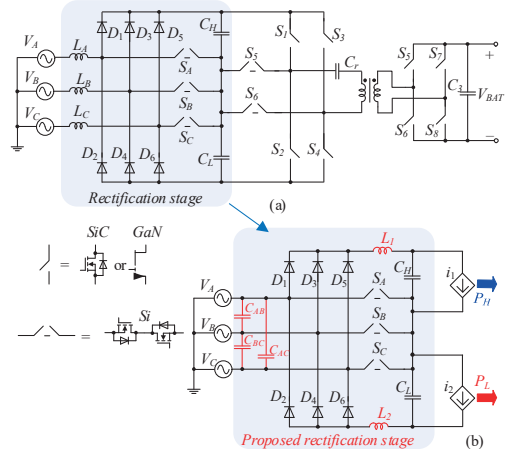


Fig. 1. (a) Conventional, and (b) proposed three-phase unfolding approach.

On the contrary, there exists a group of three-phase unidirectional PFC rectifiers that employ a dc-dc converter and a diode bridge serving the dual purpose of power factor correction (PFC) to the grid side and output regulation. The initial approach utilized a boost-type dc-dc converter [4]. Subsequently, the Swiss Rectifier, a buck-type version, was proposed in [7]-[9]. Building on this concept, other PFC

rectifier topologies can be devised using alternative dc-dc converter structures, such as SEPIC, buck-boost, or Cuk [10]. Moreover, by employing an isolated dc-dc converter, an isolated single-stage rectifier topology can be achieved [11]-[12]. The core principle remains the same across these topologies: two dc-dc converters are utilized to deliver power to a common dc output. Each of these dc-dc converters must be designed to handle a maximum power equivalent to the rectifier-rated power.

In structures provided in [13]-[18], the same concept of high-frequency dc-dc approaches is utilized connecting to the soft dc-link capacitors to serve the PFC action to the grid side.

In this paper, a three-phase unfolding-based ac-dc PFC structure with two inductors is proposed and depicted in Fig. 1b. This structure uses the same concept of utilizing high-frequency dc-dc converters to serve the power factor correction action, with adding the advantage of reducing the number of filter inductors to two compared to the three-inductors-based PFC stages of the proposed structures presented in [13]-[18]. Therefore, by using the proposed structure, the power density of the PFC stage can be increased significantly.

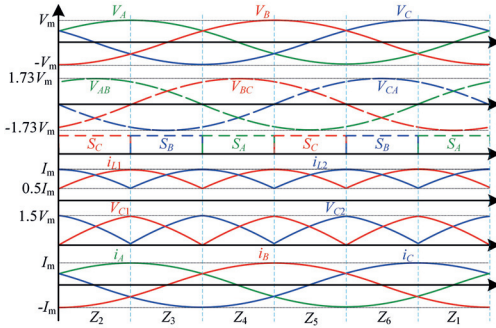


Fig. 2. Key waveforms of the proposed unfolding structure.

II. FUNDAMENTAL PRINCIPLES OF LOW-FREQUENCY UNFOLDING METHOD

In Fig. 1, the switches S_A , S_B , and S_C are Bidirectional Switches (BDS). Additionally, Fig. 2 presents the relevant ideal waveforms associated with this unfolding process, providing visual representations of the desired output waveforms at different stages of the conversion. These figures offer a clear and concise overview of the three-phase unfolding approach and its corresponding ideal waveforms.

Considering that the ac grid input voltages are balanced, they follow the positive sequences as follows:

$$\begin{bmatrix} v_A(t) \\ v_B(t) \\ v_C(t) \end{bmatrix} = V_m \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix}. \quad (1)$$

where V_m represents the peak value of the input ac grid voltage, and ω denotes the angular frequency associated with it.

The proposed three-phase rectifier which is shown in Fig. 1b takes the input voltages V_A , V_B , and V_C and converts them into two soft dc-link voltages V_{CH} and V_{CL} , which are applied to dc capacitors C_H and C_L . C_H and C_L capacitors serve as dc decoupling capacitors and play a crucial role in filtering out the switching currents from the high-frequency converter.

This ensures that only smooth currents enter the unfolding stage. However, these capacitors also draw additional reactive currents from the ac side, to create a balance between the ac input currents.

The three-phase rectifier functions as a current source and operates in six different zones (Z_1 - Z_6) based on the rotating phase angle ωt , as illustrated in Fig. 2. These zones dictate the switching sequences for the bidirectional switches S_A , S_B , and S_C . For instance, in the case of zones III and VI (Z_3 and Z_6), which are depicted in Fig. 3, they are defined when the voltages $V_A > V_B > V_C$ (or $V_{AB} > 0$, and $V_{BC} > 0$) and $V_C > V_B > V_A$ (or $V_{AB} < 0$, and $V_{BC} < 0$), respectively. To better understand, the operation of the proposed unfolding rectifier is explained in zones Z_3 and Z_6 . The operation of the rectifier in the other zones is similar to zones Z_3 and Z_6 .

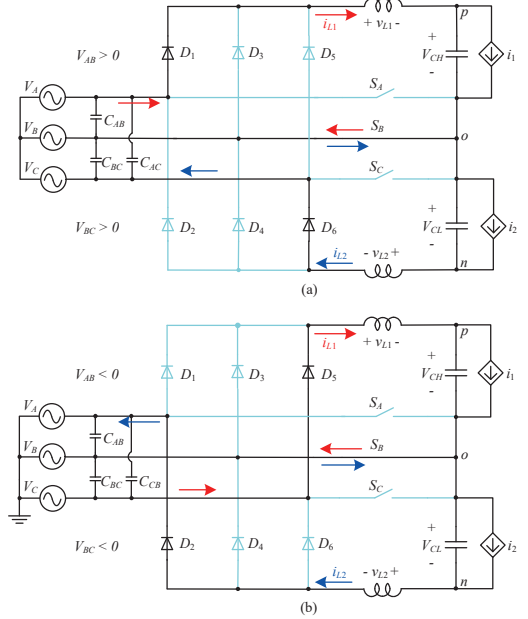


Fig. 3. Two operation modes of the proposed structure, (a) Zone III, (b) Zone VI.

Zone III [Z_3]: In this zone which is shown in Fig. 3(a), phase A always maintains a positive voltage and is connected to the high terminal through diode D_1 . On the contrary, phase C always has a negative voltage and is connected to the low terminal through diode D_6 . The remaining phase, B , can have either a negative or positive voltage. Therefore, it is connected to the middle terminal using the bidirectional switch S_B . Consequently, the middle terminal becomes floating and assumes the voltage of the middle phase.

Zone VI [Z_6]: Zone Z_6 is the vice versa of zone Z_3 . In the zone depicted in Fig. 3(b), phase A consistently maintains a negative voltage and is connected to the low terminal via diode D_2 . Conversely, phase C consistently has a positive voltage and is connected to the high terminal through diode D_5 . Phase B , on the other hand, can have either a positive or negative voltage. Consequently, it is connected to the middle terminal using the bidirectional switch S_B . As a result, the middle terminal becomes floating and assumes the voltage of phase B .

In the proposed three-phase two inductors unfolding based rectifier, inductors L_1 and L_2 act as the input current filters, instead of the three inductors in the conventional three-phase unfolding rectifiers [13]–[18]. By controlling the conducting currents through the inductors L_1 and L_2 as it is shown in Fig. 2, the three-phase ac currents i_A , i_B , and i_C can be balanced with their corresponding phase voltages as follows:

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = I_m \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) \end{bmatrix}. \quad (2)$$

In (2), I_m is the peak value of the input ac grid current. This current balance in the input ac grid currents can be realized by independently controlling the power transferred through the two high-frequency dc-dc converters which are connected to dc-link capacitors C_1 and C_2 . As an example, the dc-dc converters can be dual active bridge converters or other kinds of isolated or non-isolated dc-dc converters [13]–[18]. As a result, the proposed structure offers one significant benefit, which can be mentioned as follows. The power density of the structure is improved compared to the other previously presented three input filter inductor-based rectifiers by removing one inductor in the structures with the same provided performance.

In zone III, as depicted in Fig. 3(a), on the intermediate side, inductors L_1 and L_2 , and the neutral point are connected to the phase voltages A , C , and B , respectively. This arrangement allows the pulsating currents to be filtered through the dc-link capacitors C_1 and C_2 . The average values of these currents are determined by the corresponding references as follows:

$$Z_3 : \begin{cases} i_A = i_{L1} \\ i_B = i_{SB} \\ i_C = -i_{L2} \end{cases}. \quad (3)$$

Note that both i_{L1} and i_{L2} always have positive values. The neutral current (current through the neutral bidirectional switches S_A , S_B , and S_C) i_{SA} , i_{SB} , and i_{SC} can assume either a positive or negative value, depending on the phase condition. Its magnitude and direction are automatically determined by Kirchhoff's current law as follows:

$$i_{L1} - i_{L2} + i_{SB} = 0. \quad (4)$$

Indeed, by controlling the values of i_{L1} and i_{L2} , we can achieve balanced sinusoidal input currents for all three phases. As long as the positive currents i_{L1} and i_{L2} are appropriately regulated, the neutral current (i_{SA} , i_{SB} , or i_{SC}) will automatically adjust itself to maintain the overall balance according to Kirchhoff's current law. This control strategy allows us to achieve balanced and sinusoidal input currents for the three-phase system. As it is shown in Fig. 1, the controllable drawn currents i_1 and i_2 are considered as the load currents, which can be controlled by two independently working high-frequency (HF) dc-dc converters connected to the dc-link capacitors in the dc-dc stage. In this structure, by controlling the controllable drawn currents i_1 and i_2 the currents through the two intermediate inductors L_1 and L_2 can be controlled. As a result, by controlling the currents of the inductors L_1 and L_2 by controlling the drawn currents i_1 and i_2 through the dc-dc converters, the drawn grid input currents can be controlled and balanced sinusoidally.

III. PFC SYSTEM DESIGN

In this section, it is aimed to provide a comprehensive guideline for selecting the components in the design of the rectifier. The passive and active components' stress of the converter are calculated analytically, taking into account the operating parameters of the rectifier.

To illustrate this process, it is considered that the design of a 7.2 kW unity power factor PFC system. The rectifier will operate with an RMS voltage of $V_{RMS}=230$ V for each phase voltage. By analyzing the stresses on various components, suitable values can be determined for their specifications to meet the desired performance requirements.

A. Voltage and Current Stresses of the semiconductors

The peak voltage stress across the diodes D_1 – D_6 , and bidirectional power switches S_A , S_B , and S_C , is determined by the line-line voltage of the grid as follows:

$$V_{D1} = \dots = V_{D6} = V_{SA} = V_{SB} = V_{SC} = \sqrt{3}V_m = \sqrt{2}\sqrt{3}V_{RMS} = 563V. \quad (5)$$

To calculate the on-state losses of the semiconductors, it is necessary to calculate the RMS and average values of their conducting current. This requires deriving simple analytical approximations to facilitate the calculations. These approximations simplify the process of determining the on-state losses and allow for accurate estimations to be made. For the subsequent calculations, the following assumptions about the rectifier are considered:

- The phase current shape is purely sinusoidal.
- The main behavior is ohmic.
- There is no low-frequency voltage drop across the input filter inductors.

The RMS and average conducting currents through the diodes D_1 – D_6 are calculated as follows:

$$I_{D1}^{Avg} = \dots = I_{D6}^{Avg} = I_m \frac{\sqrt{3}}{2\pi} = 4.14A \quad (6)$$

$$I_{D1}^{RMS} = \dots = I_{D6}^{RMS} = I_m \sqrt{\frac{6\sqrt{3} + 8\pi}{48\pi}} = 7.28A. \quad (7)$$

The RMS and average conducting currents through the bidirectional switches are obtained as follows:

$$I_{SA}^{Avg} = I_{SB}^{Avg} = I_{SC}^{Avg} = I_m \frac{2 - \sqrt{3}}{\pi} = 1.28A \quad (8)$$

$$I_{SA}^{RMS} = I_{SB}^{RMS} = I_{SC}^{RMS} = I_m \sqrt{\frac{4\pi - 6\sqrt{3}}{24\pi}} = 2.55A. \quad (9)$$

B. Passive elements design: current and voltage stresses

The conducting currents through the inductors L_1 and L_2 are defined as follows:

$$\begin{cases} i_{L1}(t) = \frac{I_m}{2} + \frac{I_m}{2} \cos(1.5\omega t - \frac{\pi}{2}) \\ i_{L2}(t) = \frac{I_m}{2} + \frac{I_m}{2} \cos(1.5\omega t) \end{cases} \quad 0 \leq \omega t \leq \frac{2\pi}{3}. \quad (10)$$

Considering (10), the average and RMS conducting currents through the inductors L_1 and L_2 can be calculated as follows:

$$I_{L1}^{Avg} = I_{L2}^{Avg} = I_m \frac{3\sqrt{3}}{2\pi} = 12.42A \quad (11)$$

$$I_{L1}^{RMS} = I_{L2}^{RMS} = I_m \sqrt{\frac{6\sqrt{3} + 8\pi}{16\pi}} = 12.61A. \quad (12)$$

The maximum voltage across the dc-link capacitors C_H and C_L is equal to the $\sqrt{3}/2$ maximum value of the line-to-line voltage of the grid, which is defined as follows:

$$V_{CH}^{Max} = V_{CL}^{Max} = \frac{3}{2} V_m = 480V. \quad (13)$$

To calculate the conduction losses of the dc-link capacitors, the RMS value of their conducting current should be calculated. The RMS current value of dc-link capacitors C_H and C_L are defined as follows:

$$\begin{cases} I_{CH}^{RMS} = \sqrt{\frac{1}{\pi} \left(\int_0^{\frac{d\pi}{2}} (i_{L1}(t) - i_1)^2 dt + \int_{\frac{d\pi}{2}}^{\pi} i_{L1}^2(t) dt \right)} = 22.46A \\ I_{CL}^{RMS} = \sqrt{\frac{1}{\pi} \left(\int_0^{\frac{d\pi}{2}} (i_{L2}(t) - i_2)^2 dt + \int_{\frac{d\pi}{2}}^{\pi} i_{L2}^2(t) dt \right)} = 22.46A \end{cases} \quad (14)$$

In the above equation, d is the average duty cycle that is employed to modulate the high-frequency dc-dc converter after the unfolding stage.

IV. CONTROL SYSTEM

Fig.4 illustrates the control system of the proposed structure. The 3-phase unfolding structure operates at twice the line frequency, as shown in Fig. 2.

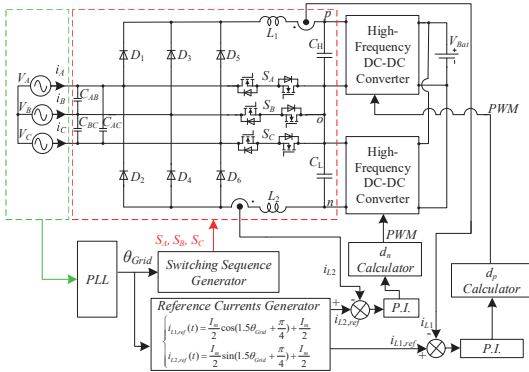


Fig. 4. Control system of the proposed structure.

This structure, on the other hand, is connected to the high-frequency dc-dc converters to draw the controlled currents and power from the grid. The control variables of the high-frequency dc-dc converters can be controlled independently and easily with Proportional-Integral (PI) controllers. Notably, voltages V_{po} and V_{on} vary at three times the line frequency. The PI control system controls the controlling variables of the high-switching frequency converters based on the variable voltage values of dc-link capacitors and transfers power to the dc-dc converters and the battery to draw the controlled currents from the 3-phase grid. In other words, the duty ratios d_p and d_n of the topology are adjusted to achieve power factor correction action and regulate the battery charging power. Considering Figs. 2 and 4 the switching method of the unfolding ac-dc structure can be understood.

The controlling grid current values are influenced by both d_p and d_n . However, controlling d_p and d_n only by sensing the currents of the inductors L_1 and L_2 simplifies the power control process by eliminating the need to sense the 3 grid currents. In the control loop shown in Fig. 1, the PI compensator processes

the difference of the inductors L_1 and L_2 currents and their corresponding reference currents $i_{L1,ref}$ and $i_{L2,ref}$ to generate the PWM signals for the two independent dc-dc converters to control the grid currents.

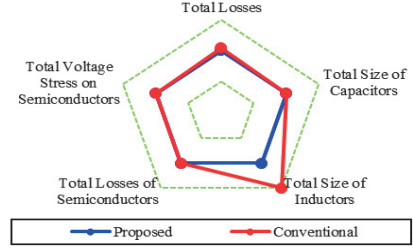


Fig. 5. Spider diagram of the performances of the proposed structure and the conventional three-phase T-type unfolding structure.

V. COMPARISON RESULTS

To better analyze the performance of the proposed converter, the proposed structure, is compared with the conventional three-inductor-based T-type three-phase unfolding structures [13]-[18] in terms of size and efficiency. The comparison results of the proposed converter with the conventional unfolding structure are shown as a spider diagram in Fig. 5. The first advantage of the proposed structure is that the proposed structure realizes the same performance compared to the conventional three inductor base structures with only two inductors.

The maximum saving energy of each of the inductors in both the conventional and the proposed structures can be defined as follows:

$$E_L = \frac{1}{2} L I_m^2. \quad (15)$$

In (15), L is the value of the filter inductors. Since in both structures, the maximum conducting currents through the inductors are equal to the maximum input current of the grid, the maximum saving energies of each of the inductors are equal. Therefore, the size of each inductor in both conventional unfolding and the proposed two inductor-based structures is equal. As a result, in the proposed structure the total size of inductors is reduced significantly to 67% compared to the conventional three-phase T-type structure. Moreover, in the proposed structure to realize the power factor correction action only two current sensors are needed to sense the currents of the inductors L_1 and L_2 , while in the conventional structure, three current sensors are needed to sense the input grid inductors currents. As a result, it can be claimed that the power density of the proposed structure is increased, and its cost is reduced significantly compared to the conventional one.

VI. SIMULATION RESULTS

To verify the performance of the proposed three-phase structure compared to the conventional three-phase structure, both structures are simulated in PSIM software in the same condition and with the same component values. The element values utilized in the simulations of both structures to assess their performance are presented in TABLE I.

The simulation results of the three-phase conventional T-type unfolding structure are shown in Fig. 6. Also, the simulation results of the proposed three-phase unfolding

structure are illustrated in Fig. 7. Considering both of the figures, it can be concluded that the proposed structure can act as a PFC like the conventional structure with the reduced number of the same size inductors to two. As a result, it can be claimed that the same performance of the conventional unfolding structure is achievable in the proposed converter along with adding the advantage of increasing the power density and reducing the cost significantly. The only difference is a slight deterioration of THD which is not significant and can be improved by more sophisticated control.

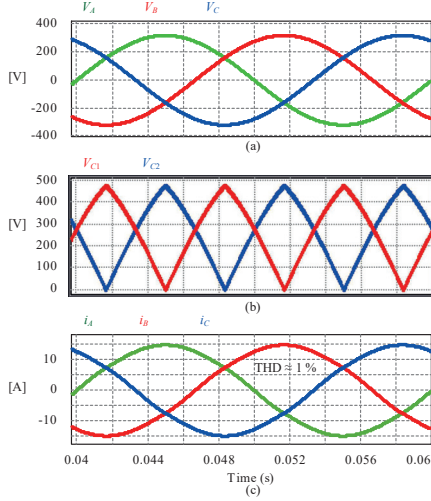


Fig. 6. Simulation waveforms of the conventional three-phase T-type unfold structure: (a) input grid phase-phase voltages V_A , V_B , and V_C , (b) dc-link capacitors voltages V_{C1} and V_{C2} , and (c) input grid phase currents i_A , i_B , and i_C .

TABLE I. CONSIDERED ELEMENTS VALUES FOR THE SIMULATIONS

Element	Value
Input voltages (V_m)	320 V
Maximum input current (I_m)	15 A
Output power (P_{out})	7.2 kW
Grid frequency	50 Hz
High-switching frequency of the dc-dc converters (f_s)	62 kHz
Filter inductors (L)	450 μ H
DC-Link capacitors (C_1 and C_2)	21 μ F

VII. EXPERIMENTAL RESULTS

To validate the proposed structure, theoretical and simulation results, a laboratory prototype of the proposed PFC structure is built, and its experimental results are provided in this section. The photograph of the built laboratory prototype is shown in Fig. 8. The laboratory results are provided under 3.6 kW output power and 50 % of the three-phase grid voltages. Two independently working conventional high-frequency buck-boost converters connecting to the dc-link capacitors C_1 and C_2 and two independent loads are utilized to interface the power between loads and the proposed PFC structure. These two high-frequency converters were acting instead of high-frequency dc-dc converters shown in Fig. 4. In this structure, the reference current values i_{L1} and i_{L2} of the filter inductors L_1 and L_2 are controlled independently by controlling the duty cycle values of the buck-boost converters, to realize the power factor correction action.

The obtained waveforms from the experiment are presented in Fig. 9. Fig. 9(a) shows the controlled currents of the

inductors L_1 and L_2 with the maximum value of 15 A, which validates the control system of the proposed structure. Also, in this figure, the voltage waveforms of the dc-link capacitors are shown.

The measured maximum voltage value of the dc-link capacitors is obtained 240 V which verifies (13) by considering 50 % of the input grid voltages. Also, the input grid currents waveforms along with the grid voltage V_A are shown in Fig. 9(b). In this figure, it is obvious that by controlling the current values of the inductors L_1 and L_2 with only two voltage sensors, the power factor correction action can be realized.

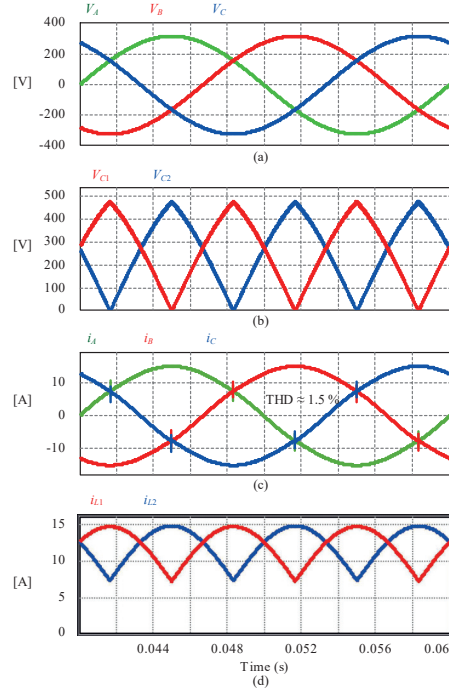


Fig. 7. Simulation waveforms of the proposed three-phase unfold structure: (a) input grid phase-phase voltages V_A , V_B , and V_C , (b) dc-link capacitors voltages V_{C1} and V_{C2} , (c) input grid phase currents i_A , i_B , and i_C , and (d) filter inductor currents i_{L1} and i_{L2} .

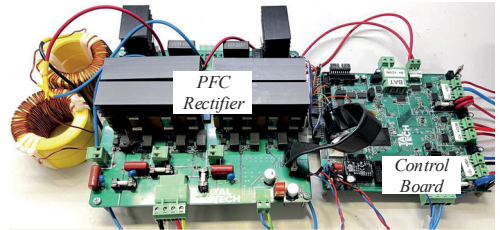


Fig. 8. Photograph of the laboratory prototype of the proposed structure.

VIII. CONCLUSIONS

This research presents a novel three-phase unfolding-based PFC rectifier design tailored for EV charging systems, featuring two filter inductors. The proposed structure efficiently achieves PFC action on the system grid side, akin to

conventional three-phase PFC configurations, but with the notable advantage of using only two filter inductors. Additionally, the PFC functionality on the grid side requires

just two current sensors to accurately measure and control the currents of the filter inductors.

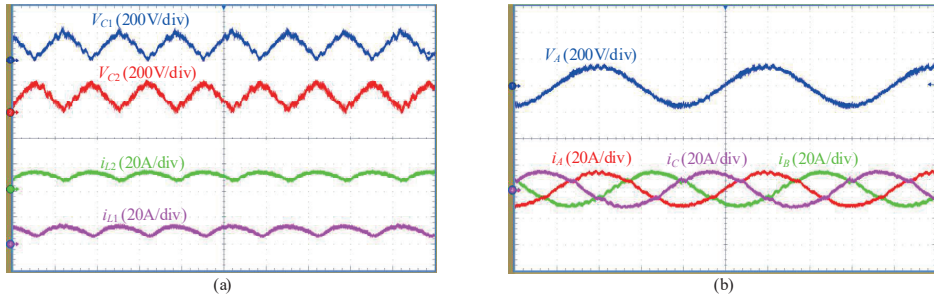


Fig. 9. Experimental waveforms of the proposed three-phase unfold structure: (a) dc-link capacitors voltages V_{C1} and V_{C2} , and filter inductors currents i_{L1} and i_{L2} , and (b) input grid phase-phase voltage V_A , and input grid phase currents i_A , i_B , and i_C .

The resulting design showcases remarkable improvements in power density and cost-effectiveness for electric vehicle battery charging systems. Through comparative analysis with the conventional three-phase T-type structure, the proposed design demonstrates its superior performance. Theoretical analysis and simulations under 7.2 kW power further confirm the validity and efficiency of the proposed structure compared to the conventional T-type counterpart. To reinforce the research findings, a 3.6 kW laboratory prototype of the proposed structure is successfully constructed and subjected to experimentation, providing tangible experimental results that further validate its effectiveness. Overall, the presented three-phase unfolding-based PFC rectifier design offers a promising solution for advancing electric vehicle charging systems, showcasing the potential for enhanced power density and cost efficiency in the pursuit of sustainable and efficient transportation.

ACKNOWLEDGMENT

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Paper VII

P. Mohseni, O. Husev, D. Vinnikov, M. Kasper, G. Deboy, and N. V. Kurdkandi, "FCB-MPC-Based Cycle Skipping Control For Soft-Switched Isolated AC-DC Converter With Reduced Inductors In PFC Stage," *Proc. IEEE IECON – 51st Annual Conference of the IEEE Industrial Electronics Society, Madrid, Spain*, Oct. 2025.

FCB-MPC-Based Cycle Skipping Control For Soft-Switched Isolated AC-DC Converter With Reduced Inductors In PFC Stage

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Abstract— This paper presents a control strategy for Electric Vehicle (EV) battery charging that combines a soft-switched isolated dc-dc converter with a three-phase unfolding-based Power Factor Correction (PFC) topology and reduced number of inductors. The proposed system introduces a finite cycle-based model predictive control method, which regulates current by optimally allocating discrete switching cycles across multiple energy paths. For instance, operating at a 25 kHz sampling rate with 40 switching cycles per interval (enabling a 1 MHz switching frequency), the controller achieves 2.5% resolution in power delivery while maintaining sinusoidal grid currents and a high power factor. Unlike conventional designs that require three inductors and separate PFC stages, the proposed architecture uses only two inductors and shifts the PFC function to the high-frequency dc-dc stage, significantly enhancing power density and reducing system complexity. A soft-switching modulation strategy ensures that all GaN-based switches operate under zero voltage switching conditions at high switching frequencies (hundreds of kHz to several MHz), effectively minimizing switching losses. Simulation results show a total harmonic distortion below 3% and confirm the proposed system's ability to deliver high efficiency, compact design, and precise regulation across a wide output range making it well-suited for next-generation EV chargers.

Keywords— *Electric vehicle charging, three-phase PFC, finite cycle-based model predictive control, cycle skipping control, soft dc-link.*

I. INTRODUCTION

The growing demand for Electric Vehicles (EVs) and renewable energy has intensified the focus on efficient, eco-friendly power conversion [1]. EV chargers, in particular, must meet key requirements such as isolation, high power density, and wide battery voltage regulation [2].

Power Factor Correction (PFC) rectifiers are key to maximizing power transfer and enhancing energy efficiency in these systems. To improve the efficiency and power density of three-phase ac-dc converters, researchers have proposed various soft dc-link topologies in recent studies [3]–[12]. Among these, three-phase unfolding-based converters have emerged as a promising category, known for their ability to enhance both system efficiency and power density, as illustrated in Fig. 1(a). The soft dc-link architecture offers significant benefits, such as reduced energy losses and improved conversion performance, making it well-suited for

compact and efficient ac-dc systems. Several three-phase topologies fall under this unfolding-based, soft dc-link approach, each offering distinct design benefits tailored to different application needs. For example, the Swiss Rectifier a buck-type topology was introduced in [4]–[6]. Expanding on this idea, other PFC rectifier configurations have been developed using different dc-dc converter types, including SEPIC, buck-boost, and Cuk converters. Additionally, integrating an isolated dc-dc stage allows for the realization of single-stage isolated rectifier designs [7]. Despite the variations in topology, the fundamental concept remains consistent: two dc-dc converters operate in parallel to supply power to a shared dc output, with each converter rated to handle the full output power of the rectifier system. In [8], authored by the same research group, a three-phase ac-dc PFC topology also shown in Fig. 1(b) is presented, which utilizes only two inductors instead of the traditional three. By delegating the power factor correction task to the high-frequency dc-dc stage, as demonstrated in earlier works [9]–[12], the proposed design maintains functional performance while enhancing power density by reducing the number of magnetic components.

In [9]–[12], compact and efficient dc-dc conversion solutions are proposed using either a 3-level asymmetric full bridge topology or a T-type converter. These approaches eliminate the need for two separate converters by employing a single 3-level structure capable of handling power from both sides of a soft dc-link. In particular, the T-type converter processes energy from the soft dc-link and directly generates a high-frequency ac output.

Paper [13], published same research group, presents a high-power-density isolated dc-dc converter based on an asymmetric CLLC topology using GaN/SiC devices, designed for applications like EV charging where isolation and wide output regulation are critical. The proposed design allows for efficient voltage and current control over a broad range and supports high-frequency operation using an air-core transformer. A 5 kW prototype operating at 500 kHz was developed to validate the concept. While initial efficiency was not exceptional, the use of GaN switches resulted in minimal semiconductor losses, and further optimization is expected to significantly boost both efficiency and power density, especially under full-load conditions.

By utilizing concepts provided in [8]–[13], this paper presents a compact EV battery charger using a soft-switched

3-Level Asymmetrical CLLC Full-Bridge Inductive Power Transformer (3LA-CLLC-FB-IPT) converter with a two-inductor, three-phase unfolding-based PFC topology.

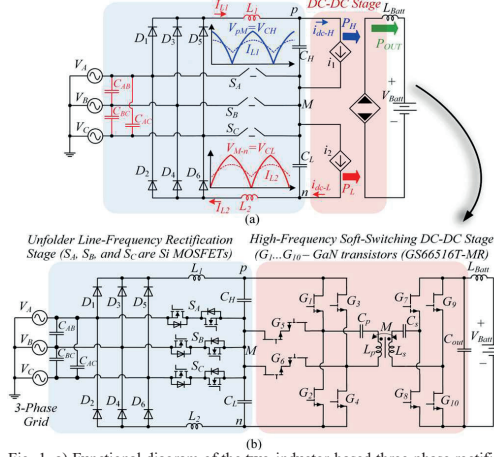


Fig. 1. a) Functional diagram of the two-inductor-based three-phase rectifier topology using an unfolded soft dc-link approach, b) The proposed 3LA-CLLC-FB-IPT converter serving as the dc-dc stage, integrated with the two-inductor-based three-phase unfolding PFC system.

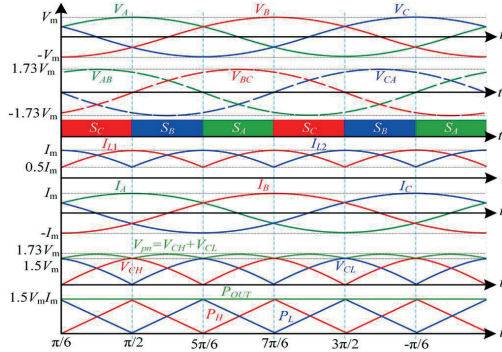


Fig. 2. Representative waveforms illustrating the operation of the unfolding-based rectifier structure.

A Finite Cycle-Based Model Predictive Control (FCB-MPC) strategy optimally allocates high-frequency switching cycles to regulate current and power with lower than 20 times lower sampling frequency. Unlike conventional approaches with dual dc-dc converters, the proposed system uses a single converter to process power from both soft dc-links, reducing complexity and enhancing power density. Operating at high frequencies with GaN switches under soft switching conditions, the system achieves low losses and acceptable grid current Total Harmonic Distortion (THD).

II. THREE-PHASE TWO-INDUCTORS UNFOLDING APPROACH

To understand the demands placed on the dc-dc stage, it's important to first look at how the three-phase unfolding-based converter works. Fig. 1(a) shows a conceptual overview of this approach. In this setup, the first stage referred to as the *unfolder* simply rectifies the incoming ac line voltages. It does not control the dc-link voltage or shape the line currents. As a result, this stage does not require Pulse-Width Modulation (PWM) and operates without high-frequency switching. The resulting dc-link is neither regulated nor stiff; it varies over

time and is considered a soft or floating link. A Three-Phase unfolding-based PFC topology with two inductors for electric vehicles battery charging is presented in [8], where the full operation and experimental validation of this architecture are discussed in detail. Fig. 1(b) shows the configuration of the three-phase unfolding-based PFC architecture, where a pair of inductors interface with a 3LA-CLLC-FB-IPT converter that serves as the system's dc-dc stage. In this work, the focus is on the dc-dc stage of the battery charger, which is responsible for shaping the inductors L_1 and L_2 to shape the input currents and regulating the output voltage. The second stage switches at high-frequency (hundreds of kHz to some MHz), handles power regulation, and ensures galvanic isolation through a high-frequency transformer, performing both energy conversion and control.

The voltages across the soft dc-link, denoted as V_{pM} (V_{CH}) and V_{Mn} (V_{CL}), follow a segmented sinusoidal waveform, as illustrated in Fig. 1(a). The switches in the unfolding bridge operate at twice the grid frequency, and transitions occur when there is zero voltage across the devices, which significantly reduces switching losses leaving only conduction losses to consider. These dc-link voltages are not constant; instead, they fluctuate over time within the range of 0 to approximately $1.5V_m$, where V_m is the magnitude of the grid's phase voltage.

The 3LA-CLLC-FB-IPT dc-dc converter is responsible for drawing currents i_{L1} and i_{L2} (defined in equation (1)) from the inductors L_1 and L_2 through the up-side and down-side dc-links [1]. These currents (i_{L1} and i_{L2}) must be controlled to match the sinusoidal shape and phase of the ac input currents to ensure proper grid interaction and achieve unity power factor. Since there are no large capacitors on the dc-link, the small filtering capacitors C_H and C_L are designed solely to suppress high-frequency ripple from the dc-dc stage, not to store bulky energy.

$$\begin{cases} i_{L1}(t) = 0.5I_m + 0.5I_m \cos(1.5\omega t - \frac{\pi}{2}) & 0 \leq \omega t \leq \frac{2\pi}{3} \\ i_{L2}(t) = 0.5I_m + 0.5I_m \cos(1.5\omega t) \end{cases} \quad (1)$$

Here, I_m represents the peak value of the sinusoidal grid current that needs to be drawn from the grid.

Fig. 2 illustrates the key waveforms of the PFC stage. For unity power factor to be maintained, the average switching behavior of the drawn currents i_{dc-H} and i_{dc-L} must mirror the inductors current waveforms i_{L1} and i_{L2} . This behavior is effectively modeled by treating the dc-dc converter's input ports as controlled current sources and the output as a dependent power source. The required instantaneous power drawn from each side of the soft dc-link, P_H and P_L , fluctuates dynamically from zero up to the output power P_{OUT} .

III. DC-DC STAGE DESCRIPTION AND MODULATION SCHEME

A. DC-DC Stage Description

The CLLC full-bridge converter is one of the most commonly adopted isolated dc-dc topologies for medium to high power applications, largely due to its ability to provide soft-switching operation. This makes it particularly suitable for systems like battery chargers. In this work, a modified version of the CLLC full-bridge converter—known as the 3LA-CLLC-FB-IPT is employed as the dc-dc stage, as shown in Figs. 1(b) and 3(a). A symmetrical full-bridge cycle-skipping control method for isolated resonant converters to regulate current and voltage waveforms is presented and experimentally verified in [13].

Unlike traditional 3-level bridges, the defining characteristic of the 3LA-CLLC-FB-IPT is that the two sections of the dc-link are not symmetrically divided, leading

to its asymmetric designation. Instead of relying on conventional CLLC control between bridge legs, this topology utilizes a more advanced cycle-skipping-based modulation scheme.

Functionally, the 3LA-CLLC-FB-IPT behaves as a three-port converter, with two series-connected input ports each linked to a different section of the soft dc-link and a single output port. The dc-dc stage operates at or slightly below the resonant frequency, typically in the hundreds of *kHz* to some *MHz* range, to enable Zero Voltage Switching (ZVS) turn-on for the GaN transistors. This eliminates C_{OSS} losses, turn-on losses, and minimizes turn-off losses, thereby achieving minimal switching losses [14]-[15]. The switching frequency of the dc-dc stage is defined as $f_{SW,dc-dc} = N \times f_{sampling}$, where N is an integer multiplier. Operating at such a high switching frequency enables the use of very compact high-frequency transformer components. Consequently, within each sampling period, N high-frequency cycles of the asymmetrical CLLC full-bridge converter can be executed. The value of N depends on the desired control resolution. As N increases, the control resolution improves, allowing for more precise regulation of the inductor currents (i_{L1} , i_{L2}), as well as the input grid current.

Both input paths contribute simultaneously to the generation of a high-frequency 3-level voltage waveform, denoted as V_{Pri} , which is shown in Fig. 3(a). During each sampling period, four types of switching cycles full-state (as shown in Fig. 3(b)), up-state (as shown in Fig. 3(c)), down-state (as shown in Fig. 3(d)), and zero-state (as shown in Fig. 3(e)) can be executed to regulate the reference currents through inductors L_1 and L_2 . The full-state is used to draw power simultaneously from both the upper and lower sections of the dc-link, enabling current shaping through both inductors L_1 and L_2 . The up-state cycle draws power only from the upper side of the dc-link, primarily shaping the current through inductor L_1 . Similarly, the down-state cycle draws power from the lower side of the dc-link, shaping the current through inductor L_2 . Zero-state cycle does not draw any power from the dc-link and acts as a freewheeling state.

The 3-level leg switching states and corresponding transformer primary side voltages are presented in TABLE I. The number of the different voltage levels, controlled by the number of cycles as parameters n_{Full} , n_{Up} , n_{Down} , and n_{Zero} , determines how the current through the inductors L_1 and L_2 are drawn to draw and shape the input energy. As shown in Fig. 3(a), the parameters n_{Full} , n_{Up} , n_{Down} , and n_{Zero} represent the number of switching cycles corresponding to different primary-to-dc-link connections. Specifically, n_{Full} denotes the number of full-state cycles where both the positive and negative terminals of the primary are connected to both the positive point p and the negative point n of the dc-link (as shown in Fig. 3(b)); n_{Up} refers to the number of up-state cycles connecting the primary to the positive point p and the mid-point M of the dc-link, associated with the upper-side capacitor C_H (as shown in Fig. 3(c)); n_{Down} corresponds to the number of down-state cycles connecting the primary to the mid-point M and the negative point n , related to the lower-side capacitor C_L (as shown in Fig. 3(d)); and n_{Zero} represents the number of zero-state cycles where the positive and negative terminals of the primary are shorted together (as shown in Fig. 3(e)). The total number of each switching cycles must be equal to the total number of cycles N as equation (2).

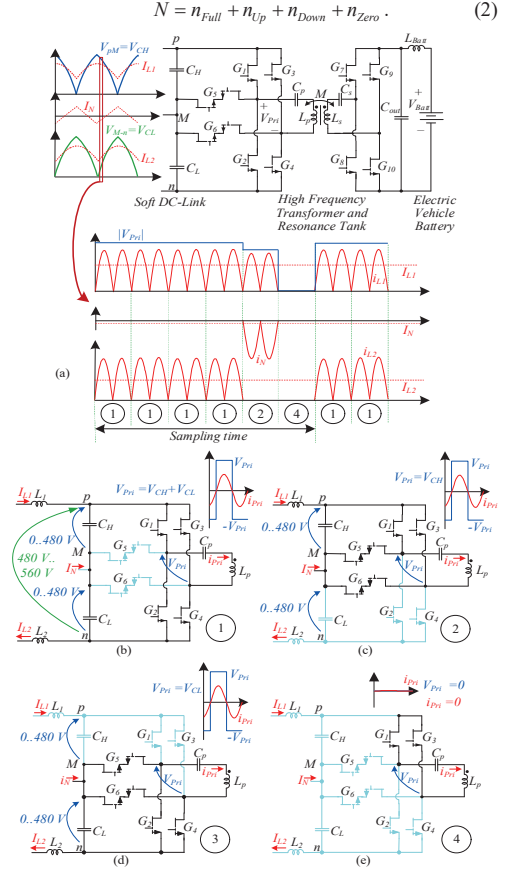


Fig. 3. Equivalent circuit diagrams of the proposed dc-dc stage operation under ZCS conditions, along with a conceptual illustration of the cycle-skipping control method used to regulate the drawn current from the inputs.

B. Modulation Scheme

The three-level legs in the converter are capable of connecting the bridge inputs to the Positive (p), Midpoint (M), or Negative (n) terminals of the dc-link. In a standard 3-level H-bridge configuration with symmetrical dc-link voltages (i.e., $V_{pM} = V_{Mn}$), there are only five distinct output voltage levels, with some redundancy: two combinations yield the half-voltage levels, while three different switch states can produce a zero voltage output. However, when the dc-link voltages on the positive and negative sides are unequal, the total number of unique output states increases to seven. All valid combinations of positive and negative legs of primary configurations that result in these output states are listed in TABLE I. Among these, the zero voltage output has three redundant switching pairs. Choosing an efficient modulation strategy is essential for maximizing system performance. A modulation scheme is proposed that both reduces conduction loss and ensures soft-switching (ZVS) for all eight switches in the 3-level legs. The selection of switching patterns follows two main principles:

Minimize conduction through 4-quadrant transistors (G_5 , G_6): These switches involve two transistors conducting

in series, which increases conduction losses. Therefore, only the zero voltage states $[G_1, G_3]$ and $[G_2, G_4]$ are utilized during zero output intervals to limit their usage.

TABLE I. 3-LEVEL LEG SWITCHING STATES AND CORRESPONDING PRIMARY SIDE VOLTAGES

Cycle Name	Positive Leg of Primary	Negative Leg of Primary	Primary Side Voltage V_{pri}	Voltage Range (V)	Related Figure
Full-Cycle	$G_1: ON, G_2: OFF$	$G_4: ON, G_3: OFF$	$V_{pm} = V_{CH} + V_{CL}$	480...560	3(b)
	$G_1: OFF, G_2: ON$	$G_4: OFF, G_3: ON$	$V_{mp} = -(V_{CH} + V_{CL})$	-560...-480	
Up-Cycle	$G_1: ON, G_2: OFF$	$G_6: ON, G_5: OFF$	$V_{pm} = V_{CH}$	0...480	3(c)
Down-Cycle	$G_1: OFF, G_2: ON$	$G_6: OFF, G_5: ON$	$V_{pm} = -V_{CH}$	-480...0	
Zero-State Cycle	$G_1: ON, G_2: OFF$	$G_3: ON, G_4: OFF$	$V_{pm} = V_{CL}$	0...480	3(d)
	$G_1: OFF, G_2: ON$	$G_3: OFF, G_4: ON$	$V_{pm} = -V_{CL}$	-480...0	
Zero-State Cycle	$G_1: ON, G_2: OFF, G_3: OFF$	$G_4: ON, G_3: OFF, G_5: OFF$	0	0	3(e)
	$G_1: OFF, G_2: ON, G_3: OFF$	$G_4: OFF, G_3: ON, G_5: OFF$	0	0	

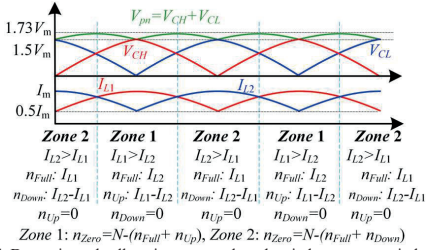


Fig. 4. Dynamic cycle allocation strategy based on inductor current imbalance for optimal power distribution and current shaping.

Enable ZVS through proper current direction: The switching transitions are arranged so that the resonant current i_{pri} flows in the direction needed to facilitate zero voltage turn-on for the devices involved. The timing and sequence of turning switches on and off are carefully coordinated to support zero voltage soft switching during each commutation event.

The cycle numbers of n_{Full} , n_{Up} , n_{Down} and n_{Zero} are tuned to ensure that the ac grid currents remain sinusoidal, fulfilling power factor correction requirements. At the same time, the total energy transferred dictated by the absolute values of these numbers of cycles is used to regulate the output current or voltage. By analyzing the average current on the primary side of the transformer during full-state cycle and up-state cycle or down-state cycle over each high-frequency period, the average currents through inductors I_{L1} and I_{L2} for each sampling period (see Fig. 3(a)) can be expressed as follows [16]:

$$\begin{cases} I_{L1} = \left(\frac{n_{Full}}{N} + \frac{n_{Up}}{N} \right) \frac{8}{\pi^2} \frac{V_{Batt}}{\omega_0 M} \\ I_{L2} = \left(\frac{n_{Full}}{N} + \frac{n_{Down}}{N} \right) \frac{8}{\pi^2} \frac{V_{Batt}}{\omega_0 M} \end{cases}, \quad (3)$$

where ω_0 is the angular resonant frequency, and M is the Mutual inductance of the inductive power transformer. As demonstrated in Fig. 4, the control strategy dynamically adjusts the cycle distribution based on the relative values of I_{L1} and I_{L2} :

Zone 1: When $I_{L1} > I_{L2}$, the shared full-state cycles n_{Full} are allocated to match I_{L2} , while the excess I_{L1} is balanced using n_{Up} cycles. Here, n_{Down} is set to zero.

Zone 2: If $I_{L1} < I_{L2}$, the roles reverse— n_{Full} follows I_{L1} , and the difference is covered by n_{Down} , while n_{Up} remains zero.

Balanced Case: When $I_{L1} = I_{L2}$, all current tracking is handled by n_{Full} alone, and both n_{Up} and n_{Down} are zero.

To achieve ZVS across all GaN transistors, the dc-dc stage operates at a constant, high switching frequency similar to that used in full-bridge CLLC resonant converters. This frequency is deliberately set equal to the resonant frequency of the primary tank. To ensure that sufficient turn-off current is available for ZVS turn-on across all switching transitions, the resonant capacitors on the primary and secondary sides are intentionally made asymmetrical. Specifically, this asymmetry is implemented by reducing the compensation capacitor on the secondary side. As a result, the input current exhibits a slightly inductive characteristic, which naturally facilitates zero voltage switching during transistor turn-on by sustaining the necessary current for soft commutation [13].

It is important to emphasize that configuring the primary and secondary resonant capacitors symmetrically at the resonant frequency leads to Zero Current Switching (ZCS) during both turn-on and turn-off events. While ZCS may reduce switching stress, it does not mitigate the considerable losses associated with the output capacitance C_{OSS} of GaN devices. These C_{OSS} -related losses, which stem from the energy stored and dissipated during switching transitions, become increasingly prominent at the high switching frequencies typically employed in modern power converters ranging from several hundred kilohertz up to the low megahertz range.

To mitigate these losses effectively, the asymmetrical configuration is considered. This allows enough resonant current to discharge the output capacitances of all full-bridge switches prior to turn-on, thereby suppressing C_{OSS} energy loss and enabling efficient soft-switching, as supported in [15]. Achieving ZVS also requires careful control of the energy stored in the transformer's primary inductance during switching transitions. This stored energy facilitates the charging and discharging of parasitic and device capacitances during the switching event. The behavior of this transition can be modeled using the following expression [14]:

$$0.5(L_M + L_{LK-p})I_{G-off}^2 \geq C_{Qeq}(V_S)V_S^2 + 0.5C_{Par}V_S^2, \quad (4)$$

where C_{Qeq} is equivalent charge-based capacitance of GaN transistors, C_{Par} is combined parasitic capacitance from PCB layout and transformer winding, I_{G-off} is turn-off current in the corresponding leg, and V_S is the voltage across the switching node. This model captures the relationship between parasitic capacitance and available current needed to drive ZVS, providing a valuable design metric for tuning converter performance at high frequencies.

IV. CONTROL SYSTEM

Fig. 5 presents the overall control scheme for the proposed system. The three-phase unfolding front-end operates at twice the grid frequency, as shown earlier in Fig. 2, and interfaces with the high-frequency 3LA-CLLC-FB-IPT dc-dc converter that is responsible for actively drawing power and shaping the input currents from the grid. These high-frequency converter is controlled through independently tuned FCB-MPC controller, which allow for simple and effective regulation of power flow.

The control logic is implemented in PSIM using a custom function block based on a C-script, operating, for example, at a 25 kHz sampling frequency. The primary function of this controller is to optimally allocate 40 high-frequency

switching cycles corresponding to a 1 MHz switching frequency across three discrete energy transfer paths: Full-path: n_{Full} , Upper capacitor path: n_{Up} , and Lower capacitor path: n_{Down} . This cycle-based modulation scheme enables fine-tuned control of the grid-side inductor currents while supporting soft-switching and reducing switching losses. The control strategy is built upon a simplified linear model for the inductor current increment caused by switching activity:

$$\Delta i_L(n) = \frac{n}{N} \frac{8}{\pi^2} \frac{V_{Bat}}{\omega_b M}. \quad (5)$$

where $\Delta i_{L(n)}$ is the expected inductor current change over n cycles.

To ensure that the inductor current references are accurately tracked, the controller searches for the optimal combination of n_{Full} , n_{Up} , and n_{Down} that minimizes a cost function based on absolute tracking error:

Case 1: $I_{L1,ref} > I_{L2,ref}$

$$\begin{cases} g_{Full} = |I_{L2,ref} - \Delta i_{L,Full}(n_{opt-Full})| \\ g_{Up} = |(I_{L1,ref} - I_{L2,ref}) - \Delta i_{L,Up}(n_{opt-Up})| \end{cases} \quad (6)$$

Case 2: $I_{L1,ref} < I_{L2,ref}$

$$\begin{cases} g_{Full} = |I_{L1,ref} - \Delta i_{L,Full}(n_{opt-Full})| \\ g_{Up} = |(I_{L2,ref} - I_{L1,ref}) - \Delta i_{L,Down}(n_{opt-Down})| \end{cases} \quad (7)$$

Case 3: $I_{L1,ref} = I_{L2,ref}$

$$g_{Full} = |I_{L1,ref} - \Delta i_{L,Full}(n_{opt-Full})| \quad (8)$$

The controller performs a brute-force enumeration over all allowable integer combinations of $n_{Opt-Full}$, n_{Opt-Up} , and $n_{Opt-Down}$ under the constraint $N \geq n_{Opt-Full} + n_{Opt-Up} + n_{Opt-Down}$. For each candidate set, the above cost function is evaluated, and the set yielding the lowest total error is selected.

Once the optimal values are found: $n_{Opt-Full}$ governs the number of full path (both capacitor) transfers, n_{Opt-Up} adds top capacitor-only current when needed, $n_{Opt-Down}$ adds bottom capacitor-only current when needed, and $n_{Opt-Zero} = N - n_{Opt-Full} + n_{Opt-Up} + n_{Opt-Down}$ represents the remaining unused switching cycles in each control period.

These cycle counts directly drive the gating signals of the 3LA-CLLC-FB-IPT high-frequency dc-dc converter. The modulation strategy is designed to ensure accurate current control and balanced power flow with reduced sensing overhead, using only inductor current feedback instead of full three-phase grid current measurement. This predictive and discrete optimization-based approach enables efficient digital control, particularly suitable for high-frequency, soft-switched EV charging systems using GaN-based power stages.

V. SIMULATION RESULTS

To validate the proposed FCB-MPC-based cycle-skipping control for the 3LA-CLLC-FB-IPT soft-switched converter in a three-phase unfolding-based PFC system, simulations were carried out in PSIM. The parameters used for these simulations are summarized in Table II.

Fig. 6(a) illustrates the performance of the proposed control system and configuration. The results show that the system achieves effective PFC by dividing each control period into 40 discrete decision points, resulting in a 2.5% control resolution. This resolution represents the smallest

incremental step the controller can make in adjusting power delivery or current through the cycle-skipping logic. Fig. 6(b) shows the voltage and current waveforms of switch G_1 , highlighting the soft-switching performance of the dc-dc stage. As observed, the switch turns on under ZVS conditions and turns off close to ZCS, minimizing switching losses even at a high switching frequency of 600 kHz. This efficient switching performance enables the use of GaN transistors such as the GS66516T-MR (650 V, 60 A) from Infineon Technologies allowing the converter to operate at even higher frequencies. This not only improves control resolution but also significantly reduces the size of passive components in the dc-dc stage. In addition, the design maintains this high efficiency with only two inductors of equal size, as opposed to three in traditional unfolding structures. The combination of high-frequency operation and soft-switching significantly enhances power density, reduces component volume, and lowers overall system cost.

The only notable trade-off observed is a slight increase in THD, measured at 2.8%, which remains within acceptable limits. This distortion can be further reduced by increasing the switching frequency or enhancing the control resolution. In summary, the proposed control method maintains comparable functionality to traditional approaches while offering significant improvements in efficiency, system integration, and power density.

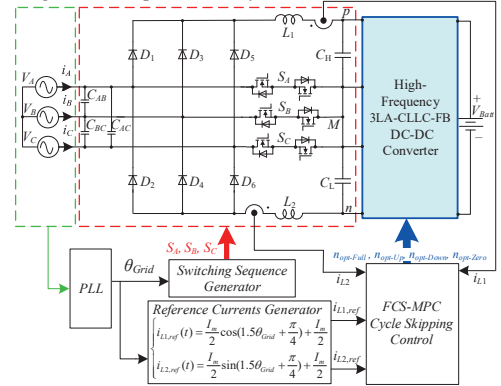


Fig. 5. Overall control architecture integrating the three-phase unfolding front-end with the high-frequency 3LA-CLLC-FB-IPT dc-dc converter for power regulation and grid current shaping.

TABLE II. SIMULATION SETUP: SELECTED COMPONENT VALUES

Component	Value
PFC Stage	
Input voltages (V_m)	320 V
Maximum input current (I_m)	30 A
Output power (P_{out})	14.5 kW
Grid frequency	50 Hz
Sampling Frequency (f_{sample})	15 kHz
Number of Cycles	40
Filter inductors (L)	100 μ H
DC-Link capacitors (C_1 and C_2)	10 μ F
Control Resolution ($1/N$)	2.5%
DC-DC Stage	
Resonance Capacitors C_p and C_s	$C_p = 7$ nF, $C_s = 6$ nF
Output capacitor C_{out}	100 μ F
Battery Inductor L_{Bat}	50 μ H
High Frequency Transformer (L_P, M, L_S)	10 μ H/ 5 μ H/ 10 μ H, Turns ratio: 1
Switching frequency of the dc-dc converter (f_s)	600 kHz
Battery Voltage V_{Bat}	700 V

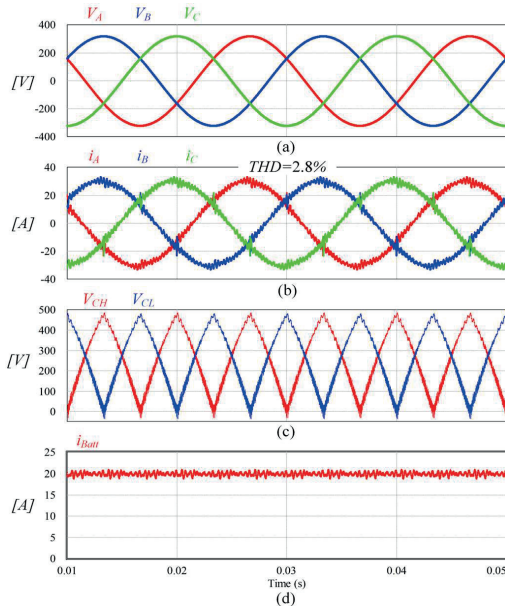


Fig. 6. Simulated results of the proposed FCB-MPC-based cycle skipping control system. (a) phase-to-phase input voltages V_A , V_B , and V_C , (b) grid input phase currents i_A , i_B , and i_C , (c) voltages across soft dc-link capacitors V_{CH} and V_{CL} , and (d) battery charging current i_{Batt} .

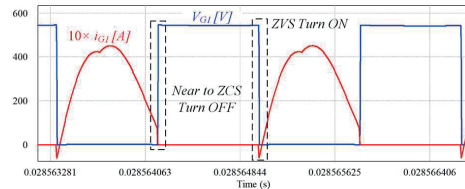


Fig. 7. Voltage and current waveforms of high-frequency switch G_1 within the dc-dc stage, demonstrating soft-switching performance.

VI. CONCLUSIONS

This paper presented a compact, high-efficiency EV battery charging system that combines a soft-switched 3LA-CLLC-FB-IPT converter with a two-inductor three-phase unfolding-based PFC topology. A FCB-MPC control strategy was introduced to optimally distribute high-frequency switching cycles, enabling precise current and power regulation while maintaining unity power factor. By merging PFC and power conversion into a single high-frequency dc-dc stage, the system eliminates the need for dual converters and reduces magnetic components boosting power density and integration. The design supports the use of GaN transistors under ZVS/ZCS conditions at high switching frequencies, reducing losses and enabling smaller passive components.

Simulation results confirm the effectiveness of the proposed approach, achieving sinusoidal grid currents with less than 3% THD, fine-grained 2.5% control resolution, and robust soft-switching performance. While a slight THD increase was observed, performance remains well within acceptable limits, with room for further improvement through higher switching frequencies or finer control.

Overall, the proposed cycle-skipping control strategy may offer a scalable, efficient solution for next-generation EV chargers, combining intelligent control with high-frequency operation and a compact system design.

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