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DESIGNING FPGA BASED IOC EMBEDDED SYSTEM FOR ESS APPLICATIONS

Master's thesis

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FPGA BAASIL IOC SARDSÜSTEEMI PROJEKTEERIMINE ESS-I RAKENDUSTELE

Magistritöö

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Author’s declaration of originality

I hereby certify that I am the sole author of this thesis. All the used materials, references to the literature and the work of others have been referred to. This thesis has not been presented for examination anywhere else.

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Abstract

In this thesis, a standalone embedded computer system was developed for the European Spallation Source (ESS) project. The embedded system is going to be implemented to the ESS Integrated Control System (ICS). Technical requirements required to have a Zynq series Field Programmable Gate Array (FPGA), which is tightly integrated with the Central Processing Unit (CPU) to provide connectivity to external interfaces. In addition, the embedded computer implements a system supervisor microcontroller that configures power supplies and starts up the FPGA, by running its own custom software. The embedded computer is planned to fit into the 120mm x 120mm x 70mm enclosure.

This thesis is written in English and is 42 pages long, including 8 chapters, 32 figures and 1 table.

Annotatsioon

FPGA BAASIL IOC SARDSÜSTEEMI PROJEKTEERIMINE ESS-I RAKENDUSTELE

Käesoleva magistritöö eesmärk on arendada *European Spallation Source* projekti raames iseseisev sardsüsteem, mida oleks võimalik integreerida rajatise *Integrated Control Systemi* ehk *ICS-i*. *ICS* on keeruline süsteem mis koosneb riistvarast, tarkvarast ja andmebaasidest, mis vastutavad rajatise info sünkroniseerimise ja testseadmete kontrollimise eest. Sardsüsteemid paigutatakse üle terve rajatise raskelt ligipääsetavaste kohtadesse ning seetõttu peab see olema võrdlemisi väike ning eriline rõhk on pööratud süsteemi töökindlusele ning kaugelt haldamisele. Sardsüsteem baseerub Zynq 7030 seeria *System-on-Chip* lahendusel, millel jookseb reaalajasüsteem. Zynq 7030 integreerib endas *FPGA* ning *ARM* protsessori, jaotudes seega kaheks osaks: *Programmable Logic* ja *Processing System.* Loogika osa kasutab sünkroniseerimiseks valguskaablitel baseeruvat liidest, mille kiirused ulatuvad kuni 3.125 Gbit/s ja pakub FMC kaardi kaudu IO ühilduvust. Süsteemi osa töötleb andmeid ja pakub ühilduvust välimiste liidestega. Kogu sardsüsteemi haldab eraldiseisev mikrokontroller, mis seadistab kõik vajalikud toited, haldab süsteemi, käivitab *FPGA* ja pakub kaugelt ligipääsu kas üle *Etherneti* või *RS-232* liidese. Mikrokontrolleri funktsiooni täidab STM32F407VGT7 mikroskeem. Kogu sardsüsteem mahub ära 120mm x 120mm x 70mm korpusesse.

Lõputöö on kirjutatud inglise keeles ning sisaldab teksti 42 leheküljel, 8 peatükki, 32 joonist, 1 tabelit.

List of abbreviations and terms

ARM	Advanced RISC Machine
CPU	Central Processing Unit
DDR	Double Data Rate
DIN	German Institute for Standardization
eMMC	Embedded MultiMediaCard
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
EPICS	Experimental Physics and Industrial Control System
ESD	Electrostatic discharge
ESS	European Spallation Source
EVR	Event Receiver
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GIT	Distributed version-control system
IO	Input/output
IOC	Input/output Controller
IC	Integrated Circuit
LDO	Low-dropout regulator
LPC	Low Pin Count
LQFP	Low Profile Quad Flat Package
NAND	NOT-AND gate
NOR	NOR gate
MAC	Medium access control
MCU	Microcontroller Unit
MDIX	Medium Dependent Interface Crossover
MGT	Multi-Gigabit Transceiver
MTCA	Micro Telecommunications Computing Architecture
OS	Operating System

PCB	Printed Circuit Board
PG	Power Good
PHY	A device implementing physical layer protocol
PL	Programmable Logic
PS	Programmable System
QSPI	Quad Serial Peripheral Interface
RAM	Random Access Memory
RJ	Registered Jack
RS-232	Recommended Standard 232
SFP	Small Form-factor Pluggable
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SW	Software
SVC	Supervisor CPU
TTL	Transistor-transistor Logic
TVS	Transient Voltage Suppressor
UART	Universal asynchronous receiver-transmitter

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1 Introduction

European Spallation Source (ESS) is a research facility which is currently being built to Lund, Sweden. It will be the largest and most powerful next-generation neutron source.

ESS will enable the scientists to develop and discover new materials in many different fields, for example: aerospace, plastics or biotechnology. The estimated cost of the whole project will be around 1.8 billion euros, at least 17 European countries are taking part in construction and operating of ESS [1].

This master's thesis will focus on designing hardware for ESS control system purposes. Software will be written by Department of Computer Systems supported by the competencies of Testonica [2]. As the Field Programmable Gate Array based Input/output Controller (FPGAIOC) will be installed in remote locations with limited accessibility, special attention shall be turned to the reliability and remote manageability aspects.

Customer requirements which are written to the technical specification will be the basis of developing the hardware and software. The device has to fit into 120 x 120 x 70mm enclosure and have a DIN rail mounting system [3].

This thesis consists of 6 chapters. "Overview", which gives an overall architecture and introduction to the project. "FPGA selection", where selecting the suitable FPGA is described. "Hardware design" describes how the schematics was designed. "PCB layout" describes how the PCB layout was designed. "Testing and verification" describes testing and verification requirements for the FPGAIOC. "Documentation" describes how and what is documented regarding the FPGAIOC development.

2 Overview

Experimental Physics and Industrial Control System (EPICS) Input/output Controller (IOC) is a Micro Telecommunications Computing Architecture (MTCA.4) crate form factor single-board computer running Linux or real-time operating system.

The computer is running iocCore, a set of EPICS routines used to define process variables and implement real-time control algorithms [4]. The general architecture of EPICS IOC consists of a Central Processing Units (CPU) subsystem with non-volatile storage (e.g. flash) and operating memory (e.g. Random Access Memory (RAM)) to run the Operating System (OS) and EPICS software (iocCore). An FPGA is tightly integrated with the CPU to provide connectivity to external interfaces for control or data acquisition. Optical fiber based interface is used to provide timing and synchronization to IOCs [3].

European Spallation Source Integrated Control System has a number of standardized EPICS IOC platforms which are generally highly capable embedded systems with Field-programmable Gate Arrays (FPGAs) and CPUs integrated. However, the ESS Integrated Control System is distributed over a large area where many remote locations have limited requirements, space and accessibility. For remote locations with limited space and accessibility the MTCA.4 crate based solution is not feasible or cost efficient. The FPGAIOC is therefore planned to have a compact, DIN-rail mountable, form factor with limited functionality and Input/Output (IO) interfaces [3].

To save space, a Xilinx Zynq or similar System-on-Chip (SoC) FPGA platform could be used for the embedded computing and connectivity platform. However, the general system structure and support for synchronization interface shall be provided in the FPGAIOC [3].

As the FPGAIOC controllers will be installed in remote locations with limited accessibility special attention shall be turned to reliability and remote manageability aspects. Customer requirements are the basis for developing the hardware. The original

customer requirements are collected from various presentations and meeting minutes. Overall overview of the system can be seen from the Figure 1 below [3].

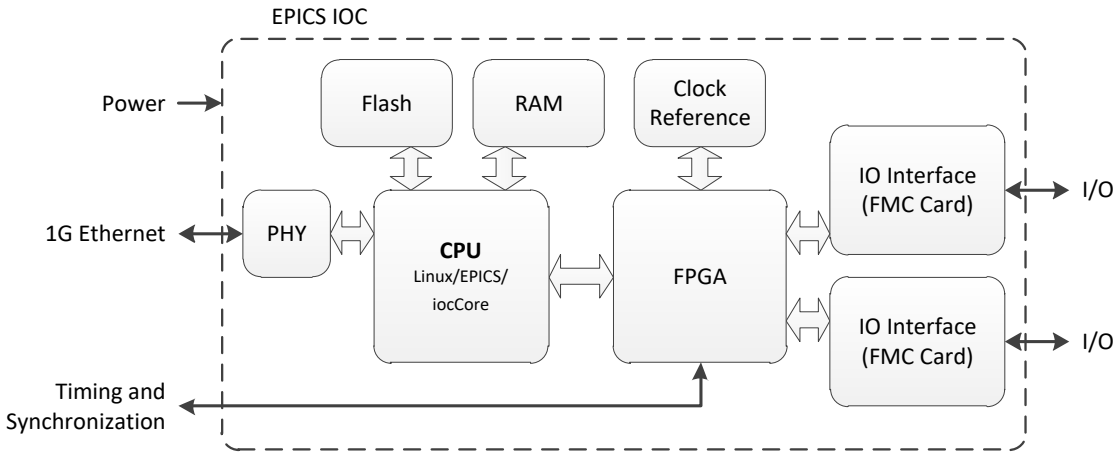

Figure 1. General overview of EPICS IOC

2.1 Architecture

In order to achieve tight integration, the CPU and programmable logic shall be integrated into a single device such as Zynq 7000 series SoC FPGA or equivalent. On board Double Data Rate (DDR) memory and Flash shall enable running embedded Linux. On top of Linux runs EPICs iocCore software (SW) in the final application. Figure 2 describes sketch architecture of the FPGAIOC [3].

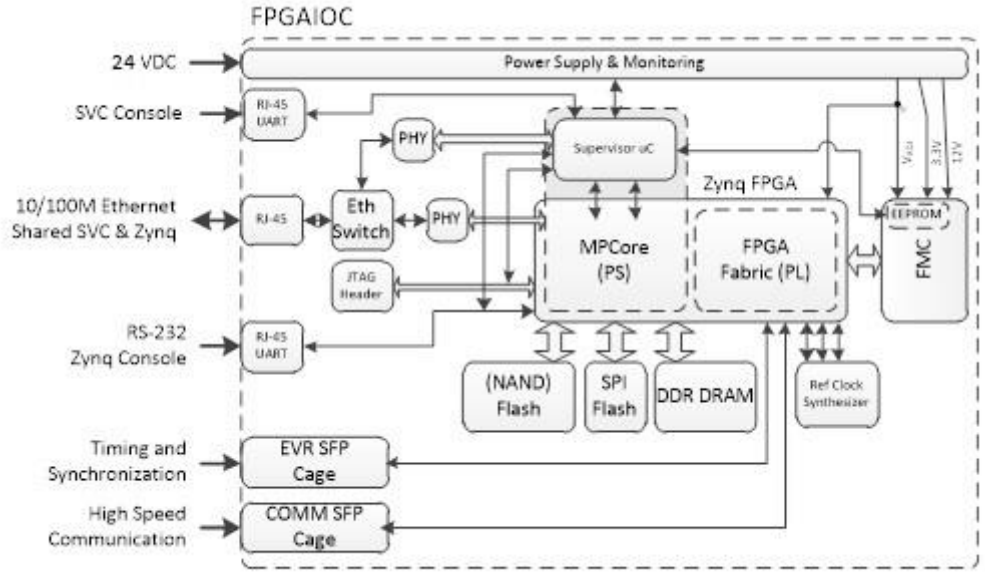

Figure 2. System Architecture sketch of FPGAIOC

The programmable logic part (FPGA) of the FPGAIOC is planned to host a timing receiver system, enable high speed communication as well as provide IO connectivity through a FPGA Mezzanine Card (FMC) connector. The timing receiver connects to the facility timing system via optical fiber connections through the Small Form-factor Pluggable (SFP) cage [3].

A dedicated clock recovery integrated circuit (IC) is required for the timing receiver. Additional SFP cage is included on-board FPGAIOC for high speed communication. In addition to the main CPU, the FPGAIOC shall integrate a system supervisor microcontroller that is responsible of configuring the power supply and starting up the Zynq FPGA [3].

The supervisor CPU runs its own custom SW which provides system management and monitoring services through shared Ethernet connection such as Zynq UART forwarding over Ethernet (Telnet), Zynq programming via Joint Test Action Group (JTAG) over Ethernet, Zynq/FPGA and FMC card power-cycling watchdog, remote reset/power cycle of the whole FPGAIOC system over Ethernet (using supervisor console commands over Telnet), remote monitoring of FPGAIOC system parameters such as supply voltages, temperature, up-time and watchdog reset counts over Ethernet (via supervisor console interface) [3].

3 FPGA selection

As the FPGA SoC is the main processing unit for the unit under development and needs to fulfil certain requirements set by the ESS, the selection of the FPGA is made first, followed by designing other hardware elements. Main requirements for the FPGA can be seen from the list below [3]:

- FPGAIOC may use low or moderate speed CPU (e.g 667MHz)
- FPGAIOC should have minimum 1GB NAND, NOR or eMMC Memory for Linux
- FPGAIOC FPGA should have multi-gigabit (up to 3.125GBit/s) transceivers
- FPGAIOC should have minimum 512 MB of RAM for Linux and SW execution
- Module size under 120 mm x 120mm

First task was to research the market in order to gather information to select the suitable SoC solutions for the FPGAIOC. Xilinx Zynq portfolio was chosen by the ESS to proceed with the SoC selection. However, exact platform was to be decided according to the requirements, cost and availability. As the quantities for the to be produced FPGAIOCs are in hundreds not in thousands, it was cost efficient to choose off the shelf FPGA development boards instead of developing the FPGA board from scratch.

The FPGA development boards also have already implemented RAM and other hardware elements needed for the FPGAIOC development. Therefore, developing hardware for SoC would have been more time consuming and expensive, therefore not fitting into time plan or project budget. List of possible Xilinx modules can be seen from the Table 1 below [5] [6] [7] [8] [9] [10].

Table 1. Selection of available Xilinx SoC modules

Module	Zynq	IO	GTX	CPU	Memory	Flash	Price (€)
PicoZed	XC7Z010 XC7Z020 XC7Z015 XC7Z030	113 148 138 148	- - - 4	Dual-core A9	1 GB DDR3	128 MB QSPI 4GB eMMC	191 234 241 331
TE0720	7020	152	-	Dual-core A9	1 GB DDR3	32 MB SPI flash 4 GB NAND	269

Mars ZX3	7020	108	-	Dual-core A9	1 GB DDR3	512 MB NAND 16 MB SPI	198
Mars XU3	Ultrascale+	108	-	ARM Quad-core A53 + Dual-core R5 + Mali-400MP2 GPU	4 GB DDR4	16 GB eMMC 64MB QSPI	195
Mercury ZX1	7030 series	150	4	ARM Dual-core A9	1GB DDR3	512 MB NAND 64 MB SPI	387
Mercury ZX5	7015/7030	146	4	ARM Dual-core A9	1 GB DDR3	512 MB NAND 64 MB SPI	259/293
Mercury+XU1	Ultrascale+	294	16	ARM Quad-core A53 + Dual-core R5 + Mali-400MP2 GPU	8 GB DDR4 ECC	16 GB eMMC 64 MB SPI	1262
Mercury XU5	Ultrascale+	178	8	ARM Quad-core A53 + Dual-core R5 + Mali-400MP2 GPU	2 GB DDR4	16 GB eMMC 64 MB SPI	340
MYC-C7Z020	7020	124	-	ARM Dual-core A9	1 GB DDR3	4 GB eMMC 32 MB SPI	152
MYC-C7Z015	7015	132	4 (6.25GBit)	ARM Dual-core A9	1 GB DDR3	4 GB eMMC 32 MB SPI	174
TE0715-04-30-1I3	7030	132	4	ARM Dual-core A9	1 GB DDR3	32 MP QSPI	299
TE0715-04-15-1I	7015	132	4 (6.25GBit)	ARM Dual-core A9	1 GB DDR3	32 MP QSPI	225
KRM-3Z7030	7030	192	4	ARM Dual-core A9	1GB LPDDR3 256 MB LPDDR3	256 MB QSPI	284

After analysing each module, it was clear that only few of them would fit into the given dimensions by the ESS [3]. Furthermore, not all modules were actually immediately available for developing purposes. Modules which would fulfil project needs and fit into the enclosure are marked with green in the Table 1. After several discussions with ESS, it was confirmed that PicoZed XC7Z030 SoM is the most suitable candidate for this application [11].

4 Hardware design

Haven chosen the suitable SoC solution for the project, additional hardware development could begin according to the electrical requirements from the technical specification document [3]. Furthermore, ESS required to have a separate CPU for the FPGAIOC, running its custom software which provides system management and monitoring services. The supervisor CPU has to independent of Zynq SoC and have an independent UART and Ethernet connectivity. As the requirements for the ESS hardware applications are very project specific, the carrier card for the SoC had to be built from scratch and could not be bought from the mass market. All schematics were designed using commercial software Altium Designer.

4.1 SVC

The supervisor CPU needs to perform initial system bring-up and monitoring. Even though the PicoZed already integrates ARM based microcontroller, it is not enough to fulfil the project requirements because it has limited amount peripherals and IO-s available. Furthermore, these IO-s are needed for FPGA related developments. As the SoC already contains ARM based MCU and software developers have extensive experience with the mentioned platform, it is reasonable to use ARM based MCU for controlling supervisory circuits of other hardware elements as well [3].

Many vendors offer ARM based microcontrollers. Considering different project needs, cost, availability, development tools and experience, STMicroelectronics was chosen as a vendor.

The MCU had to fulfil many requirements and have peripherals, such as: Ethernet, SPI, at least 2 UART, 3 I2C channels and enough available IO-s according to the technical specification document [3]. Most suitable candidate considering price and availability was the STM32F407VGT7 microcontroller. It has a 100 LQFP package which provides enough IO-s and functionality. The pinout of the STM32F407xx can be seen from the Figure 3 below [12].

One of the most important features regarding the SVC is the Ethernet connectivity, as stated in the technical specification [3]. A 50MHz clock is needed to drive the RMII

circuitry. Furthermore, the clock should have a 25ppm or better reference. Instead of a conventional crystal oscillator, a microelectromechanical system (MEMS) is used. MEMS was chosen as they are easier to integrate into the circuit design and are more reliable in general [13]. For example, MEMS does not need external load capacitors.

Furthermore, a 32.768 kHz crystal is connected to the microcontroller OSC32 inputs in order to use real time clock [12]. The crystal load capacitance is 6pF. Load capacitor values are calculated according to the equation 1. The C is the capacitance of both load capacitors and C_{stray} is estimated stray capacitance of the trace.

$$\mathrm{CL} = 2\left(C_{Load} - C_{Stray}\right) = 2(6\mathrm{pF} - 5\mathrm{pF}) = 2\ \mathrm{pF} \quad (1)$$

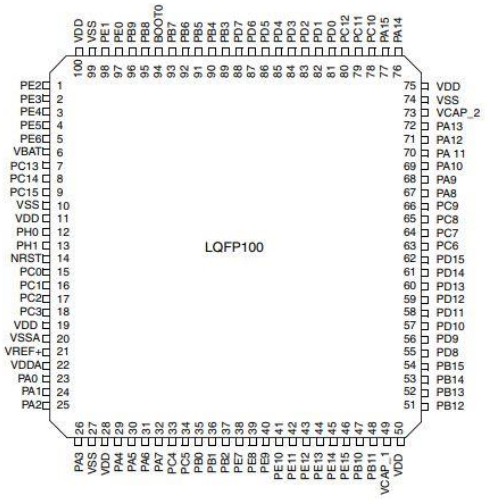

Figure 3. STM32F407xx pinout

4.2 Designing the RS-232 interface

After selection of the supervisory CPU (SVC), other hardware schematics could be designed. RS-232 interface is an important feature for the FPGAIOC module [14]. It improves the reliability and manageability of the FPGAIOC equipment on field. The RS-232 architecture is quite sophisticated and its overall structure can be seen from the Figure 4 below [3].

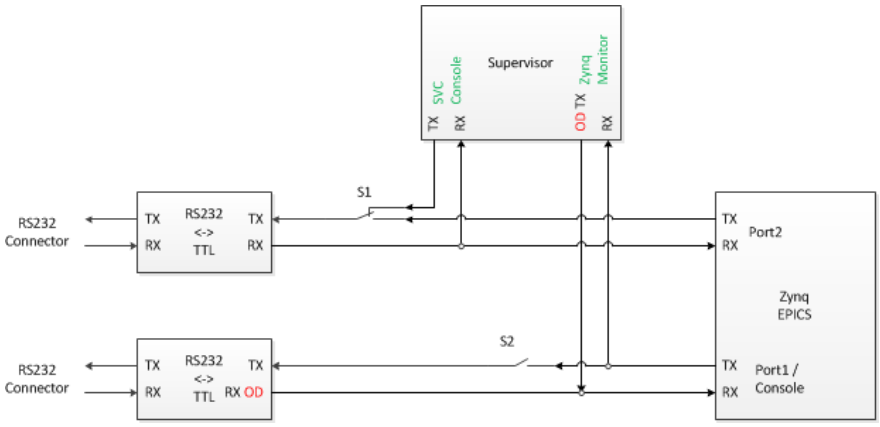

Figure 4. RS-232 architecture

There are 2 different RS-232 channels. One is meant for supervisor CPU, where client can navigate through the menu items (console commands) and can change parameters, see current status, perform actions and update firmware. Second RS-232 interface is meant for Zynq uBoot and Linux console. When Zynq console UART (Port 2) is in slave mode, SVC shall monitor Zynq console UART TxD connection and be capable of driving the RxD line at any time.

Furthermore, FPGAIOC should include circuitry to switch SVC console interface into master mode. In addition, it has to be possible to disable Zynq console serial (Port 1) TX line during Zynq boot process [3]. Disabling the Zynq console serial TX line during Zynq boot process is needed to prevent false data transmission to the RS-232 port. There are multiple ways to disable the TX line during boot process. FPGA or SVC should be able to independently enable the port after the boot process. Furthermore, when one of the devices has already enabled the port, it should not be possible to disable the TX port. As UART (TTL) logic high “1” represents no activity, the TX port could be disabled with FPGA or SVC enable signal. Enable signals are then used as NOR gate inputs, which prevents disabling the port when SVC or FPGA has already enabled it. NOR output and Zynq UART TX port are then OR-d together. The block diagram for this solution can be seen from the Figure 5 below. R1 pull-down resistor is mandatory to prevent unknown state of the Zynq TX enable signal if the FPGA has not been programmed. In this solution R1 is not needed as the OR gate output is high by default. R2 pull-down is not mandatory because after the reset SVC can immediately control this output.

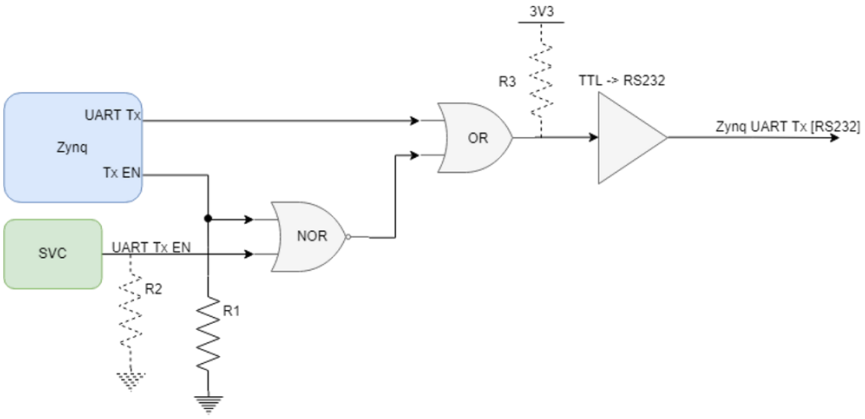

Figure 5. Enabling or disabling the Zynq TX line with logic gates

The other solution uses analog switch instead of the OR gate and NOR gate is replaced with OR gate. Either FPGA or SVC could then enable the switch. In this case, R3 is needed to guarantee logic high on TX line in default state. The block diagram can be seen from the Figure 6 below. This solution is preferred as it uses simpler logic.

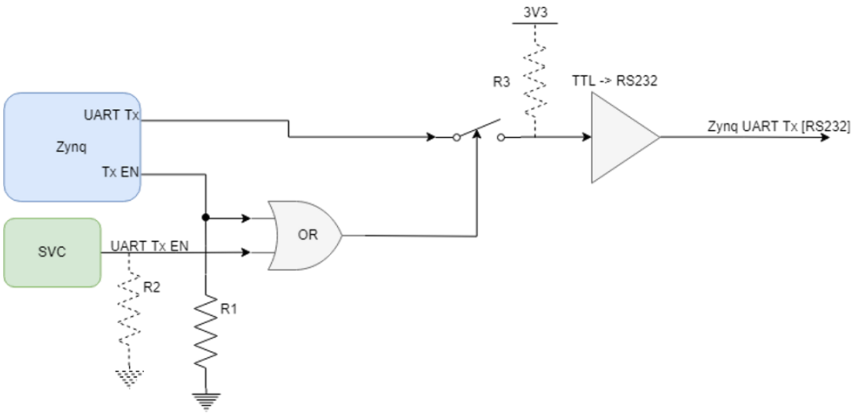

Figure 6. Enabling or disabling the Zynq TX line with analog switch

According to the FPGAIOC technical specification, the RS-232 interface needs to have 2 RJ45 sockets without embedded LED indicators on front panel. The connectors have to follow layouts, which can be seen from the Figure 7 below. RJ45 connectors are provided on FPGAIOC to maintain maximum compatibility with ESS other similar hardware [3].

Pin	RS-232
1	
2	
3	GND
4	TxD
5	RxD
6	
7	
8	

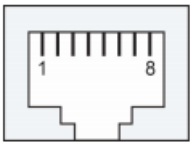

Figure 7. RS-232 RJ45 connector layout

In order to make RS-232 protocol readable for Zynq and SVC, a transceiver, which will convert RS-232 signals to universal asynchronous receiver-transmitter (UART) format, is needed [15]. The RS-232 protocol signals voltages are with respect to the common ground (GND). As the RS-232 cables will connect multiple parts of the hardware in different locations together, the grounds have to be isolated in order to exclude ground loop problems [16].

This will add even more complexity to the selection of suitable integrated circuits dedicated for RS-232 to UART and reverse signal translations. Regarding cost, availability and requirements, Maxim Integrated MAX3250 transceiver was chosen.

As the Zynq CPU IO-s operate with 1.8V volts and MAX3250 has 3.3V output logic, a voltage translation is needed between Zynq and transceiver. This is done with Texas Instruments 4-Bit Bidirectional Voltage-level Translator TXB0104 IC. Chip is widely available and a low cost solution. Signal switching logic is done with Texas Instruments portfolio IC-s, such as SN74LVC. MAX3250 and TXB0104 schematics can be seen from Figure 8 and Figure 9 accordingly.

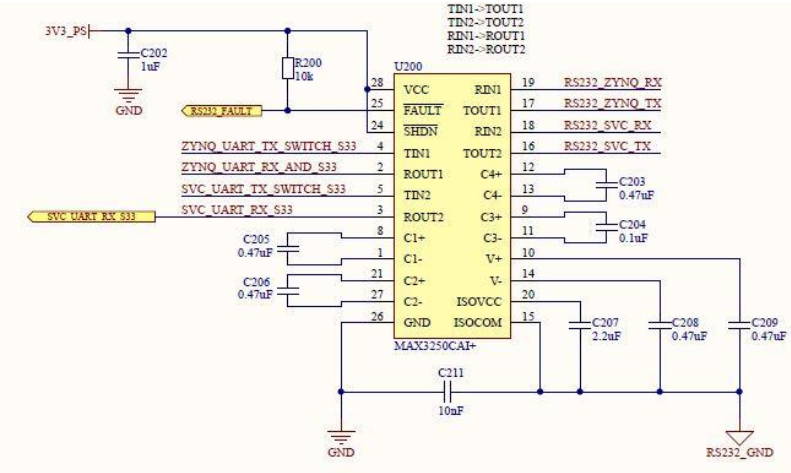

Figure 8. MAX3250 schematic

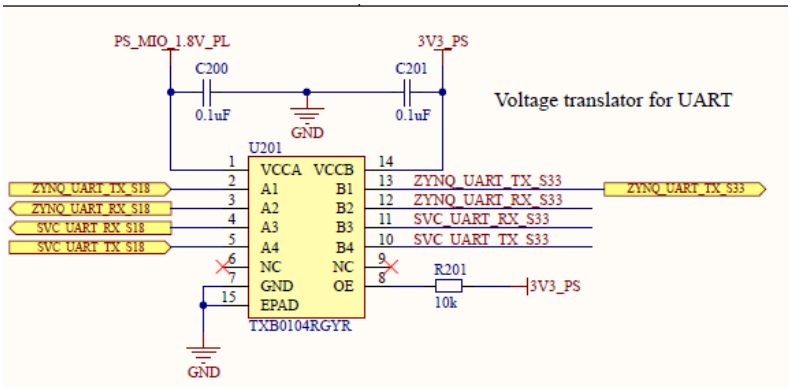

Figure 9. TXB0104 voltage translation

4.3 Ethernet

The FPGAIOC shall be remotely manageable over the Ethernet connection. For example, it is used to restart, power cycle or provide software updates for the unit. According to the FPGAIOC technical specification, the Ethernet should have one RJ45 connector with support for 100 Mbit/s, 10/100 BASE-TX interface [3]. In Ethernet protocol, data is transferred to the FPGAIOC by physical layer according to the OSI model [17] [18]. As there is only one Ethernet port available and both SVC and Zynq need to access Ethernet at the same time, there needs to be some kind of Ethernet switch.

In order to convert the analog signals to digital bits, an Ethernet PHY is needed [19]. However, the digital signals cannot be processed by PHY. This is done by a medium access control (MAC) in data link layer according to the OSI model [20].

According to the datasheets of the PicoZed FPGA, it already has PHY and MAC on board [11]. Furthermore, the SVC also implements MAC on chip [12]. To connect all three interfaces together, at least three-port switch with 10/100 BASE-TX capability is needed. Regarding availability, price and functionality, Microchip KSZ8463 Ethernet controller was chosen.

This IC provides 2 channel medium dependent interface crossover (MDIX) as well MII/RMII connectivity [21]. The RMII interface is used to connect switch to the SVC MAC [22]. Other two MDIX ports are used to connect Ethernet switch to the RJ45 connector and Zynq FPGA accordingly. Schematics regarding connectivity can be seen from Figure 10 and Figure 11.

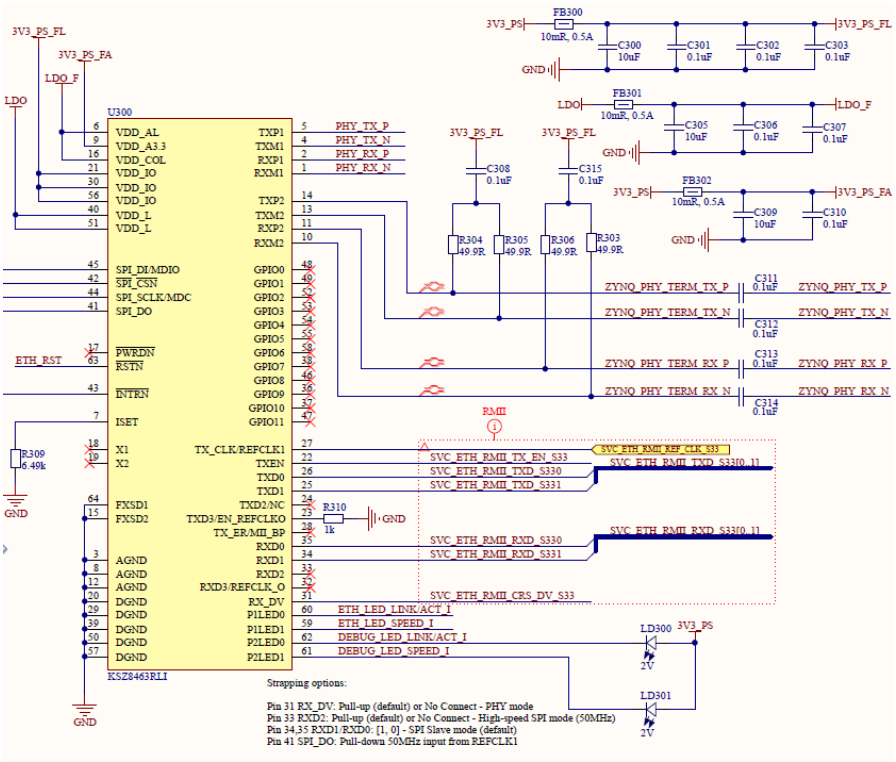

Figure 10. KSZ8463 schematics

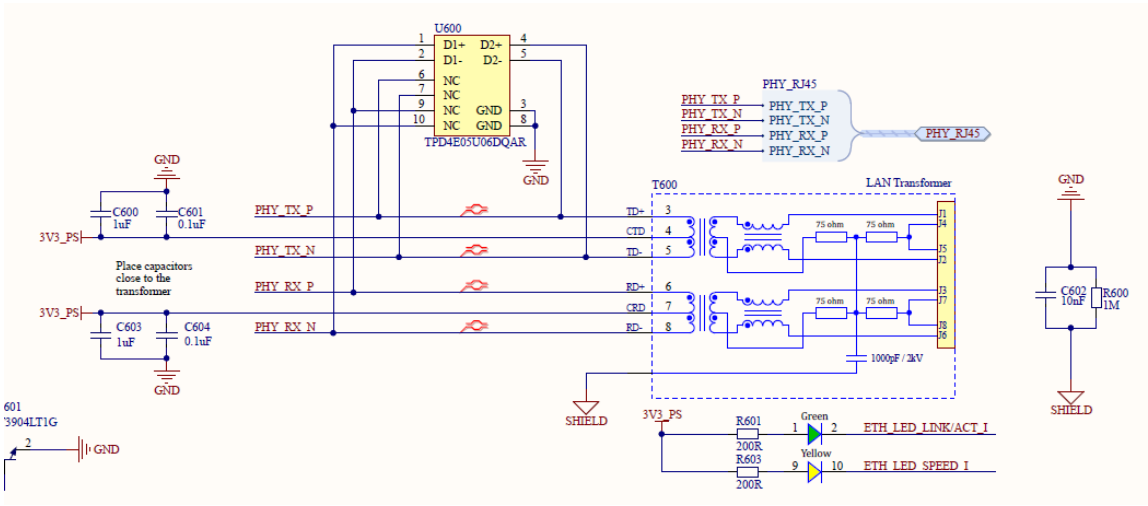

Figure 11. RJ45 schematics

The AC coupling and terminating of the MDI lines are done according to the application notes, which cover the Ethernet connectivity with and without magnetics [23] [24]. RJ45 connector is chosen with integrated magnetics suitable for 10/100 BASE-TX transmission in order to save board space and the MDI lines are also protected against ESD and transients with U600 unidirectional Transient Voltage Suppressor (TVS) based Electrostatic Discharge (ESD) protection diodes [25].

4.4 Clock synthesizers

FPGA IOC needs a programmable clock synthesizer and multiplexer in order to drive reference clock to Zynq transceivers dedicated for Event Receiver (EVR) and high speed communications.

According to the FPGA IOC technical specification, Si5346 IC was chosen for this solution in discussion with ESS [3]. Furthermore, to support EVR legacy clocking scheme as a back-up solution, a SY87739L based reference clock generator shall be designed. SY87739 has proven to be reliable in previous solutions [3].

As the FPGA IOC also supports FPGA FMC Low Pin Count (LPC) expansion modules, FMC gigabit data signals reference clock GBTCLK0 is connected to the Si5346 input in order to provide clock synchronization for FMC gigabit data signals [26]. The SY87738L and Si5346 outputs are connected together in a fashion with 0R resistors that only one IC output is active at once.

4.4.1 SY87739

The SY87739L back-up solution can generate exactly the correct frequency for transport protocols. In order to do that, it needs reference clock input frequency source, which has to follow positive emitter-coupled logic (PECL).

PECL is differential-signalling system that is mainly used in high-speed and clock-distribution circuits [27]. Specifically, Low Voltage PECL (LVPECL) is used, as it is designed for use with 3.3V or 2.5V supply. LVPECL offers the best jitter performance because of its large swing. However, the differential signal also needs to be terminated correctly. LVPECL output current is in 10mA range and this is derived from an open emitter, which requires a termination into resistive load to produce voltage.

AC coupling is used to filter out the DC bias. It is important to maintain the 50 Ω single-ended impedance on the traces. The schematic can be seen on the Figure 12. Resistors R413-R416 make the Thevenin equivalent termination and provide ~ 2V supply needed for the differential bus [28]. A 50 Ω single-ended and 100 Ω differential impedance is needed for these signals.

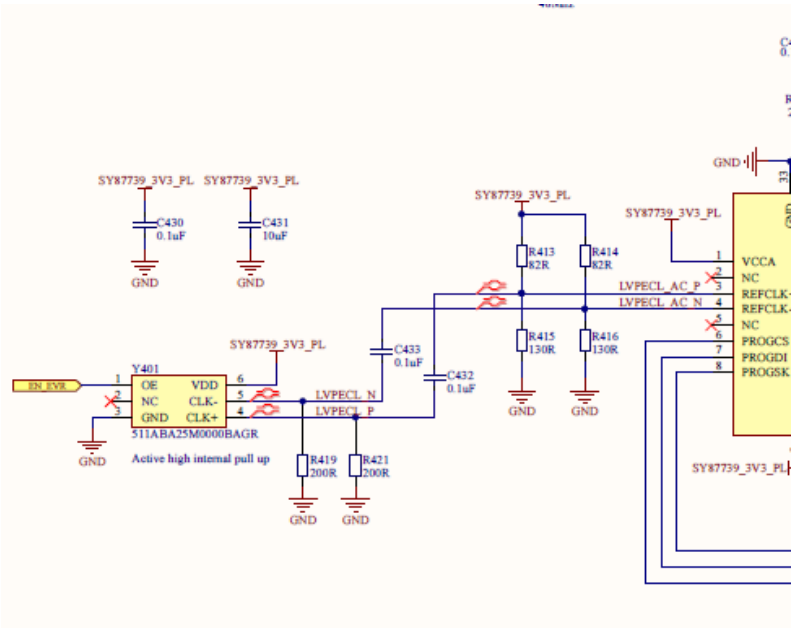

Figure 12. SY87739 LVPECL

4.4.2 Si5346

The Si5346 is the main clock synthesizer and multiplexer. It is responsible for synchronising and multiplexing clock to the FPGA. GBTCLK from the FMC is connected

to the Si5346 input. IC outputs CLKREF0, CLKREF1 and MRCC clocks. These clocks are used to drive EVR, COM and DP signals.

PicoZed has four gigabit full-duplex transceiver lanes that reside on Bank 112. EVR and COM signals are connected to this bank, as well FMC DP signals. The signalling standard is different for the Si5346 IC, using Low-Voltage Differential Signalling (LVDS).

LVDS is used as defined by the ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard [26]. As in case of LVPECL, LVDS also needs to have 50 Ω single-ended and 100 Ω differential impedance. DC component is once again removed from the signal with AC coupling, while the AC component is passed on.

Special attention is given to the outputs frequency accuracy, which is entirely dependent on the frequency accuracy of the external crystal reference clock. Any drift of the crystal frequency will be tracked at the output clock frequencies. A 48MHz crystal is chosen as suggested in the datasheet. Loading capacitors are not needed, as they are integrated into the device [29].

100 Ω split termination is used after the AC coupling capacitors in order to terminate the signal. The IC can be configured and controlled through the I2C interface. The schematics can be seen from the Figure 13 below. Schematics are designed according to the datasheet of the device [29].

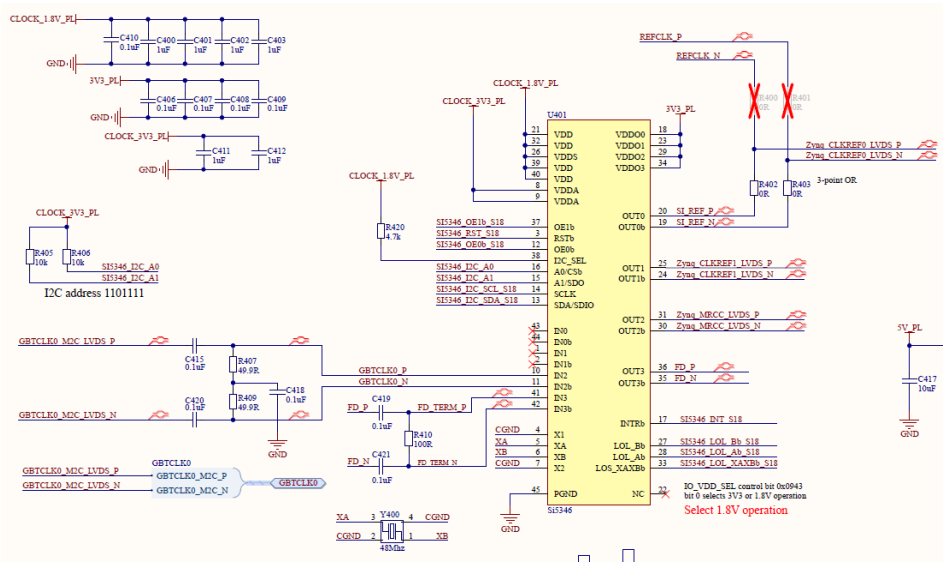

Figure 13. Si5346 schematics

4.5 SFP cage

SFP's are small optical module transceivers, which are hot pluggable [30]. The timing receiver connects to the ESS facility timing system via optical fiber connections through the small form-factor pluggable (SFP) cage. One SFP cage is reserved for timing receiver transceiver module and the other is for high speed communication transceiver module. The SFP cage TXP/TXN and RXP/RXN connections are connected to the FPGA MGT transceiver [31]. Figure 14 shows the schematic diagram on the FPGAIOC board [3].

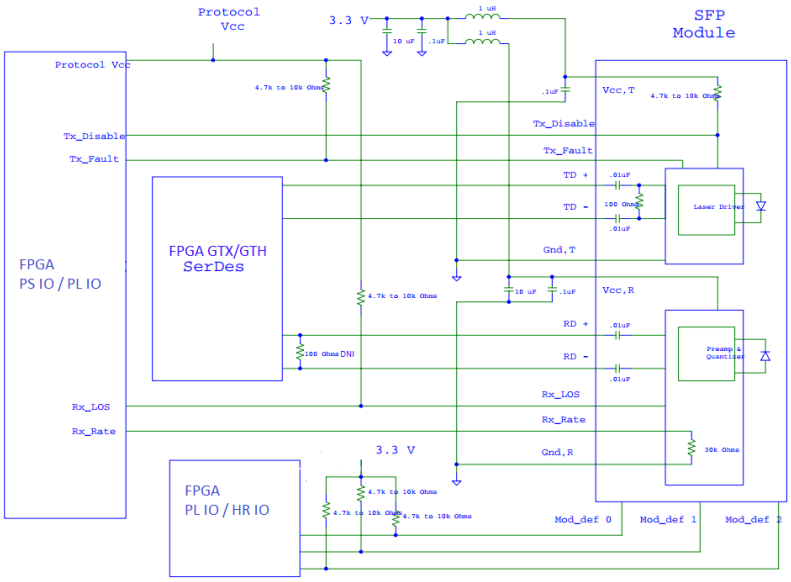

Figure 14. SFP+ module cage pin layout and numbering

4.6 I²C or SPI

There are many different integrated circuits on the boards, which many of need to be configured and monitored. This is mainly done with the I²C or SPI interface. However, as there are limited amount of channels available, different multiplexers and bus switches need to be used in order to achieve project goals.

SVC has 3 I²C channels available for communications, but one channel IO-s are used by the Ethernet interface. Second I2C channel is reserved for communication between the Zynq and SVC. For example, supervisor CPU shall notify the Zynq about any shut-down event and receive an acknowledge message from Zynq [3].

This leaves one I^2C channel for communication with other integrated circuits. Furthermore, some of the devices need to controlled by the SVC, as well by the FPGA. From the Figure 15 below, the block schematic for the whole system I2C/SPI can be seen.

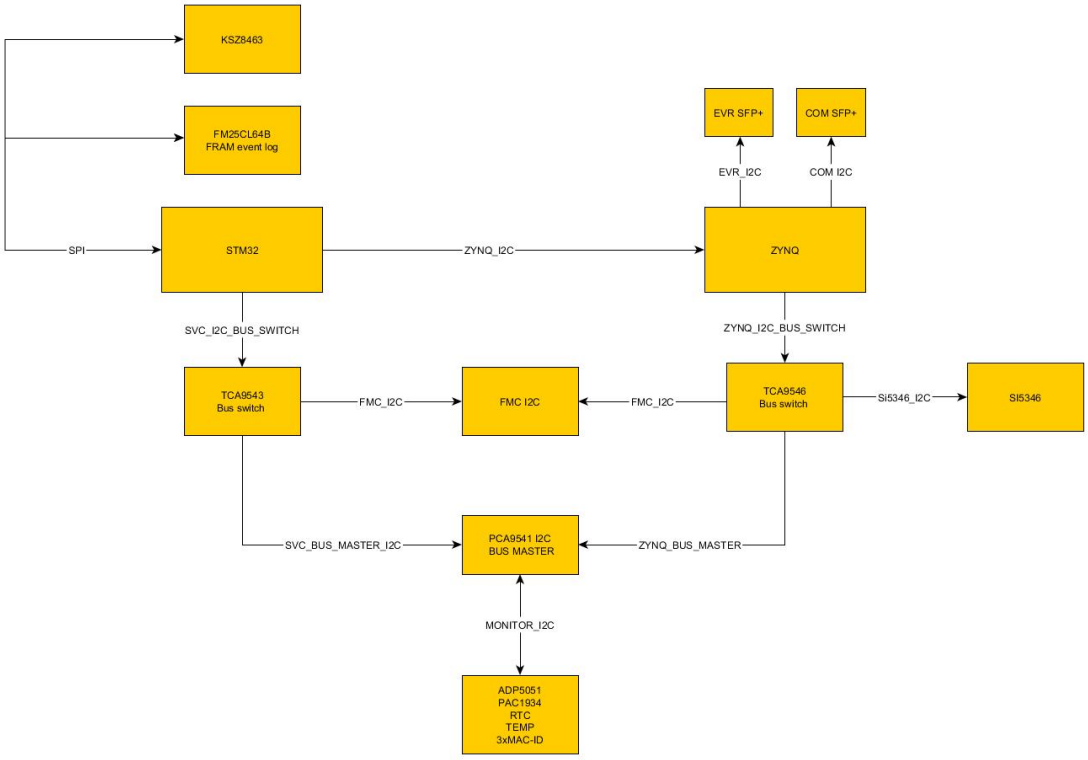

Figure 15. I2C and SPI block diagram

As can be seen from the figure, the communication architecture is built in a way that SVC uses SPI for Ethernet IC and event log memory, which do not need to be accessed by the FPGA.

Furthermore, KSZ8463 only supports SPI interface [21]. All the other peripherals can be accessed and must be available for both: SVC and FPGA [3]. As there is only one I^2C channel available for the SVC to communicate with many other devices, a dual I^2C bus switch has to be used. Texas Instruments TCA9543 IC is suitable for this operation [32]. It was selected as Texas Instruments has a wide portfolio of bus switches, which are cheap and are readily available.

One of the switch slave channels is connected to the FMC card I^2C bus, as it is required by technical specification [3]. The other slave channel is connected to the another bus

master IC: PCA9541 [33]. This IC is a 2-to-1 I^2C bus master selector with interrupt logic and reset by the NXP. Once again, it was selected due to low cost and availability.

This device is designed for high-reliability dual master I^2C bus applications. Even when one master fails, the other will remain operational. It has one slave bus. Having 2 masters is important as the slave devices on this IC need to be available for both the SVC and the FPGA at any time moment.

PCA9541 slave bus is connected to various devices, such as MAC-ID memories, real time clock as well power monitoring devices. As in case with SVC, the FPGA also has limited amount of I^2C buses available in the PS domain, therefore a bus switch is used as well.

However, instead of using TCA9543, a TCA9546 is used, as the FPGA needs 3 slave buses instead of 2 [34]. One slave channel is connected to the FMC, second one is connected to the PCA9541 and the third slave bus is connected to the Si5346.

In addition, COM and EVR I^2C buses are connected to the PL domain of the FPGA, as required by the technical specification [3]. All I^2C channels need a pull-up in order to function properly. A 10kΩ resistors as a pull-up for the 3.3V and 4.7 kΩ resistors for 1.8V bus are used [35].

4.7 Power

All the components on the FPGA IOC system need power. In ESS, where FPGA IOC-s will be installed, a 24V bus is available for supplying different devices, therefore FPGA IOC is designed to have a 24V input. The power budget excel was put together for all IC-s on the FPGAIOC in order to map the overall power consumption, which turned out to be ~ 43W. This means that the FPGAIOC will draw up to 1.8A of current from the 24V input when running at full capacity.

The FPGA IOC has 2 different power domains: Programmable Logic (PL) and Processor System (PS). The PS domain is dedicated for the supervisor CPU and all the related peripherals and the PL domain is dedicated for powering the FMC card and Zynq SoC [3].

The SVC, which is part of the PS domain, is responsible for bringing up the PL domain and selecting the correct voltage levels within the PL domain [3].

All PS and PL domains are marked with the ending _PS or _PL accordingly in the schematics. From the Figure 16, the high level block schematic can be seen for the power domains [3]. Different power domain voltages can be seen from the Figure 17.

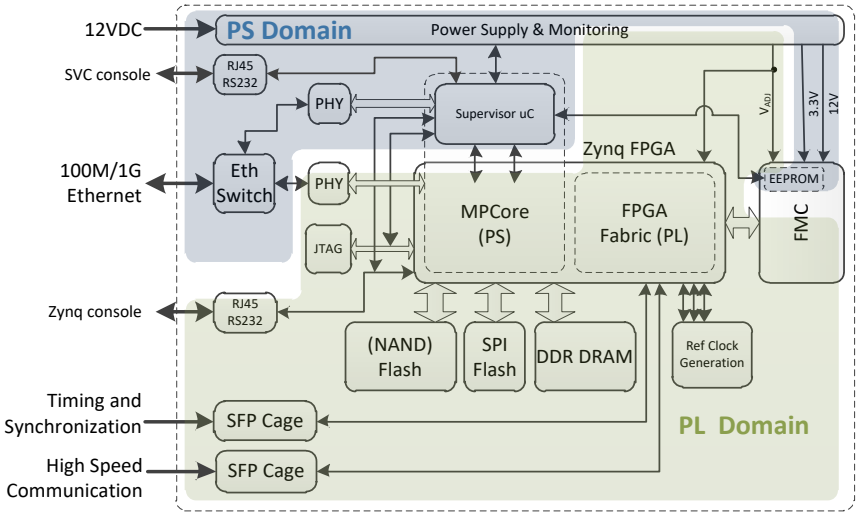

Figure 16. FPGA IOC power domains

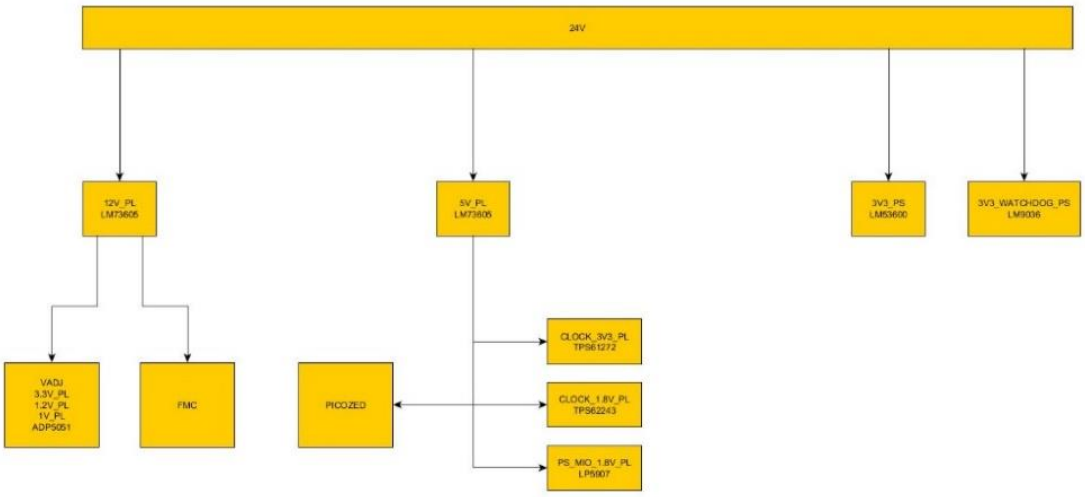

Figure 17. FPGA IOC power domain voltages

4.7.1 Input protection

The power input schematic of the FPGA IOC can be seen from the Figure 18.

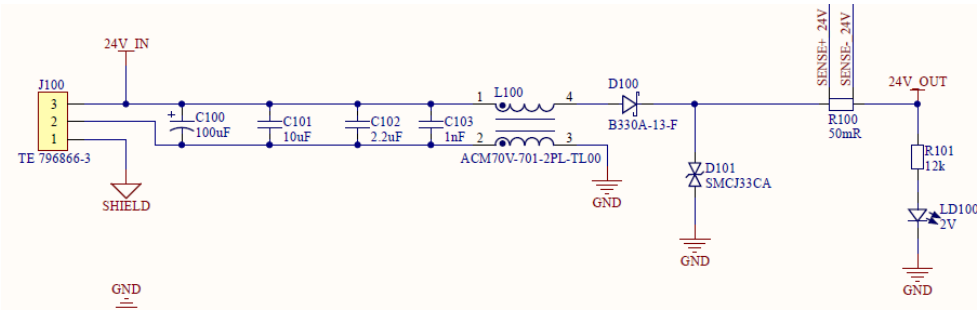

Figure 18. Input protection of the FPGA IOC power domains

Capacitors are used to prevent ripple currents and to smooth out DC bus voltage [36]. Capacitor values are chosen to decouple low as well high frequencies according to the good design practises [37].

Power line is also filtered with common mode choke (L100) [38], in order to cancel out flux, followed by a Schottky diode (D100) in order to protect against reverse voltage [39].

Schottky diode is used to minimize the voltage drop. Furthermore, TVS diode (D101) adds additional protection to the system by protecting against transient events over 33V [40]. There is also a voltage sense resistor and a green LED at the 24V output, which illuminates when voltage is applied to the input of the board.

4.7.2 PS Domain

The PS domain needs to be separated from the PL domain as the supervisor CPU needs to remain operational in the event of power supply failure in the PL domain, as well any fault in each domain should not propagate to the other [3].

The PS domain consists of two separate power rails, both 3.3V. One is dedicated for the watchdog circuit and the other for the rest of the PS domain IC-s, including the SVC.

4.7.2.1 Watchdog and its power supply

According to the FPGAIOC technical specification, the supervisor MCU should have an independent watchdog, which will reset the 3.3V_PS power domain [3]. This is needed when the SVC should hang or fail to operate normally.

The watchdog chosen to fulfil the requirements is Texas Instruments TPS3430Q. It is a standalone automotive rated window watchdog timer with programmable window and

reset delay [41]. It is relatively cheap, widely available and has a small footprint 10-VFDFN case. The watchdog schematics can be seen from the Figure 19 below.

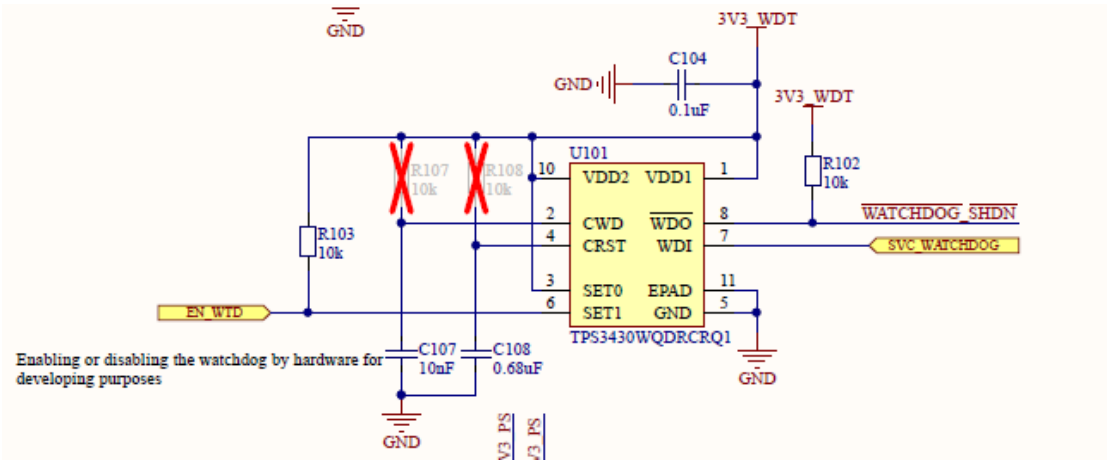

Figure 19. SVC watchdog

SVC_WATCHDOG is a signal input from the SVC. If the signal is not received in a specific time window, the watchdog will reset the 3.3V_PS domain, which will also reset all the other power domains. This excludes the situation where other power domains remain operational if the SVC is not responding.

CWD, CRST and SET0, SET1 pins determine the programmability of the device: such as watchdog timeout or window ratios. The passive component values are selected according to the datasheet of the device. The watchdog function can be turned off by pin SET1 (EN_WTD signal) with an external jumper for developing purposes [41].

The watchdog circuit has its own low-dropout regulator (LDO), because it must remain operational if something happens to PS SVC power rail [42]. LDO was chosen instead of the DC/DC converter, because watchdog circuit only draws maximum of 10 mA of current. LDO uses less board space as well and is cheaper compared to the DC/DC

regulator. TI LDO was chosen for this application, as it is AEQ-100 qualified, low cost and readily available. The schematic for the LM9036Q can be seen from Figure 20.

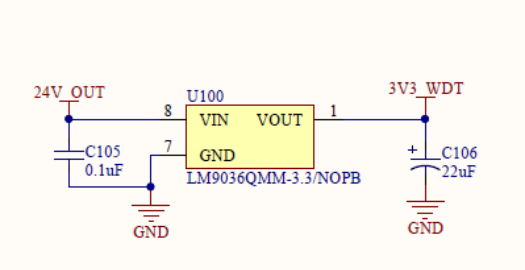

Figure 20. Watchdog power supply

Capacitors were chosen according to the datasheet of the device. Thermal calculations were done to validate that the LDO does not heat up over maximum operating temperature range. If the device outputs 10mA of maximum current and it has a voltage drop of almost 20V, the power loss could be calculated according to the power law formula, which can be seen from equation 2 [43].

$$P = (V_I - V_O) \times I_O = (24V - 3.3V) \times 10\,mA = 0.207W \quad (2)$$

Therefore, the device dissipates ~ 0.2W of power. According to the datasheet, the junction to ambient thermal resistance θ_{JA} is 200°C/W for the VSSOP-8 case. This means that the LDO's temperature will rise a maximum of 40°C, which will add to the ambient temperature of 25°C typically. 65°C will remain significantly lower than the maximum operating temperature of 125°C [44].

4.7.2.2 3V3_PS power supply

The maximum current draw in 3.3V_PS power domain is close to 0.4A. The power supply should also be able to support at least 24V input, have a power good output signal and enable pin. These parameters set the main specifications for the selection of the power supply.

As the current output is not small, a more efficient DC/DC converter has to be used instead of the LDO. The suitable candidate is Texas Instruments LM53600-Q1 automotive synchronous 2.1MHz step-down converter. It supports up to 36V input and provides 650mA of maximum current. Schematic can be seen from the Figure 21, which is designed according to the datasheet of the device [45].

The DC/DC converter has integrated MOSFETs, which reduces the costs as well board space needed for the layout. 2.1MHz switching speed allows to use small passive components.

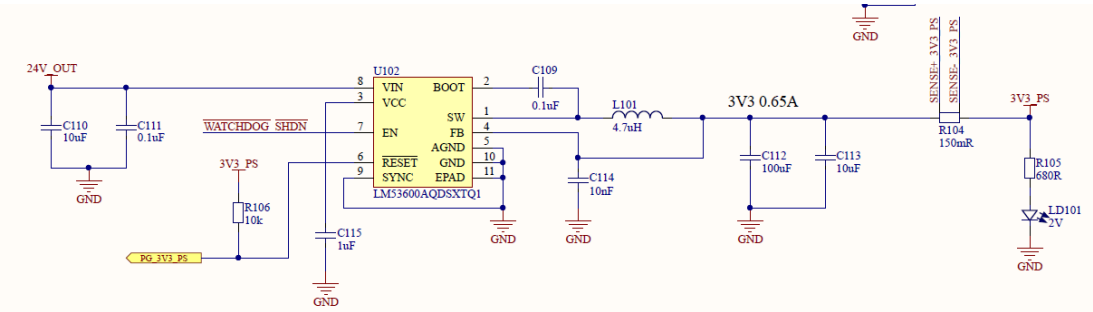

Figure 21. 3.3V_PS DC/DC converter

However, there are trade-offs in designing a high-frequency switching converter. The advantages are: smaller layout size (such as smaller inductor), faster transient response and a smaller voltage over and undershoots, but higher switching frequency has an impact on efficiency [46]. Current output is not very high and output voltage is low. Therefore, the generated heat is not a problem and benefits outweigh power efficiency aspect.

According to the TI WEBENCH tool, the regulator efficiency is 78%, which means that if it outputs 1.32W of power, the total power draw is 1.69W and therefore 0.37W of heat needs to be dissipated [47].

Junction to ambient thermal resistance can be acquired from the datasheet of the device, which is 46.2°C/W for the 10-WSON package. Therefore, the maximum temperature rise will be only 17°C over ambient temperature, which is well below maximum operating temperature of 150°C [45].

There is also a current sense resistor and a LED in the output of the converter to measure the current consumption and to show that there is a 3V3 PS domain voltage on board if the DC/DC is operational.

4.7.3 PL domain

The PL domain is dedicated to powering the FPGA and the FMC card. There are many different voltages in this domain, which can be seen from the Figure 17 described above.

4.7.3.1 5V_PL domain

The FPGA works from 5V input according to the PicoZed datasheet. PicoZed has multiple own different power supplies to power different parts on the board. The PicoZed maximum current draw is 2.1A [11].

Clock synthesizers are also part of the PL domain and work with 1.8V/3.3V inputs. They have their own power supplies. 5V_PL rail is also used to generate the PS_MIO_1.8V_PL domain. This means that the maximum overall 5V rail current consumption is around 2.5A. The 5V domain shall be also be independent and therefore shall be generated from 24V input [3].

Power supply should also have a PG (Power Good) [48] and enable signals in order to monitor and control the 5V_PL domain. As the current of the 5V rail is quite high, a DC/DC converter has to be used. The suitable DC/DC converter for this application is Texas Instruments LM73605-Q1 [49]. It is an automotive qualified synchronous step-down voltage converter and was chosen regarding the needs, availability and cost.

It implements many protection mechanisms needed for the application, such as: overcurrent, short-circuit protection and thermal protection. From the Figure 22 below, the schematic for the converter can be seen.

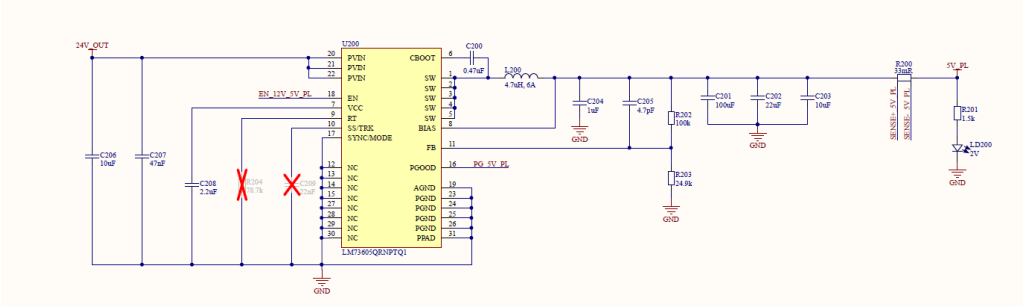

Figure 22. 5V_PL rail DC/DC converter

A 47nF capacitor is added to the input for filtering purposes. Schematics are designed according to the datasheet [37]. As the current is quite high, lower switching frequency of 500 kHz is used in order to decrease switching losses and increase efficiency.

However, the switching frequency can be changed mounting the R204 resistor on the schematic, which sets the converter frequency. The efficiency of the DC/DC converter setup is 92% [36]. Converter outputs 12.5W of power, which means of ~ 1W of heat

dissipation. The junction-to-ambient thermal resistance for the WQFN package is 34.3°C/W, which means the device will heat 34.3°C over ambient temperature (25°C).

Therefore, the device temperature at maximum current output will be ~ 60°C, which is well in operating range of -40 to 150°C [37]. As in case with other power supplies, a sense resistor and LED was added to the output of the device.

4.7.3.2 12V_PL domain

However, the FPGA needs other external voltages in addition to 5V to operate normally. The 12V_PL domain is mainly used to power the FMC card and it draws 1A of current [26].

This is done with a DC/DC converter ADP5051, which will be covered in the next chapter. ADP5051 supports to 5-15V inputs and therefore uses 12V_PL rail as an input. This makes overall 12V_PL domain to draw ~ 2.5A of current, which is the same range as with 5V_PL domain. In order to keep the BOM and schematics simple, same DC/DC converter was used as in case of 5V_PL domain. The schematic can be seen from the Figure 23.

The DC/DC converter was configured to output 12V instead of 5V with the feedback resistors R207 and R208 according to the datasheet [49]. Most of the schematic is same as in case with 5V rail, but there are few key changes that have to be made. For example, the inductor value and C211 bulk capacitor have been changed.

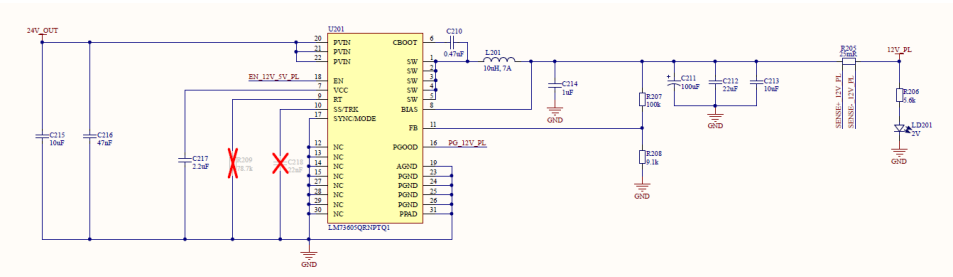

Figure 23. 12V_PL rail DC/DC converter

Inductor value is increased because the output power of the power supply is increased. Inductor value is calculated and selected according to the datasheet. The bulk capacitor has a quite large capacitance value and works at 12V, therefore it is reasonable to use aluminium electrolytic capacitor instead of a ceramic capacitor. The reason behind this is

that ceramic capacitors tend to lose capacitance when the application voltage rises and therefore tend to have low working voltages [50]. For example, 100uF rated capacitor used in 5V application only has 46uF of effective capacitance at working voltage [51].

4.7.3.3 ADP5051

PicoZed has a Zynq 7030 FPGA [11]. The PicoZed banks 13, 34 and 35 need external reference voltage in order to work properly. These voltages must be provided by the carrier card – FPGAIOC.

Bank 34 and 35 only support up to 1.8V inputs and bank 13 supports 3.3V inputs [11]. There are also 2 other supply voltages needed for GTX transceiver: MGTAVTT and MGTAVCC. MGTAVTT is used for GTX transmitter and receiver termination circuits and MGTAVCC is GTX transmitter and receiver circuit supply voltage.

They are 1.2V and 1.0V respectively [52]. In addition, FMC card has a VADJ flexible supply voltage to meet the requirements of a range of signalling standards, which voltages are used in FPGA banks as well [26]. According to the FPGAIOC technical specification, these VADJ voltages should be programmable in a range of 1.2V, 1.5V and 1.8V [3].

Furthermore, all other integrated circuits in the PL domain need a power supply and usually work with 3.3V. In total, 4 different voltage rails should be generated: VADJ, 3.3V_PL, 1.2V_MGTA and 1.0V_MGTA.

Generating each different voltage with a separate DC/DC converter is not optimal in this case, as it would increase BOM cost and would require a larger surface area for layout. Fortunately, there are DC/DC converters for purposes like supplying FPGA domains.

However, there are not many quad buck regulators available. Analog Devices ADP5051 is the most suitable candidate for this application. It supports voltage inputs from 4.5V to 15V and has 4 channels. Channels 1 and 2 are programmable to output 1.2A/2.5A/4A with low-side FET drivers and Channels 3 and 4 are fixed 1.2A sync buck regulators.

Each channel output can be separately enabled. ADP5051 also implements supervisory circuit and a voltage monitor with a watchdog function. It can be programmed over the I^2C bus [53]. As the 12V is readily available on board already for the FMC, it is used to supply ADP5051 as well. The whole ADP5051 schematic can be seen from the Figure 24 below. The schematics are designed based on the datasheet of the device [53].

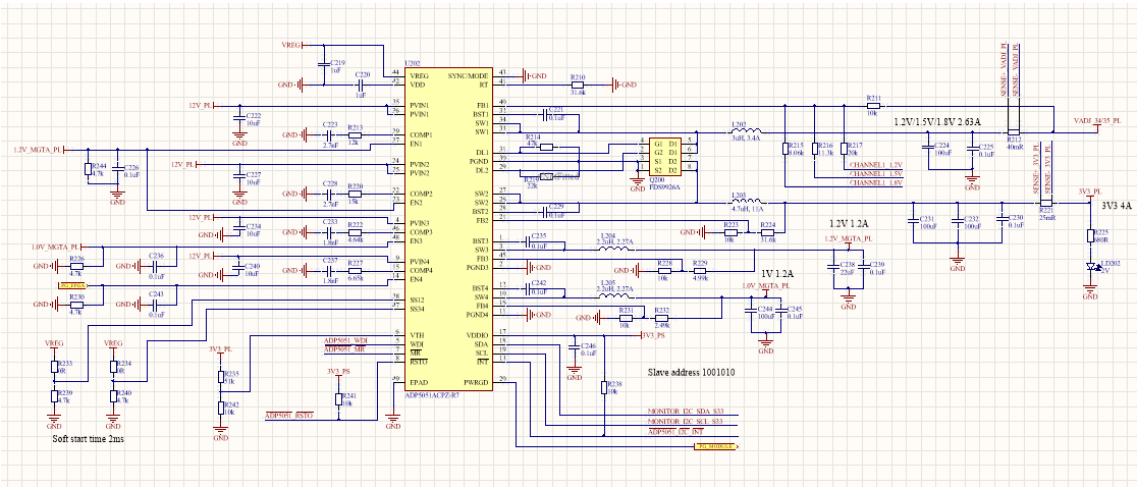

Figure 24. ADP5051 designed schematic

Design of the power supply cannot start before the switching frequency of the device has been selected. Connecting a resistor between pin 41 called RT and ground is dedicated for setting the device's switching frequency and can be calculated from the datasheet.

Frequency range of 250 kHz up to 1.4 MHz can be used. In this case, it was set to a default of 600 kHz with a resistor value of 31.6 kΩ, which achieves small enough footprint for the components and high efficiency for the converter.

Have set the frequency for the converter, design of the outputs could be started. The FB pin on each channel sets the channel output voltage which can be calculated using a formula from the datasheet [53].

Channel 3 and 4 were set to voltages 1.2V and 1.0V respectively. According to the Xilinx Zynq 7000 SoC, the 1.2V domain draws up to 0.5A and 1.0V up to 1A of current [52]. Inductor values are calculated using the equation from the ADP5051 datasheet under "Inductor selection" paragraph. Following the guidelines from the datasheet it can be calculated that suitable inductor for the Channels 3 and 4 should be a value of 10 uH and 4.7 uH respectively [53].

However, FPGA's typically have very low voltage tolerances and therefore ripple voltages, as well under- and overshoots should be taken into account. MGTAVTT and MGTAVCC only tolerates 30 mV of fluctuations [52]. Output capacitor plays crucial role

for these purposes and is chosen to be X5R 22uF ceramic capacitor for Channel 3 and 100uF for Channel 4 according to the requirements.

Using the AN-1144 application note from the Analog Devices, we could calculate the ripple peak to peak voltage for Channel 3 is only 1.8 mV and 3.6 mV for Channel 4 according to the second formula [54]. Inductor values could be therefore equalized in order to reduce cost and get better transient response and smaller footprint as the output voltage ripple could be increased.

Common 2.2uH inductor value was selected for both channels, thus increasing the output ripple to 7.3 mV on Channel 3 and 2 mV to Channel 4, which is still well below 30mV. Under- and overshoots can be calculated from the ADP5051 datasheet under "OUTPUT CAPACITOR SELECTION" paragraph [53].

Maximum undershoot is around 3mV and overshoot of 10mV for Channel 3. For Channel 4, maximum undershoot is 2mV and maximum overshoot of 20mV. Furthermore, a 0.1uF X7R capacitor is added to the outputs of the Channels 3 and 4 in order to additionally filter the noise from the supply.

Channel 2, which voltage is set to 3.3V, is needed to power the FMC card and PicoZed. FMC draws up to 3A of current and has to have a tolerance of 5%, which means that the under- and overshoots should not exceed 165mV [26]. In addition, the 3V3 domain is used to power any external 3.3_PL rail integrated circuits on FPGAIOC. The total current consumption is therefore estimated to be around 3.5A, which is in limits of the maximum output current capability [11] [26].

The DL2 pin enables to set the maximum peak current threshold for the Channels 1 and 2 with a resistor. This pin is left floating for the Channel 2, which sets the peak current limit to 4.4A according to the datasheet, but pads for resistors have been added nonetheless to provide larger peak currents if should be needed. [53].

The calculated inductor value is 3.3 uH, but once again another value of 4.7uH is selected in order to decrease the ripple voltages. Two 100uF capacitors are also added to the output which decrease the ripple voltages even more. As the effective capacitance is around

120uF and inductance is 4.7uH, it can be calculated that the ripple voltage for the 3V3_PL domain is 2.7 mV.

The worst case transient response event would be when the current would increase 0 to 3.5A. From these values the transient response under- and overshoots can be calculated from the ADP5051 datasheet [53]. With a 120uF of output capacitance, 4.7uH inductor and a load step of 3.5A it can be calculated that the under- and overshoot would be a maximum of 60mV and 140mV respectively, which is in tolerance of the system. Real life current draw however does not fluctuate between zero and maximum values and therefore under- and overshoots are smaller.

Channel 1 design is the most complicated. It is designed to fulfil VADJ requirements, which means that the output voltage has to be selectable between 1.2V, 1.5V and 1.8V. Before turning on the PL domain voltages, the SVC will read the memory of the FMC EEPROM and determine the FMC card VADJ voltage. User could then set the output voltage with the rotary switch. The rotary switch is connected to the multiple resistor networks as such that 3 different voltages can be manually set. In addition, if the switch is in “SVC” position, the SVC could control the output voltages. Each feedback resistor network has an output to the SVC so that the SVC could know which voltage is currently on Channel 1 output. Channel 1 inductor is calculated to be 3uH according to the datasheet [53]. This value suits for all named domain voltages. Channel 1 also has a voltage sense resistor connected to the output.

4.7.3.4 Current measurements

Having many different voltage levels and domains, it is important to monitor them. According to the FPGAIOC technical specification voltage levels and current consumption should be monitored by the supervisor CPU with 5% accuracy [3].

In total, 6 different important voltages are monitored: 24V, 12V, 5V, 3V3_PL, 3V3_PS and VADJ. In addition, 1.0V_MGTA and 1.2_MGTA domains can be monitored by the ADP5051. In order to keep the BOM simple and cost low, a power monitoring IC with many channels is needed. Microchip multi-channel DC power/energy monitor PAC1934 is cheap and suitable solution for monitoring the power domains. It implements High-Side 4 Channel current monitoring with 100mV full scale range and has 16 bits of

resolution, offering 1% of accuracy. It works with 3.3V and has a 16-UQFN Exposed Pad package [55].

The device is supplied from the 3.3V_PS domain because it needs to be operational even if other domains fail. As there are 6 channels to be monitored, 2 monitoring devices are needed. The communication between the SVC and PAC1934 is done through the I^2C bus. I^2C addresses are set according to the overall build-up of the whole I^2C architecture with the ADDRESEL pin.

Each monitoring device populates 3 measuring Channels and leaves one empty, giving an opportunity to add current measurement to additional domains, if that should be needed in the future. In order to measure the voltage and current of the desired power domain, a current sense resistor is needed. In order to calculate the needed R_{sense} value, a Full Scale voltage range and maximum current to measure is needed.

From the datasheet of the PAC1934 using the Equation 4-3, R_{sense} can be calculated for different voltage domains. Sense resistor is then added to the output of the calculated power domain and can be seen from previous Figures. The IC then senses the voltage drop on the resistor and calculates the current. Furthermore, knowing the bus voltage, power and energy could be calculated. This data is then processed by the SVC which can act according to the data. Schematics can be seen from the Figure 25 below. Components were selected according to the datasheet [55].

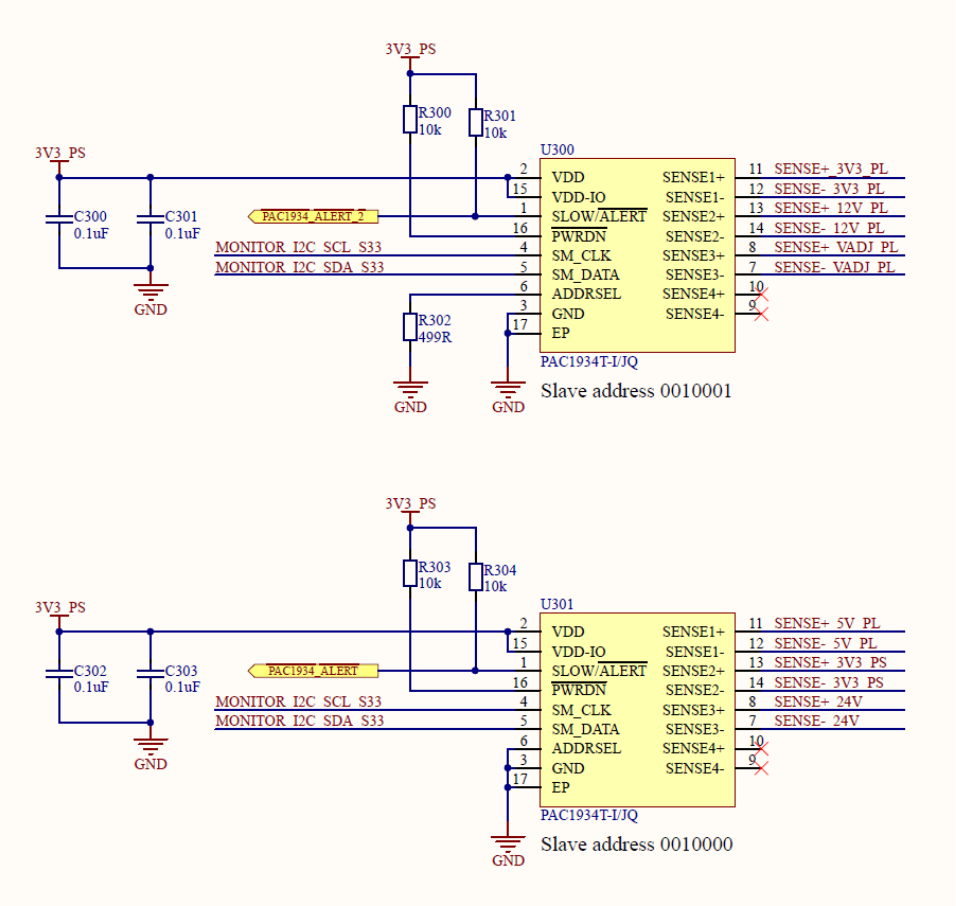

Figure 25. PAC1934 power monitoring schematics

4.8 Connectivity

The whole FPGAIOC needs to fit into the box with limited space. In total it consists of 4 different PCB boards. The 4 boards are all stacked up on each other. Counting from the bottom, these boards are: FMC, FPGAIOC power, FPGAIOC logic/peripherals and PicoZed SoM.

There are hundreds of high-speed and low-speed signals on the boards that all need to be connected. FMC and PicoZed boards are bought off the market. The self-designed boards need to transfer all these signals between different parts of the system. PicoZed has three 100 pin Amphenol high-speed receptacles connectors [11]. As it mounts on the top, the FPGAIOC logic board needs to have mating connectors to mount the PicoZed.

FMC, which is the lowest board, has a 160 low pin count connector [3]. All these signals need to reach the FPGA, which mounts on the top. Regarding all the other signals as well, it was clear that at least two 100 pin connectors are needed in between the FPGA and

FMC. To keep the BOM simple and cost low, the same 100 pin connectors were used between the power board and logic board and chosen according to the height requirements to the FPGAIOC. There are also 2 RJ-45 connectors for RS-232, 1 RJ-45 connector for Ethernet, double SFP+ cage and a power connector.

Furthermore, the FPGAIOC needs to be tested and programmed after it has been assembled. There are 2 different JTAG/SWD connectors for this purpose. IEEE 1149.1 JTAG is used, which implements daisy-chained topology [56]. JTAG architecture requirements for the FPGAIOC are complicated, as it needs to include SVC, FPGA and FMC all in one chain.

Even if the FMC card is not connected, the chain still needs to work by bypassing the FMC card. Furthermore, the supervisor CPU shall be capable of programming the Zynq FPGA via JTAG connection, when Xilinx Platform programmer is not attached. The FPGA should also be accessible over the Ethernet through SVC [3].

Following block schematic on Figure 26 was co-designed with Testonica to provide maximum flexibility in testing and programming of the FPGAIOC components.

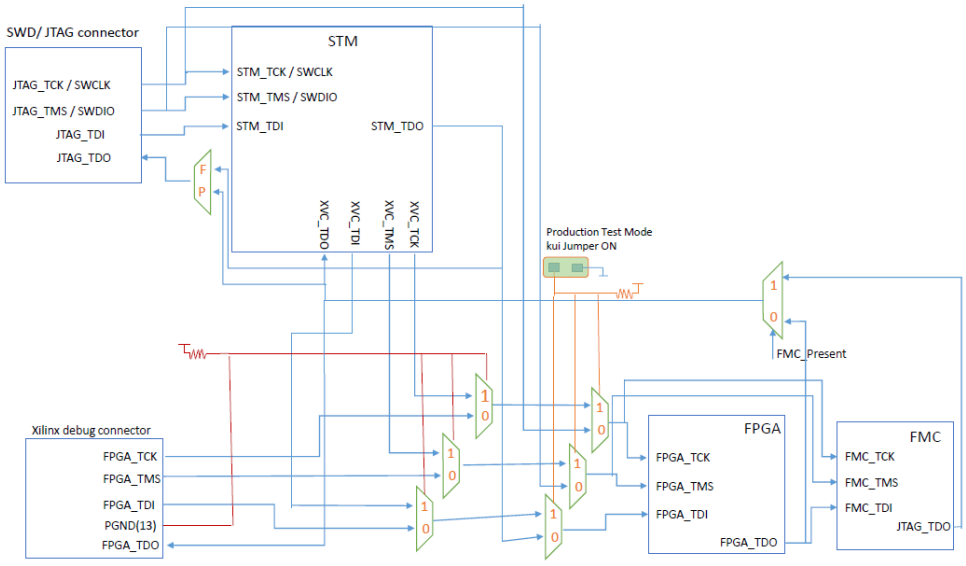

Figure 26. JTAG/SWD block schematic

There are 2 operational modes: functional and production test mode. Functional mode consists of 2 different settings: STM and FPGA-FMC. By default, in operational mode, STM is available through the SWD interface for the ST-LINK and FPGA/FMC are

controlled by the SVC through the XVC pins as can be seen from the Figure 26. If Xilinx debug connector cable is connected, then FPGA and FMC are only controlled by the debug connector, STM is still available separately through the SWD connector.

In order to put the FPGAIOC into production test mode, a jumper has to be put on the board which connects the whole board into one JTAG string STM-FPGA-FMC. Whole string is then controlled only through the SWD/JTAG connector. Two 4-channel multiplexers and one analog switch is used to realize this block schematic.

5 PCB layout

Haven designed the schematics, the Printed Circuit Board (PCB) layout could be designed. The layouts are designed in the Altium Designer software. Specifically, two printed circuit boards need to be designed in order to fit the whole construction to the FPGAIOC case. The boards need to fit to the 120mm x 120mm x 70mm enclosure [3]. This sets the overall dimension restrictions to the PCBs. Therefore, there are not many ways to fit the connectors inside of the case with the FMC card and its bezel. This sets the whole stack-up for the PCBs. Also, it is important to minimize the high-speed trace lengths. Furthermore, due to FMC board height limitations, one of the boards needs to be one-sided. Therefore, all digital logic with PicoZed SOM is placed on the top board. The middle PCB mounts most of the power supplies and provides FMC card routing to the PicoZed. The other side of the middle PCB is the FMC connector, where a FMC card can be inserted. Overall connector placement can be seen from the Figure 27 below. The PCB dimensions are 107.2mm by 110mm. 120mm x 120mm x 59mm aluminium casing is used for mounting the FPGAIOC.

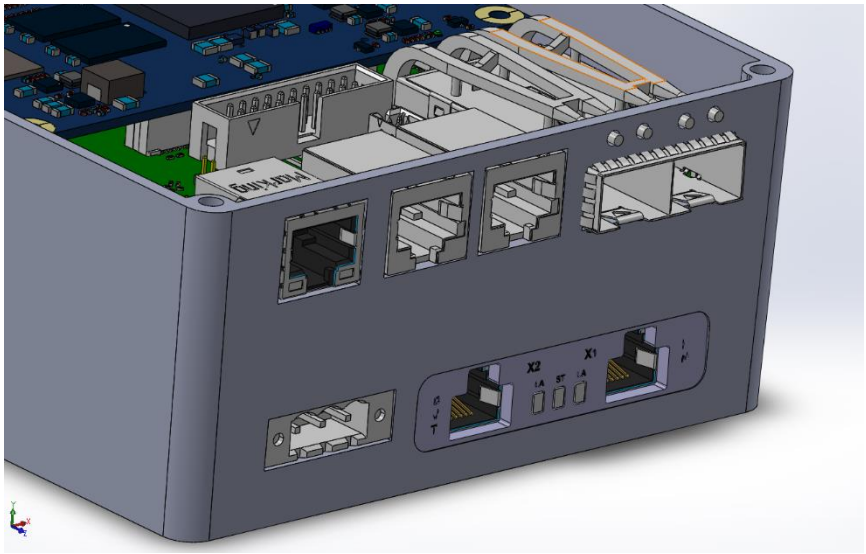

Figure 27. FPGAIOC connectors and PCB placement

5.1 Stack-up

The PCB design starts from selecting the suitable stack-up. As there are hundreds of signals on boards, the PCB-s are chosen to have 8 layers. There are multiple key objectives to be achieved when choosing a layer stack-up such as: a signal layer should

always be adjacent to a plane, signal layers should be tightly coupled to their adjacent planes, power and ground planes should be closely coupled together, high-speed signals should be routed on buried layers located between planes and multiple ground planes [57]. However, achieving all those objectives are not always possible and some compromises have to be made. The chosen layer stack can be seen from the Figure 28.

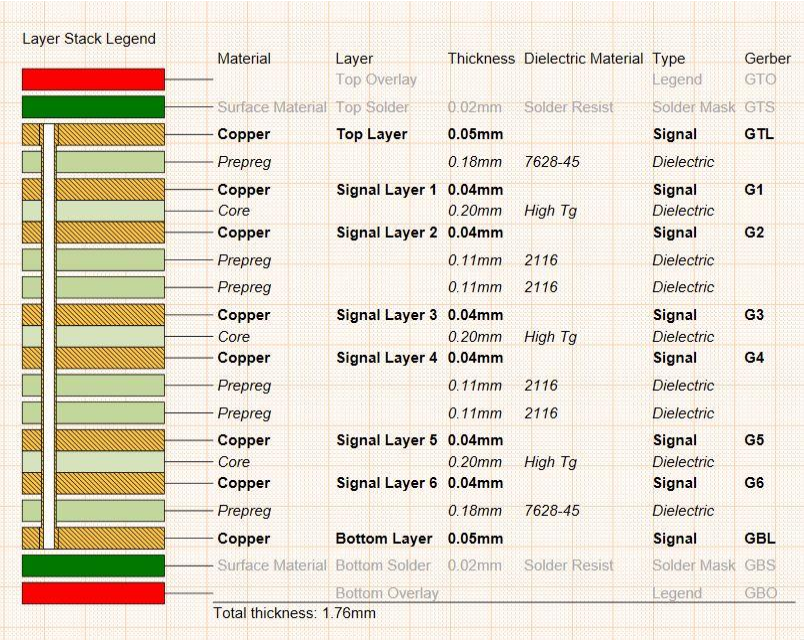

Figure 28. PCB layer stack-up

This build achieves all key objectives. The top and bottom layer are used to mount the components and route low speed signals. Signal layers 1, 4 and 6 are ground planes and are used to provide adjacent plane for signals. These layers are also stitched together to reduce the ground impedance. Signal layer 2 and 5 are used to route high speed signals. Signal layer 3 is used for providing power to the board.

5.2 FPGAIOC-2

This board is dedicated for data processing applications and is located at the top of the assembly. It mounts SFP, RS-232, RJ-45 as well JTAG/SWD connectors. It is double sided and mounts following IC-s: Ethernet controller, SVC, RS-232, memory, voltage translators and clock synthesizers. Many of these integrated circuits require impedance controlled routing. There are 2 routing technics available for the high speed signals: microstrip and stripline [58] [59]. This board mainly used stripline as the high speed signals are routed in the middle layers of the PCB to provide adequate shielding. Saturn

PCB design tool is used to calculate all trace widths and distances required to achieve specific impedance goals. Pair matching and length tuning is also important and MGT signals should be routed within 2.54mm shortest pair to longest pair. All gigabit transceiver signals within a single pair need to be within 0.6mm of each other [60]. The FPGA_IOC-2 top and bottom assembly can be seen from the following Figure 29 and Figure 30.

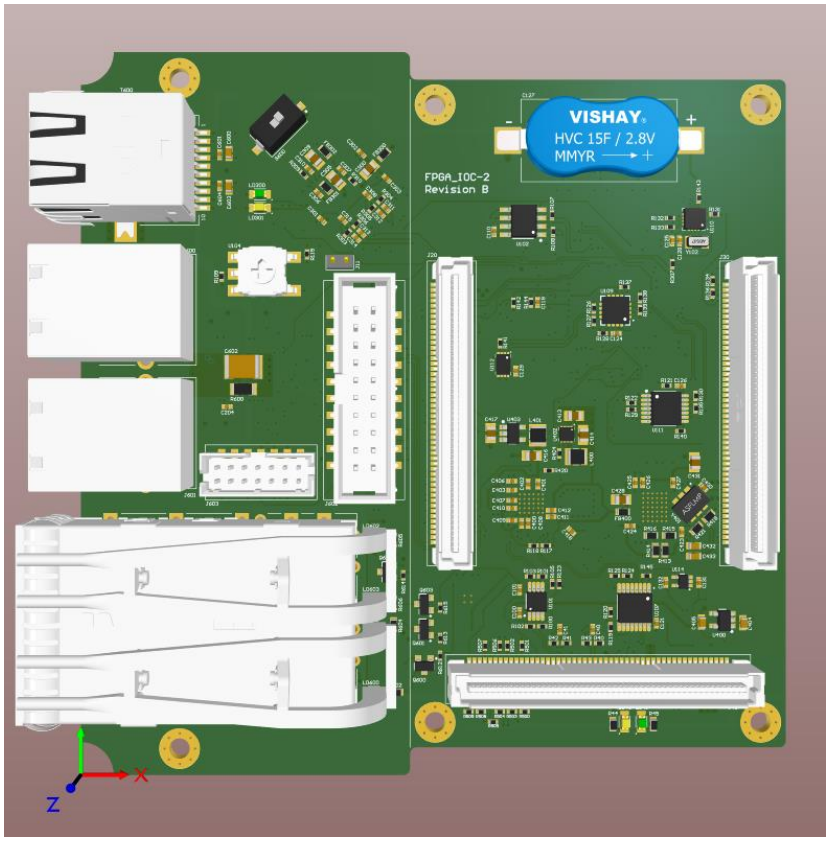

Figure 29. FPGAIOC-2 Top Assembly

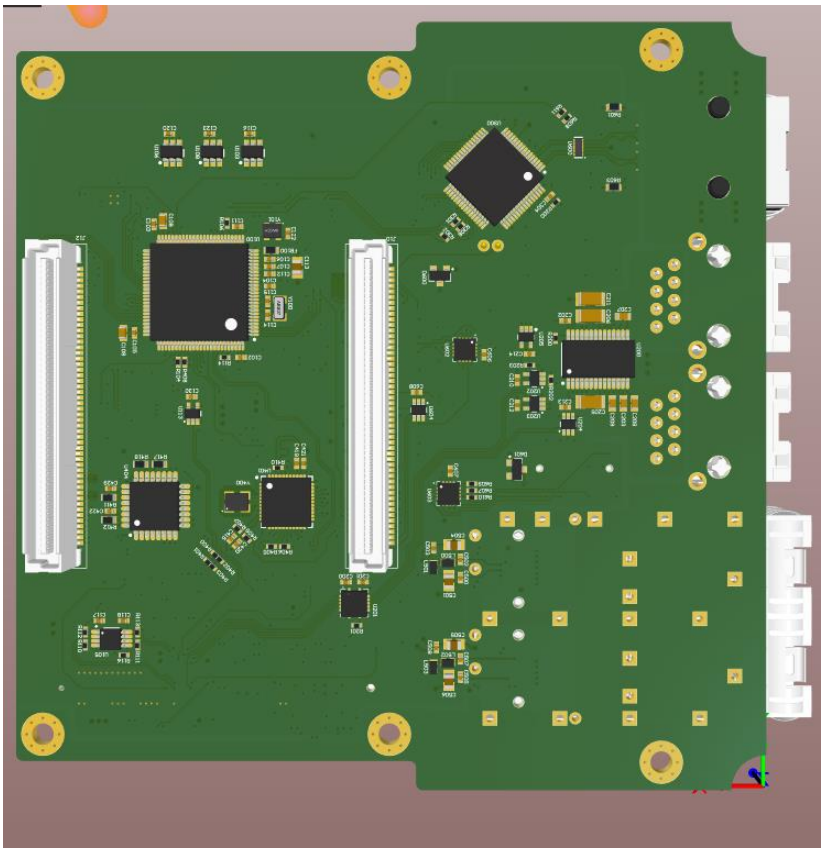

Figure 30. FPGAIOC-2 Bottom Assembly

5.3 FPGAIOC-1

The board is dedicated for the power supplies and routing of the FMC signals to the FPGA. On the top layer, all power supplies with power monitors are mounted. Bottom side mounts FMC connector. All FMC connector signals are routed through the board to the FPGAIOC-2 and PicoZed SOM. As in case with FPGAIOC-2, many differential signals are routed stripline but some of the signals are routed as microstrip in order to maintain length matching between signals. Saturn PCB tool is used to calculate trace widths. Top and bottom assembly can be seen from the Figure 31 and Figure 32 below.

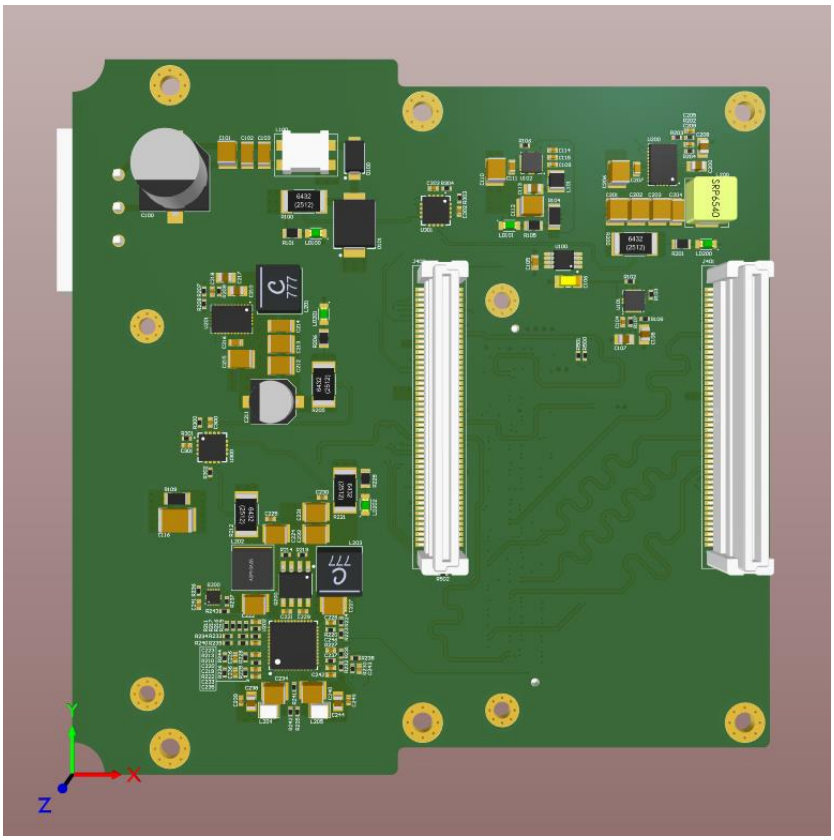

Figure 31. FPGAIOC-1 Top Assembly

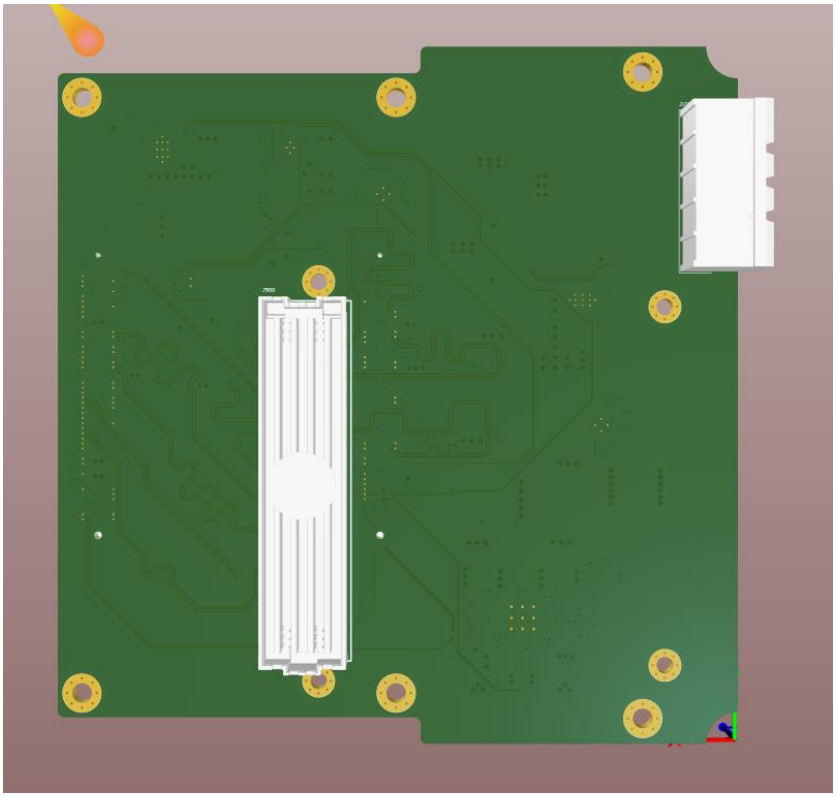

Figure 32. FPGAIOC-1 Bottom Assembly

6 Testing and verification

This section covers the verification and testing requirements for the FPGAIOC. The written technical specification, which is the basis of this development, is validated and approved by the ESS.

The testing and verification of the FPGAIOC is in the scope of the Department of Computer Systems supported by the competencies of Testonica. Testing requirements are intended to make sure that any defect or fault created in course of any phase of FPGAIOC production will be discovered and corrected.

Although mechanical vibration testing is a standard method to screen out various defects during manufacturing in automotive, military and aerospace products, it is not needed in case of FPGAIOC as the units will not experience considerable mechanical or thermal stress [3].

The FPGAIOC has to comply with electromagnetic compatibility (EMC) and electromagnetic interference (EMI) standards used for CE certification, such as EN55032 [61] and EN55035 [62] [3].

Power, RS-232, Ethernet, SFP+ cage and the FMC socket will be tested with the production tester after the assembly of the boards. The Ethernet interface shall demonstrate full speed full duplex error free operation. Same applies for the SFP+ cage. Furthermore, RAM, Flash Memories, SVC and power supplies are tested as well. Testing takes place with the production tester through the JTAG interface [3].

7 Documentation

Development of the FPGAIOC is documented and multiple documents are written during the development. FPGAIOC design documentation or technical file includes all schematic, PCB and mechanical drawings in PDF format. In manufacturing files are added to the technical documentation. User's guide document will include module description and technical overview including various instructions, for example how to select VADJ voltage or instructions to build various software images for boot modes.

Software with source files, build scripts, and pre-built binaries for both Zynq and self-developed PCB boards are stored in GIT repository environment. User guide document for describing both software architectures is written.

Manufacturing test plan document will cover the scope of testing, includes description of tools and software required for testing. Furthermore, test instructions document, which includes detailed steps how to perform testing at manufacturing supports the manufacturing test plan. Factory test report will be generated for each FPGAIOC unit consisting of product number, version, batch number, serial number and list of tests performed with test status.

8 Summary

The goal of the thesis was to develop a standalone embedded computer system for the European Spallation Source project. The FPGAIOC is integrated to the ESS Integrated Control System for data management and day-to-day running of all the equipment. The FPGAIOC was developed, which consists of a PicoZed SoM, FMC and 2 self-developed 8 layers boards, which have dimensions of 107.2mm x 110mm. FPGAIOC is mounted inside of a 120mm x 120mm x 59mm aluminium casing.

One developed board is dedicated for powering all components in the FPGAIOC system and contains many different DC/DC converters, such as ADP5051 and LM73605, as well LDO's and watchdog circuits. Second board mounts all the necessary logic for controlling the FPGAIOC and high-speed components, such as STM32F407VGT7 supervisory microcontroller, KSZ8463 Ethernet IC, MAX-3250 RS-232 IC or SFP cage for connectivity. All high-speed signals were routed using stripline as well microstrip routing techniques.

Development was based on technical specification which is based on many meeting minutes with the ESS.

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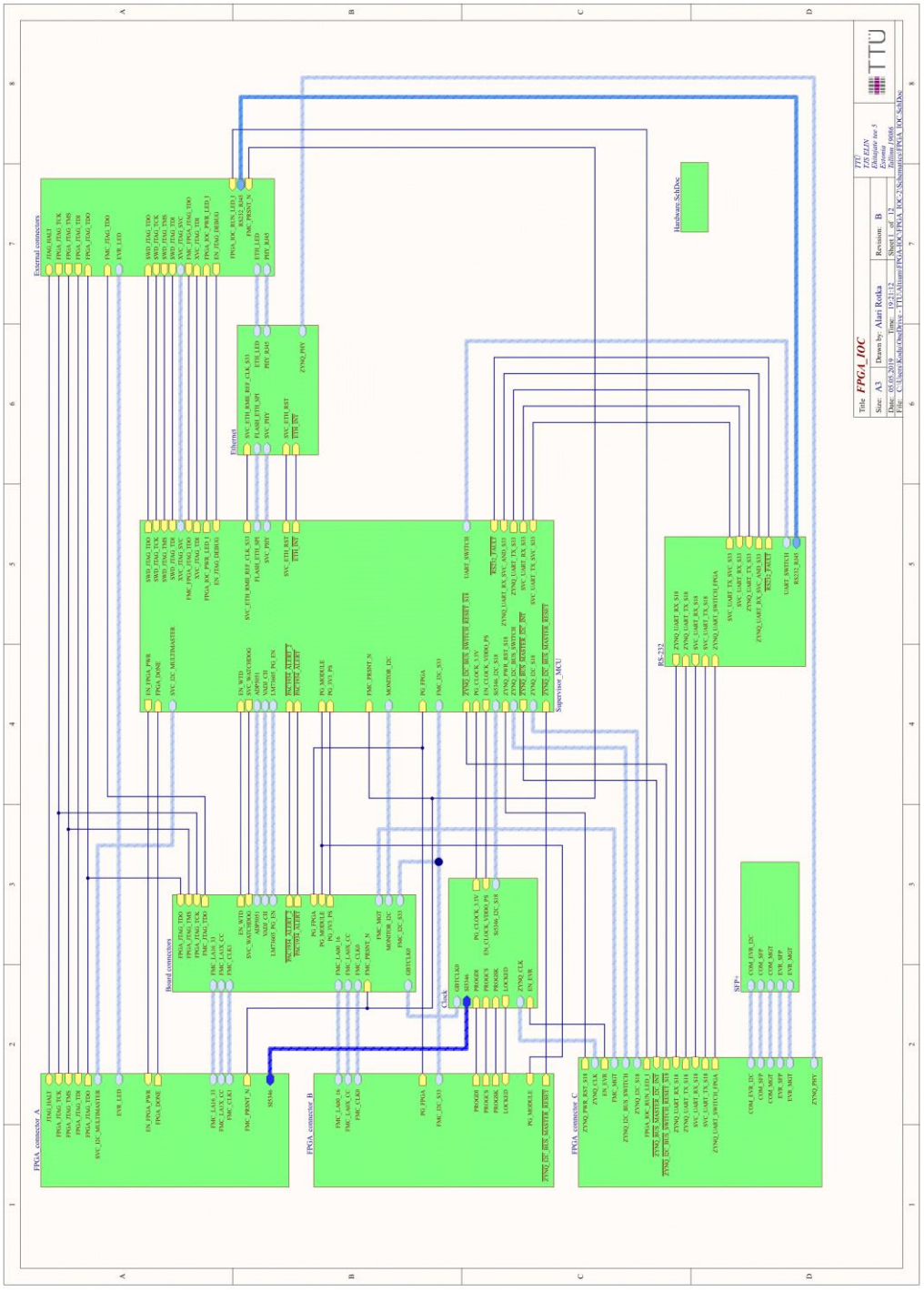
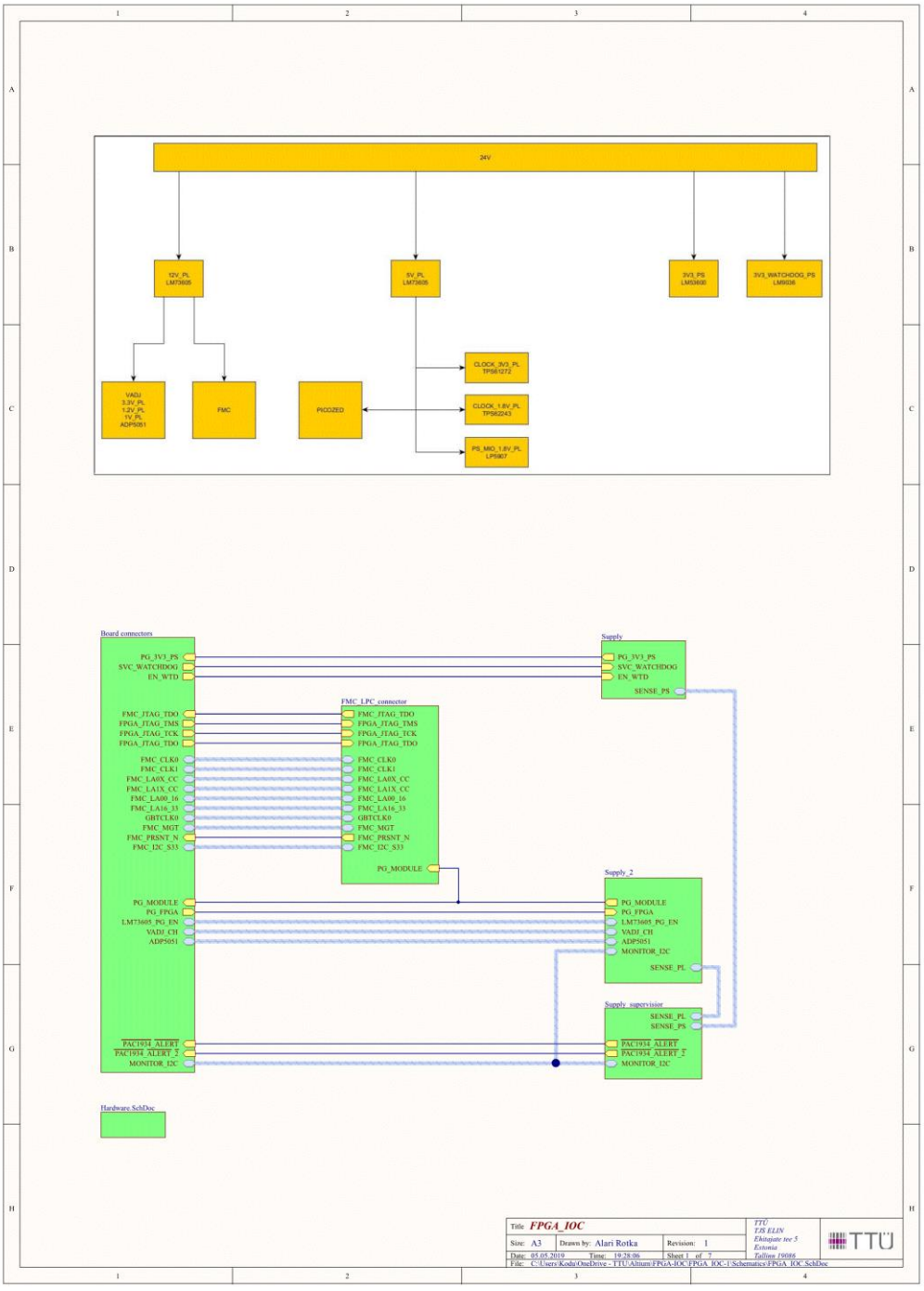
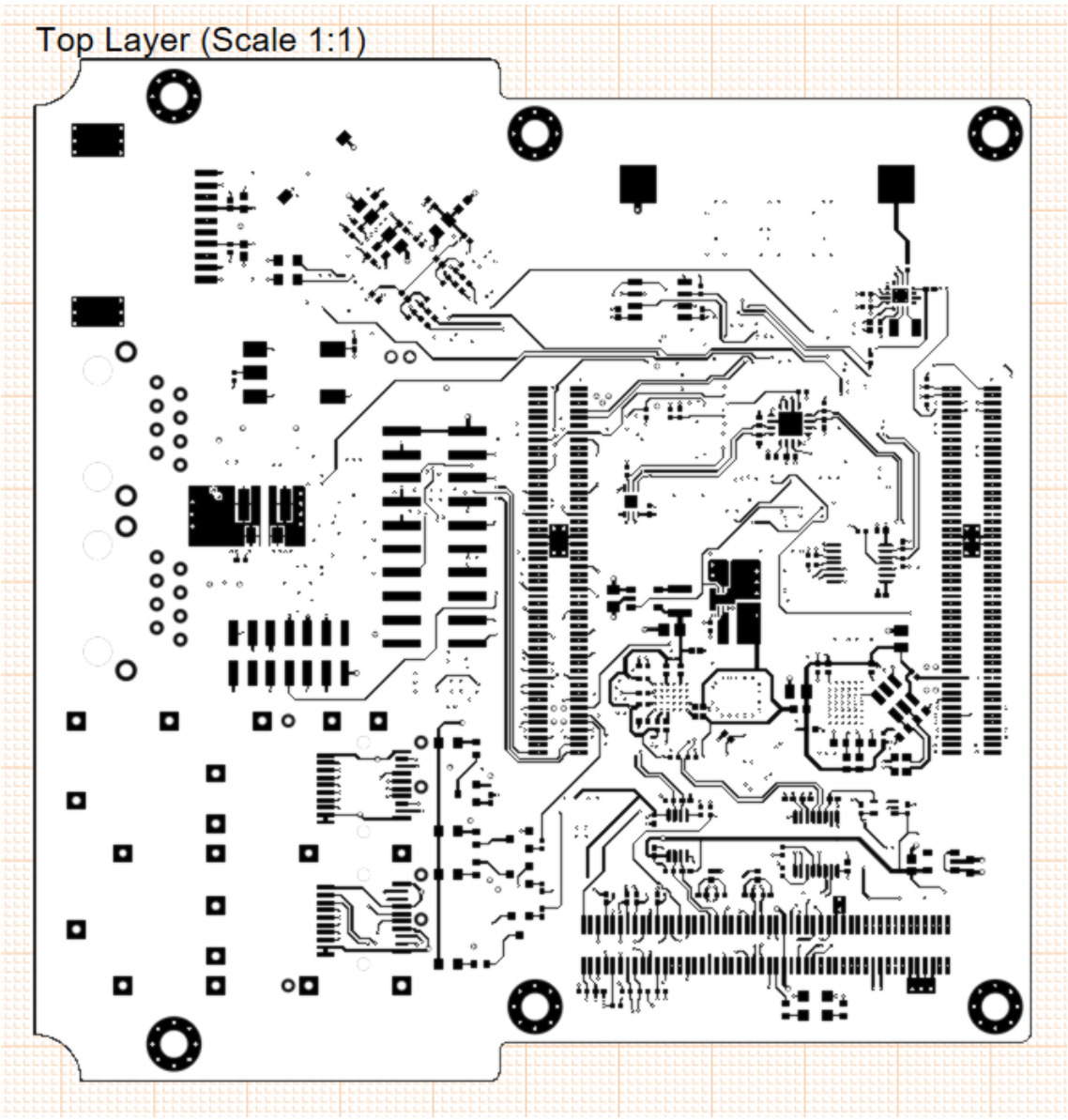
Appendix 1 – FPGAIOC-2 Schematic overview



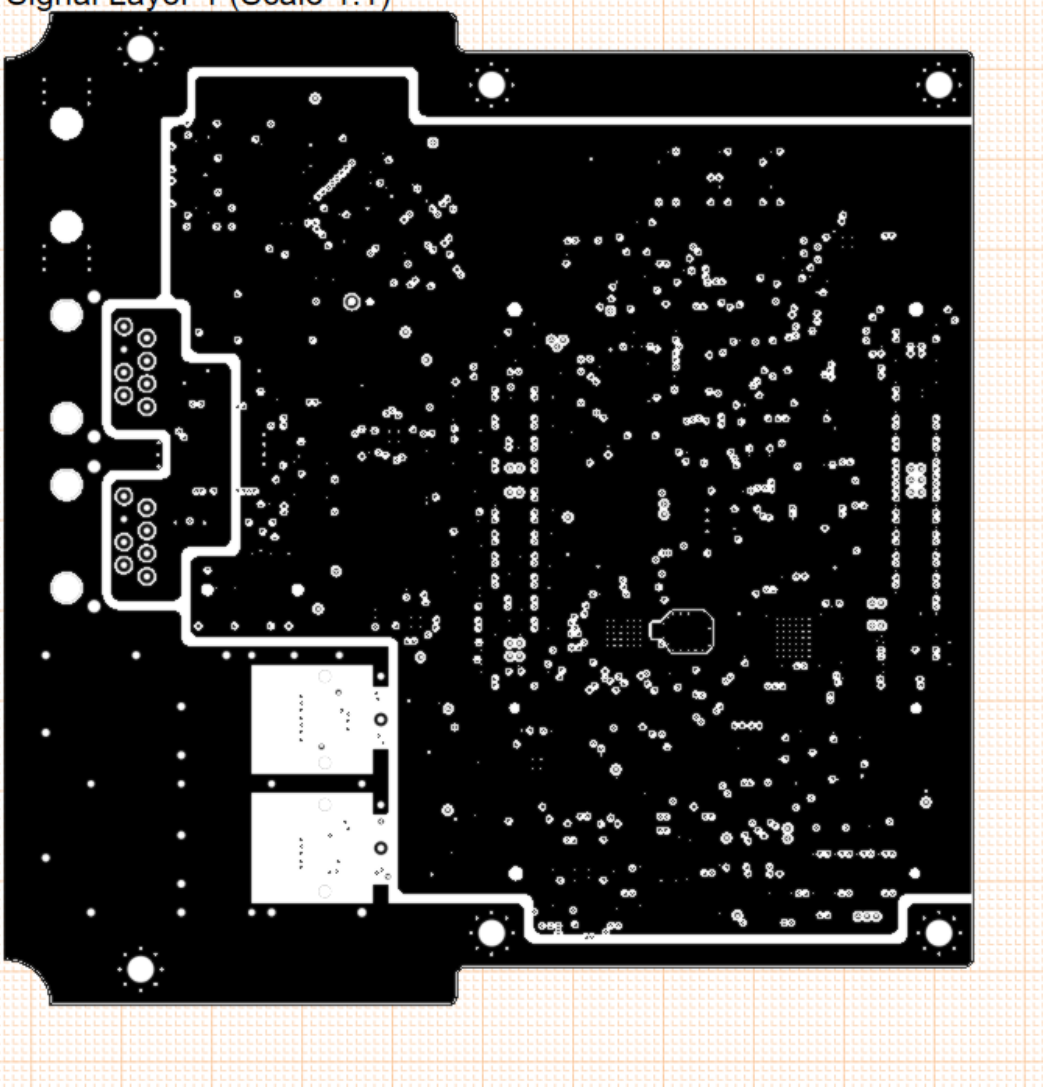
Appendix 2 – FPGAIOC-1 Schematic overview



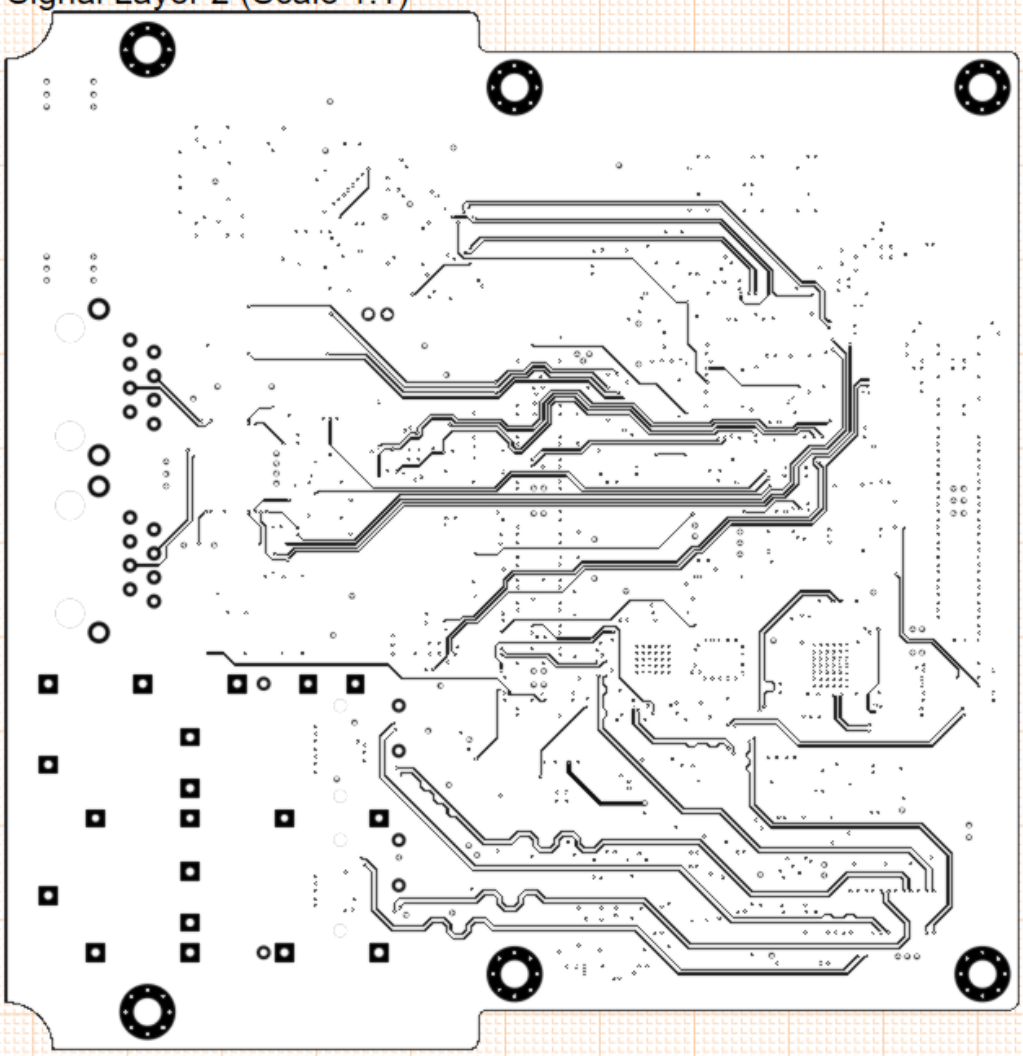
Appendix 3 – FPGAIOC-2 PCB layers



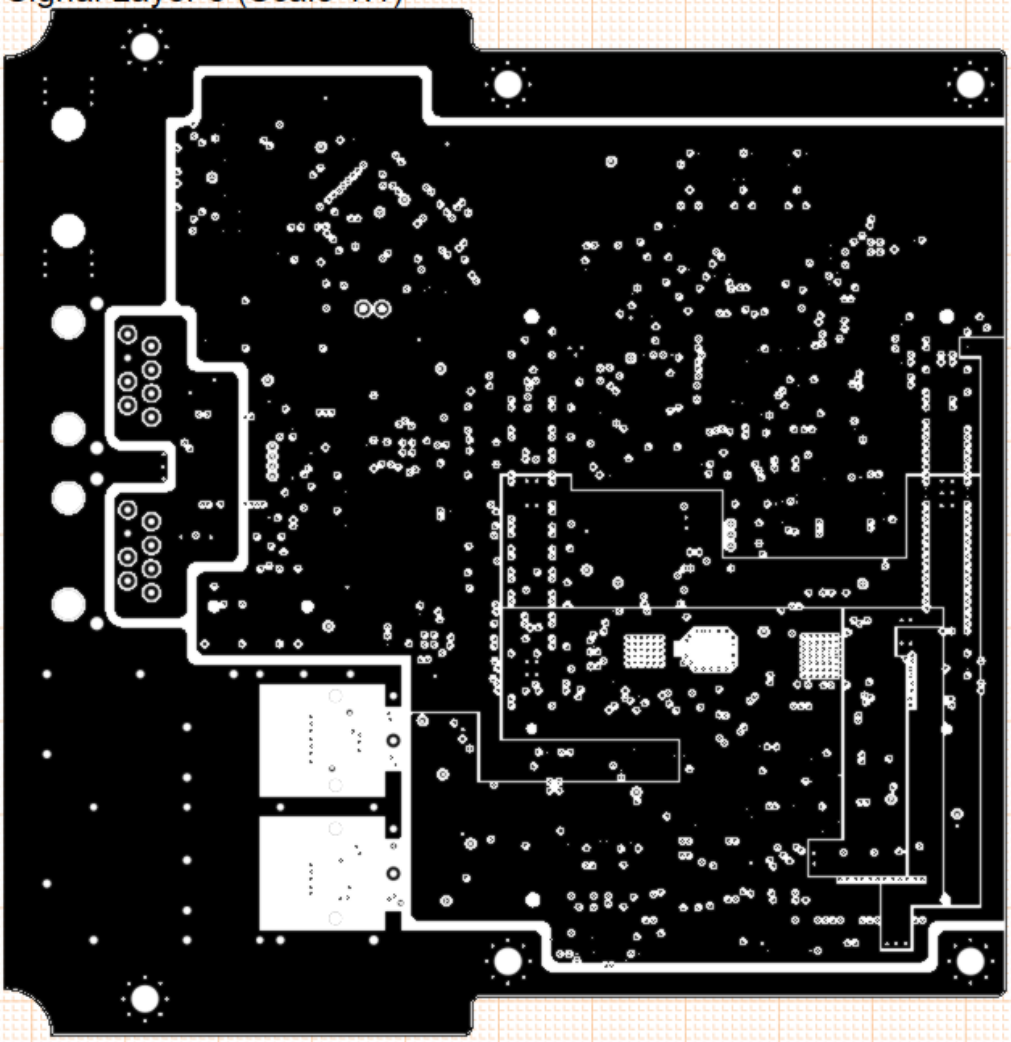
Signal Layer 1 (Scale 1:1)



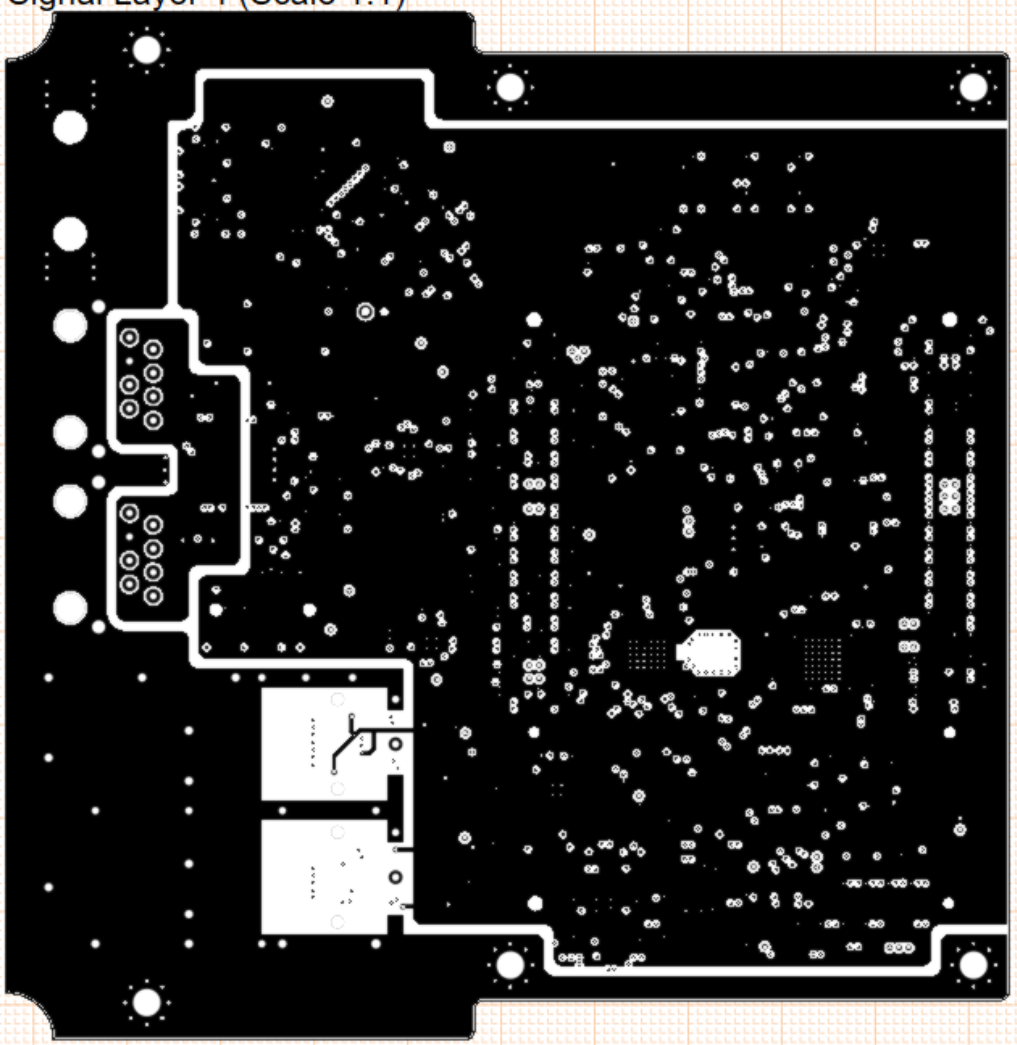
Signal Layer 2 (Scale 1:1)



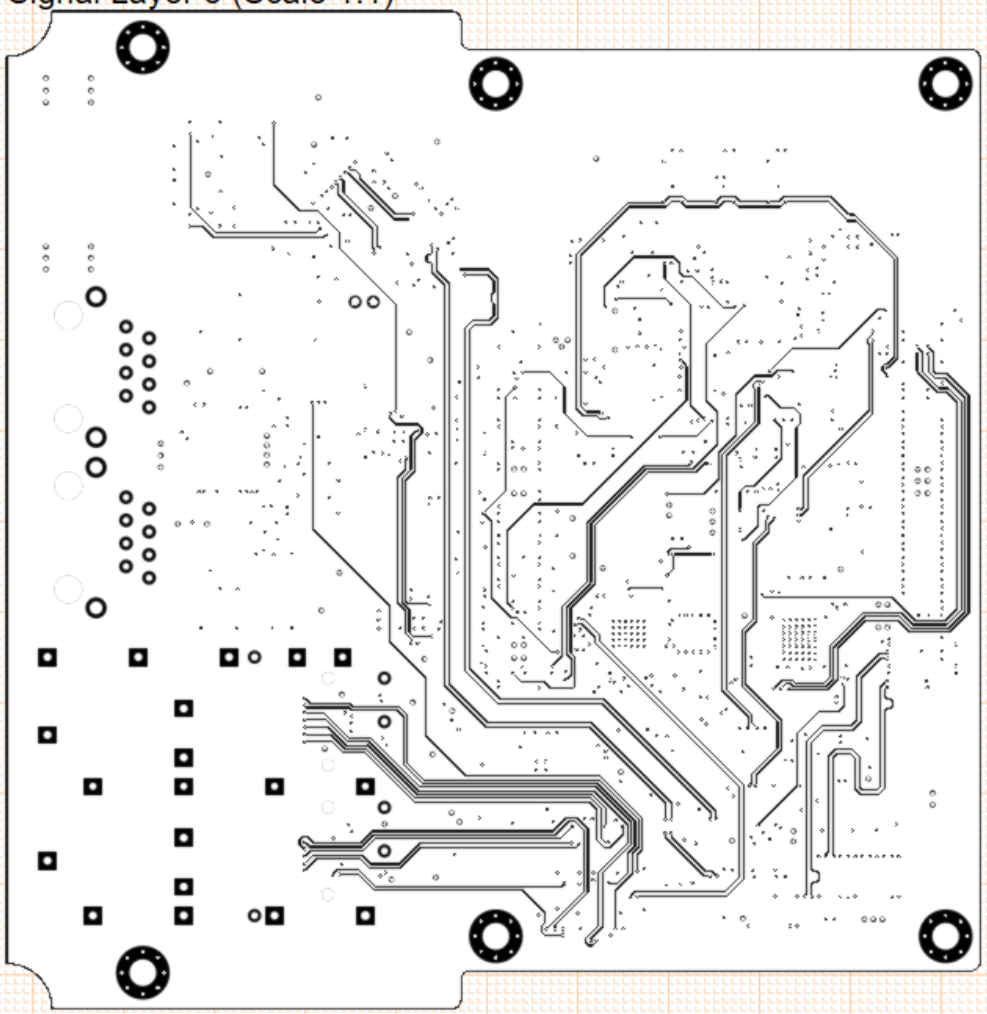
Signal Layer 3 (Scale 1:1)



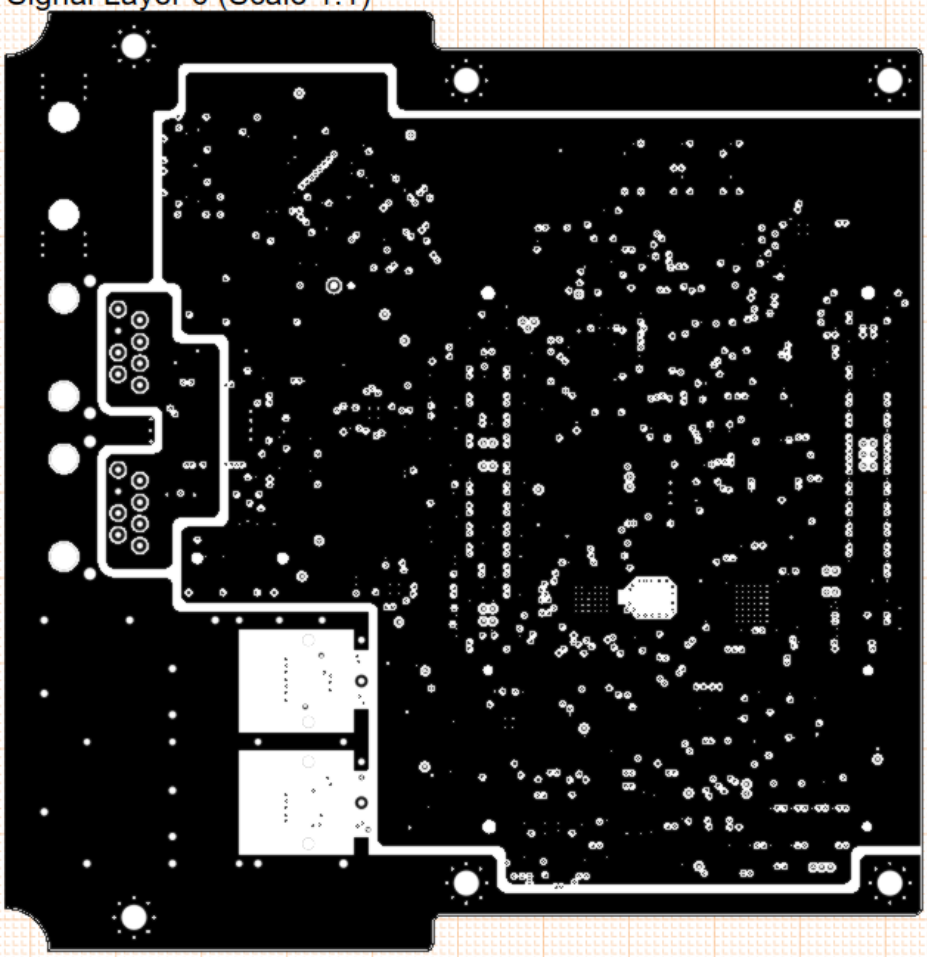
Signal Layer 4 (Scale 1:1)



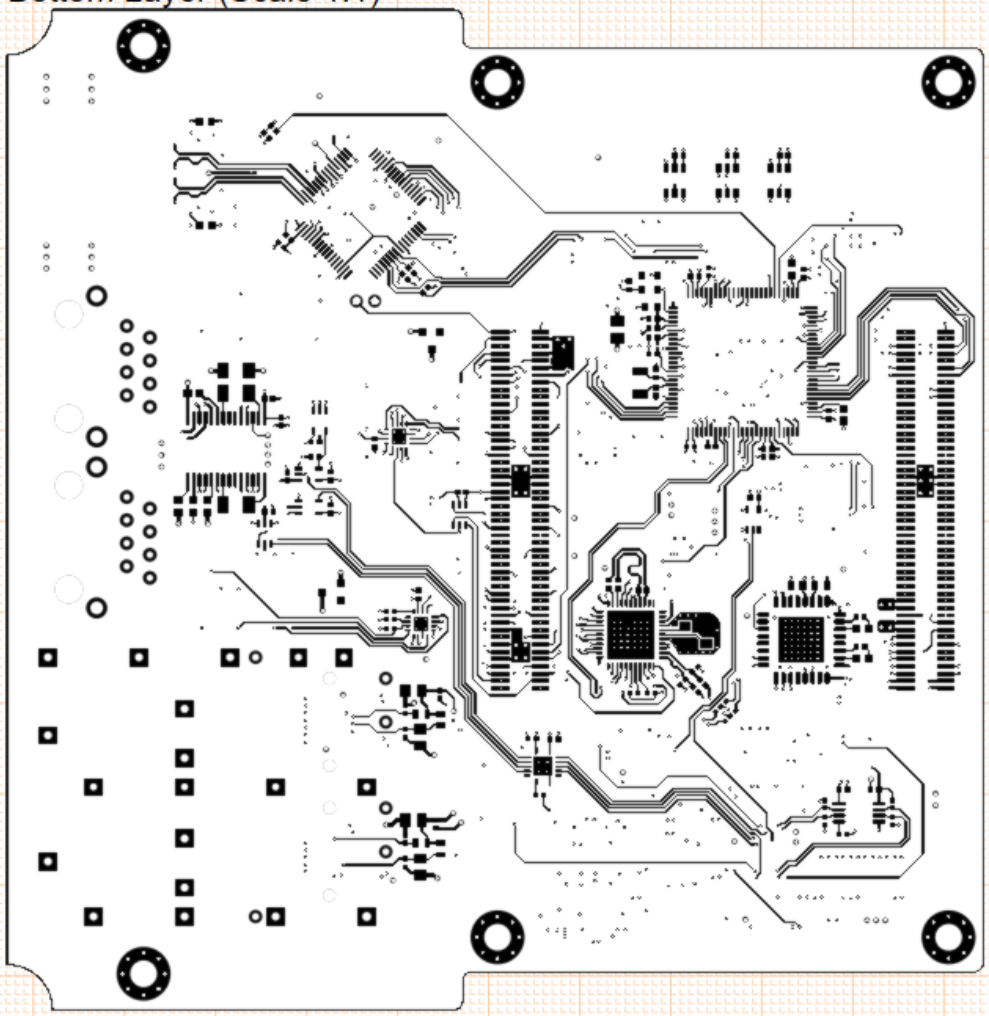
Signal Layer 5 (Scale 1:1)



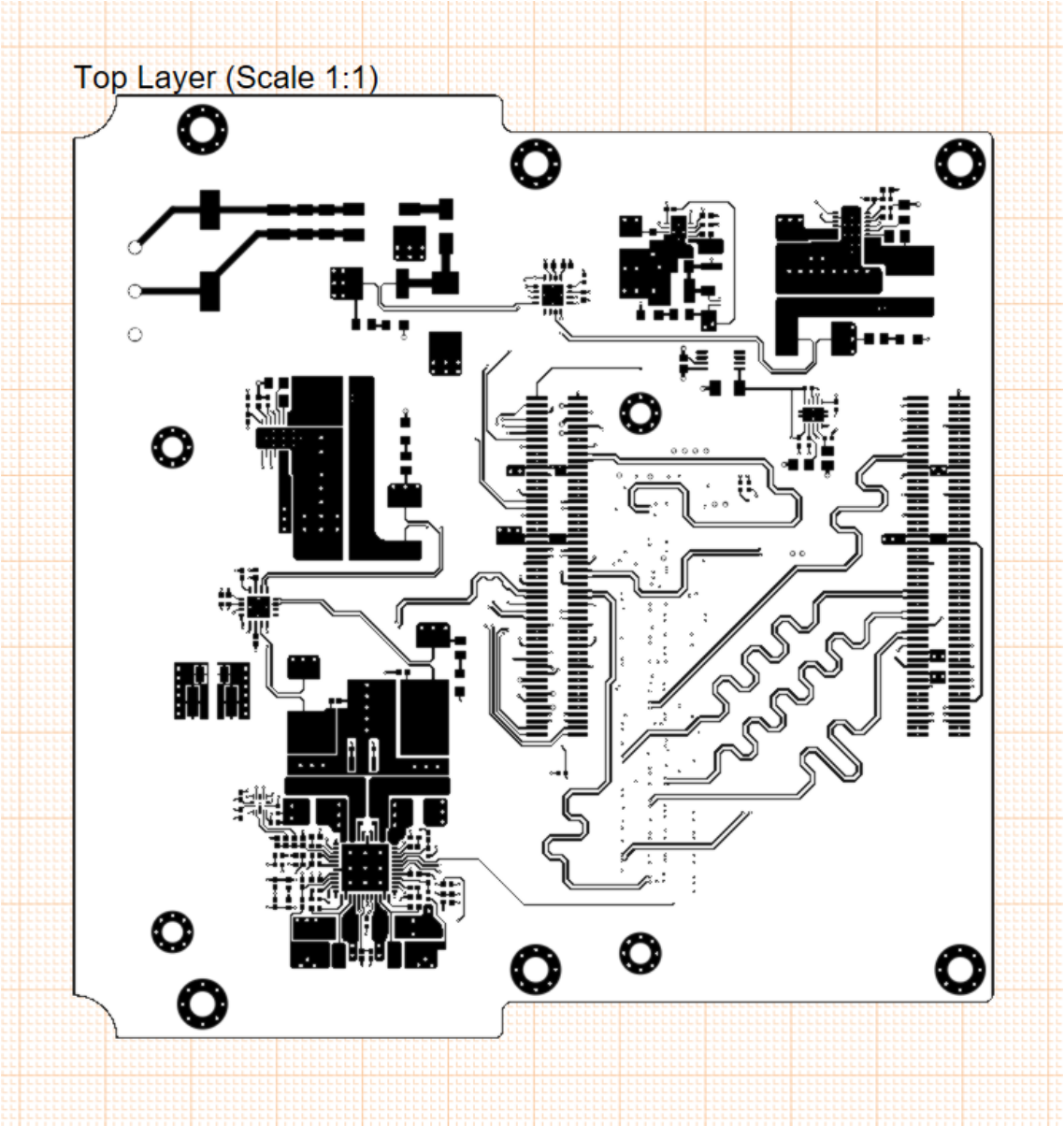
Signal Layer 6 (Scale 1:1)



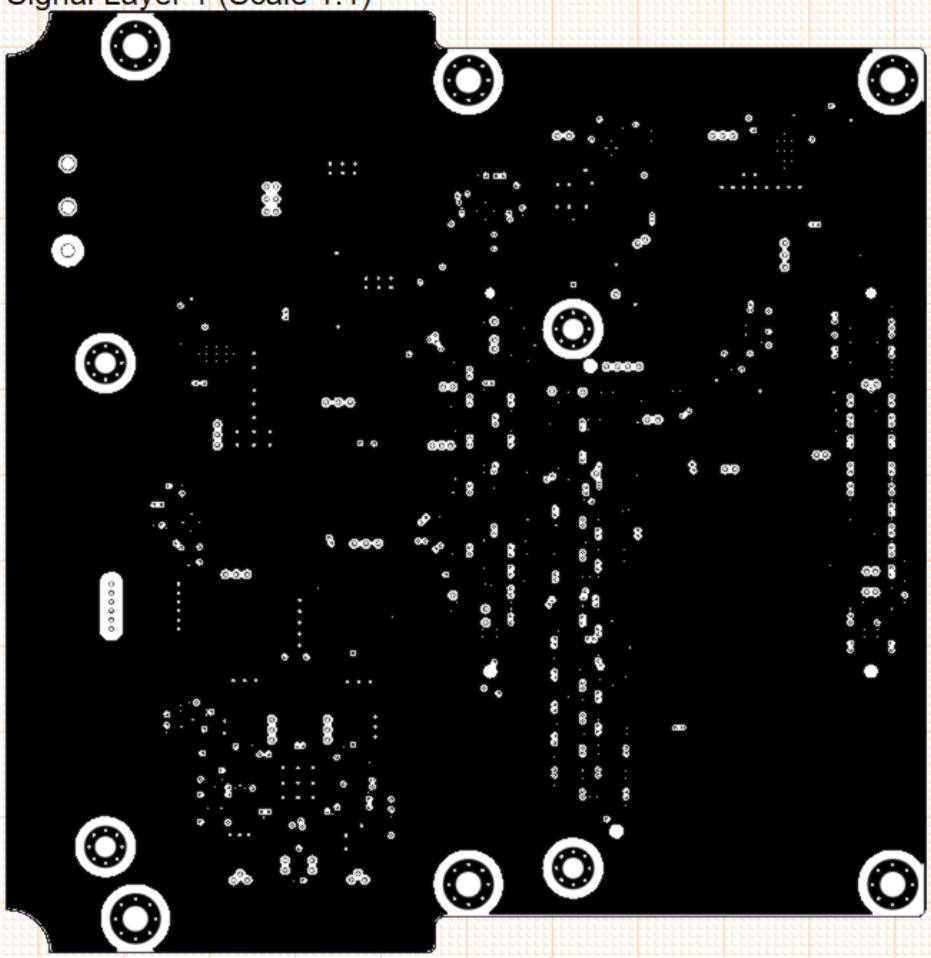
Bottom Layer (Scale 1:1)



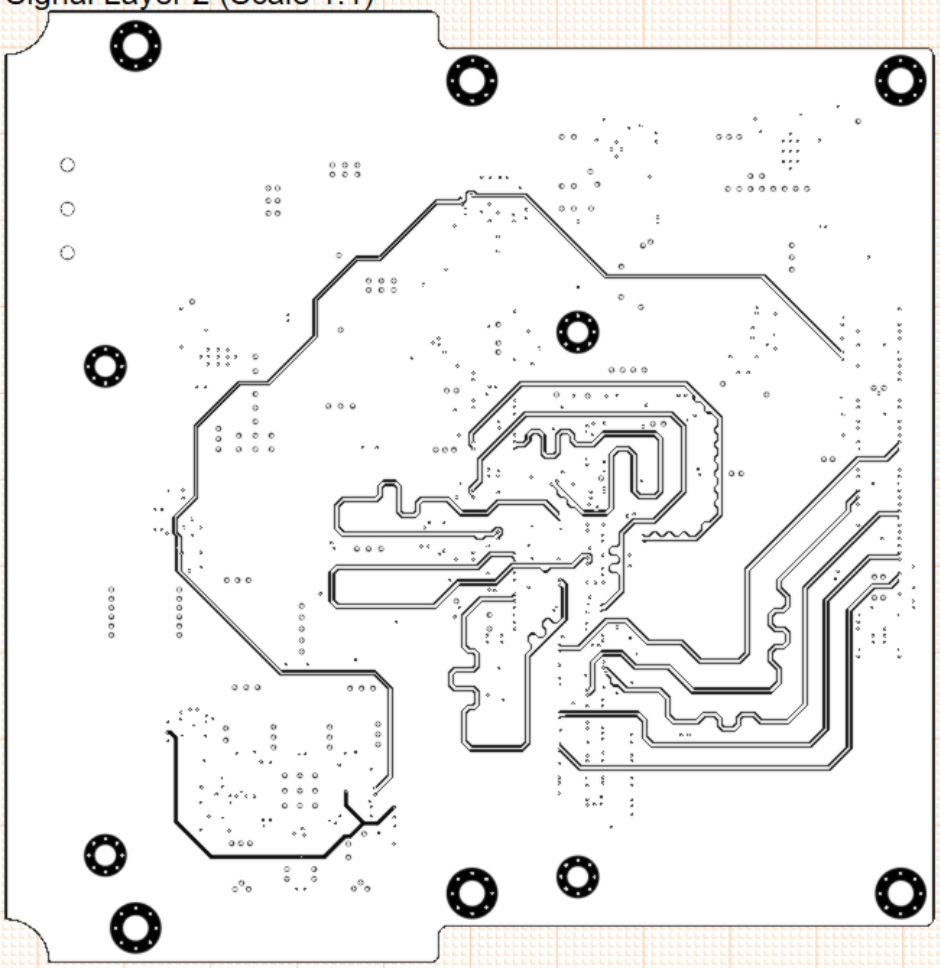
Appendix 4 – FPGAIOC-1 PCB layers



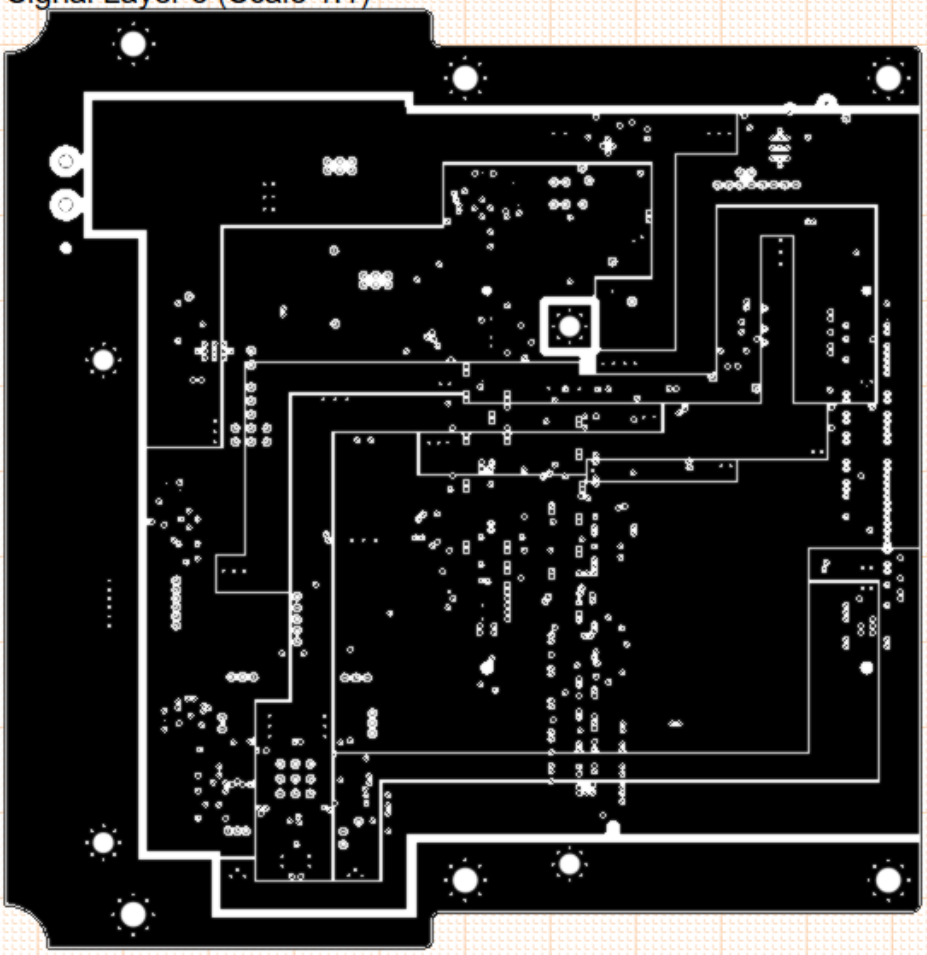
Signal Layer 1 (Scale 1:1)



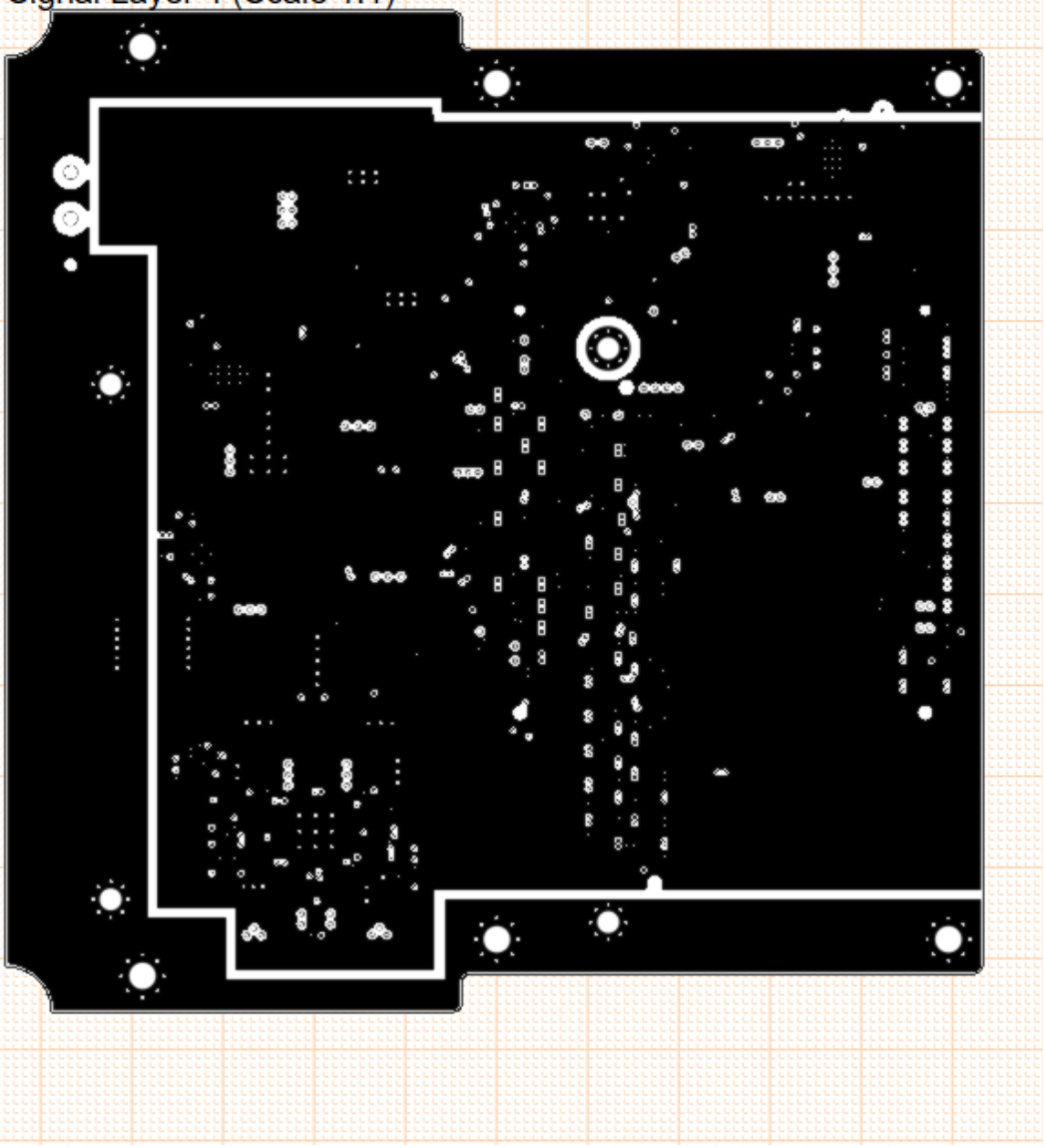
Signal Layer 2 (Scale 1:1)



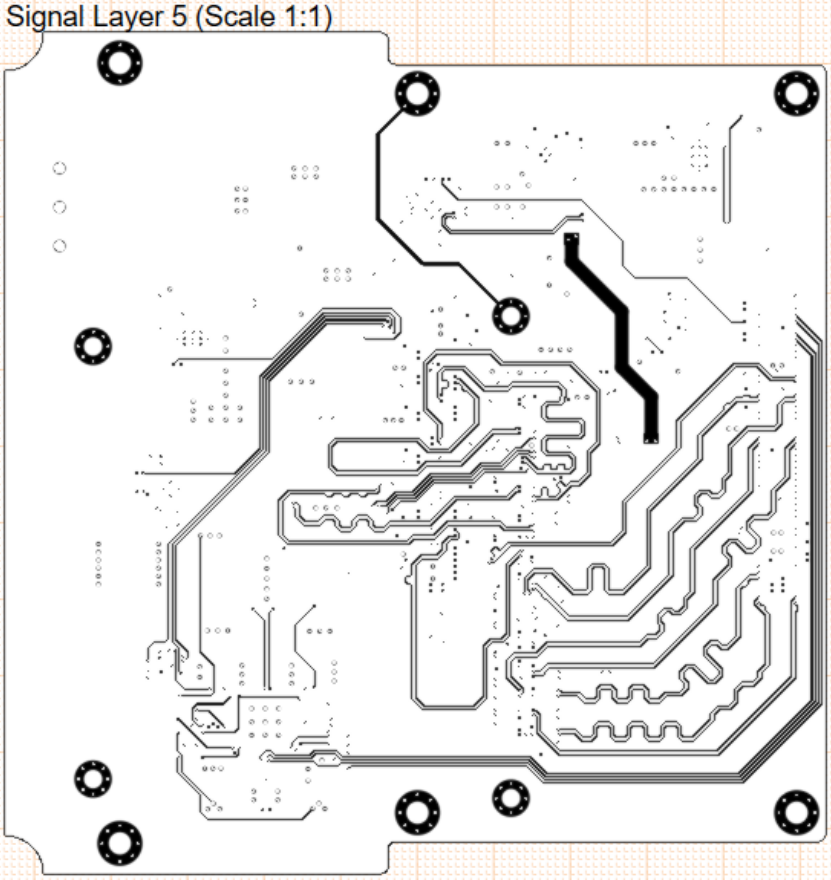
Signal Layer 3 (Scale 1:1)



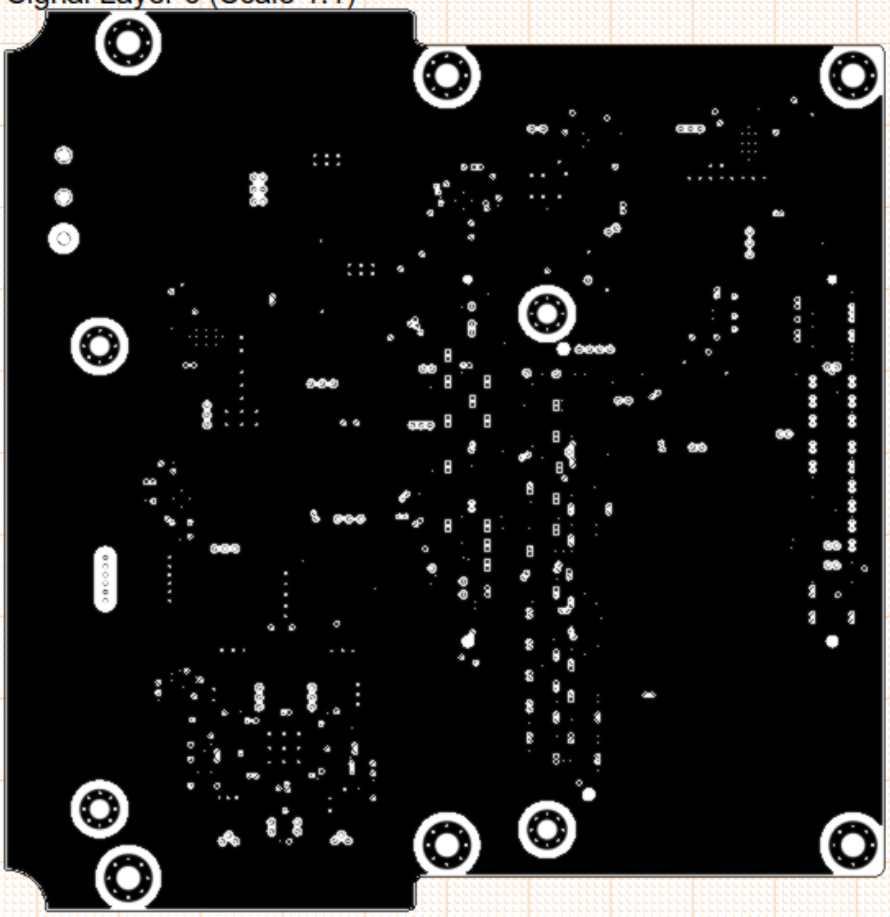
Signal Layer 4 (Scale 1:1)



Signal Layer 5 (Scale 1:1)



Signal Layer 6 (Scale 1:1)



Bottom Layer (Scale 1:1)