TAL TECH

DOCTORAL THESIS

Characterization of Interfaces Between the Metal Film and Silicon Carbide Semiconductor

Mehadi Hasan Ziko

TALLINNA TEHNIKAÜLIKOOL
TALLINN UNIVERSITY OF TECHNOLOGY
TALLINN 2021

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52/2021

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology, has not been submitted for a doctoral or equivalent academic degree.

Mehadi Hasan Ziko …….

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ISSN 2585-6898 (publication)
ISBN 978-9949-83-763-2 (publication)
ISSN 2585-6901 (PDF)
ISBN 978-9949-83-764-9 (PDF)
Printed by Koopia Niini & Rauam

TALLINNA TEHNIKAÜLIKOOL
DOKTORITÖÖ
52/2021

Metallkontakti ja ränikarbiidi vahelise liidespinna karakteriseerimine

MEHADI HASAN ZIKO

TAL TECH
KIRJASTUS

Contents

List of publications

The work of this thesis is based on the following publications:

[Paper I] Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas (2018). Numerical Simulation of p-type Al/4H-SiC Schottky barrier diodes. Proceedings of Baltic Electronics Conference BEC2018: 16th Biennial Baltic Electronics Conference BEC2018, Tallinn, Estonia, Oct. 8–10, 2018. Ed. Ants Koel, Peeter Ellervee. IEEE Catalog Number: CFP18BEC-USB. doi: 10.1109/BEC.2018.8600976.

[Paper II] Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas; Toompuu, Jana (2020). Analysis of barrier inhomogeneities of P-type Al/4H-SiC Schottky barrier diodes. Materials Science Forum, 1004, 960−972.

[Paper III] Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas; Rashid, Muhammad Haroon (2020). Investigation of barrier inhomogeneities and electronic transport on Al-Foil/p-Type-4H-SiC Schottky barrier diodes using diffusion welding. Crystals, 10, 636−647. doi: 10.3390/cryst10080636.

[Paper IV] Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas (2020). Characterization of Al-foil/p-4H-SiC SBDs fabricated by DW with variation of process conditions. Wide Bandgap Power Devices and Applications in Asia (WiPDA-Asia), Suita, Japan, Sep. 23–25, 2020. IEEE Xplore.

Author Contributions: Mehadi H. Ziko (M.H.Z.) and Ants Koel (A.K.) conceived the idea; M.H.Z. developed the diodes and performed the experiments; M.H.Z. drafted the papers; Toomas Rang (T.R.) and A.K. reviewed the papers; Jana Toompuu (J.T.) and Muhammad Haroon Rashid (M.H.R.) also reviewed Paper II and Paper III; A.K. and T.R. managed funding of the project. All authors have read and agreed to the published versions of all manuscripts.

Publications on the other topics

[1] Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas (2021). Comparative Electrical Properties Study of Al-Foil/P- and N-Type 4H/6H-SiC Schottky Barrier Diode Fabricated Using Diffusion Welded Bonding. 13th European Conference on Silicon Carbide and Related Materials (ECSCRM 2021) Tours (France), on October 24–28, 2021.

[2] Rashid, Haroon Muhammad; Koel, Ants; Rang, Toomas; Ziko, Mehadi Hasan (2020). Simulation of benzene and hydrogen-sulfide gas detector based on single-walled carbon nanotube over intrinsic 4H-SiC substrate. Micromachines, 11, 453−465. doi: 10.3390/mi11050453.

[3] Ziko, Mehadi Hasan; Ghouri, M. Siraj; Koel, Ants (2020). Modeling and simulation of MEMS capacitive displacement sensors. 15th IEEE International Conference on Nano/Micro Engineered & Molecular Systems, (IEEE-NEMS 2020), San Diago, USA, Sep. 27–30 2020. IEEE Explore.

[4] Ziko, Mehadi Hasan; Koel, Ants (2019). Theoretical and numerical investigations on a silicon-based MEMS chevron type thermal actuator. 2018 IEEE 18th International Conference on Nanotechnology (IEEE-NANO). Cork, Ireland, July 23-26, 2018, 1–5. doi: 10.1109/NANO.2018.8626366.

[5] Ziko, Mehadi Hasan; Koel, Ants (2018). Optimum electromagnetic modelling of RF MEMS switches. Elektronika ir Elektrotechnika, 24(5), 46–50, doi: 10.5755/j01.eie.24.5.21842.

[6] Ziko, Mehadi Hasan; Koel, Ants (2018). Design and optimization of AlN based RF MEMS switches. IOP Conference Series: Materials Science and Engineering, 362: 2018 International Conference on Smart Engineering Materials, ICSEM 2018; Bucharest; Romania; Mar. 7–8, 2018. doi: 10.1088/1757-899X/362/1/012002.

Symbol and abbreviation list

ϕ_M	work functions of the metal
ϕ_S	work functions of the semiconductor
χ_S	electron affinity of a semiconductor
ϕ_{Bn}	barrier of the junction for n semiconductors
ϕ_{Bp}	barrier of the junction for p-type semiconductors
q	elementary charge of electron in coulomb
E_g	energy band gap
E	energy level in a semiconductor
E_F	Fermi energy
K_BT	Boltzmann constant
$\hbar$	Planck constant
$Dc\ (E)$	densities of the state in the conduction band
$Dv\ (E)$	densities of the state in the valance band
M^*n,p	effective mass of the charge carriers for n and p semiconductor
$E_{c,v}$	conduction and valence band for n- and p-type semiconductors
$N_{C,V}$	product of electron and hole concentration
N_A, N_D	acceptor and donor semiconductor
g	degeneracy factor
E_A	activation energy
n_i	intrinsic carrier concentration
E_c	conduction band
E_v	valence band
$e_{n,p}$	electron and hole emission
$c_{n,p}$	electron and hole capture
E_i	initial energy
E_t	transition energy
$\Delta H_{n,p}$	entropy for electron and hole
$X_{n,p}$	entropy factor for electron and hole
σ_n	capture cross-section for electron

σ_p	capture cross-section for hole
$V_{th\ n,p}$	thermal velocity of electrons and holes
ΔE_n or ΔE_p	activation energy of electron or hole
D	diffusion coefficient
$\frac{\partial c}{\partial x}$	concentration gradient
M	atomic nucleus with mass
m_e	rest mass
E_e	kinetic energy
V	velocity
Ɛ	dielectric constant
C	capacitance per unit area
ΔE	activation energies
σ	capture cross-section
e_{em}	electron emission

1. Introduction

1.1. Introduction

The increasing demand for electronic devices capable of functioning at high power, frequency, and temperatures as well as in harsh environments is one of the most significant issues in modern semiconductor industries. Fig. 1.1 shows the application areas of power devices based on rated current and voltage [1]. High voltage, high power, and high operating frequency semiconductor device requirements can be fulfilled using wide bandgap semiconductors [2]. Due to some incomparability such as doping, integration with complementary metal-oxide semiconductor (CMOS), compatibility, and fabrication feasibility, most WBG semiconductors (silicon carbide [SiC], Gallium Nitride [GaN], Gallium oxide [Ga_2O_3], and diamond) are not feasible for widespread commercialization. However, SiC technology stands to revolutionize power electronics.

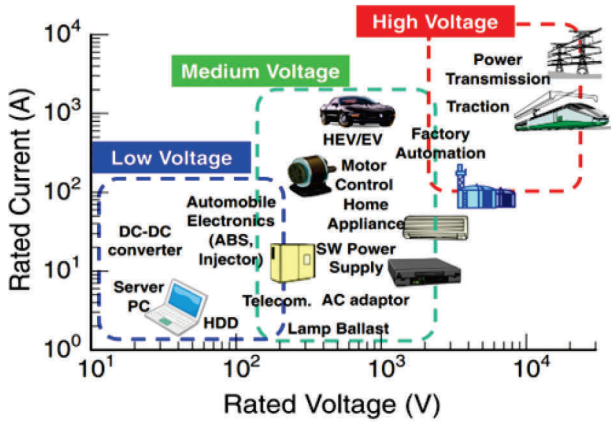


Fig. 1.1: Application areas of power devices based on current and voltage rating [1].

SiC takes the virtues of a diamond, one of the most challenging materials in the world, and combines them with the features of silicon. SiC has strong chemical bonding between silicon and carbon atoms, a feature that gives this material high hardness, chemical inertness, and high thermal conductivity. This strong bonding also provides SiC with a wide bandgap and high breakdown field strength. In addition, SiC has several poly-types and the possibility of making n- and p-type materials by controlling a wide range of doping concentrations. Table 1.1 shows a comparison of the physical and electrical properties of Si and WBG semiconductors.

Table 1.1: Comparison of Si with WBG semiconductors.

Physical and Electrical Properties	Units	Si	4H-SiC	GaN	Ga_2O_3	Diamond
Band gap, Eg	eV	1.12	3.26	3.20	4.8	5.45
Dielectric constant		11.7	9.66	8.99	16	5.5
Electron Affinity, X	eV	4.05	4.05	4.1	4	−1.27
Electron Mobility, μ_n	($cm^2/V/s$)	1400	900	1000	200	2200
Hole mobility, μ_p	($cm^2/V/s$)	450	120	350	20	850
Critical breakdown field Strength, E_{cr}	(MV/cm)	0.3	3-4	2.2	8	5-10
Satuarated electron drift velocity rate, V_s	($x10^7 cm/s$)	1	2	2.2	2	2.7
Thermal conductivity	(W/cm/°K)	1.5	3-4	1.3	12.34	22
Thermal Expansion	$10^{-6}/K$	2.6	4.3	3.17	1.54-3.15	0.4-1
Melting point	°C	1412	3103	2500	1900	4027

Referring to Table 1.1, the essential property of SiC is its bandgap, resulting in fewer electrons or holes that can cross from the valence band to the conduction band or vice versa at the specified temperature. SiC has almost 10 times more critical breakdown field strength than silicon; hence, it is capable of high-power and high-voltage application. The thermal conductivity of SiC is 2–3-times greater than silicon; thus, it can operate at high temperatures. The carrier mobility of SiC p-type SiC is lower than silicon. This property of p-type SiC leads to increased resistance-based devices. However, this device's resistivity can be controlled by reducing doping and thinning the epilayer. This thin epilayer can support low resistive, large electric fields and superior saturated electron velocity to produce devices with low switching loss and high voltage blocking power.

The development of low-cost, defectless SiC-based power devices, especially the fabrication, has been widely investigated by various research organizations and universities. As a result, contemporary SiC-based semiconductor devices are gaining wider adaption and commercialization. The main objective of the research presented in this thesis was to fabricate novel SiC-based Schottky barrier diodes (SBD) with a rarely used technology called diffusion welding (DW) and characterize the fabrication and irradiation-induced defects to produce reliable SBDs.

1.2. Research problem and research questions

A primary research task in the semiconductor industry is to develop inexpensive techniques to manufacture SBDs and reliable contacts. It is not common to join different materials like SiC and metal contacts using DW or direct bonding. Traditional sputtering, etching, and evaporation technologies have several drawbacks, such as high cost, numerous processing steps, a time-consuming nature, the realization of a metal layer with a homogeneous thickness over a large area of contact, and restrictions for the general thickness of the metal layer over the whole contact, among others. Direct bonding would reduce the fabrication cost of the devices, improve their electrical properties, and solve many processing problems. Direct bonding is possible with the DW technology proposed as the first topic in this thesis. In general, DW gives the possibility to improve some quality features of contacts as well as the metallization process [3]–[4]. The traditional contact challenges in electronic and semiconductor structures affects performance due to contact quality and reliable surfaces of two hard materials (like SiC substrate and aluminum [Al]).

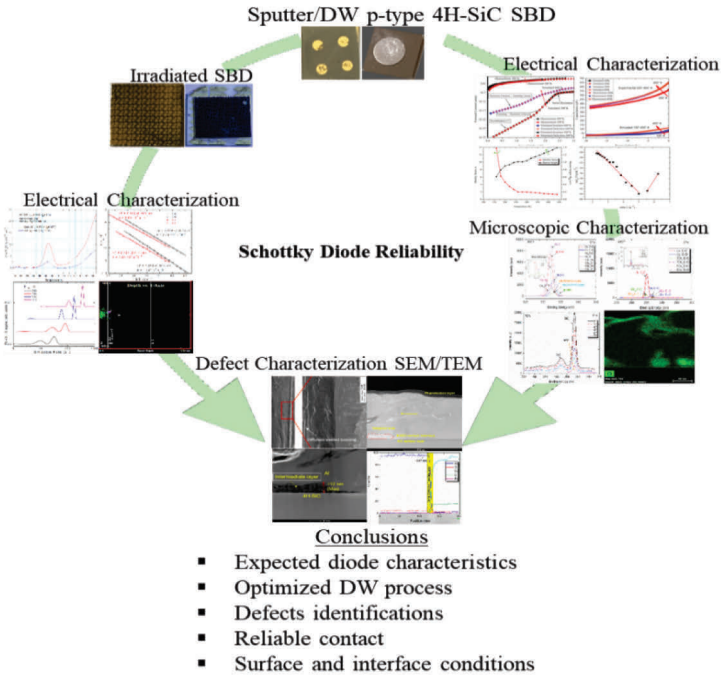


Fig. 1.2: Approach to evaluate the reliability of p-type 4H-SiC Schottky diodes.

Shear micro-deformation can occur during DW (at applied high pressure and temperature) in a subcontract surface layer of SiC. During the development of metal contacts for p-SiC substrates, it has been observed that a 25 nm amorphous layer develops between the metal film semiconductor surfaces [5]; this layer seems to influence the electrical characteristics of the Schottky structures. These traditional contact challenges in electronic and semiconductor structures affect performance due to contact quality and reliability, and finally, influence the device performance. So, it is necessary to develop a well-accepted understanding of the mechanism, and hence there is a need to investigate the reasons behind these influences. Therefore, one of the main tasks (and methods) is developing numerical models for such a multi-layer interface and to try to establish an acceptable physical explanation of the behavior of metal–p-SiC interfaces. Unfortunately, the drawbacks lie in quality: achieving a defectless contact, addressing barrier height inhomogeneity, preventing incomplete ionization of the holes, low contact resistance, good electrical contact, reliability of the contact, and surface roughness of the metal–semiconductor (MS) contacts using numerical solutions. Fig. 1.2 illustrates how to optimize the process and design to evaluate reliable SBDs using the various characterizations employed in this thesis.

This thesis addresses the following research questions:

1. What are the forward voltage drop, reverse breakdown voltage, and most dominant current transport phenomena and how do barrier inhomogeneity influence in diffusion-welded SBDs?

2. What are the prepared process parameters for diffusion-welded SBD manufacturing, and could DW be used rather than sputtering technology for Schottky diode development?
3. What are the energy levels of the defects and their electrical characteristics in Al-foil/4H-SiC diffusion-welded SBD and Au/4H-SiC sputtered SBDs?
4. What atoms/molecules interact more based on X-ray photoelectron spectroscopy (XPS) analysis, and how are the structural defects formed/initiated in diffusion-welded Al-foil/p-type SiC SBDs?
5. How are the defective layer/defects formed in diffusion-welded Al-foil/p-type SiC SBDs, and what are the maximum and minimum sizes of the defects in diffusion-welded SBDs?
6. How does electron irradiation influence and what are the defects created by electron irradiation in multi-point sputtered contact of SiC SBDs?
7. How is the carrier lifetime influenced by the irradiation decay in commercial Schottky diodes?

1.3. Motivation

During the last decade, SiC has gained significant attention, and n-type 4H-SiC has become a mature semiconductor material and commercially available in various high-voltage and high-temperature applications, even though several important topics are still under development. On the other hand, research on the p-type 4H-SiC material and their power devices have been much less studied. There is a need to understand the physics of p-type 4H-SiC devices and how to increase the growth rates of p-type SiC, metal contacts, and methods to improve the material carrier lifetime by high-temperature oxidations or carbon implantation by annealing.

Research group in Taltech introduced a DW fabrication technology as a one-step solution to ensure low cost, low forward voltage drop, low thermal resistance, and increased current rating and surge current values for power semiconductor devices. However, investigations on DW aluminum contacts to p- and n-type SiC evidence that p-type contacts differ so much from n-type contacts that p-type Schottky diodes can be considered an individual group of devices [3]–[5].

There are still fabrication difficulties of aluminum diffusion in p-type 4H-SiC DW SBD contact, leading to electrical characteristic mismatch, contact situation problems, a lack of understanding of the defects, issues with carrier lifetime, and incomplete ionization [6]. These physical explanations of the above-mentioned parameters and problems could be solved by investigating thoroughly the Al/Au contact on p-type 4H-SiC-based SBD devices. This thesis aims to contribute to optimize the fabrication parameters of p-type 4H-SiC-based SBD, process design, characterization of their surface and interfaces, understanding life-limiting defects, and understanding electron irradiation defects in p-type 4H-SiC-based Schottky diodes.

1.4. Thesis contributions

There are six main contributions of this Ph.D. thesis.

I. This thesis provides a comprehensive numerical simulation of current–voltage (I–V), capacitance–voltage (C–V), and impact ionization studies to understand the electrical behavior and their influence on the SBD devices. The experimental I–V and C–V characteristics based on the thermionic emission model in the temperature range of 300–450 K have been investigated. The ideality factor and barrier heights of identically manufactured Al-Foil/p-type-4H-SiC SBDs showing distinct deviations in their electrical characteristics have been determined. An improvement in the ideality factor of Al-foil/p-type-4H-SiC SBDs has been observed with an increase in temperature. There is an increase in barrier height in fabricated SBDs with an increase in temperature. Increases in barrier height, improved ideality factors, and abnormalities in their electrical characteristics are due to structural defect initiation, discrete energy level formation, interfacial native oxide layer formation, inhomogeneous doping profile distribution, and tunneling current formation at the SiC surfaces.

II. The reported work in this thesis has optimized the process parameters for diffusion-welded SBDs. Various manufacturing process parameters of diffusion-welded p-type 4H-SiC Schottky contact developments have been studied. Deposition temperature and pressure influence the diffusion-welded SBD electrical characteristics and their barrier inhomogeneity. A lower doping concentration in the epilayer improves the Schottky contact characteristics with the same manufacturing process parameters. In addition, Schottky contact with DW shows better electrical contact compared with the ion-sputtered deposition technique. Furthermore, temperature dependency of forward I–V, C–V, and barrier height correspond to ideality factor measurements of DW two manufacturing process parameters and show that there are greater barrier inhomogeneities at the metal–SiC interface compared with one manufacturing process parameter for Al-foil/p-4H–SiC SBDs. These optimized process parameters significantly improve the experimentally measured electrical characteristics and reduce the inhomogeneous barrier height. The resultant device minimizes the discrete energy levels, minimizes tunneling current, leads to a better ideality factor, and lowers the formation of an interfacial native oxide layer during surface preparation.

III. The diffusion-welded and sputtered p-type 4H-SiC SBD fabrication and physical characterization have been studied. The numerical and experimental descriptions illustrate the reliable operation of the device. I–V and C–V characteristics have been measured and presented. As the metallization methods were different, one could expect that the I–V and C–V curves would differ. The difference in the zero capacitance value is also apparent. The investigated deep levels spectra have revealed two peaks in both contacts: a D peak appears at about 275–290 K for the diffusion-welded contact, with an activation energy of 0.596–0.663 eV and a capture cross-section of 1×10^{-11} to 1×10^{-14} cm^2. There is a D peak at a lower activation energy 0.483 eV with a capture cross-section of 4.06×10^{-16} cm^2,

observed in as-grown samples at 310 K, and a D peak at a higher activation energy of 0.66 eV with capture cross-section of 1.0×10^{-15} cm^2 at 260 K after annealing for the sputtered Schottky contact. There are other peaks: HM_3 at 390–407 K and HM_2 at 360 K with slightly higher activation energy 0.86 eV and 0.663 eV for as-grown and after-annealed samples. The activation energy and capture cross-section values are different, but the deep-level transient spectroscopy (DLTS) spectral shape is more or less the same for both metallization techniques. Au-sputtered p-type 4H-SiC SBD has been examined using atomic force microscopy (AFM). There is the formation of a dendritic structure due to annealing temperature.

IV. There have been significant improvements in the surface properties and contaminants of the 4H-SiC using XPS analysis in this work. The with chemical treatment (WCT) sample was less contaminated compared with the without chemical treatment (WOCT) sample. The WCT sample contains some sodium, zinc, fluorine, tin, and calcium contamination along with SiC, O_2, CO_2, H_2O, CO, C-clusters, Si-pyridinic, and Si-interstitial compared with the WOCT sample. Overall, the WCT sample has less contamination based on chemical spectra.

V. The transmission electron microscopy (TEM) investigation of diffusion-welded Al-foil/4H-SiC SBDs revealed that a nano deformation intermediate layer of 120 nm, and a defective amorphous layer of ~2.67 nm is formed directly on the SiC surface after DW. This investigation shows that optimized thermal deformation parameters during DW can control the thickness of the interfacial layer and minimize the tunneling current. The TEM observations revealed that DW with Al-foil has a strong bonding interface indicating that this binding structure has good potentiality at high power and high temperature SBD development.

VI. The electron irradiation study showed about 3-5 µm of the semi-insulating layer is formed in the sputter Au-contact p-type 4H-SiC SBDs. A comprehensive DLTS study on the diffusion-welded Al-foil and Au-sputtered contact SBDs has been performed. There was a well-defined spectral peak, namely D defect center and HK_2 peaks. Laplace deep-level transient spectroscopy (LDLTS) measurements showed that the emission signal in the temperature range of 270–310 K consists of two well-separated components in both samples. Arrhenius diagrams of emission rates have been plotted, and activation energy values for emission, pre-exponential factors and capture cross-section have been derived for both samples.

These contributions are related to Papers I–IV, included in the list of publications at the beginning of this thesis. These publications are available in full in appendices. The other contributions are unpublished and are briefly discussed in chapters 4 and 5 of this thesis.

1.5. Outline of the thesis

This thesis is subdivided into six chapters as follows:

Chapter 2 An overview of the present state of the art regarding the SiC polytypes and their chemical composite: The problem of SiC in semiconductor device applications, MS contact theory, literature surveyed focusing on doping and point defects aspects in semiconductor and SiC are discussed briefly. Furthermore, the theory and characterization of deep-level defect states are discussed.

Chapter 3 The possibilities of contact materials and their technological potential: A review and mechanical arrangement of DW and their fabrication solution and bonding process are included. The diffusion bonding mechanism for diffusion-welded SBDs is described.

Chapter 4 SBD device electrical characterization and simulations using various SBD devices, suggesting optimal design and process parameters. Deep-level point defects are discussed and characterized using DLTS and LDLTS. Microscopy analyses are discussed briefly for Fermi-level pinning, the interface inhomogeneity, and defects identification in surface and interface layers.

Chapter 5 A multi-contact point electron irradiated p-type 4H-SiC SBD: The irradiated SBDs have been analysed by using various electrical characterization. In particular, to demonstrate the various identified defects and their limiting factors for the reliable carrier lifetime of the devices.

Chapter 6 A summary of the work, a list of claims, and future work.

2. Background and theoretical discussion

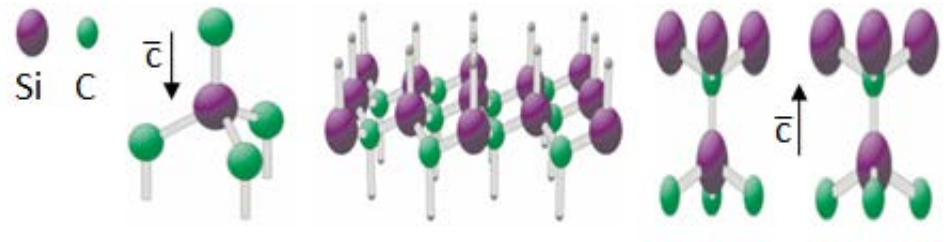
SiC is the only stable binary compound in the Si-C phase diagram with extraordinary properties, making it an ideal choice of material for thermal, high power applications. The crystal structures and doping concentration determine the SiC properties and potential applications. However, the induced defect resulting from doping plays an essential role in SiC-based power devices. Therefore, in this chapter, the theories of SiC crystal structures, problems with their application, MS approaches, transport properties in MS contacts, doping, and defects properties are discussed in detail.

This chapter is based on the following publication:

- M. H. Ziko, A. Koel and T. Rangs, "Numerical Simulation of P-Type Al/4H-SiC Schottky barrier diodes," presented at the 16th Biennial Baltic Electronics Conference (BEC), Tallinn, Estonia, October 8-10, 2018, pp. 1–4.

2.1. SiC crystal structures

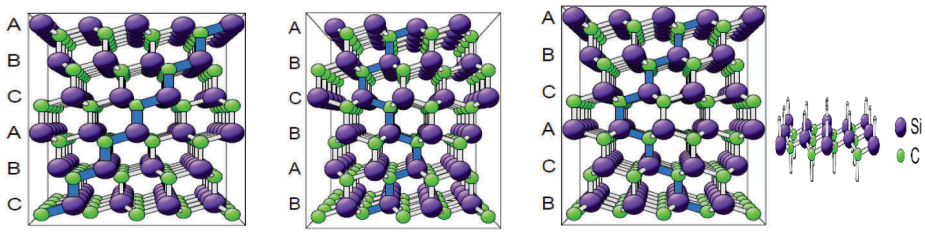
The minor component of the SiC crystal lattice creates tetrahedron bonding. In Fig 2.1, large violet spheres indicate silicon atoms, and small green spheres indicate carbon atoms. The down direction is labeled as the C-terminated SiC ($000\bar{1}$) surface, named the "C-face" (Fig. 2.1a) and the Si-terminated SiC (0001) is called the "Si-face" (Fig. 2.1c). Each surface is different and has distinct characteristics.



(a) (b) (c)

Fig. 2.1: (a) A tetrahedron building block containing Si-C with hybridized silicon and carbon atoms; (b) hexagonal SiC bilayer of the SiC crystal structure; and (c) Si-C tetrahedra bonded in identical orientation (left image) and rotated by 60° relative each other (right image), leading to cubic (zincblende) and hexagonal (wurtzite) SiC crystal structures. The images are adapted from [7].

These surface phases are the most important for the growth of SiC crystals, the physical understanding of metal–SiC interfaces in electronic devices, and their stability concerning decomposition at high temperatures. These larger tetrahedral crystal structures can be closely packed to construct Si-C bi-layers referred to as A, B, or C stacking in the enhanced thick blue line shown in Fig. 2.2. Although the different bi-layer stacking sequences do not influence the lattice parameters, but they affect the bandgap size. Crystallographically, a stacking sequence of ABC produces a zincblende structure, while only AB stacking produces a wurtzite structure.



3C-SiC (β) 4H-SiC (α) 6H-SiC (α)

Fig. 2.2: SiC Crystal structure of different polytypes. The layer orientation and stacking sequence are indicated by a thick blue line [7].

SiC has a one-dimensional large family (more than 200 crystalline modifications) of similar crystalline structures called polytypes. The main differences among the existing polytypes are the crystal structures due to different stacking layers on top of each other. The most investigated forms of SiC for electronic applications are the 15R, 3C, 4H, and 6H polytypes; out of those, only the 4H (ABCB sequence shown in Fig. 2.2) and 6H (ABC ACB sequence shown in Fig. 2.2) types are commercially available at this time. The non-cubic polytypes are referred to as closely packed cubic (zincblende structure, similar to diamond), called α-SiC (hexagonal-wurtzite structure) and rhombohedral. Only one polytype (3C-SiC) takes the cubic form, commonly referred to as β-SiC, stacked in an ABC sequence. The stacking used is referred to as Ramsdell notation. The letter refers to the symmetry of the crystal (C for cubic, H for hexagonal, and R for rhombohedral), and the number denotes the total count of double layers in one period.

The indirect band structure of each SiC polytype shows properties relevant to contact formation summarized in Table 2.1. The bandgap strongly depends on the polytype, which varies from 2.39 to 3.33 eV. 4H-SiC has a higher bandgap of 3.26 eV, and combined with the electron affinity of 3.3 eV, the position of the valence band is > 6 eV (away from the vacuum level) [11].

Table 2.1: Selected parameters of SiC (adapted from [8]–[10]).

Parameter	2H-SiC	4H-SiC	6H-SiC	3C-SiC
Stacking order	AB	ABCB	ABCACB	ABC
Percentage Hexagonality, ɣ (%)	100	50	33	0
Band Gap	3.33	3.26	3.0	2.39
Thermal Conductivity (W/cm/ °K)	3-4	3-4	3-4	3-4
Critical breakdown field Strength E_{cr} (MV/cm)		2-3	2-3	>1.5
Electron mobility μ_n (cm^2/V/s)(300K)		≤850	≤450	≤1000
Hole mobility, μ_p (cm^2/V/s) (300K)		≤120	≤100	≤40
Satuarated electron drift velocity rate V_s (x107 cm/s)		2	2	2.7

The cubic polytype has the highest reported electron mobility, but it has not been grown in bulk crystal sizes of more than a few millimeters. The 4H-SiC polytype has the greatest hole mobility, making it very interesting for many electronic applications.

2.2. Problems with the application of SiC

Although all SiC-polytypes have more favorable physical properties compared with Si, there are still many unsolved problems in the field of SiC power electronics industrial applications. For compound semiconductor 4H-SiC, p-type material can be created by doping with group III elements, such as boron or aluminum, whereas n-type doping is achieved by implantation with group V elements, like nitrogen or phosphorus with group IV elements. State-of-the-art, high-quality epitaxial n- and p-type 4H-SiC material creation is the current demand for device fabrication, especially to reduce oxidation at the Al-doped p-type SiC interface [12]. The SiC material has low dopant diffusivity properties due to its sizeable cohesive bonding energies. The ion implantation technique is considered most effective for SiC doping, leading to dramatic damage to the crystal lattice structure in the implanted region. Therefore, thermally stable Schottky and ohmic contact metallizations require annealing to repair the lattice damage and to sustain them at high temperatures. In the annealing phase, the intrinsic defects and dopant atoms known as point defects can reproduce and hence diminish the diode quality. Especially for the SiC metal, Schottky contact formation has an inhomogeneous barrier height mismatch, as discussed in [13]–[15].

Several carbon vacancy (V_c) removal techniques have been implemented to remove the defect from the SiC epilayer [16], [17]. Unfortunately, these defects could not entirely be removed from 4H-SiC materials. Additionally, the inherent n-type nature of SiC makes the p-type materials harder to grow. Hence, to increase the quality and epitaxial growth of p-type material, a semi-insulating layer is required in many power devices.

Another unsolved problem is unknown deep-level defects acting as a carrier trap exits in a sufficiently high concentration in SiC material. For example, the implementation of midgap point defects or impurity levels in the p-type SiC epilayer can control the semi-insulating layer of high-power devices. The following chapters address deep-level defects and their effect on electrical characteristics.

2.3. MS contact theory

MS contact plays an essential role in semiconductor electronics. MS devices are based upon the contact of a metal with a semiconductor; this contact can either be rectifying or non-rectifying. MS contact properties suffer due to inter-diffusion and accumulated surface charge at the interface or between the two layers, a phenomenon that adversely affects the barrier height. Schottky barrier height (SBH) dictates the behavior of Schottky and ohmic contacts [18]. The barrier height depends on the work functions of the metal and semiconductor used in ideal Schottky contacts.

Unlike PN diodes, Schottky diodes utilize a high-speed majority carrier conduction mechanism where no electron-hole recombination process is involved. This feature, coupled with lower turn-on voltages, allows higher switching speeds and lower power losses of a Schottky diode compared with a PN diode. This unipolar behavior means that SBDs have higher blocking voltages and large breakdown voltage or low resistance on a low-doped thick epitaxial layer of semiconductor beneath the metal.

Rectifying contacts are necessary for switching and rectification, while low resistive non-rectifying contacts are required in electronics to connect semiconductor devices to external circuits. A Schottky diode is the most straightforward device, consisting of metal that contacts an n- or a p-type semiconductor. Ohmic characteristics of an MS contact can be manipulated either by reducing the shape of the SBH or the width of the barrier itself or the doping concentration (the depletion region width is decreased as the doping level is increased) of the surface region of the semiconductor. Therefore, high-concentration doping is used to reduce the SBH in the substrate so that tunneling can occur. The SiC Schottky diodes are operated at near 600°C in atmospheric environments. Still, the degradation of the metal contacts limits the lifetime of the devices to only a few hours because of inter-diffusion and electro-migration alongside oxidation. These Schottky diodes have been used in this thesis as diagnostic tools to study and to understand the degradation mechanisms of metal contact; determine the barrier height, doping profiles, and deep level defects of the p-type SiC material; and to characterize defect damage due to electron irradiation.

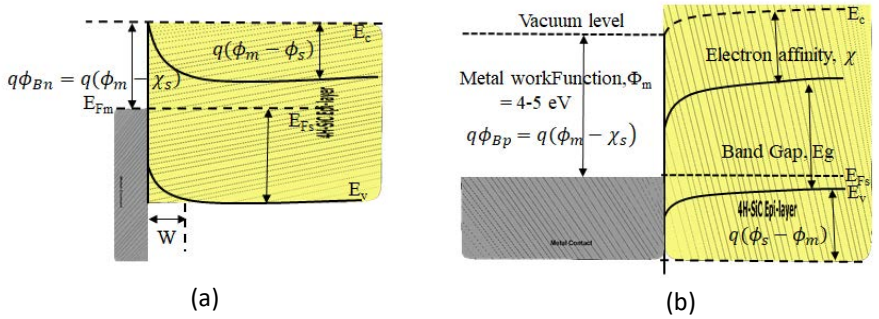


Fig. 2.3: Schottky barrier behaviors and band bending for (a) n-type (bend up causing a more positive region near the interface); and (b) p-type (bend down causing a more negative region near the interface) 4H-SiC with metal and semiconductor in close proximity. Modified from [19].

2.3.1. Rectifying and ohmic contacts

A forward bias voltage is applied to the semiconductor of the MS (p-type) SBD and the contact. The potential is reduced by $V_o - V$, which allows holes to diffuse into metal. On the contrary, by applying a reverse bias voltage to the MS (n-type) SBD and the contact potential is increased by $V_o + V_r$. In this situation, electrons have to overcome a voltage-independent barrier to diffuse into metal. When a reverse bias is applied to the semiconductor of the MS (p-type) SBD, $V_o + V_r$ reduces the contact potential. In this case, holes have to overcome a voltage-independent barrier to diffuse into the metal. Current flows primarily by majority carriers in both cases [Paper I]. The work function of most metals is between 4 and 5.5 eV, and in p-type 4H-SiC, the valence band position is > 6 eV [11]. As a result, there is a high-energy difference between the conducting carriers in the metal–4H-SiC material. However, minimal charge storage occurs, which leads to fast switching speeds in the SBD.

In the Schottky model for an ideal MS contact, the work functions ϕ_M and ϕ_S – for the metal and semiconductor, respectively—determine the ohmic or rectifying nature of the contact. Fig. 2.3 shows the Schottky barrier behavior and band bending for n- and p-type MS in close proximity and in contact.

For n-type semiconductors, the SBH is defined as the potential difference between the Fermi energy and the conduction band energy level at the MS interface shown in (2.1) [Paper I]:

$$q\phi_{Bn} = q(\phi_m - \chi_S)\,, \tag{2.1}$$

where the electron affinity of a semiconductor is represented by χ_S , ϕ_{Bp} is the barrier of the junction (ϕ_{Bn} and ϕ_{Bp} for n and p-type semiconductors, respectively), and *q* is the elementary charge of the electron in coulomb. For p-type material, the equation is slightly different because the Fermi level rises as electron flows from the metal into the semiconductor. It is represented by (2.2):

$$q\phi_{Bp} = E_g - q(\phi_m - \chi_S)\,, \tag{2.2}$$

where E_g is the energy band gap. The SBH for a p-type semiconductor is defined as the potential difference between the Fermi energy level and the valence band energy level at the MS interface deduced from (2.2). It is expressed by (2.3):

$$\phi_B = \frac{E_g}{q} + \chi_S - \phi_m\,. \tag{2.3}$$

In the rectifying contact, holes flow from p-type semiconductors to the metal with a positive barrier height $\phi_m < \phi_s$. When there is no barrier for current flow from both sides for metal to p-type semiconductor with a slight negative (dipole surface charge barrier) barrier height $\phi_m > \phi_s$ named as ohmic contact. Theoretically, under certain conditions for many semiconductors, the SBH is independent of the choice of metal. However, practically, semiconductors often possess many surfaces or interface states where carriers are trapped as donors or acceptors. The potential difference is formed at the MS interface. Then the Fermi levels at the equilibrium (ϕ_0) will become pinned. Therefore, the SBH is almost independent of the work function and follows the Bardeen limit (function of the semiconductor's bandgap and surface) and expressed by (2.4):

$$q\phi_B = E_g - q\phi_0\,. \tag{2.4}$$

The SBH controls the behavior of ohmic and Schottky contacts, but most of the material properties of SiC that maintain the metal-SiC contact are not fully understood. Hence, predicting the contact behavior is a complex task.

2.3.2. Fermi energy

In equilibrium conditions, the balance band of a p-type semiconductor is filled with charges while the conduction band is empty. As a result, there is no charge; transport is possible within a semiconductor. The electron excitation can bias the conduction band by leaving a hole in the valance band, resulting in both bands becoming conductors. At a particular energy level *E*, in a semiconductor with the Fermi energy E_F can be described by the Fermi–Dirac statistics function (2.5):

$$f(E) = \frac{1}{\exp\frac{E - E_F}{K_B T} + 1}, \tag{2.5}$$

where $K_B T$ is Boltzmann's constant. The equations can calculate the charge carrier densities in the conduction and balance band for n-type semiconductors (2.6) and p-type semiconductor (2.7):

$$n = \int_{Ec}^{\infty} \underbrace{4\pi\left(\frac{2m_n^*}{\hbar^2}\right)^{\frac{3}{2}} \cdot\sqrt{(E - E_c)}.}_{D_C(E)} \left(\frac{1}{\exp\frac{E - E_F}{K_B T} + 1}\right) dE, \tag{2.6}$$

$$p = \int_{-\infty}^{Ev} \underbrace{4\pi\left(\frac{2m_p^*}{\hbar^2}\right)^{\frac{3}{2}} \sqrt{(E_v - E)}}_{D_v(E)} \big(1 - f(E)\big) dE, \tag{2.7}$$

where $\hbar$ is the Planck constant; *Dc (E)* and *Dv (E)* are the densities of the state in the conduction band and valance band, respectively; *M*n,p* is the effective mass of the charge carrier; and E_c and E_v are the conduction and valence band, respectively, for n- and p-type semiconductors.

Replacing (2.5) with (2.6) and (2.7) produces (2.8) and (2.9):

$$n = \int_{Ec}^{\infty} 4\pi\left(\frac{2m_n^*}{\hbar^2}\right)^{\frac{3}{2}} \cdot\sqrt{(E - E_c)}.\left(\frac{1}{\exp\frac{E - E_F}{K_B T} + 1}\right) dE, \tag{2.8}$$

$$p = \int_{-\infty}^{Ev} 4\pi\left(\frac{2m_p^*}{\hbar^2}\right)^{\frac{3}{2}} \sqrt{(E_v - E)}\left(\frac{1}{\exp\frac{E - E_F}{K_B T} + 1}\right) dE. \tag{2.9}$$

Using the Fermi–Dirac integral and considering the effective densities of state and distance band edges higher than $K_B T$ ($\eta_{n,p} >> 1$), for the conduction and valence band with the product of electron and hole concentration (N_C and N_V, respectively), (2.8) and (2.9) can be rewritten as (2.10) and (2.11), respectively:

$$n = N_C . exp\frac{E_F - E_C}{K_B T}, \tag{2.10}$$

$$p = N_V . exp\frac{E_V - E_F}{K_B T}. \tag{2.11}$$

2.3.3. Current transport processes

MS contacts are mainly unipolar, where the majority of carriers are responsible for the majority of current flow. The current transport operation of the Schottky diode follows five of the transport mechanisms that occur under forward bias, illustrated in Fig 2.4. The most dominant mechanism for rectifying contacts is thermionic emission (TE), thermionic field emission (TFE), and field emission (FE), depending on the level of doping within the semiconductor.

Fig. 2.4 shows the current transport mechanisms that depend on the barrier width of the depletion region corresponds to the doping concentration. Fig. 2.4(a) shows thermionic emission, where the carrier within the semiconductor needs to gain enough energy to overcome the considerable barrier height due to low doping concentration. In the forward bias, thermionic emission and majority carrier diffusion are combined, and the current flows from the semiconductor to the metal. However, in reverse bias conduction, the barrier width (w) at the MS interface is too large to overcome, and minimal minority carrier leakage current flows. Other the hand, as the doping concentration increases, the depletion width (w) decreases, and thus field emission increases. Fig. 2.4(c) shows the most important current transport process in the highly doped semiconductor material, namely quantum mechanical tunneling.

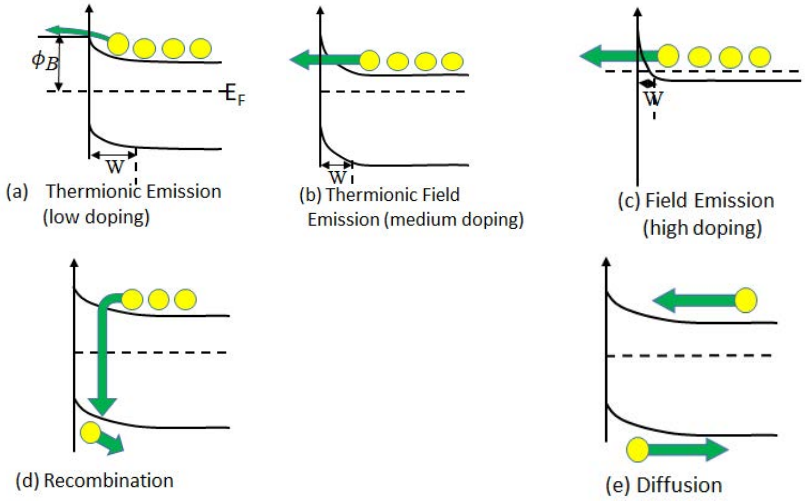


Fig. 2.4: Illustration of current flow mechanisms and their relationships to semiconductor doping: (a) thermionic emission; (b) thermionic-field emission; (c) field emission; (d) recombination; and (e) diffusion.

The band banding takes place at a very thin width or low temperature. This quantum-mechanical tunnel through the thin barrier is called a field emission. The recombination or generation of carriers occurs in the space-charge region of an MS contact whenever the thermal equilibrium is disturbed. Tiny minority carriers diffuse into the depletion region due to the large barrier width shown in Fig. 2.4(d). The diffusion process is indicated in Fig. 2.4(e), where particles move from high concentration areas to low concentration. Some minority carrier injection takes place at high forward bias, with holes diffusing from the metal to the semiconductor. Other sources include edge leakage currents and interfacial currents from traps at the MS contact.

2.4. Doping in semiconductors

Most electronic properties of semiconductors are determined by adding the kind and amount of doping defects into the pure semiconductor. The origin of defects depends on the environmental conditions during growth or process conditions – for example, oxidation, the concentration of each species, and temperature. Semiconductor crystalline defects can be classified as three-dimensional (3D, volume defects) or two-dimensional (2D, planar defects), comprising stacking faults or voids/inclusions, respectively. In one-dimensional (1D) defects (line defects), micropipes and dislocations can be found. By contrast, zero-dimensional defects are called homogeneously distributed point defects. The defect clusters along a primary knock-on atom (PKA) path will discussed in chapters 4 and 5.

2.4.1. Estimation of p-doped material

Equation (2.5) changes significantly according to the dopant (N_A or N_D) of the semiconductor. It can be expressed based on the activation probability with degeneracy factor (g) for donors and acceptors as (2.12) and (2.13), respectively:

$$N_D^+ = \frac{N_D}{\frac{1}{g}\left(\exp^{\frac{E_F - E_D}{K_B T}}\right) + 1}, \tag{2.12}$$

$$N_A^- = \frac{N_A}{g\left(\exp^{\frac{E_A - E_F}{K_B T}}\right) + 1}, \tag{2.13}$$

where E_A is the activation energy. The doping changes the charge carrier density ($n_i = n.p$), which transform the semiconductor n to p and p to n based on:

$$n > \sqrt{n_i} > p \rightarrow n - type \text{ (Case I)},$$

$$P > \sqrt{n_i} > n \rightarrow p - type \text{ (Case II)}.$$

In case I, the concentration of the electron of the conduction band increases, and the hole of the valence band decreases while Fermi energy shifts toward the conduction band. In case II, however, the Fermi level shifts toward the valence band as the hole of valence band increases and electrons of the conduction band decrease. Therefore, the charge carrier density expressed in (2.10) and (2.11) can be expressed as (2.14) and (2.15), respectively:

$$n = N_C N_V \exp\frac{E_V - E_C}{K_B T}, \tag{2.14}$$

$$p = N_C N_V \exp\frac{-E_G}{K_B T}. \tag{2.15}$$

For a high p-type doped semiconductor ($N_D=0$, $n<<p$), (2.13) can be express as (2.16) and (2.17):

$$N_A^- = p = \frac{N_A}{g\left(\exp^{\frac{E_A - E_V + E_V - E_F}{K_B T}}\right)+1}, \tag{2.16}$$

$$p = \frac{N_A}{g\left(\exp^{\frac{E_V - E_F}{K_B T}} \exp^{\frac{E_A - E_V}{K_B T}}\right)+1}. \tag{2.17}$$

By substituting (2.11) into (2.17), one can obtain (2.18) and (2.19):

$$p = \frac{N_A}{g\left(\frac{p}{N_V}\exp^{\frac{E_A - E_V}{K_B T}}\right)+1}, \tag{2.18}$$

$$p = \frac{N_A}{g\left(\frac{p}{N_V}\exp^{\frac{E_a}{K_B T}}\right)+1}. \tag{2.19}$$

The cubic equation (2.19) for p can be solved by (2.20):

$$p = \frac{N_V}{2g}\exp^{-}\left(\frac{E_a}{K_B T}\right)\left[\sqrt{1+\frac{4N_A g}{N_V}\exp\left(\frac{E_a}{K_B T}\right)}-1\right], \tag{2.20}$$

where E_a is the activation energy for a p-doped semiconductor, expressed as the distance of the band edges formulated as $E_a = E_A - E_V$. Similarly, for the n-doped semiconductor, the activation energy can be expressed as $E_d = E_C - E_D$.

For a p-type doped semiconductor where $K_B T<<E_a$ or $\exp^{\frac{E_a}{K_B T}} >>1$, (2.19) can expressed as (2.21):

$$p = \left(\sqrt{\frac{N_V N_A}{g}}\right)\exp^{\frac{-E_a}{2K_B T}}. \tag{2.21}$$

2.4.2. Point defects in semiconductors

Point defects are unavoidably created during the growth process or intentionally introduced into the semiconductor material – for example, ion implantation – or unintentionally during growth – post-processing or device fabrication in a particular procedure to tailor the material's electronic properties. The annealing process reduces the lattice damage created and activates the dopants electrically. The annealing procedure has to be chosen in an appropriate way to maintain, at a minimum, the formation of electrically inactive complexes. Therefore, investigating the annealing

behavior of intrinsic defects and dopant atoms is crucial for optimizing the doping procedure, as discussed in [Paper III]. Nevertheless, there is a need to study and to understand the multitude of radiation-induced intrinsic defect centers, origin and structure creation of defects, and annihilation effects on 4H-SiC.

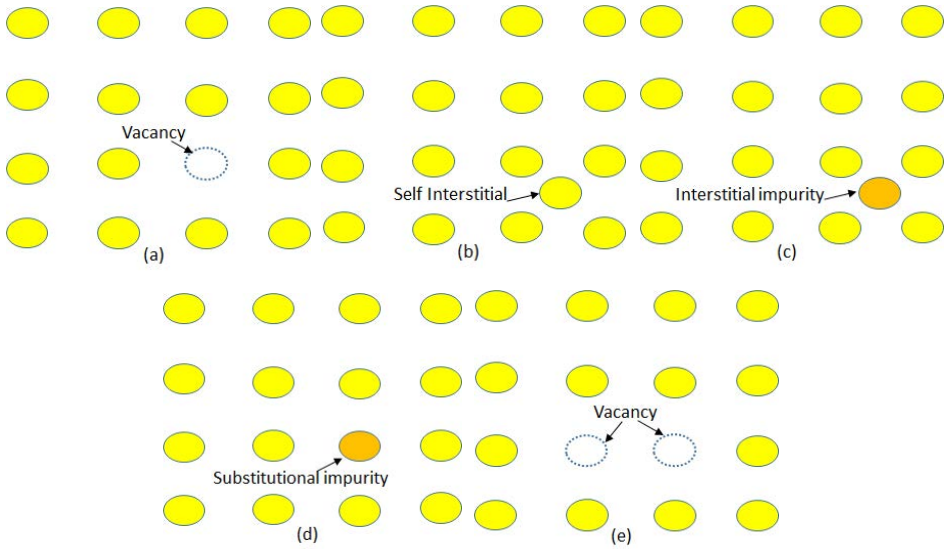


Fig. 2.5: Schematic of different point defect types: (a) vacancies; (b) self-interstitials; (c) interstitial impurity (antisite); (d) substitutional impurity (antisite); and (e) di-vacancy.

Doping is mainly an intrinsic and impurity type introduced within the fundamental bandgap for carrier capture or emission either close to the band edge (shallow defects) or near the midgap (deep level defects) on the energy of the impurity atom or annealing temperature. In most of the cases in semiconductors, shallow defects (hydrogen like) called dopants are introduced intentionally and act either as donors (if they provide an electron) or as acceptors (if they can catch an electron). Suppose the concentration of dopants N_A or N_D is high enough in a particular semiconductor. In that case, the excess charge carrier (electron and holes) distribution of the semiconductor will be changed significantly to the conduction (CB) or valance bend (VB).

Fig. 2.5 illustrates the three main types of point defects in semiconductor atoms: vacancies (missing atoms), interstitial impurities, and substitutional impurities. A vacancy is an unoccupied lattice site. An interstitial is an additional atom between lattice sites. An antisite is an atom of one species residing in a lattice site occupied by an atom of another species in compound semiconductors. These point defects in semiconductor crystal structure occur by hopping or kick out, where the impurity atom replaces these interstitial sites and may constitute substantial impurity on a random path. However, the generation of interstitial impurity defects is an unintentional and rapid development process compared with the substitutional impurity process (vacancies need to be generated for substitutional impurities). Several point defects that occur in SiC are discussed below.

2.4.3. Point defects in SiC

Although there has been notable industrial maturity and the availability of large, high-quality SiC substrates, point defects have recently gained more attention. All SiC samples used in this study are p-doped with aluminum, which supplies an additional valence hole compared with intrinsic semiconductor elements as an acceptor. This particular study of p-type 4H-SiC SBD concerns point defects that might limit the performance of devices and control the electronic properties of materials. The identifications of various defects in SiC and their scopes have been discussed in [20]–[25].

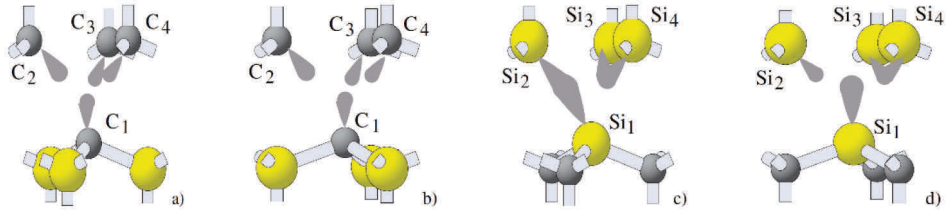


Fig. 2.6: Structural diagram of the vacancies in 4H-SiC: (a) V_{Si} at a cubic lattice site; (b) V_{Si} at a hexagonal lattice site; (c) V_C at a cubic lattice site; and (d) V_C at a hexagonal lattice site [23].

Despite substantial efforts, rather few point defects in SiC have been identified unambiguously both experimentally and theoretically for atomic structure, optical, paramagnetic, and electronic properties. According to the literature, carbon vacancy (V_C) [26], silicon-vacancy (V_{Si}) [27], divacancy (V_CV_{Si}) [28], and intrinsic defects have been found by various methods (Fig. 2.6).

Carbon vacancy (V_C): V_C is an electrically active defect in a deep level formed at lower energy (≈2.7 eV) and stable for all doping conditions [24]. This phenomenon can produce positive (V_C+) and negative (V_C -) states in the bandgap due to two different resonance spectra, as has been identified by electron paramagnetic resonance (EPR) in [26], [29], and [30]. Due to strong site dependence, this defect has a different structure for the k and h sites. The V_C in n-type 4H-SiC, labeled as $Z_{1/2}$ deep-level defects, is a well-known lifetime killer.

Silicon vacancy (V_{Si}): V_{Si} is a formed at energy of 3–4 eV due to a metastable defect for specific doping conditions and high spin ground states (stable in n-type and metastable in intrinsic and p-type SiC), as reported by [23], [31], and [32]. The nature of V_{Si} makes it favorable for positively doped and forms of intrinsic defects in group III–V compounds. References [33]–[35] expressed that V_{Si} does not process the Jahn–Teller reconstruction. As a result, carbon dangling bonds cannot be formed but point inwards to the vacancy. Bockstedte *et al*. [23] noticed V_{Si} in p-type material despite its metastability due to electron irradiation.

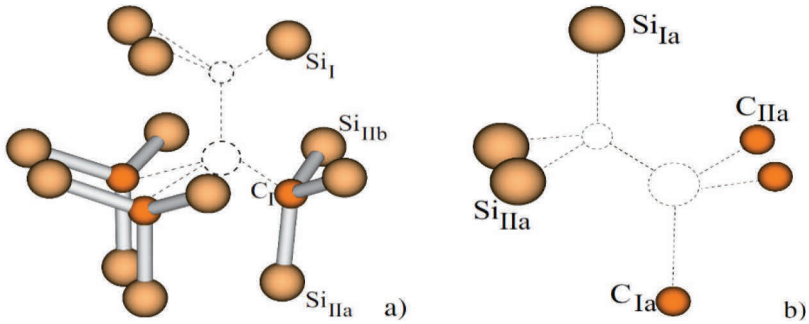


Fig. 2.7: Di-vacancy in a 4H-SiC lattice site: (a) axial complex V_C–V_{Si} (kh) at a hexagonal site and (b) off-axis complex V_C–V_{Si} (kh) [23].

Divacancy (V_CV_{Si}): Divacancy at a hexagonal site in 4H-SiC generically occurs in the nearest neighbor element or compound of the intrinsic vacancy complexes. This divacancy is predicted to be a thermally stable defect, with a dissociation energy of 4.5eV, as discussed by [23] and [36]–[38] and shown in Fig. 2.7.

Antisite defects: Inequivalence of lattice sites in 4H-SiC, antisite can be a carbon atom residing in a silicon site (Si_C) or a silicon atom occupied by the carbon antisite (C_{Si}) [38], [39]. Umeda *et al*. noted other possibilities of forming antisite defects are carbon antisite–carbon vacancy pairs ($C_{Si}V_C$) [40], or antisite–antisite pairs (Si_CC_{Si}) [41].

Defect cluster: Semiconductor clusters can be formed by agglomeration of several point defects or a defect complex (a minimum of two antisites) to create a carbon cluster together with the surrounding carbon atoms [42], [43]. The cluster can be created with a high defect density introduced after fast irradiation or during the annihilation stage of the implantation or post-implantation through the migration of point defects. Besides their composition of vacancies and interstitials, no information about their exact nature or their electrical properties within the space charge region or in their thermal equilibrium is known. According to the model of Gossick [44], many Frenkel pairs are produced in the cluster region by a PKA. According to Smirnow [45], the defects in the cluster act as recombination and generation centers. This defect cluster is formed in small regions (about 15 nm in diameter [44]) containing high defects. Gossick [44] reported that this cluster acts as a high minority carrier recombination center after gamma or electron irradiation. However, the effect is not well known due to a large number of defects collide in a small size, such as a cluster that cannot even calculate using computer simulation due to limited CPU time.

2.5. Deep-level defect states

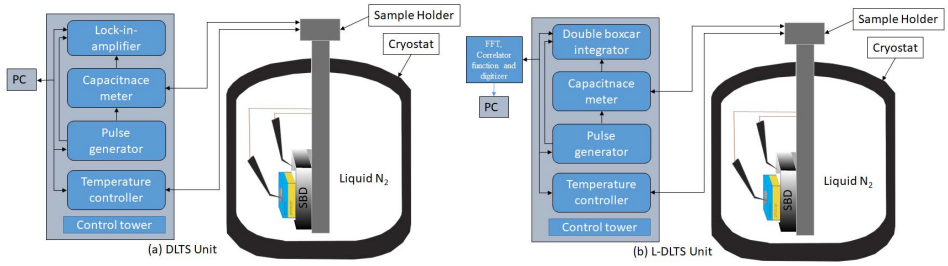


Fig. 2.8: Schemes of the setups for (a) conventional DLTS and (b) LDLTS with a cryostat at Taltech.

According to the previous discussion, deep-level defects may emanate from impurities or dangling bonds in the deeper position of the bandgap compared with the dopant levels. Their highly localized nature may introduce isolation with higher ionization energy. They are desirable for fast switching devices where quick removal of a minority carrier is necessary. The deep-level defects in indirect bandgap semiconductors like SiC diodes often interact with the growth process conditions or during irradiation and degradation in diode performance due to the trapping and de-trapping nature of charge carriers. Therefore, it is necessary to understand the process, for example, the interaction of charge carriers with deep-level defects during capture and emission of charge into the valence and conduction band that act as a center for electron-hole generation or recombination.

Such interactions could potentially hinder the doping process and reduce the net carrier concentration compared with the desired value. Shockley Read and Hall described this interaction using four different statistical approaches: (a) electron capture, (b) electron emission, (c) hole capture, and (d) hole emission kinetics at thermal equilibrium. Various experimental techniques, including DLTS or LDLTS, thermally stimulated current (TSC), minority carrier transient spectroscopy (MCTS), thermally dielectric relaxation current (TDRC), EPR, and photoluminescence (PL) spectroscopy, and measurements of the Hall constants, give information about the nature and the properties of defect centers. However, in this work, DLTS/LDLTS has been implemented based on charge capture or emission and capacitance transient methods shown in Fig. 2.8. LDLTS employs isothermal DLTS and a regularized inverse Laplace transform instead of the conventional lock-in-amplifier analysis. LDLTS can improve the emission rate resolution by an order of magnitude and separate closely spaced transients when several defects with similar emission characteristics are present.

2.5.1 Charge carrier kinetics

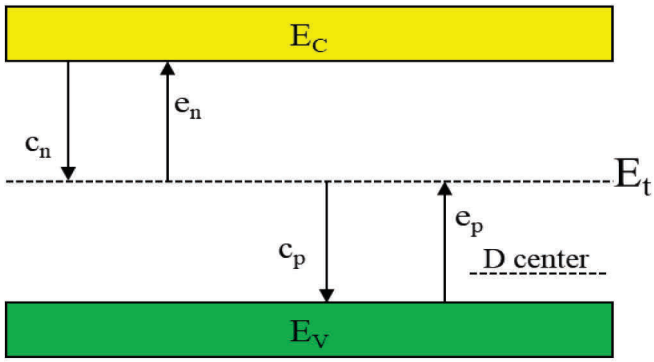


Fig. 2.9: Schematic of charge carrier kinetics for capture (denoted by c_n and c_p) and emission (represented by e_n and e_p) with mid-energy level E_t for a deep-level defect at thermal equilibrium (modified from [46]).

In indirect semiconductors like SiC, the recombination process is mainly governed by the charge carrier transition (called transition energy, E_t) via a localized energy state within the forbidden energy band gap [46]. The transition energy probability depends on the energy difference between the conduction (E_C) and valence (E_V) band edges. This transition energy is considered an intermediate or mid-energy state that can interact with the band edges and intensify substantially the recombination process. The charge carrier transition by the defect between the band edges is determined by the defect capture ($c_{n,p}$ denoted as electron and hole capture) and emission ($e_{n,p}$ represent electron and hole emission) rates for electrons and holes shown in Fig. 2.9. At equilibrium, the transition rates between conduction and valence band edge will be the same (thus, one electron or hole can occupy a defect center) and act as a trap (when $c_n >> c_p$ → electron trap or $c_p >> c_n$ → hole trap) or a recombination center ($c_n \approx c_p$). Using (2.10), (2.11), and (2.21), one can express the emission rates as (2.22) and (2.23):

$$e_n = c_n n_i \exp\left(\frac{E_t - E_i}{K_B T}\right), \tag{2.22}$$

$$e_p = c_p n_i \exp\left(-\frac{E_t - E_i}{K_B T}\right), \tag{2.23}$$

where n_i is the intrinsic carrier concentration and E_i is the initial energy. By introducing intrinsic carrier density of electron (N_C) and hole (N_V) in (2.22) and (2.23), respectively, the emission rates can be rewritten as (2.24) and (2.25):

$$e_n = c_n N_C \exp\left(\frac{E_t - E_C}{K_B T}\right), \tag{2.24}$$

$$e_p = c_p N_V \exp\left(-\frac{E_t - E_V}{K_B T}\right). \tag{2.25}$$

By considering the entropy factor X and introducing the entropy ΔH for an electron and a hole, it can also express the above equations as (2.26) and (2.27):

$$e_n = c_n X_n N_C \exp\left(-\frac{\Delta H_n}{K_B T}\right), \tag{2.26}$$

$$e_p = c_p X_p N_V \exp\left(-\frac{\Delta H_p}{K_B T}\right). \tag{2.27}$$

The unknown values of X_n, X_p, C_n, and C_p are usually defined by the capture cross-section σ_n and σ_p for electron and hole, respectively [46]. Hence, the emission rate in (2.24) and (2.25) can be rewritten as (2.28) and (2.29), respectively:

$$e_n = \sigma_n v_{th_n} N_C \exp\left(-\frac{\Delta H_n}{K_B T}\right), \tag{2.28}$$

$$e_p = \sigma_p v_{th_p} N_V \exp\left(-\frac{\Delta H_p}{K_B T}\right). \tag{2.29}$$

The capture cross-section σ_n and σ_p of the electron or hole and the thermal velocity V_{th} of electrons and holes express the carrier concentration in the conduction and valence band edge. If the capture cross-section is independent of entropy ΔH, the emission rate can be obtained as (2.30) and (2.31):

$$e_n = \sigma_n v_{th_n} N_C \exp\left(-\frac{\Delta E_n}{K_B T}\right), \tag{2.30}$$

$$e_p = \sigma_p v_{th_p} N_V \exp\left(-\frac{\Delta E_p}{K_B T}\right), \tag{2.31}$$

where ΔE_n or ΔE_p is considered the activation energy of an electron or a hole, respectively. However, if the defect charge carriers are thermally excited, the electron or hole are emitted from the conduction or valence band. Thus, the activation energy changes according to the Gibbs free energy.

2.6. Conclusion

In this chapter, a basic understanding of SiC crystal structures and the MS contact theory has been provided. The main concern of several defects in SiC and the consequences of the current transport properties and deep level defect characterizations techniques (namely DLTS) have been covered theoretically. This information should provide a better understanding of the subsequent chapters.

3. Fabrication of SiC Schottky diode

The bonding of SiC wafers can be divided into three categories: (a) bonding with a conducting interlayer, (b) bonding with an insulating interlayer, and (c) bonding without an intermediate layer. All of these categories are used extensively in the microelectronics industry. Direct bonding is a wafer-bonding process without additional intermediate layers [47]. Surface passivation is a crucial issue in the success of SiC device technology. Research has shown that achieving a level of surface roughness for extensive area bonding is also very difficult because of the hardness and inertness of SiC and renders most chemical and ineffectiveness (most of the case) of chemical-mechanical polishing processes. It is worth noting that surface conditions such as roughness and contaminations make the SiC wafer-bonding process more challenging. The physical or adhesive bonding mechanism is used in the DW, where mass transfer in the form of chemical reaction and diffusion across the interface. This chapter covers the direct bonding process, provides a short review of this technology, covers the cleaning process used in this work, and discusses in detail the mechanisms.

This chapter is based on the following publications:

- M. H. Ziko, A. Koel, T. Rang, and M. H. Rashid, "Investigation of barrier inhomogeneities and electronic transport on Al-Foil/p-Type-4H-SiC Schottky barrier diodes using diffusion welding," *Crystals*, vol. 10, no. 8, Art. no. 636, 2020.

- M. H. Ziko, A. Koel and T. Rang, "Characterization of Al-foil/p -4H-SiC SBDs Fabricated by DW with Variation of Process Conditions," preented at the 2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Suita, Japan, 2020, pp. 1–5.

3.1 Introduction

From a physical point of view, contact or joining occurs when more than one body and their asperities come together simultaneously in the enforcement condition where no point in space can be occupied. Fig. 3.1 shows two 2D bodies that can be denoted as a contractor (as metal) and target (as SiC). According to the principle of contact/joining along the impacting boundaries, no element overlap can occur [48]. This mechanical joining produces many a-spots of asperities on the two surfaces. Greenwood and Williamson [49] introduced the asperity-based joining models that depend on the deformation model based on elastic, plastic, and elasto-plastic material. Therefore, metal and SiC joining analysis can be influenced by the bonding materials, cleaning process, the roughness of joining materials (created by chemical reaction, chemical and mechanical polishing [CMP], or micro-scale deformations), stiffness properties, and various phenomena. This work used Al-foil and Au as contact materials and p-type 4H-SiC as target material to prepare SBDs using DW and sputtering, respectively. DW and comparison with other direct bonding technologies are described in this chapter, and bonding-impacted boundaries and their interfaces will be discussed in chapter 4.

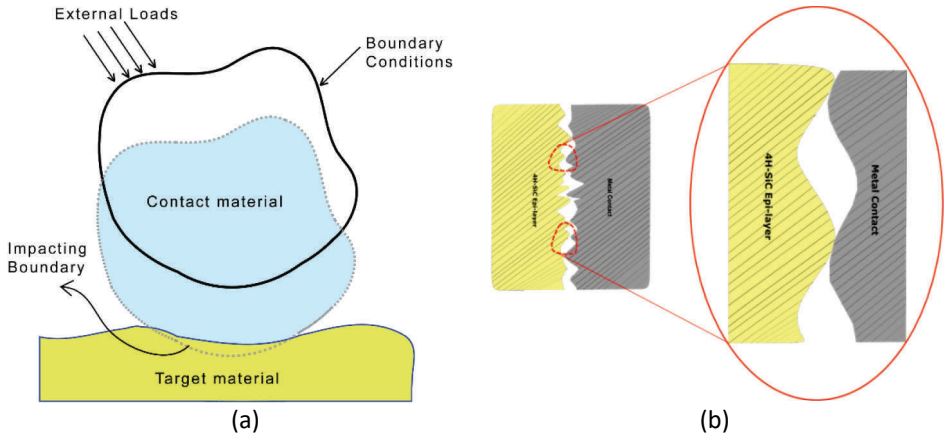


Fig. 3.1: (a) A schematic of two 2D bodies joining after bonding and (b) their a-spots of asperities.

3.2 Contact material properties

Aluminum contact metal: The contact material selection could be strongly coupled to the power diode electrical and mechanical design and application area. So, contact material properties are essential parameters for the design of an SBD. Aluminum has some unique properties such as a very low density, corrosion resistance, long-term high thermal stress stability, and low process temperature (melting point below 650°C). Moreover, the extremely low solubility of carbon (~0.1%), and silicon (> 1.5%) in solid aluminum at welding temperature (~600°C) makes it a vital material in high current density and high-temperature applications [50], [51]. Negoro *et al*. [52] noted that only the silicon atoms of SiC contribute to the reaction process of solid-state solving. Aluminum coupled with silicon (AlSi) seems to be less susceptible to defect formation. Unreacted carbon atoms combined with aluminum lead to anisotropic etching, after which the surface remains smooth and polished. It would be expected that the carbon precipitation takes place at the interface during the cooling state in DW (discussed in forthcoming section-3.5). At the substrate side, the Al-foil is used to form ohmic contacts on p-type 4H-SiC. During the fabrication (annealing) process, aluminum diffuses into the semiconductor surface, increases the doping concentration, and reduces the SBH. Thus, desirable ohmic contact on p-type 4H-SiC is observed at the substrate side.

Gold contact metal: Gold (Au) has been the most widely used metal among the candidate contact metals in SBD interconnection and packaging schemes because of its low resistivity, high resistance to oxidation [53], and high current density. However, thick Au sputtered layer have also been used to investigate the current density and defect analysis.

3.3 Review and mechanical arrangement of DW

DW involves the joining of dissimilar materials – that is, metals, metal-glass, metal-ceramic, and ceramic-glass – either directly or through the use of interlayers [54]–[56]. DW bonding is produced by applying pressure and temperature to carefully cleaned and mated metal surfaces so that they grow together by atomic diffusion. Takagi *et al*. [57] discussed Takahashi and Onzawa's proposed model to calculate the force applied to press two

dissimilar materials considering the surface morphology by summation of sinusoidal curves. This process needs to satisfy conditions that do not involve any melting or relative motion of different materials. Besides, limiting the macroscopic deformation of the contact participants requires an entirely controlled condition.

Fig. 3.2 illustrates the classification of low and high temperature direct bonding techniques for metal and glass. Surface activation bonding (SAB), DW, and ZiBond^{TM} have been investigated widely for MS or glass bonding technology. The procedural steps for SAB and ZiBond^{TM} of any metal surfaces are divided into wafer preprocessing or surface preparation, pre-bonding at room temperature, and annealing at elevated temperatures. These bonding processes are based on the chemical bonds between the two atomically smooth, flat surfaces, which adhere to each other at annealing temperatures. However, DW bonding is a one-step process, and the bonding strength is a function of temperature and applied pressure.

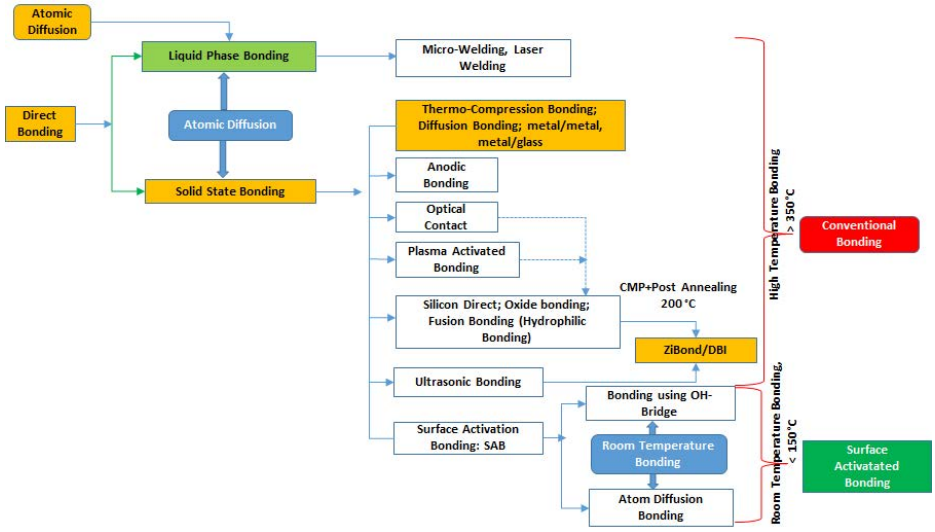


Fig. 3.2: The classification of low and high temperature bonding techniques for metal and glass.

The surface preparation for DW is effortless, as discussed in [Paper III]. In contrast to DW bonding, SAB is used for SiC–SiC, SiC–Si, or SiC–metal bonding with a low temperature or room temperature by plasma activated and modified the contact surfaces without pressure applied.

Table 3.1: Comparison of bonding methods, modified from [58] and the work in this thesis.

Bonding method	Hydropilic & Hyropobic Bonding	Plasma Activated Bonding	Surface Activated Bonding	TTU Diffusion Welded Bonding	ZiBondTM
Bonding materials	Si, SiO_2 and other III-IV Semiconductor	Si, SiO_2 and other III-IV Semiconductor	From metal to semiconductor ceramics except SiO_2	From metal to semiconductor ceramics except SiO_2	Effective for SiO_2
Cleaning process	Simple	Simple	Simple	Simple	Complicated
Bonding Strength at RT	Weak	Weak	Strong	Strong	Strong
Annealing Temperature	800-1000° C	200-400° C	Not Required	N/A	Not Required
Stress Free	NO	No	Yes	Yes	Yes
Void formation during annealing	Frequent	Frequent	No void	No void	N/A
Ambient atmosphere in the bonding process	Atmospheric pressure	Atmospheric pressure to low vacuum	Low vacuum to UHV	HV	Atmospheric pressure
Cost of Wafer bonder	Low	Low	High	Low	Low

Surface preparation prior to DW is simpler than for SAB. Table 3.1 provides a comparison of the various bonding methods. DW is feasible and less expensive compared with the other bonding methods. The wafer surfaces must be sufficiently clean, flat, and smooth should to use in the DW bonding.

3.4. Surface cleaning, contamination, and bonding process

Sample preparation procedure

The SiC wafers that were used for this SBD study were purchased from Cree, Inc. (Durham, NC, USA). These SiC wafers are p-type with a diameter of 76 mm and an average resistivity of 4.85 Ω-cm. The 350-µm thick wafers were doped with aluminum with a concentration of 1×10^{18} cm^{-3}, followed by 10 µm thick p-type epitaxial layers doped to a concentration of 1×10^{15} cm^{-3}. Si-face 4H–SiC (0001) 4° off-axis surface orientation has been polished by the chemical mechanical method on the bonding face of the wafer (i.e., the side to which diffusion bond will be made). All of the wafers were diced into 10×10 mm^2 samples.

The next endeavor involved surface preparation and cleaning, performed in three sequential steps. First, each sample was cleaned with a dredge in methanol for 5 min. Then, the sample was dipped in a solution of 48% diluted hydrofluoric acid (HF), consisting of 25:1 H_2O:HF for 5 min to remove any native silicon dioxide (SiO_2) on the front and backside of the surface epilayer and substrate layer, respectively. In the next step, the samples were dredged by rinsing in normal water for 5 min. Finally, each sample was cleaned in deionized (DI) water at room temperature for 5 min.

DW was used to deposit the Al-foil as a metal contact with a diffusion pumped chamber at a base pressure of not less than 1×10^{-4} mbar. The Al-foil and SiC surface were brought into contact with each other under the pressure of 750 N (for 5 min) at welding temperature of 575°C for 5 min. Finally, 100-µm thick Al-foil was welded as an ohmic contact on the entire surface backside of the SiC substrates, and 60-µm thick of Al-foil was welded as a Schottky contact on the center of the SiC epitaxial layer.

The SiC SBD sample preparation and deposition parameters are well described in [Paper III] and [Paper IV]. The formation of the bond at the interface determined the reliability of the joints, depending on the processing condition of the joining materials.

All surface contamination, particles between the metal (Al) and 4H-SiC/Al surface, act as spacers that strongly decrease intermolecular bonds. Size and coverage density may lead to the creation of unbonded areas and even completely prevent bonding between metal and semiconductor. The nucleation of interfacial voids may cause organic contamination during the annealing step (in-build process during bonding). In the same study, it is observed that small amounts of metal contaminants are usually present at the surface, but this presence does not affect the adhesion of sample/wafer. However, they may strongly affect the electrical properties of the interface and thus may be harmful to electronic applications of Al-foil/4H-SiC/Al bonding.

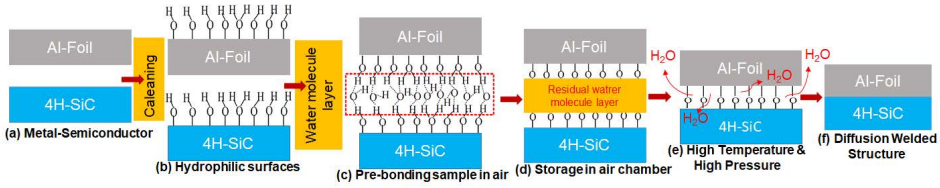


Fig. 3.3: Overview of the Al-foil/4H-SiC DW pre-/post-bonding process.

Fig. 3.3 shows the pre-/post-bonding process for the Al-foil/4H-SiC DW technology. The cleaned Al-foil and 4H-SiC exhibit hydrophilic affinity with the -OH group shown in Fig. 3.3(b). This group can enhance markedly the pre-bonding strength. When the Al-foil and 4H-SiC were brought together in moist air, they primarily bond together via a 3D network of hydrogen bonds with polar -OH and water molecules shown in Fig.3.3(c).

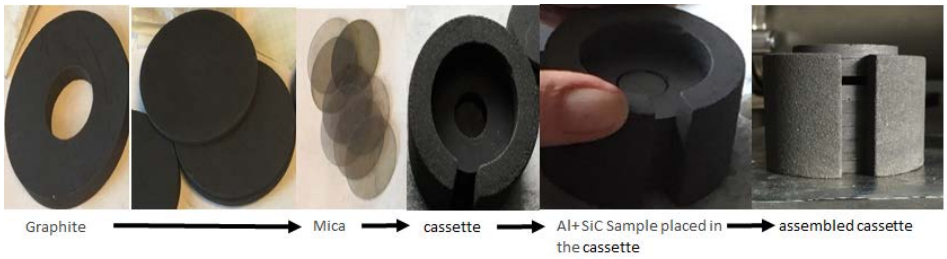


Fig. 3.4: Images of cassette stack preparation for DW bonding.

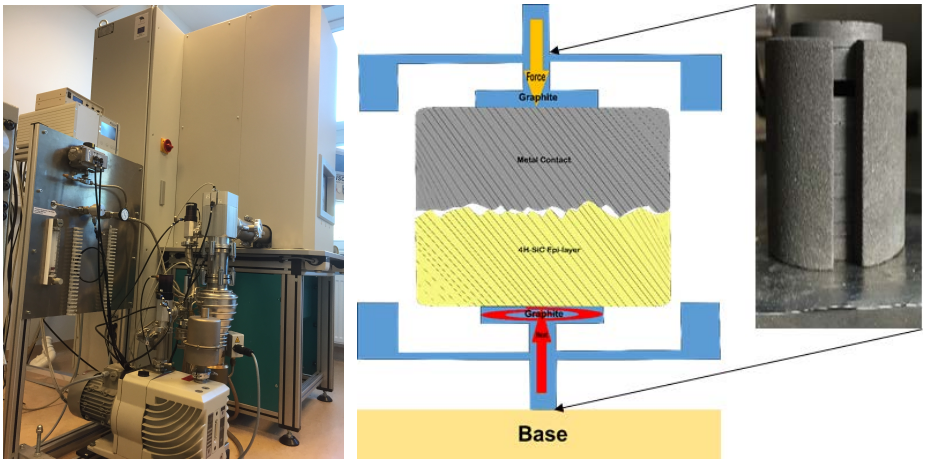
This pre-bonded Al-foil/4H-SiC/Al-foil stack shown in Fig. 3.3(d) was placed in a cassette, as shown in Fig. 3.4. The stack comprising an electrode support material that was compressed before vacuuming the chamber. At this stage, some of the water molecules were sprinkled on the mating surfaces. This special cassette with the stack was placed in the operating chamber under a vacuum of 0.07 MPa before starting DW. At this stage, the majority of the pre-bonding water molecules evaporate, and only a few water molecules remain at the end. These evaporated water molecules interact with Al and lead to the Al-OH interactions. During DW, the bonding strength increases, with hydrogen bonds are converted into the strong Al-O-Al covalent bonds by the dehydration reactions presented in (3.1)–(3.4) [59].

$$Al\text{-}OH + Al\text{-}OH \rightarrow Al\text{-}O\text{-}Al + H_2O \quad (3.1)$$

$$SiO_2 + 4H + 6F \rightarrow SiF_6 \rightarrow SiF_6 + 2H_2O \quad (3.2)$$

$$SiC + O_2 \rightarrow SiO_2 + CO_x \quad (3.3)$$

$$SiC + H_2O \rightarrow SiO_2 + H_2 + CO_x \quad (3.4)$$



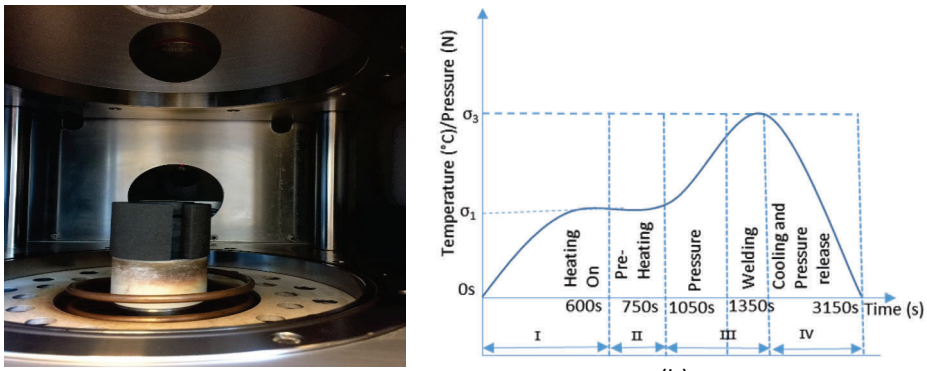
(a) (b)

Fig. 3.5: Illustration of (a) diffusion bonding system and (b) schematic of bonding using electrical resistance for heating.

Fig. 3.5 illustrates the DW system and a schematic of bonding using electrical resistance for heating. Because DW is performed in a vacuum at elevated temperature and high pressure, the water molecules diffuse out along the interface and diffuse with the COx and SiO_2 (internal process shown in Fig.3.3(e)). At this stage, there are three major types of surface forces: van der Waals forces, electrostatic forces, and short-range forces. The latter become effective when the atoms of two contacted surfaces are very close (0.2 nm). Surface forces between the two metal semiconductors determine their adhesion upon initial contact. When electron clouds of the two atoms start overlapping with each other, a bond is formed; covalent bonds are prevalent in SiC. In this chamber, the formation of a smooth and uniform bonding interface is shown in Fig. 3.3(f). The details of the bonding mechanism will be discussed in chapter 3.5.

3.5. Diffusion bonding mechanism

Fig. 3.6(a) illustrates the mechanical assembly of the cassette stack used for DW, employed in forging and equipped to pressurize from three directions for 10 min; this approach ensures consistent bond formation.



(a) (b)

Fig. 3.6: (a) The cassette position in the operational space of the welding machine and stack and (b) the kinetic curve of the process of dissimilar crystalline material bonding during DW.

Higher carbon diffusion coefficients are observed for p-type type SiC (Al doped) than n-type (N doped) SiC within the same temperature range [60]. Moreover, the self-diffusion carbon charged vacancies and vacancy-impurity complex in the Al-foil/4H-SiC SBD are not well understood. The diffusion flux and the concentration gradient at some particular point in the Al-foil/4H-SiC SBD manufacturing process vary with time can be represented by Fick's second law (3.5):

$$\frac{\partial c}{\partial t} = \frac{\partial}{\partial x}\left(D \frac{\partial c}{\partial x} \right), \tag{3.5}$$

where D is diffusion coefficient (m^2S^{-1}), $\frac{\partial c}{\partial x}$ is the concentration gradient. This model is implemented in the temperature and pressure response to time and bonding stress (σ) propagated during the processing. This kinetic curve is shown in Fig. 3.6(b), used for the diffusion-welded p-type SiC SBD development. An in-depth understanding of the diffusion process can be explained in four stages.

I. Electrical resistance for heating operations is carried out for 10 min to heat the oven within the chamber shown in Fig.3.6(a). The kinetic curve in Fig. 3.6(b) starts with heating up (bonding stress σ1) the chamber, a process that corresponds to the end of cycle 1. The thick ductile Al-foil is close enough where Al is fragile. The interplay between the molecules of the SiC epilayer surface and substrate surface interactions is initiated at asperity tips shown in Fig. 3.7(a). To obtain highly stable molecular structures, van der well forces between molecules undergo chemical reactions triggered by heat or voltage pulses to form covalently linked low-dimensional molecular architecture.

II. The duration of this period is conditioned by the continuation of high temperature and involves diffusion and growth grains between the interface to complete the weld and to eliminate the interface. The outcome of this stage is the plastic deformation of the Al-foil, yielding, and creep that leads to fewer voids, as shown in Fig. 3.7(b).

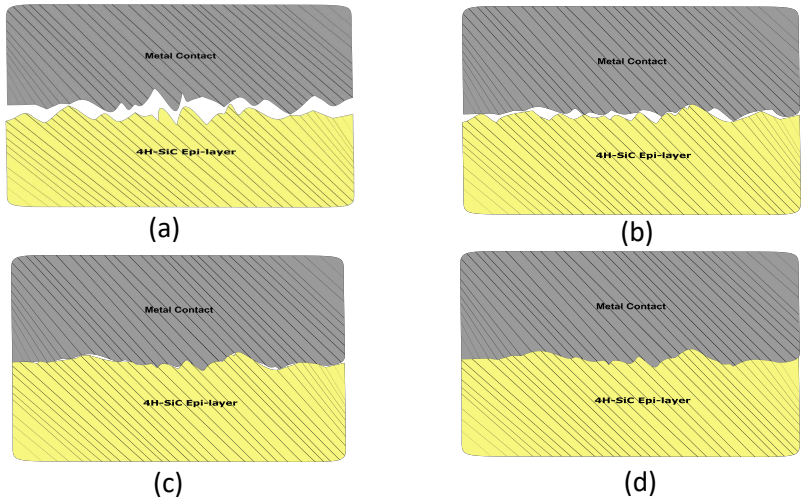


Fig. 3.7: Asperities between Al foil-4H-SiC (a) cycle 1; (b) cycle 2; (c) cycle 3; and (d) cycle 4.

III. The pressure and welding (below the melting point of the metal for only 5 min at the stage; process bonding stress σ3) begins at 750 s and lasts until 1350 s, and the active center is formed. In this cycle, deformation continues primarily in the Al-foil coupled with 4H-SiC diffusion mass transfer, leading to shrinkage of the interfacial voids shown in Fig. 3.7(c). The primary purpose of this strategy is to increase the bonding interactions between the materials at the interfaces.

IV. After the third cycle, bulk interactions develop, and the cooling process starts after Al-foil and 4H-SiC SBD have bonded perfected [61]. Of note, the real microscopic Al-foil and 4H-SiC surfaces are rough, and some contact areas of the bonding could have bonded already, and some could have started. The outcome of this stage is to form a bond, ideally as a perfect interface boundary with or without a few small voids. The process temperature parameter is the most influential factor in DW because a slight temperature change will lead to a significant difference in the kinetics, including plastic deformation and melting-related defects at the interfaces [62], [63].

The parameters have to follow the curve shown in Fig 3.6(b) because micro-roughness, macroscopic surface roughness or waviness, and surface contaminations have to be tightly controlled. Otherwise, there might unbonded areas called voids – that is, interface bubbles.

3.6. Conclusion

In this chapter, contact materials and their properties have been discussed briefly with regard to the compatibility of SiC SBD development. DW is a high-temperature bonding that is a simple, robust, and void-free bonding process compared with plasma bonding and SAB. DW is the only high bonding technique that can join any thick metal with semiconductors and glass-like substrates. It has been described DW alongside mechanical arrangement and the cleaning process. The sample preparation, chemical bonding, and the physical understanding of the bonding mechanism have been discussed. Overall, the low process cost and novel one-step technique can manufacture semiconductor devices that can fulfill high current density and high-power applications.

4. Model conformation and characterization of p-type SiC Schottky diodes

Diffusion-welded Al-foil/p-type-4H-SiC and Au-sputtered/p-type-4H-SiC SBD bonding failures can be characterized as electrical contact failures, unbonded areas, voids, or insufficient bond strength. The reliability of p-type-4H-SiC SBD performance has been examined in two ways: electrical characterization of SiC SBD devices and microscopic measurement techniques. Compliance with design parameters, the stability of process parameters, and quality assurance such as defect density and smoothness of the device surface after cleaning are described with the electrical and microscopic measurement techniques. Improvement before and after device fabrication devices have been evaluated with conformation modeling using microscale simulation (I–V and C–V) and experimental (I–V, C–V, DLTS, and LDLTS) electrical characterization. For quality assurance of the devices, non-destructive methods – AFM and XPS – and destructive methods – SEM and TEM – have been used. These measurement methods will be discussed in the latter part of this chapter (section 4.5).

This chapter is based on the following publications:

- M. H. Ziko, A. Koel, and T. Rangs, "Numerical Simulation of P-Type Al/4H-SiC Schottky Barrier diodes," presented at the 16th Biennial Baltic Electronics Conference (BEC), Tallinn, Estonia, Oct. 8–10, 2018, pp. 1–4.

- M. H. Ziko et al., "Analysis of barrier inhomogeneities of P-Type Al/4H-SiC Schottky barrier diodes," *Mater. Sci. Forum*, vol. 1004, pp. 960–972, July 2020.

- M. H. Ziko, A. Koel, T. Rang, and M. H. Rashid, "Investigation of barrier inhomogeneities and electronic transport on Al-foil/p-Type-4H-SiC Schottky barrier diodes using diffusion welding," *Crystals*, vol. 10, no. 8, Art. no. 636, 2020.

- M. H. Ziko, A. Koel, and T. Rang, "Characterization of Al-foil/p -4H-SiC SBDs fabricated by DW with variation of process conditions," presented at the 2020 IEEE Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia), Suita, Japan, Sep. 23–25, 2020, pp. 1–5

4.1. Conformation modeling of DW p-type 4H-SiC SBD

The numerical simulation of SBDs was carried out using a 2D simulator, Silvaco ATLAS TCAD software, that solves the basic set of semiconductor equations [64]. This software considers all physics and material-related parameters during the simulations of semiconductor devices. Thus, the results obtained from the simulations are very close to the physically fabricated devices. They allow more precise and accurate modeling of semiconductor devices. The simulated p-type-4H-SiC-based SBD device included 25 nm, taken as a reference from Taltech research group investigation on DW bonding [5] defective metal film on the thin epilayer [Paper I]. The I–V and C–V characteristics of the simulation have been solved using electrostatic Poisson's equation and continuity equations for electrons and holes. Calculation of I–V and C–V characteristics was applied

to the thermionic emission theory. The electron–phonon interaction, quantum-mechanical tunneling through the barrier, and barrier height influence of the image force effect diode-like behavior can be mimicked by applying a clean metal to a clean semiconductor. The simulation flow chart and parameters associated with this device are shown in Fig. 4.1, taken from [Paper I]. Forward and reverse I–V, reverse C–V, reverse breakdown voltages, impact ionization simulation, and their results are discussed in [Paper I] and [Paper II].

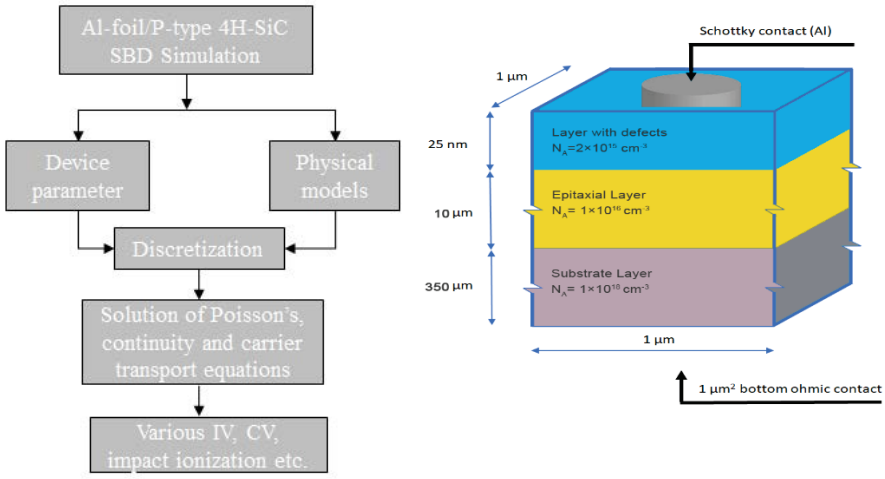


Fig. 4.1: (a) Simulation flow chart and (b) simulated device [Paper II].

4.2. Electrical characterization of diffusion-welded Al-foil/p-type 4H-SiC SBD

This section discusses temperature-dependent I–V and C–V characteristics, the ideality factor, the doping concentration plot, and DLTS and LDLTS measurements based on the electronic transport and barrier inhomogeneities of diffusion-welded Al-foil/p-type 4H-SiC SBD samples.

4.2.1 Examination of current–voltage–temperature

In this study, Al-foil/p-type-4H-SiC SBDs was fabricated with metal contacts for the first time with a novel technique, namely DW.

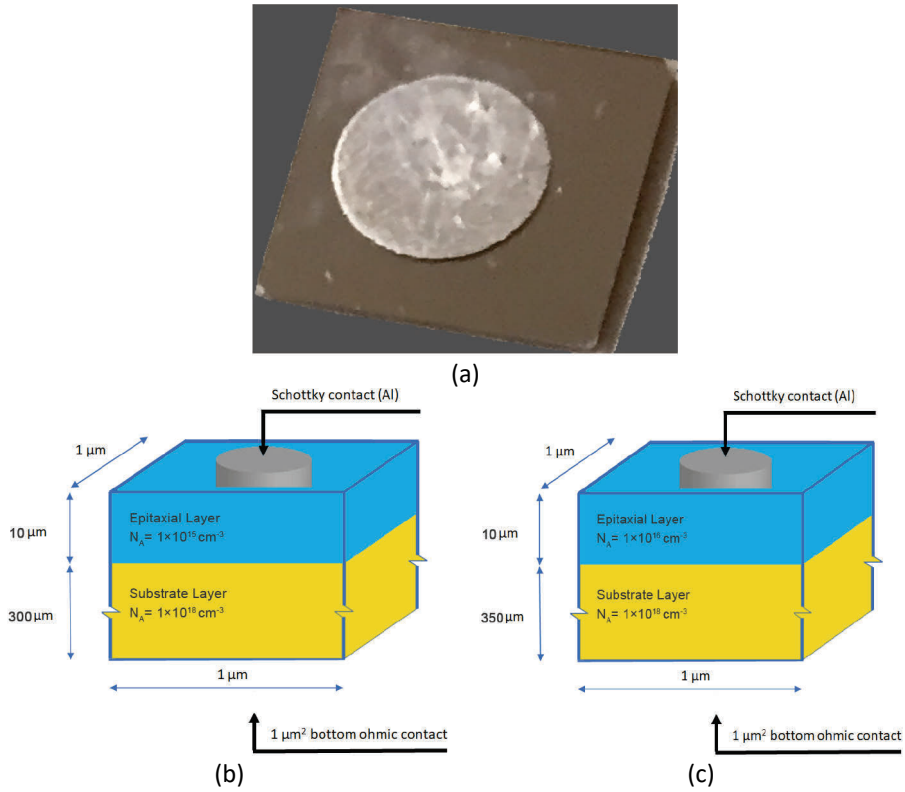


Fig. 4.2: (a) Photograph of the resulting 10 mm × 10 mm Al-foil/4H-SiC SBD by DW; illustration of the structure and doping concentration (b) $N_A = 1 \times 10^{15}$ cm^{-3} and (c) $N_A = 1 \times 10^{16}$ cm^{-3} of the SBDs. Adapted from [Paper II] and [Paper III].

A schematic of fabricated diode structures, doping concentration, and physically fabricated DW SBD is shown in Fig. 4.2. The main goal of this investigation was to explain the inhomogeneity barrier height formations and current transport phenomena, and observe their influence in identically manufactured (with the same vacuum pressure, contact force, and annealing temperature) Al-foil/p-type 4H-SiC SBDs using experimental I–V-T and C–V-T characteristics.

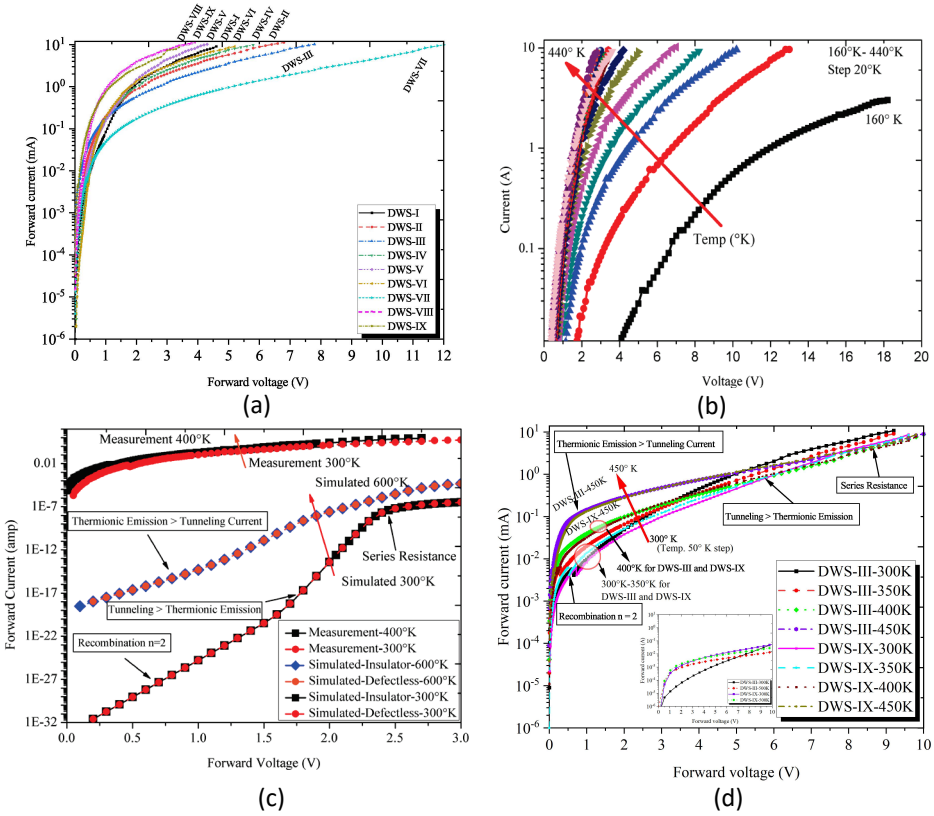


Fig. 4.3: I–V characteristics of p-type 4H-SiC (DWS-I–IX) SBDs illustrating the effect of tunneling and showing a decrease in the bulge in current as voltage increases [Paper III]; (b) Temperature dependence of forward I–V characteristics measurements for diffusion-welded p-type 4H-SiC-SBD (DWS-III) [Paper II]; (c) Measurement (DWS-III) and simulated temperature dependence of forward I–V characteristics for p-type 4H-SiC-SBDs [Paper II]; (d) Forward I–V-T characteristics of diffusion-welded p-type 4H-SiC-SBD (DWS-III and DWS-IX) showing various current transport mechanisms with a temperature step of 50 K [Paper III].

Initially, I–V analysis was carried out to check the quality of the diode. Fig. 4.3(a) shows the room temperature forward I–V characteristics, with the rectifying properties of as-deposited diffusion-welded Al-foil/p-type 4H-SiC SBDs. The diffusion-welded diode DWS-III was considered for the temperature-dependent I–V characteristic measurements. The forward characteristics show exponential behavior over a voltage range at most temperatures, as seen in Fig. 4.3(b). The measured forward voltage drop across the SBD at 1 mA is ~1.5 V. To understand the various mechanisms of current transport through the barrier of the diode and their dependence on high temperature, and the comparisons between the measurement and simulated results on the devices, described clearly in Fig. 4.3(c). From the simulated and measured devices at various temperatures, the forward current bulges are more prominent at high temperatures. By contrast, the thermionic emission current encountered overloads the tunneling current. This bulge is reduced by increasing the applied biased voltage, and it is observed that the current tunneling mechanism dominates the thermionic emission current. The current drop deviation between measurement and simulation in Fig. 4.3(c) is influenced by the

boundary conditions and mashing in the simulation and measurement systems. However, there is also a small forward voltage drop in Fig. 4.3(d) between the identically manufactured devices. This tiny discrepancy may be due to the internal thermal annealing process during DW and the cleaning process before fabrication.

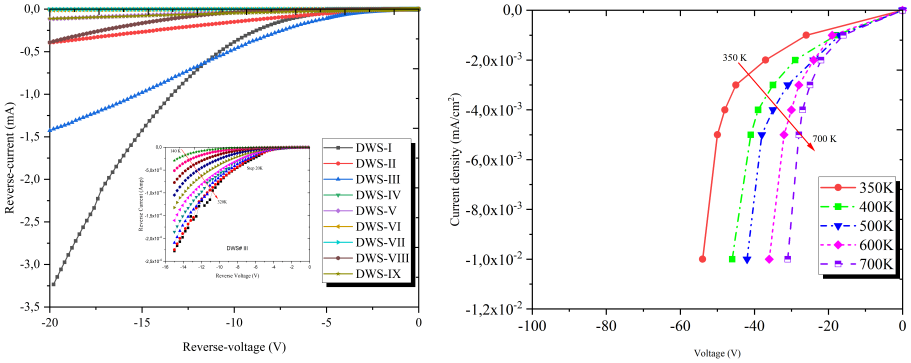


Fig. 4.4: Reverse characteristics of diffusion-welded p-type 4H-SiC SBDs: (a) room-temperature reverse current and inset low-temperature (140–320 K) reverse current for DWS-III and (b) high-temperature reverse current.

Fig. 4.4(a) shows the reverse I–V plot at room temperature for various diffusion-welded p-type 4H-SiC SBDs, and the inset shows the low-temperature (140–320 K) reverse current for DWS-III as-deposited Al-foil. Fig. 4.4(b) illustrates the high-temperature reverse current with high voltage. The reverse current increase is noted with the bias voltage, and the reverse current at -20 V is ~1.7 mA for most of the manufactured Al-foil/p-type-4H-SiC SBDs. As expected, the leakage current is primarily generated due to the tunneling of electrons from the metal to the semiconductor rather than the thermionic emission, image force lowering, and thermal generation current components, as identified from the device simulations reported in [Paper II] and [Paper III].

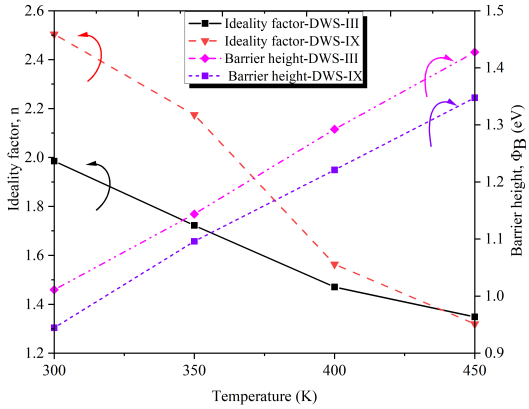


Fig. 4.5: Ideality factor and barrier height investigation of diffusion-welded p-type 4H-SiC-SBD (DWS-III and DWS-IX) as a function of various temperatures deduced from I–V measurements [Paper III].

The ideality factor and barrier height plot are shown in Fig. 4.5, extracted from the measurement of I–V-T values to describe the behavior of the inhomogeneous potential barrier for DW p-type 4H-SiC SBDs. The ideality of the diffusion-welded SBDs ranges from 1.4 to 2.5 and corresponds to the barrier height of approximately 0.9–1.42 [Paper II]–[Paper IV]. The ideality factor and barrier height change according to the manufacturing process parameters and temperature; indeed, both parameters change even at identical manufacturing process parameters, as discussed in [Paper IV]. These dissimilarities of the ideality factor and barrier height within the same manufactured SBDs suggest that the recombination current is dominated at a low forward voltage rather than thermionic emission mechanism or fractional ionization due to structural defect impurities. The detailed investigations are presented in [Paper II] and [Paper III], indicating the existence of inhomogeneous SBH at the manufactured Al-foil/p-type-4H-SiC interface. There are two distinct SBHs at high and low temperatures.

4.2.2. C–V characteristics

The C–V simulation and measurements of the diffusion-welded p-type 4H-SiC SBD devices was also performed to determine the doping concentration of non-compensated shallow acceptors and electric field distribution in the depletion region at room and high temperature (Figs. 4.6 and 4.7).

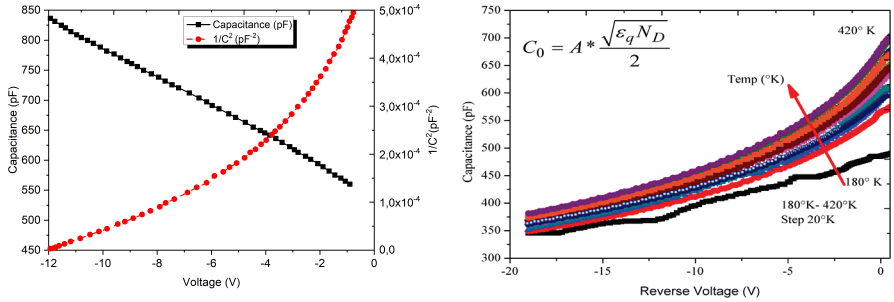


Fig. 4.6: (a) Room-temperature C–V characteristics of diffusion-welded Al-foil SBD and (b) temperature-dependent (180–420 K) reverse C–V measurements for diffusion-welded p-type 4H-SiC-SBD [Paper II].

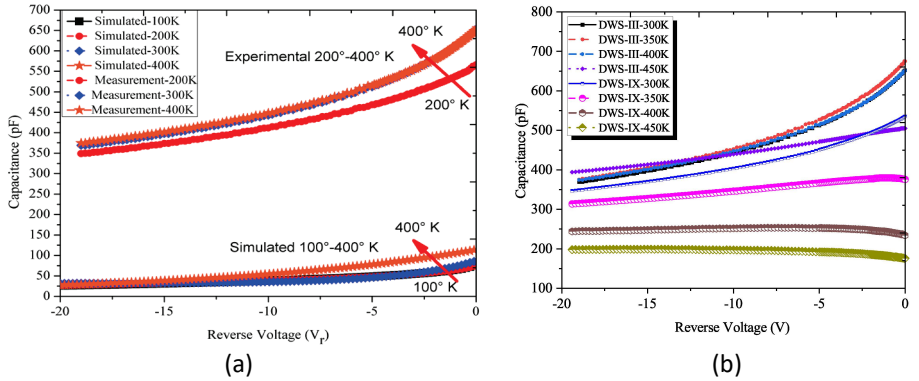


Fig. 4.7: (a) Measured (DWS-III) and simulated temperature dependence of reverse C–V characteristics for p-type 4H-SiC-SBD and (b) temperature dependence of reverse C–V characteristics for p-type 4H-SiC DW-III and DWS-IX SBDs. Adapted from [Paper II] and [Paper III].

Fig. 4.6(a) shows the $1/C^2$ – C characteristics for the as-grown sample, where capacitances are very small and exhibit minimal dependency on the bias voltage by the area of Schottky contacts. Fig. 4.6(a) shows the capacitance of the sample is 0.85 nF/cm^2 at 5 × 10^{14} cm^{-3}. Figs. 4.6(b) and 4.7(a) illustrate the capacitance increases as the temperature increases in measured and simulated C–V-T characteristics for low- to high-temperature diffusion-welded p-type SBDs. The discrepancy between the measurement and simulated C–V-T characteristics can be influenced by the device processing conditions, inhomogeneous barrier height, and measurement environment conditions. However, this analogy of temperature-dependent capacitance is not always followed for the two manufactured devices with identical parameters, as shown in Fig. 4.7(b).

The barrier height discrepancies between the I–V-T and C–V-T measurements are typically larger, about 0.1–0.3eV, as described in [Paper II] and [Paper III]. These results suggest that the Al-foil/p-type-4H-SiC interface of the SBD might be rough [65]; thus, there is surface variation in the SBH along with the interface with two different values, as reported by Defives *et al*. [66], Bhatnagar *et al*. [67], and Zhang *et al*. [68].

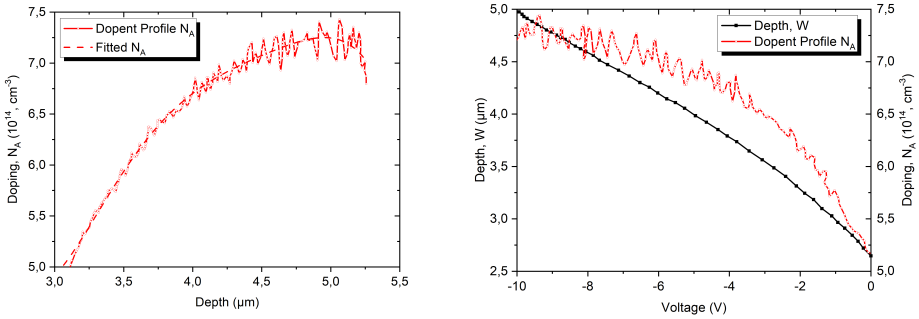


Fig. 4.8: (a) Depletion depths at the applied bias and dopant concentration profile; (b) Diffusion-welded large-area Al-doped SBD on epilayer p-type 4H-SiC C–V measurement: bias dependencies of W and N_A values.

Fig. 4.8 shows the depletion depths at the applied bias voltage and dopant concentration profile. These data illustrate the measurement capability of the epilayer thickness and the doping concentration at the bias voltage. These results suggest that regardless of the bias voltage, a depletion layer with a constant thickness exists under the Schottky contact for the Al-foil/p-type-4H-SiC sample. The net acceptor concentration determined by C–V measurements ranges from 5 × 10^{15} to 2 × 10^{16} cm^{-3}. The depletion depth at the applied bias and dopant concentration profile (N_A (W)) were calculated from the recorded C × V dependence. The bulk dopant concentration is about 7 × 10^{14} cm^{-3}, lower than the reported 1 × 10^{16}cm^{-3} value of aluminum, from which the thickness of the depletion layer is estimated as ~5.0 µm. This result indicates that the whole region of the 5-µm thick epilayers is semi-insulating, keeping the substrate conductive.

4.2.3. DLTS and L-DLTS measurements

DLTS and high-resolution LDLTS have been used to characterize deep-level defects by energetic particles and during metallization in diffusion-welded p-type SBDs. In this work, deep electronic levels were characterized with conventional DLTS and LDLTS [69]. In the DLTS measurement applies constant bias voltage and two filling pulses of different magnitude, was used to obtain the dependencies of electron emission rates on the electric field strength for deep-level traps of Al-foil/p-type-4H-SiC SBD.

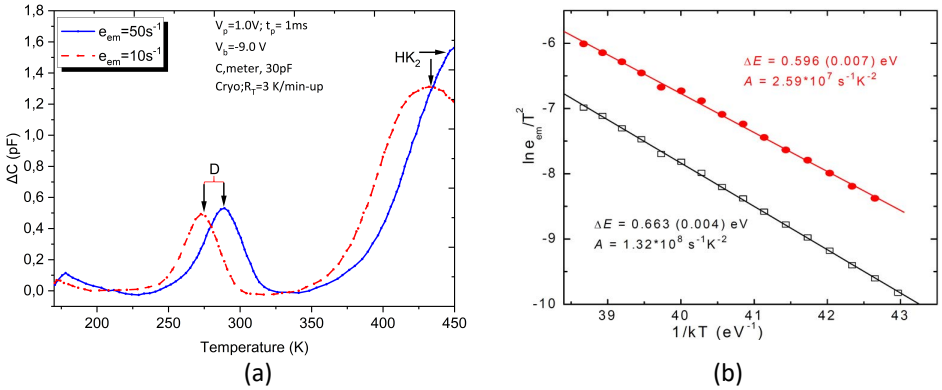


Fig. 4.9: Diffusion-welded large-area Al-doped SBD on epilayer p-type 4H-SiC: (a) conventional DLTS measurements and (b) Arrhenius plot of emission rates for the peak with its maximum at about 290 K.

Deep levels in diffusion-welded Al-foil/p-type-4H-SiC SBD epilayers were measured by Fourier-transform DLTS from 170 to 450 K. The reverse bias voltage was kept at -9 V, and the pulse voltage applied during the DLTS measurements was 1 V, with a pulse width of 1 ms and emission rates of 10 and 50 s^{-1} for all the DLTS measurements performed in this study. A temperature-independent capture cross-section was assumed when analyzing the DLTS data. Fig. 4.9(a) shows a well-defined DLTS peak "D" center with its maximum temperature of about 275 K (for electron emission, e_{em} = 10 s^{-1}) or 290 K (for e_{em} = 50 s^{-1}) and a broad feature at T > 340 K. There is another possible peak (HK_2) with its maximum temperature of about 430 K (for e_{em} = 10 s^{-1}) or 450 K (for e_{em} = 50 s^{-1}), but it could not be estimated properly due to limitations in the measurement temperature. Fig. 4.9(b) shows temperature dependencies of T^2-normalized emission rates (Arrhenius plots) of hole emission rate measured for the peak with its maximum temperature at about 290 K on as-manufactured Al-foil/p-type-4H-SiC SBD. The derived values of activation energies for emission and pre-exponential factors are E_V+ 0.596 eV (E_V, top of the valence band) and 2.59 × 10^7 s^{-1} K^{-2} or E_V+ 0.663eV and 1.32 × 10^8 s^{-1} K^{-2} for both components. The capture cross-sections for the D center were estimated to be between 1 × 10^{-11} and 1 × 10^{-14} cm^2, with a sample concentration of 2.5 × 10^{13} cm^{-3}. However, the variation in derived activation energies and pre-exponential factors differs slightly for both components. It might be possible that the same defect is responsible for the observed emission signals within the same sample at different estimation times. It could also be explained in response to the duration of DW, with crystallization and recrystallization due to welding, followed by cooling phases (with heat treatment still applied to the devices). Thus, the same defect appears at different potential trap levels

with small emission rate differences. Katsunori *et al*. [70] and [71] detected another potential trap (HK_1) at 385 K on the p-type sample. However, the HK_1 center is not visible in this sample because the intrinsic defects could have migrated during the high-temperature fabrication process. The activation energy (ΔE) and capture cross-section (σ) of the centers obtained by the Arrhenius plot of emission time constant are summarized in Table 4.1.

Table 4.1: Electrical properties of deep-levels defects in diffusion-welded p-type 4H-SiC SBD.

Label	ΔE (eV)	A (s^{-1} K^{-2})	σ (cm^2)	Observation temp (K)	Trap observation
D	0.596–0.663	2.59×10^7-1.32×10^8	1×10^{-11} to 1×10^{-14}	275–290	As-grown
Hk_2	-	-	-	430	As-grown

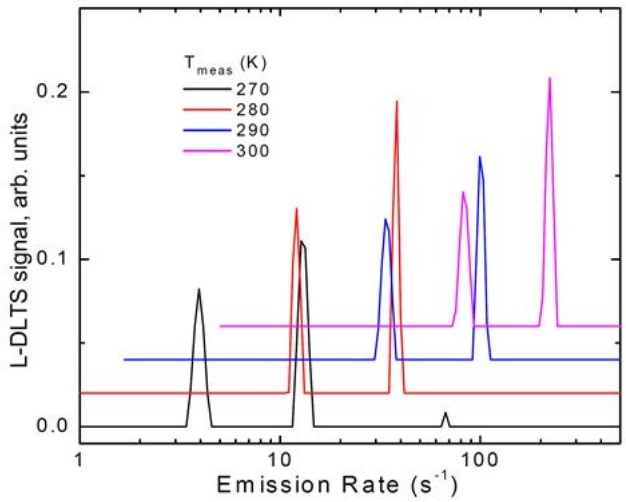


Fig. 4.10: LDLTS measurements of diffusion-welded large-area Al-doped SBD on epilayer p-type 4H-SiC.

L-DLTS: LDLTS proved particularly useful because it could separate deep levels with closely spaced energy levels that were not possible by conventional DLTS. LDLTS measurements of emission rates in the temperature range of 270–300 K are shown in Fig. 4.10. The emission signal consists of two well-defined components, which shift with the measurement temperature, indicating that the Poole–Frenkel effect [71], [72] is absent in the hole traps. The detected hole traps (i.e., D, and possible- HK_2 centers) suggested by the author as a neutral charge state after hole emission and may be donor-like (+/0) traps [71].

4.3. Electrical characterization of Au-sputtered/p-type 4H-SiC SBD

Gold metallization on p-type 4H-SiC samples were carried out and then investigated I–V, C–V, and annealing to understand Schottky behavior and the implementation of reliable multipoint contact. This information is important for subsequent irradiation of SBDs discussed in chapter-5. The sample preparation and cleaning procedures were the same as discussed in chapter 3. The sputtering technique was used to deposit gold with a thickness of approximately 100 nm on the epilayer surface. Four 2.2-mm Schottky contacts were prepared on a single chip.

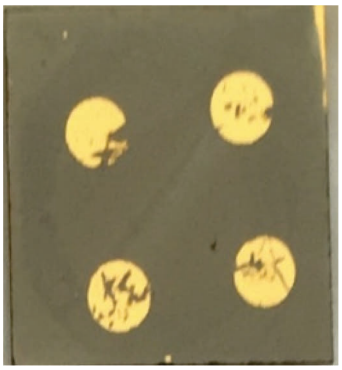
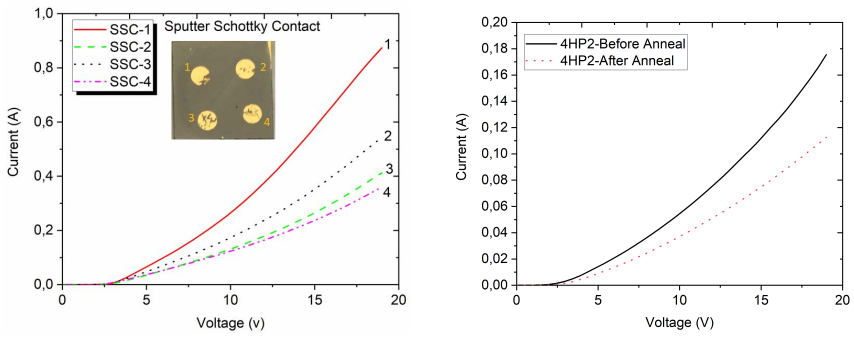


Fig. 4.11: Photograph of the resulting 10 mm x 10 mm Au/4H-SiC SBD by gold sputtering.

Fig. 4.11 shows a photograph of the Au/p-type 4H-SiC SBD. This investigation were used two Au/p-type 4H-SiC SBD samples (4HP1 for 4HP2). After deposition, four individual Schottky diodes behaviors were observed, namely 4HP1/2-1, 4HP1/2-2, 4HP1/2-3, and 4HP1/2-4, at different contact areas and doping concentrations (discussed in section 4.3.1 and 4.3.2). An additional investigation were also performed on sample 4HP2-1 after annealing at 400°C for 20 min.

4.3.1. I–V characteristics

Forward I–V characteristics were measured with the limited current of up to 1 A by a Keithley 2400 source and measurement unit with the LabVIEW program. Fig. 4.12 (a) shows the I–V characteristics of four-sputtered contacts on a single chip.



(a) (b)

Fig. 4.12: (a) I–V characteristics of four-sputtered contacts on a single chip (4HP1-1-4); (b) I–V characteristics of sample 4HP2-1 before (black) and after annealing (red).

The forward current limit from 380 to 850 mA for contact areas (sputter Schottky contact 2 to 1) shows a dominant thermionic emission mechanism. The contacts on a single chip shows different I–V curves because four different Schottky diodes have been formed within the single diode. Schottky behavior was also observed on the diffusion-welded broken SBD samples due to excess pressure during the fabrication process. These Schottky characteristics can be considered to be an individual diode for each contact. Based on Fig. 4.12(b), the measured Au/p-type 4H-SiC SBD shows rectifying properties before and after annealing. The forward current is reduced from 170 to 110 mA due to the annealing process of the SBD.

4.3.2. C–V characteristics

Fig. 4.13 shows the reverse biased C–V characteristics of four sputtered contacts on a single chip at room temperature. The capacitance varies from 95 to 120 pF for the various contact areas. Fig. 4.13(b) shows the C–V characteristics of the 4HP2 sample before (red) and after (black) annealing. The capacitance has been reduced from 51 to 44 pF due to annealing.

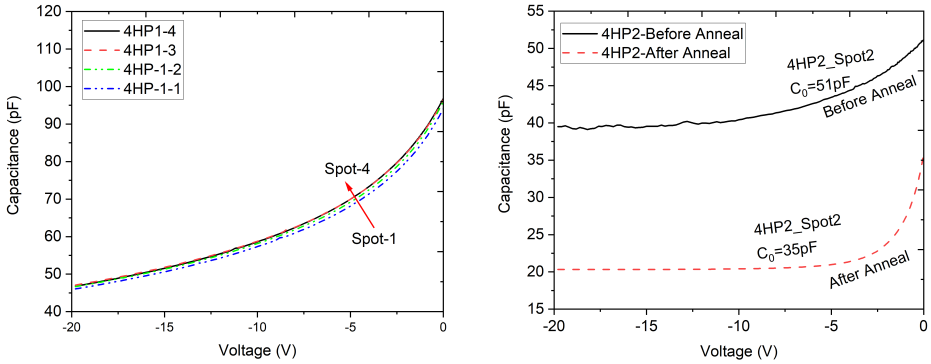


Fig. 4.13: (a) C–V characteristics of 4 sputtered contacts (4HP1-1-4) on a single ship; (b) C–V characteristics of sample 4HP2-1 before (black) and after annealing (red).

Of note, the capacitance of the diffusion-welded Al-foil/p-type 4H-SiC SBD (850 pF) is much higher than that of the Au/P-type 4H-SiC SBD (51 pF). This difference might be caused by the potential contact thickness and contact area of the SBDs.

The dependence of the dopant concentration profile investigation was carried out on the epitaxial layer depth with various Au contact areas after metallization. As seen in Fig. 4.14, the doping concentration varies with the depth profile. For a contact area of 330 µm (sample 4HP-11), 340 µm (sample 4HP-12), 320 µm (sample 4HP-21), and 310 µm (sample 4HP-22), the doping concentrations are 1.12×10^{15} cm^{-3}, 1.3×10^{15} cm^{-3}, 5.4×10^{15} cm^{-3}, and 2.34×10^{15} cm^{-3}, respectively. For 4HP1-1, the doping concentration (N_{dop}) is almost the same for the epitaxial layer depth of 2.0–2.5µm. For 4HP1-2, the doping concentration is slightly variable, and it is also almost constant for the epilayer depth of 0.55–0.73 µm (for 4HP-2-1) and 1.05–1.30µm (for 4HP-2-2). This investigation shows that the doping concentration does not change during the fabrication process.

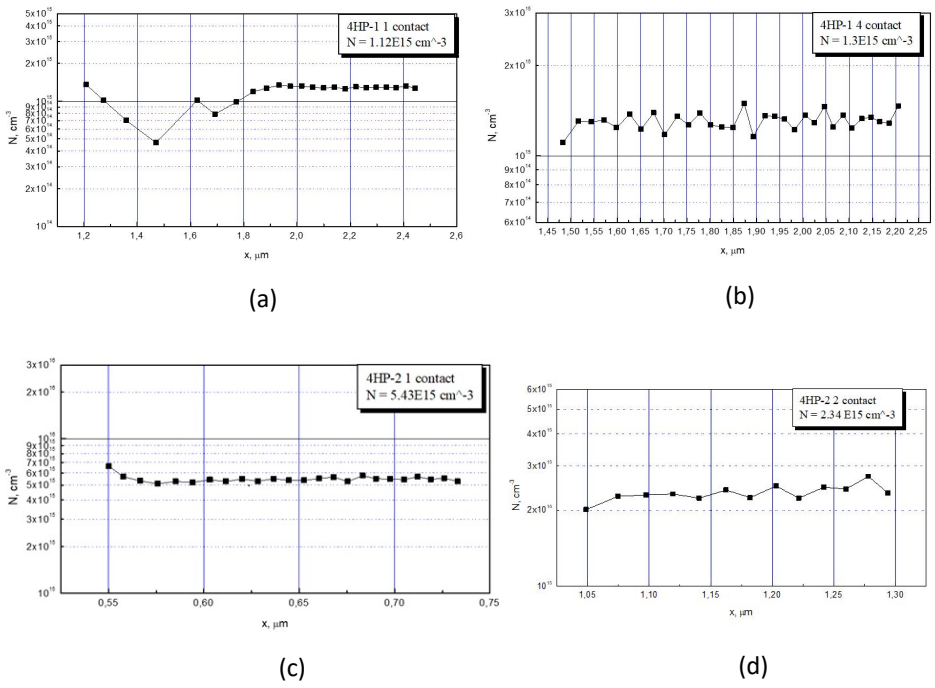


Fig. 4.14: N_{dop} dependence on the epitaxial layer depth of (a) sample 4HP1, with a contact area of 0.033 cm^2; (b) sample 4HP12, with a contact area of 0.034 cm^2; (c) sample 4HP21, with a contact area of 0.032 cm^2; and (d) sample 4HP22, with a contact area is 0.031cm^2.

4.3.3. DLTS characteristics

DLTS measurements were utilized to identify concentrated defects between the gold and p-type 4H-SiC interface in the manufactured SBDs. Fig. 4.15(a) shows DLTS measurement for one selected contact on the chip from 200 to 450 K before annealing. The DLTS peak HM_1 is at its maximum at 310 K. Other possible peaks are HM_2 and HM_3, with a maximum temperature of about 390 and 407 K, respectively. The temperature dependencies of the T^2-Arrhenius plots of the activation energy of the HM_1 peak is E_V+ 0.483 eV; above the balance band and the capture cross-section is 4.06×10^{-16} cm^2. By observing the HM_1 defect activation energy and capture cross-section, it can speculate that the HM_1 peak will be the well-known D center defect in p-type 4H-SiC, also observed in the diffusion-welded SBD sample with a shifted temperature peak. The activation energy and capture cross-section of the HM_3 peak are E_V+ 0.86 eV and 6.85×10^{-14}, respectively. Katsunori [71] also observed almost the same activation and capture cross-section for the HK_2 peak.

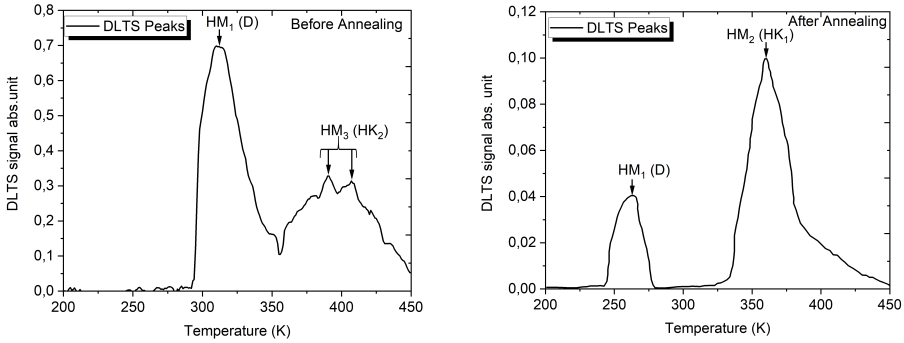


Fig. 4.15: DLTS spectra for sample 4HP2-1 gold contact from 200 to 450 K (a) before annealing and (b) after annealing.

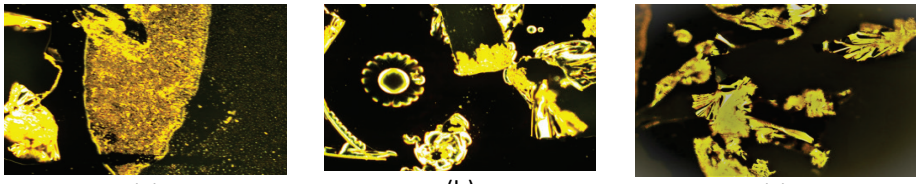
Fig. 4.15(b) shows the temperature-dependent DLTS scan on sample 4HP21 from 200 to 450 K after annealing. There are two peaks, HM_1 at ≈260 K, close to the D center, and HM_2 close to about HK_1, as described in [71], at 360 K with a lower signal intensity. The activation energy and cross-sections for the HM_2 peak are E_V+ 0.663 eV and 3.0×10^{-15} cm^2, respectively. Other than these trap centers, it is not clear why the D center shifted back and why HM_3 has been annealed out. Two reasons can explain the disappearance of those defects. The D trap might be moved due to the liquid N_2 introduced (200–450 K) during the DLTS measurements. These defects get frozen, and immediately upon reaching room temperature, the epilayer remains in the frozen state. This D trap can be identified after the DLTS measurements start from room temperature to the high temperature (without cryogenic cooling). Another defect (HM_3) at about 407 K on the as-grown sample may be annealed out, or by thermal treatment, it might migrate and could result in the formation of HM_2 defect at a lower temperature. The activation energy (ΔE) and capture cross-section (σ) of the centers obtained by the Arrhenius plot are summarized in Table 4.2.

Table 4.2: Electrical properties of deep levels defects in the Au-sputtered/p-type 4H-SiC SBD.

Label	ΔE	σ (cm^2)	Observation T (K)	Trap observation
D	0.483	4.06×10^{-16}	310	As-grown
HM_3	0.86	6.85×10^{-14}	390–407	As-grown
D	0.66	1.0×10^{-15}	260	After annealed
HM_2	0.663	3.0×10^{-15}	360	After annealed

4.3.4. AFM

Fig. 4.16 shows an AFM image of the surface of gold contacts of the Au/p-type 4H-SiC SBD after annealing. One can see in the peripheral areas of the sputtered gold to contact the presence of a liquid phase. This is evidenced by the formation of a dendritic structure when observed under the microscope. It turns out that the presence of a mono-atomic silicon layer on the carbide contact surface is sufficient for contact melting at macro depths. In that case, an additional phase appears in the MS contact with its different interphase states, which should affect the device's characteristics.



(a) (b) (c)

Fig. 4.16: (a-c) Atomic force micrographs of Au/p-type 4H-SiC SBD AFM image of the surface on the sample after annealing.

4.4. Summary of diffusion-welded Al-foil/ and Au-sputtered/p-SiC SBDs

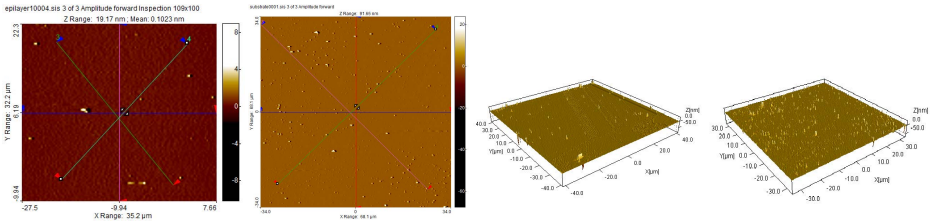
The diffusion-welded and Au-sputtered p-type 4H-SiC SBD fabrication and physical characterization were studied. The numerical and experimental descriptions illustrate the reliable operation of the device. I–V and C–V characteristics were measured and presented. As the metallization methods were different, one would expect that the I–V and C–V curves would also be different. There are also differences in the zero-capacitance value. The investigated deep-level spectra revealed two peaks in both contacts: the D peak appears at about 275 K–290 K for the diffusion-welded contact with an activation energy of 0.596 eV–0.663 eV and a capture cross-section of 1×10^{-11} to 1×10^{-14} cm^2. The D peak has a lower activation energy of 0.483 eV with a capture cross-section of 4.06×10^{-16} at 310 K in the as-grown sample, and a higher activation energy of 0.66 eV with a capture cross-section of 1.0×10^{-15} cm^2 at 260 K after annealing at gold sputtered contact. There are other peaks: HM_3 at 390–407 K and HM_2 at 360 K, with slightly higher activation energies of 0.86 and 0.663 eV, respectively, for the as-grown and after-annealed gold sputtered samples. The activation energy and capture cross-section values are different, but the shape of the DLTS spectra is more or less the same for both metallization techniques. The examined Au-sputtered p-type 4H-SiC SBD using AFM measurement revealed the formation of a dendritic structure due to annealing.

4.5. Microscopic surface analysis of diffusion-welded SBD devices

After examining the impact of metal deposition on the electrical properties of SBDs, it is necessary to examine the effects of metal deposition on the physical properties of SBDs using microscopy. Film morphology was measured before and after DW by using AFM and SEM. The surface chemical states of the 4H-SiC film were characterized by XPS. For this study high-resolution TEM were also employed combined with energy-dispersive X-ray spectroscopy (EDX) to examine crystallographic properties, and the distributions of Al, C, Si, and O atoms across the aluminum–4H-SiC SBD bonding interface.

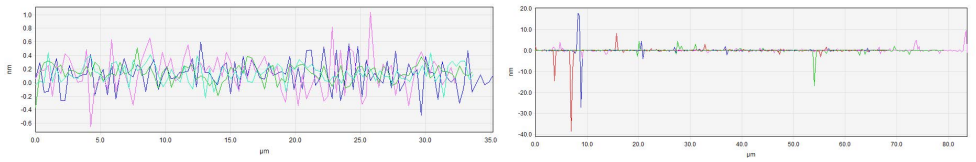
4.5.1. Surface micro-roughness using AFM

The micro-roughness of the surface (after dicing the sample (10 mm × 10 mm)) was examined using AFM. Surface roughness measurement using AFM uses root mean square (RMS) tool as a marking with a relatively short sampling length and suppresses waviness. It allows a 3D profile of the surface. The microscope can run in the following modes: contact, non-contact, and tapping. The topography of the DW Al-foil-SBD sample was investigated in the soft tapping mode. The tapping mode provides the best quality of data for surface roughness determinations. The tapping mode offers higher lateral resolution on most samples (1–5 nm), achieves relatively high scan speeds, causes less damage to soft samples imaged in the air, and leads to minimum distortion in the image.



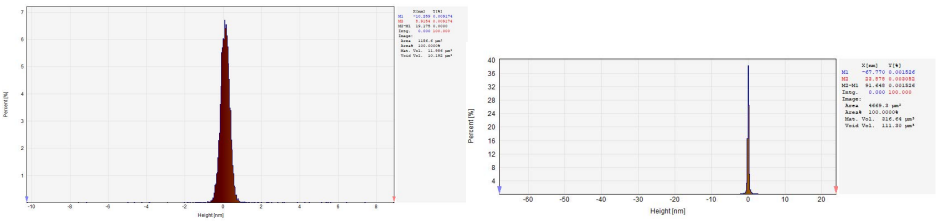
(a) (b) (c) (d)

Fig. 4.17: (a) The average roughness RMS of the epilayer side is 0.2 nm and (b) the average roughness RMS of the substrate side is 2.7–3.3 nm; 3D views of (c) the epilayer side and (d) the substrate side.



(a) (b)

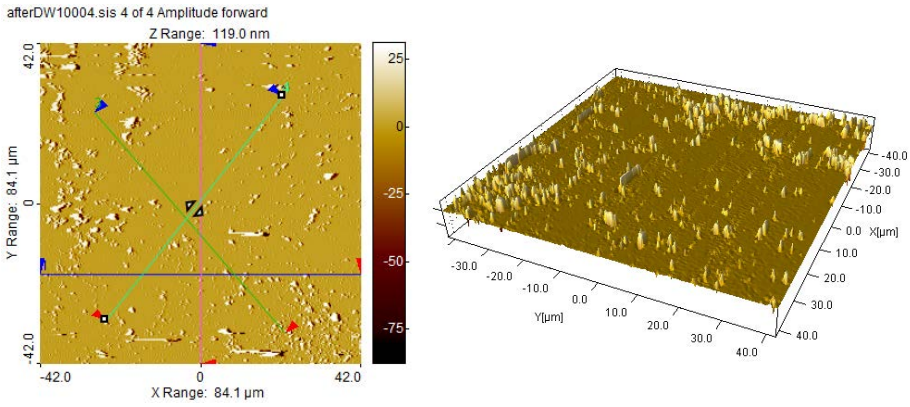
Fig. 4.18: (a) The cross-section profile of the epilayer side shows the average RMS is 0.2–0.4 nm and (b) the cross-section profile of the surface side shows the average RMS is 1.5–2nm.



(a) (b)

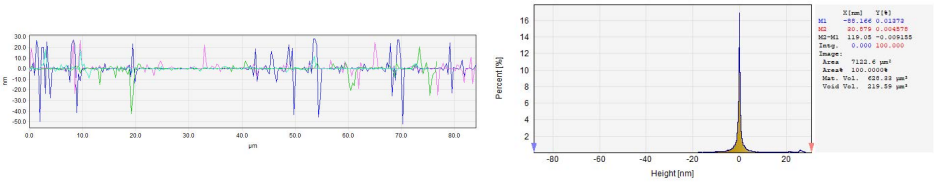
Fig. 4.19: (a) Histogram (height distribution) of the epilayer surface of p-SiC and (b) histogram (height distribution) of the p-SiC substrate surface before diffusion welding.

Fig. 4.17 shows atomic force micrographs of the epilayer and substrate sides. The sample was investigated in the initial state without any prior treatment of the surface. The average roughness RMS is 0.2 nm for the epilayer side and 2.7–3.3 nm for the surface side. Fig. 4.18 shows the average roughness mean complete profile, making no distinction between peaks and valleys. However, the average RMS is about 0.2–0.4 nm, which indicates a pretty smooth surface. As presented in Fig. 4.19, the histogram has a small tail reaching up to about 1 nm for the substrate side compared with about 2 nm for the epilayer side.



(a) (b)

Fig. 4.20: AFM (a) 2D and (b) 3D views of the surface after diffusion welding.



(a) (b)

Fig. 4.21: (a) The cross-section profile of the surface shows the average RMS is 4–10 nm and (b) a histogram (height distribution) of the p-SiC surface after diffusion welding.

For direct bonding, the surface roughness should be close to the constant lattice value: 0.3–0.5 nm. As an example, RMS roughness up to about 0.5 nm can be tolerated for room temperature direct bonding [73]. The sample was scanned again using AFM after DW. Fig. 4.20 shows that the height asymmetry in-plane and profile changed after the interaction of the Al-foil with 4H-SiC during DW. The roughness is much different after DW. According to [73], a decrease in surface roughness to 0.5 nm needs to be considered for the depth of aluminum interaction with SiC. This reduced roughness is not an indicator of dissolved silicon in aluminum, because the original crystalline matrix may be destroyed in the cleaning process or by the diffusion of silicon atoms in aluminum [74]. Hence, the histogram has a long tail reaching up to about 20 nm, which can be connected with the particles left after the cleaning process of Al-foil from the SiC surface shown in Fig. 4.21. Therefore, before DW, the specific structural features of the possible sub-contact region requires further investigation with another microscopic method to determine the precipitated carbon atom position in the epilayer.

4.5.2. XPS measurement

The reliability of SiC-based MS and metal oxide semiconductor (MOS) technology relies on their interface traps, the ability of interface defects to grow, sacrificial thermal oxidation under high temperature, high power, and radiation-attributed environment [75], [76]. There have been very few investigations on p-type SiC oxide and SiO_2 growth during pre-deposition, even though a reliable p-type oxide interface layer or low-density interface traps are required in power devices [77], [78]. Carbon clusters [79], [80], silicon and carbon dangling bonds [81], [82], and silicon oxycarbide (SiO_xC_y) bonds before and after surface cleaning are primarily considered for the interface trap or defects in the transition/interfacial layer [83]–[87]. These unwanted oxide layer or interface defects from p-type SiC lead to deficient inversion channel mobility in power devices such as metal–oxide–semiconductor field-effect transistor (MOSFET), Complementary metal–oxide–semiconductor (CMOS), bipolar junction transistors (BJT), and insulated gate bipolar transistors (IGBT) [88]–[90]. Another problem in p-type SiC is uncontrollable barrier properties in the metal-SiC diodes, especially in the fabrication of ohmic and Schottky contacts, due to the low hole mobility, low ionization energy, and extensive work function [84], [88]. However, to improve the quality of the interface layer or defects, unwanted chemical structures, contamination, and related defects must be minimized. Therefore, atomically ordered and free chemical residues of unknown chemical structures are crucial in developing high-power and high-temperature p-type SiC-based devices.

Traditional wet cleaning such as standard Radio Corporation of America (RCA) buffer, HF or HCl, hydrogen plasma treatment (HPT), high-temperature HCl vapor etching, and high-temperature hydrogen annealing have been used to clean SiC surfaces [89], [90]. However, buffered HF cleaning leaves OH and F ion impurities due to high polar bond binding affinity on the SiC surface [89]. High-temperature hydrogen annealing can limit the oxidation on the SiC surface by producing OH ions and reducing contamination. HPT by radio frequency (RF) plasma-enhanced chemical vapor deposition (PECVD) introduces hydrogen in the SiC substrate; this process is suitable for high-volume production cleaning. Still, this process requires a smoother surface [91], [92].

XPS was used to investigate the suitability of the cleaning process for p-type SiC-based Schottky contact and their atomic constituents in the interface layer. High-resolution XPS fine scans were performed on 4H-SiC, without chemical treatment (WOCT), with chemical treatment (WCT), and with standard RCA cleaning for the p-type 4H-SiC surface.

Experimental process

Sample: The Al-doped p-type 4H-SiC wafers with a 10-µm thick epilayer grown on the Si-face (0001) 4° off-axis of a 350-µm thick substrate was purchased from Cree Research Inc. Three diced 10 × 10 mm^2 samples were used in this study.

Two surface pre-deposition cleaning procedures were employed. One sample was degreased and cleaned in a conventional chemical cleaning process (discussed in chapter 3). A second sample (WCT) was degreased in standard RCA solution and then dipped in a 1% HF solution and rinsed in DI water for 5 min. The third sample (WOCT) was not subjected to any chemical solution (as purchased).

The chemical composition was studied with XPS, using a Kratos Analytical AXIS ULTRA DLD spectrometer fitted with a monochromatic Al Kα X-rays source and achromatic Mg Kα/Al Kα dual anode X-ray source. A monochromatic Al Kα anode (1486.6 eV) was used, operated at 150 W and 15 kV. A 180° hemispherical energy analyzer with a 165-mm

mean radius was performed using a hybrid lens mode at pass energy 160 eV for survey spectra and 20 eV for regions. XPS spectra were recorded at a 90° takeoff angle, and angle-resolved measurements were taken from the surface of the sample holder using a 300 µm × 700 µm aperture slot.

Samples were mounted on a stainless steel 130 × 15 mm^2 sample bar. The material was sufficiently conductive, and binding energy values were not charge corrected. The relative atomic concentrations of detected elements were determined from the appropriate core level integrated peak areas and sensitivity factors provided by the Kratos original analysis software Vision 2.2.8. Shirley background subtraction was used to calculate the relative atomic concentrations. For surface cleaning and bulk composition information, a Minibeam I ion (Ar+) source (2 kV, 10 mA, 30 s per cycle) was used. For angle-resolved X-ray photoelectron spectroscopy (ARXPS), only the RCA sample was tilted toward the Al-mono X-ray source in -15° steps from 0° to -75°.

Results and discussion

The 4H-SiC (0001) surfaces were investigated before pre-deposition without chemical (WOCT), after chemical (WCT), and after RCA treatment.

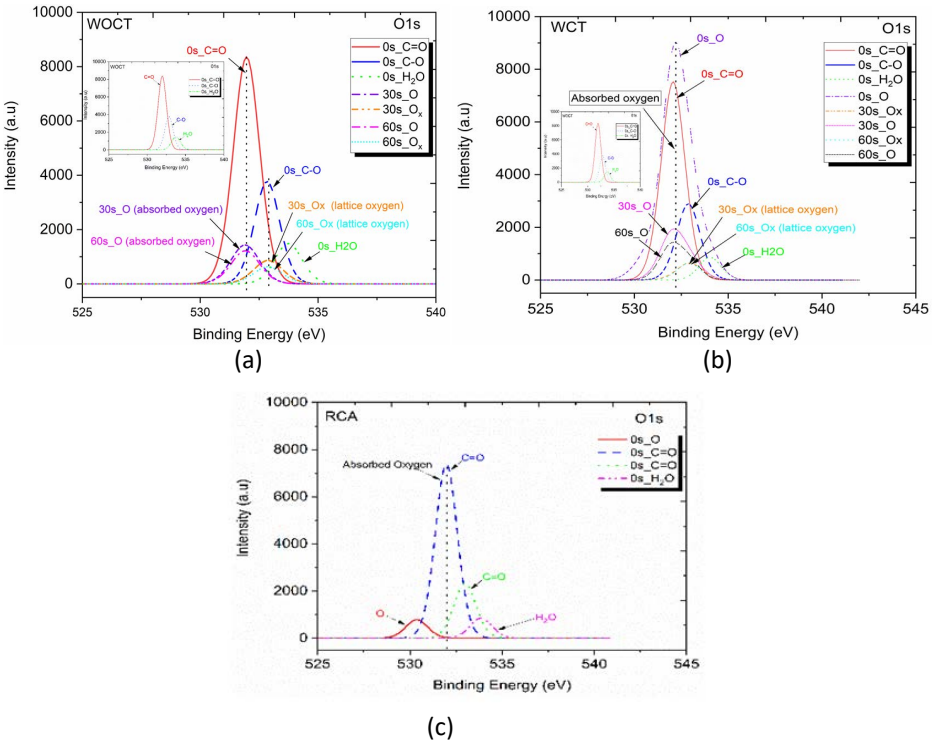


Fig. 4.22: XPS spectra of O1s for the (a) WOCT; (b) WCT; and (c) RCA samples.

Figs. 4.22, 4.23, and 4.24 show the O1s, C1s, and Si2P peaks, respectively, for each cleaning process. Compared with the C1s and Si2P spectra, the O1s peak is lower in magnitude but always present in the SiC surface regardless of the cleaning process.

Moreover, a substantial amount of oxygen is present and contaminated with stable OH rather than H ions owing to the reaction of the SiC surface after HF treatment during the last step of WCT and RCA. There are absorbed oxygen and other species present, mainly O_2, CO_2, and H_2O, and those constituents have also been observed previously [93].

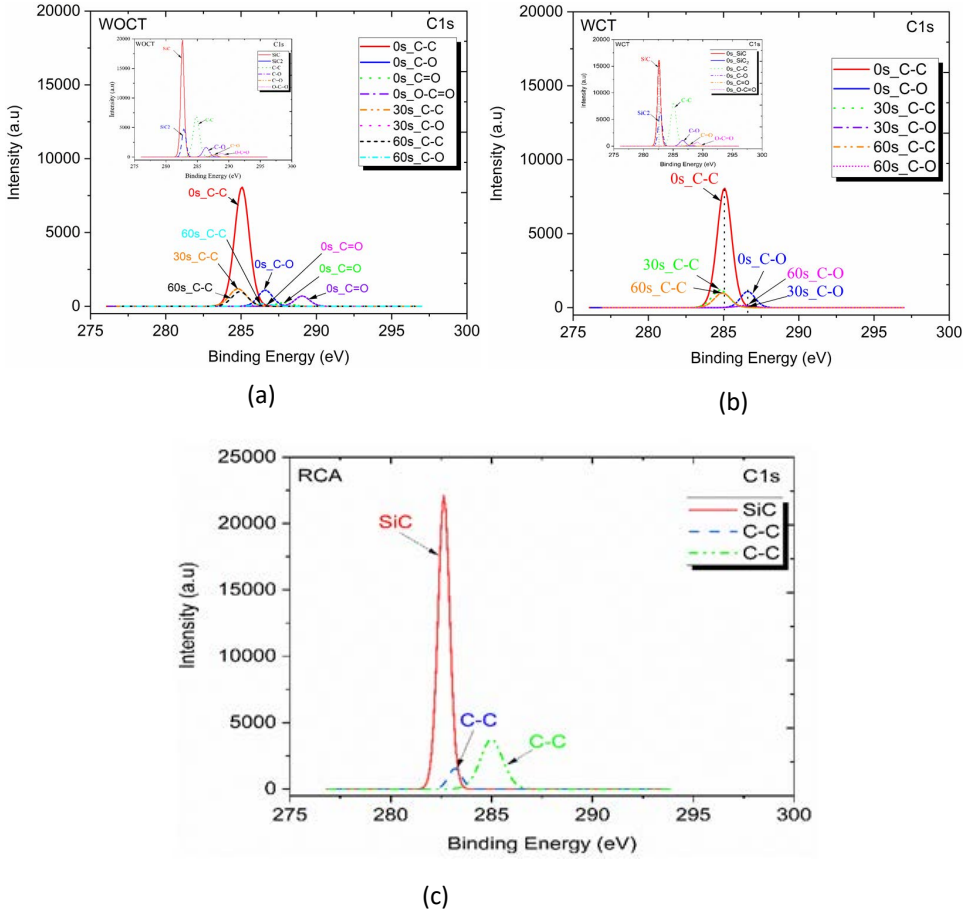


Fig. 4.23: XPS spectra of C1s for the (a) WOCT; (b) WCT; and (c) RCA samples.

Oxygen in the SiC sample is primarily responsible for reoxidation or oxygen absorption of SiC surfaces during exposure to air while transferring the samples to the XPS equipment. Another cause may residual oxygen detected by XPS from the substrate holder that maintains slightly higher than the SiC sample. References [94]–[96] introduced HPT and explained how to remove this oxygen atom contamination by effective chemical passivation of surfaces against oxidation by terminating Si dangling bonds.

C1s is present in the WOCT, WCT, and RCA spectra (Fig. 4.23); the RCA sample has the highest spectral peak. There is a higher energy tail of SiC compared with the carbon cluster (C-C) contaminants for all the samples.

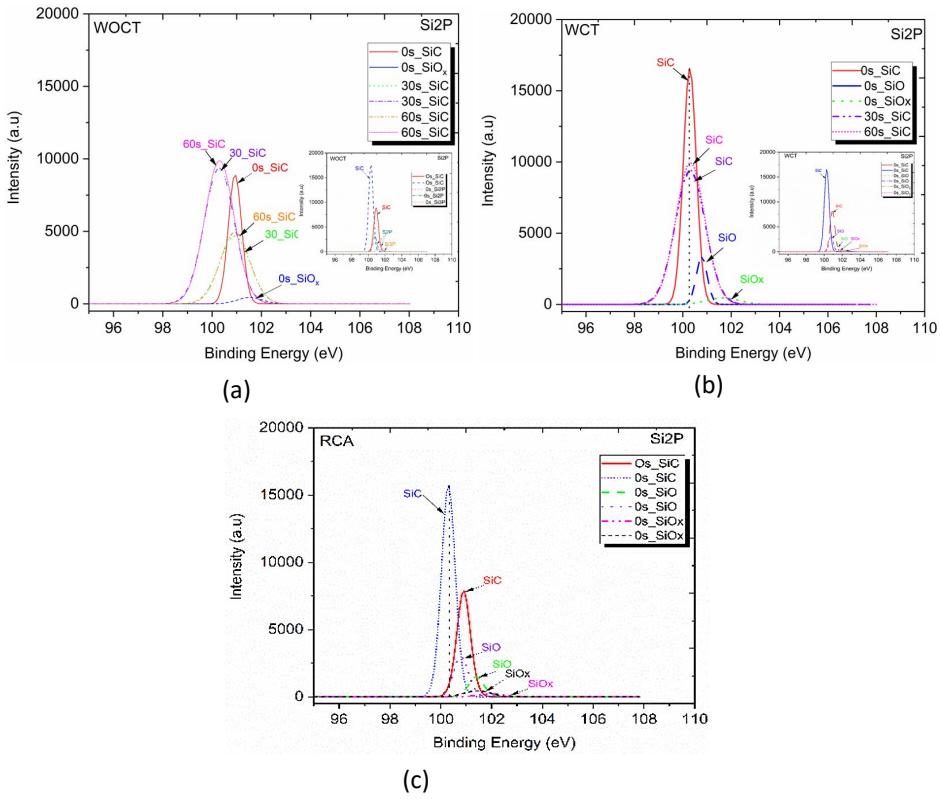


Fig. 4.24: XPS spectra of Si2P for the (a) WOCT; (b) WCT; and (c) RCA samples.

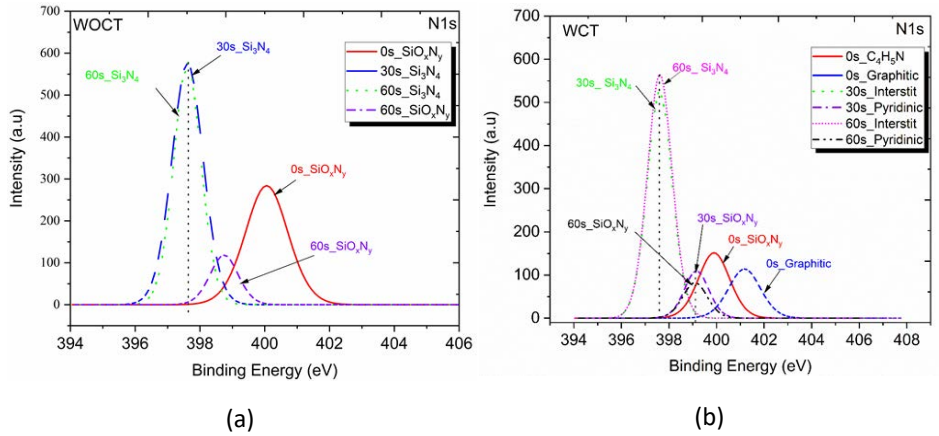


Fig. 4.25: XPS spectra of N1S for the (a) WOCT and (b) WCT samples.

Still, carbon cluster and oxocarbon (C-O) bonding energy is present after the 30- and 60-s scan, 2.5 eV higher than the SiC spectra. However, these carbon cluster spectra in the RCA sample are notable reduced compared with the WOCT and WCT samples

without a chemical shift. Carbon clusters and their residuals are present during the oxidation process due to the reaction of carbon clusters with the SiC surface as a nanoparticle. After the RCA cleaning process, the carbon clusters and their residuals are visible because they are resistant to the HF solution [97], [98]. These significant carbon residues present in all SiC samples are considered a severe problem for long-term application of high-temperature, high-power devices [99]. This carbon contamination can be removed by applying HPT and hydrogen nitrogen plasma treatment (HNPT), as suggested by [100]–[102]. During HPT, hydrogen and carbon atoms interact; this process changes the band bending energy removed as volatile C_xH_y species at 200°C. During HNPT, hydrogen and nitrogen atoms react with the carbon clusters to destroy the cluster configuration, and to create carbon dangling bonds that are passivated with nitrogen and hydrogen in SiC surface and resulting in the formation of volatile C_xH_y and C_xN_y (C-H and C-N bonds) at 250°C [91], [103]–[105].

Suppose the carbon tail is removed from the SiC samples. In that case, it is possible to change the surface Fermi level and to decrease the surface band bending due to increased binding energy of C1s. The increase in C1s binding energy improves the reliability and performance of SiC-based devices [106], [107]. References [100] and [101] suggested that implementing HPT in p-type SiC shifts the Fermi level near the valence band edge by lowering the surface band bending.

A chemically shifted SiC, lattice oxygen (SiO_x), and SiO surface component are observed in the silicon core (Si2P) spectrum due to the Si-C and Si-O bonds in WOCT, WCT, and RCA samples (Fig. 4.24). The Si-contaminated oxygen associated with silicon may be due to the tendency to form silicon-oxycarbide (Si-O-C) by the ancient oxygen contact or hydroxyl contact during the sample transfer to the XPS equipment [108]–[110]. The magnitude of the SiO and SiO_x surface component is slightly reduced for the RCA sample compared with the WCT sample. Nevertheless, the magnitude of SiC spectra remains the same, and no components were removed entirely. Huang *et al*. [101] reported that SiO and SiO_x could be removed entirely as a volatile H_2O by introducing HPT with the RCA cleaning process; this removal is due to the reaction of hydrogen.

Fig. 4.25 illustrates the N1s spectrum consisting of Si-pyridinic-(SiO_xN_y), Si-interstit (Si_3N_4), SiO_xN_y, and graphitic spectra in the WOCT and WCT samples, but the RCA sample does not present these peaks (data not shown). This removal of Si-pyridinic (SiO_xN_y) and Si-interstit (Si_3N_4) spectra is expected after RCA cleaning because the hydrogen atoms in HF can remove the oxygen atoms by interacting with SiO_x from the SiC surface and create water [78], [80]. The magnitudes of the SiO_xN_y and Si_3N_4 peaks are reduced in the WCT sample because the chemical treatment minimizes the number of N atoms for SiO_xN_y and Si_3N_4 spectra [111].

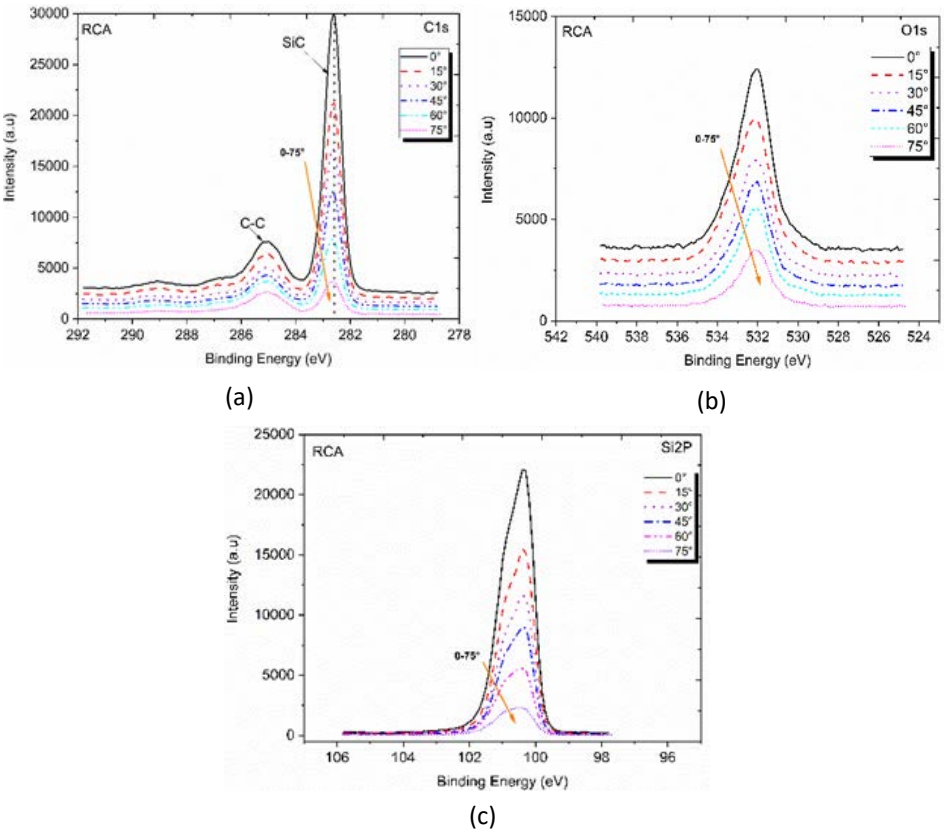


Fig. 4.26: ARXPS spectra of (a) C1s; (b) O1s; and (c) Si2P for the RCA sample.

Fig. 4.26 illustrates ARXPS measurements from 0° to 75° for the RCA sample. Figs. 4.22, 4.23, and 4.24 show the O1s, C1s, and Si2P spectra, respectively, and how as part of SiC components is reduced the rest of the contamination stays. This investigation is required because the escape depth of photoelectrons is smaller at an angle, and the signal comes from the thinner, topmost surface. In this ARXPS study, similar peaks were used to fit the previous data charge corrected for all the peaks to ensure the SiC binding energy equals 100.3 eV. From the C1s spectrum in Fig. 4.26(a), SiC with a small tail of carbon clusters is present. Overall, the C1s spectrum has a maximum signal compared with the O1s and Si2P spectra. Moreover, the O1s spectrum of the RCA sample has the highest binding energy, namely 532 eV.

Summary of XPS analysis

An SiC surface must be uniform, atomically ordered, and free from chemical residues. These features can be achieved with proper chemical treatment and time to obtain high-quality, reliable SBDs using DW. This work demonstrated marked improvements in surface properties, including fewer contaminants, of the 4H-SiC using XPS analysis. The WCT sample was less contaminated compared with the WOCT sample. The WCT sample contains some sodium, zinc, fluorine, tin, and calcium contamination and SiC, O_2, CO_2, H_2O, CO, carbon clusters, Si-pyridinic, and Si-interstitial compared with the WOCT sample, and these contaminations are smaller than in the WOCT sample.

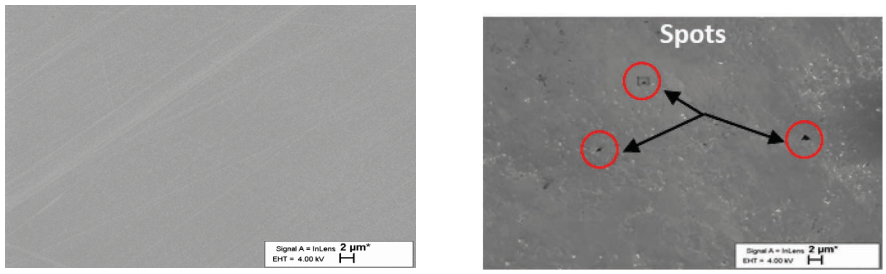
The contamination is even reduced in the RCA sample, but chlorine, sodium, zinc, fluorine, and calcium remain. It can be concluded that the SiO_2 or SiO/4H-SiC (0001) interface obtained by the oxidation process is chemically non-abrupt; graded layers and carbon clusters are present even after the WCT and RCA cleaning process. These findings suggest that HPT and HNPT minimize the SiC spectrum magnitude and remove the oxygen and carbon clusters or carbon interstitials. Furthermore, XPS spectra can be used to calculate the surface band bending. In the next section, Scanning Electron Microscopy (SEM) was utilized to understand and reveal pre-surface preparation, metal deposition, and annealing behavior, all of which can affect the development of a diffusion-welded SiC SBD.

4.5.3 SEM

A field-emission SEM (Zeiss Ultra-55) was used to examine the surface morphology of a p-type 4H-SiC sample with an accelerating voltage of 4 kV to image the epilayer and substrate layer under a vacuum condition. It also examine the DW interface and the bonding strength.

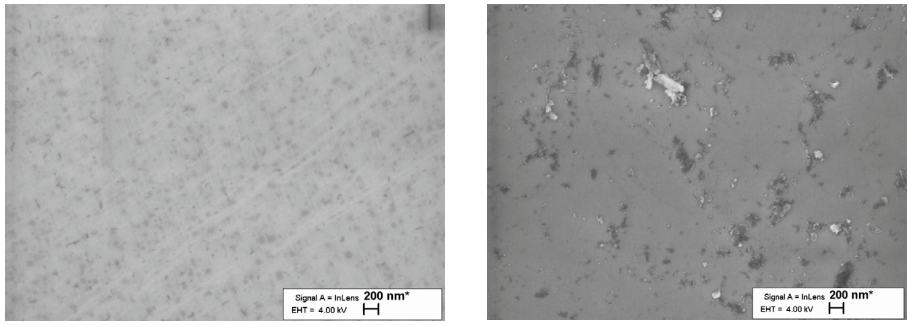
SEM of the surface before and after diffusion welding

In the beginning, the 4H-SiC sample was investigated with simple chemical treatment before DW to identify the epilayer defects before and after DW (Fig. 4.27). It is noted that several chemical interactions take place, revealing various properties of the sample. Specifically, the surface is very flat without any structure or defects, and the bottom side presents some imperfections.



(a) (b)

Fig. 4.27: The scanning electron micrographs of the p-SiC epilayer (a) before and (b) after DW.



(a) (b)

Fig. 4.28: The scanning electron micrographs of the p-SiC substrate layer (a) before and (b) after DW.

Fig. 4.28 shows the micrographs of the p-SiC substrate surfaces before and after DW. There are evident differences in the p-SiC surface. The smooth surface of the p-SiC before DW has changed into a surface with peaks and uniformities after DW, which was confirmed by the AFM investigation discussed in the section 4.5.1.

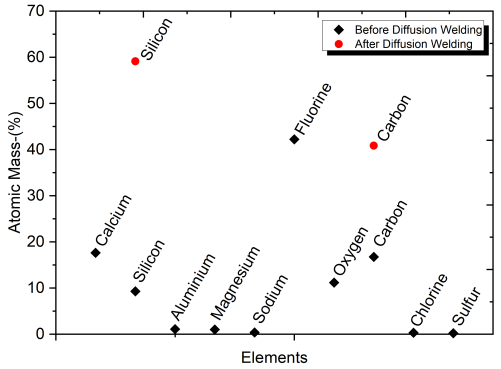
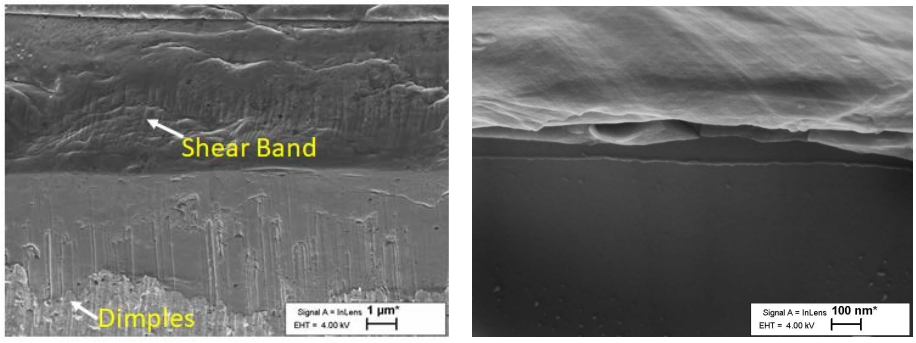


Fig. 4.29: EDS analysis before and after DW on the epilayer.

Spectral analysis was performed using energy dispersive X-ray microanalysis (EDS) with an Oxford instruments INCA energy system. As expected, the p-SiC epilayer surface before DW contains silicon and carbon with black diamond symbols (Fig. 4.29). The spectral analysis in Fig. 4.29 (with red circle) shows the elements left after the DW where SiC surface shows silicon and carbon atoms due to the imperfect surface cleaning.

In this investigation, SEM was used to gain further insight into Al-foil and 4H-SiC epilayer-bonding interfaces. Cross-sectional analysis can be performed at the bonded interface at a sub-micrometer scale. SEM revealed a newly created intermediate interface between the Al-foil and 4H-SiC epilayer.



(a) (b)

Fig. 4.30: The bonding interface observed by SEM shows no breakage but dimples and shear band due to annealing temperature within the device (a) at 1 µm magnification and (b) at 100 nm magnification created between the Al-foil and SiC.

The resulting bonding interface is visible by looking through the sapphire layer. Fig. 4.30 shows that the Al and SiC interfaces are tightly bonded together with very few bubbles or voids at the bonding interface.

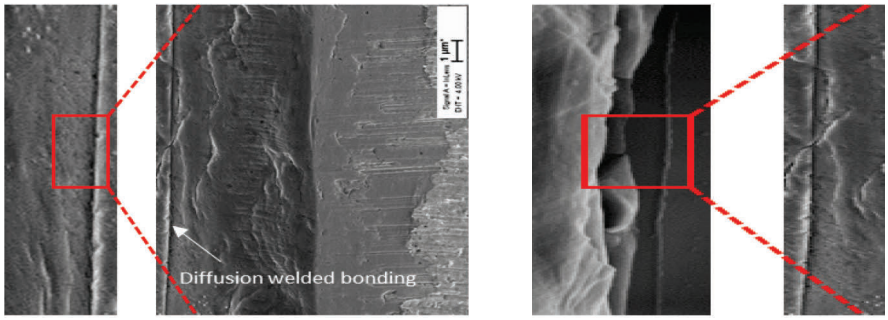


Fig. 4.31: High-resolution scanning electron micrographs of Al-foil/SiC direct bonding interface (a) at 1 µm magnification and (b) at 20 nm magnification.

There was no crack present in the interface. Unfortunately, breakage in the interface occurred while preparing the cross-section. Due to stress concentration, there are some tiny island-like dimples and shear bands. These dimples are created during the initial shear process due to their flexible nature. The shear band began due to the thermal stress present at the bonding interfaces, a phenomenon that means better bond quality with higher shear strength.

Although the crystal orientations were not precisely aligned during the pre-bonding process, there are no dislocations and defects in the region around the bonding interface in Fig. 4.31. Due to the limitation of high-resolution SEM, it is not possible to magnify atomic-level connections that occur at the bonding interface; thus, it is necessary to employ TEM.

4.5.4 TEM analysis

The interface plays an essential role in metal–SiC joint properties, such as the mechanical reliability of the joints and composites. The bonding structures were analyzed by very high-resolution microscopy (TEM) to gain further insight into the diffusion-welded Al-foil/4H-SiC SBD bonding interface.

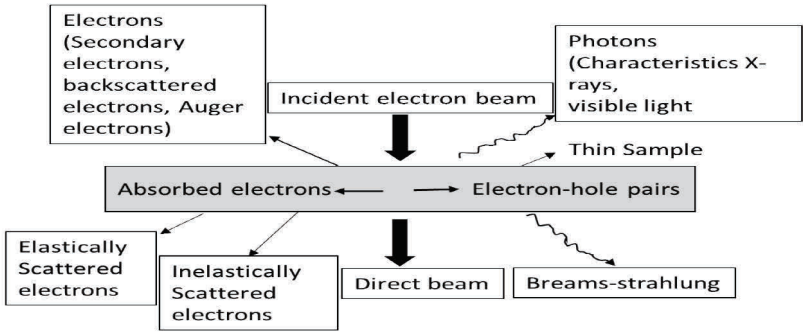


Fig. 4.32: TEM signals created by the interaction of a high-energy electron beam with a thin specimen (modified from [112]).

TEM uses a parallel beam of electrons transmitted through the sample; these electrons interact with the crystalline lattice as they pass through. When the electron beam passes through the crystalline lattice of a sample, the beam's amplitude is attenuated and the electrons are scattered. The extent of the attenuation of the beam is proportional to the square of the atomic number. The amplitude of the beam is proportional to the type of element that goes through its path. Finally, one can construct a map of elemental images based on the variations of the scattered intensity of a beam. Fig. 4.32 shows the measurable signals generated by the interactions of the beam electrons with a thin specimen. Details of TEM can be found in the textbook by D.B. Williams and C.B. Carter [112].

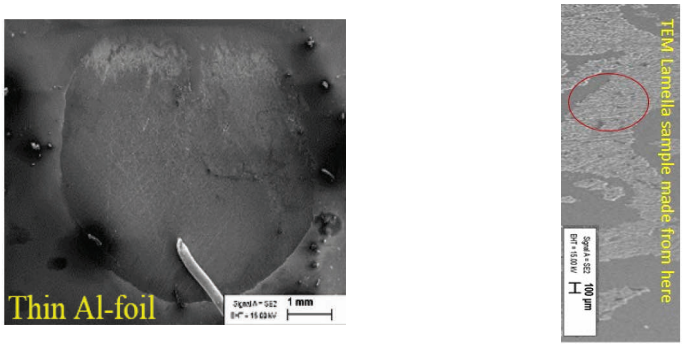
Sample preparation

The bonding interface between aluminum foil and silicon carbide epi-layer has been studied using scanning transmission electron microscopy (STEM). STEM measurements have been performed in Cs-corrected Titan Themis 200 (Thermo Fisher Scientific (former FEI)) (scanning) transmission electron microscope at 200 kV. For STEM study a thin cross-sectional lamella was prepared from the sample using Nanolab 600 Dual Beam scanning electron microscope – focused ion beam (SEM-FIB) system (Thermo Fisher Scientific (former FEI)). Here, high-resolution TEM has been used to study the Al-foil and SiC bonding interface based on detecting the signals caused by the interactions of a high-energy electron beam. To reduce the time for lamella preparation; the thickness of the Al was reduced by polishing the upper side of the sample mechanically on a diamond disc using tripod polisher.

Fig. 4.33: Photograph of the bonded high-temperature Al-foil/4H-SiC SBD. The sample thinning prepared by gluing the assembly and polishing and grinding with a diamond disk (from left to right).

The high-resolution SEM (scanning electron microscopy) was used to examine the surface of the sample after grinding to identify the areas suitable for lamella preparation by SEM-FIB. Fig. 4.34 shows micrographs at different magnifications of the Al-foil/4H-SiC SBD sample after the mechanical grinding and polishing. As can be seen in Fig. 4.34(a), the bonding interface is nearly uniform, without gaps in the long

vertical view. This means that the connection interface has good crystal quality without being damaged by high-temperature bonding. It is assumed that the sample was contaminated with carbon atoms (perhaps from diamond from the polishing or grinding).



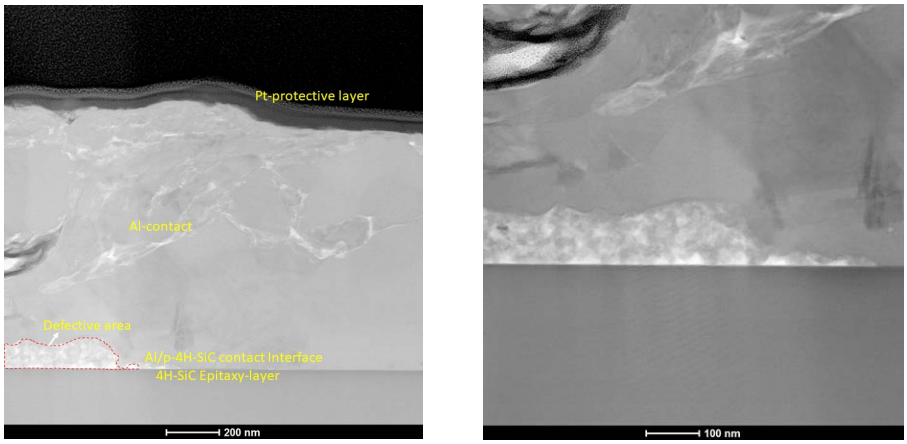
(a) (b)

Fig. 4.34: A scanning electron micrographs of the Al contact layers deposited on an SiC SBD after polishing and grinding: (a) low-magnification overview image; and (b) higher-magnification image showing the area used for preparing cross-sectional lamella for STEM studies.

To minimize the foreign defects while grinding and polishing, mask covering outer borders of aluminum film were made with the help of wax. In this way, the aluminum-free hole would be visible in the sample center by etching off aluminum. Then, the close-to-hole areas are suitable for the preparation of the lamella by FIB; Fig. 4.34(b) shows the area from where the FIB lamella was made. Thus, there is a greater possibility of finding defect(s) in the lamella. Most of the aluminum electrode was removed so that only 0.5–2 µm remains; this step decreases the time for lamella preparation and it should not affect the quality of lamella. Of note, the lateral dimensions of the lamella are also limited by FIB preparation. Usually, lamellas are 10–20 µm in length and only part of the prepared lamella is polished thin-enough for STEM observations. If larger lamella are made, they could bend before mounting on the TEM sample holder due to their thinness. The Al-foil/4H-SiC bonded structure specimen used for TEM was successfully prepared by using SEM-(Helios NanoLab 600) FIB demonstrates that the bonding interfaces also have adequate bonding strength.

TEM measurements EDS analysis

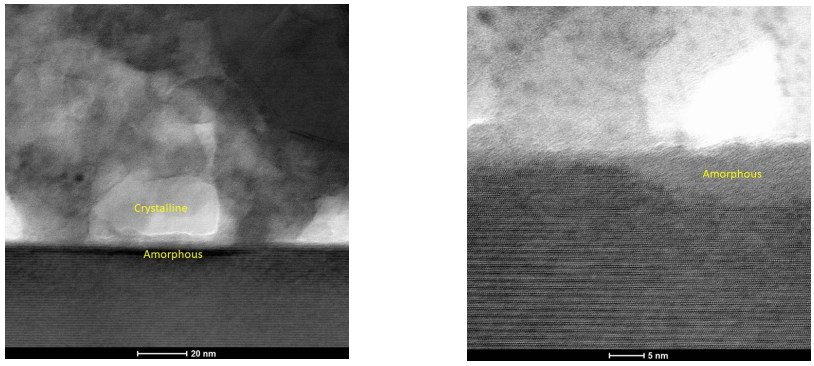
The STEM images of the bonding interface between Al contact and SiC are presented in Fig. 4.35. The interface is uniformly and firmly bonded with no sign of gaps or cracks, which confirms that a seamless bond on the micro-scale has been accomplished. This is a bright-field image, so holes appear brighter; the greater the thickness, density, and atomic number, the darker the area appears on the image. The “Pt” layer is also noted; it was introduced as a protective layer to avoid sputtering of the area of interest drying lamella preparation.



(a) (b)

Fig. 4.35: (a) Scanning transmission electron microscopy (STEM) bright-field micrograph of the SiC diffusion-welded SBD samples observed from a cross-sectional view; and (b) Higher -magnification image of the defect area.

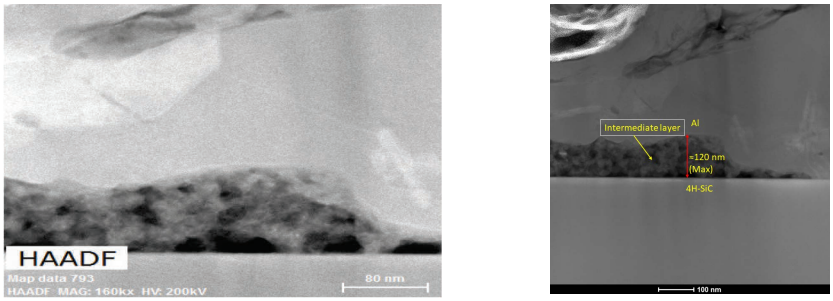
However, the interface area is not completely uniform, and some defects at the bonding interface still can be distinguished in Fig. 4.35. When the interface is amplified to a high-resolution image of 200 nm magnification, some of the areas of the bonding interface exhibit a defective sandwich structure, indicated with red marking in Fig. 4.35(a); this is a transition layer created between the Al and SiC interface. The defective (red marking) and defect free crystalline areas were further examined with higher resolution.



(a) (b)

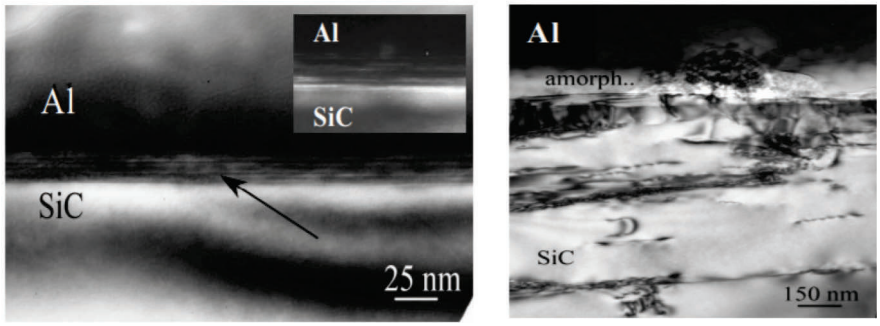
Fig. 4.36: (a) A high-resolution bright-field image of the defect in the interface; and (b) A high-resolution image of the interface (area with a significant defect).

Fig. 4.36 shows higher magnification images of the defective area. Fig. 4.36(a) demonstrates the different lattice formation patterns. The brightest areas are thinner and correspond to holes. These data indicate that the lattice arrangement of the transition layer is not the same, and the crystalline quality is not very uniform. The plane inclusions of small-grained boundaries have emerged; this may occur due to sufficient self-diffusion of interface atoms. At higher magnification, it can be seen that there are crystalline defects and few nano-meters thick area of amorphous formation without holes and rest of the interface are regular crystalline structures, clearly illustrated in Fig. 4.36(b).



(a) (b)

Fig. 4.37: (a) High-angle annular dark-field [HAADF] image of the EDX mapped area; and (b) mapping of the typical large defect area of the Al–SiC nano-film bonding interface (clearly has a defect).



(a) (b)

Fig. 4.38: Transmission electron micrographs of (a) boundary contact zone; and (b) boundary zone in diffracted SiC [5].

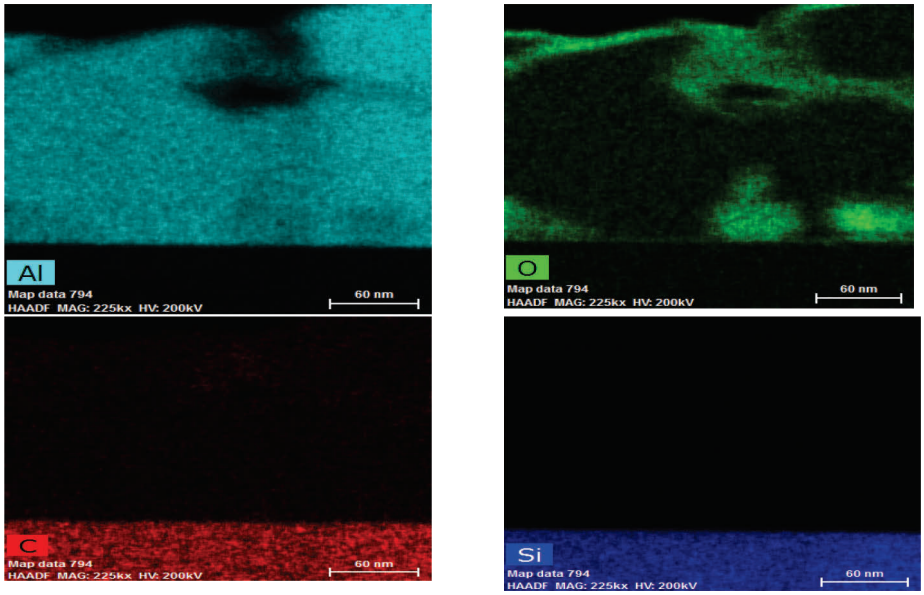
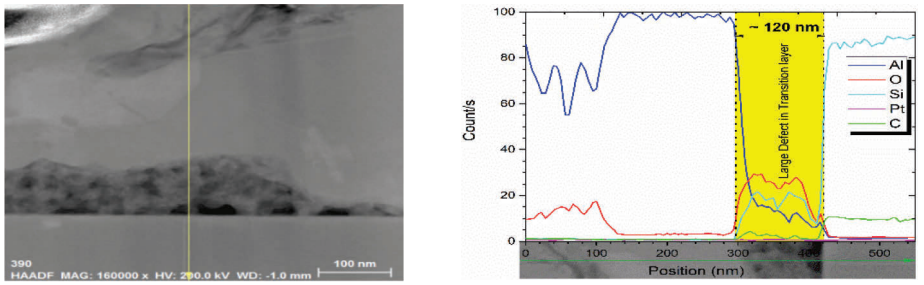


Fig. 4.39: EDS element mapping of aluminum (Al); carbon (C); oxygen (O); and silicon (Si).

Fig. 4.37(a) shows a high-resolution TEM image, with nano-precipitates in the epitaxially grown samples. In the high-angle annular dark-field (HAADF) image of the mapped area, the contrast is different from bright-field images: holes are dark. In general, the higher the atomic number, the brighter this area appears. The typical large defect areas of the Al–SiC nano-film bonding interface are about 120 nm, illustrated in Fig. 4.37(b).



(a) (b)

Fig. 4.40: EDX line analysis of the interface area containing large defect, (a) HAADF image showing the line, where the analysis has been conducted; and (b) The EDX line profiles of the elements in the analysed region.

However, this investigation on Al-foil/4H-SiC interface does not shows any boundary contact zone compared with a previous report by O. Korolkov et al. [5], as shown in Fig. 4.38. Fig. 4.39 shows the micro-defects at the direct bonding interface and corresponding EDS element mapping of aluminum, carbon, oxygen, and silicon.

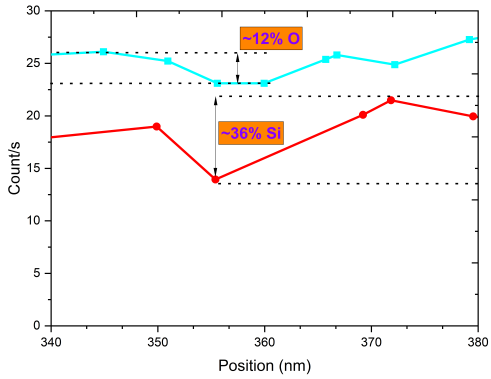


Fig. 4.41: EDX line scanning of large area defect at 120-nm bonding interfaces obtained by DW.

There is also carbon, diamond, graphite, and aluminum, contributed by the diamond disk used to prepare the sample for TEM. Aluminum is oxidized in some areas, including areas near the interface. Lattice images of nano-precipitates, silicon, carbon, oxygen, and aluminum atoms are shown in blue, red, green, and cyan, respectively.

Fig. 4.39 depicts the distributions of aluminum and oxygen atoms across the bonding interface, revealed by EDX mapping. The defect area has a significantly higher oxygen content, but surprisingly it also has a small increase in carbon and silicon content.

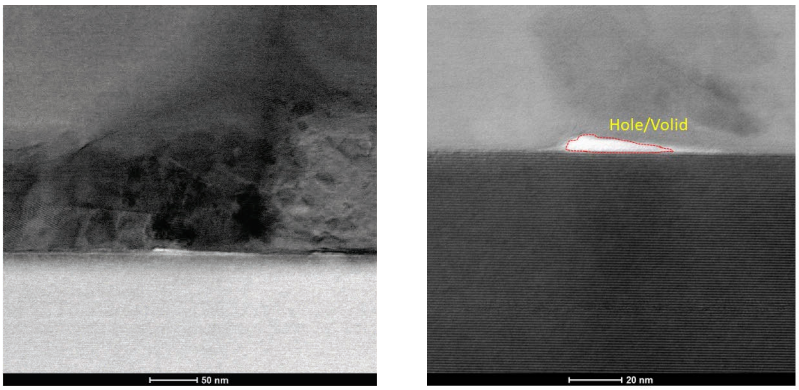


Fig. 4.42: Bright Field images of the area without significant defects. The scale marker in the left micrograph is 50 nm and the scale marker in right the micrograph is 20 nm.

Fig. 4.40(a) shows a line scan at the area with a large defect using EDX measurement. The (yellow) arrow in the image shows where the line scan has been made with a line thickness of 11 pixels (at every distance, the obtained values correspond to the average of 11 scans). There is a significant microvoid of approximately 150 nm in length at the direct bonding interface, which was investigated through the EDX mappings.

Fig. 4.41 shows a comparison of the EDX line scans of silicon and oxygen across the large area defect (at 120 nm). It is noted that the number of pulses generated in the detector by X-ray photons with energy corresponding to the energy of the characteristics X-ray of the elements per second in the EDX line profile. In the Fig. 4.41 shows the count per second on the y-axis expresses the Oxygen atoms are always present and found with a high peak in the EDX line scanning compared with silicon and carbon atoms. According to EDX mapping and linescan, aluminium is at least partially oxidized. The defective area at the interface also show significant increase of oxygen content. Fig. 4.41 evidences that surface cleaning preparation is not sufficient to remove the oxide layer. The oxygen and silicon elements in the EDX line profile are remarkably present, corresponding mainly to the 300–450-nm range. In this range, recrystallization probably starts at the interface obtained by the DW process parameters. These data indicate that some of the silicon clusters might contribute silicon atoms for recrystallization of amorphous structures with aluminum, oxygen, and carbon atoms (Fig. 4.41). However, detecting such silicon clusters using EDX measurement is impossible due to the limitation of resolution or computer power. These silicon and carbon clusters are discussed briefly and DLTS measurement in the chapter 2 section-2.4.3. and chapter 4 section-4.2.3 respectively.

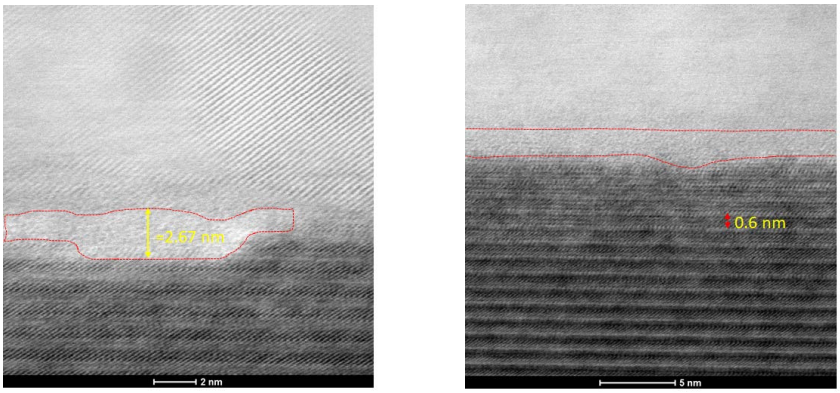
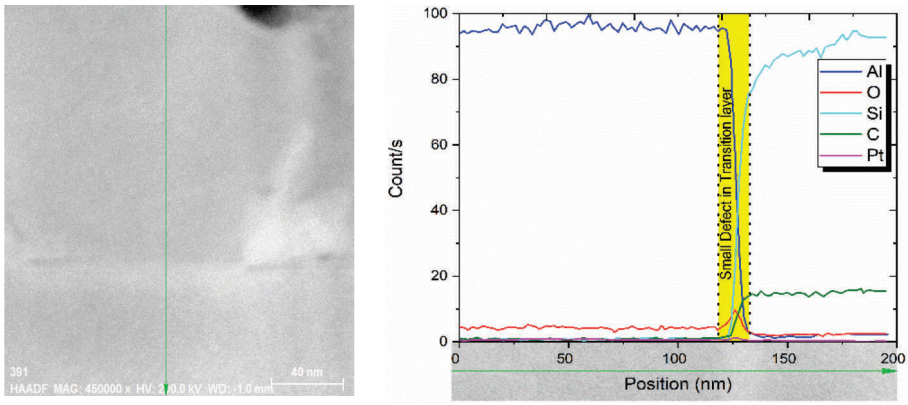


Fig. 4.43: High-resolution amorphous area with 2 nm and 5 nm magnification from left to right.

Fig. 4.41 shows that the dumping point starts from 350 nm and again rises after 360 nm. At 355 nm, oxygen and silicon spectra are reduced, a phenomenon corresponding to finding the bonding point of the interface layer. The minimum amount of silicon and oxygen atoms is 36% and 12%, respectively, less than what is found at the aluminum–SiC interface. However, the concentration of silicon after this point is higher than oxygen at the interface obtained by DW. This increase in silicon in the aluminum–SiC interface might contribute to improve bonding strength.

Even in the areas that appeared quite "nice" at low magnification, at higher magnification, there are some small holes between the SiC and aluminum contact (Fig. 4.42). As illustrated in Fig. 4.39, the bonded microvoid region is mainly composed of carbon and silicon, highlighted in red and blue, respectively. This reveals that the characteristic impurities on the epilayer surface are responsible for forming the microvoid during the bonding process.



(a) (b)

Fig. 4.44: (a) The green line is near the void but not directly at the void region (defect free area); and (b) EDX measurement in the "nice" area.

Fig. 4.43 shows that there are also areas with no void or holes. A very thin, amorphous, wavy layer with a thickness of ~1 and ~2.67 nm could be discerned at the interface. The thickness of amorphous layers changes slightly is likely caused by the

transition time difference of the DW process parameters (from cycle III to IV, discussed in chapter 3, section 3.5) changes for the metal (aluminum) and semiconductor (SiC) bonding surfaces.

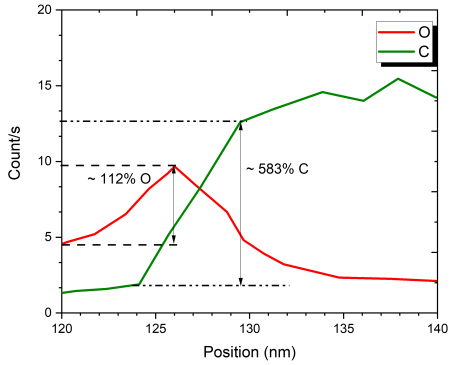


Fig. 4.45: EDX line scanning of a small-area defect at 2.67 nm at bonding interfaces obtained by DW.

However, there is not yet enough information to define precisely but it is worth considering a possibility that the Oxygen peak in this region is due to oxidation of the Al and/or epi-layer, not because of the precipitates in this amorphous region conclusively. However, the defective area is smaller compared with a previous report by O. Korolkov *et al*. [5], as shown in Fig. 4.38. This improvement in the minimized defective areas was achieved by controlled or optimized cleaning and manufacturing process parameters introduced in the recent development and analysis of diffusion-welded SBD.

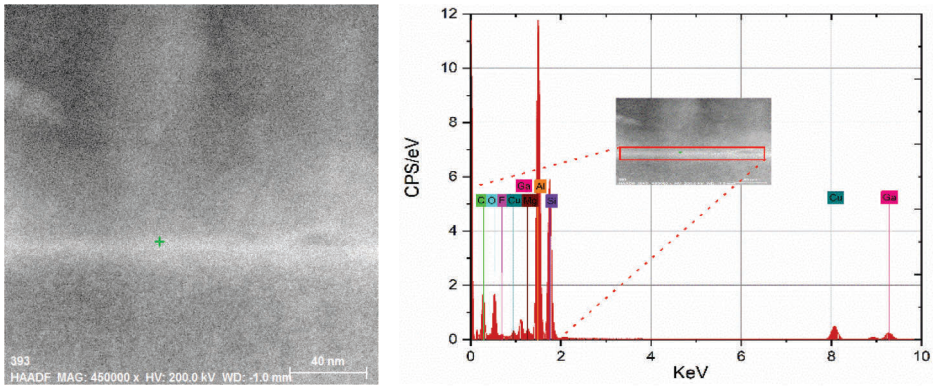


Fig. 4.46: EDX point analysis of the interface, (a) HAADF image showing the area where the point analysis has been performed is marked by green cross. This cross point has been irradiated by electron beam during analysis; and (b) EDX spectrum recorded from the area marked in (a).

Fig. 4.44 llustrates that there is a slight increase in oxygen content at the interface between Al and Si. The increase is relatively small, and the thickness of this oxygen-richer layer is only ~2.67 nm. Fig. 4.45 (deduced from Fig. 4.44) indicates that at the “nice” area where small defects are considered, the intensity of oxygen and carbon signal along with the silicon (Fig. 4.44 (b)) atoms increase at the bonding interface in the interfacial layer.

In addition, there is a clear maximum in oxygen concentration at the Al and SiC interface. The increase of C due to SiC and the increase of C profile can be gradual even in the case of sharp interface as the broadening of the electron beam in the sample (lamella). There is also some roughness at the interface shown in the Fig. 4.45.

The amount of oxygen and carbon count/s increased by 112% and 583%, respectively, at the small defect interface. The tiny oxygen defect or silicon, carbon, and oxygen cluster formation during high temperature may induce the formation of this region. However, the silicon atom concentration increases rapidly immediately after this defect or cluster formation at the interface obtained by DW. This increase in silicon and carbon at the aluminum–SiC interface might improve the bonding strength of DW. It arguably indicates that aluminum-induced amorphous layers provide consistently high thermal stability and protect it from being further oxidized at a high temperature.

Fig. 4.46 shows EDX-point element spectra in the diffusion-welded Al–SiC interface. In addition to aluminum, silicon, carbon, and oxygen present according to EDX, copper and gallium are also present. These elements are expected: the TEM grid is made from copper and therefore a copper signal is always present, and the lamella was cut using a gallium ion beam.

The atomic profile of carbon, aluminum, silicon, and oxygen across the interface was investigated by EDX-quantified line scanning, shown in Fig. 4.47.

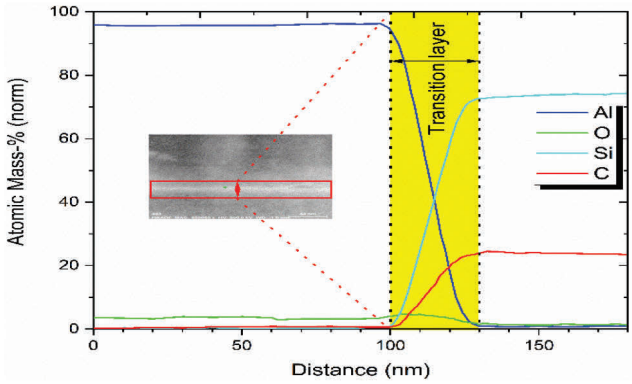


Fig. 4.47: EDX-quantified line scanning spectra of the direct bonding interface made in the "nice" area.

The carbon, aluminum, silicon, and oxygen atomic mass ratio (%) at the transitional layer region between the Al-foil and 4H-SiC amorphous layer was measured. Fig. 4.47 indicates that the surface oxide layer of the SiC epi-layer is almost constant, and a mixing layer of silicon and carbon is present primarily and increased at the interface. It is more likely that the interface between Si and C is not sharp enough because of the broadening of the electron beam of the sample. At the same time, the aluminum content decreased a phenomenon that could be due to the low solubility of aluminum deposition by DW. In addition, silicon and carbon atoms content decreases rather synchronically compare to Aluminum and Oxygen. This good atomic mass ratio diffusion into aluminum nano-films and the interfacial mixing between amorphous SiC and Al-film contribute to the robust bonding resulting as Al-foil/4H-SiC SBD.

Discussion

Based on TEM observation of the DW bonding interface, the defective area is a wavy structure with different degrees of crystallization, and some of the aluminum atoms have diffused or migrated to form atomic-level connections at the aluminum–SiC epilayer interface. Combining the XPS, SEM and TEM results, the crystallization of the aluminum and SiC films during bonding can be described as follows:

In the beginning, the SiC epilayer contains many O-H and Si-O bonds, and the Al-foil contains Al-OH bonds created during the cleaning process. During DW, as the introduced temperature and pressure increase, the O-H bond distance is reduced, and elastic deformation occurs between the Al-foil and SiC. This film rebounds to form a stable crystalline structure. Nevertheless, the transition layer remains an intermediate layer. It is assumed that the crystallization of the Al-foil and SiC starts from this interface and then crouches along the neighboring area until the two-film contact interface ends. At this stage, the distribution of the bonding interface becomes denser or thicker. Furthermore, it improves the quality of the aluminum–SiC contact depending on the DW chamber pressure. In this phase, most of the amorphous layer could be discerned at the aluminum–SiC interface. This ≈2.67-nm thick amorphous layer consists of an oxygen-richer layer, is controlled by the introduced temperature, and applied temperature during DW. It can be concluded that the intermediate transition layer is most likely the transitional crystal that is left in the process of converting the amorphous layer. Another possibility is that the minimum intermediate (≈2.67-nm thick) transition layer is not on the same crystal plane because the dislocations develop during crystallization. By optimizing the process parameters, this study shows that it is possible to improved interface defect of previously developed diffusion-welded Al-foil/n-4H-SiC SBD, where it has been observed a ≈25-nm thick layer based on TEM [5].

4.5.5. Summary of TEM analysis

The TEM analysis of DW Al-foil/4H-SiC SBD revealed that a nano deformation intermediate layer of ~2.67 nm and some amorphous layer is formed directly on the SiC surface after DW. It can be concluded that this new crystallinity and deformation of material at the subcontract layer formation are influenced by the DW process parameters (elevated temperature and tangential forces that couple and introduced shear micro-deformations during DW). It is found that optimized thermal deformation parameters during DW can control the interfacial layer thickness and minimize the tunneling current. These results represent good agreement with the XPS results, in which the initial contact surface of SiC before DW has an ideal crystal structure free of defects. The shear strength still more significant enough, indicating that this binding structure has good stability at a high temperature. These results suggest that DW with Al-foil has a strong bonding interface and demonstrate that it could potentially increase power module competitive reliability.

5. SiC SBD irradiation

Human civilization has adopted technologies in their daily life to sustain progress in society. Automotive industries, power plants, and space technology will consume more energy in the future, where the primary concerns are high temperature and radiation resistant sustainable electronics or modules. Efforts need to be taken to improve the reliability of potential requirements of those consumable electronics or modules. Semiconductors with high bonding energy, such as diamond, and SiC are traditionally thought of as radiation-resistant materials and will replace the recent Si-based technologies. High bang gap semiconductor n-type 4H-SiC has been proved as a radiation-resistant material capable of surviving exposure to high-energy particle bombardments, such as electrons, protons, neutrons, and gamma radiation, without degradation of its semiconductor or semiconductor–device material parameters. It is now of practical interest to check the reliability and to what extent the radiation resistance of p-type 4H-SiC corresponds to theoretical predictions. In this chapter, electron radiation resistance to p-type 4H-SiC Schottky barrier diode is considered to understand the general concepts of defect mechanisms and their properties of radiation defects (vacancies, interstitials, and associated defects) in SiC because of irradiation. These radiation-induced defects often have energy states in the bandgap. They can influence significantly the detection properties like energy resolution and charge collection efficiency of the diodes [113], [114].

5.1. Introduction

Development of next-generation diode structures and electronics is necessary to produce a broad scope of devices operating under elevated radiation levels, at high temperatures, and in chemically active media to ensure safety during operation at atomic and space stations in radioactively contaminated areas. These electronic hardware components should have long-term dosimetric monitoring of electron, neutrons, and charged particles at high temperatures [115]. It is assumed that there are intrinsic defect properties in both n- and p-type 4H-SiC epilayers of unipolar and bipolar devices. These play a critical role in determining its overall electric properties, and they need to be understood to overcome potential problems.

The application of radiation-defect engineering (RDE) has progressed steadily in the electronic device industries to understand radiation resistance hardness. This work, investigated electron irradiation resistance of p-type 4H-SiC SBD. Electron irradiation is an attractive method to extract electrons by commercial accelerators; it is capable of a greater penetration depth than protons and other ions to control the carrier lifetime of SiC-based devices. Electron irradiation could improve electrical parameters, namely reduce the turn-off time, reverse recovery charge, or ameliorate the recovery loss that concerns a high-speed device with a higher ON-state voltage suitable for hard switching at two- or three-level power converters and creates thick semi-insulating layers [116].

Several groups have investigated extensively deep-level electron irradiation of n-type 4H-SiC and the carrier concentration of irradiated samples [71], [117], and [118]. The most prominent low energy (up to 200 keV) electron irradiation DLTS spectrum in n-Type-4H-SiC is the Z_1 /Z_2 electron trap at about 0.7 eV below the conduction band. It usually presents in n-type 4H-SiC epilayers but can increase defect concentrations as the temperature increases [119], after electron irradiation, and with increased irradiation

time. Other detected defects include electron traps, namely EH_1, EH_2, EH_3, located at 0.4–0.7eV [120]; and EH_5, EH_6, and EH_7 defects located at 1.5–1.6 eV below the conduction band [120], as observed by high-temperature DLTS measurements [119]. However, limited information is available about deep levels in p-type epilayers (hole traps) in the lower half of the bandgap of SiC [71] and hole traps induced by irradiation [119]. Deep-level defects act as recombination and generation centers, a possible lifetime killer, and controlling deep-level defects (hole traps) is essential to create high-purity semi-insulating substrates [70], [71]. The number of deep-level defects also needs to be decreased (reduced on-state loss) to ensure a long carrier lifetime, which is essential to obtain sufficient conductivity modulation, resulting in a lower on-state voltage.

On the other hand, a lifetime that is too long will cause considerable reverse recovery, leading to redundant switching loss (removing stored excess carriers during the turn-off transient) [121] and limiting the switching frequency. Therefore, detailed investigations on hole traps (acting as minority carriers) is necessary to understand electron-irradiation-induced defect structure and the impact of individual defects on electrical parameters. The electrical investigation of irradiated p-type epi-layer of 4H-SiC SBD by examining I–V and C–V characteristics, and evaluated the charge states of trap levels in p-type epilayers by using DLTS and LDLTS.

5.2. Physical understanding of irradiation-induced defect formation

To understand the theory behind the formation of irradiation-induced defects in the p-type 4H-SiC SBD samples, it is necessary to understand the atomic vibrations, electron–matter interactions, elastic and inelastic scattering, displacement energy, energy loss mechanism, Frankel pair generation, and vacancy lifetime or irradiation duration estimation. This section also covers the generation, recombination, compensation, and trapping mechanisms for holes in 4H-SiC.

5.2.1. Electron–matter interactions and energy-loss mechanisms

When high-energy particles pass through target materials, they deaccelerate and transfer their energy to the matter. This transferred energy is adopted by the neighboring atoms and then modifies the structures and properties of the target material. There are two main mechanisms that cause the energy loss of crystalline semiconductors: (a) elastic scattering and (b) inelastic scattering (Fig. 5.1). An elastic collision conserves kinetic energy and momentum. By contrast, an inelastic collision saves total energy and momentum. Part of the electron kinetic energy is converted into excitations of the electronic (and vibrational) degrees of freedom in the material. Inelastic scattering is applicable in insulators, typically at oxides irradiated at high current densities. These local electric fields are strongly induced and interact with the electronic system of material and may contribute directly to phase transformations and damage [122]. Inelastic scattering ionization activated via radiative or Auger recombination of a core hole may weaken chemical bonds. It may convert into the momentum that activates knock-on damage at even lower electron energies [123]. Thus, damage formation in a semiconductor crystalline structure is a complex multi-body collision process (e.g., a recoil atom can bounce back to its lattice position or kick back another atom to its previous lattice position). There are several theories of electron irradiation damage based on elastic scattering because it is the dominant and most influential method in semiconductor electronics.

5.2.2. Displacement of atoms in solids

Electron irradiation damage is dominated by the displacement energy (E_d) of the atom from the bulk of the SiC crystal. Electron-irradiation-induced material transformation will occur because the projectile electron can transfer energy (E) is more remarkable than the displacement energy (E_d, several thousand eV) to the SiC lattice atoms. Andersen [124] stated that the boundary of electron energy for most materials should be greater than the formation energy of vacancy Frenkel pair generation. The minimum boundary electron energies required for the formation of radiation defects was observed by [125] as ~250 keV in a silicon sublattice and ~90 keV in a carbon sublattice on the bombardment of SiC. For the physical interaction of the electron with any material, the relativistic effect must be encountered because the transferred energy is limited strictly by momentum conservation (as an electron is ~22,000 times lighter than carbon and moves at a fraction of the speed of light). In practice, relativistic electrons pass through a thin material so fast that sample thickness and morphology play a vital role in the electron irradiation process. In inelastic scattering, an electron can transfer momentum energy *E* to rest mass m_e from an atomic nucleus with mass *M*. Moving at a velocity v parallel to the beam (c is the speed of light) may cause knock-on damage by a high electron scattering angle θ. The relativistic energy-momentum conservation leads to elastic energy transfer that can be express by (5.1).

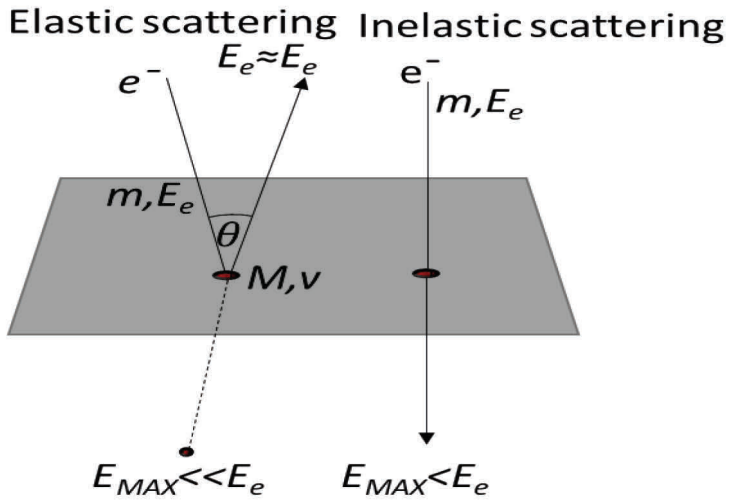


Fig. 5.1 Scattering process of an atom in solids.

$$E(E_e,\theta,v)=\frac{2\left(E_e\left(E_e+2m_ec^2\right)+\sqrt{E_e\left(E_e+2m_ec^2\right)Mvc}\right)\left(1-\cos\theta\right)+\left(Mvc\right)^2}{2Mc^2} \quad (5.1)$$

In (5.1), E_e is the scattering of an electron with kinetic energy. For a nucleus velocity at rest ($v = 0$), (5.1) is formulated according to [126] as (5.2) and (5.3):

$$E(E_e,\theta,v=0)=\frac{E_e\left(E_e+2m_ec^2\right)(1-\cos\theta)}{Mc^2}, \tag{5.2}$$

$$E(E_e,\theta,v=0)=\frac{2E_e\left(E_e+2m_ec^2\right)\left(\sin^2\frac{\theta}{2}\right)}{Mc^2}. \tag{5.3}$$

At a high electron scattering angle θ = 180° (backscattering), the maximum energy transferred, which is equal to the threshold voltage of the defect, is given by [127] as (5.4):

$$E_{\max}\left(E_e,\theta=180°,v\right)=\frac{\left(2\sqrt{E_e\left(E_e+2m_ec^2\right)}+Mvc\right)^2}{2Mc^2}. \tag{5.4}$$

Equation (5.4) can be simplified from [43], where E_{max} is the transferred energy greater than the displacement threshold energy and damage occurs according to (5.5) and (5.6):

$$E_{\max}\left(E_e,\theta=180°,v\right)=\frac{2E_e\left(E_e+2m_ec^2\right)}{Mc^2}, \tag{5.5}$$

$$E_{\max}\left(E_e,\theta=180°,v\right)=\frac{E_e\left(E_e+1.022\right)}{(469.A)(MeV)}. \tag{5.6}$$

Kozlovski *et al*. [43], [128] determined the boundary electron energy above which primary vacancy-interstitial atom (point defects) begin to be generated. According to [43], considering 0.9-MeV electron irradiation, the cross-section can be derived for intermediate-Z elements as (5.7) and (5.8):

$$\sigma_d=\left(\frac{1}{4\pi\varepsilon_0}\right)^2\left(\frac{2\pi Z^2e^4}{E_dMc^2}\right), \tag{5.7}$$

$$\sigma_d=\left[\frac{140Z^2}{AE_d(eV)}\right](barn). \tag{5.8}$$

Kozlovski *et al*. [43], [128] estimated and described the energy requirements for recoil carbon atoms and the Frankel pair generation in the carbon sublattice on the energy E_e of electrons that impinge briefly.

5.2.3. Theories of displacement of detector properties

Defects introduced by irradiation may act as acceptors or donors in Au-sputtered/p-type 4H-SiC Schottky diode, and these impact the effective doping concentration. These impurities create defective complexes and contribute to the space charge and change the properties of a detector. At an electron irradiation < 200 keV, displacement of carbon atoms mainly occurs [129]. At energy > 200 keV, displacement of both carbon and silicon atoms is introduced [118]. This displacement damage in carbon and silicon atoms may influence and degrade the SBD electrical properties in three ways: effective doping concentration, trapping of charge carriers, and increase current due to generation and recombination of charge carriers (Fig. 5.2) [130].

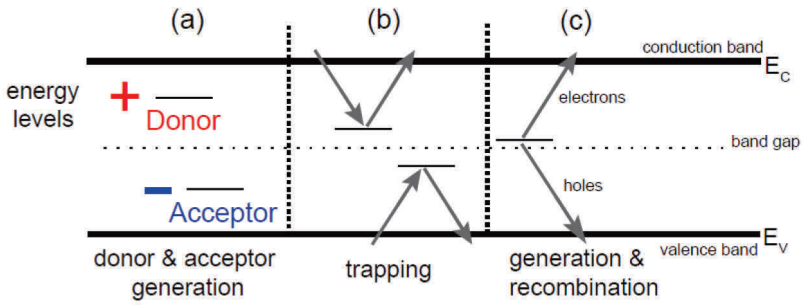


Fig. 5.2: Effects on detector properties due to radiation-induced defect levels in the band [130].

In this study high resistivity Al-doped p-type SiC material was considered with a doping concentration of 1×10^{15} cm^{-3}. It was hypothesized that the acceptors are created during irradiation. In this case, the positive space charge of the initial doping is reduced by the negative space charge of the acceptors and reduces the available free carriers, and thus the depletion voltage decreases. At a certain point, the creation of acceptors compensates for the initial Al doping. The material undergoes inversion from n-type to p-type or could still be in p-type (boron doped), with deactivated initial aluminum doping, forming vacancy–aluminum complexes or creating the E center. Defects with a high capture cross-section and a more considerable emission time constant are considered most harmful for the properties of electronics. The probabilities of these processes and the occupation of defects are discussed theoretically in chapter 2.6.1.

5.3. Irradiation sample preparation and measurements

5.3.1. Sample preparation

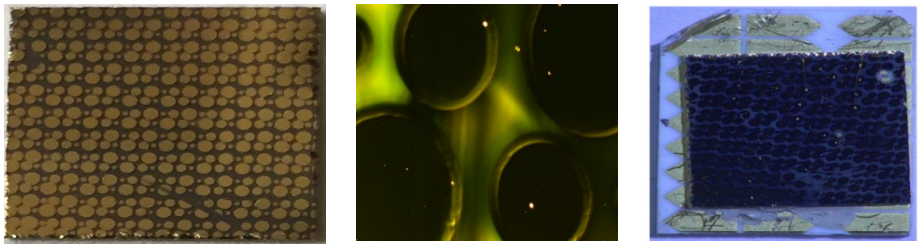
The Au-sputtered contacts have been subjected to 0.9-MeV electron irradiation at different doses at the IOFFE institute. Schottky contacts with four different diameters – 50, 100, 200, and 500 µm – of gold were deposited by sputtering on a diced 10 mm × 10 mm highly doped 4H-SiC substrate. Epilayers are 10-µm thick with $1 \times 10^{15} cm^{-3}$ Al-doped surface of the p-type 4H-SiC. The ohmic contact was formed by burning a deposited nickel film at 800°C to obtain reliable capacitance values from C–V and DLTS measurements. The electrical and microscopic analyses (before and after annealing) were performed on the sample shown in Fig. 5.3(a). The sample was irradiated with electrons and did not undergo heat treatment after contact formation. Fig. 5.3(b) shows the atomic force micrographs of the contact pattern (diffraction mode, 50x). The sample was mounted on ceramic substrates with silver paint to get better electrical results, as shown in Fig. 5.3(c).

5.3.2. Irradiation

Electron irradiation was carried out by a resonant transformer accelerator (pulse frequency 490 Hz, pulse duration 330 μs). The electron beam current density was 12.5 μA/cm$^{-2,}$ and the radiation dose (with a fluence) $\Phi = 5 \times 10^{14}$, which corresponds to the range of 0.125–3 MGy. The sample surface temperature may be increased with the irradiation time, and unintentional heating in the irradiated region can suppress the formation of point defects. The samples were placed on a water-cooled target, and no other voltage was applied to the electrodes of the structure during the irradiation. The mean free path in SiC of electrons with an energy of 0.9 MeV is ~1000 μm [128], so defects created by irradiation were generated uniformly over the entire thickness of the structure. After irradiation, thermal treatment was not performed.

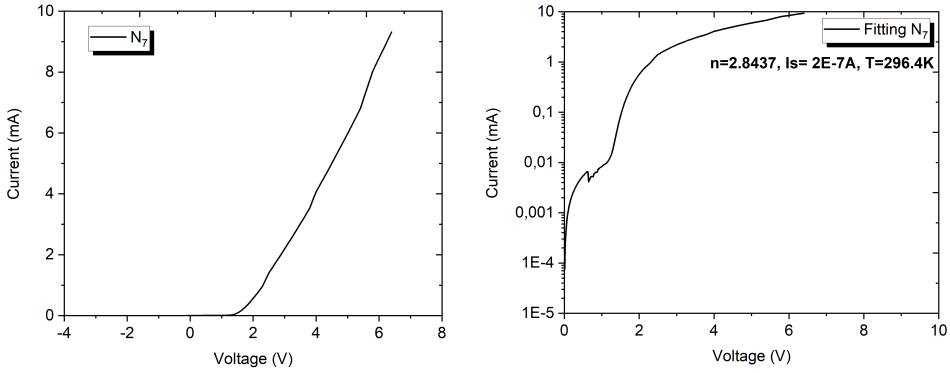
5.3.3. I–V characteristics

The I–V characteristics of Au-sputtered/p-type 4H-SiC samples were measured using the DLS-83D.



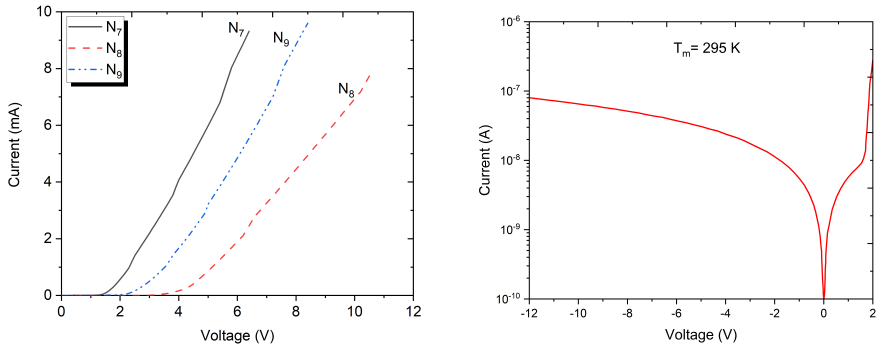
(a) (b) (c)

Fig. 5.3: (a) A photograph of the multi-point contact Au-sputtered/p-type-SiC SBD; Atomic force micrographs of (b) the Au-sputtered contacts to p-type SiC pattern (diffraction mode, 50x); and (c) mounted on ceramic substrates with silver paint.



(a) (b)

Fig. 5.4: (a) I–V characteristic and (b) fitting for detection of the ideality factor of the Au-sputtered/p-type 4H-SiC SBD epilayer after 0.9-MeV electron irradiation of a 0.56-mm contact area.



(a) (b)

Fig. 5.5: (a) I–V characteristics and (b) forward characteristics with isolating properties and reverse characteristics of the ideality factor of the Au-sputtered/p-type 4H-SiC SBD for a 0.56-mm contact area subjected to an irradiation dose of 5 × 10^{14} cm^{-2}.

I–V measurements estimated the resistivity and the ideality factor of the irradiated sample. From Fig. 5.4, the ideality factor is greater than unity (η) of ~3 with a series resistance (R_s) of ~438.73 at room temperature. Fig. 5.5 shows the plots of forward I–V characteristics for the samples subjected to 0.9-MeV electron irradiation. Fig. 5.5(a) shows that the I–V curves differ even inside of one group (with an irradiation dose of 5 × 10^{14} cm^{-2}). This influence of the electron irradiation in forward I–V characteristics within the similar dose of 6 × 10^{16} cm^{-2} was also noted in [140]. The recorded I–V curves show that the effect of irradiation is more apparent at low and high forward biases. Although forward current on the exponential part of the I–V curve does not change significantly, the recorded I–V curve in Fig. 5.5 (b) shows that there are some problems with the forward current of the diode. This problem in forward characteristics is likely caused by a layer with isolating properties. However, the leakage currents are negligible for the irradiated Au-sputtered/p-type 4H-SiC SBD sample. To understand the details of this isolation problem within the same irradiation dose, further investigation with various measurement techniques is required.

5.3.4. C–V characteristics

C-V measurements were performed to estimate the doping concentration or the depth of the semi-insulating region of Au-sputtered/p-type 4H-SiC SBD. Fig. 5.6 show the diode capacitance dependence with an irradiation dose of 5 × 10^{14} cm^{-2}. From Fig. 5.6(b), the irradiated samples exhibit a capacitance of ~38 pF; in Fig. 5.6(a), there is almost a flat dependence or reduced capacitance within the same sample for the same irradiation dose of 5 × 10^{14} cm^{-2}. This extensive variation in capacitance increase or decrease indicates trap dependency on the frequency of emission time created within the sample even by the same irradiation dose.

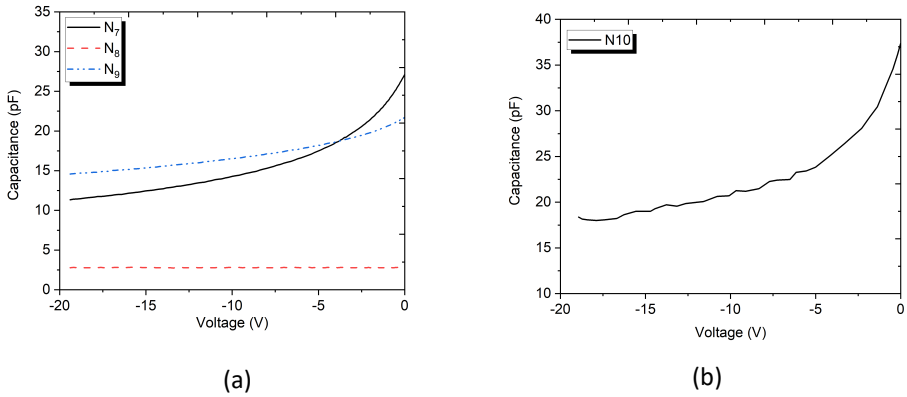


Fig. 5.6: (a) C–V characteristics and (b) high capacitance within the same Au-sputtered/p-type 4H-SiC SBD sample for a 0.56-mm contact area subjected to an irradiation dose of 5 × 10^{14} cm^{-2}.

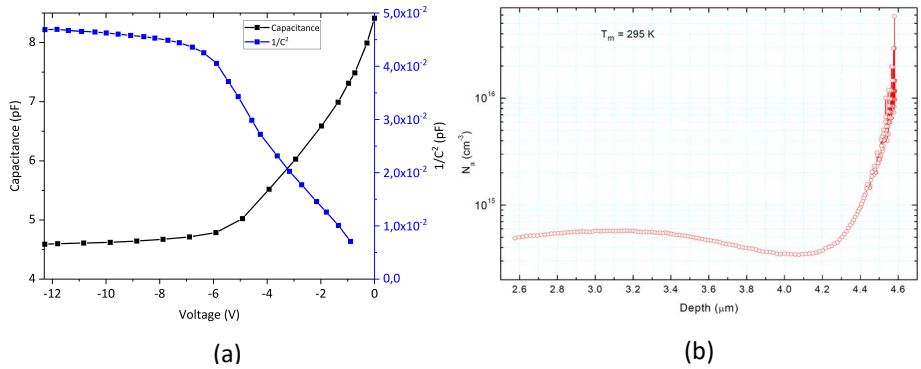


Fig. 5.7: (a) Capacitance depends on $1/C^2$ characteristics and (b) dopant concentration profile of the Au-sputtered/p-type 4H-SiC SBD subjected to electron irradiation. These graphs consider a 0.56-mm contact exposed to an irradiation dose of 5 × 10^{14} cm^{-2}.

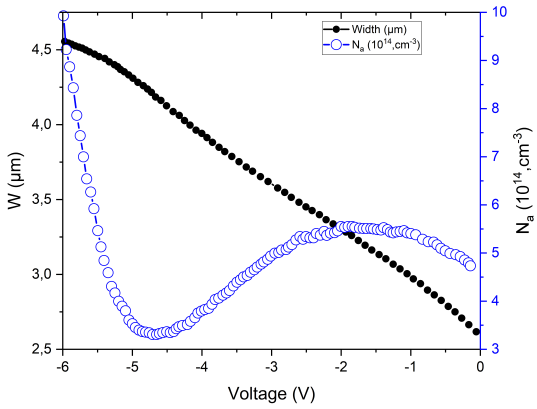


Fig. 5.8: The bias dependencies of Width and acceptor doping values for electron-irradiated Au-sputtered/p-type 4H-SiC SBD epi-layer at 295 K.

The significant increase or decrease in capacitance within the same irradiation dose could be because the capacitance of the traps is drained out and cannot contribute to the capacitance. Of note, capacitance dependences of $1/C^2$ characteristics for the irradiated 4H-SiC SBD indicate uniform space charge distribution and doping concentration.

Fig. 5.7(a) shows the recorded $1/C^2$ curves for the irradiated Au-sputtered/p-type 4H-SiC SBD sample. The capacitance is minimal and exhibits minimal dependency on the reverse bias voltage by the Au-Schottky contact. Fig. 5.7(b) shows the non-uniform capacitance with the doping profile. This indicates that the dopant concentration profile is not uniform even within the epilayer of the SiC SBD.

Fig. 5.8 presents more evidence regarding the bias dependencies of width and the distribution of doping profile values. In the region from 2.5 to 4.2 µm from the surface, the dopant concentration is about 5–6 × 10^{14} cm^{-3}; however, there is a strong increase in the high acceptor doping level deeper into the bulk. It appears that the epilayer is narrower than 10 µm (~5 µm), and a tiny portion of the epilayer became a semi-insulating layer after the electron irradiation and showed minimal dependency on the reverse bias voltage. From Fig. 5.8, a depletion layer with a very small thickness likely exists under the Schottky contact as a semi-insulating layer and controls the conductivity between the substrate and Au-contact layer regardless of bias voltage. Due to conductivity (doping), compensated semi-insulating region formation by the electron irradiation (electron fluence is very high) on n-type SiC, as also observed by [131]. The trap concentration exceeds the doping concentration (N_A-N_D) at the compensated semi-insulating region, and the deep center can capture almost all holes from the shallow acceptors. So, bias-independent capacitance and the thickness of an offset region (CR) can be estimated by (5.9):

$$d_{CR} = \frac{\varepsilon}{C}, \tag{5.9}$$

where d_{CR} is derived from the dependence of the compensated region thickness that leads the electron irradiation with fluence or doping concentration, Ɛ is a dielectric constant, and C signifies the capacitance per unit area obtained from the C–V measurements.

The depth profile of the defect center can be approximately calculated by the following (5.10) [131]:

$$d_{CR}(x) = N_0 + N_{surf}.\exp(-3.8\times10^4 x^2), \tag{5.10}$$

where x^2 is the distance/depth from the surface (cm), N_0 is the initial acceptor doping concentration before irradiation, and N_{surf} signifies the acceptor doping concentration in the surface after the irradiated samples – it can be measured easily by using DLTS.

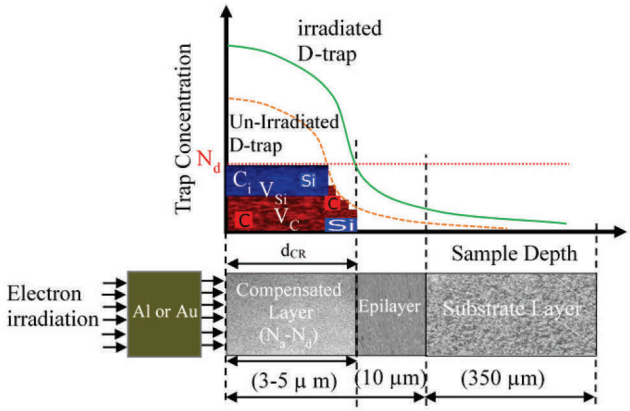
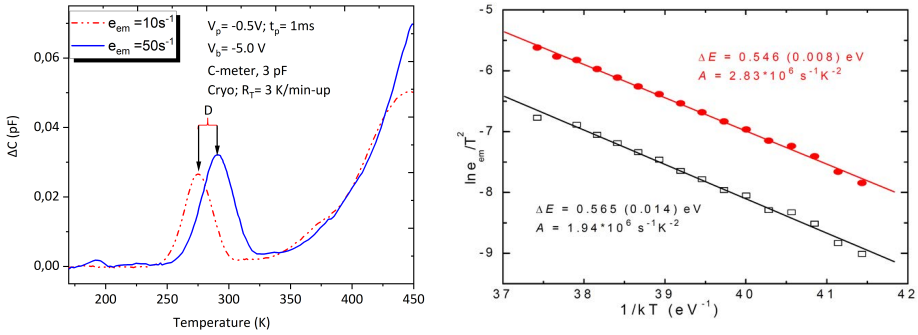


Fig. 5.9: Conceptual model of the depth profiles of the D center of the p-type 4H-SiC sample without and with high-fluence electron irradiation; modified from [131].

Fig. 5.9 shows the conceptual diagram of depth profile (N_{surf}) values of diffusion-welded Al/p-type 4H-SiC and electron-irradiated Au-sputtered/p-type 4H-SiC SBD samples obtained from C–V and DLTS measurements. A line independent of the donor concentration can be observed from estimating the C-V measurement of the N_{surf} calculated values from (5.10).



(a) (b)

Fig. 5.10: (a) Electron-irradiated conventional DLTS measurements and (b) Arrhenius plot of emission rates for the peak with its maximum at about 290 K of the Au-sputtered/p-type 4H-SiC SBD epilayer.

5.3.5. DLTS measurements

To characterize deep-level defects for irradiated SBDs DLTS was considered to utilized. Activation energies for emission and pre-exponential factors were estimated during the transient analysis. The trap concentrations were analyzed by rectifying the incomplete trap filling pulse that is close to the surface and the transition distance at the edge of the depletion region [132].

Electron-irradiated Au/p-type 4H-SiC SBD epilayer defects were determined by the DLTS measurements performed from 170 to 450 K. The transient capacitance was measured periodically for a distance developed into a Fourier series [141]. The reverse

bias voltage was kept at -5 V, and the pulse voltage applied during the DLTS measurements was 0.5 V. A period width of 1 ms was employed with an emission rate of 10 and 50 s^{-1} for all the DLTS measurements performed in this electron-irradiated Au-sputtered/p-type 4H-SiC SBD study. Fig. 5.10(a) shows a well-defined DLTS D peak with its maximum at 290 K (for electron emission, e_{em} = 50 s^{-1}). Another possible peak (HK_2) has a maximum at about 440 K (for e_{em} = 10s^{-1}) or after 450 K (for e_{em} = 50s^{-1}), but due to temperature limitations, here the latter peak will not be discussed. Fig. 5.10(b) shows temperature dependencies of the T^2-normalized hole emission rates (Arrhenius plots) for the peak, with its maximum at about 290 K on as-manufactured electron-irradiated Au-sputtered/p-type-4H-SiC SBD. The derived values of activation energies for emission and pre-exponential factors are E_V+ 0.546 eV (E_V, top of the valence band) and 2.83 × 10^6 s^{-1} K^{-2} and E_V+ 0.565 eV and 1.94 × 10^6 s^{-1} K^{-2}, respectively, for both components. The capture cross-sections for the D center were estimated to be between 1 × 10^{-13} and 1 × 10^{-14} cm^3.

Fig. 5.10(a) also shows that the D peak is a pretty broad feature at T > 340 K directly after irradiation compared with the non-irradiated sample. This broad peak is likely due to the superposition of several peaks with close activation energies. Danno and Kimoto [119] also obtained this wider peak at 265 K for low-energy electron-irradiated (116–400 KeV) p-type SiC and reported that this wider peak is due to the increase in the D center (overlapping of D and HS_2 centers). von Bardeleben *et al*. [129] investigated electron irradiation on the p-type 6H-SiC by EPR and reported that the carbon vacancy and carbon interstitials mainly participate in generating the defects at low-energy electron irradiation (116–300 KeV). However, the explanation of a wider D defect peak may be because high-energy electron irradiation generates complicated defect peaks due to both the silicon and carbon sublattices. Other possible defects may be in the high-temperature range of 500–800 K. However, the carbon interstitial may be thermally unstable due to its high mobility [134], where EP_1 and EP_2 defect spectra may be derived from carbon-interstitial-related defects. The detailed study of this problem with the above discussed/illustrated samples is beyond the framework of this work due to limited temperature scanning possibilities. The electron-irradiated activation energy (ΔE) and capture cross-section (σ) of the centers obtained by the Arrhenius plot of emission time constant are summarized in Table 5.1.

Table 5.1: Electrical properties of deep-level defects in electron-irradiated Au-sputtered/p-type 4H-SiC SBDs.

Label	ΔE (eV)	A ($s^{-1}K^{-2}$)	σ (cm^2)	Observation Temp (K)	Trap observation
D	0.546–0.565	2.83 × 10^6 to 1.94 × 10^6	1 × 10^{-13} to 1 × 10^{-14}	275–290	0.9 MeV electron irradiated

5.3.6. L-DLTS measurements

The high-resolution LDLTS with the application of a constant bias voltage and two filling pulses of different magnitudes was utilized to obtain the dependencies of electron emission rates, especially at space charge region for deep-level traps in the temperature range of 280–310 K on an irradiated sample.

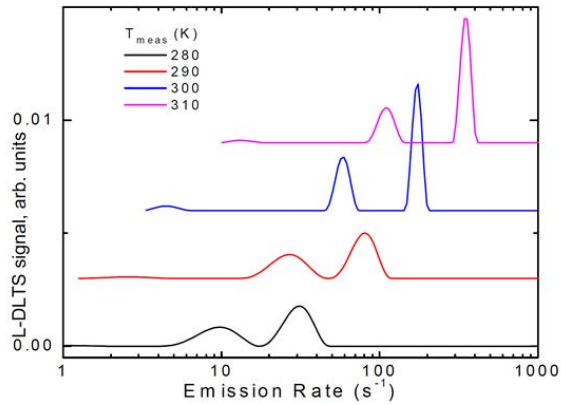


Fig. 5.11: LDLTS measurements of the electron-irradiated Au-sputtered/p-type 4H-SiC SBD epilayer.

Fig. 5.11 shows some of the recorded LDLTS spectra. The emission signal consists of two components, which shift with the measurement temperature and validate the recorded DLTS spectra of emission signals.

5.4. Comparison of samples with and without irradiation

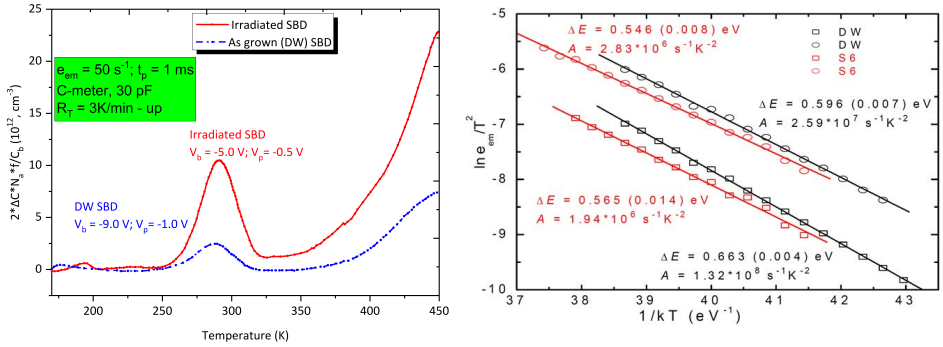


Fig 5.12: (a) Comparison of conventional DLTS measurements and (b) comparison of Arrhenius plots for electron-irradiated Au-sputtered/p-type 4H-SiC (S6) and diffusion-welded, large-area Al-foil/p-type 4H-SiC SBD sample epilayers (DW).

Deep levels in electron-irradiated Au-sputtered/p-type 4H-SiC and diffusion-welded large-area Al-foil/p-type 4H-SiC SBD sample epilayers were measured using Fourier-transform DLTS from 170 to 450 K. Conventional DLTS spectra were recorded for both samples by keeping the same rate window. It should be noted that the y-axis in the graph shows normalized values to compare concentrations of deep-level defects in those samples. A period width of 0.2 s was employed with an emission rate of 50 s^{-1} for all the DLTS measurements performed in this study. Fig. 5.12(a) shows a well-defined DLTS D peak with its maximum at 290 K (for e_{em} = 50 s^{-1}) and a broad feature at > 340 K. It appears that concentrations of deep-level defects are higher in the electron-irradiated sample.

Fig. 5.12(b) presents a comparison of the Arrhenius plots of hole emission rate measured from 270 to 310 K for the emission signals in both SBD samples. The emission rates of two components of the hole emission signal are close in both samples.

The derived values of activation energies for emission and pre-exponential factors are E_V+ 0.663 eV and E_V+ 0.596 eV (E_V, top of the valence band) and 1.32 × 10^8 s^{-1} K^{-2} and 2.59 × 10^7 s^{-1} K^{-2}, respectively, for the diffusion-welded Al-foil/p-type 4H-SiC SBD sample. On the other hand, the activation energies for emission and pre-exponential factors are E_V+ 0.565 eV and E_V+ 0.546 eV (E_V, top of the valence band) and 1.94 × 10^6 s^{-1} K^{-2} and 2.83 × 10^6 s^{-1} K^{-2}, respectively, for electron-irradiated Au-sputtered/p-type 4H-SiC SBD sample. While the derived values of the samples are slightly different, the pulse width (1 ms) and emission rate (50 s^{-1}) during the DLTS measurements are the same. It might be possible that the same defect is responsible for the observed emission signals in both samples, but for unknown reasons, the emission rates differ. However, the emission rates and the derived activation energy for emission are very close for each sample [71].

5.5. Irradiation decay study on commercial Schottky diodes

To examine irradiation-induced decay, commercial Al/n-type 4H-SiC–based Schottky diodes (CPW3-0600S002B and CPW3-1700S010) with the breakdown voltage of 600 V and 1700-Volt Schottky rectifier, from Cree Inc., were subjected to electron irradiation.

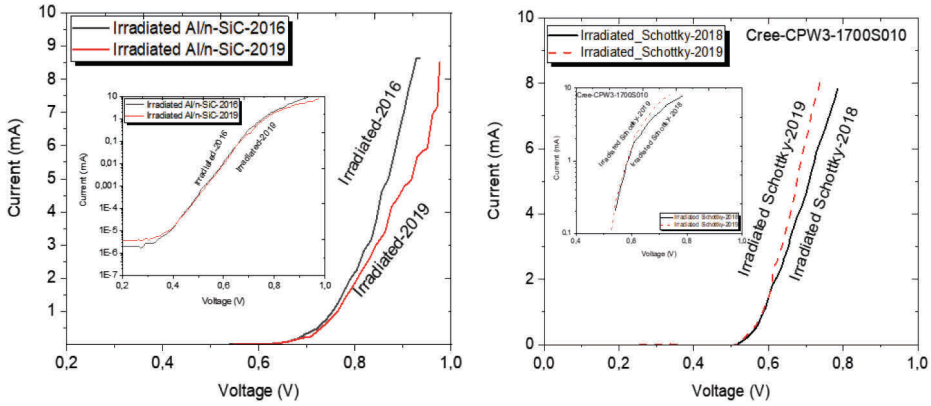


Fig. 5.13: (a) I–V measurements of the Al/n-type 4H-SiC-based Schottky diodes (CPW3-0600S002B) subjected to 0.9-MeV electron irradiation and measured immediately after irradiation in 2016 and after 3 years of storage, in 2019. The ideality factor values are n = 1.05 (2016) and n = 1.06 (2019); (b) I–V measurements of Schottky diodes (CPW3-1700S010) subjected to 0.9-MeV electron irradiation and measured immediately after irradiation in 2018 and after 1 year of storage, in 2019. The ideality factor values are n = 1.03 (2018) and n = 1.04 (2019).

Fig. 5.13 shows the irradiation decay study performed on commercial CPW3-0600S002B and CPW3-1700S010 diodes just after the 0.9 MeV electron irradiation with a dose of 1 × 10^{16} cm^{-2}. Fig. 5.13(a) shows the diode measured in 2016 and after 3 years of keeping the samples at room temperature (2019). Fig. 5.13(b) shows the decay study on the commercial JBS CPW3-1700S010 diode measured in 2018, and after 1 year of keeping the samples at room temperature (2019). Overall, the current rating decreased slightly, and the ideality factor also decreased during the time span for both diodes.

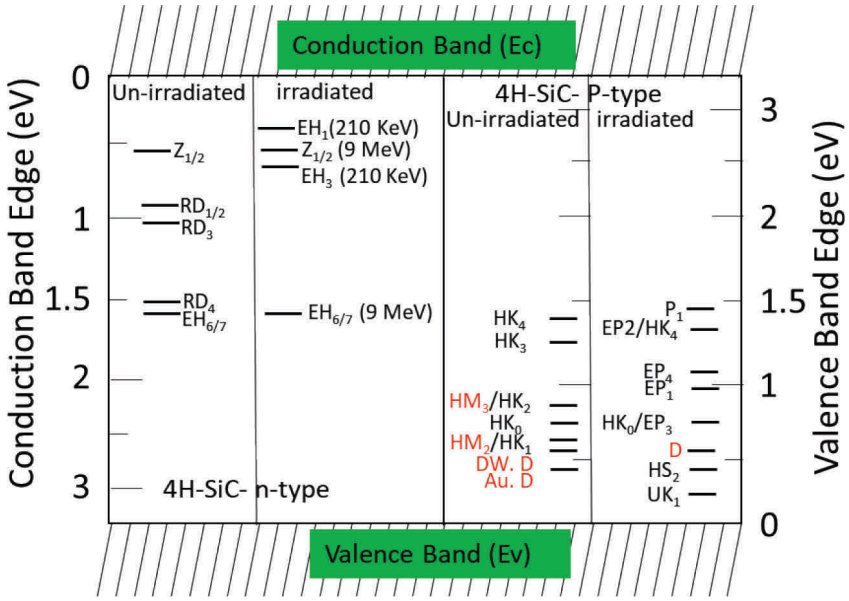


Fig. 5.14: Overview of ground states of deep levels detected in as-grown and electron-irradiated n- and p-type 4H-SiC epilayers. The data are from [70], [71], [118], [119], [129], [133], [135], [138] and this work (shown in red).

5.6. Results and discussion

Fig. 5.14 shows the significant electron and hole trap presented with levels denoted by bold lines in n- and p-type 4H-SiC. As shown in Fig 5.14, there are DLTS peaks labeled as $Z_{1/2}$, $RD_{1/2}$, RD_3, RD_4, and $EH_{6/7}$ in the n-type 4H-SiC epilayer for the as-grown sample. Other DLTS peaks EH_1 and EH_3 are observed with low-energy (210 KeV) electron irradiation in the n-type 4H-SiC epilayer. Reference [129] reported that the irradiation energy 200–400 keV is large enough to induce silicon displacement in the n-type 4H-SiC. Among them, the $Z_{1/2}$ and $EH_{6/7}$ traps are present in the as-grown devices or energy to generate these defects beginning from 100 KeV and both centers are stable even at a high electron irradiation (9 MeV) and a high annealing temperature (> 1500°C) [133]. Their concentration decreases after 1500°C in the n-type 4H-SiC samples. The $Z_{1/2}$ trap is located near the conduction band edge (~0.68 eV), and the $EH_{6/7}$ trap center occupies the midgap (~1.58 eV); both traps act as a carrier generation and recombination center [135] and are responsible for the semi-insulating property observed after electron irradiation of the n-type 4H-SiC samples. However, a very high temperature is required to detect the $EH_{6/7}$. Reference [118] discussed both $Z_{1/2}$ and $EH_{6/7}$ traps and reported that the defect complex like Vc ($V_C + \dot{\alpha}$) could not overcome the origin of $Z_{1/2}$ and $EH_{6/7}$ defects by irradiated samples if the migration energy ($\dot{\alpha}$) is lower than the thermal energy provided by the unexpected heating during irradiation. The origin of the $Z_{1/2}$ and $EH_{6/7}$ traps were also investigated in [118]; the authors suggested that both centers may be due to a carbon vacancy or carbon atom displacement and interstitials by electron irradiation. The defect spectrum $RD_{1/2}$, RD_3, and RD_4 were observed in [133] after He^+ ion implantation and annealing the sample at 430°C. Among them, $RD_{1/2}$ (~0.89–0.97, below the conduction band) and RD_3 (~0.98–1.08) are located in the upper third of the

bandgap, while RD_4 (~1.49–1.60) is positioned in the midgap in the n-type 4H-SiC. Reference [133] reported that the defect spectra of $RD_{1/2}$, RD_3, and RD_4 are detected at higher temperature and stable annealing temperatures until 1000°C (for RD_3 and RD_4) to 1400 °C (for $RD_{1/2}$). Dalibor *et al*. [133] also discussed these defects and suggested that they belong to acceptor-like and intrinsic defects in nature in the n-type 4H-SiC. The RD_3 defects are likely located at $EH_{6/7}$ centers, or they might be the same defects. The other related defects EH_1 and EH_3 are pronounced at electron energies above 210 keV and unstable at high annealing temperatures (400°C), as observed by [119]. The DLTS spectra for defects EH_1 and EH_3 are detected at 188 and 320 K. The EH_1 and EH_3 are located at the 0.41 and 0.71 eV energy states, respectively, below the conduction band edge. Storasta [119] suggested that these defects may be possible due to carbon vacancy or disbanded interstitials. The above discussion suggests that electrically active defect or defect complex centers are not particular to silicon displacement in n-type 4H-SiC above the Fermi level (upper half of mid-band gap) by electron irradiation.

As shown in Fig. 5.14, there are DLTS peaks labeled as D, HK_1, HK_0, HK_2, HK_3, and HK_4 in the p-type 4H-SiC epilayer as well as the unirradiated sample. The D defect center is located at ~0.49–0.66 eV, above the valence band in the p-type 4H-SiC irradiated and unirradiated samples. This D defect occurs at 275–290 K in the Al-doped diffusion-welded Al-foil/p-type 4H-SiC and Au-sputtered/p-type 4H-SiC as-grown sample, annealed at 400°C, and also in the electron irradiated samples at 0.9 MeV (see chapter 5.4). In Fig. 5.10, it was observed only the D defect center throughout the entire investigated temperature range (170–450 K) on the Al or Au contacts of p-type 4H-SiC SBDs. The D defect center detected at room temperature acts as an acceptor by the minority carrier concentration in the valence band. According to the conceptual model in Fig. 5.9 obtained from the C–V measurements, this D defect doping concentration decreases due to band-to-band recombination, Auger recombination, and Shockley–Read–Hall (SRH) recombination [136]. The authors of [136] investigated the boron-doped p-type epilayer by using MCTS and observed the D defect center at 290 K. The measurement shows that the D trap concentration defect is two orders of magnitude higher than the typical V_C concentration without the boron doping epilayer. The author suggested that this D defect center controls the carrier lifetimes of the p-type-based devices similarly to the $Z_{1/2}$ for the n-type devices. It is recommended that the D defect concentration control the band-to-band recombination, Auger recombination process at the higher injected hole concentration ($\geq 1 \times 10^{15}$ cm^{-3}), and should not exceed 1×10^{16} cm^{-3}. This D defect center is stable after annealing the sample at 1200°C [71]. The D defect center originates from Al-doped epilayers at low-energy electron irradiation (160 KeV) [71] or from the boron at carbon site (B_C) or boron at silicon site (B_{Si}) and carbon vacancy [137].

Other unirradiated defects are HK_1, HK_0, and Hk_2, located the 0.68, 0.79, and 0.84 eV energy states, respectively, above the valence band edge, after high temperature annealing (1200–1400°C) as well as in as-grown samples. However, HK_3 (1.27 eV) and HK_4 (1.44 eV) are present in the middle of the band above the balance band for the as-grown samples or those irradiated at 160 KeV and annealed at 950°C, as detected by the high temperature (≥ 550 K) DLTS measurements. The UK_1 and HS_2 peaks, also detected by [119], are observed at the valence band minimum produced immediately after the low-energy electron irradiation (160 or 116 KeV). The DLTS measurements detect these at a temperature < 250 K or at about 265 K. HS_2 may be considered the D

defect center because they coincide at the lattice side. Other defects in the p-type irradiated sample are discussed briefly in [71]. The most important trap in the irradiated sample is P_1 observed by Son [135] and Katsunori *et al*. [138] detected by the DLTS measurements at the temperature of about 600 K. This P_1 trap is located in the midgap above the valence band with an activation energy of 1.44–1.49 eV. At this energy level, there are other defects, namely EP_2, HK_2, and HK_3. These defects are present in the unirradiated and irradiated samples. Those are the most stable defects in the p-type 4H-SiC epilayer after high-temperature annealing (~1550°C) [71]. These traps might be located at the same position in the lattice site, or they might overlap the signal spectrum during the measurement conditions. Son *et al*. [137] detected this trap level by using photo EPR on electron-irradiated samples and suggested it as the donor (+/0) level of V_c.

5.7. Conclusion

The recorded I–V curve of the irradiated Au contact p-type 4H-SiC SBD shows reasonably good quality, with well-defined rectifying properties and acceptable leakage and forward current values. In the forward current, there is a layer with isolating properties. The recorded CV characteristics show that about 3-5 µm of the semi-insulating layer is formed due to a substantial increase in acceptor doping deeper into the bulk. Another explanation could be that the diodes on a single chip are very close to each other, and there might be a shortening of compact diodes, a phenomenon not observed by using optical microscope. Conventional DLTS spectra of both samples show a well-defined peak, namely the D defect center, with its maximum at about 290 K for e_{em} = 50 s^{-1}, and a broad emission signal in the temperature range 350–450 K occurs. LDLTS measurements have shown that the emission signal in the temperature range of 270–310 K comprises two well-separated components in both samples. Arrhenius diagrams of emission rates have been plotted, and activation energy values for emission and pre-exponential factors have been derived for both samples. The emission rates of the two components of the hole emission signal are close in both samples, but the rates and the derived activation energies and pre-exponential factors differ slightly. Perhaps the same defect is responsible for the observed emission signals in both samples; however, for reasons still unknown, the emission rates differ slightly.

6. Conclusion and future work

The main tasks of this Ph.D. work were to develop numerical models, to characterize multi-layer Schottky barrier diode (SBD) interfaces, and to try to establish an acceptable physical explanation of the behavior of metal–p-SiC 4H interfaces using diffusion Welding (DW). The first two chapters provided an introduction and reviewed the literature and background of the SiC SBD fabrication feasibility and theoretical solution of the p-type SBD. Chapter 3 discussed the development of the DW process. Chapter 4 covered the numerical model conformation, electrical and surface characterization of p-type SiC Schottky diodes. Chapter 5 discussed the electron irradiation resistance to p-type 4H-SiC SBD and understanding the radiation-induced defects and their properties in the environment. This chapter highlights the contribution of the thesis and how the research can answer the following research questions were proposed:

1. What are the forward voltage drop, reverse breakdown voltage, and most dominant current transport phenomena and how do they influence barrier inhomogeneity in diffusion-welded SBDs?
2. What are the prepared process parameters for diffusion-welded SBD manufacturing, and could DW be used rather than sputtering technology for Schottky diode development?
3. What are the energy levels of the defects and their electrical characteristics in Al-foil/4H-SiC diffusion-welded SBD and Au/4H-SiC sputtered SBDs?
4. What atoms/molecules interact more based on X-ray photoelectron spectroscopy (XPS) analysis, and how are the structural defects formed/initiated in diffusion-welded Al-foil/p-type SiC SBDs?
5. How are the defective layer/defects formed in diffusion-welded Al-foil/p-type SiC SBDs, and what are the maximum and minimum sizes of the defects in diffusion-welded SBDs?
6. How does electron irradiation influence and what are the defects created by electron irradiation in multi-contact sputtered SiC SBDs?
7. How is the carrier lifetime influenced by the irradiation decay in commercial Schottky diodes?

Finally, a summary of the claims of this Ph.D. work is presented.

Paper I

A comprehensive pre-production technological computer-aided design (TCAD) numerical simulation was performed on the SBD considering the 25-nm aluminum defects under the Al-contact layer. This preliminary forward current and reverse voltage blocking simulated characteristics in the temperature range of 300–600K to evaluate the influence of additional defects. These results are comparable with the experimental characteristics. The series resistance and tunneling behaviors are observed in the simulated forward and reverse current characteristics. The SBD device simulation shows a significant impact on the reverse current and forward voltage despite the very thin defective layers. The simulated forward I–V characteristics indicate no influence from the very thin defective layer because defects are on the highly doped epilayer. The reverse breakdown voltage results indicate the impact of defects edge leakage currents in the SBD development. The paper corresponds to research question 1.

Papers II and III

The numerical and experimental I–V-T and C–V-T characteristics have been compared in the 85–443 K temperature range; there are undesired anomalies in the I–V and C–V characteristics of SBDs. The study of measured diffusion-welded Al-foil/p-type 4H-SiC SBD shows the deviation in electrical characteristics due to excess current, dominating at low voltages (< 1 V) and temperatures (less than room temperature). Of note, thermionic emission theory is not the dominant mechanism for diffusion-welded p-type Al Schottky contacts at high temperature. An improvement in the ideality factor and increase in barrier height in fabricated Al-foil/p-type-4H-SiC SBD has been noticed as the temperature increased. The SBH and ideality factors are different when comparing within the SBDs despite their identical manufacturing process. The ideality factors are improved by annealing. At a higher temperature and higher forward voltage, the tunneling current is dominant compared with the thermionic emission current mechanism. Increases in barrier height improve ideality factors and abnormalities in their electrical characteristics are due to structural defect initiation. However, the current through the junction appears to be influenced by the carrier recombination center due to incomplete ionization at low temperature and trapping effects due to both intrinsic and doping-induced deep defects. There are also electrically active defects under the Schottky contact; these influence the SBH, barrier inhomogeneity of locally potential distribution, and tunneling current formation within the interface layers. Deep level transient spectroscopy (DLTS) measurements show the presence of a deep-level defect with an activation energy typical of multilevel trap clusters. The papers cover research questions 1 and 2.

Paper IV

Deposition temperature and pressure influence the diffusion-welded SBD electrical characteristics and influence the barrier inhomogeneity. The lower doping concentration in the epi-layer improves the Schottky contact characteristics with the same manufacturing process (MP) parameters. Temperature dependency of forward I–V, C–V, and barrier height correspond to the ideality factor measurements of DW. Two manufacturing process parameters show higher barrier inhomogeneities at the metal–SiC interface than one manufacturing process parameter for Al-foil/p-4H–SiC SBDs. These optimized process parameters significantly improve the experimentally measured electrical characteristics and reduce the inhomogeneous barrier height. The resultant device has minimized discrete energy levels, lower tunneling current, shows a better ideality factor, and has less interfacial native oxide layer formation during surface preparation. In addition, Al-foil/p-type-4H-SiC SBDs Schottky contact with DW shows better electrical contact than Au/p-type 4H-SiC SBDs ion-sputtering deposition. The paper corresponds to research question 2.

Unpublished work

The DW and sputtered p-type 4H-SiC SBD fabrication and physical characterization were studied. The numerical and experimental descriptions illustrate the reliable operation of the device. I–V and C–V characteristics were measured and presented. The investigations included deep-level transient spectroscopy in as-grown diffusion-welded Al-foil/p-type 4H-SiC and Au-sputtered /p-type 4H-SiC SBD samples. As-deposited diffusion-welded Al-foil/p-type 4H-SiC SBD shows non-ideal electrical characteristics due to the inhomogeneous SBH at the interface associated with two distinct SBHs. The investigated

deep level spectra revealed two peaks in both contacts: the D peak appears at about 275–290K for DW contact with an activation energy of 0.596–0.663 eV and a capture cross-section of 1×10^{-11} to 1×10^{-14} cm^2. There are differences in the D peak: it has a lower activation energy of 0.483 eV with a capture cross-section of 4.06×10^{-16} at 310 K in as-grown samples, and a higher activation energy of 0.66 eV with a capture cross-section 1.0×10^{-15} cm^2 at 260 K after annealing in sputtered Schottky contact. There are other peaks – HM_3 at 390–407 K and HM_2 at 360 K – with slightly higher activation energies of 0.86 eV and 0.663 eV, respectively, for the as-grown and after-annealed samples. The activation energy and capture cross-section values are different, but the DLTS spectral shape is more or less the same for both metallization techniques. Au-sputtered/p-type 4H-SiC SBD has been examined using AFM. The low forward voltage drop and low leakage current are obtained for the Au-sputtered/p-type 4H-SiC SBD before and after annealing compared with the diffusion-welded Al-foil/ p-type 4H-SiC SBD. However, at 400°C, the electrical parameters deteriorate with the annealing temperature and show distortions in the gold layer of Au-sputtered/p-type 4H-SiC SBDs. Hence, the optimum annealing temperature for the Au-sputtered/4H-SiC SBDs is slightly below 400°C. The works corresponds to research question 3.

The performance and reliability of SBDs generally depend on the interface state density, which is affected by the presence of the interfacial native oxide layer formation during surface preparation. However, the microscopic structure of most defects is poorly understood, and the appearance of their constituents depends on the growth conditions. Detailed information of defects has been observed using XPS and TEM measurements. The XPS investigation suggests that some carbon, oxygen, and unbonded silicon atoms are present after the chemical cleaning process. These atoms are present in a 120-nm interface layer and form crystalline, amorphous silicon or carbon or both V_C–C_{Si} vacancy complexes or defective layers, about 2.67 nm based on TEM investigation. The works corresponds to research questions 4 and 5.

Comparison of the deep-level transient spectroscopy in as-grown diffusion-welded Al-foil/p-type 4H-SiC and electron-irradiated multi-contact Au-sputtered/p-type 4H-SiC SBD samples has been carried out during current research. The electron-irradiated Au-sputtered/p-type 4H-SiC SBD epilayers show semi-insulating behavior at the interface between the contact and epilayer. The 3–5 µm depth compensated region is observed due to the 0.9-MeV electron irradiation. All p-type 4H-SiC samples epilayer (unirradiated Al-foil diffusion-welded SBDs, Au-sputtered contact SBD, and electron-irradiated Au-sputtered contact SBD) show the presence of D defects. Other defects, namely HM_3 and HM_2, are observed on the as-grown and as-annealed Au-sputtered SBDs samples at 390–407 K and 360 K, respectively. The D-center activation energy varies from 0.483 to 0.663 in the Au-sputtered and Al-foil contact of 4H-SiC SBDs. The capture cross-section of the centers is from 1×10^{-11} to 1×10^{-14} for the diffusion-welded Al-foil/4H-SiC SBD and 1×10^{-13} to 1×10^{-14} for the 0.9-MeV electron-irradiated Au-sputtered/4H-SiC SBD. However, the Au-sputtered contact SBDs have the highest capture cross-sections: from 1×10^{-16} (as-grown) to 1×10^{-14} (annealed at 400°C). It can be suggested that the D defect is due to the carbon vacancy and can be attributed to the formation of defects by the carbon displacement or interstitial carbon defects. It is also strange as to why different behaviors are observed in activation energy levels for identical process parameters and the same epilayer doping level. The significant increase in the ideality factor and appearance of transient non-stationary current due to irradiation can be attributed to

the formation of defects close to the Al-foil or Au-sputtered/p-type 4H-SiC interface for both types of SBDs. In addition, the 0.9-MeV electron irradiation of two commercial Al/n-type 4H-SiC Schottky diodes shows the decay of current rating and ideality factors with the time period at room temperature. The works corresponds to research questions 6 and 7.

Summary of claims

The summarized claims of the novelty of this Ph.D. thesis correspond to the contributions presented in chapter 1.4.

Claim 1: The development of p-type 4H-SiC SBD using a novel technique called DW is the main novelty of this work. The preliminary implementation of diffusion-welded SBD in the TCAD simulation to characterize various electrical characteristics has been described in detail as well as applied for practical experiments. The detailed information of the process and methodology of the DW technique are described in this Ph.D. thesis. To the author's knowledge, such an extensive summary of information has not been published previously on DW. The investigated model has been evaluated extensively using numerical and experimental approaches and has yielded novel data for p-type 4H-SiC device development. These findings correspond to Contributions I and II and [Paper I]–[Paper IV].

Claim 2: p-Type 4H-SiC SBD devices were manufactured using DW and evaluated successfully. There is sufficient forward current and acceptable reverse current in the presence of barrier inhomogeneity. At high temperatures, the tunneling current dominates even at a higher barrier height. The low-temperature junction current appears to be influenced by the carrier recombination center due to incomplete ionization. There is a deep-level defect measured with activation energy typically corresponding to multilevel trap clusters. In addition, DW process parameters (temperature and pressure) were investigated to optimize the process. Diffusion-welded Schottky contacts are prepared in a single manufacturing process to achieve better contacts. One manufacturing process notably influences the annealing process in the barrier height and diode ideality factors. These novel characteristics studied from DW p-type 4H-SiC SBD fulfill the requirements for the commercialization of the diode with a low manufacturing cost. These findings correspond to Contributions I and II and [Paper II]–[Paper IV].

Claim 3: The diffusion-welded p-type 4H-SiC SBD and novel Au-sputtered four-point contact/p-type 4H-SiC SBD fabrication and physical characterization were evaluated extensively. This comparison between the two different fabrication technologies and geometrical design (one- and four-point contacts in a single chip) has not been performed or published regarding SBD development. There are at least two deep-level defects on both Schottky diodes. The D level defect shows similar characteristics to previous studies, although the corresponding parameters are not the same. Of note, to the author's knowledge, other defects identified (HM_3 and HM_2) in the sputtered Schottky diode have not been published. This corresponds to Contribution III, and these unpublished results observed are available in chapter 4.

Claim 4: The surface properties of p-type 4H-SiC and their contamination induced by the cleaning process before DW have been evaluated. Surface analysis techniques like AFM, SEM, and XPS were utilized to investigate the surface and interface morphology of the p-type 4H-SiC before and after the chemical cleaning process. These detailed

investigations with destructive and non-destructive surface measurement techniques demonstrate the feasibility and improve the DW technology. In addition, high-resolution TEM implementation and detailed investigation revealed that a very small amorphous layer forms directly on the SiC surface after DW. The presence of nano particles influence the generation of the defects in the diffusion-welded p-type 4H-SiC SBD. These microscopic investigations and the results in this Ph.D. thesis have not been published previously. This novelty corresponds to Contributions IV and V, and these unpublished results are in chapter 4.

Claim 5: The electron irradiation investigation has been performed on the multi-point contact Au-sputtered/p-type SBDs. The sample design patterns and the electron irradiation on such p-type 4H-SiC SBD were unique. To the author's knowledge, no authors have published this kind of design of SBD and their investigated results on multipoint contacts gold-p-type SBD irradiation. This novelty corresponds to Contribution VI, and the unpublished results available in chapter 5.

Future work

It would be fascinating to perform with more high-temperature (500–700 K) DLTS and Electron paramagnetic resonance (EPR) measurements on the p-type epilayers to collect more expected results and to understand the different defect behaviors. This endeavor would pave the way to determine the cause of the unstable behavior of V_{Si} and the formation of the V_C–C_{Si} complex for p-type 4H-SiC. The above knowledge and results can be used in the development of more precise SBD, MOSFET and IGBT development. Additionally, the developed p-type SiC based Schottky diode can be used as a various radiation detector.

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Acknowledgments

I want to thank the Thomas Johann Seebeck Department of Electronics at Tallinn University of Technology for giving me the chance to pursue my Ph.D. studies. I want to express my most profound appreciation to my supervisor, Associate Professor Dr. Ants Koel, and Prof. Emeritus Dr. Toomas Rang for their invaluable guidance, advice, time, and the caring support they have given me throughout my Ph.D. research. I want to thank my second supervisor, Dr. Tamás Pardy, for his guidance and advice. I would like to thank Dr. Oleg Korolkov for his guidance, especially for hands-on training and support on diffusion welding, and Dr. Natalja Sleptsuk and Dr. Jana. Toompuu for their hands-on training on deep-level transient spectroscopy measurements. I would like to thank Prof Dr. Alexander Lebedev from St. Petersburg University for the irradiation of the diodes. I want to thank Prof. Emeritus Dr. Tony Peaker and research fellow Dr. Vladimir Markevich from the University of Manchester for discussing deep levels. Thank you to senior researcher Dr. Raul Land, especially for measurement-related issues. Many thanks to all the members of the Department of Material Science of Taltech, especially to Prof. Maarja Grossberg, for permission to work in the various microscopy labs, and Dr. Olga Volobujeva for scanning electron microscopy measurement, and hands-on training on sputtering. I want to thank Dr. Valdek Mikli for hands-on training for transmission electron microscopy sample preparation, and Dr. Jekaterina Kozlova and Prof. Dr. Aile Tamm from the University of Tartu for transmission electron microscopy measurement. Thank you to Dr. Mati Danilson for X-ray photoelectron spectroscopy measures and Dr. Kristi Timmo for help during annealing.

I am also grateful to my colleagues at Tallinn University of Technology, especially IT manager Fredrick Rang and Eva Keerov, who were always willing to solve IT- and office-related issues. Last but most important, my heartfelt thanks go to my family, especially my parents, my sisters, my brother, my wife, and my baby, Tammam Hasan. Their ongoing consideration and support have allowed me to completion of this work successfully. Finally, I thank God for guiding me. I express my gratitude to the following entities for their financial support during my Ph.D. studies:

This work has partly received funding from the European Union Horizon 2020 research and innovation program under grant agreement no. 668995 and was partially supported by the Estonian Research Council under grants PUT1435, IUT19-11, and PRG-620;

- IT Academy Scholarship at Tallinn University of Technology;
- Dora Programme and BALTECH Scholarship.

Abstract

Characterization of interfaces between the metal film and silicon carbide semiconductor

The Schottky barrier diode (SBD) has become an essential constituent of most contemporary electronic circuits. These devices are well suited for high-frequency and fast-switching digital electronic applications and circuit protection against accidental or inductive reverse voltage. In addition to extensive use as low forward voltage drop power electronic devices, Schottky diodes use sensors and light-emitting diodes. Attractive properties and a wide range of applications of silicon carbide (SiC) SBDs compared with Si-based SBDs have drawn the interest of researchers in this field. In the last few decades, SBD based on SiC polytypes have come to prominence due to their promising physical and electrical properties. The commercialization of SBD using 4H-SiC has been favored due to the high mobility and availability of the materials.

In this research, a niche technology used in the semiconductor industry, called diffusion welding (DW), has been investigated to manufacture SiC-based SBD devices with aluminum contacts. State-of-the-art SiC material, its various structures, metal–semiconductor theory, and point defects have been studied. A brief outline of the DW fabrication process and its mechanisms to optimize process conditions for reliable Al-foil/p-type 4H-SiC SBD are presented. Numerical simulations have been used to calculate their electrical characteristics. These results are compared with the measured electrical characteristics of fabricated, diffusion-welded devices.

There is also a need to investigate the surface and contact properties of the MS interface to understand the nature of introduced defects and their influence on the electrical characteristics. Traditional electrical and microscopic methods are used – Keithley measurement source and unit, deep-level transient spectroscopy (DLTS), Laplace deep-level transient spectroscopy (DLTS), atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS), scanning electron microscopy (SEM), and transmission electron microscopy (TEM) – to understand the presence of defects in the resultant SBDs. These studies show that the tunneling mechanism dominates at high temperatures in the diffusion-welded SBDs. Moreover, marked improvement of electrical characteristics reduced the inhomogeneous barrier height by minimizing the discrete energy levels. XPS analysis shows that the sample with chemical treatment was less contaminated compared with the sample without chemical treatment. TEM investigation of diffusion-welded Al-foil/4H-SiC SBD revealed an intermediate layer of ~2.67 nm and some amorphous layer formed directly on the SiC surface after DW.

The electrical and annealing temperature of the optimized Au-sputtered/4H-SiC SBDs have been studied. A maximum annealing temperature of 400°C is obtained for the Au-sputtered SBDs. In addition, this optimized multi-point design has been used for radiation hardening application. The electron irradiation study showed that about 5 μm of the semi-insulating layer is formed due to a high acceptor doping. Furthermore, conventional DLTS spectra of Al-foil and Au-sputtered SBD devices showed the appearance of a well-defined peak, namely the D defect center with its maximum at about 290 K for electron emission, e_{em}= 50 s^{-1}. LDLTS measurements revealed that in both samples, the emission signal from 270 to 310 K consists of two well-separated components. Arrhenius diagrams of emission rates have been plotted, and activation

energies for emission and pre-exponential factors have been derived for both samples. The optimal design, fabrication process, and various characterizations are discussed in this work to help the design or process engineer to better understand the reliable and high-performance SBDs for use in a high-power, high-temperature, and high-radiation environment.

Lühikokkuvõte

Metallkontakti ja ränikarbiidi vahelise liidespinna karakteriseerimine

Schottky dioodist (SBD) on saanud enamiku kaasaegsete elektroonikaskeemide oluline koostisosa. Need seadised sobivad hästi rakendamiseks kõrgsageduslikes- ja kiiret ümberlülitumist nõudvates elektroonilistes skeemides ning vooluahelakaitseks juhusliku- või induktiivse vastupinge eest. Lisaks laialdasele kasutamisele madala päripinge pingelanguga seadistena on Schottky dioodid kasutavad andurite- ja valgusdioodena. Ränikarbiidil (SiC) põhineva SBD atraktiivsed omadused ja lai valik rakendusi võrreldes ränil (Si) põhineva SBD-ga, annavad motivatsiooni valdkonnapõhiseks intensiivseks uurimis- ja arendustööks. Viimastel aastakümnetel on pälvinud tähelepanu SiC polütüüpidel põhinev Schottky diood oma väljapaistvate füüsikaliste ja elektriliste omaduste tõttu. SBD turuosa laieneb peamiselt 4H-SiC-l põhinevatel seadistel, seda materjali tehnoloogilise parema käideldavuse ja kättesaadavuse tõttu.

Käesolevas diplomitöös on uuritud pooljuhitööstuses kasutatavat nišitehnoloogiat, mida nimetatakse difusioonkeevitamiseks (DW), ja viidatud tehnoloogia rakendust alumiiniumkontaktidega SiC-põhiste Schottky dioodide (SBD) tootmiseks. Uuritakse SiC kui pooljuhtmaterjali, SiC erinevaid struktuure, metalli-pooljuhtide kontakti teooriat ja punktdefekte. Esitatakse lühike ülevaade DW protsessist ja selle mehhanismidest optimaalsete protsessitingimuste realiseerimiseks töökindlate Al-foolium / p-tüüpi 4H-SiC SBD tootmiseks. SBD elektriliste omaduste karakteriseerimiseks kasutatakse numbrilisi simulatsioone. Tulemusi võrreldakse eksperimentaalselt valmistatud (difusioonkeevitatud) seadiste mõõdetud elektriliste omadustega.

Töös on uuritud metalli ja pooljuhi liideskihi pinna- ja kontaktomadusi, et mõista leitud defektide olemust ja nende mõju elektrilistele omadustele. Saadud SBD-de mitmesuguste võimalike defektide kaardistamiseks ja tõlgendamiseks kasutatakse erinevaid traditsioonilisi elektrilisi- ja mikroskoopiameetodeid (Keithley multimeetrid, DLTS, Laplace DLTS ja AFM, XPS, SEM, STM mõõtmised). Teostatud uuringud näitavad, et tunnelleerumise mehhanism domineerib kõrgetel temperatuuridel DW SBD-des. Alumiiniumfoolium (Al-foolium) / 4H-SiC SBD puhul on tuvastatud vahekiht (2,67 nm) ja pärast difusioonkeevitamist moodustatus SiC pinnale vahelduva paksusega amorfne kiht.

Lisaks on töös uuritud optimeeritud konstruktsiooniga kuldkontaktiga 4H-SiC SBD elektriliste omaduste seost lõõmutamistemperatuuriga. Sadestatud kullaga (Au) SBD-de jaoks saadakse lõõmutamistemperatuuriks, mis parendab seadise omadusi, maksimaalselt 400°C. Eelviidatud optimeeritud mitmeetapilist protsessi kasutatakse Au-kontaktidega SBD-sid kiirgusresistentsuse tõstmiseks.

Elektronidega kiiritamise eksperiment näitab umbes 5 µm poolisoleeriva kihi moodustumist aktseptorlisandi kõrge kontsentratysiooni tõttu. Lisaks on tuvastatav Al-foolium- ja Au / kontakt-SBD-seadistel DLTS-spektris hästituntud piik, mis vastab D-defektide tsentrile maksimumiga temperatuuril 290K, elektronide emissioonil e_{em} = 50 s^{-1}. Laplace DLTS mõõtmised näitavad, et emissioonisignaal temperatuurivahemikus 270–310 K koosneb mõlema metalli puhul kahest hästi eraldatud komponendist. Koostatud on emissiooni Arrheniuse diagrammid ja mõlema

SBD tüübi jaoks on tuletatud emissiooni- ja eksponentsiaaltegurite aktiveerimisenergia väärtused. Neid optimiseeritud disaini- ja tootmise protsesse ja saadud seadiste karakteriseerimist käsitletakse käesolevas töös, et aidata disaineril või protsessiinseneril paremini mõista kõrge käideldavuse- ja suure töövõimsusega SBD-de tootmise võimalusi kõrge temperatuuri ja kõrge kiirgustasemega keskkondade jaoks.

Appendix

Publication I

Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas (2018). Numerical Simulation of p-type Al/4H-SiC Schottky barrier diodes. Proceedings of Baltic Electronics Conference BEC2018: 16th Biennial Baltic Electronics Conference BEC2018, Tallinn, Estonia, Oct. 8–10, 2018. Ed. Ants Koel, Peeter Ellervee. IEEE Catalog Number: CFP18BEC-USB doi: 10.1109/BEC.2018.8600976.

Numerical Simulation of P-Type Al/4H-SiC Schottky Barrier diodes

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***Abstract*—Wide-bandgap (WBG) power semiconductor devices have good potential to replace Silicon-based devices for operating at higher temperatures. Silicon carbide (SiC) currently represents an established WBG candidate for developing power Schottky barrier diodes (SBD) used in power electronics that are required for the next generation power devices. Very few information is available about P-type 4H-SiC substrate being used for realization of SBD. Pre-production Technological computer aided design (TCAD) simulation of SBD, where p-doped epitaxial layer on p-type 4H-SiC substrate corresponds to experimental structures (currently in manufacturing process) could generate defects under the contact. P-type SiC SBD with some defects types is also examined for evaluating the influence on the forward current and reverse voltage blocking. Forward and reverse bias static characteristics are obtained for p-type 4H-SiC SBD at temperatures in the range of 300K to 600K. The currents are shown to have a large on resistance and tunneling component depending on the defects. The SBD device simulation shows that there is significant impact on the reverse current and voltage despite of the very thin defective layer. The reverse breakdown voltages of the diodes were found to decrease from several hundred volts to -100 V indicating the presence of defects edge leakage currents. The structural properties and characteristics of the resulting defects in the schottky contact layer are discussed.**

Keywords—Silicon Carbide; Schottky Barrier diode; Defects; Al contact

I. Introduction

Silicon carbide (SiC) has been recently getting attention as a material with high potential and found its way to mainstream for imminent generation of high-power and high frequency applications. SiC represents an excellent candidate for high-temperature electronic device applications because of its high breakdown voltage, low series resistance, stability under high temperature conditions. These promising properties of SiC can be used for the fabrication of high quality power devices depending to a large extent on the quality of the metal–SiC contact.

Schottky barrier diodes are most often manufactured based on 4H-SiC, which is more preferable to power semiconductors electronics due to the high mobility of electrons in this silicon carbide polytype [1]. Processing properties, such as the availability of a substrate, ability to form stable contact metallization, purity of growth samples, and the ability to dope the materials are also major considerations when choosing a material. On the contrary, p-type of 4H-SiC has been chosen for the current SBD's study. Unique characteristics of p-type Schottky diodes indicates that the p-type SBD could have advantages over the n-type SiC Schottky diodes at very high current densities during self-heating comes important and high temperatures [2]. In the p-type 4H-SiC SBD, higher temperatures can be reached before the doped material becomes intrinsic. This is due to in p-type 4H-SiC the electrons being excited from the valence band to the conduction band exceeds by far the number of electrons donated from the impurities.

Metal/semiconductor contact plays an important role in electrical performance of all electronic devices. Therefore it is necessary to investigate the defects in the contact region under various conditions to understand their properties. Although several publications on the p-type SiC SBD using various metal contacts are carried out during the last two decades [3- 7], the current transport and the temperature dependence of the barrier height in 4H-SiC SBD and the effects caused by the defects remain a topic of continuous interest.

In the current work, the SBDs are simulated on p-type 4H-SiC substrate with p-type epitaxial layer. Silvaco TCAD is used to investigate the influence of defects on the statistical electrical characteristics. Numerical analysis is carried out to compare the performance of power SBD and the IV curves of ideal diode (without defects) and ones with the aluminium (Al) or insulator defects are discussed. This paper will discuss the possible defects and their detrimental properties. Before SiC Schottky contact devices can be reliably manufactured using direct bonding technology, more research on the degradation mechanisms and the properties of the technology induced defective region directly under Schottky contact. These numerical simulations, Schottky barrier heights, doping profiles, trap activation energies, current mechanisms, and breakdown voltages of SBD were determined.

II. Material and Specimen

Imperfections in crystal structure arise mainly due to the structural defects, impurities, and vacancies, which determine the semiconductor properties and device performance [20, 21, 22]. The SBD's are simulated on p-type 4H-SiC substrate with defects, therefore it is very important to understand the theoretical concepts behind the formation of Schottky contact. Schottky contact formation and energy band diagram are shown in the Fig. 1. A metal-semiconductor contact is called Schottky contact when it has a rectifying effect providing current conduction at forward bias (metal to semiconductor) and reveal a low saturation current at reverse bias (semiconductor to metal) [13, 15]. Fig. 1(b) shows the Schottky metal-semiconductor contact after thermal equilibrium. In both cases, it can be observed that the fermi levels are aligned between the metal and

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semiconductor. At the interface itself, the vacuum level is same for the two sides such that there is a barrier due to the difference between metal work function Φ_m and electron affinity χ. These difference, the ideal barrier of the junction, Φ_B, is given by the following (1).

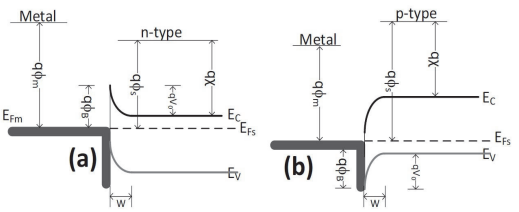

Figure. 1: Energy band diagram of metal-semiconductor Schottky contact; (a) Metal and n-type semiconductor; (b) Metal and p-type semiconductor.

$$q\Phi_B = q(\Phi_m - \chi) \tag{1}$$

The rectifying effect of the Schottky contact is caused by the formation of this barrier height ($q\Phi_B$) at the junction. So it is important to note that the condition to form a Schottky barrier for n-type semiconductor is metal work function Φ_m > semiconductor work function Φ_s and for p-type semiconductor is metal work function Φ_m < semiconductor work function Φ_s.

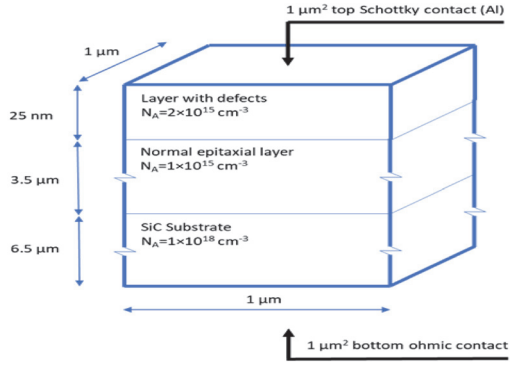

Figure. 2: Schematic of Schottky barrier diode structure simulated using ATLA

A. *Physical Models for the Simulations*

The simulation of SBD were carried out using a two-dimensional simulator, Silvaco ATLAS [8]. To obtain realistic results, one must use appropriate models and parameters values in ATLAS where compare with the loffe institute semiconductor data base values [9]. Previous investigations have shown the presence of carbon, aluminum and space (insulator) defects under Al Schottky contact [6] . These defects are partly discussed in [19 -20]. Al defects deep in substrate are donor-like hole traps, causing the recombination rate to decrease, so that, as a majority carrier device, the conduction current density in a 4H-SiC SBD increases [10]. For simulation model of current-voltage characteristics has been solved electrostatic poisson's equation together with continuity equations for electrons and holes. Because of this for calculation of current-voltage characteristics in SBD was applied of the thermionic emission theory which taken into account of the electron-phonon interaction, quantum-mechanical tunneling through barrier and reduction of barrier height under influence of image force effect [10].

B. *Device Structure and Defect Parameters*

The SBD's structure with substrate doping concentration of $1xe^{18}$ cm^{-3} were used for all ATLAS simulations. The doping concentration of epi-layer is $1xe^{15}$ cm^{-3} and epi-layer under schottky contact is $2.0xe^{15}$ cm^{-3} respectively for SBD device is schematically shown in Fig 2.

TABLE I. Simulated SBD structures parameters

Device SBD	Area	Substrate Thickness	Epi-layer	Defective area Thickness
Without defects	1 µm²	6.5 µm	3.5 µm	25nm
With Al defects	1 µm²	6.5 µm	3.5 µm	25nm
With Insulator defects	1 µm²	6.5 µm	3.5 µm	25nm

In these SBD devices, p-type epitaxial layer on p-type (6.5 µm) substrates was used for this study. The thickness of the epitaxial layer was 3.5 µm prior to the high doped thinn (25nm) defective metal film. For these SiC-based SBD, some device simulations include defects, are introduced by p-doped Al implantation along with the thin Al metal layer. The parameters associated with each of these defects are listed in Table I.

III. STATIC I-V CHARACTERISTICS

Semiconductor devices; such as SBD performances can be evaluated through current voltage (I-V) characteristics. The performance level and degradation are highly dependent upon the material, the operating current flowing through the device and series resistances. Static forward and reverse-bias current voltage (I-V) characteristics for the p-type SiC Schottky barrier diodes are investigated to verify that the devices. Simulate the I-V characteristics for Al/4H-SiC Schottky barrier diodes in the static mode of operation in the temperature range of 300K to 600K are discussed in this section. The forward characteristics of the diode shows exponential behavior over a voltage range at most temperatures is shown in the Fig.3. The reverse I-V characteristics for the SBD yielded values of reverse current density is shown in the Fig. 4. The forward current observed in the Fig. 3 dramatically increase with temperature . On the other hand, Fig. 4 shows typical reverse I-V characteristics, which shows increase in reverse-leakage current with increasing temperature. In most cases, the general behavior of the forward and reverse I-V characteristics for the SiC SBD was consistent with tunneling, diffusion, recombine and dominated by thermionic emission [15, 16, 17].

A. *Forward characteristics*

A Forward and reverse current-voltage test at various temperatures allow qualitative analysis of current voltage characteristics to determine the effects of the different current transport processes in the SBD devices. From the Fig. 3 is shows that thermionic diffusion currents are predominant, but there are also tunneling currents present. In electron, thermionic emission over the top of the barrier (holes for p-type material) in which electrons with energies greater than the barrier height can pass across the junction. Quantum mechanical tunneling, which is important for heavily doped semiconductors where the depletion width is

small. Besides this, edge leakage current may flow at the contact periphery due to high electric field. There may also be current flow due to traps at the metal-semiconductor interface. The inverse process happens under the reverse bias.

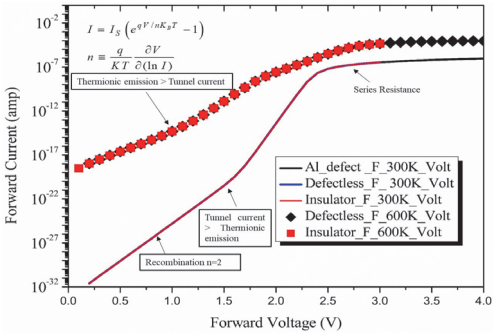

Figure. 3: Current-voltage curve of P-type Al/4H-SiC SBD illustrating the effect of tunneling and showing decrease in bulge in current at higher temperatures

The series resistance also played important rule to a large part in the behavior of current-voltage forward characteristics of p-type Al/4H-SiC SBD. This can be seen in the rounding off the linear slope at high voltages caused by the current limiting behavior of the resistance. In Fig. 3, the Al/4H-SiC SBD have high series resistance shown at various temperatures. This high series resistance causes greater bending at high temperatures because the number of carriers in the conduction band is greater, and thus currents are greater. Since series resistance affects higher currents more than lower currents, the resistance affects the curves at lower voltages for the higher temperatures. In Fig. 3, our simulation result shows that the presence of defect, there are no differences observed between forward IV calculations with and without defects (25 nm insulating layer under the Schottky electrode and aluminum inclusion under Schottky electrode)

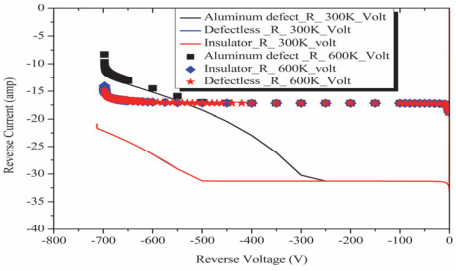

Figure. 4: Reverse I-V characteristics obtained for 4H-SiC epitaxial Schottky barrier diodes in log scale.

B. *Reverse characteristics*

For most practical SBD devices, edge leakage currents are the major current components. However, for wide band-gap semiconductors, the reverse current contains a substantial generation component as well, because of the small majority carrier concentration. The simulated reverse current-voltage plot is shown in Fig. 4. From the reverse current in Fig. 4, it shows that the devices can able to operate up to -700 V reverse bias at various temperature with and without defects.

The reverse current increase for higher temperatures and voltages due to increased recombination currents and Schottky barrier lowering represented in the Fig. 5. The Al/4H-SiC SBD simulation performed very well, passing only few micro amps of current at -700V with various temperature shown in the Fig. 4. From the electric field around the defects shown in the Fig. 6; it proves that due to the sharp cornerd the impact ionization starts earlier than in other cases. Current is increased in the Al defects due to impect ionozation.

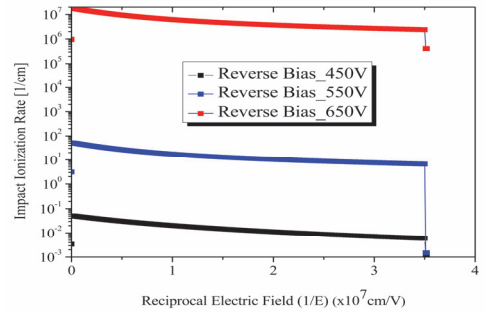

Figure. 5: Simulated Impact Ionization of SBD

For the Al defect SBD, the impect ionization start earlier where electric field is high. The carrier generation depends on the electric field extraction which is observed in the Fig. 5.

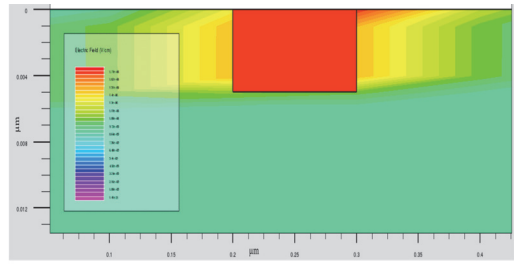

Figure. 6: Aluminum defect at reverse 300V bias, electric field around the defect.

The higher reverse current at higher temperature is expected due to the p-type dopant incomplete ionization at lower temperatures. The reverse current increase for structures at 300K, starting from 500V. This is due to the beginning of impact ionization generated carriers. The different behaviour for the structure at 300K with aluminum defect is due to the electric field concentration at the defect sharp corners, which is proved by the Fig. 6, which causes preliminary start of the impact ionization process. Reverse current decrease for 300K for the with and without defects due to impact ionization.

IV. Results and Discussions

After simulation of forward current-voltage tests revealed many interesting aspects and behaved very well exhibiting linear I-V characteristics as described by thermionic emission theory and also exhibited large tunneling components which distorted the linear behavior by bulging the curves. However, Schottky barrier diodes had a very linear portion, showing dominance by thermionic

emission currents. However, diodes that had large tunneling current components exhibited a bulge in the curve.

Fig. 3 and 4 show the current-voltage curves at different temperatures for the well-behaved Al/4H-SiC SBD with various defects and without defects were found to perform well even at 600 K. The I-V curves for the Al/4H-SiC Schottky diode with the larger tunneling component is shown in Fig. 3. It is notable that as the temperature increase, the bulge in the current slope due to tunneling decreases. Theory predicts that at higher temperatures the thermal emission of electrons over the barrier increases to the point that it dominates the tunneling currents that stay relatively constant versus temperature [16, 17, 19].

This study indicates that tunneling is a dominant process at low temperatures. On the other hand, the increase in the ideality factor to nearly three as the temperature increases are attributed to the effects of the series resistance on the current curve [22, 13, 16]. This occurs because the temperature acts as a forward bias and shifts the current to encounter series resistance at less voltage. Therefore, the Al/4H-SiC samples follow theory, even though the ideality factor increases at higher temperatures, because the series resistance effect nullifies the theoretical basis to the ideality factors [13-18]. Thus, the 4H-SiC samples had a larger tunneling component, probably caused by reactions between the metal and the carbon face of the crystal. Therefore, the higher series resistance values for the Al/4H-SiC devices come about at higher temperatures, indicating increased chemical activity with the carbon faced contact and a larger bulk resistance with higher temperature.

V. Conclusion

A comprehensive numerical study to characterize of p-type 4H-SiC SBD has been performed. The numerical simulation techniques to characterize current voltage and impact ionization studies to know electrical behavior of the devices to detect defects influence on SBD. The forward voltage drops for p-type 4H-SiC at elevated temperatures are sufficiently low for power electronic applications. It is expected that these defects will reduce the leakage current. Therefore, it is suggested that Schottky contacts made of a very thin layer of defects on the highly doped epil-ayers does not influence the IV characteristics of the SBD.

Acknowledgment

The author would like to acknowledge Mr. Kamaldeen and Marek for their support during numerical simulation. This research was supported by the Estonian Research Council through the Institutional Research Projects IUT19-11 and PUT1435, and by the Horizon 2020 ERA-chair Grant “Cognitive Electronics COEL“ —H2020-WIDESPREAD-2014-2 (Agreement 668995; TTU VFP15051).

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Publication II

Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas; Toompuu, Jana (2020). Analysis of barrier inhomogeneities of P-type Al/4H-SiC Schottky barrier diodes. Materials Science Forum, 1004, 960−972.

Analysis of barrier inhomogeneities of p-type Al/4H-SiC Schottky barrier diodes

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Keywords: 4H-SiC; Diffusion welding; SBD; TCAD; inhomogeneity; DLTS.

Abstract. The diffusion welding (DW), known as the direct bonding technique could be more used as an alternative approach to developing silicon carbide (SiC) Schottky rectifiers to existing mainstream metallization contact technologies. Measured results for *p*-type 4H-SiC Schottky barrier diodes (SBD) are presented. And comprehensive numerical study to characterize the device has been performed. The simulations are carried out with ATLAS software (Silvaco). The measured and numerically simulated forward current-voltage (*I-V*) and capacitance-voltage (*C-V*) characteristics in a large temperature range are analyzed. Some of the measured *p*-type 4H-SiC Schottky diodes show deviation in specific ranges of their electrical characteristics. This deviation, especially due to excess current, dominates at low voltages (less than 1 V) and temperatures (less than room temperature). To verify the existence of electrically active defects under the Schottky contact, which influences the Schottky barrier height (SBH) and its inhomogeneity, the deep level transient spectroscopy (DLTS) technology was applied. DLTS measurements show the presence of a deep-level defect with activation energy corresponding typically for multilevel trap clusters.

Introduction

Silicon carbide (SiC) is a well-known wide bandgap semiconductor material. SiC represents an excellent candidate for high-temperature electronic device applications due to its extraordinary properties such as high physical and chemical stability, high breakdown voltage, and low series resistance, stability under high-temperature conditions, high electron velocity, high thermal conductivity and small dielectric constant [1, 2]. Because of these properties, the most attractive applications of SiC-based devices can be used as the most attractive application area of high power, high frequency, high radiation, and high-temperature circumstances [3, 4]. Many researchers [5, 6, 7] have investigated temperature dependency for *n*-type 4H-SiC based devices to commercialize expected applications. However, promising properties of *p*-type SiC, which can be used for the fabrication of highly efficient power devices depending on the quality of the SiC layers and metal–SiC contacts, and have not accomplished yet their in full potential today.

The *n*-type 4H-SiC power Schottky barrier diodes are already present on the market for applications in the medium power range (300-1200 V, 1-20 A) where low or close to zero switching losses are required [8, 9]. Thermally stable Schottky contacts is a requirement for better performance SiC-based SBD devices [10, 11]. In particular, research work, the DW technology is used for the fabrication of SiC-based SBD devices. The DW technique is quite different from the conventional methods of metallization, and therefore to *p*-type SiC have a special interest [12, 13]. However, interface states with high densities are likely to be formed in the DW process since dangling bonds are unveiled on sample surfaces due to the annealed Al atom during the process. It was pointed out that such interface states (caused by pinning of fermi-level) modify potential barriers at the interface of SBDs. To date, the Schottky barrier height (SBH) investigations have been devoted by many researchers [14, 15] to model and explain the performance and reliability of SBDs on *p*-type 4H-SiC. It is well known that SBH controls the charge carrier's transport across the metal-semiconductor (MS)

Publication III

Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas; Rashid, Muhammad Haroon (2020). Investigation of barrier inhomogeneities and electronic transport on Al-Foil/p-Type-4H-SiC Schottky barrier diodes using diffusion welding. Crystals, 10, 636−647. doi: 10.3390/cryst10080636.

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Investigation of Barrier Inhomogeneities and Electronic Transport on Al-Foil/*p*-Type-4H-SiC Schottky Barrier Diodes Using Diffusion Welding

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Received: 30 May 2020; Accepted: 20 July 2020; Published: 23 July 2020

Abstract: The diffusion welding (DW) is a comprehensive mechanism that can be extensively used to develop silicon carbide (SiC) Schottky rectifiers as a cheaper alternative to existing mainstream contact forming technologies. In this work, the Schottky barrier diode (SBD) fabricated by depositing Al-Foil on the *p*-type 4H-SiC substrate with a novel technology; DW. The electrical properties of physically fabricated Al-Foil/4H-SiC SBD have been investigated. The current-voltage (I-V) and capacitance-voltage (C-V) characteristics based on the thermionic emission model in the temperature range (300 K–450 K) are investigated. It has been found that the ideality factor and barrier heights of identically manufactured Al-Foil/*p*-type-4H-SiC SBDs showing distinct deviation in their electrical characteristics. An improvement in the ideality factor of Al-Foil/*p*-type-4H-SiC SBD has been noticed with an increase in temperature. An increase in barrier height in fabricated SBD is also observed with an increase in temperature. We also found that these increases in barrier height, improve ideality factors and abnormalities in their electrical characteristics are due to structural defects initiation, discrete energy level formation, interfacial native oxide layer formation, inhomogenous doping profile distribution and tunneling current formation at the SiC sufaces.

Keywords: *p*-type 4H-SiC; diffusion welding; inhomogeneity; Schottky barrier diode; barrier height; ideality factor

1. Introduction

During the last few decades, SiC (a wide bandgap semiconductor material) has gained significant importance in a wide range of power electronics applications. SiC exists in many different crystalline forms, which are called polytypes. Among these polytypes, 4H-SiC, 6H-SiC and 3C-SiC are attractive for the development of power electronics devices thanks to their distinct physical and electrical attributes. Meanwhile, 4H-SiC is a potential candidate for high-power device applications due to its low-loss, low series resistance, stability at high-temperature, high electron velocity and its extraordinary high thermal conductivity and high physical and chemical stability, high breakdown voltage properties [1–4]. As a result of these properties, 4H-SiC-based power Schottky barrier diodes and modules are already commercially available. Temperature dependency for n-type SiC-based devices has been investigated by many researchers [5–7] to commercialize the expected applications. However, the prevalence of SiC has not yet been comprehensively exploited in different polytypes. In particular, the promising properties of *p*-type 4H-SiC have not yet been accomplished to their full potential for use in the fabrication of highly efficient power devices depending on the quality of the SiC layers and metal–SiC contacts. The contact formation process for soldering and attaching dies, (e.g., micro or nanoparticle pastes or solders) and their thermal stability as Schottky contacts have

been studied to realize their operational requirements and to improve the performance of SiC-based devices [8–11]. Direct bonding (DB) technology has significant attention in the development of power electronics and micro electromechanical systems [12]. This DB technology have been used in the metal-film and substrate of the same material or metal-film and substrate of different materials without concern of the crystalline relationship between them. The main concern in DB technology is smoothness of the surfaces without metallic contamination and suitability of bonding surface orientation to achieve defect-free stronger bonding and structures [13]. However, DW (high temperature DB technique) is a solid-state material joining process that can be utilized to bond various contact materials with the high performance semiconductor substrate. The DW technology can help to improve the quality of contacts. It also introduces a technological approach for the realization of the contacts with a thickness over a millimeter (mm). Thick Aluminum (Al) Foil on *p*-type 4H-SiC forms a contact using DW, which improves the the ability to handle large electric power and also increases the semiconductor device's current rating [14,15]. Additionally, interface states with high densities are likely to be formed in the DW process. These interface states (caused by pinning of fermi-level) modify the potential barriers at the interface of the diodes [16]. To date, Schottky barrier height (SBH) investigations have been done by many researchers [17,18] to improve the performance and reliable SBDs on *p*-type 4H-SiC.

In this paper, *p*-type-4H-SiC SBDs with Al-Foil as a metal contact have been fabricated for the very first time with a novel technique: DW. A schematic of fabricated diode structures, doping concentration and physically fabricated DW SBD is shown in Figure 1a,b. An attempt has been made here, to deal with distinct aspects of temperature dependent current-voltage (*I-V*) and capacitance-voltage (*C-V*), barrier height formation at the metal contact and SiC interface, ideality factor, doping concentration, current transport mechanism, and activation energy plot analysis for Al-Foil/*p*-type 4H-SiC SBD. The main goal of this work is to explain the inhomogeneity barrier height formations, current transport phenomena, and to observe their influence in identically manufactured (with the same vacuum pressure, contact force and annealing temperature) Al-Foil/*p*-type 4H-SiC SBDs using experimental *I-V-T* and *C-V-T* characteristics.

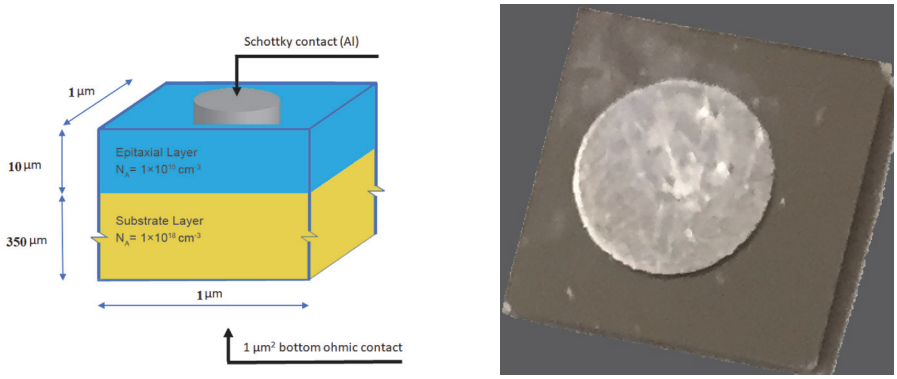

Figure 1. Illustration of the structure of a Schottky barrier diode. (**a**) Schematic of the fabricated device structures and doping concentration of Schottky barrier diodes. (**b**) Physically fabricated diffusion welded Schottky barrier diode.

2. Sample Preparation and Experimental Procedure

This section contains the experimental details and procedures that have been adopted to develop *p*-type 4H-SiC SBD.

2.1. Sample Preparation Procedure

The SiC wafers that were used for this SBD study were purchased from Cree, Inc., (Durham, NC, USA). These SiC wafers were *p*-type Al doped with a diameter of 76 mm. The average resistivity of 4.85 Ω-cm, 350 μm thick wafers were Al doped substrate to a concentration of 1×10^{18} cm^{-3}, followed by 10 μm thick *p*-type epitaxial layers doped to a concentration of 1×10^{15} cm^{-3}. Si-face 4H–SiC (0001) 4° off-axis surface orientation has been polished by the chemical mechanical method on the bonding face of the wafer (i.e., the side to which diffusion bond will be made). All of the wafers were diced into 10×10 mm^2 samples.

In the next step, surface preparation and cleaning has been done in three sequential steps. First, each sample was cleaned with a dredge in methanol for 5 min. Then, the sample was dipped in a solution of (48%) diluted HF, consisting of H_2O:HF (25:1) for 5 min to remove any native oxide (SiO_2) on the front and backside of the surface epi-layer and substrate layer, respectively. In the next step, the samples were dredged by rinsing in normal water for 5 min. Finally, each sample was cleaned in deionized (DI) water, at room temperature for 5 min.

Furthermore, the DW process has been used to deposit the Al-Foil as a metal contact with a diffusion pumped chamber at a base pressure of not less than 1×10^{-4} mbar. The Al-Foil and SiC surface were brought into contact with each other under a pressure of 750 N force (for 5 min) at 575 °C temperature for 15 min. Finally, at the same time, 100 μm thick of Al-Foil was welded as an ohmic contact on the entire surface backside of the SiC substrates and 60 μm thick of Al-Foil was welded as a Schottky contact on the center of the SiC epitaxial layer.

2.2. Electrical Measurement Procedure

The electrical properties at the interface of Al-Foil and *p*-type 4H-SiC depend on several factors such as treatment on surfaces of the substrate before bonding, temperature, contact force, subsequent annealing while DW bonding. It is noteworthy that prior to bonding, no RCA cleaning procedure was introduced on the surface of the 4H-SiC sample. The cleaning procedure was done in a normal environment. In this article, our motivation was to observed and represent Al-Foil/*p*-4H–SiC electrical behavior and inhomogeneities within identically manufactured Schottky barrier diodes. We have manufactured nine diodes by diffusion welding (DW) technology. These nine diodes are manufactured with identical cleaning process and same manufacturing process parameters. Here, we emphasized the comparative study of barrier inhomogeneities and current handling capabilities of these identically manufactured Schottky diodes. So, we have chosen two diodes out of nine SBDs. The *I-V* and *C-V* characteristics on these two *p*-type 4H-SiC SBD (DWS#III and DWS#IX) with the thickness of 365 (±2) μm measurements were performed in a temperature range of 300 K–450 K. These SiC Schottky diodes are placed in an enclosed probe station integrated with a DLS-83D temperature controller from Semilab Co. Ltd. The comparative study also observed another seven Al-Foil/*p*-type 4H-SiC SBDs that were identically manufactured by DW techniques, having an average thickness of 365 (±2) μm. However, the temperature dependence of *I-V* characteristics of the DWS# III and DWS# IX was also measured at high temperature with a Keithley 2400 source and measurement unit, with a dedicated LabVIEW program current that was set up to 1A.

3. Results and Discussion

This section is divided into four subsections: temperature dependent *I-V*, *C-V* characteristics, discussion of the *I-V*, *C-V* results, and the activation energy plot are discussed based on the electronic transport and barrier inhomogeneities for *p*-type 4H-SiC based Al-Foil contact SBDs.

3.1. Temperature Dependence of I-V Characteristics

Al has been extensively used as a metal contact and interconnects in semiconductor devices, especially for Schottky contacts because it has a low SBH and low resistivity which results in

a lower forward voltage drop. However, the barrier height is of concern for current carrier transport mechanisms through the metal and 4H-SiC barrier interfaces. Therefore, to accomplish a complete understanding of the current transport across the diffusion welded Al-Foil/*p*-4H–SiC contact SBD characteristics, it is necessary to take into the consideration of thermionic emission (TE) [19], interface state density distribution [20], the image-force lowering [21], the recombination and quantum-mechanical tunneling [22,23], distinctive high level of TFE [24] and also the lateral distribution of BH inhomogeneities [25,26] that influence the device current capabilities [27,28]. The DLS-83D measurement unit exhibits a forward *I-V* characteristic, as shown in Figure 2. This figure shows the rectifying properties of nine (DWS#I-IX) Al-Foil/*p*-type 4H–SiC SBDs at room temperature.

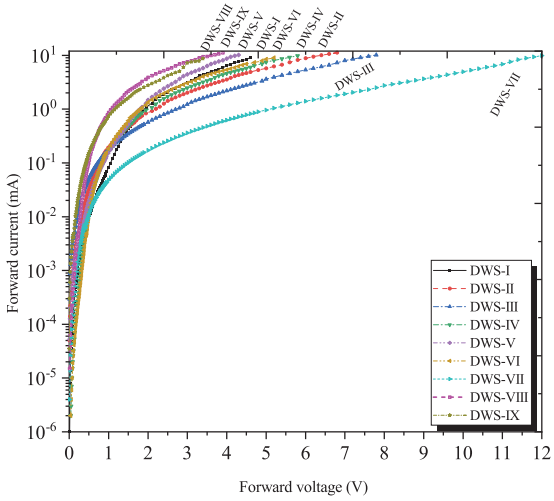

Figure 2. Current-voltage characteristics of *p*-type 4H-SiC (DWS# I-IX) SBD illustrating the effect of tunneling and showing a decrease in the bulge in current as voltage increase.

Additionally, two diffusion welded diodes (DWS# III and DWS# IX) are utilized for temperature-dependent *I-V* characteristics out of nine SBDs to study the barrier inhomogeneties and current transport process. The Figure 3 show exponential behavior over a voltage range in forward *I-V-T* characteristics for the SBDs DWS# III and DWS# IX at temperatures 300 K–450 K.

The forward current dramatically increases with temperature, as shown in Figure 3. This represents the various mechanisms of current transport dependence on temperature. It can also be observed that the measurement of forward current bulges more at high temperatures, while the thermionic emission current mechanism encountered overloads the tunneling current. However, this bulge is reduced by increasing the applied forward voltage, where the tunneling current is more prominent over the thermionic emission current, as shown in Figure 3 for the diffusion welded DWS# III and DWS# IX diodes with a temperature step of 50 K. Furthermore, a keithley 2400 and 4-point measurement unit (current set up to 1A) measures the temperature dependent forward *I-V* characteristics for the *p*-type 4H-SiC-SBD (DWS# III and DWS# IX) at room and 500 K, as shown in the inserted Figure 3. In particular, inserted Figure 3 clearly shows that with identically manufactured devices have different current loading mechanisms at different temperatures. This variation in the current handling capabilities of identically manufactured devices may be due to the thermal annealing process integrated during DW technology, as well as the cleaning process before fabrication. The total forward current that is affected by each of these temperatures at forward bias voltage for current-carrying an ideal homogeneous SBD (without considering small series resistance) can be better described by thermionic emission theory [28],

$$I = I_s \exp\left(\frac{qV}{nKT}\right)\left[1 - \exp\left(-\frac{qV}{KT}\right)\right] \quad (1)$$

$$I_s = AA^*T^2 \exp\left(-\frac{q\Phi_{B0}}{KT}\right) \quad (2)$$

where, I is the total forward current, I_s is the saturation current, Φ_{B0} is the BH, A is the area of the diode, n is the ideality factor, and A^* is effective Richardson's constant (146 Acm^{-2} K^{-2}), k is the Boltzmann's constant, q is the electron charge and T is the absolute temperature [29–31]. The temperature-dependent Φ_{B0}, n and I_s can be extracted from the experimentally obtained forward *(I-V)* characteristics, which will clarify the conduction mechanism in the Al-Foil/4H–SiC SBDs.

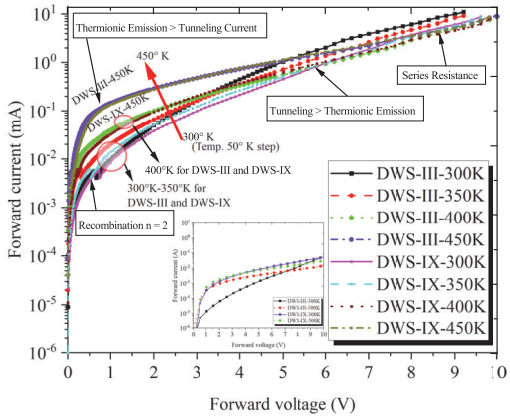

Figure 3. Forward *I-V-T* characteristic of diffusion welded *p*-type 4H-SiC-SBD (DWS# III and DWS# IX) showing various current transport mechanisms with the temperature step 50 K. The inset shows the plots of *I-V* characteristics as a function of temperature step of 200 K with current set up to 1 A.

For this purpose, the Chung and Chung procedure [32] is used to extract these parameters from the *I-V* characteristics. The saturation current I_s and the ideality factor (n) can be determined from the intercept of experimental ln (I) versus voltage (V) plot at zero voltage and the slope of the linear forward region of the ln (I) versus V plot respectively. Once I_s is determined, the barrier height Φ_{B0} and ideality factor n can be evaluated from following equations (Equations (3) and (4)) by rearranging Equations (1) and (2):

$$\Phi_{B0} = \frac{KT}{q} ln\left(-\frac{AA^*T^2}{I_s}\right) \quad (3)$$

$$n = \frac{q}{KT}\left(\frac{\partial V}{\partial(lnI_s)}\right) \quad (4)$$

Figure 4 shows the apparent barrier height and ideality factor extracted from the *p*-type 4H-SiC-SBD (DWS# III and DWS# IX) with temperature range 300 K–450 K dependent *I-V* characteristics. These obtained BH and ideality factor characteristics help to understand the behavior of the inhomogeneous potential barrier. Figure 4 demonstrate that the ideality factor decreases with increasing temperature, whereas Schottky BH increases with the increasing temperature. The large value of the ideality factor, particularly at room temperature, for both of the identically manufactured SBDs are shown in Figure 4. In DWS# III SBD, it is noted that the value of SBH Φ_{B0} has ranged from

1.03 eV to 1.42 eV, and the ideality factor decreases from 1.98 to 1.34 with increasing temperature. Barrier height variation is observed in two identically manufactured SBDs, where BH of DWS# III slightly higher than that of DWS# IX SBD are shown in Figure 4.

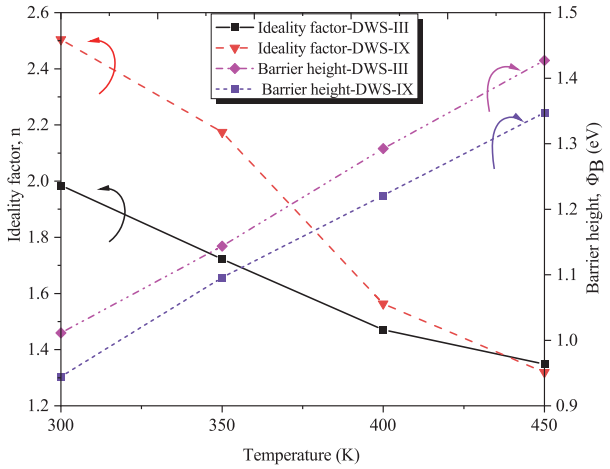

Figure 4. Ideality factor and barrier height investigation of diffusion welded *p*-type 4H-SiC-SBD (DWS# III and DWS# IX) as a function of various temperatures deduced from I-V measurement.

Unlike the DWS# III, DWS# IX SBD shows that the value of SBH (Φ_{B0}) has ranged from 0.95 eV to 1.35 eV and the ideality factor decreases from about 2.45 to 1.95 with increasing temperature. However, Raghunathan et al. [33] and other researchers [34,35] obtain a high value of the ideality factor and low value of the barrier height at low or room temperature.

These dissimilarities within identically manufactured SBD devices suggest that the recombination current is dominated at low forward voltage regions instead of classic thermionic emission theory, which is also shown in Figure 3. The noted barrier height and ideality factors divergent in both identical SBDs is resulted due to the lower electron mobility of *p*-type 4H-SiC-SBD in fractional ionization of impurities and the structural defects that are initiated by surface preparation processes or during the deposition process additionally contribute as a carrier recombination center at room temperature [36].

3.2. Temperature Dependence of C-V Characteristics

In the first scenario, the capacitance-voltage (*C-V*) characteristics of nine *p*-type identically manufactured SBDs are measured as shown in Figure 5. Except for some anomalous nature, all of the DW manufactured SBDs (DWS# I-IX) show typical *C-V* characteristics. Additionally, temperature dependent *C-V* characteristics were measured on DWS# III and DWS# IX SBDs for the SBH to study their atypical nature with a temperature range from 300 K–450 K, as shown in Figure 6. Unlike DWS# III SBD, DWS# IX shows distinct *C-V-T* characteristics, where a decrease in capacitance with increasing temperature is observed, as shown in Figure 6. In Figure 6 the *C-V-T* characteristics also shows abnormality at a higher temperature (450 K) for both DWS# III and DWS# IX SBDs. However, here it is noted that the DWS# III SBD represents more than double capacitance value at room temperature compared to that of DWS# IX at 450 K. This distinct nature within an identically manufactured SBDs could be due the to homogenous doping profile distribution. For a semiconductor with a homogenous doping profile, the differential capacitance $C = \frac{dQ}{dV}$ can be expressed by:

$$C = \frac{C_0}{\sqrt{V_{bi} - V_r}} \tag{5}$$

where

$$C_0 = A^* \frac{\sqrt{\varepsilon_q N_D}}{2}; \varepsilon = \varepsilon_0 \varepsilon_{rel}$$

In our previous paper [16], it was observed that capacitance increases with the temperature increases, such as the normal *C-V-T* characteristics for n-type 4H-SiC SBDs. However, for the DWS# III and DWS# IX SBDs, the discrepancy between these *C-V-T* characteristics can be explained by assuming the presence of inhomogeneous barrier height and the device processing as well as the measurement environment conditions, which will be discussed in the following sections.

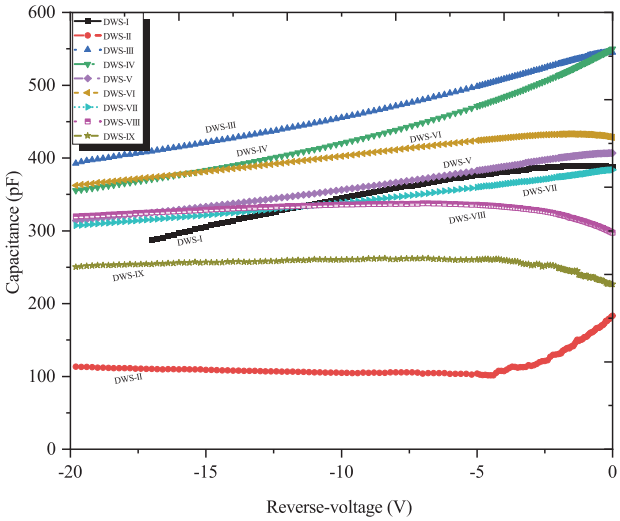

Figure 5. Room temperature C-V characteristics on various *p*-type 4H-SiC-SBDs (DWS# I-IX).

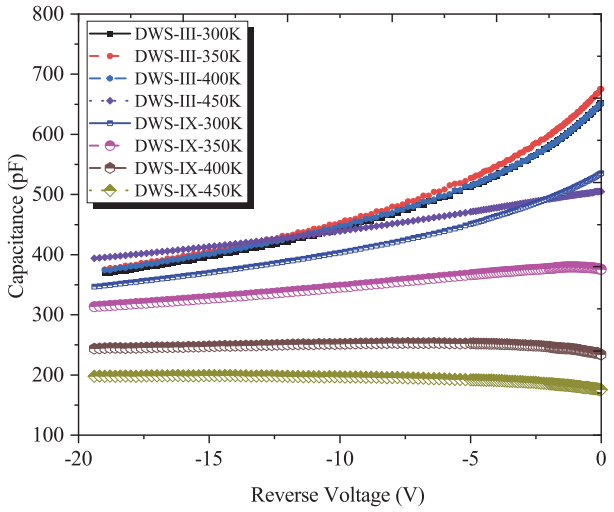

Figure 6. Temperature dependence of reverse *C-V* characteristics for *p*-type 4H-SiC- DWS# III and DWS# IX SBD.

The BH and doping concentration can be determined from the voltage intercept in plotting $1/C^2$ as a function of reverse voltage using the standard equation [36]:

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s\varepsilon_0 N_D A^2}(V_{bi} - V_r) \tag{6}$$

$$\Phi_{B0} = V_{bi} + V_n \tag{7}$$

$$V_{bi} = V_i + \frac{KT}{q} \tag{8}$$

$$V_n = \frac{KT}{q} ln(\frac{N_C}{N_D}) \tag{9}$$

$$\Phi_{B0} = V_i + \left(\frac{KT}{q}\right)\left[1 + ln(\frac{N_C}{N_D})\right] \tag{10}$$

where N_D denotes the doping concentration, V_i is the diffusion potential (voltage intercept), V_{bi} is the built-in voltage, V_r is the reverse voltage, V_n is the depth of the Fermi level (between the Fermi level position and conduction band edge), N_C is the effective density of states in the conduction band, ε_s is the static dielectric constant and ε_0 is the permittivity of free space and kT is the thermal energy. But at zero reverse voltage; the capacitance depends on doping density (N_D) and building voltage without considering the effect of image force can be represented as:

$$V_{bi} = \Phi_{B0} - (E_C - E_{Fn}) - \frac{KT}{q} \tag{11}$$

These diode doping concentrations and built-in voltages were obtained by rearranging Equation (6) from the slope and intercept of $1/C^2$ vs. V_r plot. The value of the barrier height is then determined from Equation (10). At the same time, the build-in voltages of the DW SBDs are obtained by extrapolating intersection of $1/C^2$ vs. V_r axis, which can be express by Equation (6).

Figure 7 shows the BH and doping concentration analysis obtained from the measurement of *C-V-T* values that justified the *C-V-T* characteristics. Here, it is remarkable that the higher inhomogeneous doping profile is present in DWS# IX SBD and it is one order magnitude higher than DWS# III. Additionally, the DWS# IX barrier height is lower compared to that of DWS# III SBD. Nonetheless, the values of the extracted SBH by means of *C-V* technique increase significantly as the temperature increases, as shown in Figure 7. The investigated SBH and doping density are evidently related to the effect of lattice defects in the silicon carbide, by a non-uniform interface creating inhomogeneity in the BH or thin oxide film introduced in the interface region (between Al Foil and silicon carbide layer), that was reported by Lundberg et al. [37]. Consequently, the barrier capacitance influenced in the identically manufactured DW Al-Foil/SiC Schottky contact is due to the decrease in the barrier height and formation of unknown existence of an intermediate layer.

3.3. Discussion of the I-V-T and C-V-T Results

The barrier heights of DWS# III and DWS# IX SBDs fluctuate about 0.04 eV and 0.07 eV for the *I-V-T* and *C-V-T* measurements, respectively, as noted in Figures 4 and 7. Here, we can observe that the BH variation is not significantly affected in *C-V-T* compared to that of *I-V-T* characteristics. The BH resulting from the *I-V-T* and *C-V-T* characteristic values illustrate that barrier inhomogeneity strongly depends on in the interface layer, which is caused by a slightly induced BH lowering. Another cause of the higher dependency of BH on *C-V-T* characteristics can be explained by the locally induced non-uniform interfacing lateral BH, which approaches the flat-band SBH [38,39].

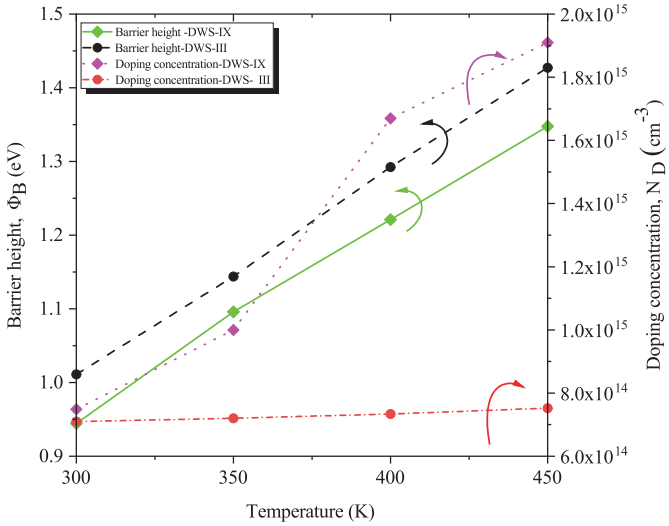

Figure 7. The barrier height and doping concentration plot as a function of various temperatures deduce from *C-V-T* measurement for diffusion welded *p*-type 4H-SiC-SBD (DWS# III and DWS# IX).

Furthermore, the barrier heights obtained from *C-V-T* characteristics are not mainly dependent on the ideality factor and therefore they are more compatible for the individual diode, as shown in Figure 7. These interfacing lateral BHs can be associated with the particular conditions, such as the cleaning preparation of these SBDs and the fabrication processing steps, especially annealing temperature [40]. This reduction in the barrier height is one of the main reasons for the effect of an intermediate layer between Al-Foil and 4H-SiC semiconductor epi-layer. Another possible justification is that a thin oxide layer is created at the interface during sample preparation, which can also act as additional capacitance in *C-V* measurements. Consequently, we can conclude that current through the contact may be significantly influenced by the existence of the inhomogeneity of BH's and this can be more justified by considering the activation energy plot for both identical Schottky diodes.

3.4. Activation Energy Plot Analysis

The activation energy plot of ln (I_s/T^2) versus $10^3/T$ expression can be retrieved from Equation (2)

$$ln(\frac{I_s}{T^2}) = ln(AA^*) - (\frac{q}{KT})\Phi_{B0} \quad (12)$$

The values of activation energy plot were calculated from the normalized *I-V-T* DWS# III and DWS# IX of Al-Foil/*p*-type 4H–SiC SBDs as shown in Figure 8. Here, the term ln (I_s/T^2) dealings with two almost parallel regions for both (DWS# III and DWS# IX) SBDs are independent of applied potential. These lines within two parallel non-uniform regions are anomalous due to the inhomogeneous barrier or potential fluctuations between the Al-Foil and *p*-type SiC epi-layer interface layer. Therefore, from these discussions, and taking into account the formation of the activation energy plot, it is assumed that at least two discrete barrier heights are present in each of the SBDs. These barrier heights are mainly concentrated locally as an interface layer existing as regions with relatively lower or higher barrier heights that is developed are due to the temperature at the boundary between these two-barrier heights regions during the formation each of the SBDs.

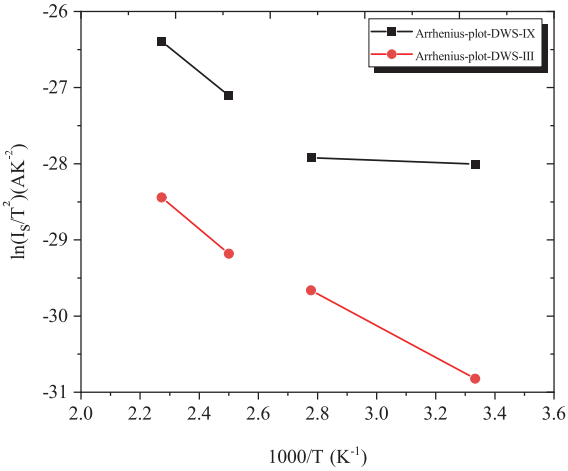

Figure 8. Activation energy plot of the ln (I_s/T^2) vs. $10^3/T$ deduced from normalized *I-V-T* data for DWS# III and DWS# IX SBDs.

4. Conclusions

In this work, we fabricated 60 µm-thick-Al foil/*p*-type-4H-SiC SBDs by DW technology. We observed Schottky like characteristics in all nine manufactured devices with identical process parameters. This investigation found undesired anomalous in their electrical characteristics and observed barrier inhomogeneties present in all SBDs. The SBH and ideality factors are different while comparing within SBDs despite their identical manufacturing process. We also found that the ideality factors is improved by annealing. It observed that at a higher temperature and higher forward voltage, the tunneling current is dominated compared to thermionic emission current mechanism. However, at room temperature, the Schottky junction current influenced by the carrier recombination center is due to incomplete ionization. These results is explained by considering the inhomogeneous barrier height due to discrete energy levels, tunneling current formation, interfacial native oxide layer formation during surface preparation and inhomogenous doping profile distribution. The results suggested that diffusion welded processing parameters and surface preparation steps need to be optimized.

Author Contributions: M.H.Z. and A.K. conceived the idea and M.H.Z. performed the developments of diodes and their experimental works. M.H.Z. drafted the article. T.R.; M.H.R. and A.K. reviewed the article. A.K. and T.R. managed funding of the project. All authors have read and agreed to the published version of the manuscript.

Funding: The Estonian Research Council through the projects IUT19-11, PUT1435 and PRG620 supported this research. We thank the support of Horizon 2020 ERA-chair Grant "Cognitive Electronics COEL"—H2020-WIDESPREAD-2014-2 (Agreement 668995; TTU VFP15051) as well.

Acknowledgments: The author would like to acknowledge Oleg Korolkov and Natalja Sleptšuk for their help during measurement related setup and discussion.

Conflicts of Interest: The authors declare no conflict of interest.

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Publication IV

Ziko, Mehadi Hasan; Koel, Ants; Rang, Toomas (2020). Characterization of Al-foil/p-4H-SiC SBDs fabricated by DW with variation of process conditions. Wide Bandgap Power Devices and Applications in Asia (WiPDA-Asia), Suita, Japan, Sep. 23–25, 2020. IEEE Xplore.

Characterization of Al-foil/*p*-4H-SiC SBDs Fabricated by DW with Variation of Process Conditions

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***Abstract*—Silicon carbide (SiC) is a wide-bandgap (WBG) semiconductor material with high thermal conductivity and radiation harness that have good potential to develop a new generation of power devices for operating at the higher temperature, high frequency, high power applications. In this paper, various manufacturing process (MP) parameters of diffusion welding (DW) *p*-type 4H-SiC Schottky contact developments are studied. Deposition temperature and pressure influence the DW Schottky barrier diodes (SBD) electrical characteristics and observed their barrier inhomogeneity. The lower doping concentration in the epilayer improves the Schottky contact characteristics with the same MP parameters. Additionally, Schottky contact with DW deposition technology shows better electrical contact compare to ion-sputtering deposition technique. Furthermore, temperature dependency of forward current-voltage (*I–V*), capacitance-voltage (*C–V*), and barrier height correspond to ideality factors measurements of DW two-MP parameters shows that there are higher barrier inhomogeneities at the metal and SiC interface compare to one-MP parameters for Aluminum (Al)-foil/*p*-4H–SiC SBDs.**

***Index Terms*—Silicon Carbide, Diffusion Welding, Schottky Barrier diode, Barrier height, *I–V*, *C–V*.**

I. Introduction

Promising properties of SiC used for the fabrication of high-quality power devices, mainly depend on the quality of the metal–SiC contacts. SiC-based SBD used in power electronics that depend on only majority carriers in contrast to bipolar devices for their operation. Unlike barrier dependent (between the *n*-type and *p*-type) p-n junction diode, Schottky diode depends on the barrier formed by the metal-semiconductor contact. SiC-based SBD privilege higher switching operation from a conducting state to a blocking state or vice versa that associate with electron-hole recombination. Unipolar behavior of *n*-type SiC SBDs already fulfilled the present market demand at the low-medium power blocking voltage range (300-1200 V, 1-20 A) [1], [2]. Designing a higher blocking voltage of an SBD reliant on the depletion region at a metal-semiconductor interface and Schottky barrier height (SBH). The selection of epilayer thickness and its doping concentration contribute to the large breakdown voltage or low on-resistance of the SBD (thick or lower doping concentration of SiC epilayer under the metal contact). The selection of lower SBH metals is vital to turn on the SBD at a lower voltage. Thick Al foil on *p*-type 4H-SiC forms a contact using DW, which shows excellent adhesion on the surface of the substrate (SiC), lower SBD height, improves the ability to handle considerable electric power and also increases the semiconductor device's current rating [3], [4], [5].

SiC consists of an endless number of crystalline forms, which are called polytypes. Among those, 4H and 6H-SiC polytypes are commercially available and attractive for the development of power electronics devices thanks to their distinct physical and electrical property [6], [7], [8]. However, the advantage of SiC, particularly the promising features of *p*-type 4H-SiC, has not yet been comprehensively accomplished to their full potential for use in the fabrication of high reliability, durability, and efficient power devices at high-temperatures. Depending on the metallization process on *p*-type 4H-SiC for rectifying contact is also very important for operating electronics at elevating temperatures [9], [10]. Besides, the quality of the material surface and the type of metal-deposition is also crucial for device performance. However, several publications on the *n*-type SiC Schottky barrier diodes using various metal contacts carried out during the last two decades [11], [12], [13], [14]. But unique characteristics of *p*-type-4H-SiC SBDs chosen for the study as it could have advantages over the n-type SiC Schottky diodes at very high current densities when self-heating comes essentially as well as high temperatures [15]. In the *p*-type 4H-SiC SBD, higher temperatures reached before the doped material becomes intrinsic. The electrons being excited from the valence band to the conduction band exceeds the number of electrons significantly donated from the impurities [15].

The Estonian Research Council, through the projects IUT19-11, PUT1435, and PRG620, supported this research. We thank the support of Horizon 2020 ERA-chair Grant "Cognitive Electronics COEL"—H2020-WIDESPREAD-2014-2 (Agreement 668995; TTU VFP15051) as well.

Also, the quality of the material surface and the type of metal-deposition are crucial for device performance. Direct bonding (DB) technology has significant attention in developing power electronics and microelectromechanical systems [16]. This DB technology used in the metal-film and substrate of the same material or metal-film and substrate of different materials without concern of the crystalline relationship between them. The main interest in DB technology is the smoothness of the surfaces without metallic contamination and the suitability of bonding surface orientation to achieve defect-free stronger bonding and structures [17]. However, DW (high-temperature DB technique) is a solid-state material joining process that utilized to bond various contact materials with the high-performance semiconductor substrate. DW technology can help to improve the quality of contacts.

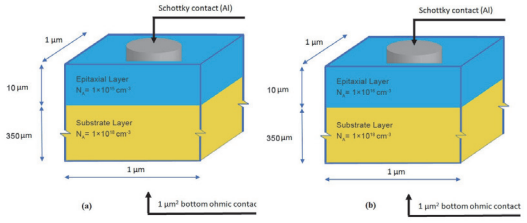

Fig. 1. Illustration of the structure and doping concentration (a) N_A=1×10^{15}cm^{-3}, (b) N_A=1×10^{16}cm^{-3} of the Schottky barrier diodes.

In this paper, *p*-type-4H-SiC SBDs with Al-foil as metal contacts fabricated with a technique: DW. Our unique DW technique can provide this direct metallization. This deposition technique improves the quality of various metal or ceramic contacts and gives one technological step to realize the better contact situation compared to other metal depositions techniques [4], [5]. The DW methods of metallization to *p*-type SiC have a particular interest in this study. A schematic of fabricated diode structures and their doping concentration is shown in Figure 1 a, b. This work aims to explain the inhomogeneity barrier height formations and current handling capabilities influenced by the manufacturing process parameters on the 4H-SiC SBDs using experimental *I-V-T* and *C-V-T* characteristics.

II. MATERIAL AND SPECIMEN

This section contains the experimental details and procedures adopted to develop *p*-type 4H-SiC SBD.

A. Sample preparation procedure

The samples used for the development of SBD consist of 10 mm x 10 mm pieces diced from a 76 mm Al doped with two *p*-type 4H–SiC wafer purchased from Cree Research Inc. The structure comprises a 10μm thick *p*-epilayer with doping N_A=1×10^{15}cm^{-3} (from Cree Inc.) and another epi ready from Nostel AB with *p*-type doping concertation N_A=1×10^{16}cm^{-3} (Nostel) grown on 350μm thick highly doped *p*+ substrate with N_A=1×10^{18}cm^{-3}. The Si-face 4H–SiC (0001) 4° off-axis surface orientation polished by the chemical mechanical method on the bonding face of the wafer (i.e., the side to which Schottky contact made).

In the sample cleaning process, samples were first degreased in methanol for 5 min, followed by a dip in (48%) diluted H_2O: HF for 5 min and rinsed in normal water for 5 min. Finally, the samples were then subjected to deionized (DI) water for 5 min.

B. Sample deposition procedure

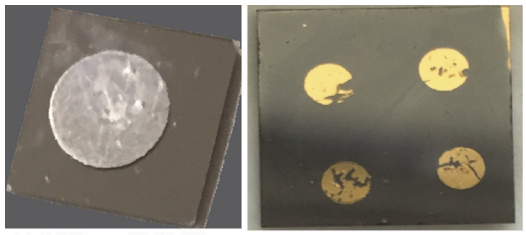

Fig. 2. Physically fabricated (a) diffusion welded (b) Sputtered Schottky barrier diode.

The Schottky and ohmic contact on the epi and substrate layer was achieved respectively by the Al-foil with a thickness of 60μm, and 100μm was diffusion welded under the base pressure 1×10^{-4}mbar. Two sets of samples fabricated by (1) one-step manufacturing process (1MP) where ohmic and Schottky contact made at a time. In this process, Al-foil and SiC surface layer brought in to contact each other under the pressure of 650N force for 5 min and applied temperature at 575°C for 15 min and (2) another sample also made by two manufacturing process (2MP). In this process, Schottky and ohmic contacts are made separately with the pressure of 650N (5 min) and 750N force (5 min), respectively, at 560°C temperature for 15 min at the vacuum pressure not less than 1×10^{-4}mbar.

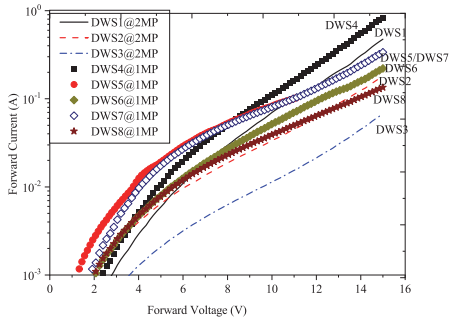

Fig. 3. Room temperature forward *I-V* characteristics of DW Al-foil/*p*-type-4H-SiC SBDs with the same doping concentration at various process conditions.

We also manufactured Au/*p*-type-4H-SiC contact by ion beam sputtering technology with room temperature substrate heating at the vacuum pressure not less than 1×10^{-4}mbar and annealed with 400°C for 20 min.

III. EXPERIMENTAL RESULTS AND DISCUSSION

In our recent work, we investigate manufacturing process parameters to developed SBDs and discuss their *I-V* and *C-V* characteristics of DW technology on *p*-type 4H-SiC SBD. A schematic of experimentally fabricated by DW and ion sputtered SBD structures are shown in Fig. 2 a, b.

For this study, we manufactured a total of 8 diodes using one MP step (5-diodes) and two MP steps (3-diodes) by DW technology. All the Al-foil/*p*-type-4H-SiC shows rectifying properties. Keithley-2400 source and measurement unit with the LabVIEW program measure forward voltage drop. The forward characteristics of those manufactured SBDs shown in Fig. 3. We considered two diodes, namely DWS4 (for 1MP), and DWS1 (for 2MP) out of 8 SBDs (1MP or 2MP), for the temperature-dependent *I-V* and *C-V* characteristics discussion.

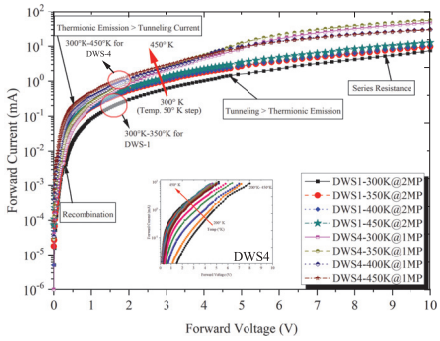

Fig. 4. Temperature dependence forward *I-V* characteristics of different manufacturing process parameters for Al-foil/*p*-type-4H-SiC SBDs.

A. Temperature dependence I-V and C-V characteristics

Al-foil/*p*-type-4H-SiC Schottky SBD (DWS1 and DWS4) performances evaluated through temperature dependence *I-V* characteristics. The performance level and degradation of the DW manufactured SBDs are highly dependent upon the Al-foil as a metal contact, process parameters, operating current flowing through the device, and series resistances. The forward *I-V* characteristics of Al-foil/*p*-type-4H-SiC SBDs measured in the temperature range of 300K to 450K.

The I-V characteristics of these diodes show exponential behavior over a voltage range at temperatures from 300K-450K. Fig. 4. shows forward current dramatically increase with temperature and more current bugling notice at a lower temperature. The general behavior of the temperature dependence forward *I-V* characteristics of Al-foil/4H-SiC SBD was consistent with thermionic emission, tunneling, diffusion, and recombine phenomena [3], [9]. Fig. 4 show that thermionic diffusion currents are predominant at low forward voltage. There are also quantum mechanical tunneling currents present for heavily doped *p*-type 4H-SiC, where the depletion width is small. Figure 4 clearly shows DWS1 (2 MP step) have different current loading capabilities compare to DWS4 at different temperatures. This variation in the current handling

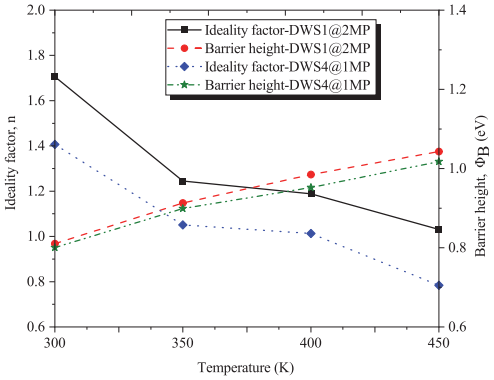

Fig. 5. Temperature dependence ideality factor and barrier height plots for DW Al-foil/*p*-type-4H-SiC SBDs (DWS1 and DW4 devices).

capabilities of DW manufactured devices may be due to the integrated thermal annealing process during DW technology. For the case of DWS1, the device undergone two times annealing process while manufacturing front and backside contacts. Fig. 4 also shows the DWS4 (1MP) Al-foil/4H-SiC SBD has high series resistance compare to DWS1 (2MP) at various temperatures. This high series resistance causes more significant bending at high temperatures because the number of carriers in the conduction band is higher, and thus currents are greater. Since series resistance affects higher currents than lower currents, the resistance changes the curves at lower voltages for the higher temperatures.

Figure 5 shows the distinct barrier height and ideality factor extrapolated from I-V characteristics that help to understand the behavior of the inhomogeneous potential barrier of the *p*-type 4H-SiC-SBD (DWS1 and DWS4). Figure 5 illustrates that the ideality factor decreases with increasing temperature, whereas Schottky BH increases with the increasing temperature. The ideality factor, particularly at room temperature for DWS1 (n=1.7), is higher than the DWS4 (n=1.4) manufactured by the DW technology shown in Figure 5. SBH estimated for DWS1 SBD ranged from 0.97 eV to 1.37 eV, and the ideality factor decreases from 1.70 to 1.03 at 300K and 450K, respectively. And SBH of DWS4 SBD increasing from 0.95 eV to 1.33 eV, and the ideality factor decreases from 1.40 to 0.78 at 300K and 450K, respectively. The barrier height and ideality factor are slightly lower for 1MP (DWS4) than to 2MP (DWS1) for temperatures 300K-450K, as shown in Figure 5.

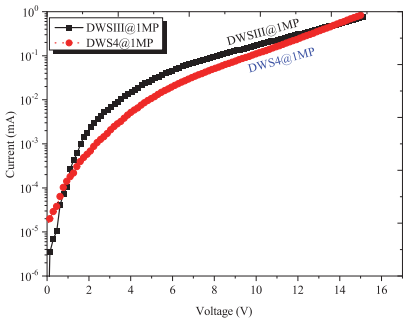

Fig. 6. Room temperature forward *I-V* characteristics show better Schottky contact for low doped DWSIII than high doped DWS4 Al-foil/*p*-type-4H-SiC SBDs manufactured by DW.

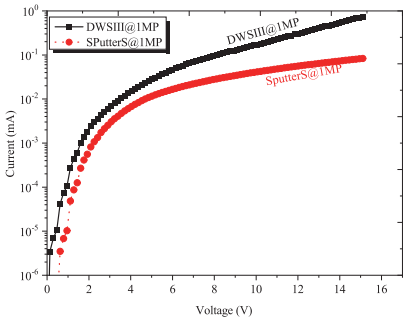

Fig. 7. Room temperature DW Al-foil/*p*-4H-SiC SBD forward I–V characteristics show better Schottky contact than Au/*p*-4H-SiC SBD manufactured by the sputtered deposition technique (N_A=1×10^{15}cm^{-3}).

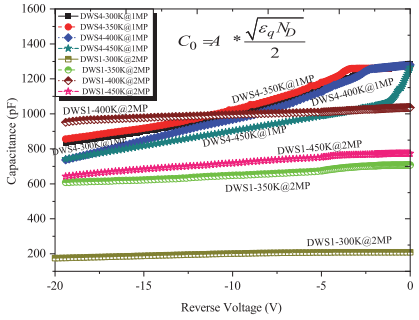

Fig. 8. Temperature dependence of reverse *C-V* characteristics of DW Al-foil/*p*-type-4H-SiC SBDs (DW4 and DWS1) with different MP parameters.

The forward *I–V* characteristics also studied at different epi-layer doping concentrations with the same MP parameters. The improvement of Schottky contact observed at the lower doping (DWSIII-N_A=1×10^{15}cm^{-3}) concentration shows in Fig. 6. This measured DW *p*-type 4H-SiC Schottky diode (DWSIII) SBH and the ideality factors discussed in our paper [18]. So, less metal Fermi-level energy is required to pass the electron, from metal to SiC for the DWSIII or DWS4 (current handling is heigh and less turn on-voltage) compare to DWS1. The detailed results of fermi-level pinning need separate attention and discussion.

We also compared DW *p*-type 4H-SiC SBD with ion-sputtered gold- *p*-type 4H-SiC SBD. The DW SBD (DWSIII) forward *I-V* shows better electrical characteristics than to ion-sputtering due to the manufacturing process parameters and their barrier height differences, as shown in Fig. 7.

B. Temperature dependence C-V characteristics

The temperature-dependence *C-V* characteristics of DWS4 and DWS1 *p*-type DW manufactured SBDs measured with a temperature range from 300K–450K, as shown in Fig. 8. Unlike DWS1 SBD, DWS4 shows distinct *C-V-T* characteristics, where a decrease in capacitance with increasing temperature observed. The *C-V-T* characteristics of DWS1 also show abnormality at a higher temperature (400K). However, the DWS4 SBD represents four times more capacitance value than that of DWS1 SBD at room temperature. This distinct nature of DWS1 SBD (2MP) manufactured by DW technology could be due to the homogenous doping profile distribution, multilevel interface layer created during the two manufacturing process steps in the DW technology compare to DWS4. There are also more defects introduced in the interfaces. As a result 2MP leads the tunneling current conversely to find the passages through minimal resistance having the energy to cross the lower barriers.

Fig. 4 and 8 indicate that tunneling current is a dominant mechanism for the 2MP (DWS1) compared to 1MP (DWS4). Thus, Al-foil/*p*-type 4H-SiC SBD samples had a more significant tunneling component, especially for 2MP steps, probably caused by reactions between the metal and carbon face of the 4H-SiC crystal. Therefore, the higher series resistance values for the Al-foil/4H-SiC devices come about at higher temperatures, indicating increased chemical activity with the carbon faced contact and a larger bulk resistance with higher temperatures.

IV. CONCLUSION

In this paper, the manufacturing process (MP) parameters (temperature and pressure) investigated the electrical properties of DW Al/*p*-type-4H-SiC SBDs. The reported work focused on the significant improvement of experimentally measured electrical characteristics of Al-foil/*p*-type-4H-SiC SBD using annealing at higher-temperature by DW. The forward current-voltage *(I–V)* characteristics studied at different doping concentrated with the same MP parameters and improvement of Schottky contact observed at the lower doping concentration. The result shows the significant influence of

annealing process in their barrier height and ideality factor that observed for Al/*p*-type-4H-SiC SBDs. This analysis helps to evaluate temperature-pressure influenced and better understand to optimized MP parameters for diffusion welded Schottky barrier diode development. Therefore, it suggested that Schottky contacts made by DW technology need to use 1MP parameters to achieve better Schottky contacts.

ACKNOWLEDGMENT

The author would like to acknowledge Mr. Raul Land for his help during measurement related setup and discussion.

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Curriculum vitae

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ISSN 2585-6901 (PDF)
ISBN 978-9949-83-764-9 (PDF)