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DEVELOPMENT OF A CAMERA PROTOTYPE FOR A FLOW CYTOMETRY SYSTEM

Master's Thesis

Supervisor: Ants Koel
Professor

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TALLINNA TEHNIKAÜLIKOOL
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KAAMERA PROTOTÜÜBI ARENDAMINE VOOLUTSÜTOMEETRIA SÜSTEEMILE

Magistritöö

Juhendaja: Ants Koel
Professor

Tallinn 2021

Author’s declaration of originality

I hereby certify that I am the sole author of this thesis. All the used materials, references to the literature and the work of others have been referred to. This thesis has not been presented for examination anywhere else.

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Abstract

Flow cytometry is a technology that has a lot of potential. With use of advanced processing techniques and embedded technologies, there can be devices that are both portable and give instant results. There are devices on the market used for substance analysis in areas like medical and biological. These devices are big and depended on external processing system.

This thesis' purpose is designing a camera system prototype for a portable, fully automated flow cytometry system. This design would be the one of the first steps in developing an improved system.

The design has been started with investigation of the base requirements and deciding the design technologies. Experiments supporting the detailing of the specification have been carried about. After the decision of the base technologies the device functional design is accomplished, suitable components for functional blocks compared and decisions taken for the final design. The camera system has been built around ONSemi PYTHON300 sensor and Xylinx Zync7000 on PicoZed 7020 carrier board. As the next step the hardware design has been finalized following the application rules of decided technologies and best practices. While making the decisions, the compactness and fast processing capabilities expected from the final flow cytometric system, have been considered.

This thesis is written in English and is 46 pages long, including 10 chapters, 24 figures and 11 tables.

Annotatsioon

Kaamera Prototüübi Arendamine Voolutsütomeetria Süsteemile

Voolutsütomeetria tehnoloogial on palju potentsiaali. Arenenud töötlemistehnikate ja sisseehitatud tehnoloogiatega on võimalik luua seadmeid, mis on kaasaskantavad ning annavad koheseid tulemusi. Hetkel on turul aineanalüüsi seadmed, mida kasutatakse meditsiini ja bioloogia valdkonnas. Need on suured seadmed, mis sõltuvad välisest töötlussüsteemist.

Käesoleva magistritöö eesmärk on disainida kaamerasüsteemi prototüüp kaasaskantava ja täielikult automatiseeritud voolutsütomeetria süsteemi jaoks. Käesolev disain oleks üks esimesi samme parendatud süsteemi loomiseks.

Disainimisprotsess algas põhinõuete uurimisest ja disainitehnoloogiate valimisest. Spetsifikatsiooni üksikasjade väljaselgitamiseks viidi läbi eksperimendid. Pärast baastehnoloogiate valimist oli võimalik luua seadme funktsionaalne disain, võrrelda sobilikke komponente funktsionaalsete plokkide jaoks ning langetada otsus lõpliku disaini osas. Kaamerasüsteem on ehitatud ONSemi PYTHON300 sensori ja Xylinx Zync7000ga PicoZed 7020 kandeplaadi ümber. Järgmise sammuna loodi riistvara disain järgides valitud tehnoloogiate ja parimate praktikate rakenduseeskirju. Otsuste vastuvõtmisel on lähtutud eeskätt sellest, et lõplik voolu tsütomeetriline süsteem oleks kompaktne ja kiire töötlemisvõimekusega.

Lõputöö on kirjutatud inglise keeles ning sisaldab teksti 46. leheküljel, 10 peatükki, 24 joonist, 11 tabelit.

List of abbreviations and terms

fps	Frames-per-second
LoC	Lab-on-a-chip
SBC	Single Board Computer
SoM	System-on-module
CPU	Central Processing Unit
GPU	Graphical Processing Unit
FPGA	Field Programmable Gate Array
PCR	Polymerase Chain Reaction
PS	Processing Unit
PL	Programmable Logic
USB	Universal Serial Bus
ARM	Advanced RISC Machine
RISC	Reduced Instruction Set Computer
SPI	Serial Peripheral Interface
IO	Input-Output
GPIO	General Purpose Input Output
LVDS	Low-Voltage Differential Signalling
DC	Direct Current
Mbps	Megabits-per-second
MOSI	Master Out Slave In
MISO	Master In Slave Out
SCLK	Serial Clock
PCB	Printed Circuit Board
LED	Light Emitting Diode
I2C	Inter-Integrated Circuit
TVS	Transient Voltage Suppressor
IQA	Image Quality Assessment
MRCC	Multi-Region Clock Capable
AXI	Advanced Extensible Interface

Table of contents

List of figures

List of tables

1 Introduction

Lab-on-a-chip (LoC) is a device that combines one or multiple laboratory functions in a small area, usually square millimetres to centimetres, to achieve high throughput data. [1]. LoC has applications in the food industry, medicine, agriculture, and other similar fields that require laboratory functions which are applicable in a LoC. Properties, like using fluids on the scale of microlitres, portability and relatively low cost of the microfluidics chip are big advantages, especially on medical testing applications.

Lab-on-a-chip (LoC) can be the future of analysis of substances, because of quick results, and room for improvement like making the system mobile and more accurate. Optical detection-based LoC systems are prevailing due to the well-developed fluorography method and less probability for sensor contamination. Optical methods use digital image sensors, optic system to gather images from a LoC and image analysis can be done manually or digital image processing by a computational system. The research topic of this thesis is designing a prototype imaging system for a LoC system.

2 State-of-the-art Overview

2.1 Other Similar Devices on the Market

2.1.1 2100 Bioanalyzer (Agilent Technologies)

An integrated system, including data processing, microfluidic chip for DNA, RNA, or protein analysis. Data processing function is performed with laptop which is provided with the device. For sensing droplets, device uses laser induced fluorescence detection. Its dimensions are 162 mm x 412 mm x 290 mm. [2]

2.1.2 Cedex HiRes Analyzer (Roche Diagnostics)

Cedex HiRes Analyzer is image processing-based technology. It takes high resolution images of the object. Device comes with a PC to analyse data. It provides information

cell concentration, cell diameters, viability, aggregates, and morphological parameters. Its dimensions are 40.5 cm x 53.3 cm x 46.5 cm. It can analyse objects1 – 90 µm in size. [3]

2.1.3 LightCycler 480 System Technology

It is a PCR (polymerase chain reaction) device that has functions like heating and cooling. Data acquisition is made with CCD camera. Data processing is done with the computer provided with the device which has special software for this operation. [4]

2.1.4 RainDrop Digital PCR System

It is a PCR system that is used for quantifying DNA and RNA. RainDrop uses droplets for quantifying. It comes with a computer for data processing.

2.2 Other Literature

There are papers about applications on imaging microfluidics, that are using high-speed imaging with FPGAs. [5] [6]. These applications are using 64fps and 71fps frame rates for imaging with up to 1 MP resolutions. There is another paper proposes real-time data collection using frame-rates exceeding 30000fps using parallelism property of FPGAs [7].

3 Problem Statement

Camera prototype is a part of a project, PRG620, Cognitronic Lab-on-a-Chip System for Highly Automated Flow Cytometry. Camera system can be defined with these parts

- Optics
- Image sensor
- Image data acquisition system

Next system will be connected to the camera is the system responsible for image processing and data analysing.

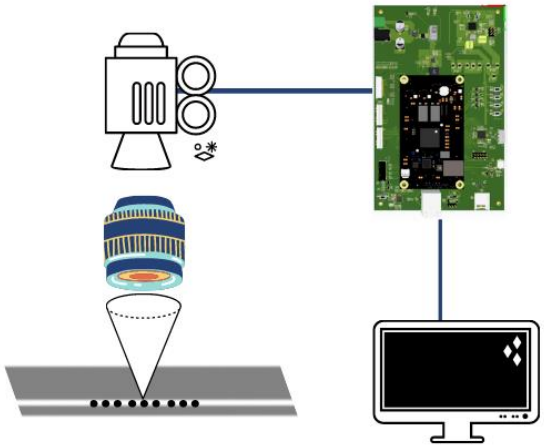


Figure 1 General LoC imaging system presentation

Image sensor and image acquisition system and part of image processing system will be taken into consideration. Selecting and developing camera and getting data from camera and transferring proper data to next system is purpose of this project.

3.1 System Requirements

Optical detection-based LoC systems need certain properties to make it work accurately and efficiently. The system can be divided into two parts: the sensor part and the image acquisition part. The sensor part consists of an image sensor and optics which are attached to it. The image acquisition part is responsible for getting image data from the sensor part and transferring the data to next system which is responsible for image processing and data analysing. These systems need to fulfil requirements of the project and can lead to final system design as first step of design process.

3.1.1 Image Sensor Requirements

Image sensor is responsible for getting image data from the channel as droplets are passing. The channel is positioned and zoomed in the sight of camera with the help of optics.

Image sensor needs to have enough resolution and frame rate for getting a footage, which is enough to get information about the substance under analysis. Depending on the type of information needed (just fluorescence detection or additional image analysis for morphology). In the project specifications, the frame rate is one of the primary

development targets, and hence it is more important than resolution. Frame rate need to be enough to be able capture droplets as they are passing and track each of them on their way. The determined minimum frame rate for this task in the current project is 1000 frames-per-second (fps).

Region-of-interest (ROI) is a region of the image that has relevant data for the purpose of the application. [8] ROI is a hardware image sensor feature. With ROI feature, data size is reduced and data acquiring, and processing will take less resources. Also, ROI feature makes it possible increasing frame rate of the image sensor by decreasing the pixel count to convert data. [9]

3.1.2 Image Acquisition System Requirements

Image acquisition system is responsible for getting raw data from image sensor and provide processable data to image processing system.

To be able to keep up with high frame rates, the image acquisition system needs to have high speed data interfaces and it requires memory for buffering data for the following image processing system which might not have high processing power or slow interface to receive the data in real time. The whole system is planned to be as compact as possible. For making the system more compact, image acquisition system can be designed to have capability of processing or pre-processing the data or even in addition to processing, analyse the data.

3.2 Objectives

The objective of this project is to create an imaging system prototype, focusing on hardware aspects, capable of acquiring images from lab-on-chip with the following requirements.

- Capable of acquiring images from sensor at minimum frame rate of 1000 fps (or, alternatively, combined with the following requirements, enabling the processing of single droplet features at a rate 1000 droplets/s).
- Camera must have enough resolution to enable processing of acquired images (separate features like presence of fluorescence, size, edges for droplets in size of 50 µm +/- 50%).

- Optics must have the capability to focus on the desired area and must have the matching capability to sensor for following image processing to produce the results.

4 Preliminary Image Acquisition Experiment

A simple setup was prepared with Raspberry-PI 4 (RPI) single board computer and RPI high-definition camera which is tuned to work with RPI using “raspistill” command line application. The purpose was to determine the general idea about the optical system architecture, how the images will look with an off-the-shelf camera, and adjust the overall system concept and specification by obtaining images from the prototype LoC. Extension tubes and different types of lenses available in the lab were used for this experiment.

4.1 Methodology

For this test, RPI SBC (single board computer) was used as an image acquisition device. A simple setup was prepared in order to stabilize the microfluid chip in front of the camera. For light source, a simple LED torch with 70lm lighting power was used. RPI high-definition camera with IMX477 image sensor was connected to RPI 4 over its MIPI CSI2 interface. The best image was attempted to be acquired by using different combinations of extension tubes and adjusting the distance between the chip and the lens.

4.2 Equipment

4.2.1 Processing Device

RPI 4 is used for interfacing camera with its MIPI-CSI2 interface.

4.2.2 Camera

High-definition camera with IMX477 image sensor from Sony for RPI 4 is used.

4.2.3 Lenses

Five different lenses were used in this test:

Table 1 List of lenses

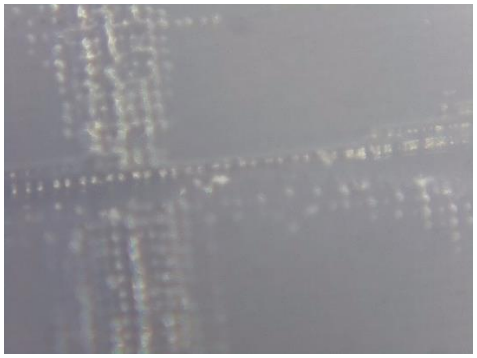
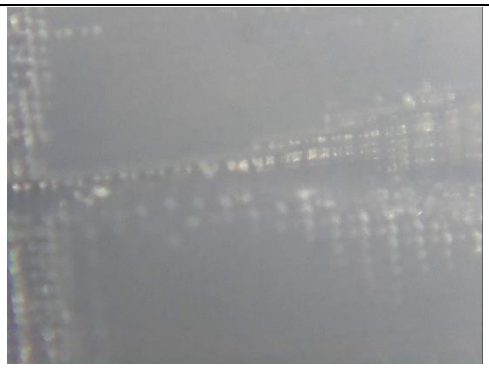
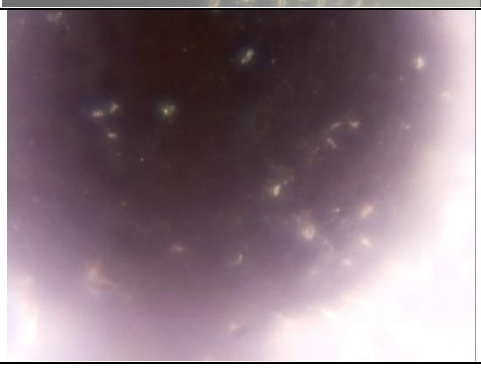
L01 Microscope lens with CS mount 10x	
L02 Canon TV Lens with CS mount, 35mm	
L03 CCTV lens 6mm, ½.5	
L04 1/3” 6-60mm, 1 : 1.6	
L05 CCTV lens 25mm, F1.4	

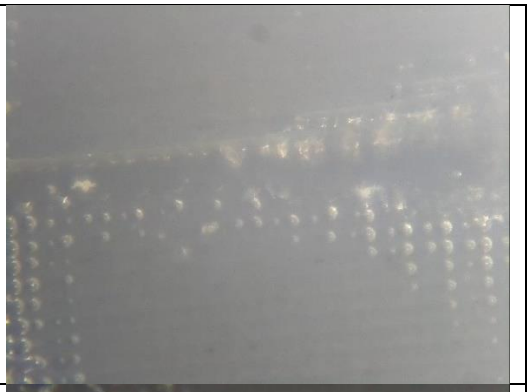
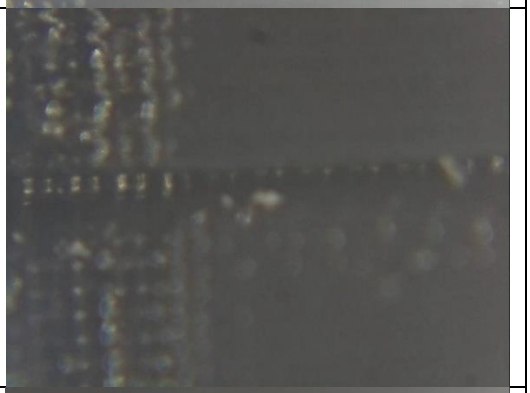
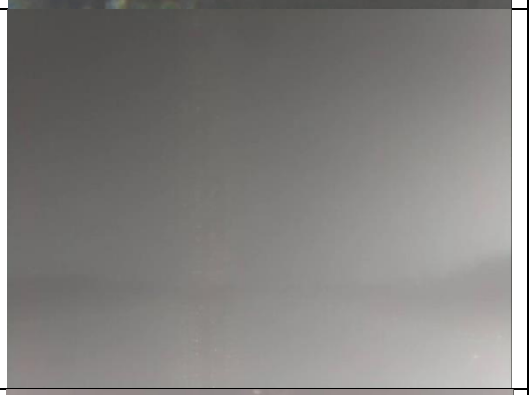
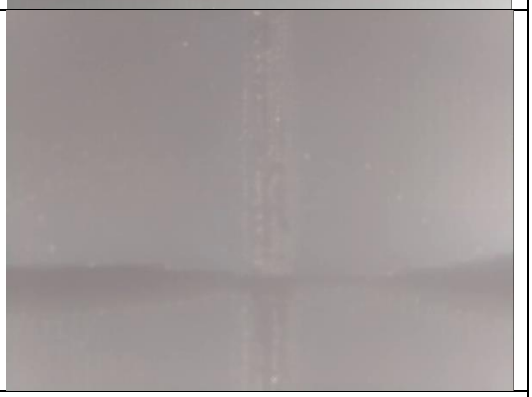
4.2.4 Tubes

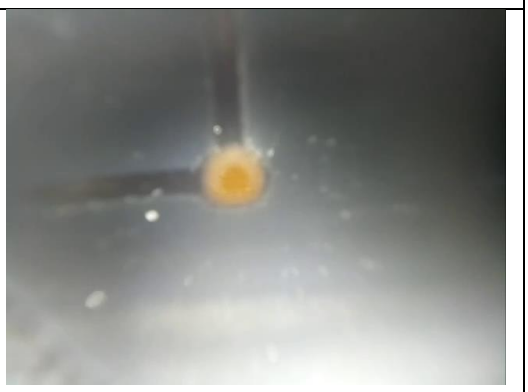
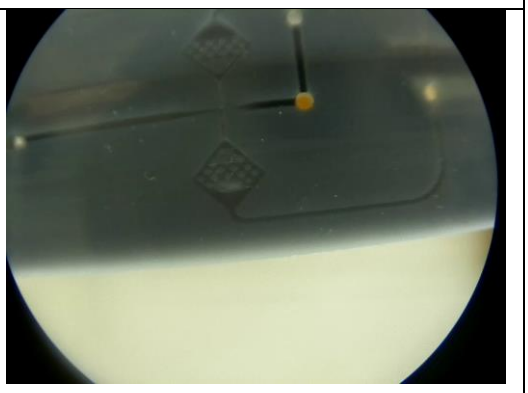
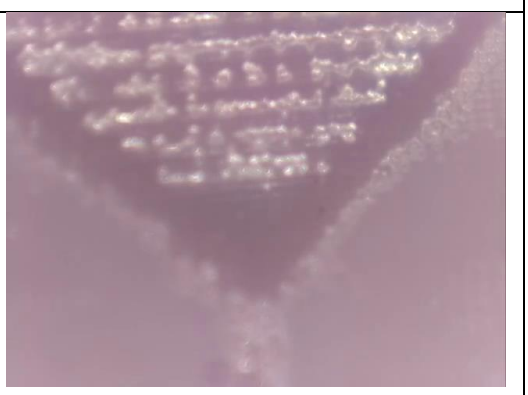
There are different lengths of tubes used for increasing zoom level of lenses. Tube lengths are 10 mm, 20 mm, 40 mm.

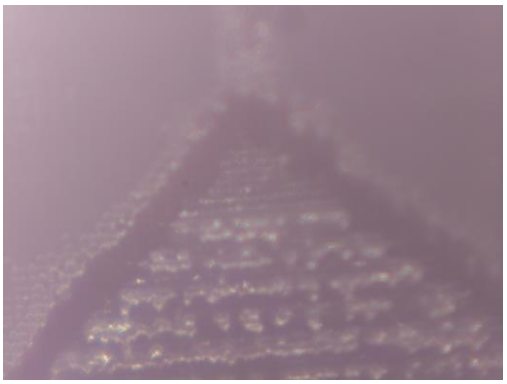
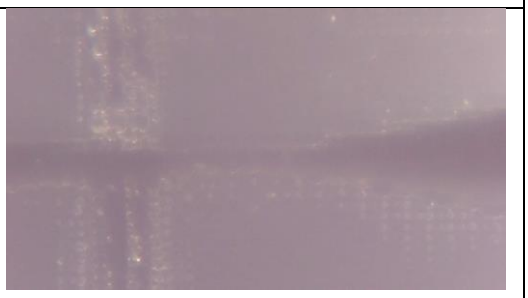
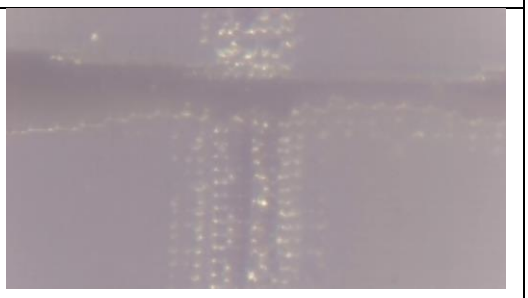
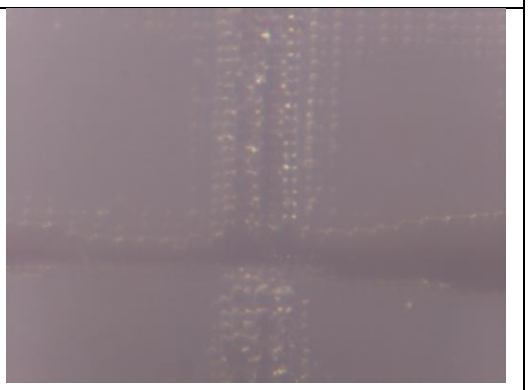
4.3 Results

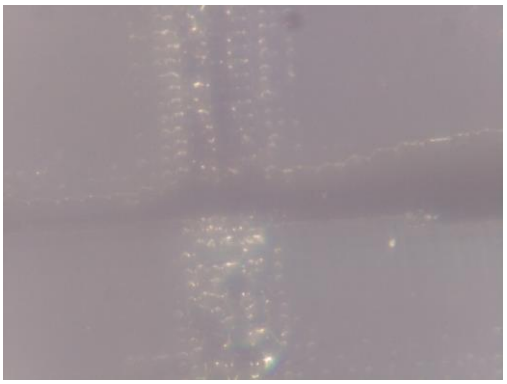
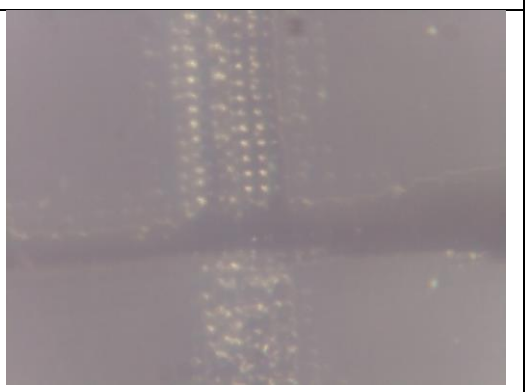
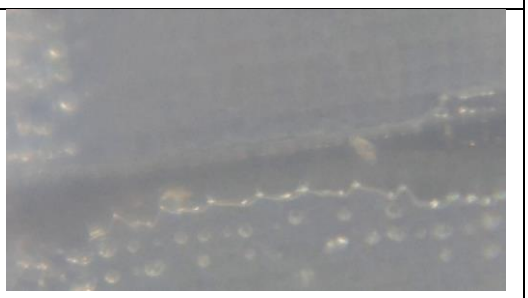
Table 2 Preliminary Image Acquisition Results

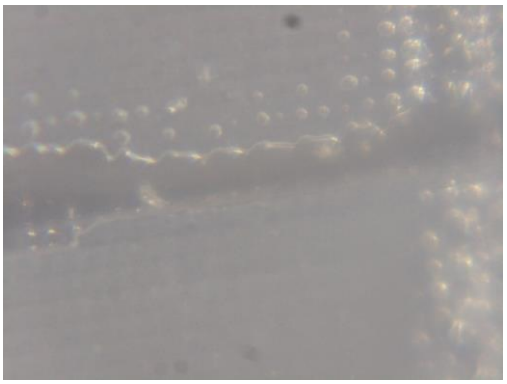
Tubes used:	**image**
Lens : L01-microscope lens Tube : 20mm Resolution : 1024x768 piqe output : 27.92	
Lens : L01-microscope lens Tube : 20mm Resolution : 1024x768 piqe output : 33.52 Channel area	
Lens : L01-microscope lens Tube : 20mm +20mm Resolution : 1024x768 piqe output : 33.61	
Lens : L01-microscope lens Tube : 20mm +20mm Resolution : 1024x768 piqe output does not matter for this image Hole area Does not offer any reference	

Lens : L01-microscope lens Tube : 20mm +20mm Resolution : 1024x768 piqe output : 32.25 Channel area	
Lens : L01-microscope lens Tube : 20mm +20mm +20mm Resolution : 1024x768 piqe output : 43.32 Channel junction area	
Lens : L02-Canon TV lens Tube : 20mm +20mm +20mm Resolution : 1024x768 piqe output : 76.28 Channel junction area, slightly out of focus	
Lens : L02-Canon TV lens Tube : 20mm +20mm +20mm Resolution : 1024x768 piqe output : 82.48 Channel junction area, more in focus	
Lens : L03 Tube : 20mm +20mm Resolution : 1024x768 chip cannot be focused with this combination	
Lens : L03 Tube : 20mm +20mm + 20mm Resolution : 1024x768	

chip cannot be focused with this combination. Adjusting back-focus did not yield a result.	
Lens : L03 Tube : no tubes Resolution : 640x480 piqe output does not matter in this image chip needs to be too close	
Lens : L04 Tube : no tubes Resolution : 1024x768 piqe output does not matter for this image chip needs to be too close	
Lens : L04 Tube : no tubes Resolution : 640x480 piqe output does not matter for this image Back-focus is increased. Image cannot be focused.	
Lens : L05 Tube : 40mm+20mm Resolution : 640x480 piqe output : 58.27 Marking area that points channel junction	

Lens : L05 Tube : 40mm+20mm Resolution : 4056x3040 piqe output : 5.86 Marking area that points channel junction	
Lens : L05 Tube : 40mm+20mm + 10mm Resolution : 1920x1080 piqe output : 47.06 Channel junction	
Lens : L05 Tube : 40mm+20mm + 10mm Resolution : 1920x1080 piqe output : 43.90 Channel junction	
Lens : L05 Tube : 40mm+20mm + 10mm Resolution : 4056x3040 piqe output : 6.23 Channel junction	
Lens : L05 Tube : 40mm+20mm + 20mm+10mm Resolution : 1920x1080 piqe output : 45.11 Channel junction	

Lens : L05 Tube : 40mm+20mm + 20mm+10mm Resolution : 4056x3040 piqe output : 5.45 Channel junction	
Lens : L05 Tube : 40mm+20mm + 20mm+20mm Resolution : 1920x1080 piqe output : 40.07 Channel junction	
Lens : L05 Tube : 40mm+20mm + 20mm+20mm Resolution : 4056x3040 piqe output : 4.61 Channel junction	
Lens : L01 Tube : 40mm+20mm Resolution : 1920x1080 piqe output : 44.97 Channel junction	

Lens : L01 Tube : 40mm+20mm Resolution : 4056x3040 piqe output : 6.13 Channel junction	

4.4 Conclusions and specification updates

There are two main types of image quality assessment (IQA) techniques. One is subjective evaluations which is assessing quality based on human observations. Other is objective evaluation which is done by computer processing. [10] In this experiment, assessment made mostly on observations.

Objective IQA methods can be full reference no reference and reduced reference methods. [11] Some of computer algorithms requires reference image to make assessment on image quality. In this case it is impossible to acquire a reference image. For IQA, Matlab function “piqe” is used for getting objective results on images. In Table 2, “piqe” function outputs can be found.

Some lenses have very long focus point that makes it not practical to use it. For example, the lens labelled as L04 was not suitable for getting close images. Using tubes reduces light input to the image sensor dramatically after a point and external light source is mandatory. External light source needs to be place in a specific angle or other special way to prevent reflections and homogenous light over the LoC. Very short working distance length has very tight depth of field makes the object in focus in very small span of distance.

It is concluded, to be able to capture very small objects, lenses and mechanical structure is more important than image sensor.

5 Decision of Components and System Structure

While designing the camera prototype, flexibility, compactness, availability, and adaptability are considered.

5.1 Image Sensor Selection

For the given requirements, a few models of image sensors are considered. Camera selection is narrowed down to three image sensors.

5.1.1 Sony IMX477 Image Sensor

IMX477 is very high resolution (12MP) camera for consumer applications. It can go up 240fps at 1080p resolution. It has ROI feature that can increase the frame rate. [12]. This sensor is used in RPI high-definition camera makes it possible to easy prototyping.

5.1.2 LUX1310 Image Sensor

LUX1310 is 3 MP camera, has applications like barcode scanning, automation, industrial and biomedical markets. It has frame rate of 1070 fps at 1280x1024 resolution. It can have multiple simultaneous ROI frames. There are 16 LVDS data lanes, each lane can have 300Mbps when working clock speed of 25Mhz or 1080Mbps when working clock speed of 90MHz. [13]

5.1.3 PYTHON 300 Image Sensor

Python 300, 0.3MP camera with ROI feature. It can have multiple simultaneous ROIs. It has 815fps at 0.3MP resolution. It can go up 1000fps target frame rate with ROI feature and ZROT (Zero ROT) as it can be seen on Python Frame Rate Calculator tool OnSemi provided.

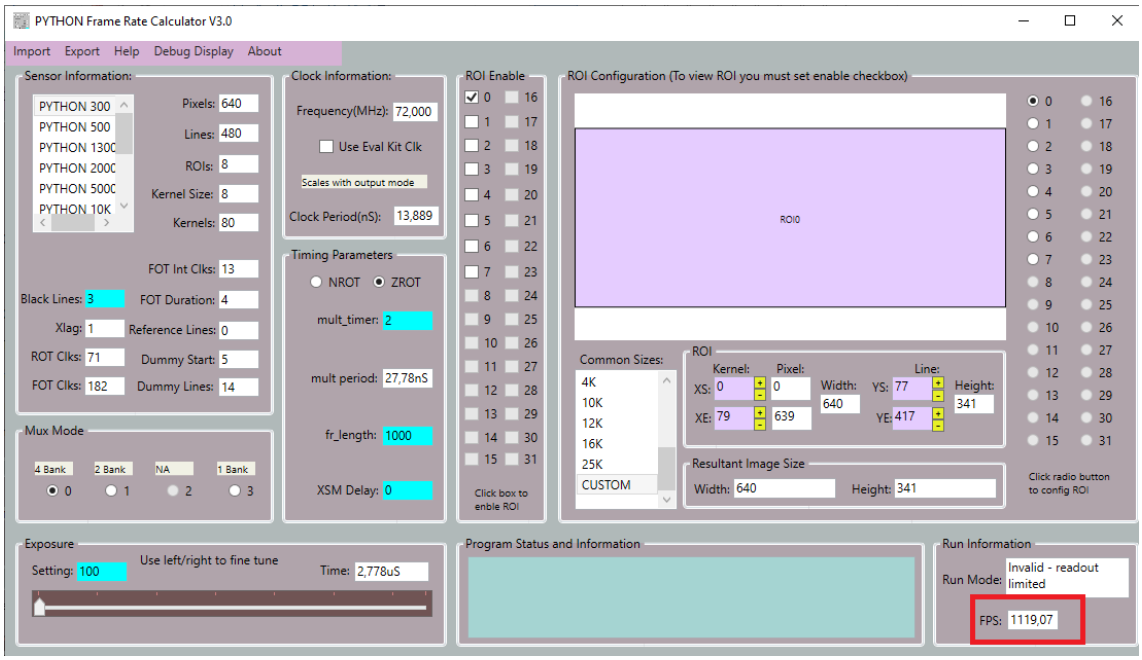


Figure 2 Python Frame Rate Calculator tool frame rate result

As It can be seen, frame rate can be over 1000fps with a possible ROI configuration and ZROT is enabled. Four or two LVDS lanes can be used as data output at 720Mbps. It can be found most of the mainstream suppliers.

5.1.4 Sensor Selection

Table 3 Sensor properties

	Max Resolution	Max FPS	ROI
IMX477	12MP	720	YES
LUX1310	3MP	1070	YES
PYTHON 300	0.3MP	815	YES

Python 300 image sensor is chosen because of its availability on mainstream suppliers and availability of design resources. It has all necessary features. At full resolution frame rate does not match with the specifications but with using ROI feature, frame rate can go up and beyond 1000fps.

5.2 Image Acquisition System Design Structure Decision

The device that is responsible for receiving image data from the sensor and transferring the data to image processing system without losing information. The system needs to do multiple tasks simultaneously. Because of incoming high-speed information, usage of memory is necessary for buffering. Also, system can be designed flexible for testing different camera options with different interfaces and different interfaces for interfacing the image processing system. There are three main approaches for interfacing the image sensor and neighbouring system.

- CPU (Central Processor Unit) based device
- GPU (Graphics Processor Unit) based device
- FPGA (Field Programmable Gate Array) based device

While the main task for the camera prototype is interfacing the image sensor and transferring the image data to image processing system, it would be more compact if all tasks can be done in one system. While choosing a structure this approach is considered.

5.2.1 CPU Based Approach

There are many kinds of off-the-shelf Single-Board-Computer (SBC) platforms. This wide variety offers wide range of memory sizes, processor speeds and interfaces. Also, image processing system can be built on an SBC which is compact and different applications can be easily developed in. This makes fewer components and less space taken in the system. But processor-based system has disadvantage of doing parallel tasks and flexibility on interfaces. As experienced on Raspberry-PI experiment, standard camera for raspberry PI has closed sources and there are no sources for registry map of IMX477. There are two MIPI CSI-2 lanes for camera interface and a custom camera approach would have to be in this limitation.

5.2.2 GPU Based Approach

There are GPU based embedded modules which provides mobility and low power requirements. Those modules have cores that can make high performance computations simultaneously. There are GPU based modules released by NVIDIA called Jetson modules. These modules have large number of CUDA cores which are computation units

with parallel computation ability and modules are equipped with ARM processors, fixed interfaces and running an operating system. [14]

This approach will provide fast image processing platform. But interfaces are not flexible and high-end modules cost more.

5.2.3 FPGA Based Approach

FPGAs (Field Programmable Gate Array) are integrated circuits that can be programmable on field with hardware description language (HDL). FPGAs consist of logic blocks which can be configured and wired as required. FPGAs can be configured for complex combinational tasks. [15]

An FPGA is suitable for doing multiple tasks simultaneously, ability to be configured with different interfaces and its high processing speed.

6 Decided System Structure

Initially FPGA is decided for implementing the system. By using FPGA, designed system will be more flexible and adaptable to modifications result of tests. For finished product, cost of the device will be less. After tests and performance results, device can be scaled up depending on performance needs and can be optimally chosen balancing cost and performance needs. FPGAs are considered from both big FPGA manufacturers, Xilinx and Altera. After considering implementation of image processing on FPGA and implementation of application processor on same FPGA to achieve single system for everything, large scale FPGAs are investigated. Large scale FPGAs are proved to be cost too much. This leads to System on Chips which consist of FPGA and application processor is put together in a single chip.

There are other projects with similar aspects exist. OpenCV based road sign recognition application implemented Zynq-7020 SoC. In this project image data is taken with resolution of 1920x1080 at 72fps. Images are pre-processed in PL system and transferred to the processing system. [16]. Another project is real time traffic sign recognition implemented on Zynq-7000. System processes images 40x40 resolution images in about

100 milliseconds. Another very similar application with this project is getting high framerate (above 1000fps) video capture from camera for microscope. [17]

Zynq SoC (System on Chip) modules comprises processor units and FPGA units together. This will provide system to have flexibility of FPGA and an application layer can be implemented in the processor unit. Xilinx has widely used Zynq SoCs comprises ARM based processor unit and FPGA unit together. This will provide parallel processing, flexible interfaces, and application layer in one chip.

For easier and quick design and prototyping, Picozed SoM (System-on-module) is selected. Picozed has Xilinx system-on-chip, XC7Z020-1CLG400 on it. XC7Z020-1CLG400 has dual-core ARM Cortex A9 MPCore which can run up to 866Mhz and Artix 7 programmable logic is embedded together. Memory and eMMC is also populated on Picozed. Using Picozed will make the design less complicated and faster.

Since there is enough RAM and eMMC memory for the data to store and process after image acquisition and, data analysing can be done with the SoM. So, system can be a standalone application. System interfaces are mostly targeted for external image processing as they are designed with fast interfaces.

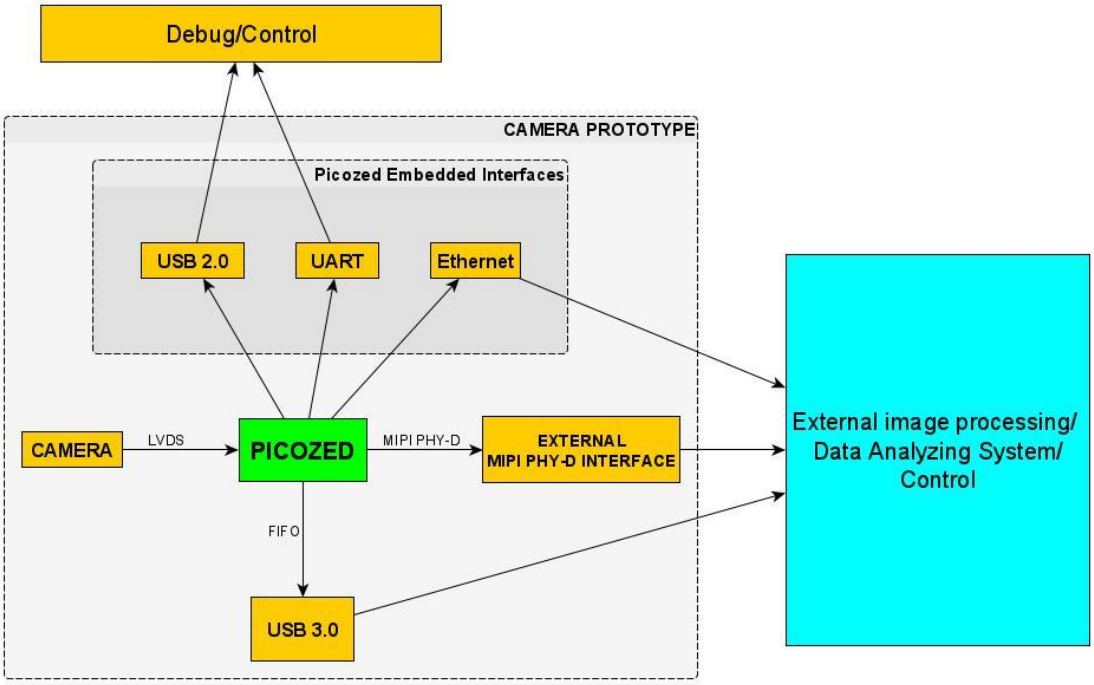


Figure 3 Determined System Structure

For ethernet, USB 3.0 possible external systems are,

- External image processing
- Device control and settings
- Live image output

For MIPI CSI-2 it is same except device control functionality.

UART and USB 2.0 interfaces can only be used for debugging, control, and settings.

7 Hardware Design

Camera board is decided to be a separate device to make the system more modular. Different camera boards can be designed and tested with the system easily by simply connecting with a FPC cable without designing whole system. This way, if it is decided to use another image sensor, it can be implemented with ease. Separate camera board also will make it easier to mount the camera on a lens setup more easily. Because small camera board will fit in small opening in a setup and will not disrupt any possible moving part. For interfacing camera board and image processing or control system, a carrier board for Picozed with necessary interfaces needs to be designed. As a result, there are two boards needs to be designed.

- Camera Board.

- Picozed Carrier Board (Image acquisition board)

Camera board to image acquisition board connection need to be designed with high-speed compatible connectors and cables which are supports LVDS standard.

The carrier board utilizes all the Picozed interfaces embedded in the SoM. Those are gigabit ethernet, UART, USB 2.0 and SDIO. Picozed can be bootable from SD-CARD or JTAG. Board size is determined to make the components placed easily, and high-speed tracks have enough space not to interfere with each other. So, board is not designed to be the smallest board as possible, but it is made prioritizing functionality and fast design.

7.1 Used Key Technologies

7.1.1 Zynq 7000 System-on-Chip

Zynq-7000 consist of single or dual core ARM Cortex A9 processing system (PS) and Xilinx programmable logic in single chip. Processing system has peripheral connectivity interfaces, memory interface and on-chip memory. Connection between PS and PL is established using AXI (Advanced Extensible Interface) based connection. [18] In this project Picozed SoM is used which has XC7Z020-1CLG400 SoC with necessary core powers 1GB of memory, 8GB of eMMC flash memory and some peripheral ICs are populated. [19]

7.1.2 LVDS (Low Voltage Differential Signal)

Latest applications require high-speed reliable transmissions between peripherals. [20] LVDS is low voltage, high speed communication technique based on standard TIA/EIA-644. It has very small differential swing which is about 350mV with a typical off-set voltage of 1.25V. LVDS driver works as fast switching current source. Logic level is decided with direction of the current. Differential pair tracks have current flowing opposite ways. This provides better EMI protection. Constant current creates voltage on 100ohm termination resistance. Since any noise is coupled both tightly coupled tracks, and it is only considered difference of the signals, common mode noise will be eliminated. Because of low voltage, current consumption is very low. [21]

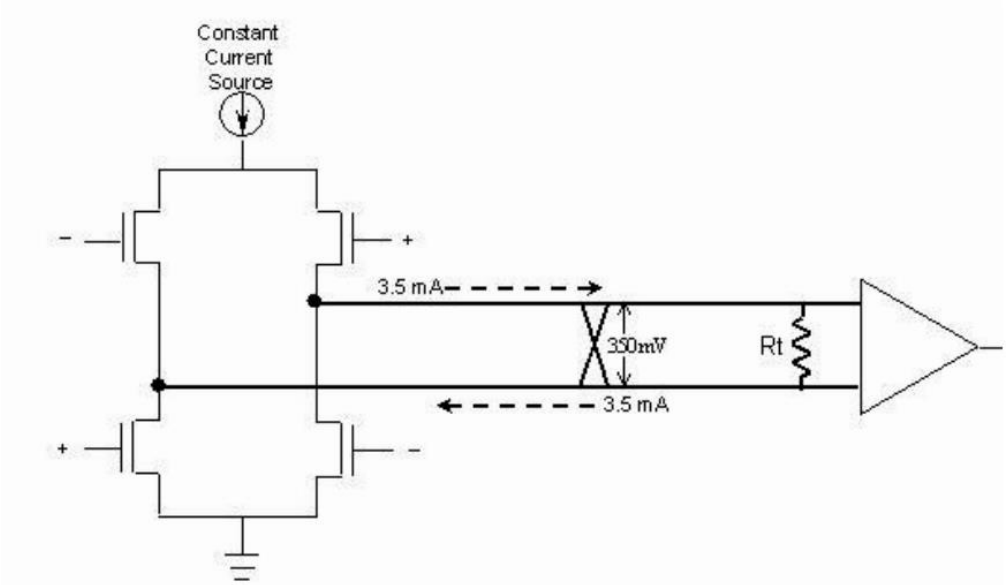


Figure 4 LVDS drivers, receiver working principle [20]

7.1.3 MIPI CSI-2 D-PHY

D-PHY mainly developed for camera and display applications. It consists of low power signalling for control and high-speed lanes for data. A clock and data line pairs makes basic D-PHY connection. D-PHY works with master and slave devices. Clock signal unidirectional and direction is master to slave. Data signals can be unidirectional or bidirectional. When high-speed mode, line pairs act differential with low-swing and when low power mode each line act as single ended. [22] RPI 4 has 2 data lanes and a clock lane accompanied by I2C for control.

7.1.4 USB 3.0

With increase of speed on computers and need for more bandwidth on peripherals with used with computers new USB versions are developed. USB 3.2 has speed up to 2GB/s, with the use of two super speed lanes consist of two wires each with the enhanced data encoding efficiency. USB 3.2 has one low speed differential lane which has backwards compatibility and two high-speed differential lanes. [23]

7.1.5 Gigabit Ethernet

Gigabit ethernet is defined in IEEE 802.3-2018 standard. It specifies speeds from 1 Mb/s to 400 Gb/s using half-duplex and full-duplex communication over common MAC (Media Access Control) protocol. Physical layer can be coaxial, fiber optic or twisted pair cables or electrical backplanes. [24] 1000BASE-T is defined in IEEE 802.3ab-1999 and

it is sub layer of gigabit ethernet. It defines gigabit ethernet over copper wiring. Only two pairs are used for negotiation and link is made automatically, no need to use crossover cables. [25]

7.2 Implementation

7.2.1 Picozed 7020 Carrier Board Design

Picozed 7020 SoM has 3 micro connectors for interfacing a carrier board. Matching receptacles are placed on carrier board. Picozed have already have peripheral ICs already placed for gigabit ethernet and USB 2.0. Necessary PS interfaces, UART and SDIO are routed out from Picozed. JTAG connector is placed and necessary connection are made.

7.2.1.1 Power Supply Design

Input voltage is chosen 12V which is a standard for off-the-shelf adapters. Maximum voltage is chosen as 14V and minimum voltage is chosen as 10V. There are multiple voltages that needs to be fed to Picozed SoM. Bank voltage inputs are for setting voltage level for the banks of the XC7Z020-1CLG400 SoC. PL banks that need to be supplied from carrier board are bank 13, bank 34, bank 35. PS banks, bank 500 and bank 501 are supplied in Picozed SoM with 1.8 Volts. Main Picozed voltage is 5V that supplies regulators for core, memory, and some bank voltages. PL pins needs to be supplied with 2.5V to be able to work as LVDS IOs. NOIP1SN0300A image sensor requires 3.3V level, control and status and SPI pins. [26] So if one of the banks are supplied with 3.3V, a voltage level translator can be avoidable. Sensor LVDS IOs are connected to bank 34 of the SoC. For LVDS functionality bank 34 is supplied with 2.5V. FT600-Q supplied with 3.3V and its IO voltages can have voltages 1.8V, 2.5V and 3.3V. [27] The additional clock generator is connected to bank 13 differential MRCC and single ended SRCC ports. Because of that bank 13 needs to be supplied with 2.5V.

Table 4 SoC bank voltages

BANK	VOLTAGE	VOLTAGE SOURCE
BANK 13	2.5V	Carrier board
BANK 34	2.5V	Carrier board
BANK 35	3.3V	Carrier board

BANK 500	1.8V	Picozed
BANK 501	1.8V	Picozed

Table 5 Peripheral voltages

Peripheral	Component	voltage
USB 3.0 supply	FT600-Q	3.3V
USB 3.0 IO	FT600-Q	3.3V
MIPI CSI-2	MT20002	1.2V
Picozed main supply	Picozed SoM	5V
Picozed bank 13	Picozed SoM	2.5V
Picozed bank 34	Picozed SoM	2.5V
Picozed bank 35	Picozed SoM	3.3V
SDIO logic level	-	3.3V
UART logic level	-	3.3V

7.2.1.1.1 Power Input

For plugging external power supply optional two connectors are placed. There are several electrolytic capacitors for preventing voltage fluctuations result of a current spike. Common mode choke is placed to prevent switching devices generate conducted electromagnetic interference. [28] Also for reverse voltage protection a Schottky diode is placed after common-mode choke. An on-off slide switch is used for switching power on and off.

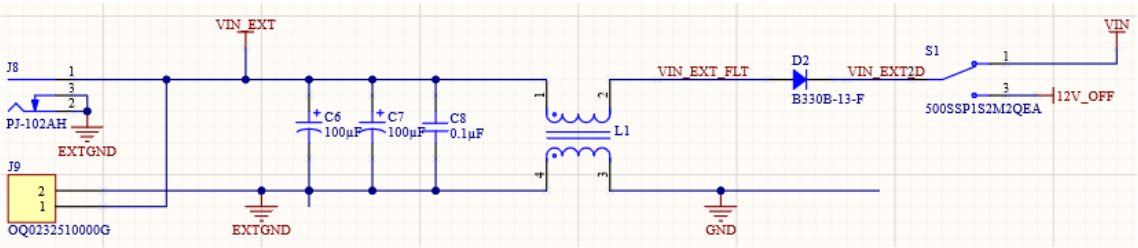


Figure 5 Power input circuit

7.2.1.1.2 Main Power Supply

Output voltage is set to 5V trough feedback resistors which are connected to the VSENSE pin. The resistors have 1% tolerance for getting accurate and stable output. Output voltage is calculated using this formula

$$R_t = \frac{V_o - V_{ref}}{V_{ref}} R_b$$

Where V_{ref} is 0.6V. From this R_t is determined as 16.2Kohms and R_b is determined as 2.21Kohms.

Inductor is selected using formula in datasheet of TPS54821RHLR.

$$L = \frac{V_{inmax} - V_{out}}{I_o . K_{ind}} . \frac{V_{out}}{V_{inmax} . f_{sw}}$$

$$L = \frac{14 - 5}{8x0.3} . \frac{5}{14x600000} = 2{,}232uH$$

Ripple current is calculated as below.

$$I_{ripple} = \frac{V_{inmax} - V_{out}}{L} . \frac{V_{out}}{V_{inmax} . f_{sw}}$$

$$I_{ripple} = \frac{14 - 5}{2.232} . \frac{5}{14x600000} = 2.4A$$

RMS current is calculated as follows.

$$ILrms = \sqrt{I_o^2 + \frac{1}{12}\left(\frac{V_o(V_{inmax} - V_o)}{V_{inmax} L_1 f_{sw}}\right)^2}$$

$$ILrms = \sqrt{8^2 + \frac{1}{12}\left(\frac{5(14 - 5)}{14x2.3x10^{-6}x6x10^5}\right)^2}$$

$$ILrms = 8.02\ Ampers$$

Minimum inductor value for output inductor is calculated as 2.232uH. XAL7070-332MEB is chosen which is 3.3µH and rated 15.1 Ampers of DC (Direct Current) voltage. Output capacitor determines output ripple and response to current peaks.

$$C_o > \frac{2 . \Delta I_{out}}{f_{sw} . \Delta V_{out}}$$

Where ΔI_{out}, current change at the output and ΔV_{out} is allowable voltage change at the output. If as a worst-case scenario load response is specified as 5% and maximum current change as 3A then

$$C_o > \frac{2\ x\ 3}{600x10^3 .\ 5x0.05}$$

$$C_o > 40\mu F$$

As output capacitor 47µF is used. [29]

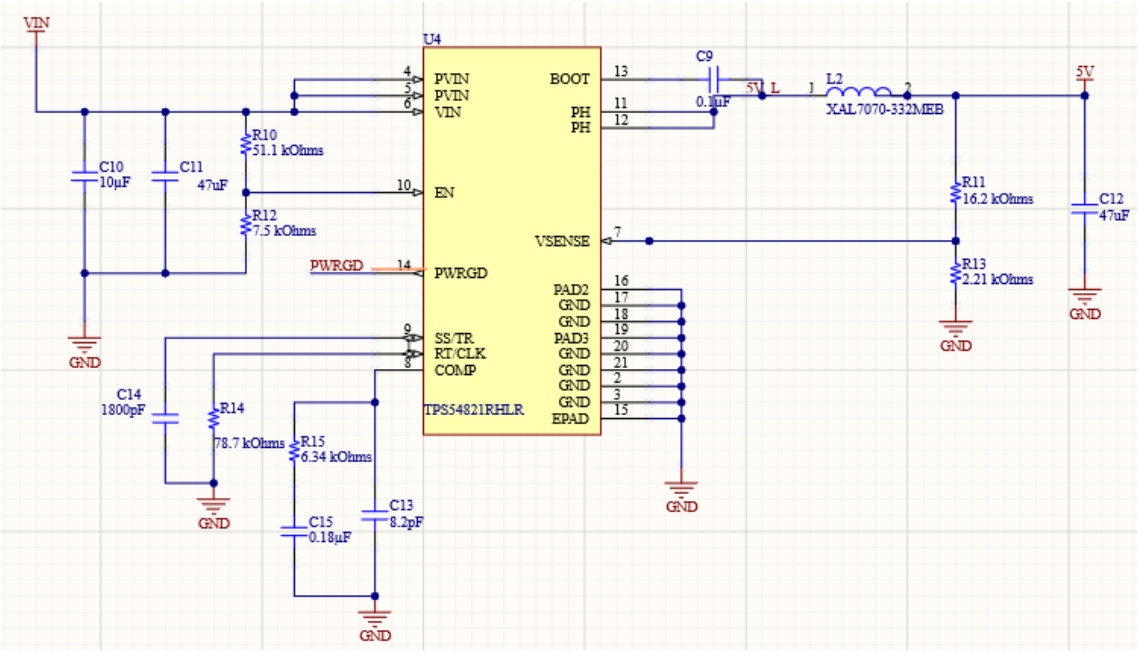


Figure 6 Supply circuit for 5V

7.2.1.1.3 Multiple Output Power Supply

For other voltages, an IC with multiple voltage outputs, ADP5052ACPZ-R7 is used. It has 4 switching outputs and one LDO (Low Dropout) output. Voltage distribution is made like in the table below.

Table 6 ADP5052ACPZ-R7 output voltages

Regulator Output	Signal Name	Voltage
Switching 1	VADJ	2.5V
Switching 2	3V3	3.3V
Switching 3	1V	1V
Switching 4	1V2	1.2V
LDO	1V8	1.8V

Design tool from Analog Devices is used for this design. Design tool is developed on Microsoft Excel. Required voltages and worst-case current values entered in the tool and schematic and layout are generated.

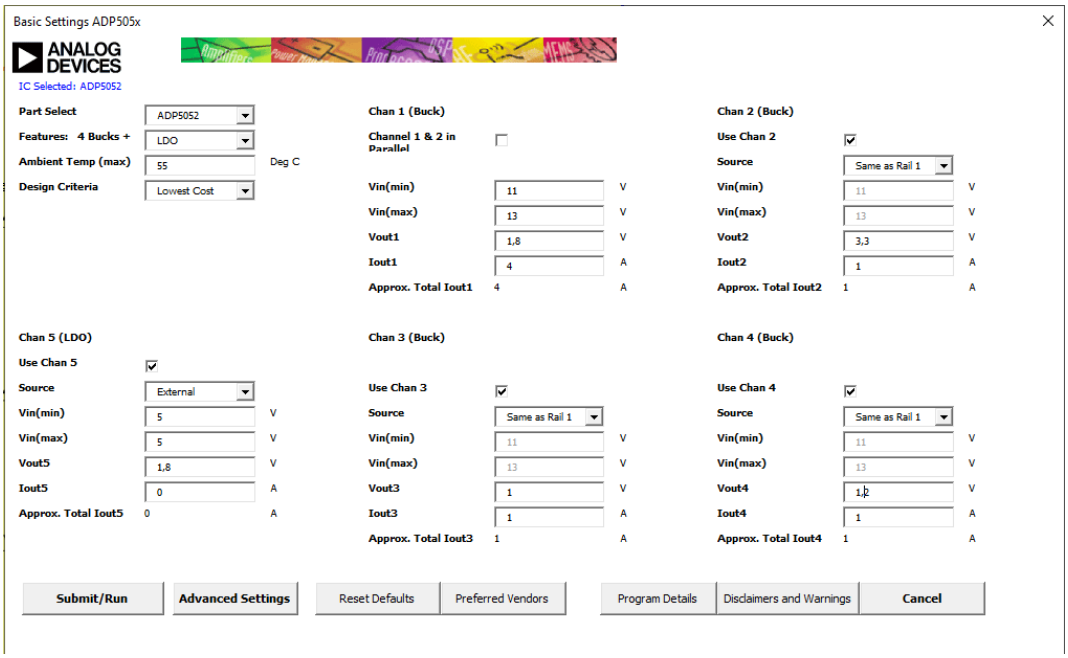


Figure 7 Design tool for ADP505x input screen for parameters

Regulator’s first output feedback is designed with a pin header jumper for adjusting first channel’s voltage between, 1.8V,2.5V and, 3.3V. Even though the bank voltages are determined, this will provide design decision and requirement changes more easily.

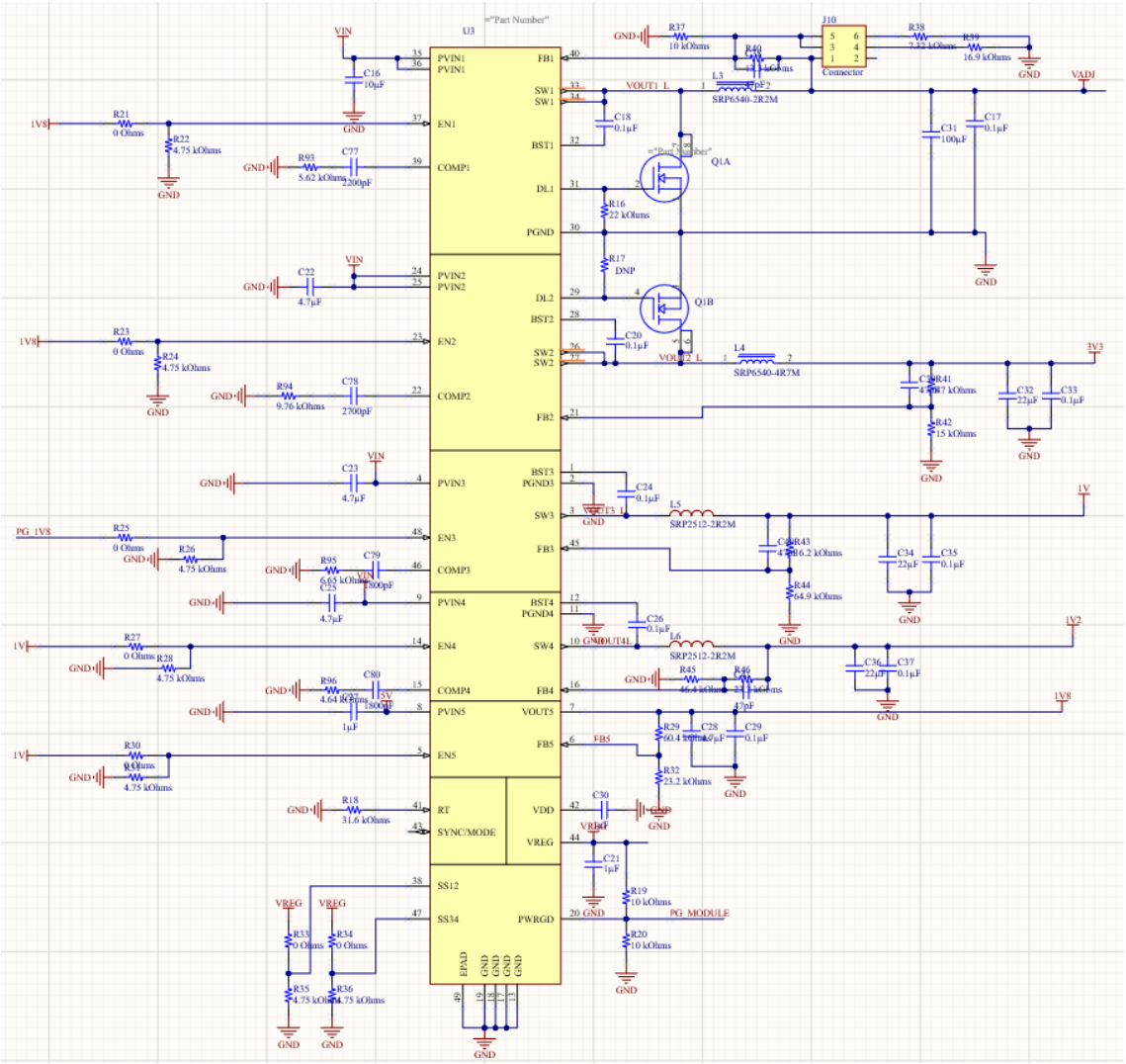


Figure 8 Multi voltage output voltage supply schematic

7.2.1.1.4 Power on Sequence

PWR_ENABLE pin is used for enabling power for the Picozed which is already pulled to VIN in Picozed. PWR_ENABLE is pulled down when device power switch, switched to off position. It is tied Before enabling bank voltages PG_1V8, indicating 1.8V supply on Picozed is on and stable, must be waited until it is high. According to this constraints, multiple voltage output enable pins are arranged. [30]

7.2.1.2 UART Interface

As suggested in Picozed schematic, PS_MIO48 is set as UART receive and PS_MIO49 pin is set as UART transmit pin. PS pins are connected to Bank 501 of the SoC which is supplied with 1.8V in Picozed. UART pins are level translated to 3.3V to be able to use standard UART-USB converter devices easily. Also, protection for voltages higher than 3.6V is added to schematic. For future design, USB-UART converter IC can be implemented instead of outputting 3.3V logic.

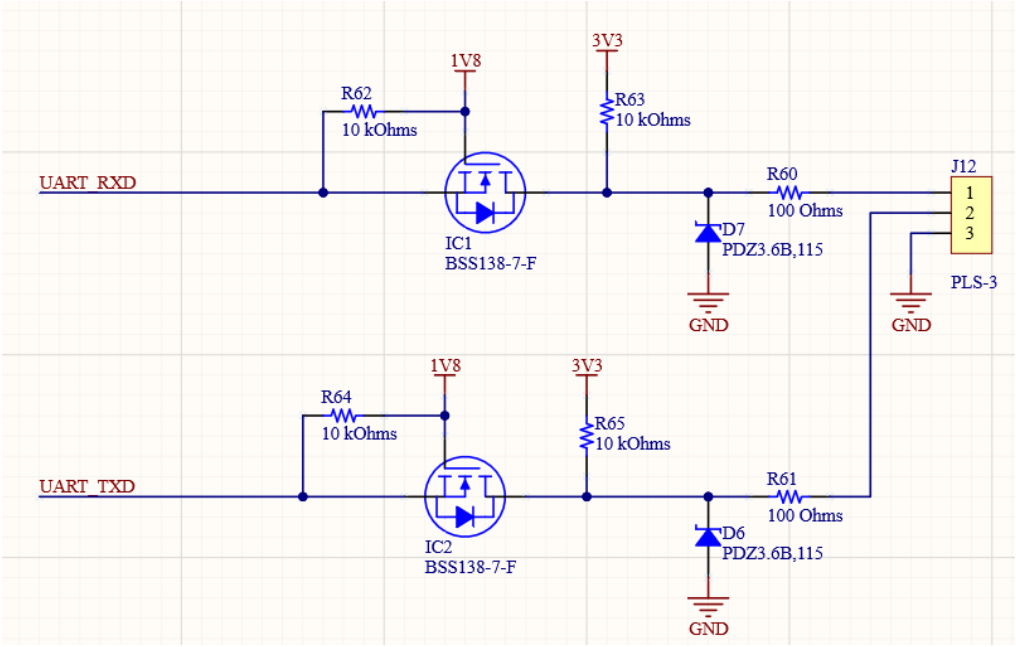


Figure 9 UART interface schematic

7.2.1.3 SD CARD Interface

SD-CARD interface must be connected to MIO pins 40 through 45 to be able to boot the SoC from SD CARD. [31] MIO pins 40 to 45 are connected to bank 501 which is supplied with 1.8V IO voltage. SD CARD works with 3.3V so a level translator IC specialized for SD CARDs (TXS02612RTWR) is used.

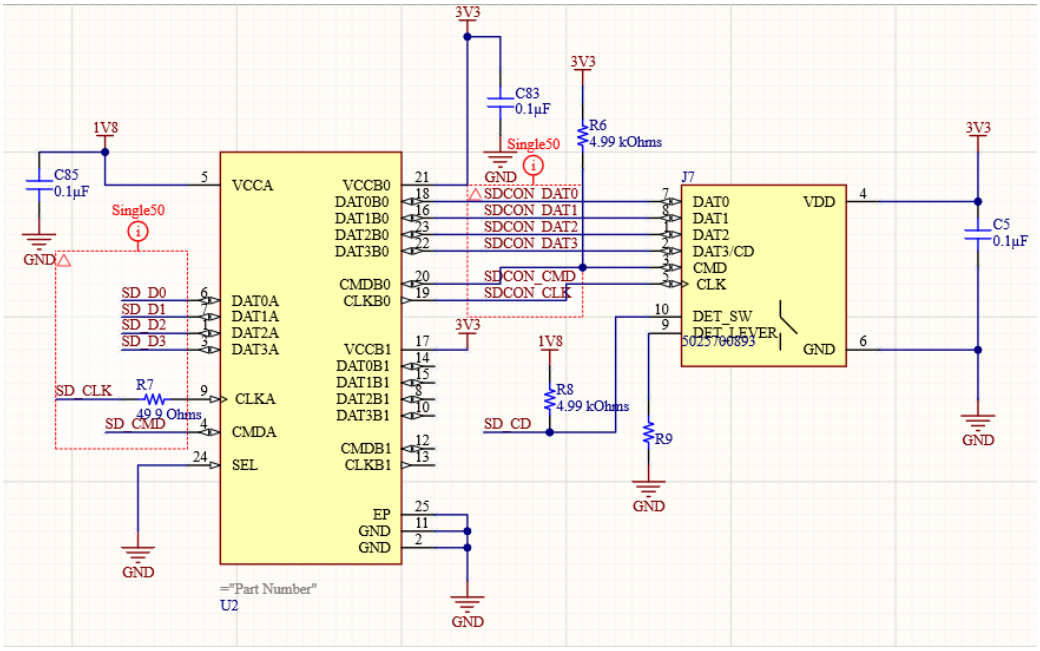


Figure 10 SD CARD interface schematic

7.2.1.4 USB 3.0 Interface Design

FT600-Q IC chosen for USB 3.0 interface. It is a USB 3.0 to 16 bits FIFO interface. FIFO voltage level is settable with VCCO pin. FIFO interface is connected to bank 35 of the SoC. Bank 35 is supplied with 3.3V so VCCO pin is connected to the bank 35 supply as well. [27] FIFO tracks on PCB should be 50 ohms and length matched. Clock track should be shorter than the FIFO data pins. USB 3.0 micro-B connector is chosen instead of Type-C connector considering simplicity and component count. USB 3.0 tracks which are connected to the USB 3.0 micro B connector needs to be 90 ohms differential impedance. [32]

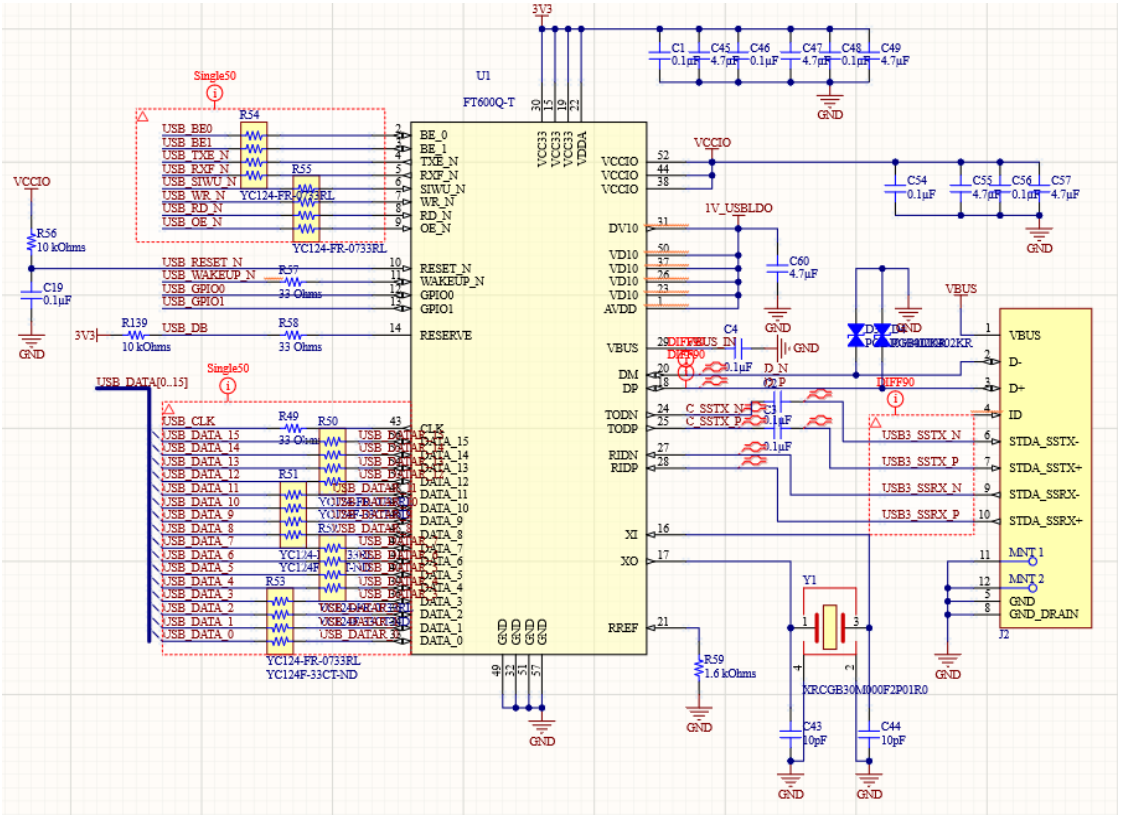


Figure 11 USB 3.0 design

ESD (Electrostatic Discharge) protection diodes are placed on high-speed and low-speed USB tracks to protect ICs.

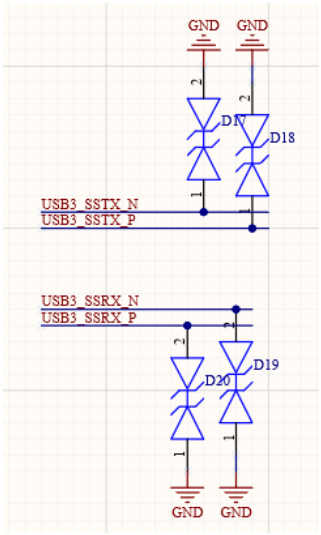


Figure 12 ESD protection for USB 3.0 interface

7.2.1.5 MIPI CSI-2 Interface Design

XC7Z020-1CLG400 pins can be used as D-PHY pins by using a specialized converter IC. MC20002 is used for converting Zynq 7000 HR signals to D-PHY signals. For each

D-PHY lane two pins are used for high-speed signalling, and two pins are used for low power signalling. I2C signals are routed from Picozed as well.

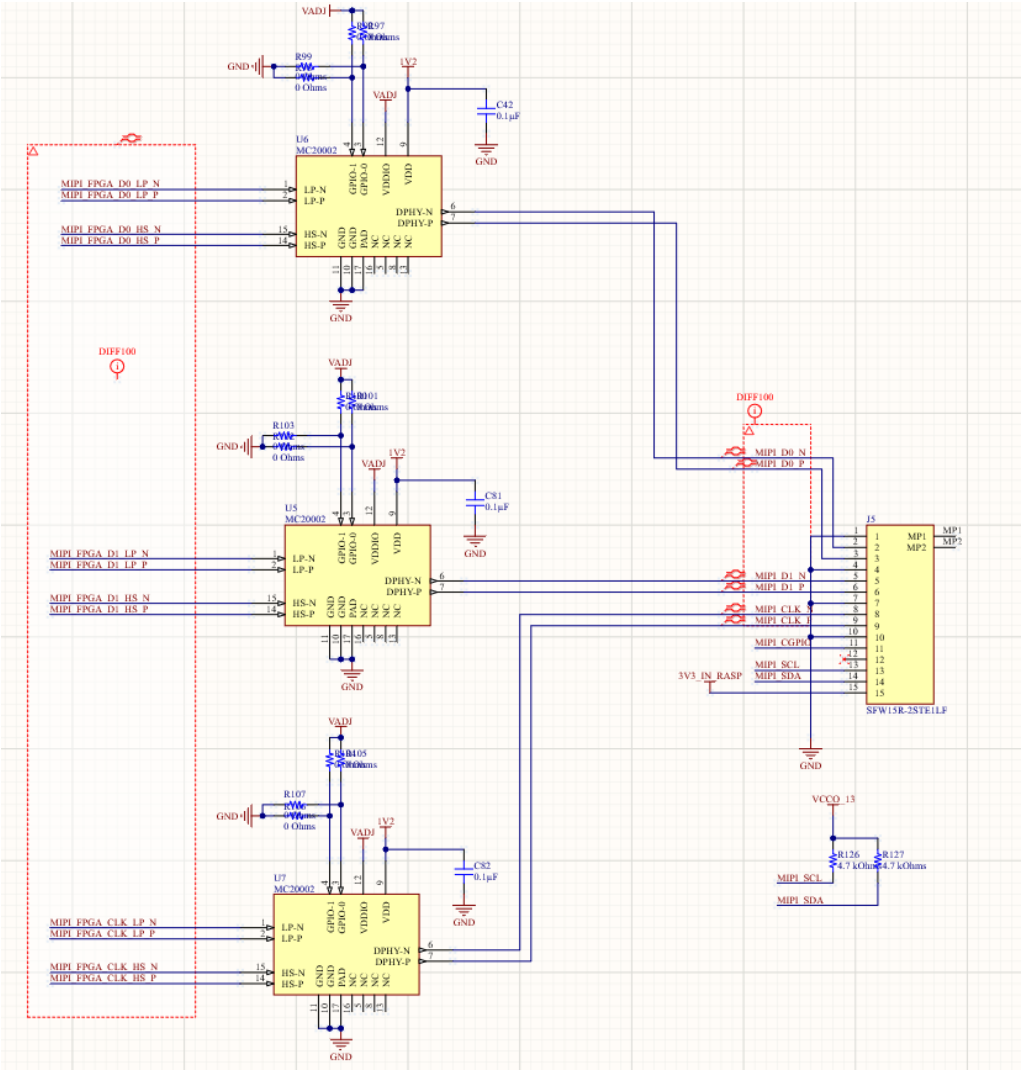


Figure 13 MIPI CSI D-PHY for interfacing Raspberry PI

7.2.1.6 Gigabit Ethernet Interface

Picozed already has gigabit ethernet physical layer IC is populated on it. On carrier board only gigabit ethernet connector needs to be placed. Molex modular connector with magnetics is chosen for this task. Embedded magnetics provide less space taken on PCB and less complicated design.

Link indicator LEDs (Led Emitting Diode) on Connector are connected through MOSFET circuit on Picozed, so anode of the LEDs connected to 3.3V and cathodes are connected to Picozed.

Data pins coming from connector are differential lanes with differential impedance of 100 ohms and they are length matched with tolerance of 0.635 mm.

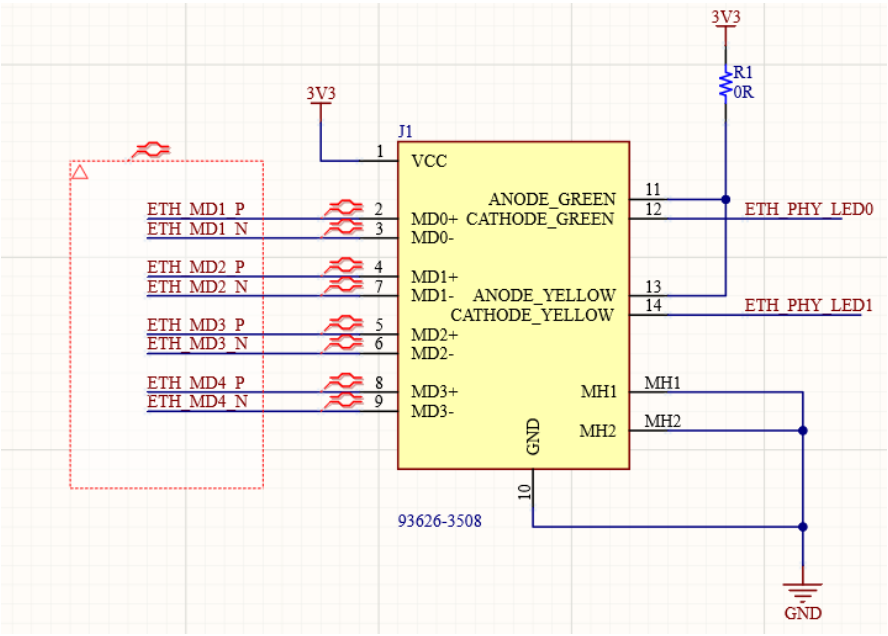


Figure 14 Gigabit ethernet connector schematic

7.2.1.7 Camera Interface

Eight LVDS lanes are routed from bank 34 of the Picozed SoM. The chosen camera has four LVDS lanes. The extra lanes are reserved for using different cameras with more data output. LVDS lanes are connected to the bank 34 which is supplied with suitable voltage for pins can work as LVDS IOs. Camera has SPI interface, control, and status IOs for controlling and getting triggers from camera. Those IOs are 3.3V voltage level so they are connected to bank 35 which is supplied with 3.3V. Also, camera supplies need to be enabled in specific order so, supply enable pins are routed to Picozed carrier board. LVDS lanes are routed with 100ohm differential impedance as specified in the standard.

For connection FPC connector 502244-3330 from MOLEX is used. 502244-3330 and matching FPC cable are LVDS compatible and has 100ohm differential impedance. Each connector pin has 0.4 Ampers of current capacity. 5V is connected to camera board through three pins which yields maximum 1.2 Ampers of current for the camera. This will be enough power to supply most of the different camera solutions.

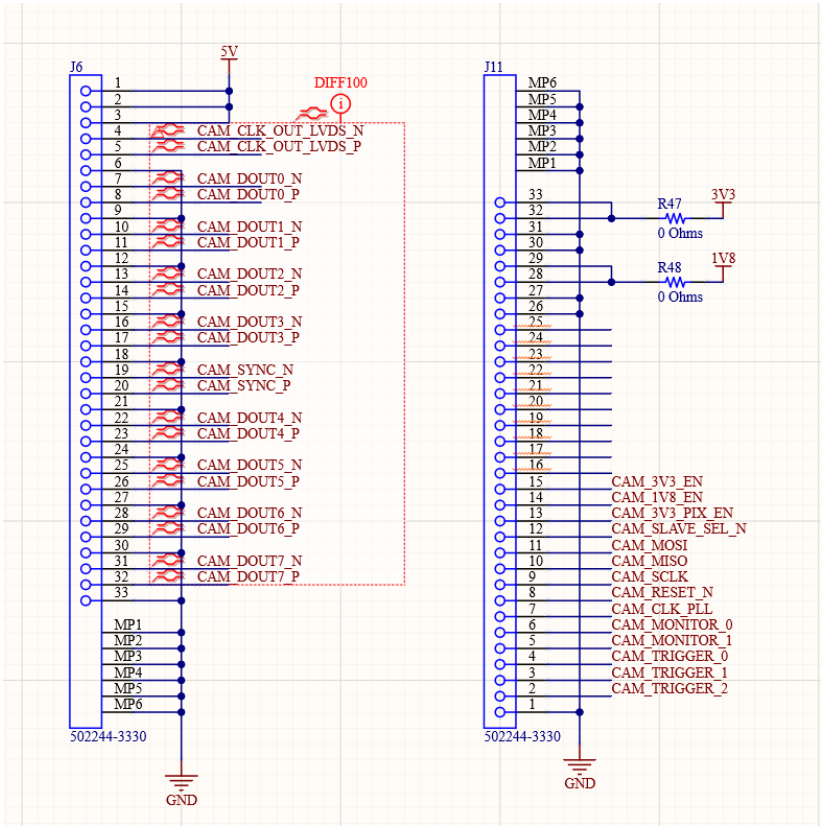


Figure 15 Camera LVDS interface connector schematic

7.2.1.8 USB 2.0 OTG Interface

Picozed has USB 2.0 interface routed out its micro header connectors. For optional extra interface for USB 2.0 is routed out on carrier board. OTG feature provides possibility of using device as both master and slave. The functionality of possible control, debugging for programming or connecting extra input/output device connection will be present on the carrier board.

OTG functionality requires sensing connected device is a master or a slave device and provide power according to that. Depending on if power exists VBUS pin, USB_VBUS_OTG pin is high or low and controller enables or disables TPS2051CDBVR power switch to switch power on and off.

Also, ESD protection is provided to USB differential lines using CDSOT23-SR208 TVS (Transient Voltage Suppressor) diode.

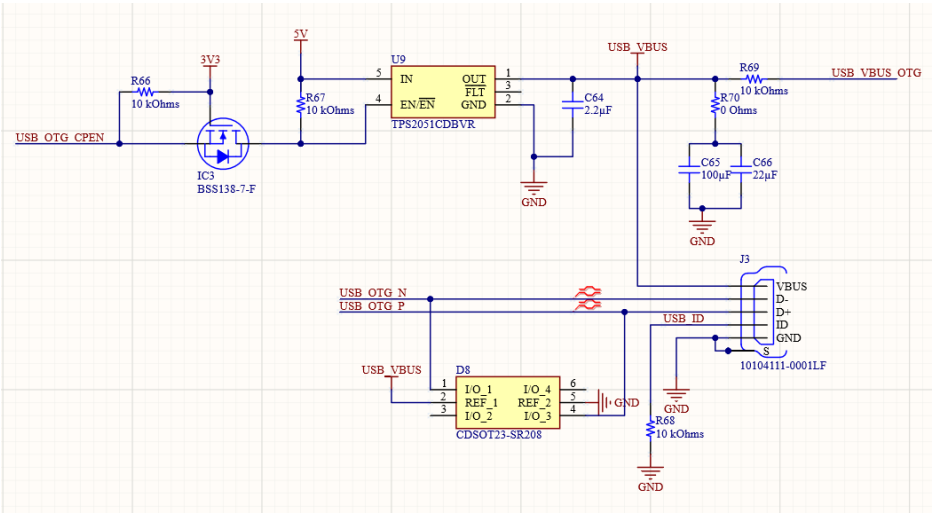


Figure 16 USB 2.0 interface

7.2.2 Camera Board Design

Python 300 image sensor (NOIP1SN300A or NOIP1SE0300A manufacturer part names) from On Semiconductor is used for imaging. Since Python 300 is pin compatible with the image sensors from Python family, it will provide more options on using image sensors without changing the design. There are image sensors in Python family which are monochrome, colour, different resolutions from 0.3 Megapixels to 1.3 Megapixels. Python 300 has 4 LVDS lanes for data accompanied with a clock and synchronization lane. Maximum data rate for LVDS is 720Mbps (Megabits-per-second). [26] Camera board is supplied with 5 volts coming from image acquisition board, necessary voltages for image sensor are produced in camera board. The voltages needed for the image sensor are not supplied directly from image acquisition board because voltage stability is important for the image sensor.

7.2.2.1 Image Sensor Supply

Camera needs three separate voltages to be supplied.

Table 7 Python 300 power pins

Pin	Description	Voltage
VDD_33	Supply voltage	3.3V
VDD_18	Supply voltage	1.8V
VDD_PIX	Pixel array supply	3.3V

VDD_PIX is pixel array voltage and need to be between 3.25V and 3.35V. For satisfying this voltage margin, pixel array voltage has its own regulator. Image sensor must be powered with specific sequence otherwise there might be high peak currents and device

may not power-on. [26] For 3.3V supplies NCP3335ADM330R2G and for 1.8V supply NCP3335ADM180R2G regulators are used. Regulators enable pins are routed to the connector to image acquisition board. So, power-on sequence will be handled by image acquisition board.

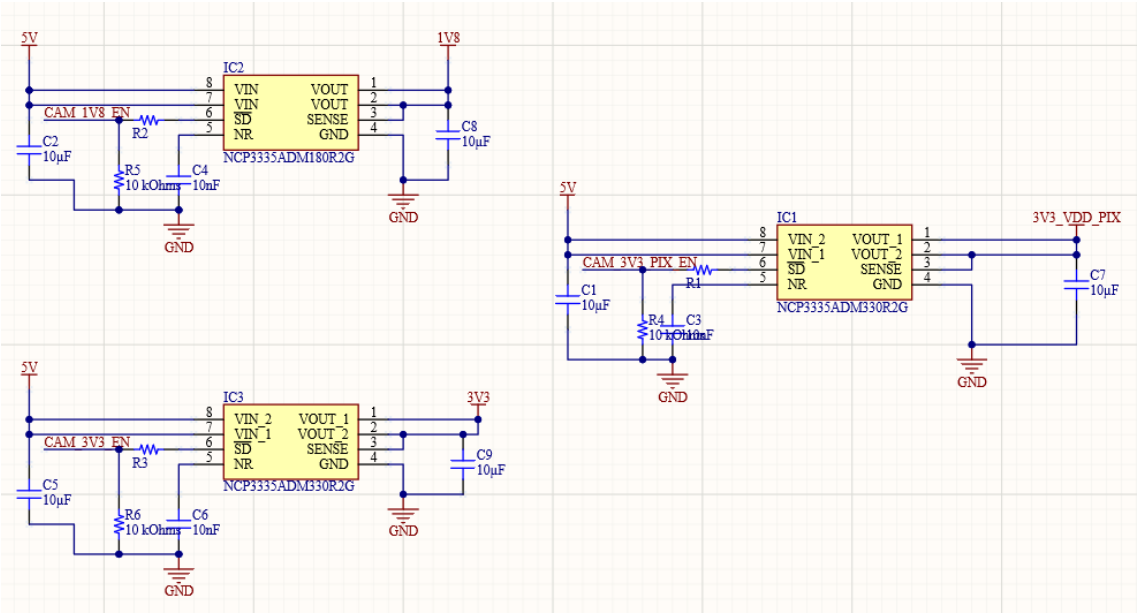


Figure 17 Power supply circuits for camera

7.2.2.2 Image Sensor Control Pins

There are several pins for controlling and getting instant feedback from image sensor. Trigger pins can be used for triggering integration. Trigger must be kept low during FOT (Frame overhead time) and monitor pin can be used getting feedback on this. [26] SLAVE_SEL_N pin is active low chip select pin. This pin used when there are multiple SPI devices connected parallel SPI pins are MOSI (Master Out Slave In), MISO (Master In Slave Out), SCLK (Serial Clock). All control pins' logic levels are 3.3V.

7.2.2.3 Image Sensor LVDS Interface

NOIP1SE0300A has four LVDS lanes with maximum data rate of 720Mbps. LVDS lines are populated to the FPC connector which is for interfacing image acquisition board. FPC connector is 502244-3330 from MOLEX which has 100ohm rated impedance and is suitable for LVDS standard with its matching FPC cables. Clock pins are connected to Zynq clock compatible LVDS lanes (MRCC) to be able use clock functionality.

7.2.2.4 Camera Board Lens Mount

There are two M2 screw holes with 2cm gap to use with most PCB lens holders.

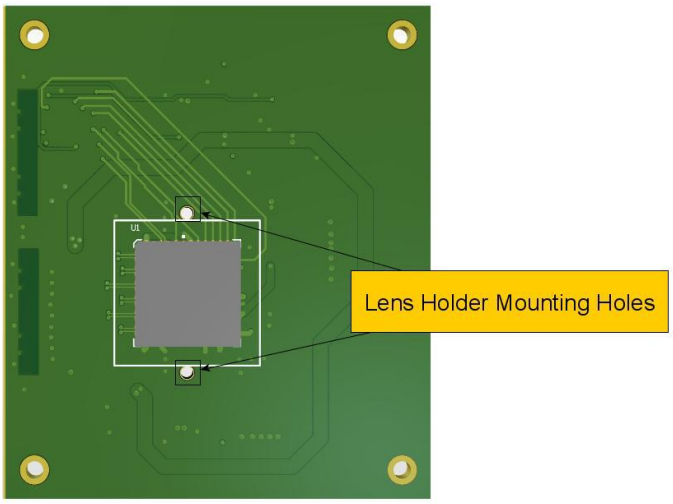


Figure 18 Lens holder mounting holes

There are no components populated to sensor side of the board except the sensor. So, any mounting option will have enough space to be placed. Other option determined for camera holder is CMR-M C-mount lens holder which can be fixed on the board using adhesive.

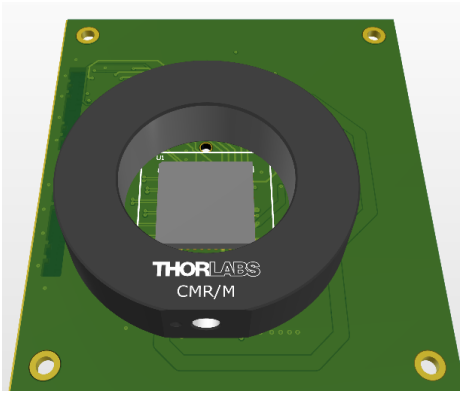


Figure 19 CMR-M lens holder on camera board

7.3 PCB Design Considerations

7.3.1 PCB Stack Up

Ground planes needs to be placed under top and bottom layers to provide necessary impedances on the impedance-controlled tracks. Eurocircuits is chosen for manufacturing the PCBs (Printed Circuit Board). Their Defined Impedance pool is used for stack-up of the PCBs. Defined impedance pool is a manufacturing standard, which multiple customers boards are produced with same specifications that are guaranteed impedance

properties. This makes boards cheaper. As PCB material, IS400 is used in this configuration.

For 6 layers and 4 layers boards stack-ups are like the tables follows.

Table 8 PCB stack up for image acquisition board properties (6 layers)

LAYER	TYPE	MATERIAL	THICKNESS (mm)	PERMITIVITY
Top Layer	Signal	Copper	0.018	-
Dielectric	PREPREG	PR2116	0.12	4.2
Inner Copper 1	PLANE (GND)	Copper	0.035	-
Dielectric	CORE	FR4	0.51	4.52
Inner Copper 2	Signal	Copper	0.035	-
Dielectric	PREPREG	PR1080	0.07	3.91
Dielectric	PREPREG	PR1080	0.07	3.91
Inner Layer 3	Signal	Copper	0.035	-
Dielectric	CORE	FR4	0.51	4.52
Inner Layer 4	PLANE (GND)	Copper	0.035	-
Dielectric	PREPREG	PR2116	0.12	4.2
Bottom Layer	Signal	Copper	0.018	-

Table 9 PCB stack up for camera board properties (4 layers)

LAYER	TYPE	MATERIAL	THICKNESS (mm)	PERMITIVITY

Top Layer	Signal	Copper	0.035	-
Dielectric	Prepreg	PR2116	0.119	4.2
Inner Copper 1	PLANE (GND)	Copper	0.035	-
Dielectric	CORE	FR4	0.119	4.7
Inner Coper 2	PLANE (GND)	Copper	0.035	-
Dielectric	Prepreg	PR2116	0.119	4.2
Bottom	Signal	Copper	0.035	-

Material values are taken from IS400 datasheet. [33]

7.3.2 Defined Impedances

Defined impedances must be referenced to adjacent power plane they are placed. On image acquisition board the under top and bottom signal layers are set as ground planes. This makes impedance-controlled tracks can only be placed on top and bottom layers. Track widths and gap between differential pairs are calculated using Eurocircuit's impedance calculating tool present in company web site. These values are more dependable than values coming from Altium calculator.

Table 10 Track dimensions for impedances on image acquisition board

Impedance	Width (mm)	Differential Gap
Single Ended 50ohm	0.184	-
Differential 100ohm	0.166	0.262
Differential 90ohm	0.184	0.193

Table 11 Track dimensions for impedances on camera board

Impedance	Width (mm)	Differential Gap

Differential 100ohm	0.166	0.262

7.3.3 Component Placement

Components are placed on top layer as much as possible. It is intended to make the board single sided to save cost on manufacturing. Very few components are placed bottom of the board. Most of them are decoupling capacitors. Decoupling capacitors need to be placed near power inputs of the ICs, due to lack of place they had to be placed on bottom. The components are placed so the tracks between them are as short as possible.

Power supplies are placed away from other components to make current paths away from other signals.

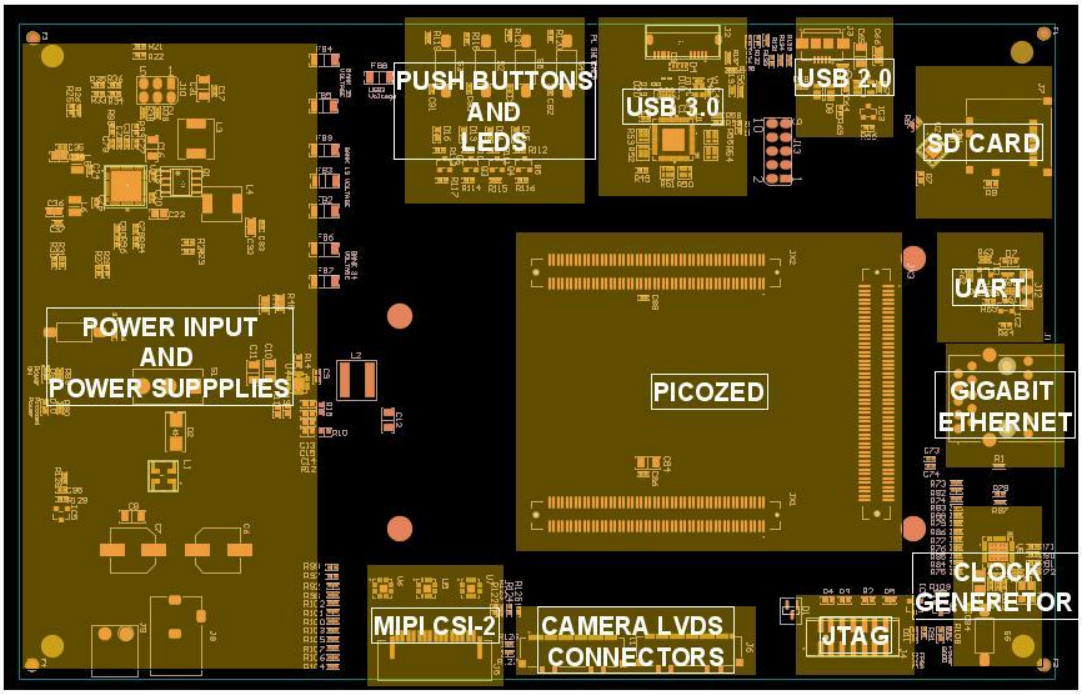


Figure 20 Component placement

7.3.4 Power Tracks

Power tracks places as wide as possible. Most of the time power planes are places as polygons and layer changes are made with multiple vias.

8 Final Device

Image acquisition board is designed as 190x210mm board.

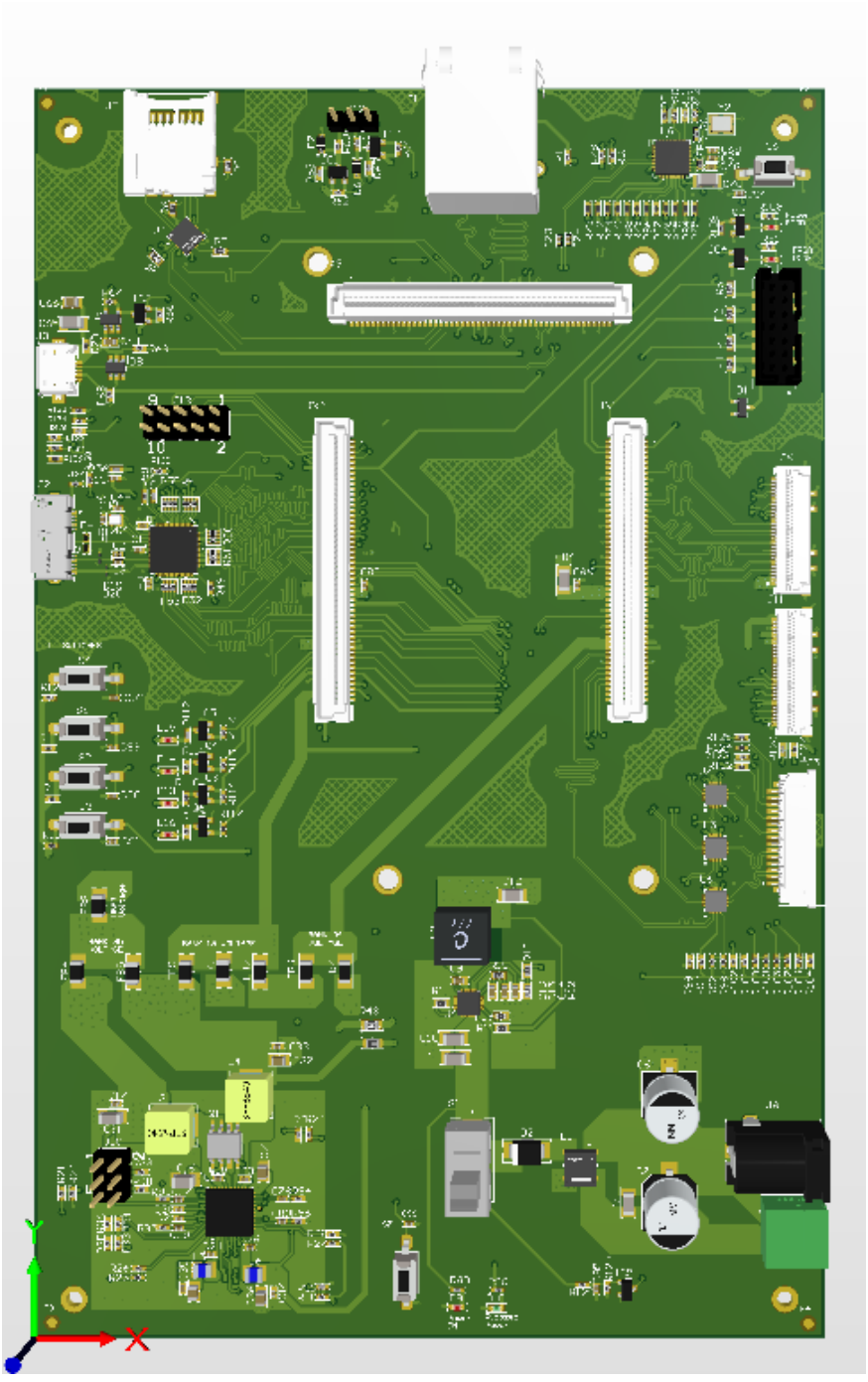


Figure 21 Image Acquisition board top view

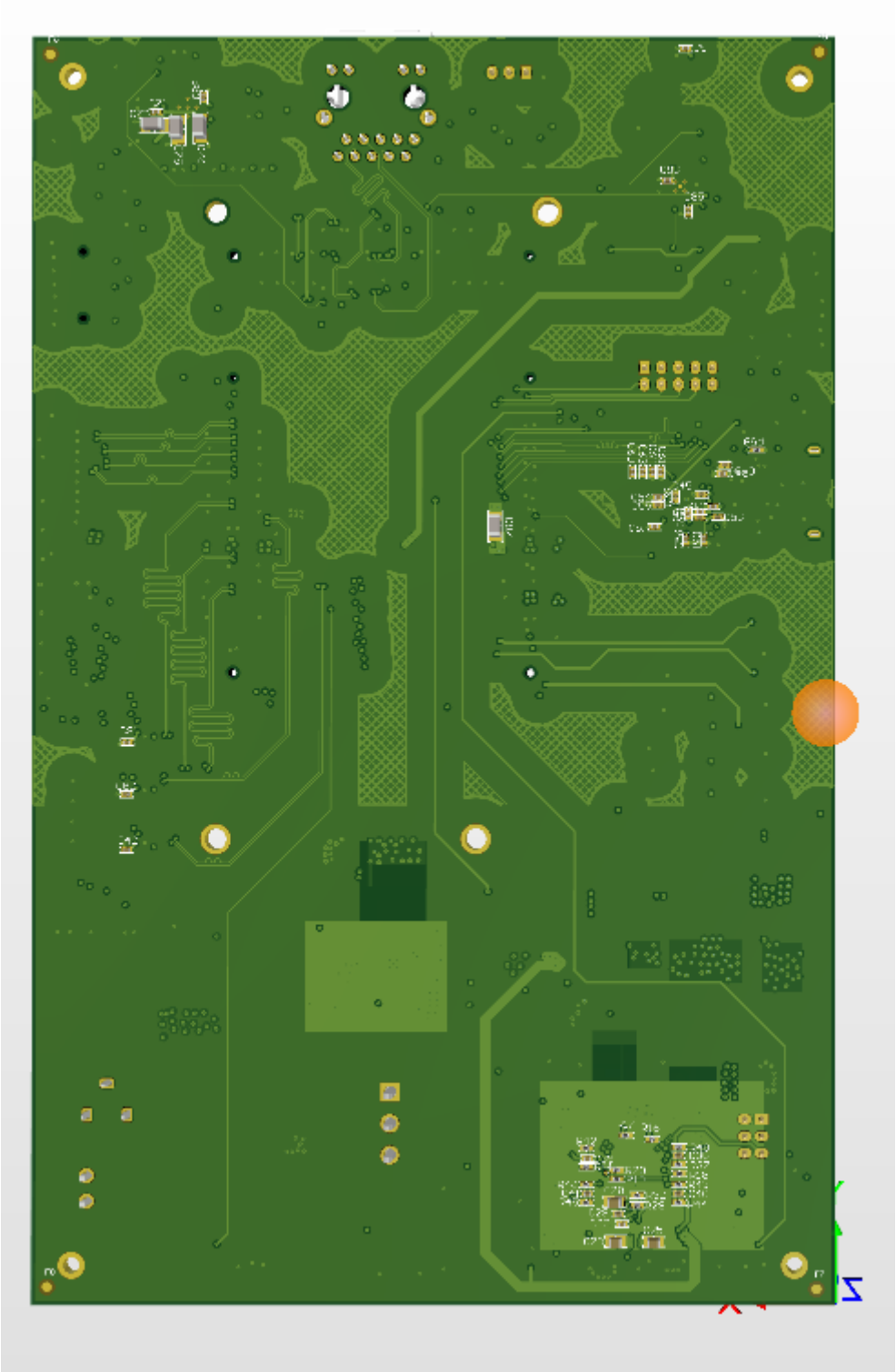


Figure 22 Image Acquisition board bottom view

Camera board is designed as 58.60x68 mm.

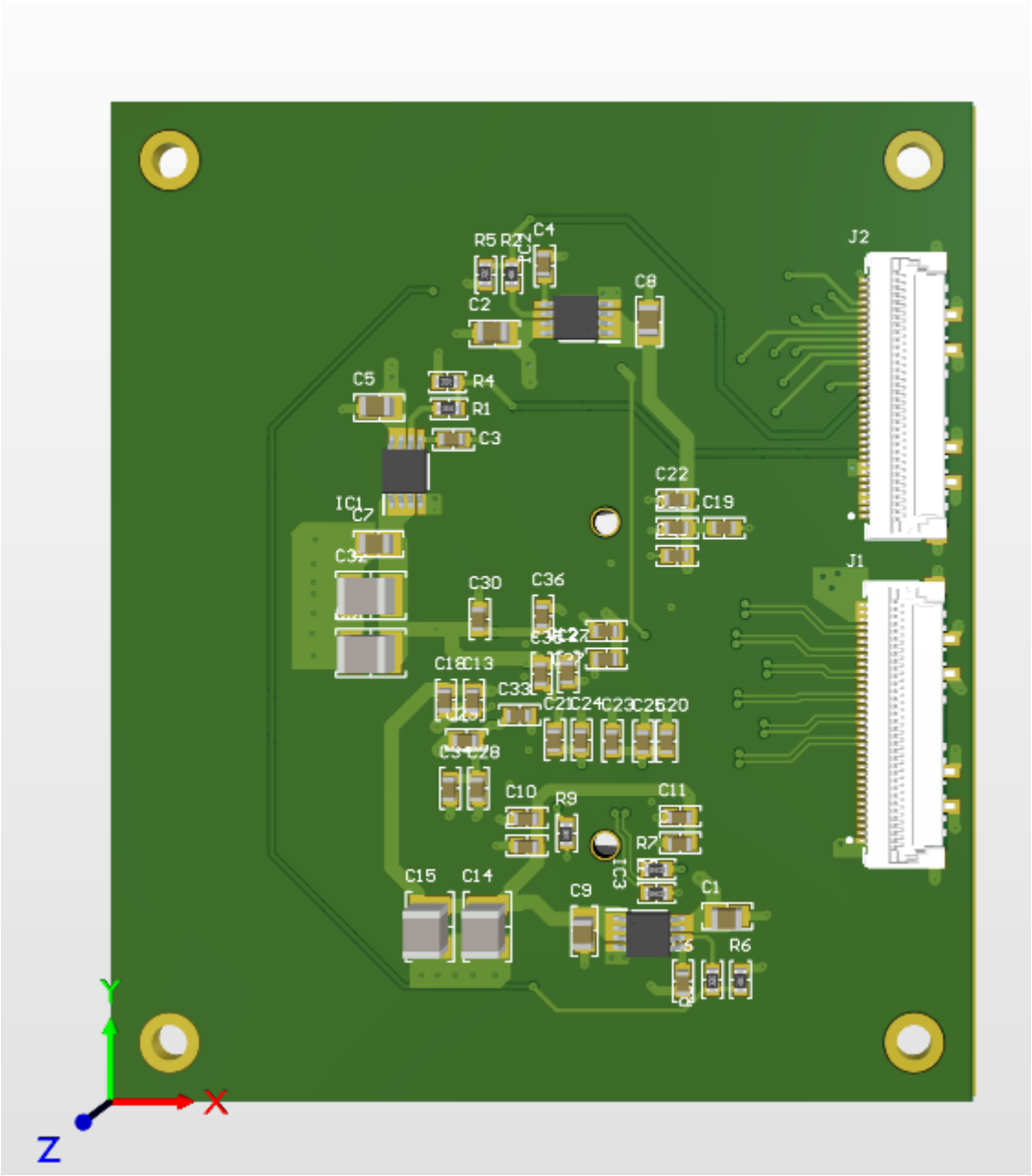


Figure 23 Camera board top view

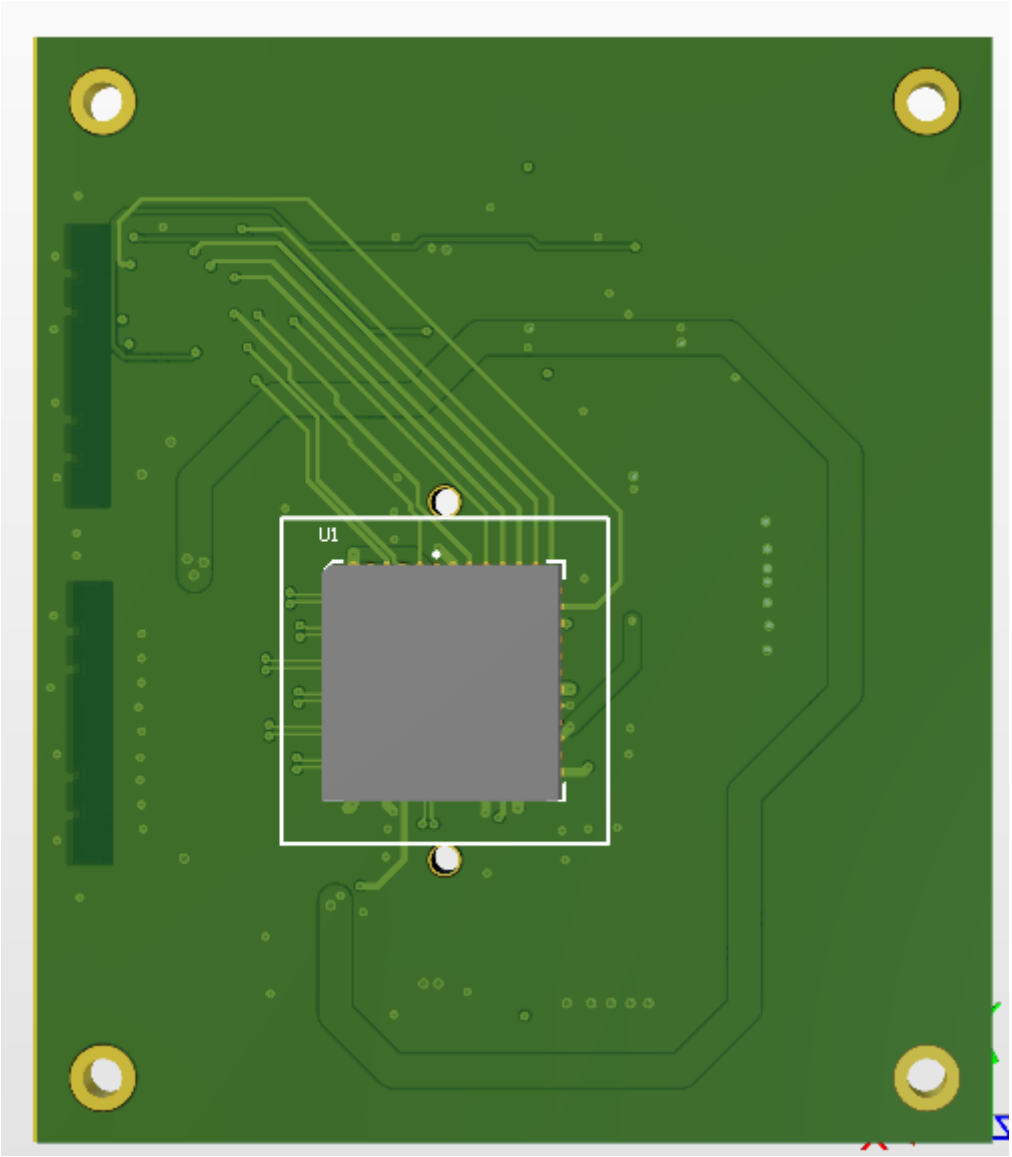


Figure 24 Camera board bottom view

9 Future Work

Driver codes needs to be written with full or enough functionality to test the device. After testing all necessary functionality, feature can be added to the system. First basic, and required features needs to be added like ability to gather footage at 1000 fps and transfer data one or more of its interfaces. If all tests are successful intended usage can be implemented step by step.

- Basic image processing like edge detection

- More advanced image processing detecting droplets, detect if they are luminous and track them as they are passing. Also, system could be able to have track of number of luminous droplets and other data related to analysis of the substance. Those features can be done either or both in the application processor and programmable logic part.

- Depending on requirements, analysis can be done in the application processor as well with necessary improvements like memory, and more powerful SoC if the current one is not enough.

- If all requirements successfully implemented on single device, then the features like user interface, remote connection, remote data collection to data base, screen and user-friendly input methods can be implemented on the device.

- After this point, device can be redesigned without using SoM, using SoC directly on the circuit with necessary interfaces making one step further to fully finished product.

- If it is seen that with unforeseen reasons everything cannot be implemented in single system then instead of SoC, simpler FPGA can be used, and data is processed in separate system.

10 Summary

Purpose of this thesis was developing a high frame-rate capable camera prototype. As a very early prototype, device is designed with different ideas to be tested. By examining similar products and given requirements device is designed with ambition of embedding all the processing capabilities in a single circuit.

With the given and determined requirements a camera with high-frame rate capability and expected extra features is designed. As a design choice image sensor and image data acquiring part designed separately as intention of mechanical advantages and modularity.

Image acquisition board is designed using Picozed SoM which is a SoC module with Xilinx Zynq SoC. SoM usage provided fast and less complicated design. Every possible interface which is embedded on SoM are routed out in the image acquisition board. These are Gigabit ethernet, USB 2.0 OTG, SDIO and UART. Also, as main design target USB 3.0 IC connectivity is provided for high-speed connectivity with other devices with intention of outputting high-speed video data. In the design, there are several places designed as some basic things can be changed without major altering on the board. All the power is provided from image acquisition board.

References

[1] "Lab-on-a-chip - Wikipedia." https://en.wikipedia.org/wiki/Lab-on-a-chip.

[2] "Bioanalyzer Instrument | Agilent." https://www.agilent.com/en/product/automated-electrophoresis/bioanalyzer-systems/bioanalyzer-instrument (accessed Oct. 18, 2020).

[3] "Cedex HiRes Analyzer Cell culture analyzer." https://custombiotech.roche.com/home/Product_Details/INS_2157.html (accessed Oct. 17, 2020).

[4] "LightCycler® 480 Instrument II." https://lifescience.roche.com/global_en/products/lightcycler14301-480-instrument-ii.html (accessed Oct. 17, 2020).

[5] C. L. Sotiropoulou, L. Voudouris, C. Gentsos, A. M. Demiris, N. Vassiliadis, and S. Nikolaidis, "Real-time machine vision FPGA implementation for microfluidic monitoring on lab-on-chips," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 2, pp. 268–277, 2014, doi: 10.1109/TBCAS.2013.2260338.

[6] Z. Wei, D. J. Lee, and B. E. Nelson, "FPGA-based real-time optical flow algorithm design and implementation," *J. Multimed.*, vol. 2, no. 5, pp. 38–45, 2007, doi: 10.4304/jmm.2.5.38-45.

[7] L. Voudouris, C. L. Sotiropoulou, N. Vassiliadis, A. Demiris, and S. Nikolaidis, "High-speed FPGA-based flow detection for microfluidic Lab-on-Chip," in *2012 20th Mediterranean Conference on Control and Automation, MED 2012 - Conference Proceedings*, 2012, pp. 1434–1439, doi: 10.1109/MED.2012.6265840.

[8] "Understanding Region of Interest — (RoI Pooling) | by Kemal Erdem (burnpiro) | Towards Data Science." https://towardsdatascience.com/understanding-region-of-interest-part-1-roi-pooling-e4f5dd65bb44 (accessed Dec. 04, 2020).

[9] T. Grob, "Implementation of a FPGA-based Interface to a High Speed Image Sensor," no. 2993, 2010.

[10] V. Wasson and B. Kaur, "Full reference image quality assessment from IQA Datasets: A review," *Proc. 2019 6th Int. Conf. Comput. Sustain. Glob. Dev. INDIACom 2019*, pp. 735–738, 2019.

[11] B. Veeramallu, C. Lavanyasusanna, and S. Sahitya, "Survey on an Image Quality Assessment Metric Based on Early Vision Features," no. 6, pp. 447–449, 2013.

[12] Sony, "Imx477-Aack," pp. 1–2, 2018.

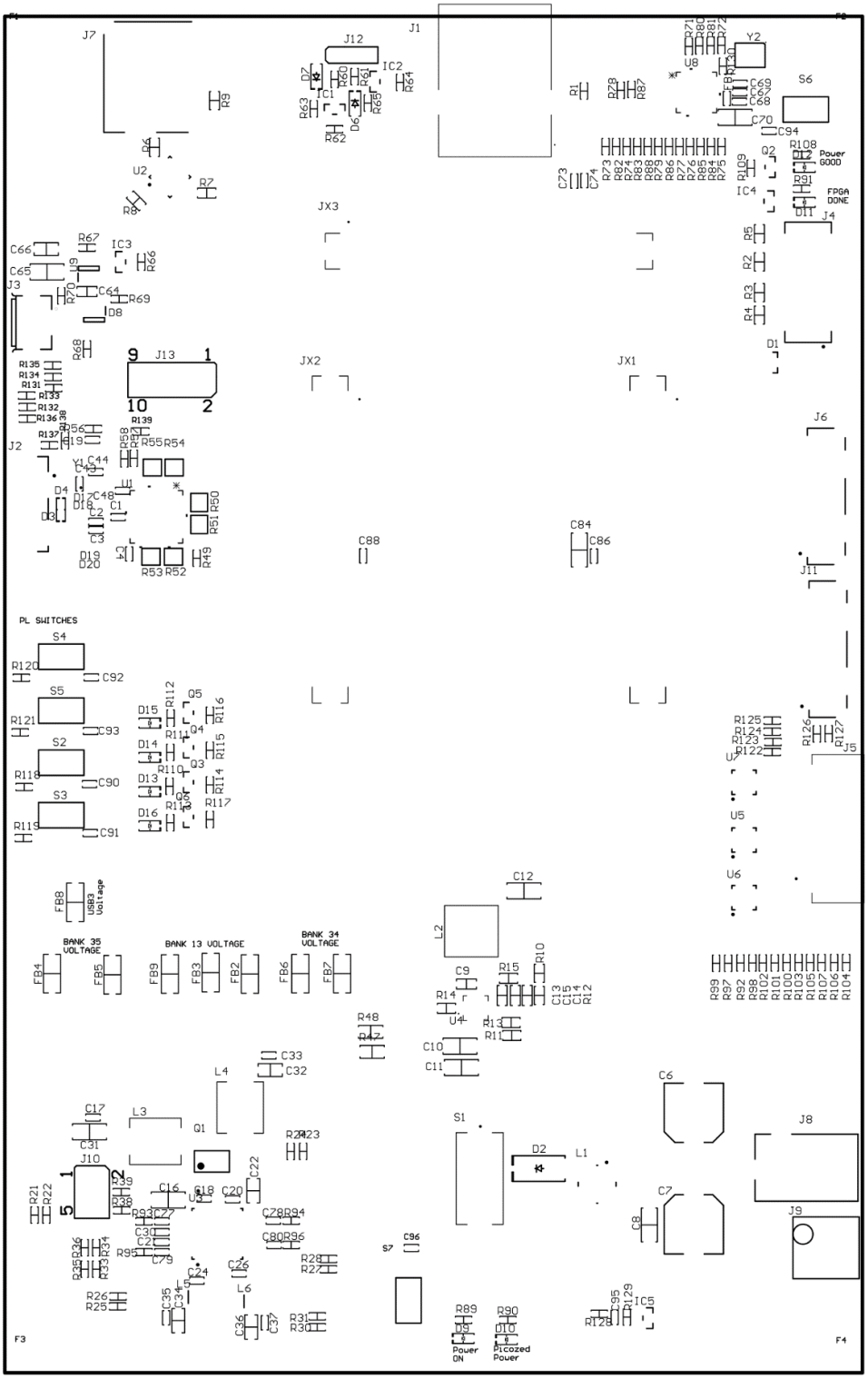
[13] Luxima, "LUX1310," no. October. p. 91107, 2016.

[14] M. Su, J. Tan, C. Lin, J. Ye, C. Wang, and C. Hung, "Constructing a Mobility and Acceleration Computing Platform with NVIDIA Jetson TK1," in *2015 IEEE 17th International Conference on High Performance Computing and Communications, 2015 IEEE 7th International Symposium on Cyberspace Safety and Security, and 2015 IEEE 12th International Conference on Embedded Software and Systems*, 2015, pp. 1854–1858, doi: 10.1109/HPCC-CSS-ICESS.2015.212.

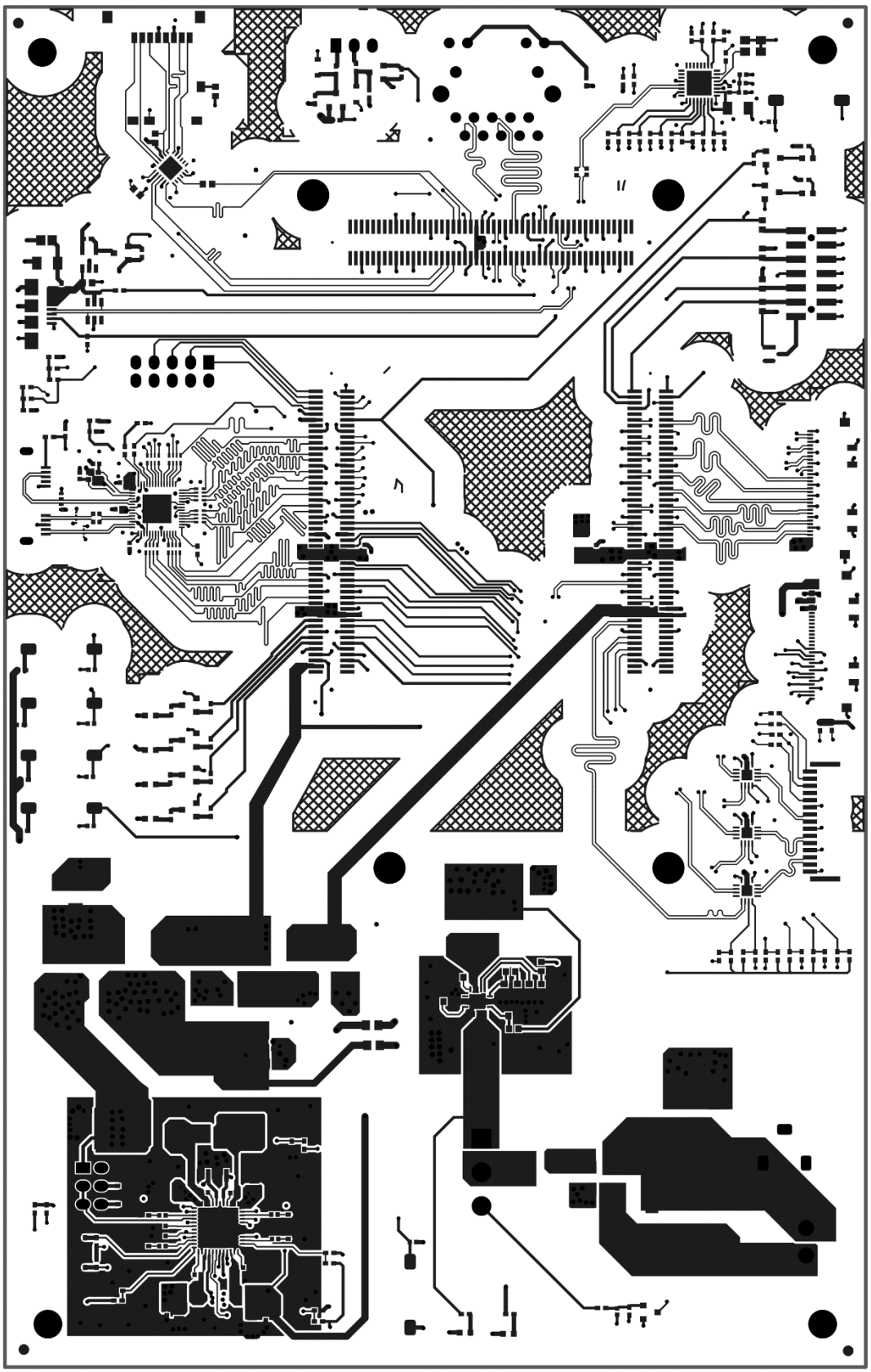
[15] "Field-programmable gate array - Wikipedia." https://en.wikipedia.org/wiki/Field-programmable_gate_array (accessed Dec. 27,

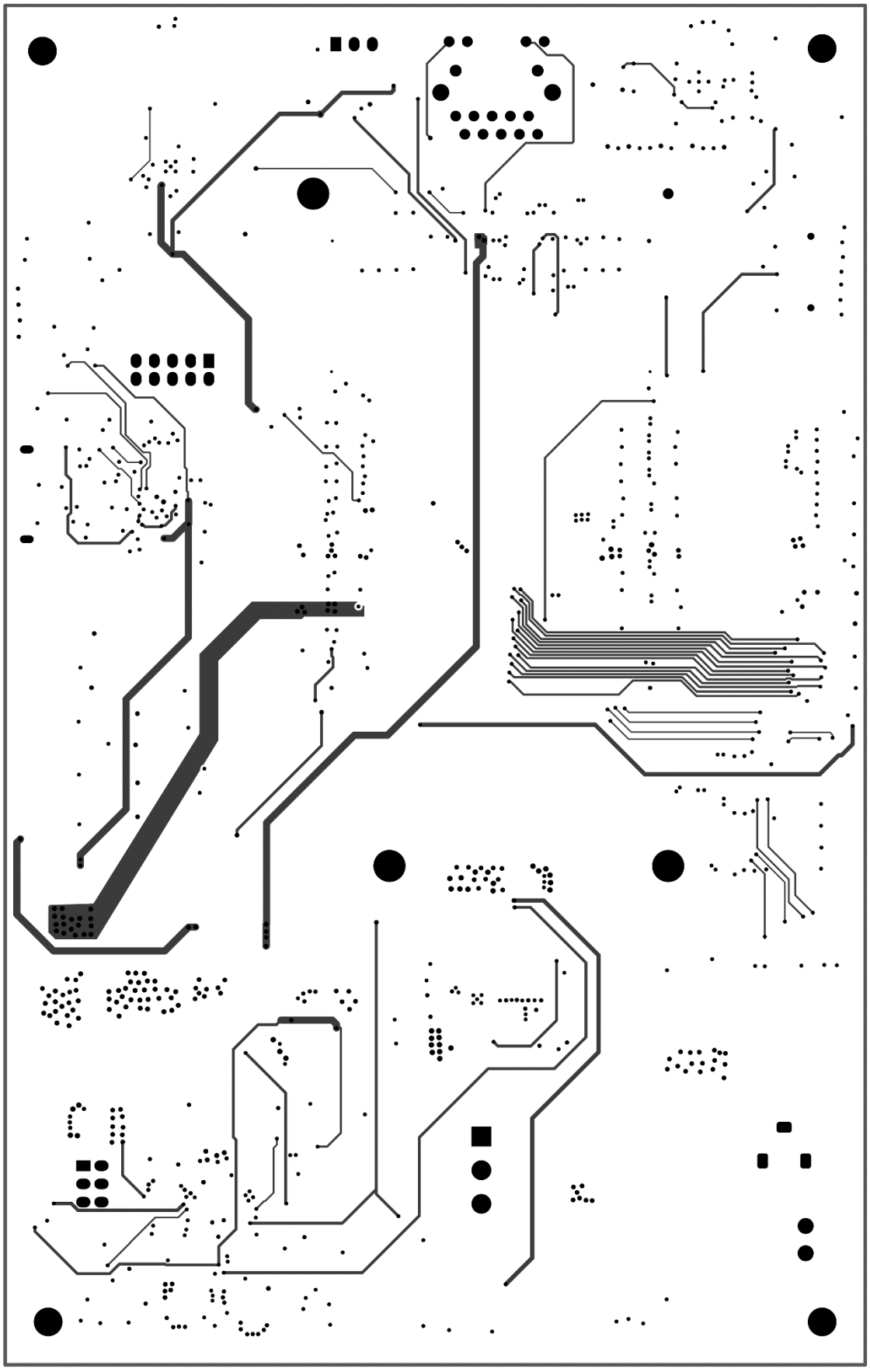
2020).
[16] M. Russell and S. Fischaber, “OpenCV based road sign recognition on Zynq,” *IEEE Int. Conf. Ind. Informatics*, pp. 596–601, 2013, doi: 10.1109/INDIN.2013.6622951.
[17] Y. Chalich, A. Mallick, B. Gupta, and M. Jamal Deen, “Development of a low-cost, user-customizable, high-speed camera,” *PLoS One*, vol. 15, no. 5, p. e0232788, May 2020, doi: 10.1371/journal.pone.0232788.
[18] Xilinx Inc., “Zynq-7000 SoC Data Sheet: Overview,” vol. 190, pp. 1–21, 2018, [Online]. Available: https://www.xilinx.com/support/documentation/data_sheets/ds190-Zynq-7000-Overview.pdf.
[19] AvNet, “PicoZed™ 7010/7020 SOM (System-On-Module) Hardware User Guide,” pp. 1–45, 2020.
[20] ON Semiconductor, “AN-5017 LVDS Fundamentals,” 2005. Accessed: Dec. 18, 2020. [Online]. Available: www.onsemi.com.
[21] Texas Instruments, “Interface Circuits for TIA/EIAA644 (LVDS) Design Notes.”
[22] MIPI Alliance, “Mipi Dphy Spec V2.5,” vol. 03, no. October, pp. 12–15, 2004.
[23] USB 3.0 Promoter Group, “Universal Serial Bus 3.2 Specification Revision 1.0,” p. 518, 2017.
[24] IEEE, “IEEE 802.3-2018 - IEEE Standard for Ethernet,” *IEEE Std 802.3-2018 (Revision of IEEE Std 802.3-2015)*, 2018. https://standards.ieee.org/standard/802_3-2018.html (accessed Dec. 20, 2020).
[25] “Overview of the Gigabit Ethernet standard.” https://searchnetworking.techtarget.com/tutorial/Gigabit-Ethernet-standard-Overview-of-1000BASE-Ethernet-lesson-5b (accessed Dec. 20, 2020).
[26] On-Semi, “NOIP1SN0300A Global Shutter CMOS Image Sensors,” pp. 1–2, 2014.
[27] Future Technology Devices International Limited, “FT600Q-FT601Q IC Datasheet (USB 3.0 to FIFO Bridge),” pp. 1–33, 2017, [Online]. Available: http://www.ftdichip.com.
[28] N. Wang, Z. Yan, J. Tang, B. Xiao, J. Lyu, and H. Wang, “Differential-mode Modeling of Common Mode Chokes for EMI filter in Switching Power Supply,” *2018 Int. Appl. Comput. Electromagn. Soc. Symp. China, ACES-China 2018*, pp. 5–6, 2019, doi: 10.23919/ACESS.2018.8669255.
[29] Texas Instruments, “TPS54821 4.5 V to 17 V Input, 8 A Synchronous Step Down Converter With Hiccup,” *Datasheet*, no. February, 2002.
[30] AvNet, “PicoZed ™ Based Embedded Computing Systems Carrier Design Guide,” pp. 1–35, 2020.
[31] Xilinx, “Zynq-7000 SoC Technical Reference Manual,” *Ug585*, vol. 585, pp. 1–1843, 2018.
[32] FTDI, “Application Notes FT60X PCB Layout Guidelines,” vol. 44, no. 0, pp. 1–10, 2017.
[33] A. Pcr and L. Kit, “IS400 Data Sheet,” 고생물학회지, vol. 31402, no. September 2004, pp. 0–1, 2012, [Online]. Available: http://www.papersearch.net/view/detail.asp?detail_key=10000715.

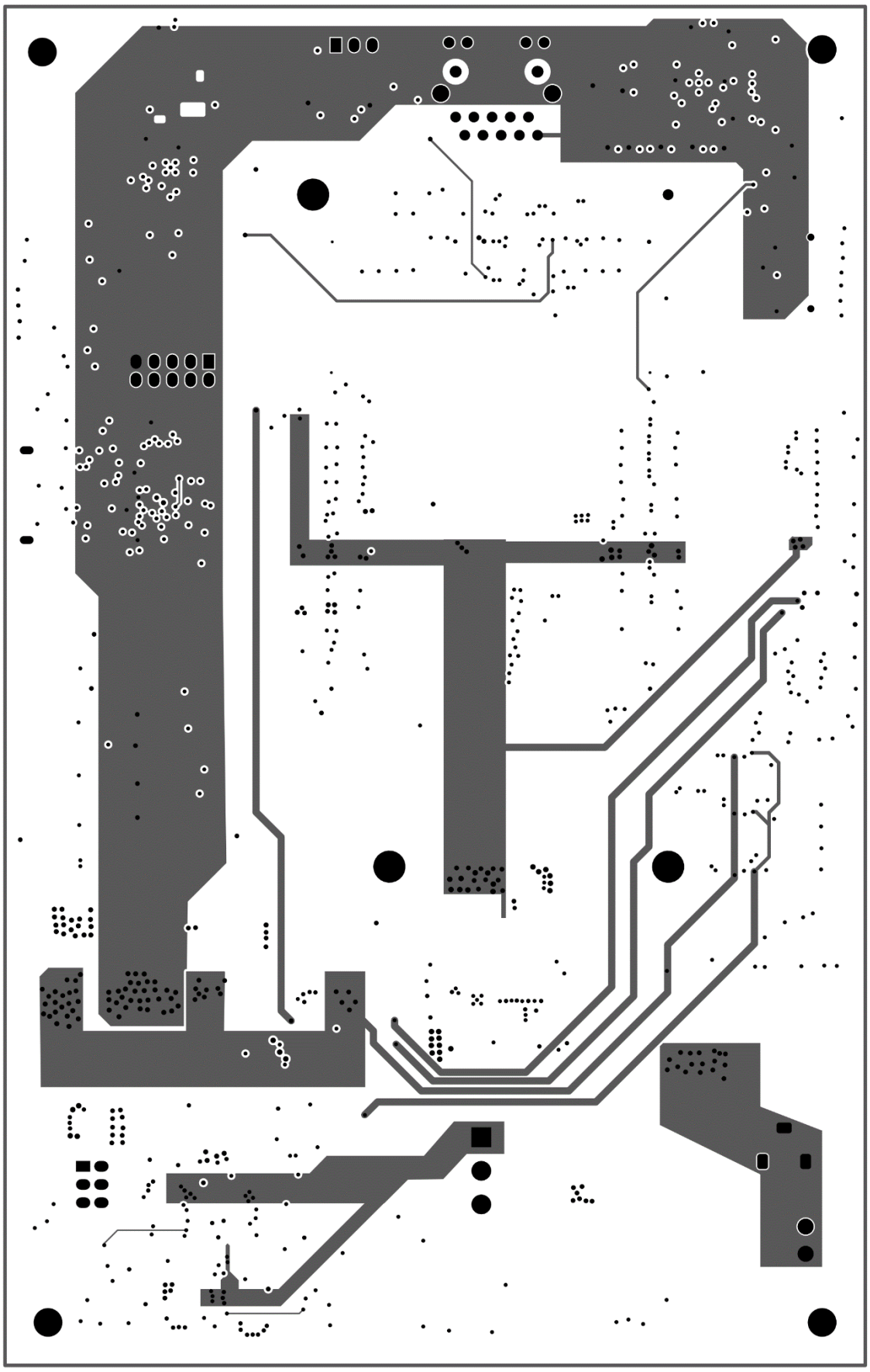
Appendix 1 – Image Acquisition Board Component Placement

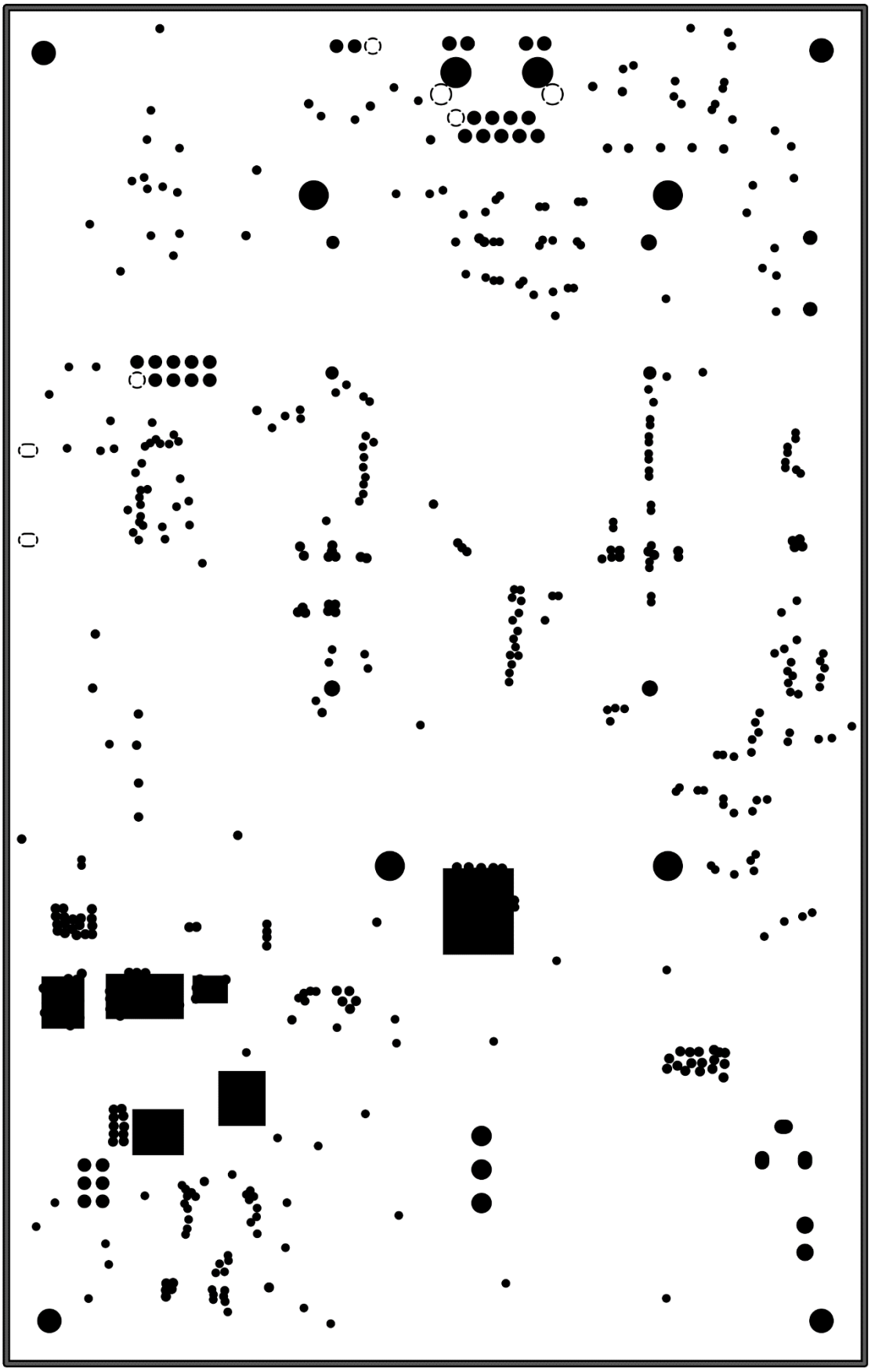


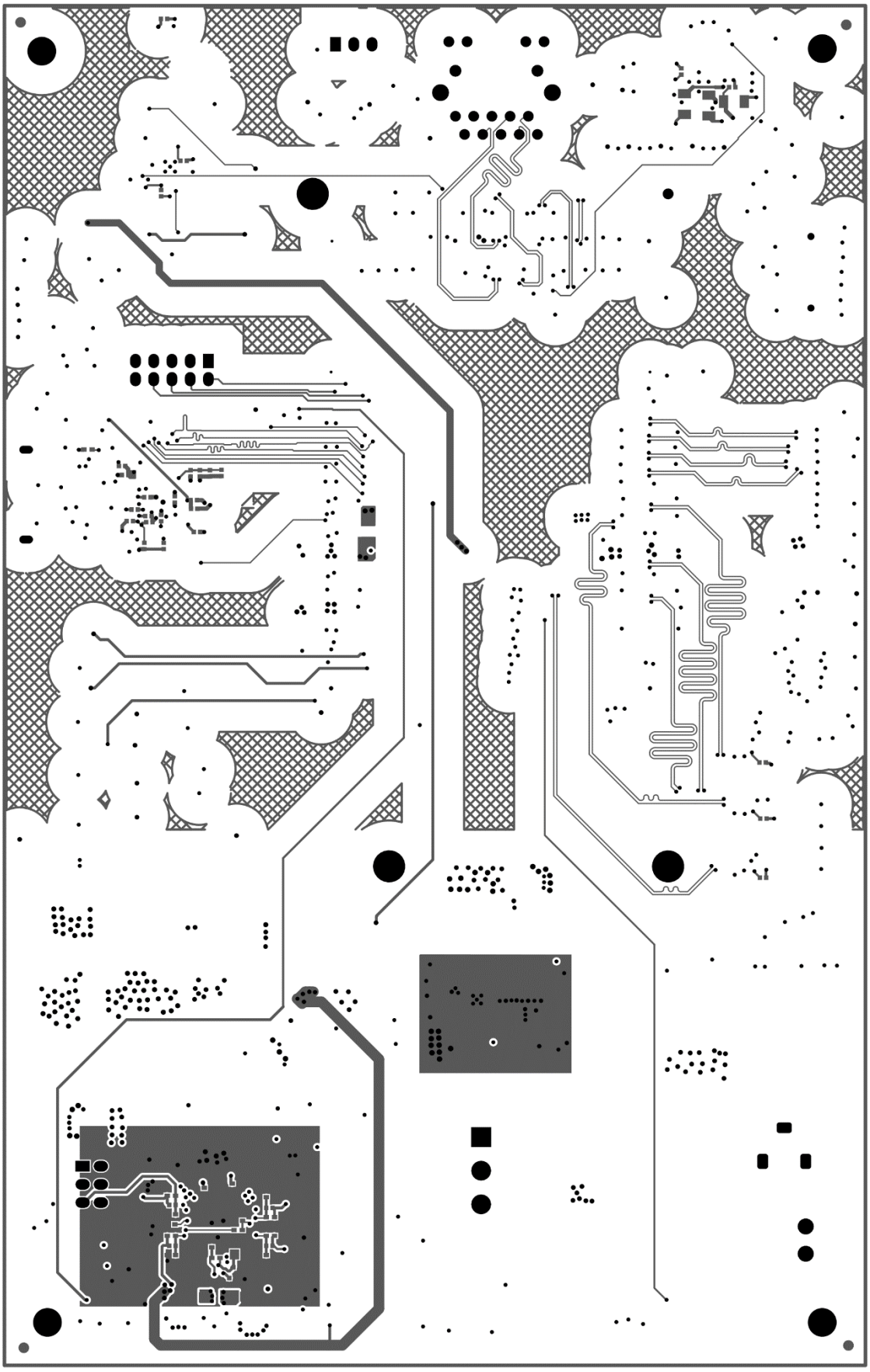
Appendix 2 – Image Acquisition Board PCB Layers



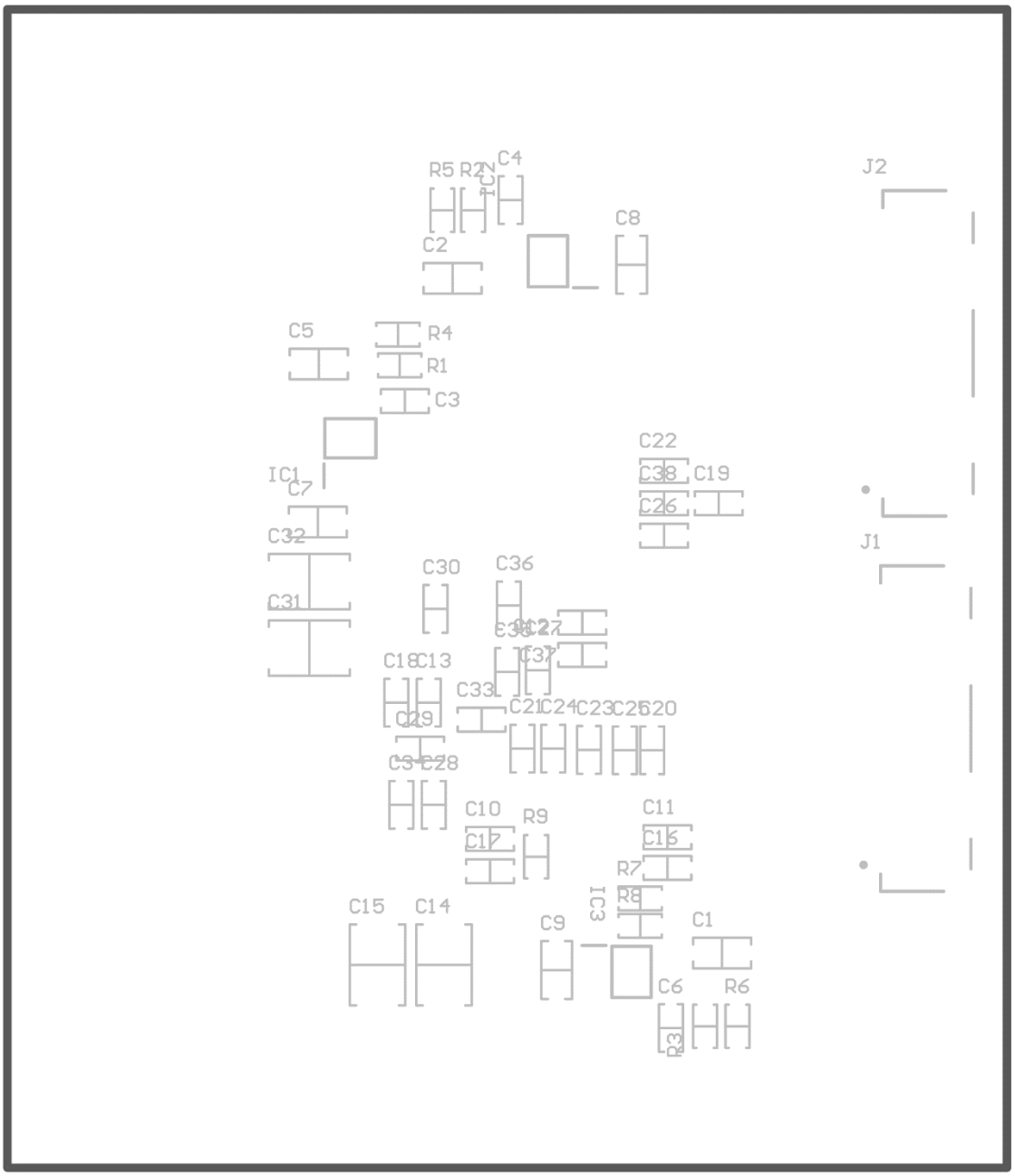


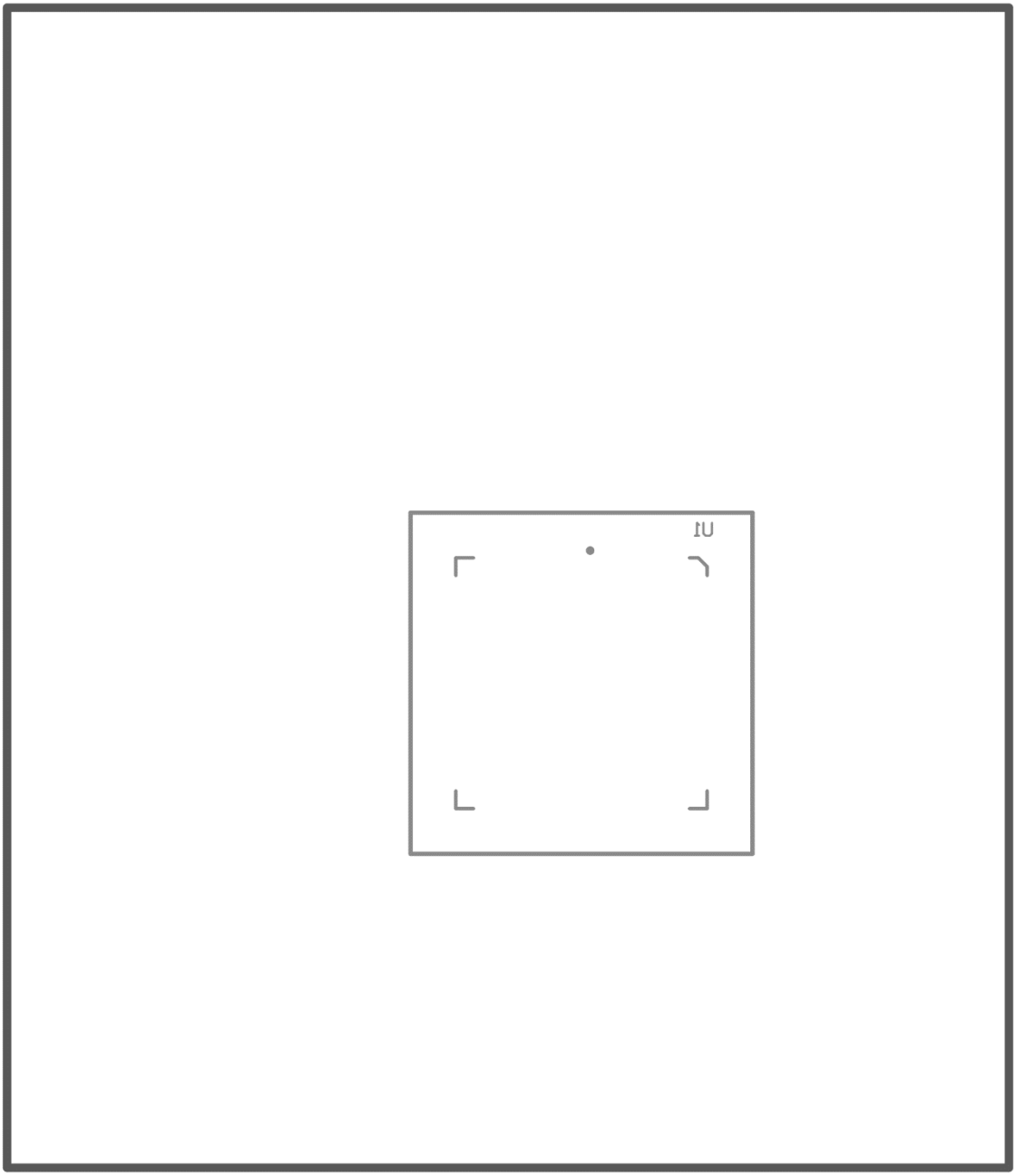






Appendix 3 – Camera Board Component Placement

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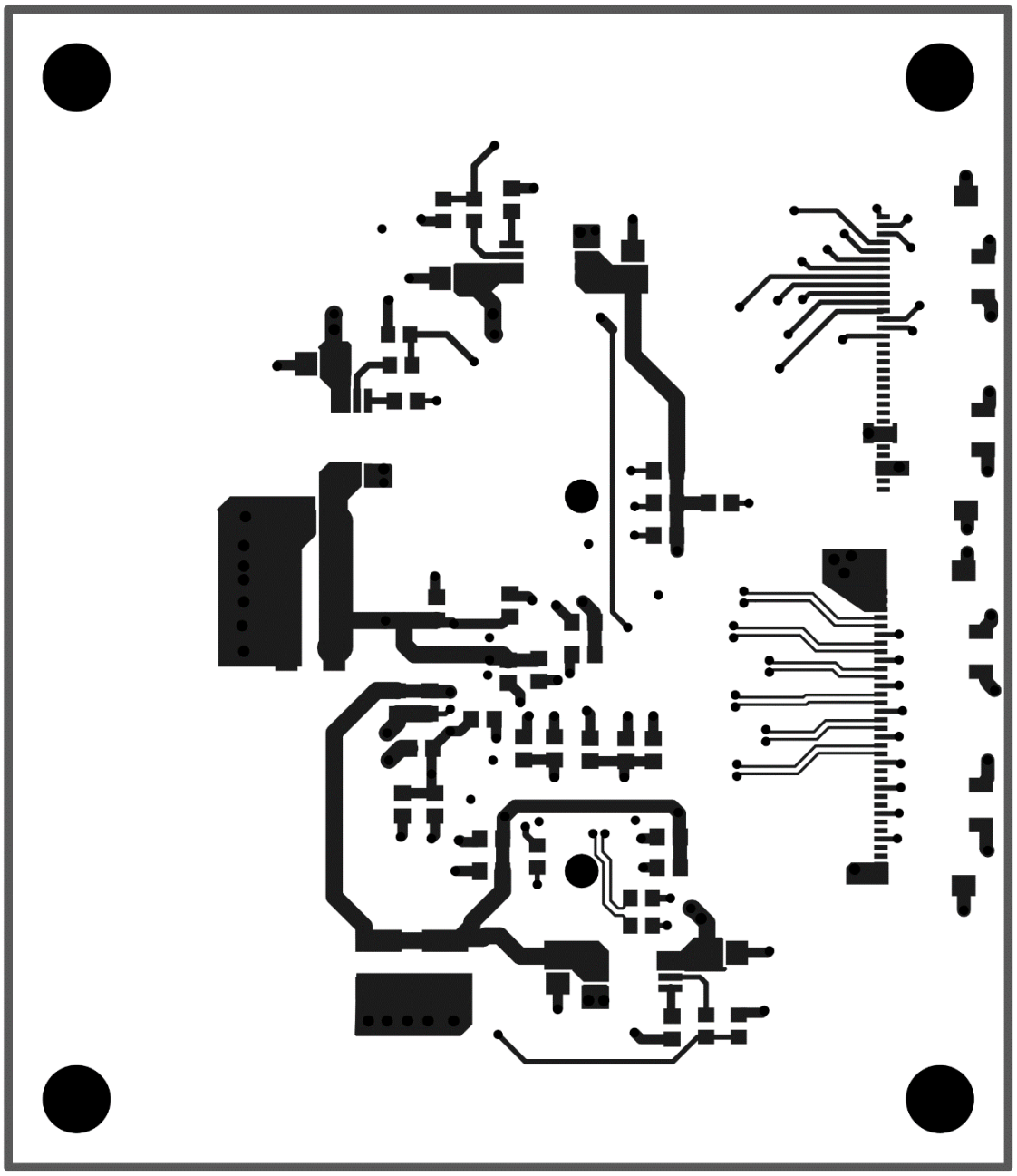
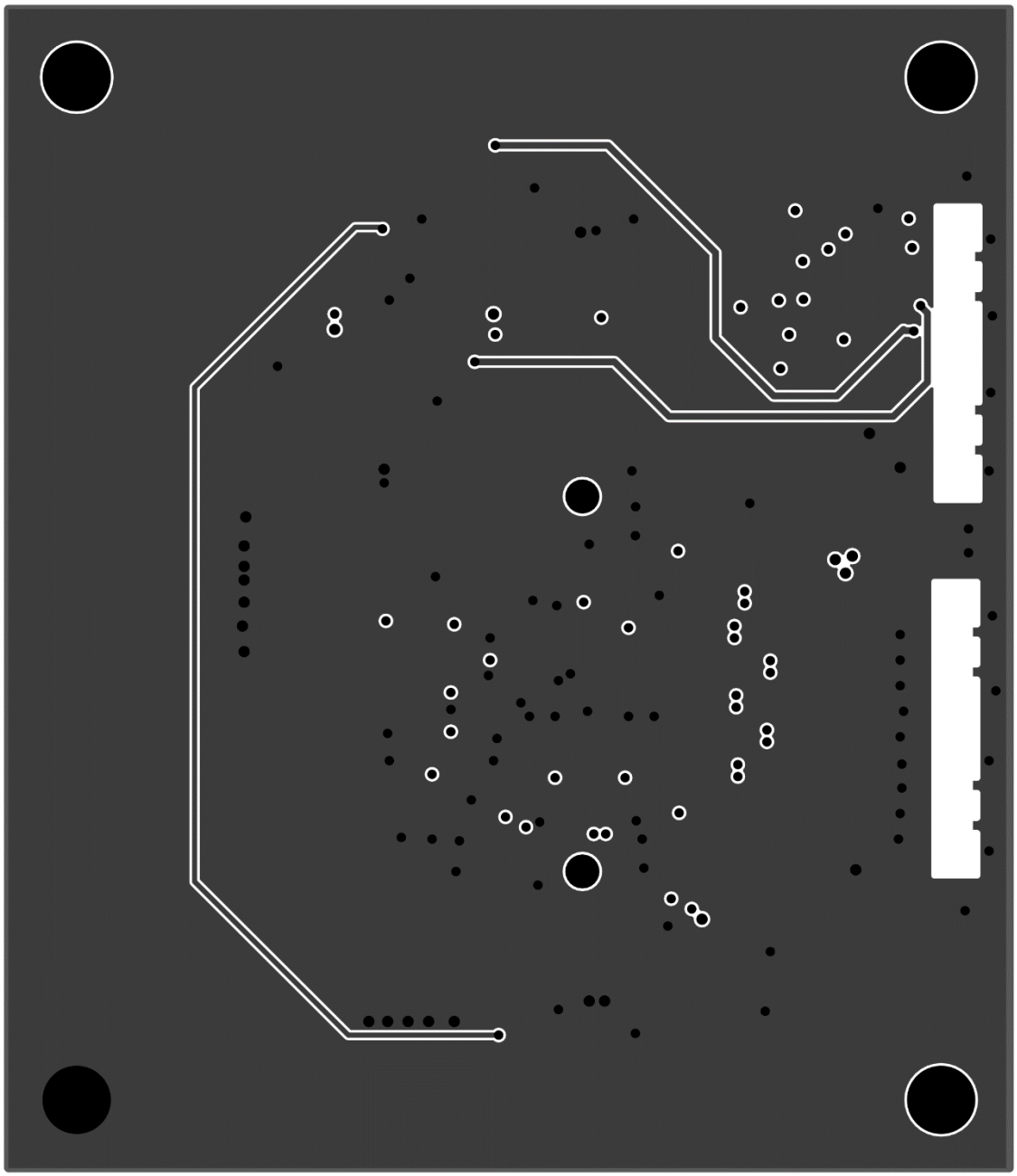
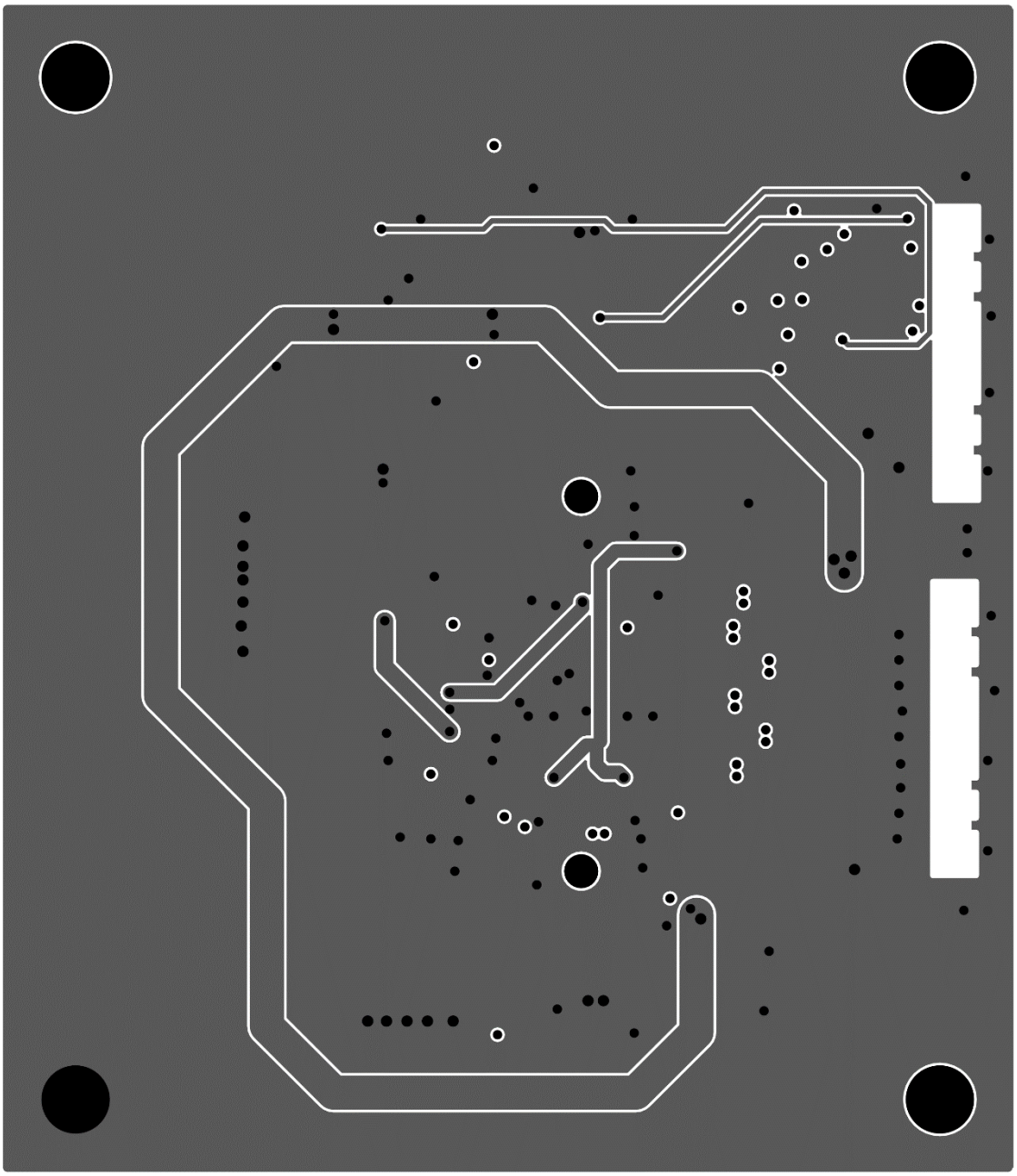
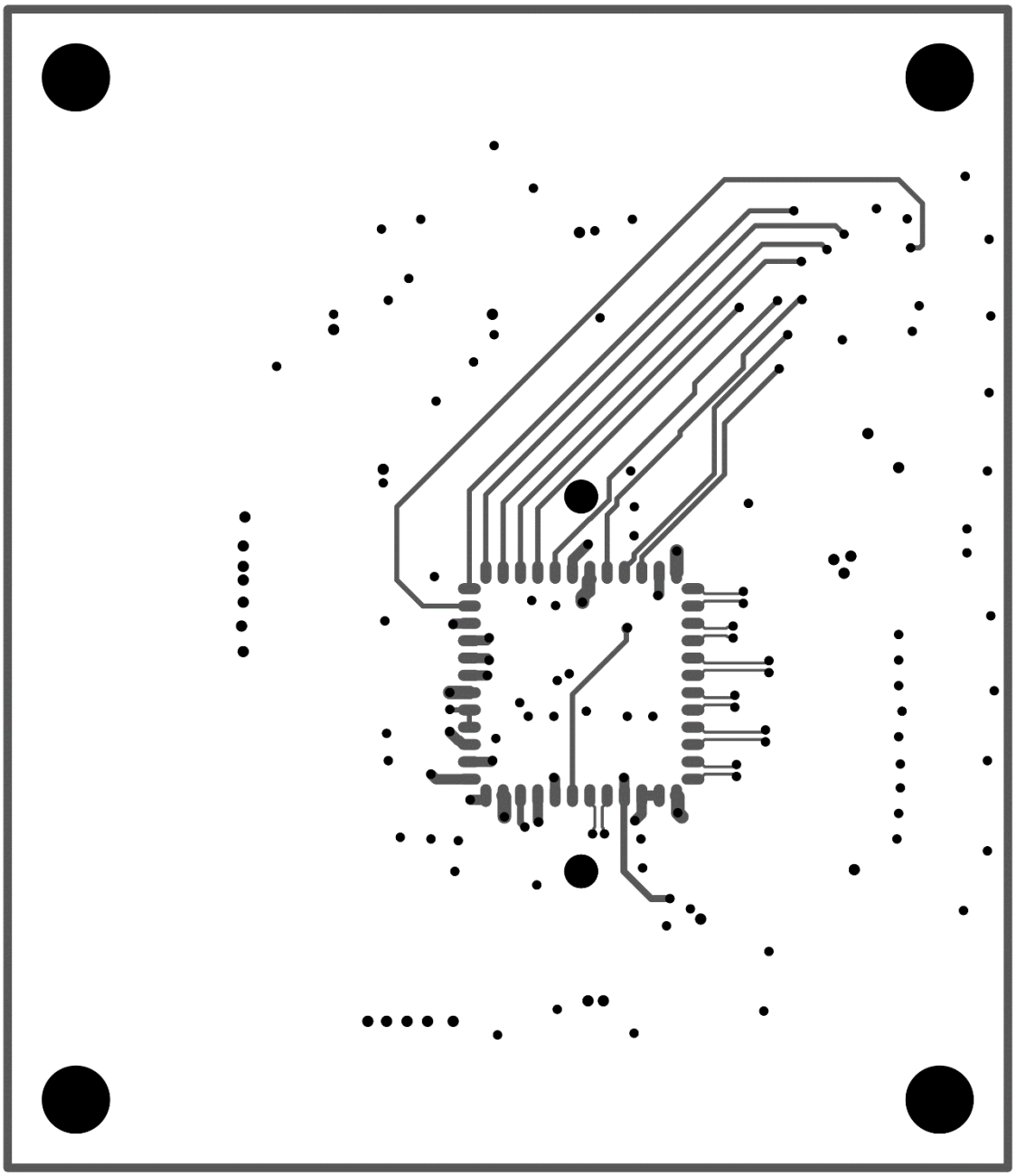
Appendix 4 – Camera Board PCB Layers









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