THESIS ON POWER ENGINEERING,
ELECTRICAL ENGINEERING, MINING ENGINEERING D72

Semiconductor Power Loss Reduction and Efficiency Improvement Techniques for the Galvanically Isolated Quasi-Z-Source DC-DC Converters

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Dissertation was accepted for the defence of the degree of Doctor of Philosophy in Engineering on May 12, 2015

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Defence of the thesis: July 1, 2015 at 12:00, room NRG-422, Tallinn University of Technology, Ehitajate tee 5, Tallinn, Estonia

Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology, has not been submitted for any academic degree.

Liisa Liivik .....

ISSN 1406-474X
ISBN 978-9949-23-790-6 (publication)
ISBN 978-9949-23-791-3 (PDF)

ENERGEETIKA. ELEKTROTEHNIKA. MÄENDUS D72

Galvaaniliselt isoleeritud kvaasiimpedantsallikaga alalispinge-muunduri pooljuhtide võimsuskao vähendamine ja kasuteguri suurendamine

LIISA LIIVIK

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Acknowledgements

My research for the degree of PhD was conducted at the Department of Electrical Drives and Power Electronics (renamed Department of Electrical Engineering) of Tallinn University of Technology. My studies were advancing along a rather thorny path through a lengthy period.

First of all, I would like to thank the department staff for inviting me back to finish my PhD thesis. My special deep thanks go to my supervisor Dr. Dmitri Vinnikov for his patience and belief in me, support during critical moments and persistence, which have made this thesis possible.

Next, I would like to express my appreciation to the consultant of my thesis Junior Researcher Andrii Chub for his invaluable help in sharing scientific knowledge of power electronics; he was always ready to take time to answer all my questions.

I am also grateful to Dr. Anton Rassõlkin for his useful advice in formatting the thesis and his comments, suggestions, and support.

I would like to thank my colleagues Dr. Indrek Roasto, Dr. Oleksandr Husev, Dr. Janis Zakis, Dr. Andrei Blinov, Dr. Tanel Jalakas, PhD student Roman Kosenko, PhD student Levon Gevorkov, and everyone who gave me invaluable advice and helped me in article publishing.

Moreover, I would like to thank Mare-Anne Laane for revising and editing English texts in my articles and the thesis.

In addition, I would like to express my sincere thanks to all colleagues from the Department of Electrical Engineering who helped me in various ways and made my work and life easier during these years.

Last but not least, my sincere thanks go to Hjalmar, Valli, Nevel, Helene and Hermann for their care, support, patience, and comprehension throughout the years of my study.

Thank you all!
Liisa Liivik

List of Abbreviations

AC	Alternating Current
CCM	Continuous Conduction Mode
CSC	Current-Source Converter
DC	Direct Current
EMI	Electromagnetic Interference
EPDN	Electronic Power Distribution Network
ESR	Equivalent Series Resistance
FB	Full-Bridge
FC	Fuel Cell
FSqZSC	Full-Synchronous Galvanically Isolated quasi-Z-Source DC-DC Converter
FSSqZSC	Full Soft-Switching Galvanically Isolated quasi-Z-Source DC-DC Converter
HB	Half-Bridge
HqZSSRC	Hybrid Galvanically Isolated quasi-Z-source Series Resonant DC-DC Converter
JFET	Junction Gate Field-Effect Transistor
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IqZSFPPC	Interleaved quasi-Z-Source-Fed Push-Pull Converter
IS	Impedance-Source
ISN	Impedance-Source Network
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
PCB	Printed Circuit Board
PEC	Power Electronic Converter
PMSG	Permanent Magnet Synchronous Generator
PSM	Phase-Shift Modulation
PV	Photovoltaic
PWM	Pulse-Width Modulation
qSZI	quasi-Z-Source Inverter
qZS	quasi-Z-Source
qZSC	Galvanically Isolated quasi-Z-Source DC-DC Converter
qZSN	quasi-Z-Source Network
qZSSRC	Galvanically Isolated quasi-Z-Source Series Resonant DC-DC Converter
RES	Renewable Energy Source
RMS	Root Mean Square
SR	Series Resonant
ST	Shoot-Through
TqZS	Trans-quasi-Z-Source
TUT	Tallinn University of Technology
TZS	Trans-Z-Source

VDR	Voltage Doubler Rectifier
VFC	Variable Frequency Control
VS	Voltage-Source
VSC	Voltage-Source Converter
VSI	Voltage-Source Inverter
WBG	Wide Bandgap
YS	Y-Source
ZCS	Zero Current Switching
ZS	Z-Source
ZSI	Z-Source Inverter
ZVS	Zero Voltage Switching
ZVZCS	Zero Voltage Zero Current Switching

List of Symbols

C_b	DC blocking capacitor
C_f	filter capacitor of the VDR
C_r	resonant capacitor
D_A	duty cycles of an active state
D_r	diode of the VDR
D_{ST}	duty cycle of a shoot-through state
D_Z	duty cycle of a zero state
G_{boost}	output voltage gain in the boost mode
G_{normal}	output voltage gain in the normal mode
f_{qZS}	operating frequency of qZSN
f_r	resonant frequency
f_{SW}	switching frequency
I_{CqZ}	qZSN capacitor current
I_D	maximum continuous drain current
I_{DC}	DC-link current
I_{DqZ}	qZSN diode current
$I_{F(AV)}$	maximum average forward current
I_{IN}	input current
I_{LqZ}	qZSN inductor current
I_{SW}	switch current
$I_{TX,pr}$	primary winding current of the isolation transformer
$I_{TX,pr(av)}$	average current per half cycle of the resonant tank
$I_{TX,pr(m)}$	amplitude value of the current through the resonant tank
$I_{TX,sec}$	secondary winding current of the isolation transformer
L_{IN}	input inductor
L_l	leakage inductance of the isolation transformer
L_m	magnetizing inductance of the isolation transformer
L_r	resonant inductor
n	transformer turns ratio
P	operating power
P_{IN}	input power
P_r	power dissipated in the resonant tank
Q_g	total gate charge of a switch
Q_{OSS}	output charge of a switch
r_c	desired peak-to-peak current ripple
$R_{DS(on)}$	drain-source on-state resistance
R_g	gate resistance
R_{ld}	load resistance
R_r	resistance of the resonant circuit
S	switch
T	switching period
t_A	active state time duration

t_{off}	OFF-state time duration
t_{on}	ON-state time duration
T_{qZ}	coupled inductor
t_{ST}	shoot-through state duration
t_Z	zero state time duration
V_C	capacitor voltage
V_{CqZ}	qZSN capacitor voltage
V_{DC}	DC-link voltage
$V_{DC(\text{peak})}$	peak DC-link voltage
V_{DqZ}	qZSN diode voltage
V_{DS}	maximum drain-source voltage of MOSFET
V_F	forward voltage drop of a diode
$V_{FV\,DqZS}$	forward voltage drop of the qZSN diode
V_G	gate voltage
V_{GS}	gate-source voltage
V_{IN}	input voltage
$V_{IN,\,min}$	minimum input voltage
$V_{IN,\,nom}$	nominal input voltage
V_{LqZ}	qZSN inductor voltage
V_{OUT}	output voltage
V_{RRM}	maximum repetitive peak reverse voltage
V_{SW}	switch voltage
$V_{TX,pr}$	primary winding voltage of the isolation transformer
$V_{TX,sec}$	secondary winding voltage of the isolation transformer
φ	phase shift angle

1 INTRODUCTION

1.1 Galvanically Isolated Quasi-Z-Source DC-DC Converter – a New Topology for Renewable Energy Applications

Galvanically isolated impedance-source (IS) DC-DC converter technology is an emerging trend of electric energy conversion alternative to voltage-source and current-source technologies. A galvanically isolated quasi-Z-source DC-DC converter (qZSC) was the first member of this family of converters. It was introduced in [1] as a new type of power conditioning system for renewable and alternative energy sources. The new topology is based on a conventional voltage-source (VS) full-bridge (FB) galvanically isolated DC-DC converter [4]; it contains a passive impedance network – a quasi-Z-source network (qZSN) at the input (Figure 1.1). The qZSN consists of two capacitors, two inductors, and one diode, all of which are connected in a specific configuration. The qZSN is an improved derivative of a baseline Z-source network [5] with another position of the input voltage source, as shown in [PAPER-VII]. The qZSC suits well for renewable energy applications thanks to continuous input current ensured by the input inductor L_{qZ1}. Improved position of input voltage source connection to the qZSN results in limited inrush current, since there is no current path at start-up, which is present in Z-source derived topologies. Moreover, qZSC is capable of converterless integration of short-term energy storages (batteries) [6], bidirectional operation capability [7], and inherent short-circuit protection.

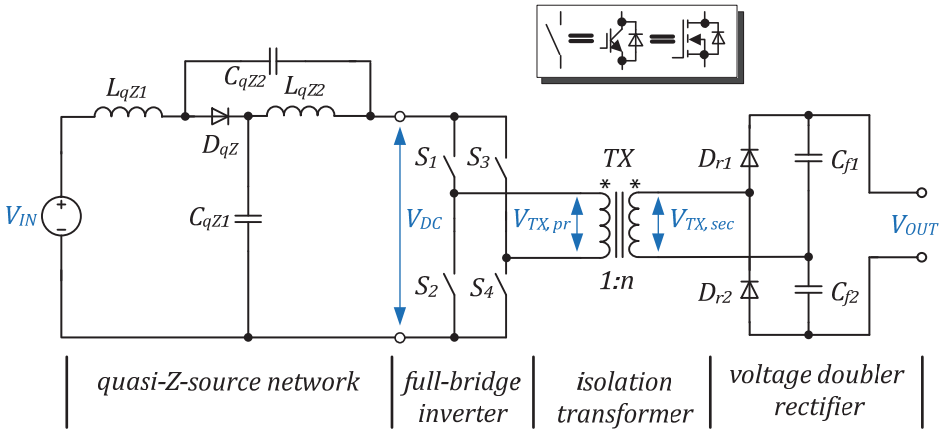


Figure 1.1 Generalized topology of the qZSC.

General operation principle of the qZSC

The qZSC is advantageous in applications with wide input voltage regulation. It keeps the DC-link voltage (V_{DC}) constant despite input voltage variations. The qZSC ensures volt-second balance and constant flux swing of

the isolation transformer if the DC-link voltage is stabilized using the PWM control with constant active state duty cycle [8]. The qZSC operates either in the *boost* or in the *normal mode* depending on the input voltage. The converter is usually designed to operate in the *normal mode* at maximum input voltage, which equals the desired DC-link voltage. The converter switches to the *boost* (shoot-through) *mode* when the input voltage decreases. The shoot-through (ST) states are used to step up the voltage across the FB inverter (V_{DC} in Figure 1.1), like in the current-source converter (CSC) [5]. During ST states, at least one leg of the primary inverter is conducting, which leads to an increase in the magnetic energy stored in the DC side inductors L_{qZ1} and L_{qZ2}. At that time, the DC capacitors C_{qZ1} and C_{qZ2} are protected from short-circuiting by the diode D_{qZ}. The higher energy stored in inductors results in the voltage step-up seen on the transformer terminals during the active states of the inverter. Therefore, the qZSN allows short- or open-circuit states without any damage of the converter.

In the *normal mode*, when the input voltage reaches the predefined DC-link voltage level, the qZSC operates without ST states. Its operation is quite similar to the conventional voltage-source converter (VSC), where the capacitor C_{qZ1} handles the whole DC-link voltage. Therefore, the qZSC features key properties of the VSC and the CSC, and thus withstands short- or open-circuit states of the main inverter without any damage.

General operating waveforms and main switching states of the qZSC are shown in Figure 1.2. The shoot-through states generated by simultaneous turn-ON of all inverter switches are advantageous due to the reduced current stress of the switches. The shoot-through state duration is evenly split into two time intervals. The switching period of the qZSC combines the shoot-through and active states and could be simply represented as:

$$T = t_A + t_{ST}\,, \tag{1.1}$$

where t_A is the cumulative duration of active states over the switching period, t_{ST} is the cumulative duration of the shoot-through states over the switching period, and T is the switching period.

The peak DC-link voltage value across the inverter bridge depends on the shoot-through state duration and is equal to the sum of voltages of the capacitors C_{qZ1} and C_{qZ2}:

$$V_{DC} = V_{CqZ1} + V_{CqZ2} = \frac{1}{1-2\cdot D_{ST}} \cdot V_{IN}\,, \tag{1.2}$$

where D_{ST} is the shoot-through state duty cycle ($D_{ST}=t_{ST}/T$).

Operating voltage and average current values of the primary side components of the qZSC during the active and shoot-through states are shown in Table 1.1 for the lossless case.

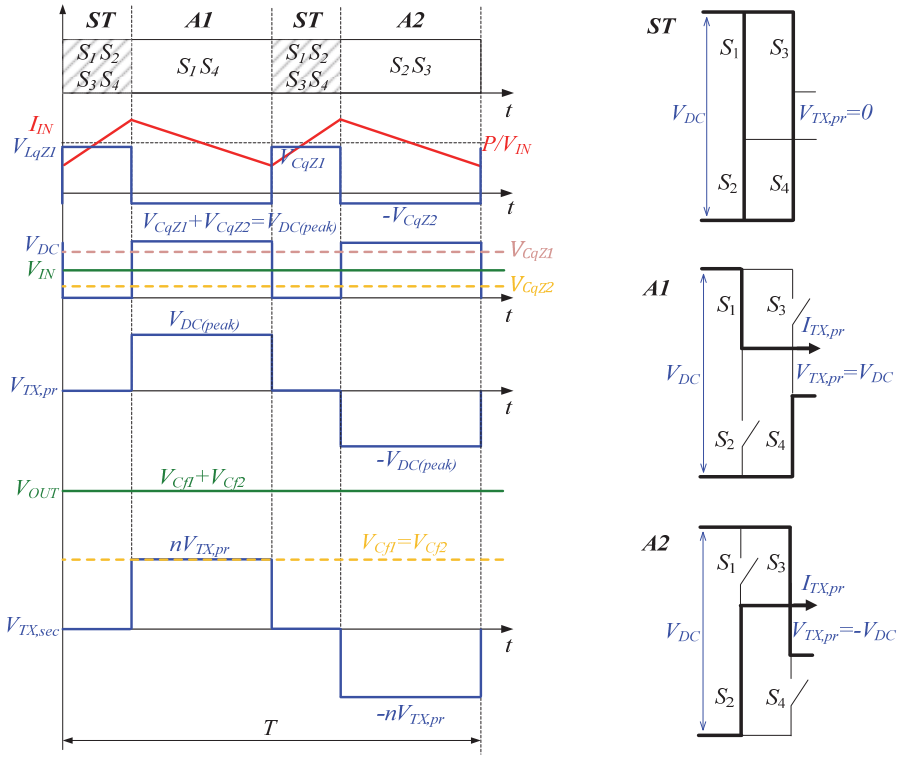


Figure 1.2 General operating waveforms and main switching states of the qZSC.

Utilization of a voltage doubler rectifier (VDR) on the secondary side of the qZSC improves power density by reducing the turns ratio of the isolation transformer. Positive voltage is applied to the transformer when the inverter is in state *A1*. This results in charging of the capacitor C_{f1} through the diode D_{r1} up to the inverter output voltage reflected to the secondary winding of the isolation transformer. Inverter output voltage is negative in state *A2*, and thus C_{f2} is charged through the diode D_{r2}. The output voltage (V_{OUT}) is a sum of voltages of the VDR capacitors, and equals twice the peak voltage of the secondary winding of the isolation transformer ($V_{TX,sec}$) [9]:

$$V_{OUT} = 2 \cdot V_{TX,\text{sec}} . \tag{1.3}$$

Taking previous equations into consideration, we can express the output voltage of the qZSC as:

$$V_{OUT} = \frac{2 \cdot V_{IN} \cdot n}{(1 - 2 \cdot D_{ST})}, \tag{1.4}$$

where n is the turns ratio of the isolation transformer.

It should be mentioned that these equations are valid if the qZSC operates in the continuous conduction mode (CCM), when the currents through the qZSN inductors L_{qZ1} and L_{qZ2} never fall to zero. At light loads and relatively low switching frequency, inductance values of L_{qZ1} and L_{qZ2} could be insufficient to

avoid the discontinuous conduction mode (DCM) [8], [10]. It causes an overboost effect of the DC-link and consequently the output voltage, which can lead to unstable operation of the qZSC. The DCM can be avoided if converter components are properly sized according to the detailed design guidelines presented for the CCM in [8], while values of the inductors L_{qZ1} and L_{qZ2} have to be dimensioned according to [11].

Table 1.1. Operating voltages and average currents of the qZSI.

State	*Active*	*Shoot-through*
Inductor voltage (V_{LqZ1}=V_{LqZ2})	$-\frac{D_{ST}}{1-2\cdot D_{ST}}\cdot V_{IN}$	$\frac{1-D_{ST}}{1-2\cdot D_{ST}}\cdot V_{IN}$
DC-link voltage (V_{DC})	$\frac{1}{1-2\cdot D_{ST}}\cdot V_{IN}$	*0*
DC-link current (I_{DC})	$\frac{P\cdot(1-2\cdot D_{ST})}{V_{IN}}$	$\frac{2\cdot P}{V_{IN}}\cdot D_{ST}$
Diode voltage (V_{DqZ})	*0*	$\frac{1}{1-2\cdot D_{ST}}\cdot V_{IN}$
Capacitor voltage (V_{CqZ1})	$\frac{1-D_{ST}}{1-2\cdot D_{ST}}\cdot V_{IN}$	
Capacitor voltage (V_{CqZ2})	$\frac{D_{ST}}{1-2\cdot D_{ST}}\cdot V_{IN}$	
Input current (I_{IN})	$\frac{P}{V_{IN}}$	
Inductor current (I_{LqZ1}=I_{LqZ2})	$\frac{P}{V_{IN}}$	
qZS diode current (I_{DqZ})	$\frac{P}{V_{IN}}$	

The qZSC could perform output voltage control through shoot-through generation in two ways: pulse width modulation (PWM) and phase-shift modulation (PSM). The shoot-through states in the PWM can be generated either by the overlap of active states [2] or by the shoot-through generation during zero states of the inverter [1]. In the PSM [3], only the shoot-through generation during zero states of the inverter is feasible.

Figure 1.3*a* represents the shoot-through control principle for the PWM performed by the overlap of active states. The control signals of the inverter diagonals are interleaved and require no dead time, while their duty cycles are greater than or equal to 0.5. The shoot-through states are generated naturally if the duty cycle is greater than 0.5 when top and bottom transistors conduct. The switching period in this control principle comprises only a shoot-through state

duration t_{ST} and an active state duration t_A Eq. (1.1). Equation (1.1) could also be represented as:

$$\frac{t_A}{T} + \frac{t_{ST}}{T} = D_A + D_{ST} = 1, \tag{1.5}$$

where D_A and D_{ST} are the duty cycles of active and shoot-through states, correspondingly. Apparently, the duty cycle of the shoot-through states can never exceed 0.5 [12].

The gating signals of the FB inverter switches measured (Figure 1.4*a*) have the same switching frequency at the PWM shoot-through control by the overlap of active states. The operating voltage and current waveforms of the inverter switch S_1 measured in the shoot-through and normal modes are shown in Figure 1.5. It can be seen that the efficiency of the qZSC is limited due to hard-switching of the inverter switches.

This control algorithm is simple and fits well IS DC-DC converters with a capacitive output filter, where the voltage amplitude of the primary winding of the isolation transformer defines the output voltage, while the active state duty cycle has minor influence. However, the active state duty cycle along with the transformer voltage amplitude has major influence on the output voltage in an IS DC-DC converter with a higher order low-pass filter, like an LC-filter, at the output side. In this case, it is needed to control the duty cycles of the active state and the shoot-through state independently to adjust the output voltage and stabilize the DC-link voltage correspondingly.

Durations of the active and the shoot-through state could be controlled separately if shoot-through states are generated during the zero states of the inverter, when either the top (S_1 and S_3) or bottom (S_2 and S_4) inverter switches short circuit the primary winding of the isolation transformer. It means that the switching period comprises three states: active, shoot-through, and zero state:

$$T = t_A + t_{ST} + t_Z. \tag{1.6}$$

Equation (1.6) could also be expressed as

$$\frac{t_A}{T} + \frac{t_{ST}}{T} + \frac{t_Z}{T} = D_A + D_{ST} + D_Z = 1, \tag{1.7}$$

where D_A is the duty cycle of an active state, D_{ST} is the duty cycle of a shoot-through state and D_Z is the duty cycle of a zero state.

Figure 1.3*b* shows the PWM control principle with shoot-through generation during zero states. In the given case, the zero states are generated only by the top inverter switches (S_1 and S_3). This method features different switching frequencies of the inverter switches. S_1 and S_3 operate at the switching frequency of the converter (i.e., with a switching period T), while S_2 and S_4 have three times higher switching frequency. Therefore, the PWM control with shoot-through generation during zero states is less advantageous than the previous one because of unequal switching losses of the inverter switches. The modification of this algorithm through diagonal and vertical swapping of the top

and bottom transistors proposed recently in [1] can be used to balance switching losses of the inverter switches.

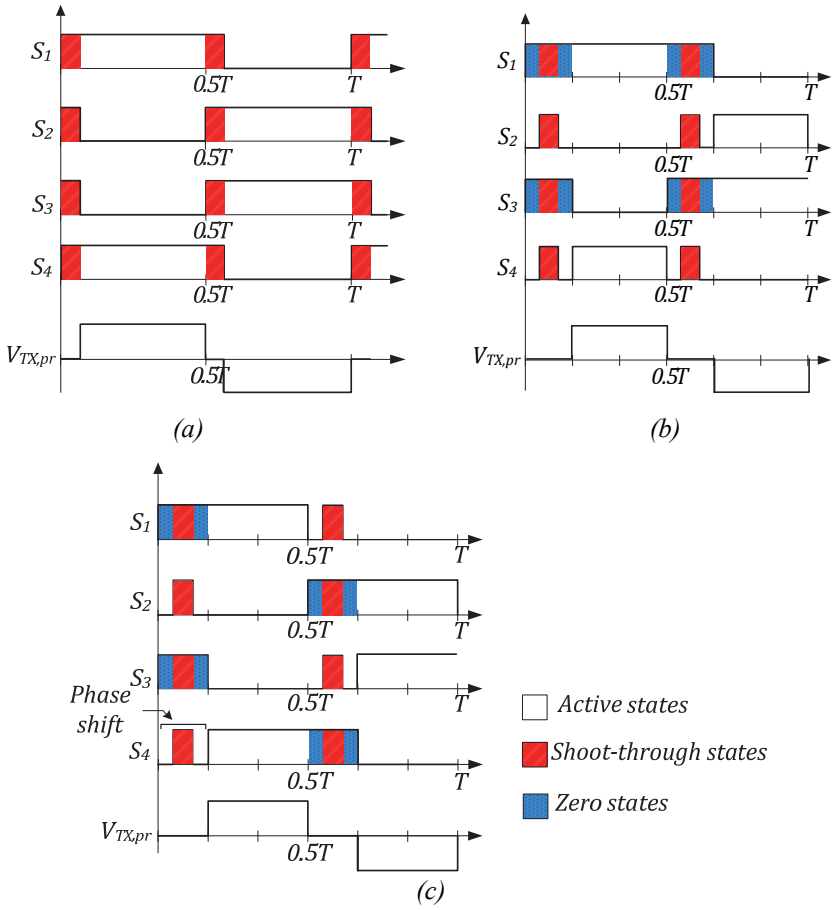


Figure 1.3 Shoot-through control principles: the PWM shoot-through control by the overlap of active states (a), the PWM control with shoot-through generation during zero states (b) and the PSM control with shoot-through generation during zero states (c).

The switching losses in the inverter switches are balanced in the PSM control principle with the shoot-through generation during zero states, which is an alternative to the previous PWM control principles, as shown in Figure 1.3*c* [3]. Zero states are generated through a phase shift between control signals. Gating signal of the inverter switches measured (Figure 1.4*c*) shows that zero states are generated twice per switching period by either the top (S_1 and S_3) or bottom (S_2 and S_4) inverter switches. This results in uniform distribution of switching losses among inverter switches.

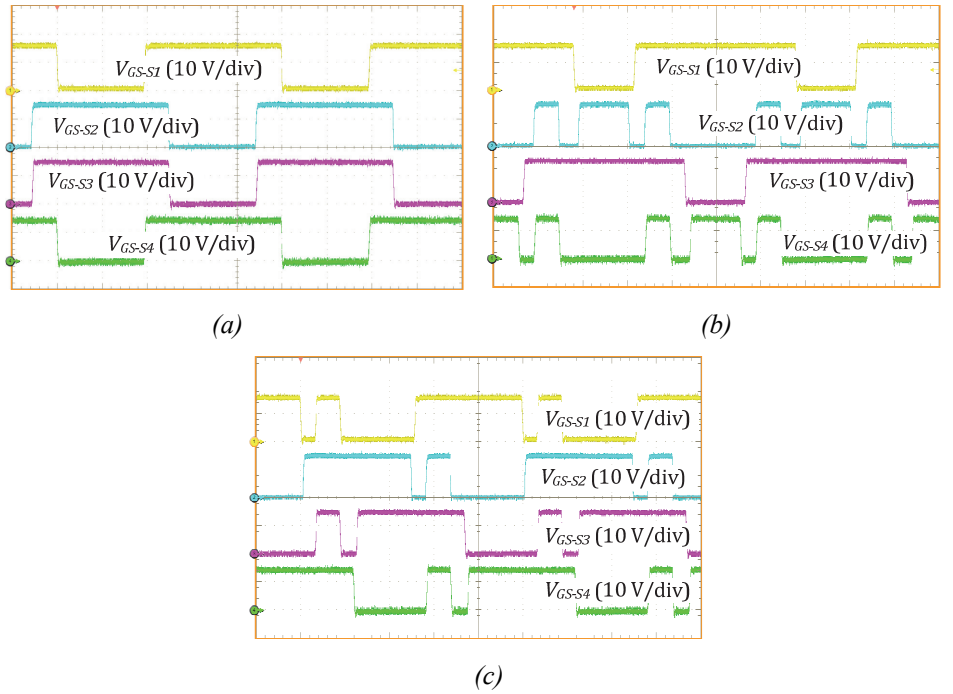
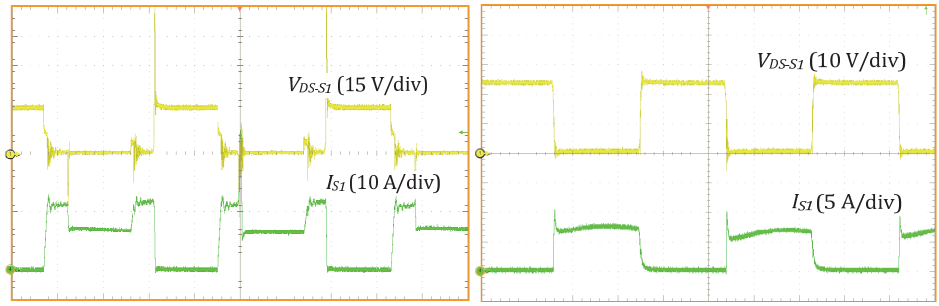


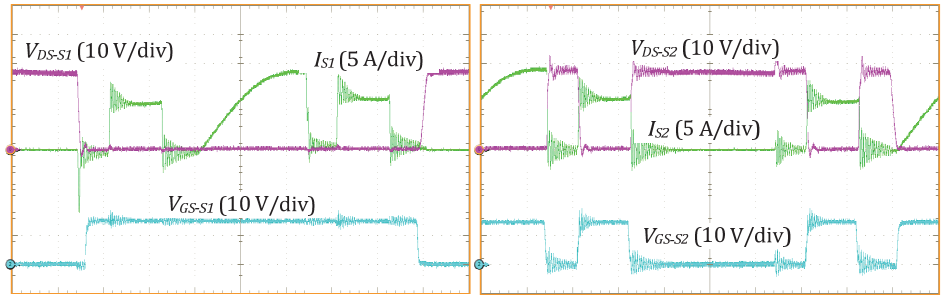
Figure 1.4 Gating signals of the full-bridge inverter switches at the PWM shoot-through control by the overlap of active states (a), the PWM control with shoot-through generation during zero states (b) and the PSM control with shoot-through generation during zero states (c).

The typical voltage, current and gating signal waveforms of the inverter switches in the boost operating mode are presented in Figure 1.6 and Figure 1.7 for the PWM and the PSM control with shoot-through generation during zero states, correspondingly. The PWM control features full soft-switching operation of the top inverter switches and partial soft-switching of the bottom inverter switches. In the PSM control, partial soft-switching of all the inverter switches is achieved. It is remarkable that they operate with ZVS and ZCS without any additional components.



(a) *(b)*

Figure 1.5 PWM shoot-through control by the overlap of active states: typical voltage and current waveforms of the inverter switches in the boost (a) and normal (b) operation modes.



(a) *(b)*

Figure 1.6 PWM control with shoot-through generation during zero states: typical voltage, current and gating signal waveforms of the top (a) and bottom (b) inverter switches in the boost operation mode.

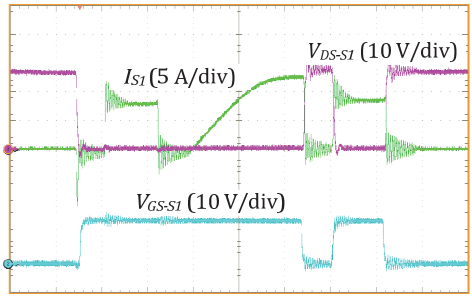


Figure 1.7 PSM control with shoot-through generation during zero states: typical voltage, current and gating signal waveforms of the inverter switches in the boost operation mode.

1.2 Motivation of the Thesis

Power electronics has an important role in the modern world where efficient and reliable power supplies and battery chargers for industrial, telecommunication and consumer electronics are required. Moreover, it is an enabling technology for modern power engineering, which includes renewable and alternative energy generation, battery energy storage systems and other applications. These applications are highly challenging and thus require versatile power electronics solutions available on the market. The qZSC has numerous advantages that suit specifically for modern applications: inherent safe operation with short- and open-circuit states of the inverter, wide input voltage regulation, continuous input current, galvanic isolation of the input and output sides, etc. Therefore, this converter topology can be highly beneficial as a power electronics building block for dispersed generation systems. Up to now, the topology has shown superior performance as a power conditioner for the fuel cells [13], PV panels [14] and residential wind turbines [15] as well as the power factor correction converter [16]. Modern applications typically require a converter capable of interfacing variable low-voltage input with a relatively high current into a DC bus at much higher voltage. Maximum peak efficiency of the qZSC has been reported to be in the range of 93 to 95% [1]. The power loss in semiconductors is the main cause of efficiency drop. Peak efficiency is typically achieved in the nominal operating mode, i.e. without voltage step-up at the input side. Input voltage regulation range is usually limited with an efficiency drop and typically lies within the range of 1:3. Converter efficiency can drop down to 85% at maximum voltage step-up when the input voltage is at a minimum level.

A simulation study of semiconductor power losses in the qZSC was performed in [PAPER-VIII] by means of PSIM simulation software with *Thermal Module*. Results allow for a wide input voltage and load regulation range according to the operating parameters described in Table 1.3 for operating points from Table 1.4. Power losses were studied for commercial semiconductor components from Table 1.2, which were used then in the experimental prototype. Simulations showed that the diode in the qZSN contributes most to the total semiconductor power loss. It is responsible for more than 50% of this power loss over the entire operating range, as shown in Figure 1.8. Losses in the qZSN diode are mostly comprised of conduction losses since a Schottky diode features near zero switching losses and depend slightly on the operation mode at constant average input current. These conduction losses are higher in the boost operation mode due to higher current ripple.

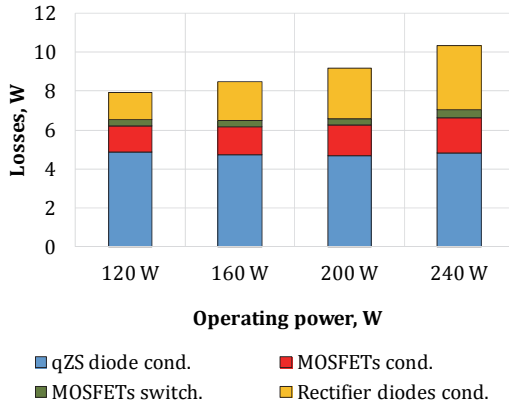


Figure 1.8 Breakdown of semiconductor power losses of the qZSC.

As can be seen from Figure 1.8, other main contributors to the losses in the qZSC are the conduction losses of the VDR diodes. They depend almost linearly on the operating power, since an average current of the VDR diode is equal to the output current (P/V_{OUT}) when the output voltage is constant. The forward voltage drop of the VDR diode remains nearly constant in the model over an operating range, while switching losses are negligible for SiC Schottky diodes.

Power losses of the inverter MOSFETs contribute a small fraction to the total power loss in the qZSC. Their switching losses remain nearly constant over the whole operating range of the converter while their conduction losses are increasing slightly with the increase of the operating power. The reason of this behavior is the redistribution between active and shoot-through states when the input power and voltage change. Two MOSFETs conduct DC-link current in the active state, while it flows through two inverter legs connected in parallel and two MOSFETs connected in series in each leg during the shoot-through state [2]. It means that the current of each inverter MOSFET is equal to the input current in the shoot-through state. It is shown in [PAPER-VIII] that conduction losses of the inverter MOSFETs can be separated into two components: losses during the active state and losses during the shoot-through state. The first component does not depend on the duty cycles, while it is defined by the output current reflected to the input side. The second component depends on the input current and the duty cycle of this state.

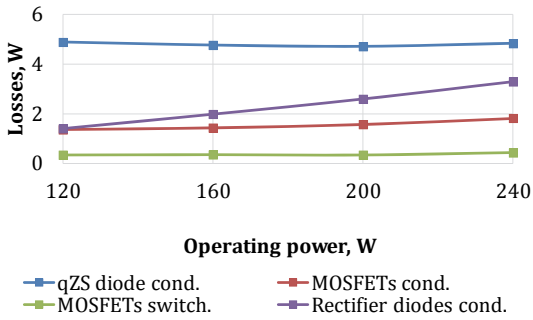


Figure 1.9 Estimated semiconductor power losses as a function of the output power of the qZSC.

The resulting losses curves obtained from the simulation study of the qZSC are presented in Figure 1.9. The conduction losses in parasitic resistances of other components of the converter (transformer, inductors, capacitors, wires, etc.) were omitted from the study to clarify power loss distribution between semiconductor components. However, in a real converter these parasitic elements decrease the efficiency by up to 2% in addition to the influence of the semiconductor losses [17].

As Figure 1.10 shows, the efficiency of the traditional qZSC cannot exceed 95.9%, considering semiconductor losses solely. In such challenging applications as module integrated converters for photovoltaic (PV) panel interfacing, the peak efficiency is typically achieved within the maximum power point range. The efficiency of the converter defines the energy yield of the PV panel and thus has to be optimized within the range of the maximum power point. Moreover, power losses result in additional heat dissipation, which leads to increased thermal stress on all the converter components. Consequently, a conclusion could be drawn that the power losses in semiconductors are the main factor limiting the performance of the qZSC, which has to be carefully addressed.

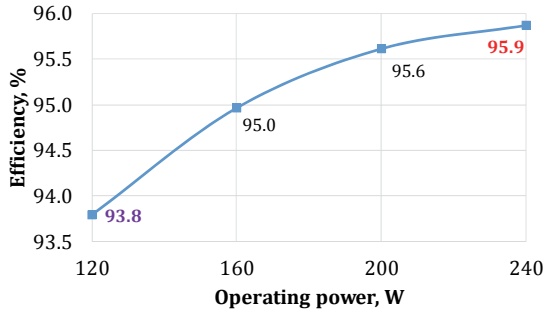


Figure 1.10 Estimated efficiency as a function of the output power of the qZSC.

This thesis is a part of the priority research program of the Power Electronics Group of Tallinn University of Technology targeted to the elaboration of new power electronics converter topologies and enhanced control methods for Electronic Power Distribution Networks (EPDNs). This activity was launched in 2010 in cooperation with Estonian (4Energia, Ubik Solutions, Estel Elektro, Clifton, MS Balti Trafo) and Norwegian (Vardar Eurus) companies. The aim is to introduce the research results to the market and thus increase their competitiveness and export potential. The research activities were directly supported by the targeted financing research project SF0140016s11 of the Estonian Ministry of Education and Research. In addition, it was co-financed by Estonian Research Council (grants G8538 and PUT744), European Center for Power Electronics (project VE554) and Estonian company Ubik Solutions (projects Lep12055, Lep13069 and LEP15006).

The main importance of this PhD project for Estonian and European science and economy lies in the development of new state-of-the-art technologies that will help to improve the efficiency of electric energy conversion and overall performance of different applications. With the recent growing demand for renewable energy, where the efficiency and flexibility improvement will lead to better utilization of the renewable energy resources, the results of this project become especially topical. Results expected from the project would substantially contribute to the faster development of modern energy efficient power electronics and reliable and sustainable power engineering, considering the growing impact of dispersed generation.

1.3 Aims, Hypotheses and Research Tasks of the Thesis

The main aim of this PhD research is to develop and experimentally validate new methods, topologies, control algorithms, and design guidelines aimed at the reduction of semiconductor power losses and, consequently, efficiency improvement of the galvanically isolated qZS DC-DC converters. It is expected that outcomes of the research will substantially contribute to the further development of the emerging field of the galvanically isolated impedance-source DC-DC converters.

Hypotheses

- Since the qZSC is a step-up converter, its operation is always connected to the low voltage and high current values at the input side, which lead to high power losses in the front-end qZS inverter. Such methods of power loss reduction as zero voltage and zero current switching performed by means of resonant switching, and advanced shoot-through generation methods could minimize the switching losses of the front-end inverter and enhance the dynamic performance of the qZSC.
- Diode of the qZSN is the main contributor of losses in the qZSC and its replacement by the synchronous low $R_{DS(on)}$ MOSFET will result in an efficiency rise of the converter by more than 1% within the entire operating range of the converter.
- Combined application of the synchronous qZSN and synchronous (active) VDR will not only improve the efficiency of the converter but also extend its flexibility by adding the bidirectional operation capability without any modifications in the hardware.

Research tasks

- Analysis of semiconductor power losses and systematization of efficiency improvement techniques for the galvanically isolated qZS DC-DC converters.
- Analytical and experimental study of different techniques of the ZCS and ZVS performance enhancement for switching loss reductions in the front-end qZS inverter.
- Analytical and experimental study of possibilities of reducing semiconductor conduction losses by the implementation of the synchronous qZSN and synchronous (active) VDR.

1.4 Research Methods and Instruments

The steady state analysis based on the ampere-second balance in capacitors and volt-second balance in inductors was used first to estimate analytically power losses in semiconductors. Studies with numerical simulations were performed using the models developed in the PSIM simulation software. Its add-on *Thermal Module* was used to assess conduction and switching losses. Simulation results obtained correspond to those in the experimental study, since models of semiconductor components obtained using *Thermal Module* are based on the device datasheet values [18].

Experimental verification of the theoretical predictions was conducted using the laboratory prototypes rated for the maximum input power of 300 W. The digital phosphor oscilloscope Tektronix DPO7254 along with the split-core AC/DC current probes Tektronix TCP0030, Rogowski coil current probe PEM CWTUM/015/R and high-voltage differential voltage probes Tektronix P5205A were used to capture operating waveforms (Figure 1.11). The efficiency of experimental converters was calculated using Eq. (1.8) as a ratio between the input and output powers of the converters, which were measured by means of the precision power analyzers Tektronix PA1000.

$$\eta = \frac{P_{OUT}}{P_{IN}} \cdot 100\% = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} \cdot 100\% \,. \tag{1.8}$$

Generalized specifications of semiconductor components used in the simulation models and the experimental prototype are presented in Table 1.2. The operating parameters of the qZSC were set according to the data presented in Table 1.3.

Table 1.2. Semiconductor components selected for simulations and experiments.

Component	*Type*	*Specifications*
$S_1 \ldots S_4$, S_{qZ}	*Vishay Si4190ADY*	V_{DS}=100 V, $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, Q_g=20.7 nC, R_g=2.2 Ω
D_{qZ}	*Vishay V60D100C*	V_{RRM}=100 V, V_F=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_{r1}, D_{r2}	*CREE C3D02060E*	V_{RRM}=600 V, V_F=1.8 V $I_{F(AV)}$=4 A
S_5, S_6	*ROHM SCT2120AF*	V_{DS}=650 V, $R_{DS(on)}$=120 mΩ I_D=29 A, Q_g=61 nC, R_g=2.5 Ω

The power losses and efficiency were generally estimated in four test points, with operating conditions described in Table 1.4. The load resistor R_{ld} was adjusted to achieve the maximum input current in each operating point.

Table 1.3. Generalized operating parameters of the experimental prototypes.

Parameter	*Symbol*	*Value*
Input voltage range, V	V_{IN}	*15…30*
Maximum input current, A	I_{IN}	*8*
Peak DC-link voltage in the boost mode, V	$V_{DC(peak)}$	*30*
Output voltage, V	V_{OUT}	*240*
Switching frequency, kHz	f_{sw}	*100*
Operating frequency of qZSN, kHz	f_{qZS}	*200 (2 f_{sw})*
Transformer turns ratio	n	*1:4*
Leakage inductance of the transformer, µH	L_l	*0.5*
Magnetizing inductance of the transformer, µH	L_m	*30*
Capacitance of qZSN capacitors, µF	C_{qz1}, C_{qz2}	*26.4*
Inductance of qZSN inductors, µH	L_{qz1}, L_{qz2}	*22*
Capacitance of output capacitors, µF	C_{f1}, C_{f2}	*2.2*

Table 1.4. Shoot-through duty cycle and operating power in the selected test points.

Test point	*1*	*2*	*3*	*4*
V_{IN}, *V*	*15*	*20*	*25*	*30*
I_{IN}, *A*	*8*	*8*	*8*	*8*
D_{ST}	*0.25*	*0.167*	*0.083*	*0*
P, W	*120*	*160*	*200*	*240*

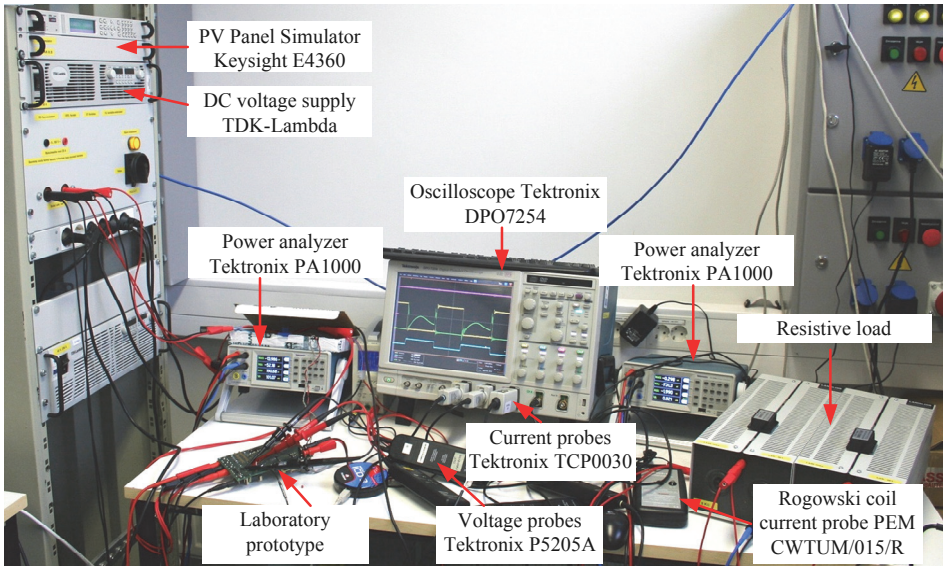


Figure 1.11 Photo of the test bench assembled for the experimental work within the PhD project.

1.5 Contribution of the Thesis and Dissemination

The aim of this thesis was to advance the family of galvanically isolated impedance-source DC-DC converters [PAPER-V] with special emphasis on the semiconductor power loss reduction and efficiency improvement of the qZSCs. The results obtained comprise both scientific and practical novelties.

Scientific novelties

- systematization and analysis of the current state-of-the-art topologies, control methods and development trends of the galvanically isolated impedance-source DC-DC converters;
- development and experimental validation of six novel shoot-through generation methods for the qZSCs (yellow background on the classification shown in Figure 1.12);
- development and experimental validation of three novel topological variations of the qZSCs (yellow background on the classification shown in Figure 1.13).

To underline the contributions of the given PhD research project to the development of the qZSCs with full-bridge switching stage, the classifications of shoot-through control methods (Figure 1.12) and topologies (Figure 1.13) in the prior research (white background) were extended by the main theoretical novelties of the project (yellow background).

Practical novelties

- design guidelines for the proposed topologies aimed at the reduction of semiconductor power losses and efficiency improvement of the qZSC,
- recommendations for the control system design to realize complex shoot-through control algorithms [PAPER-VII],
- recommendations for the elimination of the discontinuous conduction mode in the qZSC by replacement of the qZS diode by a N-channel MOSFET.

Practical results were mostly oriented to the Estonian industrial company Ubik Solutions, which is currently developing a new Smart Microinverter for the residential PV applications based on the results of this PhD project.

All the results obtained during the PhD research were reported at 6 international conferences and workshops and published in 11 papers. Four of them have appeared in international peer-reviewed journals and four are currently available in the IEEE explore database. The most important papers directly connected to the topic of the dissertation are listed in the List of Author's Publications.

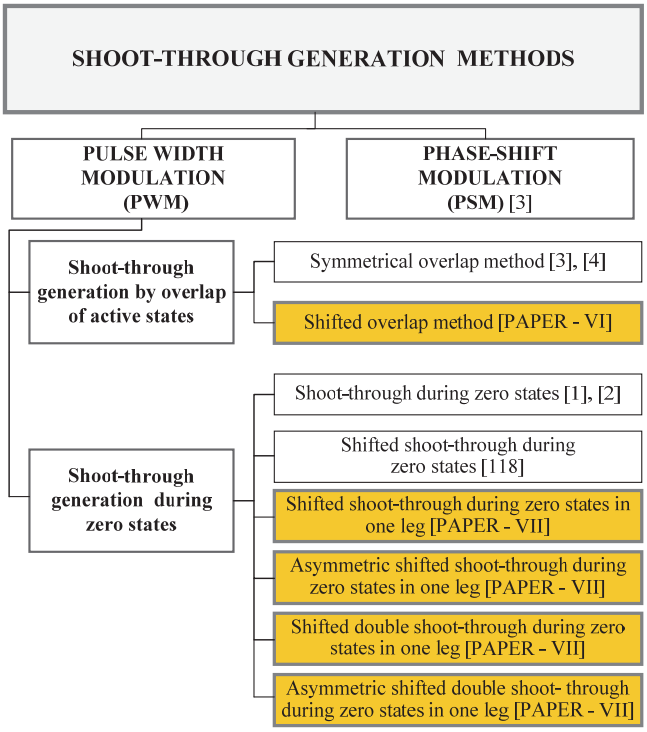


Figure 1.12 Classification of shoot-through generation methods.

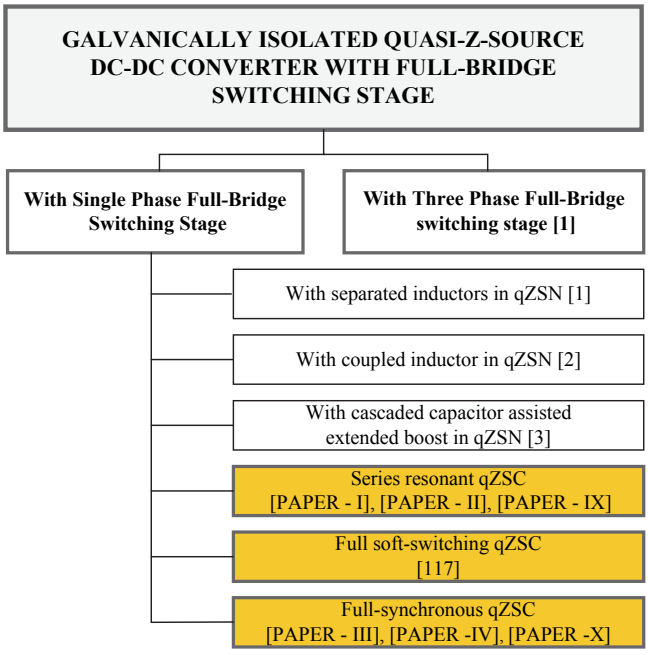


Figure 1.13 Classification of qZSCs.

2 SEMICONDUCTOR POWER LOSS REDUCTION TECHNIQUES IN GALVANICALLY ISOLATED DC-DC CONVERTERS

It is known that semiconductor components contribute to the total power loss of any converter. They occur mostly due to non-ideal switching processes and voltage drop in the conducting state. Those losses could be decreased using different techniques, which can be classified into techniques for reduction of switching and conduction losses. This section discusses power losses in semiconductor components and common methods of their reduction.

2.1 Power Losses in Semiconductors

Power losses in semiconductor components could be divided broadly into two types: switching and conduction losses. Switching losses occur during switching transients, while conduction losses are observed in the static condition of a semiconductor component.

Modern power electronic converters use mostly Si MOSFET or IGBT switches for low voltage applications [19]. Si MOSFETs have advantages in applications with blocking voltages required up to 600 V, while Si IGBTs are used above that level. The first can achieve much higher switching frequency since it uses only major carriers and thus achieves fast switching times. IGBTs have longer fall and rise times, since they employ also minor carriers and thus feature lower voltage drop in applications with blocking voltages over 1000 V. Also, IGBTs feature a "current tail" effect that results in high turn-OFF losses.

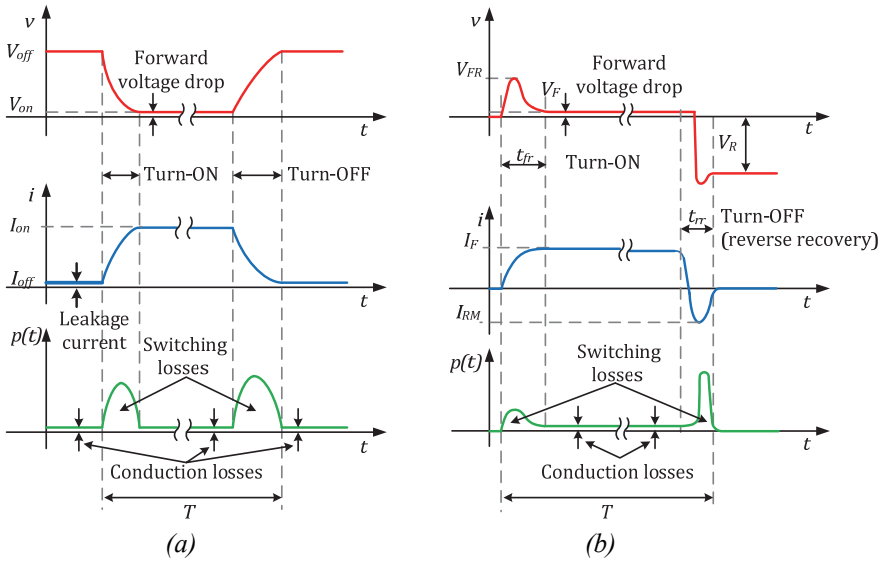


Figure 2.1 Typical switching processes and power losses in semiconductor components: transistor (a) and diode (b).

Typical switching processes of a switch are shown in Figure 2.1*a*. During turn-ON and turn-OFF states, the voltage and current of the switch are overlapping [20]. It results in high instantaneous power dissipated in the switch. Small conduction losses could occur in OFF-state due to leakage current. They are negligibly small for modern low voltage switches (up to 1200 V). Major part of the conduction losses are caused by forward voltage drop or ON-state resistance for IGBTs and MOSFETs, respectively. Modern trends in power semiconductor technology are towards their reduction.

The diode has another source of losses. In ON-state, conduction losses are caused by the forward voltage drop V_F, while there are practically no losses in OFF-state, as shown in Figure 2.1*b*. Magnitude of the voltage overshoot during turn-ON is called forward recovery voltage. It is caused by the conductivity modulation process in the p-n junction when the number of carriers is rising [21]. The major part of switching losses in the modern Si diode is introduced with the reverse recovery process during turn-OFF. Recombination of carriers in the p-n junction causes high current peak of short duration in the reverse direction. The area inside the reverse recovery current spike is a reverse recovery charge that is dependent on the diode type, forward current and reverse voltage in the given case.

Typical switching waveforms shown in Figure 2.1 describe the so-called hard-switching. This term refers to high instantaneous power dissipated in a switch or a diode during switching transients. Switching performance can be substantially improved if the overlapping of current and voltage is diminished. Switching of a semiconductor device is called *soft* if in contrast to hard-switching, it leads to dissipation of considerably smaller power in the component during switching transients.

2.2 Switching Loss Reduction Techniques

Historically, the first soft-switching converters were proposed in the 1920s [22]. Intensive research in this field was initiated only in the 1980s, when power electronics became an integral component of consumer electronics products and a key technology for modern energy generation and storage systems.

Numerous soft-switching techniques are available that could be used to minimize switching losses of a converter. Not all of them are applicable to the isolated full-bridge converter family. Moreover, a soft-switching technique is often designed to be used only within voltage- or current-source converters. This subsection describes the concept of soft-switching and soft-switching techniques used in galvanically isolated current- and voltage-fed full-bridge DC-DC converters. Soft-switching possibilities of voltage-source topologies have been extensively studied. Majority of them are based on the interaction between at least one inductor and a capacitor. In resonant converters, this interaction affects the whole switching period and thus results in higher voltage or current stress of semiconductor components and circulating power. In modern soft-switching techniques, like zero current transition (ZVT) and zero voltage transition (ZCT), resonance is controllable and utilized only during

switching transients. In contrast to the resonant topologies, this leads to the reduction of current and voltage stress in switches, but their implementation requires more components.

2.2.1 Fundamentals of Soft-Switching

The simplest way to describe differences in the switching transients of soft- and hard-switching is to draw a switching trajectory of a semiconductor component. Usually in hard-switched converters, the semiconductor components suffer from current overshoot during turning ON and voltage overshoot during turning OFF, as shown in Figure 2.2 [23]. There are two points, ON and OFF that describe the static conditions of the semiconductor component in turn-ON and turn-OFF states correspondingly. Any transition between these points is a switching, either hard or soft. The area under switching trajectory is proportional to the switching losses. Switching trajectory can be improved if a snubber is applied to the semiconductor component. However, the simplest passive snubbers are dissipative and commonly used for damping of parasitic oscillations. Non-dissipative snubbers are more complicated, while they provide better efficiency due to parasitic energy regeneration to the input or output side of the converter [24]. Snubbered switching is more advantageous than hard-switching, while it provides higher losses than those of soft-switching. The soft-switching requires the switching trajectory to be as close to the I-V axis as possible to minimize the switching losses. Commonly, it is obtained by means of lowering the current or voltage rise/fall slope depending on the application.

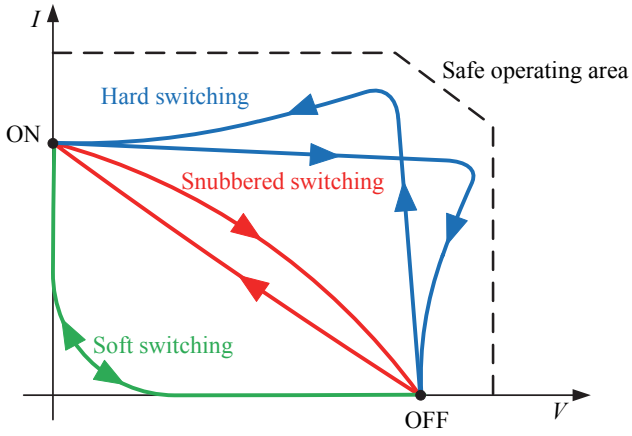


Figure 2.2 Typical switching trajectories of semiconductor components [23].

In power switches, switching occurs when the gate signal is changed. There are two types of soft-switching transients: zero voltage switching (ZVS) and zero current switching (ZCS). ZVS turn-ON and turn-OFF are defined in Figure 2.3*a*. ZVS turn-ON can be easily achieved if a body or an antiparallel diode is conducting prior to the change of the gate voltage V_G, while ZVS turn-OFF usually requires a parallel capacitor that could be partially or fully

substituted with the output capacitance of the switch [19]. Thanks to these conditions, the voltages across the switch are shifted from the switching transition interval, and thus overlap voltage and current, i.e. switching losses, are minimized. ZCS could be described as shown in Figure 2.3*b*. Usually, ZCS and ZVS in galvanically isolated full-bridge DC-DC converters are achieved with the assistance of external inductance, for example, transformer leakage inductance [25]. In the case of ZCS, additional elements may be required to keep switch current equal to zero until gate voltage changes. It could be a diode connected in series with the switch that performs ZCS.

Soft-switching type of a diode is not easily defined with regard to transistors, since they do not have control signal input. Soft-switching of a diode could be assisted with series inductance that decreases current rise/fall slope. In this case, a diode is switching naturally, which is equivalent of ZCS. Another possibility is to add a capacitor in parallel with a diode to decrease voltage rise/fall slope that leads to ZVS.

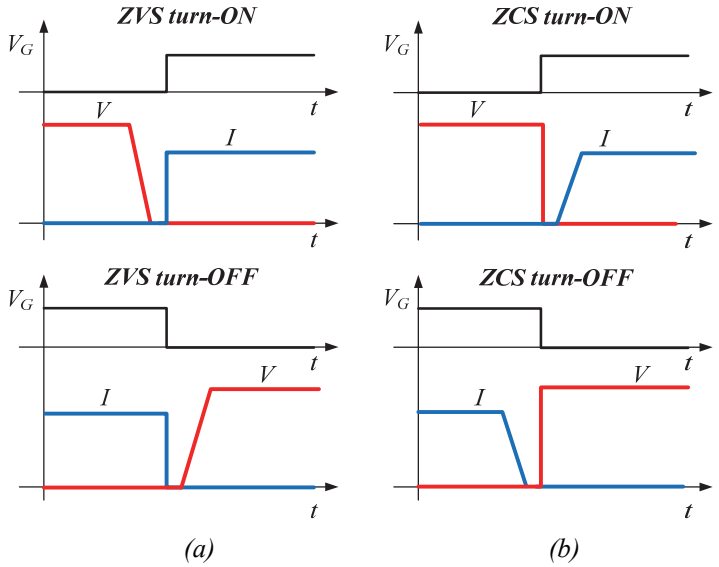


Figure 2.3 Definitions of zero voltage (a) and zero current (b) of a switch.

Only some types out of a large variety of soft-switching techniques could be utilized in galvanically isolated full-bridge DC-DC converters. Applicability of soft-switching techniques is restricted mostly due to series connection of the switches that requires transitions between active, zero, and free-wheeling states. In the active state, one pair of diagonal switches is conducting and thus transfers energy to the output. In the zero state, either both top or bottom switches are conducting. In practice, only one switch turned-ON could be enough to achieve the zero state due to the conduction of the diode in another switch, caused by the leakage inductance. In a free-wheeling state, all the switches are turned OFF. However, an equivalent of the active state could appear within a free-wheeling time interval caused by diodes conducting leakage inductance current to the input side.

2.2.2 Special Control Methods for Soft-Switching without Topology Changes

Voltage-source converters

A variety of possible switching conditions together with typical features of galvanically isolated full-bridge DC-DC converters leads to inherent soft-switching possibilities. In this thesis, the MOSFET-based converters are discussed. Any MOSFET has output capacitance and a body diode. They can interact with leakage inductance to achieve soft-switching conditions. In this case, no additional components are required, while the control of switches is crucial for the soft-switching. There are nine modulation strategies for voltage-source galvanically isolated full-bridge converters [25]. Among them, three strategies feature simultaneous turn-OFF of the diagonal switches, while six others do not. It was proven that soft-switching is achievable only for those six modulation strategies with staggered turn-OFF time of diagonal switches [26]. This allows appropriate utilization of zero states. Depending on the modulation strategy, zero state can provide nearly constant current of the leakage inductance or reset to zero of this current.

The basic voltage-source galvanically isolated full-bridge DC-DC converter is shown in Figure 2.4. Capacitors in parallel with switches could be substituted fully or partially by the output capacitance of a switch. Here transistors in the first leg (S_1 and S_2) turn-OFF before the corresponding diagonal transistors in the second leg (S_3 and S_4). Thus, the first leg is called leading, while the second is lagging. Since leakage inductance current is high when the first leg performs switching, it is easy to perform ZVS and practically impossible to achieve ZCS in the leading leg.

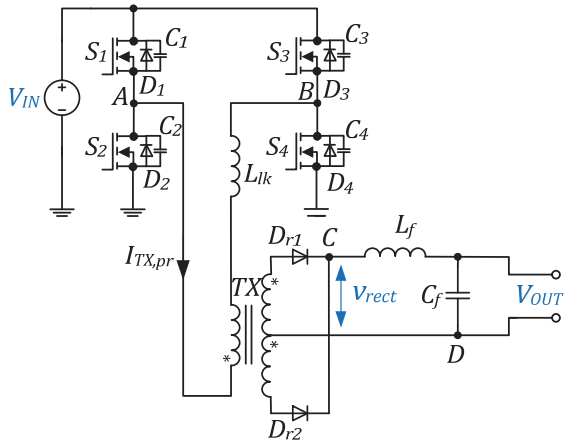
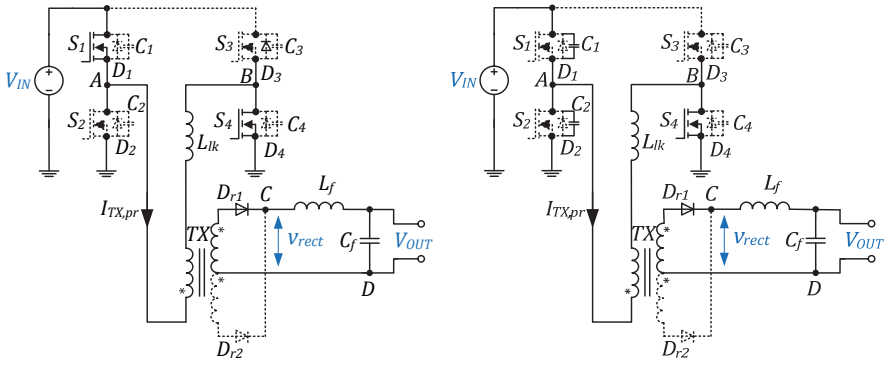


Figure 2.4 Voltage-source galvanically isolated full-bridge DC-DC converter [25].

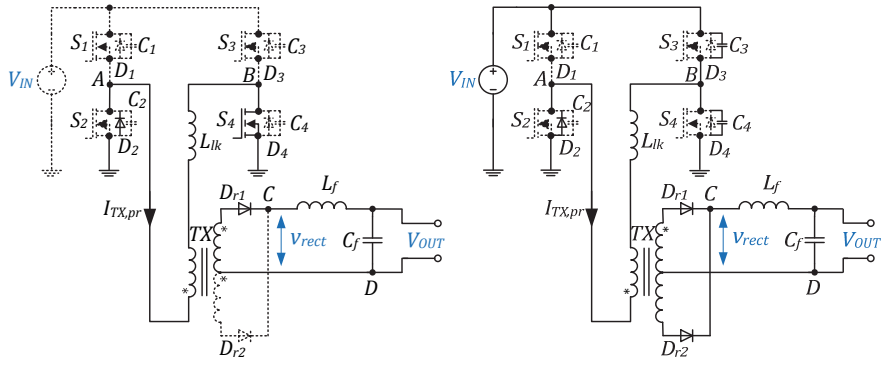
Implementation of ZVS in the leading leg is shown in Figure 2.5. At the beginning, the FB switching stage is in the active state (Figure 2.5*a*). Then switch S_1 is turning OFF that leads to charging C_1 and discharging of C_2 (Figure 2.5*b*). When the voltage of capacitor C_1 reaches V_{IN}, the body diode D_2

will start conducting and the converter will be in the zero state. S_2 could be turned ON then with ZVS. The principle of ZVS in a lagging leg is quite the same (Figure 2.6). It begins from the zero state that is shown in Figure 2.6*a* when D_2 and S_4 are conducting. After that switch S_4 turns OFF. Diode D_3 will start conducting when C_4 is charged up to V_{IN}. It will happen only if leakage inductance has enough energy.



(a) *(b)*

Figure 2.5 ZVS implementation in the leading leg: active state before switching (a) and soft-switching during deadtime (b) [25].



(a) *(b)*

Figure 2.6 ZVS implementation in the lagging leg: zero state before switching (a) and soft-switching during deadtime (b) [25].

Inherent soft-switching possibilities provide an opportunity to implement a soft-switching converter without additional components, utilizing only parasitic elements and an appropriate control algorithm. A phase-shifted full-bridge converter performs ZVS in both legs, as shown in Figure 2.7. It is one of the most commonly used converters in industry. However, utilization of solely parasitic elements leads to a narrow soft-switching range. In this case, ZVS conditions for the lagging leg can be achieved only around full load, while the

leading leg can perform ZVS up to a light load. Also, ZVS operation leads to higher current stress of switches due to circulating energy [27].

One of the possibilities to improve ZVS range is to increase the leakage inductance value, but this will lead to an increased duty cycle loss that occurs at intervals [t_2;t_5] and [t_8;t_{11}], highlighted with grey color. Merely control system modification is not enough to achieve a wide ZVS range. Numerous auxiliary circuits that operate as current sources assisting capacitors charge/discharge in ZVS have been proposed [28]-[37].

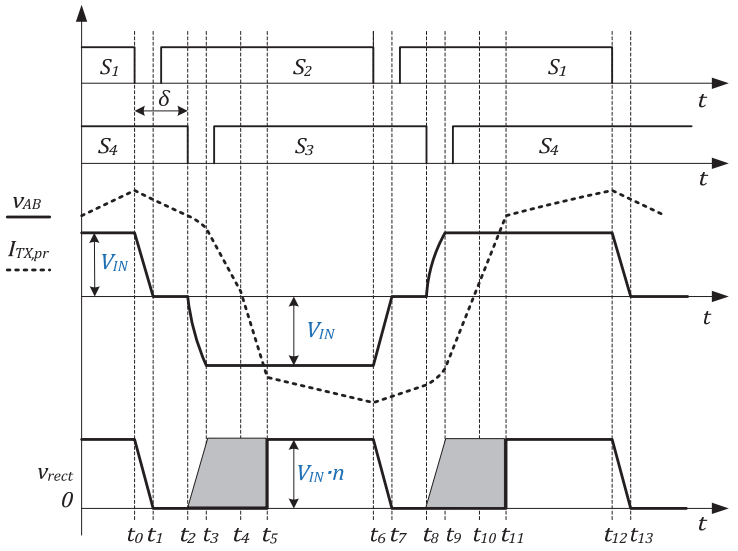


Figure 2.7 Operating waveforms of phase-shifted full-bridge DC-DC converter [25].

Another possibility of inherent soft-switching is to perform ZCS in the lagging leg, thus achieving zero voltage zero current switching (ZVZCS). ZCS is a preferable solution for IGBTs and thus ZVZCS converters have been proposed for high power applications. The conditions for this mode could be lost at high load operation. Meanwhile, current of the leakage inductance has to drop to zero before the change of the switching state in the lagging leg and has to be prevented from changing polarity. The simplest solution would be to connect diodes in series with lagging leg transistors [38]. Capacitance of these switches has to be minimized. Also, a capacitor is required in series with transformer winding to limit the current slope. Range of ZVZCS operation can be improved with the application of a saturable inductor [39], active clamping circuit at the secondary side [40], auxiliary winding at the output side [41], and current-reset circuit at the secondary side [42], [43].

Voltage-fed converters have another inherent possibility of soft-switching reported in [44]. Usually, voltage-source converters contain LC-filter for smoothing the output voltage. However, the unconventional topology with a capacitive output filter is shown in Figure 2.8. It reveals a new inherent feature of the voltage-source full-bridge converters: resonance between leakage inductance and capacitors of a voltage-doubler rectifier. This allows achieving

ZVS at the input side and ZCS at the output side in a wide range of loads without any additional components. The converter uses the same control principle as the conventional phase-shifted full-bridge converter, while circulating energy is minimized and thus high efficiency is obtained at light loads. Different results have been obtained in [45] for similar topologies with a modified control algorithm. DCM and boundary conduction mode (BCM) have been utilized to achieve ZCS of both inverter switches and rectifier diodes. However, this approach features higher circulating energy than the previous one.

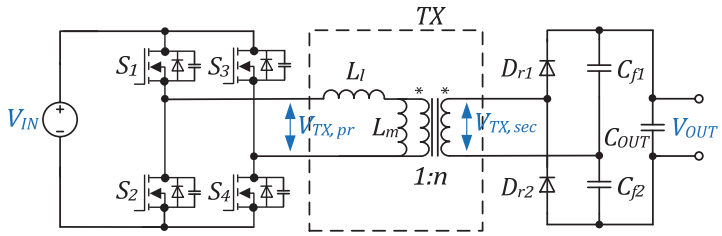


Figure 2.8 Phase-shifted full-bridge DC-DC converter with a voltage-doubler rectifier [44].

Current-source converters

Studies of current-source DC-DC converters have been less intensive than those of voltage-source. However, there are some similarities with voltage-source converters.

The first and the most obvious method to achieve soft-switching is to utilize the shoot-through states. It was first proposed in [46] to enhance the switching frequency of IGBT-based converters. Authors have proposed to handle a small part of shoot-through only by MOSFETs that have relatively high conduction losses and good dynamic performance to achieve ZVS of IGBTs, which are handling main current in the active state. It is dual to ZVS while the body diode of the MOSFET is conducting in the voltage-source converter.

Another inherent type of soft-switching could be achieved in a high power high voltage current-source converter, where the winding capacitance is sufficient to perform ZCS. The topology shown in Figure 2.9 has been derived from the voltage-source ZVS phase-shifted full-bridge converter described above using a duality principle [47]. Soft-switching is achieved due to local resonance between leakage inductance and windings capacitance during switching transients. This solution also suffers from the circulating power as its voltage-source counterpart.

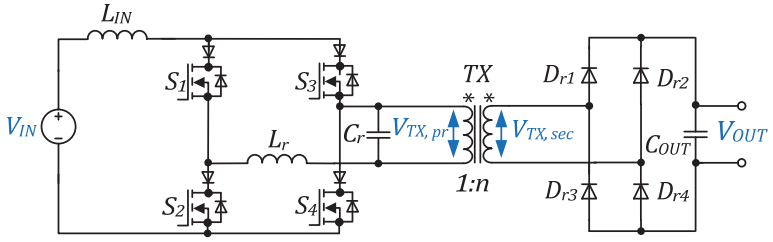


Figure 2.9 Current-source phase-shifted full-bridge DC-DC converter.

2.2.3 Hardware Methods for Soft-Switching without Change of the Basic Control Algorithm

All the soft-switching methods described before can be achieved without additional components through utilization of converter parasitic elements. Their range of soft-switching could be improved further with auxiliary circuits. Method described in this subsection require auxiliary circuits, while the power part of the converter usually is not changed and controlled with some of conventional PWM control algorithms.

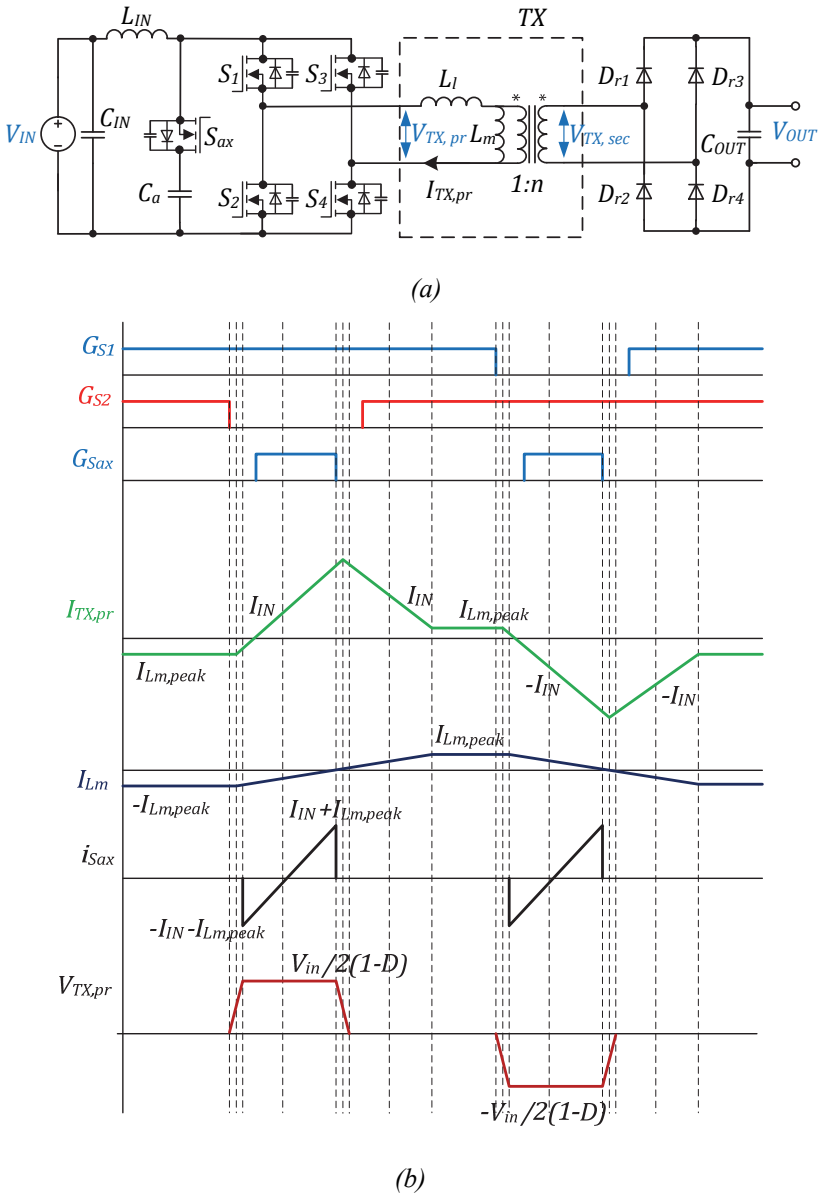


Figure 2.10 Active-clamped ZVS current-source full-bridge DC-DC converter [51].

This approach is commonly used for current-source converters. There is passive [48] and active clamping [49]-[51]. Active clamping has become popular since the end of the 1990s. First of all, active clamping has been used as a protection circuit from the voltage overshoot. It usually appears when the converter switches from the shoot-through to the active state due to mismatch in the currents of input and leakage inductors. The current-source converter (Figure 2.10*a*) operates with the conventional PWM control with symmetric overlap of active states (Figure 2.10*b*). The control system of an auxiliary switch is synchronized with this PWM control. Additional benefit of the active clamping circuit is the ZVS of inverter switches. A recent detailed analysis revealed additional support of the ZVS mode by the magnetizing current of the isolation transformer, which was described earlier [51]. However, ZVS conditions are dependent on the load level and the input voltage that is not useful for emerging applications. To improve ZVS operation range, several improved auxiliary circuits based on the active clamping principle have been proposed: with an auxiliary transformer connected to the output side [52], or to the input side [53].

This group of soft-switching methods is out of scope of recent research, since better results could be obtained with hybrid soft-switching methods, which are a modification of both hardware and control algorithm.

2.2.4 Hybrid methods for Soft-Switching with Modifications of the Control Algorithm and Topology

The most commonly used method in this group has been known for decades. It is resonant switching that implies insertion of a resonant tank into the converter and frequency control of the output voltage. There are three main types of resonant converters: series resonant (Figure 2.11*a*), parallel (Figure 2.11*b*) and series-parallel (LLC in Figure 2.11*c* and LCC in Figure 2.11*d*). However, resonant converters could be controlled also with conventional phase-shift modulation (PSM) [54]-[56]. Moreover, a combination of frequency control and PSM is used to improve efficiency at light loads [57].

Recently, LLC converters have attracted attention in the consumer electronics market as power supplies, while it requires additional efforts to calculate and design a control system with a wide range of switching frequencies. Despite complexity, it features a wide soft-switching range. It can be improved for wide output voltage and load regulation if an additional LC circuit is added to build an LLC-LC converter [58]. Parallel resonant converters suffer from high circulating energy even at light load and thus have low efficiency. They have not attracted much attention. Series resonant converters have been extensively studied and are commonly used. It is the simplest type of resonant converters and can be used to describe general principles of soft-switching possibilities in resonant converters.

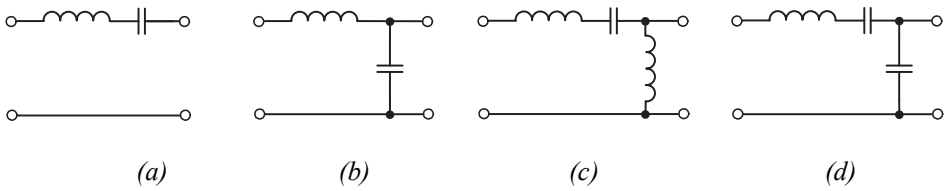


Figure 2.11 Resonant tank types: series resonant (a), parallel (b), and series-parallel LLC (c) and LCC (d).

Series resonant converters (SRC) are usually controlled with switching frequency either above or below the resonant one. Figure 2.12 represents the DC voltage gain characteristic of a SRC. Controllability of the SRC depends on the ratio between the resonant tank impedance and the load resistance. It is shown that the converter is virtually uncontrolled under light loads. That should be taken into account during the design of such converters. A normal mode when the converter has a switching frequency equal to the resonant one is the optimal operating point. In this case, the inverter feeds the resonant tank and the transformer with rectangular voltage pulses and sinusoidal current in phase with the rectangular voltage. In this case, inverter switches perform ZCS [20]. Operation below the resonant frequency leads to the hard turn-ON of diagonal switches and ZCS turn-OFF, as shown in Figure 2.13. Above the resonant frequency, the series resonant converter is expected to operate with hard turn-OFF, as shown in Figure 2.14. However, the inherent feature of the FB converter allows ZVS turn-OFF. It could be achieved when the dead-time between top and bottom transistor control is implemented, which leads to recharging of their output capacitances with the current of the resonant tank.

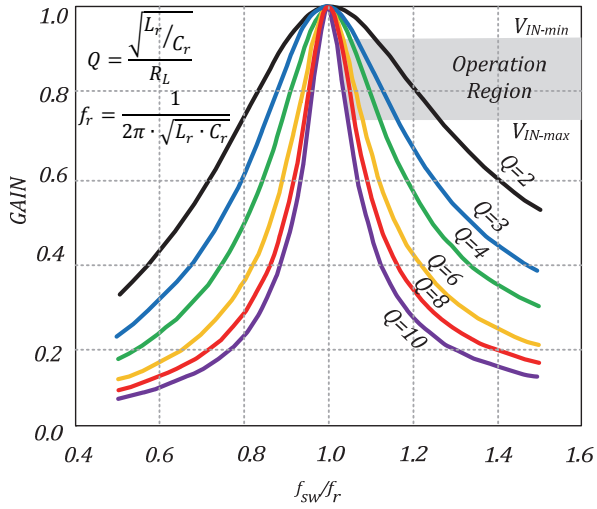


Figure 2.12 DC voltage gain characteristic of a SRC.

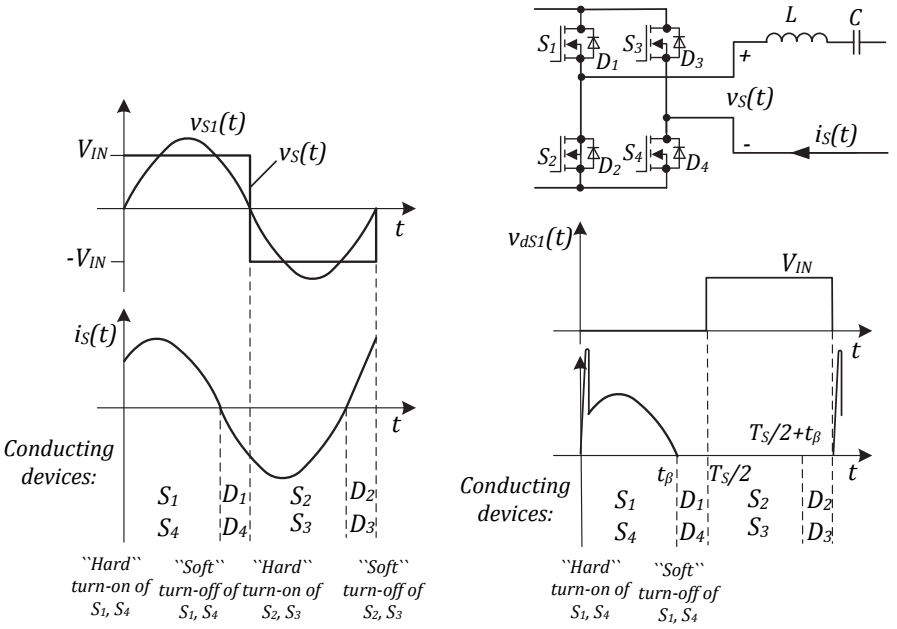


Figure 2.13 Operation of switches in a SRC below resonant frequency [20].

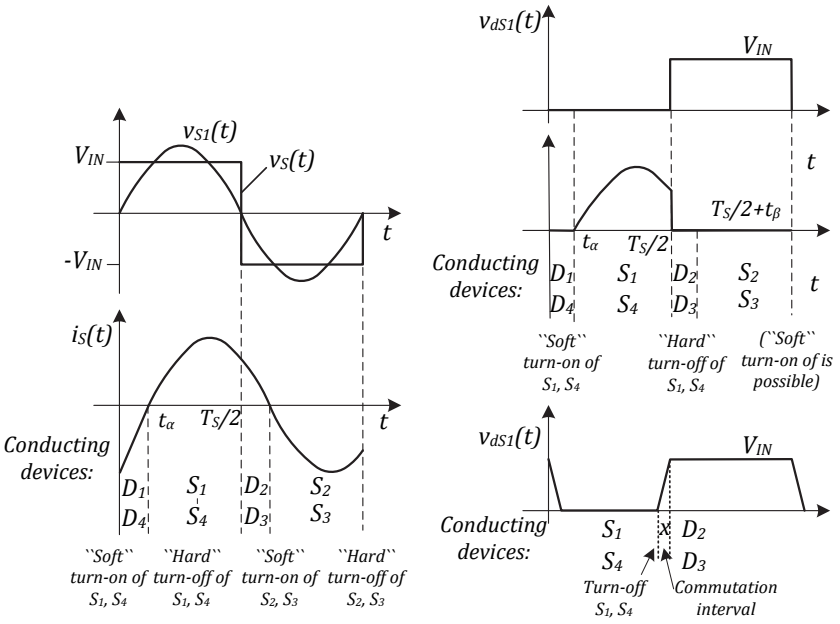


Figure 2.14 Operation of switches in a SRC above resonant frequency [20].

Since the resonant switching could be applied to both current-source and voltage-source converters, it seems to be applicable for impedance-source converters as well. All the other methods described require additional analysis.

ZVT and ZCT techniques are commonly used in modern high performance converters. They require additional active auxiliary circuits with an internal switch to utilize local resonant provided by additional components. However, it is not the case for current-source converters. The converter shown in Figure 2.15 has been proposed in [59]. The basic topology is modified by addition of an active snubber in series with the transformer primary winding. Basically, an active snubber is a four-quadrant switch with a bypass capacitor. The capacitor is bypassed by the four-quadrant switch or conducting leakage inductance current depending on the operation mode, while it is adapted to the load level. Such solution is complicated because of the number of semiconductor components. However, it allows snubber capacitor energy recuperation to the load. Main switches achieve ZCS, while snubber switches operate under ZVS with minimal additional current stress. It may be advantageous for applications with high output voltage.

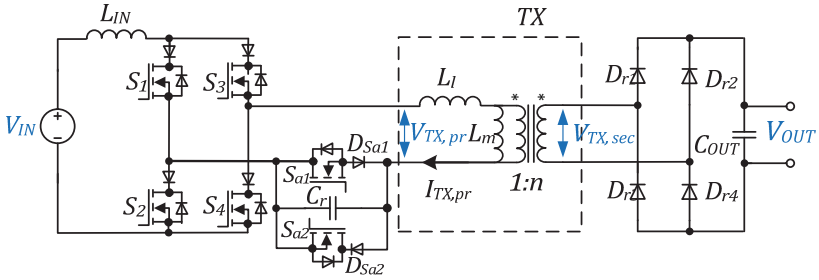


Figure 2.15 ZCS current-source full-bridge DC-DC converter with an active snubber [59].

Another possibility that could be used in both types of converters and expectedly in impedance-source converters is the implementation of active switches, instead of diodes, in the secondary side [60]. Several systems with active secondary switches and additional snubbers have been proposed recently. They feature inherent soft-switching possibilities by utilizing leakage inductances [61]. For example, a converter proposed in [62] features ZVS of the output side switches and ZCS of the input side switches. The topology of the converter is shown in Figure 2.16*a*. Series diodes are needed at the input side to assist ZCS caused by leakage inductance, while snubber capacitors at the output are used to slow down voltage rise/fall slope and thus achieve ZVS. However, a special control algorithm shown in Figure 2.16*b* is required to achieve soft-switching. It features special switching states, when three transistors are conducting, which is essential for soft-switching transitions between the shoot-through and the active state.

Soft-switching methods with fully controlled switches and a specific control algorithm are today's growing trends. They can easily achieve soft-switching in a wide range of a load and input voltage [62]. Moreover, modified topology with fully controlled switches has low conduction losses since an active rectification principle could be utilized.

The newest current-source topology proposed in [63] combines an interleaved boost, i.e. current-source, non-isolated converter and voltage-source LLC resonant converter, as shown in Figure 2.17. A two-phase interleaved boost integrated LLC resonant converter can achieve the ZVS of input switches, the ZCS of output diodes, low input current ripple and high conversion efficiency and switching frequency. Another benefit is the constant-frequency PWM control based on the asymmetrical PWM. However, it requires four magnetic elements: two input inductors, a resonant inductor, and an isolation transformer. Their design is complicated and mostly connected with ZVS operation at heavy loads that can be hardly achieved if high power density, i.e. small size of inductors, is required.

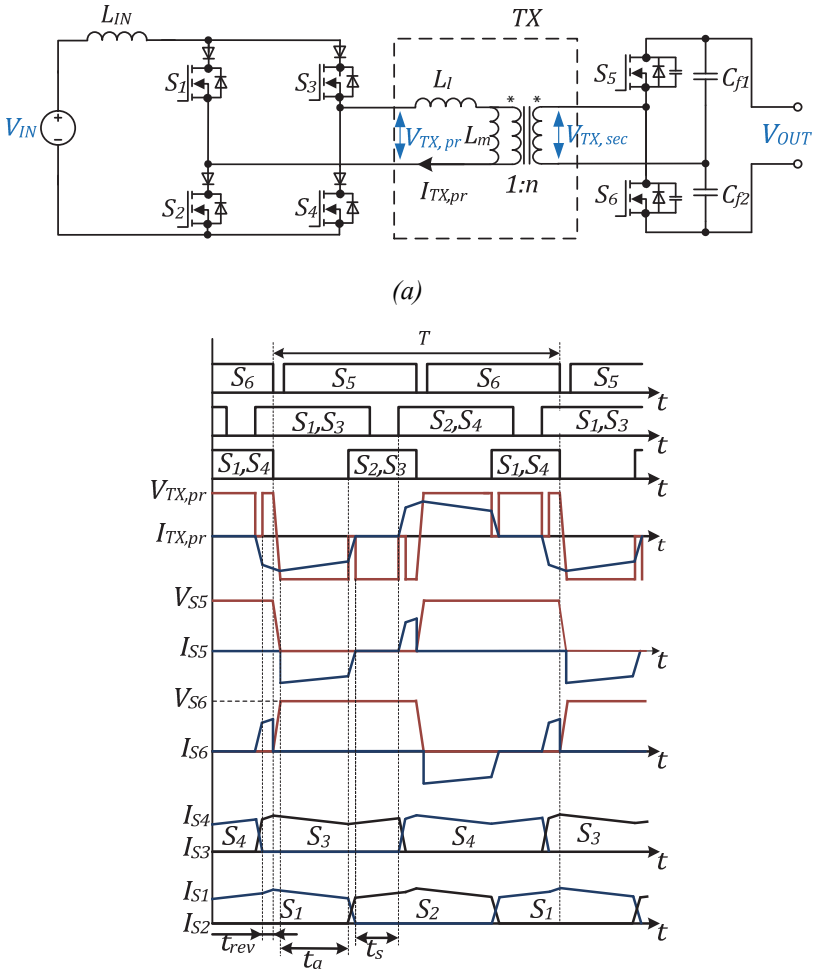


Figure 2.16 Full soft-switching high step-up current-source full-bridge DC-DC converter [62].

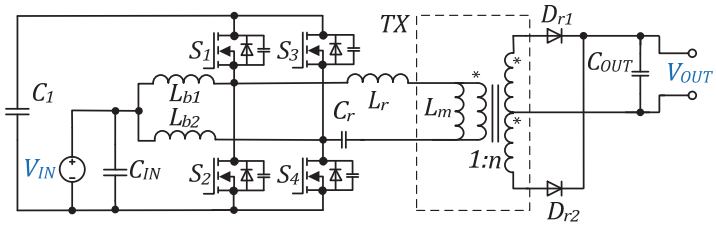


Figure 2.17 A two-phase interleaved boost integrated LLC resonant converter [63].

In this subsection, three types of soft-switching techniques were described. Their application possibilities for the galvanically isolated full-bridge DC-DC converters are analyzed. The series resonant principle seems to be the easiest to apply in the qZSC, since it is simple and influences only the current waveform of the isolation transformer in the active mode. Also, implementations with active output side switches could provide a wide range of soft-switching thanks to absence of forbidden states in the qZS inverter bridge and thus a wide variety of possible switching conditions can be utilized to achieve local resonance and soft-switching.

2.3 Conduction Loss Reduction Techniques

Conduction losses are caused by the saturation voltage or resistance of the switch, forward voltage drop of the diode, equivalent series resistance (ESR) of the passive elements, etc. Conduction losses are hard to avoid. Their minimization is usually done through an appropriate selection of the components taking into account price constraints. For example, in low-voltage high-frequency converters, Schottky diodes are usually employed owing to absence of reverse recovery losses and low forward voltage drop. Silicon Carbide (SiC) high-voltage Schottky diodes improve the efficiency of a high-voltage high-frequency converter due to negligible reverse recovery losses [64]. A SiC Schottky diode combined with an "industry accepted" super-junction MOSFET provides a cheap and efficient solution for high-voltage converters with a switching frequency up to 100 kHz [65], [66] . Further reduction of conduction losses can be achieved by two typical methods: parallel connection of semiconductor components and synchronous rectification.

2.3.1 Parallel Connection of Semiconductor Components

Voltage drop or resistance of a semiconductor component can be decreased if it employs several devices in parallel that are controlled simultaneously. The performance and requirements for paralleling of semiconductor devices strictly depend on their type. This approach is well known and has been first applied to IGBT based converters. IGBTs usually operate at switching frequencies up to 20 kHz and thus have low requirements for PCB design. IGBTs show satisfactory current balancing in non-demanding applications if a PCB is designed properly and devices are selected with derating [67], [68]. However, active gate control is required to achieve junction temperature control, even

distribution of currents, dv/dt, and di/dt control in applications where IGBTs suffer from cyclic thermal loading, or high switching frequency [69], [70]. Also, IGBTs can be used in parallel with MOSFETs to reduce conduction losses. Such connection is called a hybrid switch and has been first proposed for inverter applications [71]-[73].

Diodes can also be connected in parallel to reduce resulting forward voltage drop [74], [75]. Current balancing of diodes connected in parallel is more challenging than that for switches. It depends strictly on the PCB design [76], since current sharing can be unbalanced even if all diodes are identical. Even current sharing depends more on the physical connection structure of these diodes on the PCB [77]. In high power applications, connections require a busbar of special design [78].

Si MOSFETs are widely used for low and medium power applications with the DC-link voltages up to 400 V. Operating frequency of a MOSFET can exceed 100 kHz. This imposes additional requirements on their paralleling, since parasitic inductance shown in Figure 2.18 has considerable influence on current sharing at high switching frequencies [79]. Super-junction MOSFETs, which are popular for high-voltage applications, require no additional matching of ON-resistances, while even current sharing can be achieved through adjustment of gate resistors to equalize switching speeds of all transistors [80]. However, such matching is not practical in many cases. Then a variation of MOSFET parameters can lead to a worst case scenario with overheating or damage of one MOSFET among those connected in parallel. This situation requires additional analysis, as shown in [81].

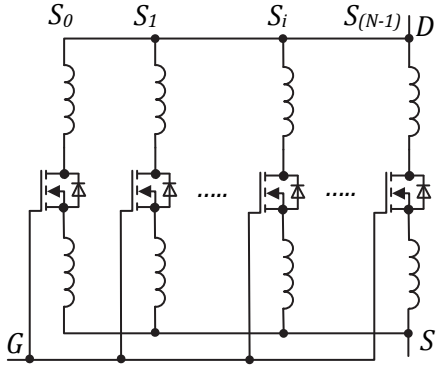


Figure 2.18 Parallel connection of MOSFETs [79].

Introduction of wide bandgap (WBG) materials for power electronics components has lifted operation voltages available for MOSFETs. For example, Silicon Carbide (SiC) MOSFETs rated for 1.7 kV are widely available now. The main difference of SiC MOSFETs from Si counterparts is significantly lower trans-conductance, faster switching, and lower conduction losses. However, higher trans-conductance and threshold voltage variations have limited its influence on current sharing of SiC MOSFETs connected in parallel

in the static mode. The sharing is nearly even if MOSFETs have similar characteristics. The value of ON-state resistance is the most influential. It has positive thermal dependence and thus provides better current sharing at high load or high temperature [82], [83]. In applications where dynamic performance of SiC MOSFETs connected in parallel is essential, the threshold voltage variations have to be compensated. Even current and losses sharing can be achieved if active control of gates is employed, when current distribution is balanced through adjustment of turn-ON delays between control channels [84]. Other available SiC devices on the market are JFETs, which are not easily paralleled. They have considerable variations of parameters and thus require independent driving circuits for each transistor to achieve reliable operation with effective paralleling [85]. Another WBG device, like GaN, could also be paralleled. However, this option is inadequately studied. Recommendations of their manufacturers are mostly related to minimization of the interconnection inductances [86].

Previously, all paralleled devices were considered to be controlled simultaneously. However, there is one more possibility available, i.e. interleaved control. It has been employed in a multidevice interleaved boost converter shown in Figure 2.19*a* [87]. The main idea is to switch only a single transistor simultaneously among those that are connected in parallel. This allows use of switches with better parameters that cannot handle the whole power of the converter. They suffer from high peak current stress, while average or rms current is within an acceptable region.

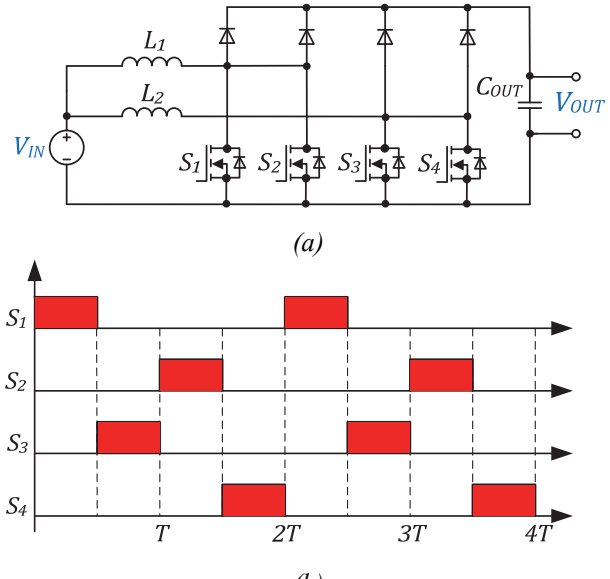


Figure 2.19 Multidevice interleaved boost converter: topology (a) and control principle (b) [87].

All techniques for reducing conduction losses with parallel connection of the semiconductor devices are associated with a higher component count. It leads to more complicated failure mechanisms [88], at the same time, to decreased reliability that has to be carefully analyzed for each converter with parallel connection of semiconductor devices [89]. This approach could be recommended in case a single-device implementation of a switch cannot handle converter power, or efficiency is of a higher concern than reliability.

2.3.2 Synchronous Rectification

Synchronous rectification is a well-known principle that employs MOSFETs with bidirectional current conduction possibilities, instead of diodes [20]. The main principle can be explained using a synchronous buck converter shown in Figure 2.20. Switch S_2 is inserted instead of a diode. Switches S_1 and S_2 are controlled complementary with dead time. The dead time is needed to avoid input supply short-circuit that could appear due to non-idealities of switches. Dead time allows separation of in time switching transients of both transistors. The body diode of the switch S_2 carries load current before the turn-ON of the switch S_1 or S_2. For better performance, the synchronous switch S_2 has to be properly selected [90].

Synchronous rectification is frequently used in step-down galvanically isolated converters with low-voltage high-current output, where conduction losses in the rectifier contribute most to efficiency drop [91]. Low voltage output allows use of the secondary winding voltage of the isolation transformer [92] - [94] or auxiliary winding [95] as the driving voltage of a synchronous switch. Such solutions are called self-driven and have been used in numerous conventional and resonant galvanically isolated step-down converters. Further improvement of synchronous rectification performance can be achieved with an employment of resonance [96].

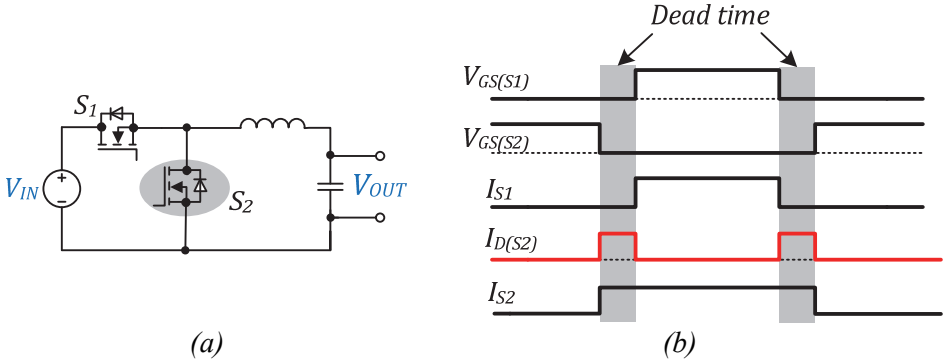


Figure 2.20 Synchronous buck converter (a) and its operation principle (b).

Proper selection of the dead time has crucial influence on the efficiency of a synchronous converter and thus has to be predefined after a comprehensive analysis [97]. Active control of the dead time can be beneficial in demanding applications with wide regulation and dynamic ranges. It can be achieved simply by the implementation of control circuit with sensors [98], [99] or

without them through utilization of a complicated control system [100]. Proper selection of dead time is especially important for converters that employ WBG semiconductor devices. For example, GaN transistors have considerable losses in a reverse conduction mode during dead time [101]. Optimal dead time depends on the type of the GaN transistor and load current, while it can be predicted with the model proposed in [102].

In summary, it has been shown by the author that conduction losses constitute a major part in the power losses in the galvanically isolated qZS full-bridge DC-DC converter [PAPER-VIII]. Implementation of synchronous rectification on the input side is highly advantageous. Utilization of active VDR could have minor influence on the improvement of efficiency if additional losses on its control and driving are taken into account. However, an active VDR can provide additional possibilities of soft-switching [62], [103], [104] and bidirectional power flow control.

3 SEMICONDUCTOR POWER LOSS REDUCTION AND EFFICIENCY IMPROVEMENT POSSIBILITIES IN GALVANICALLY ISOLATED qZS DC-DC CONVERTERS

This section is dedicated to development of new methods, topologies, control algorithms, and design guidelines aimed at the reduction of semiconductor power losses and, consequently, efficiency improvement of the galvanically isolated qZS DC-DC converters. All the proposed approaches were experimentally validated by help of laboratory testbench described in subsection 1.4.

3.1 Reduction of Switching Losses

3.1.1 Optimization of Control Strategies

This subsection discusses the influence of the shoot-through generation methods on the total efficiency of the qZSC. There are nine known shoot-through generation methods that are classified in Figure 1.12. Five out of the methods were proposed by the author. Four shoot-through generation methods proposed before are: PSM control principle with the shoot-through generation during zero states, PWM shoot-through control by the overlap of active states, PWM control with shoot-through generation during zero states and PWM control with shifted shoot-through generation during zero states. The operation principle of the first three of them was described in section 1 of the given thesis.

The methods known before and those proposed in this thesis are compared in this subsection by means of experimental measurement of efficiency for the MOSFET-based qZSC for low voltage applications. The IGBT-based converter may have a different curve of efficiency because of much higher switching losses in this type of switches, i.e. they have different loss breakdown [PAPER-VI], [PAPER-VII]. The main focus of this thesis is on the MOSFET-based converter. The four control methods were proposed at different times and different types of software have been used for our comparisons. The qZSC can perform active, open, and shoot-through state of the inverter. Each of the control strategies has its own sequence of these states during the switching period. Each isolated DC-DC converter has inherent soft-switching possibilities that depend on the switching sequence, leakage inductance of the transformer, output charge of a switch (Q_{OSS}), etc. Thus, each method will have its own efficiency curve over the input voltage regulation range.

This subsection summarizes new methods proposed in [PAPER-VI] and [PAPER-VII] and compares them with existing control methods by means of efficiency measured using the same experimental prototype with specifications described in Table 1.2. Efficiency measurements were performed over the entire input voltage regulation range of the converter, from 15 V to 30 V, at maximum

input current 8 A and with a partial load at the input current 4 A. All the new methods proposed in this thesis are within the PWM group.

Traditional shoot-through generation methods

Experimental waveforms for the PSM control principle with the shoot-through generation during zero states (Figure 1.3*c*) are shown in Figure 3.1. Zero state created by the phase shift between control signals has a fixed duration, and the shoot-through is implemented within this interval. Its duration is usually selected equal to the maximum shoot-through state duration given. Inverter switches feature a single ZCS turn-ON during the switching period. Leakage inductance of the isolation transformer assists the ZCS operation of the VDR diodes. The switching frequency of all transistors is two times higher than the operating frequency of the converter [2].

Experimental results for the PWM shoot-through control by the overlap of active states (Figure 1.3*a*) are shown in Figure 3.2. In this method the inverter bridge operates only in active and shoot-through states, while the zero state is totally eliminated. The inverter switches operate in the hard-switching conditions. The VDR diodes feature hard turn-ON and ZCS turn-OFF assisted by the leakage inductance of the isolation transformer. The switching frequency is the same as the converter operating frequency [2].

The same set of measurements was performed for the PWM control with shoot-through generation during zero states (Figure 1.3*b*), which is shown in Figure 3.3. The zero state duration is fixed and adopts shoot-through state when the voltage step-up is necessary. Here the top switches of the inverter operate with full soft-switching, while bottom switches feature only a single ZCS turn-ON assisted with the leakage inductance. Moreover, switching frequency of the hard-switched bottom transistors is three times higher. The VDR diodes operate with ZCS assisted with the leakage inductance.

The PWM control with shifted shoot-through generation during zero states (Figure 3.4) was proposed in [118] and experimental results for it are presented in Figure 3.5. The zero state is generated by either top or bottom transistors. In this case, bottom transistors generate the zero state. This control method is derived from the previous one by shifting one of the shoot-through states towards the active state. However, the number of switching transients during the switching period is lower than that in the previous case. All switches operate with a single ZCS during the switching stage: turn-ON for the top switches and turn-OFF for the bottom switches. The VDR diodes feature full ZCS operation.

The efficiency of the experimental prototype was measured over the entire input voltage regulation range at two values of the input current for these four control methods. The measurement results for four conventional control methods are presented in Figure 3.6. All of them have similar input current ripple since shoot-through occurs twice per switching period. The results obtained show that the PSM and the PWM control principle with the shoot-through generation during zero states have virtually equal efficiency curve, as shown in Figure 3.6*a* and *c*.

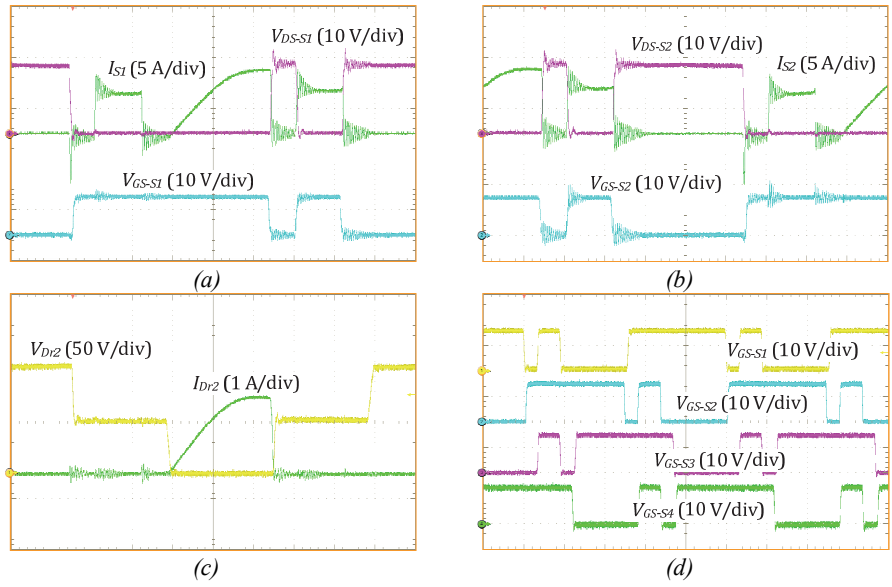


Figure 3.1 Experimental waveforms of the qZSC in the boost mode with the PSM control principle with shoot-through generation during zero states (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).

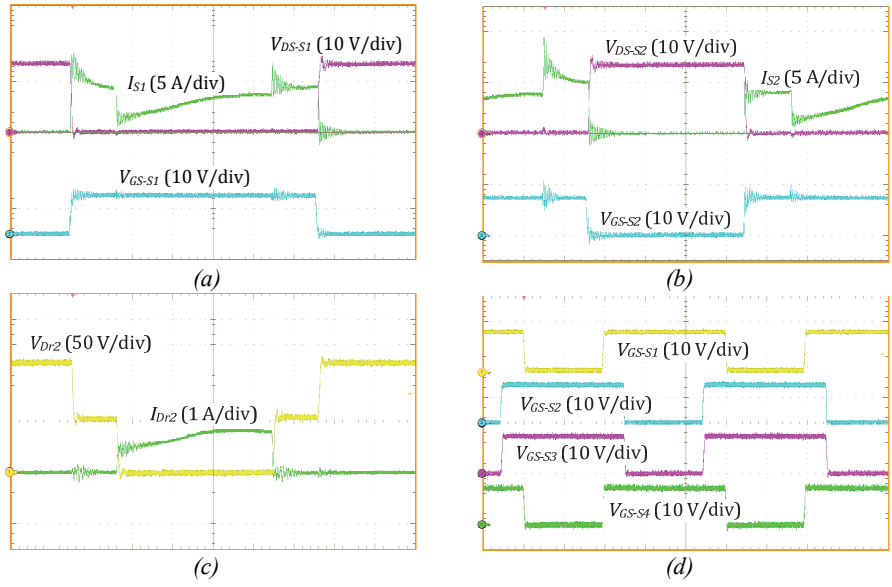


Figure 3.2 Experimental waveforms of the qZSC in the boost mode with the PWM shoot-through control by the overlap of active states (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of the VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).

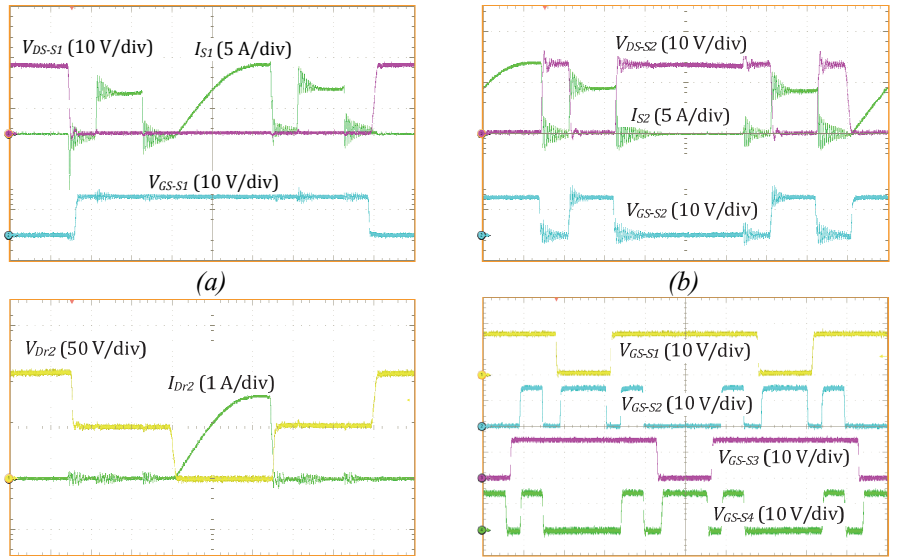


Figure 3.3 Experimental waveforms of the qZSC in the boost mode with the PWM control with shoot-through generation during zero states (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of the VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).

The reason is that despite different switching frequency of the switches, each leg has the same number of switching transients and nearly the same number of soft-switching conditions. The PWM control with shifted shoot-through generation during zero states shows slightly better efficiency at partial load (Figure 3.6*d*) due to the lower switching frequency of the inverter switches. The PWM shoot-through control by the overlap of active states has efficiency curves different from other conventional methods, as shown in Figure 3.6*b*. It operates with hard-switching on the input and output sides, which is not common for other methods. It is partially associated with the absence of zero states in the switching sequence. It leads to nearly equal total converter efficiency at the full and partial load. The control methods with zero states in the switching sequence are necessary when the converter is implemented with a higher order output side filter, like an LC-filter. The PWM control with shifted shoot-through generation during zero states is the most advantageous in terms of voltage step-up and efficiency. The PWM shoot-through control by the overlap of active states is advantageous for converters with a VDR. It suits for applications with wide load variations due to low efficiency variations with a load. Thus, these two methods were selected for further modification, which is mostly connected to shoot-through generation by a single leg.

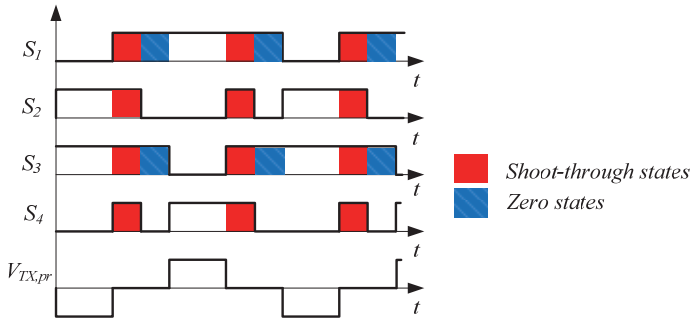


Figure 3.4 Sketch of the PWM control with shifted shoot-through generation during zero states.

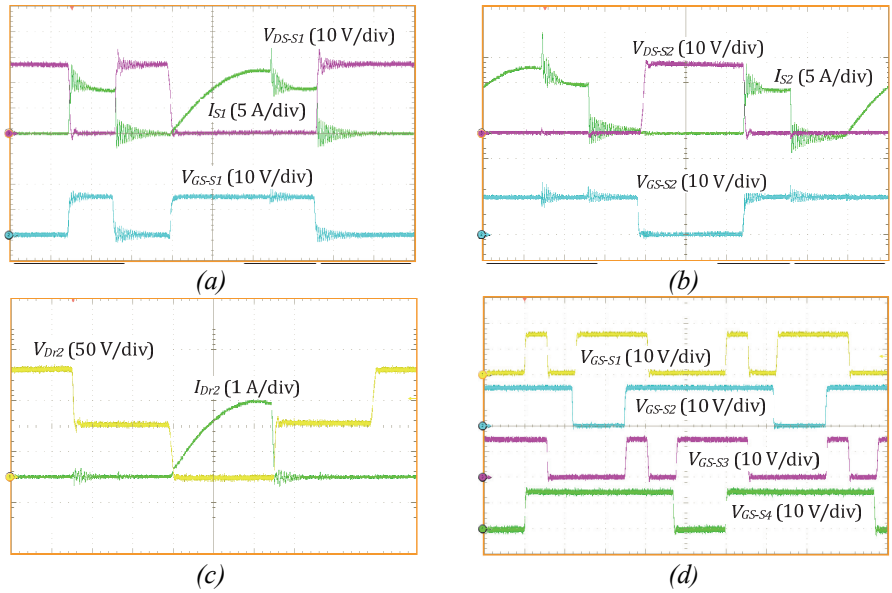
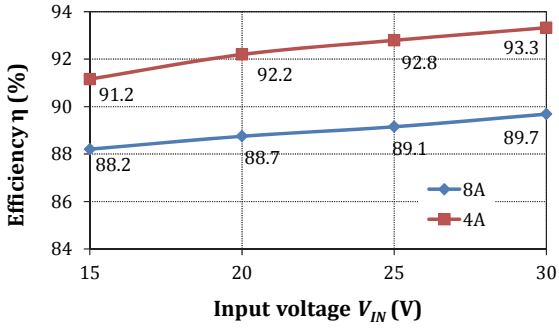
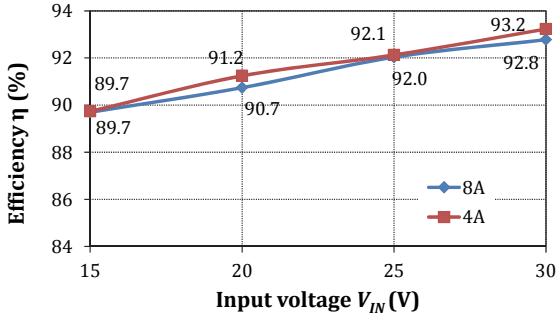


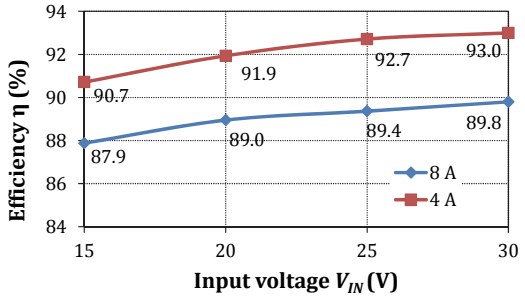
Figure 3.5 Experimental waveforms of the qZSC in the boost mode with the PWM control with shifted shoot-through generation during zero states (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of the VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).



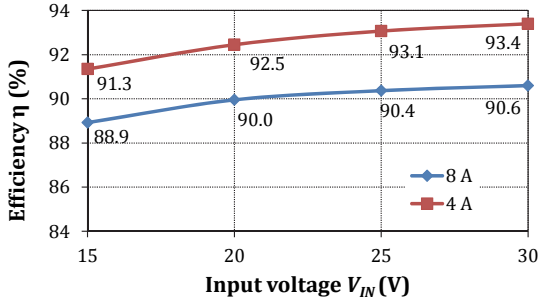
(a)



(b)



(c)



(d)

Figure 3.6 Measured efficiency of the qZSC that operates with: the PSM control with the shoot-through generation during zero states (a), the PWM shoot-through control by the overlap of active states (b), the PWM control with the shoot-through generation during zero states (c), the PWM control with shifted shoot-through generation during zero states (d).

Symmetrical and shifted overlap shoot-through generation methods

The PWM shoot-through control by the overlap of active states (Figure 3.7*a*) was further modified in [PAPER-VI]. The overlap can be performed only by a single inverter leg, as shown in Figure 3.7*b*. This modified method is called the PWM shoot-through control by the shifted overlap of active states. The experimental results obtained with this control method are shown in Figure 3.8.

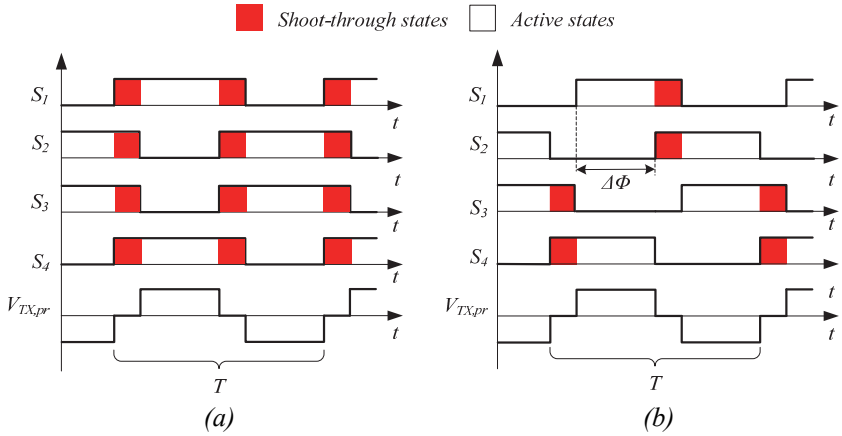


Figure 3.7 Sketch of the PWM shoot-through control methods: by the overlap of active states (a), and by the shifted overlap of active states (b).

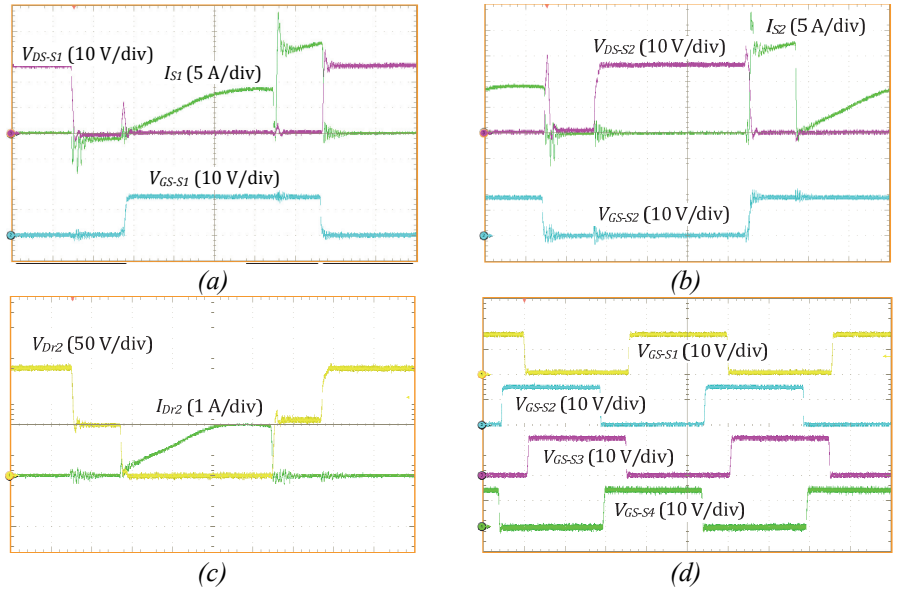


Figure 3.8 Experimental waveforms of the qZSC in the boost mode with the PWM shoot-through control by the shifted overlap of active states (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of the VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).

In PWM shoot-through control by the shifted overlap of active states the switching frequency of the switches still equals the converter operating frequency. The switching sequence contains only the shoot-through and active states. The shoot-through state occurs twice per switching period and is performed by a single leg. Also, turn-ON duty cycle of the inverter switches is fixed and is equal to 0.5. The shoot-through state is created by the phase shift between the control signals of the top and bottom transistors.

The experimental results show that inverter switches feature ZCS-ZVS turn-ON of the top switches and ZVS turn-OFF of the bottom switches. The VDR diodes operate under full soft-switching, where ZCS is assisted by the leakage inductance of the isolation transformer. Measured efficiency curves shown in Figure 3.9 differ from those of the reference converter (Figure 3.6*b*). With this control principle, losses in the inverter switches have different distribution. The conduction losses are higher, since the inverter bridge has higher resistance in the shoot-through mode. However, switching losses have to be lower due to the optimized switching sequence. The PWM shoot-through control by the shifted overlap of active states has slightly better efficiency at maximum input current than in reference control, while it is lower at partial power.

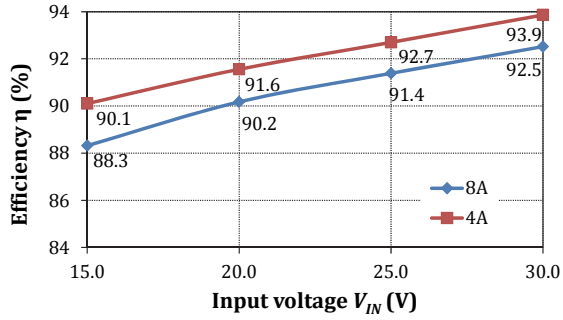


Figure 3.9 Measured efficiency of the qZSC that operates with the PWM shoot-through control by the shifted overlap of active states.

PWM Control with Shifted Shoot-Through

As it was shown before, the PWM control with shifted shoot-through generation during zero states (Figure 3.4) shows the highest efficiency among the PWM control methods with shoot-through generation during zero states. This section describes four novel control methods derived from it, which are presented in [PAPER-VII]. All of them feature the shoot-through generation only by a single inverter leg. This leads to a switching frequency lower than in the reference PWM control principle.

The PWM control with shifted shoot-through generation during zero states in one leg (Figure 3.10*a*) was derived from the reference PWM method by elimination of the short pulses in the control of the bottom transistors generating shoot-through. The experimental voltage and current measurements for this control method are shown in Figure 3.11. The top inverter switches feature ZCS

turn-OFF, while ZCS turn-ON assisted by the leakage inductance is evident in the bottom switches. The VDR diodes are switched with ZCS.

The asymmetric PWM control with shifted shoot-through generation during zero states in one leg (Figure 3.10*b*) was derived from the previous control method by moving active states towards each other and thus merging zero states into one. Zero state is placed between the shoot-through and active state. The experimental results (Figure 3.12) show that as compared to the previous method, a different arrangement of the switching sequence does not influence soft-switching conditions in the inverter bridge. Moved active states result in non-centered, i.e. asymmetric, form of the isolation transformer voltage. Different time intervals between the shoot-through states lead to additional harmonic components in the input current at the operating frequency of the converter. This control method also provides the ZCS of the VDR diodes.

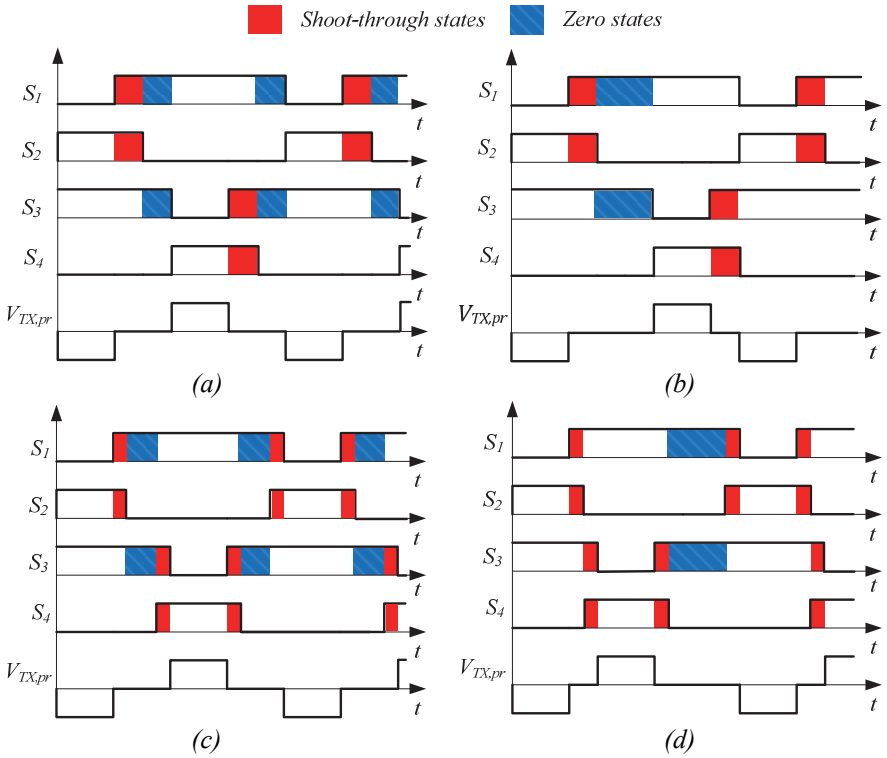


Figure 3.10 PWM control principles with shifted shoot-through: PWM control with shifted shoot-through generation during zero states in one leg (a), asymmetric PWM control with shifted shoot-through generation during zero states in one leg (b), PWM control with shifted double shoot-through generation during zero states in one leg (c), asymmetric PWM control with shifted double shoot-through generation during zero states in one leg (d).

PWM control with shifted shoot-through generation during zero states in one leg can be modified further if the shoot-through states are placed on both sides of the active state. The modified method is called the PWM control with shifted

double shoot-through generation during zero states in one leg (Figure 3.10*c*). In this way the shoot-through occurs four times per switching period and thus the qZSN has four times higher operating frequency. However, experiments (Figure 3.13) show that inverter switches operate at hard-switching conditions. The VDR also has hard turn-ON, while the turn-OFF remains in conditions of ZCS. However, each inverter switch operates at the converter switching frequency, and thus provides moderate switching losses.

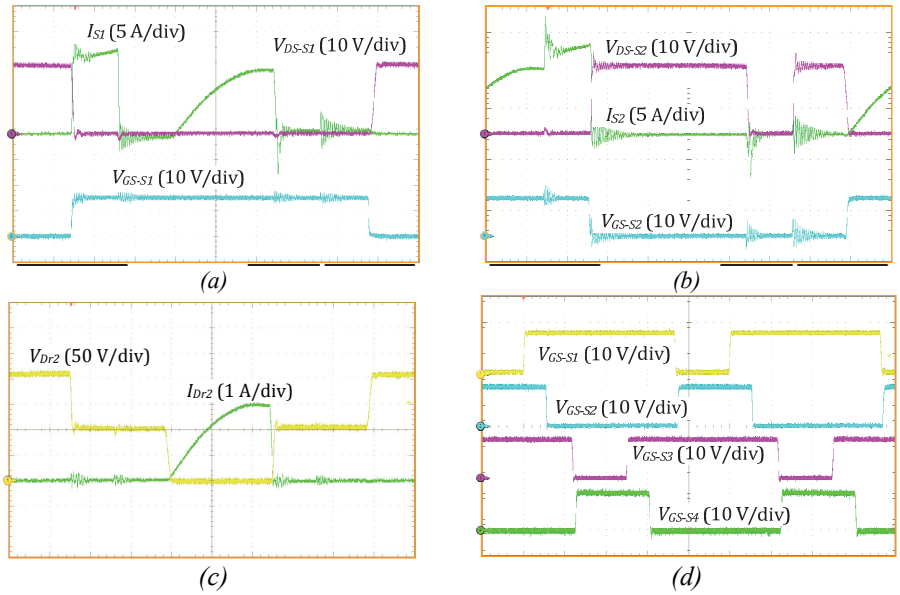


Figure 3.11 Experimental waveforms of the qZSC in the boost mode with the PWM control with shifted shoot-through generation during zero states in one leg (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of the VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).

The last method in this group is called the asymmetric PWM control with shifted double shoot-through generation during zero states in one leg (Figure 3.10*d*). It was derived from the previous control method through moving the active states towards each other, while zero states are merged into a single interval.

Measurement results obtained from the experimental prototype are presented in Figure 3.14. Two shoot-through intervals are also merged, thus only three shoot-through intervals of different duration occur during the switching period. As a result, input current ripple is higher. This switching sequence leads to a negative current flowing through the top switches during the shoot-through state in the other inverter leg. The top switches are hard-switched, while the bottom switches perform ZVS turn-OFF. Additional switching losses occur in the VDR diodes due to hard turn-ON, while turn-OFF remains ZCS.

The measured efficiency curves for these four novel shoot-through generation methods are shown in Figure 3.15. The first two control methods

with shoot-through generation by one leg show efficiency curves (Figure 3.15*a* and *b*) slightly lower than those for the reference PWM control method (Figure 3.6*d*). Apparently, switching losses lower than those of the reference method are compensated by the conduction losses rise caused by higher equivalent resistance of the inverter bridge during the shoot-through state. However, they could have better efficiency at higher switching frequencies. Another two control methods with the doubled shoot-through have even lower efficiency. Among them the PWM control with shifted double shoot-through generation during zero states in one leg has better efficiency than its asymmetric derivative. Due to four times higher operating frequency of the qZSN, it can be recommended for applications where power density is more important than efficiency. Low efficiency of its asymmetric derivative can be explained with additional conduction losses during reverse current flow in the top switches.

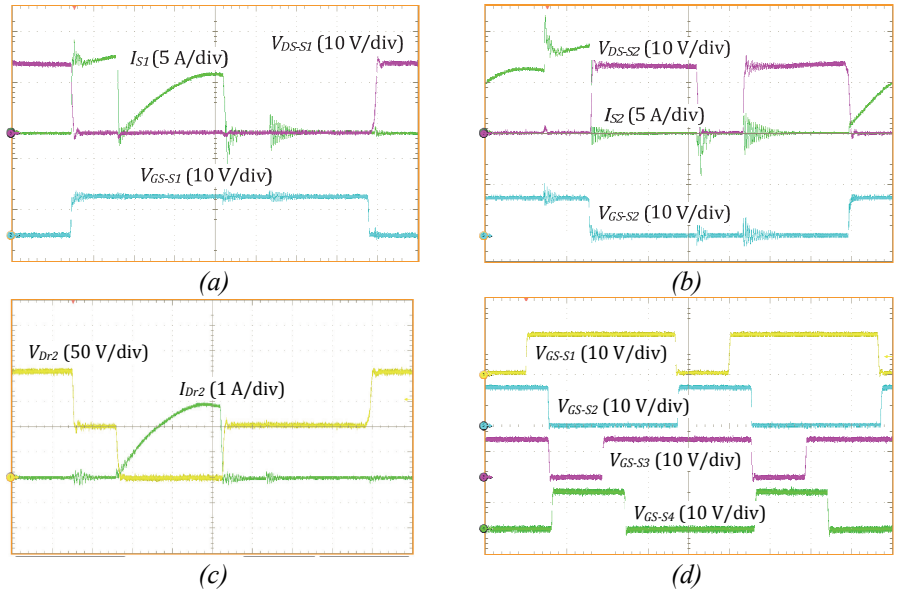


Figure 3.12 Experimental waveforms of the qZSC in the boost mode with asymmetric PWM control with shifted shoot-through generation during zero states in one leg (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of the VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).

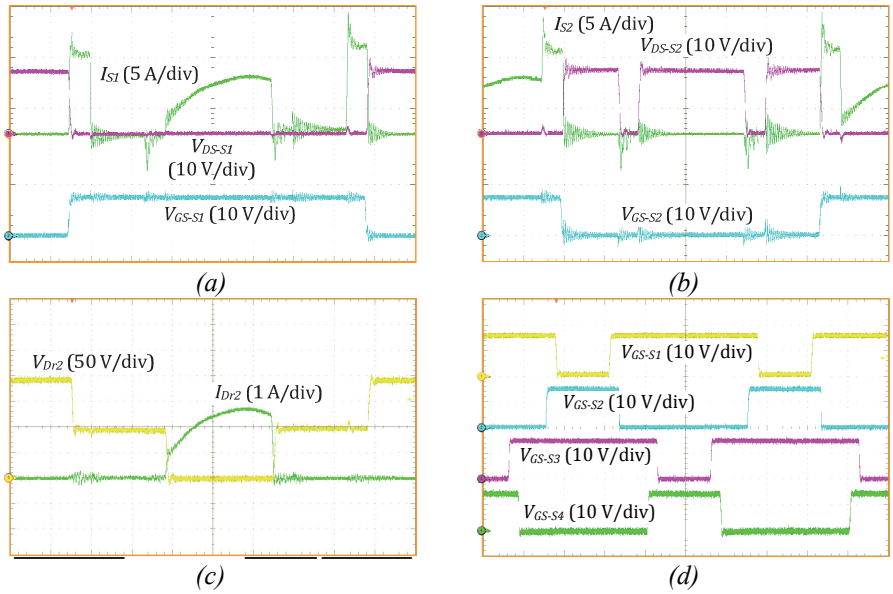


Figure 3.13 Experimental waveforms of the qZSC in the boost mode with the PWM control with shifted double shoot-through generation during zero states in one leg (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of the VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).

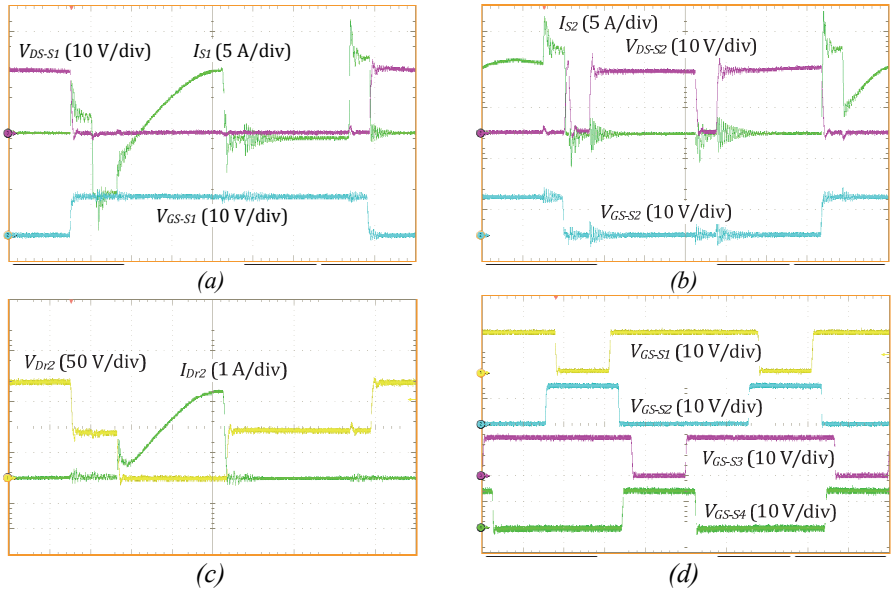
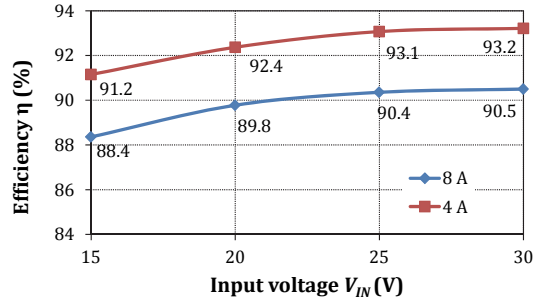
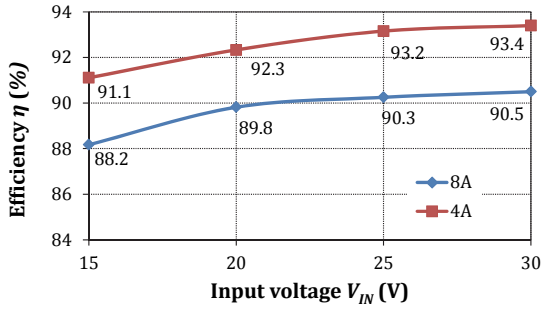


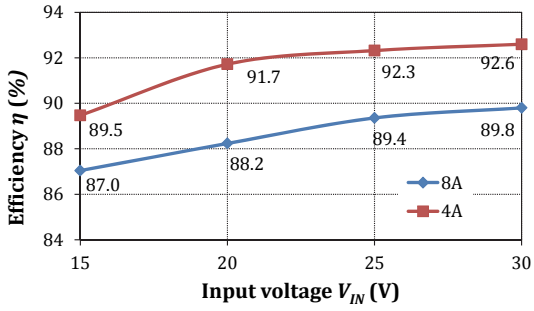
Figure 3.14 Experimental waveforms of the qZSC in the boost mode with asymmetric PWM control with shifted double shoot-through generation during zero states in one leg (D_{ST} = 0.25, V_{IN} = 15 V, I_{IN} = 8 A): voltage, current and gate signal of the MOSFET S_1 (a), voltage, current and gate signal of the MOSFET S_2 (b), voltage and current of the VDR diode D_{r2} (c), and gating signals of the inverter MOSFETs (d).



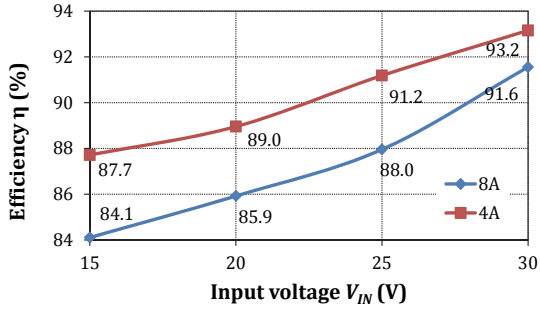
(a)



(b)



(c)



(d)

Figure 3.15 Measured efficiency of the qZSC that operates with: PWM control with shifted shoot-through generation during zero states in one leg (a), asymmetric PWM control with shifted shoot-through generation during zero states in one leg (b), PWM control with shifted double shoot-through generation during zero states in one leg (c), asymmetric PWM control with shifted double shoot-through generation during zero states in one leg (d).

3.1.2 Resonant Power Conversion

The simplest way of achieving soft-switching in the galvanically isolated qZS DC-DC converters without any changes of the control algorithm is to utilize the resonant tank. For the galvanically isolated DC-DC converters, the second or the third order resonant tank circuit is typically used, which consists of two or three energy storage elements, correspondingly [105]. In traditional resonant DC-DC converters, where the variable frequency control is used for the output voltage regulation, the optimization of the resonant tank could become an issue. In the qZSC, the resonant tank will always work at the resonance frequency since the input voltage and load regulation are performed by the variation of the shoot-through duty cycle. Therefore, a simple series resonant circuit could be implemented to achieve soft-switching in the qZSC.

Since the addition of extra discrete elements directly increases the cost and complexity of the converter, the resonant power conversion with maximum possible utilization of parasitic elements of the circuit was a very popular trend in the past years [106]-[108]. In high-frequency applications, the leakage or magnetizing inductances of the isolation transformer and parasitic capacitances of the semiconductors could be used as resonant inductors or resonant capacitors, correspondingly [109].

The series resonant qZSC (qZSSRC) is presented in Figure 3.16. It consists of an ordinary qZSN, a full-bridge switching stage, a series resonant tank formed by the capacitor C_r and the leakage inductance of the isolation transformer's primary winding, and a voltage-doubler rectifier.

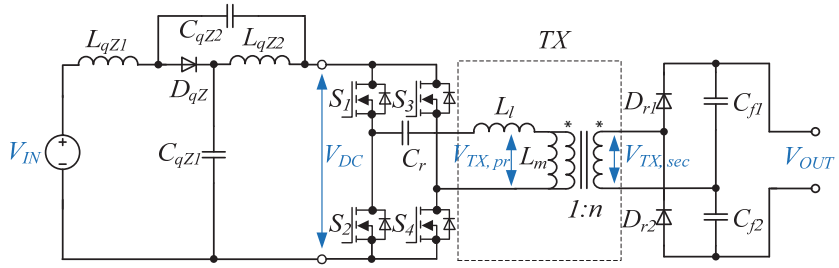


Figure 3.16 Generalized topology of the series resonant qZSC (qZSSRC).

Similarly to the baseline topology, the qZSSRC has two main operating modes: normal (or non-shoot-through) and boost (or shoot-through) mode. Further, the buck mode is now also available and provides an additional advantage gained by the implementation of the resonant network. The resulting advantages of the qZSSRC over the traditional qZSC could be listed as follows:

- full ZCS operation of the inverter and VDR in the normal mode,
- reduced switching losses of the inverter and full ZCS operation of the VDR in the boost (shoot-through) mode,
- extended input voltage regulation range due to the realization possibility of the buck mode,
- series capacitor C_r blocks the DC voltage, thus avoiding the transformer saturation.

The operation principle and experimental results of the IGBT-based qZSSRC were reported in [PAPER-I], [PAPER-II]. The results and findings of the MOSFET-based experimental prototype of the qZSSRC with specifications presented in Table 1.2 and 1.3 will be presented in the following sections.

Generalized operation principle of the qZSSRC

In the normal mode, the qZSSRC operates as a pure series resonant converter with the duty cycle of inverter switches close or equal to 0.5. The switching frequency of the inverter is equal to the resonant frequency ($f_{SW}=f_r$) and can be defined as:

$$f_{SW} = f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_l C_r}}, \tag{3.1}$$

where L_l is the leakage inductance of the isolation transformer's primary winding and C_r is the capacitance of the resonant capacitor. At the magnetic integration of the resonant inductor, it should be remembered that the second resonance frequency also exists:

$$f_{r2} = \frac{1}{2\pi}\sqrt{\frac{1}{(L_l + L_m)C_r}}, \tag{3.2}$$

where L_m is the magnetizing inductance of the isolation transformer. Typically, the leakage inductance of the transformer is below two percent of the value of magnetizing inductance [106] and the resonance frequencies f_r and f_{r2} differ by a factor of 10.

The steady-state waveforms of the normal mode are presented in Figure 3.17*a*. It is seen that the inverter switches and the rectifying diodes here can be turned ON and OFF at perfect zero current, therefore in this operating point, the qZSSRC features its maximum possible efficiency.

Neglecting losses in the components, the resulting output voltage gain in the normal mode could be expressed as:

$$G_{normal} = \frac{V_{OUT}}{V_{IN}} = 2 \cdot n, \tag{3.3}$$

where V_{IN} and V_{OUT} are the input and output voltages of the converter and n is the transformer's turns ratio.

In the normal mode, the current in the series resonant circuit can be assumed as a pure sinewave and the voltage drop across the resonant tank is zero. The output voltage of the converter can be expressed as:

$$V_{OUT} = \frac{I_{TX,pr(m)} \cdot R_{ld}}{n \cdot \pi}, \tag{3.4}$$

where $I_{TX,pr(m)}$ is the amplitude value of the current through the resonant tank and R_{ld} is the resistance of a load.

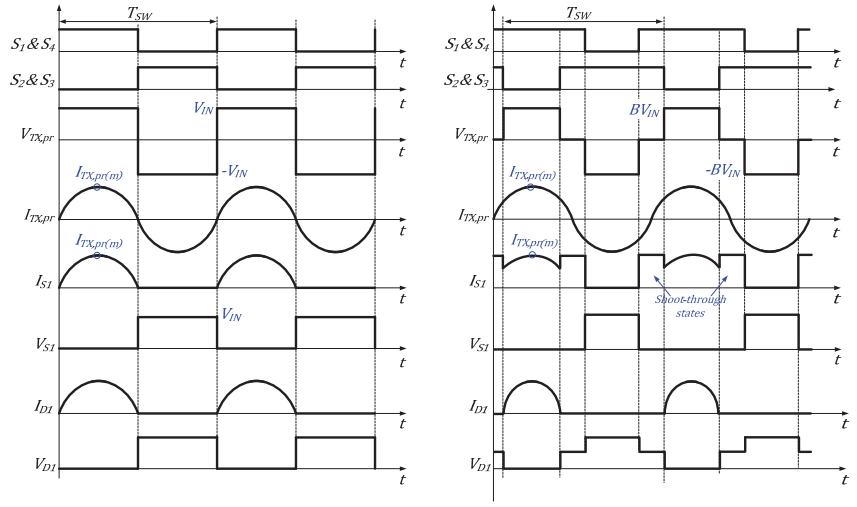


Figure 3.17 Steady-state waveforms of the qZSSRC in the normal (a) and boost (b) operation mode.

Average current of the resonant tank per half cycle is

$$I_{TX,pr(av)} = \frac{2 \cdot I_{TX,pr(m)}}{\pi} \tag{3.5}$$

The output power of the converter is

$$P_{OUT} = P_{IN} - P_r = I_{IN} \cdot V_{IN} - I_{TX,pr(rms)}^2 \cdot R_r , \tag{3.6}$$

where P_{IN} is the input power, P_r is the power dissipated in the resonant tank and $R_r = \sqrt{L_r / C_r}$ is the impedance of the resonant tank. Equation (3.6) could be rewritten as

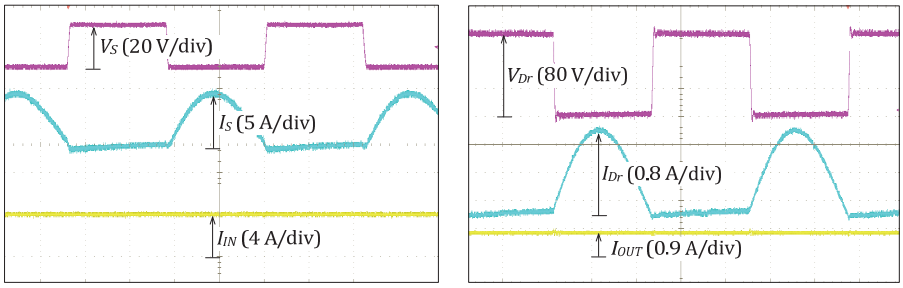
$$P_{OUT} = \frac{2I_{TX,pr(m)}}{\pi} \cdot V_{IN} - \frac{I_{TX,pr(m)}^2}{2} \cdot R_r = \frac{I_{TX,pr(m)}^2 \cdot R_{ld}}{n^2 \cdot \pi^2} . \tag{3.7}$$

Using Eq. (3.7), the amplitude value of the resonant current can be found by

$$I_{TX,pr(m)} = \frac{4 \cdot \pi \cdot V_{IN}}{\pi^2 \sqrt{\frac{L_r}{C_r}} + \frac{2 \cdot R_{ld}}{n^2}} . \tag{3.8}$$

In a general case, Eq. (3.8) could be used for the estimation of current stress of the inverter switches and elements of the resonant tank. Figure 3.18 presents the experimental voltage and current waveforms of the inverter switches and VDR diodes in the normal mode. For this experiment, the leakage inductance of the isolation transformer (L_l =0.5 μH) was utilized as a resonant inductor. To provide resonance at the switching frequency (100 kHz), a 5 uF foil capacitor was connected in series with the primary winding of the isolation transformer. It

it seen from Figure 3.18 that due to pure sinusoidal current, inverter switches and VDR diodes are operating with ZCS. Thanks to that, the switching losses are fully eliminated in contrast to the baseline topology, where inverter transistors were hard-switched (Figure 1.5). According to the analysis of converter power loss presented in Figure 1.8, the switching losses of inverter transistors comprise near 0.5 W from the total power dissipation at the maximum operation power, which corresponds to the normal mode of the qZSC. In the ideal case, the resonant switching will eliminate these losses, which could theoretically result in the efficiency rise up to 0.2%.



(a) *(b)*

Figure 3.18 Experimental waveforms of the qZSSRC in the normal operation mode: voltage and current of MOSFET and input current of the converter (a), voltage and current of the VDR diode and output current of the converter (b).

In the boost mode, the qZSSRC is controlled by the overlap of active states exactly in the same manner as in the baseline topology. As in the normal mode, the switching frequency of the inverter switches f_{SW} in the boost mode remains fixed to the resonant frequency f_r. Figure 3.17*b* shows the steady-state waveforms of the converter operating in the boost mode. Neglecting losses in the components, the resulting output voltage gain of the qZSSRC in the boost mode could be expressed as:

$$G_{boost} = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n}{(1 - 2D_{ST})}, \tag{3.9}$$

where D_{ST} is the shoot-through duty cycle.

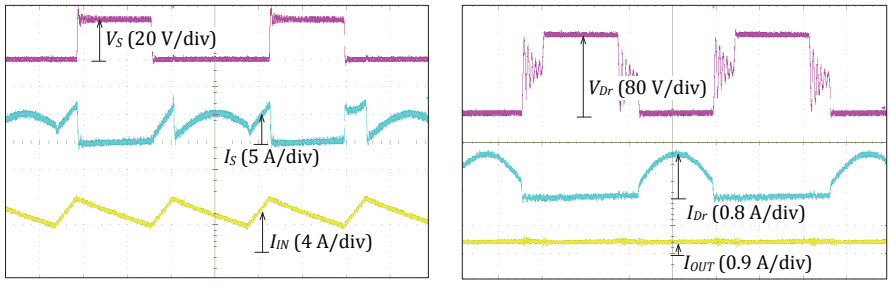
In the boost mode, the shape of the resonant circuit current ($I_{TX,pr}$) can be also assumed as a sinewave and the relation between the amplitude value of this current and the output voltage can be described using Eq. (3.4). The input current of the converter can be expressed as:

$$I_{IN} = \frac{2 \cdot I_{TX,pr(m)}}{\pi(1 - 2D_{ST})}. \tag{3.10}$$

Similarly to Eq. (3.8), the amplitude current of the resonant tank during the boost mode can be expressed as:

$$I_{TX,pr(m)} = \frac{4 \cdot \pi \cdot V_{IN}}{\left(\pi^2 \sqrt{\frac{L_r}{C_r}} + \frac{2 \cdot R_{ld}}{n^2}\right) \cdot (1 - 2D_{ST})}. \quad (3.11)$$

As it is seen from the experimental waveforms in the boost mode (V_{IN}=*15 V,* D_{ST}=*0.25*) presented in Figure 3.19, the semiconductors of the inverter bridge of the qZSSRC feature partial soft-switching – ZCS turn-ON only, while the VDR diodes operate with ZCS.



(a) *(b)*

Figure 3.19 Experimental waveforms of the qZSSRC in the boost mode at D_{ST}=0.25: voltage and current of MOSFET and input current of the converter (a), voltage and current of the VDR diode and output current of the converter (b).

According to the analysis of the power loss of the converter presented in Figure 3.20, the switching losses of the inverter bridge during the operation at the maximum shoot-through duty cycle and power of 120 W are near 0.35 W. Therefore, the resonant switching with shoot-through will reduce these losses by 75%, which in an ideal case could result in the efficiency rise up to 0.2%. However, in a real converter, this minor efficiency improvement will be cancelled by the losses in resonant elements as well as by slightly increased conduction losses caused by the sine-shape resonant current. It is seen from Figure 3.21*a* that for the same reason, the case study qZSC features 0.4% higher efficiency than its resonant counterpart.

However, the resonant switching could become more attractive with an increase in the switching frequency, when the switching losses of semiconductors increase linearly. Figure 3.20 shows the estimation of dynamic losses of the case-study converter operating at 400 kHz. It is seen that in the maximum power point, the switching losses of MOSFETs comprise 2.4 W from the total processed power. In that case, the implementation of resonant switching could result in up to 1% of the efficiency rise. The experimental results in Figure 3.21*b* show that the case study qZSSRC operating with the maximum power (normal mode) is characterized by 0.9% better efficiency than the traditional qZSC.

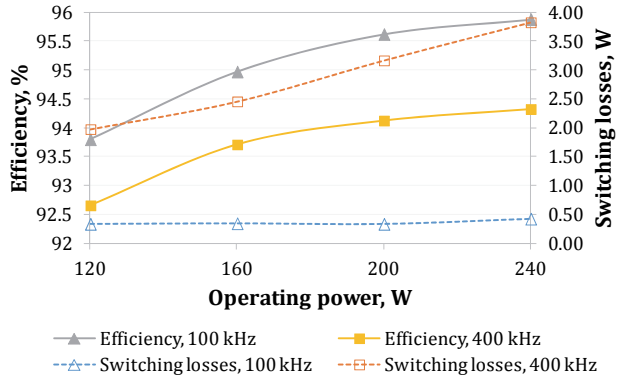
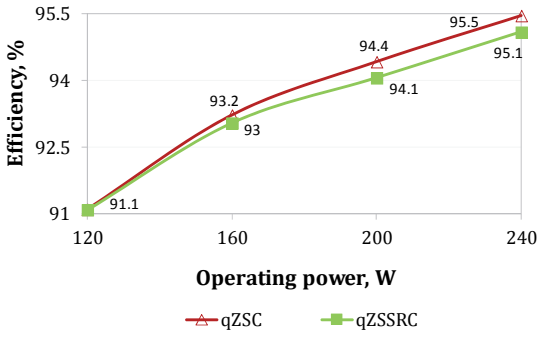
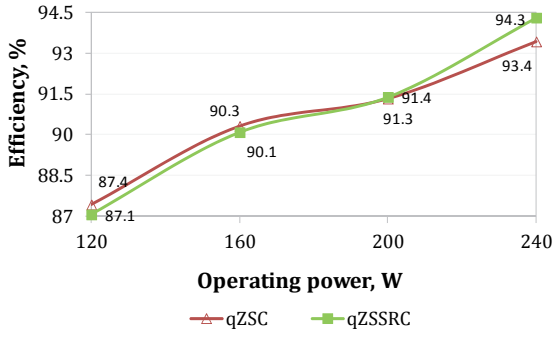


Figure 3.20 Estimated efficiency and switching losses vs. output power of the qZSC operating at 100 kHz and 400 kHz.



(a)



(b)

Figure 3.21 Comparison of measured efficiencies of the qZSC and qZSSRC operating at 100 kHz (a) and 400 kHz (b).

Buck mode realization in the qZSSRC

In the qZSSRC, the realization possibility of the buck mode is an extra benefit over a baseline solution, which could significantly extend the input voltage regulation range of the qZSC. Similarly to traditional series resonant converters [110]-[114], the output voltage in the qZSSRC could be controlled

by increasing the switching frequency of the inverter from the resonant frequency f_r to some certain value (f_{SW1}) to obtain the desired voltage gain (Variable Frequency Control, VFC). The theoretical operational waveforms in this mode are depicted in Figure 3.22. In this configuration, the resonant tank and the load act as a voltage divider. By changing the switching frequency, the impedance of the resonant circuit will also change. Since it is a voltage divider, the DC gain of the qZSSRC in this operating mode will be always lower than 1.

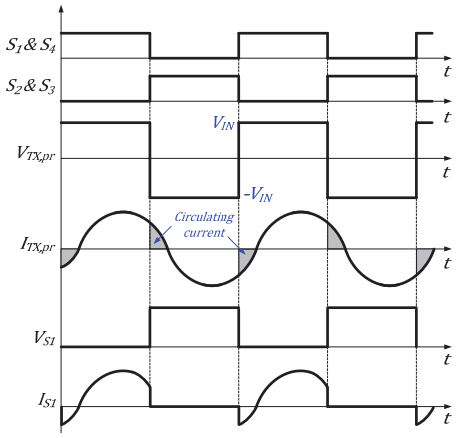


Figure 3.22 Steady-state waveforms of the qZSSRC in the buck operation mode with VFC.

The steady-state analysis of the buck mode realization in the qZSSRC by help of the variable frequency control is presented in [PAPER-IX]. The resulting voltage gain directly depends on the quality factor of the resonance network and load conditions and could be generally described as:

$$V_{OUT} = 4R_{ld}V_{IN}\sqrt{\frac{n^2\omega_{SW}^{*2}}{4R_{ld}^2\omega_{SW}^{*2} + n^4R_r^2\pi^4(\omega_{SW}^{*2}-1)^2}}, \tag{3.12}$$

where the relative switching frequency, resonant impedance and resonant frequency can be expressed by Eqs. (3.13), (3.14) and (3.15), correspondingly:

$$\omega_{SW}^{*} = \frac{\omega_{SW}}{\omega_r}, \tag{3.13}$$

$$R_r = \sqrt{\frac{L_r}{C_r}}, \tag{3.14}$$

$$\omega_r = \sqrt{\frac{1}{L_r \cdot C_r}}. \tag{3.15}$$

For the experimental validation of the buck mode realization with the VFC, the external series resonant tank was assembled by help of 2.2 µH inductor and 1.1 µF ceramic capacitor. The converter was tested in three operating points (V_{IN}=35 V, V_{IN}=40 V and V_{IN}=45 V) with the fixed input current I_{IN}=4 A. To

regulate the output voltage, the switching frequency was changed from the resonance point $f_r = 100$ kHz at $V_{IN} = 30$ V to 350 kHz at $V_{IN} = 45$ V (see Figure 3.23).

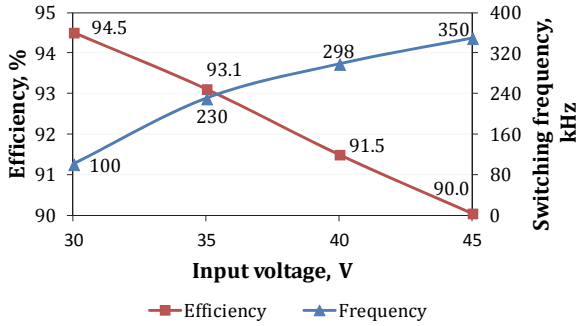
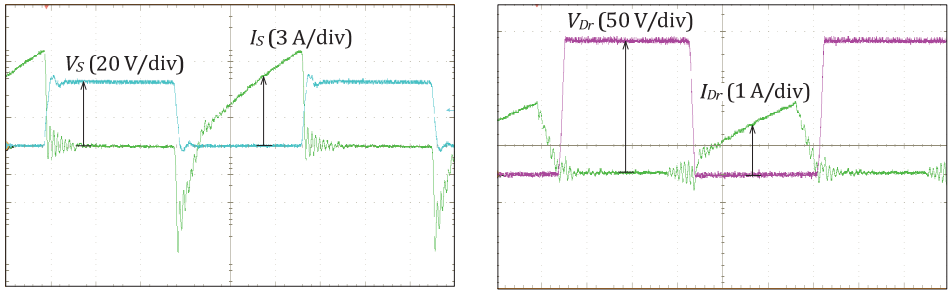


Figure 3.23 VFC buck mode: experimental efficiency and switching frequency of the case-study qZSSRC in the selected test points with the input current I_{IN}=4 A.

Figure 3.24 shows the voltage and current waveforms of the inverter MOSFETs and the VDR diodes measured at the operating point with $V_{IN} = 45$ V and $f_{SW1} = 350$ kHz. It is seen that except some power dissipation during the turn-ON of the inverter's MOSFETs, the semiconductors of the qZSSRC remain soft-switched during the buck mode. The experimental efficiency curve of the case study qZSSRC operating in the VFC buck mode is presented in Figure 3.23. Due to power dissipation in the resonant tank elements, the converter's efficiency decreases from 94.5% in the normal mode to 90% in the maximum buck mode.



(a) (b)

Figure 3.24 Experimental waveforms of the qZSSRC in the VFC buck mode at 350 kHz: voltage and current of MOSFET (a), voltage and current of VDR diode (b).

Phase-shift modulation for control of the qZSSRC in the buck mode

An alternative control possibility of a series resonant converter in the buck mode is a phase-shift modulation (PSM), when the output voltage is controlled by the phase shift angle φ between two inverter legs at the resonant frequency ($f_{SW} = f_r$) [54]. Figure 3.25 shows the steady-state waveforms of the converter in

the buck mode. Neglecting losses in the components, the resulting output voltage gain of the qZSSRC in the buck mode could be expressed as:

$$G_{buck} = \frac{V_{OUT}}{V_{IN}} = \sqrt{2} \cdot n \cdot \sqrt{1+\cos\varphi} \,. \tag{3.16}$$

The amplitude value of the resonant current can be found by

$$I_{TX,pr(m)} = \frac{\sqrt{2}\pi V_{IN} n^2}{R_{ld}} \sqrt{1+\cos\varphi} \,. \tag{3.17}$$

The input current of the converter can be expressed as:

$$I_{IN} = \frac{2V_{IN} n^2 (1+\cos\varphi)}{R_{ld}} \,. \tag{3.18}$$

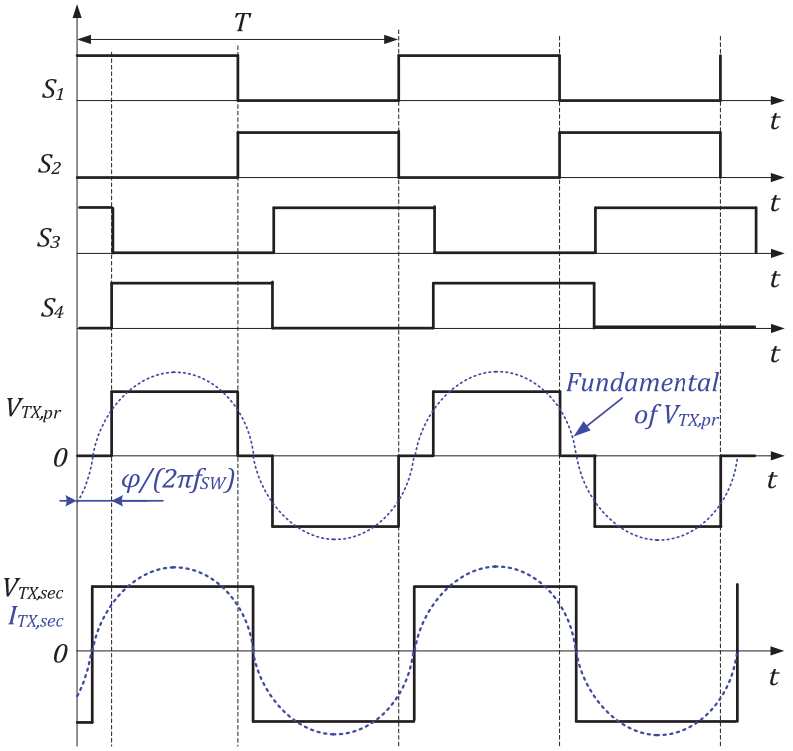


Figure 3.25 General operation waveforms of the qZSSRC in the PSM buck mode.

For the experimental validation of the buck mode realization with the PSM, the external series resonant tank was assembled by help of 2.2 µH inductor and 1.1 µF ceramic capacitor. The converter was tested in three operating points (V_{IN} = 35 V, V_{IN} =40 V and V_{IN} = 45 V) with the fixed input current I_{IN} = 4 A. To regulate the output voltage, the phase angle φ was changed from 0° at V_{IN} = 30 V to 109° at V_{IN} = 45 V (see Figure 3.26).

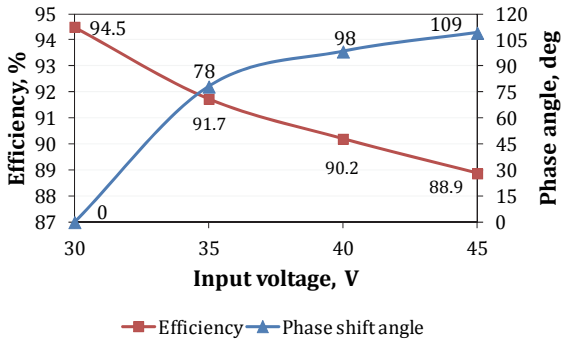
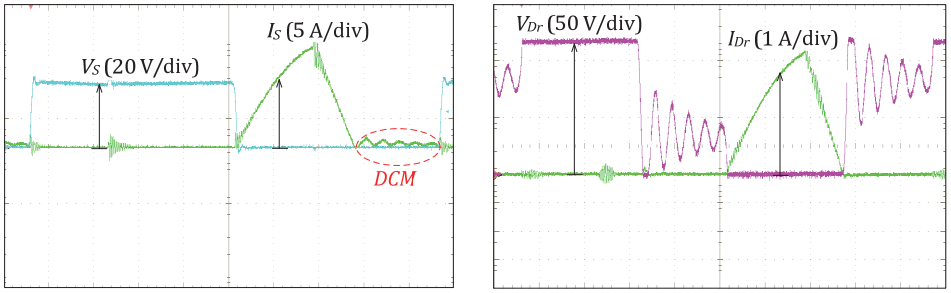


Figure 3.26 PSM buck mode: experimental efficiency and phase shift angle of the case-study qZSSRC in the selected test points at the input current I_{IN}=4 A.

Figure 3.27 shows the voltage and current waveforms of the inverter MOSFETs and VDR diodes measured at the operating point at V_{IN} = 45 V and φ = 109°. It is seen that the semiconductors of the qZSSRC feature ZCS in the buck mode with PSM.



(a) *(b)*

Figure 3.27 Experimental waveforms of the qZSSRC in the PSM buck mode at φ = 109°: voltage and current of MOSFET (a), voltage and current of VDR diode (b).

The experimental efficiency curve of the case study qZSSRC operating in the PSM buck mode is presented in Figure 3.26. Comparison with the VFC in Figure 3.23 shows that the efficiency in the PSM buck mode was reduced by more than 1% within the entire regulation range. It is mostly caused by the increased amplitude current values and therefore higher conduction losses of the inverter MOSFETs and VDR diodes than in the case of the VFC. The reason lies in the discontinuous current through the resonant inductor (Figure 3.27*a*) resulting from the parameters of the resonant tank. The condition for continuous current operation could be defined by [54]:

$$\frac{\pi^3 \cdot P \cdot n^2}{8 \cdot V_{OUT}^2} \sqrt{\frac{L_r}{C_r}} > 1. \tag{3.19}$$

In the given case study, the resonant tank with a series combination of 2.2 µH inductor and 1.1 µF capacitor features discontinuous current operation within the entire range of the buck mode. For better performance, it is recommended to select the highest possible value of the resonant inductor to operate close to the boundary described by (Eq. 3.19).

Hybrid qZS series resonant converter for wide input voltage and load variation

By combining the boost properties of the qZSC, soft-switching performance of the SRC and the buck mode realization by help of the PSM, a novel soft-switching galvanically isolated DC-DC converter for wide input voltage and load variation was derived: *Hybrid qZS Series Resonant Converter (HqZSSRC)*. In contrast to the Z-source resonant DC-DC converter with a wide regulation range discussed in [110], the main advantages of the proposed HqZSSRC are the hybridization of the operating modes, constant frequency control over the entire range of the input voltage and load variation and better soft-switching performance.

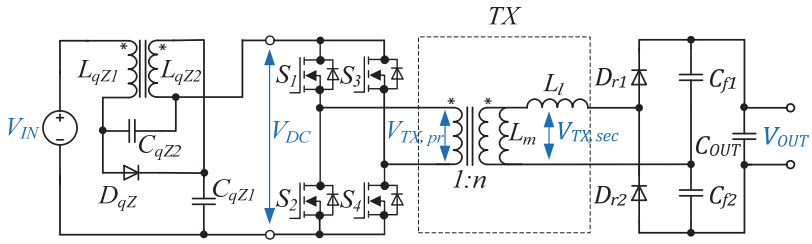


Figure 3.28 Generalized topology of the HqZSSRC.

The HqZSSRC in Figure 3.28 combines the shoot-through PWM and ordinary PSM for the realization of the boost and buck operating modes, respectively. An example of the control variables of the HqZSSRC operating within the input voltage range from 15 V to 45 V is presented in Figure 3.29.

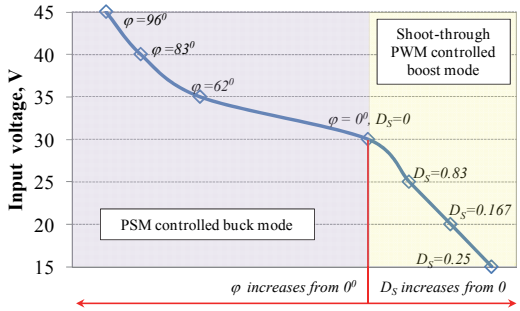


Figure 3.29 Idealized control variables of the HqZSSRC operating within the input voltage range from 15 V to 45 V.

In contrast to the traditional qZSC with twofold variation of the input voltage, the proposed HqZSSRC could widen the input voltage regulation range up to two times without any serious efficiency penalties. This converter could be a good candidate for the PV module integrated converters, where the wide input voltage and load regulation range, power conversion efficiency and power density are the main criteria of success.

Another distinguishing advantage of the proposed HqZSSRC is the integration of passive components for better power density. In the primary side, two separate inductors of the qZSN were replaced by the coupled inductor. Since the currents through qZS inductors are the same in terms of waveform and magnitude due to the flux doubling effect, we need to build two-winding coupled inductor for the same operating conditions with an magnetizing inductance twice smaller than in the case of separate inductors [115]. Finally, for the same operating parameters, the volume of a coupled inductor could be decreased by up to 40% compared to the summarized volume of two separate ones in the traditional approach.

As can be seen from Figure 3.28, no additional components were used for the resonant tank, which is now placed in the secondary side of the converter: leakage inductance of the secondary winding of the isolation transformer forms the series resonant network with the capacitors of the voltage doubler rectifier in Figure 3.28. Realization of a magnetically integrated resonant tank in the high-voltage side of the converter is more convenient for the step-up DC-DC converters since the secondary winding due to a larger number of turns has higher value of leakage inductance, which, in turn, is essential for obtaining higher quality factor values of the resonant network. The design guidelines for proper realization of the secondary resonance with integrated passive elements discussed in [116] could be summarized as follows:

$$C_r > \frac{P}{V_{OUT}^2 \cdot f_r}, \; L_r < \frac{V_{OUT}^2}{8 \cdot \pi^2 \cdot P \cdot f_r}. \tag{3.20}$$

3.1.3 Full Soft-Switching Operation

In general, numerous techniques exist that allow achieving soft-switching in the inverter bridge of the isolated full-bridge DC-DC converter. Many of them have been reviewed in section 2 of this thesis. This subsection describes a novel full soft-switching qZSC (FSSqZSC). The idea is based on the modification of both the converter topology and the switching control principle. In the converter in Figure 3.30, the second qZSN inductor L_{qZ2} is selected to operate in a boundary or discontinuous conduction mode, while the input inductor is dimensioned to operate in the CCM. Utilization of snubber capacitors across the bottom inverter switches and output VDR diodes along with the new shoot-through control method provide a soft-switching operation. The control algorithm shown in Figure 3.31 features two types of shoot-through states: with two conducting transistors and with three conducting transistors. This method was derived from the PWM shoot-through control by the shifted overlap of

active states. It was done through an increasing duration of the turn-ON time of each inverter switch by a small value over 0.5. This additional time interval is responsible for soft-switching since the shoot-through state with three transistors conducting is generated during it.

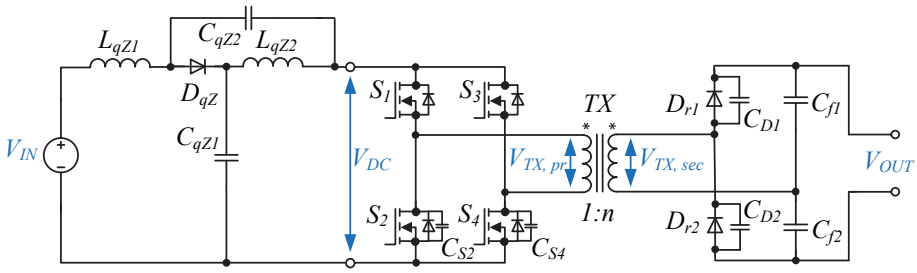


Figure 3.30 Generalized topology of the FSSqZSC.

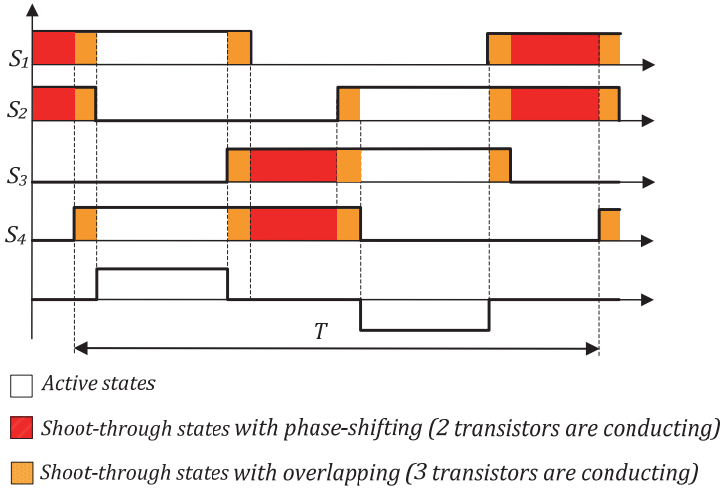


Figure 3.31 Modified control algorithm for the FSSqZSC.

The shoot-through states with three conducting transistors are short in duration and intended to perform ZCS turn-ON of a top transistor at the beginning of this interval, and ZVS turn-OFF of the other top transistor at the end of this interval. The operating principle of the FSSqZSC is shown in Figure 3.32. It is evident that ZCS turn-ON of the top transistors is assisted with the second qZSN inductor that features discontinuous current. ZVS of the bottom transistors is assisted with the small snubber capacitors that interact with leakage inductance of the isolation transformer.

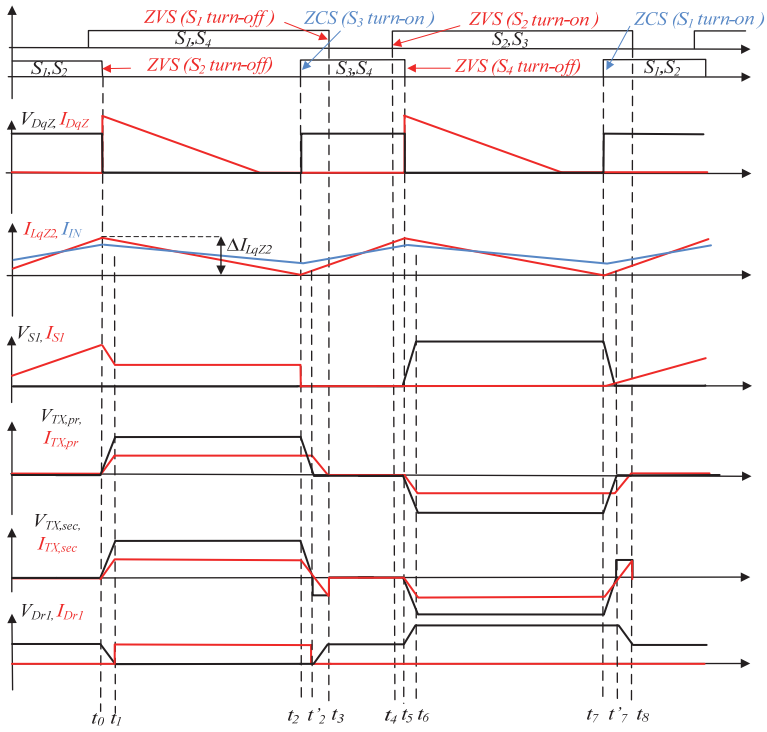


Figure 3.32 Idealized operating waveforms of the FSSqZSC.

Description of the operating intervals

At the beginning of the interval t_0-t_1, the transistor S_2 performs ZVS turn-OFF assisted with the snubber capacitor. This switching transient finishes the shoot-through operation and the converter turns to the active state. The leakage inductance limits the rate of the current rise in the transformer and inverter switches. At the same time the circuit configuration of the qZSN changes. Figure 3.33*a* demonstrates an equivalent circuit, where recharging of snubber capacitors on both sides of the transformer is shown.

At the beginning of the interval t_1-t_2, the converter reaches active state operation, when the transistors S_1 and S_4 supply the transformer. The VDR diode D_{r1} is conducting. The equivalent circuit that corresponds to this time interval is shown in Figure 3.33*b*.

The interval t_2-t_3 starts with the turn-ON transient of the switch S_3, as shown in Figure 3.33*c*. The new shoot-through state is starting. Zero current in the second qZSN inductor at the moment t_2 assists the ZCS operation of S_3. This interval can be separated into two sub-intervals, as shown in Figure 3.32. Partial discharge of the snubber capacitor C_{S2} occurs through the leakage inductance and the top transistor S_1 at the beginning of this interval. Regardless of short duration of this process, the leakage inductance could delay the change of the secondary winding voltage of the isolation transformer. After that, the ZVS transient is started in the VDR, assisted with the output side snubber capacitors, as shown in Figure 3.33*d*. This transient process finishes with the ZVS turn-

OFF of the switch S_1. Quality of this switching transient depends on the values of the snubber capacitors and the leakage inductance of the isolation transformer.

During the interval t_3-t_4, the shoot-through is performed with switches S_3 and S_4. Figure 3.33*e* shows an equivalent circuit of the converter operating in this mode.

At the interval t_4-t_5, the shoot-through is performed with three switches, since S_2 is turned ON under ZVS conditions, as shown in Figure 3.33*f*.

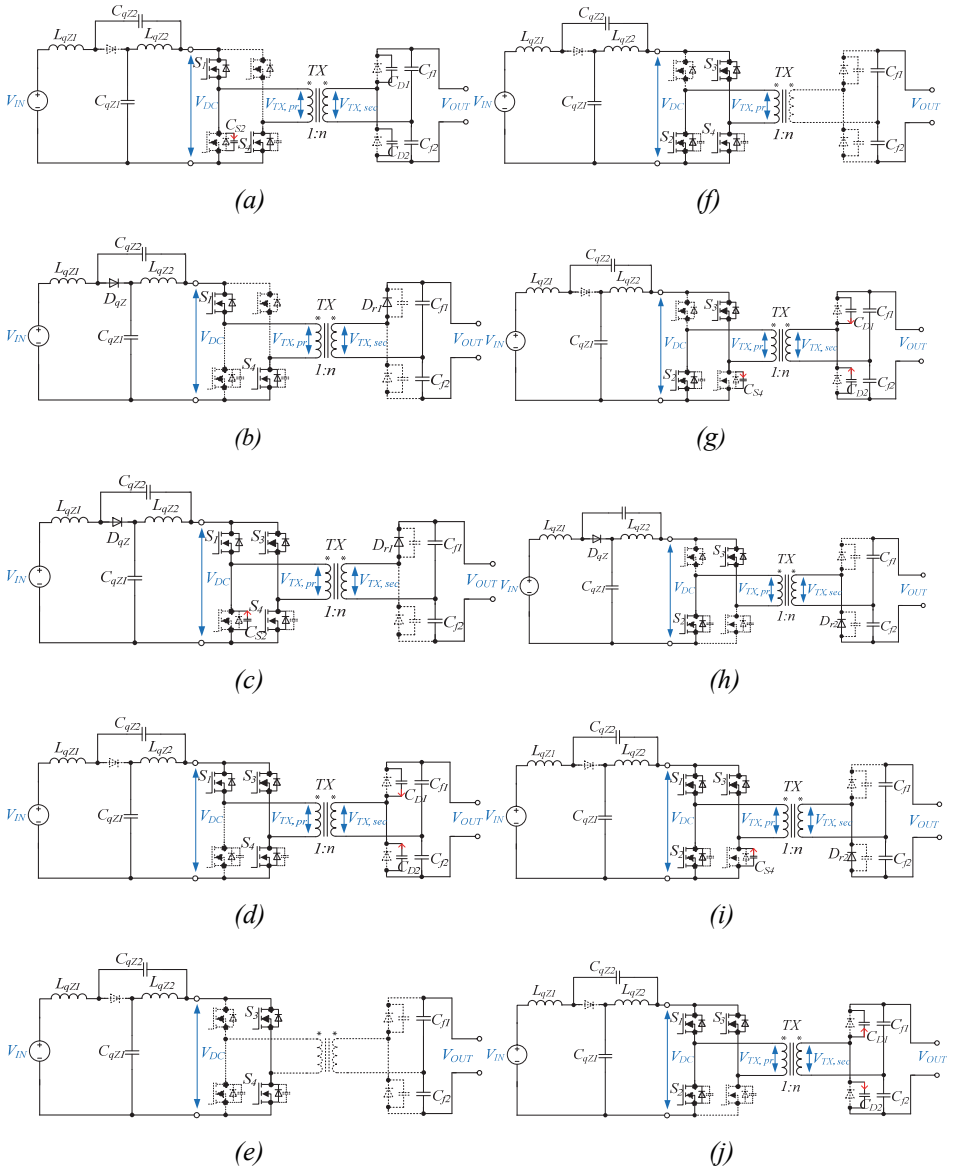


Figure 3.33 Equivalent circuits of the operation of the FSSqZSC.

The interval t_5-t_6 is started with the ZVS turn-OFF of the switch S_4, assisted with the corresponding snubber capacitor. Figure 3.33*g* provides an equivalent circuit for this time interval. The charging of the snubber capacitor C_{S4} occurs through the qZSN and switch S_3. This process lasts till the instant t_6 when the converter switches to the active state, when the switches S_2 and S_3 supply the isolation transformer. The equivalent circuit for this time interval is shown in Figure 3.33*h*.

Switching processes over the time interval t_7-t_8 are similar to those of the interval t_2-t_3. The process starts with ZCS turn-ON of S_1, assisted with the second qZSN inductor that supplies zero current at instant t_7. The equivalent circuits in Figure 3.33*i* and Figure 3.33*j* describe the operation of the converter within the time interval t_7-t_8.

It is evident from the operating principle described above that the proposed converter combines hardware and control modifications. It always operates in the boost mode, since short shoot-through states with three switches conducting are necessary on both sides of the active state to maintain the soft-switching operation. The cumulative duration of all shoot-through states defines the voltage step-up at the input side of the converter.

The modifications in the converter do not influence the general principles of the operation of the qZSN. Thus, the resulting input voltage gain of the topology proposed can be expressed as in [1]:

$$G_{boost} = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n}{1 - 2D_{ST}}, \tag{3.21}$$

where D_{ST} is a cumulative shoot-through duty cycle.

The voltage stress of the qZSN capacitors is the same as in the baseline topology. The second qZSN inductor has to be properly dimensioned to achieve a BCM or DCM within the operating range. Taking into account the basic operating principle of the qZSN and the constant output voltage, the value of the inductor L_{qZ2} can be calculated as a function of the input power P, input voltage V_{IN}, and the current ripple factor r_c:

$$L \geq \frac{T \cdot V_{IN} \cdot (V_{OUT}^2 - 4 \cdot n^2 \cdot V_{IN}^2)}{8 \cdot r_c \cdot P \cdot V_{OUT}}. \tag{3.22}$$

The BCM operation corresponds to the current ripple factor $r_c = 2$. High current ripple results in higher conduction losses in the inductor and inverter MOSFETs. It was shown in [117] that conduction losses can rise by up to 35 % in the BCM as compared to the case of ripple free input current. However, the soft-switching operation results in significantly lower switching losses. Proper dimensioning of the snubber capacitors is important for the soft-switching operation.

The proposed converter was first verified with a simulation. The basic parameters and operation conditions used were the same as for the baseline topology. However, the inductors in the qZSN have different values of inductance: 4 µH for L_{qZ1} and 1.2 µH for L_{qZ2}. The capacitance of the input side snubber capacitors C_{S2}, C_{S4} equals 22 nF, while 120 pF capacitance was taken

for the output snubber capacitors. The switching frequency was selected equal to 200 kHz. The simulation was performed in PSIM simulation software by help of *Thermal module*. The simulation results are presented in Figure 3.34. It is evident that the second qZSN inductor operates near the boundary conduction mode, while the input inductor has considerably lower current ripple. The simulation results are shown for the $D_{ST} = 0.25$. As it was mentioned before, D_{ST} is a cumulative shoot-through duty cycle and thus it cannot be lower than a certain minimum value needed to maintain a soft-switching operation.

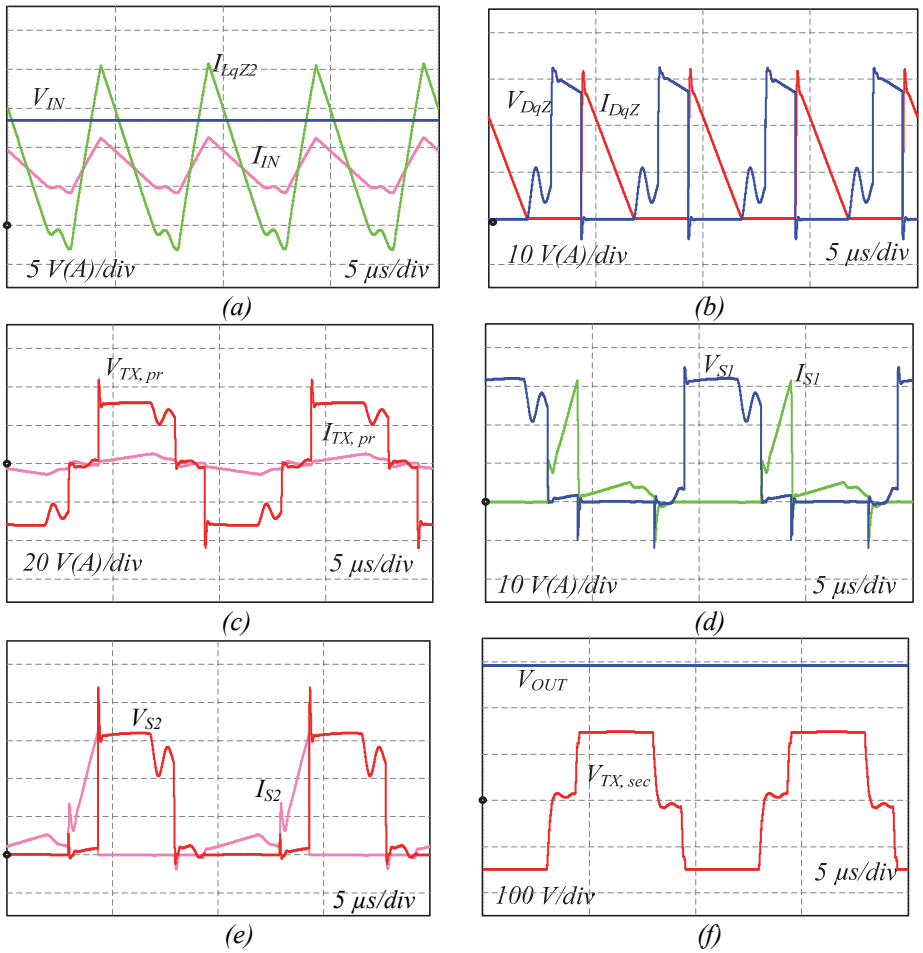


Figure 3.34 Simulation results of the FSSqZSC: the input voltage V_{IN} and currents of the qZSN inductors (a), current and voltage of the qZS diode D_{qZ} (b), current and voltage of the primary side winding of the isolation transformer (c), current and voltage of the switch S_1 (d), current and voltage of the switch S_2 (e), voltage of a secondary winding of the isolation transformer and the output voltage (f).

The semiconductor losses have been estimated in the simulation for baseline qZSC with equal inductors ($L_{qZ1} = L_{qZ2} = 4$ µH) operating at maximum boost, i.e. $D_{ST} = 0.25$, and proposed FSSqZSC at maximum and minimum boost. The

semiconductor loss breakdown obtained in the simulation is shown in Figure 3.35. The simulation shows that modified and baseline topologies are characterized by nearly the same losses. However, in the FSSqZSC, the switching losses are absent, while they contribute to semiconductor power losses in the baseline topology. It means that the FSSqZSC has to maintain nearly the same efficiency at higher switching frequency if the qZSN inductors are properly re-designed to achieve BCM or DCM at that frequency. At the same time, the efficiency of the baseline qZSC will drop due to an increase in the switching losses. The conduction losses of the FSSqZSC are lower at minimum boost due to low current ripple. At the same time, higher operating power contributes to higher power losses in the VDR diode. That is the reason why semiconductor power losses remain nearly the same in different operating modes.

The experimental results were obtained using the same converter prototype as before with small modifications, like replaced qZSN inductors and additional snubber capacitors at the input and output sides.

Figure 3.36 shows experimental waveforms obtained with the MOSFET-based experimental prototype described before, where necessary modifications were made. It shows slight differences in the waveform of the primary side inductor current in the return and direct way. It is caused by the slight difference of parasitic elements in the first inverter leg (S_1, S_2) from that in the second inverter leg (S_3, S_4) of the converter. In general, the experimental results obtained are in good accordance with the simulation and theoretical results described before.

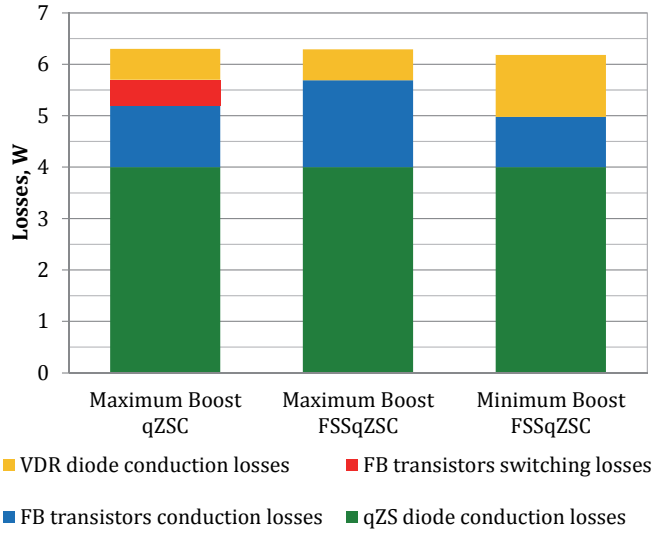
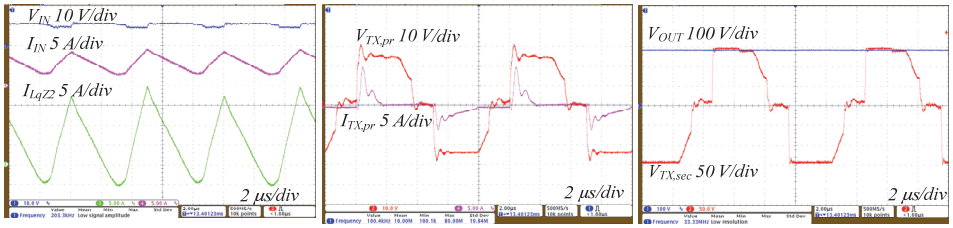


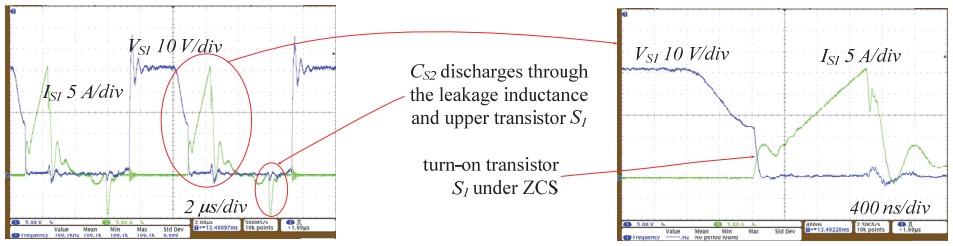
Figure 3.35 Breakdown of semiconductor losses of qZSC and FSSqZSC in different operating modes.



(a) *(b)* *(c)*

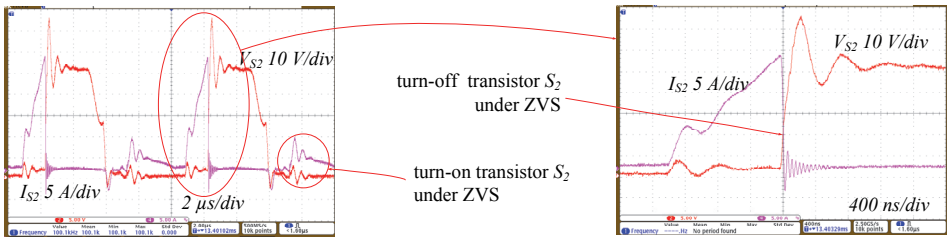
Figure 3.36 Experimental results: the input voltage V_{IN} and currents of the qZSN inductors (a), current and voltage of the primary side winding of the isolation transformer (b), voltage of a secondary winding of the isolation transformer and the output voltage (c).

A detailed study of the soft-switching transients in the inverter switch from the first leg is presented in Figure 3.37 and Figure 3.38. The first one shows experimental current and voltage waveforms of the transistor S_1 measured for a single switching period (Figure 3.37*a*), while the ZCS turn-ON is shown in zoomed time scale in Figure 3.37*b*. These experimental results are in good agreement with the simulation results in Figure 3.34*d*. Current and voltage of the switch S_1 have nearly zero overlap during the turn-ON, i.e. ZCS assisted with the second qZSN inductor occurs. The negative current spike highlighted is caused by the discharge of the snubber capacitor C_{S2} through this switch. It can be concluded that the soft-switching operation of the top switch is proved in the experiment where voltage drops almost to zero before the current rising started. Quite similar waveforms are shown in Figure 3.38 for the transistor S_2. They show that switch S_2 is turned OFF with ZVS. It is evident from the more detailed waveforms in Figure 3.38*b* that it shows no overlap between turn-OFF voltage and current. Apparently, switches S_3 and S_4 operate under similar soft-switching conditions. Thus, switching losses in the inverter switches of the proposed full soft-switching converter are negligible. The measured values of the overall converter efficiency are within the range from 92 % measured at minimum input voltage and, consequently, maximum shoot-through duty cycle, of up to 95 %, measured at maximum input voltage and therefore at minimum shoot-through duty cycle.



(a) *(b)*

Figure 3.37 Experimental current and voltage waveforms of the switch S_1: during the switching period (a) and zoomed ZCS turn-ON (b).



(a) *(b)*

Figure 3.38 Experimental current and voltage waveforms of the switch S_2: during the switching period (a) and zoomed ZVS turn-OFF (b).

Further development of this concept was reported by the author in [117]. An additional improvement obtained is the shoot-through generation by both inverter legs. It leads to lower conduction losses during the zero states. By performance and efficiency, this modified converter with a new switching control strategy is quite close to that of the qZSSRC. However, the HqZSSRC has high enough efficiency, while it performs input voltage regulation in buck and boost modes. All these solutions are competitors with close performance.

3.2 Reduction of Conduction Losses

3.2.1 Synchronous Quasi-Z-Source Network

Since the qZSC is the step-up converter topology meant for low-voltage applications, the Schottky diodes are typically used in the qZSNs. Therefore, the conduction losses are the main contributor of power dissipation:

$$P_{DqZS\_con} = V_{F\_DqZS} \cdot I_{IN}, \tag{3.23}$$

where V_{F_DqZS} is the forward voltage drop of the diode in the qZSN.

Conduction losses of the qZS diode depend on the input current of the converter. However, due to the relatively high operating current, the qZS diode generates more than 50% of the total losses within the entire operation range of the converter (Figure 1.8). Thus, it could be concluded that a qZS diode can be referred to as the efficiency limiting factor in the impedance-source converters.

The simplest way to reduce the conduction losses of the diode is to increase the number of paralleled devices. As the analysis in Figure 3.39 shows, the parallel connection of two and three diodes could result in the conduction loss reduction by 16% and 22% within the entire operation range of the case study converter. However, the disadvantages of the parallel connection of diodes are the current sharing between the devices, parasitic resonance due to stray inductance and capacitance, and the requirement for the extra installation space. The most problematic issue is the current sharing caused by the mismatch of forward characteristics of the paralleled diodes. Since the forward voltage of Si-diodes has negative temperature dependence, the current sharing problem could get even worse and result in the destruction of the diode.

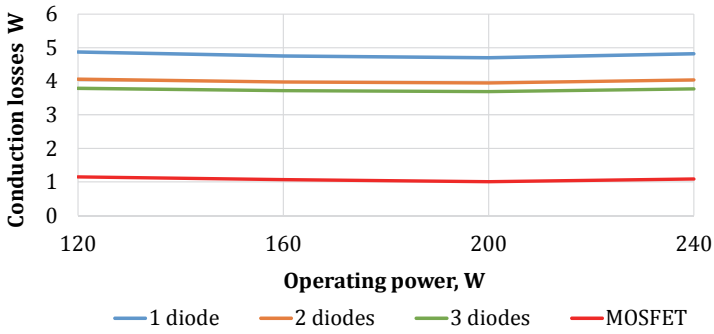


Figure 3.39 Comparison of semiconductor conduction losses of the qZSN in the case of single and paralleled diodes as well as in the case of the MOSFET-based qZSN.

An alternative approach to the paralleling of diodes is a synchronous rectification (SR), where the diode is replaced by the MOSFET. The general idea of SR is discussed in subsection 2.3.2. Typically, the MOSFET used in place of a diode can have a significantly smaller voltage drop at a given current than the diode [119]. Moreover, since the MOSFET has the positive temperature coefficient, the devices can be easier paralleled due to the more even current sharing and, therefore, optimal thermal balance between them.

To reduce the conduction power losses over a diode in the qZS-based converters, the concept of synchronous qZSN was first proposed by the author of this thesis in 2014 [PAPER-III], [PAPER-IV]. As shown in Figure 3.40, the idea behind that is to implement the low $R_{DS(on)}$ N-channel MOSFET instead of the Schottky diode. According to the analysis presented in Figure 3.39, semiconductor conduction losses of the synchronous qZSN will be reduced by roughly 80% for the case study converter as compared to its traditional (diode-based) counterpart.

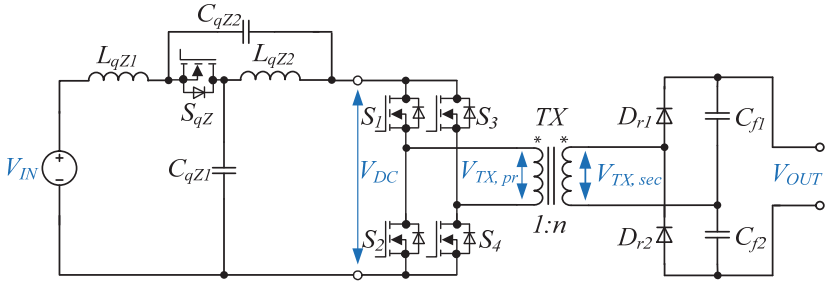
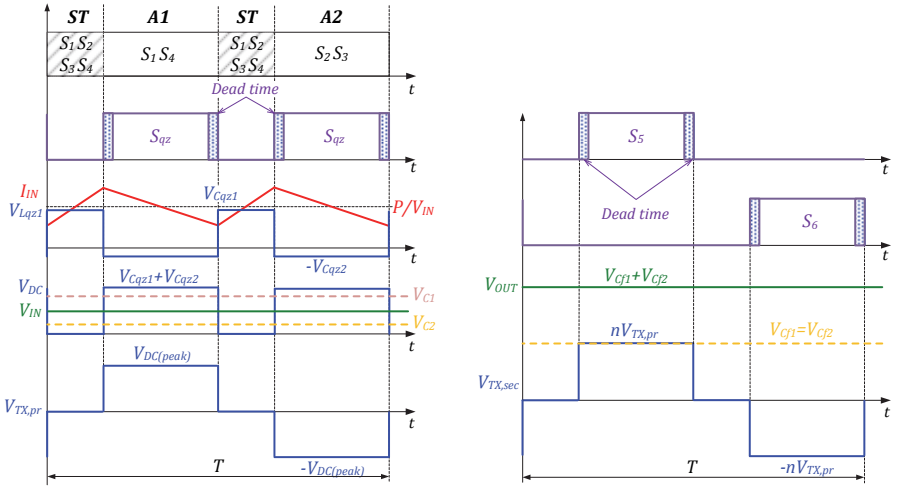


Figure 3.40 qZSC with a synchronous qZSN.

A generalized operation principle of the synchronous qZSN in the shoot-through mode is presented in Figure 3.41*a*. S_{qZ} is synchronized with the inverter switches and it conducts only during the active state and blocks the current during the shoot-through. To prevent damage of the circuit, the dead time is added before the turn-ON and turn-OFF transients of the S_{qZ}, as shown in Figure 3.41. During the dead time, the body diode of the MOSFET is

conducting, therefore to achieve maximum possible efficiency rise, it is recommended to set the dead time as short as possible. Figure 3.42 shows the experimental waveforms of the S_{qz} in the case study converter operating in the maximum boost mode (V_{IN}= 15 V, I_{IN}= 8 A, D_{ST}= 0.25). In the given case study, the Vishay Si4190ADY N-channel MOSFET with $R_{DS(on)}$ = 8.8 mΩ was used as a replacement for the Schottky diode Vishay V60D100C. As a result, with the dead time of 70 ns, the efficiency rise was 1.7 % as compared to the traditional converter with the diode-based qZSN (Figure 3.43).



(a) (b)

Figure 3.41 Generalized operation principle of the qZSC with a synchronous qZSN (a) and synchronous VDR (b).

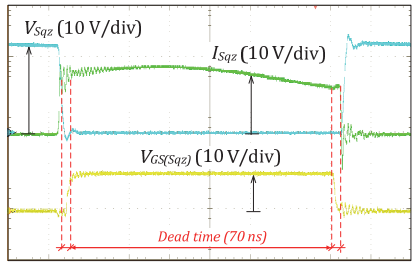


Figure 3.42 Operation of a synchronous qZSN in the test point with maximum shoot-through duty cycle: gating voltage, drain current and drain-source voltage of the MOSFET switch S_{qZ}.

In the normal mode, when the duty cycle of the active state is approaching its maximum, S_{qZ} starts operating in the static mode. The experimental study showed that the efficiency rise in this operating point is 1.2%, as compared to the qZSC with a diode-based qZSN (Figure 3.43). Therefore, considering the gate drive power of S_{qZ}, the resulting efficiency rise caused by the

implementation of the synchronous qZSN is close to 1% for the entire operation range of the case-study converter.

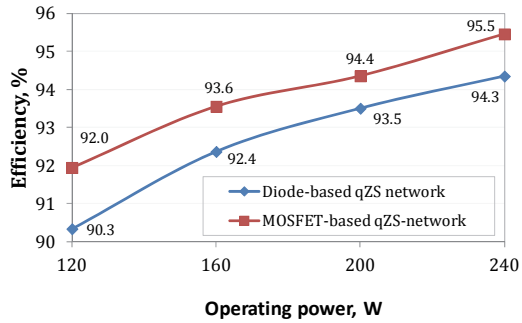


Figure 3.43 Comparison of measured efficiencies of the case-study qZSC with the traditional (diode-based) and proposed (MOSFET-based) qZSN.

3.2.2 Synchronous (Active) Voltage Doubler Rectifier

Similarly to the qZSN, the conduction losses can be reduced also in the diodes D_{r1} and D_{r2} of the voltage doubler rectifier. As the case study shows (Figure 3.44), the conduction losses of the synchronous VDR will be reduced by more than 15 times for the case-study converter as compared to its traditional (diode-based) counterpart.

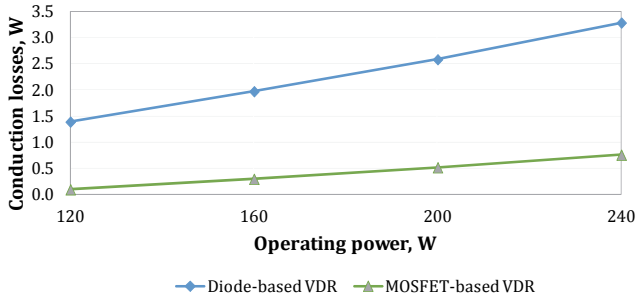


Figure 3.44 Comparison of semiconductor power losses in the case of diode- and MOSFET-based VDR.

Figure 3.41*b* shows the control principle of the synchronous VDR based on the N-channel MOSFETs S_5 and S_6. As seen from the diagram, the dead-time is also necessary before the turn-ON and turn-OFF transients of S_5 and S_6.

In our case study, the SiC Schottky rectifiers CREE C3D02060E were compared to the synchronized VDR based on the SiC MOSFETs ROHM SCT2120AF. The generalized specifications of semiconductors are presented in Table 1.2. The main reason to select the SiC MOSFET was the fast reverse recovery time of the body diode (33 ns), which in more than 20 times better than that of the Si-based superjunction MOSFETs (800 ns in the case of 650 V CoolMOS IPP65R065C7 MOSFET).

The experimental voltage and current waveforms of the VDR MOSFET S_5 are presented in Figure 3.45, where the VDR is hard-switched during the turn-

ON, therefore the resulting benefit of reduced conduction losses will be somehow affected by the switching losses of the MOSFET. The analysis of experimental efficiency shows that in the case-study converter, the implementation of synchronous (active) VDR leads to efficiency rise from 0.1 % at the maximum boost point to 0.5% in the normal mode.

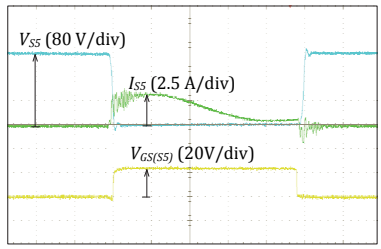


Figure 3.45 Operation of synchronous VDR in the normal mode of the case-study converter: gating voltage, drain current and drain-source voltage of the VDR MOSFET S_5.

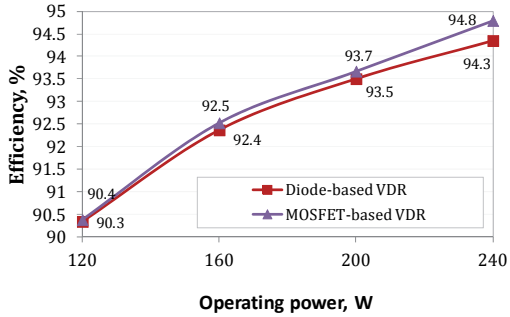


Figure 3.46 Comparison of measured efficiencies of the case-study qZSC with the traditional (diode-based) and synchronous (MOSFET-based) VDRs.

3.2.3 Full-Synchronous Quasi-Z-Source DC-DC Converter

By merging the overall idea of the qZSC with the concepts of synchronous qZSN and synchronous VDR discussed in sections 3.2.1 and 3.2.2 respectively, a novel topology of the high-performance DC-DC converter could be derived. As compared with the baseline qZSC in Figure 1.1, the novel *Full-Synchronous qZSC (FSqZSC)* (Figure 3.47) has the following advantages:

- improved efficiency over the entire range of the input voltage and load variations thanks to synchronous rectification,
- bidirectional operation capability without any modifications in the hardware,
- elimination of the discontinuous conduction mode (DCM) thanks to the synchronous qZSN.

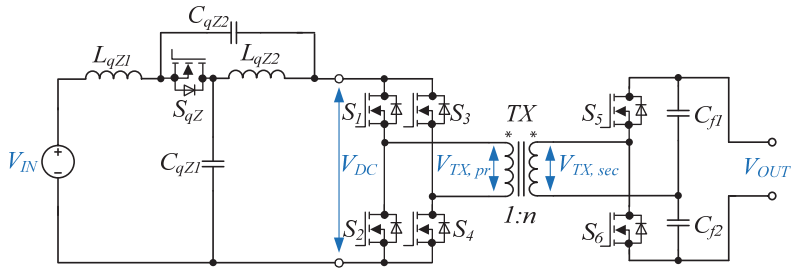


Figure 3.47 Generalized topology of the FSqZSC.

It is shown in Figure 3.48 that due to decreased conduction losses, the replacement of diodes by the N-channel MOSFETs in the qZSN and the voltage doubler rectifier has resulted in the efficiency by 1.8% and 1.9% for the maximum boost and normal operating modes, correspondingly. In order to further maximize the efficiency, special attention should be paid to the proper selection of the dead time before the turn-ON and turn-OFF transients of the synchronous switches to limit the conduction time of the body diodes.

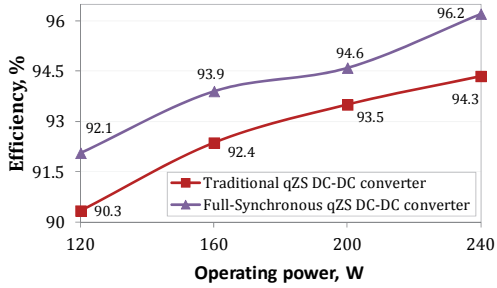
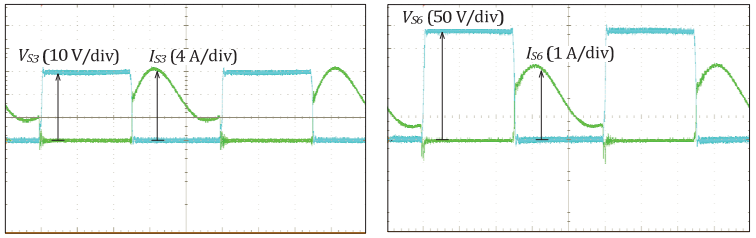


Figure 3.48 Comparison of measured efficiencies of the qZSC and FSqZSC.

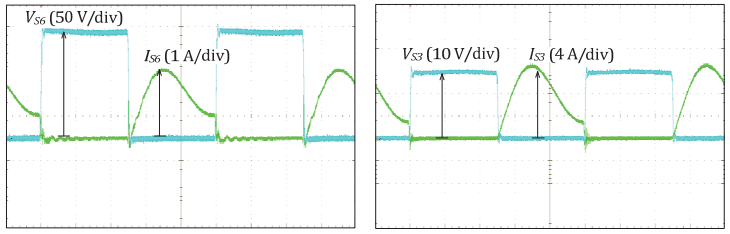
Since the FSqZSC is realized on the controlled switches, it features the bidirectional operation capability without any hardware modifications. The concept of the bidirectional qZSC was first proposed in [120] as an interface converter for the ultracapacitor powered applications. The discussed topology was based on the combination of a full-bridge qZS inverter and half-bridge VSI on the low-voltage and high-voltage sides, correspondingly. During the operation the power flow is controlled only by the front-end inverter, while the integrated (freewheeling) diodes of the second inverter bridge are used as a passive rectifier. Moreover, to ensure the bidirectional power flow, the diode of the qZSN should be bypassed by the external switch or a contactor. Finally, it was suggested that the discussed topology suffers from the lack of efficiency and overall performance since the dynamic and static properties of the antiparallel diodes are significantly worse than those of their discrete counterparts.

The advantage of the proposed FSqZSC is that it could operate in the configuration “inverter-synchronous rectifier” in both directions. The control of the output voltage in the forward mode (low-to-high voltage conversion) is similar to that of the traditional qZSC. During the operation in reversed mode (high-to-low voltage conversion) the MOSFET of synchronous qZSN is turned ON and the power flow is controlled from the high-voltage side by the duty cycle variation of the half-bridge inverter. As it is seen from experimental results (Figure 3.49 and 3.50), the FSqZSC features soft-switching in both directions: ZCS turn-OFF in the forward mode only, and full ZCS in the reverse mode. Experimental study shows an efficiency rise from 93.3% to 95.9% in the forward mode and from 91.1% to 95.3% in the reversed mode after activation of synchronous rectification at the operating power of 240 W.



(a) *(b)*

Figure 3.49 Experimental waveforms of FSqZSC in the forward mode (low-to-high voltage conversion): drain current and drain-source voltage of the full-bridge MOSFET S_3 (a) and drain current and drain-source voltage of the half-bridge MOSFET S_6 (b).



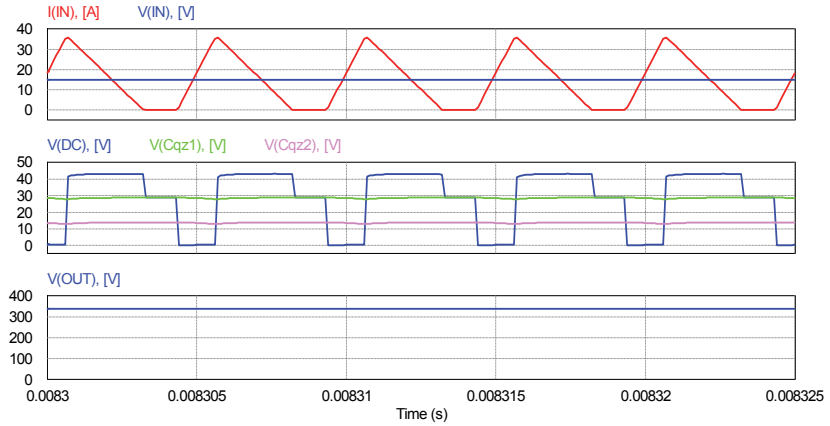
(a) *(b)*

Figure 3.50 Experimental waveforms of FSqZSC in the reverse mode (high-to-low voltage conversion): drain current and drain-source voltage of the half-bridge MOSFET S_6 (a) and drain current and drain-source voltage of the full-bridge MOSFET S_3 (b).

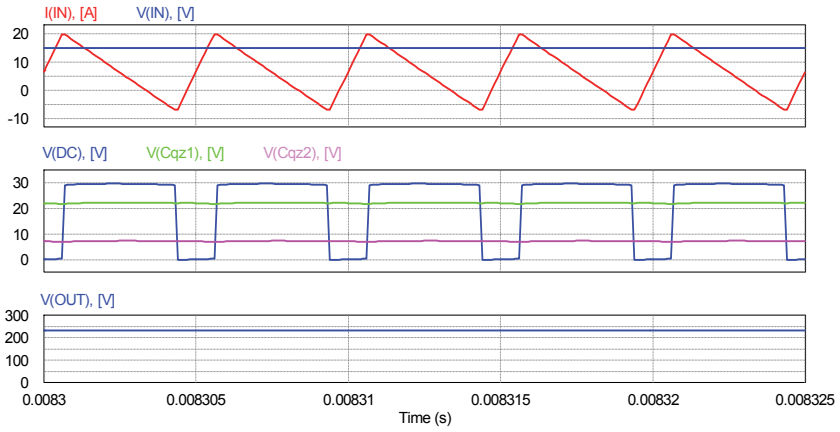
In the synchronous qZSN, the MOSFET operates in the third quadrant and its current flows from the source to drain. This eliminates fully the discontinuous conduction mode (DCM) operation [8], [115], which could occur in the DC-DC converter with a diode assisted qZSN at light load, relatively low switching frequency and low inductance values of qZS inductors [10].

In a traditional approach during the DCM, the qZS diode stops to conduct and the current of the qZS inductor falls to zero. Finally, it causes the overboost effect of the intermediate DC-link voltage V_{DC} and excess rise of the output

voltage [115]. Moreover, the voltage stresses on the components during the DCM operation are significantly increased, which could finally result in the destruction of the converter. In the FSqZSC, the synchronous switch S_{qz} always operates in continuous conduction, thus eliminating the DCM. Figure 3.51 presents the simulation results of the case-study converter with the significantly reduced inductance value of the qZS inductors (1 µH against 22 µH for the baseline converter). It is seen that in the maximum boost point, the converter operates in the DCM, which results in more than 40% increase of the amplitude voltage value of the intermediate DC-link and, consequently, more than 100 V higher output voltage for the same operating conditions as in the case of the converter operating in the CCM. The implementation of the synchronous qZSN helps to keep the intermediate DC-link voltage on the desired level and, therefore, normally control the output voltage of the qZSC within a wide range of load variations.



(a)



(b)

Figure 3.51 Generalized waveforms of the traditional qZSC operating at DCM (a) and resulting effect caused by the implementation of the synchronous qZSN (b).

4 CONCLUSIONS AND FUTURE WORK

Focus in this PhD research was on the development and experimental validation of new methods, topologies and control algorithms aimed at the reduction of semiconductor power losses and, consequently, efficiency improvement of the galvanically isolated qZS DC-DC converters (qZSCs). First, power losses in semiconductors of the MOSFET-based qZSC were analyzed in detail to define the research directions. It was found that the diodes are the main limiters to efficiency and performance of the case-study qZSC. Next, the state-of-the-art techniques of the semiconductor power loss reduction in the traditional voltage- and current-source galvanically isolated DC/DC converters were systematized and analyzed, which allowed selecting the most suitable approaches to be applied in the qZSC. This was followed by the comprehensive research and development work, which has resulted in a variety of novel efficiency and performance improvement techniques proposed for the family of impedance-source galvanically isolated DC-DC converters, and for the qZSCs, in particular. It was found that the soft-switching performance of the qZSC could be enhanced by the modification of the control algorithm (five novel shoot-through generation methods were proposed), by the modification of the topology (new *Hybrid quasi-Z-source series resonant DC-DC converter*) and by modifying both, the control algorithm and the topology (new *Full-soft switching quasi-Z-source DC-DC converter*). To reduce the conduction power losses over a diode in the quasi-Z-source network, the concept of synchronous qZSN was first proposed in this thesis. Moreover, it was experimentally validated that due to reduced conduction losses, the combination of synchronous qZSN and synchronous VDR could feature the efficiency rise of the qZSC up to 1.9% as compared to the traditional diode-based counterpart.

It is important to note here that all the proposed efficiency improvement techniques were initially meant for the qZSC with the full-bridge switching stage, i.e. where the inverter is composed from four switches and supplies the isolation transformer with symmetrical voltage pulses of equal magnitude. Typically, this approach requires four independent gate driving circuits to realize the shoot-through control strategies properly. In several price-sensitive applications, such as microconverters for PV systems, this requirement could create some feasibility concerns.

To overcome this disadvantage, several qZS-derived DC-DC converters with a reduced number of switches were recently developed: the qZS push-pull converter [121] and the symmetrical qZS half-bridge DC-DC converter [124]. Both topologies have two transistors in their switching stage, which reduces complexity of the switching stage and simplifies its control.

In contrast to the push-pull counterpart, the symmetrical qZS half-bridge DC-DC converter is characterized by twice reduced voltage stress of the transistors and a two-winding isolation transformer. In addition, the converter could be supplied either from one or two input voltage sources. However, to ensure the symmetrical structure of the impedance-source network, mirror

connection of two identical qZS networks is required. That seems to be the main drawback of the symmetrical qZS half-bridge DC-DC converter since it uses twice more passive components and is more costly and less efficient than the traditional full-bridge qZSC.

For furtherance of the research and development activity described in the thesis, the author proposes a novel asymmetrical qZS half-bridge DC-DC converter to be evaluated as an alternative approach to qZS-derived DC-DC converters with reduced count of switches. This topology shown in Figure 4.1 was derived by the combination of the single-switch qZSC [122] and the half-bridge galvanically isolated DC-DC converter [123]. The proposed topology is simpler than the symmetrical qZS half-bridge DC-DC converter discussed in [124] since it is based on a single qZSN.

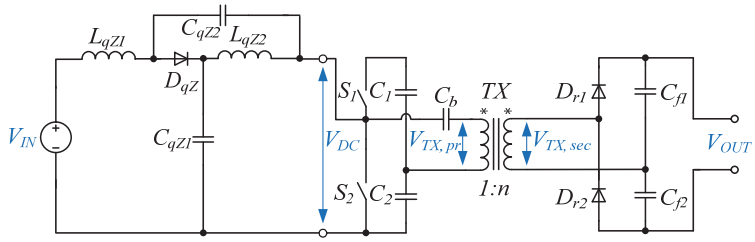


Figure 4.1 New asymmetrical qZS half-bridge DC-DC converter.

The preliminary study results of the proposed topology presented in Figure 4.1 were already discussed in [PAPER-XI]. The converter is composed from the qZSN, an isolation transformer and a VDR with the parameters similar to those presented in Table 1.2. Two 100 µF electrolytic capacitors were used to create the half-bridge configuration of the inverter. Since the transformer is supplied by the asymmetrical pulses, the 5.5uF DC blocking capacitor C_b is added in series with the primary winding of the isolation transformer to prevent the transformer's saturation. The topology was studied with the input voltage V_{IN} = 25 V, shoot-through duty cycle D_{ST} = 0.3, switching frequency 100 kHz and operating power 200 W. Figure 4.2 shows that the proposed converter ensures the demanded gain of the input voltage (V_{OUT} = 240 V) and continuous input current with peak-to-peak ripple of 6 A. The simulation results also show the sine wave current of the primary winding of the isolation transformer. This effect is caused by the series resonant circuit formed by the DC blocking capacitor C_b and the primary winding leakage inductance of the isolation transformer. By proper utilization of those elements, soft-switching could be achieved for the half-bridge inverter switches.

The proposed asymmetrical half-bridge topology could be simplified further by the reconfiguration of the switching stage. In that case, the upper capacitor C_1 of the half-bridge switching stage should be short-circuited, as shown in Figure 4.3. The general operating principle of the modified topology remains the same. Minimization of components count will lead to higher voltage stress of the primary side capacitors. Capacitor C_1 should be dimensioned for the

operating voltage equal to the amplitude value of the intermediate DC-link voltage V_{DC}. The blocking capacitor C_b needs to withstand higher DC voltage because the half-bridge switching stage supplies the transformer with unipolar voltage pulses in contrast to bipolar in the previous topology.

The next challenge for the author will be to analyze the resonant switching processes and the resulting soft-switching performance as well as the experimental study of power losses and efficiency enhancement methods of the proposed converters.

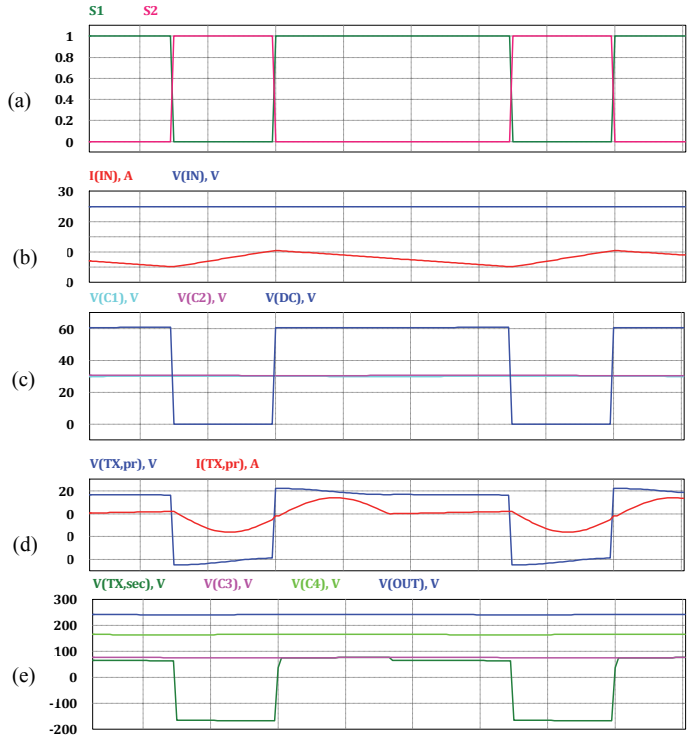


Figure 4.2 Simulation study of the proposed topology: gating signals of switches (a), input voltage and current (b), voltages of half-bridge capacitors and intermediate DC-link voltage (c), voltage and current of the primary winding (d) and secondary winding voltage, voltages of VDR capacitors and output voltage of the converter (e).

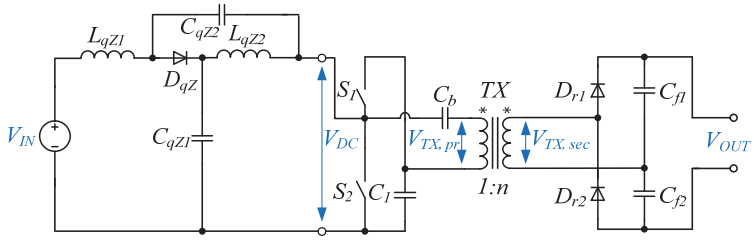


Figure 4.3 Asymmetrical qZS half-bridge DC-DC converter with a single capacitor in the half-bridge switching stage.

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List of Author's Publications

The present doctoral thesis is based on the following publications that are referred to in the text by Roman numbers.

[PAPER-I] Vinnikov, D.; Zakis, J.; **Liivik, L.**; Rankis, I. qZS-Based Soft-Switching DC/DC Converter with a Series Resonant LC Circuit. *Energy Saving. Power Engineering. Energy Audit*, 2013, 114(8-2), 42 - 50.

[PAPER-II] Zakis, J.; Rankis, I.; **Liivik, L**. Loss Reduction Method for the Isolated qZS-based DC/DC Converter. *Electrical, Control and Communication Engineering*, 2013, 4, 13 - 18.

[PAPER-III] **Liivik, L.**; Vinnikov, D.; Jalakas, T. Synchronous Rectification in Quasi-Z-Source Converters: Possibilities and Challenges. *IEEE International Conference on Intelligent Energy and Power Systems (IEPS2014)*, June 2-6, 2014, Kyiv, Ukraine, 32 - 35.

[PAPER-IV] **Liivik, L.**; Vinnikov, D.; Zakis, J. Simulation Study of High Step-Up Quasi-Z-Source DC-DC Converter with Synchronous Rectification. *55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, 2014, 34 - 37.

[PAPER-V] Chub, A.; **Liivik, L.**; Vinnikov, D. Impedance-Source Galvanically Isolated DC/DC Converters: State of the Art and Future Challenges. *IEEE 55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, 2014, 67 - 74.

[PAPER-VI] Roasto, I.; **Liivik, L.**; Vinnikov, D. Control of Quazi Z-source DC-DC Converter by the Overlap of Active States: New Possibilities and Limitations. *14th Biennial Baltic Electronics Conference*, Tallinn, Estonia, October 6-8, 2014, 217 - 220.

[PAPER-VII] Vinnikov, D.; Roasto, I.; **Liivik, L.;** Blinov, A. Four Novel PWM Shoot-Through Control Methods for Impedance Source DC-DC Converters. *Journal of Power Electronics*, 2015, 15(2), 299 - 308.

[PAPER-VIII] Kosenko, R.; **Liivik, L.;** Chub, A.; Velihorskyi, O. Comparative Analysis of Semiconductor Power Losses of Galvanically Isolated Quasi-Z-Source and Full-Bridge Boost DC-DC Converters. *Electrical, Control and Communication Engineering*, 2015, 8, 5 - 12.

[PAPER-IX] Zakis, J.; Rankis, R.; **Liivik, L.;** Chub, A. Analysis of Buck Mode Realization Possibilities in Quasi-Z-Source DC-DC Converters with Voltage Doubler Rectifier. *IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG)*, Riga, Latvia, 11-13 May, 2015, 1 - 5.

[PAPER-X] **Liivik, L.**; Chub, A.; Vinnikov, D.; Zakis, J. Experimental Study of High Step-Up Quasi-Z-Source DC-DC Converter with Synchronous Rectification. *9th International Conference on Compatibility and Power Electronics. (CPE),* Lisbon, Portugal, 24-25 June, 2015 pp. 1-6.

[PAPER-XI] Vinnikov, D.; Chub, A.; **Liivik. L**. Asymmetrical Quasi-Z-Source Half-Bridge DC-DC Converters. *9th International Conference on Compatibility and Power Electronics. (CPE)*, Lisbon, Portugal, 24-25 June, 2015 pp. 1-4.

Author's Own Contribution

This section describes the author's contribution to the papers listed in the thesis as author's publications.

[PAPER-I] Liisa Liivik co-authored the paper, responsible for the data collection, modeling, analyses, and literature review.

[PAPER-II] Liisa Liivik co-authored the paper, responsible for the literature review, data collection, calculations, and modeling. She presented the paper at 54th International Scientific Conference (RTUCON 2013), 14-16 October, Riga.

[PAPER-III] Liisa Liivik is the main author of the paper, responsible for the literature review, data collection, and calculations. She had a major role in writing.

[PAPER-IV] Liisa Liivik is the main author of the paper, responsible for the literature review, data collection, and calculations. She had a major role in writing. She presented the paper at IEEE 55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON 2014).

[PAPER-V] Liisa Liivik co-authored the paper, responsible for the data collection, calculations, and literature review. She had a major role in writing. She presented the paper at IEEE 55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON 2014).

[PAPER-VI] Liisa Liivik co-authored the paper, responsible for the literature review, data collection, analyses. She presented the paper at IEEE 14th Biennial Baltic Electronics Conference (BEC 2014), Tallinn, Estonia, 6-8 October 2014.

[PAPER-VII] Liisa Liivik co-authored the paper, responsible for the literature review, data collection, and analyses.

[PAPER-VIII] Liisa Liivik co-authored the paper, responsible for the data collection, performed calculations, modeling, and literature review.

[PAPER-IX] Liisa Liivik co-authored the paper, responsible for the literature review, data collection, calculations, and experimental measurements. She presented the paper at IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG), Riga, Latvia, 11-13 May 2015.

[PAPER-X] Liisa Liivik is the main author of the paper, responsible for the literature review, data collection, calculations, and modeling. She had a major role in writing. She presented the paper at 9th International Conference on Compatibility and Power Electronics. (CPE 2015). Lisbon, Portugal, 24-25 June 2015.

[PAPER-XI] Liisa Liivik co-authored the paper, responsible for the data collection, literature review, and performed calculations and simulations. She presented the paper at 9th International Conference on Compatibility and Power Electronics. (CPE 2015). Lisbon, Portugal, 24-25 June 2015

Abstract

Semiconductor Power Loss Reduction and Efficiency Improvement Techniques for the Galvanically Isolated Quasi-Z-Source DC-DC Converters

Galvanically isolated impedance-source (IS) DC-DC converter technology is an emerging trend of electric energy conversion alternative to voltage-source and current-source technologies. A quasi-Z-source DC-DC converter (qZSC) is the most advantageous representative of the family of galvanically isolated IS DC-DC converters. The qZSC features continuous input current, immunity to shoot-through and open states of the inverter bridge, low inrush current, high control flexibility, wide input voltage regulation, galvanic isolation of the input and output sides, etc. Therefore, the qZSC can be highly beneficial as a power electronics building block for dispersed generation systems.

However, despite all its benefits, the qZSC topology is still not "industrially recognized" mostly due to its efficiency limitations. Since the qZSC is a step-up converter, its operation is always connected to the low voltage and high current values at the input side, which lead to high power losses in the front-end quasi-Z-source (qZS) inverter. According to the analysis of losses, the diode in the qZS-network is the main contributor to total power dissipation of the qZSC. It is responsible for more than 50% of power losses generated by the semiconductors over the entire operating range of the converter. By considering also the power dissipation in the inverter switches and diodes of the voltage doubler rectifier it could be stated that the power losses in semiconductors solely limit the peak efficiency of qZSC at the moderate level of 95.9%.

The main aim of this PhD research was to develop and experimentally validate new methods, topologies, control algorithms, and design guidelines aimed at the reduction of semiconductor power losses and, consequently, efficiency improvement of the qZSC. As a result of a comprehensive research and development work, a variety of hardware and software improvement possibilities of the qZSC were proposed and experimentally validated. For example, it was found that the synchronous qZS-network could feature an efficiency rise close to 1% for the entire operation range of the qZSC. Moreover, such novel topological variations of the qZSC as *Hybrid quasi-Z-source series resonant DC-DC converter* and *Full-soft switching quasi-Z-source DC-DC converter* proposed by the author of the thesis are not only aimed at the reduction of switching losses of semiconductors but will also help to improve the power density and widen the input voltage and load regulation range of the qZSC.

Since all the efficiency improvement methods proposed in this thesis are applicable to all existing types of the impedance-source networks it is expected that outcomes of this research will substantially contribute to the further development of the emerging field of the galvanically isolated impedance source DC-DC converters.

Kokkuvõte

Galvaaniliselt isoleeritud kvaasiimpedantsallikaga alalispingemuunduri pooljuhtide võimsuskao vähendamine ja kasuteguri suurendamine

Seniste pinge- ja/või voolutoiteliste energiamuundamistehnoloogiate kõrval on uueks alternatiivseks arengusuunaks galvaaniliselt isoleeritud kvaasiimpedantsallikaga alalispingemuundur. Kvaasiimpedantsallikaga (qZS) alalispingemuundur on galvaaniliselt isoleeritud alalispingemuundurite klassi kõige tulemuslikum. Selle muunduri iseloomulikeks omadusteks on katkematu (võrgusõbralik) sisendvool, immuunsus muundursilla lühis- ja avatud olekute suhtes, väike käivitusvool, juhtimise paindlikkus, sisendpinge laiaulatuslik reguleeritavus, sisend- ja väljundpoole galvaaniline eraldatus jne. Nende omaduste tõttu võib qZS-muundur osutuda väga kasulikuks jõuelektroonika elemendiks elektritootmise hajasüsteemide loomisel.

Kõigile headele omadustele vaatamata ei ole qZS-muundur siiski leidnud "tööstuslikku tunnustust" peamiselt oma madala kasuteguri tõttu. Kuna qZS-muundur on pinget tõstev muundur, siis on ta sisendis alati madal pinge ja suur vool, mis põhjustab seal suuri võimsuskadusid. Kadude analüüs näitab, et muunduri võimsuskao peamiseks põhjustajaks on kvaasiimpedantsahelas olev diood. Diood põhjustab üle 50% muunduri kõigi pooljuhtide poolt kogu töötsükli jooksul tekitatud kadudest. Võttes arvesse ka kaovõimsuse muunduri lülitites ja pingekordistusalaldi dioodides, võib väita, et ainuüksi juba pooljuhtide võimsuskadude tõttu ei saa qZS-muunduri kasutegur tõusta üle 95,9%.

Antud doktoritöö eesmärk oli arendada ja eksperimentaalselt kinnitada uusi meetodeid, topoloogiaid ja juhtimisalgoritme ning kujundada suunised isoleeritud kvaasiimpedantsallikaga alalispingemuunduri pooljuhtide võimsuskadude vähendamiseks, et parendada muunduri kasutegurit.

Põhjaliku uurimis- ja arendustöö tulemusena on antud töös pakutud erinevaid qZS-muunduri riist- ja tarkvara täiustamise võimalusi, mis on eksperimentaalselt kontrollitud. Näiteks leiti, et sünkroonse qZS-ahelaga võib saavutada kasuteguri tõusu kuni 1% võrra muunduri kogu tööpiirkonnas.

Veel enam, sellised doktoritöö autori poolt pakutud qZS-muunduri uuenduslikud topoloogilised variatsioonid nagu hübriid kvaasiimpedantsallikaga järjestikresonants-alalispingemuundur ja pehme kommutatsiooniga qZS-muundur ei ole mõeldud üksnes pooljuhtide lülituskadude vähendamiseks, vaid aitavad parandada ka võimsustihedust ja laiendada muunduri sisendpinge ja koormuse reguleerimise ulatust.

Kuna kõik käesolevas teadustöös pakutud meetodid on rakendatavad kõikidele olemasolevatele kvaasimepedantsallikatega ahelatele, loob selle töö tulemuste kasutamise eeldused kaasa edasisele galvaaniliselt isoleeritud kvaasiimpedantsallikaga alalispingemuundurite arengule.

Elulookirjeldus

1. Isikuandmed

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TTÜ elektriajamite ja jõuelektroonika instituut	1998	Diplomeeritud inesener
Tartu 4.keskool	1993	Keskharidus

3. Keelteoskus (alg-, kesk- või kõrgtase)

Keel	Tase
Eesti keel	Kõrgtase
Vene keel	Kõrgtase
Inglise keel	Kesktase

4. Teenistuskäik

Töötamise aeg	Tööandja nimetus	Ametikoht
2002-2007	Tallinna Tehnikaülikool	Lektor
1998-2002	Tallinna Tehnikaülikool	Assistent
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5. Teaduspreemiad ja tunnustused

2000; Eesti Teaduste Akadeemia üliõpilastetööde konkursi II preemia magistritöö eest „Raalarvutused elektrotehnikas”

6. Teadustöö põhisuunad

Loodusteadused ja tehnika, Energeetikaalased uuringud, Energeetika

7. Jooksvad projektid

- Aktiivsete elektrijaotusvõrkude muundurite topoloogiad ja juhtimismeetodid
- Pehmelülitusega galvaaniliselt isoleeritud alalispingemuundurite uus perekond

Curriculum Vitae

1. Personal data

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TUT Department of Electrical Drives and Power Electronics	2000	Master of Science
TUT Department of Electrical Drives and Power Electronics	1998	Diploma Engineer
Tartu Secondary School No 4	1993	Secondary education

3. Language competence/skills (fluent; average, basic skills)

Language	Level
Russian	Fluent
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English	Average

4. Professional Employment

Period	Organization	Position
2002-2005	TUT Department of Electrical Drives and Power Electronics	Lecturer
1998-2002	TUT Department of Electrical Drives and Power Electronics	Assistant
01.09.1998-31.01.1999	TUT Engineering Service	Engineer

5. Honours & Awards

2000 II award for master thesis "Numerical Calculations of Electrical Engineering" from Estonian Academy of Sciences

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Natural Sciences and Engineering, Energetic Research, Energy research

7. Current grants & projects

- New Converter Topologies and Control Methods for Electronic Power Distribution Networks
- New Family of Full Soft-Switching Galvanically Isolated DC/DC Converters

Appendix

[PAPER-I] Vinnikov, D.; Zakis, J.; **Liivik, L.**; Rankis, I. qZS-Based Soft-Switching DC/DC Converter with a Series Resonant LC Circuit. *Energy Saving. Power Engineering. Energy Audit*, 2013, 114(8-2), 42 - 50.

УДК 621.314.1

qZS-BASED SOFT-SWITCHING DC/DC CONVERTER WITH A SERIES RESONANT LC CIRCUIT

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This paper discusses further modifications of the recent popular qZS-based DC/DC converter design by the introduction of the resonant LC circuit in series to the primary winding of the isolation transformer. The primary aim is to achieve the zero voltage and zero current switching of transistors. As an additional benefit of the resonant LC circuit, the converter is able to perform the voltage buck function simply by changing the switching frequency of the transistors. The control principle of the converter and its main operating modes are explained. The theoretical assumptions are experimentally verified by help of the small-scale testbench of the converter.

Keywords: qZS-based DC/DC converter, series resonant DC/DC converter, soft switching.

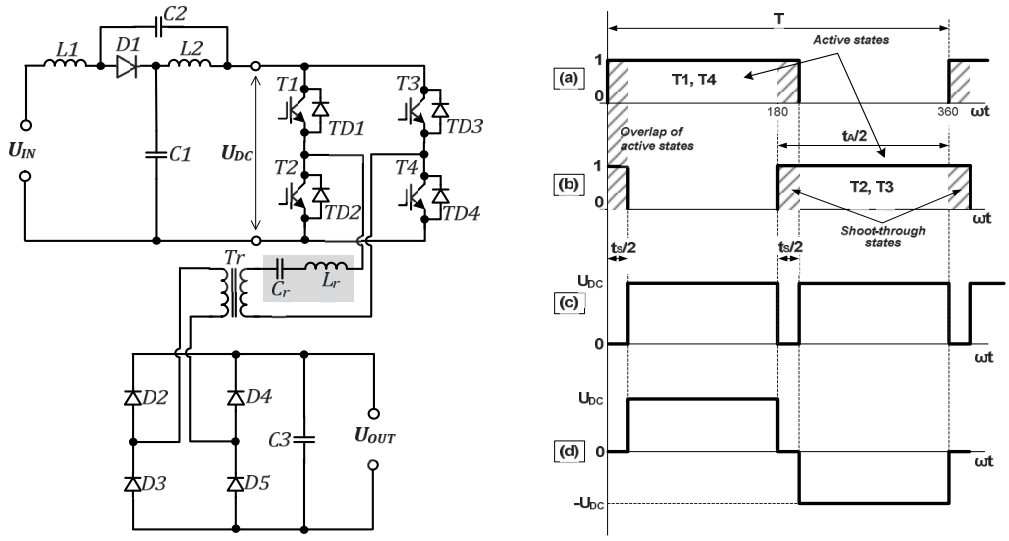
Introduction. The quasi-Z-source (qZS) based DC/DC converter is a novel approach to the galvanically isolated step-up DC/DC converters [1, 2]. Thanks to the qZS-network at the input side, the converter features such important benefits as continuous input current, shoot-through immunity, low inrush current during start-up, and wide regulation freedom of the inverter (integrated buck-boost functionality). Due to its properties, the converter is especially suitable as a power conditioner for renewable energy sources.

Further modification of the qZS-based DC/DC converter is analyzed here. The new topology was derived simply by adding the resonant LC circuit in series with the primary winding of the isolation transformer (Fig. 1*a*). As in a baseline topology, the output voltage is controlled by the variation of the shoot-through duty cycle, which could be realized in different ways [3]. In our case the shoot-through states are created by the overlap of active states, as shown in Fig. 1*b*. It is remarkable that the inverter operates without dead time and the duty cycle of active states of transistors is greater than or equal to 0.5. If the active state duty cycle is greater than 0.5, overlapping occurs and the shoot-through states will be created. During this operating mode the current through the inverter switches reaches its maximum, the voltage across the inverter bridge (U_{DC}) and, consequently, the voltage of the primary winding of the isolation transformer (U_{Tr}) drops to zero. The operating period of the isolation transformer in this control method consists of a shoot-through state t_S and an active state t_A:

$$\frac{t_A}{T}+\frac{t_S}{T}=D_A+D_S=1, \tag{1}$$

$$T=t_A+t_S. \tag{2}$$

where D_A and D_S are the duty cycles of an active and a shoot-through state, correspondingly. As Eq. (1) and Fig. 1*b* show, the duty cycle of the active state will vary with the variation of the shoot-through duty cycle. It approaches its maximum in the non-shoot-through mode, when the input voltage is high enough and the shoot-through states are eliminated, and vice versa, in the conditions of minimal input voltage where the shoot-through duty cycle is maximal, the duty cycle of active states will have a minimum value. It should also be noted that for the proposed voltage-fed qZS topology with the positive input voltage, the maximum shoot-through duty cycle should never exceed 0.5 or the system could get instable.



(a) *(b)*

Fig. 1

Based on this methodology, the switching states sequence is presented in Table 1. The states are shown for one switching period of the isolation transformer. As it can be seen, the transistors work with the same switching frequencies, thus have equal switching losses.

Table 1

States	**T1**	**T2**	**T3**	**T4**
Active state	1	0	0	1
Shoot-through state	1	1	1	1
Active state	0	1	1	0
Shoot-through state	1	1	1	1

Operation Modes of the Proposed Converter. The proposed qZS-based resonant DC/DC converter could operate in three basic modes: normal (or non-shoot-through), boost (or shoot-through) and buck (or series resonant) mode. The first two modes are similar to those of the traditional qZS-based DC/DC converter, however the buck mode provides an additional advantage gained by the implementation of the resonant network.

In the normal mode the input voltage is equal to the DC-link voltage (U_{IN}=U_{DC}). The switching frequency of the inverter switches is equal to the resonant frequency (f_{SW}=f_r) and can be defined as

$$f_{SW} = f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_r C_r}}, \tag{3}$$

where L_r and C_r are the inductance and capacitance values of the resonant inductor and the capacitor, respectively. Fig. 2 shows the theoretical operating waveforms of the qZS-based resonant DC/DC converter topology in the normal mode. Switches here can be turned on and off at perfect zero voltage and zero current condition. Therefore, in this mode, maximum efficiency can be achieved. In this operation mode the current in the resonant circuit can be assumed as a sine wave but the total voltage across both of the reactive elements is zero. It is assumed that diagonal switches (*T1*, *T4* and *T2*, *T3*) are conducting half the period. At the current i_r>0, the voltage applied to the resonant circuit is

$$U_r = U_{IN} - U_{OUT} \cdot k_{Tr}, \tag{4}$$

where U_{OUT} is the output voltage of the converter and k_{Tr}=N_1/N_2 is the transformer turns ratio.

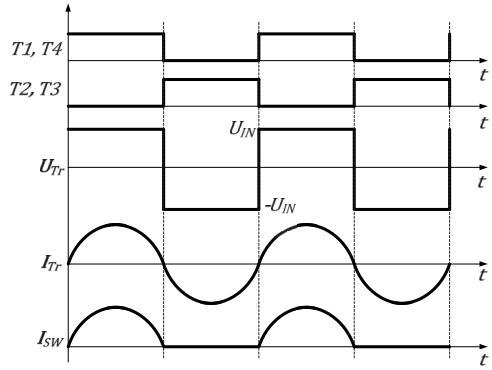


Fig. 2

The same voltage is also applied to the resistance R_r that is actually the impedance of the resonant circuit. Output voltage U_{OUT} of the converter can be expressed as

$$U_{OUT} = \frac{2I_{Tr,m} \cdot k_{Tr} \cdot R_l}{\pi}, \tag{5}$$

where R_l is the resistance of a load. Average current per half cycle of the resonant circuit is

$$I_{Tr} = \frac{2 \cdot I_{Tr,m}}{\pi}. \tag{6}$$

Taking into account that the input power of the converter is $P_{IN}=U_{IN}\cdot I_{IN}$, the power balance between the resonant circuit and load can be expressed as

$$\frac{2I_{Tr,m}}{\pi}\cdot U_{IN}-\frac{I_{Tr,m}^2}{2}\cdot R_r=\frac{4I_{Tr,m}^2\cdot k_{Tr}^2\cdot R_l}{\pi^2}. \tag{7}$$

The amplitude value of the resonant circuit current can be found as

$$I_{Tr,m}=\frac{4\cdot\pi\cdot U_{IN}}{\pi^2R_r+8k_{Tr}^2R_l}. \tag{8}$$

If the input voltage of the converter drops below the nominal value, the converter starts operation in the boost mode. In order to boost the input voltage during this mode, a special switching state — the shoot-through state — is implemented in the inverter control. During the shoot-through states, the primary winding of the isolation transformer is shorted through all switches of both phase legs. This shoot-through state (or vector) is forbidden in the traditional voltage source inverters because it would cause a short circuit of DC capacitors and destruction of power switches. The qZS-network makes the shoot-through states possible, effectively protecting the circuit from damage. Moreover, the shoot-through states are used to boost the magnetic energy stored in the DC-side inductors *L1* and *L2* without short circuiting the DC capacitors *C1* and *C2*. This increase in the magnetic energy, in turn, provides the boost of the voltage seen on the inverter output during the active states. In this operation mode the switching frequency of inverter switches f_{SW} is fixed to the resonant frequency f_r. Fig. 3 shows general operation waveforms in the boost mode where switches can be turned on and off at almost perfect zero voltage and zero current condition.

In the boost operating mode the shape of the resonant circuit current (I_{Tr}) can be also assumed as a sine wave and the relation between the amplitude value of this current and the output voltage can be described using (5). Power losses in the resonant circuit can be calculated as $0.5\cdot I_{Trm}^2\cdot R_r$. However, some additional power losses caused by the shoot-through states of the qZS-inverter will appear in the boost mode. These losses can be simply described as $I_{IN}^2\cdot R_{qZS}$, where I_{IN} is the input current of the converter and R_{qZS} is the equivalent resistance of the qZS-network during shoot-through states.

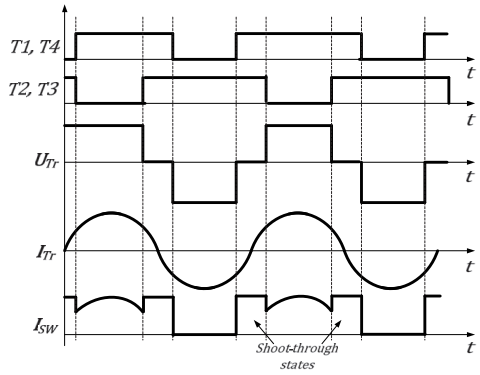


Fig. 3

For the boost mode, the input current of the converter can be expressed as

$$I_{IN} = \frac{2 \cdot I_{Tr,m}}{\pi(1-2D_S)}. \tag{9}$$

Neglecting losses in the transformer and the rectifier, the power balance of the converter can be written as

$$P_{IN} = \Delta P_{qZS} + \Delta P_{Rr} + P_{OUT}. \tag{10}$$

Inserting the corresponding expressions in the power balance equation (10), the amplitude current of the resonant circuit during the boost mode can be expressed as

$$I_{TR,m} = \frac{4 \cdot U_{IN}\pi(1-2D_S)}{8R_{qZS} + 8k_{Tr}^2 R_l (1-2D_S)^2 + \pi^2 R_r (1-2Ds)^2}. \tag{11}$$

In the proposed topology the buck mode is an extra benefit over a baseline solution. In the buck mode the qZS-based resonant DC/DC converter operates as a conventional series resonant converter [4-8] and controls the output voltage by increasing the switching frequency of the qZS-inverter from the resonant frequency f_r to its maximum switching frequency ($f_{sw,max}$). The theoretical operational waveforms in this mode are depicted in Fig. 4. In this configuration, the resonant tank and the load act as a voltage divider. By changing the switching frequency, the impedance of the resonant circuit will also change. Since it is a voltage divider, the DC gain of the qZS-based resonant DC/DC in this operating mode will be always lower than 1.

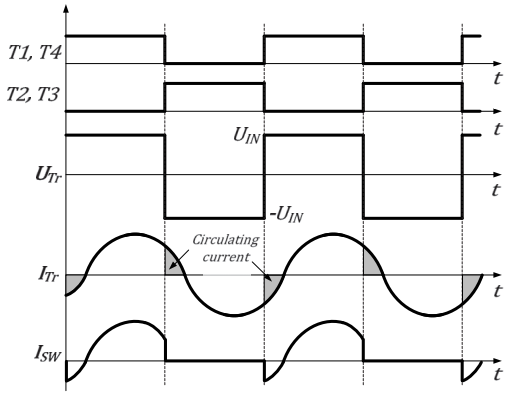


Fig. 4

Experimental Verification. To verify the theoretical assumptions an experimental prototype (Fig. 5) was assembled in accordance with the schematics shown in Fig. 1*a*. Its main component types and values are specified in Table 2. The switching frequency of the qZS-inverter was set to 23 kHz. The series resonant tank was also designed for 23 kHz resonance frequency and consists of a 48 uH inductor and 1 uF capacitor. During the experiments the converter was studied in three operating points according to Table 3.

Fig. 5

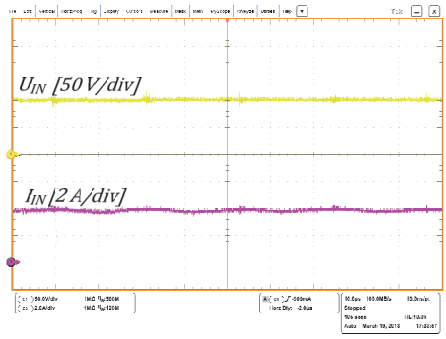
Table 2

Component	Type	Value
C1, C2	Chip Monolithic Ceramic Capacitor SMD1210 X7R 2.2uF 100V GRM32ER72A225K	13μF (matrix configuration)
C3	Metallized Polypropylene Film Capacitors EPCOSB32776G4406	40 uF
L1, L2	Low Profile, High Current SMD Inductors IHLP-6767GZ-A1	56μH (matrix configuration)
Tr	Payton Planar	n=1/1
D1	SiC diode CREE C3D20060D	20A/600 V
T1-T4	N-Channel Si MOSFET FCH47N60N	47A/600 V
Driver core	ACPL-H342-000E	2.5A/15-30V

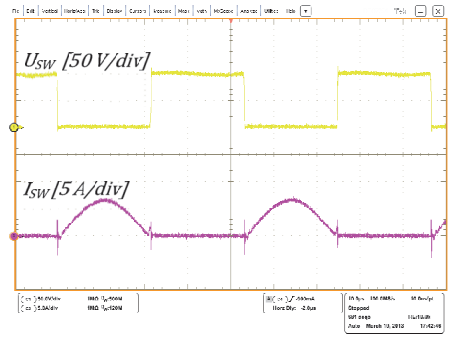
Table 3

Operating point	U_{IN} (V)	D_S	D_A	f_{sw} (kHz)	U_{OUT} (V)	Power (W)
1 (normal mode)	100	0	1	23	95	500
2 (boost mode)	50	0.25	0.75	23	95	500
3 (buck mode)	150	0	1	45	95	500

First experiments (Figs. 6-8) were made at the nominal input voltage when the qZS-inverter operates as a traditional voltage source inverter. The switching frequency was $f_{SW}=f_r=$ 23 kHz. Inverter switches operated at their maximum possible active state duty cycle (D_A =1) without any deadtime.



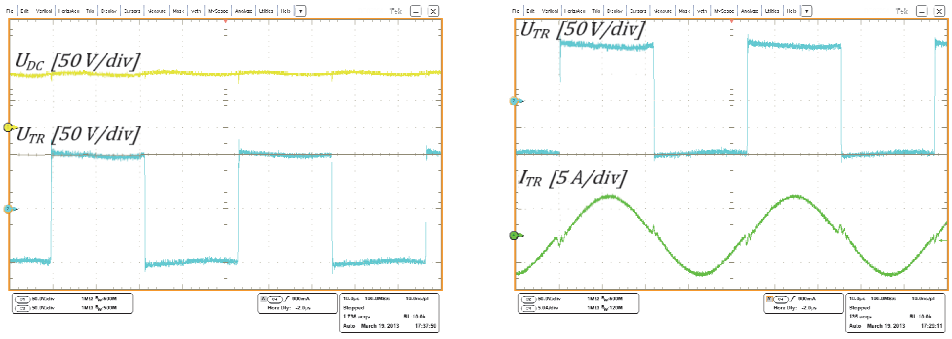
(a)



(b)

Fig. 6

Fig. 6*a* shows that the input voltage and current have linear shapes without any intolerable ripple. The intermediate DC-link voltage U_{DC} equals the input voltage U_{IN}. Fig. 6*b* shows that transistor switches turned on and off at zero voltage and zero current. As shown in Fig. 7*b*, the current shape of the transformer current is close to a sine wave. Moreover, there is no circulating component in the transformer current. Thus, it could be expected that the maximal efficiency of the converter can be achieved in this operation mode.



(a) *(b)*

Fig. 7

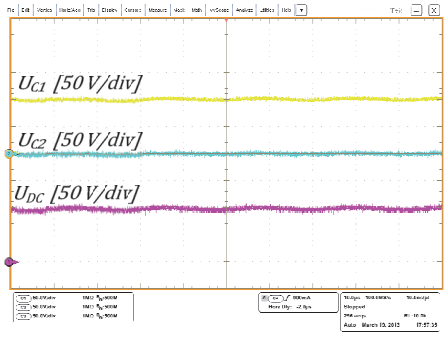
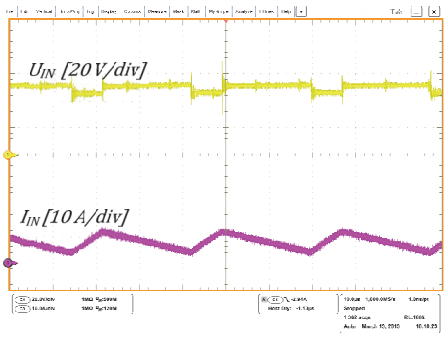
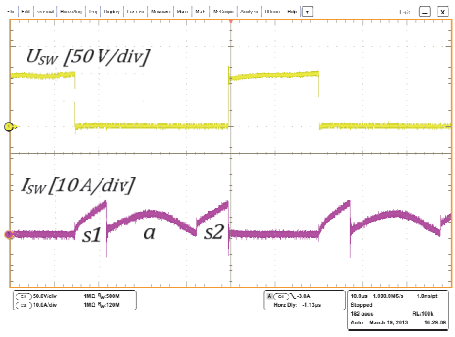


Fig. 8

In the second operating point the converter was tested at the minimum input voltage (U_{IN}=50 V) when the maximal shoot-through duty cycle (D_S) was applied in order to obtain the rated output voltage (U_{OUT}=95 V). Operation frequency of transistor switches f_{SW} corresponds to the resonant frequency f_r of the resonant circuit (f_{SW}=f_r=23 kHz). Fig. 9*a* shows the input voltage and input current when the inverter switches (*T1*…*T4*) are operated at the maximal shoot-through duty cycle (D_S=0.25). The input current shape shows that the converter operates in the continuous conduction mode (CCM). Fig. 9*b* shows that during the first shoot-through state (*s1*) and active state (*a*) intervals, the transistors are fully soft switched. The second shoot-through state (*s2*) starts in the zero voltage conditions but its turn-off is hard switched. The current shape of the transformer current is still close to a sine wave (Fig. 10*b*). Fig. 11 presents both capacitor voltages (U_{C1} and U_{C2}) and the intermediate DC-link voltage of the qZS-inverter. As predicted theoretically, U_{DC} is a sum of capacitor voltages of the qZS network.

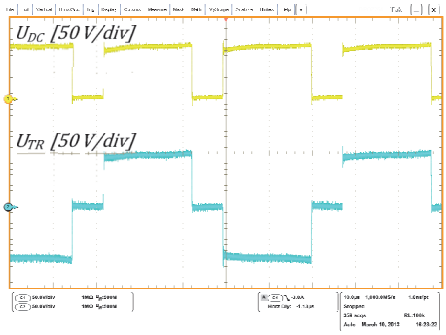


(a)

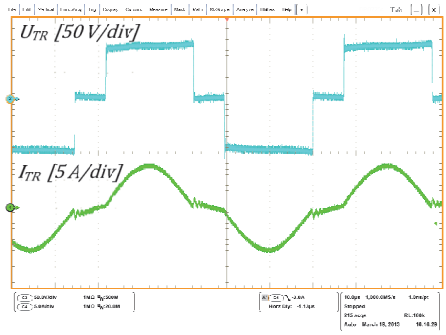


(b)

Fig. 9



(a)



(b)

Fig. 10

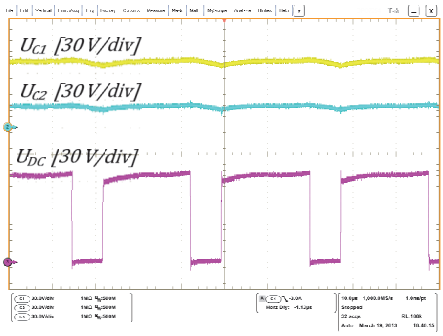
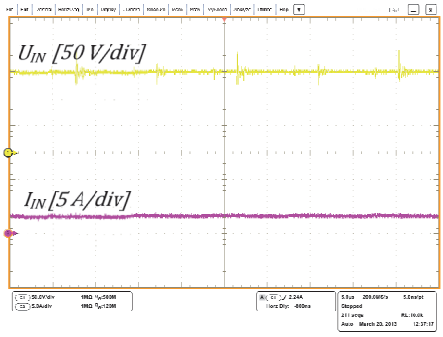
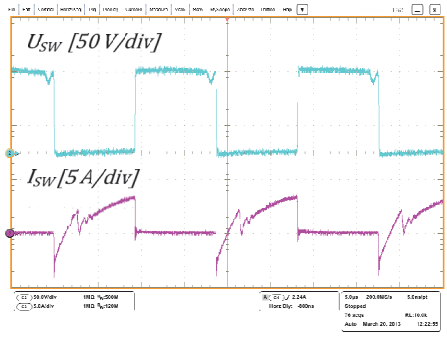


Fig. 11

To verify the converter in the buck mode the input voltage U_{IN} was set to its maximum value (150 V) and U_{OUT} was regulated to 95 V level. The procedure was similar to that of the traditional series resonant DC/DC converter - by increasing the switching frequency of transistors up to 45 kHz. The circulating current in this mode does not contribute to the power transfer of the converter (Figs. 12*b* and 13*b*). The input voltage and current waveforms (Fig. 12*a*) are similar to those of the normal operating mode (Fig. 6*a*). Another distinction of the buck operation mode is that the transformer voltage and current are phase-shifted.

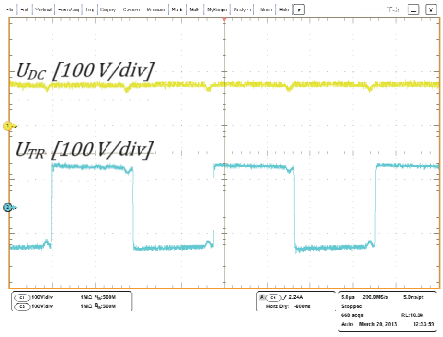


(a)

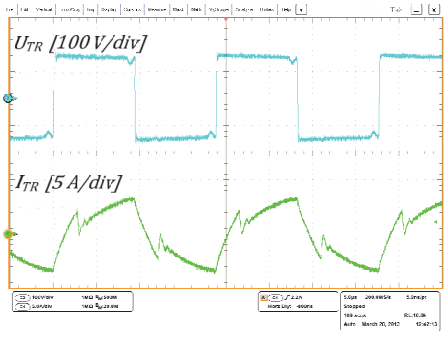


(b)

Fig. 12



(a)



(b)

Fig. 13

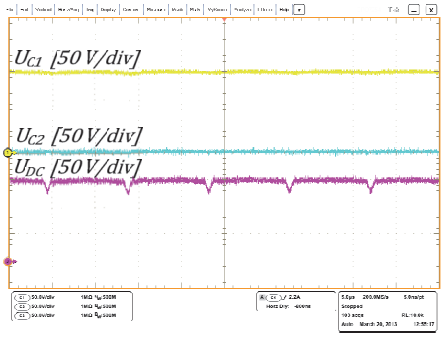


Fig. 14

Conclusions. The proposed qZS-based resonant DC/DC converter is a modified version of the traditional qZS-based DC/DC converter. It can operate in the buck and boost operation mode in contrast to a traditional series resonant converter that performs only the voltage buck function. Thus it is a very desirable circuit topology when the input voltage and the load range of the converter are very wide. Experimental results showed that thanks to the implemented series resonant LC circuit, the qZS-based DC/DC converter could be soft-switched in all operating points except minor power dissipation at the turn-off transient of the

second shoot-through state in the shoot-through mode. Moreover, the new topology combines the advantages of the series resonant DC/DC converter with those of the qZS-based DC/DC converter:

- voltage buck mode could be realized by increasing the switching frequency from the resonance frequency point;
- series capacitor C_r blocks the DC voltage, thus avoiding the transformer saturation,
- continuous input current,
- shoot-through immunity,
- low inrush current during start-up.

Acknowledgments. This research work was financed by Estonian Ministry of Education and Research (project SF0140016s11), Estonian Research Council (Grant G8538) and Latvian Council of Science (Grant 416/2012).

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УДК 621.314.1

КВАЗИ-ИМПЕДАНСНЫЙ DC/DC ПРЕОБРАЗОВАТЕЛЬ С ПОСЛЕДОВАТЕЛЬНЫМ РЕЗОНАНСНЫМ LC-ЗВЕНОМ И МЯГКОЙ КОММУТАЦИЕЙ

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Предложена модификация схемы квази-импедансного DC/DC преобразователя путем последовательного включения резонансного LC-звена и первичной обмотки изолирующего трансформатора. Это позволяет достичь коммутации транзисторов при нулевом токе и нулевом напряжении. К дополнительным преимуществам предложенной схемы DC/DC преобразователя можно отнести способность понижать напряжение путем изменения частоты коммутации транзисторов. Рассмотрен принцип управления преобразователем и его основные режимы работы. Предложенные гипотезы были экспериментально подтверждены с помощью лабораторного макета.

Ключевые слова: *квази-импедансный DC/DC преобразователь, DC/DC преобразователь с последовательным резонансным контуром, мягкая коммутация*

КВАЗІ-ІМПЕДАНСНИЙ DC/DC ПЕРЕТВОРЮВАЧ З ПОСЛІДОВНОЮ РЕЗОНАНСНОЮ LC-ЛАНКОЮ І М'ЯКОЮ КОМУТАЦІЄЮ

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Запропонована модифікація схеми квазі-імпедансного DC/DC перетворювача шляхом послідовного включення резонансної LC-ланки та первинної обмотки ізолюючого трансформатора. Це дозволяє досягти комутації транзисторів при нульовому струмі та нульовій напрузі. До додаткових переваг запропонованої схеми DC/DC перетворювача можна віднести здатність понижувати напругу шляхом зміни частоти комутації транзисторів. Розглянутий принцип керування перетворювачем

та його основні режими роботи. Запропоновані гіпотези були експериментально підтверджені за допомогою експериментального макету.
Ключевые слова: *квазі-імпедансний DC/DC перетворювач, DC/DC перетворювач з послідовною резонансною ланкою, м'яка комутація*

[PAPER-II] Zakis, J.; Rankis, I.; **Liivik, L**. Loss Reduction Method for the Isolated qZS-based DC/DC Converter. *Electrical, Control and Communication Engineering*, 2013, 4, 13 - 18.

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doi: 10.2478/ecce-2013-0016
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Loss Reduction Method for the Isolated qZS-based DC/DC Converter

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Abstract **– This paper presents an isolated quasi-Z-source inverter-based (qZSI) resonant DC/DC converter. The explanation of selection of the proposed topology is justified. Both the normal and the boost modes are discussed. Theoretical operation waveforms as well as basic expressions for the calculation of currents and voltages are proposed. A 1500 W laboratory prototype was built and experimentally verified at two operation points: that of light-load (300 W) and full-load (1500 W). All the experiments were also carried with resonant circuit and without it. The experimental results as well as performance of proposed qZSI based resonant DC/DC converter laboratory setup are presented and analyzed. Experimental and calculated characteristics showing the dependence of the load voltage and supply current on the load resistance in both modes were presented. The dynamic losses in the transistors were evaluated for the cases with the resonant circuit and without it. The main conclusions based on this study are summarized and the future tasks for development of proposed converter were defined.**

Keywords **– DC-DC power converters, resonant inverters, zero current switching, zero voltage switching.**

I. Introduction

In recent years the most challenging tasks for power electronics engineers are connected with efficiency enhancement in switch mode converters.

Focus here is on an efficiency enhancement method for the quasi-impedance-source based (qZS-based) DC/DC converter. According to earlier papers [1-6], the qZS converter has many advantages over other DC/DC converters, such as voltage step-up property in a single stage, continuous input current, excellent immunity of cross-conduction of both switches of one inverter leg, etc. However, very common drawback in all switch mode converters that are coupled with inverters are the dynamic losses during the commutation process of inverter bridge switches [3,4,7,8].

For this reason resonant converters are used due to high efficiency, high switching frequency and high power density. The operation and differences of series resonant converter and parallel resonant converter were studied a lot [9-12]. Each of those converters has its pros and cons [13].

The idea of this paper is to combine advantages of qZSI based DC/DC converter and resonant converter. Series resonant converter topology is the simplest and widely used [9, 10, 14] and will be selected for more detailed study.

Fig. 1 presents the proposed converter which consists of qZS-network (L_1, L_2, C_1, C_2, D) coupled with an inverter (T_1,-T_4), a resonant circuit (L_r and C_r), a transformer (TR), a voltage doubler rectifier (D_1, D_2, C_3, C_4) and a load (R_{ld}). The operation of the converter depends on the input voltage (U_1). If it is at its rated level and equal to U_{DC}, then the converter works as a conventional voltage source inverter (VSI), but if $U_1<U_{DC}$, then the shoot-through switching state of the inverter switches (cross-conduction of both switches of one inverter leg) is introduced [1-6, 15]. By adjusting a proper shoot-through duty-cycle of inverter switches (D_S), the DC-link voltage U_{DC} can be kept on the predefined level.

This paper shows how to improve the efficiency of an inverter by introducing the resonant elements (L_r and C_r) [16] in the transformer circuit.

II. Operation Modes of Proposed Converter

A. Normal Mode

In this operation mode the input voltage is equal to the DC-link voltage ($U_1=U_{DC}$). The switching frequency of inverter switches is equal to the resonant frequency ($f_{SW}=f_r$) and can be defined as

$$f_{SW} = f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_r C_r}}, \qquad (1)$$

where L_r and C_r are resonant inductor and capacitor respectively.

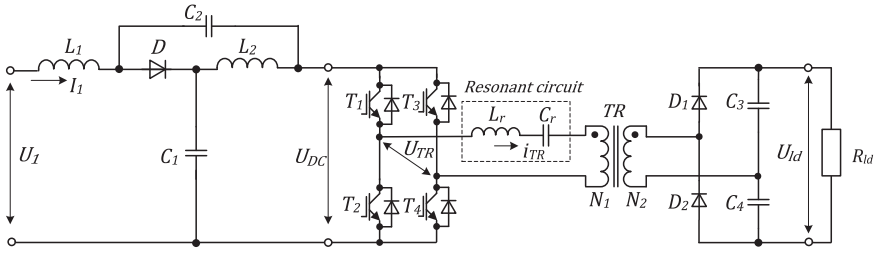


Fig. 1. General circuit diagram of the proposed converter.

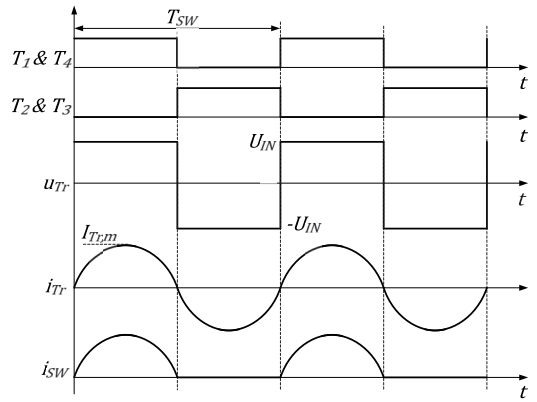


Fig. 2. Theoretical operation waveforms of the proposed converter in the normal operation mode.

Fig. 2 shows the theoretical operation waveforms of the resonant qZSI based converter. Switches here can be turned on and off at almost perfect zero voltage and zero current condition. Therefore, in this mode, maximum efficiency can be achieved.

In such operation mode the current in the resonant circuit can be assumed as a sine wave but the total voltage across both reactive elements is zero. It is assumed that diagonal switches (T_1, T_4 and T_2, T_3) are conducting half the period. At the current $i_{TR}>0$, the voltage applied to the resonant circuit is

$$U_r = U_1 - 0.5U_{ld} \cdot k_{TR}, \quad (2)$$

where U_{ld} is the load voltage and $k_{TR}=N_1/N_2$ is the transformer turns ratio. This voltage is also applied to the resistance R_r that is actually the resistance of the resonant circuit. The load voltage U_{ld} in the circuit diagram in Fig. 1 can be expressed as

$$U_{ld} = \frac{I_{TR,m} \cdot k_{TR} \cdot R_{ld}}{\pi}. \quad (3)$$

Average current per half cycle of the resonant circuit is

$$I_{TR} = \frac{2 \cdot I_{TR,m}}{\pi}, \quad (4)$$

but the input power is $P_1=U_1 \cdot I_1$. Therefore, the power balance of the resonant circuit-load can be expressed as

$$\frac{2I_{TR,m}}{\pi} \cdot U_1 - \frac{I_{TR,m}^2}{2} \cdot R_r = \frac{I_{TR,m}^2 \cdot k_{TR}^2 \cdot R_{ld}}{\pi^2}. \quad (5)$$

The amplitude of the resonant circuit current can be found as

$$I_{TR,m} = \frac{4 \cdot \pi \cdot U_1}{\pi^2 R_r + 2R_{ld} \cdot k_{Tr}^2}. \quad (6)$$

Using the current of the resonant circuit (I_{TR}) allows finding load voltage, load power, input power, loss power and also the amplitude value of the capacitor voltage:

$$U_{Cm} = I_{Cm} \cdot \sqrt{\frac{L_r}{C_r}}, \quad (7)$$

where $\sqrt{\frac{L_r}{C_r}}$ is the resonant impedance.

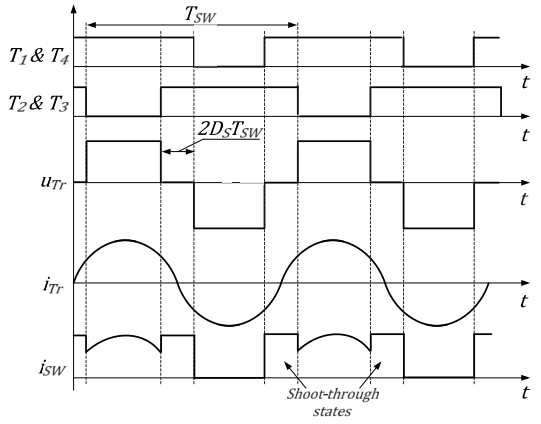


Fig. 3. Theoretical operation waveforms of the proposed converter in the boost operation mode.

B. Boost mode

If the input voltage of the converter drops below the rated value, the shoot-through switching state of inverter switches is introduced to boost the input voltage [1-5, 15].

Also, in this operation mode the switching frequency of inverter switches f_{SW} is fixed to the resonant frequency f_r. Fig. 3 shows general operation waveforms in the boost operation mode. Here the shape of the resonant circuit current (I_{TR}) can also be assumed as a sine wave and then the connection between the amplitude value of this current and the load voltage can be described using (3).

Power losses in the resonant circuit resistance R_r can be calculated as $0.5 \cdot I_{TR,m}^2 \cdot R_r$. However, extra power losses from the shoot-through state of the qZSI appear here, which can be described as $I_1^2 \cdot R_{qZS}$, where the supply current I_1 can be calculated as

$$I_1 = \frac{2 \cdot I_{TR,m}}{\pi(1-2 \cdot D_S)}, \quad (9)$$

where R_{qZS} is an equivalent resistance of the qZS-network during the shoot-through state.

The power balance of the circuit can be categorized as

$$P_1 = \Delta P_{qZS} + \Delta P_{Rr} + P_{ld}. \quad (10)$$

Inserting corresponding expressions in the power balance expression (10), the amplitude of the current of the resonant circuit can be expressed as

$$I_{TR,m} = \frac{4 \cdot U_1 \pi(1-2D_S)}{8R_{qZS} + 2k_{Tr}^2 R_{ld}(1-2 \cdot D_S)^2 + \pi^2 R_r(1-2Ds)^2}. \quad (11)$$

III. Experimental Verification

To evaluate the operation of the proposed converter (Fig. 1) an experimental setup was built. General circuit parameters are summarized in Table I. We made our experiments at two operation points: at light load (300W) when the input voltage is equal to the rated voltage and at full load (1500W) when

TABLE I

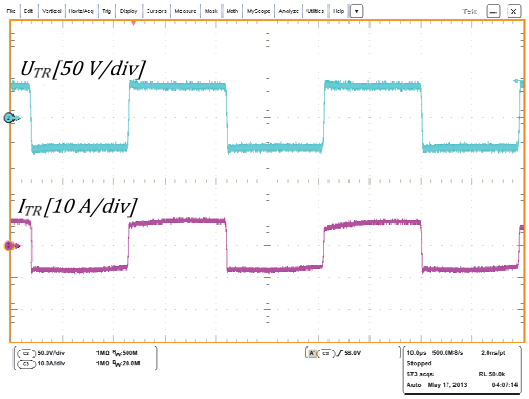
GENERAL OPERATING PARAMETERS, COMPONENT TYPES AND VALUES

Operating parameters	**Value/type**
Nominal input voltage, $U_{1,nom}$	50 V
Minimal input voltage, $U_{1,min}$	25 V
DC-link voltage, U_{DC}	50 V
Output voltage, U_{ld}	550 V
Switching frequency, f_{SW}	23 kHz
Components	
k_{TR}	1:6
L_r	14.5 µH
C_r	3 µF

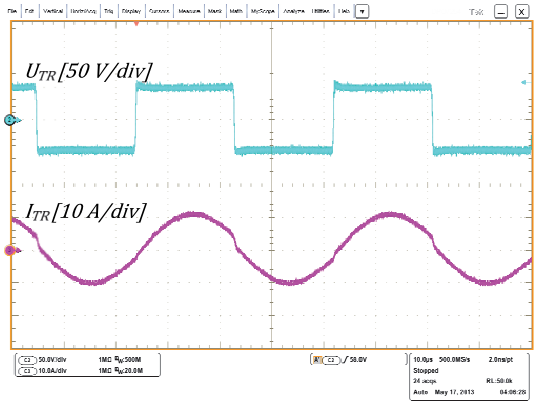
the input voltage is a half of the rated and the maximal shoot-through duty cycle (D_S) of inverter switches should be introduced. The shoot-through state is created by overlapping of active states [15]. The switching conditions of all switches in this case are equal.

A. Experiments with a load power of 300 W

Here we present general waveforms of the converter in light-load operation when the input voltage is at its rated value (50 V).

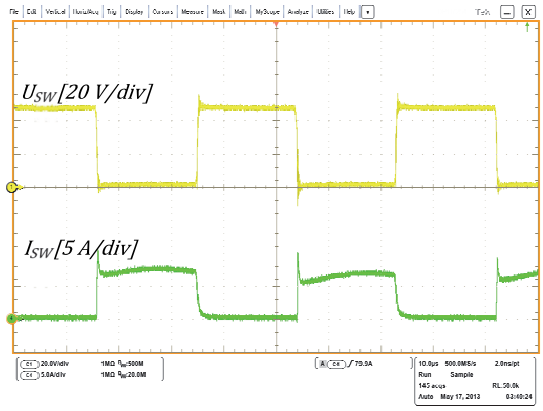


(a)

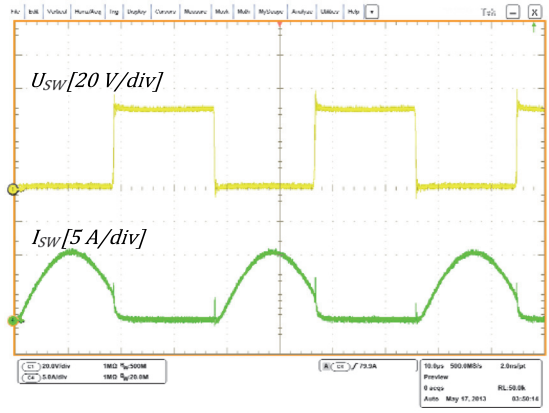


(b)

Fig. 4. Transformer voltage and current of the proposed converter in the normal mode: without the resonant circuit (a) and with the resonant circuit (b).



(a)



(b)

Fig. 5. Voltage and current of one transistor in the normal mode: without the resonant circuit (a) and with the resonant circuit (b).

Fig. 4(a) shows the transformer voltage (U_{TR}) and the current (I_{TR}) without the resonant circuit, but Fig. 4(b) – with the resonant circuit.

As it can be seen, the current form of the transformer is close to a sine wave. In this operation mode the maximal efficiency can be achieved.

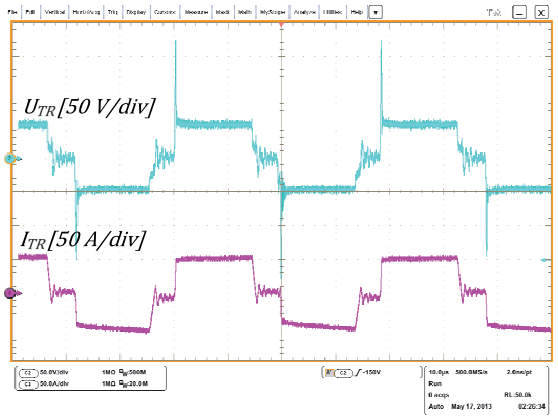
Fig. 5(a) shows the transistor switch voltage (U_{SW}) and the current (I_{SW}) without the resonant circuit, but Fig. 5(b) – with the resonant circuit.

As it can be seen, the resonant circuit can provide turn-on and -off of the switch at almost perfect zero voltage and zero current condition.

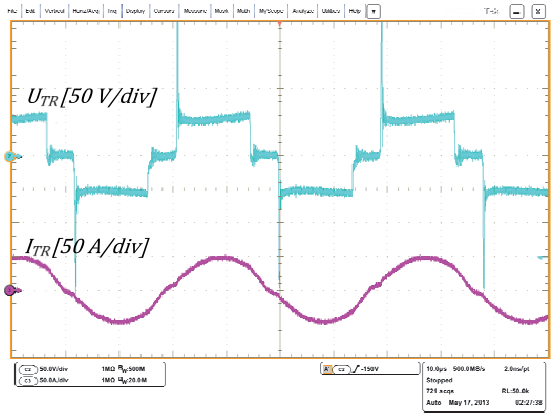
B. Experiments with a load power of 1500W

Fig. 6(a) shows the transformer voltage (U_{TR}) and the current (I_{TR}) without the resonant circuit, but Fig. 6(b) – with the resonant circuit.

As shown, the resonant circuit can reduce transformer voltage oscillations during the shoot-through state of inverter switches. However, voltage spikes are greater with the resonant circuit.

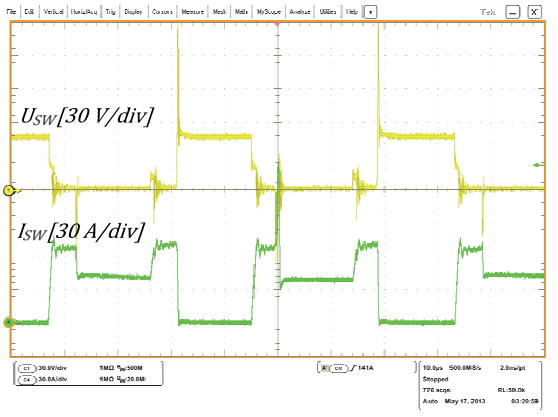


(a)

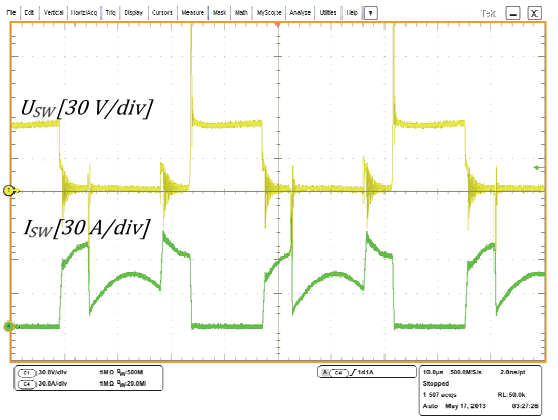


(b)

Fig. 6. Transformer voltage and current of the proposed converter in the boost mode: without the resonant circuit (a) and with the resonant circuit (b).



(a)



(b)

Fig. 7. Voltage and current of one transistor in the boost mode: without the resonant circuit (a) and with the resonant circuit (b).

Fig. 7(a) shows the transistor switch voltage (U_{SW}) and the current (I_{SW}) in the boost operation mode without the resonant circuit, but Fig. 7(b) – with the resonant circuit.

IV. Verification of Theoretical Expressions

A. Normal Mode

The simplified equations obtained can be verified using the results of our experimental investigation, which for the scheme and regime were made at U_I=50V, operation frequency f_{SW}=23 kHz, which corresponds to the applied parameters of the resonant circuit C_r=3 μF, L_r=14.5 μH and different values of the load resistance R_{ld}. Transformer windings ratio is k_{TR}=1/6. Power measurements of the circuit show that an equivalent resistance of the resonant circuit in this case is R_r=0.254 Ω. Fig. 8 presents experimental and calculated characteristics ($U_{ld}=f(R_{ld})$ and $I_I=f(R_{ld})$) depending on the load resistance R_{ld}. As it can be seen, the calculated characteristics almost correspond to those experimentally obtained that confirms the applicability of the simplified expressions obtained. Calculated amplitudes of the current through resonant circuit change from 61.12 A at R_{ld}=140 Ω to 13.38 A at R_{ld}=800 Ω, creating the amplitude of the resonant capacitor voltage respectively from 134.4 V to 29.42 V. Rather high value of the resistance of the resonant circuit caused by the skin effect at a relatively high switching frequency indicates a high power loss in the resonant inductor and causes its heating. To reduce power losses in the resonant inductor L_r it is recommended to pay attention to the cross-section of the conductor in the winding. Also, Litz wire or foil would be more preferable due to the skin effect at high frequencies [15, 16]

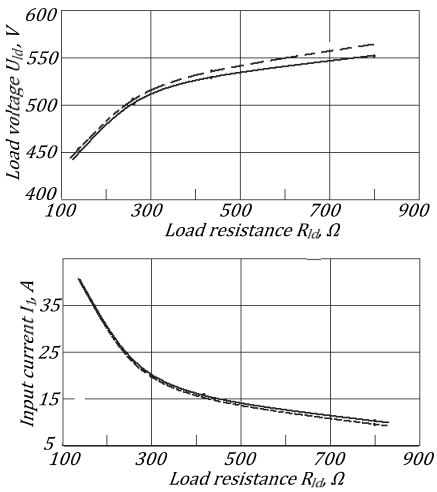


Fig. 8. Experimental and calculated (dashed lines) characteristics showing the dependence of the load voltage U_{ld} and the supply current I_I on the load resistance R_{ld} in the normal mode.

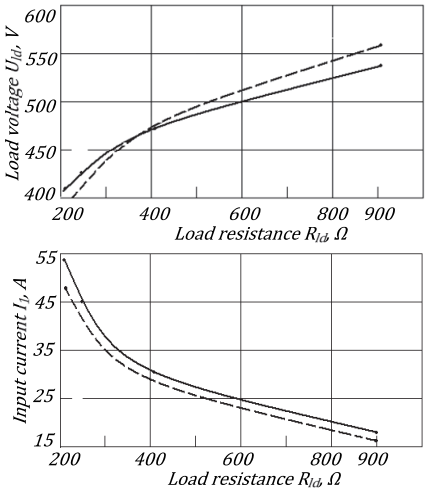


Fig. 9. Experimental and calculated (dashed lines) characteristics showing the dependence of the load voltage U_{ld} and the supply current I_I on the load resistance R_{ld}. in the boost mode.

TABLE II

DYNAMIC POWER LOSSES AT P=300 W

P=300 W, U_{IN}=50V			
With resonant circuit		Without resonant circuit	
P_{ON}, (W)	P_{OFF}, (W)	P_{ON}, (W)	P_{OFF}, (W)
0.07	2.35	0.37	2.2

TABLE III

DYNAMIC POWER LOSSES AT P=1500 W

P=1500 W, U_{IN}=32V			
With resonant circuit		Without resonant circuit	
P_{ON}, (W)	P_{OFF}, (W)	P_{ON}, (W)	P_{OFF}, (W)
0.2	26.7	8.8	42.1

B. Boost Mode

The simplified equations obtained can be verified using the results of our experimental investigation, which for the scheme and boost mode were conducted at U_I=25 V, operation frequency f_{SW}=23 kHz, which complies with the applied parameters of the resonant circuit C_r=3 μF, L_r=14.5μH and different values of the load resistance R_{ld}. Transformer windings ratio k_{TR}=1/6. Power measurements of the circuit show that an equivalent resistance of the qZS-network in this case is R_{qZS}=0.15Ω, but the resistance of the resonant circuit is the same as in the previous case (normal mode), i.e. R_r=0.254 Ω.

In the experiments, the shoot-through duty cycle accepted was D_S=0.27. Fig. 9 presents the experimental and the calculated $U_{ld}=f(R_{ld})$, $I_I=f(R_{ld})$ characteristics.

Fig. 9 shows that the calculated and the experimentally obtained characteristics agree sufficiently well for the accepted application. It means that the obtained expressions can be used for rough engineering calculations. Similarly to the normal operation mode, load voltage is increasing with the rise of load resistance but the input current is decreasing. Also, relations of load voltage and supply voltage in the boost mode and input currents at the respective values of load resistance increase.

V. EVALUATION OF POWER LOSSES IN TRANSISTORS

This section describes the impact of the resonant circuit on dynamic power losses in transistors switches of the inverter bridge (T_1-T_4). Since the commutation processes of all transistors of the inverter bridge are equal, Tables II and Table III show the dynamic power losses only in one transistor. The experimental measurements of power losses in the transistor during turn-on and -off were made with Tektonix DPO 7254 oscilloscope and afterward processed in MS Exel.

It is obvious that the implementation of the resonant circuit reduces dynamic power losses in inverter switches. Tables II and III show that the resonant circuit implemented almost eliminates the switching-on losses of the transistor in both operation modes.

VI. CONCLUSIONS AND FUTURE WORK

This paper has proposed a qZSI based step up resonant DC/DC converter that is very promising in a very wide input voltage or load range. In spite of the additional resonant elements introduced in the transformer circuit the proposed converter performs the voltage step-up and step-down features.

The expressions used allow us to obtain a rough calculation of the converter parameters. Also, theoretical waveforms are in good agreement with those experimentally obtained.

Experimental waveforms show that the introduction of resonant elements in the transformer circuit excludes voltage oscillations in the transformer voltage during the shoot-through state.

The resonant circuit implemented enables us to achieve transistor commutation at almost perfect zero voltage and zero current conditions in the normal mode and reduced dynamic losses in the boost mode. According to Table II and III, the dynamic power losses during the turn-on of the transistor are almost eliminated but during the turn-off of the transistor the losses are reduced up to 40 %. Due to the reduction of dynamic losses it is possible to increase the switching frequency and increase the power density of the converter in the future.

The future work will focus on the reduction of power losses in magnetic components, especially in the resonant circuit of the proposed converter topology.

ACKNOWLEDGMENT

This research work has been supported by Latvian Council of Science (Grant 416/2012).

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[PAPER-III] **Liivik, L.**; Vinnikov, D.; Jalakas, T. Synchronous Rectification in Quasi-Z-Source Converters: Possibilities and Challenges. *IEEE International Conference on Intelligent Energy and Power Systems (IEPS2014)*, June 2-6, 2014, Kyiv, Ukraine, 32 - 35.

2014 IEEE International Conference on Intelligent Energy and Power Systems (IEPS)

Synchronous Rectification in Quasi-Z-Source Converters: Possibilities and Challenges

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***Abstract*— This paper addresses an approach to improve the efficiency of the quasi-Z-source (qZS) converters. By replacing the qZS diode by the n-channel MOSFET, the power loss over a diode can be reduced in a qZS network. The paper presents operation basics of the approach, analysis and comparison of the power losses of the traditional and proposed designs and experimental validation of the theoretical assumptions.**

Keywords—quasi-Z-source network, optimization, efficiency, synchronous rectification, DC-DC converters, DC-AC converters

I. INTRODUCTION

The history of the quasi-Z-source converter (qZSC) family started in 2005, when the quasi-Z-source inverter (qZSI, Fig. 1*a*) was introduced [1]. qZSIs are particularly suitable for applications which require a large range of gain, such as in motor controllers or renewable energy. The distinctive feature of the qZSI is that it can boost the input voltage by utilizing an extra switching state - the shoot-through state. The shoot-though state is the simultaneous conduction of both switches of the same phase leg of the inverter. This operation state is forbidden for the traditional voltage source inverter (VSI) because it causes the short circuit of the dc-link capacitors. In the qZSI, the shoot-through state is used to boost the magnetic energy stored in the dc-side inductors (L_1 and L_2 in Fig. 1*a*) without short-circuiting the dc capacitors C_1 and C_2. This increase in inductive energy, in turn, provides the boost of the output voltage V_{OUT} during the traditional operating states (active states) of the inverter.

Another representative of the qZSC family is the quasi-Z-source (qZS) based isolated DC-DC converter (Fig. 1*b*), which was first introduced in 2009 as a power conditioning system for the renewable energy applications [2]. In general, this new topology was derived from a classical voltage source full-bridge isolated DC-DC converter by adding a qZS network to its input terminals. Thus, the varying output voltage of the renewable energy source is first preregulated by adjusting the shoot- through duty cycle; afterwards, the isolation transformer is being supplied with a voltage of constant amplitude value.

The qZSC family has a common property - the input inductor L_1 that buffers the source current. It means that during the continuous conduction mode (CCM) the input current never drops to zero, thus featuring the reduced stress of the input voltage source. Thanks to that the qZSC is reported as the most promising single-stage boost-buck power conversion approach for different renewable power applications [1]. However, the voltage gain of the qZSC is limited and comparable with the conventional system of a voltage source inverter with the auxiliary step-up DC-DC converter in the input stage [3]. The concept of extending the qZSC gain by the implementation of the cascaded qZS-network and without increasing the number of active switches was studied in [4, 5]. These new converter topologies are known as extended boost (or cascaded) qZSC.

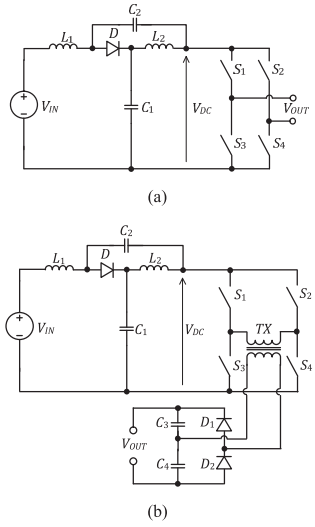

Fig. 1. Main representatives of the qZSC family: qZSI (a) and qZS-based isolated DC-DC converter (b).

Another issue of the qZSC family is the power conversion efficiency at the high input voltage gain due to the power losses in the semiconductors. It was found in [6] that 50% reduction of the forward voltage drop of the qZS diode *D* will follow to the efficiency rise of at least 3% at the twofold input voltage gain.

Focus here is on the possibility of efficiency improvement of the qZSC. The idea is to replace the qZS diode *D* by the n-channel MOSFET to reduce the power loss over a diode in a qZS network.

This research work was co-financed by Estonian Ministry of Education and Research (project SF0140016s11), Estonian Research Council (Grant G8538) and European Social Fund. Latvian partner research work has been supported by Latvian Council of Science (Grant 416/2012)

978-1-4799-2266-6/14/$31.00 ©2014 IEEE

II. Operation Basics of the qZSC

Generally, the qZSC is a combination of a passive qZS-network and an inverter bridge. The qZS-network (Fig. 2*a*) consists of one diode *D*, two identical inductors (L_1 and L_2) and capacitors (C_1 and C_2). To simplify the analysis, the inverter bridge is replaced by the single MOSFET switch S. When *S* is turned on, the shoot-through state occurs and the magnetic energy is stored in the dc side inductors L_1 and L_2 without short-circuiting the dc capacitors C_1 and C_2. During this time interval, the inductor current ramps up (Fig. 2*c*) and V_{OUT} is disconnected from V_{IN}. When *S* is turned off, the active (non-shoot-through) state emerges and previously stored magnetic energy in turn provides the boost of voltage seen on the load terminals.

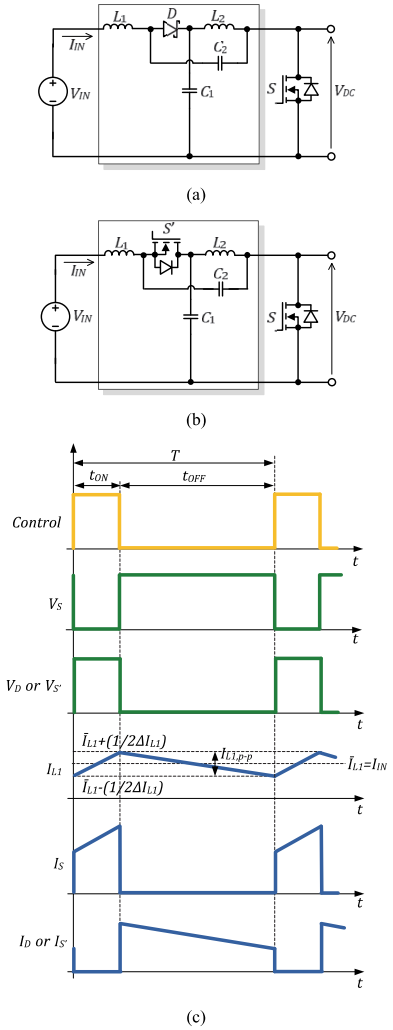

Fig. 2. Traditional (a), synchronous (b) qZS-networks and their idealized voltage and current waveforms (c).

For a synchronous qZS-network (Fig. 2*b*), the MOSFET *S'* is used for the rectifying switch instead of Schottky diode *D* in the traditional (nonsynchronous) topology.

The peak output voltage of both topologies is

$$V_{DC(peak)} = \frac{1}{1-2\cdot D_S}\cdot V_{IN},$$

where D_S is the shoot-through duty cycle:

$$D_S = \frac{t_{ON}}{T},$$

where t_{ON} is the ON-state time of the MOSFET switch *S* and *T* is the switching period.

The operating dc voltages of the capacitors C_1 and C_2 could be estimated as

$$V_{C1} = \frac{1-D_S}{1-2D_S}\cdot V_{IN},\ V_{C2} = \frac{D_S}{1-2D_S}\cdot V_{IN}.$$

Assuming that the capacitances are equal, the capacitance needed to limit the peak to peak DC-link voltage ripple by $r_{V,DC}$ could be calculated as

$$C = \frac{2\cdot P\cdot D_S}{V_{IN}\cdot v_{DC(peak)}\cdot f\cdot r_{V,DC}},$$

where *C* is the capacitance of each capacitor in the qZS-network, *P* is the power rating of the converter, *f* is the switching frequency and $r_{V,DC}$ is the desired peak to peak voltage ripple at the output of the converter.

The main task of the inductors in the qZS-network is to limit the current ripple through the switch during the shoot-through states. Choosing an acceptable peak to peak current ripple r_C the required inductance can be estimated by

$$L = \frac{V_{C1}\cdot D_S\cdot V_{IN}}{P\cdot f\cdot r_C},$$

where *L* is the inductance of each inductor in the qZS-network, V_{C1} is the operating dc voltage of the capacitor C_1 and r_C is the desired peak to peak current ripple through the inductor.

III. Comparative Analysis of Power Losses and Efficiency

To compare the efficiencies of two different approaches, the power dissipation was analyzed by the help of *Thermal Module*, which is an add-on module to the *PSIM software* [7]. In this software the switching and conduction losses of the semiconductor are calculated based on the device datasheet values. In the case of the traditional qZS network, the dual trench MOS barrier Shottky rectifier V60D100C was selected and two diodes were paralleled externally, thus ensuring the smallest possible forward voltage drop. In the synchronous topology the n-channel MOSFET Si4190ADY was implemented to ensure the optimal switching and static properties. The generalized specifications of semiconductors are presented in Table I and the simulation parameters of the circuit were set according to the data presented in Table II. It was assumed that the qZSC is supplied from the photovoltaic

panel, which provides 8.3 A within the range of 15 to 35 V. In order to ensure the demanded output voltage gain (peak output voltage $V_{DC(peak)}$=40 V) within the wide input voltage range, the shoot-through duty cycle was set in accordance with Table III.

The rectifying switch *S'* in the synchronous qZSC is controlled by the inverted control signal of the main switch *S*. Moreover, the special delay (dead time) of 120 ns was added before the turn on of the rectifying switch to avoid both transistors conducting at the same time. If this occurs, the output voltage shorts to ground through both switches, causing high currents that can damage the switches.

TABLE I. SEMICONDUCTOR COMPONENTS SELECTED FOR POWER LOSS ANALYSIS

Component	Type	Specifications
Main switch *S* Synchronous switch *S'*	Vishay Si4190ADY	V_{DS}=100 V; $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, Q_g=20.7 nC, R_g=2.2 Ω
Drivers for *S* and *S'*	Avago ACPL-H312	2.5 A output current gate driver with optocoupler
qZS diode *D*	Vishay V60D100C	V_{RRM}=100 V; V_F=0.66 V $I_{F(AV)}$=2x30 A (common cathode)

TABLE II. SIMULATION PARAMETERS OF THE QZSC

Parameter	Symbol	Value
Input voltage range, V	V_{IN}	15…35
Input current, A	I_{IN}	8.3
Peak output voltage, V	$V_{DC(peak)}$	40
Switching frequency, kHz	f_{sw}	100
Capacitance of qZS capacitors, uF	C_1, C_2	26.4
Inductance of qZS inductors, μH	L_1, L_2	22
Converter power rating, W	P	300

Both approaches were studied at the same operating conditions according to the parameters presented in Table III. The maximum input voltage gain of 2.7 was achieved at the minimum operating voltage (15 V) and power (125 W). At the maximum power point (which corresponds to the maximum input voltage), the shoot-through duty cycle has the minimum value and the resulting voltage gain is near 1.2.

TABLE III. SHOOT-THROUGH DUTY CYCLES FOR ENSURING THE DEMANDED VOLTAGE GAIN AT THE SELECTED TEST POINTS

Test point	1	2	3	4	5
V_{IN}, V	15	20	25	30	35
D_S	0.313	0.25	0.188	0.125	0.63
P, W	125	166	208	249	291

Fig. 3 shows the semiconductor power losses of both designs. It is clear that the synchronous rectification could help to reduce the power losses of the qZS diode by more than 70% in all operating points. Finally, it could result in more than 2% efficiency rise at the operation point corresponding to the smallest power, when the shoot-through duty cycle reaches its maximum (Fig. 4). At the maximum power point, the resulting efficiency rise was near 1.2%.

Next, both designs were studied at the boundary operating points with the maximal and minimal input voltages and in variable load conditions. In the first case (Fig. 5), the qZSCs were tested with the smallest shoot-through duty cycle (Test point 5) and the power was decreased in five steps from 280 to 105 W. The replacement of the qZS diode by the MOSFET in that case provides near 1% efficiency improvement in the whole range of power variation. In the case of smaller powers (up to 120W) and the highest input voltage gain, the synchronous qZSC features 2 to 2.3% efficiency rise (Fig. 6).

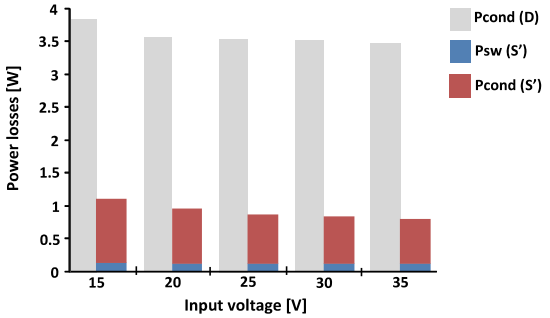

Fig. 3. Comparison of power losses of the qZS diode *D* and synchronous switch (*S'*) at the selected test points.

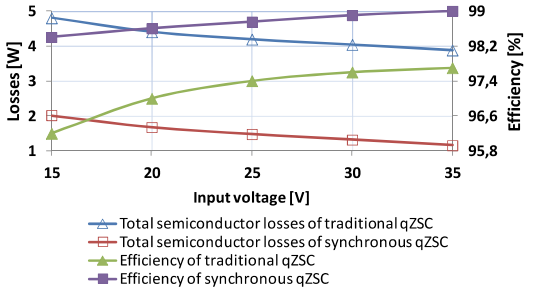

Fig. 4. Comparison of total semiconductor power losses and efficiency of the traditional and synchronous qZSCs at the selected test points.

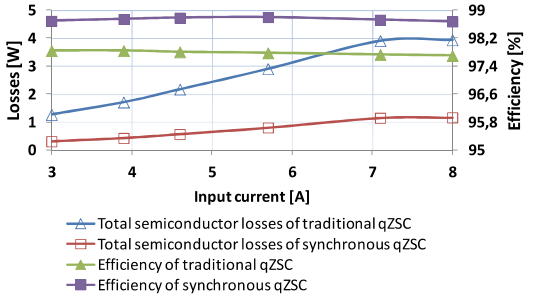

Fig. 5. Comparison of total semiconductor power losses and efficiency of the traditional and synchronous qZSCs at the low input voltage gain.

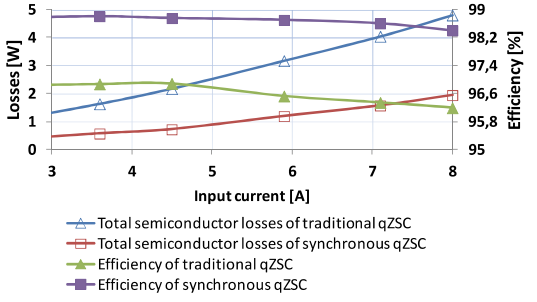

Fig. 6. Comparison of total semiconductor power losses and efficiency of the traditional and synchronous qZSCs at the high input voltage gain.

IV. Experimental Verification

In order to verify our theoretical assumptions, the experimental setup with the power ratio of 300 W (Fig. 7) was assembled in accordance with the schematics shown in Fig. 2 and a series of experiments were carried out. The synchronous switch was placed in parallel with the qZS-diode and both designs were tested in similar conditions. The control of transistors was performed by the arbitrary function generator Tektronix AFG3022B. Measurements were made by the digital oscilloscope Tektronix DPO7254, current probes Tektronix TCP0030, and voltage probes Tektronix P5205A. The results of efficiency measurements are shown in Figs. 8-10.

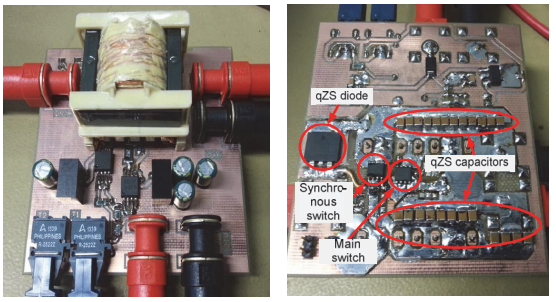

Fig. 7. Top and bottom views of the experimental prototype.

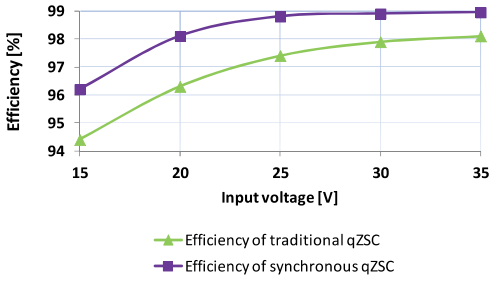

Fig. 8. Measured efficiency of the traditional and synchronous qZSCs at the selected test points.

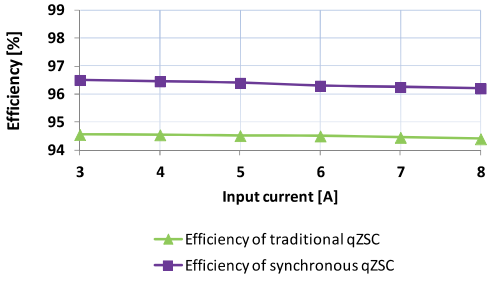

Fig. 9. Comparison of total semiconductor power losses and efficiency of the traditional and synchronous qZSCs at the high input voltage gain.

As it was theoretically predicted, the synchronous qZSC provides an efficiency rise of 2% at the test point with the maximum input voltage gain and the lowest power (Fig. 8). It was also found that the resulting efficiency of both designs in this operating point (Fig. 9) was about 1.5% smaller than that theoretically predicted. The main reason was the unpredicted AC losses in the coupled inductor caused by the high ripple current during the operation with high shoot-through duty cycle values. At the maximum power point and low input voltage gain, the efficiency rise was near 1.2% and the resulting efficiency was close to that theoretically predicted (Fig. 10).

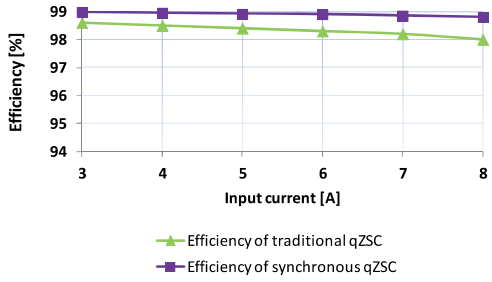

Fig. 10. Measured efficiency of the traditional and synchronous qZSCs at the low input voltage gain.

V. Conclusions

This paper has explored the possibility of replacing the diode by the n-channel MOSFET in order to reduce the power loss over a diode and increase the efficiency of a qZSC. It was found that due to decreased conduction losses the proposed method could result in the efficiency rise by up to 2%. During the design of the synchronous qZSC, special attention should be paid to the selection of proper delay before the turn on of the rectifying switch to avoid both transistors conducting at the same time that can easily destroy the converter.

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[PAPER-IV] **Liivik, L.**; Vinnikov, D.; Zakis, J. Simulation Study of High Step-Up Quasi-Z-Source DC-DC Converter with Synchronous Rectification. *55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, 2014, 34 - 37.

Simulation Study of High Step-Up Quasi-Z-Source DC-DC Converter with Synchronous Rectification

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***Abstract* – This paper discusses the performance improvement method of the recently popular galvanically isolated quasi-Z-source DC-DC converter. In order to decrease the conduction losses in the quasi-Z-source network and voltage doubler rectifier the replacement of diodes by the N-channel MOSFETs was analyzed. The proposed approach was validated by the computer simulations in PSIM environment with accurate models of the semiconductors based on the device datasheet values. Finally, the power losses and resulting efficiency of the proposed quasi-Z-source DC-DC converter with synchronous rectification were compared to those of the traditional topology.**

***Keywords* – DC-DC power converters, Energy efficiency, Pulse width modulation converters.**

I. Introduction

Quasi-Z-Source DC-DC (qZS DC-DC) converter is a new emerged topology from the step-up DC-DC converter family. It could be realized either as the transformerless or the galvanically isolated converter. In the first case the topology is quite similar to the traditional boost converter and can be used as the maximum power point tracker (MPPT) for the photovoltaic (PV) applications [1]. The converter demonstrates high efficiency even at the threefold input voltage gain therefore could be used as the front-end voltage preregulator in the fuel cell power systems of other similar applications with the varying input voltage. The galvanically isolated qZS DC-DC converter has the intermediate AC link with the high frequency transformer [2], which allows setting the desired input voltage gain simply by changing the turns ratio of the transformer. In high gain applications the transformer also plays the role of a galvanic isolation, required in several cases. Furthermore, in the PV power systems the galvanic isolation is essential to reduce ground leakage currents and grid current total harmonic distortion [3].

In [4] the practical realization challenges of the qZS DC-DC converter with galvanic isolation are reported. From one side the topology features such benefits as continuous input current, low start up inrush current, converterless integration of short-term energy storages, soft switching of transistors during active states and the inherent "shoot-circuit immunity" caused by the properties of the qZS-network. From another side, the converter suffers from the lack of efficiency at the high shoot-through duty cycle values, which is mostly caused by the increased power dissipation in the qZS diode D (Fig. 1*a*) [5]. The implementation of module integrated freewheeling diodes as rectifiers described in [6] could also decrease the efficiency and affect the performance of the qZS DC-DC converter, especially in the applications with bidirectional power flow.

This paper discusses the performance improvement method of the recently popular galvanically isolated qZS DC-DC converter by the replacement of all the diodes by the controlled switches (preferably, MOSFETs). The design issues, control principles and analysis of the resulting efficiency rise are reported.

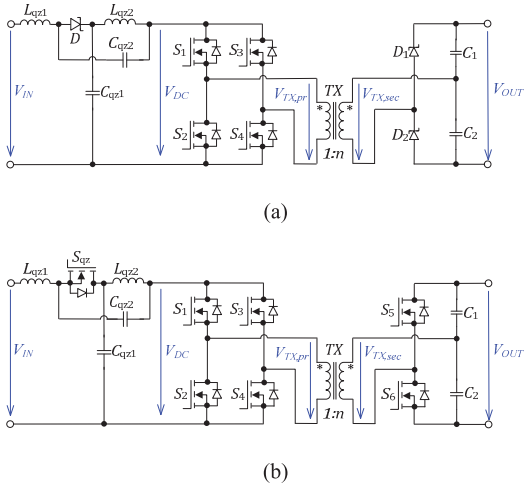

Fig. 1. qZS DC-DC converters with galvanic isolation: traditional (a) and proposed approach, where the diodes are replaced by the N-channel MOSFETs (b).

II. Design and Control Issues

As it was stated before, the diode D is one of the main sources of power dissipation in the traditional qZS DC-DC converter (Fig. 1*a*). This diode is reverse biased during the shoot-through states (Fig. 2*a*) and starts conduction during the active states of the converter (Figs. 2*b* and 2*c*). In the conditions of varying input voltage V_{IN} the output voltage of the qZS DC-DC converter V_{OUT} could be regulated by the variation of the shoot-through duty cycle D_S:

$$V_{OUT} = 2 \cdot V_{IN} \cdot n \cdot \left(\frac{1}{1 - 2 \cdot D_S} \right), \quad (1)$$

where n is the turns ratio of the isolation transformer ($n=V_{TX,sec}/V_{TX,pr}$).

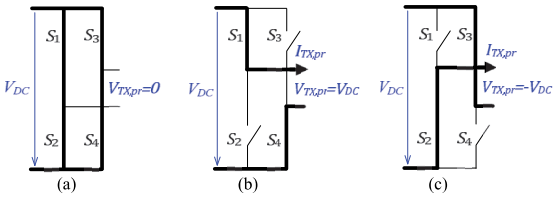

Fig. 2. Main operating states of the front-end inverter: shoot-through (a) and active states (b and c).

The simplest and most efficient method of the shoot-through states generation is the overlap of the active states, shown in Fig. 3 [7]. The duty cycle of active states of transistors is greater than or equal to 0.5. If the duty cycle of active states is greater than 0.5 the cross-conduction of top and bottom transistors (shoot-through) will occur in both inverter legs. During this operating mode the current through inverter switches reaches its maximum, the transformer voltage ($V_{TX,pr}$) drops to zero. From the practical point of view due to the conduction losses in semiconductors it is not advisable to operate at the shoot-through duty cycles higher than 0.33. Basically, the diode D of the qZS-network is only needed to avoid short-circuiting of the capacitors C_{qz1} and C_{qz2} during the shoot-through states. At the same time the diode will noticeably increase conduction losses during the active states. To minimize those losses, the N-channel MOSFET S_{qz} could be placed instead the diode D, as shown in Fig. 1*b*. The basic idea and main challenges of such modification were explained in [8]. In the given application the S_{qz} is synchronized with the inverter switches and it only conducts during the active state and blocks the current during the shoot-through (Table I).

TABLE I

SWITCHING STATES SEQUENCE PER ONE PERIOD (FRONT-END INVERTER AND SYNCHRONOUS QZS-NETWORK)

	Top side		**Bottom side**		**Synchr. switch**
	S_1	S_3	S_2	S_4	S_{qz}
Active state	x			x	x
Shoot-through	x	X	x	x	
Active state		X	x		x
Shoot-through	x	X	x	x	

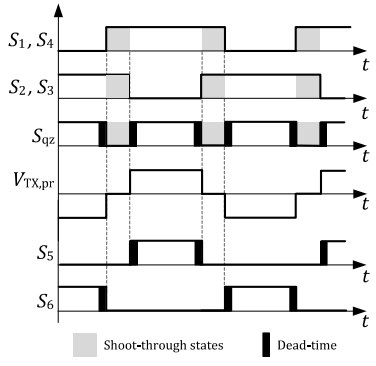

Fig. 3. Proposed control principle of the qZS DC-DC converter with synchronous rectification.

To prevent damage of the circuit, it is advisable to add small dead-time (100 ns…400 ns, depending on the application) before the turn on and off transients of the S_{qz}, as shown in Fig. 3. From the opposite side, it is not recommended to have a dead-time longer than 1 us in order to limit the conduction time of the body diode, and, therefore, to decrease the power losses.

Similarly to qZS-network the conduction losses can be reduced also in the diodes D_1 and D_2 of the voltage doubler rectifier (VDR). Fig. 3 shows the control principle of the synchronized VDR based on the N-channel MOSFETS S_5 and S_6. As it is seen from the diagram the dead-time is also necessary before the turn on and off transients of the S_5 and S_6.

III. COMPARATIVE ANALYSIS OF POWER LOSSES AND EFFICIENCY

To estimate the efficiency rise available from the proposed approach, the power loss analysis was performed in the PSIM simulation environment by using the Thermal Module. In this software the switching and conduction losses of the semiconductor are calculated based on the device datasheet values. For the primary side of the converter the dual trench MOS barrier Shottky rectifier Vishay V60D100C with externally paralleled diodes was compared to synchronous switch realized on an N-channel MOSFET Vishay Si4190ADY. For the secondary side the SiC Shottky rectifiers CREE C3D02060E were compared to the synchronized VDR based on the SiC MOSFETs ROHM SCT2120AF. The generalized specifications of semiconductors are presented in Table II and the simulation parameters of the circuit were set according to the data presented in Table III.

TABLE II

SEMICONDUCTOR COMPONENTS SELECTED FOR THE POWER LOSS ANALYSIS

Component	Type	Specifications
$S_1…S_4$, S_{qz}	Vishay Si4190ADY	V_{DS}=100 V; $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, Q_g=20.7 nC, R_g=2.2 Ω
D	Vishay V60D100C	V_{RRM}=100 V; V_f=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_1, D_2	CREE C3D02060E	V_{RRM}=600 V; V_f=1.8 V $I_{F(AV)}$=4 A
S_5, S_6	ROHM SCT2120AF	V_{DS}=650 V; $R_{DS(on)}$=120 mΩ I_D=29 A, Q_g=61 nC, R_g=2.5 Ω

TABLE III

SIMULATION PARAMETERS OF THE HIGH STEP-UP QZS DC-DC CONVERTER

Parameter	Symbol	Value
Input voltage range, V	V_{IN}	15…30
Maximum input current, A	I_{IN}	10
Peak DC-link voltage, V	$V_{DC(peak)}$	30
Output voltage, V	V_{OUT}	300
Switching frequency, kHz	f_{sw}	100
Operating frequency of qZS-network, kHz	f_{qZS}	200 (2·f_{sw})
Transformer turns ratio	n	5

Capacitance of qZS capacitors, uF	C_{qz1}, C_{qz2}	26.4
Inductance of qZS inductors, µH	L_{qz1}, L_{qz2}	22
Capacitance of output capacitors, uF	C_1, C_2	2.2
Converter power rating, W	P	300

The power losses and efficiency were estimated in four test points with operating conditions described in Table IV. The load resistor R_L was adjusted to achieve the maximum input current in every operating point.

TABLE IV

SHOOT-THROUGH DUTY CYCLE, RESISTANCE OF THE LOAD AND OPERATING POWER IN THE SELECTED TEST POINTS

Test point	1	2	3	4
V_{IN}, V	15	20	25	30
D_S	0.25	0.167	0.083	0
R_L, Ω	600	450	360	300
P, W	150	200	250	300

IV. ANALYSIS OF SIMULATION RESULTS

First, the possible benefits of the synchronous rectification (SR) in the qZS-network were studied. The compared converters had fully identical inverter stages, isolation transformers and VDRs, the difference lied only in the realization of the qZS-networks (diode vs. MOSFET). Fig. 4 shows the comparison of conduction and switching losses of both designs within the studied operating range of the converter. The Shottky diode implemented in the traditional qZS-network features almost zero switching losses, however, its conduction losses are more than twice higher than those of MOSFET in the synchronized qZS-network. Finally, it resulted in more than 1.2% efficiency rise within the whole operating range of the studied DC-DC converter (Fig. 5). The efficiency could be further increased by the implementation of eGaN FETs with ultra-low RDS(ON) (up to 3.2 mΩ, [9]).

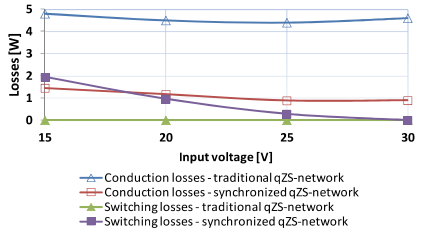

Fig. 4. Semiconductor power losses of the traditional and synchronized qZS-networks in the studied operating range of the converter.

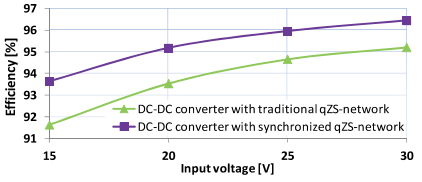

Fig. 5. Efficiency comparison of the qZS DC-DC converter with traditional and synchronized qZS-networks.

In our case study the 200 ns dead-time was implemented before the turn on and off transients of the synchronous switch S_{qz}. Taking into account that the qZS-network operates with twice switching frequency of the converter the selected dead-time formed 4% of the operating period of the synchronous switch. In order to understand the influence of the dead-time on the efficiency of the DC-DC converter a series of simulations was performed. The dead-time was changed with the variable steps from 200 ns to 2 us. It is seen from Fig. 6 that threefold increase of the dead-time will result in almost 1% of the efficiency drop at the minimum input voltage, when the shoot-through duty cycle reaches its maximum. If the dead-time will be increased to 2 us the benefits of SR will be almost cancelled since the resulting efficiency will be quite close to that of the DC-DC converter with traditional qZS-network.

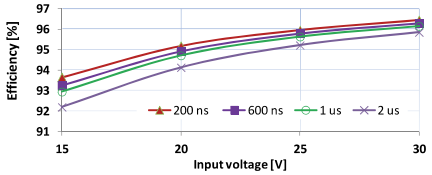

Fig. 6. Influence of the dead-time on the efficiency of the qZS DC-DC converter with synchronized qZS-network.

Next, the possible benefits of the SR in the VDR were analyzed. The compared converters had fully identical inverter stages and diode based qZS-network explained before but this time the difference lied in the realization of the VDR (diode vs. MOSFET). Fig. 7 shows the comparison of conduction and switching losses of both discussed designs within the studied operating range of the converter. Typically, application of the VDR in the galvanically isolated DC-DC converters is associated with the soft switching of semiconductors used in it, therefore, both approaches demonstrate near zero switching losses.

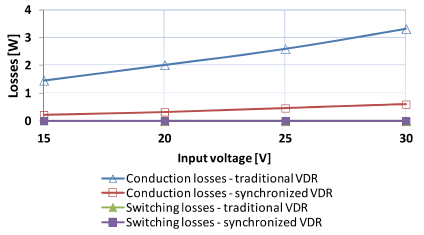

Fig. 7. Semiconductor power losses of the traditional and synchronized VDR in the studied operating range of the converter.

In the studied VDR, conduction losses of the N-channel SiC MOSFET operated with 200 ns dead-time were more than 5 times smaller than those of SiC diode, which resulted in about 1% higher efficiency of the topology with synchronized VDR.

Finally, it was found that the implementation of SR in the high step-up qZS DC-DC converter could provide the overall efficiency improvement of the converter from 2% to 3%, depending on the operation point (Fig. 9).

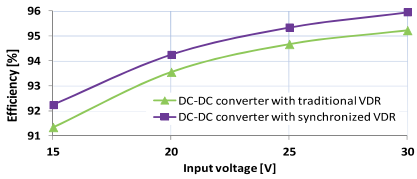

Fig. 8. Efficiency comparison of the qZS DC-DC converter with traditional and synchronized VDRs.

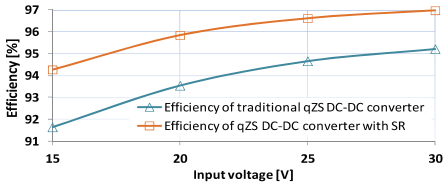

Fig. 9. Overall efficiency rise of the step-up qZS DC-DC converter resulted by the implementation of the synchronized qZS-network and VDR.

V. Conclusions

In this paper the benefits of synchronous rectification in the high step-up qZS DC-DC converter were analyzed. It was shown that due to decreased conduction losses the replacement of diodes by the N-channel MOSFETS in the qZS-network and voltage doubler rectifier could result in the efficiency rise by more than 2% within the whole operation range of the converter. In order to maximize the efficiency, special attention should be paid to the proper selection of the dead-time before the turn on and off transients of the synchronous switches to limit the conduction of body diode.

Recent efforts of the research group are directed toward the development of the experimental setup of the step-up qZS DC-DC converter with synchronous rectification. This test bench will be used for validation of the proposed ideas as well as for the study of implementation possibilities of GaN MOSFETs for further efficiency improvement of the converter.

Acknowledgements

This research work was co-financed by Estonian Ministry of Education and Research (project SF0140016s11), Estonian Research Council (Grant G8538) and European Social Fund. Latvian partner research work has been supported by Latvian Council of Science (Grant 416/2012).

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[PAPER-V] Chub, A.; **Liivik, L.**; Vinnikov, D. Impedance-Source Galvanically Isolated DC/DC Converters: State of the Art and Future Challenges. *IEEE 55th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, 2014, 67 - 74.

Impedance-Source Galvanically Isolated DC/DC Converters: State of the Art and Future Challenges

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Abstract **– Impedance-source switched mode converters are an emerging technology in electric energy conversion. They overcome limitations of conventional solutions by the utilization of specific impedance-source networks. Previous review papers cover impedance-source networks. Focus of this paper is on the topologies of the impedance-source galvanically isolated DC/DC converter. These converters are particularly appropriate for distributed generation systems with renewable or alternative energy sources which require input voltage regulation in a wide range. This paper presents a concise review of basic existing topologies for researchers and engineers. All the reviewed topologies of the impedance-source galvanically isolated DC/DC converter are classified by the element that transfers energy from the input to the output: a transformer or a coupled inductor. This classification undoubtedly reveals wide space for further research and the most promising research directions in this field.**

Keywords **– DC/DC power converters, galvanic isolation, impedance-source converters, renewable energy sources.**

I. Introduction

Power electronics could be considered as a key technology in the renewable and alternative energy generation, modern energy storage systems, sustainable transportation, adjustable-speed drives, etc. Photovoltaic, wind and fuel cell energy applications have high capacity of power electronics converters [1]. Generation of the renewable energy has highly dispersed nature. PV systems are the most challenging application because only micro-converters can efficiently utilize generated power from the PV panels [2]. In this case, isolated DC/DC converters are used to couple PV panels with the common DC bus of the power harvesting system.

Research in the field of impedance-source (IS) converters has been initiated by the invention of the Z-source (ZS) inverter that is based on the ZS network [3]. ZS inverters (ZSIs) are able to provide buck-boost behavior in the single-stage and improved reliability due to the inherent shoot-circuit immunity. These advantages urge active research in the field of impedance-source inverters (ISIs). Recent ten years have seen a growing number of studies published in this area. IS technology was applied to all four basic converter types (DC/DC, AC/AC, etc.). Application field of IS converters is very broad. It varies from modern energy generation systems (renewable and alternative) to DC circuit breakers and electronic loads [4]. Impedance-source network is a key element of any converter in this group. It consists of inductors, capacitors and diodes (or switches). Any basic IS network could be represented as a two-port network. In general, IS converters are derived from the current-source or the voltage-source converters. Utilization of IS network (ISN) allows improved reliability, DC voltage (or current) gain, and provides immunity to shoot-through and open states. A number of novel ISN have been proposed to improve performance, cost and reliability of IS converters [4].

Wide penetration of energy sources with low output voltage, like PV panels or fuel cells, has stimulated rapid research into isolated step-up DC/DC converters with wide input voltage variations. They are intended for the integration of low voltage energy sources to the common DC link with much higher operating voltage. In this case a magnetic element is used not only for galvanic isolation; it also defines the DC gain range. Input voltage variations can be compensated at the controlled step-up stage inside the converter. DC gain of this step-up stage is usually within the range of 1:3. This approach keeps the efficiency of the controlled step-up stage in an acceptable range, while a major voltage step-up occurs at the isolation magnetic element with high efficiency.

IS galvanically isolated DC/DC converters were reported as a suitable solution for the interfacing of the low voltage renewable or alternative energy sources as well as for the battery storage applications [4],[5]. They have improved voltage step-up capabilities and reliability. The first IS based galvanically isolated DC/DC converter was derived from the three-phase ZSI by adding a three-phase transformer, a rectifier and a filter, as shown in Fig. 1. The three-phase intermediate high frequency AC-link is useful for high power applications, and it facilitates thermal design. This converter was intended for the grid integration of low-voltage high-current fuel cells.

Basic ISN structures have been comprehensively reviewed in [4]. The aim of this paper is to review all known basic IS galvanically isolated DC/DC converters, as some of them were not included in the classification proposed in [4]. The classification proposed has several hierarchical levels and is intended to show possible research directions. Also, the most promising future research trends in this field are indicated.

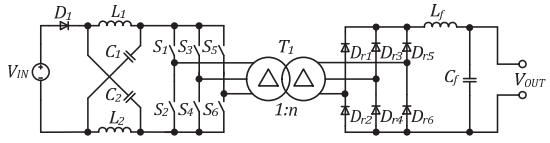

Fig. 1. ZSI based three-phase isolated DC/DC converter.

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State-of-the-art IS galvanically isolated DC/DC converter topologies could be classified into two main groups by means of the component which transfers energy from the input to the output side:

- transformer based
- coupled inductor based

II. Transformer Based IS Galvanically Isolated DC/DC Converters

This class of converters contains topologies that use a transformer for galvanic isolation and energy transfer. They can be divided into three groups:

- with three-phase full bridge switching stage
- with single-phase full bridge switching stage
- with push-pull switching stage

The first two categories could be merged into one with the full bridge switching stage.

A. Converters with Full Bridge Switching Stage

A generalized functional scheme for this group is shown in Fig. 2a. The input part of the converter between the input terminals and the transformer is the basic structure of the IS inverter. It could have either one or three-phases. These DC/DC converters consist of an IS inverter, a transformer, a rectifier and a filter. Here the shoot-through states when one or all legs of the inverter are short-circuited are used for the voltage step-up. The turns ratio n of the isolation transformer defines the range of the DC voltage gain. In this case the IS network serves for adjusting of the voltage across the transformer windings when the input voltage varies.

Z-source

ZS based converters utilize the ZS network that consists of two capacitors C_1, C_2, two inductors L_1, L_2, and diode D_1, as shown in Fig. 1. The converter shown in the same figure is the historically first in this group. It is based on the ZSI. This converter has inherited from the ZSI advantages, like buck-boost regulation and improved reliability, and drawbacks, like high components stress and discontinuous input current. The discontinuous input current substantially limits application possibilities and performance of this converter. For example, it can be used with renewable energy sources, but it requires an additional filter at the input, which increases the system cost,

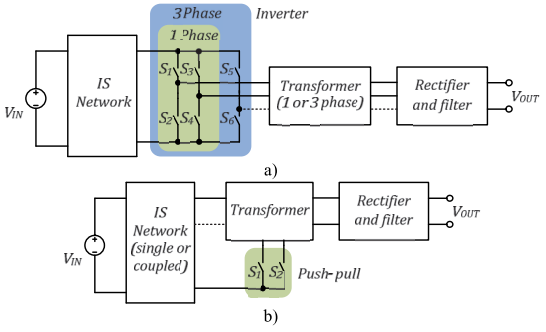

Fig. 2. Generalized functional schemes of transformer based isolated IS DC/DC converters with: a) full bridge and b) push-pull switching stage.

volume and failure rate. Also, bi-directional operation is possible if this converter is implemented in a symmetrical configuration [7]. But it still has all the drawbacks of the ZSI, and the application range of such solution is uncertain. The single-phase version of the converter is analyzed in [8], and with the distributed Z-source network in [9].

The ZS based converter with a single-phase full bridge switching stage can easily utilize series resonant (SR) circuit in series with a transformer [10]. Leakage inductance of the transformer could serve as a part of resonance circuit, thus improving power density. In this case SR converter has a narrow regulation range in the frequency domain and improved buck-boost features.

Quasi-Z-source

The quasi-Z-source (qZS) inverter family was proposed in [11]. The qZS inverter (qZSI) has inherited all the advantages of the ZSI, but it has lower component stress and continuous input current. The single-phase and the three-phase qZSI based converter have been proposed in [12]. Single-phase implementation is shown in Fig. 3. The qZS network contains the coupled inductor T_{qZ}, capacitors C_1, C_2. Implementation of the qZS network with the single coupled inductor is advisable to improve power density. Advantages inherited from the qZSI make this converter a superior solution for the modern distributed energy generation systems. Additional benefit is gained with the use of the voltage doubler rectifier (VDR) based on diodes D_{r1}, D_{r2} and capacitors C_{f1}, C_{f2}. The use of the VDR is advisable for any converter in the transformer based group. It enables the use of the transformer with reduced turns ratio n, which leads to lower transformer parasitic elements. It has proven performance for the fuel cells and permanent magnet synchronous generator (PMSG) based wind turbines [13], [14]. Three-phase implementation is recommended for high power applications.

The qZSI based DC/DC converter has received much attention of researchers because of numerous advantages of the qZS network in power conversion. Several topological variations have been derived in order to further improve this topology. SR version of this converter is proposed in [10] and discussed in [15]. It requires additional research on control issues and detailed design guidelines. Also, the possible range of soft switching should be analyzed.

Another attempt to improve the qZSI based topology is employing the cascaded qZS network. An inverter with the cascaded qZS network has been proposed in [16] to further improve the step-up performance. Diode assisted and capacitor assisted families of cascaded qZSI topologies have been analyzed. Capacitor assisted topologies have better voltage step-up performance and less semiconductor elements

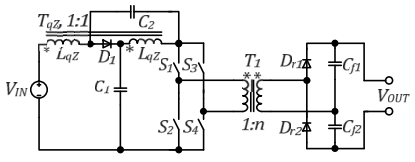

Fig. 3. QZSI based isolated DC/DC converter.

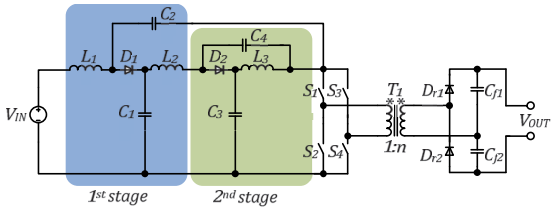

Fig. 4. Capacitor assisted two-stage qZSI based isolated DC/DC converter.

than those of diode assisted. That is why the capacitor assisted extended boost (CAEB) topology was applied to the qZSI based DC/DC converter in [17]. This topology with two qZS stages is shown in Fig. 4. Cascaded two-stage implementation of the qZS network contains two times more components and can provide higher step-up than the qZSI based converter with the same shoot-through duty cycle. Such solution was proposed for the sake of better transformer utilization, to narrow shoot-through duty cycle regulation range. In practice, additional components bring in losses and additional volume that cannot be compensated by the improvements of the transformer operation mode. The cascaded converter cannot overcome the simple qZSI based converter by total performance mostly due to the increased losses.

Among these two topologies derived from the basic qZSI based one, the topology with SR seems more promising.

The review of the ISNs proposed in [4] shows that only some IS networks can provide continuous input current, which is needed in most of the modern power electronics applications for distributed generation. The qZS network has a superior region of continuous input current. There are several Z-source based IS networks that have inside coupled inductors (with non-unity turns ratio) which influence the DC gain factor by their turns ratio m, for example: Γ-Z-source [18], trans-Z-source [19] and Y-source [20]. They usually have discontinuous input current. Such converters have better step-up possibilities than the conventional ZS or qZS. In the case of the transformer based isolated DC/DC converters, these networks allow DC voltage gain to be distributed between the transformer (defined by n) and the coupled inductor (defined by m). This leads to distributed parasitic elements and better switching performance.

Trans-Z-source

Trans-Z-source based isolated DC/DC converter family was proposed in [21]. It consists of the trans-Z-source (TZS) single-phase inverter based converter and the trans-quasi-Z-source (TqZS) single-phase inverter based converter. They are shown in Fig. 5. Three-phase implementation could be easily derived from a single-phase. In these converters DC voltage gain of TZS or TqZS networks depends not only on the shoot-through duty cycle, but also on the turns ration of the coupled inductor m. The IS network contains less passive elements: one capacitor C_1, coupled inductor T_1, and diode D_1. Both converters have discontinuous input current. Experimental verification has shown that the TqZS inverter based converter has lower start-up current than that of the TZS inverter based. In the future, it is required to derive the application range and detailed design guidelines.

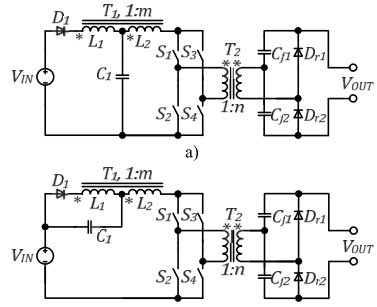

Fig. 5. IS isolated DC/DC converters: a) trans-Z-source inverter based and b) trans-quasi-Z-source inverter based.

B. Converters with Push-Pull Switching Stage

A generalized functional scheme for this group is shown in Fig. 2b. In comparison with full bridge based converters, this group has several advantages: lower number of switches, simpler control, lower conduction losses in low input voltage applications. Usually the switches work interleaved to improve the input current ripple.

Quasi-Z-source

The quasi-Z-source-fed push-pull converter family has been proposed recently [23]. It is derived from the current-fed push-pull converter family by replacing the input inductor with the qZS network. Such family could be derived for almost any ISN, but almost none of them have continuous input current. The family proposed in [23] includes the quasi-Z-source-fed push-pull converter (qZSFPPC) and the interleaved quasi-Z-source-fed push-pull converter (IqZSFPPC), as shown in Fig. 6. They have fewer switches than IS inverter based converters.

The QZSFPPC employs a simple qZS network. It has the operation principle quite similar to that of the qZSI based converter. The IqZSFPPC contains a magnetically coupled qZS network which could be represented as two qZS networks with full magnetic coupling in the coupled inductor T_{qZ}. In this converter, leakage inductances of the coupled inductor define the input current ripple, while magnetizing inductance defines the current ripple in the windings. This dependence leads to complicated design of the magnetic component for the IqZSFPPC. The control principle of these converters is very similar to the reference current fed push-pull converter family except the duty cycle regulation range, because of improved voltage step-up performance.

The leakage inductances are not taken into account in [23]. This means that in practice these converters will utilize active or passive clamping at the input side. Nevertheless, these converters are recommended for low input voltage and high input current applications, because only one power switch is in the input current loop. This can ensure lower conductance losses. The interleaved converter from this family has more passive elements, but they are rated for lower current or voltage stress. Therefore, the final power density of both converters could be close.

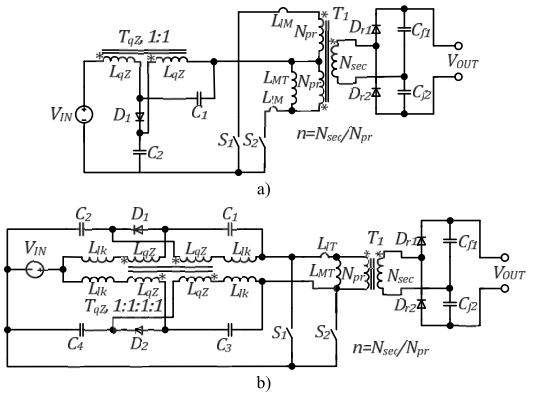

Fig. 6. Quasi-Z-source-fed push-pull converter family: a) quasi-Z-source-fed push-pull converter and b) interleaved quasi-Z-source-fed push-pull converter.

Y-source

Recently several new IS converters have been proposed with the use of the novel Y-source (YS) network [4]. One of them that belongs to the group of transformer based isolated DC/DC converters with the push-pull switching stage is shown in Fig. 7. The YS network consists of the capacitor C_1, the coupled inductor T_Y, and the diode D_1. That network is regarded under the group of IS networks with coupled inductors. In this case the coupled inductor T_Y has three windings giving some level of freedom during the design of this converter, because the characteristic value m depends non-linearly on the number of turns of each winding. This value defines the step-up characteristic of the YS network. Also, the proposed inverter utilizes the Greinacher VDR, while the bridge VDR is the most commonly used and has slightly better efficiency [5].

According to reports available, the performance of the YS network converter is close to that of the trans-Z-source network. However, it suffers from voltage overshoots caused by the leakage inductances of the coupled inductor due to discontinuous input current [22], like any other IS network with a coupled inductor. Moreover, the three-winding coupled inductor is more complicated to design than the two-winding inductor used in the TZS or TqZS networks. Comprehensive studies of the closed loop control of the YS based converters and their application possibilities are required. The YS and some other IS networks with coupled inductors (TqZS, Γ-Z-source, etc.) have to be compared through analysis and experiments to evaluate practical application possibilities and overall performance of the YS network based converters.

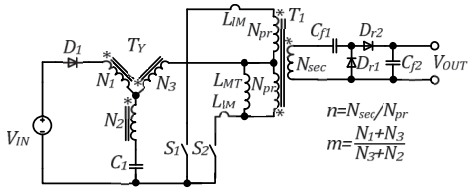

Fig. 7. Y-source push-pull converter.

III. Coupled Inductor Based IS Galvanically Isolated DC/DC Converters

This class of converters contains topologies that use a coupled inductor as a part of the IS network, as well as for galvanic isolation and energy transfer from the input side to the output side. Those converters are not as numerous as the previous one. The first converter appeared in the literature at the beginning of 2012 [24]. During the last three years several new converters have been proposed. They could be divided into two main groups:

- with push-pull switching stage
- with single switch

A. Converters with Push-Pull Switching Stage

This group consists of two push-pull based converters that could be organized into one family based on the commonly used qZS network. A generalized functional scheme for this group is shown in Fig. 8a.

Quasi-Z-source

The quasi-Z-source derived push-pull DC/DC converter with two coupled inductors has been proposed in [24] and analyzed in [25]. It consists of two quasi-Z-source networks C_1, C_2, T_1, D_1 and C_3, C_4, T_2, D_2, as shown in Fig. 9a. Three-winding coupled inductors T_1 and T_2 provide galvanic isolation and store energy in the form of equivalent magnetizing current (i.e. flux through the core of the coupled inductors). The turn-on state of the transistors corresponds to the shoot-through behavior of the IS inverter. This converter shows good performance in wind power applications due to its wide feasible input voltage regulation range. It could be considered as two single-switch converters connected in parallel at the input and in series at the output, where they are sharing a common output rectifier and a filter. At low step-up this converter transfers energy in the narrow pulses with high current amplitude, which is the main drawback that limits the practical regulation range. Flat efficiency curve at high switching frequency could be achieved in all-SiC implementations [26].

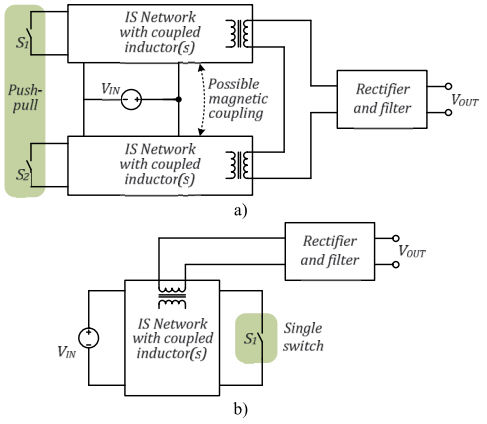

Fig. 8. Generalized functional schemes of coupled inductor based isolated IS DC/DC converters with: a) push-pull switching stage and b) single-switch.

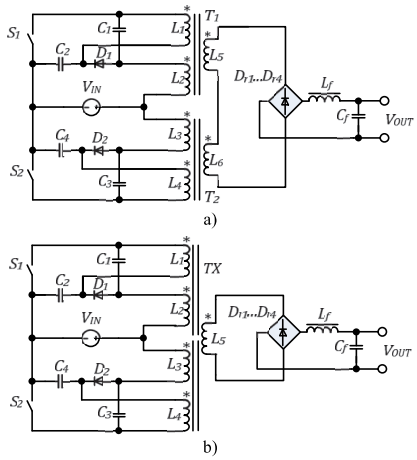

Fig. 9. Quasi-Z-source derived push-pull DC/DC converter with: a) two coupled inductors, and b) a single coupled inductor.

Further improvement in the group of push-pull based converters is possible through magnetic coupling of qZS networks [24]. Coupling between T_1 and T_2 should not be full, because it leads to self-compensation of windings, and such converter is not feasible. Partial coupling is a good option that leads to single coupled inductor implementation of the push-pull based topology. The quasi-Z-source derived push-pull DC/DC converter with a single coupled inductor is shown in Fig. 9b. This topology proposed in [24] looks promising, but there is no research on the design of the coupled inductor *TX* along with full design guidelines.

Both converters use a bridge diode rectifier with a conventional LC filter at the output. These topologies require careful design to avoid high voltage oscillation over the rectifier diodes and tertiary windings of coupled inductors during the freewheeling state, when voltages across L_5, L_6 compensate each other.

B. Converters with Single Switch

This group contains three recently proposed converters based on typical qZS and ZS networks. A generalized functional scheme for this group is shown in Fig. 8b.

Quasi-Z-source

Quasi-Z-source based single-switch converter with two inductors has been proposed in [27]. In the qZS network the second inductor is replaced with the coupled inductor T_1, as shown in Fig. 10a. Magnetizing inductance reflected to the primary winding serves as part of the qZS network along with L_{IN} to store energy. Inductor T_1 also provides galvanic isolation and energy transfer to the output. The output part contains the switched capacitor cell D_{SC1}, D_{SC2}, C_{SC1}, C_{SC2} for additional voltage step-up and the rectifier D_r with the filter capacitor C_f. The output side utilizes leakage inductance of the coupled inductor as a part of the rectifier that limits the current ripple. The main advantage is that the output current ripple is reflected to the qZS network, but does not influence the input current with low ripple. On the other hand, such implementations require two magnetic components.

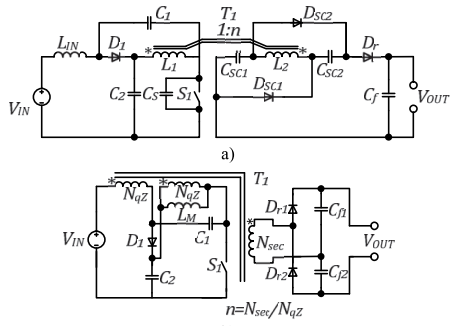

Fig. 10. Single-switch isolated qZS DC/DC converters with: a) two inductors and b) one inductor.

Another single-switch qZS based DC/DC converter shown in Fig. 10b has been derived from the quasi-Z-source push-pull DC/DC converter (Fig. 9a) [5], [29]. It contains only one magnetic component. In contrast to the previous qZS converter, this converter has continuous input current with higher ripple, because the reflected output current ripple is shared between the primary windings. It also utilizes the bridge VDR, which provides continuous output capacitor current (only one of them charges simultaneously) and low component count. Here the slight drawback with higher input current ripple can be neglected when the converter operates at a high step-up and couples low and high voltage sides. This converter shows good performance in the wide input voltage range [29].

Z-source

Finally, another converter in this group is derived in the same manner as the qZS based single-switch converter with a single coupled inductor [28]. Both inductors of the single-switch ZS isolated DC/DC converter are coupled to maintain symmetrical structure of this network, as shown in Fig. 11. In contrast to the conventional ZS network, this current in ZS inductors has higher ripples due to the reflection of the output current to the input side. Leakage inductance of secondary windings serves as a filter in the output side. Input current is discontinuous. As compared to single-switch qZS converters, this converter has higher stress of elements. This topology can be improved by magnetic coupling of coupled inductors T_1 and T_2. Full coupling seems to be the best choice. In this case the ZS network would be based on the three-winding coupled inductor that carries two times higher flux. Feasibility of such system needs to be investigated with the VDR, which also seems to be a superior solution for the IS isolated DC/DC converters.

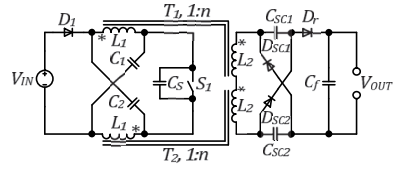

Fig. 11. Single-switch isolated ZS DC/DC converter.

Coupled inductor based converters are more complicated to design as compared to transformer based converters. They have shown good performance in wind energy applications where the input voltage varies most of all. This class of converters contains several topologies. Many novel topologies could be derived with other IS networks that have not been applied yet.

IV. Classification of IS Galvanically Isolated DC/DC Converters

All the reviewed topologies could be considered as basic. Many other converters could be derived from them by parallel connection of basic topologies without magnetic coupling [30], or with magnetic coupling between IS networks [30], [31]. These basic topologies could be used in different parallel-series energy conversion systems [29], [32]. Implementation of the secondary side with active switches allows bi-directional operation of basic topologies [7], [33].

To clarify the converter derivation process and show the potential white spots in this field, a classification was made. The first level in the classification is based on the energy transfer principle: energy could be transferred from the input to the output side through either a transformer or a coupled inductor. The next level of classification is based on the implementation of the switching stage. The third level of classification shows which IS networks have been applied to the basic structures shown in Figs. 2 and 8. The fourth level is used to indicate topological variations of the basic principle defined by the first three levels.

The proposed classification is shown in Fig. 12. The first two levels define only five basic principles. Only one or two IS networks have been applied to four of them. This offers further research space for applications of other IS networks.

Converters based on the single-phase qZSI have been studied most extensively. This group has the widest topological variations. The single-phase IS inverter based group contains more topologies than other groups. It is because this derivation principle is natural and the simplest, therefore numerous IS inverters have been comprehensively investigated. Many results could be reused in the DC/DC converters design.

The proposed classification shows wide possibilities of research on new IS isolated DC/DC converter topologies on the third and fourth level of the classification. The studies will focus on the utilization of IS networks and their topological variations.

Moreover, an extension of the classification at the first and second levels is possible. Recently numerous topologies with combined energy transfer using transformers and coupled inductors have been proposed. Novel class of IS isolated DC/DC converters with combined energy transfer would also utilize this principle. Second classification level also shows possibilities for extension. The most obvious is application of the half-bridge switching stage in the transformer based topologies.

Therefore it could be concluded that the proposed classification is versatile and could be used as a basis for future derivation and systematization of novel galvanically isolated IS DC/DC converters.

V. Future Research Challenges

Modern renewable energy market requires versatile power electronics solutions. The review of the converters above reveals that the qZSI based isolated DC/DC converter could be chosen for further development as the basic power electronics building module for dispersed generation systems. Coupled inductor based topologies are more complicated to design and control and less effective, but they show better performance where wide regulation is needed. They are required only in some applications with wide input voltage variations, for instance, in PMSG based wind turbines.

Several steps have already been made towards improvement of this converter. A shift to resonant bridge with series resonant circuit which utilizes leakage inductance of the transformer was proposed. This allows considerable reduction of the losses and switching frequency rise, leading to volume reduction. Additional research is needed towards new control strategies and design guidelines derivation.

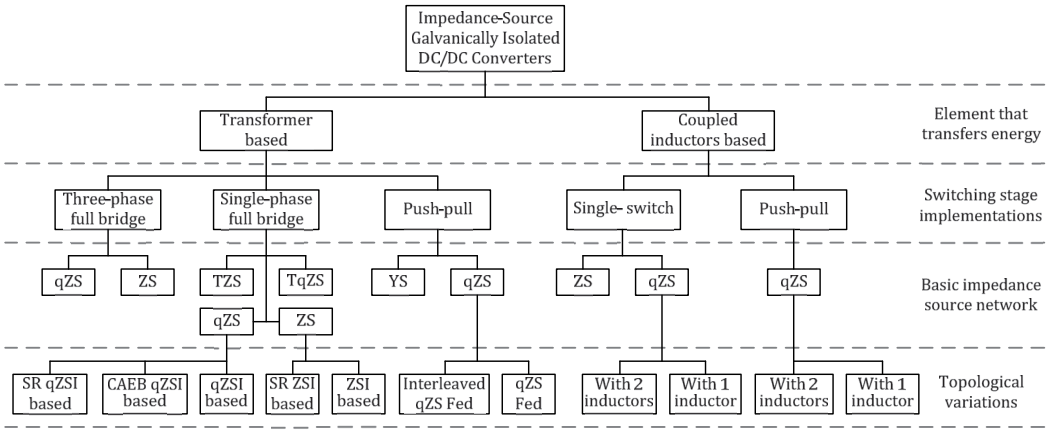

Fig. 12. Classification of the impedance-source galvanically isolated DC/DC converters.

Another possibility is synchronous rectification in the IS network. Preliminary results reported in [34] show reduction in the losses in the qZS network with the implementation of the MOSFET instead of the qZS diode. It allows an efficiency rise by 2 % within the qZS network. Active rectification is also possible at the VDR side. If all semiconductor components within the converter are active (e.g., MOSFETs), not only rise of the efficiency in the VDR and IS stages, but also controllable bi-directional operation can be achieved [33].

Utilization of new materials is the most popular recent trend in the modern power electronics industry. New magnetic materials can reduce the size of the implemented ISN. Also, the utilization of the new wide-bandgap semiconductors, like SiC and GaN, allows further loss reduction along with the switching frequency rise. GaN MOSFETs have shown good performance at the low voltage side in the PV micro-converters. Modern SiC MOSFETS could be used in the active VDR on the high voltage side. Appropriate selection of new wide-bandgap transistors and analysis of achieved benefits along with economic concerns require additional research and development of new design guidelines.

Utilization of all major trends towards improvement of the qZSI based DC/DC converter leads to the topology shown in Fig. 13. This topology could show superior results in modern power electronics applications, like renewable and alternative energy, battery storages, etc. Currently available transistors are recommended for the all-GaN implementation of the primary low voltage side: switches S_{qZ}, $S_1 \ldots S_4$. High voltage SiC MOSFETs are recommended to be used at the output side: transistors S_5, S_6. In future they could be replaced with high voltage GaN transistors. Technology of the GaN high voltage transistors is immature still, only one supplier has started selling (Transphorm), and another is starting in October 2014 (GaN Systems). Active secondary side provides bi-directional energy transfer possibilities. It will require a complicated control system.

The proposed qZSI based fully active DC/DC topology raises numerous scientific and practical challenges. Further research in this direction is advisable. Eventually it should lead to highly efficient, versatile universal DC/DC converter with bi-directional power transfer possibility. It would be totally based on the GaN technology when we have appropriate components off the shelf.

VI. Conclusions

Existing isolated impedance-source DC/DC converters were reviewed. Derived classification shows numerous white spots in this field. Converters from the transformer based class are simpler to design, more flexible, and have a wider application range. Coupled inductor based converters perform well in certain applications with wide input voltage variations. Numerous topics for further research have been indicated in this article. Four generalized functional proposed schemes could be used to understand the derivation process of the IS isolated DC/DC converter topologies. Practicing engineers may find this article a concise review of the field with a short reference list, sufficient to be introduced into this technology.

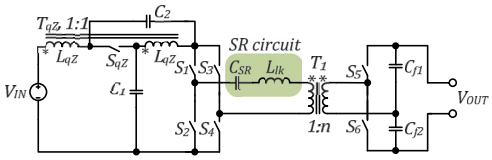

Fig. 13. QZSI based SR DC/DC converter with active secondary half-bridge.

The quasi-Z-source inverter based converter is the most advantageous among other topologies. Further directions to improvements of that converter were discussed. Main directions from future research are series resonant implementations, active rectification in the input and the output sides, bi-directional operation, and implementation of new materials and semiconductors.

Acknowledgement

This research work was financed by Estonian Ministry of Education and Research (project SF0140016s11), Estonian Research Council (Grant G8538) and European Social Fund (Project Doctoral School of Energy and Geotechnology II).

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[PAPER-VI] Roasto, I.; **Liivik, L.**; Vinnikov, D. Control of Quazi Z-source DC-DC Converter by the Overlap of Active States: New Possibilities and Limitations. *14th Biennial Baltic Electronics Conference*, Tallinn, Estonia, October 6-8, 2014, 217 - 220.

Control of Quasi-Z-Source dc-dc Converter by the Overlap of Active States: New Possibilities and Limitations

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***Abstract*—previous studies have clearly shown that shoot-through generation by the overlap of active states has better operating parameters than other shoot-through generation methods. However, due to some disadvantages, this method has never been studied in detail. This paper is filling the gap by examining the shoot-through generation method by the overlap of active states. The disadvantages are explained and solutions are proposed. Moreover, a novel shifted overlap shoot-through modulation method is proposed and compared with the known symmetrical overlap method. Theoretical analysis is verified by the experiments on a real test prototype.**

Keywords— qZS inverter; shoot-through; dc-dc converter; overlap; modulation methods;

I. Introduction

Typically, quasi-Z-source (qZS) inverter has been used as a sine wave inverter for AC loads [1]-[3]. The dc-link voltage is controlled by the special shoot-through state, which can be generated by three different ways in one phase system: shoot-through via any one bridge leg, and via both two bridge legs [4]. The Shoot-through is usually generated within a zero vector. This method allows achieving soft switching without additional components, which increases efficiency of the converter. Several new PWM control methods such as shifted shoot-through control and swapped PWM control have been proposed recently, which allow to improve the performance even more [5].

However, previous studies have clearly shown that shoot-through generation by the overlap of active states has better operating parameters than other shoot-through generation methods. The switching frequencies of transistors are the smallest and are equally distributed between all switches. The overvoltages have moderate values compared to the other methods [6]. However, the method utilizes active states overlapping to generate the shoot-through states, which inherently connects shoot-through (D_S) and active state (D_A) duty cycles such that they cannot be changed separately and D_A directly depends on D_S. It could be a drawback in some applications e.g. in isolated dc-dc converters, where the transformer has been optimized to work in one operating point i.e. with fixed active state duty cycle. This is only true in the case of relative small switching frequencies, where the transformer losses are dominating. Also this method cannot be used in the qZS inverters where the active state duty cycle is modulated to form sinusoidal output voltage. As mentioned above, qZS based sine wave inverter has been the major application and thus, the shoot-through generation by the overlap of active states has not really been in research focus.

Today the trend is to increase switching frequency as much as possible that results in reduced magnetic component size and increased energy density. In the high frequency (>50 kHz) isolated qZS dc-dc converters the transformer losses are negligible compared to switching losses. Thus, in such applications the total efficiency of the converter is more depending on the chosen modulation algorithm than optimal utilization of magnetic components. Therefore, the shoot-through generation by the overlap of active states is an attractive control method that needs to be studied more detailed.

In this paper a novel overlap method (shifted overlap) is proposed and investigated. The new method is compared with the classical overlap method, which is called as symmetrical overlap method. The common feature of these methods is the shoot-through state generated by the overlap of active states i.e. without zero states. Due to this feature soft switching without additional components can be achieved. Only two switching states (active and shoot-through) also make the generation of control signals easier, which means that less expensive control units can be used. Considering conduction losses, all shoot-through modulation methods are similar. The biggest difference comes from switching losses. Thus, the main focus of this paper was also laid on switching losses.

The control methods where investigated both theoretically and experimentally. The experiments were conducted on a 2 kW demonstrator based on the qZS dc-dc converter topology (Fig. 1). It consists of the qZS-network, an inverter, an isolation transformer, a voltage doubler rectifier (VDR) and a resistive load. VDR eliminates the dependency between the

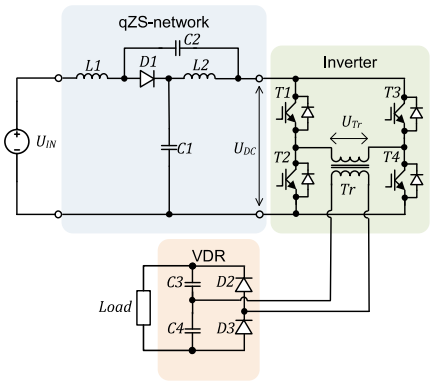


Fig. 1. Isolated qZS dc-dc converter.

output voltage and the active state duty cycle of the transformer. Thus, the shoot-through method by the overlap of active states can be used without any disturbing effects on the output voltage.

II. Shoot-through Generation by the Overlap of Active States

A. *Symmetrical overlap method*

Typically the shoot-through is achieved by increasing the duty cycle of active states over 0.5. This causes the active states of bottom (*T2, T4*) and top (*T1, T3*) side transistors to overlap with each other symmetrically (Fig. 1). As a result, the shoot-through state occurs, as shown in Fig. 2.

During shoot-through mode all four transistors of the qZS inverter are conducting and the current through inverter switches reaches its maximum, the transformer voltage (U_{Tr}) drops to zero (Fig. 2).

The operating period of the isolation transformer in this control method consists of a shoot-through state t_S and an active state t_A:

$$T = t_A + t_S . \quad (1)$$

The (2) could also be represented as

$$\frac{t_A}{T} + \frac{t_S}{T} = D_A + D_S = 1 , \quad (2)$$

where D_A and D_S are the duty cycles of active and shoot-through states, correspondingly. From Eq. (2) results that the duty cycle of the active state is directly connected to the duration of the shoot-through state. Thus, it approaches its maximum (0.5) in the non-shoot-through mode. And vice versa, when the shoot-through duty cycle is maximal, the duty cycle of active states will have a minimum value. The theoretical limit for shoot-through duty cycle is 0.5. From practical point of view due to the losses shoot-through duty cycles longer than 0.3 are not advisable.

The number of switching states per period of top and bottom transistors is equal (Table 1) i.e. the transistors operate with the same frequency. The states are shown for one period of the isolation transformer. The conducting switches are indicated by 'x'. Equal frequency results in equalized switching losses in all transistors. Moreover, compared to the other shoot-through modulation methods, the switching frequency of transistors is lower, which results in better efficiency.

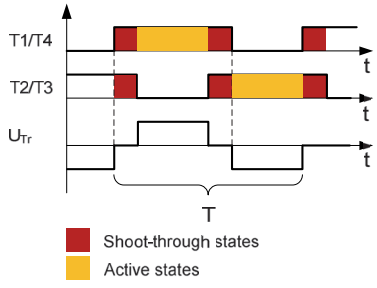


Fig. 2. Symmetrical overlap method where shoot-through is created by the active state duty cycle greater than 0.5.

TABLE 1 SWITCHING STATES SEQUENCE PER ONE PERIOD. SHOOT-THROUGH GENERATION BY THE OVERLAP OF ACTIVE STATES

	Top side		Bottom side	
	T1	*T3*	*T2*	*T4*
Active state		x	x	
Shoot-through	x	x	x	x
Active state	x			x
Shoot-through	x	x	x	x

B. *Shifted overlap method*

In this paper a novel shoot-through generation method is proposed. According to the symmetrical overlap principle, the shoot-through states are generated by increasing the duty cycle of active states. The idea of the proposed new method is to create shoot-through by shifting the active states towards each other while keeping the duty cycle constant 0.5. The new method will be named as shifted overlap.

In Fig. 3 the shoot-through generation principle by the shifted overlap is shown. Two complementary signal pairs *T1/T3* and *T2/T4* are generated. The shoot-through duration can be changed by changing the phase shift ($\Delta\Phi$) between complementary transistor pairs, as shown in Fig. 4.

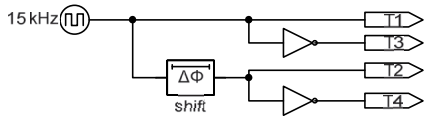


Fig. 3. Shoot-through generation principle in the shifted overlap method.

In Table 2 the states are shown for one period of the transformer. The conducting switches are indicated by 'x'. Unlike the symmetrical overlap method, where shoot-through is generated by simultaneously switching on four switches in the case of shifted overlap method only two switches at the time are conducting, as shown in Fig. 4. Since, the conducting transistor pairs are alternating twice in each period, they can be considered as equally loaded. The switching frequency of bottom and top transistors is equal, as indicated in Table 2.

TABLE 2. SEQUENCE OF SWITCHING STATES PER ONE PERIOD. SHOOT-THROUGH GENERATION BY THE SHIFT OF ACTIVE STATES

	Top side		Bottom side	
	T1	*T3*	*T2*	*T4*
Active state		x	x	
Shoot-through		x		x
Active state	x			x
Shoot-through	x		x	

III. Experimental verification

To verify the presented theoretical assumptions an experimental setup of the qZS inverter-based single-phase dc-dc converter was developed and tested. The operating parameters are presented in Table 3. For both control algorithms investigated the input voltage of the converter was set as U_{IN} = 30 V, the output voltage U_{OUT} = 600 V and the input power P_{IN} = 1000 W. The qZS-network boosts the input voltage to the desired value U_{DC} = 60 V. The isolation transformer operates with the frequency 15 kHz. Since there are two shoot-through states per period, the frequency of the qZS-network is twice higher i.e. 30 kHz.

TABLE 3. DESIRED OPERATING PARAMETERS OF THE CONVERTER.

Parameter	Value
Input voltage, U_{IN}	30 V
dc-link voltage amplitude, U_{DC}	60 V
Desired output voltage of the converter, U_{OUT}	600 V
Input power P_{IN}	1 kW
Operating frequency of qZS-network, f_{qZS}	30 kHz
Operating frequency of isolation transformer, f_{TR}	15 kHz

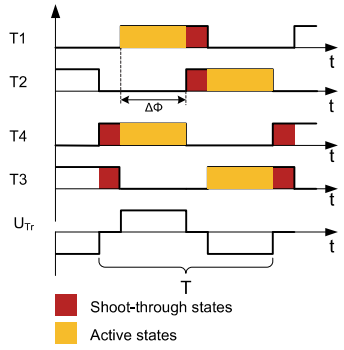


Fig. 4. Shifted overlap method where shoot-through is created via phase shift $\Delta\Phi$.

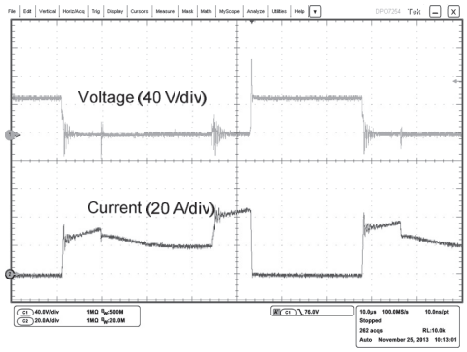


Fig. 5. Shoot-through by the symmetrical overlap of active states. Voltage and current of the transistors *T1...T4*.

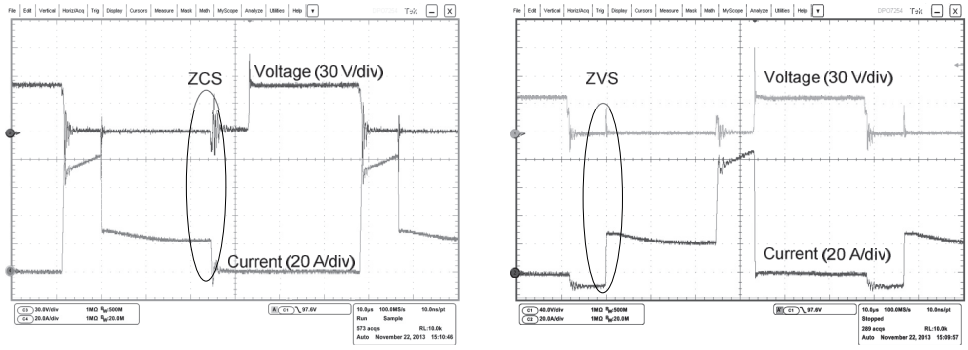
The collector-emitter voltages and collector currents of transistors T1 and T4 were measured. In the case of the symmetrical overlap method, all transistors have identical switching pattern and equal switching frequency, as shown in Fig. 5. Thus, the switching losses are also equally distributed between transistors. Each transistor is set into shoot-through state twice per period.

In Fig. 6 current and voltage of the transistors *T1* and *T4* in the case of shifted overlap is shown. The shoot-through is generated alternately by transistor pairs *T1/T2* and *T3/T4*. Unlike in symmetrical overlap method, each transistor is set into shoot-through only once per period. This allows achieving additional soft switching states, as indicated in Fig. 6. In the top side transistors (*T1, T3*) zero current switching (ZCS) is achieved and in the bottom side transistors (*T2, T4*) zero voltage switching (ZVS) is achieved.

To compare both methods the total switching losses were calculated based on measured waveforms. In Table 4 the results are shown. Turn on and turn off losses of a top side and a bottom side transistor are estimated. Also total losses per pair (*T1/T4*) and of all four transistors (*T1…T4*) are calculated. In the case of symmetrical overlap method all transistors have both: turn on and turn off losses. The total switching loss is about 37 W. Additional soft switching occurs in the shifted shoot-through method resulting in zero turn on losses in bottom side transistors and zero turn off losses in top side transistors, as indicated in **Error! Reference source not found.**. However, since only two transistors are conducting in the shoot-through state, the current is twice bigger compared

TABLE 4. COMPARISON OF SWITCHING LOSSES OF THE SYMMETRICAL AND SHIFTED OVERLAP SHOOT-THROUGH GENERATION METHODS

	Losses during switching transients [W]				Total T1/T4 [W]	Total T1…T4 [W]
	Turn on		Turn off			
	T1	*T4*	*T1*	*T4*		
Symmetrical overlap	3.1	3.1	6.1	6.1	18.4	36.8
Shifted overlap	11.4	0	0	16.4	27.8	55.6



(a) (b)

Fig. 6. Collector-emitter voltage and collector current of the top side transistor *T1* (a) and bottom side transistor *T4* (b).

to the symmetrical overlap method. This leads to higher turn on and turn off losses. The total switching loss is about 56 W, which is 1.5 times more than in the case of symmetrical overlap method. In terms of operating power (1 kW) the switching losses constitute 3.7 % and 5.6 % accordingly.

In conclusion, the symmetrical overlap method has lower switching losses and about 3 % higher efficiency. However, experiments showed more voltage and -current spikes than in the case of shifted overlap method. This is probably related to the fact that in the shifted overlap method the shoot-through is generated only by two transistors and there is no current imbalance between phase-legs. Thus, this method could be implementable in the EMI sensitive equipment.

IV. Conclusions

This paper proposed a novel shifted overlap shoot-through generation method and compared it with the known symmetrical overlap method. The common feature of these methods is the shoot-through generated by the overlap of active states i.e. without zero states. Due to this feature soft switching without additional components can be achieved. In general, the shoot-through generation by the overlap of active states has proven to be the most efficient shoot-through control method.

The main difference between both methods is that in the case of shifted overlap, the shoot-through is generated only by two transistors. Due to that additional soft switching states can be achieved. It was experimentally proven that the additional soft switching states did not reduce total switching losses as expected. On the contrary, due to the higher shoot-through current in the shifted overlap method the switching losses were increase 1.5 times. Thus, the symmetrical overlap method has lower switching losses and about 3 % higher efficiency. However, the shifted overlap method did show more stable behavior with respect to voltage and current spikes. Thus, the shifted shoot-through method might have some advantages in the EMI susceptible devices. This is still to be studied in the future.

Acknowledgment

This research was supported by Estonian Ministry of Education and Research (Project SF0140016s11) and Estonian Science Foundation (Grant ETF8687). Latvian partner research work has been supported by Latvian Council of Science (Grant 416/2012).

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[PAPER-VII] Vinnikov, D.; Roasto, I.; **Liivik, L.;** Blinov, A. Four Novel PWM Shoot-Through Control Methods for Impedance Source DC-DC Converters. *Journal of Power Electronics*, 2015, 15(2), 299 - 308.

JPE 15-2-1

http://dx.doi.org/10.6113/JPE.2015.15.2.299
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Four Novel PWM Shoot-Through Control Methods for Impedance Source DC-DC Converters

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Abstract

This study proposes four novel pulse width modulation (PWM) shoot-through control methods for impedance source (IS) galvanically isolated DC-DC converters. These methods are derived from a PWM control method with shifted shoot-through introduced by the authors in 2012. In contrast to the baseline solution, where the shoot-through states are generated by the simultaneous conduction of all transistors in the inverter bridge, our new approach is based on the shoot-through generation by one inverter leg. The idea is to increase the number of soft-switched transients and, therefore, decrease the dynamic losses of the front-end inverter. All the proposed approaches are experimentally verified through an insulated-gate bipolar transistor-based IS DC-DC converter. Conclusions are drawn in accordance with the results of the switching loss analysis.

Key words: DC-DC power converters, Pulse width modulation converters, Pulse width modulation, Quasi-Z-source inverter, Shoot-through control methods, Switching losses, Zero current switching, Zero voltage switching

I. INTRODUCTION

Impedance source (IS) DC-DC converter (IS DC-DC) is a new type of step-up galvanically isolated DC-DC converter first introduced in [1] as a power conditioning system for renewable energy applications. The new topology is generally derived from a classical voltage source full-bridge isolated DC-DC converter [2] by adding a passive impedance network to its input terminals (Fig. 1). The impedance network is a two-port passive circuit that consists of capacitors, inductors, and diodes in a special configuration. The specific feature of the impedance network is that it can be short-circuited, which, in turn, will increase the voltage across the input terminals of the main converter (V_{DC} in Fig. 1) [3].

Given that IS DC-DC is a step-up converter, its operation is always connected to a low voltage and high current values at the input side, which can lead to high losses at the front-end inverter. The shoot-through switching states used for the stepping up of the input voltage are also associated with certain power dissipation. Therefore, special attention must be paid to the reduction in losses both in wiring and in the semiconductors of the primary (low-voltage) part of the converter. One of the benefits offered by IS DC-DC is the inherent soft-switching achieved by proper control methods [4]. The number of soft-switching transients depends on the selected modulation method. Both zero current switching (ZCS) and zero voltage switching (ZVS) can be achieved within a wide operation range [4].

This paper describes the results of the comparative study on the novel pulse width modulation (PWM) shoot-through control methods proposed by the authors for the family of IS DC-DC converters. The purpose is to minimize the switching losses of the front-end inverter.

II. IS DC-DC CONVERTERS: OPERATING PRINCIPLE, REALIZATION POSSIBILITIES, AND BASIC CONTROL METHODS

A. Operating Principle

In the family of IS galvanically isolated DC-DC converters, quasi-Z-source converter (qZSC) is the most advantageous [Fig. 2(a)]. The impedance network of qZSC consists of two capacitors, two inductors, and one diode, all of which are connected in a specific configuration [outlined by the gray color in Fig. 2(a)]. The quasi-Z-source network was derived

Manuscript received Jun. 12, 2014; accepted Oct. 4, 2014
Recommended for publication by Associate Editor Honnyong Cha.
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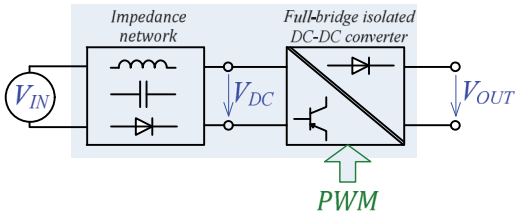

Fig. 1. Generalized block diagram of the IS galvanically isolated DC-DC converter.

from the baseline Z-source network [3] simply by changing the position of the input voltage source. Thanks to the presence of the input inductor L_{qz1}, the qZSC features continuous input current, which is especially important in renewable energy applications. Owing to the absence of a current path at start-up, qZSC has the feature of inrush-current limitation in contrast to Z-source-derived topologies. Other advantages of qZSC include the possibility of converterless integration of short-term energy storages (batteries) [5], bidirectional operation capability [6], and inherent short-circuit protection.

Regarding its operation principle, qZSC is similar to the galvanically isolated current-fed full-bridge boost converter [CFFBBC, Fig. 2(b)], which also uses shoot-through switching states for the stepping up of the input voltage [7]. In contrast to qZSC, CFFBBC has the disadvantage of inductive overvoltage across the inverter bridge, which leads to additional clamping circuits to be applied [8], [9]. Another issue of CFFBBC, the inrush current during start-up at a low output voltage, requires auxiliary start-up circuits to be implemented [10]. As a result, the introduction of these necessary sub-circuits increases the complexity of CFFBBC and can seriously affect its efficiency.

In both topologies, the peak voltage across the inverter bridge (V_{DC}) depends on the shoot-through duty cycle D_{ST}, that is,

$$D_{ST} = \frac{t_{ST}}{T}, \tag{1}$$

where t_{ST} is the cross conduction time of the switches in the inverter bridge, and T is the switching period. The idealized voltage boost across the inverter bridge in qZSC is

$$B_{qZSC} = \frac{V_{DC(peak)}}{V_{IN}} = \frac{1}{1-2\cdot D_{ST}}. \tag{2}$$

In the case of CFFBBC, the idealized voltage boost is

$$B_{\mathrm{CFFBBC}} = \frac{V_{DC(peak)}}{V_{IN}} = \frac{1}{1-D_{ST}}. \tag{3}$$

A comparison of idealized voltage boost properties shows that qZSC features a higher voltage step-up capability for the same shoot-through duty cycle D_{ST} than CFFBBC (Fig. 3). The twofold input voltage gain, typical for the power conditioners for renewable energy sources, can be obtained by D_{ST} of 0.25 and 0.5 for qZSC and CFFBBC respectively.

Given that the duty cycles of the shoot-through and active states are interdependent in both topologies ($D_A = 1 - D_{ST}$), this will result in a higher root mean square current through the primary switches of CFFBBC for the same operating conditions.

qZSC is theoretically possible to operate with shoot-through duty cycles up to 0.5. A high D_{ST} will lead to instabilities in the system. In practical applications at high step-up ratios, shoot-through duty cycles higher than 0.33 are not commonly recommended because they will lead to high conduction losses and a dramatic decrease in efficiency.

B. Realization Possibilities

IS converters have been actively studied during the last decade, and a number of new configurations of impedance networks have been proposed [3], [11]-[17]. All of them can be used to construct IS DC-DC converters. In several cases, the cascaded configurations of impedance networks and switched inductor or switched capacitor concepts can be used to increase converter performance [18]-[21]. An up-to-date comparative analysis of recently proposed impedance networks can be found in [22].

In galvanically isolated step-up DC-DC converters, a voltage-doubler rectifier (VDR) is the most efficient and simplest approach to obtain the highest possible voltage gain. The bridge VDR shown in Fig. 2 consists of two diodes (*D1* and *D2*) and two output capacitors (*C1* and *C2*). With the output capacitors connected in series, the output voltage V_{OUT} at every time instant will be the sum of the two capacitor voltages or twice the peak voltage ($V_{TX,sec}$) of the secondary winding of the isolation transformer. VDR can also be realized according to Greinacher topology, in which only one capacitor directly supplies the output load, and the second one serves as an intermediate energy storage element [23].

Recent research in the field of IS DC-DC converters focuses on the improvement of power conversion efficiency. In this context, methods such as resonant power conversion and synchronous rectification can significantly enhance the performance of IS DC-DC converters. The first series resonant IS DC-DC converter was proposed in [24]. Owing to the implemented series resonant LC circuit, a qZS-based DC-DC converter can be soft-switched in all operating points, except for minor power dissipation at the turn-off transients of the shoot-through states [25].

Another issue of IS DC-DC converters is the power conversion efficiency at high shoot-through duty cycle values because of the conduction losses in the diode D_{qz} of IS network. The diode D_{qz} is basically only needed to avoid short-circuiting the capacitors C_{qz1} and C_{qz2} during the shoot-through states. At the same time, the diode will noticeably increase conduction losses during the active states. To minimize such losses, N-channel metal-oxide-semiconductor field-effect transistor (MOSFET)

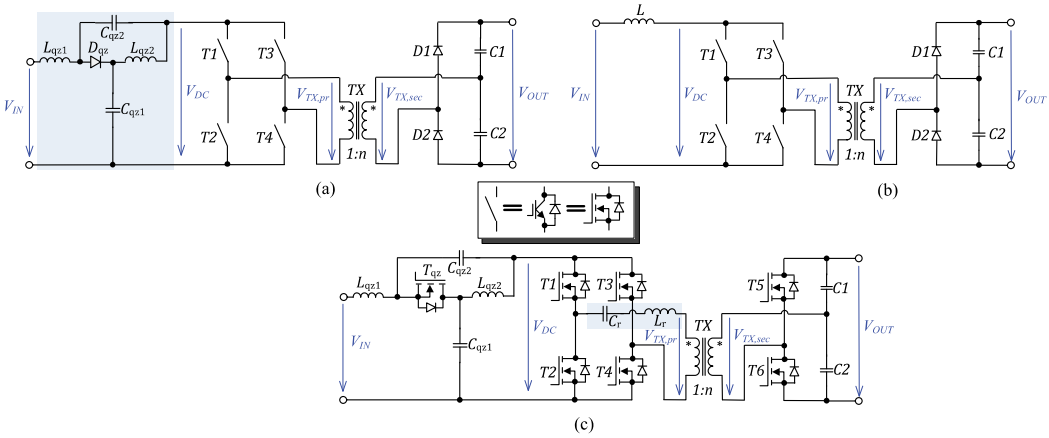

Fig. 2. Generalized topologies of the step-up galvanically isolated DC-DC converters. (a) qZSC, (b) CFFBBC. (c) High-performance qZSC with resonant power conversion and synchronous rectification.

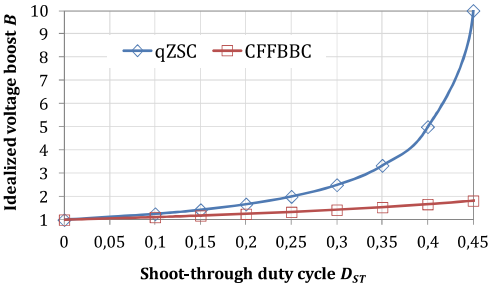

Fig. 3. Idealized voltage boost factor B as a function of the shoot-through duty cycle D_{ST} for qZSC and CFFBBC.

can be replaced by D_{qz} [26]. T_{qz} is synchronized with the inverter switches, and it only conducts during the active state and blocks the current during shoot-through.

Similar to the IS network, conduction losses can also be reduced in the diodes *D1* and *D2* of VDR. The implementation of transistors instead of diodes in VDR will result in the bidirectional operation capability of IS DC-DC converter. In consideration of all the mentioned modification possibilities, an example of a high-performance qZSC is presented in Fig. 2(c).

C. Basic Control Principles

In [27] and [28], two basic shoot-through control methods for IS DC-DC converters were proposed, namely, PWM and phase shift modulation (PSM). Shoot-through states [Fig. 4(a)] are typically generated within zero states [Figs. 4(d) and (e)], wherein the zero and shoot-through states are equally distributed over the switching period, so that the number of high harmonics in the transformer primary can be reduced. To minimize switch losses, the number of shoot-through states per period is limited to two.

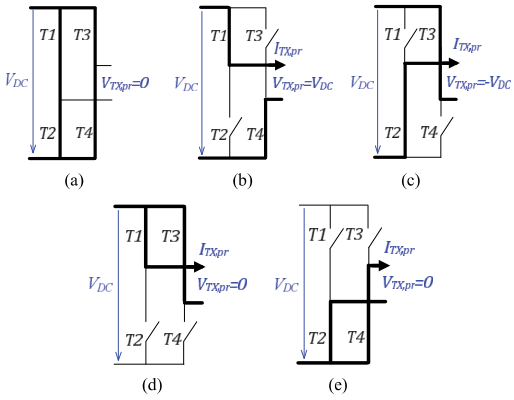

Fig. 4. Main operating states of the front-end inverter in qZSC: (a) Shoot-through state. (b), (c) Active states. (d), (e) Zero states.

Shoot-through current is also evenly distributed between both inverter legs by switching on all four transistors.

In consideration of conduction losses, both shoot-through control methods (PWM and PSM) are fairly identical because the number of conduction states and their duration will not be changed [29]. In case of the PSM shoot-through control method, the switching losses are increased by more than 20% because of an increased number of hard-switched commutations. PSM results in higher overvoltages in the system in comparison with the PWM shoot-through control method [28]. Hence, PWM shoot-through control seems to be a better method for IS DC-DC converters than PSM.

III. New PWM Shoot-Through Control Methods

All the proposed control methods were specially developed

TABLE I
METHOD A: SWITCHING-STATE SEQUENCE PER PERIOD

	Top transistors		Bottom transistors	
	T1	*T3*	*T2*	*T4*
active state		x	x	
shoot-through	x	x	x	x
zero state	x	x		
active state	x			x
shoot-through	x	x	x	x
zero state	x	x		

TABLE II
METHOD B: SWITCHING-STATE SEQUENCE PER PERIOD

	Top transistors		Bottom transistors	
	T1	*T3*	*T2*	*T4*
active state		x	x	
shoot-through	x		x	
zero state	x	x		
active state	x			x
shoot-through		x		x
zero state	x	x		

for the family of IS galvanically isolated DC-DC converters. IS DC-DC converter was based on the full-bridge single-phase inverter, where the top and bottom groups of transistors are denoted as *T1*, *T3* and *T2*, *T4*, respectively.

A. PWM Control with Shifted Shoot-Through (Method A)

This method was first introduced in [30] as an improved alternative to the conventional PWM shoot-through control. Two shoot-through states occur per period. To minimize the switching losses of transistors, one shoot-through state is shifted toward an active state until they merge, as shown in Fig. 5(a). This shift results in a reduced number of hard-switching transients for the bottom transistors (*T2*, *T4*), as shown in TABLE I. The states are shown for one period of the isolation transformer. The conducting switches are indicated by "x." ZVS is achieved for the bottom transistors (*T2*, *T4*) because of the merged shoot-through state. The shoot-through states are generated inside zero states to reduce the number of high harmonics in the transformer voltage. The experimental results prove that *Method A* enables the efficiency of a 1 kW full-bridge front-end inverter to be increased by 4% in comparison with the traditional PWM method [30].

B. PWM Control with Shifted Shoot-Through in One Leg (Method B)

This method is a new modulation technique derived from *Method A*. Instead of generating shoot-through with all four switches, only two switches of one leg are used at a time [Fig. 5(b)]. This technique eliminates two hard-switching transients of the bottom transistors.

The switching frequency of these transistors is reduced in comparison with *Method A*. As a result, in *Method B*, the switching frequencies of the top and bottom transistors are equal, as indicated in TABLE II.

TABLE III
METHOD C: SWITCHING-STATE SEQUENCE PER PERIOD

	Top transistors		Bottom transistors	
	T1	*T3*	*T2*	*T4*
active state		x	x	
shoot-through	x		x	
zero state	x	x		
active state	x			x
shoot-through		x		x

TABLE IV
METHOD D: SWITCHING-STATE SEQUENCE PER PERIOD

	Top transistors		Bottom transistors	
	T1	*T3*	*T2*	*T4*
active state		x	x	
shoot-through	x		x	
zero state	x	x		
shoot-through		x		x
active state	x			x
shoot-through		x		x
zero state	x	x		
shoot-through	x		x	

However, the amplitude value of the shoot-through current is increased, which leads to high power losses during the shoot-through state.

C. Asymmetric PWM Control with Shifted Shoot-Through in One Leg (Method C)

In *Method B*, a zero state is always placed between two subsequent active states (TABLE II). The idea of *Method C* is to shift active states toward each other, so that one of the two zero states can be eliminated [Fig. 5(c)]. An additional soft-switching state for transistor *T4* can then be introduced. The switching frequencies of the top and bottom transistors are equal, as indicated in TABLE III.

However, the frequency of shoot-through states in *Method C* is variable, which affects the input current ripple. The voltage of the isolation transformer is also asymmetrical, which will affect the output voltage ripple.

D. PWM Control with Shifted Double Shoot-Through in One Leg (Method D)

This modulation technique is a derivation from *Method B*. The shoot-through states are split into two and positioned on both sides of the active states [Fig. 5(d)]. As a result, the appearance of shoot-through states will be changed into an irregular one, which will reduce the input current ripple.

TABLE IV shows the switching sequences of the top and bottom transistors. The switching frequencies of the top and bottom transistors are equal, as shown in Fig. 5(d). However, no additional soft-switching states are introduced, and an increased shoot-through current is being switched during commutations.

E. Asymmetric PWM Control with Shifted Double Shoot-Through in One Leg (Method E)

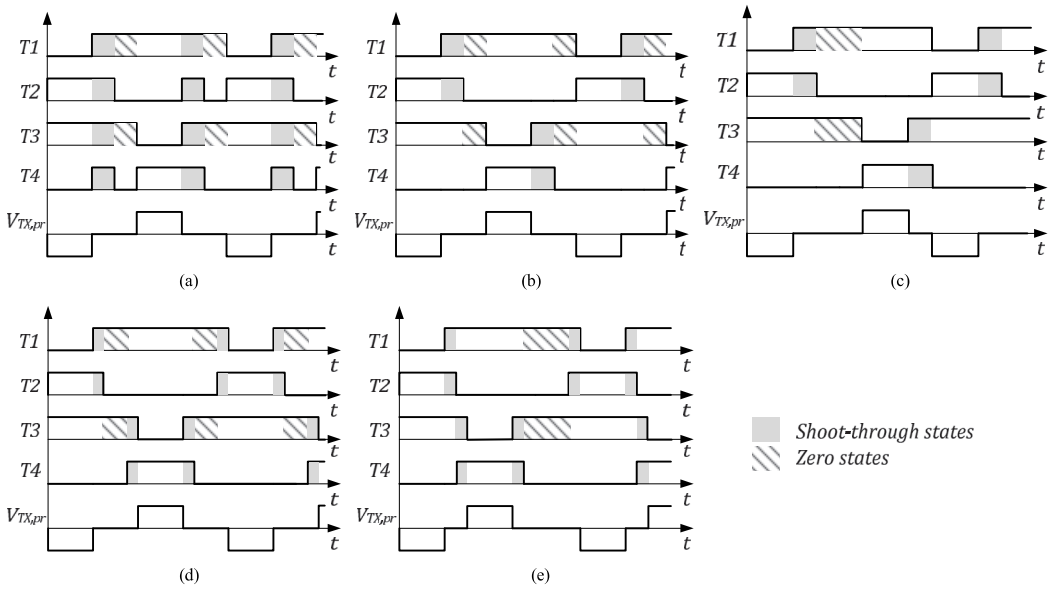

Fig. 5. Studied PWM shoot-through control methods: *Methods* (a) *A*. (b) *B*. (c) *C*. (d) *D*. (e) *E*.

TABLE V
METHOD E: SWITCHING-STATE SEQUENCE PER PERIOD

	Top transistors		Bottom transistors	
	T1	*T3*	*T2*	*T4*
active state		x	x	
shoot-through	x		x	
shoot-through		x		x
active state	x			x
shoot-through		x		x
zero state	x	x		
shoot-through	x		x	

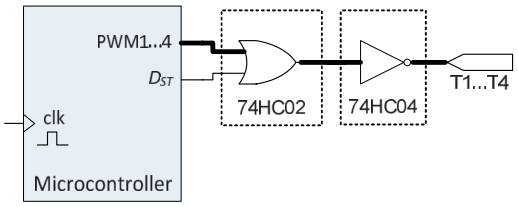

Fig. 6. Shoot-through generation principle by using a microcontroller combined with an external logic circuitry.

The asymmetric PWM control with shifted double shoot-through in one leg was derived from *Methods C* and *D*. The basic idea behind *Method E* is to shift active states toward each other, so that the shoot-through states around the active states can be merged [Fig. 5(e)]. An additional soft-switching state can then be introduced. *Method E* will also reduce the input current ripple in comparison with *Method A*. The switching sequences of each transistor are shown in TABLE V. The switching frequencies of the top and bottom transistors are equal, as indicated in Fig. 5(e).

IV. PRACTICAL GUIDELINES FOR BUILDING THE CONTROL SYSTEM

Microcontrollers generate PWM using timers and compare values. As a rule, conventional microcontrollers have only one or two compare values per timer, which are sufficient in most cases. Currently, the situation is complicated because of shoot-through states.

Up to five compare values are needed to generate PWM with shoot-through states. Consequently, PWM with shoot-through is impossible to implement on most microcontrollers. The following three methods can be considered as a solution to the problem:

1. Using a field-programmable gate array (FPGA).
2. Using a microcontroller combined with an FPGA.
3. Using a microcontroller combined with an external logic circuitry.

In the current project, price and development time were prioritized over flexibility. Thus, the third option was selected. The main idea was to generate the shoot-through state separately from PWM and mix signals through an external logic, as indicated in Fig. 6. We needed only one "NOR" logic block, such as 74HC02, to link PWM and shoot-through D_{ST} signals in the microcontroller output. "NOR" logic inverted the input signal. Additional hex inverters 74HC04 were used to obtain a signal in phase with the microcontroller

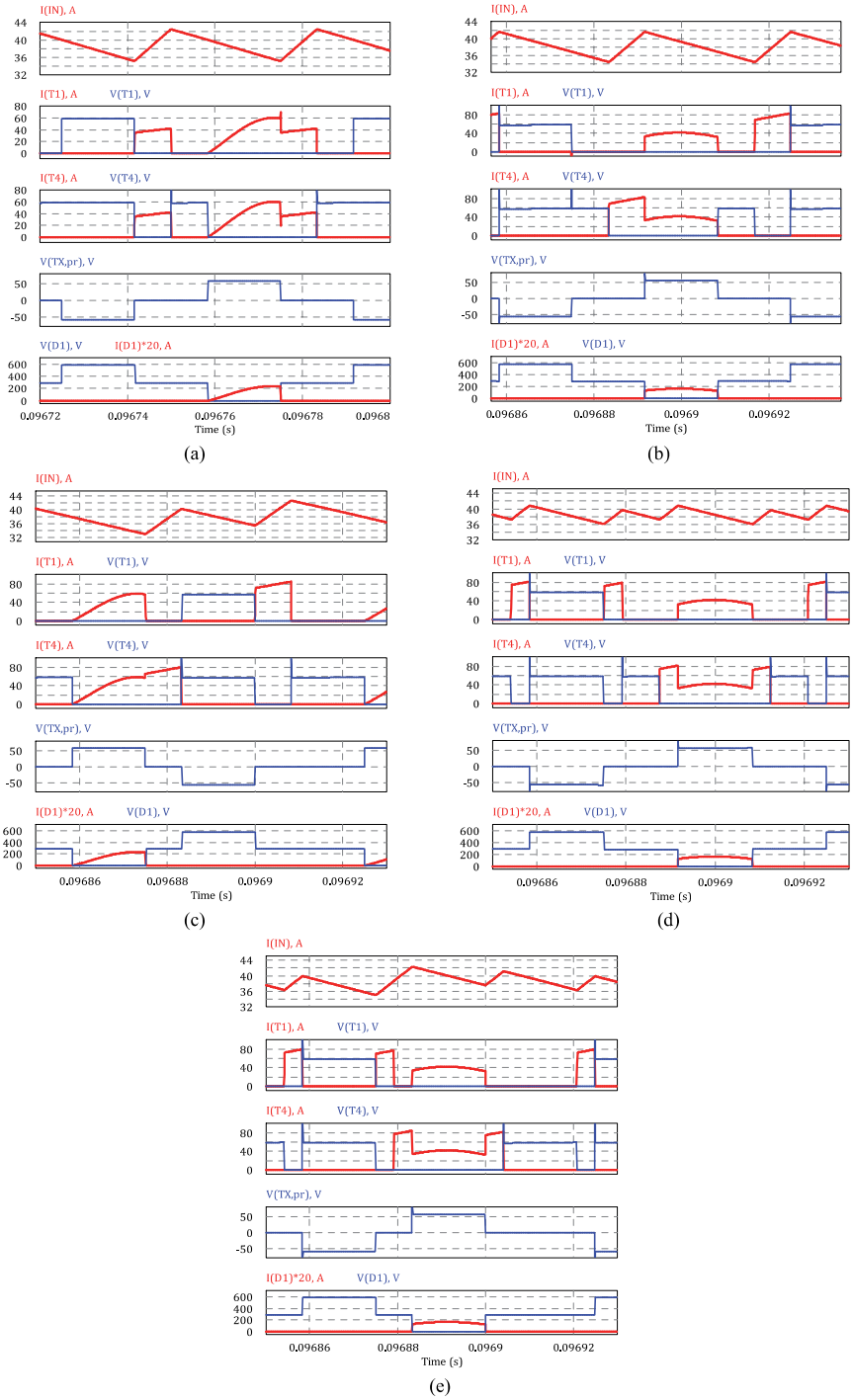

Fig. 7. Simulation results of *Methods* (a) *A*, (b) *B*, (c) *C*, (d) *D*, and (e) *E*.

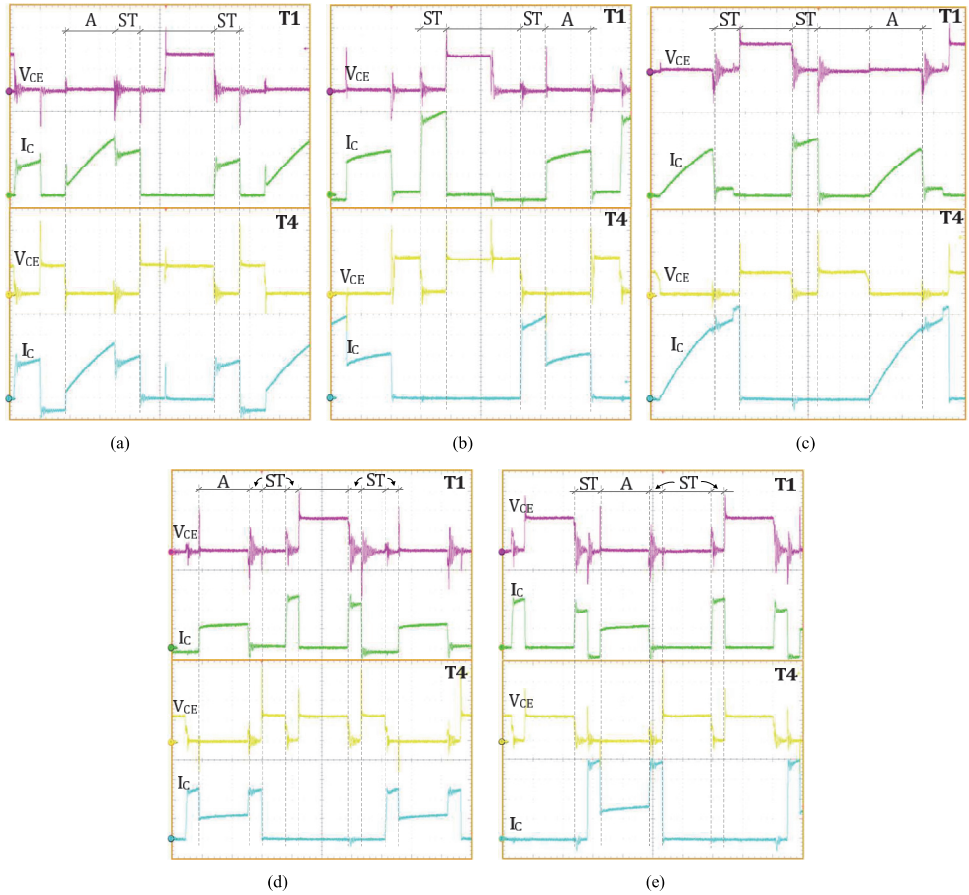

Fig. 8. Experimental waveforms of *Methods* (a) *A*, (b) *B*, (c) *C*, (d) *D*, and (e) *E*.

TABLE VI
OPERATING PARAMETERS OF THE CASE STUDY CONVERTER

Parameter	**Value**
input voltage, V_{IN}	30 V
desired DC-link voltage, V_1	60 V
output voltage, V_{OUT}	600 V
switching frequency, f	15 kHz
shoot-through duty cycle, D_{ST}	0.25
duty cycle of active state, D_Z	0.25
duty cycle of active state, D_A	0.5
load resistance, R_L	300 Ω
operating power, P	1 kW

output. This option is the cheapest and simplest of the three options.

V. SIMULATION STUDY

Lossless models were developed in the PSIM simulation software to evaluate and compare the proposed control methods. The following component values were assumed for the converter during simulations: $C_{qz1} = C_{qz2} = 700$ µF, $L_{qz1} = L_{qz2} = 50$ µH, and $C1 = C2 = 25$ µF. The turn ratio of the isolation transformer was 1:5. qZSC was studied at the operation point with the parameters presented in TABLE VI to demonstrate the basic operating waveforms with the different control methods.

The simulation results are shown in Fig. 7. Figs. 7(b)–(e) show that the proposed shoot-through generation by one inverter leg resulted in the twice-increased amplitude of the shoot-through current in comparison with the baseline approach, in which the shoot-through current was distributed between all of the transistors in the inverter bridge [Fig. 7(a)]. The double shoot-through approach introduced in *Method D* [Fig. 7(d)] decreased the peak-to-peak input current ripple by more than 6% in comparison with *Methods A* and *B* (12% for *Method D* vs. 19% for *Methods A* and *B*). The variable frequency of the shoot-through states in the asymmetric

TABLE VII
COMPARISON OF SWITCHING LOSSES GENERATED BY DIFFERENT PWM SHOOT-THROUGH CONTROL METHODS

	Losses during switching transients, W								Losses per diagonal, W	Total losses, W
	ST (ON)		ST (OFF)		A (ON)		A (OFF)			
	TOP	BOT	TOP	BOT	TOP	BOT	TOP	BOT		
Method A	3.0	3.7	0	27.9	0	0	0	0	34.6	69.2
Method B	0	8.8	18.3	0	0	0	0	11.1	38.2	76.4
Method C	17.2	0	0	17.3	0	0	0	0	34.5	69.0
Method D	14.9	9.5	9.7	18.8	0	0	0	0	52.9	105.8
Method E	11.9	0	9.3	19.6	0	0	0	0	40.8	81.6

PWM control (*Methods C* and *E*) seriously affected the input current ripple by increasing it by more than 6% in comparison with the alternative approach with the symmetric PWM control (*Methods B* and *D*). Therefore, the maximum peak-to-peak input current ripple of 25% was measured with the asymmetric PWM control with shifted shoot-through (*Method C*), which was more than double the case of the symmetric PWM control with the shifted double shoot-through (*Method D*).

In the diodes of VDR, *Methods A* and *C* featured the ZVS of rectifying diodes [Figs. 7(a) and (c)]; however, in *Methods B*, *D*, and *E*, the diodes were hard-switched.

VI. ANALYSIS OF EXPERIMENTAL RESULTS

To experimentally verify the proposed control methods, a 1 kW test setup of IS DC-DC converter was assembled. The front-end inverter was realized on the dual insulated-gate bipolar transistor (IGBT) modules Semikron SEMiX 202GB066HDs. Generalized parameters of the test setup are shown in TABLE VI. The control system was based on the microcontroller dsPIC 33FJ64GS606.

During the experiment, the collector–emitter voltage V_{CE} and the collector current I_C were simultaneously measured on the top (*T1*) and bottom (*T4*) transistors of one diagonal of the inverter bridge. Measured waveforms are presented in Fig. 8. The switching losses of IGBTs were calculated in accordance with the methodology presented in [29]. Losses were calculated for all the switching transients of the corresponding transistor (TOP or BOT) over one operating period, that is, turn-on (ON) and turn-off (OFF) of the shoot-through (ST) and active (A) states. The results are shown in TABLE VII. All the proposed PWM shoot-through control methods featured similar conduction losses and differed only by the number of soft-switching transients (TABLE VII). When considering inverter switching losses, *Methods A* and *C* had total switching losses of approximately 70 W, which was 34% less than that in the case of *Method D*. *Methods B* and *E* had intermediate switching losses of 76 and 82 W respectively.

In *Methods A–C*, two shoot-through states per period were generated; in *Methods D* and *E*, four were generated. *Methods D* and *E* clearly showed that considerable shoot-through states cause an increase in switching losses. However, the increased number of shoot-through states over an operating period also resulted in decreased input current ripple for the same inductance of the inductors in IS network.

Although *Method C* showed good results with respect to switching losses, it also introduced unsymmetrical transformer voltage. In some cases, this result can have some drawbacks, for example, DC-biased primary winding and additional magnetic losses.

VII. CONCLUSIONS AND FUTURE WORK

This study analyzed four novel PWM shoot-through control methods for IS DC-DC converters. The common feature of the new methods is the shoot-through generated by a single inverter leg. An overview of IS DC-DC converter was given, and the operating principle of each control method was explained through the switching-state sequence. Simulation results were verified by experiments. The proposed methods enable no considerable power loss reduction in the IGBT-based front-end inverter. However, they double the number of shoot-through states over one operating period without a significant increase in switching losses. A large number of shoot-through states will increase the effective frequency of the input current ripple, which in turn will result in a decreased value of the inductors and a compact design of the IS network. This issue will be addressed by the authors in detail in future publications.

ACKNOWLEDGMENT

This research work was supported by the Estonian Research Council (Projects SF0140016s11 and PUT744) and the Latvian Council of Science (Grant 416/2012).

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[PAPER-VIII] Kosenko, R.; **Liivik, L.;** Chub, A.; Velihorskyi, O. Comparative Analysis of Semiconductor Power Losses of Galvanically Isolated Quasi-Z-Source and Full-Bridge Boost DC-DC Converters. *Electrical, Control and Communication Engineering*, 2015, 8, 5 - 12.

Comparative Analysis of Semiconductor Power Losses of Galvanically Isolated Quasi-Z-Source and Full-Bridge Boost DC-DC Converters

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***Abstract* – This paper compares semiconductor losses of the galvanically isolated quasi-Z-source converter and full-bridge boost DC-DC converter with active clamping circuit. Operation principle of both converters is described. Short design guidelines are provided as well. Results of steady state analysis are used to calculate semiconductor power losses for both converters. Analytical expressions are derived for all types of semiconductor power losses present in these converters. The theoretical results were verified by means of numerical simulation performed in the PSIM simulation software. Its add-on module "Thermal module" was used to estimate semiconductor power losses using the datasheet parameters of the selected semiconductor devices. Results of calculations and simulation study were obtained for four operating points with different input voltage and constant input current to compare performance of the converters in renewable applications, like photovoltaic, where input voltage and power can vary significantly. Power loss breakdown is detailed and its dependence on the converter output power is analyzed. Recommendations are given for the use of the converter topologies in applications with low input voltage and relatively high input current.**

***Keywords* – DC-DC power converters, energy efficiency, pulse width modulated converters, current-fed converters, impedance-source converters, semiconductor device modeling.**

I. Introduction

Isolated full-bridge boost (IFBB) DC-DC converters are a well known and proven topology [1]-[5]. Up to recently, its spread is limited due to the inherent drawbacks of the current-fed technology, such as high inrush current during start-up and high voltage stress of the transistors. Nevertheless, the IFBB converters can perform voltage step-up and maintain continuous input current in a wide operation range. At the same time, a new quasi-Z-Source (qZS) DC-DC converter topology has emerged that has all the benefits of the IFBB topology and does not suffer from the high inrush current, has even higher step-up factor and therefore potentially wider operation range [6]-[8], [22], [23]. Therefore, the topologies with an input stage that can work as a current-source could be preferable in such low-voltage applications as power conditioners for photovoltaic panels and fuel-cells.

Focus in this paper is on the comparison of these two topologies in terms of energy efficiency in low voltage applications. The generalized power circuit layouts of the qZS and IFBB DC-DC converters are presented in Figs. 1 and 2.

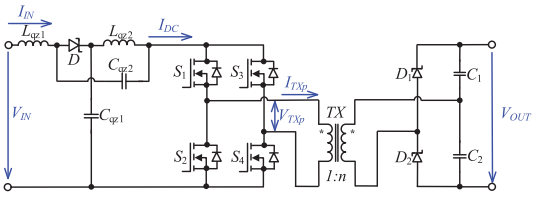

Fig. 1. Galvanically isolated qZS full-bridge DC-DC converter.

Both converters use the voltage doubler rectifier (VDR) to provide a higher voltage step-up factor and reduce the transformer turns ratio. The IFBB converter accommodates an active clamping circuit, which consists of a switch S_{CL} and a capacitor C_{CL} (Fig. 2). It is used to recycle the inductive energy when switching from the shoot-through to the active state, thus minimizing the turn-off losses and reducing the voltage stress of the switches.

II. Operation Principle of the Converters

Fig. 3 shows the basic waveforms of the galvanically isolated qZS full-bridge DC-DC converter. The symmetric overlap of active states is used to control the converter in the continuous conduction mode (CCM). It requires generation of two control signals for the diagonal switches (one for S_1,S_4 and the other for S_2,S_3). These signals are of equal duration and phase-shifted by 180 degrees. The switching period consists of four time intervals:

- a) and c) are the shoot-through state intervals. All four inverter switches are conducting, qZS network inductors are accumulating energy;
- b) is an active state interval when diagonal switches S_1 and S_4 are conducting and energy is transferred to the output filter capacitor C_2;
- d) is another active state when diagonal switches S_2 and S_3 are turned on and energy is transferred to the output filter capacitor C_1.

The operation principle of the qZS DC-DC converter is detailed in [8],[9].

The waveforms of the IFBB DC-DC converter are generalized in Fig. 4. The converter has an additional switch (S_{CL}), but in general the operation principle in the continuous conduction mode is similar to that of the qZS converter.

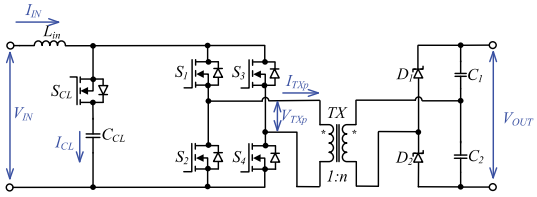

Fig. 2. Galvanically isolated full-bridge boost DC-DC converter.

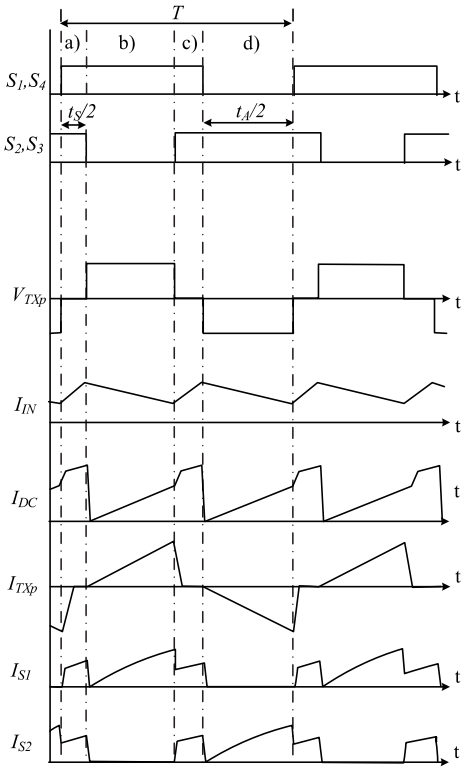

Fig. 3. Generalized waveforms of the qZS full-bridge DC-DC converter.

- a) and c) are the shoot-through intervals. All four inverter stage switches are conducting, the boost inductor L_{IN} is accumulating energy, the clamping switch S_{CL} is turned off;
- b) diagonal switches S_1 and S_4 are conducting, energy is transferred to the output filter capacitor C_2, the clamping switch S_{CL} is turned on to protect inverter switches from the voltage overshoot during the transition from the shoot-through to the active state and back;
- d) diagonal switches S_2 and S_3 are conducting, energy is transferred to the output filter capacitor C_1, the clamping switch S_{CL} is turned on to protect inverter switches from the voltage stress during the transition from the shoot-through to the active state and back.

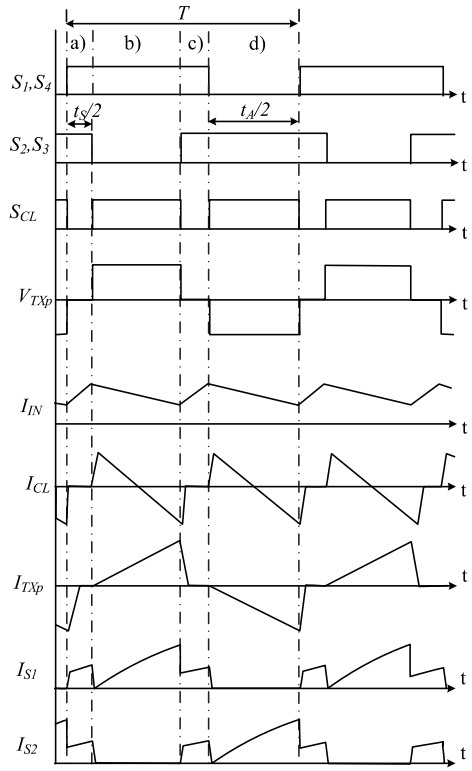

Fig. 4. Generalized waveforms of the IFBB DC-DC converter.

The operation principle of the IFBB DC-DC converter is detailed in [10], [11].

Comparison carried out in this paper is limited to the semiconductor losses because of their strong influence on the performance of both of the converters. To ensure reliable results, the converters were analyzed in the same conditions. Passive elements parameters were calculated to ensure the same input current ripple for both topologies. L_{IN}, L_{qz1} and L_{qz2}were selected to achieve peak-to-peak input current ripple at the level of 10% of the nominal current.

As seen from Figs. 3 and 4, the current through the primary transformer winding (I_{TXp}) is nearly the same for both topologies. Thus, the losses in the magnetic elements have to be nearly equal for both converter topologies. They were excluded from our analysis, since the main difference in the power losses is within semiconductor losses.

III. Design Consideration

Both of the compared topologies are boost-enabled, and their switching period T consists of the shoot-through and the active state. The duty cycles of the shoot-through and the active state are interdependent, as shown in (1):

$$\frac{t_A}{T}+\frac{t_S}{T}=D_A+D_S=1, \tag{1}$$

where t_A and t_S are the duration of the active and the shoot-through state, correspondingly, D_A and D_S are the duty cycles of the active and the shoot-through state, correspondingly.

The output voltage of the qZS full-bridge converter can be expressed as

$$V_{OUT} = 2n \cdot \frac{1}{1-2D_S} \cdot V_{IN}, \quad (2)$$

where n is the transformer turns ratio, V_{IN} is the input voltage of the converter, and V_{OUT} is the output voltage of the converter. For the IFBB converter, the output voltage can be calculated as

$$V_{OUT} = 2n \cdot \frac{1}{1-D_S} \cdot V_{IN}. \quad (3)$$

The main advantage of the discussed converters is the ability to operate with continuous input current. To maintain the CCM, the energy accumulating inductors must be selected based on the converter operation parameters.

For the IFBB converter, minimal inductance of the boost inductor required to limit the input current ripple on the level of $\Delta I_{\%}$ can be calculated as [12]

$$L_{in} = \frac{V_{IN\min}^2 \cdot D_{S\max}}{f_{SW} \cdot P \cdot \Delta I_{\%}} \cdot 100, \quad (4)$$

where f_{SW} is the switching frequency, $\Delta I_{\%}$ is the selected peak-to-peak input current ripple, D_{Smax} is the maximum shoot-through duty cycle, P is the rated power of the converter, and V_{INmin} is the minimum input voltage of the converter.

The inductance of the qZS network inductors required to limit the input current ripple on the level of $\Delta I_{\%}$ from the nominal is expressed by [9]

$$L_{qz1} = L_{qz2} = \frac{1-D_{S\max}}{1-2D_{S\max}} \cdot \frac{V_{IN\min}^2 \cdot D_{S\max}}{f_{SW} \cdot P \cdot \Delta I_{\%}} \cdot 100. \quad (5)$$

The capacitance of the capacitors in the qZS network required to limit the ripple of the DC-link voltage can be calculated as [13]:

$$C_{qz1} = C_{qz2} = \frac{2n \cdot P \cdot D_{S\max}}{V_{OUT} \cdot \Delta V_{\%} \cdot V_{IN\min} \cdot f_{SW}} \cdot 100, \quad (6)$$

where $\Delta V_{\%}$ is the peak-to-peak voltage ripple of the capacitors.

To limit the output voltage ripple on the level of $\Delta V_{\%}$, the capacitance of VDR capacitors should be at least [8]:

$$C_1 = C_2 = \frac{P \cdot D_{S\max}}{\Delta V_{\%} \cdot f_{SW} \cdot V_{OUT}^2} \cdot 100, \quad (7)$$

where V_{OUT} is the nominal output voltage of the converter.

The capacitance of the clamping capacitor (C_{CL}) is based on the LC circuit resonant frequency. The clamping capacitor (C_{CL}) can resonate with either the boost inductor (L_{in}) or with the transformer leakage inductor (L_{TX_leak}). This resonant frequency should be lower than the doubled switching frequency f_{SW}. Since the IFBB converter circuit has two inductors, the clamping capacitance is calculated as the maximum of two values, which is usually determined by L_{TX_leak} [14]:

$$C_{CL} = \frac{1}{16 \cdot L_{TX\_leak} \cdot f_{SW}^2 \cdot \pi^2}. \quad (8)$$

IV. Comparative Analysis of Power Losses and Efficiency

The semiconductor losses of the converter can be categorized to a few major types. Analytical expressions of semiconductor losses in both topologies are well described in [9], [11], [15]-[17]. Here some of the resulting expressions adapted for the discussed converters and applications are presented.

A. Inverter Losses

The primary low-voltage MOSFET semiconductor losses are calculated based on the MOSFET on-state resistance, the average input current, and transformer primary winding current averaged over on the half of the period. The use of average input current value instead of RMS value simplifies the analytical expressions for conduction losses during shoot-through state without significant impact on precision. For example, for the input current with ripple of 50% the difference between average and RMS values is around 1% only [17]. Conduction losses are different for the active and the shoot-through state as the different number of MOSFETs are conducting (Fig. 5). So the resulting equation consists of these two components. Total conduction losses in inverter MOSFETs of IFBB DC-DC converter are expressed by:

$$P_{Ms\_con} = R_{DS(on)} \cdot \left(\frac{P}{V_{IN}}\right)^2 \cdot D_S + 2 \cdot R_{DS(on)} \cdot \left(\frac{4 \cdot n \cdot P}{\sqrt{3} \cdot V_{OUT}}\right)^2, \quad (9)$$

where $R_{DS(on)}$ is the on-state resistance of the MOSFET.

Total conduction losses in inverter MOSFETs of qZS DC-DC converter are expressed by:

$$P_{Ms\_con} = R_{DS(on)} \cdot \left(\frac{2 \cdot P}{V_{IN}}\right)^2 \cdot D_S + 2 \cdot R_{DS(on)} \cdot \left(\frac{4 \cdot n \cdot P}{\sqrt{3} \cdot V_{OUT}}\right)^2, \quad (10)$$

As seen from (9) and (10) component of the inverter MOSFETs conduction losses that corresponds to the active state is the same for both topologies as the difference in RMS values of the transformer primary winding current is compensated by difference in duty cycles of the active state. At constant input current (P/V_{IN}), the MOSFET current during the shoot-through state interval is two times higher in qZS converter than in IFBB converter. However, the shoot-through duty cycle (D_S) for qZS converter is two times lower than for IFBB converter. Therefore component of the inverter

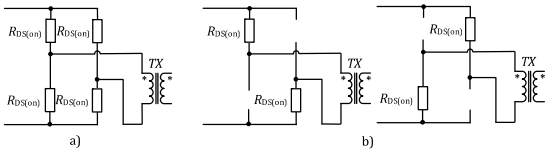

Fig. 5. Equivalent scheme of the inverter during the shoot-through (a) and the active (b) state.

MOSFETs conduction losses that corresponds to the shoot-through state is only two times higher than in IFBB converter. Impact of this component decreases as the shoot-through duty cycle decreases and thus inverter MOSFETs conduction losses are equal for both converters at unity step-up factor.

Switching losses consist of turn-on and turn-off losses:

$$P_{M\_sw} = 4 \cdot \left(P_{M\_on} + P_{M\_off} \right), \tag{11}$$

where P_{M_on} and P_{M_off} are the MOSFET turn-on and turn-off losses accordingly [19]:

$$P_{M\_on} = \frac{1}{2} \cdot \alpha \cdot (I_{IN} - I_{IN} \cdot \Delta I_{\%} / 200) \cdot \frac{V_{out}}{2n} \times \times \left(\frac{Q_{SW}}{V_{drive}} \cdot (R_g + R_{drive}) \right) \cdot f_{SW}, \tag{12}$$

where I_{IN} is the converter input current, Q_{SW} is the MOSFET switching charge, V_{drive} is the MOSFET driver logical "high" voltage (15 V), R_g is the MOSFET internal gate resistance, R_{drive} is the MOSFET driver current limiting resistor (2 Ω);

$$P_{M\_off} = \frac{1}{2} \cdot \alpha \cdot (I_{IN} + I_{IN} \cdot \Delta I_{\%} / 200) \cdot \frac{V_{out}}{2n} \times \times \left(\frac{Q_{SW}}{V_{drive}} \cdot (R_g + R_{drive}) \right) \cdot f_{SW}, \tag{13}$$

In both equations (12)-(13) the coefficient α is used to take into account difference between MOSFET current in shoot-through state in the qZS and IFBB converters. In the worth case, when all switching transients are hard, the inverter MOSFET switching losses differs by two times, since α = 0.5 for IFBB converter and α = 1 for qZS converter. At constant input current, the switching losses of the inverter MOSFETs do not depend on the duty cycle and are fully determined by the parameters of the MOSFETs and the isolation transformer.

B. VDR Losses

The conduction losses of VDR diodes could be estimated by [20]

$$P_{VDR\_con} = 2 \cdot \left(V_{FV\_Vrect} \cdot \frac{P}{V_{OUT}} \right), \tag{14}$$

where V_{FV_Vrect} is the forward voltage drop of the VDR diode.

As seen from (14), conduction losses are growing with the output power.

C. Power losses in the qZS diode

Since the diode is used in the qZS network, the conduction losses depend only on its average current [18], [19]:

$$P_{DqZS\_con} = V_{FV\_DqZS} \cdot I_{IN}, \tag{15}$$

where V_{FV_DqZS} is the forward voltage drop of the qZS diode.

Conduction losses of the qZS diode depend on the shoot-through duty cycle. Taking into account the change of D_S in the range of 0…0.25 (for the converter operating with the twofold input voltage range), the conduction losses will change roughly only by 6%.

D. Losses in Clamping MOSFET

Total power losses on the clamping switch consist of three components:

$$P_{CL} = P_{CL\_con} + P_{CL\_on} + P_{CL\_off}, \tag{16}$$

where P_{CL_con} is the clamping switch conduction losses, P_{CL_on} and P_{CL_off} are the clamping MOSFET turn-on and turn-off losses [11], [16]:

$$P_{CL\_con} = \frac{R_{DS(on)} \cdot I_{IN}^2}{2} \cdot (1 - D_S), \tag{17}$$

$$P_{M\_on} = \frac{1}{2} \cdot (I_{IN} - I_{IN} \cdot \Delta I_{\%} / 200) \cdot \frac{V_{out}}{2n} \times \times \left(\frac{Q_{SW}}{V_{drive}} \cdot (R_g + R_{drive}) \right) \cdot f_{SW}, \tag{18}$$

$$P_{M\_off} = \frac{1}{2} \cdot (I_{IN} + I_{IN} \cdot \Delta I_{\%} / 200) \cdot \frac{V_{out}}{2n} \times \times \left(\frac{Q_{SW}}{V_{drive}} \cdot (R_g + R_{drive}) \right) \cdot f_{SW}. \tag{19}$$

Equations (17)-(19) indicate that only conduction losses depend on the shoot-through duty cycle. So, at constant input current, the total losses of the clamping switch will be growing, moving toward the unity step-up factor (D_S=0).

V. Simulation Results

The 300 W solar module-integrated converter (MIC) was selected as the case study for the modeling. Typically MICs working with a single PV-panel have the nominal output power in the range 240-275 W and maximum power point voltage near 30 V at standard test conditions. The converter parameters must be within that range. The simulation parameters of the converters are listed in Table I.

The power losses and efficiency of both converters were analyzed in four operating points, which cover the whole input voltage range (Table II). The operation parameters of each point were selected to achieve the maximum input current. As seen from Table II and (2), (3), the shoot-through duty cycle D_S needed to achieve the desired voltage boost factor is two times smaller for the qZS converter as compared to the IFBB converter counterpart. This has considerable influence on the distribution of the losses in the converters.

The power loss was analyzed by means of the PSIM simulation software with Thermal Module. It enables the calculation of the power loss in the semiconductor elements based on their datasheet parameters. The semiconductor

elements selected for the simulation and their main parameters are presented in Table III.

To compare simulation and theoretical results, the losses calculated using (9)-(19) are shown in Tables IV and V for qZS and IFBB converters, respectively. The IFBB converter shows up to 4.7% higher calculated efficiency in boost mode.

The simulation results are presented in Tables VI and VII for qZS and IFBB converters, respectively. Fig. 6 shows the graphical representation of the semiconductor losses for both topologies. The dependence of semiconductor losses on the output power for the qZS and IFBB converters are shown in Figs. 7 and 8, respectively. In both converters the contribution of switching losses of the MOSFETs to the total losses remains nearly the same for the whole operation range. The IFBB converter has lower switching losses due to the clamping network that brings inverter stage MOSFET operation mode to partial soft-switching at higher loads.

It is observed that in the qZS converters the main contributor of losses is the qZS diode. It generates more than 50% of the total losses in the entire operation range. As the power increases, the conduction losses on the qZS diode are decreasing due to the minimization of the input current ripple in the operating point with the unity step-up factor.

The second main source of losses in the qZS and the main one in the IFBB converter is the conduction losses of the VDR diodes. In both cases they are increasing almost linearly along with the output power increase. This is due to the increase of the output current while the rectifier diodes forward voltage drop remains nearly constant. In the point with the unity step-up factor, the VDR conduction losses are equal for both topologies as they are working with the same output current

TABLE I

PARAMETERS OF THE COMPARED DC-DC CONVERTERS

Parameter	**Symbol**	**Value**
Input voltage range, V	V_{IN}	15…30
Maximum input current, A	I_{IN}	10
Output voltage, V	V_{OUT}	300
Switching frequency, kHz	f_{SW}	100
Transformer turns ratio	n	5
Capacitance of output capacitors, uF	C_1, C_2	2.2
Converters power rating, W	P	300
Peak-to-peak input current ripple, %	$\Delta I_{\%}$	10
Peak-to-peak voltages ripple, %	$\Delta V_{\%}$	1
Transformer magnetizing inductance, uH	L_{TX_m}	60
Transformer primary leakage ind., uH	L_{TX_leak}	0.38
qZS converter		
Capacitance of qZS capacitors, uF	C_{qz1}, C_{qz2}	33
Inductance of qZS inductors, µH	L_{qz1}, L_{qz2}	28
IFBB converter		
Inductance of boost inductor, µH	L_{in}	38
Capacitance of clamping capacitor, uF	C_{CL}	17

TABLE II

INPUT VOLTAGE AND POWER IN THE SELECTED OPERATING POINTS

Operating point	**1**	**2**	**3**	**4**
V_{IN}, V	15	20	25	30
P, W	150	200	250	300
D_{S_qZS}	0.25	0.167	0.083	0
D_{S_IFBBB}	0.5	0.333	0.167	0

TABLE III

SEMICONDUCTOR COMPONENTS SELECTED FOR THE SIMULATION

Component	**Type**	**Specifications**
S_1…S_4,S_{CL}	Vishay Si4190ADY	V_{DS}=100 V; $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, C_{OSS}=695 pF, R_g=1.1 Ω, Q_g=67 nC
D	Vishay V60D100C	V_{RRM}=100 V; V_F=0.66 V I_F=2x30 A
D_1, D_2	CREE C3D02060E	V_{RRM}=600V; V_F=1.8 V, I_F=4 A

TABLE IV

CALCULATED POWER LOSSES OF THE QZS CONVERTER

	Output power, W			
	150	200	250	300
qZS diode (cond.), W	6.60	6.60	6.60	6.60
MOSFETs (cond.), W	1.47	1.63	1.92	2.35
MOSFETs (switch)., W	1.10	1.10	1.10	1.10
Rectifier diodes (cond.), W	1.80	2.40	3.00	3.60
Total losses, W	10.97	11.73	12.62	13.65
Efficiency, %	92.7	94.1	95.0	95.5

TABLE V

CALCULATED POWER LOSSES OF THE IFBB CONVERTER

	Output power, W			
	150	200	250	300
Clamping MOSFET, W	0.50	0.57	0.64	0.72
MOSFETs (cond.), W	1.03	1.34	1.78	2.35
MOSFETs (switch)., W	0.55	0.55	0.55	0.55
Rectifier diodes (cond.), W	1.80	2.40	3.00	3.60
Total losses, W	3.87	4.86	5.97	7.21
Efficiency, %	97.4	97.6	97.6	97.6

TABLE VI

SIMULATED POWER LOSSES OF THE QZS CONVERTER

	Output power, W			
	150	200	250	300
qZS diode (cond.), W	6.45	6.31	6.28	6.24
MOSFETs (cond.), W	1.98	2.07	2.37	2.50
MOSFETs (switch)., W	0.39	0.39	0.37	0.49
Rectifier diodes (cond.), W	1.39	1.99	2.60	3.30
Total losses, W	10.21	10.76	11.62	12.53
Efficiency, %	93.2	94.6	95.4	95.8

TABLE VII

SIMULATED POWER LOSSES OF THE IFBB CONVERTER

	Output power, W			
	150	200	250	300
Clamping MOSFET, W	0.41	0.44	0.48	0.52
MOSFETs (cond.), W	1.70	1.94	2.22	2.49
MOSFETs (switch)., W	0.29	0.25	0.21	0.20
Rectifier diodes (cond.), W	1.69	2.24	2.78	3.34
Total losses, W	4.09	4.87	5.69	6.55
Efficiency, %	97.3	97.6	97.7	97.8

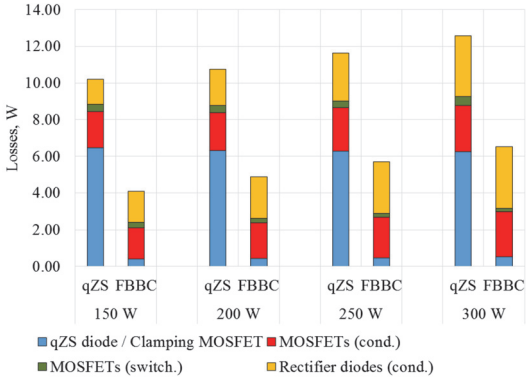

Fig. 6. Semiconductor power losses breakdown of the qZS and IFBB converters.

and duty cycle. At the same time, in other operating modes the VDR losses in the qZS topology are lower than in the IFBB topology. The reason is that to provide the same average output current with a lower active state duty cycle, the VDR diode peak current in the IFBB converter must be higher.

In the IFBB converter, the D_A increases with the output power growing. Therefore, the losses in the clamping MOSFET are rising, since it is conducting only during the active state. In general, the direct impact of the clamping MOSFET losses on the converter efficiency is insignificant.

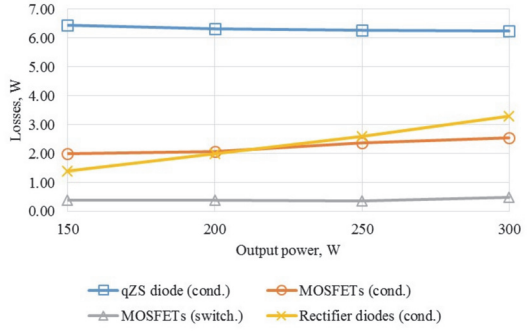

Fig. 7. Semiconductor power losses versus output power in the qZS converter.

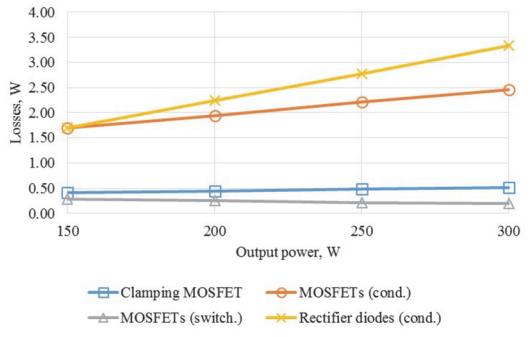

Fig. 8. Semiconductor power losses versus output power in the IFBB converter.

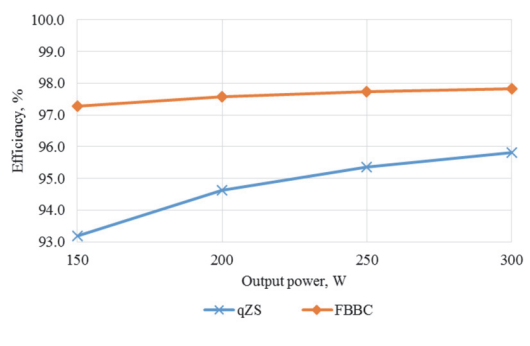

Fig. 9. Efficiency of qZS and IFBB converters versus output power.

Nevertheless, the clamping network has substantial impact on the inverter MOSFET switching losses [10], [15].

The switching losses of the inverter MOSFETs in qZS converter are higher than that in the IFBB converter. It is a result of the higher switching current in boost mode for qZS, as predicted by (12)-(13), and soft-switching possibilities of the IFBB converter with active clamping [24]. This soft-switching performs better at higher load and leads to lower switching losses of the inverter MOSFETs.

The last component in the power losses is the MOSFET conduction losses. They are increasing with the output power increase due to the higher power losses during active state, which depend on the load. In the active state, two MOSFETs are connected in series with the transformer primary winding and conducting output current reflected to the primary winding of the isolation transformer. With given test conditions for both converter topologies the RMS current of the inverter MOSFETs during active state interval differs in boost mode. However they feature equal conduction losses in active state, since different in RMS currents is compensated by the difference of active state duty cycles. The difference in total conduction losses of the inverter MOSFETs for these two converters is determined by the losses during shoot-through state. As shown in Fig. 5, in the shoot-through state the input current is flowing through the parallel connection of two branches with two conducting MOSFETs connected in series [7]. For the IFBB converter in the shoot-through state, the RMS current through each inverter MOSFET is equal to half of the average input current. In the qZS converter the RMS MOSFET current equals to the average input current. Consequently, the conduction losses during shoot-through state in the inverter MOSFETs of the qZS converter are two times higher than that of the IFBB converter, taking into account two times higher duty cycle required for IFBB converter to achieve the same voltage step-up as in the qZS converter. In both converters the conduction losses during the shoot-through state are proportional to its duty cycle. Therefore their impact growing as the step-up factor increases, i.e. the converter input voltage decreases). Since the difference in the conduction losses between two converters is determined only by the component caused from the shoot-through state, the inverter MOSFETs conduction losses are equal for both

topologies in the operating point with the unity step-up factor, which was confirmed by the simulation.

The dependences of the efficiency on the output power for both converters are summarized in Fig. 9. As can be seen, the efficiency curve of the IFBB converter is flat over the whole operation range, while the qZS converter efficiency drops significantly with the decrease of the output power. This efficiency drop is caused mainly by the nearly constant qZS diode conduction losses. They have a crucial impact on the efficiency at light loads.

In general, the distribution of the losses and their dependence on the output power corresponds to the analytical expressions in section III of this paper.

VI. Conclusions

In this paper the semiconductor losses in the isolated qZS and IFBB converters were analyzed and compared.

The comparison shows that the IFBB DC-DC converter topology could be more preferable in low-voltage applications than the conventional qZS full-bridge converter topology with a diode in the qZS network. At the same time, the IFBB converter topology has a number of drawbacks that limit its use. Major drawbacks are the high inrush current and higher voltage stresses under hard-switching as compared to the qZS and conventional voltage fed topologies. Additional active clamping circuit is commonly used in the IFBB converters to improve their switching performance.

Nevertheless, both topologies can be significantly improved in terms of efficiency. For example, by accommodating synchronous qZS-network and synchronous rectification it is possible to increase the maximum efficiency of the qZS converter by up to 3% [7]. This eliminates the main drawback of the qZS converter in low voltage applications. By accommodating separated commutation and four quadrant active switches to the IFBB converter, it is possible to limit voltage stress by achieving full soft-switching and to minimize rectifier stage conduction losses by the use of synchronous rectification [4],[20].

Efficiency is not a single factor in topology selection for low voltage applications. The following additional points for consideration have resulted from our comparison of the discussed topologies in terms of practical applications:

1) qZS converters need fewer MOSFETs, which provides cost savings on MOSFETs themselves, driver circuits, and control system.
2) IFBB converters have only one energy-accumulating inductor as compared to two inductors in the qZS topology. At the same time, the inductance of the IFBB converter inductor is higher than the inductance of the qZS inductors. Moreover, the qZS network inductors can be magnetically coupled, which allows the required inductance value to be reduced two times in the same operating conditions [13],[21]. It means that the qZS can be implemented with a single magnetic component like the IFBB converter.
3) qZS DC-DC converters can work in both the shoot-through and the open state of the inverter, while the IFBB converter needs special circuits and more complex control algorithms to protect the inverter from the voltage overshoot caused by the boost inductor if the open state occurs in the inverter bridge.
4) qZS DC-DC converters have comparatively low efficiency in low voltage applications but can additionally operate in the buck mode (without any additional switches), providing a wider operation range without any need for clamping circuits to protect switches from the voltage stress.
5) qZS DC-DC converters have higher step-up factor (up to 3 with an acceptable level of MOSFET conduction losses), which extends the operating range as compared to that of the IFBB converter [7].

By adopting modern control algorithms and semiconductor devices, current fed topologies have all chances to become widespread in low voltage applications, especially those requiring continuous input current. The choice of a particular topology is determined by the specific application and the additional requirements to the converter.

Acknowledgment

This study was co-financed by Estonian Ministry of Education and Research (project SF0140016s11) and Estonian Research Council (grant PUT744).

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[PAPER-IX] Zakis, J.; Rankis, R.; **Liivik, L.;** Chub, A. Analysis of Buck Mode Realization Possibilities in Quasi-Z-Source DC-DC Converters with Voltage Doubler Rectifier. *IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG)*, Riga, Latvia, 11-13 May, 2015, 1 - 5.

Analysis of Buck Mode Realization Possibilities in Quasi-Z-Source DC-DC Converters with Voltage Doubler Rectifier

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***Abstract*—A series resonant tank in the quasi-Z-source (qZS) DC-DC converter with a voltage doubler rectifier could significantly increase the input voltage regulation range by adding the buck mode realization possibility. This paper discusses two different control approaches of the qZS series resonant DC-DC converter in the buck mode: variable frequency control and phase shift modulation. Both methods are explained by means of steady-state analysis. To verify the theoretical background, a 200 W experimental prototype was built. Experimental results are compared with theoretical predictions.**

Keywords—DC-DC power converter; pulse width modulation converter; resonant inverter.

I. INTRODUCTION

Functionality and flexibility as well as reliability of switch mode converters are the key parameters in the competition between industrial companies. For that reason, converters are designed to have as many functions as possible to achieve universal product requirements without reducing basic advantages and complicating their basic circuit diagram.

Numerous studies have described the advantages of impedance source inverters, highlighting their reliability and simplicity, as step-up converters are mainly intended for renewable energy sources [1], [2]. Fig. 1 presents the quasi-Z-source (qZS) based step-up DC-DC converter first proposed in [3]. It consists of the qZS network, an inverter, an isolation transformer and a voltage doubler rectifier (VDR). If the input voltage is equal to the rated DC-link voltage (U_1=U_{DC}), then the inverter (S_1...S_4) works as a conventional voltage fed full-bridge DC-DC converter. If the input voltage drops below the rated DC-link voltage (U_1<U_{DC}), the converter works in the boost mode by implementing the shoot-through switching states in the control of the inverter bridge to increase the input voltage amplitude up to the rated DC-link level.

In some cases, the output voltage provided by the distributed energy source (PV panels, wind generators or fuel cells) can be higher than required (U_1>U_{DC}) but still the load voltage of the converter should remain at the rated level. The disadvantage of such topology (Fig. 1) is an inability to operate in the step-down (buck) mode because the VDR tends to keep the output voltage on the level of the twofold transformer voltage amplitude. Buck mode could be possible if a full-bridge rectifier and LC-filter are combined on the secondary side of the converter [8], [9].

The aim of this paper is to study the buck function realization possibilities in the qZS DC-DC converter with a VDR in order to extend its input voltage regulation range.

II. TOPOLOGY AND OPERATION

Fig. 2 shows a general circuit diagram of the proposed quasi-Z-source based series resonant DC-DC converter with a VDR. It consists of the qZS network (L_1, L_2, C_1, C_2, D) where both inductors are built on the same core performing magnetic coupling [4], inverter (S_1....S_4) and series resonant circuit (L_r and C_r) in the primary side of the isolation transformer TR and VDR (D_1, D_2, C_3, C_4) with a load (R_{ld}) on the secondary side. Implementation of series resonant elements in the transformer primary circuit was proposed in [5].

This topology enables three operation modes - normal, boost and buck. In the normal operation mode when the input voltage U_1 is nominal and equal to the required DC-link voltage U_{DC}, the commutation frequency of inverter switches is set the same as the resonance frequency (f_{sw}=f_r), thus the full zero current switching (ZCS) operation of inverter switches can be achieved. In the boost operation mode when U_1<U_{DC}, the inverter is controlled by the shoot-through pulse width modulation by an overlap of active states to boost the input voltage U_1 level up to the nominal DC-link voltage level. Normal and boost operation modes were studied in detail in [6], [7].

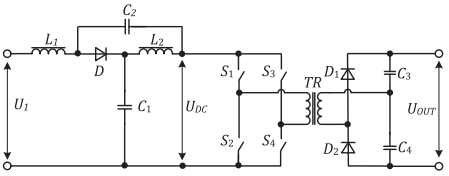


Fig. 1. Generalized topology of the qZS-based step-up DC-DC converter [3].

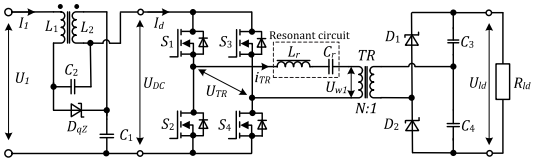


Fig. 2. General circuit diagram of the discussed qZS series resonant DC-DC converter.

If the input voltage is higher than the DC link voltage (U_I>U_{DC}), then the proposed converter should perform a buck function. The realization possibilities of the buck function are further discussed in the next sections.

III. Buck Mode Realization Possibilities

Generally, two main control methods exist for the control of a series resonant DC-DC converter: variable frequency control (VFC) [10] and phase-shift modulation (PSM) [11]. Next, these two approaches will be evaluated as the buck mode control methods for the qZS based series resonant DC-DC converters.

A. Variable Frequency Control

Fig. 3 presents the generalized operation waveforms of the qZS based series resonant DC-DC converter controlled by the VFC. This control method can be performed by changing switching frequency up or down from the resonant frequency. However, the control with higher switching frequency has advantages over its counterpart with lower frequency. It allows soft-switching in the buck mode through utilization of the resonant inductor current for charging the output capacitance of the switches during the deadtime to achieve the zero voltage switching. When the switching frequency is higher than the resonant frequency, the current of one half-cycle that is conducted by one diagonal switch pair is interrupted before the end of the normal sinus wave of the transformer current i_{TR}. Diodes of the second switch pair of the inverter bridge start to conduct the current in the direction reverse to the qZS-network, thus creating a circulating current.

In the interval when diagonal transistors are turned off, the current of the circuit circulates through the DC source (qZS network), diodes of the inverter and primary winding of the transformer. As can be seen, the current through the resonant circuit is not interrupted and is symmetrical to the time axis. With a certain approximation, it can be accepted that the current i_{TR} in that case is close to a sine wave shape, i.e. the current keeps quasi-sinusoidal properties. This mode is called the continuous conduction mode (CCM) of the series resonant converter, usually achieved through proper dimensioning of the resonant tank inductor [12].

Since the switching frequency of the inverter is higher than the resonant frequency, the rms voltage of the resonant capacitor C_r is lower than the rms voltage of the inductor L_r, i.e. there occurs a certain rms voltage across the resonant tank U_{reac}. Assuming that the current in the resonant circuit is sinusoidal, the basic processes can be represented with a vector diagram (Fig. 4) in which the transformer is accepted as a linear element.

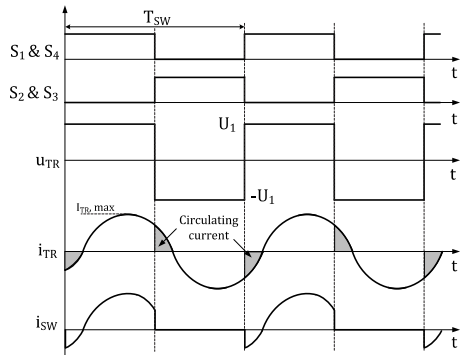


Fig. 3. Generalized operation waveforms of the VFC-controlled qZS based series resonant DC-DC converter.

The balance of resonant circuit voltages can be described from the vector diagram as

$$U_{TR(1)}^2 = U_{reac}^2 + U_{w1(1)}^2 , \tag{1}$$

where $U_{TR(1)} = \frac{4U_1}{\pi\sqrt{2}}$ is the *rms* value of the fundamental component of the bridge output voltage, while $U_{w1(1)} = \frac{4N \cdot U_{ld}}{2\pi\sqrt{2}} = \frac{\sqrt{2}N \cdot U_{ld}}{\pi}$ is the *rms* value of the fundamental component of the primary winding voltage of the isolation transformer.

The voltage across the reactive elements can be expressed as

$$U_{reac} = \frac{I_{rm}}{\sqrt{2}}\left(\omega_{SW} L_r - \frac{1}{\omega_{SW} C_r}\right). \tag{2}$$

The amplitude of the current in the resonant circuit is

$$I_{rm} = 4\pi U_1 \sqrt{\frac{\omega_{SW}^{*2}}{4R_{ld}^2 N^4 \omega_{SW}^{*2} + \rho_r^2 \pi^4 (\omega_{SW}^{*2} - 1)^2}} , \tag{3}$$

while the load voltage is

$$U_{ld} = 4NR_{ld}U_1 \sqrt{\frac{\omega_{SW}^{*2}}{4R_{ld}^2 N^4 \omega_{SW}^{*2} + \rho_r^2 \pi^4 (\omega_{SW}^{*2} - 1)^2}} , \tag{4}$$

where the normalized switching frequency can be expressed as $\omega_{SW}^{*} = \omega_{SW}/\omega_r$, the impedance of the resonant network $\rho_r = \sqrt{L_r/C_r}$ and the resonant frequency $\omega_r = 1/\sqrt{L_r \cdot Cr}$.

It is evident from (4) that the output voltage can be stepped down in the buck mode simply by adjusting the switching frequency. Moreover, sensitivity of the converter to the switching frequency variations depends on the quality factor of the resonant tank, which is a ratio between the impedance of the resonant tank and the load resistance reflected to the input side.

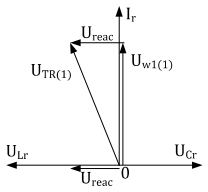


Fig. 4. Vector diagram of currents and voltages in a resonant circuit at the increased switching frequency.

B. Phase Shift Modulation

In the PSM method, the buck function is realized by overlapping the gating signals of the inverter top switches S_1 and S_3 or bottom switches S_2 and S_4. In this case, circulating currents pass through the circuits inside the inverter. Fig. 5 presents theoretical waveforms of the PSM method.

The switching frequency of the transistors is the same as the resonant frequency ($f_{PSM}=f_r$). In the overlapping intervals with the shift phase φ, an input voltage of the resonant circuit is $u_{TR}=0$ but the variation of the current depends on the counter-operation of the voltage across the primary winding of the transformer u_{w1}. Obviously, in the course of the shift, interval current of the resonant circuit changes to a form different from the sine wave. Fundamentals of the resonant circuit current depend on both fundamentals – the input voltage u_{TR} and the primary voltage of the transformer u_{w1}.

If the amplitude of the input voltage is U_1 but its pulse length is shortened from π-φ, the rms of the input voltage can be presented as

$$U_{TR(rms)} = \frac{2U_1}{\pi}\sqrt{1+\cos\varphi}\,, \tag{6}$$

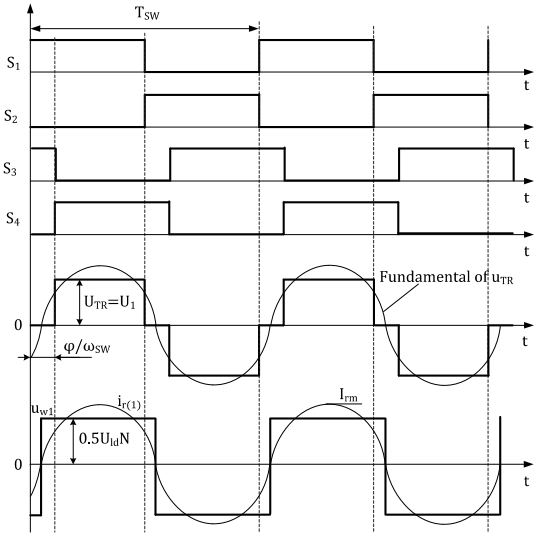


Fig. 5. Generalized operation waveforms of the PSM-controlled qZS series resonant DC-DC converter.

but the rms value of the primary winding of the transformer at its rectangular shape with an amplitude $0.5U_{ld}N$ is

$$U_{w1(rms)} = \frac{2U_{ld}N}{\pi}, \tag{7}$$

where N is the transformer turns ratio.

Since both voltages are equal, the load voltage can be presented as

$$U_{ld} = \frac{\sqrt{2}U_1}{N}\sqrt{1+\cos\varphi}\,. \tag{8}$$

It should be noted that (8) is valid only in the case when the current in the resonant circuit is sinusoidal, i.e. the resonant converter operates in the CCM.

The amplitude of the current in a resonant circuit can be expressed as

$$I_{rm} = \frac{\sqrt{2}\pi U_1}{R_{ld}N^2}\sqrt{1+\cos\varphi}\,, \tag{9}$$

but the current of a DC source as

$$I_d = \frac{2U_1(1+\cos\varphi)}{R_{ld}N^2}. \tag{10}$$

It is shown that the PSM control allows a series resonant converter to operate with a constant switching frequency. Theoretically, the change in the load voltage depends nonlinearly on the phase shift angle φ between the control signals of the inverter legs. Further, if the phase shift angle is 0°, then the output voltage is maximal, since this corresponds to the normal operation mode of the converter. Meanwhile, the output voltage decreases with the increasing phase shift angle, and reaches zero output voltage when the phase shift angle equals 180°.

IV. Concept Verification and Discussion

A. Case Study Converter

For the experimental verification of the theoretical background, the 200 W prototype of the qZS series resonant DC-DC converter was designed and assembled. General operating parameters and the components used are listed in Table I. Load resistance values presented in the table were measured from the experiment. This converter operates in the normal mode at 35 V at the input, when it provides 400 V at the output. The components of the resonant tank have been tuned to achieve 100 kHz resonant frequency and CCM in the experimental prototype.

All calculations and measurements were performed for three operating points in the buck mode and for the normal mode, all at the constant input current. Similar operating conditions are common for renewable applications. For example, photovoltaic module integrated converter can operate in the buck mode at start-up when the panel open circuit is applied to its input. The operating points used in this study are described in Table II. Theoretical and experimental

results for the four operating points are described, discussed and compared below to show differences between the two buck control methods.

B. Theoretical Calculations

Theoretical calculations were performed to show the differences between the two buck control methods under study. In each operating point, the power is different and thus the load resistance and the quality factor are different.

Dependence of the output voltage on the normalized switching frequency obtained from (4) for the case study converter controlled with the VFC is shown in Fig. 6 for operating points *A*…*C*. It is evident that the switching frequency will be changing in a narrow range to stabilize the output voltage at the same level. This is due to different quality factors and output voltage values at the resonant frequency for each point. Here losses could be accounted as an additional resistance in the circuit, and thus the quality factor lower than that calculated theoretically will define the behavior of the converter. Therefore, the frequency measured experimentally has to be higher than that predicted theoretically.

TABLE I. GENERAL OPERATING PARAMETERS

Operating parameters	**Value/type**
Rated power, P	200 W
Input voltage, U_I	35…50 V
Output voltage, U_{Id}	400 V
Resonant frequency, f_{SW}	100 kHz
Components	
Switch, S_1...S_4	Si4190ADY
Diode, D	V60D100C
Inductors L_1=L_2	22 µH
Capacitors C_1=C_2	26.4 µF
Capacitors C_3=C_4	2.2 µF
Resonant inductor L_r	23.3 µH
Resonant capacitor C_r	93 µF
Transformer turns ratio, N	1:6.5

TABLE II. OPERATING POINTS USED IN THE STUDY

Operating point	**Input voltage, U_I**	**Load resistance, R_{Id}**	**Input current, I_I**
Point *A*	40 V	1210 Ω	4 A
Point *B*	45 V	1100 Ω	4A
Point *C*	50 V	1012 Ω	4A
Point *D*	35 V	1370 Ω	4 A

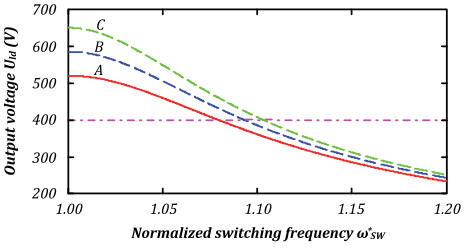


Fig. 6. Regulation characteristics of the case study converter with the VFC.

A set of regulation characteristics were obtained using (8) for the case of the PSM control (Fig. 7) for operating points in the buck mode. They have a similar dependence on the phase shift angle, while the output voltage at the zero angle is different. At the same time, theoretical voltage in the normal mode for point *D* equals 455 V and thus control angles at each curve have to be taken at this level. Further, they will be compared with those obtained from the experiment. This control method does not suffer from sensitivity to the load resistance. However, the losses will lead to a lower output voltage. Thus, experimental values of the phase shift angle have to be lower than those calculated theoretically.

C. Experimental Verification

The experimental prototype was tested to verify theoretical predictions. The test bench includes the digital phosphor oscilloscope Tektronix DPO7254 equipped with high-voltage differential voltage probes Tektronix P5205A and the Rogowski coil current probe PEM CWTUM/015/R for capture of operating waveforms.

Experimental waveforms were obtained at the experimental prototype for operation point *C,* i.e. at maximum input voltage, for both control methods. Our experiment shows that the switching frequency equal to 114 kHz is required in the case of the VFC to obtain 400 V at the output of the converter, when 50 V voltage is applied to its input. The phase shift angle equal to 84.6° was needed to perform the same voltage step-down in the case of the PSM.

Fig. 8 presents the current and voltage of one inverter switch (S_3) for both control methods – the VFC (Fig. 8*a*) and the PSM (Fig. 8*b*). In the first case, the switch handles negative current and thus can be turned on with zero voltage switching (ZVS) if proper deadtime is used to achieve body diode conductivity in the beginning. Since the transformer current is high before the turn-off transient, the ZVS turn-off assisted with leakage inductance is possible if deadtime is used and selected properly to ensure switch output capacitance recharge. In the second case, the ZVS can be achieved with proper deadtimes with the difference that the leakage inductance assists ZVS turn-on, while ZVS turn-off is ensured with a body diode.

Fig. 9 presents the voltage and current of the input side winding of the isolation transformer for both control methods. In the case of the VFC (Fig. 9*a*), the transformer voltage is rectangular without zero level intervals, while in the case of the PSM (Fig. 9*b*), it features zero level intervals at the input

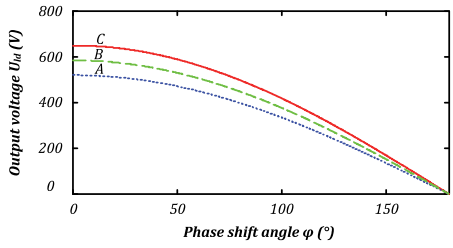
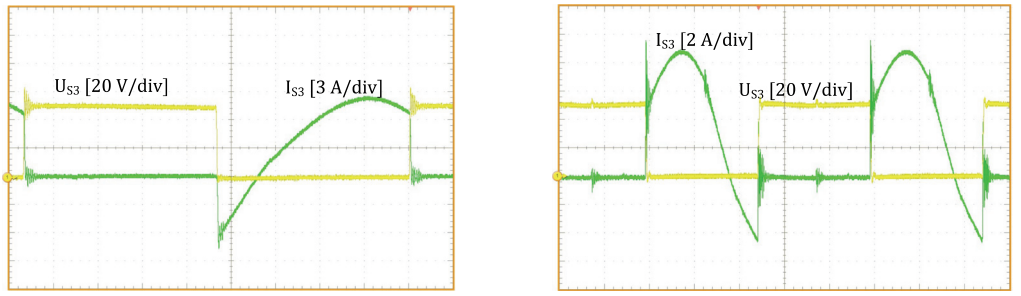


Fig. 7. Regulation characteristics of the case study converter with PSM.

side winding. However, the output side winding voltage is rectangular without zero level intervals and synchronized with zero crossing instants of the transformer current. Duration of the zero level intervals at the input side winding is directly proportional to the phase shift angle φ.

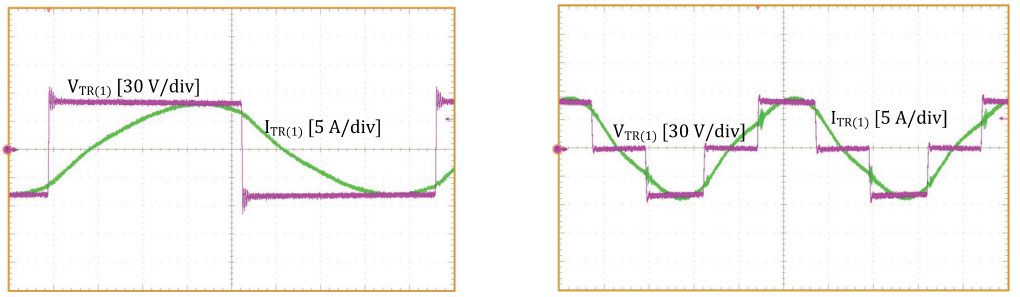
Fig. 10 presents the voltage and current of diode D_2 of the VDR. The VDR diodes feature ZCS operation assisted with the leakage inductance of the isolation transformer for both control methods. It is evident that both control methods properly exploit soft-switching possibilities of the series resonant converter.

Regulation characteristics of both of the buck mode realization methods measured are presented and compared with theoretical predictions in Fig. 11. Fig. 11*a* illustrates the frequency to be applied to the converter if the input voltage is higher than the rated one. Apparently, the switching frequency measured is higher than that predicted theoretically. It is mostly due to higher losses that result from a lower quality factor, which requires higher frequency for the same voltage step-down. However, the frequency regulation range is still narrow, as it was predicted theoretically. Similarly, Fig. 11*b* illustrates the inverter phase shift angle to be used when the



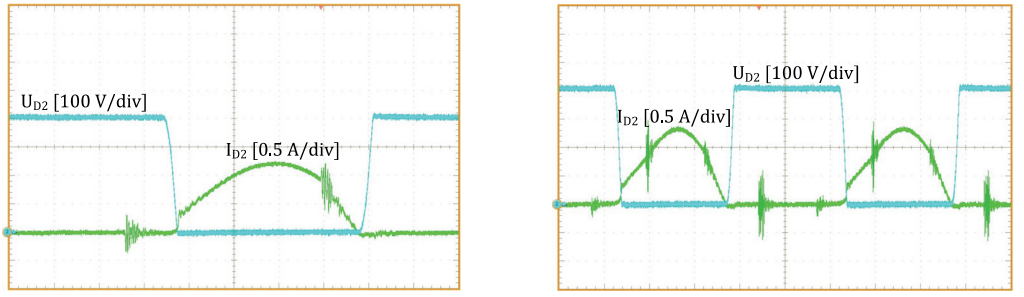
(a) (b)

Fig. 8. Experimental waveforms of the switch S_3 of the inverter: a) VFC in time scale 1 μs/div; b) PSM in time scale 2 μs/div.



(a) (b)

Fig. 9. Experimental waveforms of the transformer primary voltage and current: a) VFC in time scale 1 μs/div; b) PSM in time scale 2 μs/div.



(a) (b)

Fig. 10. Experimental waveforms of the VDR diode D_2: a) VFC in time scale 1 μs/div; b) PSM in time scale 2 μs/div.

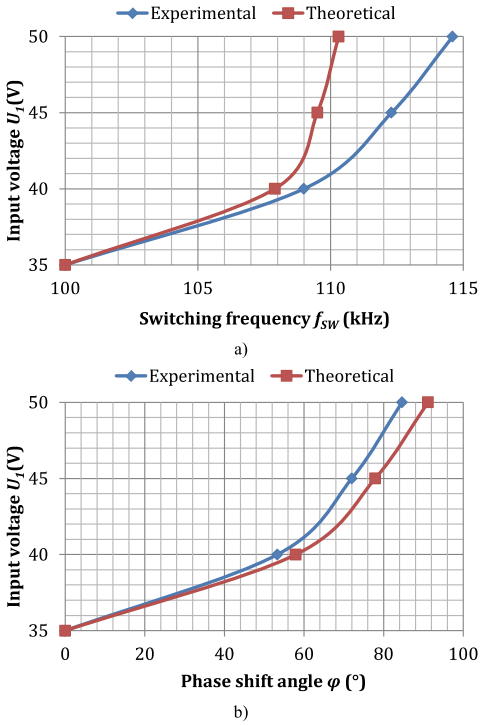


Fig. 11. Regulation characteristics in the buck mode for VFC (a) and PSM (b).

input voltage is higher than 35 V. These results are also in good agreement with the predictions. The converter requires a slightly lower phase shift angle than predicted theoretically, since the power loss in the converter leads to additional voltage step-down.

V. Conclusions

In this paper two different buck mode control methods for the galvanically isolated qZS based series resonant DC-DC converter were presented and verified. Both of them allow realization of the buck mode in the qZS based series resonant DC-DC converter with the VDR.

In the given case, an input voltage rise by more than 40% over the nominal value was considered. It means that the regulation range of the converter can be easily doubled if the voltage step-up in the boost mode is limited by 1:2. Moreover, both methods show an ability to step the voltage even further down. In other words, the combination of buck and boost operating modes allows the design of the qZS converter with an ultra-wide input voltage range.

Among the two buck mode realization methods, the PSM seems to be superior over the VFC. The PSM does not depend on the load resistance and provides constant switching frequency. It avoids poor controllability at light loads typical for the VFC. Moreover, in PSM the converter power loss results in a smaller phase shift than necessary for the voltage step-down as compared to the phase shift angle calculated theoretically. At the same time, the converter power loss leads to higher switching frequency than that calculated theoretically in the case of the VFC. This is due to the high sensitivity of the VFC regulation characteristic to the quality factor of the converter that depends on the load resistance and indirectly on the converter power loss. Due to power losses in the converter, higher frequency is required in the VFC than that theoretically predicted. At the same time, smaller phase shift angle will be required to achieve the nominal output voltage level in the PSM.

Finally, soft-switching operation of the converter can be maintained for both of the buck mode realization methods.

Acknowledgment

This research work has been supported by Latvian Council of Science (Grant 416/2012) and by Estonian Ministry of Education and Research (project SF0140016s11).

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[PAPER-X] **Liivik, L.**; Chub, A.; Vinnikov, D.; Zakis, J. Experimental Study of High Step-Up Quasi-Z-Source DC-DC Converter with Synchronous Rectification. *9th International Conference on Compatibility and Power Electronics. (CPE),* Lisbon, Portugal, 24-25 June, 2015 pp. 1-6.

Experimental Study of High Step-Up Quasi-Z-Source DC-DC Converter with Synchronous Rectification

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***Abstract*—Quasi-Z-source DC-DC converters have attracted research interest due to their numerous advantages in emerging applications. However, they suffer from relatively low efficiency. This paper presents semiconductor loss breakdown of the quasi-Z-source DC-DC converter to show that conduction losses in semiconductors contribute most to overall losses. Synchronous rectification realized through replacement of diodes with N-channel MOSFETs was proposed to improve the converter efficiency in prior works. Our detailed experimental study of efficiency improvement with synchronous rectification was based on a 250 W prototype. Results were first obtained for replacement of diodes in the primary side only, then in the secondary side only. Finally, a converter that contains only controlled switches was evaluated. Efficiency curves measured were compared with those for the baseline diode-based topology. The experimental study was performed using operating points typical of photovoltaic module integrated converters.**

Keywords—DC-DC converter, synchronous rectification, quasi-Z-source, power losses, photovoltaic energy converter.

I. Introduction

The technology of galvanically isolated impedance-source DC-DC converters is an emerging trend in the modern power electronics [1]. It has gained popularity as a novel type of electric energy conversion alternative to current- and voltage-source converters. Among impedance-source converters, the quasi-Z-source (qZS) full-bridge DC-DC converter (Fig. 1) proposed in [2] suits best for renewable and alternative energy applications according to [3]-[5]. It features a wide input voltage regulation range performed within a single stage, continuous input current, immunity to shoot-through and open states of the inverter bridge, low inrush current, high control flexibility, etc. However, all these advantages are achieved at the cost of higher number of passive components and relatively low efficiency in emerging applications, which are usually associated with high input current and low input voltage values.

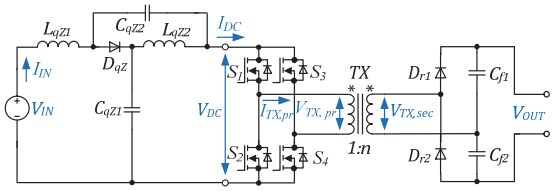

Fig. 1. Diode based quasi-Z-source full-bridge DC-DC converter.

Simulation study of the qZS DC-DC converter (qZSC) in [6] shows that conduction losses in semiconductors are the major cause of relatively low efficiency. Efficiency improvement through synchronous rectification was proposed and verified by help of simulation in [7]. It was suggested to replace diodes with N-channel MOSFETs in order to reduce conduction losses that are smaller in transistors than in diodes. Such replacement can be extremely advantageous even at higher cost related to the driver circuit implemented and additional losses for MOSFET driving. Fig. 2 shows an example of simplified calculation of conduction power losses in the Schottky diode with forward voltage drop $V_F = 0.6$ V, and in the MOSFET with on-state resistance $R_{DS(on)} = 9$ mΩ when they operate at constant current. Moreover, the MOSFETs feature the positive temperature coefficient of an on-state resistance and thus can be easily paralleled [8].

The simulation results in [7] show that the efficiency of the converter under discussion can be increased roughly by 2%. The aim of this paper is to verify this prediction experimentally. Section II describes the operating principle of the baseline converter and the simulation study of its semiconductor power losses. Then, three different realization possibilities of synchronous rectification are covered in Section III. Experimental measurements of efficiency for three topological variations of the case study converter are presented and compared with that for baseline diode based topology in Section IV.

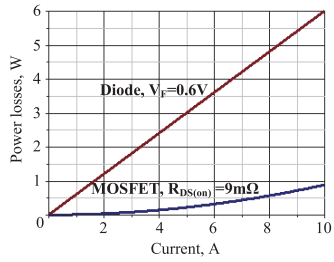

Fig. 2. Conduction losses in a diode and a MOSFET conducting constant current as functions of that current value.

II. Operating Principle and Semiconductor Power Losses of the Case Study Converter

A. Operating Principle of the qZS DC-DC Converter

The qZSC (Fig. 1) contains a qZS network, which comprises two capacitors C_{qZ1}, C_{qZ2}, two inductors L_{qZ1}, L_{qZ2}, and a single diode D_{qZ}. It couples input terminals and a full-bridge inverter $S_1 \ldots S_4$ that supply the step-up isolation transformer *TX* with rectangular bipolar voltage pulses. At the output side, this voltage is rectified and filtered with a voltage doubler rectifier (VDR), which contains two diodes D_{r1}, D_{r2} and two filter capacitors C_{f1}, C_{f2} that feed an output load. The converter performs voltage step-up at the input side through the PWM inverter control that contains shoot-through states in a switching sequence. The idea is to stabilize the inverter input voltage V_{DC} to maintain constant output voltage. Numerous shoot-through generation methods are available [9]-[12]. In the given case, the PWM with symmetrical overlap of active states seems to be the most appropriate, since its switching sequence contains no zero states that are virtually useless for control purposes due to the utilization of a VDR. Idealized voltage and current wave shapes of the given converter that features PWM with symmetrical overlap of active states are shown in Fig. 3.

This paper considers only continuous conduction mode, which requires proper dimensioning of the qZS network inductors [13]. Hence, the switching period T contains a combination of shoot-through states, which are used to step up input voltage and active states when energy is transferred from the input side to the output side through the isolation transformer *TX*. Shoot-through state is created by all four switches during the intervals (1) and (3) shown in Fig. 3. The qZS network limits the input current of the inverter I_{DC} at the level of cumulative currents of the qZS network, i.e. two times higher than the input current I_{IN}. The converter increases the energy stored in the qZS inductors, while the diode D_{qZ} is reverse biased. Cumulative duty cycle of the shoot-through states equals D_S. The other part of the switching period is dedicated to the active state, when one of the inverter diagonals supplies the isolation transformer with the voltage V_{DC} (intervals (2), (4) in Fig. 3). The qZS network behaves as a voltage source with the output voltage equal to the sum of qZS capacitor voltages. Transformer current is rising linearly with a slope defined by the leakage inductance of the isolation transformer. It charges the VDR capacitor C_{f1} or C_{f2} through the VDR diode D_{r1} or D_{r2}, respectively. Cumulative duty cycle of the active states equals $D_A = 1\text{-}D_S$. In case the input voltage of the converter equals the inverter nominal voltage, the converter operates without shoot-through states, similar to a conventional voltage-fed full-bridge converter (normal mode operation). The voltage across qZS network capacitors and the voltage gain of the converter B depend on the input voltage and shoot-through duty cycle [2]:

$$V_{CqZ1} = \frac{1-D_S}{1-2\cdot D_S}\cdot V_{IN}\,,\; V_{CqZ2} = \frac{D_S}{1-2\cdot D_S}\cdot V_{IN}\,, \tag{1}$$

$$B = \frac{V_{OUT}}{V_{IN}} = \frac{2\cdot n}{1-2\cdot D_S}\,, \tag{2}$$

where n is the turns ratio of the isolation transformer.

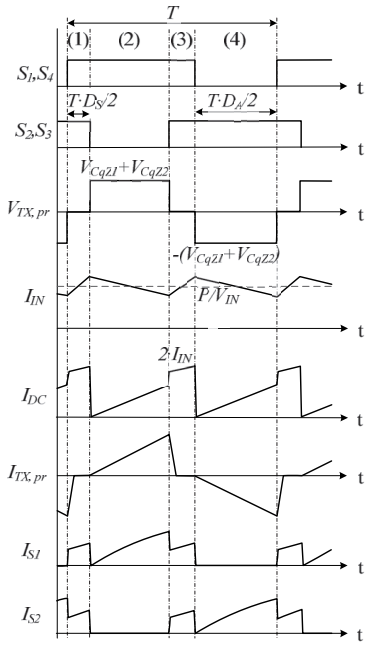

Fig. 3. Idealized current and voltage wave shapes of the qZSC.

B. Description of the Case Study qZS DC-DC Converter

Focus in this paper is on the MOSFET based qZSC designed as a photovoltaic module integrated converter. The operation range of the converter is limited by the rated operating power (P) of 240 W and the maximum continuous input current of 8 A. These limitations are common for interface converters for 60-cell solar panels. Usually, the maximum power point of such panes is within the range from 15 V to 30 V, depending on the weather conditions. For further studies, four operating points described in Table I were selected: three in the boost mode when shoot-through is utilized to step up the input voltage, which is lower than the nominal value, and one in the normal mode when the input voltage equals the nominal value. Evidently, the converter has to operate with different power and voltage step-up levels, while the input current remains constant for all operating points. All numerical simulations in this paper were performed using PSIM software with "Thermal module" add-on, which allows assessment of semiconductor power losses using datasheet parameters. Semiconductor devices described in Table II were used in the experimental prototype, while the simulation model implemented was based on their datasheet parameters. Table III presents the operating range, switching frequency and values of the passive components.

C. Analysis of Semiconductor Power Losses

First, the simulation study of semiconductor power losses was performed for the baseline diode-based qZSC for given operating parameters. Detailed distribution of semiconductor power losses for all operating points is presented in Fig. 4. It shows that the majority of losses present in the converter are conduction losses. It is evident that a qZS Schottky diode contributes most to semiconductor power losses relative to conduction losses, while its switching losses are close to zero. The conduction losses of the qZS diode (P_{DqZ}) are nearly constant, since they are defined by the forward voltage drop of the diode V_{F_DqZ} and the constant input current:

$$P_{DqZ} = V_{F\_DqZ} \cdot I_{IN} . \quad (3)$$

The conduction losses in the VDR diodes (P_{Dr}) change with the operating power linearly, since they depend on the forward voltage drop of the VDR diodes (V_{F_Dr}) and the output current, which depends on the operating power P linearly due to the constant output voltage V_{OUT}:

$$P_{Dr} = V_{F\_Dr} \cdot \frac{P}{V_{OUT}} . \quad (4)$$

The conduction power losses in the inverter MOSFETs (P_{Mcond}) contribute the last part to the semiconductor conduction power losses in the converter. They can be separated into two parts [6]:

$$P_{Mcond} = R_{DS(on)} \cdot P^2 \cdot \left(\left(\frac{4}{V_{IN}} \right)^2 \cdot D_S + 2 \cdot \left(\frac{8 \cdot n}{\sqrt{3} \cdot V_{OUT}} \right)^2 \right). \quad (5)$$

The first part is caused by the shoot-through state and depends on its duty cycle and the operating power. The second part is defined by the active state and depends only on the operating power value. Conduction power losses in the MOSFETs are rising slowly due to changes of both operating power and shoot-through duty cycle between the given operating points. It leads to their redistribution, while cumulative value changes slightly. These losses can be reduced if MOSFETs with lower on-state resistance ($R_{DS(on)}$) are used. However, they will require higher driving power and will provide slower switching dynamics due to higher parasitic capacitances.

Finally, the switching losses in MOSFETs are low due to low operating voltage and high dynamic performance of low-voltage MOSFETs. Their further reductions could require significant efforts without reasonable effect. Obviously, the simplest way to improve the efficiency of the converter considerably is to reduce conduction losses in the diodes. Synchronous rectification is commonly used to decrease semiconductor conduction losses. Three possible implementations of synchronous rectification in the qZSC are described in the next section.

TABLE I. OPERATING POINTS USED IN THE STUDY

Parameters	Test point			
	1	*2*	*3*	*4*
V_{IN}, V	15	20	25	30
I_{IN}, A	8	8	8	8
Voltage step-up (V_{DC}/V_{IN})	2.0	1.5	1.2	1
P, W	120	160	200	240

TABLE II. SPECIFICATIONS OF SEMICONDUCTORS USED IN THE STUDY

Component	Type	Specifications
$S_1 \ldots S_4$, S_{qZ}	Vishay Si4190ADY	V_{DS}=100 V; $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, Q_g=20.7 nC, R_g=2.2 Ω
D_{qZ}	Vishay V60D100C	V_{RRM}=100 V; V_{F_DqZ}=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_{r1}, D_{r2}	CREE C3D02060E	V_{RRM}=600 V; V_{F_Dr}=1.8 V $I_{F(AV)}$=4 A
S_5, S_6	ROHM SCT2120AF	V_{DS}=650 V; $R_{DS(on)}$=120 mΩ I_D=29 A, Q_g=61 nC, R_g=2.5 Ω

TABLE III.
GENERALIZED OPERATING PARAMETERS OF THE CONVERTERS

Parameter	Symbol	Value
Input voltage range, V	V_{IN}	15…30
Maximum input current, A	I_{IN}	8
Nominal DC-link voltage, V	V_{DC}	30
Output voltage, V	V_{OUT}	240
Switching frequency, kHz	f_{sw}	100
Operating frequency of the qZS-network, kHz	f_{qZS}	200 ($2 \cdot f_{sw}$)
Transformer turns ratio	n	1:4
Leakage inductance of the transformer, µH	L_l	0.5
Magnetizing inductance of the transformer, µH	L_m	30
Capacitance of qZS capacitors, µF	C_{qz1}, C_{qz2}	26.4
Inductance of qZS inductors, µH	L_{qz1}, L_{qz2}	22
Capacitance of output capacitors, µF	C_{f1}, C_{f2}	2.2

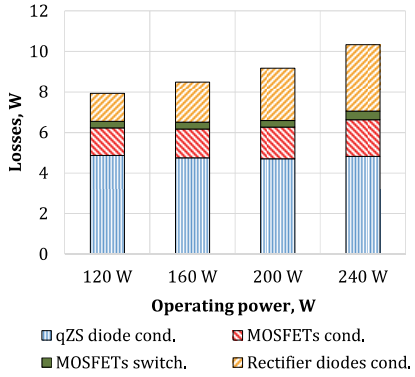

Fig. 4. Estimated semiconductor power loss breakdown.

III. Realization of Synchronous Rectification

A. qZSC with Synchronous qZS Network

The semiconductor power loss breakdown (Fig. 4) shows that diode D_{qZ} in the qZS network contributes from 49% to 64% of the conduction losses, depending on the operating point. These results were obtained for a Schottky diode, which is the most advantageous type for step-up converters that handle low voltage and high current at the input side. Nevertheless, it features considerable conduction losses, while its switching losses can be neglected. The qZS network diode D_{qZ} can be replaced with an N-channel MOSFET that is controlled synchronously with inverter switches in order to increase the converter efficiency, as shown in Fig. 5.

Control principle for that topological variation is shown in Fig. 6. Realization of synchronous rectification does not change the operating principle of the converter, while its efficiency can be improved. In the boost mode (Fig. 6*a*), the qZS MOSFET S_{qZ} must be turned off in the shoot-through state to prevent short-circuiting of the qZS capacitors. Hence, the dead-time of a proper duration must be utilized to avoid the failure and consequently, ensure high efficiency. Usually it is up to 100 ns for low-voltage MOSFETs. In the normal mode (Fig. 6*b*), the qZS MOSFET must be turned-on continuously to achieve the best performance.

A body diode of the qZS MOSFET conducts current during dead-time periods. Its dynamic performance is worse than that of the Schottky diode. Thus, effect from the implementation of the qZS MOSFET will be somewhat diminished by the switching losses of the body diode, mostly caused by the reverse recovery processes. Also, forward voltage drop of the body diode is higher than that of the Schottky diode, which results in additional conduction losses during the dead-time. Thus, the dead-time should not be overdimensioned. These drawbacks can be avoided if a small Schottky diode is connected in parallel to the qZS MOSFET to shunt its body diode [8].

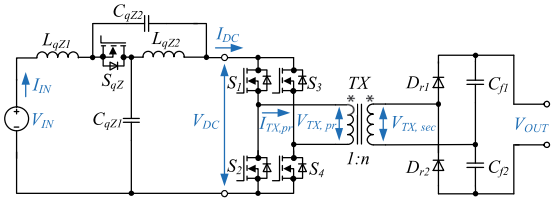

Fig. 5. Modified qZSC with the synchronous qZS network.

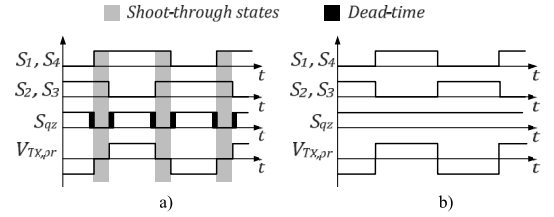

Fig. 6. Control principle of the qZSC with the synchronous qZS network in: a) the boost mode, and b) the normal mode.

B. qZSC with a Synchronous (Active) VDR

The conduction losses in the VDR diodes can be reduced in the same manner as in the qZS network, as shown in Fig. 7. In the baseline topology, the SiC Schottky diodes are common in the VDR due to their negligible switching losses, which is essential for the output high-voltage side of a high-frequency converter. To improve the efficiency of the VDR, high-voltage MOSFETs with low on-state resistance are required. Si superjunction (SJ) MOSFETs, like CoolMOS from Infineon, and SiC MOSFETs feature low enough resistance. Overall performance of the SiC devices is better than that of Si counterparts [15]. The Si SJ MOSFETs have high reverse recovery charge and parasitic capacitances, which leads to high driving power and switching losses [14]. Moreover, reverse recovery time of SiC MOSFETs is smaller by a factor of ten than that of the Si MOSFETs. Thus, they were selected for our further experimental study. The control principle for the topological variation with a synchronous VDR is shown in Fig. 8. It utilizes dead-times to avoid short-circuiting of the VDR capacitors. Switching losses of high-voltage switches are higher than those of low-voltage ones. Thus, reduction of conduction losses in the VDR will be affected by additional switching losses.

C. Full-Synchronous qZSC

The concept of a full-synchronous qZSC is derived by a combination of two topological variations described in this section above. The topology (Fig. 9) contains seven fully controlled switches. It has to combine benefits of the previous two topologies. Moreover, it can provide bidirectional power transfer [16]. All additional MOSFETs are controlled synchronously with inverter switches and utilize dead-time, as shown in Fig. 10. The dead-time of the qZS MOSFET S_{qZ} is avoided in the normal mode to improve the overall converter efficiency. At the same time, the VDR MOSFETs S_5, S_6 require dead-time for proper operation in both modes.

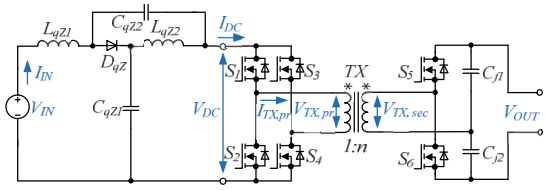

Fig. 7. Modified qZSC with a synchronous VDR.

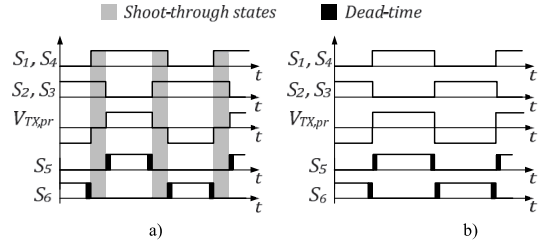

Fig. 8. Control principle of the qZS DC-DC converter with a synchronous VDR in: a) the boost mode, and b) the normal mode.

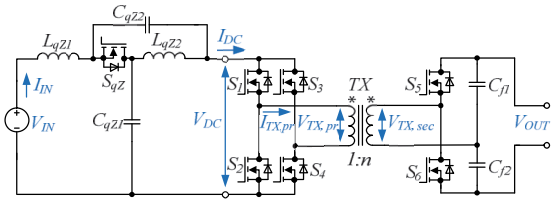

Fig. 9. Full-synchronous qZSC.

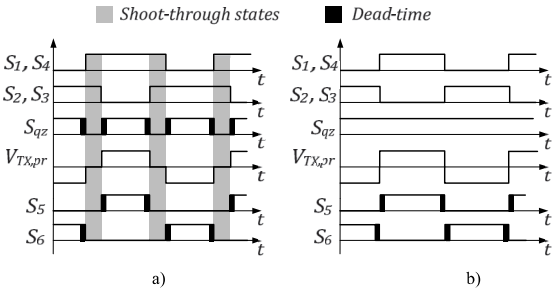

Fig. 10. Control principle of the full-synchronous qZSC in: a) the boost mode, and b) the normal mode.

IV. Experimental Results and Discussion

In this section results of our experimental study of three topological variations of the baseline qZSC are described. Specifications of all semiconductor devices used are described in Table II. First, the qZSC with the synchronous qZS network was tested. Current and voltage waveforms of the qZS MOSFET captured in the first operating point with the highest voltage step-up are shown in Fig. 11. The dead-time of 70 ns duration is evident there. This value was selected as a result of our preliminary experimental study. The measured efficiency curves for the qZSC with traditional and synchronous qZS networks are compared in Fig. 12. The converter efficiency rise is within the range from 0.9% to 1.7%, depending on the operating point.

A set of measurements similar those above was performed for the second topological variation, which contains the

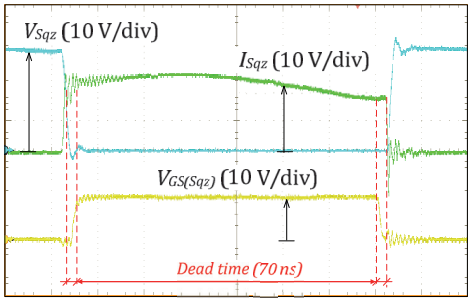

Fig. 11. Voltage and current waveforms of gating voltage, drain current and drain-source voltage of the MOSFET S_{qZ} captured in the test point with maximum shoot-through duty cycle.

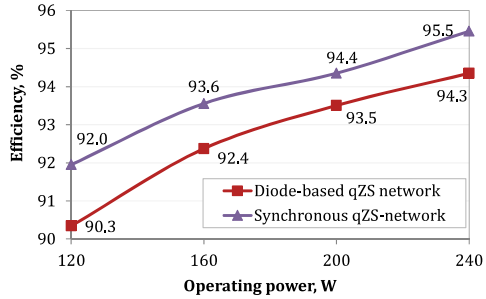

Fig. 12. Comparison of efficiencies measured in the case study qZSC with the diode-based and the synchronous qZS networks.

synchronous VDR. Voltage and current waveforms of the VDR MOSFET S_5 are shown in Fig. 13 for the normal mode. Hard turn-on of the switch, which results in very low efficiency rise is evident. Fig. 14 shows that the efficiency measured is up to 0.5% higher than that of the baseline converter, without consideration of driving losses.

Finally, the efficiency curve of the full-synchronous qZSC was obtained experimentally and compared with that of the baseline diode-based topology (Fig. 15). The cumulative efficiency rise is within the range from 1.1% to 1.9%, which is close to the efficiency rise by 2% predicted in [7].

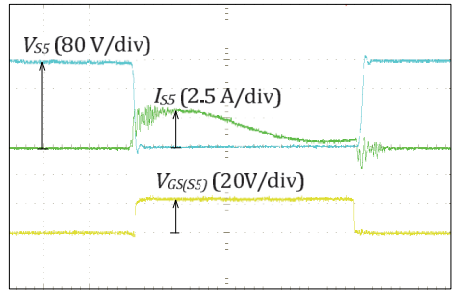

Fig. 13. Voltage and current waveforms of gating voltage, drain current and drain-source voltage of the MOSFET S_5 captured in the normal mode.

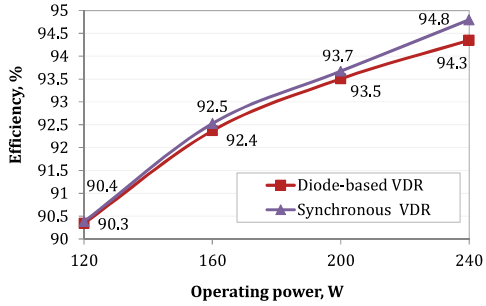

Fig. 14. Comparison of measured efficiencies of the case study qZSC with the diode-based and the synchronous VDRs.

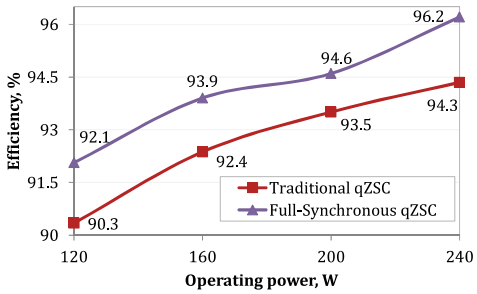

Fig. 15. Comparison of measured efficiencies of the full-synchronous and the traditional qZSC.

From the experimental results presented in this section it is evident that synchronous rectification can improve the efficiency of the case study qZSC by up to 2%. However, losses in the control system and driving were not taken into account in the efficiency measured. It means that 0.5% efficiency rise, i.e. 1.2 W in the given case obtained with the synchronous VDR can be easily suppressed by the driving losses of two high-voltage SiC MOSFETs. From a practical point of view, only qZSC with the synchronous qZS network seems to be an attractive solution if the driving losses and the cost of realization are taken into account, while bidirectional power transfer is not required.

V. Conclusions

Focus in this paper was on the efficiency improvement of the galvanically isolated quasi-Z-source full-bridge DC-DC converter through the realization of synchronous rectification. The study was performed for four operating points typical for photovoltaic applications. Our simulation study showed that in the given case, semiconductor power losses contain virtually only conduction losses. Moreover, conduction losses in the diodes contribute around 80% of the semiconductor losses in all operating points, while they can be easily reduced if diodes are replaced with N-channel MOSFETs. Three possible ways to realize synchronous rectification were studied: synchronous qZS network, synchronous VDR, and full-synchronous qZSC.

Efficiency curves were measured experimentally for the three topological variations proposed and compared with the baseline topology. It is shown that all topological variations provide a rise in efficiency. However, the measurements did not take into account the power required for driving additional MOSFETs, which can also involve power losses. Thus, the qZSC with the synchronous qZS network was found to provide best performance at the lowest cost if the driving losses are considered. Therefore, it will be advantageous as a high-performance photovoltaic module integrated converter.

Acknowledgements

This research work was financed by Estonian Ministry of Education and Research (project SF0140016s11). Latvian partner research work has been supported by Latvian Council of Science (Grant 416/2012). The authors are also thankful to Ubik Solutions llc. for financial support of this study.

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[PAPER-XI] Vinnikov, D.; Chub, A.; **Liivik. L**. Asymmetrical Quasi-Z-Source Half-Bridge DC-DC Converters. *9th International Conference on Compatibility and Power Electronics. (CPE)*, Lisbon, Portugal, 24-25 June, 2015 pp. 1-4.

Asymmetrical Quasi-Z-Source Half-Bridge DC-DC Converters

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***Abstract*— This paper presents a novel quasi-Z-source half-bridge DC-DC converter family derived by a combination of the single-switch qZS DC-DC converter and the half-bridge galvanically isolated DC-DC converter. The novel topologies have only two active switches and are a cheaper alternative to the galvanically isolated quasi-Z-source DC-DC converters with a full-bridge switching stage. Such promising features as circuit simplicity, low cost, high efficiency, and high reliability are attributed to the new alternative solution. A 200W prototype was assembled and tested. Simulation and experimental results are presented to verify the step-up performance of the topology.**

Keywords*— *impedance-source converters, DC-DC power converters, galvanic isolation, renewable energy sources

I. INTRODUCTION

The quasi-Z-source (qZS) full-bridge DC-DC converter (Fig. 1) is a new emerged topology of the galvanically isolated step-up DC-DC converters [1]. Its specific properties, such as continuous input current, wide input voltage and load regulation range, increased reliability and inherent soft-switching properties, have contributed to the popularity of the topology in the renewable energy applications as power conditioners for the fuel cells [2], PV panels [3] and residential wind turbines [4]. Since its appearance in 2009, increasing research efforts in the field of qZS DC-DC converters have been made. New approaches, such as cascaded qZS-network [5], advanced shoot-through control methods [6], synchronous rectification [7], and resonant power conversion [8], are targeting improved step-up performance and efficiency of the baseline topology. Moreover, two new topologies of the magnetically coupled qZS DC-DC converters with reduced number of switches were developed: the qZS push-pull converter [9] and the symmetrical qZS half-bridge DC-DC converter [3] (see Fig. 1). Both topologies have two transistors in their switching stage, which leads to reduced complexity of the switching stage and its simpler control.

In contrast to the push-pull counterpart, the symmetrical qZS half-bridge DC-DC converter features twice reduced voltage stress of the transistors and a two-winding isolation transformer. In addition, the converter could be supplied either from one or two input voltage sources. However, to ensure the symmetrical structure of the impedance source network, mirror connection of two identical qZS networks is required. That seems to be the main drawback of the symmetrical qZS half-bridge DC-DC converter since it uses twice more passive components and is more costly and less efficient than the traditional full-bridge qZS DC-DC converter.

This paper proposes an asymmetrical qZS half-bridge DC-DC converter with its experimental validation. The novel topology was derived by the combination of the single-switch qZS DC-DC converter and the half-bridge galvanically isolated DC-DC converter. The structure of this topology is simpler than that of the symmetrical qZS half-bridge DC-DC converter since it is based on a single qZS network.

II. ASYMMETRICAL QUASI-Z-SOURCE HALF-BRIDGE DC-DC CONVERTER

A. General description

The proposed step-up DC-DC converter has the qZS network, two switches and two capacitors on the low-voltage input side, a step-up isolation transformer and a Voltage Doubler Rectifier (VDR) on the high-voltage output side (Fig. 2*a*).

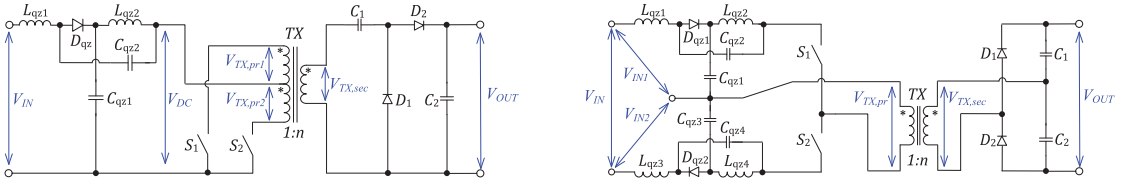

Fig. 1. State-of-the-art qZS galvanically isolated DC-DC converters with reduced switch count: qZS push-pull DC-DC converter (a) and symmetrical qZS half-bridge DC-DC converter (b).

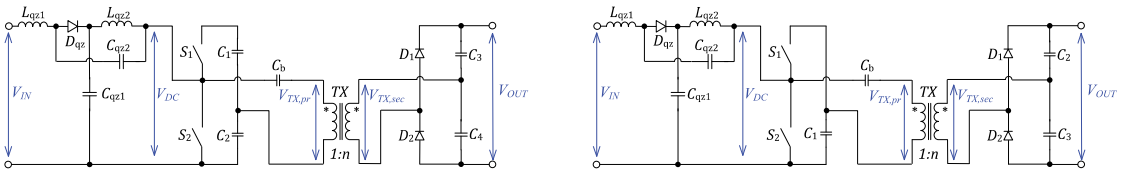

Fig. 2. New asymmetrical qZS half-bridge DC-DC converters: with two (a) and single (b) capacitor in the half-bridge switching stage.

The qZS network is composed from two inductors (L_{qz1} and L_{qz2}), two capacitors (C_{qz1} and C_{qz2}), and a diode (D_{qz}). To prevent the saturation of the isolation transformer *TX*, DC blocking capacitor C_b is added in series with the primary winding of the isolation transformer.

B. Generalized Operating Principle

In the proposed topology (Fig. 2*a*), the high-side (S_1) and the low-side (S_2) switches of the half-bridge inverter are driven complimentary without dead time (Fig. 3).

In the converter, the switch S_2 performs shoot-through for DC voltage gain regulation similarly to other qZS derived topologies [10], therefore the amplitude value of the intermediate DC-link voltage V_{DC} could be represented as

$$V_{DC} = \frac{V_{IN}}{1-2\cdot d_2} = B\cdot V_{IN}, \qquad (1)$$

where V_{IN} is the input voltage of the converter, d_2 is the duty cycle of S_2 and B is the input voltage boost factor (B=1/(1-2·d_2)). The half-bridge capacitors C_1 and C_2 are

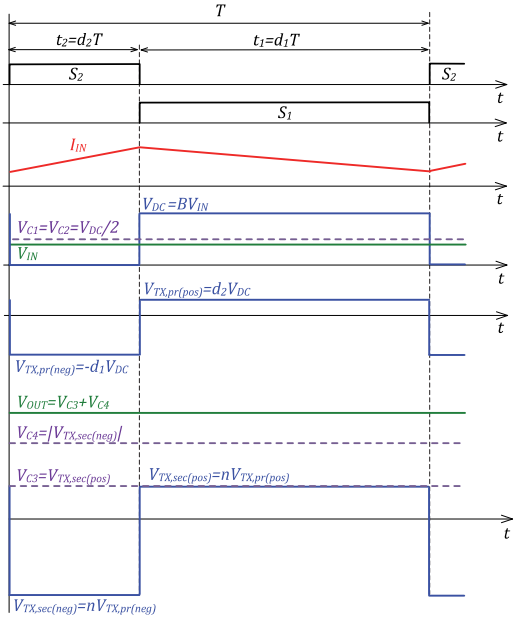

Fig. 3. Control principle and idealized operating waveforms of the proposed converter.

equally charged to half of the V_{DC} value each. The energy is transferred through the isolation transformer *TX* by the asymmetrical pulses, which leads to unequal voltages across the VDR capacitors C_3 and C_4 (Fig. 3). The output voltage of the proposed topology is directly regulated by the variation of the duty cycle of S_2:

$$V_{OUT} = \frac{V_{IN}\cdot n}{1-2\cdot d_2}, \qquad (2)$$

where n is the turns ratio of the isolation transformer.

If inductors L_{qz1} and L_{qz2} are properly dimensioned [11], the qZS network will maintain the continuous input current, thus reducing the stress of the input voltage source. As compared to the galvanically isolated qZS DC-DC converter with the full-bridge switching stage [1], the proposed converter has only one shoot-through state per switching period. Therefore, the qZS-network operates with the frequency equal to the switching frequency and its passive components have double values as compared to those of the full-bridge counterpart.

C. Topology Modification Possibility

The proposed asymmetrical half-bridge topology could be simplified further by the reconfiguration of the switching stage. In that case, the upper capacitor of the half-bridge switching stage should be short-circuited, as shown in Fig. 2*b*. The general operating principle of the modified topology remains the same. Minimization of components count will lead to higher voltage stress of the primary side capacitors. Capacitor C_1 should be dimensioned for the operating voltage equal to the amplitude value of the intermediate DC-link voltage V_{DC}. The blocking capacitor C_b needs to withstand higher DC voltage because the half-bridge switching stage supplies the transformer with unipolar voltage pulses in contrast to bipolar in the previous topology.

III. Simulation and Experimental Study

To verify the step-up performance of the proposed topology, the numerical simulations were performed in the PSIM environment. Generalized simulation parameters are presented in Table I. Fig. 4 shows that the converter ensures the demanded gain of the input voltage (V_{IN} = 25 V and V_{DC} = 62 V) and continuous input current with peak-to-peak ripple of 6 A. The amplitude voltage values of the positive and negative cycles of the isolation transformer's primary winding can be calculated as follows:

$$V_{TX,pr(pos)} = d_2V_{DC} \approx 19V, \quad V_{TX,pr(neg)} = -((1-d_2)V_{DC}) \approx -43V. \qquad (3)$$

TABLE I
SIMULATION PARAMETERS OF THE QZS HALF-BRIDGE DC-DC CONVERTER

Parameter	Symbol	Value
Input voltage, V	V_{IN}	25
Average input current, A	I_{IN}	8
Output voltage, V	V_{OUT}	240
Duty cycle of S_2 (shoot-through duty cycle)	d_2	0.3
Switching frequency, kHz	f_{sw}	100
Transformer turns ratio	n	4
Capacitance of qZS capacitors, µF	C_{qz1}, C_{qz2}	26.4
Inductance of qZS inductors, µH	L_{qz1}, L_{qz2}	23
Capacitance of half-bridge capacitors, µF	C_1, C_2	100
Capacitance of the DC blocking capacitor, µF	C_b	5.5
Capacitance of VDR capacitors, µF	C_3, C_4	2.2

As it was previously predicted, the VDR capacitors are charged to different voltages, which could be estimated by

$$V_{C3} = d_2 V_{DC} n \approx 76V\,, \quad V_{C4} = (1-d_2) V_{DC} n \approx 172V\,. \qquad (4)$$

Finally, the output voltage is the sum of the voltages of C_3 and C_4, which properly matches the theoretical prediction. The simulation results show the sine wave current of the primary winding of the isolation transformer. This effect is caused by the series resonant circuit formed by the DC blocking capacitor C_b and primary winding leakage inductance of the isolation transformer. By proper utilization of those elements the soft switching could be achieved for the half-bridge inverter switches.

To validate the proposed topology, the 200 W prototype converter was assembled in accordance with the schematic in Fig. 2*a* and technical specifications in Tables I and II.

TABLE II
GENERAL SPECIFICATIONS OF SEMICONDUCTORS USED IN THE EXPERIMENT

Component	Type	Specifications
S_1, S_2	Vishay Si4190ADY	V_{DS}=100 V; $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, Q_g=20.7 nC, R_g=2.2 Ω
D_{qz}	Vishay V60D100C	V_{RRM}=100 V; V_F=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_1, D_2	CREE C3D02060E	V_{RRM}=600 V; V_F=1.8 V $I_{F(AV)}$=4 A

The qZS network was built on low-profile SMD inductors Vishay IHLP-6767GZ (two 47 uH inductors in parallel for each qZS inductor). The isolation transformer was wound on the ETD34 core made from ferrite N87 and its leakage inductance referred to the primary was 0.35 µH. Chip multilayer ceramic capacitors SMD1210 2.2 µF 100 V from Murata were used to assemble the qZS network and the voltage doubler rectifier (12 units connected in series for each qZS capacitor and 9 units connected in 3x3 matrix configuration for the VDR capacitors).

As seen from Fig. 5, the experimental waveforms are matching the theoretical predictions and the simulation study. The topology features the demanded step-up performance, continuous input current and sine wave current of the primary winding of the isolation transformer. Due to losses in components, the converter has slightly lower DC voltage gain which was also influenced by the leakage inductance of the isolation transformer. Measured voltage across VDR capacitors was 70 V and 155 V in contrast to 76 V and 172 V estimated in (3).

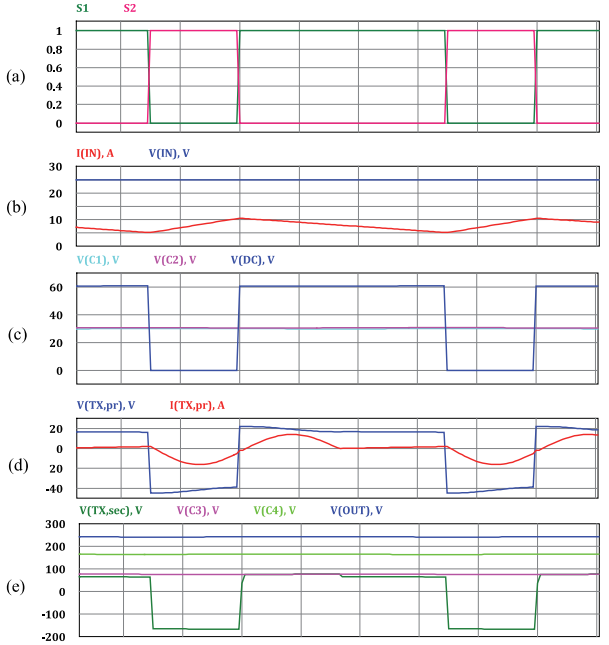

Fig. 4. Simulation results of the proposed topology: gating signals of switches (a), input voltage and current (b), voltages of half-bridge capacitors and intermediate DC-link voltage (c), voltage and current of the primary winding (d) and secondary winding voltage, voltages of VDR capacitors and output voltage of the converter (e).

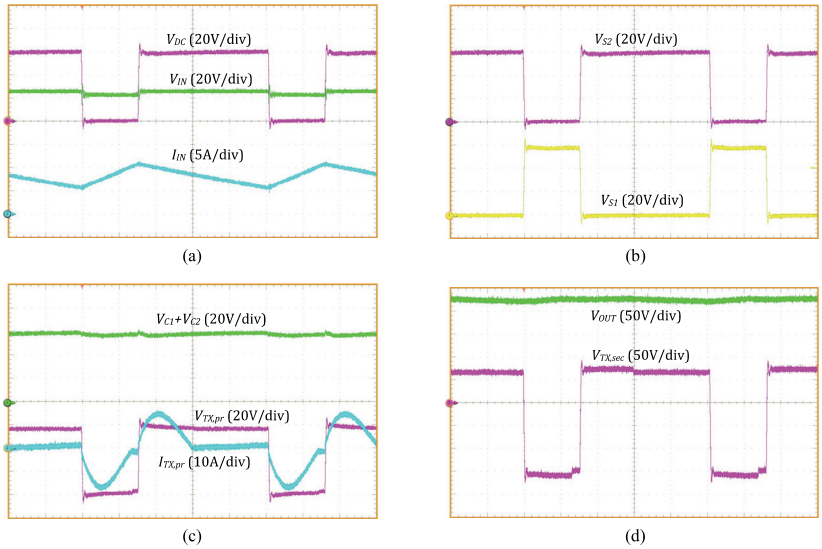

Fig. 5. Experimental waveforms of the proposed topology: input voltage, input current and intermediate DC-link voltage (a), operating voltages of switces (b), summarized voltage of the half-bridge capacitors, voltage and current of the primary winding (c) and secondary winding voltage and output voltage of the converter (d).

IV. Conclusions and Future Work

This paper proposed a novel galvanically isolated asymmetrical qZS half-bridge DC-DC converter, a new member of the galvanically isolated impedance source DC-DC converter family. It was derived by the combination of the single-switch qZS DC-DC converter and the half-bridge galvanically isolated DC-DC converter. The converter features simple control due to reduced switch count and continuous input current in the CCM operation. If properly realized, the series resonant circuit formed by the DC blocking capacitor and primary winding leakage inductance of the isolation transformer will result in the soft switching of the half-bridge inverter switches.

To validate the proposed topology, the experimental prototype with a rated power of 200 W was assembled and tested. Experimental results have verified all the theoretical assumptions and computer simulations. Voltage stresses of the capacitors and transistors all conformed to the theoretical predictions.

Further research will be directed towards the analysis of the resonant switching processes and resulting soft switching performance of the proposed converter.

Acknowledgment

This research work was financed by Estonian Ministry of Education and Research (project SF0140016s11) and supported by the Estonian Research Council (grant PUT744).

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