TAL TECH

DOCTORAL THESIS

Universal Galvanically Isolated DC-DC Converters with Topology Morphing Control

Vadim Sidorov

TALLINNA TEHNIKAÜLIKOOL
TALLINN UNIVERSITY OF TECHNOLOGY
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Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for doctoral or equivalent academic degree.

Vadim Sidorov

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VADIM SIDOROV

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Contents

List of Publications

A list of the author's publications, on the basis of which the thesis has been prepared:

I V. Sidorov, A. Chub, D. Vinnikov and F. Z. Peng, "Survey of Topology Morphing Control Techniques for Performance Enhancement of Galvanically Isolated DC-DC Converters," in *IEEE Open Journal of the Industrial Electronics Society*, vol. 3, pp. 751-777, 2022, DOI: 10.1109/OJIES.2022.3225265.

II V. Sidorov, A. Chub, D. Vinnikov and A. Bakeer, "An Overview and Comprehensive Comparative Evaluation of Constant-Frequency Voltage Buck Control Methods for Series Resonant DC–DC Converters," in *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, pp. 65-79, 2021, DOI: 10.1109/OJIES.2020.3048003.

III V. Sidorov, A. Chub and D. Vinnikov, "Topology Morphing Control with Soft Transients for Multimode Series Resonant DC-DC Converter," *2021 IEEE 22nd International Conference of Young Professionals in Electron Devices and Materials (EDM)*, 2021, pp. 331-336, DOI: 10.1109/EDM52169.2021.9507621.

IV S. Rahman, V. Sidorov, A. Chub and D. Vinnikov, "High-Frequency Split-Bobbin Transformer Design with Adjustable Leakage Inductance," *2021 IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, 2021, pp. 1-5, DOI: 10.1109/RTUCON53541.2021.9711708.

V V. Sidorov, A. Chub and D. Vinnikov, "Bidirectional Isolated Hexamode DC–DC Converter," in *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12264-12278, Oct. 2022, DOI: 10.1109/TPEL.2022.3170229.

VI V. Sidorov, A. Chub, D. Vinnikov and A. Lindvest, "Novel Universal Power Electronic Interface for Integration of PV Modules and Battery Energy Storages in Residential DC Microgrids," in *IEEE Access*, vol. 11, pp. 30845-30858, 2023, DOI: 10.1109/ACCESS.2023.3260640.

VII V. Sidorov, A. Chub and D. Vinnikov, "Input Source Identification Algorithm For Isolated Buck-Boost DC-DC Converter," *2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2022, pp. 1-6, DOI: 10.1109/COMPEL53829.2022.9829973.

Author's Contribution to the Publications

The author's contributions to the papers in this thesis are:

I Vadim Sidorov, as the first author of the paper, was responsible for the literature analysis, the collection and classification of topology morphing techniques, and the writing. Vadim Sidorov took part in the review and editing of the paper.

II Vadim Sidorov, as the first author, developed the methodology for the calculation of power losses in the dc-dc converter. He has experimentally validated the proposed methodology and compared the buck fixed-frequency control modulations for the series resonant converter. He was responsible for submission and contact with editors during peer-reviewing rounds.

III Vadim Sidorov, as the first author, developed the algorithm for soft transition between topology configurations. Vadim Sidorov was responsible for developing a closed-loop control system, obtaining experimental results, and writing a draft. He presented the paper at the IEEE 22nd International Conference of Young Professionals in Electron Devices and Materials (EDM) 2021.

IV Vadim Sidorov, as a co-author, has proposed and designed the transformer with the adjusted leakage inductance based on the hybrid split bobbin. Vadim Sidorov presented the paper at the IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON) 2021.

V Vadim Sidorov, as the first author of the paper, was responsible for the implementation of control modulations, experimental tests, theoretical and experimental waveforms, thermal analysis of a prototype, and writing. He was responsible for submission and contact with editors during the peer-review process.

VI Vadim Sidorov, as the first author of the paper, provided experimental verification of the high-efficiency universal power electronic interface for seamless integration of PV modules and battery energy storages into residential dc microgrids. He has developed a universal closed-loop control system providing a global maximum power point tracking of different PV modules and the droop control for charging/discharging different battery types. Vadim Sidorov was responsible for the writing and took part in the review and editing of the paper.

VII Vadim Sidorov, as the first author of the paper, was responsible for the algorithm development for the identification of input sources, its experimental stage, and writing the paper draft. Vadim presented the paper at the IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL) 2022.

Abbreviations

1.5xVM	1.5-Times Voltage Multiplier
ADC	Analog-to-Digital Converter
APWM	Asymmetrical Pulse-Width Modulation
A-TL	Active Three-Level
COMPx	Comparator X
DC or dc	Direct Current
DAB	Dual Active Bridge
DFBI	Double Full-Bridge Inverter
EMI	Electro-Magnetic Interference
FBI	Full-Bridge Inverter
FBR	Full-Bridge Rectifier
GaN	Gallium Nitride
HV	Half-Voltage
H-TLI	Hybrid Three-Level Inverter
H-TL FBI	Hybrid Three-Level Full-Bridge Inverter
GMPP	Global Maximum Power Point
GMPPT	Global Maximum Power Point Tracking
HBR	Half-Bridge Rectifier
HBI	Half-Bridge Inverter
HV FBI	Half-Voltage Full-Bridge Inverter
HRTIM	High-Resolution Timer.
HPWM	Hybrid Pulse-Width Modulation
HPSM	Hybrid Phase-Shift Modulation
IBBC	Isolated Buck-Boost converter
IHMC	Isolated Hexa-Mode Converter
ISPWM	Improved Shifted Pulse-Width Modulation
LLC	LLC Resonant Converter
LMPP	Local Maximum Power Point
MPP	Maximum Power Point
NOCT	Nominal Operating Cell Temperature
OLM	Overlap Modulation
PWM	Pulse-Width Modulation
PSM	Phase-Shift Modulation
PWM	Pulse-Width Modulation
PV	Photovoltaic
PCB	Printed Circuit Board
QBI	Quarter Bridge Inverter
RMS	Root Mean Square
SAR	Semi-Active Rectifier
SiC	Silicon Carbide

SOA	Safe Operating Area
SoC	State of Charge
SoH	State of Health
SPWM	Shifted Pulse-Width Modulation
SRC	Series Resonant Converter
SRIBBC	Series Resonant Isolated Buck-Boost Converter
SSCB	Solid-State Circuit Breaker
SSI	Single-Switch Inverter
SSR	Single-Switch Rectifier
TL	Three-Level
TLI	Three-Level Inverter
TMC	Topology Morphing Control
TQBI	Three-Quarter Bridge Inverter
UPEI	Universal Power Electronic Interface
VDR	Voltage-Doubler Rectifier
VFR	Voltage-Fivefolder Rectifier
VQR	Voltage-Quadrupler Rectifier
VSR	Voltage-Sixfolder Rectifier
VTR	Voltage-Tripler Rectifier
ZCS	Zero-Current Switching
ZVS	Zero-Voltage Switching

Symbols

G	Dc voltage gain of a dc-dc converter
G_{FE}	Voltage gain of a front-end inverter in a dc-dc converter
G_{BE}	Voltage gain of a back-end rectifier in a dc-dc converter
G_{TX} , n	Turns ratio of an isolating transformer
$V_{FE(pk-pk)}$	Peak-to-peak voltage applied to a transformer
$V_{BE(pk-pk)}$	Peak-to-peak voltage fed by a transformer
V_{in}	Input voltage
V_{out}	Output voltage
I_{in}	Input current
I_{out}	Output current
L_{lk}	Leakage inductance of an isolating transformer
L_m	Magnetizing inductance of an isolating transformer
C_x	Capacitor
TX	Isolation transformer
G_n	Normalized dc voltage gain of a dc-dc converter
ω_r	Angular resonant frequency of the resonant tank
f_r	Resonant frequency of the resonant tank
f_{sw}	Switching frequency
V_{HV}	Voltage in high-voltage side
V_{LV}	Voltage in low-voltage side
I_{HV}	Current in high-voltage side
I_{LV}	Current in low-voltage side
C_r	Equivalent resonant capacitance
B_{max}	The maximum flux density of a transformer
A_e	Effective core area
N_{pr}	Number of turns of the primary winding
N_{sec}	Number of turns of the secondary winding
T_D	Dead time
ΔV_{Cx}	Peak-to-peak voltage ripple of a capacitor C_X
$V_{CX(max)}$	Maximum voltage stress of a capacitor C_X
$R_{\theta JA}$	Thermal resistance of a transistor from a junction to ambient
T_J	Temperature of MOSFET junction
$T_{J(max)}$	Maximum temperature of MOSFET junction
D	Duty cycle
D_{bk}	Duty cycle of buck modulations
D_{bt}	Duty cycle of boost modulations
D_{am}	Duty cycle of the soft transition algorithm
ΔD	Step of duty cycle
V_{LVMIN}	Minimum operation voltage
$V_{LV(ref)}$	Reference voltage at the low-voltage side

$V_{LV(OC)}$	Open-circuit voltage
ΔV_{LV}	Differential voltage of a connected input source
ΔI_{LV}	Differential current of a connected input source
$\Delta I_{LV}/\Delta V_{LV}$	Differential conductance of a connected input source
I-V	Current-voltage curve
t_{scan}	Scanning time
t_{returm}	Return time
$P_{LV(ref)}$	Reference power at the low-voltage side

1 Introduction

1.1 Background

The European Commission has set the Energy Directive to at least a 55% reduction in greenhouse gas emissions and a 40% increase in the use of renewable energy sources in buildings by 2030 [1]. As reports show, residential and commercial buildings contribute close to 40% of the total energy consumption in the European Union and the U.S.A. [2]. This constantly expanding sector is bound to increase its energy consumption and carbon footprint [3].

One of the solutions for achieving these targets is to install photovoltaic (PV) systems in residential buildings. As reports show, the annual growth rate of new grid-connected PV systems worldwide has increased from 30 GW/year in 2012 to over 175 GW/year in 2021 [4], [5]. This trend is primarily associated with the proliferation of utility-scale and residential PV systems, which showed an increase in their cumulative installed capacity of 19% and 41%, respectively, in 2021 [6]. According to the forecasts, the distributed solar PV capacity can reach over 530 GW by 2024 [7].

On the other hand, using a dc microgrid instead of the utility ac grid can save more than 11% of energy consumption in residential or small-commercial buildings [8], [9]. This results from PV modules and battery energy storage being naturally dc energy sources. Moreover, many consumer electronic devices and home appliances are inherently dc loads or feature an intermediate dc bus, such as chargers for phones or laptops, TVs, LED lighting, etc. In this case, dc microgrids prevent unnecessary double energy conversion (dc-to-ac and ac-to-dc) between energy sources and loads. At the same time, dc microgrids also provide the opportunity to integrate battery energy storage directly without transforming energy into ac. A battery energy storage is required in energy-efficient buildings to maximize self-consumption.

An example of a residential power system based on the dc microgrid is shown in Figure 1.1. The dc microgrid consists of the centralized dc bus, an interface inverter for connecting to the utility grid, distributed energy sources, and storages. The centralized inverter operates as a master for voltage regulation in the dc microgrid. A nominal voltage of 350 V is considered based on the Dutch national practical guidelines NPR 9090 [10] – the available recommendations for dc buildings in the EU.

1.2 Motivation of the Thesis

Front-end dc-dc converters are required for interfacing PV modules and batteries into dc microgrids. However, manufacturing various specific front-end converters for each type of energy source increases the cost of the final products. In addition, handling different stock-keeping unit types could cause mistakes in installation, creating additional expenses for system installers and integrators. In applications requiring many converter types, the industry found it more practical to use universal converters to alleviate these issues. One of the best industrial examples is the railway dc-dc converters delivering an 18:1 dc voltage regulation range to cover voltage ranges defined in the EN50155 standard. Typically, such a converter would be built with two-stage energy conversion.

This thesis embraces the trend toward the universalization of power electronic converters by extending their input/output voltage range. Single-stage energy conversion is considered the desired approach, especially for cost-sensitive applications such as residential power generation.

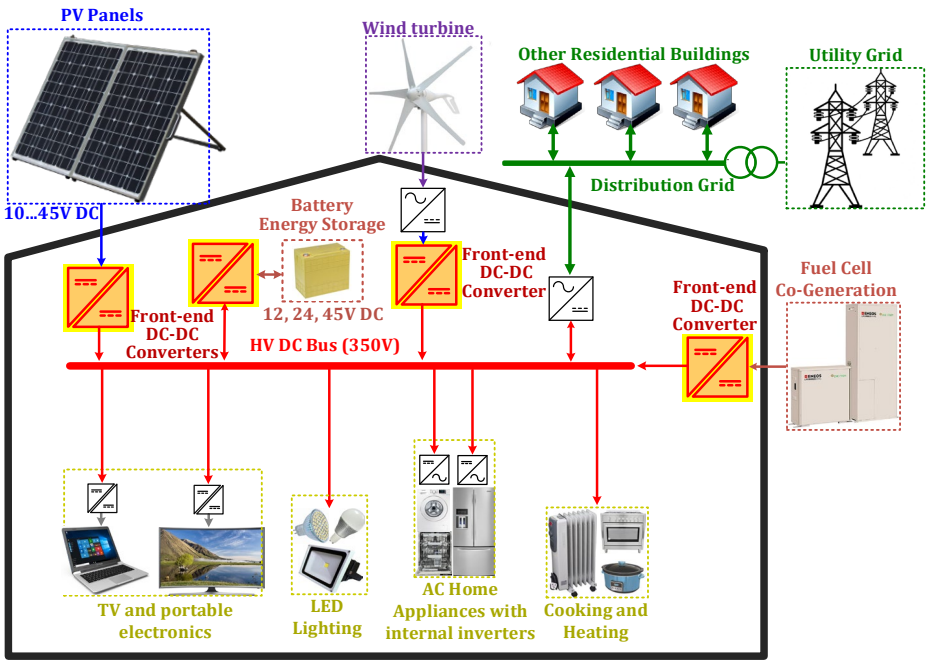


Figure 1.1. Residential power system based on the 350 V dc microgrid.

This thesis proposes the concept of a universal front-end dc-dc converter for connecting a PV module or a low-voltage battery energy storage to the dc microgrid operating at a much higher voltage. Compatibility with various energy source types implies flexible control of the converter. The thesis aims to develop a concept of a universal power electronic interface (UPEI) for residential dc microgrid applications with single-stage energy conversion and flexible control. The selected application of the developed technology is timely considering the forthcoming uptake of energy-efficient dc houses and supports circular economy principles.

To provide the possibility of connecting various PV modules and battery types, the UPEI as a converter should operate in the wide input voltage range from 10 up to 60 V, in the range of output voltage from 320 to 380 V. In addition, the UPEI should provide galvanic isolation to ensure the safety of users. Considering the typical parameters of residential PV modules and low-voltage batteries on the market, the input voltage range of 10 to 60 V could be justified using Figure 1.2. Under opaque or partial shading conditions, the global maximum power point (GMMP) of a PV module could appear at lower voltages due to the utilization of three bypass diodes in its junction box. Therefore, each type of PV module features three possible operating input voltage ranges. At the same time, the output voltage of batteries varies in a relatively wide range depending on temperature, state of charge (SoC), state of health (SoH), etc.

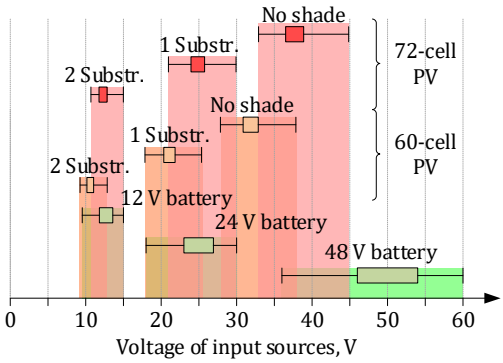


Figure 1.2. Voltage ranges of low-voltage energy sources used in residential applications.

The control system of the UPEI should include a global maximum power tracking (GMPPT) algorithm for harvesting maximum energy from a PV module under any conditions. In the case of operation with a battery, the control system should implement a SoC estimation algorithm. At the same time, the UPEI should apply the droop control for operating in parallel with other sources and devices to share energy in an autonomous dc microgrid [11]. This algorithm has gained popularity for enabling energy sharing between parallel converters by regulating the output power of each converter depending on the dc bus voltage without communications. Ultimately, the universal front-end converter should be capable of identification of the input energy source type. Thus, the UPEI includes functions of different isolated dc-dc converters, as shown in Fig. 1.3.

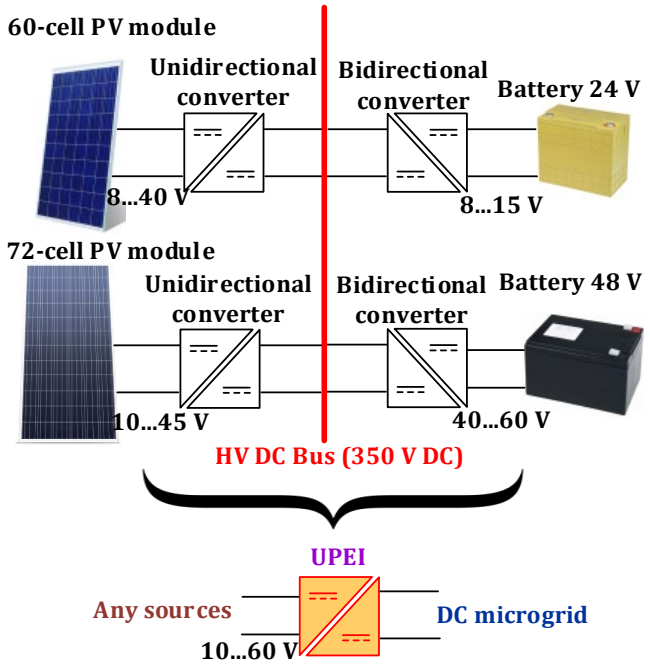


Figure 1.3. Concept of the universal front-end interface converter for residential dc microgrids.

This thesis was conducted according to one of the research directions of the Power Electronics Group of Tallinn University of Technology. The aim is to gather knowledge on single-stage galvanically isolated dc-dc converters with a wide regulation range and develop a universal power electronics interface for connecting a PV module or a low-voltage battery energy storage to a dc microgrid. The Estonian Research Council supported the current work under the following grant and projects: PSG206 "DC-DC Converters with Ultra-Wide Regulation Range and Post-Fault Operation Capability," EAG9 "Universal photovoltaic-to-microgrid interface (UniPV2μG)," and PRG1086 "Future-Proof Power Electronic Systems for Residential Microgrids." The research results obtained were the converter into FlexiVerter® technology within the LEEEE20047 "Flexible Power Electronic Interface for DC Grid Integration of Residential Photovoltaic and Battery Energy Storage Systems (FPEI)" co-funded by Ubik Solutions OÜ and the Estonian Research Council.

1.3 Aim, Hypotheses, and Research Tasks

The main aim of the Ph.D. research project is to develop galvanically isolated dc-dc converters with a wide input voltage range and experimentally validate a concept of a universal power electronic interface compatible with different types of PV modules and batteries for the fast deployment of dc microgrids. The topology morphing control (TMC) is identified as a powerful tool for performance enhancement of power electronics converters needed for UPEI realization. The developed technology will facilitate the mass adoption of droop-controlled dc microgrids in residential and small-business buildings. The author set the goal of obtaining acceptable efficiency of the universal interface dc-dc converter with any type of input energy source. The outcome of this work is to develop and launch TRL 4 prototype in a dc microgrid.

Hypotheses:

1. Series resonant isolated buck-boost converters (SRIBBCs) based on hybrid H-bridge switching cells with series capacitors could be used as a universal tool for uni- and bi-directional applications without hardware modifications.
2. Symmetrical and asymmetrical control modulations could provide the highest efficiency in full-bridge and half-bridge SRIBBCs, respectively, reducing power losses by up to 20%.
3. Application of topology morphing control (TMC) with hybrid switching cell based SRIBBC could allow for dc voltage gain range extension from 1:3 to at least 1:6.
4. An isolation transformer design with a partially overlapping split bobbin could achieve minimum power loss for a given dc regulation range by embedding the optimal resonant inductance value with 10% tolerance.
5. Universal converters based on SRIBBC with TMC could identify input source type by observing its differential conductance while avoiding sizable input current and voltage distortions.

Research tasks:

1. To review and compare existing TMC techniques and application cases.
2. To synthesize power electronics interface requirements for simultaneous applicability with the most popular energy sources in the dc microgrid.
3. To develop an SRIBBC-based topology with topology morphing control, which would be compatible with different low-voltage uni- and bi-directional energy sources used in residential dc microgrids.

4. To develop an analytical model of SRIBBC for its performance optimization in uni- and bi-directional applications.
5. To synthesize a hierarchical control system architecture and control algorithms adaptable to the targeted set of different energy source types.
6. To design an experimental setup and experimental performance verification of the universal isolated dc-dc interface in residential dc microgrids.

1.4 Research Methods

The results presented in the thesis were provided by mathematical, simulation, and experimental analyses. The volt-second, amp-second, and power balances are utilized for deriving dc voltage gains of SRICCB under different buck and boost control modes. Furthermore, the volt-second and amp-second balances were applied to provide the analytical model of series resonant converters for calculating current stress in components and its power losses and optimization of the resonant inductance. The simulation of SRIBBC operation in PSIM simulation software approves the analytical model. Theoretical and simulation results were corroborated by experimental analysis of SRIBCC prototypes. The experimental analysis was carried out in the Power Electronics Research Laboratory of TalTech, using digital oscilloscopes, power quality and efficiency analyzers, power supplies, solar array and battery emulators, microprocessor development tools, PCB prototyping, assembling tools, etc.

To verify the operation of the developed converter with different PV modules and batteries in unfavorable conditions, the developed converters were tested using daily mission profiles under different solar irradiance profiles and profiles of dc microgrid voltage. MATLAB software was used for generation profiles as well as for the analysis of experimental results. Moreover, the data were also visualized in MATLAB.

1.5 Contribution and Dissemination

The results of this research have been presented via scientific publications, conferences, symposiums, doctoral schools, and presentations. During the PhD studies, the author contributed to 19 publications. Among them, nine papers were published in peer-reviewed international journals and one book chapter and have been presented at nine international IEEE conferences. The dissertation is based on seven main scientific publications, including four journal and three conference papers presented at three IEEE international conferences.

Scientific novelties:

- Comparison, collecting, systematization, categorization, and classification of the knowledge on the topology morphing control techniques for isolated dc-dc converters.
- Development of the advanced TMC technique with topology reconfiguration on both sides of the SRIBBC, resulting in eight possible operating modes with no additional components.
- Analytical model of the bidirectional SRIBBC topology for calculation of its dc voltage gain and power losses for all known control modulations.
- Method of the input source type identification by observing its differential conductance.

Practical novelties:

- Analysis of application requirements and design guidelines for the UPEI based on the bidirectional SRIBBCs with a wide input voltage range.
- Efficiency benchmark of the constant-frequency buck and boost control methods.
- Methodology for optimal sizing of the SRIBBC resonant inductance.
- The algorithm for soft transitions between SRIBBC topology configurations.
- Simple and low-cost implementation of the synchronous rectifier for the discontinuous resonant current mode of the SRIBBC.
- Development of a three-level hierarchical control algorithm for UPEI based on SRIBBC.
- Demonstration of UPEI operation with 60- and 72-cell monocrystalline Si PV modules and with 24 V and 48 V $LiFePO_4$ batteries, integrated into the 350±30 V residential dc microgrid.

1.6 Experimental Setup and Instruments

The power electronics laboratory of Tallinn University of Technology has been used for the experimental setup. Figure 1.4 shows the workplace in the lab. The following measurement equipment was used: oscilloscope Tektronix DPO7254, differential voltage probes Tektronix P5205A, AC/DC current probe Tektronix TCP0030A and PEM ultra-mini CWT015, a precision power analyzer Yokogawa WT1800, and thermal camera Fluke Ti25. ITECH IT6006C-800-25 Bi-directional Power Supplies were used for imitation of the dc microgrid and batteries. PV modules were imitated by the Solar Array Simulator Keysight E4360A.

1.7 Thesis Outline

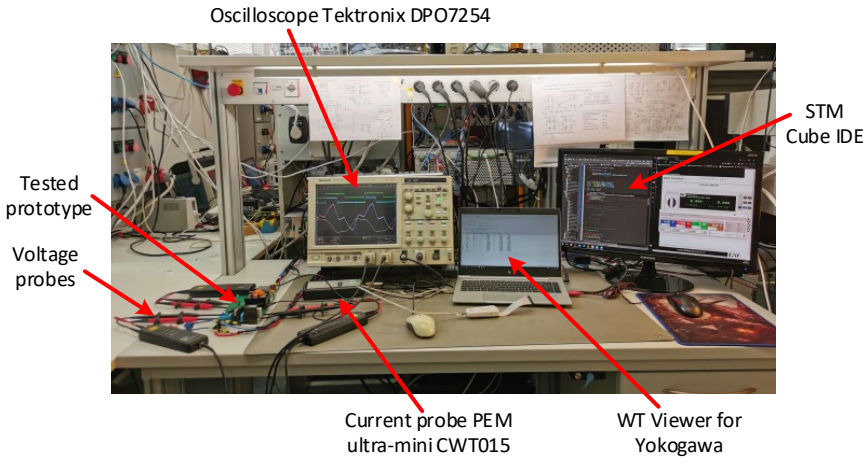
Chapter 2 focuses on the comparison, systematization, and classification of the knowledge on the TMC techniques for galvanically isolated dc-dc converters. Furthermore, the challenges of applying TMC techniques are discussed in Chapter 2.

The topology and theoretical analysis of SRIBBC are described in Chapter 3. Moreover, the algorithm for soft transition between control modes is discussed.

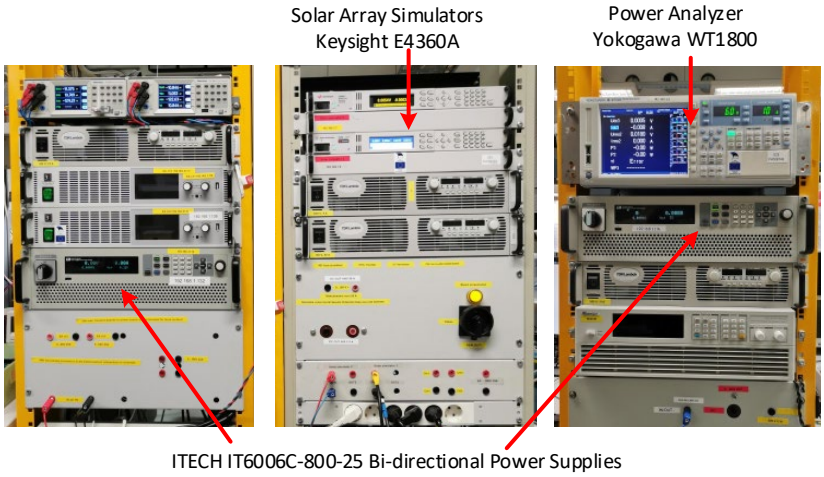
Chapter 4 describes the design guidelines for ultra-wide range bidirectional IBBC. The design of an isolation transformer with an optimal leakage inductance is presented as one of the main components in the SRIBBS.

The verification of UPIE operation with different PV modules and batteries is presented in Chapter 5.

The final chapter, Chapter 6, discusses the possibility of increasing the universality of the UPEI for the different standards of the dc microgrids.



(a)



(b)

Figure 1.4. Workplace in the Power Electronics Research Laboratory (a); main used equipment: solar array simulators, bidirectional power supplies, and precision power analyzer (b).

2 Survey of Topology Morphing Control Techniques for Galvanically Isolated DC-DC Converters

The term “topology morphing control” (TMC) in the power electronics field first appeared in 2015 [12], while some of the TMC techniques were demonstrated in 2005 [13]. The TMC is achieved by the online reconfiguration of a converter topology to extend voltage or power ranges or to provide fault tolerance without changing the hardware. It is essential to underline that TMC techniques have existed for a long time but have never been systematized.

In this study, the author focuses on the TMC techniques for galvanically isolated dc-dc converters. Typically, the generalized topology of galvanic isolated dc-dc converters consists of a front-end high-frequency inverter, an isolation transformer, and a back-end rectifier, as shown in Figure 2.1. Therefore, the dc voltage gain of the converter could be defined as [14]:

$$G = \frac{V_{out}}{V_{in}} = G_{FE} \cdot G_{TX} \cdot G_{BE}\,, \tag{1}$$

where G_{FE} is the voltage gain of the front-end inverter defined as the ratio between the peak-to-peak voltage applied to the transformer $V_{FE(pk\text{-}pk)}$ and the double of the input voltage V_{in} [14]:

$$G_{FE} = \frac{V_{FE(pk-pk)}}{2V_{in}}\,; \tag{2}$$

$G_{TX} = n$ is the turns ratio of the isolation transformer; G_{BE} is the voltage gain of the back-end rectifier defined as the ratio between the double of the output voltage V_{out} and the peak-to-peak voltage $V_{BE(pk\text{-}pk)}$ fed by the isolation transformer G [14]:

$$G_{BE} = \frac{2V_{out}}{V_{BE(pk-pk)}}\,. \tag{3}$$

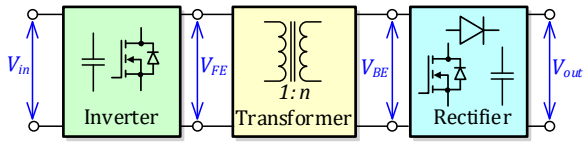


Figure 2.1. Generalized topology of a galvanically isolated dc-dc converter [Paper I].

Usually, the dc gain of a converter is constant or regulated in a narrow range. However, applying TMC in any converter stage allows for extending these values and typically changing in integer steps. The [Paper I] overviews all existing TMC techniques and provides categorization and classification of the knowledge on the TMC to create a single point of reference. According to the review, all TMC techniques can be categorized based on the stage where a converter changes its topology: at the input side and at the output side. Furthermore, there are advanced techniques that cannot be classified into these two groups (Figure 2.2). In addition, these three categories are divided into sub-categories depending on the number of modes. For example, the converter can operate in two, three, four, or six modes with different dc voltage gains.

As shown in Figure 2.2, all the techniques can be broadly referred to as one of the two main groups. First, most TMC techniques target the dc voltage regulation range extension. However, they could also be used for achieving fault-tolerance when a converter needs to recover its operation by modifying the voltage gains of the dc-dc converter parts to compensate for damaged components. On the other hand, some TMC techniques target switching power loss reduction at light load to flatten the converter efficiency curve across its input power range. To briefly cover each category of TMC techniques, a few examples of TMC techniques are shown in Subchapters 2.1, 2.2, and 2.3.

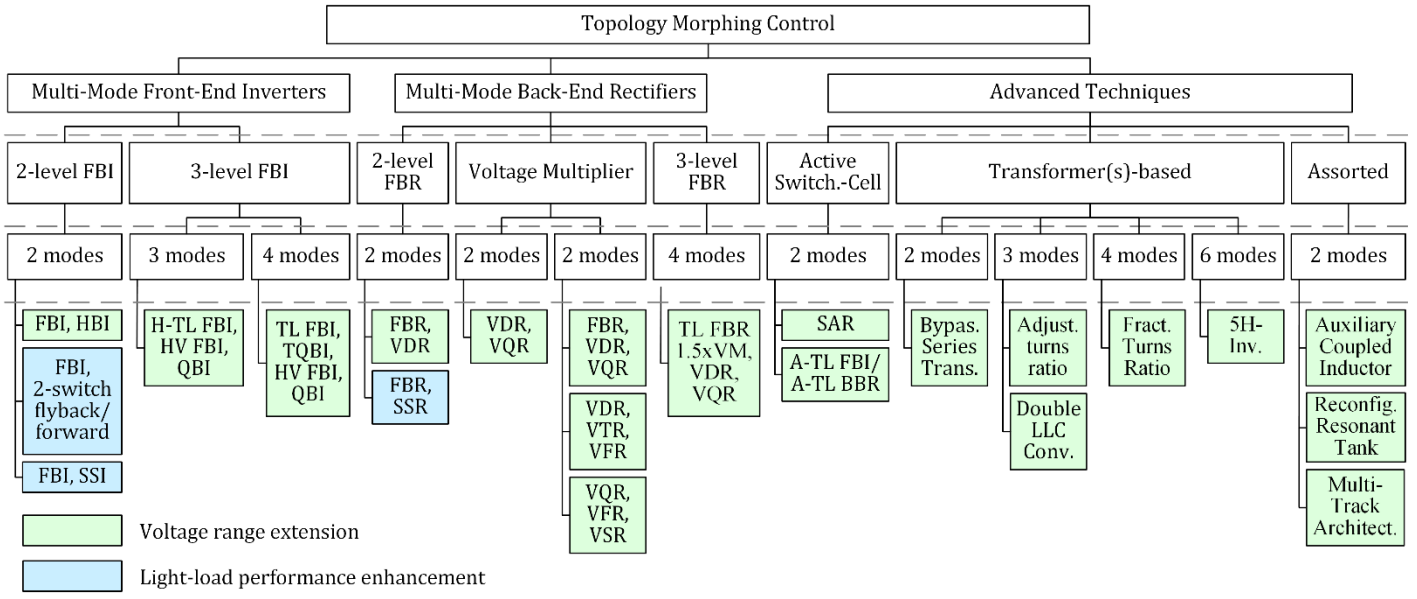


Figure 2.2. Classification of the TMC techniques [Paper I].

2.1 Input Side TMC Techniques

Many TMC techniques for the front-end inverter are aimed at decreasing the voltage gain G_{FE} in integer steps depending on the number of topology configurations. Other techniques aim to flatten the efficiency curve of a converter at a light load.

Among them, the most widespread example of the TMC for the front-end inverter of galvanically isolated dc-dc converters is the reconfiguration from a full-bridge inverter (FBI) to a half-bridge inverter (HBI). This technique can be realized by using an addition capacitor leg and an additional switch [12], [15] - [17], or a blocking capacitor C_B [18] - [21], as shown in Figure 2.3.

The second approach is suitable for LLC, CLLC, or series resonant converters (SRCs). It does not require additional components because a series blocking capacitor forms a resonant tank. In the HBI, one switch in one leg is turned on continuously, and the other one is turned off. As a result, the average voltage of the blocking capacitor C_B equals half of the input voltage. The amplitude of the inverter output voltage equals $V_{FE(pk\text{-}pk)}=\pm 0.5V_{in}$ (Figure 2.4). This TMC technique changes the voltage gain G_{FE} from 1 to 0.5 and can extend an input or output voltage range by two times.

The drawback is increasing RMS current in the series capacitor, the primary winding(s) of an isolation transformer, and the switch S_4 by √2 times. This should be taken into account in the thermal design of the converter.

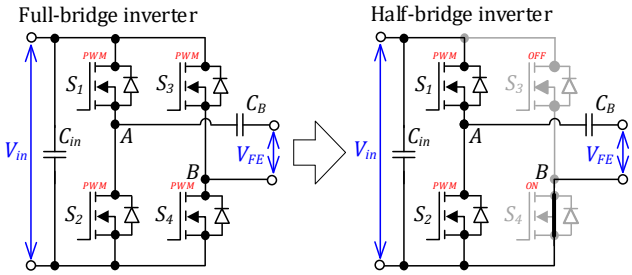


Figure 2.3. Reconfiguration of the front-end inverter with the blocking capacitor from the full-bridge to the half-bridge [Paper I].

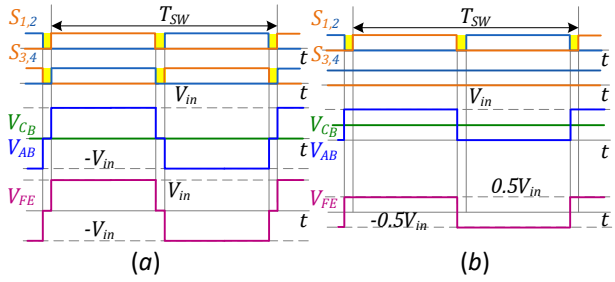


Figure 2.4. Operation of the front-end inverter with the blocking capacitor as FBI (a) and HBI (b) [Paper I].

2.2 Output Side TMC Techniques

In the case of the TMC for the back-end rectifier, TMC techniques increase the voltage gain G_{BE} or improve efficiency at a light load, as shown in [Paper I]. The reconfiguration from the full-bridge rectifier (FBR) to the half-bridge rectifier (HBR), also known as the voltage-doubler rectifier (VDR), is one of the most popular TMC techniques for a back-end rectifier. Similar to the FBI-HBI reconfiguration described above, this TMC can be realized by the capacitor leg and an additional switch [22], [25] or the blocking capacitor [16], [20] [16], [20], [26], [27]. The second case is shown in Figure 2.5. In the VDR mode, one switch in a leg is continuously turned on while the other is turned off, as shown in Figure 2.6. The transition from the FBR to VDR increases the voltage gain G_{BE} by two times from G_{BE} = 1 to G_{BE} = 2.

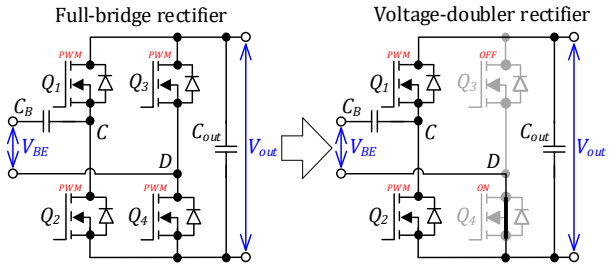


Figure 2.5. Reconfiguration of the front-end inverter with the blocking capacitor from the FBI to the HBI [Paper I].

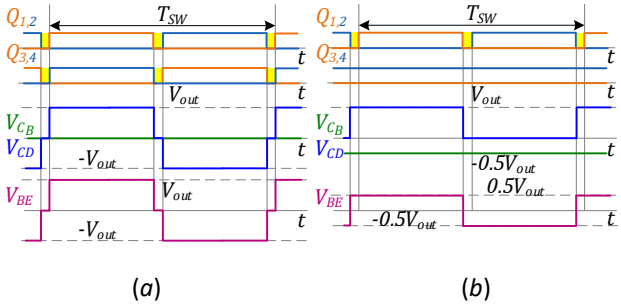


Figure 2.6. Operation of the front-end inverter with the blocking capacitor in the FBI (a) and HBI (b) modes [Paper I].

2.3 Advanced TMC Techniques

Besides TMC techniques for the front-end inverter and the back-end rectifier, advanced techniques target the dc voltage gain range extension. Most of these techniques are based on reconfiguring an isolation transformer or require several transformers [28] - [30]. Some of the techniques apply active pulse-width modulation (PWM) to extend the voltage gain [31], [32]. Moreover, some advanced TMC techniques use complex topologies that could be justified only for niche applications [33] - [35].

As a popular example of an advanced TMC technique, the double full-bridge LLC converter based on a reconfigurable three-leg inverter is shown in Figure 2.7. The presented converter consists of three-leg FBI and FBR, and two parallel transformers and series capacitors, which form two resonant tanks. The three-leg inverter can operate as the double full-bridge inverter (DFBI) and supply two transformers or operate as the FBI or the HBI while supplying only one of the transformers. In the DFBI mode, both resonant tanks operate in parallel, and the total turns ratio of transformers is $G_{GX} = n_1+n_2$. The main drawback of this approach is the doubled number of components compared with the conventional LLC.

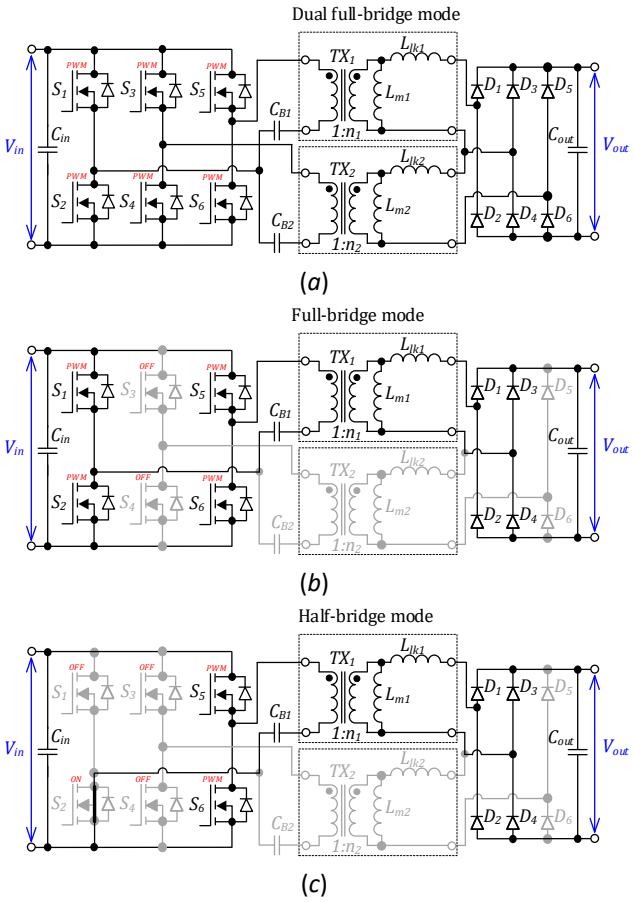


Figure 2.7. Reconfiguration of the transformer with two secondary windings [Paper I].

2.4 TMC Application Examples

The implementation of the TMC is reflected in different practical applications. All the practical examples can be combined into four groups based on targets: extension of an input or an output voltage range, operation with different standard voltage ranges, and the converter efficiency curve flatting.

Applying the TMC for flattening the efficiency curve across a power range in a PV microconverter was demonstrated in [36]. The topology of the microconverter is based

on the FBR, an isolation transformer, and the active FBR, as shown in Figure 2.8. At loads below 40%, the topology is reconfigured into the flyback converter to improve efficiency by up to 8% at a light load (Figure 2.9). The main drawback of the proposed approach is the requirement for using one bidirectional switch in the rectifier for blocking one leg in the single-switch mode.

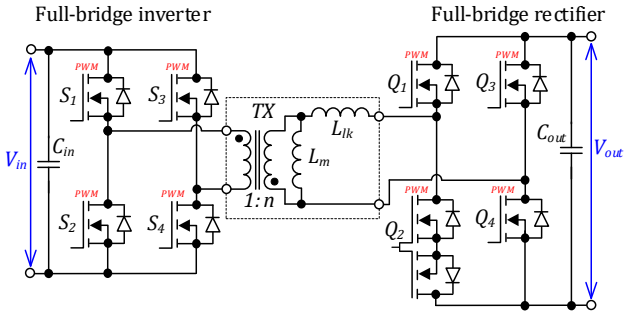


Figure 2.8. Dual-active bridge converter with flattened efficiency curve [Paper I].

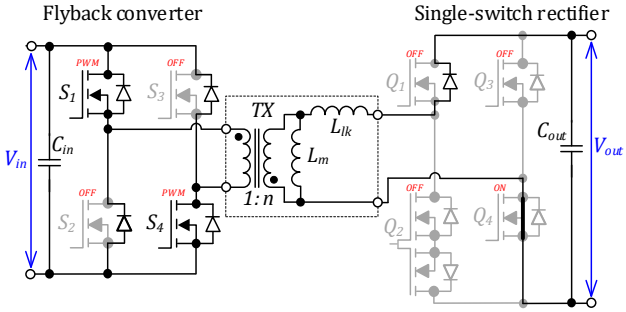


Figure 2.9. Dual-active bridge converter reconfigured to the flyback converter at a light load [Paper I].

2.5 Summary

The author reviewed and systematized all existing TMC techniques for galvanically isolated dc-dc converters and provided recommendations for applying TMC in different applications in [Paper I], making a significant contribution to the field of power electronics. The main principle of the TMC lies in reconfiguring a converter topology depending on voltage or power conditions for operating with higher efficiency. It could be concluded that the application of the TMC provides a low-cost opportunity to improve converter performance, such as increasing efficiency in a wide dc voltage gain range or a power range in galvanically isolated dc-dc converters.

Most of the TMC techniques could be summarized in the following basic principles: reducing the voltage or current stress of semiconductors in a wide voltage range by reconfiguring the topology; reducing the number of switching components to improve light-load efficiency; recovering converter gain after a semiconductor fault; increasing converter dc gain at the output side to enable input side operation in a wider voltage range while keeping the input-side duty cycle in an optimal range. However, TMC techniques

resulting in high complexity of the converter design can be recommended for niche applications, where strict performance requirements could justify associated extra costs.

The proliferation of the dc nano- and micro-grids, battery energy storage systems, and residential PV generation systems would create demand for high-performance low-cost converters and, consequently, facilitate industrialization of the TMC. Based on the recommendation provided in [Paper I], the FBI-HBI and the FBR-HBR based on a blacking series capacitor can be highlighted as simple, low-cost TMC techniques for a step-up isolated dc-dc converter, which can be utilized for interfacing a single PV module or a battery storage in dc microgrids.

However, applying TMC techniques comes with some challenges. The first challenge is the integration of TMC into a control system of a converter. It requires an additional control loop for reconfiguring a topology depending on the input and output voltage or power. In addition, the parameters of a regulator in the control system should be adapted to a topology reconfiguration due to changes in the small-signal converter model for each topology configuration. The second challenge in control is the implementation of soft transitions between topology configurations with stabilized input and output voltage and current to avoid overcurrent in components. The solutions for these issues are described in the following chapter.

3 Ultra-Wide Range Bidirectional SRC-Based IBBC

To design an ultra-wide range bidirectional isolated buck-boost converter (IBBC) for implementation of the UPEI, the two approaches of TMC have been merged and utilized in one converter. The final topology is presented in Figure 3.1. This topology has been presented for the first time in [37] as an isolated bidirectional dc-dc CLLC converter with frequency modulation. However, this topology can also operate as the dual active bridge (DAB) [39] - [41], the conventional LLC converter [42] - [44], or the SRIBBC with fixed switching frequency [45] - [47]. The differences between these converters are in the values of the leakage L_{lk} and the magnetizing L_m inductances of the isolation transformer TX and two series capacitors C_2 and C_3.

All these converter types are suitable for low-power step-up applications. Implementation of the UPEI concept requires a converter with galvanic isolation, a wide voltage range, high efficiency, and a high power density. However, the LLC, the CLLC, and the DAB have some limitations for operation in wide voltage and power ranges.

Due to the switching frequency variation in a wide range needed for voltage gain regulation, the LLC and the CLLC feature the following significant drawbacks:

1) degradation of the converter electromagnetic interference (EMI) performance with decreasing switching frequency for regulation of the voltage gain;

2) challenging design of magnetic and filter components and optimization;

3) reduced converter efficiency with the regulation of the voltage gain, which results from increased circulating current;

4) the inability to regulate the voltage gain at a light load;

5) the power flow direction cannot be changed smoothly.

In the case of the DAB, due to the leakage inductance utilized as a buck or boost inductor, the following drawbacks can be highlighted:

1) the maximum transferred energy through the TX depends on the input voltage that varies significantly;

2) non-sinusoidal transformer current resulting in higher losses in the windings of a high step-up transformer;

3) low efficiency at a light load due to the lost zero-voltage switching (ZVS).

At the same time, the voltage gain can be regulated in a wide range in the SRIBBC by using pulse-width modulation (PWM) or phase-shift modulation (PSM). The SRIBBC converter avoids the described drawbacks, making it a suitable candidate for implementing the UPEI concept.

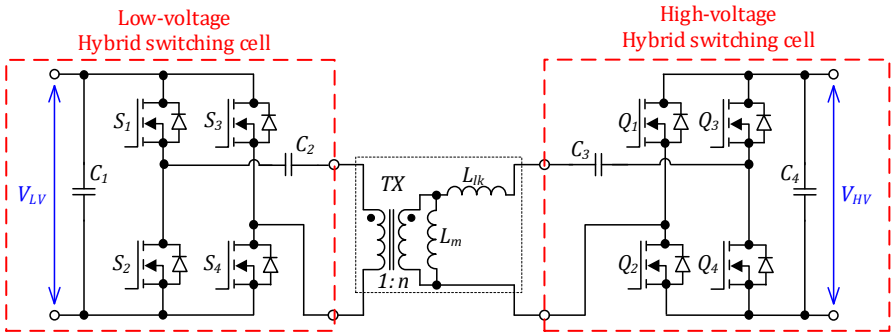


Figure 3.1. Series Resonant Isolated Buck-Boost Converter [Paper V].

3.1 Topology Description

As described above, the topology of the SRIBBC in the given study consists of the low-voltage and the high-voltage hybrid switching cells based on MOSFETs and the isolation transformer. The series blocking capacitors neutralize a dc bias in the transformer current in any power flow direction, which allows the possibility for applying asymmetrical control modulation for voltage regulation. At the same time, blocking capacitors allow the possibility for morphing the hybrid switching cells from the full-bridge to the half-bridge by turning on one switch and turning off the other one in the same inverter leg, as shown in Figure 3.2.

Thereby, the topology of the converter can operate in the following configurations: FBI-FBR, HBI-FBR, FBI-HBR, and HBI-HBR. The combination HBI-HBR is not used in the converter because the gain is the same as in the FBI-FBR, but it suffers from doubling the current stress. Therefore, the normalized voltage gain of the converter equals either 0.5, 1, or 2. The normalized dc voltage gain for the forward power flow is defined as in [14]

$$G_n = \frac{V_{HV}}{V_{LV} \cdot n}, \tag{4}$$

and for the backward power flow, the voltage gain can be defined as in [14]

$$G_n = \frac{V_{LV} \cdot n}{V_{HV}}, \tag{5}$$

where V_{HV} is the voltage at the high-voltage side, V_{LV} is the voltage at the low-voltage side.

At these points, the converter operates as a dc-dc transformer with a virtually sinusoidal transformer current. At the same time, the switching cells allow the application of different buck and boost control methods. In total, the converter in the given study operates in six control modes, as shown in Figure 3.3. The sequence of control modes is the same for both power directions. According to the number of control modes, this converter has been named “Isolated Hexa-Mode Converter (IHMC).”

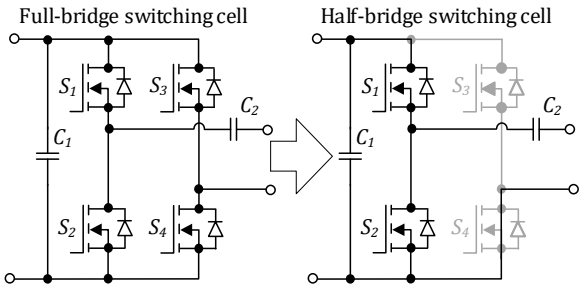


Figure 3.2. Reconfiguration of the hybrid switching cell [Paper V].

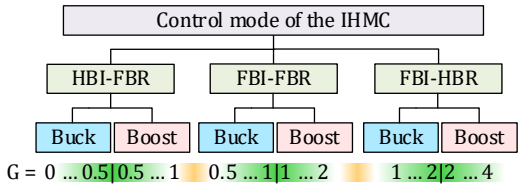


Figure 3.3. Control modes of IHMC [Paper V].

The series capacitors and the leakage inductance of the transformer form an equivalent resonant tank in the given SRIBBC converter. Hence, the angular resonant frequency of the resonant tank is defined as in [Paper V]

$$\omega_r = \sqrt{\frac{1}{L_{lk}C_r}}, \tag{6}$$

where C_r is the equivalent resonant capacitance calculated as in [Paper V]

$$C_r = \frac{C_2 C_3}{C_3 n^2 + C_2}. \tag{7}$$

In the SRC, the magnetizing inductance is usually significantly higher than the leakage inductance (L_m >> L_{lk}). Therefore, the magnetizing inductance is not taken into the resonant tank.

It has been considered that this topology operates in the discontinuous resonant current mode for providing zero-current switching (ZCS), i.e., with the resonant tank quality factor significantly below one. Hence, the switching frequency f_{sw} should be 5-10% lower than the resonant frequency f_r to implement sufficient dead time for soft-switching employing the transformer magnetizing current [45], [48].

3.2 Benchmarking of Buck Control Modulations

As mentioned above, the primary switching cells allow for applying different buck modulation methods to reduce the dc voltage gain. Previously, various buck modulations have been presented and described, such as the PWM [45], the hybrid PWM (HPWM) [49], the PSM [50], the hybrid PSM (HPSM) [51], the shifted PWM (SPWM) [52], the improved shifted PWM (ISPWM) [49], and the asymmetrical PWM (APWM) [53].

[Paper II] provides the classification (Figure 3.4) and detailed theoretical and experimental analysis of the buck modulations. The experimental benchmarking of the listed modulation has been presented based on the FBI-VDR topology of a unidirectional SRC converter in [Paper II].

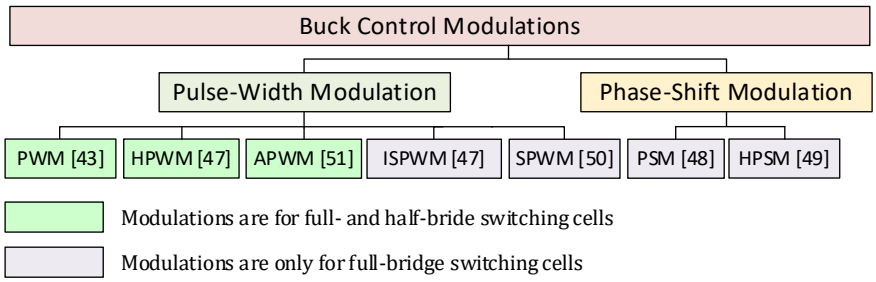


Figure 3.4. Classification of the buck control modulations [Paper II].

To understand and choose the best buck modulation for the FBI-FBR topology, the benchmarking of the selected buck control methods has been carried out and presented in Figure 3.5. The general components of the converter utilized in the benchmarking are listed in Table 3.1. The semiconductor components were selected based on experimental benchmarking. The input and output capacitors are selected to ensure the ripple of the input and output currents is below 5%. Capacitor C_2 was selected to avoid its participation in the resonance, while C_3 was chosen as the main resonant

capacitor. The transformer turns ratio was selected to match input and output nominal voltages, while its magnetizing inductance is sized by adjusting the air gap to provide soft-switching.

The benchmarking of the buck modulations is shown in Figure 3.5. The PWM, the SPWM, and the ISPWM are included in the benchmark because these modulations have the lowest performance in the previous study. As can be seen, the HPSM shows the best performance for the FBI-FBR topology configuration in the wide voltage range. The HPWM and APWM can be applied to buck the input voltage in the HBI-FBR topology configuration. However, even in the FRI-FBR topology, the APWM has the lowest power losses compared to the HPWM. The same conclusion has been provided in [Paper II] for the FBI-VDR topology.

Table 3.1 Specification of components of the UPEI.

$S_1 \dots S_4$	On Semiconductor FDMS86180
$Q_1 \dots Q_4$	Wolfspeed C3M0120100K
C_1, C_4	150 µF
C_2	52.8 µF
C_3	25 nF
L_{lk}	100 µH
L_m	2 mH
n	12.8

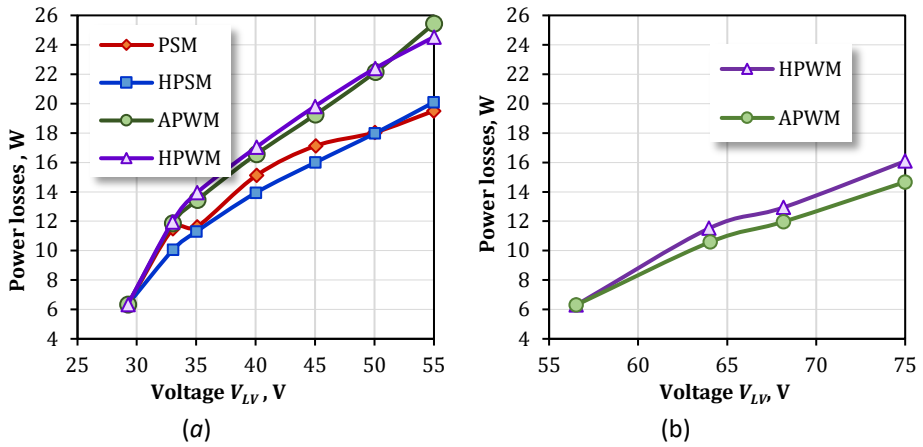


Figure 3.5. Experimental benchmarking of buck control modulations for the FBI-FBR (a) and for the HBI-FBR (b) [Paper II].

3.3 Benchmarking of Boost Control Modulations

Using the active switching cell allows the application of boost control modulations in any topology configuration to extend the voltage gain range. A similar benchmarking can be carried out for the boost control modulations. In [54], all boost modulations have been collected and described in detail. The study covers the following boost modulations: the PSM [55], the overlap modulation (OLM) [56], the PWM [57], the HPWM [58], and the APWM [59]. The classification of the boost modulation is presented in Figure 3.6.

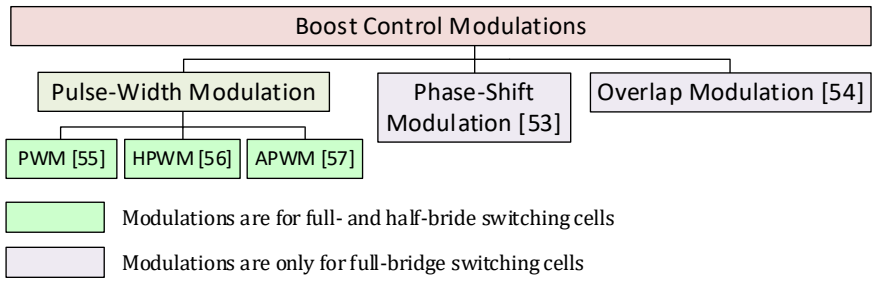


Figure 3.6. Classification of the boost control modulations.

Similar to the benchmarking of the buck modulations, benchmarking of the selected boost modulations has been provided for the same FBI-FBR topology with the general components listed in Table 3.1. Figure 3.7a shows the experimental benchmarking of the boost modulations. The PSM has the lowest power losses in the wide voltage range.

Among the analyzed modulations, the HPWM and the APWM can also be applied in the FBI-HBR topology. To determine the best boost modulation for the HBR, the additional benchmarking for the FBI-HBR topology is shown in Figure 3.7b. This test shows that the APWM is the best boost modulation for the FBI-HBR topology. These results were not published and are presented in this thesis for the first time.

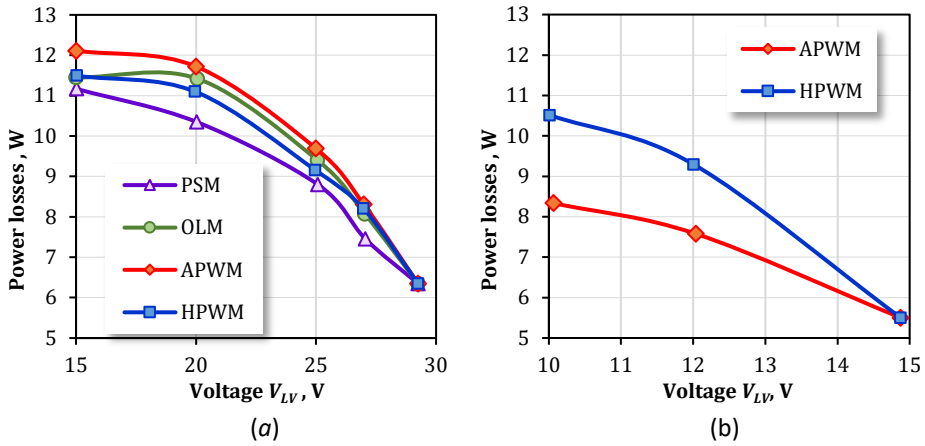


Figure 3.7. Experimental benchmarking of boost control modulations for the FBI-FBR (a) and the FBI-HBR (b) converter configurations.

3.4 Analysis of the Converter Operation

In addition to the benchmarking of the buck modulations, [Paper II] describes a methodology for deriving a mathematical model of the voltage gain and calculation of power losses for any control modulations and topology configurations. This methodology is based on calculation switching and conduction losses in transistors, body diodes of MOSFETs, the transformer, input and output filter capacitors, series capacitors, and input and output resistance of a printed circuit board (PCB). To verify the proposed methodology, the theoretical voltage gain has been calculated for the buck HSPM and the boost PSM control modulations and compared with the experimental results for the FBI-FBR topology configuration in Figure 3.8.

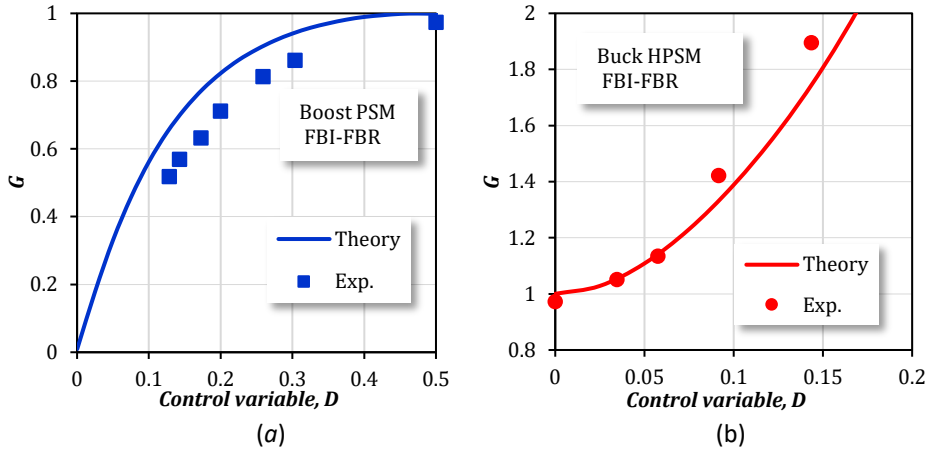


Figure 3.8. Comparison of theoretical and experimental voltage gains for the boost FBI-FBR (a) and the buck FBI-FBR (b) control modulations.

In addition, Figure 3.9 shows the comparison of power losses for the same control modulations. With an increase or decrease in the input voltage, efficiency decreases. This is mostly associated with the increasing RMS and switching currents in the converter. As can be seen, the deviation between theoretical and experimental results is less than 10%. This deviation is primarily associated with the non-modeled non-linear behavior of the parasitic elements. Therefore, this methodology can be used for other control modulations and the thermal design of a prototype.

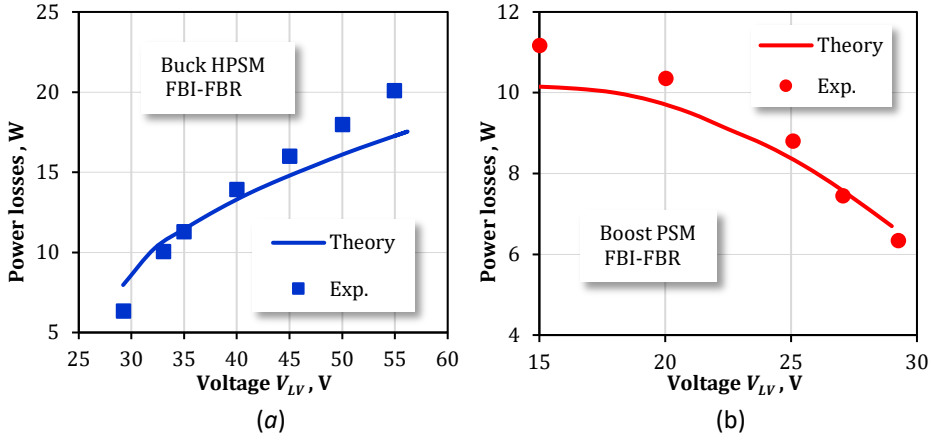


Figure 3.9. Comparison of theoretical and experimental power losses for the buck FBI-FBR (a) and the boost FBI-BR (b) control modulations.

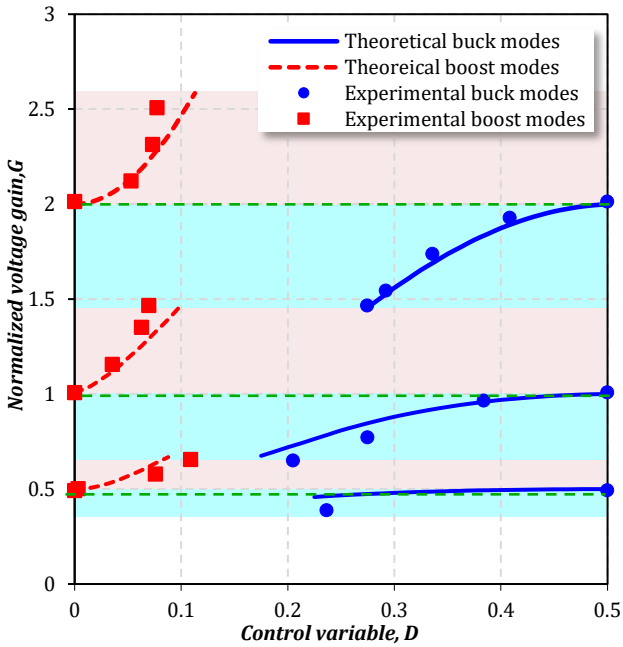


Figure 3.10. Verification of the proposed analysis methodology for the best-performing modulation of the SRIBBC [Paper V].

By using the methodology, the theoretical voltage gain curves for all six control modes are plotted in Figure 3.10 as the function of the generalized control duty cycle D. In addition, experimental dc gains values in each control mode are shown in Figure 3.10, where the sequence of control modes is the same in both power flow directions. As can be seen, the converter can operate in a wide voltage gain from 0.4 to 2.5 thanks to the TMC. Figure 3.10 shows deviations of <5% between experimental and theoretical gain curves, proving the validity and versatility of the proposed analysis methodology.

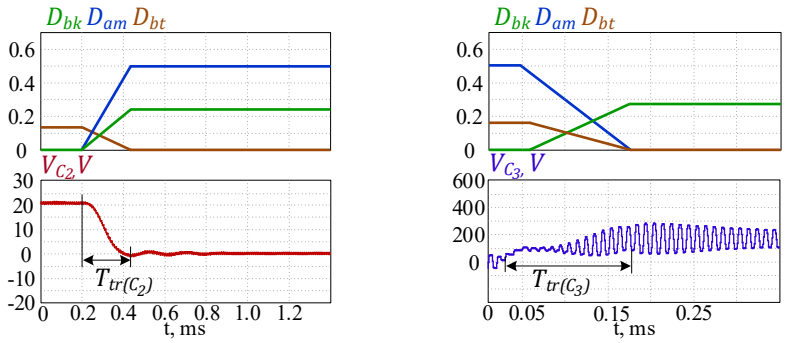
The gain ranges between the boost HBI-FBR and the buck FBI-FBR modes; the boost FBI-FBR and the buck FBI-HBR modes are transition regions. Points of transitions between these modes are selected based on experimental or estimated efficiency.

3.5 Soft Topology Reconfiguration

The series capacitors feature different dc voltage stress in different topology configurations. For example, the dc voltage of capacitor C_2 equals half of the input voltage in the boost HBI-FBR mode and zero in the buck FBI-FBR mode. The algorithm for soft transition has been proposed in [Paper III] to avoid high current stress and oscillation during transitions between different topology configurations.

The main idea of the soft-transition algorithm is to increase the duty cycle D_{am} linearly to switch transistors in a leg from a modulated state to the static state (one transistor is turned on continuously, and the other one is turned off) when transiting from the full-bridge configuration to the half-bridge configuration of a hybrid switching cell. In the reverse case, the algorithm linearly decreases the duty cycle to switch the transistor into a modulated state. At the same time, the soft-transition algorithm linearly transits between buck and boost control modulations by linearly changing the buck and boost

duty cycles (D_{bk} and D_{bt}). The simulated result of the transitions between the boost HBI-FBR and the buck FBI-FBR as well as between the boost FBI-FBR and the buck FBI-HBR are shown in Figure 3.11.



(*a*) (*b*)

Figure 3.11. Comparison of theoretical and experimental power losses for the buck FBI-FBR (a) and the boost FBI-HBR (b) control modulations [Paper III].

A special algorithm is not required for mode transition within one topology configuration, e.g., between the buck FBI-FBR and the boost FBI-FBR modes, because the converter smoothly crosses the boundary operating point.

3.6 Summary

Based on the theoretical review of isolated dc-dc converters, the author has proven the hypothesis that the SRC is a universal tool for uni- and bi-directional dc microgrid applications when its functionality is extended by applying hybrid H-bridge switching cells. It is selected for implementation of the UPEI concept. The author synthesized a simple advanced TMC technique that allows the converter to operate in four topology configurations: FBI-FBR, HBI-FBR, FBI-HBR, and HBI-HBR. At the same time, buck and boost control modulation can be applied to regulate the voltage gain. The SRIBBC, with the proposed advanced TMC technique, can operate in eight modes. Thus, applying TMC with hybrid switching cell-based SRIBBC allows the possibility to operate in the wide dc voltage gain from 0 to 4. This extends the voltage gain range from 1:3 to at least 1:6 in comparison with conventional solutions, which proves the third hypothesis.

Experimental benchmarking of various constant-frequency control modulations performed by the author proves the second hypothesis that symmetrical (HPSM) and asymmetrical (APWM) modulations provide the best buck control modulation for the FBI-FBR/FBI-HBR and the HBI-FBR configurations, respectively. Similarly, the PSM and the APWM are the best boost control modulation for the FBI-FBR/HBI-FBR and the FBI-HBR, respectively, as was hypothesized.

In addition, the author has developed a methodology for deriving a mathematical model of the dc voltage gain and power loss for different control modulations. An analytical model of SRIBBC was derived and verified experimentally to be further used for the converter performance optimization in uni- and bi-directional applications.

In addition, the algorithm for soft transition between topology configurations described in this chapter was proposed by the author and verified by numerical simulations. The algorithm allows the possibility for recharging series capacitors and stabilizing input current and voltage during transitions between topology configurations.

4 Design Guidelines for SRIBBC

This chapter focuses on the design and selection of critical components such as the isolation transformer, series capacitor, and semiconductor components for designing an ultra-wide range bidirectional isolated buck-boost converter.

4.1 Integrated Transformer Design

Selecting turns ratio *n* of the isolation transformer is the most critical point in the UPEI design. The converter should maintain high efficiency with a selected voltage source under any conditions. Depending on the temperature and degradation, the input source voltage can vary widely. For example, the GMPP of a PV module could move to a low voltage under partial shading. Figure 4.1 summarizes the probable operating voltage range of typical 60- and 72-cell PV modules and LiFePO4 batteries (24 V and 48 V).

As described in Chapter 3, the IHMC features three nominal voltage gains *G*=0.5, 1, and 2, where the converter theoretically has the maximum efficiency due to the transformer current being virtually sinusoidal and all transistors turned on and off at zero current. With an increase or decrease in the input voltage, efficiency decreases because RMS and switching currents are increased when moving from the three nominal dc gain values. The bold vertical green lines in Figure 4.1 show the theoretical maximum efficiency voltages and green gradient fields demonstrate the decreasing efficiency.

To provide high converter efficiency in a wide input source voltage range, the turns ratio of the transformer has been selected as *n*=12.7 by using Eq. (4) and (5). This ensures high efficiency at the most probable input source operation voltages.

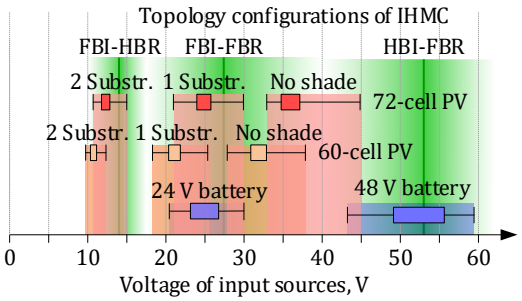


Figure 4.1. Voltage characteristics of selected PV and batteries modules and resulting target operating range for the UPEI.

The maximum flux density B_{max} is the next important design parameter of the transformer. The theoretical analysis shows that the flux density achieves the maximum value at the normal voltage gain under the FBI-FBR topology configuration in any direction. The flux density B_{max} in the forward and backward directions was calculated by the author, respectively, as

$$B_{\max(fw)} = \frac{V_{LV}}{4 \cdot f_{SW} \cdot A_e \cdot N_{pr}}, \tag{8}$$

$$B_{\max(bw)} = \frac{V_{HV}}{4 \cdot f_{SW} \cdot A_e \cdot N_{sec}}, \tag{9}$$

where A_e is the effective core area, and N_{pr} and N_{sec} are the numbers of turns of the primary and secondary windings, respectively.

The next design parament of the transformer is the magnetizing inductance L_m. The magnetizing current circulated through low- or high-voltage sides (depends on a control modulation and a direction of power flow) recharges output capacitances of MOSFETs during the dead time T_D between the control pulse of transistors. The highest magnetizing current for the same dead time is required in the forward and backward boost HBI-FBR modes. Therefore, the maximum value of the magnetizing inductance for the forward direction can be defined as in [Paper V]

$$L_{m(\max)} \le \frac{T_{D(LV.bt)} \cdot n^2}{16 \cdot f_S \cdot C_{oss(LV)}}, \tag{10}$$

for the backward mode, the maximum value of the magnetizing inductance is defined as

$$L_{m(\max)} = \frac{T_{D(HV.bt)}}{16 \cdot f_S \cdot C_{oss(HV)}}, \tag{11}$$

where $C_{oss(LV)}$ and $C_{oss(HV)}$ are the parasitic output capacitances of low- and high-voltage side switches, respectively.

The fourth design parameter of the transformer is the leakage inductance L_{lk}. The analysis in [Paper II] showed that the leakage inductance should be as much as possible to achieve the lowest amplitude of the resonant current and, as a result, the smallest conduction and switching losses in the converter (Figure 4.2). On the other hand, for operation in the discontinuous current mode, the leakage inductance should be limited. As the theoretical analysis in [Paper V] based on the proposed methodology shows, the critical mode for limiting the leakage inductance is the forward buck FBI-HBR mode. Therefore, the maximum value of the inductance can be defined as

$$L_r < \frac{V_{out} \cdot f_S}{I_{out} \cdot \omega_r^2}, \tag{12}$$

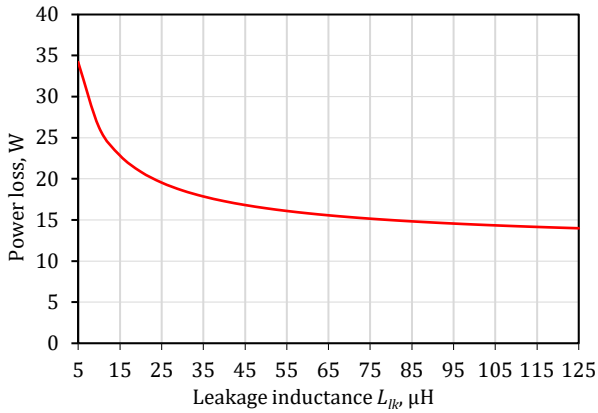


Figure 4.2. Theoretical dependence of losses on the leakage inductance [Paper II].

Usually, an external inductor is required to achieve a high resonant inductance. However, [Paper IV] proposed a transformer design based on the hybrid split bobbin to integrate the required inductance values into the isolation transformer. The novelty of the proposed approach is in the partial overlap of the secondary and primary windings. At the same time, most of the secondary winding turns are in split bobbin arrangement regarding the input side winding. The design of the transformer based on an ETD core is shown in Figure *4.3*. The same approach can be realized based on a planar core as an alternative solution for achieving a compact design for the converter.

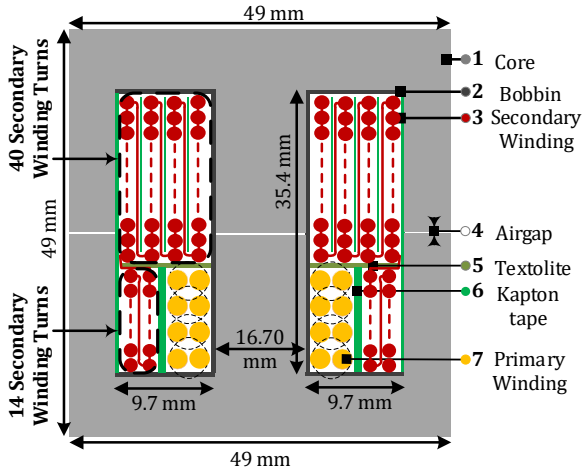


Figure 4.3. Transformer design with the hybrid split bobbin [Paper IV].

Finally, using Litz wire with a strand diameter of 0.04 mm has been considered to reduce the skin and proximity effects. This strand diameter considers that the shape of the resonant current changes from sinusoidal to triangular during operation in a wide voltage range. Hence, the resonance current spectrum in each mode includes a set of odd harmonics up to the 11th.

4.2 Selection of Resonant Capacitors

The selected topology of the UPEI (Figure 3.1) includes two series capacitors: C_2 on the low-voltage side and C_3 on the high-voltage side. Each of them or both capacitors can be used for forming a resonant tank. However, low-voltage high-current capacitors, such as ceramic capacitors, show high capacitance deviations due to varying dc bias voltage and operating temperature. At the same time, high-voltage film capacitors feature low variations of capacitance and low volumetric capacitance density.

According to these aspects, the capacitor C_3 has been selected for forming the resonant tank. Therefore, to avoid deviation of the resonant frequency, the capacitance of capacitors C_2 should be much higher than C_3 ($C_2 >> C_3$). Furthermore, the effective resistance of the C_2 should be as low as possible to carry a high transformer current at the low-voltage side.

The equations for calculation capacitance and voltage for C_2 and C_3 have been presented in [Paper V]. The value of the capacitor C_3 is calculated as

$$C_3 \approx \frac{1}{L_{lk}\omega_r^{\,2}}. \tag{13}$$

The maximum operating voltage of the capacitor C_3 is achieved in the forward buck FBI-HBR mode at a low duty cycle and can be defined as

$$V_{C3(\max)} = \frac{V_{HV} + \Delta V_{C3}}{2}, \tag{14}$$

where ΔV_{C3} is the peak-to-peak voltage ripple of the capacitor C_3:

$$\Delta V_{C3} = \frac{I_{out}}{C_3 \cdot f_S}, \tag{15}$$

where I_{out} is the output current in the forward mode.

In the forward boost HBI-FBR mode, the low-voltage capacitor C_2 is under maximum voltage stress that equals

$$V_{C2(\max)} = \frac{V_{LV} + \Delta V_{C2}}{2}. \tag{16}$$

where ΔV_{C2} is the peak-to-peak voltage ripple of the capacitor C_2:

$$\Delta V_{C2} = \frac{I_{in}}{C_2 \cdot f_s \cdot n}, \tag{17}$$

where I_{in} is the input current in the forward mode.

4.3 Selection of Semiconductor Components

The selection of transistors plays a vital role in the total power losses of the converter. The transistors should have the lowest channel resistance to reduce conduction losses. However, MOSFETs with a low resistance feature high parasitic capacitance, significantly increasing switching losses. Therefore, there is a trade-off between conduction and switching losses.

Based on the theoretical analysis, a few 100 V Si MOSFETs with a cost of below 5 € have been selected for experimental benchmarking. Because only two switches have high switching currents, two different types of transistors can be used on the low-voltage side to optimize power losses based on operating conditions.

Figure 4.4 shows experimental benchmarking of low-voltage switches in forward buck FBI-FBR mode. The lowest power losses are achieved using FDMS86180 switches or combining FDMS86180 and FDMS86181. The FDMS86180 switch type from On Semiconductors was selected as the optimal solution with a high-performance transistor for the primary side.

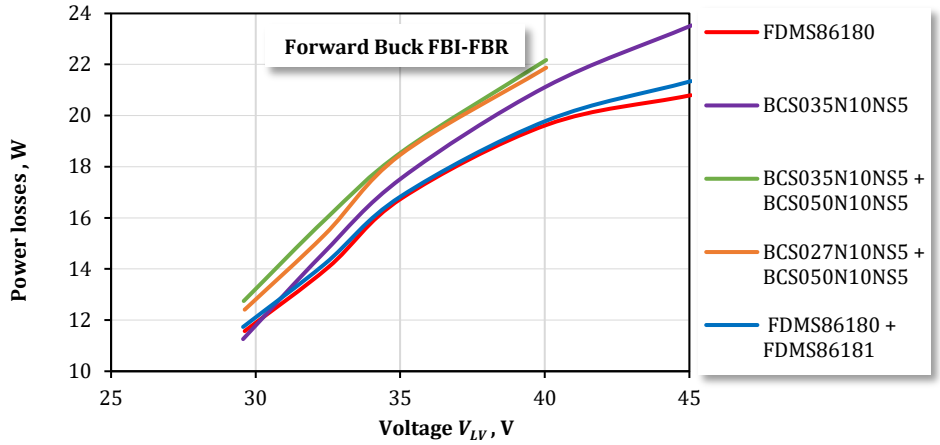


Figure 4.4. Experimental benchmarking of low-voltage switches.

A similar benchmarking can be carried out for high-voltage side switches. In the forward boost modulations, two high-voltage switches have high switching current. Therefore, two different types of transistors can also be used on the high-voltage side. Theoretical analysis showed that SiC MOSFETs from CREE/Wolfspeed, Infineon, Littelfuse, and GaN transistors from Transphorm have the potential for high performance in the UPEI. The benchmarking shows that SiC MOSFET C3M0075120 from CREE/Wolfspeed allows

for achieving the lowest power losses. Moreover, it can be noted that GaN transistors for low-power high-voltage applications and switching frequency of 100 kHz feature higher power losses than SiC MOSFETs. One of the problems with GaN transistors is the high forward voltage drop of body diodes, which conduct current during dead time.

It can be concluded from the benchmarking results presented in Chapter 3 that using two different transistors does not reduce total power losses. The first reason is that all transistors in one switching cell have the same RMS current in a full-bridge mode. The second reason is the low switching losses of transistors with high switching current due to zero voltage switching, as analyzed in [Paper V]. Moreover, transistors also switch magnetizing current, which circulates through the low- or high-voltage side, depending on the control mode. Therefore, only one type of switch can be selected for each side.

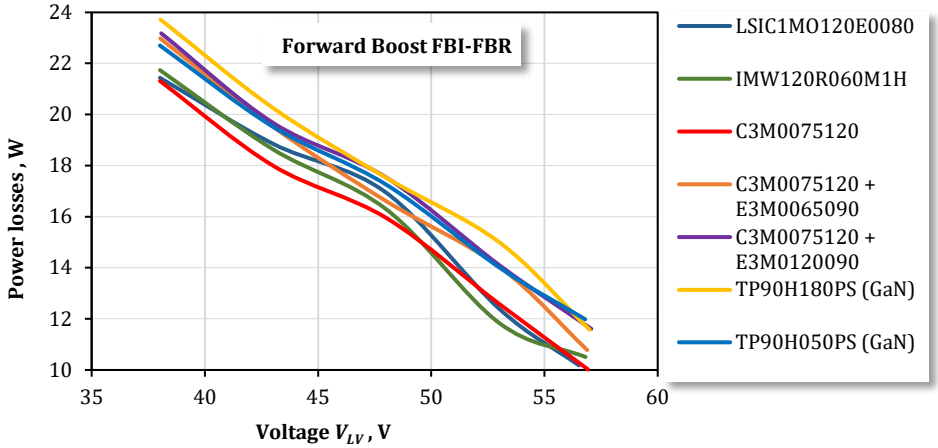


Figure 4.5. Experimental benchmarking of high-voltage switches.

4.4 Thermal Design for Passive Cooling

The theoretical analysis of power losses at different control modes was described in [Paper V] (Figure 4.6). The worst control modes in terms of power losses are the buck FBI-HBR and the boost FBI-FBR in both directions. As can be seen from Figure 4.6, the highest power losses in low-voltage switches are observed in the backward boost FBI-FBR mode. The worst mode for high-voltage switches is the backward buck FBI-FBR mode. The maximum power losses in one low- and high-voltage switch equal 1.8 W and 0.75 W, respectively.

It was mentioned in the datasheet of MOSFET FDMS 86180 from On Semiconductor [60] that the transistor soldered on a 1 in^2 ≈ 16.4 mm^2 pad of one-layer board with 2 oz copper has the thermal resistance from a junction to ambient $R_{\theta JA}$ of 45 °C/W without an additional heatsink. To limit the junction temperature T_J to 100°C at the ambient temperature of 40 °C, the thermal resistance $R_{\theta JA}$ should be less than 33 °C/W for operation in the worst-case conditions.

One way to minimize the thermal resistance is to increase the area of the pad up to 22.5 mm^2. However, the popular solution is using the top and the bottom layers in a four-layer PCB for cooling transistors. To provide the lowest thermal resistance between the layers of a PCB, in [61] the author recommends using a high number of vias. Following this implementation approach, the pad area of 12 mm^2 on both sides of a PCB with

48 vias between them should be sufficient for cooling each low-voltage MOSFET in the worst-case conditions, considering the thermal resistance of a via equal to 261 °C/W [62].

In the case of the high-voltage MOSFETs, the thermal resistance $R_{\theta JA}$ without a heatsink equals 40 °C/W according to the datasheet of C3M0075120 [63]. At the ambient temperature of 40 °C, the maximum temperature of the junction will be around 70 °C in the backward buck FBI-FBR mode. This value of junction temperature is significantly less than the maximum junction temperature of $T_{J(max)}$ = 175 °C indicated in the datasheet. Therefore, the selected high-voltage SiC MOSFETs can be utilized in a prototype of the UPEI without a heatsink.

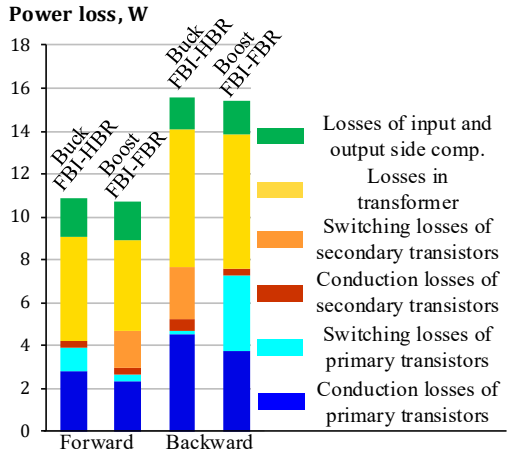


Figure 4.6. Power losses in the SRIBBC under the forward buck FBI-HBR and boost FBI-FBR mode at V_{LV} = 17 V, P_{LV} = 205 W, and under the backward buck FBI-HBR and boost FBI-FBR mode at V_{LV} = 38 V, P_{LV} = 350 W. [Paper V].

4.5 Control System Implementation

The final important part of the converter design is the control system, which is commonly based on a microcontroller. The first requirement applied to the microcontroller is a high precision of PWM peripherals. The microcontroller should provide high-frequency gating signals with a controlled dead time of about 50 – 200 ns. The second requirement is high calculation performance for implementing the soft transition algorithm and a closed-loop control system. Based on these requirements, STM32 microcontrollers with high-resolution timers can be highlighted as an appropriate solution.

Another important part of the control system is measurement circuitry. To implement the soft transition algorithm, the control system should measure voltages and currents on both sides of the converter. Therefore, the microcontroller should have a minimum of four analog-to-digital converter (ADC) channels. It was considered to supply the control system from the low-voltage side to reduce the implementation cost. Therefore, non-isolated sensors can be used on the low-voltage side. The cheapest voltage and current sensors are resistive dividers and current shunts. On the high-voltage side, sensors should be isolated from the control system.

As described in [Paper V], synchronous rectification improves converter efficiency significantly. The simple approach based on the current transformers and comparators embedded in the microcontroller allows the possibility for the correct detection of an

instant when the switches should be turned off (Figure 4.7). Two measurement circuits are used on the low- and high-voltage side of the transformer to neutralize the effects of the magnetizing current. Therefore, the current transformer on the high-voltage side and comparators COMP3 and COMP4 are responsible for operation in the forward mode, and the current transformer on the low-voltage side and comparators COMP1 and COMP2 are responsible for operation in the backward mode.

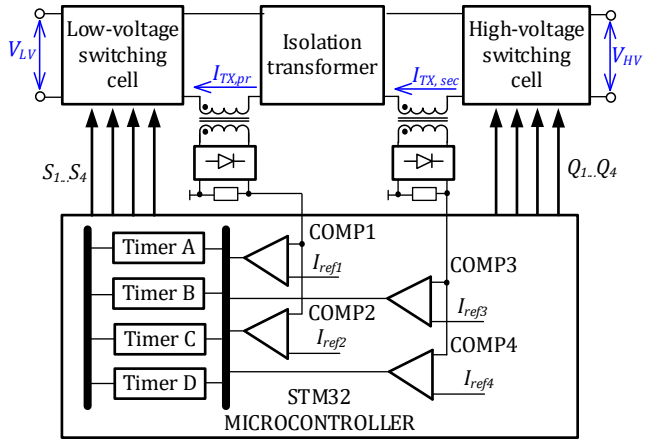


Figure 4.7. Control circuit of the synchronous rectifier [Paper V].

To implement the synchronous rectification, the microcontroller should include a minimum of four internal comparators. Two additional comparators can be used to realize overcurrent protection on the low- and high-voltage sides. Therefore, STM32G474 microcontroller has been used for the UPEI implementation.

4.6 Summary

To summarize the design guidelines developed by the author for the ultra-wide range bidirectional series resonant isolated buck-boost converters, the selected components of the converter are listed in Table 4.1. The best-performing low- and high-voltage MOSFETs have been selected based on theoretical and experimental benchmarking. To control selected MOSFETs, isolated dual channels 5 V/0 and +15/-5 drivers have been implemented for low- and high-voltage transistors, respectively. The filter capacitors C_1 and C_4 on the low- and high-voltage have been selected to provide maximum voltage and current ripple of 5%.

The methodology for optimization of the resonant inductance sizing in the SRIBBC was proposed in this chapter. Using the methodology, the leakage inductance of 100 µH was calculated as a trade-off between power losses in the converter and the wide dc gain regulation range. This chapter demonstrates the practical confirmation of the fourth hypothesis that the isolation transformer design with a partially overlapping split bobbin can implement the optimal leakage inductance. The proposed transformer design avoids using an additional resonant inductance.

The simple and low-cost circuit for implementation of the synchronous rectifier at the discontinuous resonant current was described in this Chapter. The synchronous rectifier circuit is realized based on current transformers and internal comparators of the microcontroller.

Table 4.1 General specification of the UPEI.

Power Components	
$S_1 \ldots S_4$	On Semiconductor FDMS86180
$Q_1 \ldots Q_4$	CREE C3M0120100K
TX	Custom based on ETD 49 3C95 ferrite core
L_{lk}	100 µH
L_m	2 mH
n	12.8
C_3	15 nF, B32641B0153J and 10 nF, MC1206F106Z160CT
C_4	4.7 µF, ECWFG1B475J and 0.47 µF, B32653A0474J000
Control, driving and measurement	
Microcontroller	ST STM32G474
Drivers for low-voltage MOSFETs	Silicon Labs SI8233BB-D-IS1R
Drivers for high-voltage MOSFETs	Texas Instr. UCC21521ADW
Aux. power supply	Texas Instr. LM5010MH/NOPB
Low-voltage side voltage sensor	Resistive divider 1:20
Low-voltage side current sensor	Shunt 0.003Ω and OP Microchip MCP6L02T-E/SN
High-voltage side voltage sensor	Texas Instr. AMC1200
High-voltage side current sensor	Shunt 0.01Ω and Texas Instr. AMC1200

5 A High-Efficiency Universal Front-End Interface Converter

This chapter summarizes all previous chapters and presents the concept of the UPEI as the result of the given study. The chapter focuses on realizing the control algorithms for operation with PV modules and batteries and identifying a connected input source. This chapter also covers the results of the studies published in [Paper V], [Paper VI], and [Paper VII].

5.1 Prototype

A prototype of the UPEI includes the power circuit, auxiliary power supply circuit, drivers, sensors, and microcontroller unit on one four-layer PCB shown in Figure 5.1. The prototype was designed to operate in the safe operating area (SOA) within the input voltage range from 10 to 60 V and within the power and current profiles shown in Figure 5.2. The SOA covers the operation ranges of typical market-leading PV module types (60- and 72-cells silicone PV modules) and batteries (24 V and 48 V).

It should be noted that the prototype has no electrolytic capacitors to increase the reliability and lifetime of the converter. The second important aspect of the prototype is the absence of any heatsinks. As mentioned in the previous chapter, semiconductors are cooled using the PCB surface.

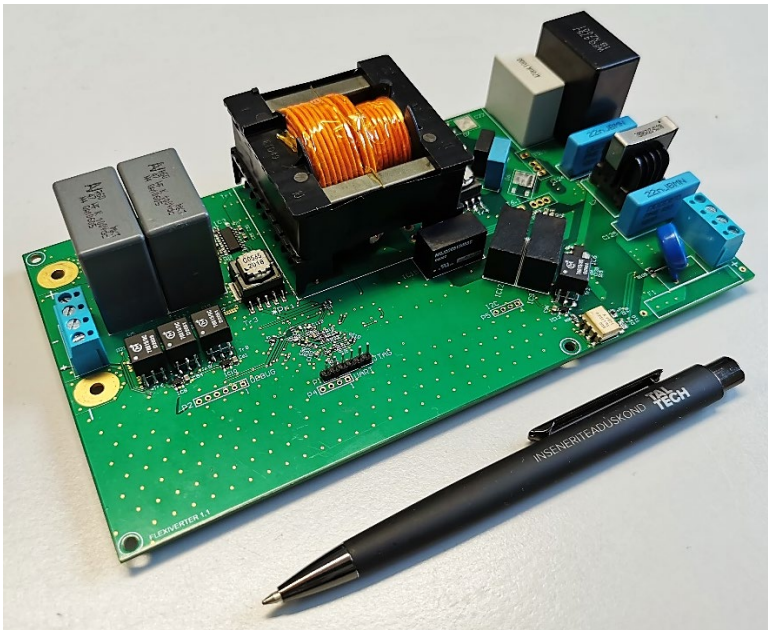


Figure 5.1. Prototype of the UPEI [Paper VI].

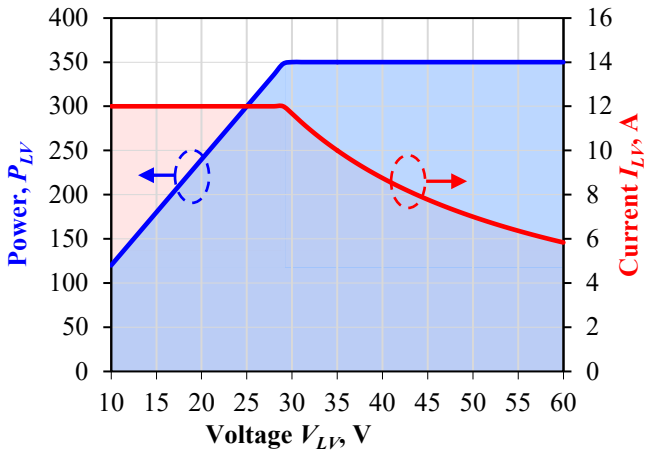


Figure 5.2. Safe operation area for the UPEI prototype [Paper V].

5.1.1 Efficiency

The precision power analyzer Yokogawa WT1800 has been used to measure the efficiency of the designed prototype at different low voltages, different levels of power, and the nominal voltage of the high-voltage side of 350 V. The efficiency map is shown in Figure 5.3. As can be seen, in the wide voltage and power ranges, the efficiency curve varies in the range from 95% to 98.1%. With decreasing the current of the low-voltage side down to 2 A, the efficiency drops rapidly because the synchronous rectifier cannot operate at a low resonant current, as noted in Chapter 4. The second reason is constant power losses related to the transformer core losses and conduction losses from parasitic oscillations.

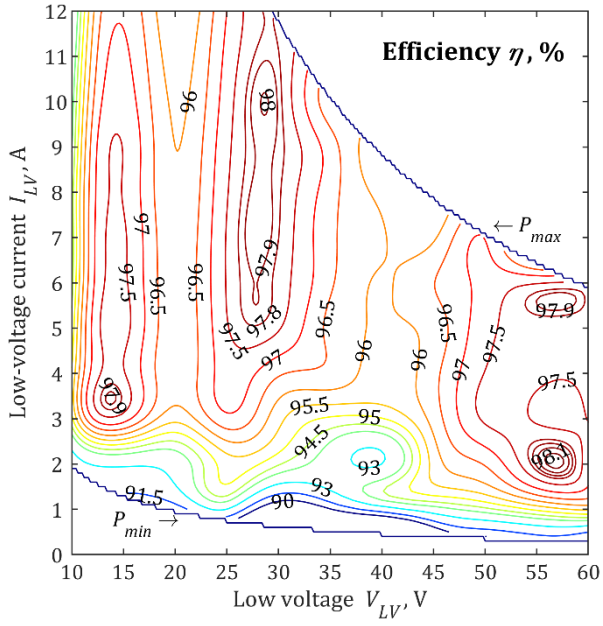
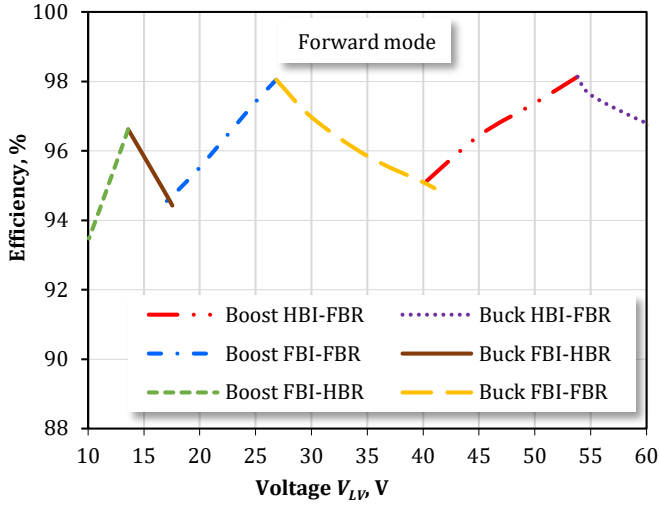


Figure 5.3. Experimental efficiency map of the UPEI [Paper VI].

The peak efficiency of the converter equals 98.1% at V_{LV} = 56 V. Moreover, the converter features three peak efficiencies at V_{LV} = 14, 28, and 56 V, when it operates in the normal control modes. In these points, the transformer current is virtually sinusoidal.

Detailed measured efficiency of the converter operating in the forward and the backward power flows at the borders of the SOA is plotted in Figure 5.4. These figures have been published in [Paper V]. They show that topology configurations are morphed from HBI-FBR to FBI-FBR and from FBI-FBR to FBI-HBR at 17 V and 40 V on the low-voltage side, respectively.



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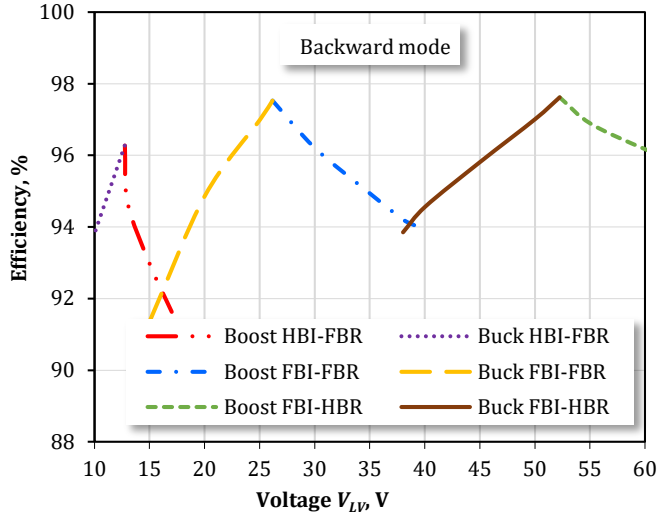


(*b*)

Figure 5.4. Efficiency of the UPEI operating in the forward (a) and the backward (b) power flows at the borders of the safe operating area [Paper V].

The efficiency is higher than 93.8% in the forward mode and 92% in the backward mode. In both directions, the power at the low-voltage side has been used as a reference for calculation of efficiency. Another reason for the efficiency difference is longer dead times for the high-voltage side transistors. The maximum efficiency in the backward mode is 97.6%.

5.1.2 Thermal Analysis

Thermal camera Fluke Ti25 has been used in experiments to measure the temperature of components in the prototype under maximum stress. Figure 5.5 shows temperature distributions in the prototype for the forward and the backward power flow under the buck FBI-HBR and the boost FBI-FBR modes. The thermal images were taken by the thermal camera at a distance of 5 cm from the PCB at an ambient temperature of 25 °C. At each measured mode, the prototype operated for a minimum of 15 min.

As the theoretical analysis showed in Chapter 4, the highest power losses stand out in the backward buck FBI-HBR and the boost FBI-FBI control modes. Therefore, components in the prototype have the highest temperature in these modes. The experimental results show that the low- and high-voltage switches achieve 90°C and 60°C under the buck FBI-HBR at V_{LV} = 38 V and P_{LV} = 350 W. The temperatures achieved are less than the calculated values. Therefore, the designed PCB can cool down the selected semiconductor devices without any heat sinks.

5.1.3 Closed-Loop Control System

The microcontroller STM32G474 has been justifiably selected in Chapter 4 to implement the control system. The block diagram of the power circuit and the control system is shown in Figure 5.6.

The state machine has been applied to design the high-level part of the control architecture. The state machine is switched between 11 states depending on the control algorithms described in the next sub-chapters.

The medium level of the control architecture includes the following function blocks: Protection, Filters, Timer for PV rescanning, Synchronous rectifier, and Calculation of compare values. The protection block enables the control system if all voltages and currents are within the safety limits. In the case of any faults, all switches and the solid-state circuit breaker (SSCB) are turned off. Moreover, the SSCB provides a soft plug-in to the dc microgrid by charging the high-voltage capacitor C_4.

The synchronous rectifier block enables or disables control of rectifier switches depending on the power level, control modulation, and control mode. The timer for PV rescanning restarts global maximum power point tracking (GMPPT) every 30 minutes if the UPEI operates with a PV module. The Calculation of compare values block recalculates and sets required compare values from a control variable for each channel of the high-resolution timer (HRTIM).

The low-level control system includes HRTIMs, ADCs, and internal comparators (COMP2, COMP3, COMP5, and COMP6). The comparators are utilized to realize the control of the synchronous rectifier. The output signals of the sensors are converted into a digital form by using integrated 12-bit ADCs of the microcontroller.

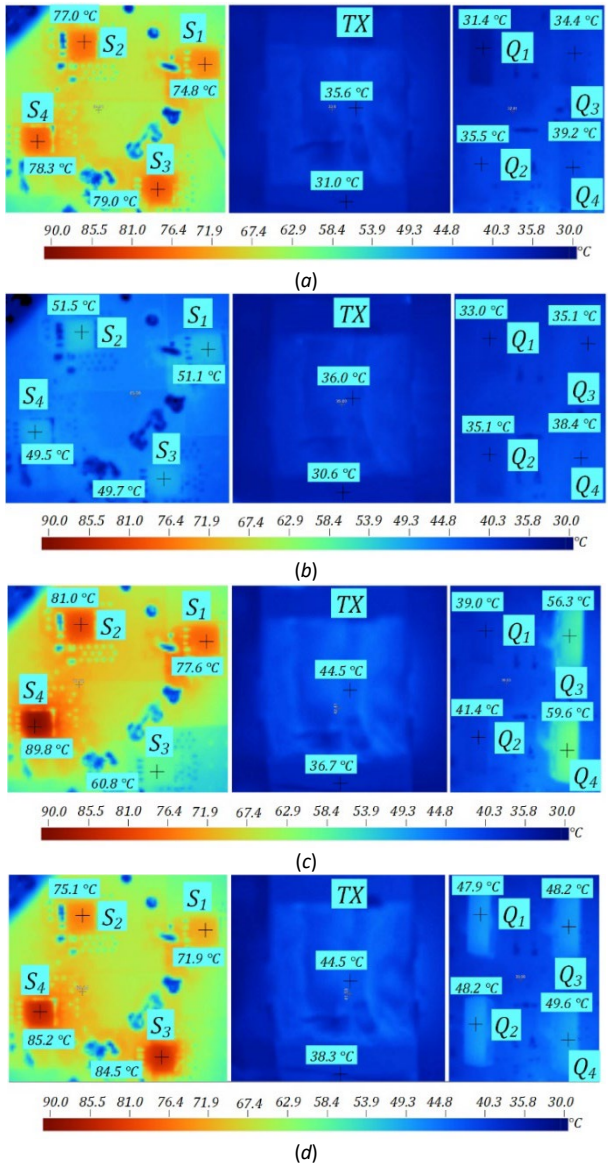


Figure 5.5. Temperature distribution in the UPEI prototype in the forward mode under the buck FBI-HBR (a) and the boost FBI-FBI (b) mode at V_{LV} = 17 V and P_{LV} = 205 W; in the backward mode under the buck FBI-HBR (c) and the boost FBI-FBI (d) mode at V_{LV} = 38 V and P_{LV} = 350 W [Paper V].

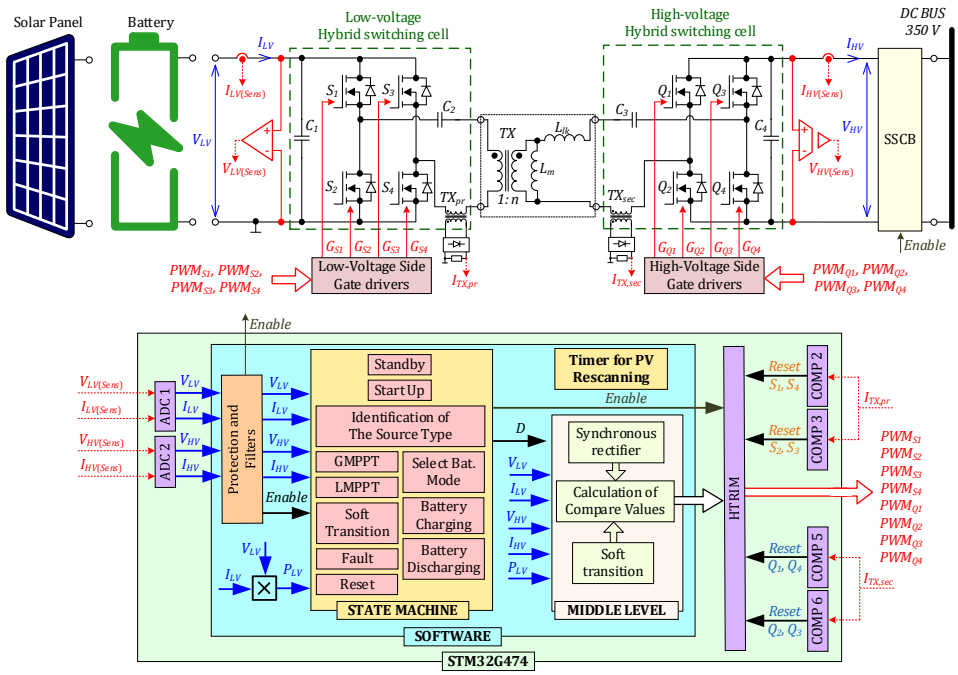


Figure 5.6. Power circuit diagram and control system diagram of the developed UPEI [Paper VI].

The block diagram of the middle-level control system is presented in Figure 5.7. The input control signal for the middle-level control system is a power flow direction and a control variable D, which can be the duty cycles of buck modulations D_{bk} or the duty cycles of boost modulations D_{bt}. The mode selector automatically chooses a control modulation depending on low and high voltages and a required power direction. Furthermore, the mode selector changes a control modulation when the duty cycle achieves saturation.

5.2 Photovoltaic Operation Mode

The first high-level control mode is the PV mode. In this mode, the converter only operates in the forward power direction and the wide voltage range.

5.2.1 Maximum Power Point Tracking

For harvesting maximum energy from a PV module under any conditions, the UPEI should track a global maximum power point. Among the different tracking approaches, the voltage sweep GMPPT has been selected as a simple, effective, and robust algorithm, which does not require knowledge of the electrical characteristics of a PV module and can operate with different types of PV modules [64].

The operation principle of the voltage sweep GMPPT tracking is based on scanning a power-voltage curve of a PV module by decreasing the reference voltage $V_{LV(\mathrm{ref})}$ of a closed-loop control system from the open-circuit voltage $V_{LV(OC)}$ to the minimum operation voltage V_{MIN} of the converter with a voltage step V_{step}, as shown in Figure 5.8. After reaching the minimum operation voltage V_{LVMIN}, the GMMPT algorithm analyses stored MPP data and finds the GMPP. Then the algorithm transits to the GMPP by setting

the reference $V_{LV(ref)}$ equal to the GMPP voltage. Following this, the control system switches to the local MPPT (LMPPT) based on an improved perturb and observe algorithm to maximize the MPPT efficiency [65].

The closed-loop control system for the GMPPT and the LMPPT algorithms has been realized based on a PI-regulator for controlling the PV voltage (voltage V_{LV} on the low-voltage side) (Figure 5.8). When switching control modulation is in the middle control level, the control system also changes the parameters of the PI-regulator.

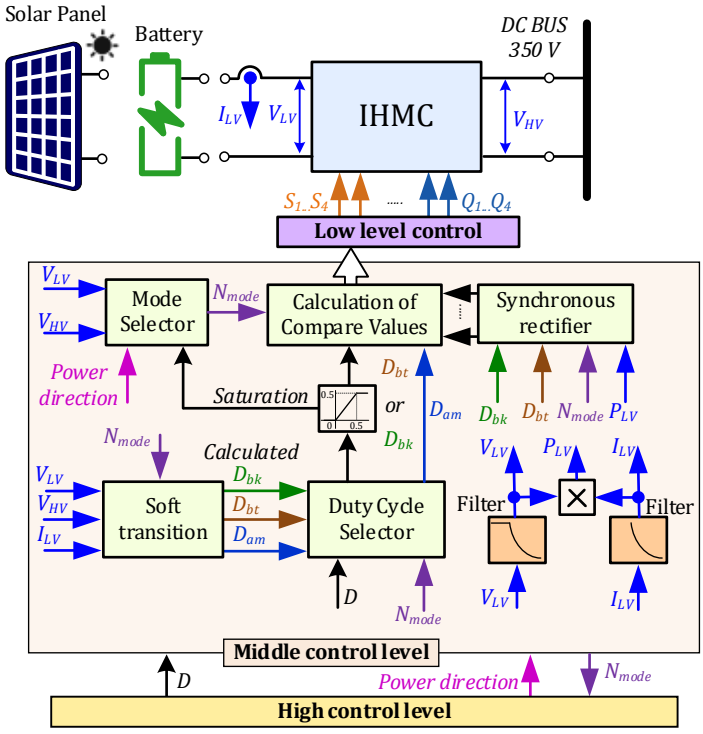


Figure 5.7. Block diagram of the developed middle-level control system [Paper VI].

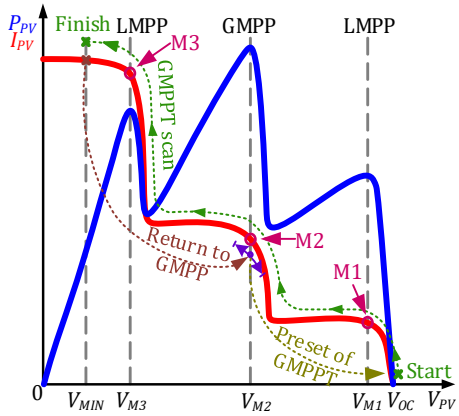


Figure 5.8. Tracking process of the used GMPPT algorithm [64].

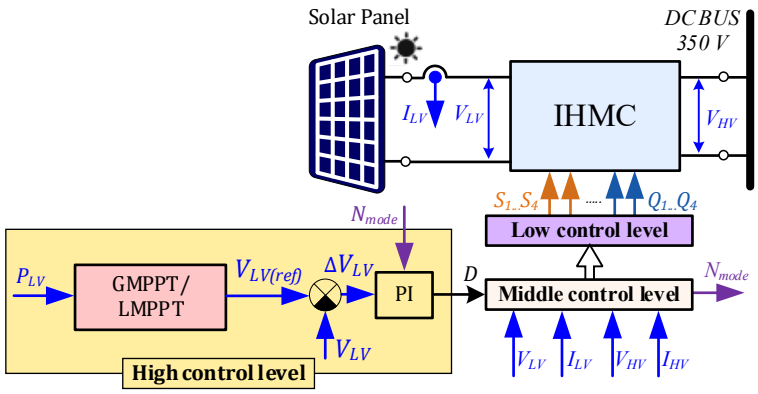


Figure 5.9. Block diagram of the proposed high-level control system in the PV mode [Paper VI].

5.2.2 GMPPT Performance Benchmarking

To verify the UPEI performance in operation with different PV modules, the Solar Array Simulator Keysight E4360A was used to emulate the following PV modules: Longi LR4-60HBD-350M [66] and Longi LR4-72HBD-425M [67]. ITECH IT6006C-800-25 Bi-directional Power Supply emulated the dc microgrid. The following measurement equipment was used in the experiments: oscilloscope Tektronix DPO7254, differential voltage probes Tektronix P5205A, current probes Tektronix TCP0030A, and PEM ultra-mini CWT015.

Figure 5.9 represent the soft transition algorithm. Figure 5.10 shows the scanning of the LR4-72HBD-425M PV module under a cold weather conditions when the open-circuit voltage of the PV module achieves the highest value ($V_{LV(OC)}$ = 57 V). The pre-set voltage ramp changes the reference voltage between the PV open-circuit voltage and the converter minimum operating voltage. During the scanning, the middle-level control system switches through all the control modulations from the buck HBI-FBR to the boost FBI-HBR. This experiment also verifies the continuous operation of the UPEI in the wide voltage range.

The soft transition algorithm allows the control system to recharge series capacitors and change topology configurations smoothly while keeping the voltage and current at the low-voltage side at the same value during the transitions. There are small oscillations in the voltage after transitions, but they do not influence GMPPT scanning since the control system is waiting for the low voltage stabilization before it continues the scanning.

The experimental results in Figure 5.11 verify the performance of the GMPPT algorithm under a partial shading condition. The algorithm correctly finds the GMPP within the scanning time interval t_{scan} = 62 ms. After achieving the minimum voltage, the control system returns to the GMPP and switches to the LMPPT algorithm. The return time t_{return} equals 23 ms. Therefore, the total time of PV scanning required 85 ms.

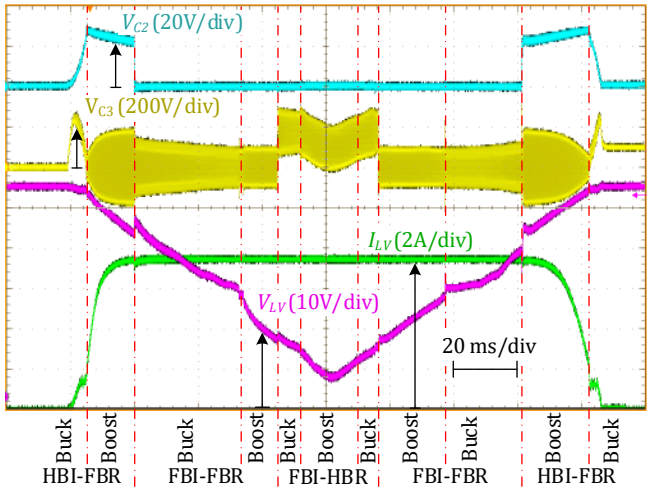


Figure 5.10. Scanning of the LR4-72HBD-425M PV module under a cold weather conditions with irradiation of 800 W/m².

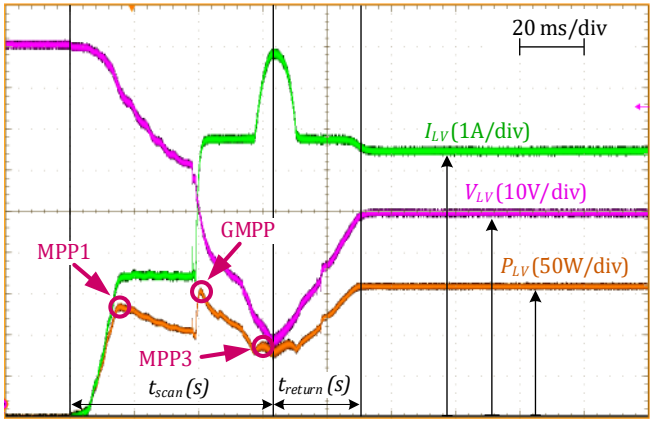


Figure 5.11. Tracking performance of the voltage sweep GMPPT algorithm with the LR4-72HBD-425M PV under following shading profiles of the three substrings: 800/600/300 W/m² [Paper VI].

5.2.3 Daily PV Energy Yield Tests

To verify the operation of the UPEI with different types of PV modules in variable conditions, two case study mission profiles were synthesized using real measured data of the solar irradiance and ambient temperature.

The first profile has been measured under the Nominal Operating Cell Temperature (NOCT) condition with a maximum solar irradiation of 800 W/m² and a maximum temperature of 47 °C (Figure 5.12a). The second profile demonstrates the solar irradiation of a PV module under partial shading from a neighboring building (Figure 5.12b). In the second case, one substring of a PV module is shaded during a part of the day when only 25% of the overall irradiance reaches it in the form of diffuse solar irradiance. It only operates under full irradiance during the morning and evening.

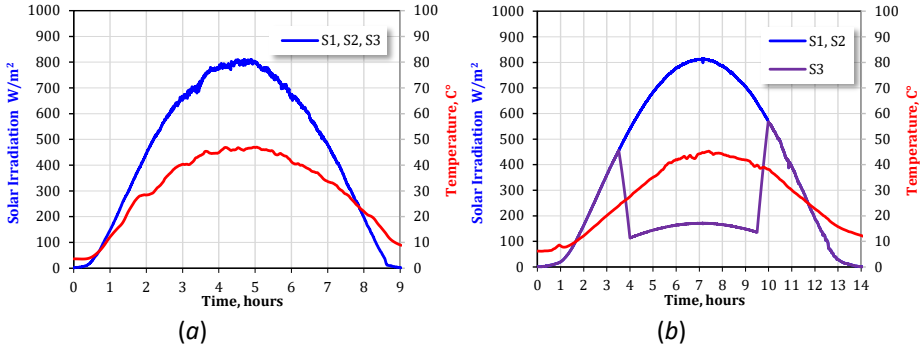


Figure 5.12. Daily profiles of solar irradiance and a PV cell temperature under NOCT conditions (a) and partial shading from a neighboring building (b).

Four daily tests have been completed to verify the performance of the UPEI with different types of PV modules. Figure 5.13a and Figure 5.14a show experimental results of UPEI operation with LR60-350M and LR72-425M PV modules, respectively, under the NOCT condition. The performance of the UPEI with chosen PV modules under partial shading conditions is shown in Figure 5.13b and Figure 5.14b.

All these figures consist of the following parts:

1) The red curve is the maximum available power from a PV module in the GMPP; the blue curve is the power drawn by the UPEI.
2) The red curve is the voltage of GMPPT; the blue curve is the real voltage of the PV module.
3) The magenta curve is the efficiency of MPPT.
4) The red curve is the efficiency of the UPEI.

The UPEI tracks the GMPP with average MPPT efficiency of around 99.5% in each test. As can be seen, the control system rescans P-V curves of a PV module every 30 minutes to find the GMPP. In the case of the partial shading profile, there are small deviations between maximum available power and real power when the converter is stuck at the previous MPP until the next rescanning. The data were logged with a time step of 200 ms, which is less than the scanning time. Therefore, the rescanning process is not completely visible in the figures.

It can be seen that, with the decreased power, the converter efficiency decreases at the end of the tests. It is primarily associated with disabling the synchronous rectification by the control system. At the beginning of the tests, the synchronous rectifier is enabled after reaching the required power.

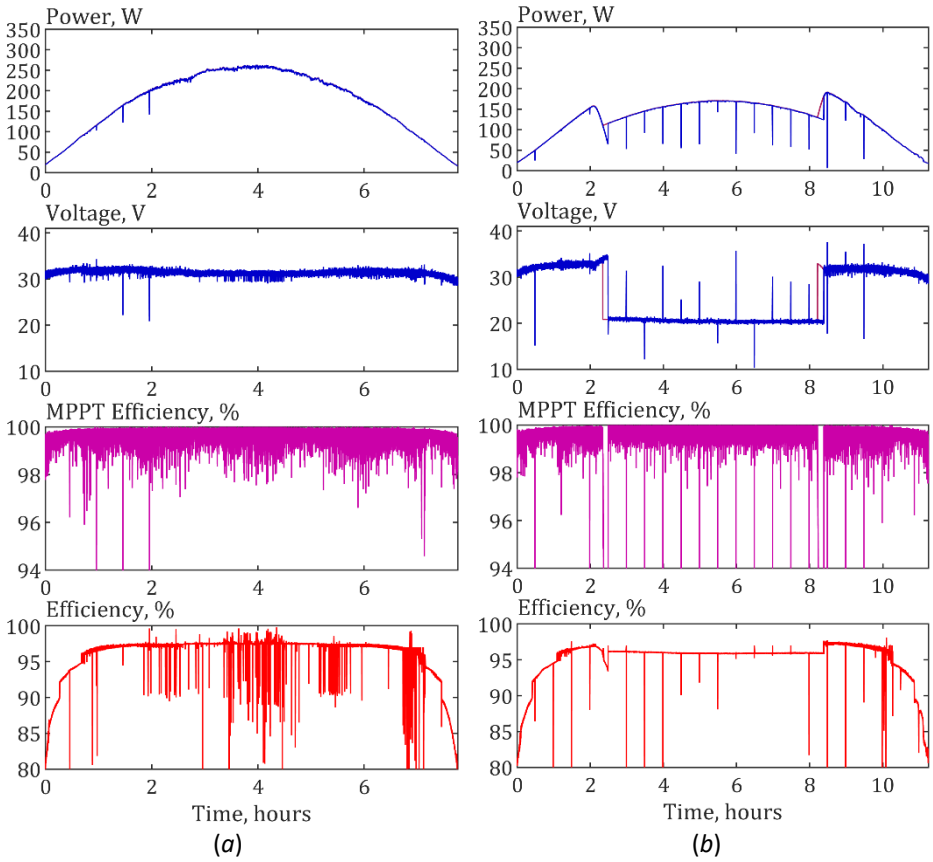


Figure 5.13. UPEI operation with LR60-350M PV module under the NOCT conditions (a) and the synthesized partial shading from a neighboring building (b).

As the numerical result of the daily tests, Table 5.1 shows the following measured and calculated values, which have been presented in [Paper VI]: available PV energy in the GMPP E_{GMPP}, the energy harvested by the UPEI E_{PV}, and the energy delivered to the dc microgrid E_{DC}. In addition, MPPT efficiency E_{PV}/E_{GMPP}, the converter efficiency E_{DC}/E_{PV}, and the overall efficiency E_{DC}/E_{GMPP}. As can be seen, the daily MPPT efficiency E_{PV}/E_{GMPP} is around 99.5%. The efficiency of the UPEI E_{DC}/E_{PV} during daily tests is around 96%. Considering these two efficiencies, the overall system efficiency is around 95.5%.

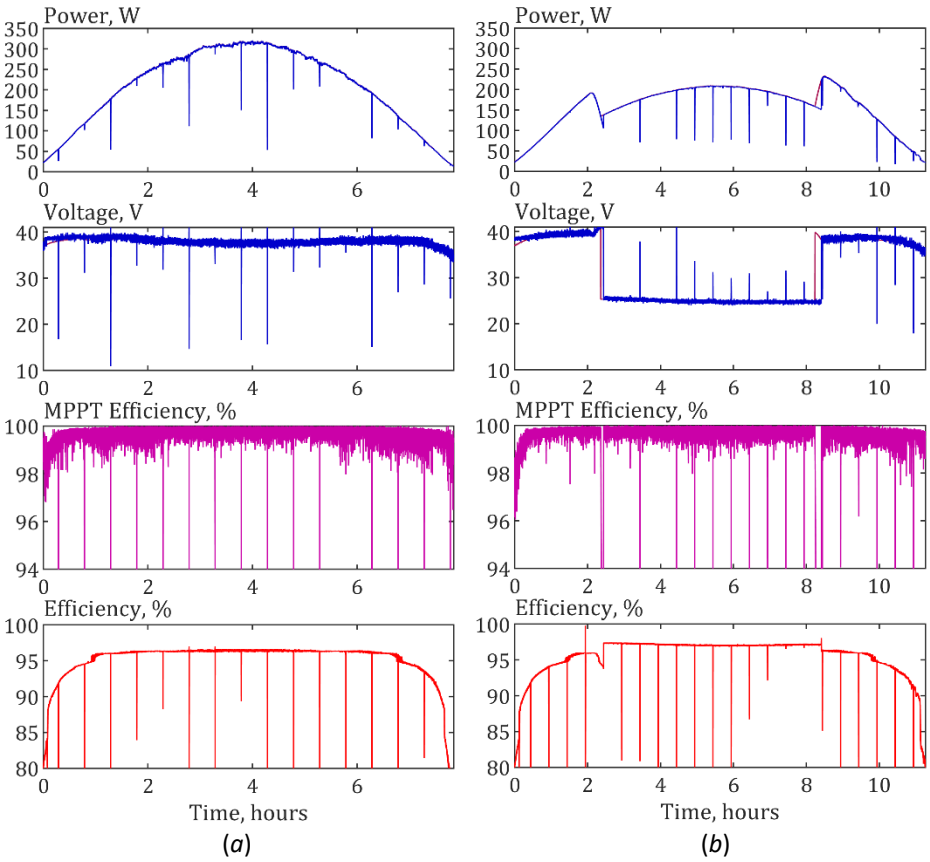


Figure 5.14. UPEI operation with LR72-425M PV module under the NOCT conditions (a) and the synthesized partial shading from a neighboring building (b).

Table 5.1 Daily Operation of the UPEI Two PV Modules Under Different Conditions [Paper VI].

Energy and Efficiency	Profile and Type of PV module			
	NOCT		Build shade	
	60 cells	72 cells	60 cells	72 cells
E_{GMPP}, Wh	1355	1648	1478	1801
E_{PV}, Wh	1351	1644	1465	1788
E_{DC}, Wh	1312	1577	1403	1719
E_{PV}/E_{GMPP}, %	99.7	99.8	99.1	99.3
E_{DC}/E_{PV}, %	97.1	95.9	95.7	96.1
E_{DC}/E_{GMPP}, %	96.8	95.7	94.9	95.5

5.3 Battery Operation Mode

5.3.1 Application of Droop Control

In the battery mode, the UPEI operates with bidirectional power flow. For sharing power naturally between parallel converters and stabilizing voltage of the dc microgrid without any communication in the dc microgrids, the droop control has been applied in the battery mode, as described in [Paper VI] and [68] in detail. The idea of the droop control is based on the derivation of the power reference value that linearly depends on the dc-bus voltage deviation from the nominal value.

The block diagram of the high-level control system in the battery mode is shown in Figure 5.15. The control system is designed based on the PI regulator to control a battery current (low-voltage current I_{LV}). As with the PV mode, the PI regulator parameters change with control modulations and the direction of the power flow.

Depending on the voltage of the dc microgrid, the droop control block sets a reference battery power $P_{LV(ref)}$. The state of charge (SoC) block recalculates the reference power to the reference current $I_{LV(ref)}$. However, the SoC block can limit the battery current if the SoC of the battery is out of the range [5%:95%].

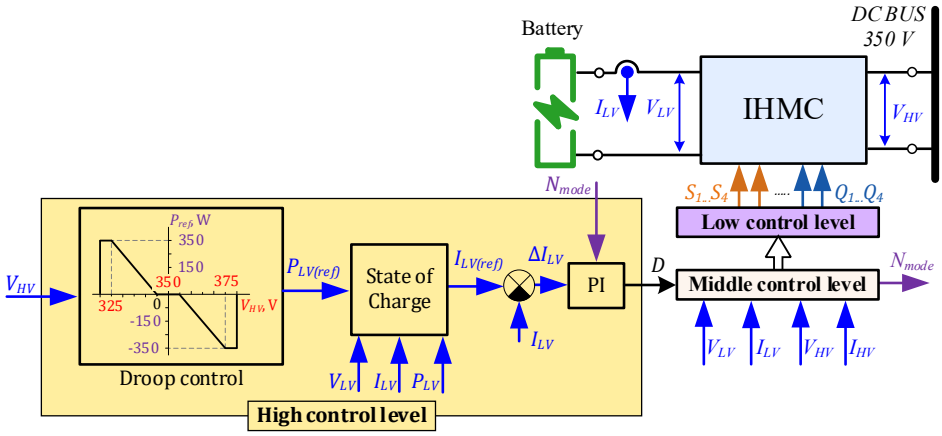


Figure 5.15. Block diagram of the high-level control system in the battery mode [Paper VI].

5.3.2 Performance Benchmarking of the Droop Control

For validating the performance of the UPEI in the battery mode, two batteries, Power Brick+ 24V 32Ah LiFePO4 [69] and Power Brick+ 48V 25Ah LiFePO4 [70], have been selected. The dc microgrid and selected batteries were emulated in experimental tests by two ITECH IT6006C-800-25 Bi-directional Power Supplies. The experimental result in Figure 5.16 shows the operation of the UPEI with the 48 V LiFePO4 battery under droop control. As can be seen, the control system regulates the low-voltage current and changes the polarity of the current without any significant spikes and oscillations.

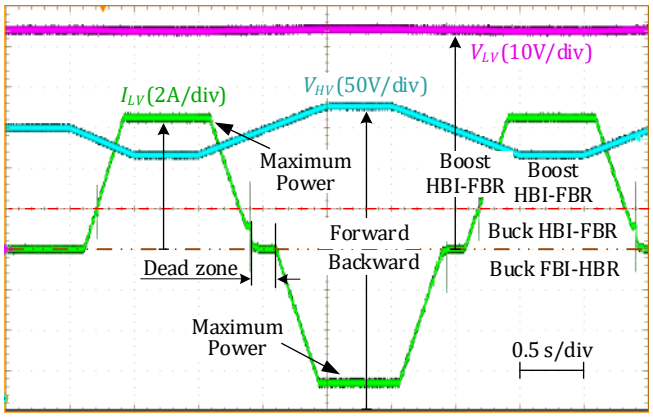


Figure 5.16. Operation of the UPEI with 48 V LiFePO4 battery according to droop control [Paper VI].

5.3.3 Daily Tests of UPEI with 24 V and 48 V Batteries

The 24-hour test of the UPEI with the 24V 32Ah LiFePO4 battery is presented in Figure 5.17. A similar test with the 48V 25Ah LiFePO4 battery was shown in [Paper VI]. To synthesize a daily profile of dc microgrid voltage, a measured daily load profile of a house (the first plot in Figure 5.17) and a measured daily profile of PV generation (the second plot in Figure 5.17) have been used. The power consumption profile has two recognizable maximums of 3.4 kW and 3.3 kW at 7 a.m. and 6 p.m., respectively, i.e., during breakfast and dinner hours. To cover the energy consumption of the house, it was considered that 15 PV modules are connected to the residential dc microgrid.

According to droop control, the synthesized voltage of the dc microgrid is linearly proportional to the difference between consumption and generated power (the third plot in Figure 5.17). When the generated power is higher than the consumption, the dc microgrid voltage is higher than the nominal value of 350 V. In the opposite case, the voltage is below the nominal value. At the power difference peaks, the dc microgrid voltage is within the 320 V to 380 V range.

As Figure 5.17 shows, the UPEI transferred energy from batteries to the dc microgrid. When the dc microgrid voltage increases up to 355 V, the UPEI switches to charging mode to draw PV energy to batteries. The SoC of the battery was limited in the range [5%:95%]. The experimental result showed that the efficiency of the UPEI was around 97% during the 24-hour test.

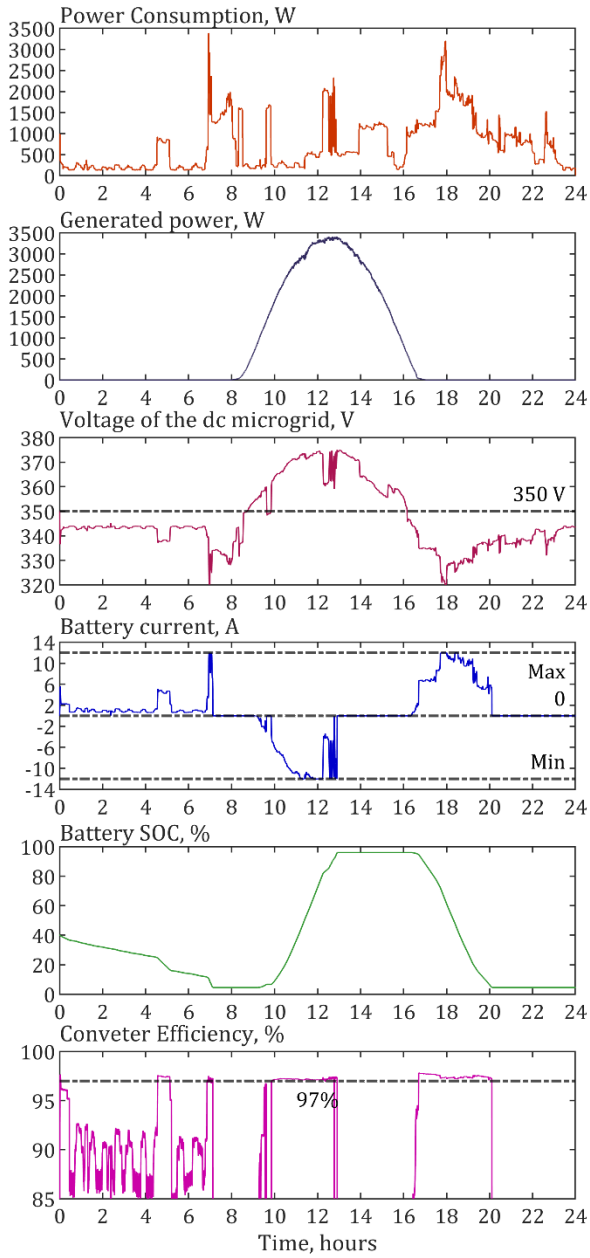


Figure 5.17. UPEI operation with Power Brick+ 24V 32Ah LiFePO4 battery for 24 hours.

Transferred energy and efficiency of the UPEI have been calculated in [Paper VI] and listed in Table 5.2 for two battery types. It lists calculated energy transferred to batteries from the dc microgrid and energy transferred from batteries to the dc microgrid. In the case of charging from 5% to 95% of SoC, the efficiency of the UPEI $E_{BAT(ch)}/E_{DC(ch)}$ equals 96.3 % and 97.6% in the cases of 24 V battery and 48 V battery, respectively. In the discharging mode, the converter efficiency (from 95% to 5% of SoC) $E_{DC(disch)}/E_{BAT(disch)}$ equals 97.3% and 97.5%. The round trip efficiency $E_{DC(disch)}/E_{DC(ch)}$ demonstrates how

much of the stored energy was returned to the dc microgrid. It includes converter efficiencies in both modes and battery efficiency. As Table 5.2 shows, the roundtrip efficiency equals 87.7% and 88.5% for 24 V and 48 V batteries, respectively.

Table 5.2 Daily Operation of the UPEI Two PV Modules Under Different Conditions [Paper VI].

Operation mode	Energy and Eff.	Batteries	
		24V 32Ah	48V 25Ah
Charging (from 5% to 95%)	$E_{DC(ch)}$, Wh	-841	-1179
	$E_{BAT(ch)}$, Wh	-809	-1151
	$E_{BAT(ch)}/E_{DC(ch)}$, %	96.3	97.6
Discharging (from 95% to 5%)	$E_{BAT(disch)}$, Wh	757	1071
	$E_{DC(disch)}$, Wh	737	1044
	$E_{DC(disch)}/E_{BAT(disch)}$, %	97.3	97.5
Round trip	$E_{DC(disch)}/E_{DC(ch)}$, %	87.7	88.5

5.4 Source Identification Algorithm

5.4.1 Description of the Algorithm

The UPEI must be capable of identifying the input energy source type. Hence, the source identification algorithm has been developed and described in detail in [Paper VI].

The operation principle of the identification algorithm is based on scanning the I-V characteristic of a connected input source and calculating the differential conductance $\Delta I_{LV}/\Delta V_{LV}$. The differential conductance of a PV module is not linear: 1) $\Delta I_{LV}/\Delta V_{LV} \ll 0$ from the $V_{LV(OC)}$ to the maximum power point (MPP); 2) $\Delta I/\Delta V < 0$ at the MPP; 3) $\Delta I/\Delta V \approx 0$ after the MPP. In the case of a battery, the $\Delta I_{LV}/\Delta V_{LV}$ is virtually constant for one condition of the state of charge, and its absolute value is much higher than that of any PV module.

The scanning process starts from an open-circuit voltage $V_{LV(OC)}$ and the minimum duty cycle for a selected control modulation by the middle-level control system. By increasing the duty with the step ΔD, the control system measures the voltage and current and calculates the differential conductance $\Delta I_{LV}/\Delta V_{LV}$ value of the input power source, and analyses the data. The flowchart of the source identification algorithm is shown in Figure 5.18.

If the low-voltage current achieves the maximum value $I_{LV(max)}$, the control system switches to the battery charging/discharging mode, depending on the high voltage value. If the control system reaches the MPP during the scanning, the control system switches to the PV mode and continues the GMPPT scanning until the minimum voltage $V_{LV(min)}$ is achieved. The algorithm also identifies the type of the connected PV module (60-cells or 72-cells) or battery (24 V or 48 V).

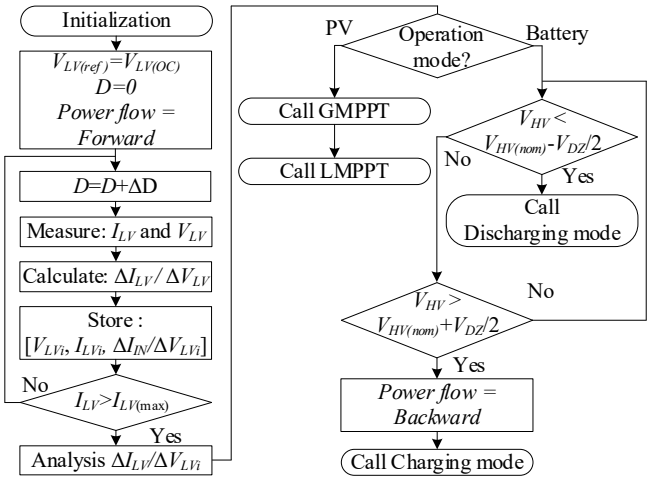


Figure 5.18. Flowchart of the developed input source identification algorithm [Paper VI].

The high-level control system sets the duty cycle for the middle-level system directly during the identification process. Figure 5.19 show the block diagram of the high-level control system. The algorithm uses measured and filtered values of voltage and current from the low-voltage side to calculate a differential conductance of a connected energy source.

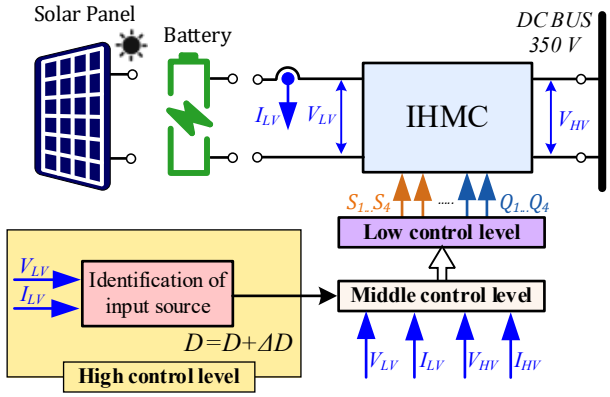


Figure 5.19. Block diagram of the high-level control system implementing the proposed identification algorithm [Paper VI].

5.4.2 Experimental Verification of the Input Source Identification Algorithm

To verify the performance of the identification algorithm experimentally, the UPEI has been tested with the LR4-72HBD-425M PV module and the 48V/25Ah battery. The experimental results are shown in Figure 5.11 and Figure 5.20, respectively.

In the case of the PV module, the algorithm scans the I-V curve of the PV module until the first MPP is achieved. Then the high-level control system switches to the GMPPT algorithm and continues scanning the I-V curve. The algorithm takes 18 ms to identify the PV module.

In the case of the battery, the control system gradually increased the battery current up to the maximum value. During the scan, the middle-level control system switches control modulations from the forward buck HBI-FBR to the forward boost HBI-FBR without significant battery current distortions. After achieving the maximum current, the control system switches either to the charging mode (Figure 5.20a) or the discharging mode (Figure 5.20b). It sets the reference power depending on the voltage of the dc microgrid. In the case of the charging mode, the battery current dropped to zero as fast as possible, and then the control system switched to the backward buck FBI-HBR mode. In the first case, the scanning and return times took 48 ms and 154 ms, respectively. In the second experiment with the battery, the scanning and return times equal 31 ms and 2 ms, respectively.

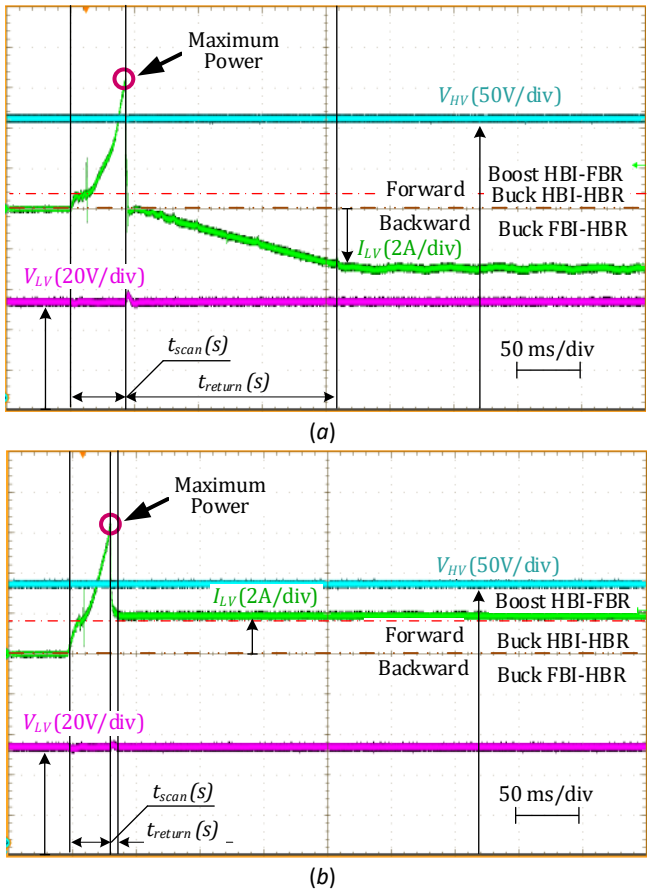


Figure 5.20. Identification of the battery and tracking performance of the discharging mode at V_{HV} = 330 V (a) and the discharging mode at V_{HV} = 370 V (b) [Paper VI].

5.5 Summary

The author has provided conclusive experimental proof of the high performance of the designed UPEI in the wide voltage range from 10 to 60 V with different PV modules and batteries. The topology morphing control allowed the converter to achieve an efficiency higher than 94% and 93% in the forward and backward power flows, respectively. This result further proves the hypothesis that the SRIBBC based on hybrid H-bridge switching cells with series capacitors can be used as a universal tool for uni- and bi-directional applications without hardware modifications.

The author has proposed a versatile control system for the UPEI, which has a hierarchical three-level architecture. The firmware of the UPEI developed by the author includes the following algorithms: the soft transition, the identification algorithms, global and local maximum power point tracking, state of battery charge estimation, constant current/constant voltage charging and discharging, and fault protection. The developed source identification algorithm allows the UPEI to automatically recognize input source type by observing its differential conductance while avoiding sizable input current and voltage distortions. The obtained results conclusively prove the feasibility and effectiveness of the input source type identification hypothesized by the author.

The daily tests verify high flexibility of the developed algorithms and quantify the performance of a UPEI operating with 60- and 72-cell PV modules and 24 V and 48 V LiFePO4 batteries. In the case of PV modules, the overall daily efficiency, including the MPPT and the converter efficiencies, is in the range of 94.9 to 96.8%. The daily roundtrip efficiency of the prototype equals 96.3% and 97.6% for 24 V and 48 V LiFePO4 batteries, respectively, in the charging mode, and 97.3% and 97.5% in the discharging mode.

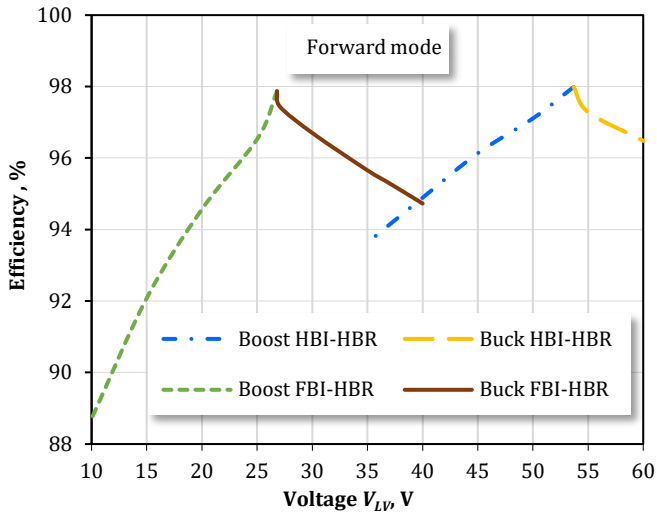
These results justify the universality of the developed converter as the front-end interface. The UPEI is able to harvest maximum energy from various solar modules under different partial shading conditions or save it in battery energy storage with high efficiency. Thanks to the TMC and the transformer based on the hybrid split bobbin, the prototype of the UPEI has a simple topology based on only one magnetic component.

6 Future work

This work has shown how the topology morphing control extends the voltage dc gain range of galvanically isolated dc-dc converters without any changes in hardware. The author demonstrated how this feature could be utilized to develop the universal front-end interface converter with a wide low voltage range from 10 to 60 V for connecting different PV modules and low-voltage battery energy storages to the dc microgrid. However, the TMC can also extend UPEI operation to be compatible with two voltage standards of dc microgrids, namely 350 and 700 V. The voltage standard of 700 V provides an opportunity for managing more energy in a dc microgrid. This type of dc microgrid can be utilized in industrial buildings.

To double the output high voltage, the topology of the converter should operate in the HBI-HBI and the FBI-HBR configurations in the forward power flow. Therefore, the HBI-HBR and the HBI-FBR topology configurations are used in the backward mode. The efficiency curves of the UPEI in both power direction modes are shown in Figure 6.1. As can be seen, the efficiency of the UPEI is higher than 90% at V_{HV}=700 V in the most probable operation range. This result has been achieved with the same components and without any changes in the prototype.

The control system does not require any significant change for operating with two standards of dc microgrids. The mode selector in the middle-level control system calculates the voltage gain based on measured low and high voltages. In the case of V_{HV}=700 V, the mode selector automatically sets the required control modulation and topology configuration. However, the voltage sensor should be able to measure high voltage correctly from 320 to 760 V. Therefore, the high-voltage transistors, the series capacitor, and the filter capacitor should be rated for the maximum voltage of 760 V.



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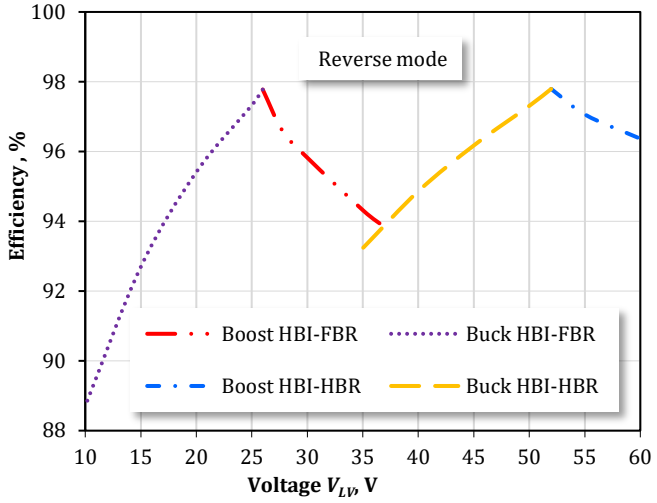

(*b*)

Figure 6.1. Experimental efficiency of the UPEI operating at V_{HV}=700 V in the forward (a) and the backward (b) power flows at the borders of the safe operating area.

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Abstract
Universal Galvanically Isolated DC-DC Converters with Topology Morphing Control

This PhD thesis is dedicated to the development of a novel concept in power electronics – a high-efficiency universal front-end interface converter for the integration of PV modules and battery energy storages into residential dc microgrids.

In this work, the topology morphing control (TMC) was justified as a tool for the performance enhancement of power electronic converters. This term defines a special class of control techniques relevant to power electronic converters based on changing the converter topology by modifying its modulation sequence.

The combination and classification of various TMC techniques were provided. From the literature review, low-cost TMC techniques have been selected for the realization of a bidirectional isolated buck-boost converter based on the series resonant topology. The active switching cells in the low and high voltage side allow for applying buck and boost control modulation to control voltage gain smoothly. As a result, the synthesized converter operates under six control modes in each direction, combining topology configurations and control modulations. A methodology for calculating the dc voltage gain and power losses has been developed, which shows deviations between theoretical and experimental power losses of less than 10%.

The benchmarking of control modulations based on the comprehensive analysis of the operating modes and power losses was performed. The hybrid phase-shift and asymmetric pulse-width modulations are the best for voltage buck operation of the FBI-FBR/ FBI-HBR and the HBI-FBR topology configurations, respectively. The phase-shift and asymmetric pulse-width modulations are selected for voltage boost operation of the FBI-FBR/HBI-FBR and the FBI-HBR topology configurations, respectively. In addition, a soft transition algorithm was proposed to avoid current/voltage stress transitions between topology configurations and verified experimentally in both power flow directions.

A prototype of the universal front-end interface converter was built to be compatible with different PV modules and battery types. In the case of the battery, the droop control algorithm is used for power flow balancing in dc microgrids. Furthermore, the algorithm for the identification of the input source type was proposed in this study. The algorithm can detect the type of connected input energy source, such as a PV module or a battery, based on scanning an I-V curve and estimating the differential conductance of the input source.

The test results show a substantial practical value of the proposed concept. Daily tests with 60- and 72-cells PV modules showed that the overall daily efficiency of the developed prototype, including the MPPT and the converter efficiencies, is in the range of 94.9–96.8%. The daily efficiency of the prototype with 24 V and 48 V LiFePO4 batteries equals 96.3% and 97.6%, respectively, in the charging mode, and 97.3% and 97.5% in the discharging mode.

The theoretical findings substantially contribute to the field of galvanically isolated dc-dc converters by creating and organizing the knowledge regarding the topology morphing control techniques. In turn, the practical results demonstrate the benefits of the topology morphing control and provide useful solutions for resolving its drawbacks, such as soft mode transitions. Moreover, the practical results obtained by the author justify the benefits of universal power electronic interface converters and demonstrate their attractiveness for fast deployment of residential dc microgrids to the industry.

Lühikokkuvõte
Universaalsed topoloogiat muutva juhtimisega galvaaniliselt isoleeritud alalispingemuundurid

Doktoritöö käsitleb uudset kontseptsiooni jõuelektroonikas – ülitõhusat universaalset liidesmuundurit PV moodulite ja aku energiasalvestite integreerimiseks eramute alalisvoolu mikrovõrkudesse.

Töös kasutati topoloogiat muutvat juhtimist (TMC) kui vahendit jõuelektrooniliste muundurite jõudluse parandamiseks. TMC kuulub erilisse juhtimismeetodite klassi, mis põhineb muunduri topoloogia muutmisel läbi modulatsiooni meetodi.

Töös esitati erinevate TMC tehnikate kombinatsioonid ja klassifikatsioon. Kirjanduse ülevaate põhjal valiti odavad TMC tehnikad jadaresonantstopoloogiaga kahesuunaline isoleeritud pinget tõstva-vähendava muunduri realiseerimiseks. Madala- ja kõrgepinge aktiivsed lülituselemendid võimaldavad pinge kasvu sujuvaks reguleerimiseks rakendada vähendavat ja tõstvat juhtmodulatsiooni. Kombineerides topoloogia konfiguratsioone ja juhtimismodulatsioone töötab sünteesitud muundur kahesuunaliselt kuues juhtimisrežiimis. Alalispinge võimenduse ja võimsuskadude arvutamiseks on välja töötatud metoodika, mis näitab alla 10 % kõrvalekaldeid teoreetilise ja eksperimentaalse kaovõimsuse vahel.

Analüüsides põhjalikult töörežiime ja võimsuskadusid toodi välja juhtimismodulatsioonide võrdlus. Hübriid-faasinihke ja asümmeetrilise pulsilaiusmodulatsioon on parimaks meetodiks pinge vähendamiseks järgmistes topoloogiates täissildvaheldi-sildalaldi/täissildvaheldi-poolsildalaldi ja poolsildvaheldi-sildalaldi. Pinge tõstmiseks on aga parimaks lahenduseks faasinihke ja asümmeetriline pulsilaiusmodulatsioon. Lisaks pakuti välja sujuv siirdeprotsessi algoritm, et vältida suuri voolu/pinge kõikumisi topoloogia muutmiste vahel. Tulemused kontrolliti eksperimentaalselt kahesuunalise energiavoo korral.

Loodud universaalne liidesmuunduri prototüüp ühildub erinevate päikesepaneelide ja akutüüpidega. Aku puhul kasutatakse alalisvoolu mikrovõrkudes võimsuse tasakaalustamiseks “droop” juhtimisalgoritmi. Lisaks pakuti selles uuringus välja sisendallika tüübi tuvastamise algoritm. Algoritm suudab tuvastada sisendenergiaallika tüübi (näiteks PV-mooduli või aku) tuginedes I-U kõvera skaneerimisele ja allika diferentsiaaljuhtivuse hindamisele.

Katsetulemused näitavad pakutud kontseptsiooni olulist praktilist väärtust. Igapäevased testid 60- ja 72- elemendiliste päikesepaneelidega näitasid, et väljatöötatud prototüübi igapäevane efektiivsus (sisaldades maksimumvõimsuspunkti otsimist ja muunduri kasutegurit) on vahemikus 94,9–96,8%. Prototüübi igapäevane efektiivsus 24 V ja 48 V LiFePO4 akudega on laadimisrežiimis vastavalt 96,3% ja 97,6% ning tühjendusrežiimil 97,3% ja 97,5%.

Doktoritöö tulemused aitavad oluliselt kaasa galvaaniliselt isoleeritud alalisvoolumuundurite valdkonna arengule, luues ja korrastades teadmisi topoloogiat muutvate juhtimismeetodite kohta. Praktilised tulemused näitasid topoloogiat muutva juhtimise eeliseid ja pakkusid ka lahendusi selle puudustele, nagu nt sujuvad siirderežiimi üleminekud. Veelgi enam, autori saadud praktilised tulemused tõid esile universaalsete liidesmundurite eelised ja loovad hea eelduse eramute alalisvoolu mikrovõrkude kiiremaks kasutuselevõtuks.

Appendix

Publication I

V. Sidorov, A. Chub, D. Vinnikov and F. Z. Peng, “Survey of Topology Morphing Control Techniques for Performance Enhancement of Galvanically Isolated DC-DC Converters,” in IEEE Open Journal of the Industrial Electronics Society, vol. 3, pp. 751-777, 2022, DOI: 10.1109/OJIES.2022.3225265.

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Survey of Topology Morphing Control Techniques for Performance Enhancement of Galvanically Isolated DC-DC Converters

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ABSTRACT This article provides a systematic survey on the topology morphing control techniques used in the galvanically isolated dc-dc converters. Existing techniques are broadly categorized based on the part where a converter changes its topology: at the input side, at the output side, and the advanced techniques that cannot be categorized in the first two groups. The techniques span from the simple reconfiguration between the full- and half-bridge switching cells similar to the conventional power supplies with universal ac input to the advanced multitrack topology and reconfigurable resonant tanks. In addition, the described variety of application examples proves the wide application range and versatility of the topology morphing control. These include fault tolerance, efficiency curve flattening, input voltage range extension, and other advantages. Hence, this article provides a single comprehensive source for researchers and engineers willing to enter the topic of topology morphing control.

INDEX TERMS Galvanically isolated dc-dc power converter, series resonant converters, topology morphing control.

I. INTRODUCTION

In recent years, widespread electrification has been considered the primary tool for more efficient energy generation and end-use due to the increase in renewable electric energy generation [1], [2]. DC distribution enables cost-efficient integration of renewable energy sources in comparison with the conventional ac systems [3], [4], [5], [6], [7]. The benefits of dc distribution are already justified in electric ships and vehicles, as well as electric aircrafts [6], [8], [9], [10]. The need for dc-dc converters combined with safety precautions led to intensive studies of galvanically isolated dc-dc topologies [11], [12].

The galvanically isolated dc-dc converters could be broadly categorized into three main classes: voltage–source, current–source, and impedance-source [12]. The voltage–source topologies are widely accepted by industry due to their simplicity, but they cannot withstand short-circuiting of the input capacitors and may require protection from misgatings. Contrary to that, the current–source topologies must avoid switching states that could interrupt the input inductor current. The impedance–source converters allow for any switching state, which increases their voltage regulation flexibility.

All these converters could be designed to be step-up when the output voltage is always higher than the input voltage, step-down when the output voltage is always lower than the input voltage, or step-up/down. From the voltage regulation point of view, the voltage–source topologies are essentially buck converters that have normalized dc voltage gain below one. The current–source topologies are boost converters that have normalized dc voltage gain above one. The impedance–source topologies could be either boost or buck-boost converters. Each converter type has performance limits, like limited input voltage regulation range, poor light load efficiency, power density, etc.

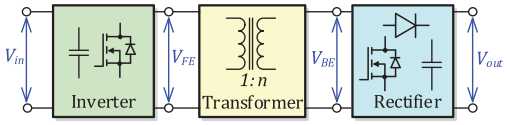

FIGURE 1. Generalized galvanically isolated dc-dc converter.

Optimization of converter hardware design is one possibility to improve converter performance by applying wide bandgap semiconductors or new magnetic materials [13], [14], [15]. Also, topologies could be hybridized to attain the benefits of several converter classes. For example, the buck-boost galvanically isolated dc-dc converter [16] is implemented by combining galvanically isolated boost impedance–source and buck series-resonant voltage–source dc-dc converter topologies.

Other possibilities of hardware design optimization include the following:

1) interleaved implementation of dc-dc converters, which allows for phase shedding at light loads for better efficiency;
2) integration of magnetic elements into a single planar component embedded in a PCB for higher power density;
3) switching frequency increased to MHz level along with soft-switching for high power density.

Converter performance optimization using advanced control is a new trend that provides cost-efficient results [17]. Typically, those are advanced nonlinear techniques, like model predictive control or sliding mode control. However, many converters can have several modes of operation. Therefore, control techniques that take advantage of the best characteristics of each mode are possible. Also, in conventional ac–dc power supplies, a full-bridge rectifier operating in 230 V ac grids can be reconfigured to a half-bridge (the voltage doubler) circuit that can operate in 120 V ac grids. This kind of control could be referred to as the topology morphing control (TMC).

The term "topology morphing control" first appeared in 2015 [18], while some of the concepts covered in this review date back to 2005. The topology morphing control is realized by the online reconfiguration of a converter topology to extend voltage or power ranges or to provide fault tolerance without changing the hardware. The switching between discontinuous and continuous conduction modes is not TMC. Hence, it is essential to provide a systematic survey on this topic to cover different existing converters that can be categorized as those employing the TMC. This survey systematizes and organizes this topic for the first time to provide a single point of reference for engineers and researchers.

Furthermore, the article compares all existing TMC techniques and provides recommendations for applying TMC in different application cases. The article is organized as follows. Section II explains the essence of the TMC. Section III covers the known TMC applications at the input side of galvanically isolated dc-dc converters. Section IV describes different reconfigurable rectifiers that could be utilized on the output side. Other advanced techniques that cannot be categorized in the first two groups are covered in Section V. Section VI illustrates how TMC can be used in the galvanically isolated dc-dc converters and which performance indicators could be improved. Finally, Section VIII concludes this article.

II. MAIN PRINCIPLE OF TMC

Typically, galvanically isolated dc-dc converters consist of a high-frequency front-end inverter, an isolation transformer, and a back-end rectifier (see Fig. 1). Hence, the converter dc voltage gain could be defined as follows:

$$G = \frac{V_{\text{out}}}{V_{\text{in}}} = G_{FE} \cdot G_{TX} \cdot G_{BE} \tag{1}$$

where G_{FE} is the voltage gain of the front-end inverter defined as the ratio between the peak-to-peak voltage applied to the transformer and the double of the input voltage

$$G_{FE} = \frac{V_{FE(pk-pk)}}{2V_{\text{in}}} \tag{2}$$

$G_{TX} = n$ is the turns ratio of the isolating transformer; G_{BE} is the voltage gain of the back-end rectifier defined as the ratio between the double of the output voltage and the peak-to-peak voltage fed by the isolation transformer

$$G_{BE} = \frac{2V_{\text{out}}}{V_{BE(pk-pk)}}. \tag{3}$$

Typically, these gain values are constant. However, applying TMC in any stage allows for regulating these values, typically in integer steps. This article outlines reconfiguration in different stages that can bring different benefits.

Based on these definitions, a classification of TMC techniques could be derived, as shown in Fig. 2. Among the known techniques, the application of two- and three-level full-bridge inverters (FBIs) was found in the literature. The two-level FBIs typically employ reconfiguration from the full-bridge to another mode with less active switches, like half-bridge, flyback, or forward. On the other hand, the three-level FBIs could feature at least three different operation modes. Similarly, multimode rectifiers could be active two- and three-level circuits or passive voltage multipliers with static switches reconfiguring their gain/mode. Some of them can reach up to sixfold gain, but only up to four different modes were observed for some of them in the literature.

Static reconfiguration of the input or output stages is a typical TMC approach. However, more advanced techniques are available too. First, some rectifiers could contain switches controlled at the switching frequency while still providing static dc gain control by changing switching patterns, achieving up to two TMC modes. A wide range of techniques also manipulate the transformer turns ratio G_{TX}. These techniques are referred to as advanced TMC techniques as they typically involve two transformation stages and changing front-end

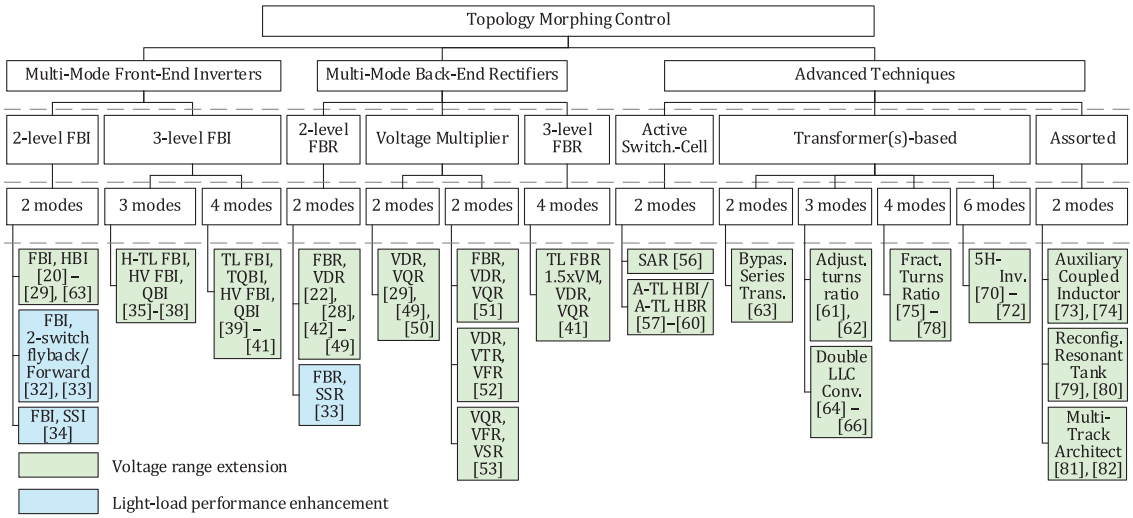

FIGURE 2. Classification of the TMC techniques.

inverter stage switching patterns. Some of them could be complicated due to the implementation of six possible operating modes.

The last group of the assorted advanced TMC techniques is not categorized based on their unique implementation. They include the reconfiguration of the resonant tank using a bidirectional switch, the use of auxiliary inductor winding to establish an additional power transfer link between the input and output sides, and cascaded integration of several typical switching cells to create a versatile multitrack dc-dc architecture.

As shown in Fig. 2, all the techniques included in this survey can be broadly categorized into two main groups. First, most TMC techniques target the dc voltage regulation range extension. However, they could also be used for achieving fault-tolerance when a converter needs to recover its operation by modifying gains of the dc-dc converter parts to compensate for damaged components. On the other hand, some TMC techniques target switching power loss reduction at light load to flatten the converter efficiency curve across its input power range.

The following sections follow the generalized classification of the TMC techniques. Therefore, the next section covers different reconfiguration types of the high-frequency front-end inverter.

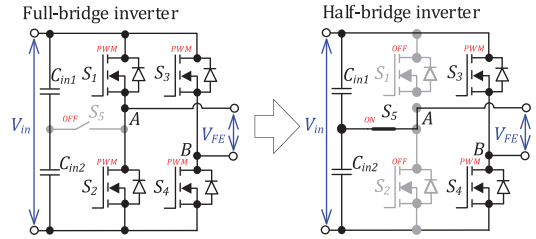

FIGURE 3. Reconfiguration of the front-end inverter with an additional switch from the full-bridge to the symmetrical half-bridge.

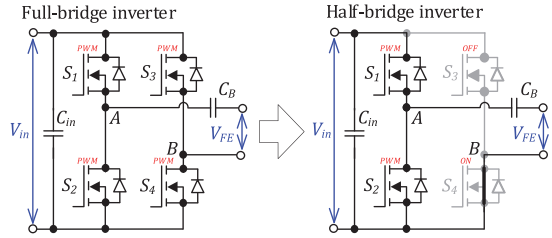

FIGURE 4. Reconfiguration of the front-end inverter with the blocking capacitor from the full-bridge to the asymmetrical half-bridge.

III. INPUT SIDE TMC TECHNIQUES

A. FULL-BRIDGE INVERTER TO HALF-BRIDGE INVERTER

The most widespread example of the TMC at the input side of galvanically isolated dc-dc converters is the reconfiguration from a FBI to a half-bridge inverter (HBI). It can be realized using a capacitor leg (C_{in1} and C_{in2}) and an additional switch S_5 (see Fig. 3), or by a blocking capacitor C_B (see Fig. 4). In the first case, the additional switch S_5 is bidirectional and can be an electromechanical relay or two series MOSFETS [19], [20], [21], [22]. In the FBI mode, the switch S_5 is turned OFF; in the HBI mode, the switch S_5 is turned ON, and one transistor leg (S_1 and S_2) is turned OFF (see Fig. 5).

Usually, the series blocking capacitor is utilized in resonant topologies, such as the LLC, the CLLC, or the series resonant converters (SRC) [19], [23], [24], [25], [26], [27], [28], [62]. In the HBI, one switch in one leg could be turned ON

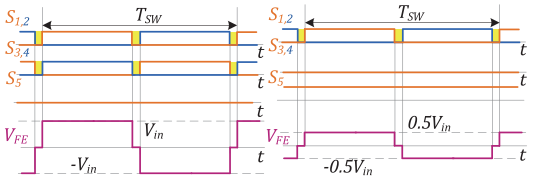

FIGURE 5. Operation of the front-end inverter with an additional switch as (a) FBI and (b) HBI.

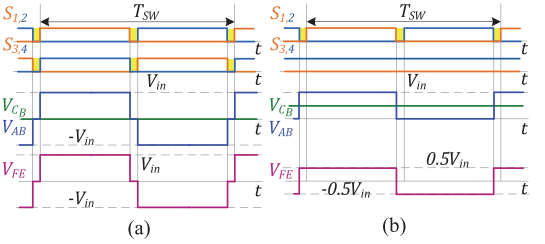

FIGURE 6. Operation of the front-end inverter with the blocking capacitor as (a) FBI and (b) HBI.

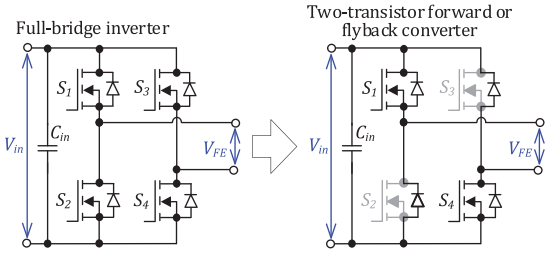

FIGURE 7. Reconfiguration of the front-end inverter from the full-bridge to the two-transistor forward or flyback inverter.

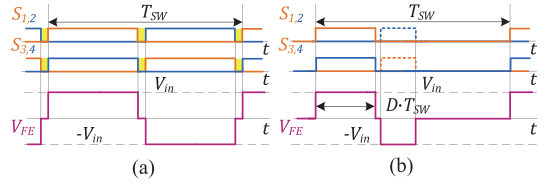

FIGURE 8. Operation of the (a) FBI and (b) two-transistor forward or flyback inverter.

continuously, while the other one is turned OFF. As a result, the average voltage of the blocking capacitor C_B equals half the input voltage. The amplitude of the inverter output voltage equals $V_{FE} = \pm 0.5V_{\text{in}}$ (see Fig. 6). In both cases, the reconfiguration of the inverter from the FBI to the HBI changes the voltage gain G_{FE} from 1 to 0.5. Therefore, the HBI mode can double the input or output voltage range. However, RMS currents in the blocking capacitor, the primary winding of a transformer, and the switch S_4 are increased $\sqrt{2}$ times at the same operating point. It should be considered in the thermal design of the converter.

Frequency modulation (FM) or symmetrical or asymmetrical pulse-width modulations (PWM or APWM) with fixed switching frequency could be applied to regulate the voltage gain in the HBI mode, depending on the converter topology. At the same time, FM and different types of PWM or phase-shift modulations can be applied in the FBI mode [30].

B. FULL-BRIDGE INVERTER TO THE FLYBACK OR FORWARD MODE

In the next example, the TMC is reconfigured from the FBI into the two-transistor forward or the two-transistor flyback converter (see Fig. 7). The type of a reconfigurable converter depends on the type of an isolation transformer. The reconfiguration into the two-transistor forward and flyback converters is exemplified in [31] and [32], respectively. Reconfiguration to the forward or the flyback mode in the light load conditions provides lower switching and gate-driver losses (two switching devices versus four devices). According to the study, these reconfigurations improve the light-load efficiency of a converter by up to 40%. Fig. 8 shows control signals of switches

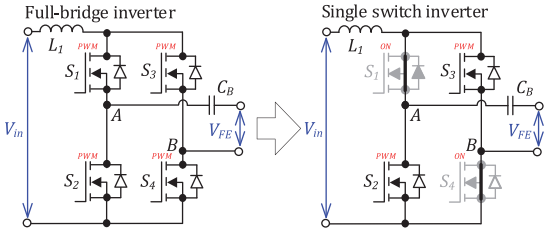

FIGURE 9. Reconfiguration of the front-end inverter from the full-bridge to the single-switch inverter.

in the FBI mode and the two-transistor forward or flyback mode. In the two-transistor forward and flyback modes, body diodes of switches S_3 and S_2 conduct the transformer current when the active switches S_1 and S_4 have been turned OFF and the magnetizing current decreases to zero. It is the main drawback of the two-transistor forward and flyback modes because the forward voltage and reverse recovery losses could be relatively high in the body diodes.

C. FULL-BRIDGE INVERTER TO SINGLE-SWITCH INVERTER

The following example of the TMC is the reconfiguration of the FBI to the single-switch inverter (SSI), as shown in Fig. 9. This TMC is possible only in the current- and impedance-source topologies with an inductor or an impedance-source network at the input, such as quasi-Z-source networks described in [33]. In the SSI mode, diagonal switches (for

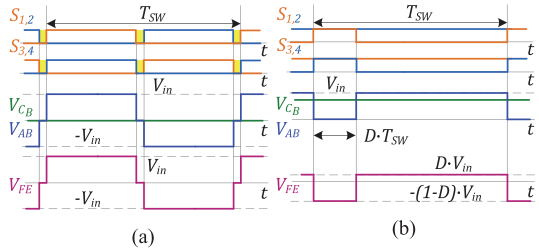

FIGURE 10. Operation of the FBI (a) before and (b) after its reconfiguration into SSI.

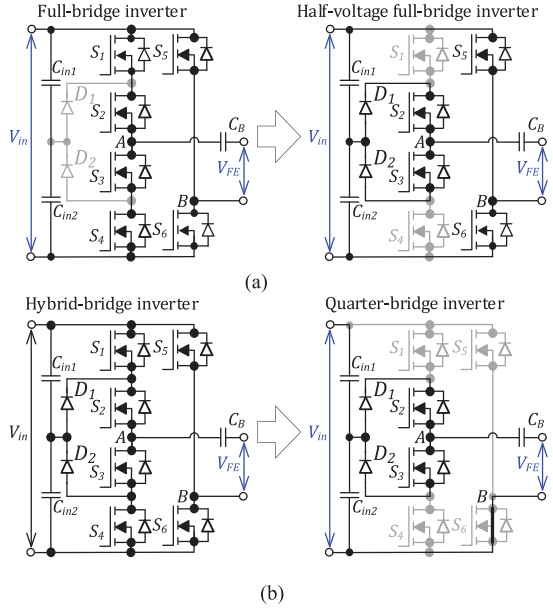

FIGURE 11. Reconfiguration of the hybrid three-level inverter from (a) FBI to HV FBI mode and (b) QBI mode.

example, S_1 and S_4) are turned ON continuously, and the inverter operates as the buck-boost converter with the nominal gain that equals $G_{FE} = 1$ at the duty cycle $D = 0.25$.

The other diagonal switches (S_2 and S_3) are operating during the duty cycle, thus shorting the inverter (see Fig. 10). The blocking capacitor C_B balances the voltage applied to a transformer as in the HBI mode. According to the study [33], the SSI has higher performance at a light load and higher input voltage than the FBI. The main disadvantage of this TMC is high current stress in the diagonal switches S_1 and S_4.

D. HYBRID THREE-LEVEL FULL-BRIDGE INVERTER TO HALF-VOLTAGE FULL-BRIDGE INVERTER AND QUARTER-BRIDGE INVERTER

In high-voltage applications, three-level inverters (TLIs) are a solution to the voltage stress reduction of the switching devices. Though the three-level inverters are complex, low voltage rating power MOSFETS feature low cost, low drain–source ON-state resistance, and low output capacitance. As a result, conduction and switching losses can be reduced compared to a full-bridge converter with high voltage rating power switches. In addition, a complex circuit of the TLI facilitates flexible control and the TMC. The first example of the TMC in three-level inverters is the reconfiguration of a hybrid three-level inverter (H-TLI) from the FBI mode to the half-voltage FBI (HV FBI) mode [34], [35], [36], [37]. Besides, the blocking capacitor C_b allows for operating in the quarter bridge inverter (QBI) mode.

One leg of the H-TLI consists of two transistors like the conventional FBI, and the other leg consists of four switches, two diodes, and two capacitors, as shown in Fig. 11. The operation principle of the H-TLI in four modes is shown in Fig. 12. In the HV FBI mode, half of the input voltage on capacitors $C_{\text{in}1}$ and $C_{\text{in}2}$ is applied between points A and B through a diode D_1 or D_2. In the HV FBI mode, the nominal voltage gain equals $G_{FE} = 0.5$. Also, the H-TLI can operate in the hybrid three-level mode, where the gain is regulated in the range $G_{FE} = 0.5 \ldots 1$ by the variation of a duty cycle D [see Fig. 12(c)]. In the QBI mode, the gain equals $G_{FE} = 0.25$. The H-TLI can operate in three nominal points: $G_{FE} = 1$, 0.5, and 0.25. The main disadvantages of TLIs are challenging converter optimization and the high complexity of the circuits related to the control and driving of switches.

TLIs require many isolated auxiliary supplies for each transistor. Another disadvantage of the H-TLI is that it has two different types of transistors because the voltage stress equals half the input voltage in the first leg and the full input voltage in the other leg.

E. THREE-LEVEL FULL-BRIDGE INVERTER TO THREE-QUARTERS BRIDGE INVERTER, TO HALF-VOLTAGE FULL-BRIDGE INVERTER, AND QUARTER-BRIDGE INVERTER

The latest example of the TMC in three-level inverters is the reconfiguration of the three-level full-bridge inverter (TL FBI), which can operate in four modes: the FBI, the three-quarter bridge inverter (TQBI), the HV FBI, and the QBI mode, as described in [38], [39], [40]. Terms like TQBI reflect the main characteristic of the front-end inverter—its dc-ac voltage gain. TL FBI consists of two four-transistor legs ($S_1 \ldots S_8$), flying capacitors (C_{f1} and C_{f2}), two input capacitors ($C_{\text{in}1}$ and $C_{\text{in}2}$), and four diodes ($D_1 \ldots D_4$).

This example is suitable for high voltage applications with a wide voltage gain range. Flying capacitors help with the voltage balancing across the switches. The voltage of the flying capacitors equals $0.5V_{\text{in}}$. Flying capacitors do not conduct current only in the FBI mode. In the other modes, it is necessary to control the voltage of the flying capacitors by alternating the active transistors. An implementation example of this TMC technique is shown in Fig. 13. The dc-ac voltage gains in the FBI, the TQBI, the HV FBI, and the QBI mode

TABLE 1 Comparison of TMC at the Input Side

TMC	Nominal voltage gain G_{FE}	Number of components[1]			Cost[2]	Advantage	Disadvantage	Application examples		
		S	D	C				Input dc voltage, V	Output dc voltage, V	Power, W
FBI to HBI (Fig. 5)	1; 0.5	4	0	2	$	Voltage gain range extension up to two times	High current stress in one switch	100–400	48	800 [19]
								120–240	24	480 [20]
								30–60	200/400 V	500 [21]
								120–240	96	1000 [22]
								600	180–540	1400 [26]
								150–400	1650	2500 [28]
FBI to 2T-flyback or 2T-forward (Fig. 7)	1	4	0	1	$	Light-load efficiency enhancement (+5 %)	High conduction and reverse recovery losses in body diodes	36	200	20–300 [31]
								20–30	170/ 200–270	10–100 [32]
FBI to SSI (Fig. 9)	1	4	0	L=1	$	Light-load efficiency enhancement (+3 %)	High current stress in the diagonal switches	10–60	400	25–250 [33]
H-TL FBI to HV FBI, to QBI (Fig. 11)	1; 0.5; 0.25	6	2	2	$$	Voltage gain range extension up to four times	Unequal voltage and current stress in switches	200–400	360	1500 [34]
								240–480	30–60	1200 [35]
								385	225–378	6600 [36]
								200–400	60	1200 [37]
TL FBI to TQBI, to HV FBI, to QBI (Fig. 13)	1; 0.75; 0.5; 0.25	8	4	4	$$$	Voltage gain range extension up to six times	High number of switches, unequal current stress in switches	750	50–600	20000 [38]
								100	20–100	500 [39]
								200	200–700	3500 [40]

Note: [1]S=switch; D=diode; C=capacitor; L=inductor.
[2]Estimated cost: $ is a low cost; $$ is a medium cost; $$$ is a high cost.

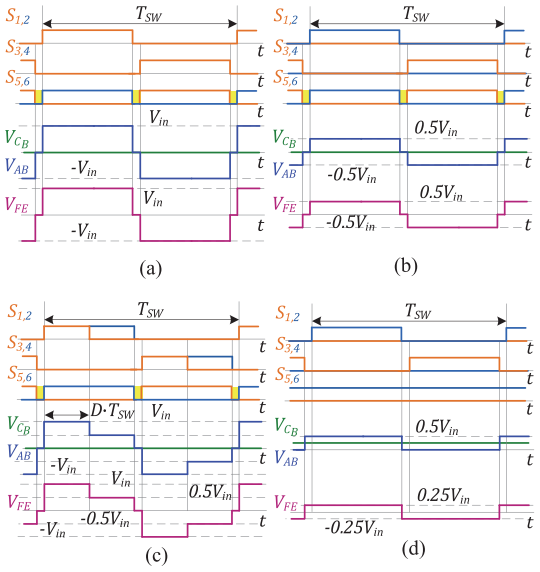

FIGURE 12. Operation of the hybrid three-level inverter as (a) FBI, (b) HV FBI, (c) hybrid three-level inverter, and (d) QBI.

equal 1, 0.75, 0.5, and 0.25 (see Fig. 14), respectively. This TL inverter type features the largest number of nominal voltage gains. However, three-level resonant converters working with a wide input/output voltage range still encounter many difficulties, including high conducting losses, challenging converter optimization, and high circuit complexity related to the control and power stage.

F. SUMMARY

The TMC techniques in the front-end inverters are compared in Table 1. Nominal voltage gain values are reference values that do not consider modulation necessary to achieve gain values between them. The input-side TMC techniques, such as reconfigurations of the FBI to the two-switch flyback or forward mode or the SSI, enhance efficiency at a light load. Other examples extend the voltage gain range and improve performance in a wide range of voltage gain.

The voltage gain extension could be easily achieved in the given techniques as the front-end inverter defines the voltage swing applied to the isolation transformer. However, in some cases, reducing the number of active switches could reduce switching losses at a light load, resulting in efficiency enhancement. The literature shows that two-mode techniques, like reconfiguring the FBI into HBI, could yield sufficient performance for most applications. Multimode topologies derived from TL FBI could be used in niche applications where the dc voltage gain is wide and the maximum operating voltage is high. Considering asymmetrical maximum voltage and current stress of semiconductor devices, future research should target new design approaches tailored to applications by proper dimensioning of the semiconductors and corresponding cooling system.

IV. OUTPUT SIDE TMC TECHNIQUES

TMC can also be applied at the output of galvanically isolated dc-dc converters. Besides, inverters with TMC can operate

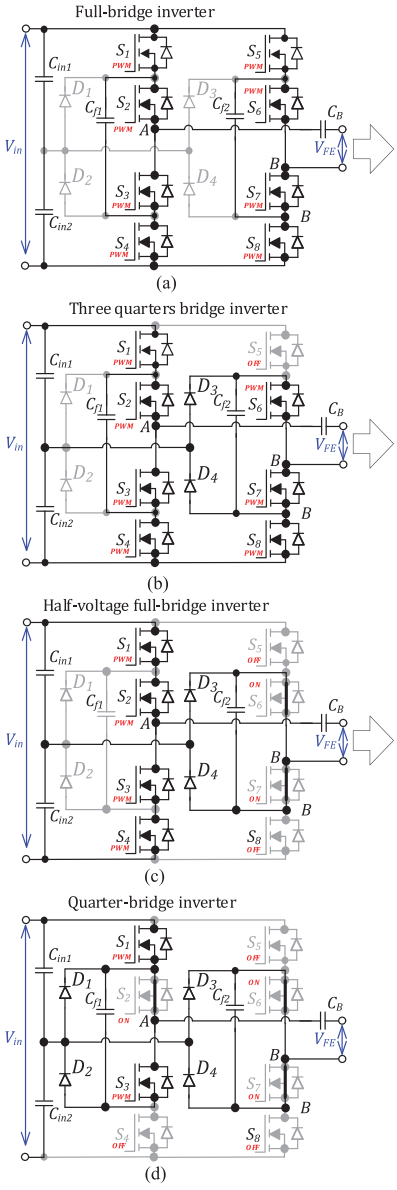

FIGURE 13. Reconfiguration of the three-level full-bridge inverter from (a) FBI to (b) TQBI, to (c) HV FBI, and to (d) QBI mode.

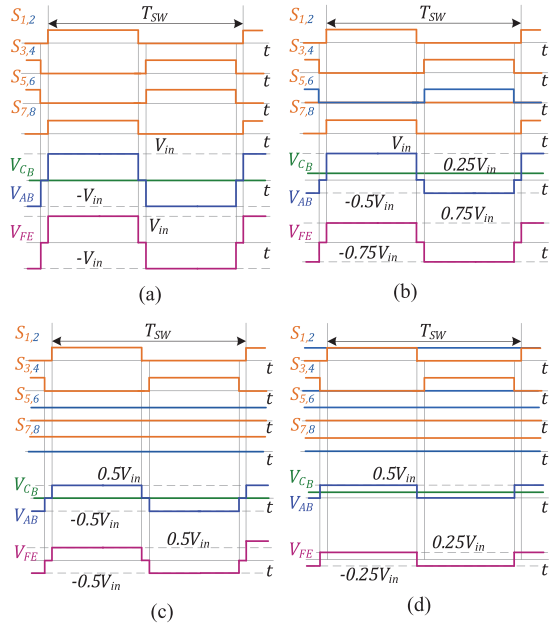

FIGURE 14. Operation of the three-level full-bridge inverter as FBI (a), half-voltage FBI (b), hybrid three-level inverter (c), and QBI (d).

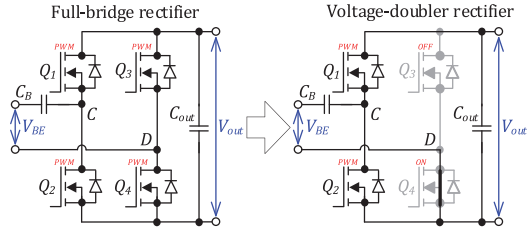

FIGURE 15. Reconfiguration of the back-end rectifier with the blocking capacitor from the full-bridge to the half-bridge.

as a rectifier in the backward power flow direction. In this case, presumably, all examples of the TMC in inverters can be considered for rectifiers.

A. FULL-BRIDGE RECTIFIER TO VOLTAGE-DOUBLER RECTIFIER

The first example of TMC at the output side is a transition from the full-bridge rectifier (FBR) to the half-bridge rectifier (HBR), also known as the voltage-doubler rectifier (VDR). This TMC can be realized by the capacitor leg and an additional switch [41], [42], [43], [44] or the blocking capacitor [21], [27], [45], [46], [48], similar to the FBI–HBI reconfiguration described in the previous section. Fig. 15 shows the reconfiguration from the FBR to the VDR with the blocking capacitor. The rectifier operation after the reconfiguration is the same as the operation of the half-bridge inverter (see Fig. 16). In the FBR mode, all transistors operate as a synchronous rectifier; in the VDR mode, two switches, Q_1 and Q_2, operate as a rectifier. The voltage gain of the rectifier in the FBR mode equals $G_{BE} = 1$, and the gain in the VDR mode equals $G_{BE} = 2$. In the VDR mode, the current stress of the blocking capacitor and the switch Q_4 are two times higher than that in the FBR mode.

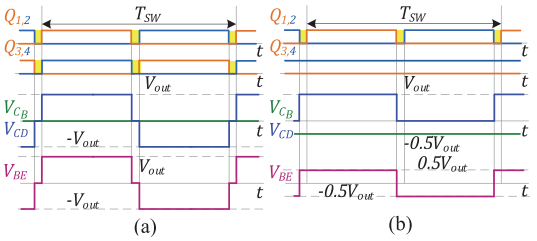

FIGURE 16. Operation of the back-end rectifier with the blocking capacitor as (a) FBR and (b) VDR.

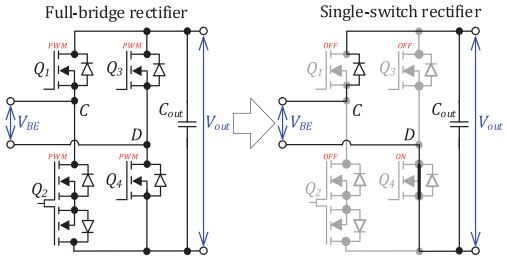

FIGURE 17. Reconfiguration of the back-end rectifier with a bidirectional switch from the full-bridge to the single-switch rectifier.

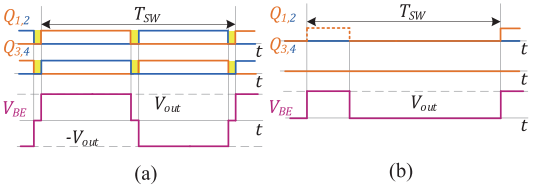

FIGURE 18. Operation of the back-end rectifier with a bidirectional switch as (a) FBR and (b) SSR.

B. FULL-BRIDGE RECTIFIER TO SINGLE-SWITCH RECTIFIER

This TMC technique is based on the rectifier reconfiguration from the FBR to a single-switch rectifier (SSR), also called a half-wave rectifier. Terminology-wise, the SSR shows the duality between TMC application at the input and output sides. This type of TMC requires a bidirectional switch Q_2 in one rectifier leg for blocking this conduction path (see Fig. 17). A switch Q_4 in another leg is turned ON continuously, and the switches Q_1 and Q_3 are turned OFF. Thus, only the body diode of switch Q_1 operates in the SSR mode, or switch Q_1 operates as a synchronous rectifier (see Fig. 18). SSR is suitable for operation as a rectifier of the flyback converter. For example, in [32], the inverter is reconfigured from the FBI to the two-switch flyback converter. At the same time, the rectifier is reconfigured from the FBR to the SSR. This TMC allows for improving performance at a light load. The voltage gain in both modes is the same. However, using the bidirectional switch is a drawback of this TMC technique.

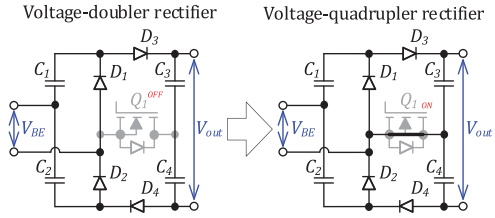

FIGURE 19. Reconfiguration of the back-end rectifier with an NPC switch from VDR to VQR.

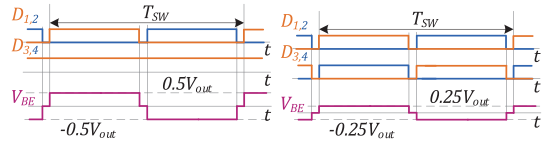

FIGURE 20. Operation of the back-end rectifier with an NPC switch as (a) VDR and (b) VQR.

C. VOLTAGE-DOUBLER RECTIFIER TO VOLTAGE-QUADRUPLER RECTIFIER

The third example of TMC at the output side is the VDR reconfiguration into the voltage-quadrupler rectifier (VQR) [28], [48], [49], as shown in Fig. 19. In this circuit, the NPC switch Q_1 operates in ON/OFF mode and selects the mode of the rectifier. The diodes D_3 and D_4 are required in the VQR mode for blocking the reverse current. The capacitors C_3 and C_4 perform second voltage doubling in the VQR mode and operate as the output filter in the VDR mode. The operation principle of the diodes and the switch under both modes is shown in Fig. 20. In this figure and further in the article, active levels for diodes show when they are expected to conduct current under ideal conditions.

The voltage gain of the rectifier equals $G_{BE} = 4$ in the VQR mode. In the VQR mode, the current stress of the blocking capacitor and the switch Q_4 is two times higher than that in the VDR mode, which is the drawback of this TMC.

D. FULL-BRIDGE RECTIFIER TO VOLTAGE-DOUBLER RECTIFIER AND VOLTAGE-QUADRUPLER RECTIFIER

The combination of the first and the third case of the TMC at the output side is described in [50]. This example shows reconfiguration between the FBR, the VDR, and the VQR (see Fig. 21). The circuit of the rectifier consists of six diodes, four capacitors, two of which are blocking, and two transistors operate in the ON/OFF mode. TMC is implemented by switching the transistors: both transistors are turned off in the FBR mode (but the body diode of the Q_2 conducts current), the transistor Q_1 is turned ON in the VDR mode, and both transistors are turned ON in the VQR mode, as shown in Fig. 22. In some modes, only part of the circuit is operational. For example, diodes D_3 and D_4, the blocking capacitor C_{B2}, and the capacitor C_2 operate only in the VQR mode. At the same

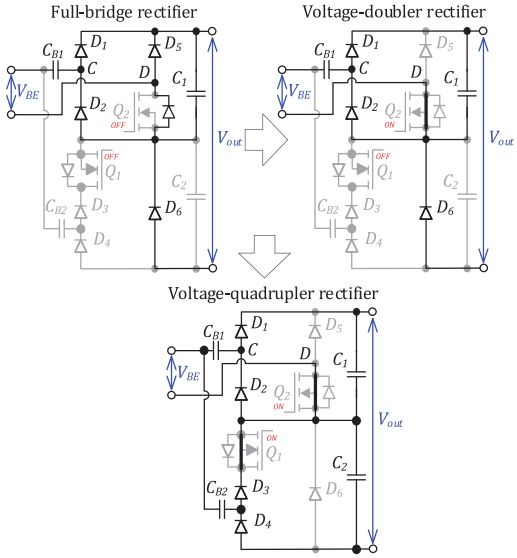

FIGURE 21. Reconfiguration of the three-mode back-end rectifier from the FBR to the VDR and the VQR.

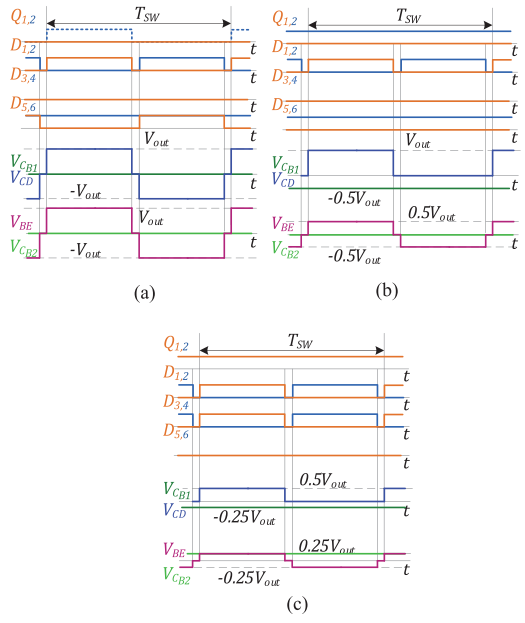

FIGURE 22. Operation of the three-mode back-end rectifier as (a) FBR, (b) VDR, and (c) VQR.

time, the diode D_5 operates only in the FBR mode. The main advantage of this example is the wide voltage gain range of the rectifier, considering that the voltage gain equals G_{BE}=1, 2, and 4. Drawbacks of this approach are a large number

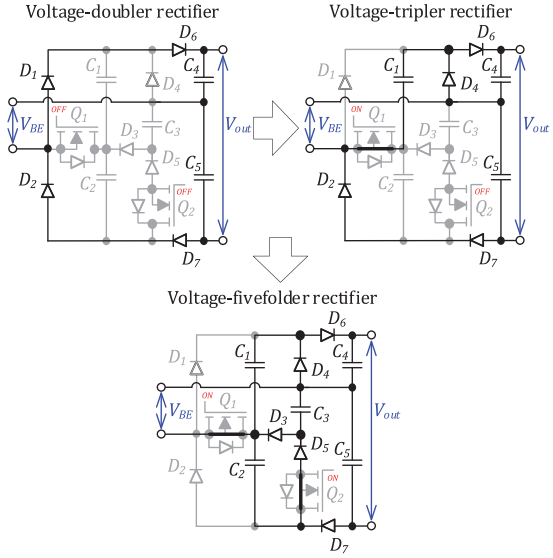

FIGURE 23. Reconfiguration of the three-mode back-end rectifier from VDR to VTR and VFR.

of semiconductor devices, unequal current stress of diodes, and high current stress of components in the VQR mode. In each mode, two diodes and one transistor conduct the current, increasing the parasitic series equivalent resistance of the rectifier. These drawbacks can be neutralized by selecting suitable semiconductor devices and the thermal design of the rectifier.

E. VOLTAGE-DOUBLER RECTIFIER TO VOLTAGE-TRIPLER RECTIFIER AND TO VOLTAGE-FIVEFOLDER RECTIFIER

An alternative implementation of a three-mode rectifier was proposed in [51]. It can operate in the VDR, the voltage-tripler rectifier (VTR), and the voltage-fivefolder rectifier (VFR) modes (see Fig. 23). The proposed rectifier consists of seven diodes, five capacitors, and two transistors. As in previous examples, the transistors operate in the ON/OFF mode and control the rectifier mode. In the VDR mode, both transistors are turned OFF; in the VTR mode, the Q_1 is turned ON; in the VFR mode, both transistors are turned on. Depending on the operation mode, the voltage gain of the rectifier can equal G_{BE} = 2, 3, and 5. Though the voltage gain in the VFR mode is high, the voltage gain range of this reconfigurable rectifier is not as wide as in the previous example. The high number of utilized components is the main drawback of this reconfigurable rectifier. Also, three diodes simultaneously conduct current in the VTR and VFR modes (see Fig. 24). This feature increases conduction losses and requires using Schottky diodes with low forward voltage.

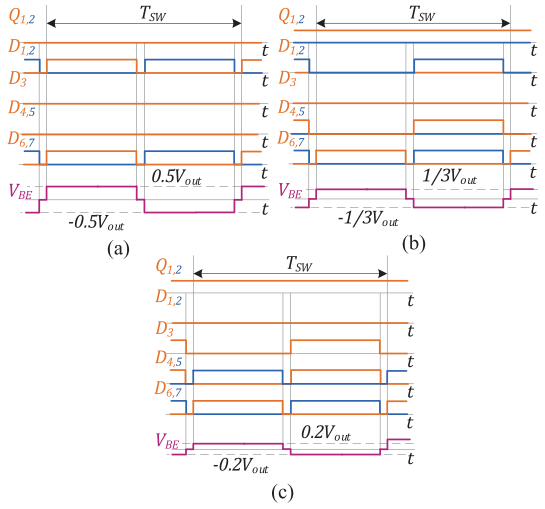

FIGURE. 24. Operation of the three-mode back-end rectifier as (a) VDR, (b) VTR, and (c) VFR.

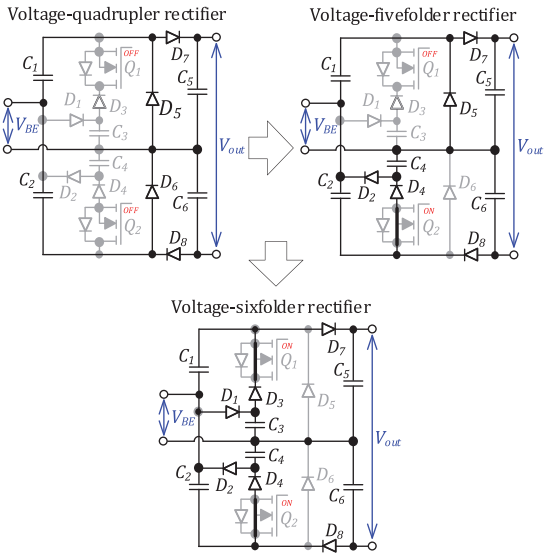

FIGURE 25. Reconfiguration of the three-mode back-end rectifier from VQR to VFR and VSR.

F. VOLTAGE-QUADRUPLER RECTIFIER TO VOLTAGE-FIVEFOLDER RECTIFIER AND VOLTAGE-SIXFOLDER RECTIFIER

The study in [52] presents a rectifier operating in the VQR, the VFR, and the voltage-sixfolder rectifier (VSR) modes (see Fig. 25). Mode is selected by turning ON/OFF the static transistors like in the previous case. Fig. 26 explains the operation of switches and diodes in different modes. In the listed

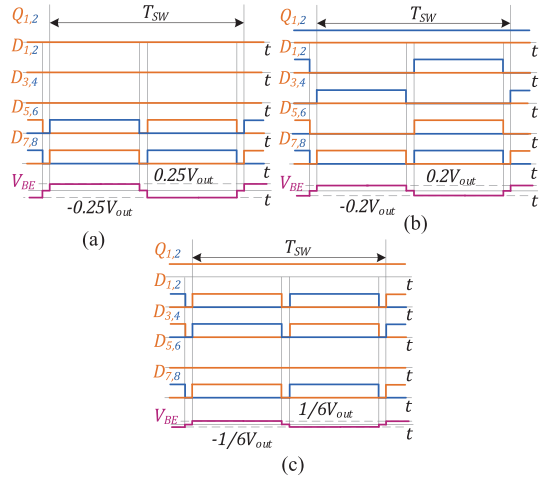

FIGURE 26. Operation of the three-mode back-end rectifier as (a) VQR, (b) VFR, and (c) VSR.

modes, the voltage gain of the rectifier G_{BE} equals 4, 5, and 6. Although the voltage gain has high values, the voltage gain range is not as wide as in the previous three-mode rectifiers. At the same time, compared with the previous examples, component count is the largest: eight diodes, six capacitors, and two transistors, which is a serious drawback of this approach.

G. THREE-LEVEL FULL-BRIDGE RECTIFIER TO 1.5-TIMES VOLTAGE MULTIPLIER, TO VOLTAGE-DOUBLER RECTIFIER, AND VOLTAGE-QUADRUPLER RECTIFIER

In high-voltage applications, three-level rectifiers can be applied to decrease the voltage stress of the components and, as a result, reduce component costs. The three-level inverters, such as the TL HBI and the TL FBI, can be used as rectifiers. An example of using the three-level full-bridge rectifier (TL FBR) is described in [40]. The operation principle is similar to that of the TL FBI. Depending on the modulation, the rectifier can operate as the FBR, the 1.5-times voltage multiplier (1.5xVM), the VDR, or the VQR, as shown in Fig. 27. The voltage gain G_{BE} equals 1, 1.5, 2, and 4 in the mentioned modes. At the same time, the average voltage of the blocking capacitor V_{Cb} equals zero in the FBR and the VDR modes and $0.25V_{\text{out}}$ in the $1.5\times$VM and the VQR modes, respectively (see Fig. 28). The voltage stress of the components is equal to half the output voltage. The drawback of this approach is the highest component count and the most complex circuit of the rectifiers described above.

H. SUMMARY

The topology morphing control in the back-end rectifiers is compared in Table 2. The nominal voltage gain values are defined by the converter operating points when no boost or buck voltage regulation is performed, which is similar to the converter operation as a dc transformer. The dc gain values

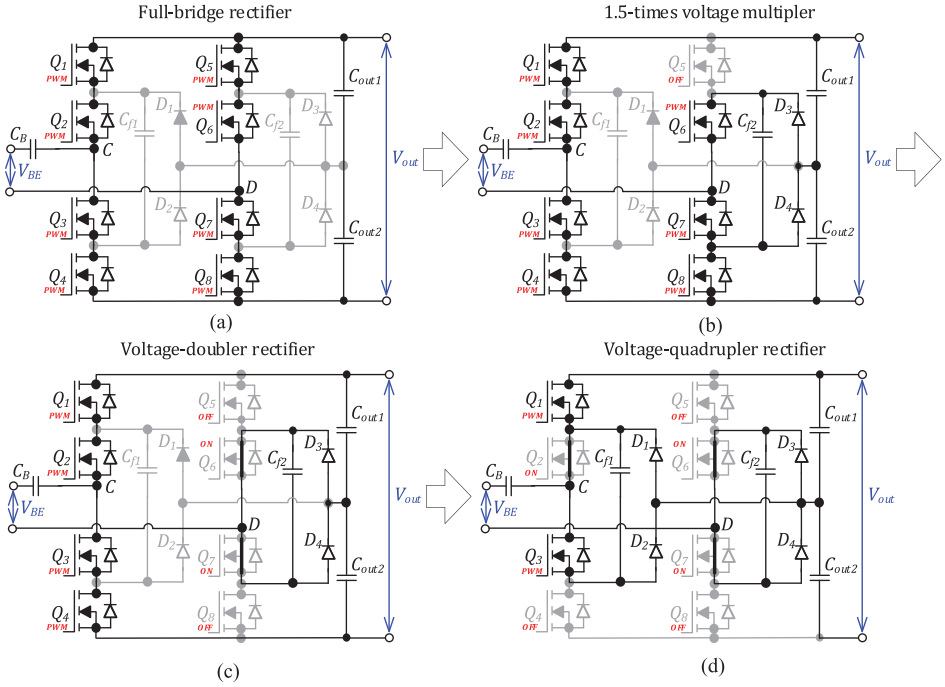

FIGURE 27. Reconfiguration of the three-level half-bridge rectifier from (a) the FBR to (b) the 1.5xVM, (c) the VDR, and (d) the VQR.

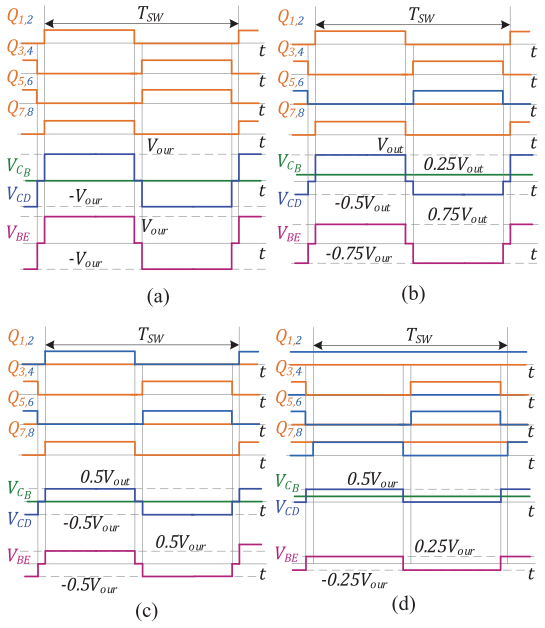

FIGURE 28. Operation of the three-level half-bridge rectifier as the (a) FBI, (b) the VDR, (c) the 1.5xVM, and (d) the VQR.

between them could be achieved only by implementing boost or buck voltage regulation using a pulsewidth or frequency modulation.

Most of the case studies in the techniques surveyed were dedicated to extending the converter gain range, with the fourfold extension being the best-reported result. Only one technique that applies SSR as one of the modes was used to enhance the efficiency, but it was combined with the corresponding input-side reconfiguration. Hence, the resulting efficiency improvement cannot be associated with the rectifier reconfiguration alone. Most of the techniques implement integer steps in the rectifier ac–dc gain G_{BE}, which makes them useful for the extension of the regulation range. The gain steps allow for keeping the control variable of the front-end inverter in the range of favorable efficiency, as it does not need to regulate the input voltage more than twofold before the rectifier changes its mode again. However, the mode changes could result from the considerable input and output voltage or current transients.

These techniques typically yield no significant efficiency improvement. Instead, they allow keeping its values in a wider input voltage range where a converter would not be able to operate due to limits of its input voltage regulation and power loss dissipation. In particular, full-bridge step-up dc-dc converters typically feature efficiency rising with the input

TABLE 2 Comparison of TMC at the Output Side

TMC	Nominal voltage gain G_{BE}	Number of components[1]			Cost[2]	Advantage	Disadvantage	Application examples		
		S	D	C				Input dc voltage, V	Output dc voltage, V	Power, W
FBR to VDR (Fig. 15)	1; 2	4	0	2	$	Voltage gain range extension up to two times	High current stress in one switch and blocking capacitor	30–60	200/400 V	500 [21]
								390	250–450	900
								17–43	340–430	250
								400	100–420	1500
								36–60	340–380	800
								18–36	12	120
								800	200–950	3300 [46]
FBR to SSR (Fig. 17)	1	4	0	1	$	Light-load efficiency enhancement (+8%)	High conduction and reverse recovery losses in body diodes	20–30	170/ 200–270	10–100 [32]
VDR to VQR (Fig. 19)	2;4	1	3	4	$	Voltage gain range extension up to two times	High current stress in one switch and blocking capacitor	150–400	1650	2500 [28]
								300–700	6600	2500 [49]
FBR to VDR, to VQR (Fig. 21)	1;2;4	2	6	4	$$	Voltage gain range extension by 4 times, reduced voltage stress by two times	High number of semiconductors, unequal current stress of diodes, and high current stress of components	5–110	400	360 [50]
VDR to VTR, to VFR (Fig. 23)	2; 3; 5	2	7	5	$$	Voltage gain range extension by 2.5 times, voltage stress by 2 times	High number of utilized components, high current stress in diodes.	25–100	500	250 [51]
VQR to VFR, to VSR (Fig. 25)	4; 5; 6	2	8	6	$$	Voltage gain range extension by 1.5 times	High number of switches, unequal current stress in switches	25–50	760	300 [52]
TL FBR to 1.5xVM, to VDR, to VQR (Fig. 27)	1; 1.5; 2; 4;	8	4	4	$$$	Voltage gain range extension up to four times, reduced voltage stress by 2 times		200	200–700	3500 [40]

Note: [1]S=switch; D=diode; C=capacitor; L=inductor.
[2]Estimated cost: $ is a low cost; $$ is a medium cost; $$$ is a high cost.

voltage, which could result in significant efficiency ripple at the rectifier mode transitions [53]. Such a step in the converter losses at the mode change could compromise the converter reliability due to the thermal cycling of components. Therefore, the reconfigurable rectifiers are much more suitable for application with front-end inverters featuring a reduced number of components, like HBI or SSI, as those feature symmetrical efficiency curves regarding the middle of their duty cycle regulation range. Contrary to this, the resonant converters with dc voltage gain close to one show much lower efficiency variation in their typical regulation range. The application of reconfigurable rectifiers could extend their voltage gain range while keeping a relatively flat efficiency curve.

More complicated circuits based on the three-level FBR could be useful in applications where the output voltage must vary in a wide range, reaching values above the blocking capacity of a single device. An example of such an application could be the electric vehicle charging standard CHAdeMO, which requires the charging voltage range from 50 to 1000 V [54].

The most critical points to be addressed are achieving a smooth transition between the modes and assessment of the associated damage accumulation in the converter components.

V. ADVANCED TMC TECHNIQUES

This section describes advanced TMC techniques not covered in the previous two sections.

A. SEMI-ACTIVE RECTIFIER WITH VARIABLE STRUCTURE

In Sections II and III, examples of static TMC were described. In those cases, some transistors operate in ON/OFF mode and switch an inverter or a rectifier circuit between different modes/topologies. However, there is also an active TMC when all transistors operate in the PWM mode, and the voltage gain of the converter is dependent on the PWM method. In the first example of the active TMC [55], a semi-active rectifier was demonstrated (see Fig. 29), which can operate as the VDR or the VQR depending on the switching patterns shown in Fig. 30. The circuit of the reconfigurable rectifier consists of two transistors, two diodes, and three capacitors. To balance voltage between the capacitors C_1 and C_2 in the VQR mode, the transistors operate sequentially one after the other: Q_1 is turned ON during one period, Q_2 is turned ON during the other period. The advantage of the rectifier with the active TMC is a lower component count than in the similar rectifier with the passive TMC from Section III-C.

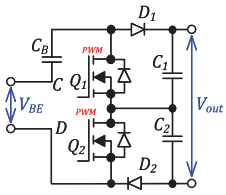

FIGURE 29. Active rectifier with variable structure.

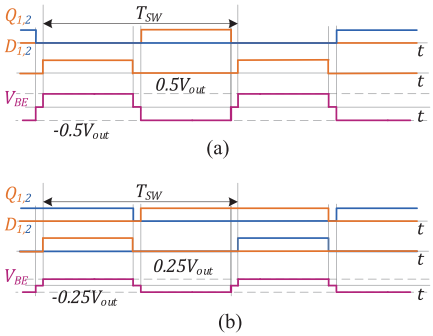

FIGURE 30. Operation of the semi-active rectifier as (a) VDR and (b) VQR.

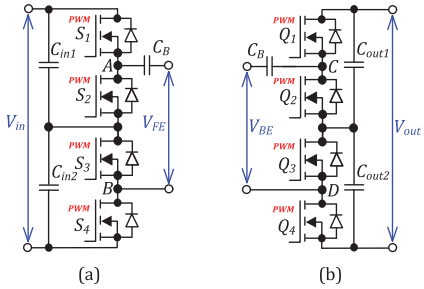

FIGURE 31. Active three-level half-bridge (a) inverter and (b) rectifier.

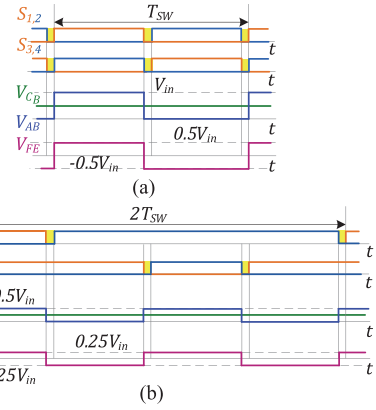

FIGURE 32. Operation of the active TL HBI inverter as (a) HBI and (b) QBI.

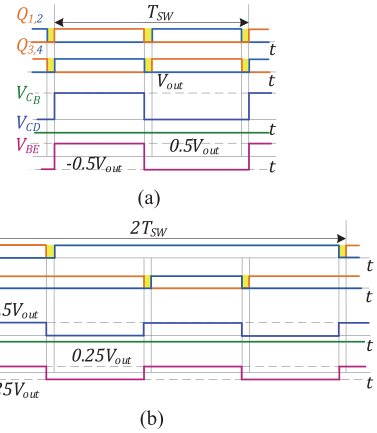

FIGURE 33. Operation of the active three-level half-bridge rectifier as the (a) VDR and the (b) VQR.

B. ACTIVE THREE-LEVEL HALF-BRIDGE INVERTER AND RECTIFIER WITH VARIABLE STRUCTURE

Another example of an active TMC is utilized for the three-level half-bridge inverter and rectifier, as shown in [56], [57], [58], [59]. Fig. 31 shows the topologies of the active TL HBI and the active TL HBR. The inverter and rectifier can operate in the HBI or the QBI mode, i.e., the VDR or the VQR mode, respectively. The circuits and operation principles of the inverter and the rectifier are similar. Therefore, only the operation of the inverter is described below. Half of the input voltage is applied to a transformer by turning ON the transistors S_1 and S_4 simultaneously (see Fig. 32(a)). The zero states in the switching cell are realized by turning ON switches S_2 and S_3. The QBI mode is realized by turning ON transistor pairs S_1 and S_3 or S_2 and S_4 (see Fig. 32(b)). To balance the voltage of the input capacitors C_{in1} and C_{in2} in the QBI mode, two pairs of transistors should be turned ON during equal time intervals. All inverter transistors are switched in this case, but the switching frequency is twice lower than that in the HBI mode. The voltage gain of the TL inverter G_{FE} equals 0.5 and 0.25 in the HBI mode and the QBI mode, respectively. The voltage gain of the TL rectifier G_{BE} equals 2 and 4 in the VDR and the VQR mode, respectively (see Fig. 33). The voltage stresses of the components in the inverter and rectifier equal half the voltage. The main disadvantage of the three-level half-bridge inverter and rectifier is the uneven current stress of the switches in the QBI and the VQR modes.

C. ADJUSTING THE TRANSFORMER TURNS RATIO

Another approach for extending the voltage gain of a converter is adjusting the turns ratio of a transformer by switching transformer tap windings. This simple approach has been applied in power engineering for a long time. The idea is to divide the output-side transformer windings into tapped sections and switch between them. Thus, the turns ratio of

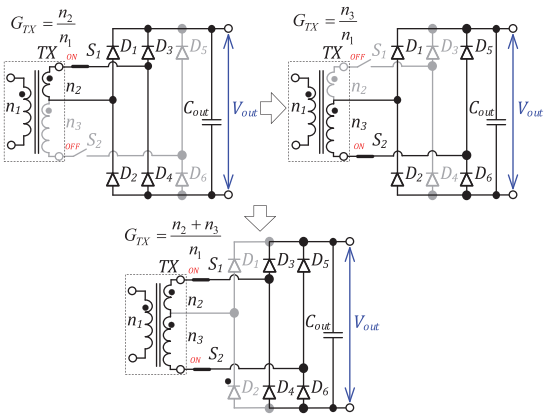

FIGURE 34. Reconfiguration of the transformer with two secondary windings.

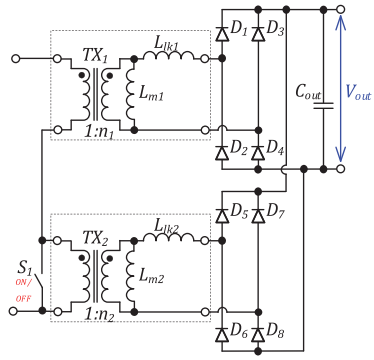

FIGURE 35. Reconfigurable topology with an enabled series transformer.

the transformer can be adjusted. As described in [60] and [61], this approach can also be applied to galvanically isolated dc-dc converters. Bidirectional switches enable or disable secondary windings and connect them to the three-leg full-bridge rectifier. Depending on the states of the switches, the turns ratio of the transformer G_{TX} takes three values, as shown in Fig. 34. Using bidirectional switches is the main disadvantage of this approach since each switch consists of two MOSFETS connected in the back-to-back configuration. In the described circuit, two MOSFETS and two diodes conduct current in two configurations, and four MOSFETS and two diodes conduct current in the third configuration. As a result, the series resistance of the rectifier is higher than that of the conventional FBR. Also, these MOSFETS require isolated drivers, which complicates the control system.

D. BYPASSING A SERIES TRANSFORMER

Besides switching windings of a transformer, switching between parallel transformers or enabling series transformers can be used to extend the range of the dc voltage gain of a converter. Fig. 35 shows a converter with two series transformers and two parallel FBRs proposed in [62]. The bidirectional switch S_1 enables or bypasses the second transformer TX_2, depending on the state of the switch. When the S_1 is turned OFF, the primary windings of the transformers are connected in series. Thus, the total turns ratio of the two transformers equals

$$G_{TX} = \frac{n_1 \cdot n_2}{n_1 + n_2} \tag{4}$$

where n_1 and n_2 are the turns ratio of transformers TX_1 and TX_2, respectively. Thus, enabling the second transformer decreases the total turns ratio and redistributes voltage between two series primary windings. It reduces the flux density in the first transformer when the front-end inverter provides voltage above a certain threshold. This approach was applied to the LLC converter, where enabling the second transformer also increases the equivalent magnetizing inductance of the resonant tank and minimizes the magnetizing current. As a result, the dc voltage gain of the given LLC converter is extended more than two times. However, an obvious disadvantage of the proposed approach is the doubled number of transformers and rectifier diodes compared with the conventional LLC converter.

E. DOUBLE FULL-BRIDGE LLC CONVERTER BASED ON RECONFIGURABLE THREE-LEG INVERTER

Another TMC technique of switching parallel–series transformers is described in [63], [64], and [65]. The proposed converter consists of a three-leg FBI and FBR, and two parallel transformers and series capacitors, which form two resonant tanks (see Fig. 36). The three-leg inverter can operate as the double full-bridge (DFBI) and supply two transformers or operate as the FBI or the HBI while supplying only one of the transformers. In the FBI and the HBI modes, the converter operates like the conventional LLC converter based on one transformer. In the DFBI mode, both resonant tanks operate in parallel, and the total turns ratio of transformers is $G_{GX} = n_1 + n_2$ because the secondary windings of the transformers are connected in series. Thus, the proposed converter operates under three modes, which cover a wide range of voltage gain.

A similar approach is proposed in [66], [67], and [68]. These studies demonstrate the LLC converter based on the dual HBI (DHBI), which operates under two similar modes: the DHBI mode and the conventional HBI mode. The difference between the DFBI and the DHBI is that a capacitor leg replaces a switch leg.

The main drawback of the dual-bridge approach is the double number of components, which is the same as in the previous examples.

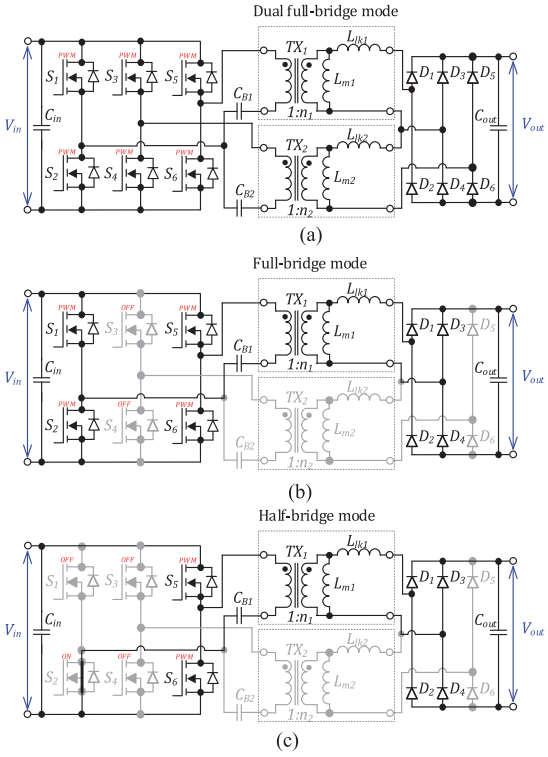

FIGURE 36. Reconfigurable double full-bridge LLC converter from the (a) DFBI to the (b) FBI and the (c) HBI.

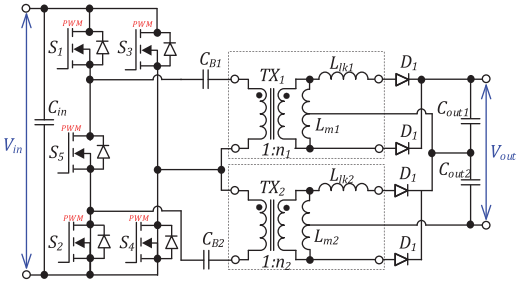

FIGURE 37. Five-switch bridge based reconfigurable converter.

F. FIVE-SWITCH RECONFIGURABLE INVERTER

Another TMC technique employing two transformers is presented in [69], [70], and [71]. Instead of the three-leg inverter, the five-switch bridge inverter (5H-inverter) is utilized along with two transformers. Both transformers are parts of parallel resonant converters, as shown in Fig. 37. The six operation modes of the 5H-inverter are shown in Fig. 38. Depending on the switching sequence, the first or/and second resonant converters operate with the HBI or the FBI. Theoretically, the same number of modes, i.e., equivalent topologies, is possible for the previous example. The main difference between the

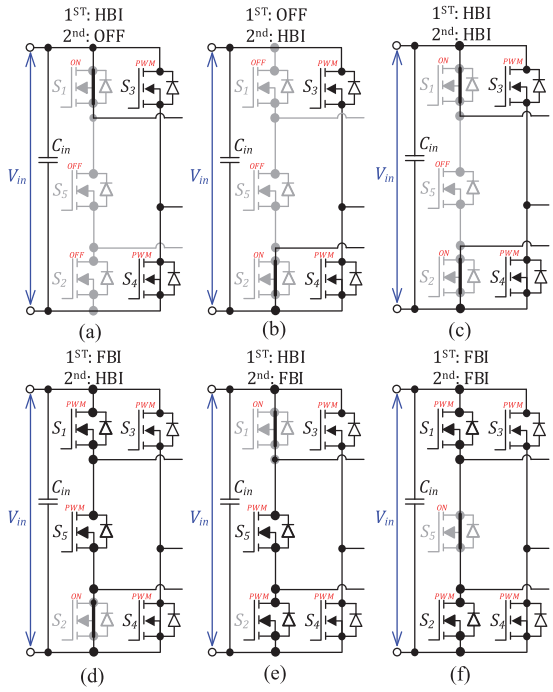

FIGURE 38. Operation modes of the 5H-inverter. (a) HBI / OFF. (b) OFF / HBI. (c) HBI / HBI. (d) FBI / HBI. (e) HBI / FBI. (f) FBI / FBI.

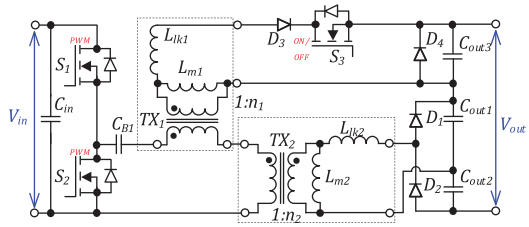

FIGURE 39. LLC converter with an auxiliary transformer and a half-wave rectifier.

DHBI and the 5H-inverter is in the number of switches: six against five.

G. LLC WITH AUXILIARY COUPLED INDUCTOR

In the TMC examples with two transformers described above, the rated power of the transformers in each converter is the same. However, converters with an auxiliary coupled inductor have been proposed in [72] and [73] to extend the voltage gain range of the resonant converters. The auxiliary coupled inductor is connected to a half-wave rectifier (HWR), which consists of diodes D_3 and D_4, and capacitor C_3 (see Fig. 39). When the bidirectional switch S_1 is disabled, the topology operates like the conventional LLC converter with the VDR. The magnetizing inductance of the coupled inductor TX_1 is part of the resonant tank. When the switch S_1 is enabled,

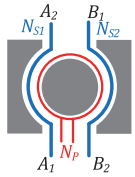

FIGURE 40. Transformer with secondary fractional turns.

the output voltage will be equal to the summed outputs of the HWR and VDR. The drawback of this approach is the power loss in the auxiliary coupled inductor even when the HWR is disabled because the resonant current flows through the primary winding of the inductor TX_1.

H. TRANSFORMERS WITH A FRACTIONAL TURNS RATIO

Another approach of TMC in the transformer stage is proposed in [74], [75], [76], and [77]. In their approach, a transformer with fractional turns ratio is utilized as an isolation transformer in the LLC converter. Dividing flux from the transformer turns allows for achieving a fractional turns ratio. It can be used in step-up/down applications with a high turns ratio for decreasing the number of turns. The proposed transformer has N_P total turns wound on the primary side and two secondary turns implemented from half turns (see Fig. 40). Each secondary half-turn is connected to an FBR through a blocking capacitor, as shown in Fig. 41.

Each rectifier can operate in the FBR, the HBR, or the zero mode. When both rectifiers operate in the FBR mode, the effective turns ratio of the converter equals N_P:0.5. The combination of operation modes in the rectifier gives four different effective turns ratios: N_P:0.5, N_P:2/3, N_P:1, N_P:2, achieved by combining FBR and FBR, FBR and HBR, HBR and HBR, and HBR and the zero modes, respectively. Implementation of the transformer with fractional turns requires a specific design. The examples described in the literature are based on planar cores with the printed circuit board (PCB) turns to optimize the size of converters. The PCB-based implementation could reduce the production cost of such converters. However, this TMC technique requires high semiconductor component count and associated circuitry.

On the other hand, an advanced planar transformer design along with an active TL HBI at the input and two active FBR cells at the output side resulted in the variable–inverter–rectifier–transformer concept [74]. It is the ultimate example of the TMC in the galvanically isolated dc-dc converters, providing numerous operating modes and, consequently, significantly extending the range of voltage gain regulation.

I. RECONFIGURABLE RESONANT TANK

Apart from controlling the resonant inductance and the equivalent turns ratio of transformers in the LLC converters, the TMC can be applied to the resonant tank. Studies in [78] and [79] describe modified resonant converters, where the LLC resonant tank could be reconfigured to the LLCC resonant tank. As can be seen from Fig. 42, a bidirectional switch controls the type of the resonant tank. When the switch is turned ON, the converter operates as the LLCC topology. When the switch is turned OFF, it operates like the conventional LLC topology. It allows for extending the voltage gain range while operating within a narrow switching frequency range. The described approach is one of the simple methods for extending the voltage gain range in the LLC converters.

J. MULTITRACK CONVERTER ARCHITECTURE

Another scalable and reconfigurable architecture of galvanically isolated dc-dc converters employing the TMC is presented in [80], [81]. Its simplest embodiment, the two-track converter, consists of the switched inductor (boost) circuit, hybrid double inverter, and isolation stage (with two transformers). The switched inductor circuit operates as the boost converter when the input voltage is less than V_X, where V_X and $2V_X$ are two related intermediate bus voltages, as shown in Fig. 43. When the input voltage is between V_X and $2V_X$, the switch S_3 is turned ON continuously and S_4 is turned OFF, while the switches S_1 and S_2 balance voltages of capacitors C_1 and C_2. The hybrid inverter consists of switches $S_{5\ldots8}$, capacitors $C_{1\ldots3}$, and blocking capacitors C_{B1} and C_{B2}. The inverter structure implies operation with a dual-primary-winding transformer or two parallel transformers. The proposed TMC technique is based on merging several typical converter stages. It allows for operating in a wide voltage gain range and optimizing current and voltage stress in the components. The simplest implementation of the multitrack architecture requires at least eight transistors, each with the galvanically isolated auxiliary supply for the driving circuit, which limits its use in practice.

K. SUMMARY

Table 3 compares advanced TMC techniques and demonstrates advantages, disadvantages, typical voltage and power for each technique. The nominal voltage gain value in the table takes into account the voltage gain of a converter at a nominal voltage. As can be observed, the given techniques all target the voltage gain range extension. There is a distinct group based on using multiple transformers and reconfiguring their connections. The flexibility of these techniques depends on the combination of their turns ratios, which are restricted by the regulation range of the original topology. Also, some of the advanced TMC techniques use very complex topologies that could be justified only for niche applications where the achieved flexibility could rationalize the cost of implementation.

VI. TMC IMPLEMENTATION EXAMPLES

This section focuses on the implementation of the TMC in practical applications.

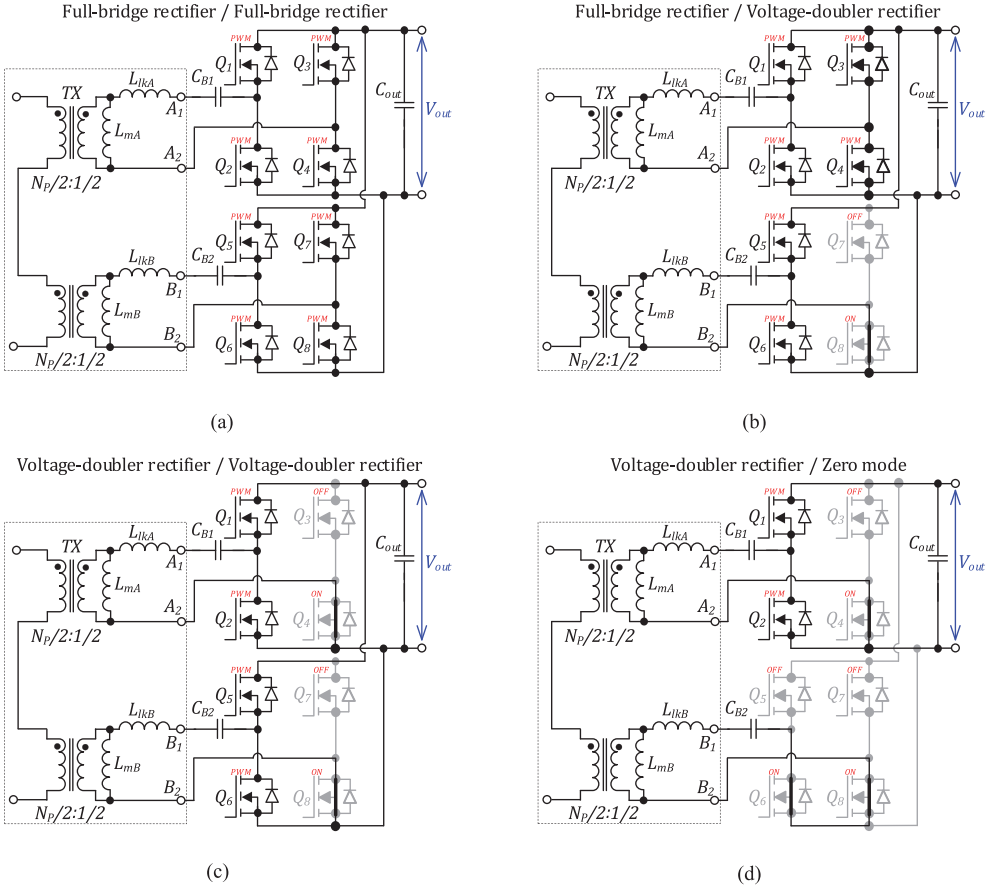

FIGURE 41. Reconfigurable LLC converter based on a transformer with fractional turns. (a) FBR / FBR, (b) FBR / VDR, (c) VDR / VDR, (d) and VDR / Zero mode.

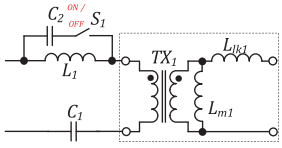

FIGURE 42. Reconfiguration from LLC to LLCC resonant tank.

A. FAULT-TOLERANT PV MICROCONVERTER

The TMC could be implemented for fault tolerance in a galvanically isolated high step-up photovoltaic (PV) microconverter. The study in [47] proposed a galvanically isolated dc-dc converter consisting of the quasi-Z-source network at the input, the FBI, an isolation transformer, and the reconfigurable rectifier with one active switch (see Fig. 44). To extend the input voltage range, the proposed microconverter can operate in the boost and buck modes. The PV microconverter can tolerate transistor faults in the FBI as the most stressed part of the microconverter. When a short-circuit failure (SCF) happens in one of the inverter switches, the inverter is reconfigured from the FBI to the SSI or the HBI in the boost mode or the buck mode, respectively, as shown in Fig. 45. At the same time, the rectifier is reconfigured from the FBR to the VDR in both modes. After the reconfiguration, the inverter changes the voltage gain from $G_{FE} = 1$ to $G_{FE} = 0.5$, and the rectifier changes the voltage gain from $G_{BE} = 1$ to $G_{BE} = 2$. Thus, the total dc voltage gain remains the same after the SCF and the microconverter can continue normal operation in the same voltage range.

B. SHADE-TOLERANT PV MICROCONVERTER

In the second example from paper [82], the TMC was utilized for extending an input voltage range of a PV microconverter to minimize power losses under the partial shading condition of a PV module. The proposed PV microconverter consists of the front-end quasi-Z-source SSI, an isolation transformer, and a reconfigurable rectifier, as shown in Fig. 46. Below a certain input voltage, the rectifier operates as the VQR. It is reconfigured into the VDR when the input voltage is above that

TABLE 3 Comparison of Advanced TMC Techniques

TMC	Nominal voltage gain G	Number of components[1]				Cost[3]	Advantage	Disadvantage	Typical input dc voltage, V	Typical output dc voltage, V	Typical power, W
		S	D	C	TX						
SAR (Fig. 29)	$2{\cdot}n$; $4{\cdot}n$	2	2	3	1	$	Voltage gain range extension up to two times	Switching losses in transistors	400	100–500	1500 [55]
A-TL FBI/ A-TL BBR (Fig. 31)	$0.5{\cdot}n$; $0.25{\cdot}n$ / $2{\cdot}n$; $4{\cdot}n$	4	0	3	1	$			400	50–450	300 [56], [57]
									160–280	18	100 [58]
									85–340	20	50 [59]
Adjusting turns ratio (Fig. 34)	n_1; n_2; $n_1{+}n_2$	8	6	1	1[2]	$$$	Voltage gain range extension depending on turns ratios	High number of semiconductor devices, using of bidirectional switches, using two transformers	390	250–450	1350 [60]
									390	60–450	900 [61]
Bypass. Series Transformer (Fig. 33)	n_1; $\frac{n_1 \cdot n_2}{n_1 + n_2}$	6	8	1	2	$$			25–100	210	250 [62]
Double LLC Conv. (Fig. 36)	n_1; n_2; $n_1{+}n_2$	6	6	4	2	$$		High number of semiconductor devices, using two transformers	50–300	50	250 [63]
									700	18–126	5000 [65]
									400	250–400	3200 [66]
									80–200	400	1000 [67]
									120–240	96	1000 [68]
5H-Inverter (Fig. 37)	$0.5n_1$; $0.5n_2$; $0.5n_1{+}0.5n_2$; $n_1{+}0.5n_2$; $0.5n_1{+}n_2$; $n_1{+}n_2$;	5	4	5	2	$$		Using two transformers	390	100–420	1100 [69]
									390	80–450	1000 [70]
									320–420	55–420	1000 [71]
LLC with Auxiliary Coupled Inductor (Fig. 39)	n_1; $n_1{+}n_2$	3	4	5	2	$$			5–65	400	400 [72]
									22–40	400	240 [73]
Fractional Turns Ratio (Fig 41)	$n_P{:}0.5$, $n_P{:}2/3$, $n_P{:}1$, $n_P{:}2$,	12	0	4	1[2]	$$$	Voltage gain range extension up to four times	Complex design of a transformer, high number of transistors	120–380	5, 9, 12	36 [74]
									380	12	1000 [75]
									250–500	10.5–15	1000 [77]
Reconfig. Resonant Tank (Fig. 42)	n; $2.5{\cdot}n$	6	4	4	1	$	Voltage gain range extension up to 2.5 times	Using of a bidirectional switch	150–400	400	1000 [78]
									140–400	400	1000 [79]
Multi-Track Architecture (Fig. 43)	$0.5\ n$; n	8	4	6; L=1	1[2]	$$$	Voltage gain range extension up to two times	High number of components	18–80	5	75 [80]
									80–370	12	150 [81]

Note: [1]S=switch; D=diode; C=capacitor; L=inductor, TX=transformer;
[2]A transformer with two primary or secondary windings.
[3]Estimated cost: $ is a low cost; $$ is a medium cost; $$$ is a high cost.

threshold value. The rectifier operation modes are selected by switching a mode-changing switch Q_1, which operates in the ON/OFF mode. Thus, high performance was achieved in the input voltage range from 8 up to 50 V, despite the simplified front-end inverter utilizing fewer switches. This range enables the maximum power point tracking under different partial shading conditions of the widespread 60-cell Si-based PV modules.

C. PV MICROCONVERTER WITH FLAT EFFICIENCY CURVE

TMC is also applied in PV microconverters for efficiency flattening across a power range [32]. The given PV microconverter consists of the FBI and the active FBR, as shown in Fig. 47; the aim is to achieve bidirectional power flow for possible battery integration. The idea presented in the article is based on the reconfiguration of the FBI to the flyback converter and the FBR to the SSR at a light load (see Fig. 48). According to the study, applying this reconfiguration at loads below 40% allows for improving the efficiency by up to 8%. The main drawback of the proposed approach is the requirement for using one bidirectional switch in the rectifier for blocking one leg in the SSR mode. It increases the cost of the rectifier and conducting losses in the FBR mode compared to the conventional FBR. Moreover, this approach is useful in low-power applications as the transformer air gap shall be large enough to handle power transfer in the flyback mode, which increases the conduction losses from the magnetizing current in the FBI mode.

D. UNIVERSAL HIGH STEP-UP INTERFACE CONVERTER FOR DC MICROGRIDS

Another example of TMC application that allows for a wide input voltage range and flattened efficiency curve is presented

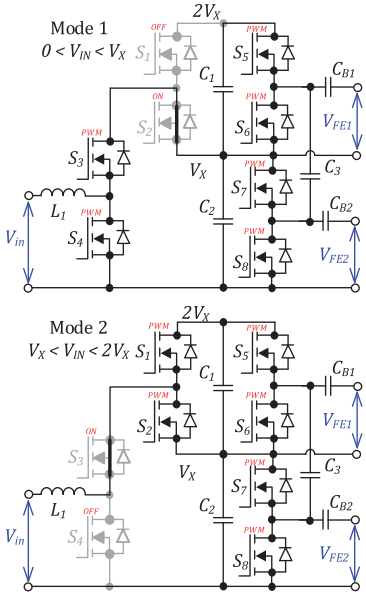

FIGURE 43. Operation modes of the two-track converter.

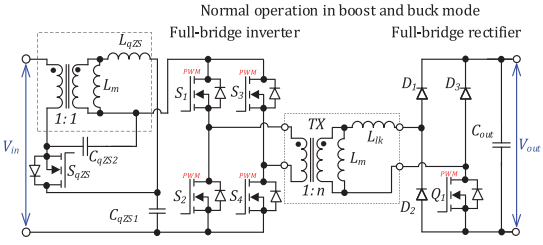

FIGURE 44. Quasi-Z-source galvanically isolated PV microconverter.

in [83]. In that study, the bidirectional isolated hexa-mode dc-dc converter (IHMC) based on the SRC topology is presented. The converter has a symmetrical structure that utilizes hybrid FBI cells both at the input and output sides. Each hybrid switching cell can operate as the FBI or the HBI. Thus, the IHMC operates under three topology configurations in each power flow direction: the FBI-FBR, the HBI-FBR, and the FBI-VDR (see Fig. 49).

In each mode, the converter operates as a buck-boost converter with the synchronous rectification. A special modulation is applied at the input side to step down the input voltage by reducing the active state duration at the isolation transformer, thus lowering the power throughput of the resonant tank. Similarly, using a special modulation at the output side allows for the input voltage boosting by short-circuiting the secondary winding with the resonant inductor, using the latter as an ac boost inductor. The TMC in this example provides for achieving a wide input voltage range from 10 to 60 V with an efficiency higher than 92% and the peak efficiency of 98%.

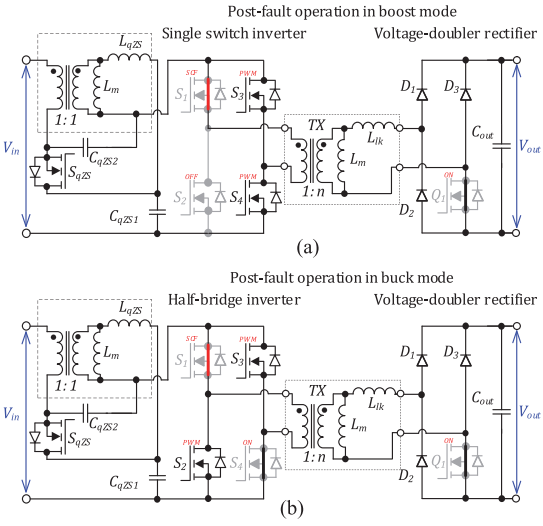

FIGURE 45. Post-fault operation of the quasi-Z-source galvanically isolated PV microconverter in the (a) boost and (b) buck modes.

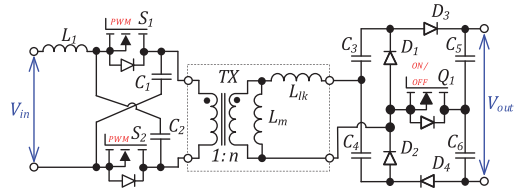

FIGURE 46. PV microconverter with a reconfigurable rectifier.

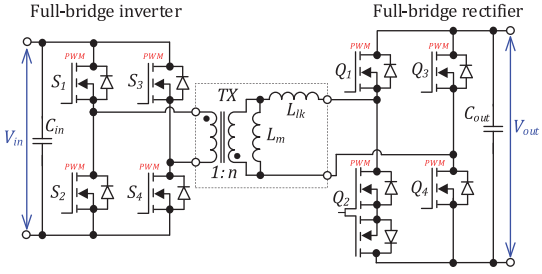

FIGURE 47. Dual-active bridge converter with flattened efficiency curve.

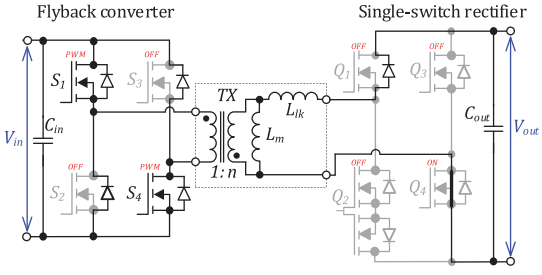

FIGURE 48. PV microconverter reconfiguration to the flyback converter at a light load.

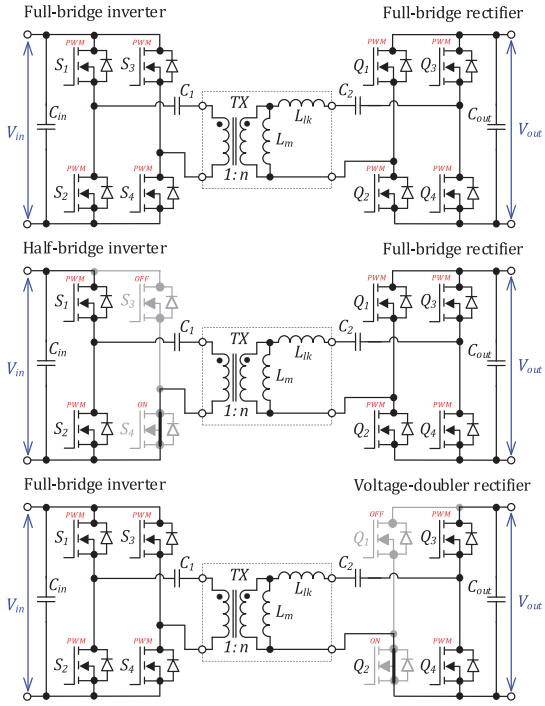

FIGURE 49. Operation modes of the galvanically isolated bidirectional hexa-mode dc-dc converter.

E. MICROCONVERTER WITH DUAL-STANDARD OUTPUT VOLTAGE FOR PV APPLICATIONS

TMC was also used in a PV microconverter for operation with two different voltage levels of a dc link, such as 200 and 400 V. This makes the microconverter compatible with inverters operating at different ac voltage levels: 110/120 V and 220/230/240 V, extending their applicability in different geographic locations. As a solution, a universal PV microconverter is proposed in [21], in which the FBI can be reconfigured in the HBI, and the FBR can operate as the VDR (see Fig. 50).

The converter has three topology configurations: HBI-FBR, FBI-FBR, and FBI-VDR. The maximum normalized voltage gain of the converter in these modes equals $G = 0.5$, 1, and 2, respectively. Reconfiguration of the rectifier is applied for operation at different output voltage levels. At the same time, the inverter can operate in the FBI or the HBI mode. In the study, a hybrid mode for controlling the inverter was applied. During the active states, the inverter operates as the FBI. During the zero states, the inverter is reconfigured to the HBI to levelize the peak transformer magnetizing current and avoid incomplete zero-voltage switchings. Thus, the proposed converter operates with efficiency of up to 96% at the input voltage range from 30 to 60 V, and two output voltage levels of 200 and 400 V.

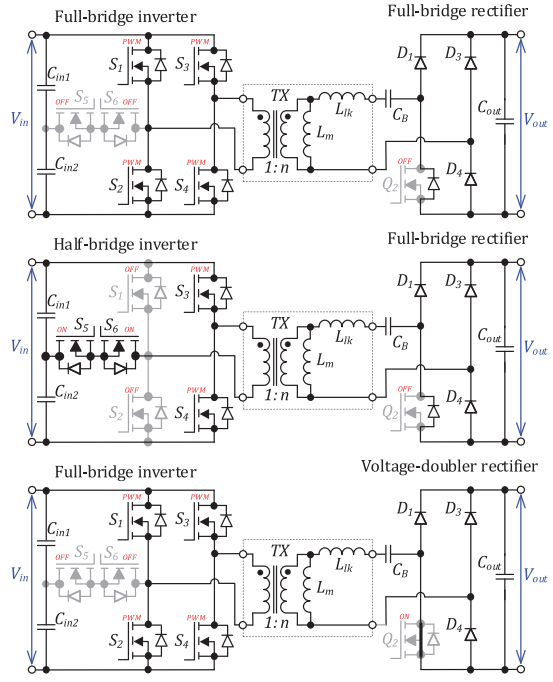

FIGURE 50. Operation modes of a universal PV microconverter.

F. TELECOM BACKUP POWER SUPPLY WITH DUAL-STANDARD OUTPUT VOLTAGE

One more example of TMC application in this section exhibits an LLC converter for supplying telecom systems from a battery with a wide voltage range [19]. The proposed converter is designed for a 100–400 V input voltage, a 48/24 V output voltage, and a maximum power of 800 W. The wide input voltage range was achieved by applying the TMC in the front-end inverter, as shown in Fig. 51. In the input voltage range of 100–240 V, the front-end inverter operates in the FBI mode. In the input voltage range of 240–400 V, it switches to operation in the HBI mode. Thus, the TMC allows for achieving efficiency above 90% in the wide input voltage range. The study describes also a method for soft transition between modes and stabilization of the output voltage. However, the mode reconfiguration transitions limit the converter feasibility in applications with tight voltage regulation.

G. ELECTRIC VEHICLE CHARGER WITH A WIDE OUTPUT VOLTAGE RANGE

A good example of advanced TMC techniques is the electric vehicle charger presented in [69]. It utilizes a five-switch reconfigurable bridge with two transformers shown in Fig. 37. The authors demonstrate how this topology can interchange its normalized dc voltage gain between 1, 2, 3, and 4. It was verified using a 1.1 kW protype fed with 390 V input voltage. Using TMC, it achieves a fourfold output voltage range from 100 to 420 V. This converter not only outperforms

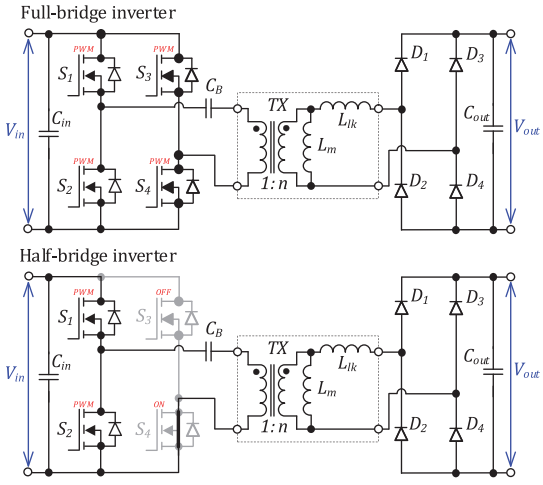

FIGURE 51. Reconfigurable LLC converter with wide input voltage range for the telecom system.

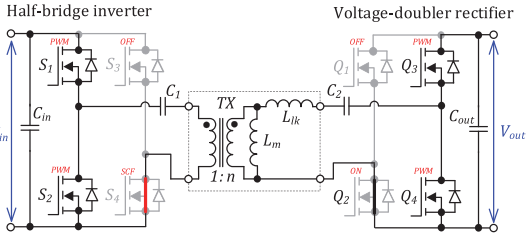

FIGURE 52. Post-fault operation of the dual active bridge converter.

the reference LLC converter-based chargers, but also features a narrow frequency regulation range. Owing to the use of TMC, it maintains its efficiency over 96% across the output voltage range and achieves the peak efficiency of 97.6%. Its obvious disadvantages are uneven thermal loading of the switches throughout the output voltage regulation range and overall complexity, which, however, could be acceptable for the applications where different standards require a very wide output voltage range from the chargers.

H. FAULT-TOLERANT CONVERTER FOR MORE ELECTRIC AIRCRAFTS

In more electric aircrafts, dc distribution is based on the use of two dc buses: 28 and 270 V. A converter interlinking them is required, where the dual active bridge is a common choice. In such a mission-critical system, a switch fault can occur, but it must not result in converter failure. For example, at an SCF in the switch S_4, the dual active bridge converter can continue operation as a dual half-bridge converter, as shown in Fig. 52. It is essential to mention that this converter could provide fault tolerance with zero redundancy, i.e., no redundant components. There are following two possible implementations of the converter:

1) conventional with a large inductor L_{lk} and phase shift modulation;
2) series-resonant implementation with a small L_{lk} that is likely to be embedded into the transformer *TX*.

It could be shown that zero-redundancy post-fault operation of the conventional implementation is not feasible due to the low power throughput of the post-fault dual half-bridge converter, which is four times lower than that before a fault.

On the other hand, the resonant implementation can handle post-fault operation at the same switching frequency. It can match the low-voltage port range from 18 to 50 V and the high-voltage port range from 200 to 330 V [84]. Pre-fault efficiency of a 300 W prototype ranges from 91% to 97.8%. The post-fault efficiency values ranging from 86% to 96% result from much increased current stress of the remaining healthy components.

VII. DISCUSSION

A. GENERALIZATION

Most of the TMC techniques could be summarized in the following basic principles: reducing voltage or current stress of semiconductors in a wide voltage range operation by reconfiguring the topology; reducing the number of switching components to improve light-load efficiency; recovering converter gain after a semiconductor fault; increasing converter dc gain at the output side to enable input side operation in a wider voltage range, while keeping the input-side duty cycle in an optimal range. It is worth mentioning that TMC has not shown power density improvement of the baseline converters. In some cases, power density could even be reduced due to specific thermal design requirements or the complicated design of magnetic components. On the other hand, the TMC enables single-stage high-performance dc-dc converters that could be smaller than the typical two-stage converter with the same functionality.

Several generalizations could be drawn from the literature surveyed in this article. Galvanically isolated dc-dc converters with low dc gain changing in a relatively wide range are typically designed for applications from several kW and higher, like on-board EV charging. Their implementation with LLC or series resonant switching with TMC on the input side could be recommended in the case of the wide input voltage range, or TMC on the output side in the case of the wide output voltage range to keep the stress of semiconductor components constrained. Most of these applications would not require more than two-mode TMC techniques. TMC techniques based on three-level topologies would be helpful when the voltage range spans to voltages above the voltage blocking capability of generic semiconductor switches.

Applications with high dc gain typically deal with low power, often below a kilowatt. As a result, the front-end inverter is often rated for high current stress, leading to considerable input voltage and power efficiency variations. These efficiency variations could result in significant efficiency steps, i.e., thermal cycling, when a converter changes

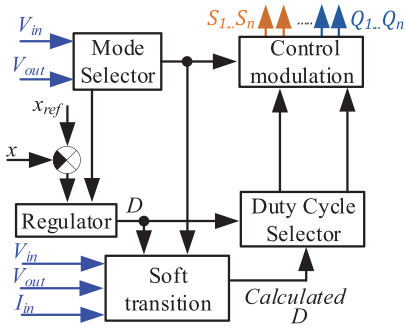

FIGURE 53. Example of TMC control integrated into a close-loop control system.

its operation mode based on TMC. However, the best-in-class dc gain range with no efficiency steps at the mode changes was observed in the converter combining boost half-bridge with reconfigurable rectifier [50]. Research efforts are required to determine whether this issue could be resolved for the full-bridge circuits.

Only a handful of techniques target efficiency improvement at light loads. These techniques have been used for low-power applications where reducing the number of active semiconductor devices at a light load could be very effective. At the same time, asymmetrical requirements for heat dissipation of devices are easy to manage in these applications. Nevertheless, some TMC techniques, such as reconfiguring FBI into HBI for better efficiency at a light load, could be useful in medium and high-power applications [85].

In addition, many advanced techniques resulting in high complexity of the converter design have been demonstrated for applications with high dc gain changing in a wide range. Their use can be recommended in niche applications, where strict performance requirements could justify associated extra costs.

B. CHALLENGES

Application of TMC techniques is challenging. First, the integration of TMC into a control system of a converter requires an additional control loop for reconfiguring a topology depending on the input and output voltage or power. In addition, the parameters of a regulator in the control system should be changed with topology reconfiguration due to changes in the small-signal converter model for each topology configuration. An example of a control system is shown in Fig. 53. The mode selector block changes topology configuration when voltage gain changes and crosses a threshold. With changing topology configuration, the mode selector also changes the parameters of the regulator.

The second challenge in control is the implementation of transitions between topology configurations with stabilized input and output voltage and current. Hard transitions between configurations cause high current stress in components that can damage a converter. Few studies have presented soft-transition algorithms [19], [86]. During the soft transition, the control system disables a regulator and sets a precalculated value for control variable D. Subsequently, the control system switches back to normal operation.

An efficiency step change that happens after a transition between topology configurations can be highlighted as the third challenge. The efficiency step change results in a considerable difference in power losses after the transition. Therefore, when the converter crosses the transition point, the temperature of the converter components changes. It would result in accelerated degradation of the converter components. To minimize the thermal stress of the components, the converter should be designed to map the mode transition points away from the most probable operation voltages or currents, if possible. Moreover, the thermal design of the converter should be based on the worst-case analysis of losses in each component for different modes.

C. PROMISING APPLICATIONS

As our review of the literature shows, the TMC is becoming more popular in applications with a wide input or output voltage range, such as chargers or battery interfaces. This trend suggests that TMC will gain even more attention in connection with the development of new portable electronic devices, electric scooters and bicycles [87]. In addition, the accelerating adoption of battery energy storage systems could benefit from the use of more flexible power electronic interface converters [88], [89].

The second expected trend is power electronics for supplying new USB Power Delivery (PD) specification (revision 3.1) that allows for delivery of up to 240 W over the USB type-C interface. USB fast chargers are expected to become a ubiquitous solution for portable electronics. The TMC could be a solution for the realization of efficient chargers capable of providing all output voltages requested by the USB PD specification (5, 9, 12, 20, 28, 36, and 48 V) [90].

The other promising application field for the TMC is fast chargers and on-board chargers for electrical vehicles (EV) and hybrid plug-in vehicles due to a wide voltage range of on-board batteries. The battery voltage standard has increased from 400 to 800 V [91]. Predictably, higher battery voltages allow for decreasing conduction losses in EVs. The TMC enables new chargers with a wide output voltage range.

Besides EVs, more electrical aircrafts could become a priority application area for the TMC [92], [93]. TMC increases the efficiency of converters operating in a wide range of on-board dc bus voltages and enables low-cost implementation of fault tolerance [84].

DC-microgrids for residential and small commercial buildings are becoming more popular due to their high efficiency compared to the ac grid [94], [95]. A variety of residential solar photovoltaic modules and battery types for energy storage requires numerous application-specific interface converters. The TMC can also enable a new class of universal interface converters to integrate renewable energy sources into the dc

microgrids with a minimum number of stock keeping unit types [50].

Residential PV systems suffering from partial shading of PV modules need interface converters capable of global maximum power point tracking [96]. This feature requires those converters to ensure a wide input voltage range that could be achieved at a low cost using TMC [82].

Fuel cells have been under the spotlight due to recent governmental support to cleantech. Their application requires the development of dc-dc converters capable of wide input voltage range regulation and delivering the maximum power at the maximum dc gain [97], [98]. TMC could help to optimize current stress in components for this challenging application, but more studies focusing on application of TMC are needed to show all possible benefits [34].

D. PROTECTED INTELLECTUAL PROPERTY

It is important to mention that a number of TMC techniques identified are protected by patents by companies and inventors from academia.

Several designs were patented by ShanghaiTech University: TMC with two secondary windings (see Fig. 34) [99], 5H-inverter (see Fig. 38) [100], and reconfigurable rectifier from Fig. 25 [101].

Delta Electronics holds several patents for TMC techniques applied on the converter input side: TMC based on TL HBI (see Fig. 31) [102], [103], and FBI/HBI reconfiguration in the front-end inverter (see Fig. 5) [29].

Murata Manufacturing Co. holds a patent describing the flying capacitor TL FBI capable of operating in the FBI mode with full voltage swing on the transformer and HBI mode with twice reduced voltage swing applied to the transformer [104]. This TMC technique could be considered a reduced subset of the technique shown in Fig. 13.

Huawei Digital Power Technologies also holds a patent that covers reconfiguration of both stages of a galvanically isolated dc-dc converter, where they demonstrate embodiments similar to TMC implementing FBR/VDR (see Fig. 15) and three-level half-bridge rectifier (see Fig. 31) [105], [106].

Shanghai Fengtian Electronics Co. holds a pending patent application describing two techniques for LLC resonant converter: FBI/HBI reconfiguration of the front-end inverter and hybrid modulation when one of the legs operating at three times reduced frequency [107].

The list of the TMC techniques protected by patents will get more comprehensive with time. Hence, it could be recommended to look out for possible patent infringements or limit the use of TMC techniques in commercial products to those published in the public domain.

VIII. CONCLUSION

This article has reviewed the present state-of-the-art in the topology morphing control for galvanically isolated dc-dc converters, covering the most recent contributions, implementation techniques, and application examples. It can be concluded that the topology morphing control is increasingly applied for extending the dc voltage gain range or flattening the efficiency of galvanically isolated dc-dc converters. The main principle of the TMC is in the reconfiguration of a converter topology depending on voltage or power conditions for operating with higher efficiency. The article provides a "one-stop" information source with comprehensive categorization of topology morphing control techniques for galvanically isolated dc-dc converters. Furthermore, the term "topology morphing control" has been established and justified for use in future publications.

This review divides the TMC into categories based on the converter side where the TMC is applied, such as the input and the output sides, an isolation transformer, or a resonant tank. In addition, advanced TMC techniques are described in a separate section. The described TMC application example shows that the prevalent dc-dc converter topologies utilizing the TMC are the resonant LLC or SRC. Both typically contain a series dc blocking capacitor allowing the use of the hybrid full-bridge switching cell that can easily be reconfigured from the full-bridge to the half-bridge. Most of the TMC techniques are based on static control of switches or the use of static switching patterns defining the operating mode. Hence, a simple control with smooth transitions between the modes is typically feasible. On the other hand, switching between TMC modes could result in a sizable efficiency step, which could have negative influence on the converter lifetime. This requires additional analysis with the focus on the minimization of mode transition instants, how to reduce efficiency steps at the mode transitions, and how these efficiency steps and their frequency influences the accumulated damage of components.

In conclusion, the application of the TMC gives a low-cost opportunity to improve converter performance, like increasing efficiency in a wide voltage gain range or a power range in galvanically isolated dc-dc converters. Publications on the subject have doubled in the past few years, revealing that there is still plenty of room for further development. Obviously, the proliferation of the dc nano- and microgrids, battery energy storage systems, and residential PV generation will create demand for high-performance low-cost converters and, consequently, will facilitate industrialization of the TMC.

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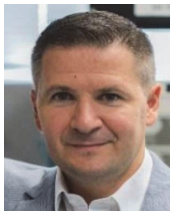

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An Overview and Comprehensive Comparative Evaluation of Constant-Frequency Voltage Buck Control Methods for Series Resonant DC–DC Converters

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ABSTRACT The paper focuses on galvanically isolated series-resonant dc-dc converters with a low quality factor of a magnetically integrated resonant tank. These converters can be controlled at a constant switching frequency to achieve the input voltage buck regulation. The paper compares various buck control methods, such as conventional pulse-width modulation, hybrid pulse-width modulation, shifted pulse-width modulation, hybrid shifted pulse-width modulation, improved shifted pulse-width modulation, asymmetrical pulse-width modulation, pulse-width modulation, and hybrid pulse-width modulation applied to the series-resonant dc-dc converter. The study considers step-up implementation of the series-resonant dc-dc converter topology with the voltage doubler rectifier, which makes it suitable as a front-end dc-dc converter for the integration of renewable energy sources in dc microgrids. The voltage buck control methods considered were compared analytically in terms of the cumulative power losses calculated theoretically. The theoretical results were compared with the experimental measurements to confirm the calculations and benchmark the voltage buck control methods. The experimental validation was performed using a 250 W prototype that demonstrated the hybrid PSM achieves the best performance. The experimental results were found in good agreement with analytically predicted values of the power loss.

INDEX TERMS Series resonant converters, dc-dc converters, pulse-width modulation, phase-shift modulation, dc microgrids.

I. INTRODUCTION

Sustainable development of humanity requires a wider use of electricity as a means of energy generation, transmission, and end-use [1]. Delay in widescale electrification would result in a technological barrier for economy that is net positive relative to the objectives of reduction of greenhouse emissions [2]. Wider adoption of renewable energy sources for electricity generation ensures low pollution and allows for adoption of highly decentralized or even autonomous power systems featuring high power supply security [3], [4]. The ongoing COVID-19 pandemic has proved the advantages of sustainable energy generation such as flexibility of energy generation, high reliability, little need for maintenance, and no dependence on the supply of fossil fuels [5]. Cutting lifecycle costs of renewables is essential to achieve grid parity in most of countries, which is also associated with the reliability and cost of the power electronic systems [6].

Dc distribution is a promising technology that can improve the overall efficiency of renewable energy generation and distribution [7]. Dc microgrids will be the backbone of the future autonomous households and smart districts [8]–[10]. Considering that the renewable energy sources usually provide variable dc output voltage, the importance of the dc-dc converters cannot be overestimated. Currently, solar photovoltaic (PV)

energy is considered the main technology that can achieve the lifecycle cost low enough to ensure the market viability of the dc microgrids in the near future [11]. The best performance of the PV energy generation could be achieved using the module-level power electronics [12]. This application requires dc-dc converters with a wide input voltage range of up to one to six. The galvanically isolated buck-boost dc-dc converters (IBBCs) show the best performance in these applications [12]. Among them, the series resonant converter (SRC) topologies have attracted much attention of the researchers [13]. These topologies aim for magnetic integration of the resonant inductor to achieve high power density, which, however, results in operation at low quality factors of the resonant tank. This implementation of the resonant tank makes the SRC nearly insensitive to the conventional variable frequency control [15]. On the other hand, they can be controlled at a fixed switching frequency.

An SRC-based IBBC with a low quality factor operates as a dc transformer (DCX) at a certain voltage V_{th} when all semiconductor components are soft-switched. The boost mode at the constant switching frequency can be used at the input voltages (V_{in}) below the V_{th}, which requires an active or semi-active rectifier to step-up the voltage at the rectifier side using the resonant inductor as an ac boost inductor [14]. The buck mode is used at $V_{in} > V_{th}$ and requires a certain modulation method to be applied to the input-side transistors [16]–[18]. The boost control methods were proposed recently by applying circuits used in the power factor correction [13]. On the other hand, the buck control methods were known from late 1980s [15] and gained more attention in the last decade [16]. A generalized methodology for the analysis of the dc voltage gain has been presented in [16]. However, some of the existing buck control methods have not been analyzed systematically before.

The goals of this study are to overview, generalize, classify, and benchmark the constant frequency buck control methods for the SRC with low quality factor, which cannot be controlled with variable frequency modulation due to low sensitivity of the converter dc voltage gain to the switching frequency variations [15]. Employing these methods in the primary side of the converter, and constant frequency boost control methods in the active or semi-active secondary side enables SRC-based IBBC with a wide input voltage range This study covers the conventional pulse-width modulation (PWM) [15], the hybrid PWM (HPWM) [16], the conventional phase-shift modulation (PSM) [17], [18], the hybrid PSM (HPSM) [19], [20], the shifted PWM (SPWM) [24], the hybrid shifted PWM (HSPWM) and the improved shifted PWM (ISPWM) [16], and the asymmetrical PWM (APWM) [21], [22]. The shifted PWM is excluded for brevity as it was proven in [16] that its hybrid and improved derivatives show better performance. The main contributions of this study are methodology for the calculation of power losses in the SRC and comprehensive benchmark of the constant-frequency buck control methods, which were verified experimentally for high step-up applications.

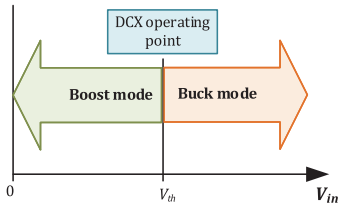

FIGURE 1. Arrangement of operating modes of an SRC-based IBBC.

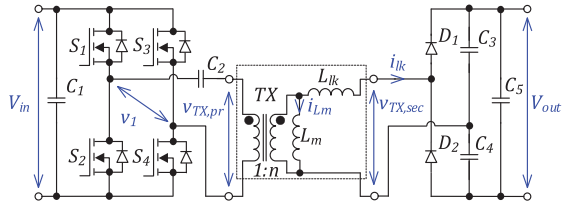

FIGURE 2. Topology of the series resonant converter under study.

This article is organized as follows. Section II of this article describes the SRC topology used in this study. Classification and generalized analysis methodology are

presented in Section III. Section IV provides a short description of the buck control methods. Next, Section V presents a systematic study of power losses for all considered buck control methods. In Section VI, the experimental waveforms are given to corroborate the idealized operating principle presented, and the measured power loss values are compared with those calculated theoretically. The results are discussed along with the future trends in Section VII. The last section draws conclusions.

II. DESCRIPTION OF SERIES RESONANT DC-DC CONVERTER

The topology of the high step-up SRC-based IBBC is shown in Fig. 2. It consists of the input-side full-bridge cell based on MOSFETs, an output side voltage doubler rectifier, an isolation transformer, and dc blocking capacitor in series with the transformer primary winding [23].

The angular resonant frequency of the resonant tank is defined as

$$\omega_r = \sqrt{\frac{1}{L_{lk}C_r}} \tag{1}$$

while the characteristic impedance is calculated as

$$Z_r = \sqrt{\frac{L_{lk}}{C_r}} \tag{2}$$

where L_{lk} is the leakage inductance of the transformer and C_r is equivalent resonant capacitance. The leakage inductance is considered as the only inductive element in the resonant tank. In general, the equivalent resonant capacitance the equivalent

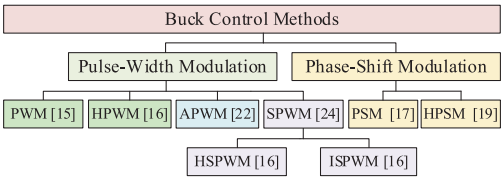

FIGURE 3. Classification of the buck control methods.

resonant capacitance considers influence of the blocking capacitor C_2 and output capacitors $C_3 - C_5$ as follows:

$$C_r = \frac{C_2\,(C_4C_5 + C_3(C_4 + C_5))}{C_4C_5n^2 + (C_3n^2 + C_2)(C_4 + C_5)} \tag{3}$$

The blocking capacitor neutralizes any dc bias current in the isolation transformer windings, which allows for the use of the asymmetrical control methods. Also, the capacitor allows for reconfiguration of the full-bridge switching cell into half-bridge. Typically, the capacitors C_2 and C_5 are dimensioned large enough to minimize their influence on the resonance. In such a case, the resonance frequency is defined mostly by the capacitors C_3 and C_4, and the expression (3) for equivalent resonant capacitance could be simplified as $C_r = (C_3 + C_4)$.

In the considered case, the topology operates under the discontinuous resonant current mode. Hence, the switching frequency should be 5–10% below the resonant frequency to implement sufficient dead-time needed for soft-switching employing the transformer magnetizing current [24].

III. GENERALIZATION OF THE BUCK CONTROL METHODS

A. CLASSIFICATION

All buck control methods of the SRC operation with discontinuous current and fixed frequency are classified in Fig. 3. There are two main types of the buck control methods: the PWM and the PSM. The main difference between them is in duty cycle of the switches. In the PWM, the duty cycle of two or more transistors is variable, thus the voltage is controlled. In the PSM, the duty cycle of all transistors equals 0.5; the output voltage is controlled by the shift angle between the leading leg switches S_1, S_4 and the lagging leg switches S_2, S_3. The PWM is subdivided into the classical PWM, the HPWM, the APWM, and the SPWM. The SPWM, in turn, is subdivided into the HSPWM and the ISPWM. In PWM methods, the duty cycle defines pulse width of switches. The PSM methods are subdivided into classical and hybrid PSM, where the duty cycle is a shift angle between the leading and lagging legs of the inverter. Section VI presents a detailed description of each method.

B. METHODOLOGY OF DC GAIN CALCULATION

An algorithm for deriving a closed-form expression of the dc voltage gain is demonstrated for the PWM methods of the SRC in [16]. This algorithm can be also applied for other buck control methods. The dc voltage gain of the converter normalized with respect to the transformer turns ratio n is defined similar to [24]:

$$G = \frac{V_{out}}{2 \cdot n \cdot V_{in}} \tag{4}$$

The analysis of the circuit is based on the assumption of lossless components. An expression for the converter dc voltage gain can be derived using the power balance:

$$P_{in} = P_{out} \tag{5}$$

First, it is assumed that the input power equals the average power fed by the input-side inverter to the isolation transformer (ignoring the influence of the magnetizing inductance):

$$P_{in} = \frac{1}{T_{SW}} \int_0^{T_{SW}} v_1(t) \cdot n \cdot i_{lk}(t)dt \tag{6}$$

where v_1 is a piecewise-linear function of the input-side inverter voltage, i_{lk} is a piecewise function of the resonant current, T_{SW} is the switching period.

Output power is defined by the output voltage and the load as follows:

$$P_{out} = \frac{V_{out}^2}{R} \tag{7}$$

where V_{out} is the average output voltage and R is the load resistance.

Considering how (6)–(7) can be substituted into (5), the power balance can be represented as:

$$\frac{1}{T_{SW}} \int_0^{T_{SW}} v_1(t) \cdot n \cdot i_{lk}(t)dt = \frac{V_{out}^2}{R} \tag{8}$$

Taking into account (4), an equation of the converter dc gain can be derived from (8) analytically or numerically as a function of the converter parameters, duty cycle D_{SD}, and the input voltage:

$$G = f\,(V_{in}, D_{SD}, n, R, L_{lk}, C_r, T_{SW}) \tag{9}$$

This methodology is universal for all buck control methods considered in this paper. The only difference is how the time-functions of v_1 and i_{lk} are defined. A derivative example of the dc gain closed-form expression for the PWM, HPWM, and SPWM methods is presented in [16]. Similarly, closed-form expressions of dc gain for the APWM, PSM, and HPSM buck control methods can be calculated.

IV. DESCRIPTION OF BUCK CONTROL METHODS

This section focuses on the operation principle of the described methods. The methods were grouped into four based on the operation principle. In each method, the duty cycle is equal to a duration of voltage pulses applied to the resonant tank. The duty cycle controls the transferred energy through the resonant tank. Thus, the output voltage is controlled.

A. PWM AND HPWM

First, the PWM [15] is analyzed, which is the simplest buck control method for the full-bridge as well as the half-bridge application. The transistors in each leg of the input-side inverter are controlled with the same duty cycle and 180 degrees phase shift between the gating signals. As can be

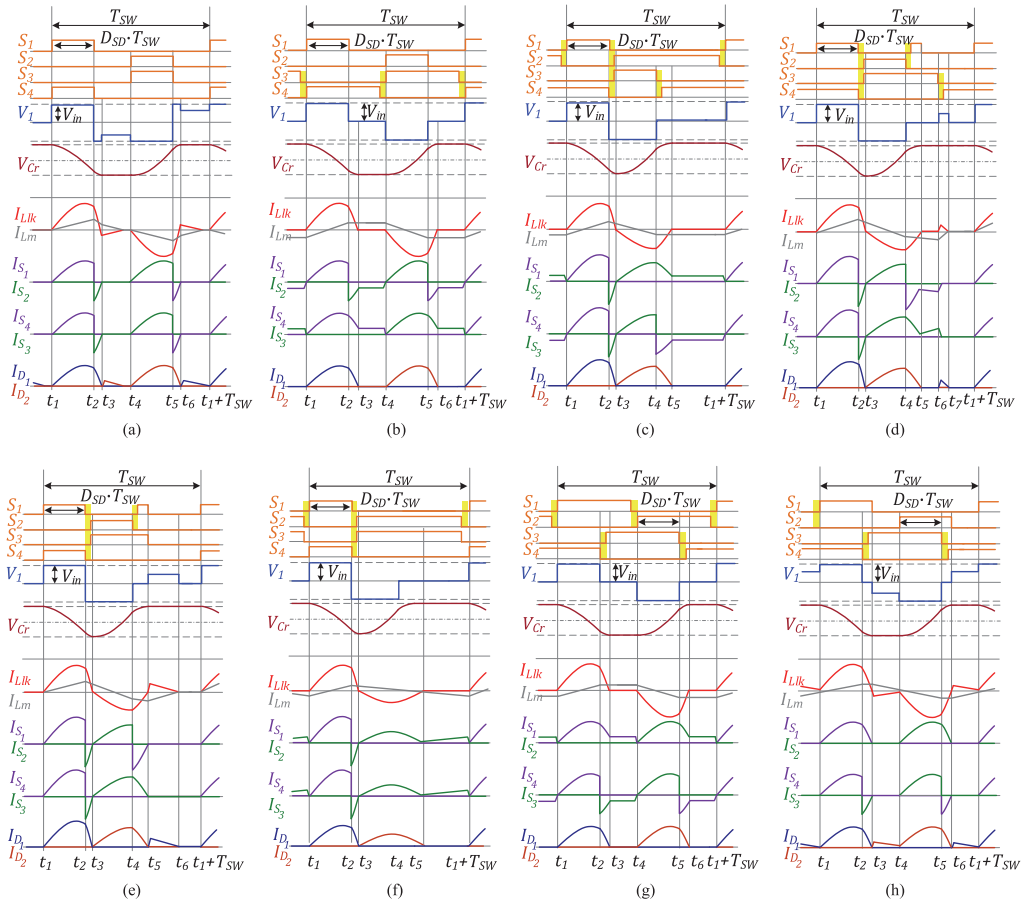

FIGURE 4. **Idealized steady-state waveforms of the SRC controlled by the PWM (a), HPWM (b), SPWM (c), HSPWM (d), ISPWM (e), APWM (f), PSM (g), and HPSM (h).**

seen from Fig. 4, the switches are turned on at zero current, but their turn-off is hard. When the transistors are turned off, the resonant current flows through the body diodes of MOSFETs. This is a significant drawback of this modulation method since transistors have high switching losses and the body diodes have high conduction losses and reverse recovery losses. At the instants t_3, the currents of switches $I_{S1}...I_{S4}$ are equal to zero; however, the resonant current is equal to the magnetizing current of the transformer, which flows through the secondary side of the transformer and rectifier diodes (Fig. 4(a)). Thus, in this control method, the magnetizing current adds conduction and reverse recovery losses to the rectifier diodes.

The normalized gain of the PWM method can be calculated using the methodology (4)–(9)

$$G = \frac{1}{2}\left(B(1-A) - 1 + \sqrt{(B(A-1)+1)^2 + 4AB}\right) \tag{10}$$

This equation was first presented in [16]. There are three parameters used to simplify the equation:

$$A = C_r R f_{SW} \tag{11}$$

$$B = 1 - \cos(\omega_r D_{SD} T_{SW}) \tag{12}$$

where D_{SD} is the duty cycle of the active states of the front-end inverter. In the case of asymmetrical control, D_{SD} is the smaller of two duty cycles.

The hybrid PWM method was proposed in [16] to reduce the transistor switching losses and conduction losses of the body diodes. The duty cycle of switches S_3, S_4 is always nearly 0.5, taking into account dead-time. This is the main difference from the PWM. These switches bypass their body diodes connected in parallel when the resonant current falls to zero. As can be seen from Fig. 4(b), only two transistors (S_1 and S_2) are turned off at a high current, other transistors are turned off at a low current, which is equal to the magnetizing current flowing through the transformer primary winding. It is because in this case, the magnetizing current flows through

the input-side bridge cell and influences the conduction and switching losses of the transistors. This method can be applied to control only the full-bridge cells, which is another difference from the PWM.

The normalized gain of the HPWM method is the same as the gain of the PSM method [17] and equals

$$G = \frac{1}{4}\left(B(1-A) + \sqrt{B^2(A-1)^2 + 8AB}\right) \tag{13}$$

B. SPWM, HSPWM AND ISPWM

The second group of the buck control methods is represented by various shifted PWM methods. As compared to the PWM, here, the control signals of the switches S_2 and S_3 are shifted in the vicinity of the control signal of the switches S_4 and S_1; they are separated by the dead-time. It is the main feature of each shifted method. As a result, the conduction losses in the MOSFETs body diodes are reduced because the switches S_2, S_3, and S_4 bypass their body diodes when the resonant current drops to zero at intervals $[t_2; t_3]$ and $[t_4; t_5]$ (Figs. 4(c)–4(e)). Switches S_2, S_3, and S_4 turn on at zero voltage, which would also reduce the switching losses, since their body diodes conduct during a short dead-time.

The voltage applied to the transformer and the output voltage are controlled by the duty cycle of S_1 and S_2 which are switched synchronously.

The SPWM demonstrated in [25] is similar to the modulation in [20]. Transistors operate complimentary with the dead-time. In the SPWM method, during the zero states of the inverter, when the resonant current is dropped to zero, two transistors S_2 and S_4 continue to conduct the magnetizing current. This feature increases conduction and switching losses in these MOSFETs since the magnetizing current is n times higher when it flows in the transformer primary winding compared to the secondary winding.

To avoid this drawback of the SPWM, the HSPWM was proposed in [16]. Ideal steady-state waveforms of the HSPWM are shown in Fig. 4(d). In the HSPWM, the zero state was eliminated by decreasing the duty cycle of the switch S_2. The switch S_1 turns on again after the switch S_2 is turned off, which reduces the conduction losses as the body diode of the switch S_1 is bypassed. The second turn-on of the switch S_1 occurs at zero voltage after the dead-time, following the instant t_4 because the body diode is conducting. The switch S_1 is turned off at the instant t_5 when the resonant current is equal to zero. Switches S_3 and S_4 operate complimentary with the duty cycle nearly 0.5. During conduction of the switch S_3, the magnetizing current flows through the input-side inverter, similar to the case of the SPWM. At the instant t_6, when the switch S_3 is turned off, the magnetizing current stops flowing in the input side and starts flowing in the secondary side of the transformer. This effect adds switching losses in the MOSFETs.

Another modified version of the SPWM method is the ISPWM (Fig. 4(e)), which was also described in [16]. The main difference from the HSPWM is in the duty cycles of switches S_3 and S_4. The duty cycle of the S_4 equals the duty cycle of the switch S_1. The switch S_3 conducts between the instants t_2 and t_5 when the resonant current is not zero. In this case, the magnetizing current flows only in the secondary side through the rectifier diodes.

The ISPWM and HSPWM can be used to control both the full-bridge and the half-bridge cells unlike the SPWM, which is used only to control the full-bridge cells.

The closed-form solution in a compact form was presented neither for the SPWM, HSPWM, and ISPWM methods nor for the PWM and the HPWM. Theoretical analysis of these shifted PWM method was performed using the numerical algorithm described in [16]. According to the power balance, the output voltage value can be found.

C. APWM

The APWM is another buck control method described and applied in [21], [22]. This method (Fig. 4(f)) can be applied to control both full-bridge and half-bridge cells. The positive part of the resonant current looks like in the previous modes; however, the negative part is always sinusoidal because the long conduction interval provides sufficient time for a complete sinusoidal half-wave. This improves the soft-switching performance of the converter. The voltages of the resonant tank and output voltage are controlled only by the duty cycle of switches S_3 and S_4. There is also the zero state similar to the SPWM where the magnetizing current flows through the input-side MOSFETs and influences their conduction losses.

Taking into account (4)–(9), the normalized dc voltage gain of the SRC for the APWM method equals

$$G = \frac{1}{4}\left(B(1-2A) - 1 + \sqrt{(B(2A-1)+1)^2 + 16AB}\right) \tag{14}$$

Previously, only an explicit expression of the dc gain was provided for the SRC controlled with the APWM [21], [22]. The expression (14) is presented here for the first time.

D. PSM AND HPSM

The last group of the buck control methods is represented by the phase-shift control methods, i.e., the PSM and the hybrid PSM. These two methods can be applied to control only full-bridge cells.

Figure 4(g) shows the idealized waveforms of the SRC operating with the PSM. In this case, the voltage applied to the resonant tank is controlled by the phase shift angle between the leading-leg switches S_1 and S_2, and the lagging-leg switches S_3 and S_4. In each leg, complementary gating signals are applied to the switches. The phase shift angle defines the duration of the zero states in the input-side inverter when either top switches S_1 and S_3 or lower switches S_2 and S_4 conduct the magnetizing current (Fig. 4(g)). In addition, the conduction losses of the body diodes are eliminated because the switches S_3 and S_4 bypass the diodes. In the zero state, the

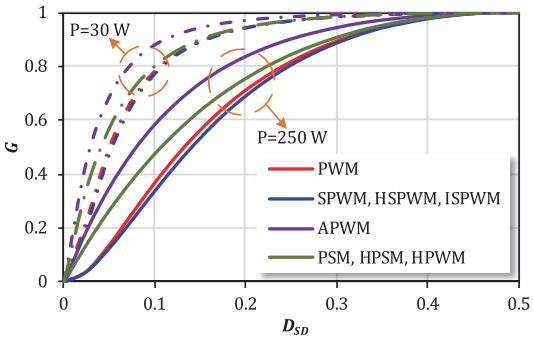

FIGURE 5. Theoretical normalized voltage gain of the case study SRC for PWM, HPWM, SPWM, HSPWM, ISPWM, PSM, and HPSM control methods.

resonant current drops to zero. In the PSM method, turn-off of two switches S_3 and S_4 is hard with the high resonant current and turn-off of the other two switches S_1 and S_2 is also hard but with low magnetizing current. The reason is that the magnetizing current flows through the primary windings of the transformer and the inverter. This increases conduction and switching losses in the transformer and MOSFETs.

The HPSM was proposed in [19] to improve the classical PSM control method. The zero states are avoided by decreasing the duty cycle of the switches S_1 and S_2 (Fig. 4(h)). As a result, when the resonant current equals zero, the magnetizing current stops flowing in the input side and starts flowing through the rectifier diodes.

The normalized dc voltage gain of the SRC for the PSM and the HPSM control methods corresponds to expression (13) first presented in [16].

E. COMPARISON OF GAINS

The normalized dc voltage gain of the case study converter calculated as a function of the duty cycle is plotted in Fig. 5 for two values of the operating powers, 30 W and 250 W, using (10)-(14) and the numerical analysis for the SPWM methods, as described in [16]. Table 1 presents the parameters used for the gain calculations. It could be appreciated from Fig. 5 that the described buck control methods have similar gain curves.

It is worth mentioning that each buck control method features a dead control zone, where the dc voltage gain G depends weakly on the duty cycle D_{SD}. When the load is changed, the Q-factor of the resonant tank is also changed. It has an impact on the voltage gain. Increase in the operating power results in the change of the dc voltage gain curve where the dead control zone is decreased.

As can be seen from Fig. 5, the gain curves of the PWM method are close to the curves of the SPWM, HSPM, and ISPWM. Accordingly, the gain (10) of the PWM can be used to calculate the theoretical normalized dc voltage gain for the SPWM method.

TABLE 1. Generalized Specifications of the Case-Study Converter

Operating parameters	
Input voltage, V_{in}	25…75 V
Output voltage, V_{out}	350 V
Switching frequency, f_{SW}	100 kHz
Operating power range	30…300 W
Components	
S_1 ... S_4	On Semiconductor FDMS86180
D_1,D_2	CREE C3D02060E
C_1, C_5	150 µF
C_2	52.8 µF
C_3, C_4	38 nF
L_{lk}	35 µH
L_m	1 mH
n	7.1

V. DERIVATION OF POWER LOSS MODELS

This section addresses a methodology for the calculation of power losses in the SRC. The methodology can help to understand the nature of power losses and compare buck control methods.

A. METHODOLOGY

Waveforms of the currents flowing through the resonant tank and switches as well as the shape of the resonant capacitor voltage are fairly similar for all the buck control methods (Fig. 4). The main difference lies in the time interval during which the resonant current decreases to zero. Nevertheless, the piecewise function of the resonant current can be defined as

$$i_{lk}(t) = \frac{v_1(t_i)\cdot n - v_{Cr}(t_{i-1}) - \Psi_{D_1}(t_i)\cdot V_{out}}{Z_r} \times \sin(\omega_r \cdot (t - t_i)), \tag{15}$$

where $v_1(t)$ is a piecewise function of the input-side inverter voltage, t_i is the i-th time instant, $\Psi_{D1}(t)$ is a switching function of diode D_1 that can be written as

$$\Psi_{D_1}(t) = \begin{cases} 1, & \text{if} D_1 \text{ is conducting;} \\ 0, & \text{if } D_1 \text{ is off.} \end{cases} \tag{16}$$

The piecewise function of the resonant capacitor voltage could be defined as

$$v_{Cr}(t) = \frac{1}{C_r}\frac{di_{lk}(t)}{dt}. \tag{17}$$

At the same time, a piecewise-linear function of the magnetizing current equals

$$i_m(t) = \frac{\left(v_1(t_i) - v_{C_2}(t)\right)\cdot n}{L_m} \cdot \frac{t - t_{i-1}}{t_i - t_{i-1}} + i_m(t_{i-1}) \tag{18}$$

where $v_{C_2}(t)$is an average voltage of the input-side resonant capacitor C_2. In the symmetrical control methods, the average voltage is equal to zero. The calculation of the magnetizing

current assumes that each piece of the magnetizing current function is linear.

The three main (15), (17), and (18) define the current and the voltage of all circuit components.

Depending on the buck control method, the magnetizing current could flow through the primary or the secondary winding of the transformer, as can be seen from Fig. 4. Therefore, the current of the transformer primary winding equals

$$i_{TX,pr}(t) = \begin{cases} (i_{lk}(t) + i_m(t)) \cdot n; \\ i_{lk}(t) \cdot n. \end{cases} \quad (19)$$

By the same principle, the secondary side current of the transformer can be written

$$i_{TX,sec}(t) = \begin{cases} i_{lk}(t); \\ i_{lk}(t) - i_m(t). \end{cases} \quad (20)$$

From (19), currents of the input-side switches $S_1 \ldots S_4$ are defined by the switching functions as follows:

$$i_{S_k}(t) = i_{TX,pr}(t) \cdot \Psi_{S_k}(t) \quad (21)$$

where k is the number of a switch, $\Psi_{S_k}(t)$is a switching function of a switch, which is defined similar to (16).

In the same way, the currents of the rectifier diodes are defined

$$i_{D_j}(t) = i_{TX,sec}(t) \cdot \Psi_{D_j}(t) \quad (22)$$

where j is the number of a rectifier diode.

The input current of the inverter is

$$i_{in}(t) = i_{TX,pr}(t) \cdot sign\,(v_1(t)) \quad (23)$$

The output current of the voltage doubler rectifier is

$$i_{out}(t) = i_{D_1}(t) \quad (24)$$

It is assumed that ac components of the primary and secondary winding currents flow through the input capacitor C_1 and the output capacitor C_4, respectively. An LCR bridge HAMEG HM8118 was used for the measurement of the winding equivalent resistances (ERs) of the magnetic components and resistances of a PCB.

The conduction losses of the MOSFETs, the transformer, the input and output capacitors are calculated using conventional methods, where each element is replaced with a corresponding resistor [26], [27]. For example, a drain-to-source resistance given in Table 2 represents a MOSFET in the on-state. ER of the transformer, the input and the output capacitors is imitating elements in AC with the switching frequency. Therefore, conduction power losses of these elements can be calculated as

$$P_{cond(element)} = I^2_{RSM(element)} \cdot R_{(element)} \quad (25)$$

Where $I_{RMS(element)}$ is the RMS current of an element, $R_{(element)}$ is an equivalent resistance of an element, which is shown in Tables II and III. It has to be taken into account that the input capacitor C_1 is a combination of SMD ceramic and film capacitors and the output capacitor C_5 is a combination of film and electrolytic capacitors. Also, the input and output resistance of a PCB was included in the power loss calculation. The equivalent input- and output-side resistances of a PCB are 5 mΩ and 3 mΩ, correspondingly.

TABLE 2. Datasheet Parameters of Semiconductor Components Used For Calculation of Losses

MOSFET On Semiconductor FDMS86180	
ON-state resistance	3.7 mΩ
Output capacitance	3250 pF
Gate-source voltage	9 V
Total gate resistance	3.5 Ω
Miller effects voltage	4.8 V
Rise time	12 ns
Fall time	7 ns
Gate-drain capacitance (V_{DS}=0 V)	530 pF
Gate-drain capacitance (V_{DS}=35 V)	68 pF
Body diode forward voltage	0.8 V
Body diode on resistance	28 mΩ
Body diode charge	109 nC
Diode Cree C3D02060E	
Forward voltage	0.8 V
On resistance	0.25 Ω
Total capacitance	10.5 pF
Total charge	120 nC

To calculate conduction losses in a body diode of a MOSFET or a rectifier diode, a diode is considered as a series connection of a voltage source and a resistance, imitating the forward voltage drop and the differential resistance of a diode [26]. Therefore, conduction power losses of a diode can be calculated as

$$P_{cond(diode)} = I^2_{rms(diode)} \cdot R_{(diode)} + I_{av(diode)} \cdot V_{f(diode)} \quad (26)$$

where $I_{av(diode)}$is the average current, $V_{f(diode)}$ is the forward voltage and $R_{(diode)}$is the on-resistance of a diode. These parameters are listed in Table 2.

The calculation of switching losses in MOSFETs and diodes is based on the methodology from [27]. It uses the most conventional approach based on the datasheet parameters, such as parasitic output capacitance, fall and rise times, gate resistance and capacitance, etc.

The methodology of power losses calculation in a transformer core with non-sinusoidal waveforms is described in detail in [28]. An equation for power losses in a transformer core can be calculated as

$$P_{core} = \frac{V_e k_i (\Delta B)^{\beta-\alpha}}{T_{SW}} \sum_m \left| \frac{B_{m+1} - B_m}{t_{m+1} - t_m} \right|^{\alpha} (t_{m+1} - t_m) \quad (27)$$

where V_e is an effective volume of the core, k_i, α, β are Steinmetz coefficients determined by fitting of curves from the datasheet of the core material, B_m is the magnetic flux at

TABLE 3. Parameters of the Transformer and Capacitors Used For Calculation of Losses

Transformer RM14 3C95	
ER of windings	990 mΩ*
Primary turns	8
Secondary turns	50
μ_i	3000
Effective volume	13900 mm^3
Effective length	70 mm
Effective area	198 mm^2
α	1.045
β	2.44
k_i*	8.21
ESR of input and output capacitors	
ESR of C_1 (f = 100 kHz)	9 mΩ
ESR of C_3 (f = 100 kHz)	250 mΩ

*at 70°C

the instant t_m, ΔB is the peak-to-peak magnetic flux during the switching period T_{SW}.

The parameters of the transformer used for the calculation of the power losses are listed in Table 3. It has to be taken into account that the isolation transformer *TX* was implemented using RM14 core made of 3C95 ferrite material with an air gap of 0.6 mm, eight turns in the primary winding, and equivalent series resistance of 850 mΩ (at 25 °C) referred to the secondary winding [29], [30].

B. COMPARISON OF LOSS MECHANISMS

To benchmark the described buck control methods, current stresses have to be analyzed. Seven main current stresses were considered:

- RMS current of the MOSFET channel $I_{rms(S)}$ (considering current flowing only when a switch is turned on) - as it influences the conduction losses of the switches;
- average current $I_{av(bdS)}$ and the RMS current $I_{rms(bdS)}$ of the body diode (considering negative current flowing when a MOSFET is turned off) – as it could increase the conduction losses in the switches significantly;
- turn-off current $I_{off(S)}$ - as it defines the switching losses of the MOSFETs;
- RMS current of the transformer in the secondary side $I_{rms(TX,sec)}$ - as it influences the conduction losses of the transformer windings;
- RMS current of the rectifier diodes $I_{rms(in)}$ - as it influences the conduction losses of the rectifier diodes and the output-side capacitor;
- input RMS current $I_{rms(in)}$ - as it influences the conduction losses of the input-side capacitor;
- maximum current of the magnetizing inductance $I_{max(Lm)}$ - as it influences the conduction losses of the input- or output-side components, which depends on the buck control method used.

TABLE 4. Current Stress of Elements At Vin = 35 V, P = 250 W for Different Buck Control Methods

Parameter	Value of current, A				
	PWM	HPWM	SPWM, HSPWM, ISPWM	APWM	PSM, HPSM
$I_{rms(S)}$	22.1	21.2	23.7	21.9	23
$I_{av(bdS)}$	3.5	4.1	0	0	0
$I_{rms(bdS)}$	8.9	8.9	0	0	0
$I_{off,max(S)}$	5.4	5.1	5.2	6.9	5.10
$I_{rms(TX,sec)}$	2.4	2.3	2.3	2.2	2.3
$I_{rms(D)}$	2.4	2.3	2.3	2.2	2.3
$I_{rms(Cin)}$	16.8	13.7	15.1	15.4	13.7

TABLE 5. Current Stress of Elements At Vin = 60 V, P = 250 W for Different Buck Control Methods

Parameter	Value of current, A				
	PWM	HPWM	SPWM, HSPWM, ISPWM	APWM	PSM, HPSM
$I_{rms(S)}$	24.9	22	28	24.5	26.4
$I_{av(bdS)}$	6.7	7.1	0	0	0
$I_{rms(bdS)}$	16	14.4	0	0	0
$I_{off,max(S)}$	8.8	6.9	8.5	9.5	6.9
$I_{rms(TX,sec)}$	2.9	2.6	2.7	2.4	2.6
$I_{rms(D)}$	2.9	2.6	2.7	2.4	2.6
$I_{rms(Cin)}$	20.9	11.8	16.4	17.3	11.8

The average current stress of the input and the output side is virtually the same for all the buck control methods and thus is excluded from the benchmarking. To compare symmetrical and asymmetrical control methods correctly, the cumulative RMS current of the MOSFETs was calculated as

$$I_{rms(S)} = \sqrt{\sum_{k=1}^{4} I_{rms(S_k)}^2} \tag{28}$$

The RMS currents of the body diodes and the rectifier diodes were calculated in the same way. The average current of the body diodes is a sum of the average currents of each body diode.

These calculated steady-state current stresses for the studied control methods at points V_{in} = 35 V and V_{in} = 60 V at P = 250 W are shown in Tables 4, 5, and 6. The SPWM, the HSPWM, and the ISPWM methods have the same current

TABLE 6. Maximum Magnetizing Current At P = 250 W and Different Input Voltage for Different Buck Control Methods

	$I_{max(Lm)}$, A	
Methods	V_{in}=35 V	V_{in}=60 V
PWM	0.43	0.47
HPWM	0.22	0.18
SPWM	0.41	0.44
HSPWM	0.44	0.46
ISPWM	0.41	0.44
APWM	0.29	0.24
PSM	0.22	0.18
HPSM	0.39	0.35

TABLE 7. Features of The Buck Control Methods

Method	Transistors switched at high current	Number of conducting body diodes	Winding conducting the magnet. current
PWM	4	4	Secondary
HPWM	2	2	Primary
SPWM	3	0	Primary
HSPWM	3	0	Primary and secondary
ISPWM	3	0	Secondary
APWM	2	0	Primary
PSM	2	0	Primary
HPSM	2	0	Secondary

stress of the main components except for the maximum magnetizing current. For this reason, these methods, as well as the PSM and the HPSM methods, were grouped in one column. As shown in Tables 4 and 5, the PWM method has the highest current stress of elements (red values). Furthermore, the number of transistors switched at high current and the number of conducting body diodes is shown in Table 7. As can be seen from Table 7, the PWM has large amounts of switching transistors and conducting body diodes. Also, the body diodes of MOSFETs are conducting in the HPWM method, which is the main drawback of this method.

The PSM and the HPSM feature the lowest current stress and the smallest count of switching transients than other methods. Drawbacks of the shifted methods are the high RMS value of the current flowing in MOSFET channels (i.e., not taking into account MOSFET current flowing through the body diodes), three transistors switched at high current, and high magnetizing current (Table 6). In this case, it means that core losses of the transformer are increased as well as additional conduction losses in the converter caused by the

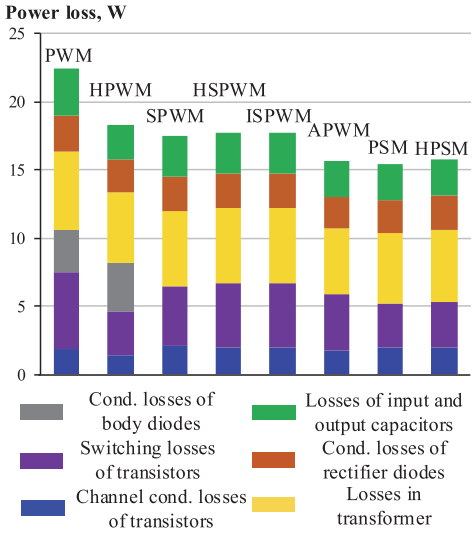

FIGURE 6. Diagram of power losses in the SRC at V_{in} = 35V, P = 250 W for different buck control methods.

magnetizing current. The APWM method features moderate current stress and two transistors switched at high current, but as compared to other methods, these transistors are turned off at the highest current. It can be seen from Tables 4 and 5 that current stress in the circuit are increasing with increase of input voltage. This is mostly associated with decrease of the duty cycle D_{SD}, as can be seen from Fig. 5. However, the same trend among current stresses is observed in Table 5 when compared to Table 4.

Table 7 also shows the side(s) where the magnetizing current flows during the switching period. In the case when the magnetizing current flows in the input side, it increases the conducting losses in the primary winding of the transformer and MOSFETs as well as the switching losses in MOSFETs. Therefore, in the other case, the magnetizing current adds conducting losses in the secondary winding of the transformer and the rectifier diodes. It should be noted that the magnetizing current flowing in the primary winding of the transformer is n times higher than in the secondary winding. Therefore, the magnetizing current flowing in the secondary winding is less harmful for the converter efficiency compared to when it flows in the primary winding.

Power losses calculated at $V_{in} = 35$ V and $P = 250$ W based on the described methodology are shown in Fig. 6. The bar chart includes conduction losses of transistors (blue), switching losses of transistors (magenta), conduction losses of body diodes (gray), conduction losses of the transformer windings (yellow), conduction losses of rectifier diodes (orange), and combined losses of input and output side components (green). These losses are dominant in the given converter. All buck control methods feature nearly equal but low conduction losses of transistors. This results from using high-performance

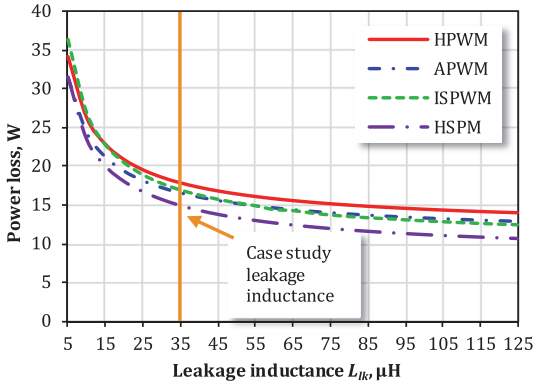

FIGURE 7. Dependence of losses on the leakage inductance.

MOSFETs with low on-state resistance. The main difference is in the duty cycle deviations and the magnetizing current path in the circuit, which also influences the transformer and rectifier diodes losses. Different magnetizing current values influence the transformer losses that consist of the copper losses and the core losses.

The PWM and HPWM feature conduction losses of the body diodes, which is a significant drawback. They would result in increased temperatures of transistors and should be taken into account in the converter thermal design.

The main drawback of the SPWM and PWM method is high switching losses. The reason revealed in Table 7 is that a large number of transistors are turned off at high current in comparison with other methods. The APWM and two PSM methods have a nearly equal total power loss. However, in the case of the APWM, transistor switching losses and losses of input and output capacitors are higher in comparison with PSM methods, while conduction losses of transistors and the transformer are higher in the PSM methods. This aspect would result in increased temperatures of these two MOSFETs and should be taken into account during the thermal design of the converter.

An amplitude of the resonant current influences directly all types of power losses. As can be seen from (15), the amplitude depends inversely on the impedance of the resonant tank (3), which is dependent directly on the leakage inductance. The dependence of total losses on the leakage inductance for four high-performance methods at $V_{in} = 35$ V, $P = 250$ W is summarized in Fig. 7. These four curves feature virtually the same shape. With the inductance increasing, total losses are decreasing. Above 50 µH, the total losses are weakly dependent on the inductance. In the case study converter the transformer with the internal leakage inductance 35 µH was used. This is the maximum value of the internal leakage inductance for this transformer type. The difference in the power losses between values 35 µH and 100 µH is about 4.5 W. However, the values of more than 50 µH can be achieved by an external inductor, which, however, increases the conduction losses, cost, size, and weight of the converter.

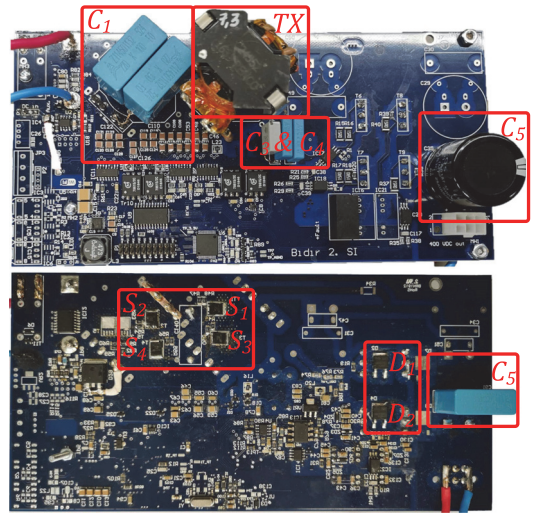

FIGURE 8. Experimental prototype of the series resonant converter.

VI. EXPERIMENTAL RESULTS

A prototype of the SRC converter was built to verify the operation of the buck control methods and compare experimental results with the theoretical methodology. The main specifications of the prototype are listed in Table I. The prototype is shown in Fig. 8.

A. STEADY-STATE WAVEFORMS

Voltage and current waveforms of the SRC operating in PWM, HPWM, APWM, SPWM, HSPWM, ISPWM, PSM, and HSPM control methods at $V_{in} = 35$ V, $P = 250$ W are shown in Fig. 9. The following measurement equipment was used: oscilloscope Tektronix DPO7254, differential voltage probes Tektronix P5205A, current probes Tektronix TCP0030A, and a precision power analyzer Yokogawa WT1800.

The measured waveforms of transformer current (Fig. 9) correspond to the theoretical curve of the resonant current in Fig. 4 for each buck control method. However, in the case of PWM, HSPWM, ISPWM, and HPSM, the voltage shape of the transformer primary winding has a parasitic oscillation between the output capacitances of semiconductor devices and the leakage inductance (Fig 9(a), 9(e), 9(f), and 9(h)). In the cases of HPWM, APWM, SPWM, HSPWM, and PSM, the secondary transformer voltage has a parasitic oscillation between the junction capacitances of the rectifier diodes and the leakage inductance (Fig. 9(b), 9(c), 9(d), and 9(g)). The HSPWM method features parasitic oscillations after the transistor S_3 is turned off and S_4 is turned on after a short dead-time (Fig. 9(e)). In the case of the ISPWM method, there are parasitic oscillations between the output capacitances of the semiconductor components and the magnetizing inductance of the transformer (Fig. 9(f)). All the described parasitic oscillations occur when the resonant current drops to zero.

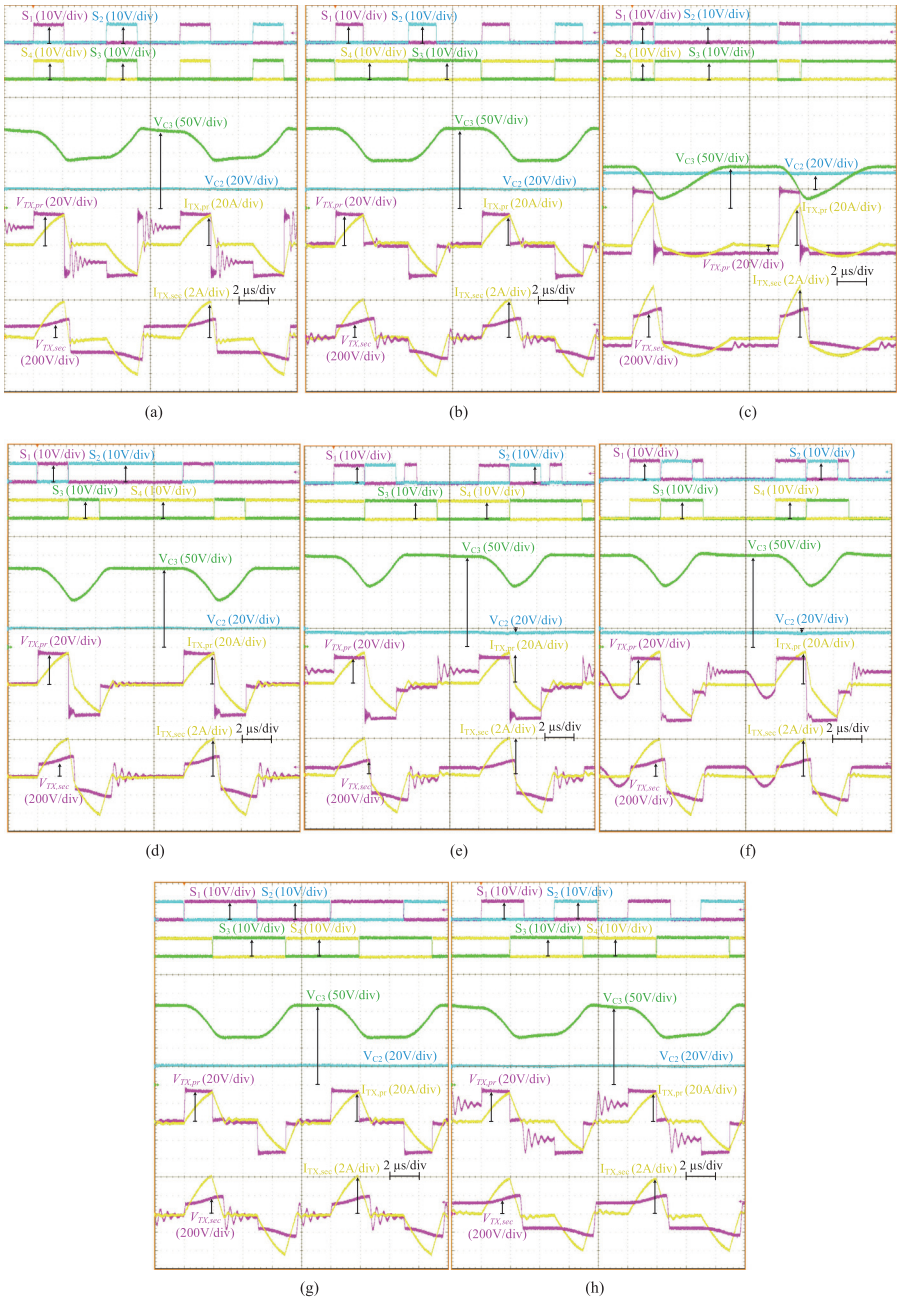

FIGURE 9. Experimental steady-state waveforms of the SRC operating at V_{in} = 35 V, P = 250 W for PWM (a), HPWM (b), APWM (c), SPWM (d), HSPWM (e), ISPWM (f), PSM (g), and HPSM (h) buck control methods.

These oscillations add extra conduction losses in the transformer and semiconductor devices.

As can be seen from Fig. 9, the voltage of capacitor C_3 is changing when the resonant current is equal to zero in PWM, HSPWM, ISWPM, and HPSM methods. It is the result of the magnetizing current flowing in the secondary winding of the transformer.

The magnitudes of the transformer current depend on the quality factor of the resonant tank, the turns ratio of the transformer, and the load power. Therefore, the magnitudes

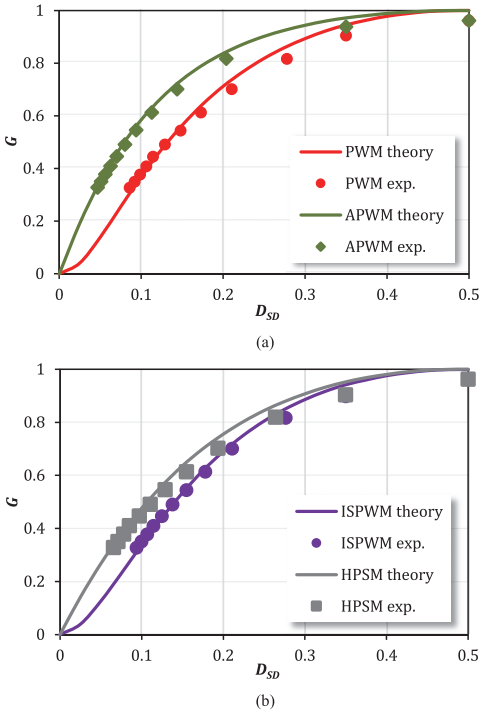

FIGURE 10. Normalized voltage gain of the case study SRC for PWM and APWM (a), ISPWM and HPSM (b) at $P = 250$ W.

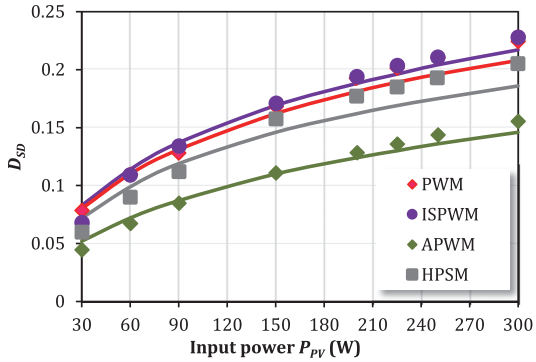

FIGURE 11. Duty cycle of the case study SRC for PWM and APWM (a), ISPWM and HPSM (b) at $V_{in} = 35$ V and different power.

of the transformer current are practically the same for some modulation methods. But thwe magnitude is the highest for the APWM method, as described in Section V.

B. COMPARISON OF EXPERIMENTAL AND THEORETICAL CONTROL VARIABLES

Experimental and theoretical values of the normalized dc voltage gain of the case study converter were plotted for the PWM, APWM, ISPWM, and the HPSM methods as a function of the duty cycle D_{SD} in Fig. 10. At the same time, Fig. 11 presents the duty cycle D_{SD} as a function of the input power for the same methods. Hereinafter, in figures, solid lines correspond to the theoretical values, while dots present experimental data. Theoretical curves in Figs. 10 and 11 were obtained using (10), (13), (14), and the numerical analysis for the ISPWM described in [16]. They are compared to the experimental results for the input voltage range from 25 V to 75 V (Fig. 10) and for the input power range from 30 to 300 W (Fig. 11). It can be seen from the figures that the voltage gain curves are almost identical for all the compared methods. The four methods considered in Figs. 10 and 11 show good agreement between the theoretical and experimental results. It is worth mentioning that that experimental values of the duty cycle D_{SD} for PWM and ISPWM are virtually identical, which proves assumption of equivalence of their dc gain curves made in [16]. Small differences between theoretical and experimental values occur outside the target regulation range and are mostly associated with the assumptions of a lossless system, neglecting the influence of the magnetizing inductance during the analysis. As can be seen from Fig. 5, other reviewed methods have theoretical gain curves that conised with those for the four selected methods. Therefore, other methods were omitted from Figs. 10 and 11 for better clarity and readability.

C. COMPARISON OF EXPERIMENTAL AND THEORETICAL POWER LOSSES

Figures 12 and 13 show the results of the calculation of theoretical power losses (solid lines) based on the described methodology in comparison with experimental losses (markers) for all buck control methods at $P = 250$ W and different input voltages (Fig. 12), at $V_{in} = 35$ V and a different power (Fig. 13), respectively. Increasing the input voltage increases the power losses since the duty cycle is decreased. With increased power, the resonant current and the duty cycle are increased. Therefore, the resonant current influences conduction losses in the elements and switching losses of the transistors.

As can be seen from Figs. 12 and 13, the methodology described in Section V shows good agreement with the experimental results. Thereby, this methodology can be used in the future research work. Deviations between the theoretical and experimental results are mostly associated with uncertainties and temperature drift of the datasheet parameters, and parasitic power losses in a PCB.

D. EFFICIENCY

Efficiencies of the prototype as a function of the input voltage and as a function of power for different control methods are shown in Fig. 14.

The maximum efficiency of the prototype equals 96.7% at $V_{in} = 25$ V, $P = 250$ W, $D_{DS} = 0.5$ for all control methods. This is a point of the maximum dc voltage gain. At this point, switches are turned on and off at zero current because the resonant current is virtually sinusoidal. With an increase of

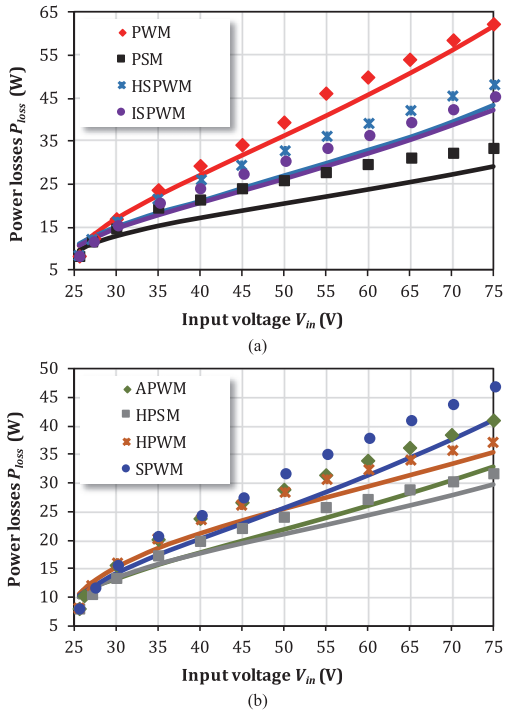

FIGURE 12. Power losses of the converter for PWM, PSM, HSPWM, ISWPM (a); APWM, HPSM, HPWM, SPWM (b) at $P = 250$ W.

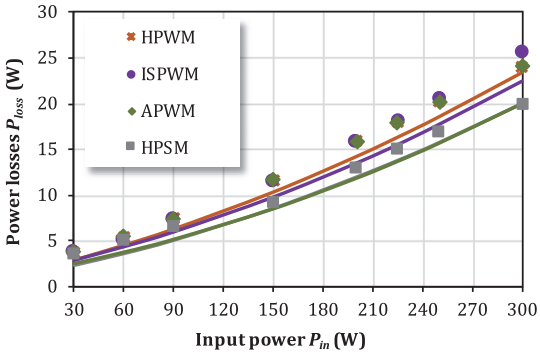

FIGURE 13. Power losses of the converter for HPWM, ISWPM, APWM, HPSM at $V_{in} = 35$ V.

the input voltage, the duty cycle decreases, thus increasing the power losses. The difference in the efficiency is mostly associated with the conduction losses in the body diodes of the MOSFETs, switching losses in the transistors, and power losses from the magnetizing current. In each control method, the efficiency is decreased at a low power range since the transformer core losses from the magnetizing current and parasitic oscillation prevail over other types of losses.

The HPSM has the highest efficiency at different voltages and different powers. The main difference of the efficiency

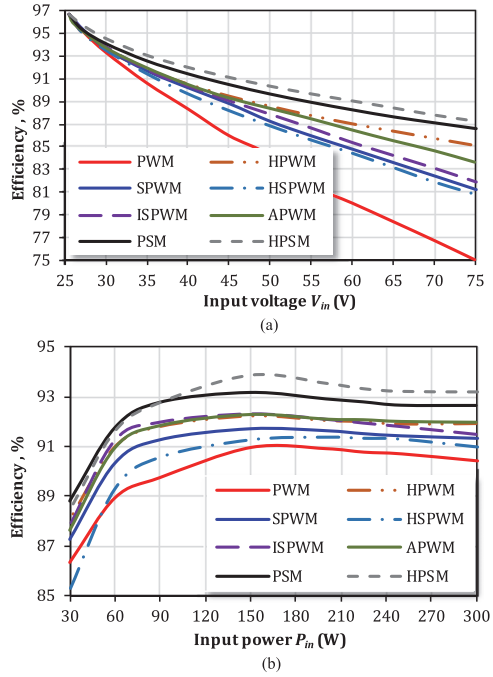

FIGURE 14. Efficiency of the case study SRC at $P = 250$W and different voltage (a); at $V_{in} = 35$ V and different power (b).

between the PSM and the HPSM is associated with the difference in the conduction losses resulting from the magnetizing current flowing through different converter components and the parasitic oscillations, as it was described in Section VI. The number of transistors switched at high current is also two in the APWM and the HPWM methods as well as in the PWM and the HPSM. However, as Table 4 shows, the APWM features the highest amplitude of the switching current and the HPWM has high conduction losses of body diodes. The efficiency curves of the shifted methods are close to each another. The differences of these curves are caused by influence of the parasitic oscillation and the transformer magnetizing current that flows through different converter components. The main drawback of this method is the cumulative switching losses of transistors in comparison with the previous four methods. The PWM has the lowest efficiency. When using the PWM control methods, all transistors are turned off at high current, which results in the dominance of the switching losses.

VII. DISCUSSION OF RESULTS AND FUTURE RESEARCH

This paper focuses on the comparison of the buck control methods to control the SRC. Eight different methods were described in detail. For a comprehensive comparison of these methods, the methodology of power loss calculation was proposed. This methodology is based on the calculation of current and conduction and switching power losses in the used elements of the circuits, such as transistors, body diodes of

MOSFET, rectifier diodes, the transformer, input and output capacitors, input and output resistance of the PCB. Also, the methodology involves the calculation of normalized dc voltage gain.

As can be seen from the experiments, theoretical calculation of the dc voltage gain and power losses based on the methodology are in good agreement with experimental results. However, there are small deviations between the calculated and measured values. In the case of the dc voltage gain, small differences are mostly associated with the assumptions of a lossless system. In the case of power losses, reasons for deviations are parameter drift of circuit elements, variation in the operating temperature of the elements, conduction, and parasitic losses in the PCB. Also, it should be noted that copper losses of the transformer were calculated as conduction losses in the ER of the primary and secondary windings, which was referred to the secondary winding only for simplicity. The magnetizing current usually flows only in one of the windings. This depends on the control method (Table 6). Therefore, the estimation of the transformer copper losses is either slightly overestimated or underestimated. This is a minor drawback of the proposed methodology. In any case, transformer losses prevail over other losses in the built prototype. Future research should address the design of a high-efficiency transformer with high leakage inductance for the SRC as the conventional designs usually result in high ac resistance caused by high proximity losses in the secondary winding of the step-up transformer.

In summary, comparison of the buck control methods shows that the hybrid PSM is the best performing buck control method for the SRC converter. However, the HPSM cannot be used to control a half-bridge converter. Only the PWM, the ISPWM, and the APWM can be used for both full- and half-bridge converters. The results of the comparison between these methods showed that the APWM has high efficiency at different input voltages and different power levels.

It should be noted that in the APWM, two transistors have high switching current; therefore, they have high switching losses and, consequently, higher junction temperature. Thus, the feasible input voltage could be limited. This aspect should be taken into account during the thermal design of the converter.

The other control methods have one, two, or more drawbacks mentioned above, which increases the power losses in the converter. Future research will focus on a synthesis of new control methods based on optimal use of the existing methods and transition between them to achieve high efficiency within a wide input voltage range, which would further extend the converter operating range.

VIII. CONCLUSION

The paper has compared the buck control methods applied to the SRC with the discontinuous resonant current and fixed frequency. This study targets applications with high input current and low input voltage. Eight existing control methods were considered in detail. A methodology of power loss calculation was proposed for the benchmarking. As the experiments demonstrated, the theoretical calculations based on the proposed methodology showed a good compliance with the experimental results. However, a drawback of the methodology is related to the theoretical transformer model. Future research will focus on improving this model.

In summary, the theoretical and experimental comparisons of the buck control methods revealed the HPSM as the best performing buck control method for a full-bridge SRC. It was also found that the APWM is the best buck control method for a half-bridge SRC.

As the analysis of the control methods showed, the main drawback of the SRC with a low-quality factor is in the operation at low duty cycle values, resulting in high RMS current stress of the components, which deteriorates the converter efficiency. Nevertheless, two directions of efficiency improvement could be suggested for the future research: analysis of soft-switching implementation possibilities to reduce the switching losses, optimization of the transformer design to reduce the equivalent resistance of the windings, which causes high conduction losses while keeping relatively high leakage inductance of the transformer.

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Publication III

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Topology Morphing Control with Soft Transients for Multimode Series Resonant DC-DC Converter

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***Abstract*—The paper focuses on the galvanically isolated series-resonant dc-dc converter (SRC) operating at low values of the quality factor of the resonant tank. This topology is considered as a step-up front-end dc-dc converter with buck-boost functionality for integration of renewable energy sources in dc microgrids. The paper proposes the algorithm for soft transitions between half-bridge and full-bridge configurations in the input and output sides of the converter. The converter operates in a wide input voltage range with four control modes and performs soft transitions between them. The algorithm allows for linear recharging of blocking capacitors and stabilizing input voltage and current during transition intervals. The theoretical findings are corroborated with experimental study of converter capability to perform global maximum power point tracking of a photovoltaic module.**

Keywords— Series resonant converter, dc-dc, PSM, soft switching, dc microgrid, half-bridge, full-bridge, transition.

I. Introduction

Residential distributed power systems are becoming increasingly popular due to their high flexibility compared to centralized power systems. Some power sources and storage can operate autonomously and independently from other parts of this system. This feature improves the reliability and resiliency of the distributed power system significantly.

The distributed power systems can be realized based on an ac microgrid or dc microgrid [1]. Using the ac microgrid is the conventional approach because ac grids are utilized for power distribution in the centralized power system for a long time. However, currently, dc renewable energy sources such as solar photovoltaic (PV) modules proliferate rapidly in residential settings. PV energy generation was recognized as the main technology that can achieve the lifecycle cost that is low enough to ensure the market viability of the residential distributed power systems [2]. In practice, PV modules operate in a wide voltage range that depends on solar irradiance, weather conditions, and dirt accumulation on the surface of the modules. As a result of partial shading, one of the substrings can provide more power than the others. Therefore, a global maximum power point tracking (MPPT) is required to find out the voltage and current points of the local and global maximum power points.

Also, the distribution power systems could include energy storage that is usually based on dc batteries. The battery energy storages are getting popular due to simple power scaling and easy installation in comparison with other types of energy storage [2]. On the other side, many devices in buildings are supplied by dc, such as chargers for phones or laptops, TVs, LED lighting, ac home appliances with internal inverters, etc. According to these aspects, using the dc microgrid allows avoiding double transformation energy from dc to ac and then from ac to dc between energy sources, storage, and loads compared to ac grids. As a result, dc microgrids have an efficiency that is more than 11% higher than that of the ac microgrids. Therefore the dc microgrids will be the backbone of the future power distribution system in residential buildings [1], [3].

However, dc microgrids require a front-end step-up dc-dc converter for connecting various dc energy sources and storages to a centralized dc bus with the typical voltage of 350 V. These dc-dc converters should provide a wide input voltage range, galvanic isolation, high efficiency, maximum power point tracking for each energy source, and high-power density. To satisfy these requirements, a galvanically isolated buck-boost converter (IBBC) based on a series resonant dc-dc converter (SRC) with low quality factor of the resonant tank and fixed switching frequency could be used as a front-end converter [4]. The main advantage of this SRC is the availability of numerous control modes resulting in different configurations of a topology. Input and output switching cells of the SRC can operate in full-bridge modes as well as half-bridge modes and can be reconfigured between these operation modes [4], [5]. Using different operation modes allows for changing the normalized dc voltage gain of the converter from 0.5 up to 2. At the same time, buck or boost control modes such as the buck phase-shift modulation (PSM) and the boost PSM can be applied to control input voltage in a wide voltage range in each operation mode (Fig. 1) [6], [7]. Combining different operation modes and different control modes of the converter allows for extending the input voltage range and achieve topology morphing control [8].

Resulting from different configurations of a switching cell, the series blocking capacitors feature different dc voltage stress. During a transition between two switching cell configurations, for example, from a full-bridge to a half-bridge, the blocking capacitor must be rechargeable. This causes high current stress in the circuit, and, consequently, the power semiconductor devices of the SRC can be destroyed [5]. This study aims to achieve soft transitions between possible configurations of the SRC switching cells to avoid high current stress in the circuit.

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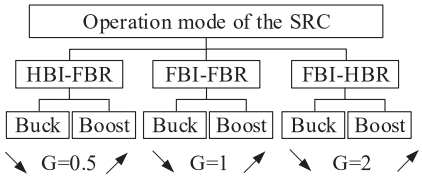

Fig. 1. Operation modes of the multimode SRC

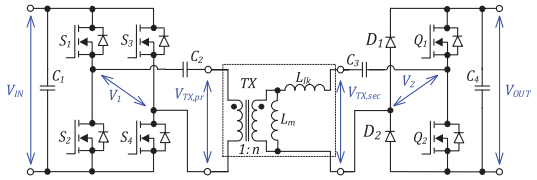

Fig. 2. Topology of the unidirectional multimode series resonant converter

The main contribution of this study is the soft transient algorithm for recharging blocking capacitors in multimode SRC-based IBBC converter with topology morphing control. As an experimental example for algorithm verification, the converter was used as a PV converter operating in a wide input voltage range.

II. Multimode SRC DC-DC Converter

The topology of the given unidirectional multimode SRC-based IBBC is shown in Fig. 2. The topology includes the input inverter based on MOSFETs, the isolation transformer, the primary and secondary blocking capacitors, and the boost rectifier based on diodes and MOSFETs [4], [9]. In this case, only two MOSFETs are used in the rectifier to reduce the number of converter components. The blocking capacitors and leakage inductance of the transformer form the equivalent series resonant tank along with the transformer leakage inductance and the series capacitors. Hence, the angular resonant frequency is defined as

$$\omega_r = \sqrt{\frac{1}{L_{lk} C_r}}, \tag{1}$$

where C_r is the equivalent resonant capacitance calculated as

$$C_r = \frac{C_2 C_3}{C_3 n^2 + C_2}, \tag{2}$$

and L_{lk} is the leakage inductance of the transformer, n is the turn ratio of the transformer.

This topology is considered to operate in the discontinuous resonant current mode, i.e., with the resonant tank quality factor much below one. Hence, the switching frequency should be 5-10% lower than the resonant frequency to implement sufficient dead-time for soft-switching employing the transformer magnetizing current [4].

The blocking capacitors neutralize any dc bias current in the isolation transformer windings. Also, the primary and secondary capacitors allow for reconfiguration of the inverter and rectifier from the full-bridge switching cell into a half-bridge. Therefore, three converter configurations based on combinations of the full-bridge inverter (FBI) or half-bridge inverter (HBI) at the input side, and full-bridge rectifier (FBR) or half-bridge rectifier (HBR) at the output side can be used to extend the input voltage range (Fig. 1).

Previously, the theoretical and experimental analysis showed many different buck and boost control methods for the SRC [4], [6], and [7]. The buck and boost PSM methods can be highlighted as simple and high-efficiency methods for different topology configurations, among others. Below these methods were described in detail.

A. Boost HBI- and FBI-FBR Modes

The boost PSM method can be used in FBI-FBR and HBI-FBR configurations (Fig. 3). In the case of the FBI-FBR configuration, four switches ($S_1 \ldots S_4$) are controlled in two diagonals with complementary signals separated by the dead-times. The average voltages of the blocking capacitors C_2 and C_3 equals zero. In the HBI-FBR configuration, one switch of (S_4) is conduction continuously, while the other is turned off (S_3) compared to the FBI mode. The median voltage $V_{\text{med(C2)}}$ of the primary capacitor C_2 equals $V_{in}/2$. In both configurations, switches Q_1 and Q_2 also operate complementarily. The control signals of the switches are shifted by the duty cycle D_{bt} relative to the control signals of the inverter switches ($S_{1\ldots}S_4$). This modulation shorts the output side of the resonant tank and allows it to accumulate energy. It should be noted, the two output-side transistors (Q_1 and Q_2) are turned off at a high switching current, as can be seen in Fig. 3.

The normalized dc voltage gain of the SRC is defined as

$$G = \frac{V_{out}}{V_{in} \cdot n}. \tag{3}$$

And the gain for the boost mode and the FBI-FBR configuration equals

$$G = \frac{1}{2 - B}\left(1 + \sqrt{1 + 4 A \cdot B \cdot (2 - B)}\right). \tag{4}$$

The expression (4) is presented here for the first time. There are three parameters used to simplify it:

$$A = C_r R f_{SW}, \tag{5}$$

$$B = 1 - \cos(\omega_r D T_{SW}). \tag{6}$$

where R is the resistance of the load, T_{SW} is the switching period, f_{SW} is the switching frequency, D is a duty cycle.

Also, the equation for the duty cycle for the same mode can be written as

$$D_{bt} = \frac{1}{\omega_r \cdot T_{SW}} \arccos\left(1 - \frac{G^2 - G}{0.5 \cdot G^2 + 2 \cdot A \cdot G}\right). \tag{7}$$

The Eq. (7) was presented previously in [6] in another form. In the case of the HBI-FBR configuration, the gain in the boost mode equals

$$G = \frac{1}{2 - B}\left(\frac{1}{2} + \sqrt{\frac{1}{4} + A \cdot B \cdot (2 - B)}\right). \tag{8}$$

And the duty cycle of the boost HBI-FBR mode equals

$$D_{bt} = \frac{1}{\omega_r \cdot T_{SW}} \arccos\left(1 - \frac{2G^2 - G}{G^2 + A \cdot G}\right). \tag{9}$$

The Eqs. (8) and (9) are presented here for the first time.

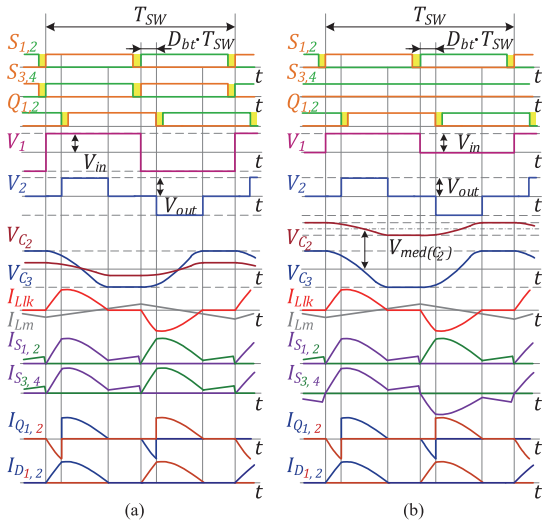

Fig. 3. SRC operation in the boost mode for the (a) FBI-FBR and (b) HBI-FBR configurations

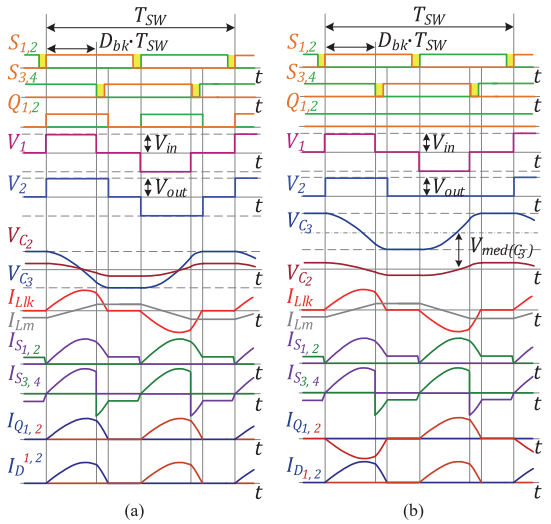

Fig. 4. SRC operation in the buck mode for the (a) FBI-FBR and (b) FBI-HBR configurations

B. Buck FBI-FBR and FBI-HBR Modes

The conventional PSM is used as the buck control method in this study for the FBI-FBR and FBI-HBR configurations (Fig. 4). In these modes, switches of the inverter operate complimentary as in the previous boost modes. However, control signals of one leg (S_3 and S_4) are shifted by the duty cycle D_{bk}. The switches Q_1 and Q_2 operate as synchronous rectifiers in the FBI-FBR mode when the median voltages of two blocking capacitors equal to zero. In the FBI-HBR mode, the switch Q_1 is turned off continuously, while Q_2 is turned on. The median voltage $V_{med(C3)}$ of the secondary-side blocking capacitor equals $V_{out}/2$. In both buck modes, two transistors (S_3 and S_4) are turned off at a high switching current.

The normalized dc voltage gain of the SRC for the buck control method in the FBI-FBR mode equals

$$G = B\left(\frac{1}{4} - A\right) + \sqrt{B^2\left(A - \frac{1}{4}\right)^2 + 2AB}\,. \qquad (10)$$

In addition, an equation for the duty cycle can be defined as

$$D_{bk} = \frac{1}{\omega_r \cdot T_{SW}} \arccos\left(1 - \frac{G^2}{2\cdot A - G\cdot(A - 0.25)}\right). \qquad (11)$$

Equations (10) and (11) are presented the first time here.

In the case of the FBI-HBR mode, an equation for the gain was presented in [10] in the following form:

$$G = \frac{1}{2}\left(B(1-A) + \sqrt{B^2(A-1)^2 + 8AB}\right). \qquad (12)$$

The duty cycle was presented in [5] and can be rewritten as

$$D_{bk} = \frac{1}{\omega_r \cdot T_{SW}} \arccos\left(1 - \frac{G^2}{2\cdot A - G\cdot(A - 1)}\right). \qquad (13)$$

TABLE I. GENERAL PARAMETERS

Operating parameters	
Input voltage, V_{in}	15…60 V
Maximum input current, I_{in}	12 A
Output voltage, V_{out}	350 V
Switching frequency, f_{SW}	100 kHz
Operating power range	30…300 W
Components	
S_1 … S_4	On Semiconductor FDMS86180
D_1,D_2	CREE C3D02060E
Q_1,Q_2	CREE C30075120D
C_1 , C_4	150 µF
C_2	52.8 µF
C_3	25 nF
L_{lk}	95 µH
L_m	2 mH
n	12

III. IMPLEMENTATION OF TRANSITIONS BETWEEN MODES

Described four operation methods enable the SRC to operate at the normalized voltage gain from 0 up to 2. It allows for covering a wide input voltage range in the case of PVapplications. A wide input voltage range is needed for finding the maximum power points of a PV module under partial shading conditions. During a global scanning of a PV-module I-V curve, all control modes are used sequentially from the boost HBI-FBR mode to the buck FBI-HBR. The control system of the converter changes the operation mode modes according to the input voltage (PV module voltage). In the boost and buck FBI-FBR modes, the median voltages of the blocking capacitors equal zero (Fig. 3*a* and Fig. 4*a*). However, the median voltages of the primary or secondary capacitors do not equal to zero when the primary or secondary switching cells operate in the corresponding half-bridge mode, as shown in Figs. 3*b* and 4*c*, respectively. Therefore, when the control system of the converter changes a full-bridge mode to the corresponding half-bridge mode, one of the blocking capacitors has to be recharged.

A. Hard Transitions between Control Modes

Fig. 6*a* shows simulation results of hard transitions from the boost HBI-FBR to the buck FBI-FBR mode, and Fig. 6*b* shows the same from the boost FBI-FBR to the buck FBI-VBR mode. This simulation was carried out in the PSIM software. Table I shows the general parameters of the case-study SRC. The control system was implemented as a closed-loop control system based on the PI-regulator for stabilization of the input voltage according to the reference from the maximum power point tracking (MPPT) algorithm ($V_{in(ref)}$ in Fig. 5). In both mode transitions, the duty cycle of the next control mode was precalculated to reduce over-regulation of input voltage by using equations (7), (9), (11), and (13) according to the next mode.

As can be seen from Fig. 6*a*, when the control system changes the control mode, the high resonance current arises in the primary side of the transformer, the magnetizing inductance, and in the primary switches $S_1 \ldots S_4$ as a result of the fast recharging of the capacitor C_2. This resonant oscillation circulates between the magnetizing inductance L_m and the capacitor C_2. There is a similar situation in recharging the secondary side capacitor C_3 when the control system changes the control mode from the boost FBI-FBR to the buck FBI-VBR (Fig. 6*b*). In this case, the resonant oscillation circulates between the leakage inductance L_{lk} and the capacitor C_3. As can be seen from Fig. 6*b*, the secondary-side switches Q_1, Q_2, and rectifying diodes D_1, D_2 also suffer from high current stress during the transition. In practice, that level of current can destroy semiconductor devices or significantly reduce their lifetime. Besides, the oscillations in the converter could cause unstable operation of the closed-loop control system.

B. Soft Transitions between Control Modes

In this study, a soft transition algorithm is proposed to avoid high current stress in the converter and keep the input voltage tightly regulated. Fig. 7*a* shows ideal waveforms of the converter with the soft transition from the HBI to the FBI, while Fig. 7*b* shows the same from the FBR to the HBR. The main idea of the soft transition algorithm is in linear incrementation or decrementation of the duty cycles of switches S_3, S_4 or Q_1, Q_2 due to their static operation in one of the adjacent modes during the transition. For example, in the transition from the boost HBI-FBR to the buck FBI-FBR mode, the switches S_3 and S_4 should come to switching operation with the duty cycle D_{am} of 0.5 from the opened and closed states, respectively. At the same time, the control duty cycle of the corresponding buck or boost mode changes linearly too. For the same example, the boost duty cycle D_{bt} is decreased from initial value before the transition to zero, and the buck duty cycle D_{bk} is decreased from 0.5 to the precalculated value according to Eq. (10). This algorithm provides linear recharging of the capacitor C_2 and allows for maintaining the input voltage at a regulated level during the transition time $T_{tr(C2)}$, which can be calculated as

$$T_{tr(C2)} \geq 2 \cdot \pi \cdot \frac{\sqrt{L_m \cdot C_2}}{n} . \qquad (14)$$

In the case of transition from the FBR to the HBR, the buck and boost duty cycles are changed linearly in the same way as in the previous transition. Simultaneously, switches Q_1 and Q_2 are switched with linearly decreasing and

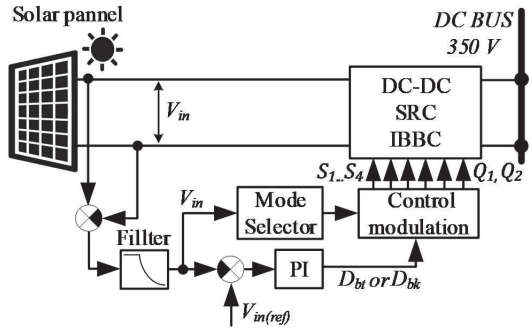

Fig. 5. Block diagram of the control system

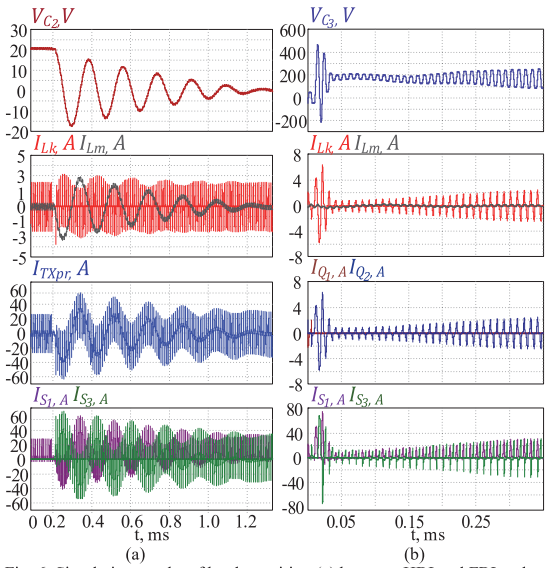

Fig. 6. Simulation results of hard transition (a) between HBI and FBI and (b) between FBR and HBR modes

increasing duty cycle, respectively, during the transition time $T_{tr(C3)}$. The transition time is defined as

$$T_{tr(C3)} \geq 2 \cdot \pi \cdot \sqrt{L_{lk} \cdot C_3} . \qquad (15)$$

Simulation results of the algorithm implementation for two types of transitions are shown in Fig. 8. In both cases, transitions are being implemented without any overcurrent or parasitic oscillations.

IV. Experimental Results

For verification of the operation in the described modes and transitions between them, a prototype of the SRC converter was built (Fig. 9). The main components used in the prototype are listed in Table I. The previous analysis showed that a high value of the resonant inductance decreases power losses in the converter [7]. For this reason, an external inductor L_r was used in series with the secondary winding of the transformer. The following measurement equipment was used: oscilloscope Tektronix DPO7254, differential voltage probes Tektronix P5205A, current sensors Tektronix TCP0030A, and precision power analyzer Yokogawa WT1800.

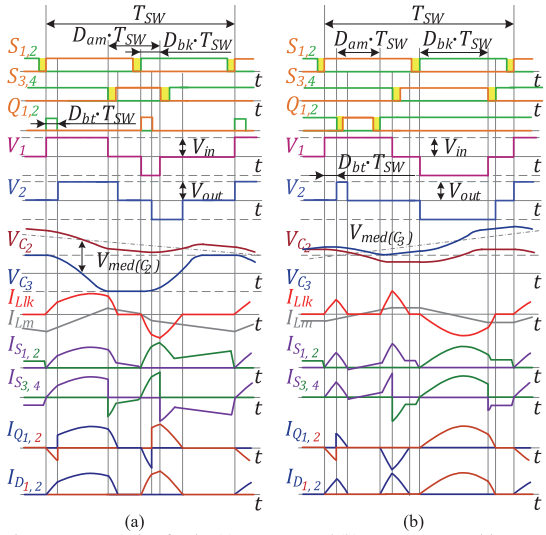

Fig. 7. SRC operation for the (a) HBI-FBI and (b) FBR-HBR transitions

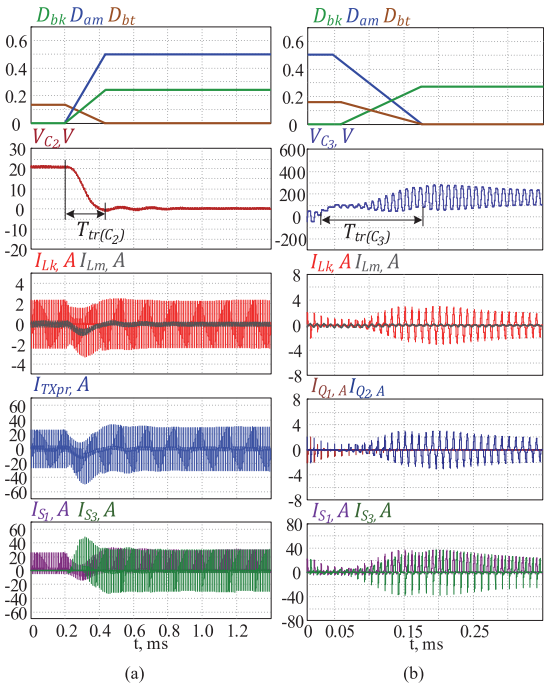

Fig. 8. Simulation results of soft transition (a) between HBI and FBI, and (b) between FBR and HBR

A. Static Characteristic

Static experimental analysis shows the efficiency of the prototype with the described control modes at $I_{in} = 12$ A for the input voltage range of $V_{in} = 15…25$ V, and at $P_{in} = 300$ W for the input voltage range of $V_{in} = 25…60$ V (Fig. 10), which are the maximum input current and power of the prototype. At $V_{in} = 15$ V, $V_{in} = 29$ V, $V_{in} = 59$ V, the SRC operates in the normal mode, where switches are turned on and off at zero current because the transformer current is virtually sinusoidal. With an increase or decrease of the input voltage, efficiency decreases. This is mostly associated with

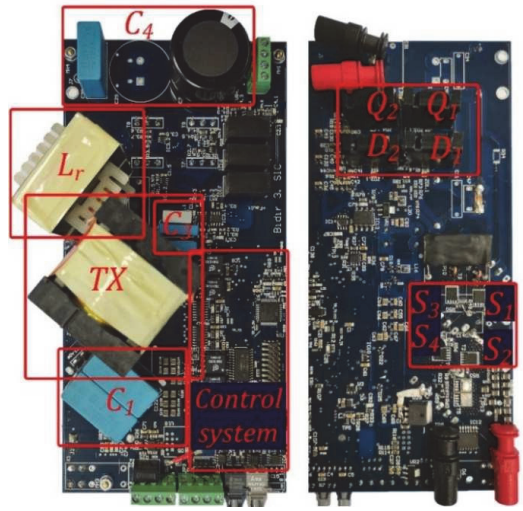

Fig. 9. Prototype of the SRC converter

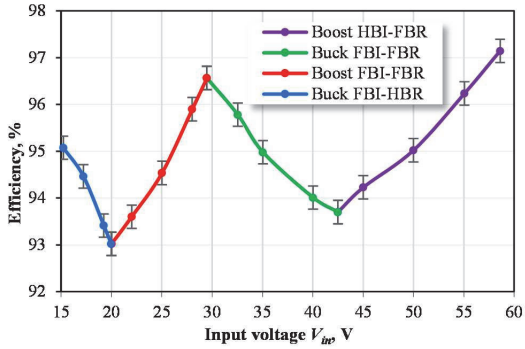

Fig. 10. Measured efficiency of the SRC prototype for four modes

TABLE II. PARAMETERS OF PV MODULE LR4-72HBD-425M

Irradiance	700 W/m^2
Temperature	20 ^{0}C
Open circuit voltage, V_{OC}	48 V
Short circuit current, I_{SC}	7.85 A
Maximum power, P_{MAX}	300 W
Voltage at maximum power, V_{MP}	39.9 V
Current at maximum power, I_{MP}	7.42 A
Module efficiency	19.6 %

the increasing RMS and switching currents in the converter. As a result, losses in the prototype components are increased. The maximum efficiency of the prototype equals 97.2% at $V_{in} = 59$ V and $P = 300$ W. As can be seen from Fig. 10, the efficiency curves of the boost HBI-FBR and buck FBI-FBR modes are crossed at $V_{in} = 42$ V. This is the point for the transition between the HBI and the FBI configurations. In addition, $V_{in} = 20$ V is the point for the transition between the FBI-FBR and the FBI-HBR configurations.

B. Transitions between Control Modes

In dynamic transitions between configurations, the proposed algorithm allows the control system to change control modes smoothly. Fig. 11 shows the global MPPT

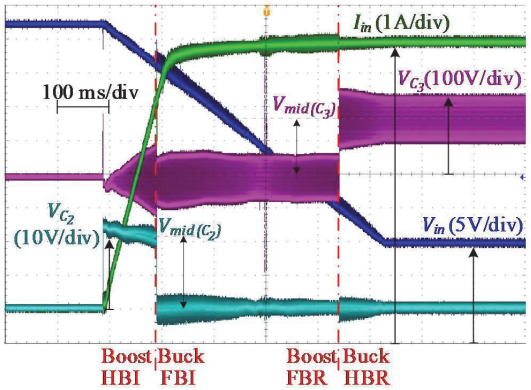

Fig. 11. Global MPPT scanning of the PV module characteristics.

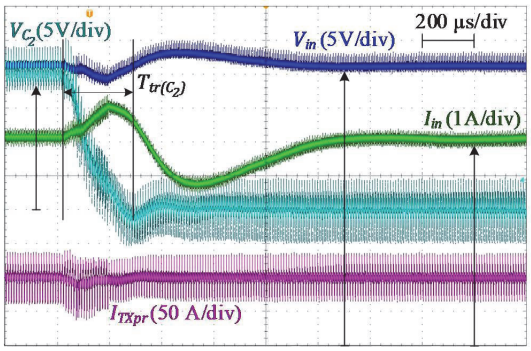

Fig. 12. Experimental waveforms of the transition from the boost HBI-FBR to the buck FBI-FBR mode at V_{in} = 42 V.

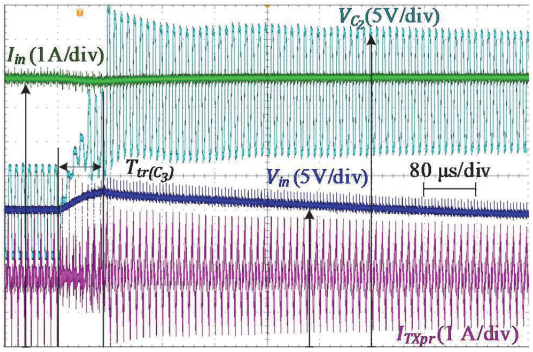

Fig. 13. Experimental waveforms of the transition from the boost FBI-FBR to the buck FBI-HBR mode at V_{in} = 20 V.

scanning of a PV module in the voltage range from 48V to 15 V. The PV module was simulated using Keysight Modular Solar Array Simulator E4360A. The parameters of the PV module are listed in Table II. The control system changes configurations of the inverter at V_{in} = 42 V and the rectifier at V_{in} = 20 V.

Zoomed intervals of two transitions between the HBI and FBI, and between the FBR and HBR configurations are shown in Figs. 12 and Fig. 13, respectively. The converter transits between modes without oscillations or high peaks in currents and voltages. Moreover, the experimental results correspond to simulation results shown in the previous section in Fig. 8. There are small oscillations in the input voltage and current after transitions between modes, but they do not influence global MPPT scanning since the control system is waiting for the input voltage stabilization before it continues the scanning.

V. Conclusion

The paper has demonstrated the proposed algorithm for soft transitions between different control modes and topology configurations of the SRC. The algorithm allows for avoiding oscillations and high peaks in currents of the converter caused by recharging blocking capacitors. The experimental results show that the input voltage and current are stabilized during the mode transitions. It was achieved by online calculations of the control duty cycle expected after mode transition for each method. Then, the duty cycles of the switches and the control duty cycles were changed linearly according to the precalculated critical transition duration times. As a result, smooth transitions were also achieved experimentally.

The paper has shown that using different control modes allows the converter to operate in the wide input voltage range from 15 V to 60 V with high efficiency of up to 97.2%. Future research will focus on application-oriented studies of the given SRC.

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Publication IV

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High-Frequency Split-Bobbin Transformer Design with Adjustable Leakage Inductance

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***Abstract*—**While designing a high-frequency transformer, its parasitic components should be modeled with caution as it influences the performance of the transformer. In many converter topologies, a transformer with specific parasitic components could be needed. For example, in the phase-shifted full-bridge converter, bidirectional dual active bridge converter dc-dc converters, or LLC resonant converters, the leakage inductance of the transformer needs to be precise as it influences the overall performance of the converter. In this paper, a simple yet effective technique has been investigated to design high-frequency transformers with adjustable leakage inductance. The transformer is designed to be used in a 100 kHz series resonant dc-dc converter, where the leakage inductance of the transformer is used as the resonant inductor. The proposed design technique utilizes the variation of the winding structures where a split bobbin separates primary and secondary windings. At first, the finite element analysis (FEA) based simulation is performed to estimate and analyze the leakage inductance with different winding structures, and then the experimental investigations are performed. Both the simulation and experimental results demonstrate that by simply varying the winding arrangements in the hybrid split-bobbin transformer, the leakage inductance can be changed while keeping the magnetizing inductance of the transformer constant.

Keywords—high-frequency transformer, leakage inductance, split-bobbin transformer, series resonant converter

I. INTRODUCTION

High-frequency transformers are essential elements in power electronic converters for changing the voltage level as desired. Depending on the windings, they can step up or down the voltage to the target level. They also add galvanic isolation to the converters. However, one of the main design concerns for designing a high-frequency transformer is to keep the parasitic components of the transformer within the desired range, as the parasitic components have a significant impact on the transformer efficiency and performance.

Two main parasitic components in a transformer are leakage inductance and stray capacitance. This paper mainly focuses on the estimation and adjustment of leakage inductance of the transformer, which is an inductive element resulting from the imperfect magnetic linking between two windings. Higher leakage inductance in a transformer indicates weaker coupling between the primary and secondary windings, which could reduce the efficiency of the transformer due to more substantial proximity effect increasing losses in windings. Furthermore, higher leakage inductance could lead to voltage spikes across the switches in some topologies. Also, it causes electromagnetic interference (EMI) in the converter, which increases switching losses and reduces the overall efficiency [1], [2]. Therefore, many research works have been published on reducing the leakage inductance in a transformer. For example, the interleaved winding arrangement has been proven an effective method for reducing the leakage inductance [3].

On the other hand, in many applications, transformers with tuned leakage inductance are required. Phase-shifted full-bridge dc-dc, bi-directional dc-dc, LLC resonant dc-dc converters can be mentioned to name a few topologies that essentially utilize the transformer leakage inductance. For example, in phase-shifted full-bridge dc-dc converters, the value of leakage inductance, i.e., the energy stored in the transformers leakage inductance, sets the achievable load range under the soft switching (zero voltage switching) operation [3]. In this case, a comparatively large leakage inductance is required. In [4], a 15% volume reduction has been achieved from a more precise design of the leakage inductance value. The efficient operation of resonant converters could rely on the precise value of the transformer leakage inductance. For instance, the LLC topology utilizing the transformer leakage as a resonant inductor drastically reduces the converter weight, size, and volume [5]

Several attempts have also been made on optimizing the leakage inductance, and different parameters are taken into consideration in this regard. In [3], non-interleaved, interleaved, partial interleaved, and the proposed half-turn winding structures are compared for different leakage inductance values. A new method of interleaving foil windings named “Partial interleaving” is proposed in [6] to adjust the leakage inductance. However, the limitation of this method is that the partial interleaving is typically suitable for transformers having a turns ratio close to 1. In [7], Toroidal, UU and EE cores in combination with windings structure variations are used to achieve a wide range of leakage inductance for high-frequency isolation applications. In [8], with the help of 2-D FEA analysis, it is demonstrated that an optimal leakage inductance can be achieved using different combinations of winding arrangements. In this study, the arrangement of both the primary and the secondary windings is changed.

The transformer that has been discussed in this study is a step-up transformer that is to be used in a 100 kHz Series Resonant Converter (SRC) capable of working in a wide range of input voltage and rated power. This converter is particularly

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suitable to be used as a front-end converter in dc microgrids. The converter operates in discontinuous resonant current mode (DrCM) operation. The leakage inductance of the equipped transformer for the specified SRC converter needed to be optimized so that the converter is allowed to function in DrCM and wide operation range. At the same time, the winding loss of the transformer is also minimized. A study with graphical illustration is presented in [9] on how leakage inductance impacts the power loss for the considered SRC converter.

A simple design technique is proposed in this paper in order to tune the leakage inductance for a split-bobbin transformer having a turns ratio of 4:54. In a split-bobbin transformer, the primary and secondary windings are placed vertically side-by-side on a bobbin with an insulation barrier between the two windings. This type of winding architecture provides superior isolation and low capacitive coupling between the windings [10]. The proposed design takes advantage of this split-bobbin design implemented in an ETD 49/25/16 core type. It has been demonstrated in this paper that by placing a portion of the secondary windings (i.e. several turns of the secondary winding) just next to primary winding (or in other words overlapping portion of the secondary winding with the primary), the leakage inductance value changes significantly. Moreover, the value of the magnetizing inductance is not affected, which is desired in this application. Therefore, the proposed design technique offers a degree of design flexibility since the leakage inductance can be designed independently of the magnetizing inductance of the transformer.

The paper is arranged as follows: Section II describes the considered the case study SRC topology; the winding structures of the proposed split-bobbin transformer are presented in Section III; simulation and experimental results are demonstrated in Section IV; finally, Section V concludes the paper.

II. Series Resonant Dc-Dc Converter

The series resonant dc-dc converter (SRC) offers a number of advantages such as high efficiency, galvanic isolation, soft-switching which makes it a suitable candidate to be used in dc microgrid systems. Furthermore, according to a recent study conducted on SRC with the discontinuous resonant current mode (DrCM) converters, the SRC converters are capable of operating in a wide input voltage range [11].

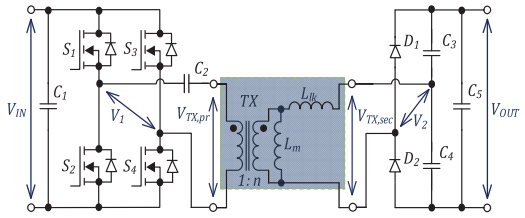


Fig.1. Schematic Diagram of the Series Resonant dc-dc Converter

The schematic diagram of the SRC converter considered for this study is shown in Fig.1. The converter consists of three main parts: the input side full-bridge inverter, isolation transformer, and the output side voltage doubler rectifier (VDR). In the full-bridge inverter, MOSFETs are used as the switching elements, and the voltage doubler circuit is consists of two diodes and two capacitors. A dc blocking capacitor is connected in series with the transformer primary winding, which neutralizes any dc bias current in the isolation transformer winding. Thus, reconfiguration of the full-bridge switching cell to the half-bridge configuration is also possible. In this study, the SRC converter functions in the discontinuous resonant current mode (DrCM), meaning that the resonant tank quality factor is below 1. Hence, the switching frequency should be 5-10% lower than the resonant frequency to implement sufficient dead-time for soft-switching employing the transformer magnetizing current [12].

The angular resonant frequency of the resonant tank of the converter is formulated as [13]

$$\omega_r = \frac{1}{\sqrt{L_{lk} C_r}}, \tag{1}$$

where L_{lk} is the leakage inductance of the transformer, the resonant capacitance can be derived as follows [13]

$$C_r = \frac{C_2[C_4C_5 + C_3(C_4 + C_5)]}{C_4C_5n^2 + (C_3n^2 + C_2)(C_4 + C_5)}, \tag{2}$$

where C_2,..., C_5 are the capacitors shown in the schematic diagram (Fig .1), and n is the transformer turns ratio.

III. Split-Bobbin Transformer Design

A. Transformer Parameters

For the specified SRC converter, a step-up transformer with 4:54 turns ratio is designed using split-bobbin to separate the primary and secondary windings. The transformer parameters are listed in Table I. Depending on the input-output parameters and operating frequency Ferroxcube ETD 49/25/16 core from 3C95 material is selected and verified experimentally. This core has a window area of 342 mm^2 and an effective cross-section area of 211 mm^2. More information about the core and 3C95 material can be found in [14] and [15].

TABLE I. Transformer parameter specification

Parameters	Values
Primary Voltage	27-75 V
Secondary Voltage	350 V
Max Primary Current	25 A
Max Secondary Current	1.8 A
Switching Frequency	100 kHz
Duty Cycle	< 0.5
Np: Ns	4: 54
Core	ETD 49/25/16
Air gap	0.2 mm

FR4 material (textolite) is used for splitting the primary and secondary windings. Polyimide tape is used for general insulation purposes. Litz wires are popularly used in high-frequency transformers for minimizing the skin and proximity effects. For the primary winding of the transformer, 2 parallel wires of 2000×0.04 mm (each has 2.8 mm outer diameter) are

used to share the input winding current. The diameter of the secondary side wire of 660×0.04 mm equals 1.5 mm.

B. Winding Structures

Three different winding structure cases are considered for comparison and evaluation of the proposed technique of leakage inductance adjustment. The technique is based on hybrid split-bobbin transformer design. In a conventional split-bobbin design, the primary and secondary turns are completely separated from each other by insulation material as shown in Fig. 2(a). From Fig. 2(a), the primary turns are wound around the central leg of the transformer and placed in the bottom section. On the other hand, the secondary winding turns are completely separated from the primary windings and are placed at the top section in the core. This is a conventional split-bobbin winding structure. However, it is found that if a portion of the secondary winding is placed next to the primary winding at the bottom side making overlapping of the primary and secondary winding at the bottom side, leakage inductance in the transformer reduces. This is because when a portion of secondary turns are placed close to the primary turns and overlap, the coupling between the two winding increases which in turn reduces the leakage inductance.

Three winding arrangements considered in this study are as follows:

Case 1: Conventional Split-bobbin winding arrangement as illustrated in Fig. 2(a). The complete secondary winding (all 54 turns) is placed at the top section. The primary winding is at the bottom section.

Case 2: Primary winding is fixed and placed at the bottom section. However, four secondary turns are placed at the bottom side next to the primary winding, side by side, as shown in Fig. 2(b). Thus, in this case, 50 secondary turns are at the top section and 4 secondary turns at the bottom section.

Case 3: Fourteen secondary turns are placed at the bottom side next to the primary winding, and the rest (40 turns) are in the top section. It is to be mentioned here that considering the core geometry and the diameter of the wires, maximum of 14 secondary turns can be placed at the bottom section next to the primary winding. The winding arrangement for case 3 is demonstrated in Fig. 2(c).

IV. Simulation and Experimental Results

The inductance values for the three above-mentioned cases are at first estimated through simulation. Power Electronics Magnetics (PEmag ™) powered by ANSYS is used for calculating the inductance and ac resistance values. PEmag is used for generating and solving magnetic component models based on either analytical expressions or Finite Element Analysis (FEA) calculations. The generated model can also be transferred to ANSYS Maxwell.

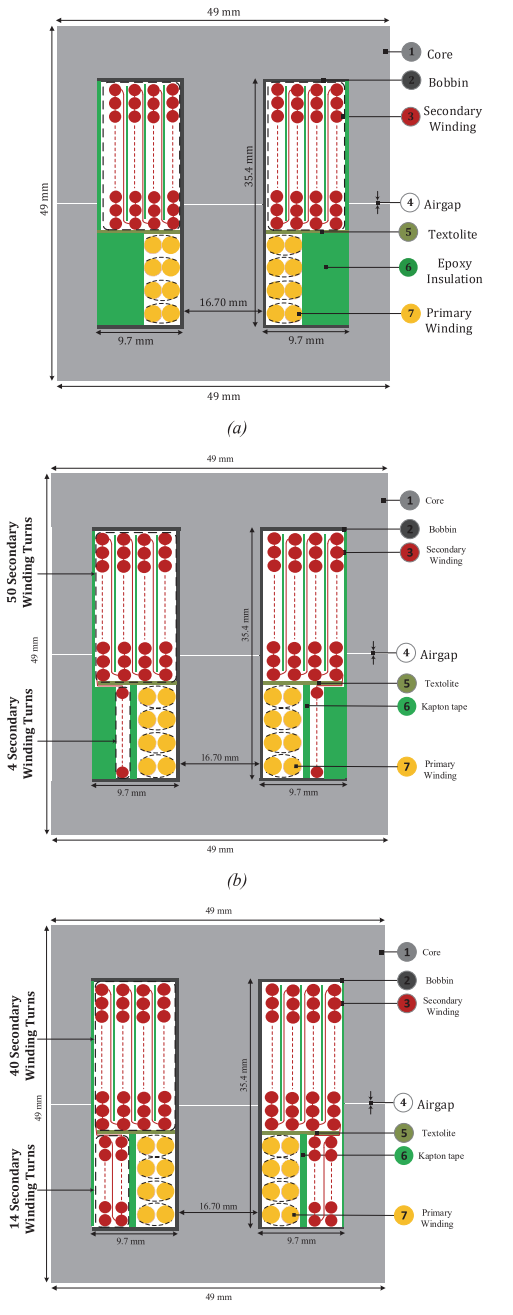
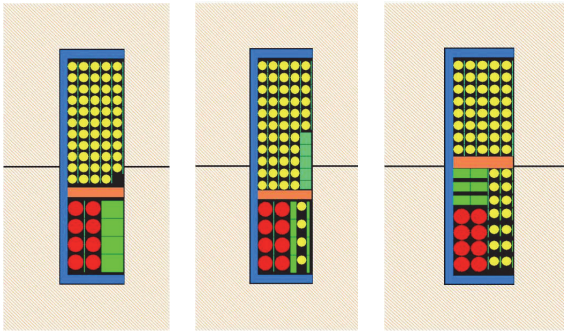


Fig. 2. Three winding arrangements: (a) Case 1 – all the secondary winding turns are placed at the top section of the core, (b) Case 2 – 50 secondary winding turns are at the top section and 4 winding turns are at the bottom section, (c) Case 3 – 40 secondary winding turns are placed at the top section and 14 winding turns are placed at the bottom section

The transformer models of the three different cases (Case 1, 2, and 3) constructed in PEmag are illustrated in Fig 3. The inductance values for the three winding configurations (Case 1, 2 and 3) are also listed in Table 2 and compared with the experimental values. It should be noted that the values for the leakage inductance specified in this study are reflected to the secondary side of the transformer as represented in Fig. 1.

After estimating the leakage inductance of the transformer through PEmag simulation, a prototype transformer was built and measurements were taken for the three cases separately using Hameg HM8118 LCR Bridge. The experimental setup and device arrangements are shown in Fig 4.

The simulated and measured inductance values are listed in Table II. The table shows that the leakage inductance value in the designed split-bobbin transformer is highest for Case 1 and lowest for Case 3 design. The leakage inductance value decreases from Case 1 to Case 3, meaning that as more secondary turns are placed over the primary winding in the bottom part of the transformer, the coupling between the primary and secondary sides increases.



(a) (b) (c)

Fig 3. Winding arrangements in PEmag: (a) Case 1, (b) Case 2, and (c) Case 3.

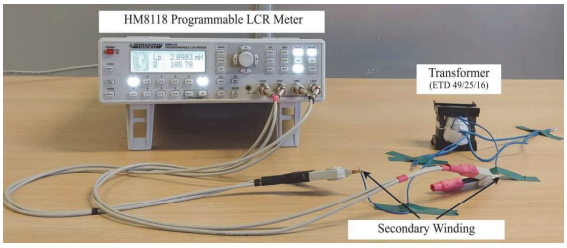


Fig 4. Experimental setup for measurements.

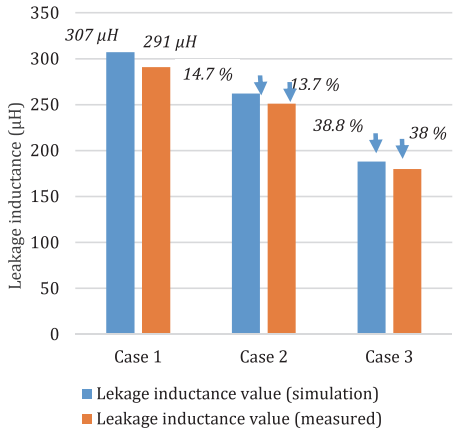


Fig 5. Variation of leakage inductance with partially overlapping windings.

The leakage inductance reduction (in percentage) with the overlapping of the primary and secondary windings is illustrated in Fig 5. Both simulated and measured values are presented in Fig 5. The percentage of the leakage inductance reduction has been calculated with respect to the leakage inductance value with no windings overlapping (Case 1). As the overlapping between the primary and secondary winding increases by placing more secondary winding next to the fixed primary winding, the leakage inductance reduces significantly. From the measurements, 13.7 % of leakage inductance reduction is achieved by the placement of only 4 turns of secondary next to the primary winding. The leakage inductance reduction of 38 % was achieved for Case 3, where the maximum number of the secondary turns (14) overlaps with the primary winding.

Another significant advantage of this design technique is that it is not affecting the value of the magnetizing inductance. From Table II, the changes in the magnetizing inductance at the primary and secondary winding are negligible. Therefore, by only overlapping a portion of the secondary winding in a split-bobbin transformer, the transformer leakage inductance can be adjusted. It is difficult to get an exact estimation of magnetizing and leakage inductance value through simulation since, in practice, some non-idealities always exist in the transformer core geometry and overall assembly. Hence, the finite element simulation provides a very good estimation of the transformer leakage inductance which matches the experimental measurements.

TABLE II. Comparison of inductance values between simulation and experimental results

Winding configuration	Simulation results			Experimental results		
	Magnetizing inductance of the primary winding	Magnetizing inductance of the secondary winding (L_m)	Leakage inductance (L_{lk})	Magnetizing inductance of the primary winding	Magnetizing inductance of the secondary winding (L_m)	Leakage inductance (L_{lk})
Case 1	11.73 µH	2.09 mH	307 µH	12.92 µH	2.12 mH	291 µH
Case 2	11.73 µH	2.08 mH	262 µH	12.93 µH	2.16 mH	251 µH
Case 3	11.85 µH	2.08 mH	188.2 µH	12.90 µH	2.09 mH	180.5 µH

V. Conclusion

This paper describes a simple method of tuning the transformer leakage inductance in a hybrid split-bobbin transformer design. The split bobbins are used in many high-frequency transformers, where an insulation barrier separates the primary and secondary windings. Thanks to this design method, transformers can be constructed more compactly without compromising the insulation requirement. However, the split-bobbin transformer offers another design advantage that is not explored much in the previous studies. That is by partially overlapping the primary and secondary windings, the leakage inductance of the transformer can be adjusted. Moreover, magnetizing inductance is not affected by changes in windings overlap, which enables the independent design of the leakage and magnetizing inductances.

The investigated design technique can be beneficial to design transformers for high-frequency applications such as resonant converters, where leakage inductance plays a crucial role. The proposed technique is validated by simulation results and experiments are performed on a prototype transformer in support of the claims. They demonstrate up to 38% reduction in the transformer leakage inductance by overlapping up to 14 turns out of 54 secondary turns with the primary winding.

Acknowledgment

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Publication V

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Bidirectional Isolated Hexamode DC–DC Converter

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***Abstract*—The proposed isolated buck–boost series resonant dc–dc converter contains two full-bridge hybrid switching cells capable of half-bridge operation. This feature is regarded as topology morphing control. Voltage buck regulation requires special modulations applied to the primary-side hybrid switching cell. In contrast, voltage boost regulation requires special modulations for the secondary-side hybrid switching cell. Combining the topology morphing control with the buck–boost regulation capability, a novel dc–dc converter operating in six different modes was derived. Moreover, the converter is capable of bidirectional operation. This article describes the influence of the topology morphing control on the dc voltage gain of the converter, which results in three boost and three buck modes. The six modes are described, and equations for the converter's dc voltage gain are provided. Based on the selected design guidelines for the power part and the control system, a 350-W prototype was designed and built. Experimental results confirm the theoretical expressions for the converter's dc voltage gain. Experimental efficiency is provided in a wide input voltage range for both energy transfer directions. Operating points with the highest thermal stress of components are analyzed with corresponding power loss breakdown calculations, confirming the measured thermal results.**

***Index Terms*—Bidirectional power flow, DC-DC power converters, microgrids, series-resonant converters, topology morphing control.**

I. Introduction

THE proliferation of dc distribution is anticipated in energy-efficient buildings in the near future [1]. Considering the dc nature of renewable energy sources and battery storage, high step-up dc–dc converters have been extensively studied in the last decade [2]. Numerous topologies, both nonisolated and isolated, were proposed. The isolated dc–dc converters could be considered a preferable solution for residential applications since the isolation barrier serves as an extra safety measure [4].

Recent studies have focused on isolated dc–dc converters with a wide input voltage range to accommodate the demands of emerging applications, such as parallel photovoltaic (PV) power optimizers, modular battery energy storage, and chargers for electric vehicles. Isolated buck–boost converters show the most promising performance in the distributed energy generation [5], [6]. They could be implemented using either one advanced switching cell, like quasi-Z-source [7], or two switching cells [8]. Among the latter type, series resonant buck–boost converters with the low quality factor of the resonant tank are justified as suitable solutions for numerous applications [9]. They are characterized by simple implementation, constant switching frequency, soft-switching, and a wide input voltage range [10].

Initially, series resonant topologies are buck converters by their nature, which can be controlled at the fixed switching frequency if their quality factor is below unity for all operating conditions [11]. By adding a secondary-side semiactive or active switching cell, it can achieve a voltage boost functionality [12]. This cell short-circuits the resonant inductor or the resonant tank to increase the energy stored, like in the conventional boost converter. The transition point between the two modes is tuned for the nominal input and output voltage.

Recent literature mainly describes the application of different voltage boosting cells at the secondary side of the series resonant converters (SRCs) to extend their regulation range. All of those cells are based on the concepts of active and semiactive rectifiers used in ac–dc applications. One of the first and simplest approaches is to short-circuit the resonant inductor by a four-quadrant switch while feeding the transformer secondary winding with voltage [8]. Even though this approach attracted significant interest [13]–[16], it suffers from the input voltage regulation range that is limited at high step-up ratios and load currents [17]. Boosting cells that short-circuit the entire resonant tank provide better voltage regulation capabilities, but higher losses in semiconductors.

In high step-up applications, the use of the half-bridge, i.e., the voltage doubler rectifier, could be recommended. There are two known implementations: with two switches and balanced current stress of the resonant tank [12] and with one switch resulting in higher efficiency but increased current stress of the resonant tank components [18]. Nevertheless, an SRC-based buck–boost converter with a full-bridge semiactive rectifier demonstrated high performance in [19]. On the other hand, its light-load efficiency was reduced compared to the converter with the half-bridge rectifier (HBR) due to the extra losses in a higher number of components and a transformer with a twice higher turns ratio.

The main drawback of the SRC-based isolated buck–boost dc–dc converters is that their performance deteriorates when the

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voltage boost or buck ratio is increased. As a result, efficiency at the maximum or minimum input voltage is much lower than at the nominal voltage with no voltage boost or buck. The latter operating point could be regarded as the pass-through or dc transformer (DCX) mode that provides the highest possible efficiency for the given arrangement of the primary-side inverter and secondary-side rectifier. The topology morphing control (TMC) can make use of these DCX modes and provide a more balanced converter performance across a wide input voltage range [10]. It can be done by reconfiguring one switching cell into another, like full-bridge to half-bridge.

Recently, several attempts were made to apply the TMC to the SRC-based buck–boost dc–dc converters. However, they considered only limited cases of TMC. For example, in [20], the secondary-side boosting switching cell was reconfigured between asymmetrical full-bridge and asymmetrical half-bridge. This provided a sizable extension of the high efficiency range. However, it was proposed for a low step-up converter, whereas it is known from [21] that the asymmetrical full-bridge boost rectifier provides relatively poor performance in high step-up applications. Second, in [22], the primary-side switching cell changed its operation by changing modulation to extend the high efficiency range. Third, the primary-side full-bridge was reconfigured into the half-bridge in [22], which improved efficiency but resulted in a significant efficiency step change, compromising the converter's long-term reliability.

Another but less obvious advantage of the TMC application in the given converters is avoiding abnormal operation conditions when the voltage of the resonant capacitor(s) exceeds a certain limit, and a converter could suffer from high circulating currents [24]. This could happen at high-voltage boosting factors, whereas in TMC applications, this factor should not exceed twofold [10].

This article aims to demonstrate the full power of the TMC in an application of the SRC-based buck–boost converter by utilizing the hybrid switching cell capable of operating with different modulations on both converter's sides. Section II presents the proposed converter that features six operating modes, three buck and three boost modes, along with the analysis of the converter's operation. Section III deals with the selected design guidelines for the power part and control system. Our experimental results are given in Section IV. Finally, Section V concludes the article.

II. Bidirectional Isolation Hexamode DC–DC Converter

The topology of the proposed isolated hexamode bidirectional dc–dc converter (IHMC) consists of two versatile hybrid switching cells and a step-up isolation transformer (see Fig. 1). The topology is symmetrical; therefore, the IHMC can operate in two power flow directions. Blocking capacitors are included in the hybrid switching cells that allow for morphing the hybrid switching cells from full-bridge to half-bridge by turning ON one switch and turning OFF the other one in one leg, as shown in Fig. 2. Topology morphing in each switching cell causes a change in the dc voltage gain G of the converter. Therefore, the

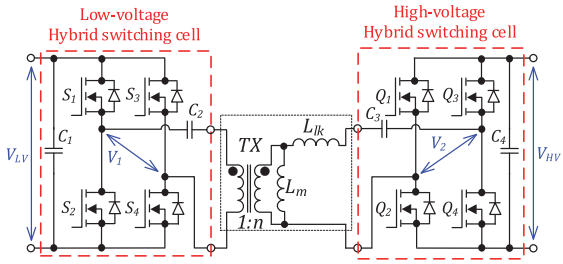

Fig. 1. Proposed isolated bidirectional hexamode dc–dc converter.

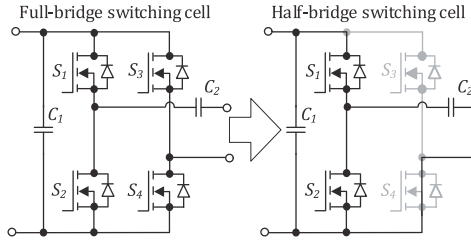

Fig. 2. Reconfiguration of the hybrid switching cell.

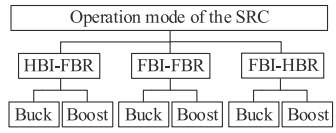

Fig. 3. Operation modes of the proposed hexamode SRC.

converter can operate in three configurations based on combinations of the full-bridge inverter (FBI) or the half-bridge inverter (HBI) at the input side, and the full-bridge rectifier (FBR) or HBR at the output side can be used to extend the input voltage range (see Fig. 3). At the same time, the switching cells allow for applying different buck and boost control methods. The combination HBI–HBR is not used in the proposed converter because the gain is the same as in the FBI–FBR, but it suffers from doubling the current stress.

In addition, the blocking capacitors neutralize any dc bias current in the isolation transformer windings, which allows for applying different asymmetrical control methods [9]. Besides, the blocking capacitors and leakage inductance of the transformer form the equivalent series resonant tank along with the transformer's leakage inductance and the series capacitors.

Hence, the angular resonant frequency is defined as follows:

$$\omega_r = \sqrt{\frac{C_3 n^2 + C_2}{L_{\rm lk} C_2 C_3}} \tag{1}$$

where $L_{\rm lk}$ is the leakage inductance of the transformer and n is the turns ratio of the transformer.

This topology is considered to operate in the discontinuous resonant current mode, i.e., with the resonant tank quality factor much below unity. Hence, the switching frequency should be

5%–10% lower than the resonant frequency to implement sufficient dead-time for soft-switching employing the transformer magnetizing current [10].

Different buck and boost control methods have been demonstrated for controlling the gain in SRCs [9], [10]. Among others, the hybrid phase-shift modulation (HPSM) and the asymmetrical pulsewidth modulation (APWM) can be highlighted as the high-efficiency buck control methods for FBI and HBI configurations, respectively. Among the boost control methods, the PSM and the APWM are the methods that perform best for both FBR and HBR configurations, respectively. The same control modes can be applied for the backward as well as for the forward power flow directions.

The normalized dc voltage gain of the IHMC for the forward power flow can be defined as follows:

$$G = \frac{V_{\rm HV}}{V_{\rm LV} \cdot n} \tag{2}$$

and for the backward power flow, the voltage gain equals

$$G = \frac{V_{\rm LV} \cdot n}{V_{\rm HV}}. \tag{3}$$

The operation modes for the forward power flow described below are grouped into boost and buck, as this converter is still essentially a buck–boost converter with three configurations.

A. Buck Control Modes

In the HPSM, the voltage gain is controlled by the phase-shift duty cycle $D_{\rm bk}$ between the leading-leg switches (S_1 and S_2) and the lagging-leg switches (S_3 and S_4), as shown in Fig. 4(b) and (c). To avoid parasitic oscillations and maintain magnetizing current circulation on the primary side, the conduction times of switches S_1 and S_2 are decreased. Switches Q_1–Q_4 operate as synchronous rectifiers. At the beginning of each half-period, one pair of switches, either Q_1 and Q_3 or Q_2 and Q_4, is turned ON, increasing the current that circulates through respective switches. When the current is decreased to zero, the rectifier switches are turned OFF. However, in the FBI–HBR mode, switch Q_1 is turned OFF continuously, whereas Q_2 is turned ON. And only two switches, Q_3 and Q_4, operate as synchronous rectifiers. As a result, the median voltage $V_{\rm med(C3)}$ of the secondary-side blocking capacitor equals $V_{\rm HV}/2$ [see Fig. 4(c)], whereas in the FBI-FBR mode, the median voltage $V_{\rm med(C3)}$ equals zero [see Fig. 4(b)]. The median voltage is used here as the average value is different from it due to the asymmetric operation of each switching cell. In both buck modes, all transistors are turned ON at zero current, and only two transistors (S_3 and S_4) are turned OFF at a high switching current.

The normalized dc voltage gain of the IHMC for the voltage buck control and the FBI–FBR configuration presented in [25] equals

$$G = B\,(\,0.25 - A) + \sqrt{B^2(\,A - 0.25)^2 + 2\,AB}. \tag{4}$$

There are two parameters used to simplify it

$$A = C_r R f_{\rm SW} \tag{5}$$

$$B = 1 - \cos(\omega_r D T_{\rm SW}) \tag{6}$$

where R is the equivalent resistance of the load, $T_{\rm SW}$ is the switching period, $f_{\rm SW}$ is the switching frequency, and D is the control duty cycle, either buck or boost. In addition, an equation for the duty cycle can be defined as follows:

$$D_{\rm bk} = \frac{1}{\omega_r \cdot T_{\rm SW}} \arccos\left(1 - \frac{G^2}{2 \cdot A - G \cdot (A - 0.25)}\right). \tag{7}$$

The equations of the voltage gain and the duty cycle are based on the assumption of lossless components of the converter.

In the case of the buck FBI–HBR mode, an equation for the gain was presented in [23] in the following form:

$$G = \frac{1}{2}\left(B\,(\,1 - A) + \sqrt{B^2(\,A - 1)^2 + 8\,AB}\right). \tag{8}$$

The duty cycle presented in [23] can be rewritten as follows:

$$D_{\rm bk} = \frac{1}{\omega_r \cdot T_{\rm SW}} \arccos\left(1 - \frac{G^2}{2 \cdot A - G \cdot (A - 1)}\right). \tag{9}$$

The APWM is applied to control the voltage buck gain in the HBI–FBR configuration. In this mode, switch S_3 is turned OFF, and switch S_4 is turned ON continuously. The control signals of switches S_1 and S_2 are complementary, separated by the dead-times, and asymmetrical [see Fig. 4(a)]. The control signal of switch S_1 equals the duty cycle $D_{\rm bk}$. The condition time of switch S_2 is decreased, as in previous modes, and provides sufficient time for a complete sinusoidal half-wave of the resonant current. This improves the soft-switching performance of the converter. Only transistor S_1 is turned OFF at a high switching current in this mode.

The normalized dc voltage gain of the SRC for the APWM control method in the HBI–FBR configuration equals [23]

$$G = 0.5\left(B\,(\,0.5 - A) + \sqrt{(\,B\,(\,A - 1))^2 + 4\,AB}\right). \tag{10}$$

An equation for the duty cycle can be written as follows:

$$D_{\rm bk} = \frac{1}{\omega_r \cdot T_{\rm SW}} \arccos\left(1 - \frac{G^2}{A - G \cdot (A - 0.5)}\right). \tag{11}$$

B. Boost Control Modes

The phase-shift boost modulation is used in the FBI–FBR and HBI–FBR configurations [see Fig. 4(d) and (e)]. In the FBI–FBR configuration, the primary-side switches (S_1–S_4) are controlled complementarily in two diagonals. The median voltages of the blocking capacitors C_2 and C_3 equal zero. In the HBI–FBR configuration, switch S_4 is turned ON continuously, whereas the other, S_3, is turned OFF. The median voltage $V_{\rm med(C2)}$ of the input-side capacitor C_2 equals $V_{\rm LV}/2$. In both configurations, the control signals of the switches (Q_3 and Q_4) are complementary and shifted by the duty cycle $D_{\rm bt}$ relative to the control signals of the inverter switches (S_1–S_4). This modulation shorts the output side of the resonant tank and charges energy into it. The other switches (Q_1 and Q_2) operate as the synchronous rectifier. They are turned ON softly and turned OFF at a high switching current, whereas other transistors are switched at zero current.

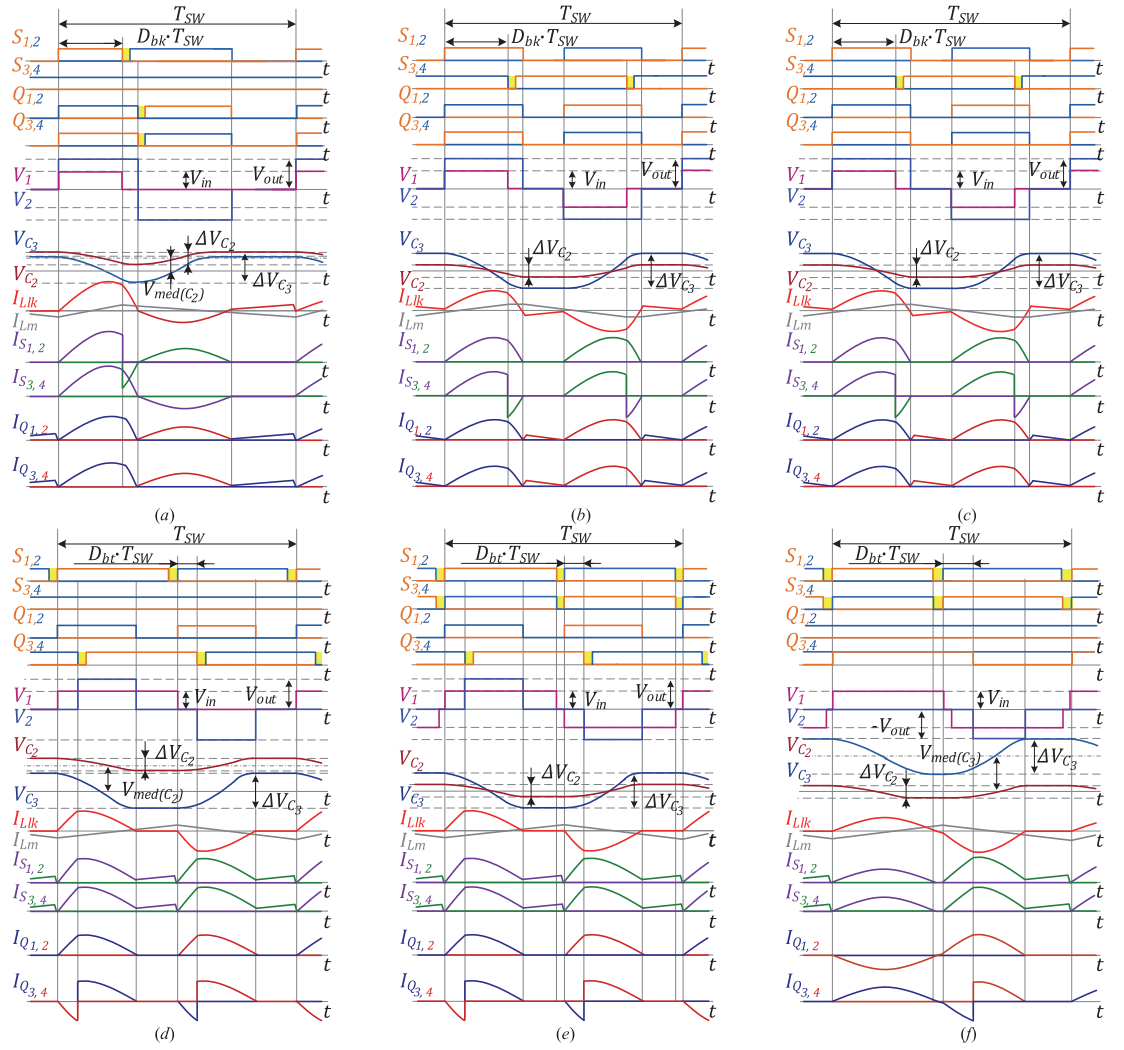

Fig. 4. IBMC operation in the buck mode for three configurations: HBI–FBR (a), FBI–FBR (b), and FBI–HBR (c). IBMC operation in the boost mode for three configurations: HBI–FBR (d), FBI–FBR (e), and FBI–HBR (f).

The gain for the boost mode and the FBI–FBR configuration presented in [25] equals

$$G = \frac{1}{2-B}\left(1+\sqrt{1+4\,A\cdot B\cdot(2-B)}\right). \tag{12}$$

From (12), the duty cycle could be obtained as follows:

$$D_{\text{bt}} = \frac{1}{\omega_r \cdot T_{\text{SW}}}\arccos\left(1-\frac{G^2-G}{0.5\cdot G^2+2\cdot A\cdot G}\right). \tag{13}$$

In the HBI–FBR configuration, the gain in the boost mode is given as follows [25]:

$$G = \frac{1}{2-B}\left(\frac{1}{2}+\sqrt{\frac{1}{4}+A\cdot B\cdot(2-B)}\right). \tag{14}$$

And the duty cycle of the boost HBI–FBR mode is given as follows:

$$D_{\text{bt}} = \frac{1}{\omega_r \cdot T_{\text{SW}}}\arccos\left(1-\frac{2G^2-G}{G^2+A\cdot G}\right). \tag{15}$$

In the case of the FBI–HBR configuration, the asymmetrical PWM voltage boost is applied for controlling the converter gain [see Fig. 4(f)]. In this mode, the output-side switch Q_1 is

TABLE I
SEQUENCE OF OPERATION MODES

$\frac{V_{HV}}{V_{LV}\cdot n}$	Modulation	
	Forward	Backward
0–0.5	Buck HBI-FBR (Fig 4a)	Boost FBI-HBR (Fig 4f)
0.5–1	Boost HBI-FBR (Fig 4d) Buck FBI-FBI (Fig 4b)	Buck FBI-HBR (Fig 4c) Boost FBI-FBR (Fig 4e)
1–2	Boost FBI-FBR (Fig 4e) Buck FBI-HBR (Fig 4c)	Buck FBI-FBR (Fig 4b) Boost HBI-FBR (Fig 4d)
2 >	Boost FBI-HBI (Fig 4f)	Buck HBI-FBR (Fig 4a)

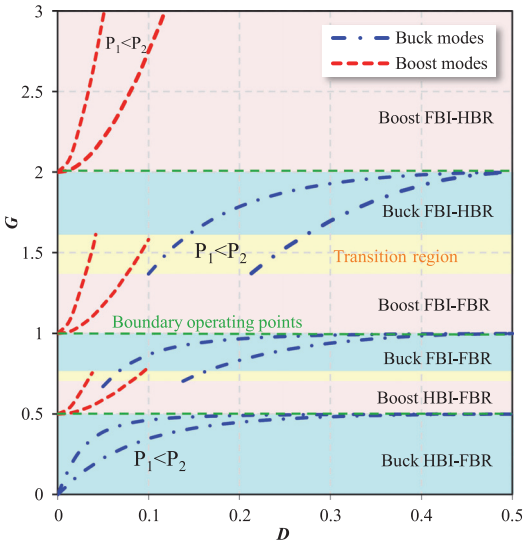

Fig. 5. Normalized voltage gain characteristics for the IHMC.

turned OFF continuously, whereas Q_2 is turned ON. The energy is charged in the resonant tank by extending the conduction time of the switch Q_4 by the duty cycle $D_{\rm bt}$. At the same time, switch Q_3 operates as the synchronous rectifier. In the first-half period, the resonant current is always sinusoidal. It should be noted that the duty cycle of switches S_1 and S_4 is decreased from 0.5 to D_p for achieving zero current switchings.

Therefore, the duty cycle of switches S_2 and S_3 equals $(1 - D_p)$. In this mode, only switch Q_4 is turned OFF at a high switching current.

For the FBI–HBR configuration, the gain in the boost mode equals [26]

$$G = \frac{1}{1-0.5B}\left(1+\sqrt{1+4\,A\cdot B\cdot(1-0.5B)}\right). \quad (16)$$

The corresponding duty cycle is given as follows [26]:

$$D_{\rm bt} = \frac{1}{\omega_r \cdot T_{\rm SW}} \arccos\left(1-\frac{G^2-2G}{0.5\cdot G^2+4\cdot A}\right). \quad (17)$$

C. Normalized Voltage Gain

Each control method can be applied in the forward power direction as well as in the backward direction. Table I shows the sequences of operation modes for both directions with respect to the voltage ratio between the high- and low-voltage ports.

The normalized voltage gain of the IHMC in any direction is plotted in Fig. 5 as the function of the generalized control duty cycle D for two values of the operating powers P_1 and P_2 using (4), (8), (10), (12), (14), and (16). Measured voltage gain characteristics will be provided in Section IV (see Fig. 15). As described above, the converter operates under six control modes. Relative to the definition of the voltage gain (2) and (3), the sequence of operation modes is the same in both directions. The gain ranges between the boost HBI–FBR and the buck FBI–FBR modes; the boost FBI–FBR and the buck FBI–HBR modes are transition regions. Points of transitions between these modes are selected based on the experimental or estimated efficiency curves.

It should be noted that the buck control methods feature a dead control zone, where the voltage gain G depends weakly on the duty cycle. This zone is nonusable for the converter control in practice, especially at a light load.

III. DESIGN AND CONTROL GUIDELINES

A. Isolation Transformer

The efficiency of the IHMC depends on the design of the isolation transformer. The first parameter of the transformer is the turns ratio n. The turns ratio is selected based on the required voltage gain range. As shown in Fig. 5, theoretically, the voltage gain range of the proposed converter can cover the range $G = 0$–3. However, for optimization of the converter's performance, the minimum duty cycle $D_{\rm bk(min)}$ in the buck HBI–FBR mode and the maximum duty cycle $D_{\rm bt(max)}$ in the boost FBI–HBR mode should be limited. The reason is that the duty cycle values close to zero in the buck mode would result in a very short conduction time of the switch S_1. At the same time, the duty cycle values close to one in the boost mode would result in very high charged energy in the resonant tank. Both cases cause a high peak and rms currents in switches and the transformer and, consequently, high switching and conduction losses in the converter. Thus, selection of the operation voltage gain range is a tradeoff between the power losses and the voltage gain range.

In summary, the turns ratio of the transformer can be calculated as follows:

$$n = \frac{V_{\rm HV(max)}}{V_{\rm LV(min)}\cdot G_{\rm max}} \quad (18)$$

where $V_{\rm HV(max)}$ is the maximum operation voltage of the high-voltage side; $V_{\rm LV(min)}$ is the minimum operation voltage of the low-voltage side; $G_{\rm max}$ is the maximum voltage gain in the boost FBI–HBR mode (16), which is calculated using $D_{\rm bt(max)}$.

The next parameter of the transformer is the flux density $B_{\rm max}$ that achieves its maximum value in the boundary operating points between the boost and the buck modes under the FBI–FBR topology in any direction. The flux density $B_{\rm max}$ in the forward and backward directions can be calculated, respectively,

as follows:

$$B_{\max(\mathrm{fw})} = \frac{V_{\mathrm{LV}}}{4 \cdot f_S \cdot A_e \cdot N_{\mathrm{pr}}} \tag{19}$$

$$B_{\max(\mathrm{bw})} = \frac{V_{\mathrm{HV}}}{4 \cdot f_S \cdot A_e \cdot N_{\mathrm{sec}}} \tag{20}$$

where A_e is the effective core area, and N_{pr} and N_{sec} are the turns numbers of the primary and secondary windings, respectively.

The following parameter is the magnetizing inductance L_m, which influences the dead-time $T_{D(\mathrm{pr}.lc)}$ between input-side switches in the boost modes directly. Moreover, the longest dead-time is required in the boost HBI–FBR mode. Therefore, the maximum value of the magnetizing inductance for the forward direction can be defined as follows:

$$L_{m(\max)} \leq \frac{T_{D(\mathrm{in}.lc)} \cdot n}{16 \cdot f_S \cdot C_{\mathrm{oss(LV)}}} \tag{21}$$

where $C_{\mathrm{oss(LV)}}$ is the parasitic output capacitance of one low-voltage switch.

In the backward direction, the maximum value of the magnetizing inductance can be calculated as follows:

$$L_{m(\max)} = \frac{T_{D(\mathrm{in.bt})}}{16 \cdot f_S \cdot C_{\mathrm{oss(HV)}}} \tag{22}$$

where $C_{\mathrm{oss(HV)}}$ is the parasitic output capacitance of the high-voltage switches.

During the dead-time, the body diodes of switches conduct the current. It increases the conduction losses of the converter due to a high forward voltage and resistance of the body diodes. On the other hand, a low magnetizing inductance is a reason for a high magnetizing current, which circulates through the primary side in the boost modes and through the secondary side in the buck modes. As a result, it increases the conducting losses in the transformer windings and MOSFETs on both sides, as well as the switching losses of the primary-side MOSFETs. Therefore, there is a balance between the minimum dead-time and power losses from the magnetizing current.

Previous analysis [9] shows that the inductance of the resonant tank L_r should be as large as possible for achieving the lowest amplitude of the resonant current and, as a result, the lowest conduction and switching losses in the converter. On the other hand, the maximum value of the leakage inductance is limited by the input voltage range and the maximum power. The maximum value can be defined in the buck FBI–HBR mode as follows:

$$L_r < \frac{V_{\mathrm{out}} \cdot f_S}{I_{\mathrm{out}} \cdot {\omega_r}^2}. \tag{23}$$

To achieve a high resonant inductance value, an external inductor is usually added in series with the isolation transformer. However, an approach used for the transformer design based on the hybrid split bobbin was described in [27]. It allows for increasing and adjusting the leakage inductance and, consequently, avoiding an external inductor.

Finally, it is important to consider the winding resistance in the design of the transformer. Since the spectrum of the resonance current in each mode includes a set of odd harmonics, the wires of windings should have low resistance at harmonics up to 11 and reduce the skin and proximity effects. The best solution is to use the Litz wires with the lowest diameter strands (0.04 mm in the given case).

B. Series Blocking Capacitors

Considering the ac voltage across the blocking/resonant capacitors, only a few types of capacitors can be selected for operation in the resonant tank. In practice, low-voltage high-current capacitors, such as ceramic capacitors, have a high deviation of capacitance due to changing applied voltage and operating temperature. At the same time, film capacitors can operate with high voltage and have a low deviation of capacitance but feature low capacitance density per volume. According to these aspects, the resonant frequency can be adjusted by the high-voltage film capacitors C_3. The capacitance of the low-voltage ceramic capacitors C_2 should be much more than C_3 ($C_2 >> C_3$) to avoid deviation of the resonant frequency.

The value of the capacitor C_3 can be calculated as follows:

$$C_3 \approx \frac{1}{L_{\mathrm{lk}} {\omega_r}^2}. \tag{24}$$

The maximum operating voltage of the capacitor C_3 is achieved in the forward buck FBI–HBR mode at a low duty cycle and can be defined as follows:

$$V_{C3(\max)} = \frac{V_{\mathrm{HV}} + \Delta V_{C3}}{2} \tag{25}$$

where ΔV_{C3} is the peak-to-peak voltage ripple of the capacitor C_3

$$\Delta V_{C3} = \frac{I_{\mathrm{out}}}{C_3 \cdot f_S}. \tag{26}$$

In the forward boost HBI–FBR mode, the low-voltage capacitor C_2 is under maximum voltage stress that equals

$$V_{C2(\max)} = \frac{V_{\mathrm{LV}} + \Delta V_{C2}}{2} \tag{27}$$

where ΔV_{C2} is the peak-to-peak voltage ripple of the capacitor C_2

$$\Delta V_{C2} = \frac{I_{\mathrm{in}}}{C_2 \cdot f_S \cdot n}. \tag{28}$$

C. Semiconductors

Typically, the transistors are selected based on the maximum voltage and current stresses. The maximum voltage of the low-voltage side transistors equals V_{LV}, and the maximum voltage of the high-voltage side transistors equals V_{HV}. At the current stress, switches provide different peaks and rms currents in different operation modes and power flow directions. The highest current stress of the low-voltage and high-voltage side transistors is achieved in the buck FBI–HBR mode in the backward and forward directions, respectively. Expressions for the calculation of the peak and rms currents in the buck FBI–HBR mode are derived in Appendix A.

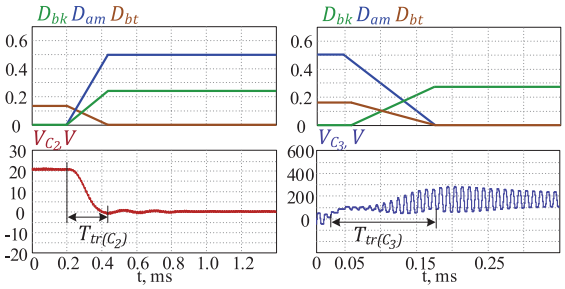

Fig. 6. Simulated soft transition (a) between HBI–FBR and FBI–FBR and (b) between FBI–FBR and FBI–HBR.

D. Converter Control

Several aspects should be taken into account in the design of a control system for the IHMC. One of the aspects is the dead-time $T_{D(hc)}$ between control signals of switches, which operate with a high switching current. The dead-time is dependent on the output capacitance, operation voltage, and current of transistors. The maximum dead-time is required at a low operating power. For the low-voltage side transistors, the minimum dead-time can be calculated as follows:

$$T_{D(\text{in}.lc)} \geq \frac{2 \cdot C_{\text{oss(LV)}} \cdot V_{\text{LV(max)}}}{I_{Llk_m(\text{min})} \cdot n} \tag{29}$$

where $I_{Llk_m(\text{min})}$ is a minimum switching current.

For the high-voltage side transistors, the minimum dead-time equals

$$T_{D(\text{in}.lc)} \geq \frac{2 \cdot C_{\text{oss(HV)}} \cdot V_{HV(\text{max})}}{I_{Llk(\text{min})}}. \tag{30}$$

The second aspect is transitions between the configurations of the topology. The series blocking capacitors feature different dc voltage stresses in different configurations. For example, for the HBI–FBR configuration, the median voltage $V_{\text{med(C2)}}$ of the input-side capacitor C_2 equals $V_{\text{LV}}/2$, but in the FBI–FBR, $V_{\text{med(C2)}}$ equals zero. It means that the capacitor must be recharged during a transition between two topology configurations. This causes high current stress in the circuit, and consequently, the power semiconductor devices can be destroyed. However, the algorithm for soft transitions between different control modes and topology configurations has been proposed in [25]. The main idea of the soft transition algorithm is in the linear increase or decrease in the duty cycles of switches S_3, S_4 or Q_1, Q_2 due to their static operation in one of the adjacent modes during the transition, as shown in Fig. 6. Fig. 7(a) and (b) shows the control signals of switches during the soft transition between HBI and FBI and between FBR and HBR, respectively. The duty cycle of the next operation mode is calculated based on the feed-forward control using (7), (9), (13), and (15). As shown in [25], voltage points for transition between control modes have to be selected based on the efficiency curves of each mode. To avoid voltage oscillation at the transition points, it is necessary to apply hysteresis in the transition algorithm.

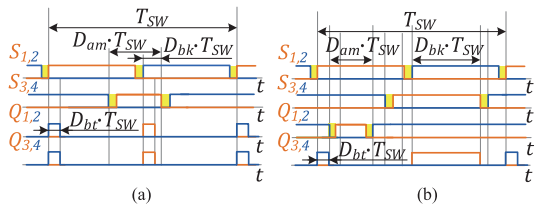

Fig. 7. Control signals of switches during the soft transition (a) between HBI and FBI and (b) between FBR and HBR.

This algorithm provides recharging of the blocking/resonant capacitors and allows for avoiding oscillations and high peaks in the currents of the converter and maintaining the input voltage at a regulated level during the transition time, which can be calculated for the transition between the FBI and the HBI as

$$T_{\text{tr}(C2)} \geq 2 \cdot \pi \cdot \frac{\sqrt{L_m \cdot C_2}}{n} \tag{31}$$

and for the transition between the FBR and the HBR, the transition time is defined as follows:

$$T_{\text{tr}(C3)} \geq 2 \cdot \pi \cdot \sqrt{L_{\text{lk}} \cdot C_3}. \tag{32}$$

A special algorithm is not required for the transition between buck and boost modes within one topology configuration, e.g., between the buck FBI–FBR and the boost FBI–FBR modes because the converter crosses the boundary operating point smoothly. The reason is that at these points, the duty cycle of buck modes of 0.5 and the duty cycle of boost modes of 0 are technically the same operating point.

Implementation of the synchronous rectifier is the third aspect of the IHMC control system. A simple approach for the realization of the synchronous rectifier control circuit is based on the measurement of current transformers and comparators, as shown in Fig. 8. Some microcontrollers, such as STM32, have internal comparators connected with PWM timers. It allows for the implementation of a compact control circuit. The comparators detect a low level of the falling resonant current and send a signal to timers for turning OFF rectifier switches.

Since the IHMC operates in two directions and the magnetizing current can circulate through the low-voltage or the high-voltage side, two control circuits on low- and high-voltage sides are used in the control system of the synchronous rectifier to neutralize the effects of the magnetizing current. It allows for correct detection of an instant when the switches should be turned OFF. Thus, the current transformer on the high-voltage side and comparators COMP3 and COMP4 are responsible for operation in the forward mode, and the current transformer on the low-voltage side and comparators COMP1 and COMP2 are responsible for operation in the backward mode. Fig. 9 presents an example of the control signal generation in the buck FBI–FBR and the boost FBI–FBR modes in the forward direction based on microcontroller timers. Based on this example, other modes in both directions can be realized. This control circuit is also used for controlling the primary switches in the buck mode. The current transformer measuring the secondary winding current should have reinforced isolation.

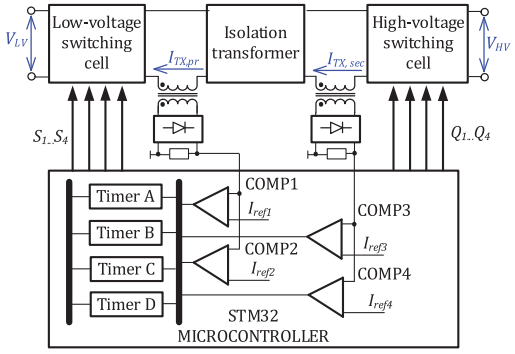

Fig. 8. Control circuit of the synchronous rectifier.

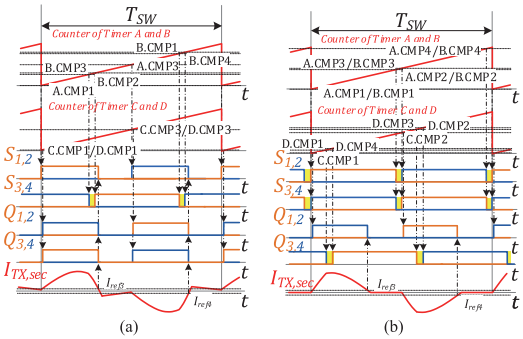

Fig. 9. Generalized principle of the control signal generation in the (a) buck FBI–FBR and (b) boost FBI–FBR modes in the forward power direction.

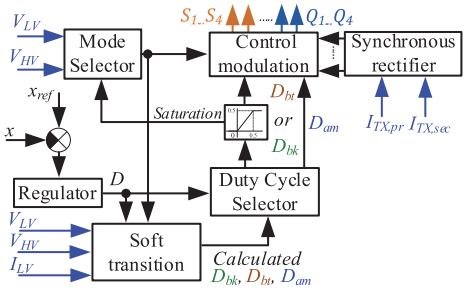

Fig. 10. Block diagram of a closed-loop control system.

In summary, the example of a closed-loop control system for the regulation of some variable x is shown in Fig. 10. The mode selector chooses a control mode automatically; therefore, the duty cycles D_{bk} and D_{bt} are based on an operation voltage gain. At the same time, when the system achieves one of the thresholds for the soft transition between the boost HBI–FBR and the buck FBI–FBR or the boost FBI–FBR and the buck FBI–FBH, the control system switches to the soft transition algorithm during the required time and operates with calculated duty cycles D_{bk}, D_{bt}, and D_{am}. This example of the control system can be used in both power directions.

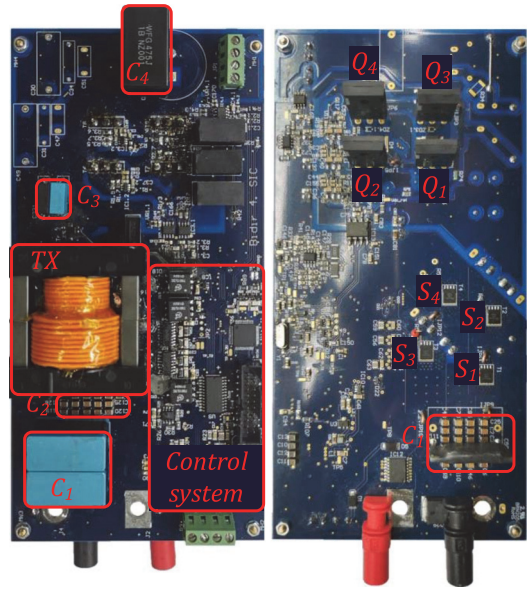

Fig. 11. Prototype of the IHMC.

TABLE II
PROTOTYPE PARAMETERS AND COMPONENTS

Operating parameters	
Low voltage, V_{LV}	10…60 V
Maximum low-voltage current, I_{LV}	12 A
High voltage, V_{HV}	350 V
Switching frequency, f_{SW}	100 kHz
Operating power range	20…350 W
Components	
$S_1...S_4$	On Semiconductor FDMS86180
$Q_1...Q_4$	LittleFuse LSIC1MO120E0080
C_1	150 µF
C_2	52 µF
C_3	25 nF
C_4	5.2 µF
L_{lk}	115 µH
L_m	1.95 mH
n	13.5

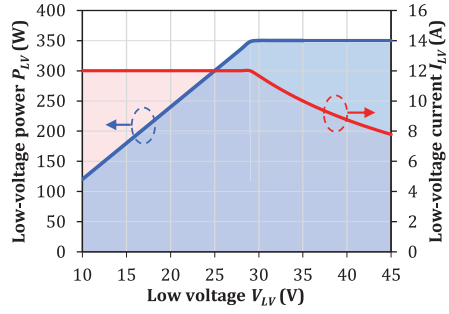

Fig. 12. Case study safe operation area for the designed IHMC prototype.

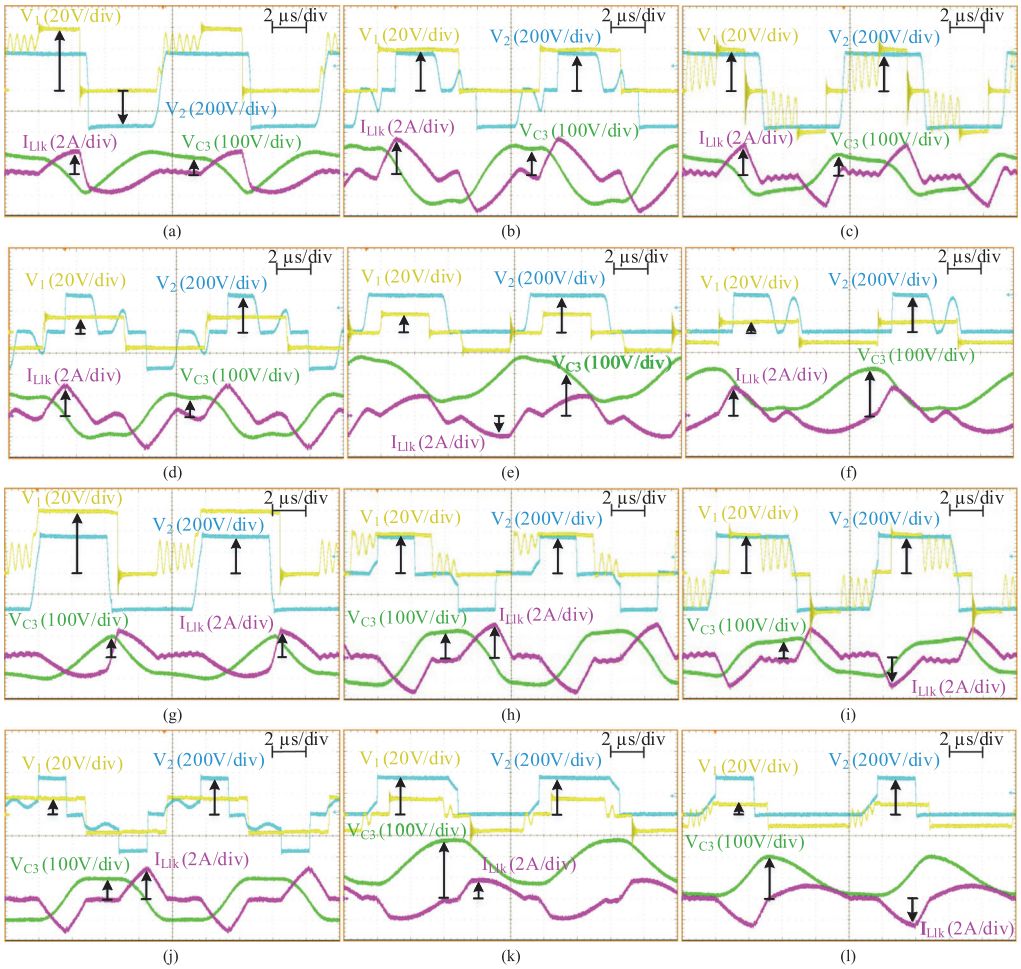

Fig. 13. Experimental steady-state waveforms of the IHMC operating in the forward mode at $V_{LV} = 60$ V and $P_{LV} = 350$ W for the buck HBI–FBR (a), at $V_{LV} = 40$ V and $P_{LV} = 350$ W for the boost HBI–FBR (b) and the buck FBI–FBR (c), at $V_{LV} = 17$ V and $P_{LV} = 205$ W for the boost FBI–FBR (d) and the buck FBI–HBR (e), and at $V_{LV} = 10$ V and $P_{LV} = 120$ W for the boost FBI–HBR (f); in the backward mode at $V_{LV} = 60$ V and $P_{LV} = 350$ W for the boost FBI–HBR (g), at $V_{LV} = 40$ V and $P_{LV} = 350$ W for the buck FBI–HBR (h) and the boost FBI–FBR (i), at $V_{LV} = 17$ V and $P_{LV} = 205$ W for the buck FBI–FBR (j) and the boost HBI–FBR (k), and at $V_{LV} = 10$ V and $P_{LV} = 120$ W for the buck HBI–FBR (l).

IV. Experimental Results

A prototype of the IHMC shown in Fig. 11 was built to validate the converter's performance in a wide voltage gain range in both power flow directions. Table II lists the main components used in the prototype. The isolation transformer was designed based on the hybrid split bobbin [27] that eliminates the need for an external inductor. It should be noted that electrolytic capacitors are not used in the prototype according to the requirements of parallel PV power optimizer applications. The following measurement equipment was used: oscilloscope Tektronix DPO7254, differential voltage probes Tektronix P5205A, current sensors Tektronix TCP0030A and PEM ultra-mini CWT015, precision power analyzer Yokogawa WT1800, and thermal camera Fluke Ti25.

The prototype was designed for operation in the safe operating area (SOA) shown in Fig. 12. The SOA covers the operation ranges of typical market-leading PV module types (60- and 72-cell silicone PV modules) and batteries (12 V, 24 V, and 48 V).

A. Steady-State Waveforms

Fig. 13 shows measured steady-state waveforms of the output voltage of the low-voltage (yellow) and high-voltage (blue) switching cells, the voltage of the high-voltage side resonant

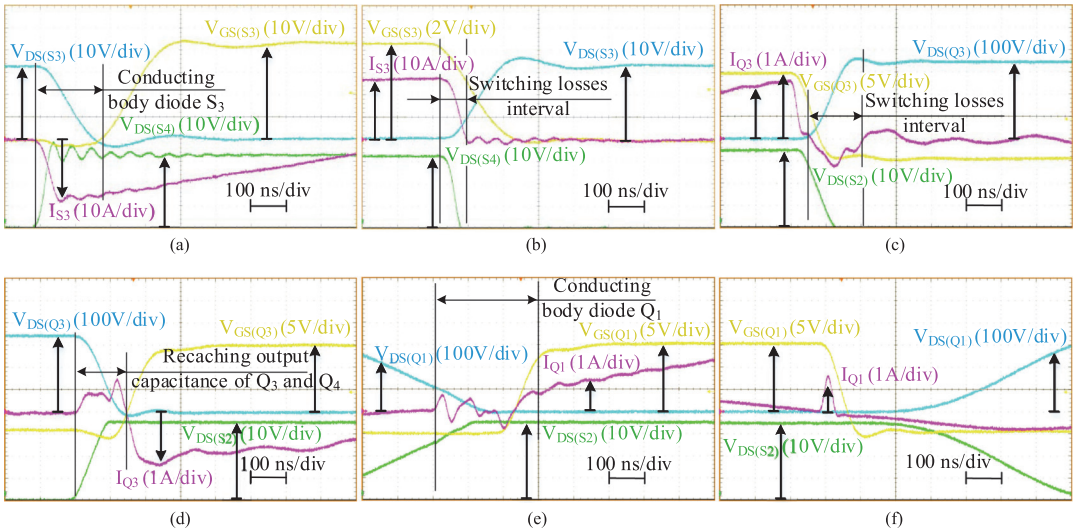

Fig. 14. Experimental switching-ON (a) and -OFF (b) waveforms of transistor S_3 at $V_{LV} = 35$ V and $P_{LV} = 250$ W under the buck FBI–FBR, switching-ON (c) and -OFF (d) waveforms of transistor Q_3, and switching-ON (e) and -OFF (f) waveforms of transistor Q_1 at $V_{LV} = 20$ V and $P_{LV} = 200$ W under the boost FBI–FBR in the forward mode.

capacitor C_3 (green), and the current of the high-voltage side transformer current (magenta) of the IHMC operating in the boundary points of each control mode. In all buck modes, the transformer current and voltage of switching cells have a parasitic oscillation between the output capacitances of the inverter transistors and the leakage inductance in the zero states. Also, boost modes feature parasitic oscillations between the output capacitances of the rectifier transistors and the leakage inductance.

In the waveforms of the transformer current, the magnetizing current circulates through the high-voltage side in the buck mode for the forward power flow and the boost mode for the backward power flow. Therefore, in other modes, the leakage inductance current circulates through the low-voltage side. The leakage inductance produces additional power losses in the convert sides; however, it allows for recharging output capacitances of transistors and achieving soft switching.

B. Varification of Soft-Switching Operation

Fig. 14 shows zoomed experimental switching-ON and -OFF waveforms of the transistor S_3 in the buck FBI–FBR mode and transistors Q_1 and Q_3 in the boost FBI–FBR mode, all in the forward mode. These are the most critical switching cases. As described above, two primary transistors S_3 and S_4 and two secondary transistors Q_3 and Q_4 are turned OFF at high switching current. The waveforms of the transistors S_3 and Q_3 show that the output capacitance of transistors in a leg is recharged by a high switching current after switching OFF one of the transistors. After that, a body diode of the next transistor conducts the current during the dead-time. Thus, the next transistor in the leg is turned ON at zero voltage.

Rectifier switches [Q_1 in Fig. 14(e) and (f)] are turned ON and OFF at zero current. During the zero-current state, output capacitances of the rectifier switches are recharged. Under the same condition, primary switches S_1 and S_2 are switched under the buck FBI–FBR and the buck FBI–HBR modes and all primary switches in the boost modes.

According to Fig. 14, it can be summarized that all transistors are turned ON at zero voltage or current. Thus, the IHMC operates without switch-ON losses, and only two transistors are switched OFF at high current.

C. Comparison of Experimental and Theoretical Control Variables

Fig. 15 shows the calculation results of the theoretical dc gain (solid lines) based on (4), (8), (10), (12), (14), and (16) in comparison with the measured gain values (markers) for all control methods in both power flow directions, while staying within the SOA. The figures show good agreement between the theoretical and experimental results for all the applied methods. Small differences between theoretical and experimental values occur outside the target regulation range and are mostly associated with the assumptions of a lossless system, neglecting the influence of the magnetizing inductance and power losses during the analysis.

D. Efficiency Evaluation

The measured efficiency of the IHMC is shown in Fig. 16 for both power flow directions, which was measured at the

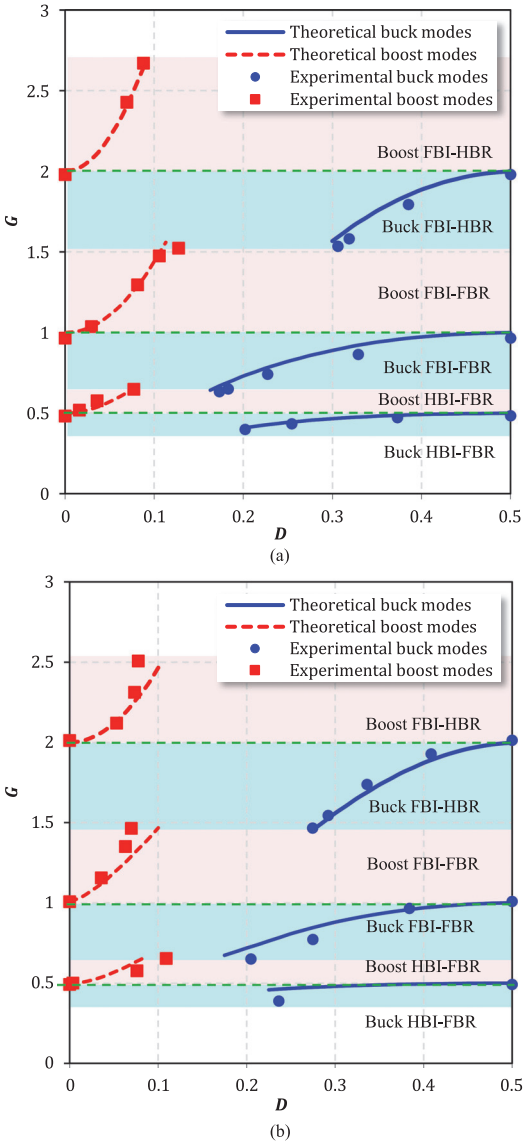

Fig. 15. Experimental and theoretical normalized voltage gain characteristics for the IHMC in the forward mode (a) and in the backward mode (b).

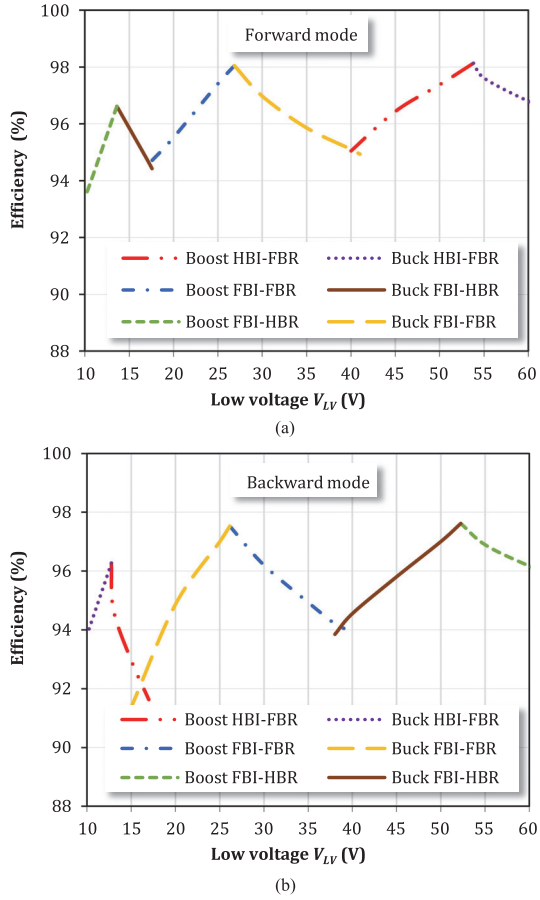

Fig. 16. Efficiency of the IHBC operating in the forward (a) and the backward (b) directions at the borders of the SOA from Fig. 12.

SOA envelope, i.e., maximum current and maximum power ranges. The converter operates with a 50% duty cycle (like a dc transformer) at $V_{\mathrm{LV}} = 13$, 26, and 52 V, where the efficiency achieves the maximum values. At this point, the transformer current is virtually sinusoidal, and as a result, all switches are soft-switched. The maximum efficiency of the IHMC is 98.1% in the forward mode and 97.6% in the backward mode at $V_{\mathrm{LV}} = 52$ V. This difference in peak efficiency results from the SOA application regarding the low-voltage side power. It means that the input power (on the high-voltage side) in the backward power flow direction is higher than the power on the low-voltage side. Another reason for the efficiency difference between power in the flow directions is the longer dead-times for the high-voltage transistors. With an increase or decrease in the input voltage from the DCX points, the converter operates in buck or boost mode, and the efficiency decreases. This is mainly associated with the increasing rms and switching currents in the converter, which results from the shortening of the active states applied to the isolation transformer. As can be seen from Fig. 16, the efficiency curves of the boost HBI–FBR and buck FBI–FBR modes are crossed at $V_{\mathrm{LV}} = 40$ V. The efficiency curves of the boost FBI–FBR and buck FBI–HBR modes are crossed at $V_{\mathrm{LV}} = 17$ V. These are the points recommended for implementing the transition between the HBI–FBR and the FBI–FBR configurations and between FBR–FBR and FBI–HBR, respectively, by using the proposed approach of the linear duty cycle ramp.

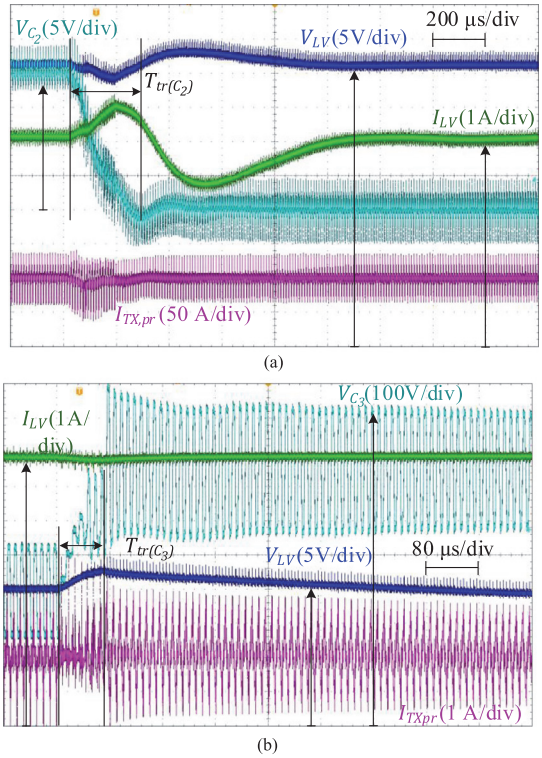

Fig. 17. Experimental waveforms of the soft transition (a) from the boost HBI–FBR to the buck FBI–FBR at $V_{\mathrm{LV}} = 40$ V and (b) from the boost FBI–FBR to the buck FBI–HBR at $V_{\mathrm{LV}} = 20$ V.

E. Verification of the Soft Mode Transitions

For verification of the described algorithm of soft transition, experimental waveforms of transitions from the boost HBI–FBR mode to the buck FBI–FBR mode and the boost FBI–FBR mode to the buck FBI–HBR mode are shown in Fig. 17. These two cases of transition between modes are the most critical due to the need of recharging capacitances in series with the transformer windings. Therefore, these cases have been selected for experimental verification. As described in Section III, other cases of transitions are automatic and smooth since the converter operates with a duty cycle of 0.5 at the boundary operation points between the buck and the boost modes, as shown in Figs. 5 and 15.

F. Thermal Analysis of the Prototype

Temperature distributions in the IHMC prototype for the forward and the backward power flow directions under the buck FBI–HBR and the boost FBI–FBR modes are shown in Fig. 18. The highest thermal stress is achieved in the forward and backward power flow directions at $V_{\mathrm{LV}} = 17$ V, $P_{\mathrm{LV}} = 205$ W and $V_{\mathrm{LV}} = 38$ V, $P_{\mathrm{LV}} = 350$ W, respectively. These modes were selected for thermal analysis as the highest stressed

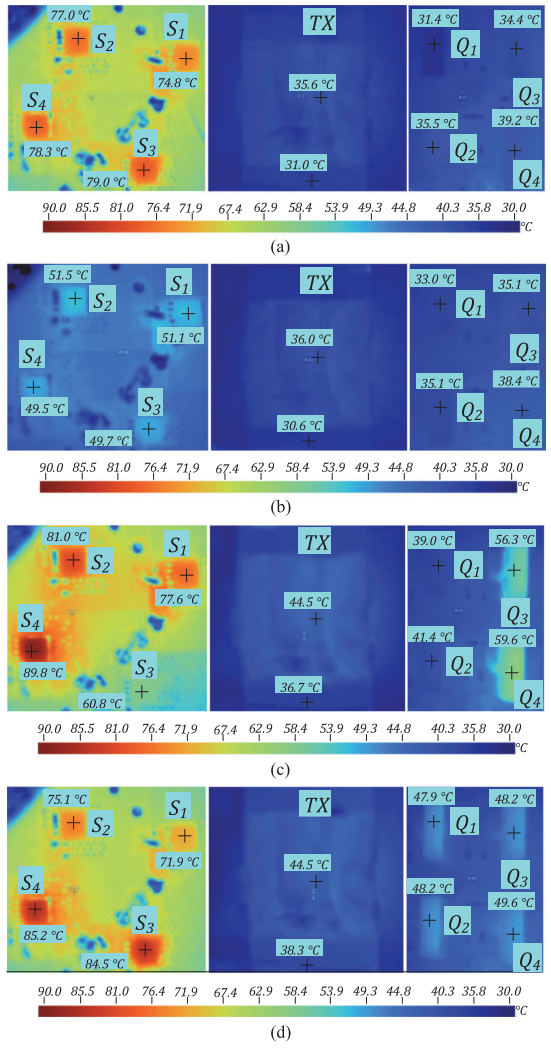

Fig. 18. Temperature distribution in the IHMC in the forward mode under the buck FBI–HBR (a) and the boost FBI–FBI (b) modes at $V_{\mathrm{LV}} = 17$ V and $P_{\mathrm{LV}} = 205$ W and in the backward mode under the buck FBI–HBR (c) and the boost FBI–FBI (d) modes at $V_{\mathrm{LV}} = 38$ V and $P_{\mathrm{LV}} = 350$ W.

modes based on theoretical analysis, which was described in the previous section. Other operating points feature lower thermal stress. The two-times higher secondary-side resonant current and the maximum power in the backward buck FBI–HBR mode are the reasons for the high temperature of the transistors and the transformer, as can be observed from the figures. In the forward buck FBI–HBR mode, the low-voltage switches also have a high temperature, but thermal stress is distributed evenly. However, the core temperature of the transformer in all modes is small because the transformer has been designed for the nominal input voltage $V_{\mathrm{LV}} = 27$ V and the maximum flux density of roughly 90 mT.

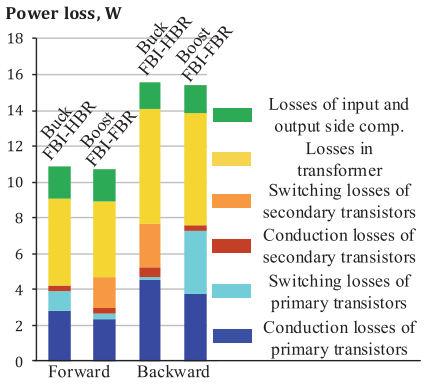

Fig. 19. Power losses in the IHMC under the forward buck FBI–HBR and boost FBI–FBR modes at $V_{\mathrm{LV}} = 17$ V and $P_{\mathrm{LV}} = 205$ W and under the backward buck FBI–HBR and boost FBI–FBR modes at $V_{\mathrm{LV}} = 38$ V and $P_{\mathrm{LV}} = 350$ W.

It follows from the analysis of thermal modes that the proposed IHMC could experience insignificant thermal cycling during the transition between topology configurations. However, these transitions are relatively infrequent (easily ensured by control) as they happen mostly during scanning a source, e.g., during global maximum power point tracking of a PV module. Thus, it could be concluded that they will not threaten the converter's lifetime; passive cooling via printed circuit board surface could be used in the proposed IHMC.

G. Distribution of Power Losses

In order to fully understand the distribution of power losses in the converter in high-stressed operating points, the methodology described in detail in [9] was applied to calculate the conduction losses of primary and secondary transistors (blue and brown), switching losses of primary and secondary transistors (light blue and orange), conduction losses of the transformer windings (yellow), and combined losses of the input- and output-side components (green) in the buck FBI–HBR and boost FBI–HBR control modes at $V_{\mathrm{LV}} = 17$ V and $P_{\mathrm{LV}} = 208$ W in the forward direction and at $V_{\mathrm{LV}} = 38$ V and $P_{\mathrm{LV}} = 350$ W in the backward direction (see Fig. 19). The calculated power loss breakdowns correlate with the experimental results and the temperature of the components in both converters. The conduction losses of the low-voltage side switches and conduction and switching losses of the high-voltage side switches are the highest in the backward buck FBI–HBR mode. The switching losses of the low-voltage side switches are the highest in the backward boost FBI–FBR mode. These observations prompt the conclusion that total losses of the converter are higher in the backward direction. Therefore, this aspect should be taken into account in the thermal design of the IHMC.

V. Conclusion

In this article, the bidirectional isolated hexamode dc–dc converter is proposed for wide gain range applications in dc microgrids. Thanks to the TMC based on the hybrid switching cells, the converter operates under six control modes in both directions. The operating principles and theoretical equations for the calculation of the dc voltage gains and the duty cycle of each mode are described. Compared to conventional two-mode buck–boost converters, the proposed converter avoids any abnormal operation by keeping the converter buck or boost factor below twofold.

A 350-W rated prototype with a low-voltage range from 10 up to 60 V and a 350 V output voltage was built to be compatible with typical residential PV modules and batteries. It was demonstrated that the converter can keep the efficiency above 94% in the forward direction by harnessing the high efficiencies of three DCX operating points. This remarkable result was achieved despite converter operation at the SOA envelope, i.e., maximum power/current. The peak efficiency of the built prototype achieved is 98.1% in the forward direction and 97.6% in the backward direction. The proposed converter achieves the high-efficiency zero-voltage switching and/or zero-current switching of the input and output side switches. It should be noted that the converter operates under a fixed switching frequency, and only one or two switches are turned OFF with high current in each of the six operating modes.

Appendix

Expressions for the calculation of switching and rms current in the converter under the buck FBI–HBR mode in any direction are derived below.

The amplitude of the resonant current during the active state can be defined as follows:

$$I_{\mathrm{lk1}} = \frac{V_{\mathrm{in}} \cdot n + \frac{V_{\mathrm{out}}}{2} - \frac{\Delta V_{Cr}}{2}}{Z_r} \tag{33}$$

where Z_r is the impedance of the resonant tank and ΔV_{Cr} is the peak-to-peak voltage ripple of the equivalent resonant capacitor C_r, which are given as follows:

$$Z_r = \sqrt{\frac{L_{\mathrm{lk}}}{C_r}} \tag{34}$$

$$\Delta V_{Cr} = \frac{I_{\mathrm{out}}}{C_r \cdot f_S} \tag{35}$$

$$C_r = \frac{C_2 \cdot C_3}{C_2 + C_3 \cdot n^2}. \tag{36}$$

The peak of the magnetizing current equals

$$I_{Lm(\max)} = \frac{V_{\mathrm{in}} \cdot n \cdot D_{\mathrm{bk}}}{2 \cdot L_m \cdot f_{\mathrm{SW}}}. \tag{37}$$

Therefore, the switching current of primary-side lagging-leg transistors can be calculated as follows:

$$I_{\mathrm{in,tr(SW)}} = n \cdot \left(I_{\mathrm{lk1}} \cdot \sin\left(D_{\mathrm{bk}} \cdot T_{\mathrm{SW}} \cdot \omega_r\right) + I_{Lm(\max)}\right). \tag{38}$$

The voltage of the equivalent resonant capacitor C_r at the end of the active state equals

$$V_{Cr(D)} = I_{\mathrm{lk1}} \cdot Z_r \cdot \cos(D_{\mathrm{bk}} \cdot T_{\mathrm{SW}} \cdot \omega_r) - V_{\mathrm{in}} \cdot n. \tag{39}$$

The amplitude of the resonant current during the falling state can be calculated as follows:

$$I_{\text{lk2}} = \sqrt{\left(I_{\text{lk1}} \cdot \sin\left(D_{\text{bk}} \cdot T_{\text{SW}} \cdot \omega_r\right)\right)^2 + \left(\frac{V_{Cr(D)}}{Z_r}\right)^2}. \quad (40)$$

Period of falling the resonant current equals

$$\Delta t_f = \frac{1}{\omega_r} \arcsin\left(\frac{I_{\text{lk1}} \cdot \sin\left(\omega_r \cdot D_{\text{bk}} \cdot T_{\text{SW}}\right)}{I_{\text{lk2}}}\right). \quad (41)$$

For simplifying the following description, three equation are taken

$$O_1 = {I_{\text{lk1}}}^2 \left(D_{\text{bk}} \cdot T_{\text{SW}} \cdot \omega_r - \cos\left(D_{\text{bk}} \cdot T_{\text{SW}} \cdot \omega_r\right) \times \sin\left(D_{\text{bk}} \cdot T_{\text{SW}} \cdot \omega_r\right)\right) \quad (42)$$

$$O_2 = {I_{\text{lk2}}}^2 \left(\cos\left(\Delta t_f \cdot \omega_r\right) \cdot \sin\left(\Delta t_f \cdot \omega_r\right) + \Delta t_f \cdot \omega_r\right) \quad (43)$$

$$O_3 = \frac{f_{\text{SW}}}{2 \cdot \omega_r}\left(O_1 + O_2\right). \quad (44)$$

The rms currents of the transformer primary and secondary windings equal

$$I_{\text{TX,pr(RMS)}} = n \cdot \sqrt{2 \cdot O_3 + 2 \cdot {I_{Lm(\max)}}^2 \cdot \left(\Delta t_f \cdot f_{\text{SW}} + \frac{D_{\text{bk}}}{3}\right)} \quad (45)$$

$$I_{\text{TX,sec(RMS)}} = \sqrt{2 \cdot O_3 + 2 \cdot {I_{Lm(\max)}}^2 \cdot \frac{\Delta t_2 \cdot f_{\text{SW}}}{3}} \quad (46)$$

where $\Delta t_2 = 1 - \Delta t_f - D_{\text{bk}} \cdot T_{\text{SW}}$.

The rms current of primary-side switches equals

$$I_{\text{in,tr(RMS)}} = n \cdot \sqrt{O_3 + {I_{Lm(\max)}}^2 \cdot \left(\Delta t_f \cdot f_{\text{SW}} + \frac{D_{\text{bk}}}{3}\right)}. \quad (47)$$

The rms current of output-side switches (Q_1 and Q_2) equals

$$I_{\text{out,tr}_{1,2}\text{(RMS)}} = \sqrt{O_3 + {I_{Lm(\max)}}^2 \cdot \frac{\Delta t_2 \cdot f_{\text{SW}}}{3}}. \quad (48)$$

The rms current of the output-side switch (Q_4) equals

$$I_{\text{out,tr}_4\text{(RMS)}} = I_{\text{TX,sec(RMS)}}. \quad (49)$$

The rms current of the output-side filter capacitor (C_4) also equals to the rms current of transformer secondary windings

$$I_{\text{out},C_4\text{(RMS)}} = I_{\text{TX,sec(RMS)}}. \quad (50)$$

The rms current of the input filter capacitor (C_1) equals

$$I_{\text{in},C_1\text{(RMS)}} = n \cdot \sqrt{\frac{f_{\text{SW}}}{\omega_r} O_1}. \quad (51)$$

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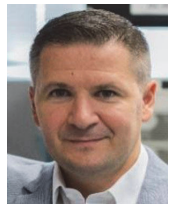

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Publication VI

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APPLIED RESEARCH

Novel Universal Power Electronic Interface for Integration of PV Modules and Battery Energy Storages in Residential DC Microgrids

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ABSTRACT This paper introduces the novel concept of a highly versatile smart power electronic interface for fast deployment of residential dc microgrids. The proposed approach has bidirectional power flow control capabilities, wide operating voltage range, and high efficiency resulting from the topology morphing control utilization. This enables universal compatibility with the majority of the commercial 60- and 72-cell photovoltaic modules, as well as the efficient charge/discharge control of the 24 V and 48 V battery energy storages using the same hardware platform. The proposed concept features fully autonomous operation where switching between the photovoltaic and battery interfacing modes is automatically done using the input source identification algorithm. Moreover, the proposed universal interface converter employs droop control and solid-state protection, making it fully compatible with the emerging standards and requirements for power electronic systems used in dc microgrid environments. A 350 W prototype was developed and tested in the residential 350 V dc microgrid with droop control to validate the proposed concept experimentally.

INDEX TERMS Microgrids, DC–DC converters, battery chargers, photovoltaic systems, universal converter.

I. INTRODUCTION

The European Commission has set the Energy Directive for at least a 55% reduction in greenhouse gas emissions and increasing renewable energy sources by 40% in buildings by 2030 [1]. Residential and commercial buildings contribute close to 40% of the total energy consumption in the European Union and U.S. [2]. One of the solutions for achieving these targets is to install photovoltaic (PV) and energy storage systems in residential buildings [3], [4], [5].

However, PV alone cannot cut carbon footprint of the building stock significantly. It should be accompanied by system-level energy efficiency optimization. Dc power distribution is the next technology step that can push the limits of possible efficiency optimization. Dc distribution minimizes losses in the residential power system and maximizes its utilization, improving the overall power supply reliability [6].

Dc houses could provide up to 15% higher efficiency in residential buildings and close to 20% in commercial buildings compared to those with ac distribution [7], [8]. Currently, a lack of standards and associated equipment impede the wider deployment of residential dc microgrids [9], while some countries, like the Netherlands, showed strong efforts in standardization [10].

New types of power electronic converters need to be developed to facilitate the deployment of residential dc microgrids. Modularity could enable new plug-and-play interface converters to be easily scalable for the needs of every customer, ensuring their low cost, simple system design, and fast deployment, as was shown for different power electronics applications [11], [12], [13], [14], [15], [16], [17], [18]. In residential applications, modular converters were shown

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for battery energy storage [12], [17], small wind turbines [14], and PV module-level power electronics [15].

Recent research proposes complementing modularity with application flexibility by extending the input-voltage regulation range [19]. As a result, the same stock-keeping units can be reused for deploying dc microgrids based on different technologies, like silicon (Si) and thin-film PV modules [27]. Extending the universal applicability concept from a single application type to several is logical. Matching PV modules with standardized battery packs in low-voltage dc microgrids (like 24 V or 48 V) is common. This inspired the proposed idea of the universal power electronic interface (UPEI) that can be universally used to integrate Si PV modules or low-voltage batteries.

The proposed concept of the UPEI is novel and provides unique features compared to the solutions on the market and in the literature. Previously presented isolated dc-dc converters have been highly specialized according to a type of input source. However, they feature virtually similar voltage ranges: dc-dc converters for single PV modules mostly operate within input voltage from 15 to 50 V [20], [21], [22], and battery converters operate from 20 to 60 V [23], [24], [25]. Recently, only one universal converter was present in the literature, capable of operating with a PV module and a battery [26]. However, the presented converter operates in the input range of 40…80 V and the output voltage between 60 V and 120 V, which does not allow connecting market-leading PV modules and batteries to the dc microgrid with the voltage bus of 350V. Furthermore, the maximum efficiency of the converter is less than 94% due to high voltage stress on the switches.

Generally, the UPEI follows the trend for universalization is evident in research and industry, especially in the recent decade. This trend could be observed in the following fields:

- universal solar converters with wide input voltage range for capability with different types of PV modules such as 60- or 72-cell Si-based, or CdTe- and CIGS-based thin-film types [27], [28], [29];
- universal electric vehicle chargers for different standards of battery packs (320, 360, 400, 450, 600, and 800 V) [30];
- rail-grade converters with wide input voltage range from 14 to 160 V and different output voltages such as 5, 12, 24, and 48 V needed to fit a wide variety of battery types used in the railway industry as defined by EN50155 standard [31], [32], [33];
- universal converters for USB Power Delivery 3.1 with different output voltages such as 5, 9, 12, 20, 28, 36, and 48 V [35].

The universality of power electronics reduces the soft cost of deployment in final systems, like those related to staff training, shipping and supply chain management, warranty claims, after-sale support, etc. For example, in residential solar systems, the soft costs correspond to 65% of the total system cost [34]. UPEI allows for simpler deployment of different PV modules or batteries in dc microgrids using a single stock-keeping unit. It is instrumental in the current state of the residential dc microgrid industry when a wide range of PV and battery products is emerging on the market. There are no solutions for the fast deployment of dc microgrids like UPEI. Hence, it is essential to validate UPEI performance in the target applications.

This paper presents an entirely novel concept of a highly versatile bidirectional power electronic interface for the fast deployment of residential dc microgrids. The proposed approach is characterized by enhanced voltage control capabilities based on the application of topology morphing control. This paper discusses the realization and experimental validation of the proposed UPEI concept. Section II focuses on the realization of the UPEI. Section III and Section IV describe the operation of the UPEI in the PV and battery interfacing modes, respectively, with selected design guidelines and experimental verifications. Further, Section V presents the input source identification algorithm allowing for the implementation of plug&play functionality. Finally, the conclusions of the paper are drawn in Section VI.

II. IMPLEMENTATION OF THE UPEI

The proposed UPEI was inspired by the bidirectional isolated hexa-mode dc-dc converter (IHMC), recently proposed by the authors in [36]. This section explains design requirements and provides a brief description of the topology and its modulation techniques used to implement the novel UPEI concept.

A. UPEI TECHNOLOGY

The converter consists of the MOSFET-based low- and high-voltage hybrid switching cells connected by a high-frequency transformer (Fig. 1). The UPEI provides buck-boost voltage regulation along with bidirectional operation capability, which significantly extends its voltage regulation range in both directions of power flow. The converter is controlled using the topology morphing control (TMC) principle [36], where the topology of both hybrid switching cells can be reconfigured on-the-fly from a full-bridge to a half-bridge and back. This allows the converter dc gain to be changed in the wide range in both directions of power flow. The capacitors C_2 and C_3 are primarily intended for blocking the dc bias when a hybrid switching cell is configured to a half-bridge. These capacitors form a series resonant tank with the leakage inductance (L_{lk}) of the transformer TX. The resonant tank is designed with a quality factor below 1 to operate under the discontinuous resonant current mode. The mathematical analysis of the IHMC was described in detail in [36].

The application of TMC is one of the distinguishing features of the proposed bidirectional UPEI. The TMC is realized on the fly by turning on one switch and turning off the other one in one leg, as shown in Fig. 2. By utilizing the TMC, the UPEI can operate with three topological configurations in both directions of power flow: full-bridge inverter (FBI) – the full-bridge rectifier (FBR), the half-bridge inverter (HBI) – FBR, and FBI – the

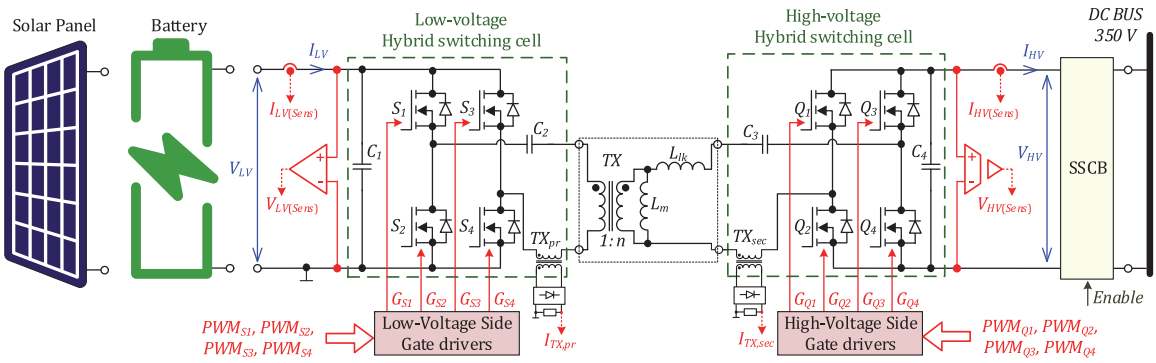

FIGURE 1. Power circuit diagram of the proposed UPEI.

half-bridge rectifier (HBR). Hence, the hybrid switching cells allow for applying six different control modulations in each power flow direction. The combination of topology configurations, operating modes, and corresponding ranges of the normalized dc gain are demonstrated in Fig. 2a.

There are two transition regions between the buck mode of one configuration and the boost mode of another one. Points of transitions are selected empirically or by estimating the converter efficiency. To avoid high current stresses during transitions, the algorithm for soft transitions and recharging series capacitors C_2 and C_3 was proposed in [40]. The main idea of the soft-transition algorithm is linearly increasing or decreasing the duty cycle of transistors in a leg. This results in the transistor being phased out from modulated to static state or vice versa to keep the input voltage and current levels at the same values.

There is no need for a special control algorithm to transition between buck and boost modes within one topology configuration, e.g., between the FBI-FBR buck and boost modes. This results from the modulations for the buck and modes providing the same switching sequence at these points. The series capacitors C_2 and C_3 neutralize any dc bias current in the transformer.

B. DESIGN AND SPECIFICATIONS OF THE PROTOTYPE

The bidirectional UPEI was designed to operate in the safe operating area (SOA) within the low voltage (LV) from 10 V to 60 V, the high voltage (HV) from 320 V to 380 V, the maximum power of 350 W, and the maximum current at the low-voltage side of ±12 A in both power directions. The SOA covers operation ranges of typical market-leading 60- and 72-cell Si PV modules and typical 24 V/48 V batteries. The bidirectional UPIE was designed for operation in droop-controlled 350 V dc microgrids deployed in the Netherlands according to the national standard [10]. Selected components and cooling conditions limit the maximum current and the maximum power of the converter.

Selecting the isolation transformer turns ratio is critical in designing a universal converter. A voltage of an input source can vary in a wide range. In addition, the global maximum power point (GMPP) of a PV module could move to a lower voltage under partial shading. Fig. 3 shows the most probable voltage operating ranges of typical 60- and 72-cells PV modules for different numbers of shaded substrings and two types of LiFePO4 batteries (24 V and 48 V) as the most used types in residential systems. In Fig. 3, boxes show the most probable operating range in residential applications, while the whiskers depict theoretically possible operating voltage. For example, typical 60-cell Si PV modules are arranged in three substrings with three bypass diodes. Without partial shading conditions, its global maximum power point would typically fall between 31 and 33 V, but it could be out of this range in very cold or hot climates.

However, if one substring is severely shaded, the global maximum power point could fall in the typical range of 20 V to 22 V. In some cases, when only one substring is not shaded, the global maximum power point could be near 10 V. Similar behavior could be observed for 72-cell Si PV modules. Moreover, batteries also have a specific operating voltage range that depends on the depth of discharge, which could be 80% to optimize the battery lifetime. All target applications could be fit in the input voltage range from 10 V to 60 V.

Thanks to the topology morphing control, the IHMC features three efficiency peaks at the normalized dc voltage gain equal to 0.5, 1, and 2. With an increase or decrease in the input voltage, efficiency would decrease because the converter operates with buck or boost control modulations, respectively. The efficiency decrease is mainly associated with the increasing RMS and switching currents in the converter. Bold green vertical lines in Fig. 3 show theoretical maximum efficiency voltages, and green gradient fields demonstrate the decreasing efficiency. This placement of maximum efficiency points considers the most probable ranges of the operating voltage and integer steps in the converter dc voltage gain.

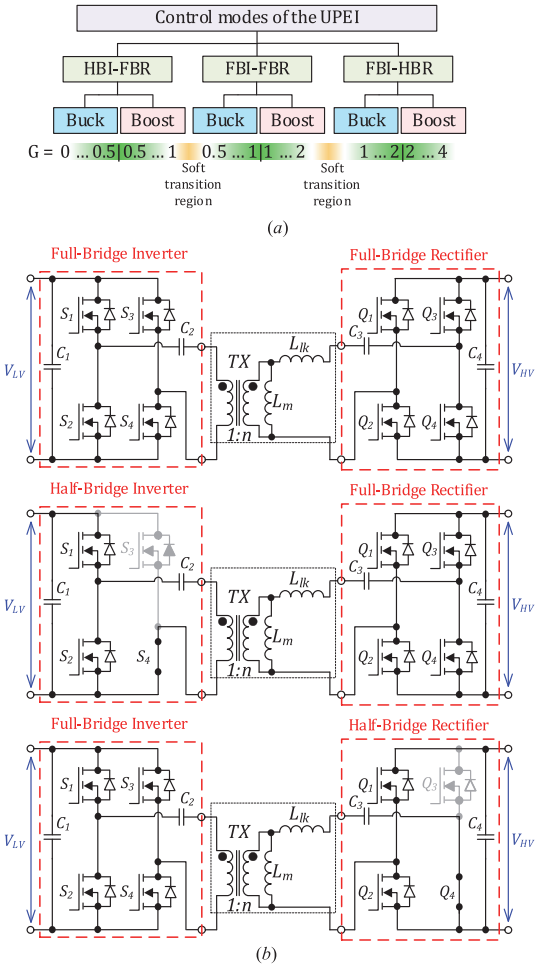

FIGURE 2. Topological configurations, operating modes, normalized voltage gains, and regions of soft transitions of the proposed UPEI (a); equivalent circuits of topology configurations (b).

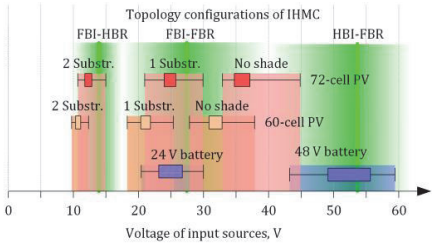

FIGURE 3. Operating voltage range of selected PV module and battery types and resulting target operating range for the UPEI.

The normalized dc voltage gain of the IHMC for the forward power flow can be defined as

$$G = \frac{V_{HV}}{V_{LV} \cdot n}, \tag{1}$$

and for the backward power flow, the voltage gain equals

$$G = \frac{V_{LV} \cdot n}{V_{HV}}. \tag{2}$$

To ensure high efficiency of the convert operating with a variable input source, the turn ratio of the transformer has been selected $n = 12.7$. This turns ratio provides high efficiency at the most probable input voltage values. A switching frequency f_{SW} of 100 kHz is selected as a compromise between component size and efficiency.

As described in [36], the forward buck FBI-HBI mode is the most critical mode for selecting resonant inductance. Previous analysis [37] shows that the inductance of the resonant tank L_{lk} should be high enough to achieve the lowest conduction and switching losses in the converter. On the other hand, the maximum value of the leakage inductance is limited by the Q-factor of the resonant tank, which should be below one for providing the discontinuous resonant current.

The maximum value can be defined in the buck FBI-HBR mode as

$$L_r < \frac{V_{out} \cdot f_S}{I_{out} \cdot \omega_r^2}. \tag{3}$$

By using Eq. (3), the loss-optimized leakage inductance equals 100 μH for operation in the required voltage and power ranges at $f_{SW} = 100$ kHz.

The magnetizing inductance L_m provides zero-voltage switching of low- and high-voltage side transistors in the forward and reverse modes, respectively, by recharging the output capacitances of switches. Therefore, the maximum value of the magnetizing inductance for the forward direction can be defined as

$$L_{m(\max)} \le \frac{T_{D(LV)} \cdot n}{16 \cdot f_S \cdot C_{oss(LV)}}, \tag{4}$$

where $C_{oss(LV)}$ is the parasitic output capacitance of a low-voltage switch, $T_{D(LV)}$ is the dead-time of the low-voltage side switches.

In the backward power direction, the maximum value of the magnetizing inductance can be calculated as

$$L_{m(\max)} = \frac{T_{D(HV)}}{16 \cdot f_S \cdot C_{oss(HV)}}, \tag{5}$$

where $C_{oss(HV)}$ is the parasitic output capacitance of the high-voltage side switches, $T_{D(HV)}$ is the dead time of high-voltage side switches.

FDMS86180 MOSFETs with $C_{oss(LV)} = 2663$ pF from On Semiconductor were selected as the low-voltage switches. For the high-voltage side, C3M0120100K MOSFETs with $C_{oss(HV)} = 48$ pF from Wolfspeed were chosen. The dead times of $T_{D(LV)} = 100$ ns and $T_{D(LV)} = 150$ ns are selected for low- and high-voltage switches, respectively, resulting in the magnetizing inductance Lm = 2 mH selected.

The flux density achieves the maximum value in the forward buck FBI-FBR at the duty cycle of 0.5. The EE64/21 ferrite planar core from 3C95 material is selected for the transformer. Considering the feasible copper cross-section

area and core losses, the maximum flux density of 90 mT was achieved, and the turns number of the low- and

high-voltage windings equals 2 and 26, respectively. The windings were designed by using a custom 3D-printed split bobbin, which eliminates an external resonant inductor.

Another critical component of the topology is the series resonant capacitors C_2 and C_3. Due to a high current circulating through the low-voltage side, ceramic capacitors were used for realizing C_2. High-voltage film capacitors are selected for C_3 and used for adjusting resonant frequency due to low capacitance variations. The capacitance of the low-voltage ceramic capacitors C_2 should be much more than $C_3 (C_2 \gg C_3)$ to avoid deviation of the resonant frequency. The value of the capacitor C_3 can be calculated as

$$C_3 \approx \frac{1}{L_{lk}\omega_r^2}. \tag{6}$$

From the calculation, the C_3 equals 25 nF and should carry the maximum voltage of 380 V. For the low-voltage side, the capacitor of 52 μH was selected, considering the maximum voltage stress of 60 V.

As was analyzed in [38], voltage ripple at any frequency influences the efficiency of PV power harvesting. For providing the maximum power reduction of 0.1%, the voltage ripple should be less than 1% of the nominal voltage at a maximum power point (MPP). At the same time, modern batteries can operate with any current or voltage ripples [39]. Therefore, the LV filter capacitor C_1 should be calculated considering PV applications. According to the requirement, the C_1 was selected at 150 μF with a maximum voltage stress of 60 V.

There is no requirement for voltage ripple in the dc microgrid due to a lack of standardization. However, it was considered to limit the voltage ripple of the HV side by 5% of the V_{HV} =350 V at the maximum power. To provide this, the capacitor C_4 of 5 μF was calculated. In practice, dc microgrid would have a substantially higher capacitance to avoid any voltage oscillations.

By using equations for the normalized voltage gains presented in [36] and Eq. (1), the curves of the low voltage as fictions of the duty cycles are plotted in Fig. 4 for two values of the operating powers $P_1 < P_2$ at $V_{HV} = 350$ V. The voltage ranges between the boost HBI-FBR and the buck FBI-FBR modes; the boost FBI-FBR and the buck FBI-HBR modes are transition regions. Points of transitions between these modes are selected based on the experimental or estimated efficiency curves.

A developed UPEI prototype embeds the power circuit, auxiliary power supply, gate drivers, sensors, protection circuitry, and microcontroller unit in a single four-layer PCB (Fig. 5). The components and parameters are listed in Table 1. The prototype was designed to operate within the maximum current of $\pm$12 A and the maximum power of 350 W, forming a safety operation limit. It should be noted that according to the strict lifetime requirements for the PV microconverters, the developed prototype employs no electrolytic capacitors. The UPEI features natural convection cooling via PCB with

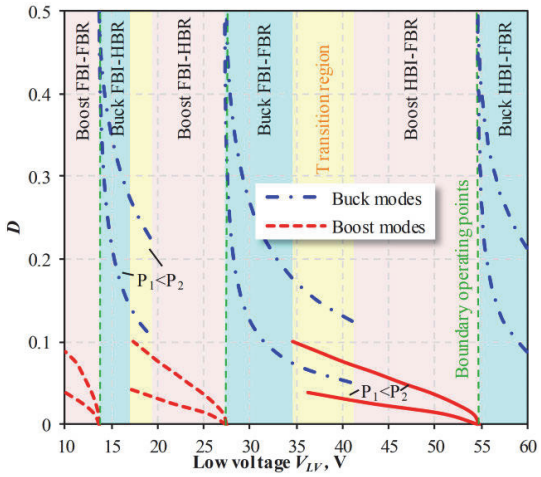

FIGURE 4. Low voltage as a function of the duty cycle.

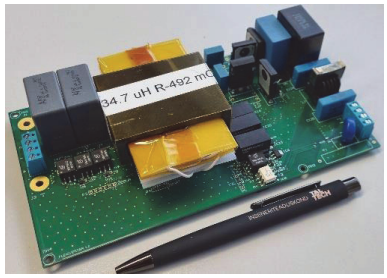

FIGURE 5. Developed 350 W prototype of the UPEI.

specially optimized thermal pads and vias used to move the heat from the parts into the core layers, thus eliminating the hotspots.

The control system of the UPEI (Fig. 6) was realized on the ST STM32G474 microcontroller unit (MCU). The control system has common ground with the low-voltage side of the converter. It allows for a low-cost non-isolated resistive divider for voltage sensing and a shunt for current sensing. The high-voltage side sensors use isolated operation amplifiers connected to the integrated 12-bit analog-to-digital converter pins of the MCU. The state machine has been used in the high-level part of the control architecture. The state machine is switched between eleven states depending on the control algorithms described in Sections III, IV, and V.

The middle level of the control architecture incorporates the following functions: Protection, Filters, Timer for PV rescanning, Synchronous rectifier, and Calculation of compare values. The last block calculates and sets required compare values for each high-resolution timer (HRTIM), implementing the control modulation for the needed direction of power flow. The synchronous rectifier block enables or disables control of rectifier switches depending on power, control

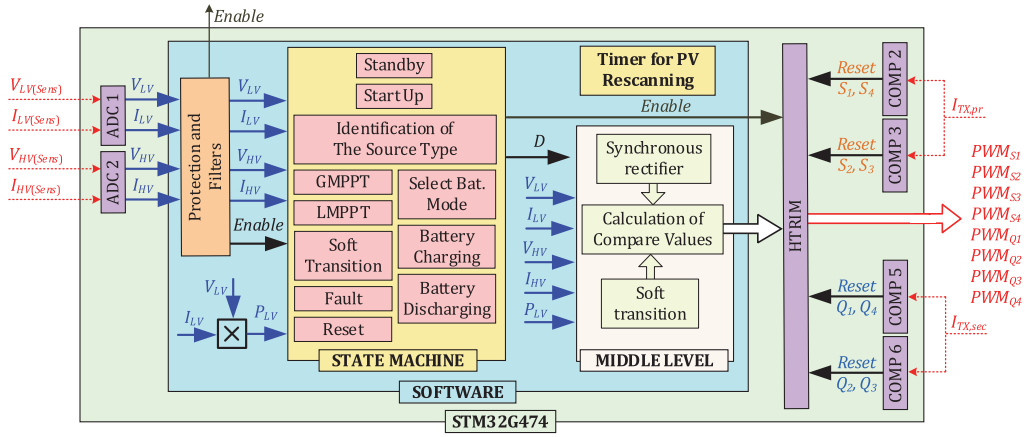

FIGURE 6. Control system of the UPEI.

TABLE 1. General specifications of the UPEI.

Operating Parameters	
V_{LV}	10…60 V
I_{LV}	±12 A
V_{HV}	320…380 V
I_{HV}	±1.1 A
f_{SW}	100 kHz
P	20…350 W
Power Components	
S_1...S_4	On Semiconductor FDMS86180
Q_1...Q_4	Wolfspeed C3M0120100K
TX	EE64/21 planar core, n = 12.8, L_{LK} = 100 µH, L_m = 2 mH
C_1	24 pcs. C1210C225K1R + 2 pcs. R60ER54705040K
C_2	24 pcs. C1210C225K1R
C_3	1pc. B32641B0153J + 1 pc. MC1206F106Z160CT
C_4	1 pc. ECWFG1B475J + 1 pc. B32653A0474J000
Driving and Measurements	
S_1...S_4 drivers	Silicon Labs SI8233BB-D-IS1R
Q_1...Q_4 drivers	Texas Instr. UCC21521ADW
Aux. power	Texas Instr. LM5010MH/NOPB
V_{LV} sensor	Resistive divider 1:20
I_{LV} sensor	Shunt 0.003Ω with OP Microchip MCP6L02T-E/SN
V_{HV} sensor	Texas Instr. AMC1200
I_{HV} sensor	Shunt 0.01Ω with Texas Instr. AMC1200

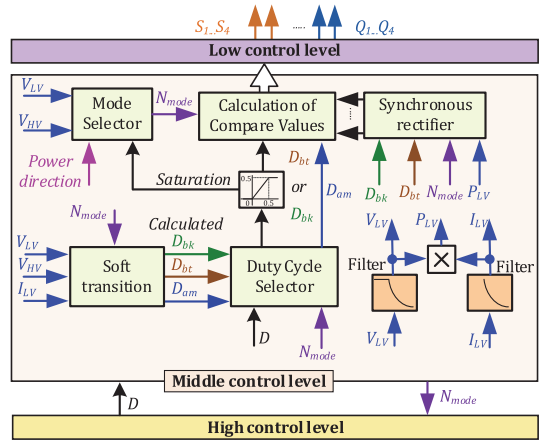

FIGURE 7. Block diagram of the middle-level control system.

modulation, and control mode. The timer for PV rescanning restarts global maximum power point tracking (GMPPT) every 30 minutes if the UPEI operates with a PV module. The software control algorithms execute only when the measured values are within the safety limits.

The SSCB provides a soft plug-in to the dc microgrid by charging the high-voltage capacitor C_4. On the low level, synchronous rectification has been implemented using current transformers and MCU internal comparators (COMPs) to improve the converter efficiency in each control mode [36]. These comparators are connected to the HRTIMs and can be selected as reset sources for output signals, providing a simple and effective solution. At low power, the control system disables the synchronous rectifier and switches from the hybrid phase shifted modulation (PSM) with synchronous rectification to the conventional PSM since the comparators cannot correctly detect the falling resonant current. A look-up table of minimum power has been generated for each control mode to define synchronous rectification limits.

To sum up described algorithms, the block diagram of the middle-level control system is presented in Fig. 7. The input control signal for the middle-level control system is a duty cycle D, which can be the duty cycles of buck modulations D_{bk} or the duty cycles of boost modulations D_{bt}. The high-level control system sets the duty cycle in the closed-loop control system. Depending on the dc voltage gain of the converter and the required power direction, the mode selector automatically chooses a control mode.

Besides, the mode selector changes a control mode when the duty cycle achieves saturation.

At the same time, when the system achieves one of the thresholds for the soft transition, the control system switches to the soft transition algorithm, and duty cycle selector applies calculated duty cycles D_{bk}, D_{bt}, and D_{am} for calculation of compare values.

Due to a lack of standardization, there are still no requirements for the control bandwidth of voltage or current regulation in dc microgrids. However, due to high capacitance, the dc microgrids feature a high voltage inertia. Therefore, fast regulation is unnecessary, and current or voltage regulators can be tuned for a low crossover frequency. The conventional PI regulator is a suitable and simple solution for controlling the voltage of a PV module as well as the current of a battery.

The parameters of the regulator should be tuned or calculated for each control mode and each type of energy source. During switching between control modes, the mode selector in the middle-level control system changes the parameters of regulators according to the control modes.

The SmartCtr tool in PSIM software is used to tune the regulator parameters. The criteria for the regulator in any control mode are a phase margin of 60 degrees and a crossover frequency of 300 Hz. These criteria provide aperiodic voltage or current step response.

C. EFFICIENCY MAPPING

To evaluate the performance of the designed UPEI in wide voltage and power range, efficiency has been measured by the precision power analyzer Yokogawa WT1800, approximated by thin-plate splines, and plotted in Fig. 8. The power of the converter is limited in the range from 20 W to 350 W, the maximum current at the low-voltage side is 12 A. The experimental analysis shows that the UPEI demonstrates efficiency above 90%, with a peak of 98.1% in both power directions. As described above, thanks to the TMC, the converter has three pronounced efficiency peaks at $V_{LV} \approx 14$, 27, 56 V when the converter operates between buck and boost mode with the lowest power losses. At low power, the synchronous rectifier does not operate, which results in efficiency reduction.

III. PV INTERFACING MODE

This section presents the control algorithm and experimental evaluation of UPEI in the PV interfacing mode.

A. MAXIMUM POER POINT TRACKING

Thanks to the ultrawide voltage gain regulation capability, the developed UPEI performs global maximum power point tracking (GMPPT) in all possible operating scenarios, including opaque shading of substrings. Among different global tracking approaches, the voltage sweep GMPPT was applied as a simple, effective, and robust algorithm that can operate with different types of PV modules [42].

The voltage sweep GMPPT is based on scanning a power-voltage curve of a PV module by decreasing the reference voltage $V_{LV(ref)}$ from the open-circuit voltage (OCV) to the minimum operation voltage V_{MIN} of the converter with

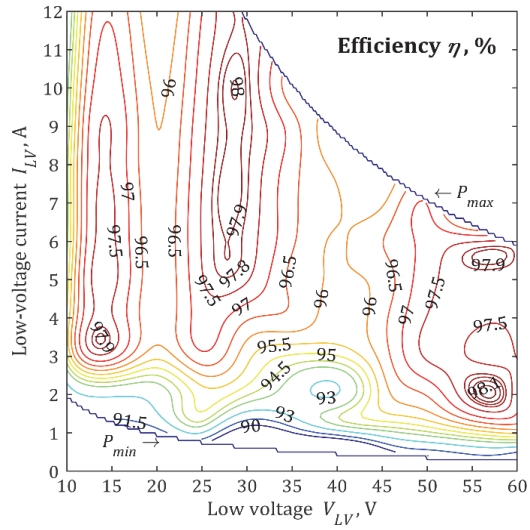

FIGURE 8. Efficiency map of the UPEI.

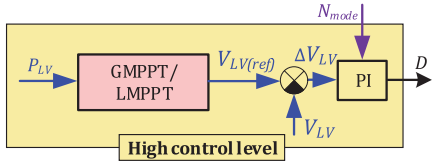

FIGURE 9. Block diagram of the high-level control system in the PV mode.

a voltage step V_{step}. After reaching the minimum operation voltage V_{MIN}, the GMMPT algorithm analyzes stored MPP data and finds the GMPP. Then the algorithm transits to the GMPP by setting the $V_{LV(ref)}$ equal to the voltage of the GMPP. After that, the control system switches to the local MPPT (LMPPT) based on the P&O algorithm.

The closed-loop control system for the GMPPT and LMPPT algorithms has been realized based on PI-regulator for controlling the PV voltage, as shown in Fig. 9. Moreover, the GMPPT and LMPPT operate only when the high voltage is in the operating range. In the PV mode, the UPEI operates as unidirectional convert and the control modulations corresponding to the reverse power flow are disabled.

B. MAXIMUM POER POINT TRACKING

To verify the UPEI performance in the PV mode, Longi LR4-60HBD-350M [48] and LR4-72HBD-425M [49] PV modules have been selected. The Solar Array Simulator (SAS) Keysight E4360A was used to emulate these PV modules. For emulating the dc microgrid iTECH IT6006C-800-25 Bi-directional Power Supply was utilized. The used measurement equipment includes an oscilloscope Tektronix DPO7254, differential voltage probes Tektronix P5205A,

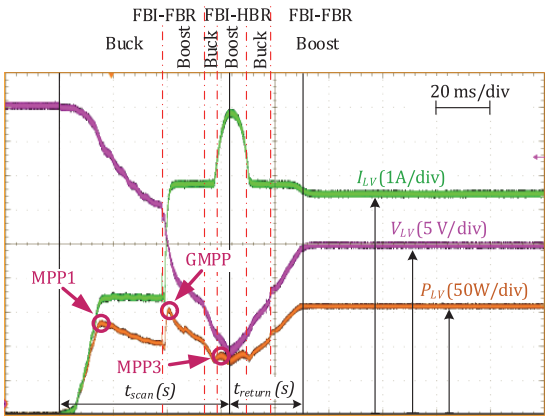

FIGURE 10. Tracking performance of the voltage sweep GMPPT algorithm with the LR4-72HBD-425M PV module operating under partial shading (irradiance of the substrings: 800 W/m^2, 600 W/m^2 and 300 W/m^2).

current probes Tektronix TCP0030A and PEM ultra-mini CWT015 Rogowski coil probe, and power analyzer Yokogawa WT1800.

The experimental result in Fig. 10 shows the performance of the voltage-sweep GMPPT algorithm with LR4-72HBD-425M PV module under a partial shading condition. The preset voltage ramp changes the reference voltage between the OCV and the minimum operating voltage. During the scanning, the middle-level control system switches through all the control modulations from the buck FBI-FBR to the boost FBI-HBR.

The soft transition algorithm allows the control system to recharge series capacitors and change topology configurations smoothly while keeping the voltage and current at the low-voltage side at the same value during the transitions. There are small oscillations in the voltage after transitions, but they do not influence GMPPT scanning since the control system is waiting for the low voltage stabilization before it continues the scanning. This experiment also verifies the continuous operation of the UPEI in the wide voltage range. After achieving the minimum voltage, the control system returns to the GMPP and switches to the LMPPT algorithm. The scanning time t_{scan} equals 62 ms, and the return time t_{return}took 23 ms, resulting in a total scanning time of 85 ms.

C. DAILY ENERGY YIELD TESTS

To verify the UPEI operation with a PV module under unfavorable conditions, a daily mission profile of solar irradiance and a module temperature under partial shading from a neighboring building were synthesized based on measurements (Fig. 11). One of the substrings in a PV module is shaded during the morning and evening hours.

Fig. 12 shows experimental results of UPEI operation with the LR72-425M PV module, under the partial shading conditions. Fig. 12 contains four parts from top to bottom:

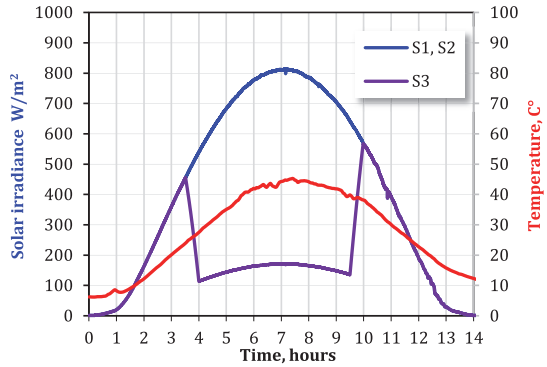

FIGURE 11. Daily profiles of solar irradiance of three PV module substrings under partial shading from a neighboring building and a cell temperature.

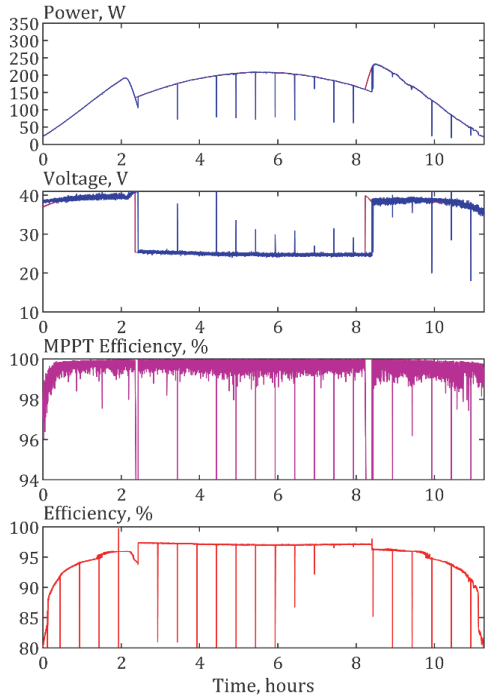

FIGURE 12. UPEI operation with LR72-425M PV module under synthesized partial shading from a neighboring building.

1) The red curve is the maximum available power from a PV module in the GMPP; the blue curve is the power drawn by the UPEI.
2) The red curve is the voltage of GMPPT, the blue curve is the instantaneous voltage of the PV module.
3) The magenta curve is the MPPT efficiency.
4) The red curve is the efficiency of the UPEI.

The UPEI tracks the GMPP with average MPPT efficiency of about 99.5 %. It could be recognized that the control

TABLE 2. UPEI operation with two PV module types under different shading conditions.

Energy and Efficiency	Profile and Type of PV module			
	NOCT		Build shade	
	60 cells	*72 cells*	*60 cells*	*72 cells*
E_{GMPP}, Wh	1355	1648	1478	1801
E_{PV}, Wh	1351	1644	1465	1788
E_{DC}, Wh	1312	1577	1403	1719
E_{PV}/E_{GMPP}, %	99.7	99.8	99.1	99.3
E_{DC}/E_{PV}, %	97.1	95.9	95.7	96.1
E_{DC}/E_{GMPP}, %	96.8	95.7	94.9	95.5

system rescans P-V curves of a PV module every 30 minutes to find the global MPP, as it was mentioned before. There are slight deviations between the maximum available power and the extracted power when the converter is stuck at the previous MPP until the next rescanning. The data were logged with a time step of 200 ms, which is less than the scanning time. In this connection, rescanning is not completely visible in the figures. At low powers, the converter efficiency has a step at the beginning and the end of the tests. It is mainly associated with enabling or disabling the synchronous rectifier by the control system.

The UPEI has been tested with SAS emulating LR60-350M and LR72-425M PV modules under partial shading and without it when the PV modules reach Nominal Operating Cell Temperature (NOCT) conditions dung the peak energy production hours. The second corresponds to the mission profile of solar irradiance of the third substring S_3 being the same as S_1 in Fig. 11.

To summarize the daily tests, the energy yield was calculated and listed in Table 2. It includes three energy values: available PV energy in the GMPP E_{GMPP}, the energy harvested by the UPEI E_{PV}, and the energy delivered EDC to the dc microgrid. In addition, MPPT efficiency E_{PV}/E_{GMPP}, the converter efficiency E_{DC}/E_{PV}, and the overall efficiency E_{DC}/E_{GMPP} are calculated. The tests show that the daily MPPT efficiency E_{PV}/E_{GMPP} is around 99.5%. The efficiency of the UPEI E_{DC}/E_{PV} during daily tests is around 96%. Considering these two efficiencies, the overall system efficiency is around 95.5 %.

IV. BATTERY INTERFACING MODE

This section presents the control algorithm and experimental evaluation of UPEI in the battery interfacing mode. It demonstrates how the droop control should be integrated at the high control level.

A. IMPLEMENTATION OF DROOP CONTROL

In the case of operation with a battery, the control system operates with the droop control algorithm when the battery

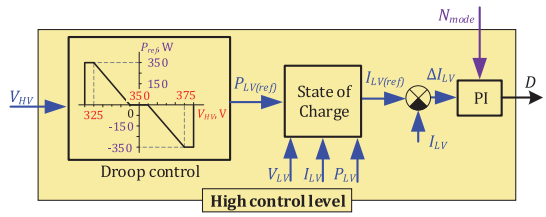

FIGURE 13. Block diagram of the high-level control system in the battery mode.

state of charge is within the allowed limits. The droop control allows for natural power sharing between parallel power sources and stabilizes the operation of the dc microgrid without any communication between converters [44].

The idea of the droop control for the battery mode is based on the derivation of the power reference value that linearly depends on the dc-bus voltage deviation from the nominal value outside the dead band of $V_{DB} = 10$ V around the nominal voltage $V_{HV(nom)} = 350$ V (Fig. 13). Based on the dc microgrid voltage (V_{HV}), the control system regulates the reference power of the converter and the power flow direction. When $V_{HV} > V_{HV(nom)}+V_{DB}/2$, the control system operates in the battery charging mode. In the case of $V_{HV} < V_{HV(nom)} - V_{DB}/2$, the control system switches to the battery discharging mode. According to the Dutch national practical guidelines NPR 9090 [10], the high voltage is limited in the range of 320 V to 380 V. In the case of PV mode, the UPEI operates with the maximum available power within the permitted range of dc-microgrid voltages between 325 V and 375 V.

The block diagram of the high-level control system under the battery mode is shown in Fig. 13. The droop control block sets the reference power. The state of charge estimation block (SOC) protects the battery from under- or over-charging.

The state of charge estimation and control algorithm implements conventional constant voltage/constant current charging [45]. In the discharge mode, the control system operates with a constant current until the battery is fully discharged. To extend the battery lifetime, the control system limits the SOC of the battery in the range of 5% to 95%.

B. OPERATION WITH DROOP CONTROL

The experimental waveforms in Fig. 14 verify the operation of the UPEI with the selected Power Brick+ 48V 25A LiFePO4 battery at a SOC of 50% under droop control at both power flows. Two iTECH IT6006C-800-25 Bidirectional Power Supplies were emulating the dc microgrid and a battery. The bidirectional power supplies have an arbitrary generator function allowing for programming dc bus voltage and software for battery emulation with realistic SOC behavior. The closed-loop control in the battery mode linearly regulates and stabilizes the battery current depending on the dc microgrid voltage.

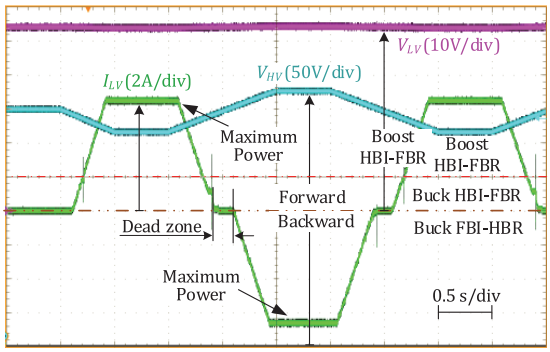

FIGURE 14. Operation of the UPEI with 48 V LiFePO4 battery with droop control.

The maximum current is limited to 6.8 A at the maximum operation power of 350 W with the battery 48 V.

At the nominal voltage of 350 V, the control system switched between the forward buck HBI-FBR and the backward buck FBI-HBR control modulations without current distortions.

C. DAILY TESTS OF UPEI WITH 24 V AND 48 V BATTERIES

To verify the UPEI operation in the battery mode, a daily profile of dc microgrid voltage was synthesized based on a daily load profile of a house and a daily profile of PV generation, as shown in Fig. 15. The power consumption profile has two recognizable maximums of 3.4 kW and 3.3 kW at 7 a.m. and 6 p.m., respectively, during breakfast and dinner hours.

To reproduce the dc microgrid operation under the droop control, the synthesized microgrid voltage is linearly proportional to the difference between consumption and generated power (the third plot in Fig. 15). Also, the dc microgrid voltage is limited in the range of 320 V to 380 V. During the night, the PV power equals zero, which results in the dc microgrid voltage below the nominal value of 350 V. With increasing generated power, this voltage increases in the morning. When the PV power falls to zero, the dc microgrid voltage drops below the nominal value.

Using the synthesized profile of dc-microgrid voltage, UPEI has been tested for 24 hours with two battery types: Power Brick+ 24V 32A LiFePO4 [47] and Power Brick+ 48V 25A LiFePO4. The test with the latter is shown in Fig. 15. The bottom four parts of the figure include the voltage mission profile of the dc microgrid (red curve), the corresponding battery current (blue curve), SOC of the battery (green curve), and the UPEI efficiency (magenta curve). Depending on the instantaneous dc microgrid voltage, the UPEI operates in the charging or discharging mode, as described in Section IV.

From midnight till morning, the UPEI transfers energy from the battery energy storage to the dc microgrid. When the dc microgrid voltage increases up to 355 V, the UPEI switches to charging batteries with PV energy. The maximum battery

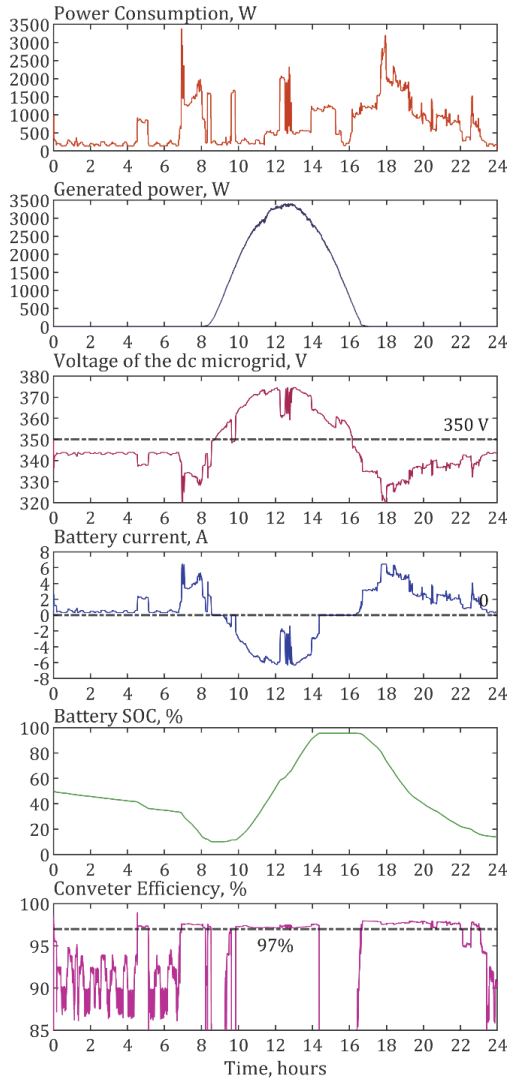

FIGURE 15. UPEI operation with Power Brick+ 48V 25A LiFePO4 battery for 24 hours.

SOC is limited by 95%. In the battery mode, the efficiency of UPEI is around 97%. However, the efficiency drops at low power when the synchronous rectifier cannot operate.

Table 3 lists calculated charged energy into batteries and transferred energy from batteries to the dc-microgrid. The full-charging efficiency (from 5% to 95% of SOC) $E_{BAT(ch)}/E_{DC(ch)}$ of the UPEI equals 96.3 % and 97.6% in the cases of 24 V battery and 48 V battery, respectively. In the discharging mode, the converter full-discharge efficiency (from 95% to 5% of SOC) $E_{DC(disch)}/E_{BAT(disch)}$ equals 97.3% and 97.5%. The round trip efficiency $E_{DC(disch)}/E_{DC(ch)}$ demonstrates how much of stored energy was returned to the

TABLE 3. UPEI 24H operation with two LFP battery types.

Operation mode	Energy and Eff.	Batteries	
		24V 32Ah	48V 25Ah
Charging (from 5% to 95%)	$E_{DC(ch)}$, Wh	-840.8	-1179.4
	$E_{BAT(ch)}$, Wh	-809.4	-1151.4
	$E_{BAT(ch)}/E_{DC(ch)}$, %	96.3	97.6
Discharging (from 95% to 5%)	$E_{BAT(disch)}$, Wh	757.4	1070.8
	$E_{DC(disch)}$, Wh	737.2	1044.0
	$E_{DC(disch)}/E_{BAT(disch)}$, %	97.3	97.5
Round trip	$E_{DC(disch)}/E_{DC(ch)}$, %	87.7	88.5

dc-microgrid and includes converter efficiencies in both modes and the losses in the battery. As Table 3 shows, the roundtrip efficiency equals 87.7% and 88.5% for 24 V and 48 V batteries, respectively.

V. SOURCE IDENTIFICATION ALGORITHM

This section introduces the algorithm of the input source type identification and provides its experimental verification.

A. ALGORITHM DESCRIPTION

As was described in the introduction, the UPEI can operate as a front-end PV microconverter or a front-end battery converter. After connecting an energy source, the converter should identify a type of connected source. The input source identification algorithm was previously proposed for the 2-mode version of the given converter [41]. This section shows how to integrate it into the UPEI and verifies its performance.

The main idea of the algorithm for the input source identification is based on scanning the I-V characteristic of a connected input source and calculating the differential conductance $\Delta I/\Delta V$. This approach allows for avoiding influences from the drift of source parameters, for example, due to aging or temperature changes. Therefore, it can be applied to different types of input sources.

The algorithm can identify input sources such as different PV modules and battery types. The main difference in I-V characteristics of these types of sources is the differential conductance $\Delta I/\Delta V$. In the case of a PV module, the differential conductance is not linear:

1) $\Delta I/\Delta V \ll 0$ from the OCV to the MPP;
2) $\Delta I/\Delta V < 0$ at the MPP;
3) $\Delta I/\Delta V \approx 0$ after the MPP.

In the case of a battery, the $\Delta I/\Delta V$ is virtually constant for one condition of the state of charge, and its absolute value is much higher than that of any PV module.

The flowchart of the identification algorithm is illustrated in Fig. 16, where ΔD is the incrementing step of the duty cycle, $I_{LV(max)}$ is the maximum current on the low-voltage side, which the UPEI can carry continuously. The identification process starts with an OCV of a connected input source.

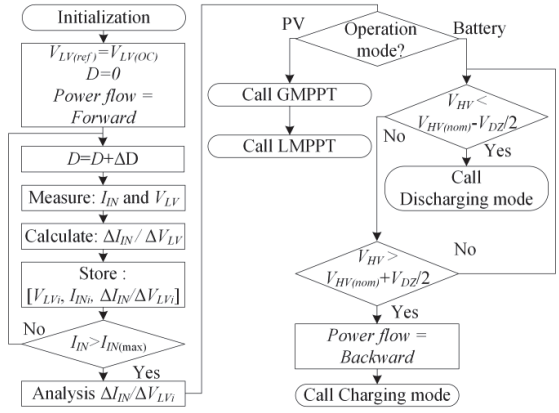

FIGURE 16. Flowchart of the identification algorithm.

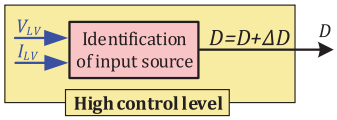

FIGURE 17. Block diagram of the high-level control system under the identification algorithm.

During identification, the control system increments the duty cycle to increase the low-voltage side current and decrease the voltage V_{LV}. After every duty cycle step, the control system calculates the input source differential conductance $\Delta I/\Delta V$.

This process continues until the current achieves the maximum $I_{LV(max)}$ value or an MPP. In the first case, the control system switches to the battery charging/discharging mode depending on the dc microgrid voltage. In the case of a connected PV module, the control system switches to the LMPPT/GMPPT algorithms. The algorithm also identifies a type of connected PV module (60-cells or 72-cells) or a battery (24 V or 48 V). Fig. 17 shows the implementation of the high-level control system. The algorithm block feds the duty cycle to the middle-level control system, which selects a control modulation automatically. The algorithm uses measured and filtered low-voltage side voltage and current for differential conductance calculations.

B. EXPERIMENTAL VERIFICATION OF THE INPUT SOURCE IDENTIFICATION

The experimental verifications of the identification algorithm with the LR4-72HBD-425M PV module and the Power Brick+ 48 V 25 A battery are shown in Figs. 10 and 18, respectively.

In the case of the PV module, the algorithm increased the duty cycle until the first MPP was found. Then, the high-level control system switched to the GMPPT algorithm and scanned the P-V curve of the PV module. After achieving the minimum voltage, the control system returned to the GMPP

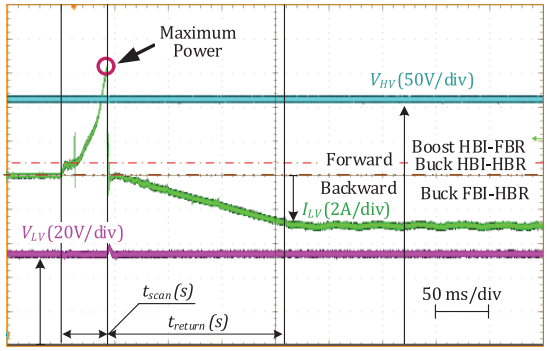

FIGURE 18. Identification of the battery and tracking performance of the discharging mode at $V_{HV} = 330$ V.

and switched to the LMPPT algorithm. The total time of PV scanning required is 85 ms.

The experimental results also verified the performance of the identification algorithm with the battery at the grid voltage V_{HV} of 330 V (Fig. 18). The control system

gradually increased the battery current I_{LV} until the maximum power was achieved. Depending on the dc microgrid voltage, the control system switches to the charging or discharging mode and sets the reference power. After identification, the control system decreases the battery current to zero as fast as possible and then switches to the backward buck HBI-FBR control mode to charge the battery, as shown in Fig18. The SOC block limits the slope of the reference current for correctly estimating the SOC of the battery. The scanning time took 48 ms, and the return time equals 154 ms.

VI. CONCLUSION

This paper demonstrates and provides experimental validation of the novel universal power electronic bidirectional interface for integration of PV modules and battery energy storages in residential dc microgrids. The analysis of application requirements shows that the proposed UPEI should have an input voltage range of 10 V to 60 V, bidirectional power flow capability, and be capable of operating with 350 ± 30 V residential droop-controlled dc microgrids. A technology demonstrator has been developed to validate the proposed concept and show its operation with various PV modules and battery energy storage types in residential dc microgrids.

Using the same hardware platform for different PV modules and storage batteries allows for simpler system design and faster deployment of dc microgrids. The UPEI concept is enabled by applying the topology morphing control in multimode dc-dc converters. The proposed UPEI operates in the wide input voltage range, which covers the voltage ranges of the most popular PV modules and storage batteries on the market. The wide input voltage range and the developed control algorithms allow the UPEI to recognize a connected energy source automatically and switch to a respective mode during 200 ms.

Daily tests with 60- and 72-cell PV modules under normal and partial shading conditions verified the high performance of the UPEI in both sunny and partially shaded conditions. The overall daily efficiency, including the MPPT and the converter efficiencies, is in the range of 94.9 – 96.8 %, depending on the operating conditions. The UPEI executes the GMPPT scanning in less than 100 ms.

The same prototype was used for the integration of battery energy storages. Its daily efficiency with 24 V and 48 V LiFePO4 batteries equals 96.3% and 97.6%, respectively, in the charging mode, and 97.3% and 97.5% in the discharging mode.

These results justify the high performance of the novel UPEI concept. It can be used to integrate either PV modules or batteries in residential dc microgrids thanks to its bidirectional power flow and input source identification capabilities. Applicability of this concept is limited to low-voltage PV modules and batteries operating at voltages below 60 V, which does not cover some residential thin-film PV modules and high-voltage battery energy storages. Nonetheless, the UPEI operates with the most commercially available residential PV modules and batteries. Further work will focus on efficiency optimization at a light load, economic viability analysis, and performance verification of the multiple UPEIs operating in one dc microgrid.

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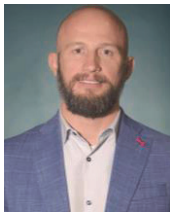

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Publication VII

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Input Source Identification Algorithm For Isolated Buck-Boost DC-DC Converter

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***Abstract*—The paper focuses on the galvanically isolated series-resonant dc-dc converter (SRC) operating at low values of the quality factor of the resonant tank. This topology is considered a bidirectional step-up front-end dc-dc converter with buck-boost functionality for integrating renewable energy sources or battery energy storage in dc microgrids. The main aim of the study is to develop a universal dc-dc converter, which can operate with different input voltage sources such as PV modules or batteries. The paper presents an input source identification method capable of distinguishing between a PV module or a battery energy storage connected to the input. The developed algorithm is based on the I-V curve scanning of an input source. Experimental results show the effectiveness of the developed algorithm in the identification of a PV module under different partial shading conditions and a battery with subsequent charging or discharging.**

Keywords—DC-DC convertor, dc microgrid, SRC, identification, PV module, storage battery.

I. Introduction

Residential power distribution systems are becoming increasingly popular. Such a distribution system could be realized based on an ac microgrid or dc microgrid [1]. Dc microgrid avoids double energy transformation from dc to ac and then from ac to dc between energy source(s) or storage and loads compared with ac microgrids. Nowadays, many consumer electronic devices and home appliances in buildings are inherently dc or feature an intermediate dc bus, such as chargers for phones or laptops, TVs, LED lighting, etc. As a result, dc microgrids could improve the overall efficiency of residential power systems by more than 11% compared to ac microgrids [1], [2].

On the other hand, dc microgrids require a front-end step-up dc-dc converter for interfacing various low-voltage dc sources or battery energy storage into a centralized dc bus. This study targets the bus voltage of 350 V due to its use in residential dc microgrids in the EU. These dc-dc converters should provide a wide input voltage range, galvanic isolation, high efficiency, maximum power point tracking for each energy source, and high-power density. At the same time, converters should be bidirectional for operation with a battery. The main idea of this study is to develop a universal front-end dc-dc converter (UFEC) for operation with a single PV module or a single storage battery.

To meet these requirements, a bidirectional isolated buck-boost converter (IBBC) based on a series resonant dc-dc converter (SRC) with a quality factor of the resonant tank below one and fixed switching frequency could be used as a front-end converter (Fig. 1) [3]. Combining buck and boost control methods in the converter extends the input voltage regulation range.

For operation with a PV module, the UFEC should apply algorithms of the global and local maximum power point tracking (GMMPT and LMPPT) to harvest maximum energy from a PV module [4]. At the same time, the UFEC should apply the droop control for operating in parallel with other sources and devices to share energy in an autonomous dc microgrid [5]. This algorithm gained popularity for enabling sharing of energy between parallel converters without communication between them by the regulation output power of each converter depending on the dc bus voltage.

Moreover, the developed UFEC should identify a connected input voltage source such as a PV module or a battery. This feature allows to simplify the use of the converter for consumers and avoid any mistakes in the commutation of input sources in a dc microgrid. This study aims to develop an algorithm for identifying an input source type connected to the IBBC based on SRC.

II. Description of Isolated Buck-Boost Converter

A. Topology

The topology of the proposed IBBC SRC-based is shown in Fig. 1. The converter consists of a switching cell based on MOSFETs on the low-voltage side full-bridge, the voltage doubler rectifier (VDR) based on MOSFETs on the high-voltage side full-bridge, and the series resonant tank formed by the blocking capacitor C_2 and the leakage inductance L_{lk} of the isolation transformer *TX* [3]. Using the active VDR as a rectifier for low-power and high-voltage converters halves the number of secondary winding turns. Furthermore, as a result, it positively influences the size and the cost of the transformer. At the same time, the active rectifier can be utilized for boost modulations.

The given converter topology operates at a constant switching frequency in the discontinuous resonant current mode (DrCM), i. e., with the resonant tank quality factor below one. Hence, the switching frequency should be 5-10% lower than the resonant frequency to implement sufficient dead-time needed for soft-switching employing the transformer magnetizing current [6].

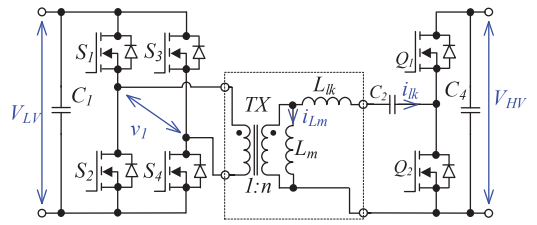

Fig. 1. Topology of the unidirectional multimode series resonant converter.

B. Operation Modes

In the forward mode, low- and high-voltage switching cells operate as the full-bridge inverter (FBI) and the active voltage-double rectifier (VDR), respectively. In the backward power flow direction, the topology configuration is the following: the half-bridge inverter (HBI) and the full-bridge active rectifier (FBR).

Previous studies have concluded that the phase-shift modulation (PSM) and have been highlighted as a simple and efficient buck and boost control method for full-bridge switching cells. At the same time, the asymmetrical pulse-width modulation (APWM) is the highest performance buck and boost control method for the half-bridge switching cells [6], [7], [8]. Therefore, the buck PSM and the boost APWM control methods can be used for the FBI-VDR configuration as well as the buck APWM and the boost PSM can be used for the HBI-FBR configuration.

The theoretical control characteristic of the IBBC in the buck and the boost control methods for two values of the operating powers is shown in Fig. 2. The control characteristic describes how the normalized voltage gain G depends on the duty cycle D for each control method. The equation for calculating the control characteristics for each control method has been presented in [6].

The normalized gain of the converter for the forward power flow is defined as

$$G = \frac{V_{HV}}{V_{LV} \cdot n}, \quad (1)$$

and for the backward power flow, the voltage gain equals

$$G = \frac{V_{LV} \cdot n}{V_{HV}}. \quad (2)$$

The control characteristic and the sequence of control methods are the same in the forward and backward power flows.

As shown in Fig. 2, the converter operates in the buck mode in the gain range 0…2. Then the converter switches to the boost mode. The transition between buck and boost control methods does not require any specific algorithms due to $D = 0$ for the boost control method is exactly the same operation point of the converter as $D = 0.5$ for the buck method.

It is worth mentioning that the buck control method features a dead control zone, where the dc voltage gain G weakly depends on the duty cycle D. This zone is nonusable for controlling the converter in practice, and it could be skipped in the implementation of a closed-loop system.

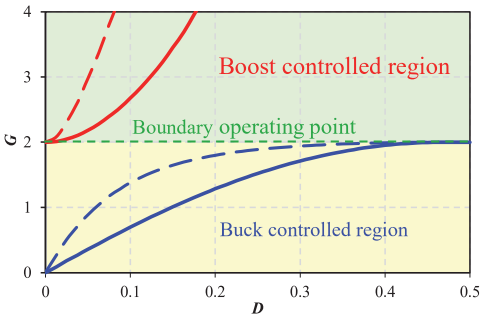

Fig. 2. Example of normalized voltage gain as functions of control variables for the buck and boost modes.

III. Description of the Identification Algorithm

The developed algorithm for the input source identification is based on scanning the I-V characteristic of a connected input source and calculating the differential conductance $\Delta I/\Delta V$. This approach does not depend on the drift of source parameters, for example, due to aging or temperature changes. Therefore, it can be applied to different types of input sources.

The paper considers the input source type identification among different PV modules and battery types. The main difference in I-V characteristic of these types of sources is the differential conductance $\Delta I/\Delta V$ observed for PV modules from the open-circuit voltage (OCV) to the maximum power point (MPP). In addition, the differential conductance of a PV module is not linear: 1) $\Delta I/\Delta V \ll 0$ from the OCV to the MPP; 2) $\Delta I/\Delta V < 0$ at the MPP; 3) $\Delta I/\Delta V \approx 0$ after the MPP. In the case of a battery, the $\Delta I/\Delta V$ is virtually constant for one condition of the state of charge, and its absolute value is much higher than that of any PV module. Fig. 3a shows an example of I-V and P-V characteristics for LR4-60HBD PV module under different shading conditions for three substrings [9]. The I-V characteristic for Power Brick+ 48V 25A LiFePO4 battery under normal conditions is shown in Fig. 3b [10].

The algorithm starts scanning an I-V characteristic by applying the minimum dc voltage gain, which would automatically correspond to OCV in the case of a PV module. During scanning, the duty cycle gradually increases with step ΔD until it reaches an MPP, in the case of PV module, or the maximum current limit of the converter, in the case of a battery. To verify the input source, the algorithm calculates $\Delta I/\Delta V$ during scanning with a voltage step ΔV.

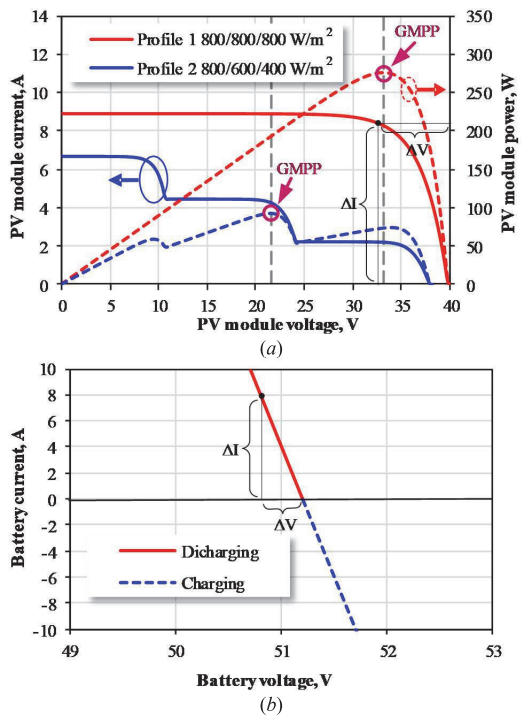

Fig.3. I-V curves of LR4-60HBD PV module under different conditions (*a*) and Power Brick+ 48V 25A LiFePO4 battery at the nominal conditions (*b*).

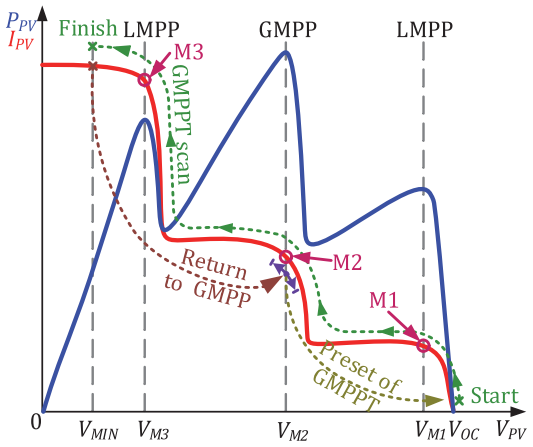

Fig. 4. P-V curve sweep GMPPT algorithm.

A. PV Mode of the Control System

In the PV mode, the control system switches to the voltage sweep global maximum power point tracking (GMPPT) algorithm based on the voltage regulation for finding out the global (real) MPP (Fig. 4). During the GMMPT scanning, the reference voltage of a closed-loop control system decreases with a voltage step V_{step}. When the GMMPT reaches the third MPP or minimum operation voltage V_{MIN}, the GMMPT algorithm analyzes stored MPP data and finds the GMPP. Then the algorithm transits to the GMPP by gradually decrementing the duty cycle to the recorded value. After that, the control system activates the local MPPT (LMPPT) based on the P&O algorithm to maximize the MPPT efficiency [7]. The converter harvests as much as possible energy from a PV module and transfers it to the dc microgrid.

B. Battery Mode of the Control System

In the battery mode, the control system switches to the droop control algorithm with a dead-zone (V_{DZ}) for battery energy storage in the dc microgrid. Depending on the microgrid voltage V_{HV}, the control system operates in two modes, as shown in Fig. 5: 1) battery charging mode if $V_{HV} > V_{nom}+V_{DZ}/2$ (nominal voltage of the dc microgrid); 2) battery discharging mode for supplying the grid from the battery if $V_{HV} < V_{nom} - V_{DZ}/2$. Therefore, the droop control stabilizes the voltage of the dc microgrid without communication between converters. The droop control algorithm provides the reference power level for the closed-loop control system of the converter. Moreover, in the battery charging mode, charging current and voltage are limited according to the conventional constant current/constant voltage strategy [11].

It should be noted that the maximum current and the maximum power of the converter are limited by selected components and heat dissipation from components. Therefore, this is one more limit for a battery charging or discharging. For the same reason, available models of PV modules for connection to the converter are also limited to market-dominating types.

C. Implementation of the Identification Algorithm

To sum up the description of the identification algorithm, the flowchart is presented in Fig. 6, where ΔD is the incrementing step of the duty cycle, $I_{LV(\max)}$ is the maximum

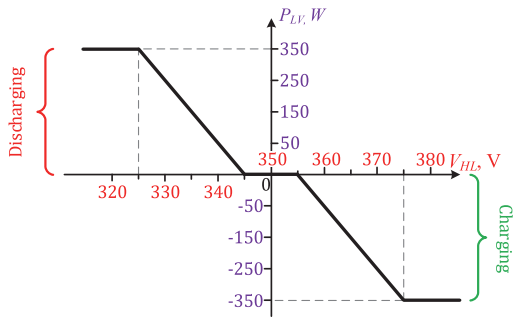

Fig. 5. Droop control algorithm for a battery energy storage.

current on the low-voltage side, which the IBBC can carry continuously.

The identification process starts with an open circuit (OC) voltage of a connected input source. During the identification process, the control system increments the duty cycle to increase the low-voltage side current and decrease the voltage V_{LV}. At each step of the duty cycle ΔD, the control system calculates the differential conductance $\Delta I/\Delta V$ value of the input power source. This process continues until the current achieves the maximum $I_{LV(\max)}$ value.

After that, the control system analyzes the stored data of the connected sources and identifies a type of source based on a trend of the $\Delta I/\Delta V$. Then, the control system switches to the LMPPT/GMPPT mode or the charging/discharging mode, depending on the input source type.

The block diagram of the closed-loop control system based on the PI-regulator for the IBBC is shown in Fig. 7. The modulation selector chooses a control mode based on the measured dc bus voltage V_{HV}, the voltage V_{LV} of a connected source. Furthermore, the modulation selector changes a power flow direction depending on the reference current in the battery mode. In addition, the control mode is changed when the duty cycle in any control mode achieves the limit [0; 0.45].

In the PV mode, a control variable for the control system is the voltage V_{LV}. The GMPPT and LMPPT algorithms scan a power curve of a connected PV module to harvest the maximum energy by incrementing or decrementing the reference voltage $V_{LV(\text{ref})}$.

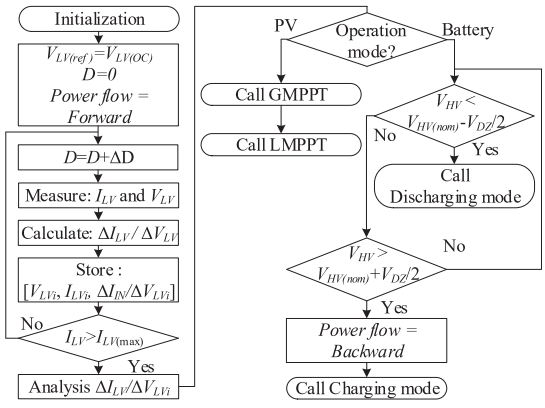

Fig. 6. Flowchart of the identification algorithm.

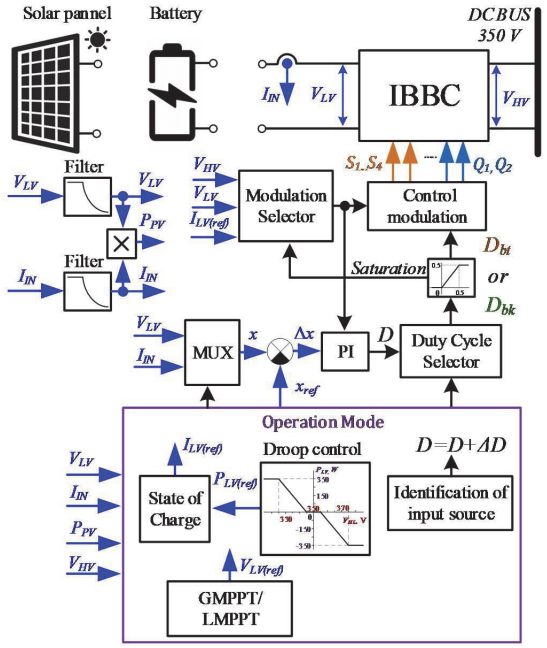

Fig. 7. Block diagram of the control system.

In the case of the battery mode, the control system regulates the current I_{LV} and changes the power flow direction according to the droop control, which sets the reference power for the converter. However, the maximum power for charging and discharging can be limited by the state of charge of a battery. For this reason, the state of charge block is added into the closed-loop control system to avoid the abnormal operation of a battery. The operation principle of the state of charge block in the charging mode is based on the conventional constant voltage/constate current algorithms [11]. In the discharging mode, the block watches the voltage of a connected battery and limits the current when the battery is fully discharged. The algorithm estimating the battery state of charge is generic and out of the scope of this study.

IV. Esperimental Results

A prototype of the universal IBBC is presented in Fig. 8. The prototype was designed and built to verify the identification algorithm. The safe operating area of the converter envelopes voltage/current ranges of the most popular PV modules (60- and 72-cells Si PV modules) and batteries (12, 24, and 48 V batteries) on the market (Fig. 9). The main components used in the prototype and general parameters of the IBBC are listed in Table I. The prototype can process the maximum power of 350 W and the maximum current of 12 A at the fixed switching frequency of 100 kHz.

The following measurement equipment was used: oscilloscope Tektronix DPO7254, differential voltage probes Tektronix P5205A, current probes Tektronix TCP0030A, and precision power analyzer Yokogawa WT1800. For verification of droop controlled operation for the IBBC, two ITECH IT6006C-800-25 Bi-directional Power Supplies were used for imitation of the dc microgrid and the battery Power Brick+ 48V 25A LiFePO4. The bi-directional power supplies have the arbitrary generator function allowing for programming dc bus voltage and setting the state of charge for the emulated battery. The PV module LR4-60HBD was imitated by the Solar Array Simulator Keysight E4360A.

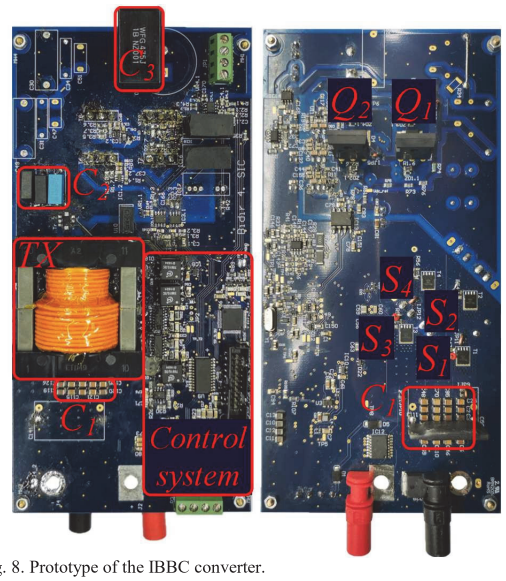

Fig. 8. Prototype of the IBBC converter.

TABLE I. GENERAL PARAMETERS

Operating parameters	
Input voltage, V_{in}	10…60 V
Maximum input current, I_{in}	10 A
Output voltage, V_{out}	350 V
Switching frequency, f_{SW}	100 kHz
Operating power range	30…350 W
Components	
S_1 … S_4	On Semiconductor FDMS86180
Q_1, Q_2	LittleFuse LSIC1MO120E0080
C_1	105 µF
C_2	81 nF
C_3	0.47 µF
L_{lk}	35 µH
L_m	0.9 mH
n	5.5

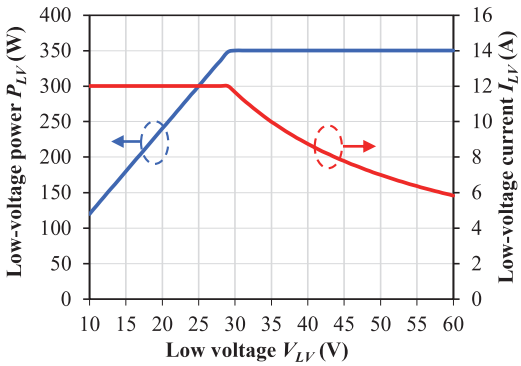

Fig. 9. Safe operation area for the designed IBBC prototype.

A. Static Efficiency Evaluation

Static experimental analysis shows that the prototype operates in a wide input voltage range of 10 to 60 V (Fig. 10). The peak efficiency of the converter is 98 % at the nominal input voltage equals 33 V (the normalized voltage gain equals two). The efficiency is higher than 92% in the most probable operation region. The efficiency levels achieved close to the upper and lower voltage range boundaries are acceptable considering the low-cost design with balanced performance.

The achieved high efficiency in the wide input voltage range verifies the possibility of the universal IBBC operation with different types of batteries such as 12, 24, and 48 V or different types of PV modules such as 60-cells and 72-cells.

B. PV Mode Verification

During the identification process, the control systems achieved the first MPP of the LR4-60HBD PV module under different partial shading conditions (Fig. 11). After that, the control system switched to the P-V curve sweep GMPPT algorithm and scanned a P-V curve of the PV module. During the scanning, the converter operates under the forward buck and boost modes. A low parasitic oscillation can be seen in the experimental curves due to the non-linear real dc gain characteristics of the converter. Nevertheless, these oscillations do not influence the performance of the GMPPT. After scanning, the control system switches to the LMPPT, where the converter operates without parasitic oscillations.

C. Battery Mode Verification

Fig. 12 shows the operation of the IBBC under the proposed algorithm with Power Brick+ 48V 25A battery at the grid voltage V_{HV} of 330 and 370 V. The control system gradualy, increases the battery current before the maximum power of the converter ($I_{LV(max)}$=6.8 A, $P_{LV(max)}$=350 W) is achieved to identify the input source type. According to the droop control from Fig. 5, the control system switches to the battery charging or discharging mode after identifying the input source. In the first experimental case, the converter operates under the forward buck control mode. A regulation rage of this control mode covers the current range in the discharging mode. In the second case, after the input source identification, the control system gradually decreased the reference current and switched to the backward boost mode. Then, it increased the current in the backward power flow direction up to the required reference level. It should be noted that the converter changes the control modes between the forward and backward power flow directions without zero current distortions and spikes.

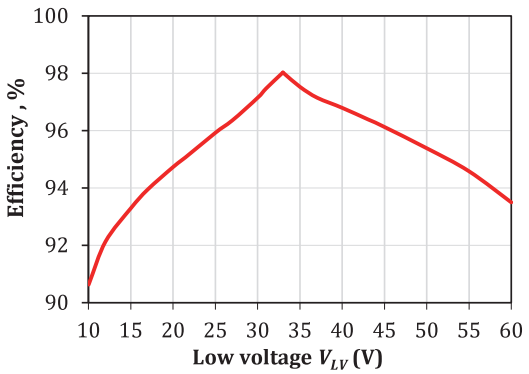

Fig. 10. Measured efficiency of the IBBC.

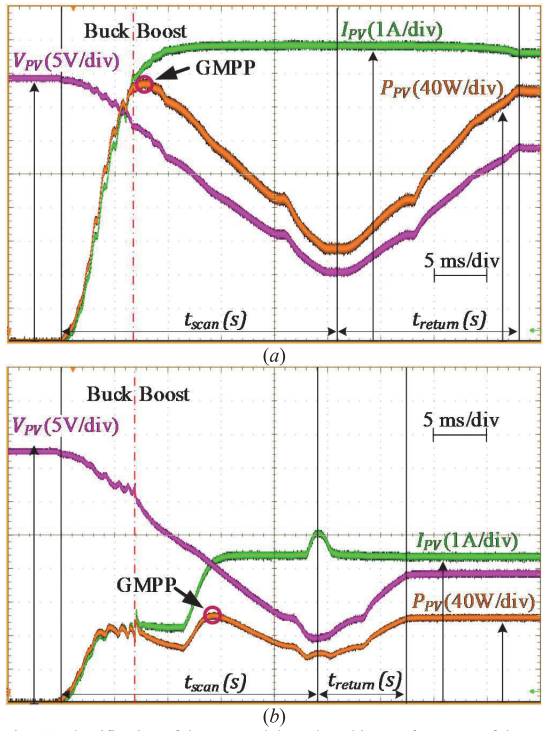

Fig. 11. Identification of the PV module and tracking performance of the voltage sweep GMPPT algorithm under two shading profiles of the three substrings: (a) 800/800/800 W/m2 and (b) 800/600/400 W/m2.

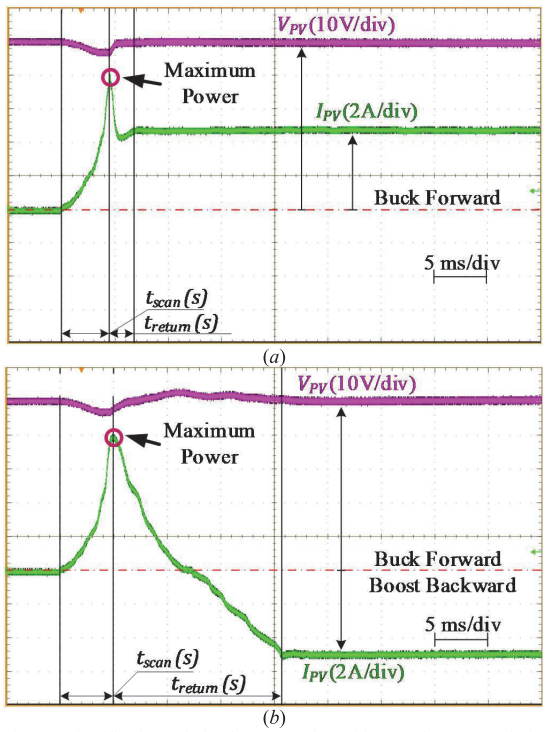

Fig.12. Identification of the battery and tracking performance of the discharging mode at VHV = 330 V (a) and the discharging mode at VHV = 370 V (b).

V. Conclusions

The paper has demonstrated the universal front-end dc-dc converter based on the isolated buck-boost series resonant converter for connection of individual 60- or 72-cells Si PV modules or 12/24/48V LiFePO4 batteries to the 350 V dc microgrids. Experimental analysis of the converter shows that the converter operates in the wide input voltage from 10 V to 60 V with a peak efficiency of 98%. The main contribution of the paper is the algorithm for the input voltage source type identification. Experimental results show that the proposed algorithm correctly detects input voltage sources. After the identification, the control system switches to the global maximum power point tracking in the case of operation with a PV module or the charging/discharging mode according to the droop control characteristics of the battery energy storage in the case of operation with a battery. In addition, the converter changes the power flow direction without zero current distortions and spikes in the case of the operation with the battery.

Acknowledgment

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