THESIS ON INFORMATICS AND SYSTEM ENGINEERING C19

Investigation of electrical characteristics of SiC based complementary JBS structures

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Declaration

Hereby I declare that this thesis is my original, unaided work. It is submitted for degree of Doctor of Philosophy in Engineering of Tallinn University of Technology, Tallinn, Estonia. It has not been submitted before for any degree or examination.

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Abstract

The main target in power electronics is to decrease the energy losses. This is never ending task, which deals from one side with the design and study of new devices and from another side with introduction of new materials. Junction Barrier Schottky (JBS) diode is very promising new device and silicon carbide (SiC) is the material, which could overstep the silicon weaknesses.

This thesis presents results of simulation of SiC based complementary JBS devices.

The first chapter gives overview of promising semiconductor material: silicon carbide (SiC). SiC material properties, device manufacturing technologies, applications, and problems are described. The second chapter introduces novel rectifying device: JBS diode. Device working principles are described, different realizations are shown, and state of the art is introduced. Third chapter describes methods, which were used in this thesis for simulations: description of mathematical model used for simulation of electrical processes in semiconductor, overview of numerical simulation and description of software used is given. Fourth chapter consists of the results of simulations and discussion.

The most interesting results of this thesis include: the inner processes of JBS device are shown in 3D, as 2D figures may not give complete information about the behaviour of the device; the best *n* and *p* substrate based JBS devices for power application are found in means of device dimensions, material type (4H- vs 6H-SiC), epitaxial layer concentration, Schottky contact metal work function values, relation of *pn* and Schottky area; comparison of *p* and *n* substrate based JBS devices is done.

Total 95 pages, included 5 added publications on 29 pages.

Kokkuvõte

Jõuelektroonika peamiseks eesmärgiks on vähendada energia kadusid. See on lõputu töö mis seisneb ühelt poolt uudsete seadiste väljatöötamises ja uurimises ning teiselt poolt uudsete materjalide kasutuselevõtus. *pn* siirde ja Schottky barjääriga (JBS) diood on heade omadustega uus seadis ja ränikarbiid on materjal mis suudab ületada paljud räni nõrkused.

Käesolev väitekiri esitab ränikarbiidil põhinevate JBS dioodide simulatsioonide tulemused.

Esimene peatükk annab ülevaate paljulubavast pooljuhtmaterjalist, ränikarbiidist (SiC). Kirjeldatakse ränikarbiidi omadusi, seadiste tootmise tehnoloogiaid, rakendusi ja probleeme. Teine peatükk tutvustab uudset alaldavat seadist, JBS dioodi. Kirjeldatakse seadise tööpõhimõtteid ja erinevaid variatsioone, tutvustatakse uusimaid saavutusi. Kolmas peatükk kirjeldab antud väitekirjas esitatud simulatsioonitulemuste saamise meetodeid: toodud on pooljuhis toimuvate elektriliste protsesside kirjeldamise matemaatiline mudel, numbriliste arvutuste põhimõtted ja kasutatud tarkvara kirjeldus. Neljas peatükk koosneb simulatsioonitulemustest ja arutelust.

Kõige huvitavamad väitekirjas saadud tulemused sisaldavad: simulatsioonitulemuste kolmemõõtmelisi graafikuid, millest saadav informatsioon on paremini haaratav ja täielikum kui seni kirjanduses kasutatud kahemõõtmelised graafikud; jõuelektroonika rakendusteks parimate *n* ja *p* alustel põhinevate JBS seadiste kirjeldusi (seadise mõõtmed, materjali tüüp 4H vs 6H, epitaksiaalkihi lisandikontsentratsioon, Schottky kontakti metalli väljumistöö, *pn* ja Schottky alade suhe); *p* ja *n* alusel põhinevate JBS seadiste võrdlust.

Töö sisaldab kokku 95 lehekülge, sealhulgas 5 lisatud publikatsiooni 29 leheküljel.

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I would also like to thank Ph.D. Andres Udal for developing and guiding me to use *SiC-DYNAMIT-2DT* simulation software, but also his in-depth teaching method in explaining me aspects of the physics of semiconductors.

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Introduction

The main target in power electronics is to decrease energy losses. This is never-ending task, which deals from one side with the design and study of new devices and from another side with introduction of new materials. Junction Barrier Schottky (JBS) device is very promising new device and Silicon Carbide (SiC) is the material, which could overstep the silicon weaknesses.

The author of this thesis has been studying devices with different Schottky barriers over 7 years. Different barrier heights in the same device were investigated as well (e.g. [1], [2]). There are many aspects in these devices, what are similar to ones in JBS (e.g. current crowding phenomenon). Due to the fact that almost all effects observed earlier, take place also in JBS devices, I chose the JBS device for study object in this work. From another point of view the JBS devices have specific advantages compared to traditional simple *pn* or Schottky devices and there was the second main reason to do this research. This is the reason why JBS is the study object of this thesis.

There have been many experimental results published till today dealing with simulation of JBS devices. Almost all simulation reports discuss relatively small number of the best relation of *pn* and Schottky areas, only some of the reports are dealing with the different Schottky contact metals, size and placing of implanted regions, thickness and doping concentration of drift region. There have been no papers about JBS devices based on *p*-type SiC. Very poorly is investigated the processes inside of JBS devices. The electric field strength distribution and minority carrier distribution in the device has been studied and those studies have been done only in certain parts inside the device and in one dimension.

First task of this work is to define the properties of the "best device" (with some restrictions) using two-dimensional solutions. Clear picture of current crowding has been observed, which is very important for the whole device analysis. The second task of this work is to study and compare the behaviour of complementary JBS devices.

The simulations in this work have been done with simulation software mostly developed by Andres Udal (Department of Electronics, TUT), called *SIC-DYNAMIT-2DT* aided by *bash* shell scripts for automation of simulations and *gnuplot* for presenting the results.

1. Silicon Carbide

1.1. Introduction

The technology of producing Si power devices has practically reached its physical limits [3]. There is very little room for new developments in this field. It is time for search of new materials. SiC has many advantages over Si. SiC properties make it suitable to use the material in high temperature, high power, high frequency and radiant resistant applications, where Si starts to fail. There are semiconductor materials like GaAs, AlN, GaN, BN, diamond, ZnSn and others with good properties for such applications. Still, SiC has the widest use in named applications because of several advantages. Most important of them is the fact that the technology of producing SiC semiconductor devices is close to well-known Si technology. About 30 years ago, the GaAs was thought as universal future semiconductor material. Nowadays it has found only a small part of wide semiconductor materials market. Compared to GaAs, SiC has 8 to 10 times higher thermal conductivity than GaAs and twice the band gap of it, which makes SiC more promising in high power applications, but also in high packaging density integral circuits and other applications. However, there are still many technological problems in taking SiC technology into wider use. The quality of the crystal is not good enough, the quality of native oxide SiO_2 is poor, etching is difficult because of inertness of SiC to chemical reactions, diffusion process is unusable because of high temperatures needed, high temperature contacts are to be developed to use the ability of SiC to work on high temperatures. Because of high electric field strength in SiC Schottky diode, the junction termination and passivation issues are very important [4]. There are many problems to solve, like it mostly is with new technologies.

The knowledge that SiC can be used as semiconductor material for electronics purpose is not new. In fact, SiC crystals were grown already in 1893 by Acheson and a light emitting diode in SiC was produced in 1907 by Round [5]. SiC as a material for electronics got wider use by inventing the Lely high quality crystal growth technology in 1955 [6]. In 1978 was invented seeded sublimation growth technique (modified Lely technique), which made possible to grow bulk crystals [7]. This was the beginning of active research in this field, which led to foundation of first commercial supplier of SiC substrates: CREE Research in 1987.

1.2. Properties

SiC polytypes have many superior electrical properties compared to Si:

- wide bandgap (~3 times of Si),
- good thermal conductivity (3.3 times of Si, the thermal conductivity exceeds even that of copper),
- high electric field break down strength (~10 times of Si),
- high saturation drift velocity (~2.5 times of Si) [5].

Those and other important parameters of some SiC polytypes compared to GaAs, Si and Diamond are brought in table 1.

SiC is also better from Si on other physical aspects:

- The inertness of SiC to chemical reactions allows using it in hostile environments for sensors.
- The hardness of SiC allows operating devices on extreme pressures. SiC is also used as the grit coating on sandpaper.
- SiC is extremely radiation hard and can be used close to reactors or for space electronic hardware.

Table 1. Comparison of semiconductor properties [8]

Property	***3C-SiC***	***4H-SiC***	***6H-SiC***	***GaAs***	***Si***	***Diamond***
Melting point [C]	2830	2830	2830	1238	1420	4000
Thermal Conductivity [W/cmK]	5	4.9	4.9	0.46	1.5	20
Bandgap [eV]	2.39	3.26	3.02	1.43	1.1	5.45
Electron mobility [cm^2/Vs]	1000	1000	370	8500	1500	2200
Hole mobility [cm^2/Vs]	50	50	90	400	600	1600
Saturation Electron Drift Velocity [$x10^7$ cm/s]	2.2	2	2	1	1	2.7
Break down field [$x10^5$ cm/s]	20	30	30	6	3	100
Dielectric constant	9.7	9.7	9.7	12.5	11.8	5.5

All these properties make SiC very good solution for conditions unsuitable for Si. The same properties, which make SiC usable on high temperatures, make it hard to produce SiC devices. SiC needs very high temperatures on device production. The strong bond of SiC lattice makes unreasonable to use diffusion methods, well known from Si device production.

SiC has many good parameters, but it is hard to compare different semiconductor materials on base of many parameters simultaneously. Figures of merit are good solution for this purpose. Figures of merit combine important parameters and result only in one number. This makes it easy to compare different semiconductors physical usability for certain application. It makes even possible to say how much is one semiconductor better than other.

Johnson's Figure of Merit is for high frequency and high power applications [9]. As seen from formula of Johnson's Figure of Merit (1), it depends on break down electric field strength and electron saturation velocity, and therefore can be described as: how fast and how high electrical fields strength can a device from this semiconductor material possibly drive.

$$JMF = \frac{E_B^2 v_s^2}{4\pi^2} \qquad (1)$$

E_B - break down electric field strength,
v_s - electron saturation velocity.

If we compare the *JMF* of SiC and Si, then SiC looks about 281 times better than Si. Of course, this is the case only if technologies of both materials could be able to make devices near the edge of physical limits. This is almost true for Si, but long away for SiC. Still, there are already many SiC devices with better characteristics than physical limits allow producing from Si.

The Keyes' Figure of Merit is mostly for integrated circuit application, where high-density packaging and working frequencies are important [9]. As seen from formula (2), this figure of merit depends on thermal conductivity and electron saturation velocity. The thermal conductivity of material takes into account how dense can packaging be without overheating and electron saturation velocity takes into account how fast can circuit be.

$$KMF = \chi\sqrt{\frac{cv_s}{4\pi\varepsilon_0\varepsilon_r}} \qquad (2)$$

χ - thermal conductivity
c - velocity of light
ε_0 - dielectric constant of vacuum
ε_r – relative dielectric permittivity of semiconductor

According to Keye's Figure of Merit, SiC is 6.5 times better than Si.

Electron and hole mobility are parameters, which affect the high frequency performance, transconductance, and other important device parameters. The low and anisotropic electron mobility of 6H-SiC is one of the primary reasons for the growing popularity of 4H-SiC. The mobility of electrons in perpendicular to c axis is about 1.25 times lower than in parallel to c axis in 4H-SiC and 4.8 times higher in 6H-SiC at 300K. Also other parameters vary widely on different polytypes.

1.3. Applications

Nowadays SiC is mostly used for applications where Si can not offer acceptable results. SiC is used for high-voltage switching in public electric power distribution and electric vehicles. It allows producing more powerful microwave electronics for radar and communications. The use of SiC devices for "smart" electric power distribution could reduce energy production about 5% and allows to carry about 50% more power over existing power lines [10]. SiC can offer electronics for power distribution networks, which can save about 50 billion USD during next 25 years in North America [8]. The sensors and controls for cleaner-burning more fuel-efficient jet aircraft and automobile engines are often not possible to make on Si because of hostile environment in engines. The first SiC devices, which reached high volume sales, were blue light emitting diodes. Ultraviolet sensitive photodiodes and high temperature JFET's have also been commercially available for some time. SiC can also be better solution because of measures and weight. For example SiC power MOSFET's and diode rectifiers would have die sizes nearly 20 times smaller than correspondingly rated silicon-based devices [11]. The weight and measures are especially important in spacecraft. Material advantages allow thinner heavily doped drift region compared to silicon, which results in up to 2 orders of magnitude lower specific on-resistance compared to Si device with same break down voltage. SiC SBD has about 200 times lower specific on-resistance theoretical limit than analogous Si SBD diode [4]. Due to good thermal properties of SiC devices it is possible that some day it will be cheaper to use it even on everyday high speed logic chips like microprocessors. Higher working

temperatures and better thermal conduction make cooling easier. Cooling, in fact, can be sometimes extremely expensive. One breakthrough in computer technology could be dynamic memories on SiC. The band gap of SiC is so wide, that charges put into microscopic SiC device at room temperature, can be read after 100 years. In computer technology this means ultra fast and very reliable hard disks without mechanical parts [12].

1.4. Polytypes

Polytypes are structures, built from the same layers with different stacking order. Each layer of SiC consists of two planes of Si and C atoms. There is one Si atom over every C atom. One chemical bond is between every pair of Si and C atoms laying one over other. Each atom has three bonds connected to other layers. Each SiC bilayer can be oriented into only three possible positions with respect to the lattice. These three positions can be marked as A, B and C. The order of these layers result in different polytypes.

There are many different polytypes of SiC. The polytypes are divided into three crystallographic categories: cubic (C), hexagonal (H), and rhombohedral (R). One cubic, about 70 hexagonal and 170 rhombohedral lattice SiC crystal structure arrangements are possible [13]. Over about 200 of them are already discovered. The polytypes are marked as follows. First part of the code shows the number of layers needed for periodicity, the letter shows the overall symmetry of the crystal: C, H or R. The structure ABAB... is called 2H-SiC, it is 2 bi-layer structure with hexagonal symmetry. All except 2H and 3C polytypes form one-dimensional superlattice structures. There is only one cubic SiC polytype: 3C-SiC. It is also known as α-SiC. The hexagonal structures are grouped as β-SiC. The best known from rhombohedral polytypes is 15R-SiC. Better-known polytypes are 3C, 2H, 4H, 6H, 8H, 9R, 10H, 14H, 15R, 19R.

1.5. Device production

1.5.1. Substrate

The monocrystals of SiC are mostly growed using technologies based on the modified Lely process. This is a process, where SiC vapours sublimate from higher temperature (2400 K) polycrystalline source and condense on lower temperature (2200 K) crystal seed. The result is a single polytype monocrystal. Growth rates for this technology are up to few millimetres per hour [8].

Most important problem in production of SiC devices is the quality of bulk SiC. The SiC bulk tends to have micropipes. Micropipes are defects, which start from the seed and propagate through the whole crystal, and even through the epitaxially grown layers. Micropipes are pipes with hexagonal cross-section in diameters about 0.1 to 5 μm. The mechanisms causing the micropipes are not fully identified. Nowadays wafers with micropipes density below 5 micropipes per cm^2 are commercially available [14], [15]. It is also possible to close micropipes using liquid phase epitaxial growth [15].

The sizes of wafers must also grow before SiC can find wider use. Right now 76 mm SiC wafers are commercially available [14], [16]. One solution could be PolySiC, which has almost same properties as monocrystalline SiC, but production of such wafers is much easier and there is no micropipes. Such wafers with measures up to 200 mm are already commercially available [17].

1.5.2. Doping control

Mainly two techniques are used for doping control in SiC device: epitaxially controlled doping and hot ion implantation. The diffusion is not possible because of high temperatures (over 1800 ˚C)

needed to overcome high bond strength in SiC. Ion implantation requires also high temperatures. Implantation is performed at 600-800 °C to reduce lattice damages and later the object is annealed at 1000-1700 °C to activate the dopants [12]. The most widely used dopants for SiC are N (*n*-type) and Al (*p*-type). For *n*-type is also used P and for *p*-type B, Ga, Sc.

In case of epitaxially controlled doping, the deepness of doping is controlled from 10^{19} cm^{-3} to 10^{14} cm^{-3} with varying Si and C source gases: silane and propane respectively. N and C compete for C sites and Al and Si compete for Si sites in SiC crystal. Epitaxial doping is useful because it does not cause lattice damage and there is no need for high temperature anneal.

Ion implantation is widely used because of absence of usable diffusion process. For *p*-type implantation, B is easier to implant than Al because of heavy mass of Al compared to B. Al causes much lattice damage to SiC on implantation. The implantation is performed on high temperatures (over 700 °C) to avoid amorphisation of SiC. Annealing at 1100 °C to 1650 °C is also necessary after implantation for activating dopants. Ion implantation is used to do selective doping.

1.5.3. Etching

Etching is also a big problem compared to Si processing. Wet etching is only possible with molten salts at high temperatures, which is not feasible. There are several dry etching techniques (reactive ion etching, electron cyclotron etching, photoelectrochemical etching) used successfully for SiC.

1.5.4. Oxidation

Oxidation is a process, which is compatible with Si processing and makes it possible to use the same technology for SiC. The technique for oxidation is the same as for Si, only grow-rates are slower. Obtaining a high quality SiO_2 on *p*-type SiC is a problem because of the carbon on the surface of SiC crystal and also off-axis epitaxial layers. The growth of oxide depends strongly on surface's orientation and face. Bad quality SiC-SiO_2 interface area leads to a significant degradation in the channel mobility leading to a low transconductance of FET transistor. The deposited dielectrics are used to avoid poor quality of SiO_2. The other way to overcome this problem is to use devices, which do not relay on quality of oxide: like MESFET.

1.5.5. Ohmic contacts

The ohmic contact is a weak point in SiC technology. For high current devices the resistance of contact to semiconductor is extremely important. A little bit too high contact resistivity can cause overheating of contact on high current densities. As SiC is able to work on high temperatures, the contact can become a bottleneck from the point of view of chosen metal. For example, widely used Al contacts for *p*-type SiC are easily oxidizing. The B_4C may provide an answer here in stability compared to Al/Ti alloys. For *n*-type contacts Ni_2Si and $CoSi_2$ are widely used.

1.5.6. Schottky contacts

The Schottky contacts barrier height is important for using MESFETs and Schottky rectifiers on high temperatures. There is wide range of metals used for Schottky contacts: Ni, NiCr, Au, Ti, Mg, Co, Al, Hf and Pd. The barrier height depends on surface quality of SiC, metal deposition process, polytype, n- or *p*-type SiC, C- or Si-face. The highest Schottky barriers on Si face of 6H-SiC have Au and Ni with about 1.47 eV and 1.27 eV respectively [5].

1.5.7. Diffusion welding in Institute of Electronics, TTU

At the Institute of Electronics, TTU, SiC Schottky diodes are produced on 6H- and 4H-SiC substrates with 8mm diameter (area about 50 mm^2) Al contacts. Contacts are formed by diffusion welding process in 500 sec under pressure of 50 MPa at temperature 600 ^{o}C. The Al contact on C-face forms Schottky contact with the barrier height about 1.3 eV in both cases. The contact on Si-face (bottom) forms ohmic contact. More detailed information has presented in [18], [19].

1.6. Problems in long term operation

SiC power devices have one important disadvantage, namely forward degradation during operating period. The reason is structural defects, which are formed by electrical stress [20]. The stacking faults are acting as recombination centres and reduce the carrier lifetime in semiconductor. The result is the increase of static forward voltage drop during operation period. Some of the authors have reported even as much as an order of magnitude forward voltage degradation [21].

1.7. Conclusions

There are all presumptions for rapid development of SiC technology for semiconductor devices (in spite of all difficulties and limitations cited further):

- Si technology is near its physical limits.
- New technologies are needed for several applications.
- SiC technology is close enough to Si for starting.

There are some limitations, which are holding down the speed migrating from Si to SiC. Resolving of those problems seems to be the question of time:

- quality of bulk SiC,
- technology for managing with chemically inert SiC,
- forward degradation.

2. Junction Barrier Schottky diode

2.1. The Device

There are two basic diode types:

a) ***pn* barrier diodes**, which have low leakage current but long reverse recovery time. The reverse recovery time can be shortened by impurities that reduce the lifetime of minority carriers, but this also increases forward voltage drop and reverse leakage current.

b) **Schottky barrier** diodes, which have short reverse recovery time, but high leakage current and low break down voltage.

Basically, *pn* barrier diode works great in case of reverse voltage and Schottky diode in case of forward voltage and switching processes. The advantages of those two devices can be combined in device where both structures are connected in parallel. This device is called a JBS (Junction Barrier Schottky) diode and a section of it is shown in Fig. 1 c.

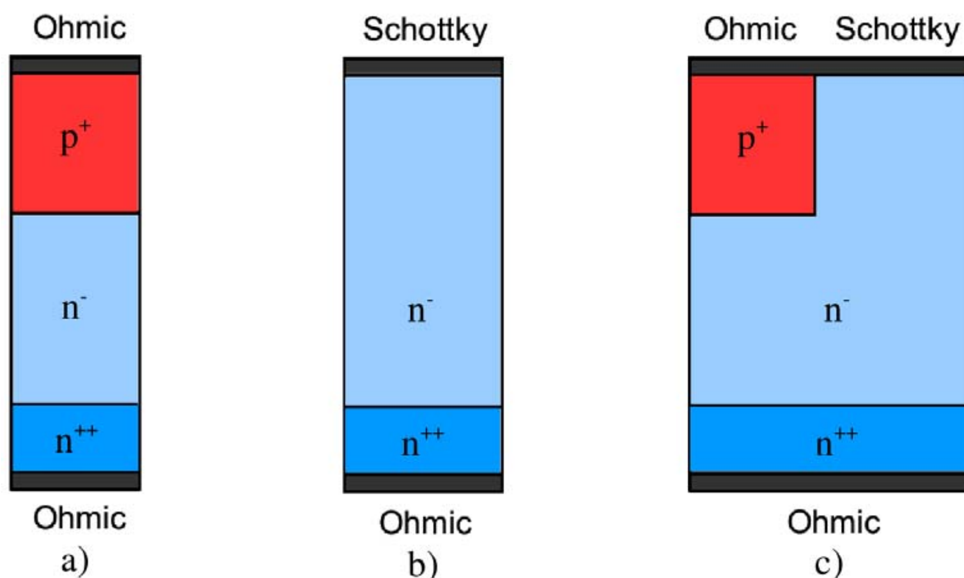

Figure 1: a) pn diode, b) Schottky diode c) JBS diode

Such device works as Schottky diode except in case of reverse voltage, when *pn* barrier forms depletion region, which limits electric field strength on Schottky barrier, and thus also limiting Schottky barrier lowering and in conclusion also whole reverse current.

The idea of using parallel Schottky and *pn* junctions is dated from 1984, when Si JBS Rectifier was introduced by B.J. Baliga [22].

2.2. JBS diodes variations

There are different constructions for JBS diodes. First devices were made using opposite conductivity diffusion regions under Schottky contact pretty much like shown in Fig.1 c. As such

kind of devices were introduced to overcome power devices *pin* and Schottky diode problems, those are also called Merged P*in* Schottky, or Merged P*n* Schottky (MPS) diodes. Later different JBS device constructions were studied to get even better results. One of such improving methods is bringing *pn* junction deeper into the device. Bringing *pn* junction deeper into device, *pn* junction areas can be made thinner and having still the same ability to block Schottky leakage current. Thinner *pn* regions save more contact area to Schottky contact and those allowing bigger forward currents [23]. There have even proposed devices where opposite doping areas are made almost through the epitaxial layer or even down to the epitaxial layer. Such JBS diodes are named Super Junction MPS rectifiers [24].

One interesting solution is replacing *pn* junction with MOS structure. This kind of device has oxide isolated metal contacts in the device in place where JBS device has implanted semiconductor regions. Such kind of devices are called Trench MOS Barrier Schottky (TMBS) devices. This solution results in better blocking of Schottky leakage current. It can even work efficiently at large epitaxial layer doping of $10^{17}cm^{-3}$. As larger doping concentrations result in lower resistance this solution can be used to get rectifier devices with much better on-state characteristics without sacrificing off-state leakage currents [25]. The illustration of TMBS device is brought in Fig. 2.

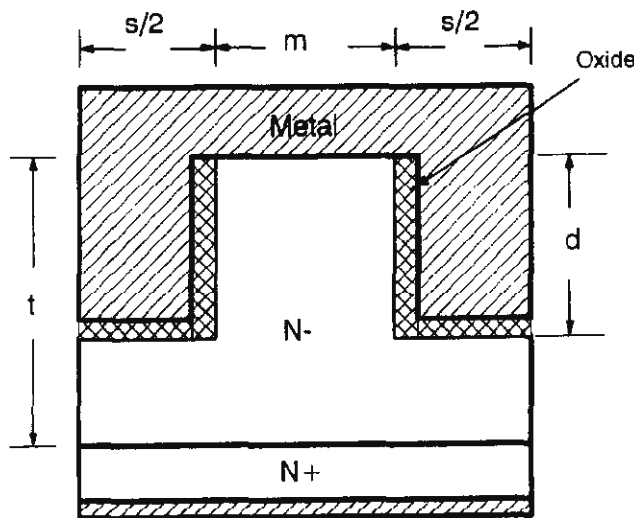

Figure 2: TMBS device. Illustration from [21]

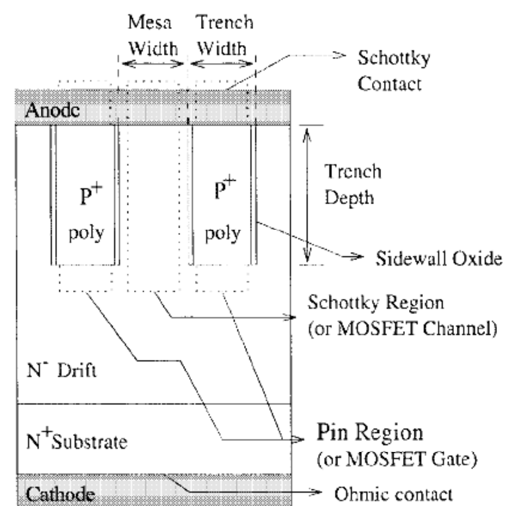

Figure 3: TSOX-MPS rectifier. Illustration from [22]

The example of oxide isolated poly silicon trench version of Si JBS have been used to simulate and produce a device, which has better characteristics than ordinary JBS. The device is called silicon Trench Sidewall OXide Merged P*in* Schottky (TSOX-MPS) rectifier [26]. The structure of TSOX-MPS is shown in Fig. 3.

Even better reverse voltage parameters can be achieved with another modification of TMBS. There are two electrical field peaks in ordinary TMBS device, one just below the Schottky contact and another in the device around the end of trench region. Electrical field between those peaks is very low. It is possible to produce such a device, where the whole area from Schottky contact to end of trench regions has almost the same electrical field, which results in higher reverse break down voltages. This is realized by using graded doping concentration where doping concentration is lower under Schottky contact and increases linearly down to the substrate. Such device is named Graded Doping Trench Merged Barrier Schottky diode (GD-TMBS) [27], [28]. The structure of GD-TMBS is shown in Fig. 4.

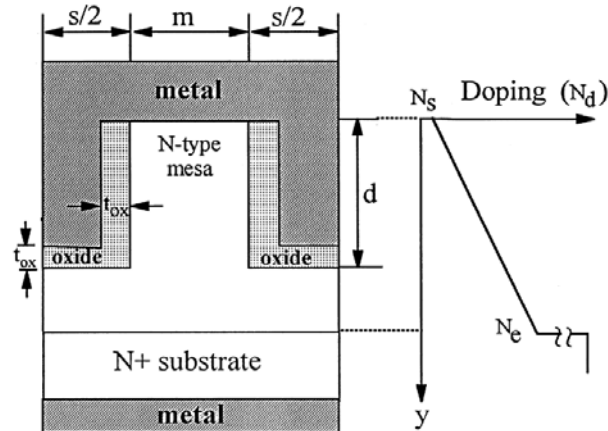

Figure 4: GD-TMBS diode. Illustration from [23]

As graded doping concentration production can be more expensive than uniform, there are also variants of JBS there almost same electric field strength from Schottky contact to the end of trench bottom can be achieved by method called Thick Oxide Trench MOS Barrier Schottky (TO-TMBS) [29]. The structure of TO-TMBS is shown in Fig. 5.

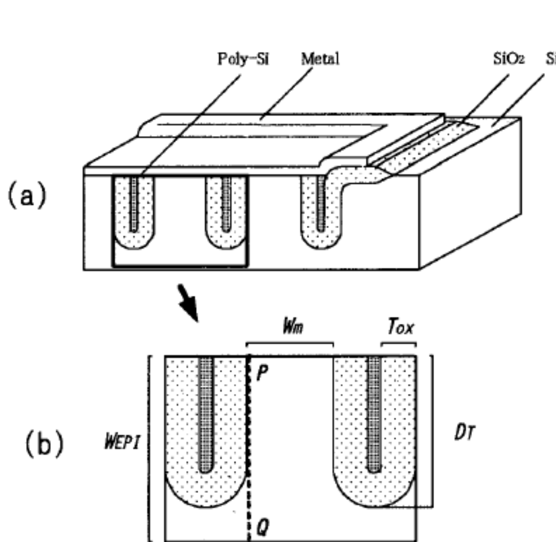

Figure 5: TO-TMBS device. a)structure, b) unit cell. Illustration from [25]

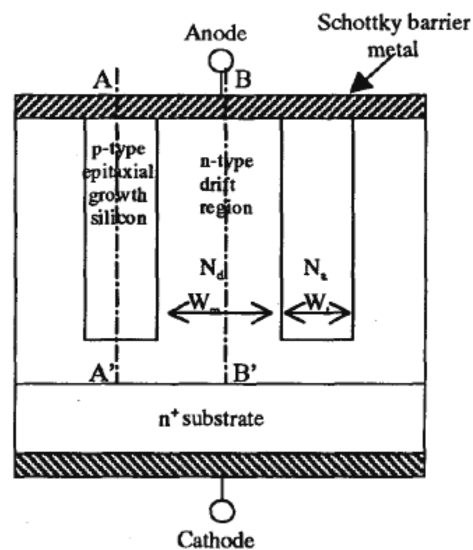

Figure 6: MR-JBS device. Illustration from [26]

The same group has also proposed another possibility of producing JBS rectifiers: by filling trench region with single crystal silicon. Such devices are called Multi RESURF Junction Barrier Rectifiers (MR-JBS) [30]. The structure of MR-JBS device is shown in Fig. 6.

Since formation of deep implantation regions into SiC is very difficult, there is also proposed a device where area with implantation is replaced with another metal, which work function is higher than one of the main metal. Such device is called Trench Schottky Barrier Schottky (TSBS) diode [31] with structure shown in Fig. 7 or Dual Metal Trench (DMT) diode [32] with structure shown in Fig. 8.

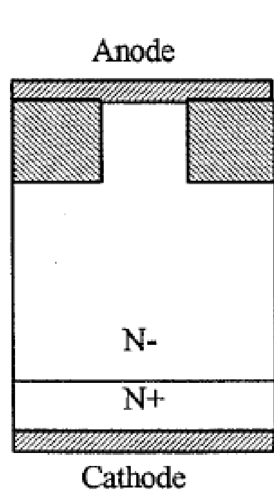

Figure 7: TSBS device. Illustration from [27]

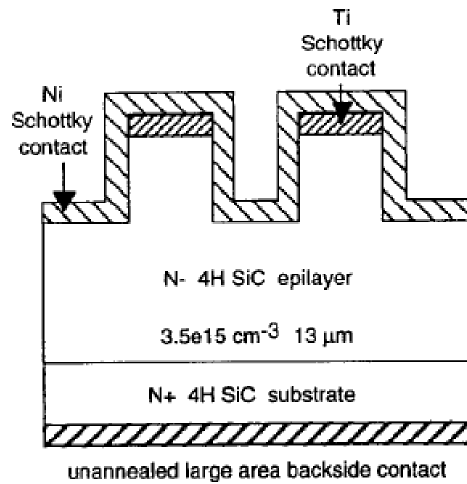

Figure 8: DMT device. Illustration from [28]

Studies on sub micron technology JBS have also been done and found that small measures (around 1 µm) of *pn* and Schottky regions can improve device parameters but junction depth lower than 0.3 µm are not usable [33].

2.3. Electrical behaviour

As mentioned above, JBS has Schottky-like on-state characteristics (on low voltages) and *pn*-like off-state characteristics. Both on- and off-state illustrations are shown in Fig. 9.

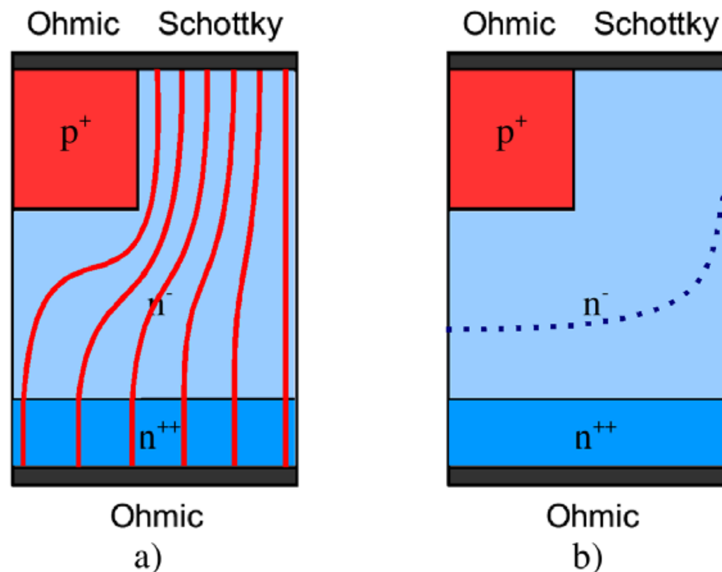

Figure 9: a) on-state JBS diode, lines show current flow; b) off-state JBS diode, dotted line shows the edge of depletion region. (Lines have illustrative meaning only)

On low forward voltages only Schottky part of JBS conducts (current lines in Fig. 9 a). Voltage drop and resistance is defined by lower ohmic contact quality, resistance of epitaxial layer region,

Schottky contact barrier height and quality. Device works basically like a Schottky diode. On higher forward voltages also the *pn* part of the JBS starts to conduct.

In case of reverse voltage the picture is somehow different. Although in case of separate devices Schottky diode has higher leakage current than *pn* junction, the leakage of Schottky contact in JBS does not determine the leakage current of the whole device. The Schottky contact leakage current is cut away by the depletion region of the *pn* junction (dotted line in Fig. 9 b). Formed depletion region shield also protects Schottky structure from high electric fields and thus avoids Schottky barrier lowering.

Switching speed is also higher. On low forward voltages main current flows through Schottky area as said earlier. As current flows through Schottky area, there is no significant minority carrier charge store and no need to discharge it. The switching speed may be slower on high forward currents because of the same minority carrier charge, which builds up also in JBS devices in case of high forward currents.

2.4. State of the art situation

2.4.1. Device fabrication and measurements results

There have been quite many experimental SiC JBS fabrication an measurement reports published. Some of those deal with practical design and manufacturing issues like material quality, junction termination and passivation problems, which are extremely important [34], [35]. One has to be aware that ideal simulation results are far from reality in experimental measurements if termination and passivation is not done correctly. Also material defects can influence results much more because of higher electric field strength in SiC compared to Si. As there is a trade off between forward voltage drop and leakage current, this aspect has been studied by many authors by comparing different Schottky and *pn* junction area relations [36], [37], [38]. It has been shown that the trade off between forward voltage drop and leakage current does not depend only on Schottky and *pn* area relation, but also on *pn* junction deepness. Deep and narrow *pn* junctions give good results on reverse voltage blocking, but also do not take much of contact surface allowing bigger Schottky contact areas, and thus better forward characteristics [23]. It has also been shown that V_F/I_R relationship does not depend only on Schottky-*pn* area relations but also on geometrical layout of those [39]. It has been shown that JBS has V_F/I_R trade off advantage over conventional Schottky barrier diode at low current density, but almost no advantage at high current densities (above about 85 A/cm^2) [36]. Also different authors have studied contact properties. Temperature annealing effect to reduce surface damaging is shown and influence on device parameters are measured [37], [38], [40]. Both forward and reverse characteristics temperature dependence is done [41], [40], [42]. *pn* part implantation area doping concentration varying is done [40]. Also one of JBS good qualities, its high switching speed, has been studied [41], [42].

Most of authors are dealing just with performance and price of JBS devices. For mass production purpose there is one very important factor more: stability. In commercial systems a device must last without failure even tens of years. The stability of JBS can be in some situations quite questionable. It is shown that leakage current of SiC JBS rectifier may raise as much as five orders of magnitude during 50 h of constant reverse blocking mode [43].

2.4.2. Simulations

Compared to experimental results, there are very few simulation results published. Simulations have been done for analysing dependence of device parameters on Schottky contact area and *pn* junction area relations and grids [39].

Different Schottky metals, size and spacing of implanted regions and thickness and dopant

density of drift region have been altered using simulator *MINIMOS-NT* [44].

Some of authors have been dealing also with inner processes of Si JBS device. Additionally to *I-V* characteristics and switching characteristics there have been simulated minority carrier concentration profiles along the drift region of the device with simulation software *ATLAS* and *MIXEDMOD* by Silvaco. Minority carrier concentration is important in switching process of the device. In same work also electric field strength distribution in JBS device is shown to explain why JBS device has better reverse characteristics than bare Schottky device [45]. Electric field strength has great importance for understanding reverse leakage decreasing of rectifier. Electric field strength is studied also in TMBS structures using *MEDICI* simulator [25].

Another aspect of using SiC devices is lack of models for circuit level simulator. Some steps toward improving the situation are done by developing such models for *Saber* circuit simulator. Both MPS and *pin* models are developed and verified [46].

3. Simulation model

3.1. Shockley-Roosbroeck system

Traditional simulation software uses Shockley-Roosbroeck system [47] containing Poisson's equation, electron and hole continuity equations and current equations:

$$\varepsilon_0 \varepsilon_r \operatorname{div}\vec{E} = q\left(p - n + N_D^+ - N_A^-\right) \tag{3}$$

$$\operatorname{div}\vec{j}_n = +q\left(R - G + \frac{\partial n}{\partial t}\right) \tag{4}$$

$$\operatorname{div}\vec{j}_p = -q\left(R - G + \frac{\partial p}{\partial t}\right) \tag{5}$$

$$\vec{j}_n = q\mu_n n\vec{E} + qD_n \operatorname{grad} n \tag{6}$$

$$\vec{j}_p = q\mu_p p\vec{E} - qD_p \operatorname{grad} p\ , \tag{7}$$

where

ε_0 -	dielectric constant of vacuum,
ε_r -	relative dielectric permittivity of semiconductor,
N_D^+ -	ionized donor doping concentration,
N_A^- -	ionized acceptor doping concentration,
R -	electron-hole pairs recombination rate,
G -	electron-hole pairs generation rate,
μ_n -	mobility of electrons,
D_n -	diffusivity of electrons,
μ_p -	mobility of holes,
D_p -	diffusivity of holes.

The Poisson's equation (3) relates the changes of electric field strength vector to local space charge density. The continuity equations (4) and (5) represent carrier concentration balances due to recombination rates and difference of in- and out flowing currents. The current equations (6) and (7) represent current densities as sums of drift and diffusion currents.

Additionally to formulas (3)- (7), Maxwell's total current equation is used:

$$\vec{j} = \vec{j}_n + \vec{j}_p + \varepsilon_r \varepsilon_0 \frac{\partial \vec{E}}{\partial t}. \tag{8}$$

Equations (6) and (7) are not enough to take into account Electron Hole Scattering (EHS) effect. Instead, following equations are used in *SIC-DYNAMIT-2DT* package [47]:

$$\begin{aligned} \vec{j}_n &= \beta_{nn}\vec{J}_{n0} - \beta_{np}\vec{J}_{p0} \\ \vec{j}_p &= \beta_{pp}\vec{J}_{p0} - \beta_{pn}\vec{J}_{n0} \end{aligned}\ , \tag{9}$$

where $\vec{J}_{n0}$ and $\vec{J}_{p0}$ are EHS-free currents and β-multipliers are dimensionless.

There are also several supporting relations used. For example relation between electric field strength and electrostatic potential:

$$\vec{E} = -\mathrm{grad}\varphi , \qquad (10)$$

Einstein relations between mobilities and diffusion coefficients:

$$D_{n,p} = \frac{k_B T}{q} \mu_{n,p} , \qquad (11)$$

where k_B is Boltzmann constant.

Additional coefficients are used for high electron and hole concentrations. Also mobilities dependence of doping concentration, temperature, electrical field, electron and hole concentrations are used.

For simulation, boundary and initial conditions must be described to complete the model. Also external circuits formulas are needed. Boundary conditions can be:

- ohmic contacts,
- rectifying metal-semiconductor (Schottky) contacts,
- semiconductor-dielectric interface,
- neutral interface with zero fields/currents in normal direction (symmetry based cut off plane).

3.2. Boundary conditions

As mentioned above, there can be several boundary conditions. Here are the models of those.

3.2.1. Ohmic contact

At an ideal ohmic contact, carrier concentration is specified by the thermal equilibrium values. Charge neutrality

$$p - n + N_d - N_a = 0 \qquad (12)$$

and infinite recombination velocity are assumed.

For electrostatic potential, boundary conditions are defined by thermal equilibrium electrostatic potential and external voltage:

$$\varphi = \varphi_0 - U . \qquad (13)$$

φ_0 is related to other variables using Boltzmann's statistics:

$$n = n_i e^{\frac{+\varphi_0 q}{k_B T}} , p = n_i e^{\frac{-\varphi_0 q}{k_B T}} . \qquad (14)$$

3.2.2. Schottky model

There are several mechanisms of current transport in Schottky barrier: thermionic emission of carriers across the Schottky barrier, the quantum-mechanical tunnelling through the barrier, the recombination current and diffusion of carriers from the semiconductor into metal. Some of those

can be neglected. The tunnelling current of low-doped epitaxial regions can be neglected, as we are interested in high voltage situations. Recombination current is of very low importance and can also be neglected. The diffusion current is important only in high barriers. The only leftover is thermionic emission current transport mechanism. Boundary conditions of Schottky contact for electrons and holes can be written as:

$$J_n = A_n^{**} T^2 \frac{n - n_0}{N_c}, \tag{15}$$

$$J_p = A_p^{**} T^2 \frac{p - p_0}{N_v}, \tag{16}$$

where A_n^{**} and A_p^{**} are the effective Richardson constants for electrons and holes, n, p and n_0, p_0 are the actual and zero bias surface concentrations of electrons and holes, N_c and N_v are the effective density of states in the conduction and valence bands. The surface electrostatic potential is fixed by the Schottky barrier to be for p-type semiconductor:

$$\varphi = \varphi_{Bn} - \frac{E_C - E_F}{q} - U \tag{17}$$

and for n-type semiconductor:

$$\varphi = \varphi_{Bp} + \frac{E_C - E_F}{q} - \frac{E_g}{q} - U\ . \tag{18}$$

Schottky barrier depends also on applied electrical field due to image force:

$$\Delta\varphi = \sqrt{\frac{qE}{4\pi\varepsilon_r\varepsilon_0}} \tag{19}$$

where E is the electric field strength across the metal-semiconductor interface.

3.3. Numerical solution technique

In ideal case analytical modelling gives very well usable and accurate results, but unfortunately due to complexity of Shockley-Roosbroeck system many simplifications need to be made. Those simplifications shrink very much the usability of analytical models resulting only very special cases when it is useful.

Numerical solution techniques, in contrary, can give results without simplifications but have its limitations in no easily reversible relations between input and output parameters relations, long calculation times, difficulty of numeric algorithms development and so on.

Numerical approach consists of three steps:

Area under simulation has to be divided into finite number of sub domains. Sub domains must cover the entire domain and sub domains may not overlap with each other.

Differential equations have to be approximated by algebraic equations in each sub domain. Those algebraic equations have to involve only values of continuous dependent variables at discrete points in the domain.

The system of those equations has to be solved.

There are two basic methods: finite differences method and finite elements method [48].

In finite differences method the simulated domain is divided into sub domains by mesh, which lines are parallel to coordinate axes. For each mesh point an algebraic equation has to be derived from differential equation. In classical case the mesh lines continue from one boundary of the

device to other. Generally there are small regions in semiconductor devices that need to be divided into very small sub domains to get acceptable accuracy. This results also in unnecessary small sub domains in regions of no such interest, wasting computer resources. Finite boxes method is a variant of finite difference method. The difference from classic finite difference method is that in finite boxes method mesh lines can start and end not only in domain boundaries but also in boundaries of sub domains (but not two neighbouring mesh lines terminating in nearest neighbouring points).

In finite elements method the mesh is not restricted to be parallel to axes. In finite elements method sub domains can be with any shape. Most common is the use of triangular shape. Sub domains with different shapes can also be used together.

3.3.1. Solving system of non linear algebraic equations

The equations obtained from finite difference or finite elements method has to be solved. This can be done by using iterative methods such as Gummel's iterative method or Newton's iterative method.

Gummel's method relays on solving Poisson's equation and continuity equations separately. Nonlinear Poisson's equation is solved first. Obtained potential is substituted into the continuity equations. Continuity equations become linear and can be solved directly. The result is substituted back into Poisson's equations until convergence is reached. Gummel iteration process step does not need much computational power but convergence can take long time or sometimes can solution also be missed.

Newtons method relays on solving Poisson's equation and continuity equations together. This method has to solve all three equations in one iteration step. This results in much bigger computational cost (typically 20 times bigger) because of inversion of matrix, which is 3 times bigger in both dimensions compared to Gummel's method. Contrary to Gummel's method, convergence is usually fast if initial condition is close to the solution. Both methods can also be composed in such a way that Gummel's method is first used for some iterations to find good start point for Newton's method and then Newton's method can be used to get final solution [49].

3.3.2. History

1964 - The history of numerical simulations started when Gummel proposed successive iteration scheme (separately iterating Poisson's equation and continuity equations).
1967 - Coupled solution of equations (Newton's method) was used. This method is more computation resource demanding but also avoided convergence problems.
1967 - Scharfetter-Gummel current density discretization method was used first time. This method allows obtaining acceptable results even on very rough meshes. This method is used in most numerical device simulators up to now.
1968 - The first 2D simulations were published by Loeb et al. and Schroeder and Muller.
1974 - The use of finite elements discretization technique was first time published.
1974 - The first non-isothermal simulations were done.
1980 - The first 3D-simulations were done.
1990-s - Commercial device simulators appeared.

This short historical overview is based on dates available in [47].

3.4. Software

Simulations have been done using *SiC-DYNAMIT-2DT* simulation package. This package is a numerical solver using two-dimensional set of Poisson´ s equation and the electron and hole carrier continuity equation in semiconductor. It involves also heat flow equation and different external circuit equations can be defined.

3.4.1. History of SiC-DYNAMIT-2DT

Shortly the history of development of 2D device simulators at the Department of Electronics is the following:

1970-s -	The prehistory of *SiC-DYNAMIT-2DT* started in 1976 when Dr. Boris Freydin began to develop the numerical device simulators at the Department of Electronics, TUT.
1980 -	After convergence problems with Gummel successive solution algorithms Dr. A. Udal started to develop Newton method based coupled solution techniques including all Shockley-Roosbroeck equations and external circuit equations into common Jacobian matrix.
1982 -	External circuit equations were introduced (main and gate electrode circuit).
1987-1989 -	First non isothermal 2D transient processes calculations of silicon power GTO-s and bipolar transistors; also investigation of current squeezing process in GTO thyristors (program *DYNAMIT-2D* with rather restricted device geometry and grid).
1990-1993 -	Development of a commercial silicon software *GIGA-2D* in Silvaco International (Santa Clara, USA); also investigation of ESD (Electrostatic Discharge) break down processes (program with open geometry and list of semiconductors, including separate open geometry of electro thermal task).
1993-1996 -	Development and application of *Si-DYNAMIT-2DT* for a ultra-fast-turn-on silicon double thyristor design.
1994-1995 -	Development of silicon carbide version of program *SiC-DYNAMIT-2DT* including possibility of specification of anisotropic physical parameters.
2002 -	Added possibility of SiC Schottky contacts specification.
2004 -	Added the incomplete ionization sub models (deep dopant levels) and possibilities to simulate C (diamond), GaN, GaAs and other material devices.

3.4.2. Physical models

The physical models used in device equations are:

- mobility models,
- Shockley-Read-Hall (SRH) and Auger recombination models,
- heavy doping band-gap narrowing model.

Temperature dependences of basic electro physical parameters are incorporated into models.

3.4.3. Mesh

SiC-DYNAMIT-2DT uses classical finite difference method and rectangular mesh. In this work, mesh is defined by hand.

4. Results and discussion

4.1. The device under study

The simulations were performed on 6H-SiC and 4H-SiC JBS structures (Fig. 10), which dimensions and parameters were changed to study the influence of those changes to electrical parameters and characteristics of the device. The upper left corner is considered as 0 point for both x and y dimensions.

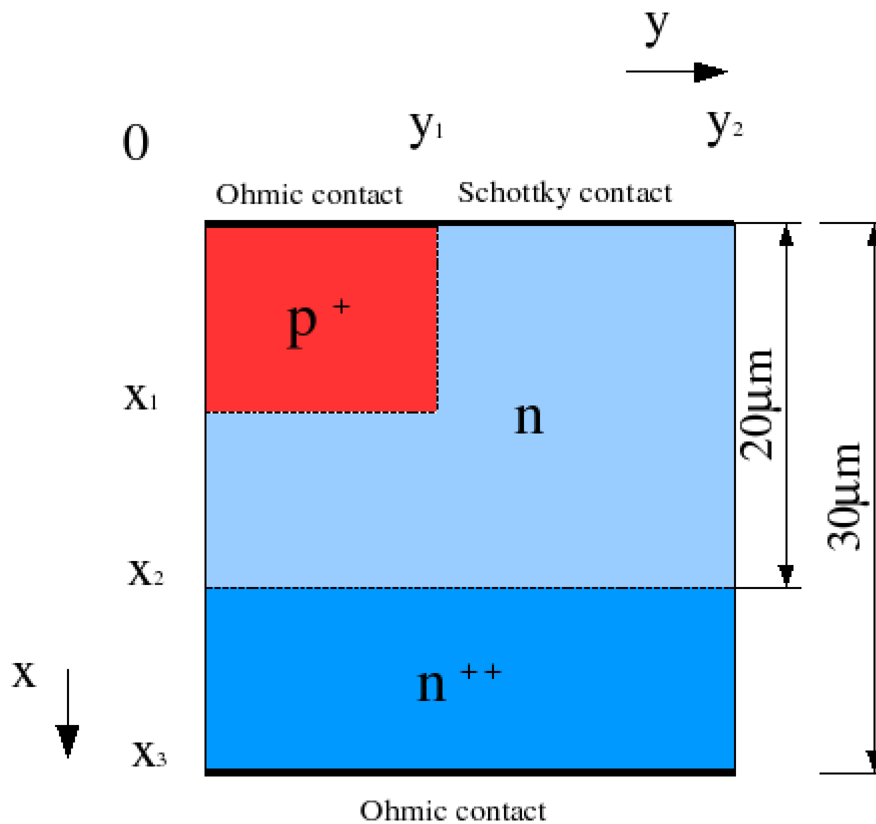

Figure 10: The device under study

The parameters of device are:

width of the device (y_2) 1...15 µm,

width of p^+ area (y_1) 0.25...5 µm, depth (x_1) 1...20 µm and acceptor doping concentration 5×10^{16} cm-^{3},

epitaxial layer (*n* area) depth (x_2) 20 µm with donor doping concentration 1×10^{15}...4×10^{15} cm^{-3},

part of the substrate (n^{++} area) depth (x_3-x_2) 10 µm with donor doping concentration 1×10^{19} cm^{-3},

Schottky contact metal work function 5.1...5.7 V,

temperature 300...900 K,

the area of the device was chosen to be always 1 cm^2, to get current and current density equal,

also complementary *p* semiconductor based device with previously described data was simulated.
Avalanche ionization coefficients of SiC semiconductor were taken to be [50] for 4H-SiC:
$\alpha_{n\infty}$=2.51x10^7 $\alpha_{p\infty}$=4.07x10^6 β_n=2.76x10^7 β_p=1.30x10^7
and for 6H-SiC:
$\alpha_{n\infty}$=5.75x10^8 $\alpha_{p\infty}$=3.98x10^6 β_n=5.33x10^7 β_p=1.5x10^7.

4.2. Explanations to simulation results presented

As most of simulation results are presented in same way, an explanation for most of the following figures is given here.

Forward characteristic. Increasing forward voltage from 0 to 5 V is applied on device terminals and current flowing through the device is registered.

Reverse characteristic. Reverse voltage started from 0 is increased until device reverse current achieves 0.01 A. This happens normally near reverse break down voltage. Current flowing through the device is registered.

Electric field strength distribution. Electric field strength picture is taken at the edge of simulated piece, under Schottky contact (at $y=y_2$, $x=0...x_3$ in Fig. 10) at reverse voltage 1000 V. Electric field strength under Schottky contact is most important due to the Schottky contact high leakage current. The named edge is at the middle of the Schottky contact in whole device, as the simulated piece is just a part of the whole device and both left and right boundaries of the simulated piece are mirror surfaces. The reverse voltage of 1000 V is chosen for comparison of electric field strength on devices with different reverse break down voltage as all the devices reverse break down voltage was over 1000 V.

Turn-off characteristic. Turn-off characteristics are taken on device switching from 100 A forward current to 99.9 V reverse voltage with 100 V applied reverse voltage source connected to device through 0.01 Ω current limiting resistor.

4.3. Choosing geometric dimensions of the JBS device

First task in parametric simulations is dimensioning of the JBS device. To achieve this, the width and depth of the emitter of the device are altered simultaneously and different input parameter sets are chosen for simulations. Relevant simulation results are compared to find optimum combination for power application: device with low power losses, high reverse breakdown voltage, and fast turn-off characteristic.

Chosen input parameters are:
1. width of the *pn* part of the device (x_2 in Fig. 10): 0.25-1 μm (1/6-2/3 of the whole area),
2. depth of the emitter of the *pn* part of the device (x_1 in Fig. 10): 1-15 μm.

Other parameters are fixed.

Four different simulation results are compared:
1. forward characteristics,
2. reverse characteristics,
3. electric field strength distribution under reverse bias,
4. turn-off characteristics.

4.3.1. Forward characteristics

It is clearly seen from forward characteristics (Fig. 11) that devices with wider emitter have worse forward characteristics, especially in region of low voltages. Closer look at currents in case of wide

emitter at 0.3 V forward voltage is taken at Fig. 12 (current density x component), 13 (current density y component), and 14 (electron concentration). Current density x component Fig. (12) reveals that most of the current flows through *pn* part of the device. There is a little current swing towards Schottky part of the device under emitter region (dark stripe around x=10...11 μm in Fig. 13), but in few micrometers above it, even bigger current swing takes place in opposite direction (high peak around x=8...9 μm in Fig. 13). The fact what Schottky part of the device is not conducting can be explained by lack of free electrons under Schottky contact (Fig. 14). The length of Schottky contact area (0.5 μm) is small enough that built-in voltage of *pn* junction forms depletion region under whole Schottky device and eliminates most of the free electrons. Schottky device as majority carrier device functioning is disturbed. The influence to the whole device is higher at low voltages because JBS forward characteristics at low forward voltages are mostly defined by Schottky area. On higher voltages the current flows through both Schottky and *pn* part. The influence of Schottky part weakens. In case of wider Schottky area there is no lack of electrons any more (Fig. 15). Majority of current flows through Schottky contact at 0.3 V forward voltage (Fig. 16). Current swing to Schottky part of the device takes place below emitter area (dark area around x=11 μm in Fig. 17). There is another, opposite direction current redistribution just below the surface (light area around x=10...1 μm in Fig. 17). The concentration of electrons is higher in this area resulting in lower resistance and allowing easy current redistribution in horizontal direction under Schottky barrier. The current density distribution of JBS device at 5 V forward voltage is shown in Fig. 18 (x component) and Fig. 19 (y component). As seen from figures both pn and Schottky part of the device have quite high current density (lighter areas in Fig. 18). The low x direction current density region under Schottky contact near emitter (darker areas in Fig. 18) can be explained by lack of electrons in this area. Current density y distribution figure reveals that current swings away from *pn* part of the device under emitter and also in few micrometers region under Schottky contact (dark areas in Fig. 19). There is a little region above emitter lower end where the current flows towards pn part of the device (lighter areas in Fig. 19).

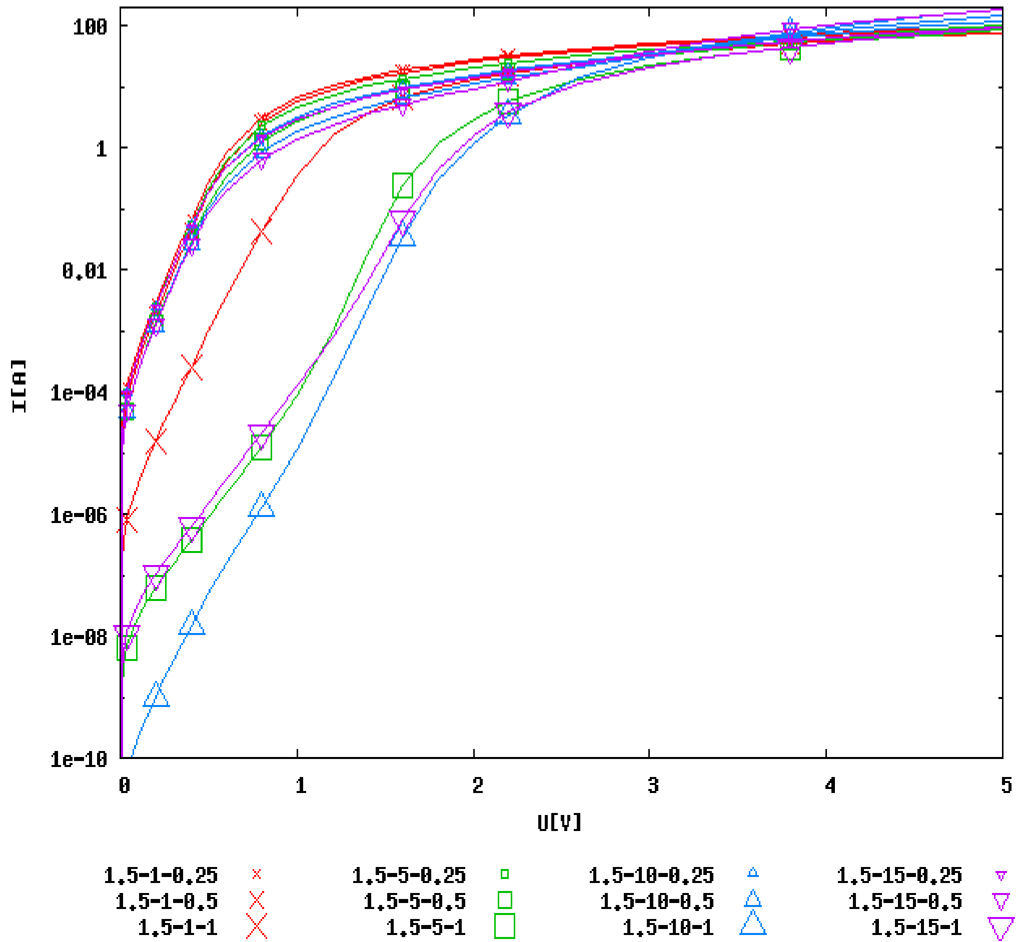

Figure 11: Forward I-V characteristics of JBS devices with different emitter area deepness and width. Legend shows width of the whole structure, deepness of emitter, width of the emitter in µm

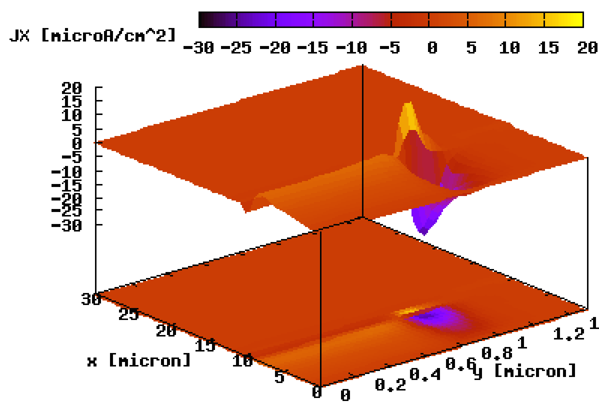

Figure 12: Current density x component in device "1.5-10-1" at 0.3 V forward voltage. Current density direction is opposite to x axis direction

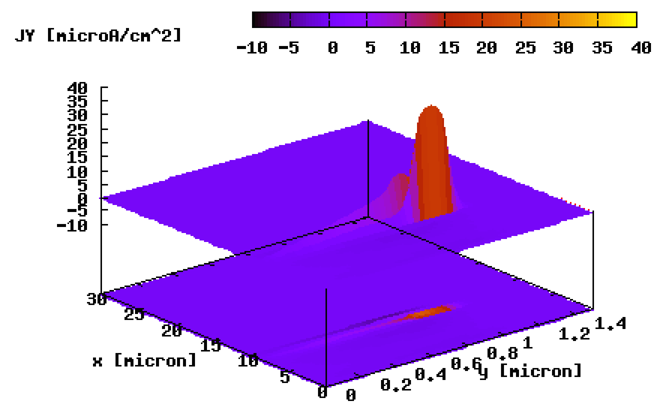

Figure 13: Current density y component in device "1.5-10-1" at 0.3V forward voltage. Current density direction is opposite to x axis direction

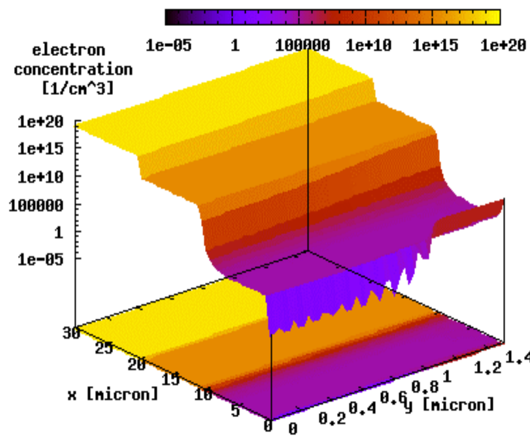

Figure 14: Electron concentration in device "1.5-10-1" at 0.3 V forward voltage

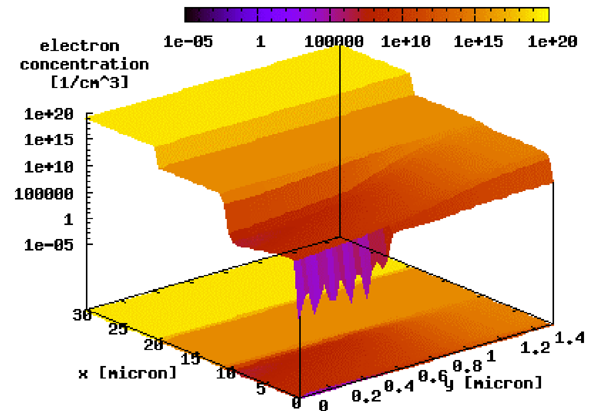

Figure 15: Electron concentration in device "1.5-10-0.5" at 0.3 V forward voltage

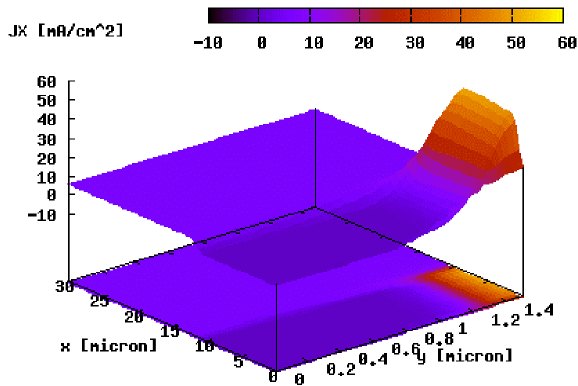

Figure 15: Current density x component in device "1.5-10-0.5" at 0.3 V forward voltage. Current density direction is opposite to x axis direction

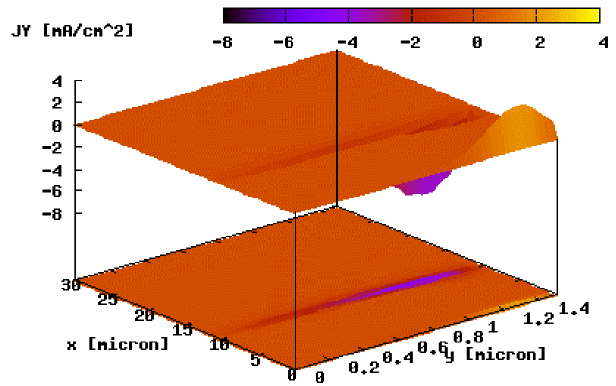

Figure 17: Current density y component in device "1.5-10-0.5" at 0.3 V forward voltage. Current density direction is opposite to x axis direction

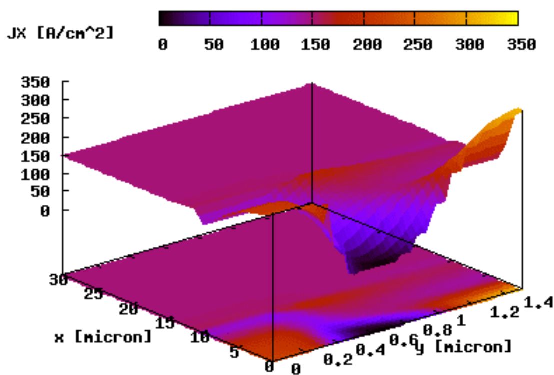

Figure 18: Current density x component in device "1.5-10-0.5" at 5 V forward voltage. Current density direction is opposite to x axis direction

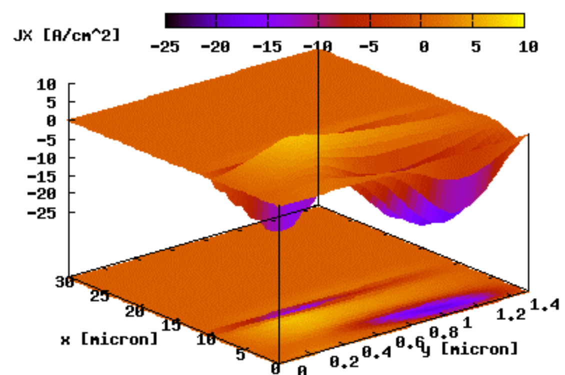

Figure 16: Current density y component in device "1.5-10-0.5" at 5 V forward voltage. Current density direction is opposite to x axis direction

4.3.2. Reverse characteristics

As seen from reverse characteristics (Fig. 20), the difference is not big if we exclude characteristics of 1 μm emitter area width devices. Devices with narrow emitter area are not blocking Schottky reverse leakage current. Reverse current of the device is flowing mostly through the Schottky part (lighter area in Fig. 21). Reverse leakage current crowding to Schottky part is taking place around lower part of epitaxial layer (darker area in Fig. 22) and current is redistributing under Schottky contact (lighter area in Fig. 22). Devices with wide emitter are able to block effectively Schottky leakage current. In this case most of reverse leakage current flows through *pn* part of the device (lighter area on Fig 23).

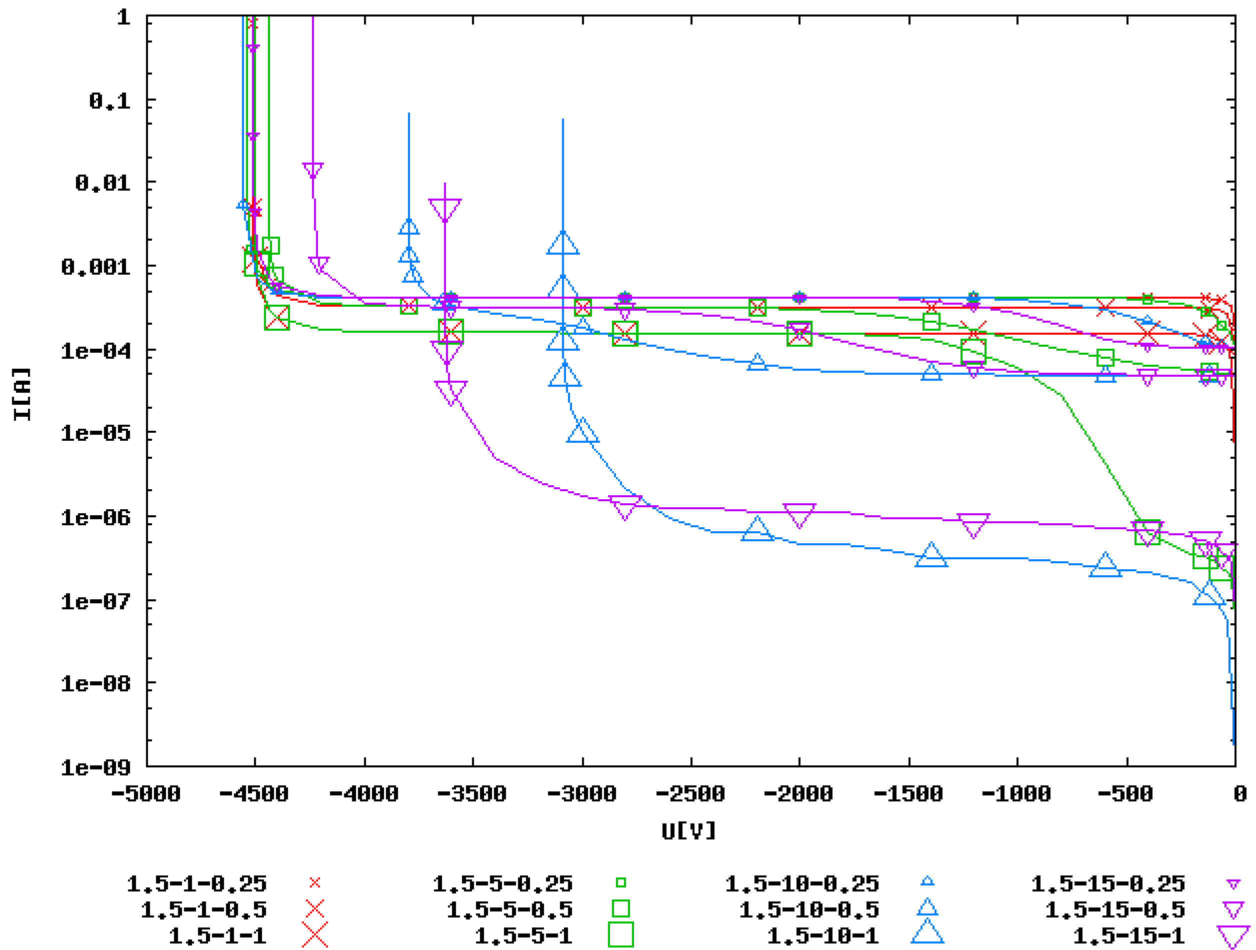

Figure 17: Reverse I-V characteristics of JBS devices with different p doping area deepness and width. Legend shows width of the whole structure, deepness of p doping area, width of the p doping area in μm

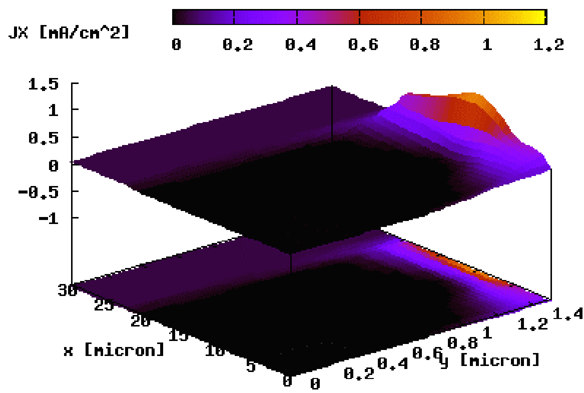

Figure 18: Reverse current density x component in device "1.5-10-0.5" at 1000 V reverse voltage. Current density direction is opposite to x axis direction

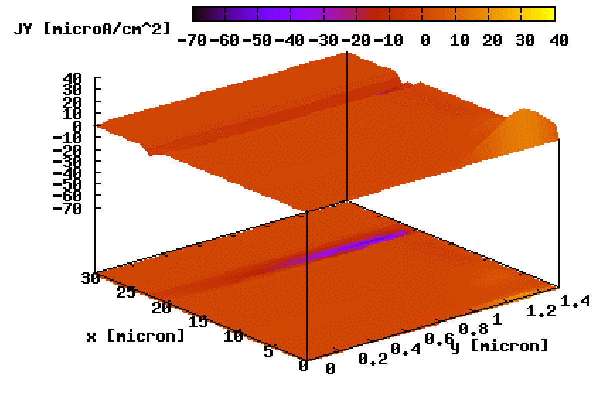

Figure 19: Reverse current density y component in device "1.5-10-0.5" at 1000 V reverse voltage. Current density direction is opposite to x axis direction

There exist two regions where reverse current swings to *pn* part of the device: lower part of epitaxial layer and middle of emitter (lighter areas in Fig. 24). Some of the current swings back to Schottky part of the device in upper half of the emitter (darker areas in Fig. 24). This behaviour causes also current peak in emitter (Fig. 23).

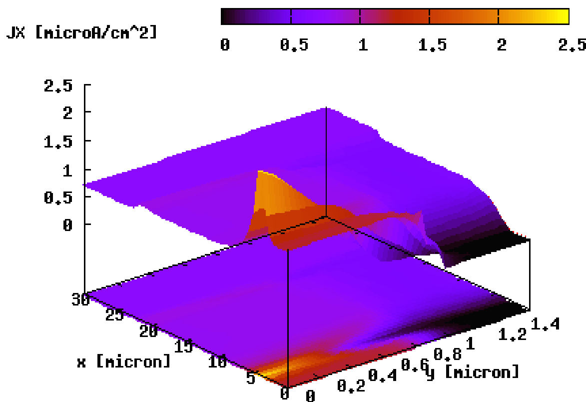

Figure 23: Reverse current density x component in device "1.5-10-1" at 1000 V reverse voltage. Current density direction is opposite to x axis direction

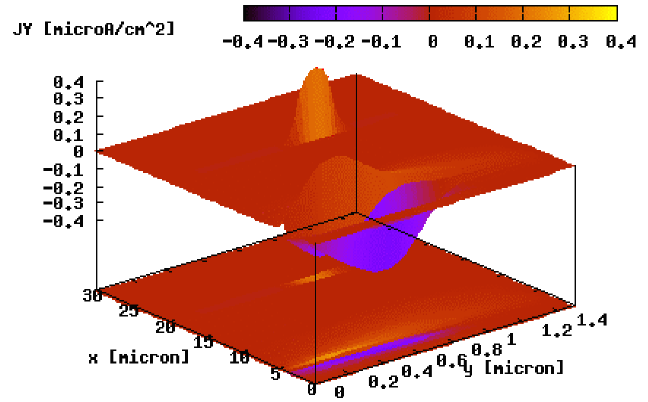

Figure 24: Reverse current density y component in device "1.5-10-1" at 1000 V reverse voltage. Current density direction is opposite to x axis direction

4.3.3. Electric field strength distribution under reverse bias

More information from the point of view of choosing the initial configuration than reverse current characteristics has electric field strength distribution. There are two aspects to consider:

1. The maximum electric field strength inside the device should not be too high, due to limited ability of semiconductor to handle high electric field strengths.

2. The electric field strength under contact should be as low as possible to reduce the effect of Schottky barrier lowering in one hand. Lower electric field strength near the surface means also fewer problems in passivation of the device on another hand. The second point should be

considered even more important as device passivation has great importance, especially in case of SiC, where electric field strengths reach much higher values than in case of Si.

The worst case can be considered from the solution where emitter depth is small (Fig. 25). In this case the electric field strength distribution in device under Schottky contact matches with the Schottky diode electric field strength distribution: field is the highest under the contact and lowers linearly over epitaxial layer until the substrate. This distribution has quite high maximum electric field strength and what worse, electric field strength under contact is close to its maximum value.

Electric field distribution in case of device with 10 µm deep and 0.5 µm wide emitter is shown in Fig. 26. Electric field distribution is quite alike both in Schottky and *pn* part of the device. Electric field strength maximum is through all of the device below depth of the emitter (around x=11 µm).

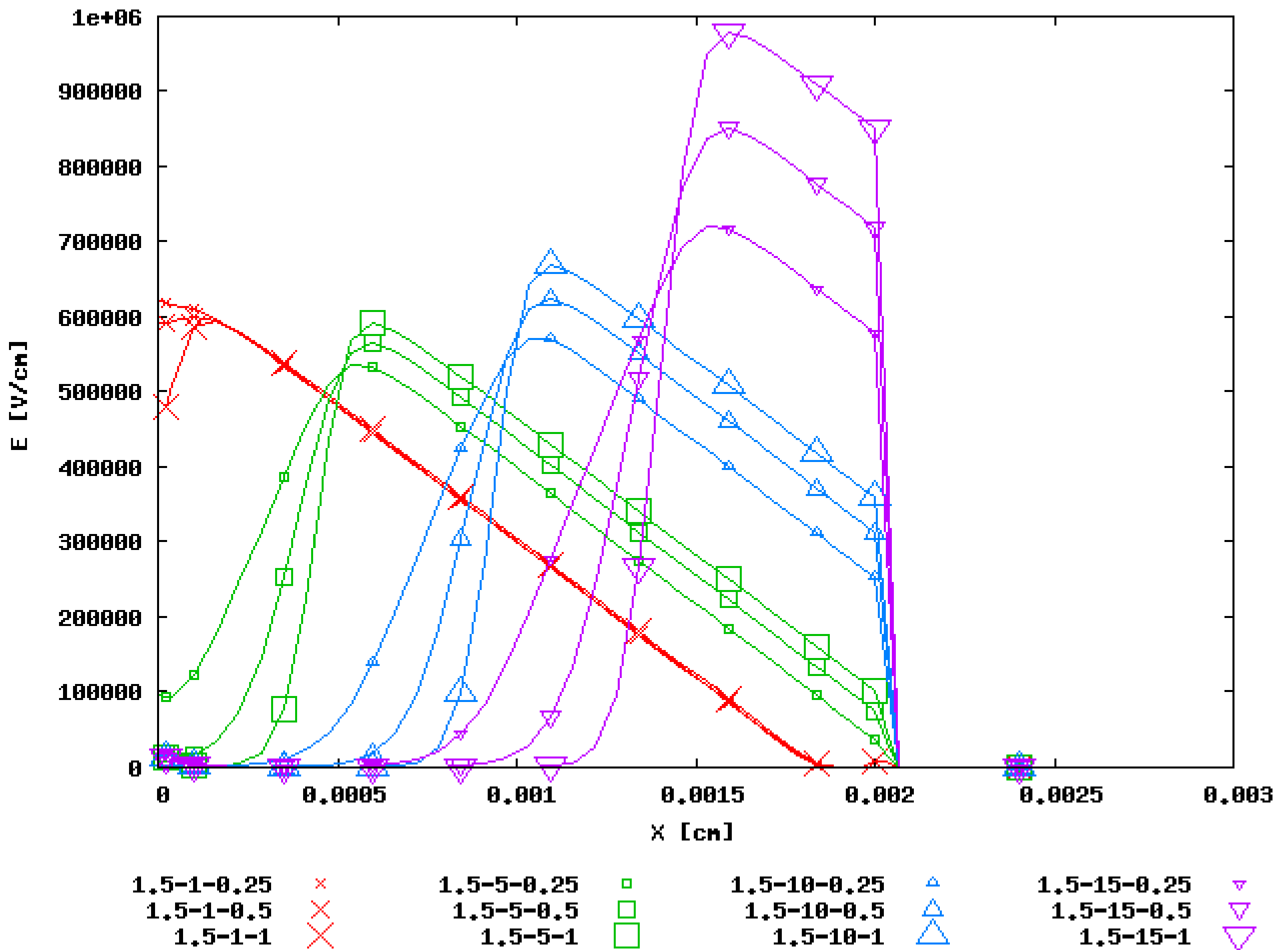

Figure 20: Electric field strength distribution characteristics under Schottky contact of JBS devices with different emitter deepness and width. Legend shows width of the whole structure, deepness of emitter, width of the emitter in µm

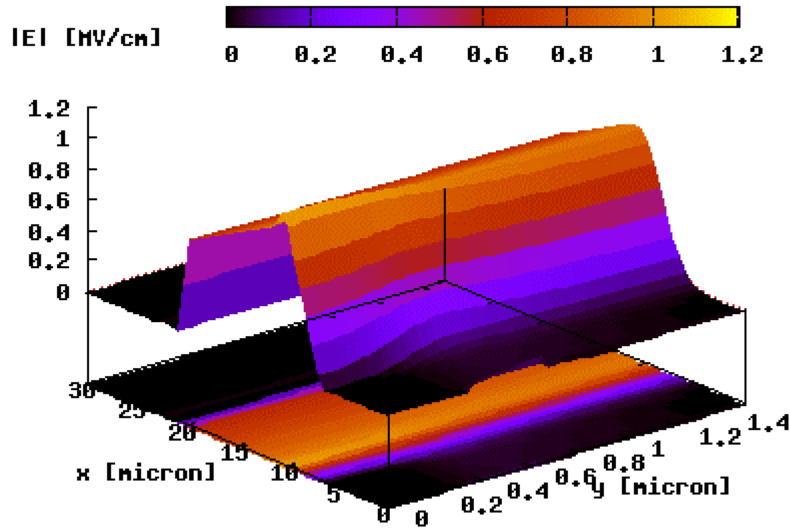

Figure 21: Electric field distribution at reverse voltage 1000 V in case of device "1.5-10-0.5"

4.3.4. Turn-off characteristics

As seen from turn-off characteristics Fig. 27, devices with lowest depth of emitter have worse parameters. The region where minority carriers are located and the number of those can explain this. Deep emitter area causes also large number and area of majority carriers. Hole distribution at 5 V forward voltage in case of "1.5-10-0.5" device is shown in Fig. 30. Lighter area shows higher concentration of holes. Hole distribution at 5 V forward voltage in case of "1.5-1-0.5" device is shown in Fig. 31. As seen from those two figures, the amount of holes needed to be carried out from device depends strongly on deepness of emitter. The amount of electrons needed to carry out during turn-off has high influence also on turn-off time and is the main reason in turn-off time dependence on emitter area dimensions.

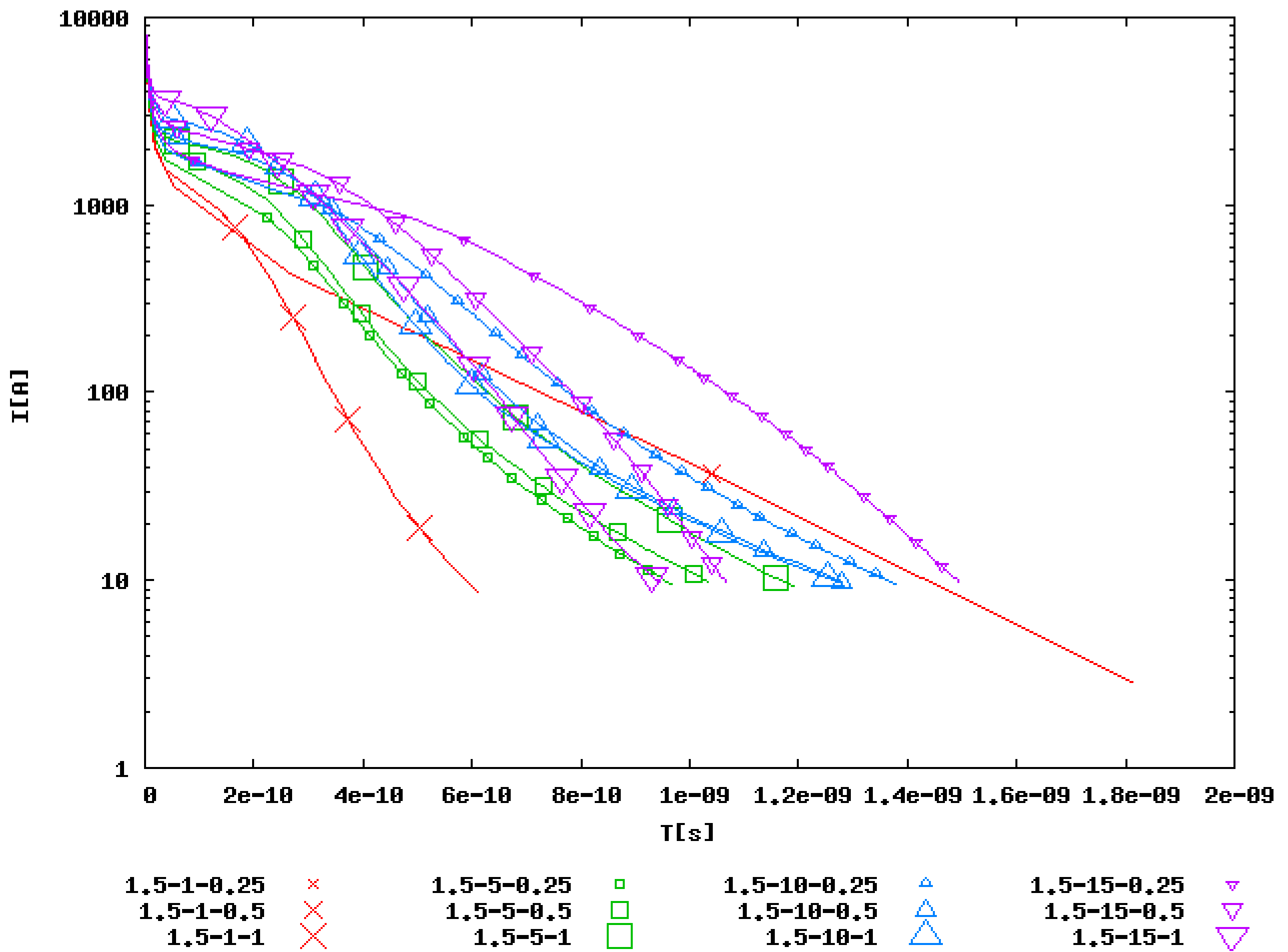

Figure 22: Turn-off current switching JBS from 100 A to -100 V with different emitter deepness and width. Legend shows width of the whole structure, deepness of emitter, width of the emitter in μm

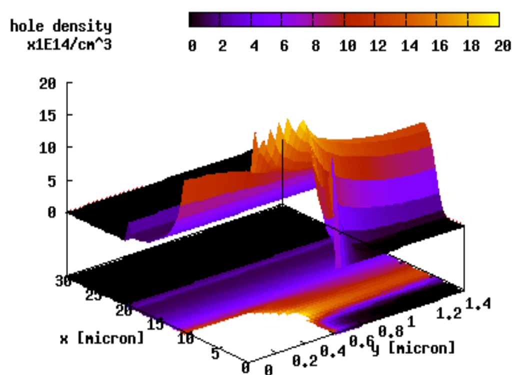

Figure 23: Hole density at 5 V forward voltage in case of "1.5-10-0.5" device. Emitter area hole concentration is out of the range and not shown

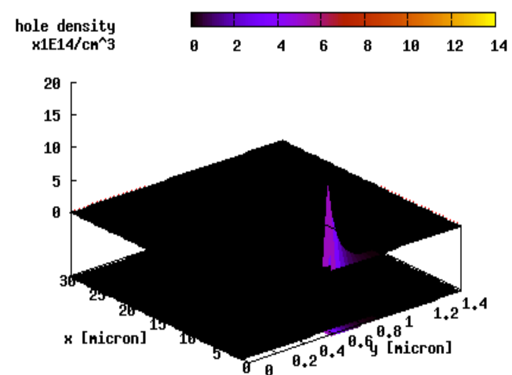

Figure 24: Hole concentration at 5V forward voltage in case of "1.5-1-0.5" device

4.3.5. Conclusions

The width of emitter. First, the small width of emitter prolongs the slope of turn-off characteristics. Second, the large width of emitter distorts forward characteristics. Therefore the width of emitter is chosen equal to 0.5 μm.

The depth of emitter. As electric field strength both under Schottky contact and in the bulk of semiconductor are low in case of average depth of emitter, the depth of emitter is chosen equal to 10 μm.

Similar simulations have been finished with 6H-SiC JBS device. Although different materials behave differently, the best results were obtained with the same geometric dimensions.

The basic dimensions of JBS device under study will be:

length of the whole device (y_2): 1.5 μm,

length of the emitter (y_1): 0.5 μm,

deepness of the emitter (x_1) 10 μm.

4.4. Parametric simulations

4.4.1. Material *type*: 6H-SiC versus 4H-SiC

Forward characteristics. 6H-SiC has higher currents at low voltages (below 0.4 V) than 4H-SiC and much lower currents at higher voltages (Fig. 30). Higher currents of 6H-SiC at low voltages can be explained by lower band gap of 6H-SiC than of 4H-SiC. This results in lower voltage drop on Schottky barrier of Schottky part of the device. Still, this influence is seen only on low voltages because the resistance of the 6H-SiC semiconductor is higher than of 4H-SiC due to much lower carrier mobility along the c axis in 6H-SiC.

Reverse characteristics. 6H-SiC based device has higher reverse current and higher break down voltage than 4H-SiC based (Fig. 31). Higher reverse current is caused by properties of Schottky contact. Schottky part of the device has higher leakage current in reverse voltage situation and it also determines the reverse current of the whole device. Lower reverse break down voltage is caused by lower break down electric field strength of 4H-SiC.

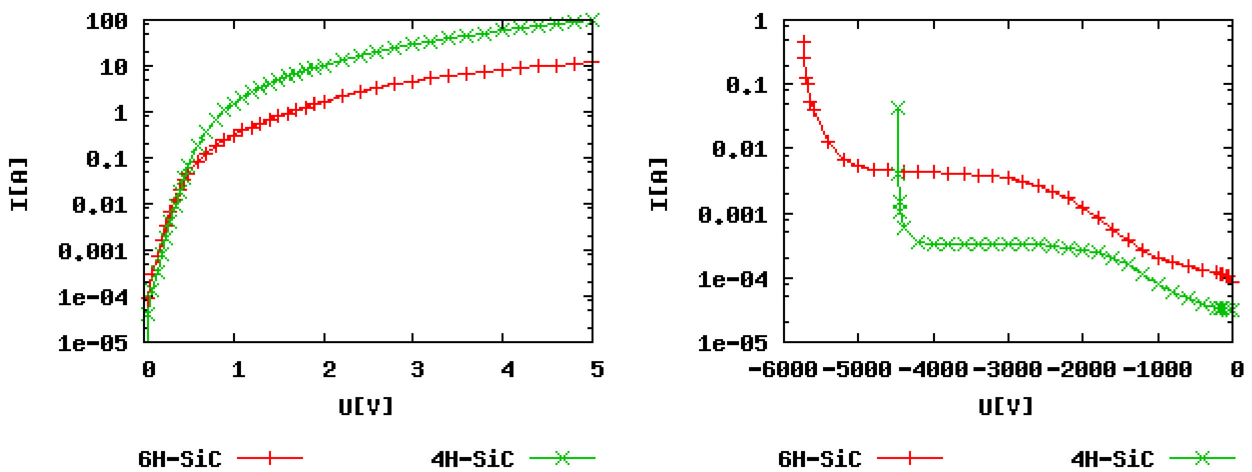

Figure 25: Forward I-V characteristics 6H-SiC vs 4H-SiC *Figure 26: Reverse I-V characteristics 6H-SiC vs 4H-SiC*

Electric field strength distribution. Electric field strength (Fig. 32) is the same for both materials. Although the polytype is different, the relative resistance profile of the device for both 6H and 4H-SiC is the same.

Turn-off characteristics. Turn-off characteristic (Fig. 33) show that 6H-SiC device is slower. The reason here is the lower mobility of carriers in 6H-SiC.

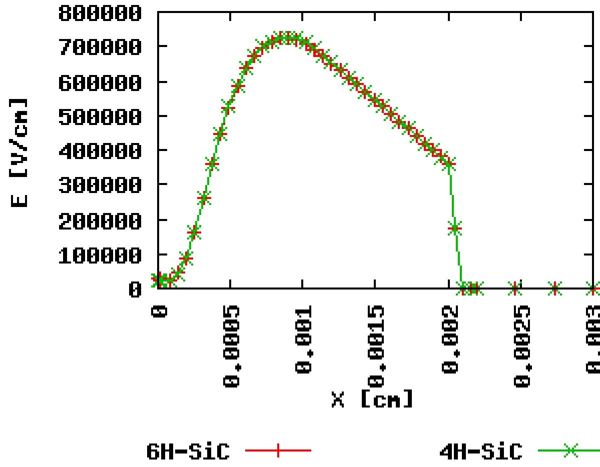

Figure 32: Electric field strength distribution 6H-SiC vs 4H-SiC

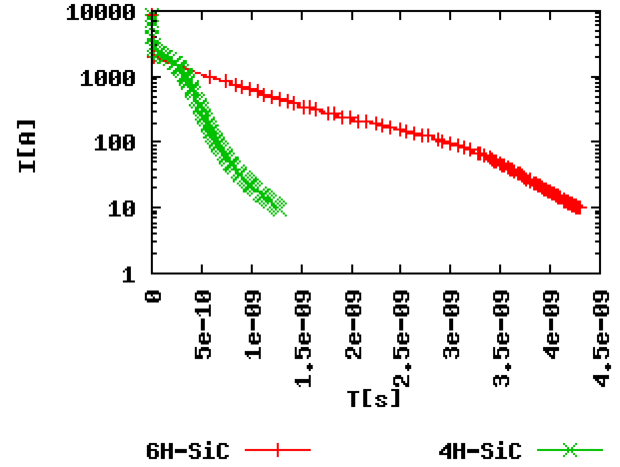

Figure 33: Turn-off I characteristics 6H-SiC vs 4H-SiC

Conclusion. Comparison of 4H-SiC and 6H-SiC shows that 4H-SiC is better in almost every aspect except its lower break down voltage. The main reason of better performance of 4H-SiC is the lower mobility of charge carriers in 6H-SiC resulting in higher resistance. The lower break down voltage is caused by lower break down electric field strength of 4H-SiC.

4.4.2. Epitaxial layer doping concentration variations

Forward characteristics. Epitaxial layer concentration has two different influences on forward characteristics (Fig. 34). Schottky junction characteristics dependence on epitaxial layer concentration causes difference in low voltage part of the forward characteristics. Epitaxial layer resistance change caused by its concentration change is seen on higher voltages. Device with higher concentration of epitaxial layer has lower resistance and thus bigger current at same voltage.

Reverse characteristics. On reverse bias the resistance of epitaxial layer is not important. On higher voltages reverse characteristics are identical (Fig. 35). There is a difference on lower reverse voltages. The concentration of electrons under Schottky contact is low on case of low epitaxial layer doping concentration at low reverse voltages and majority of current flows through *pn* part of the device. The level of electrons is much higher in case of higher epitaxial layer doping concentration and leakage current of Schottky part of the device determines reverse leakage of the device.

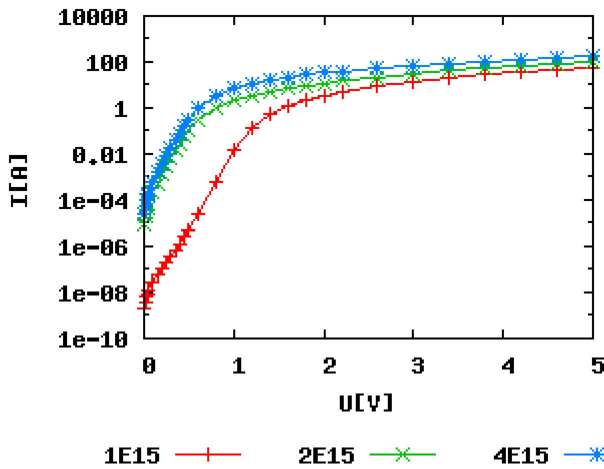

Figure 27: Forward characteristics dependence on epitaxial layer doping concentration

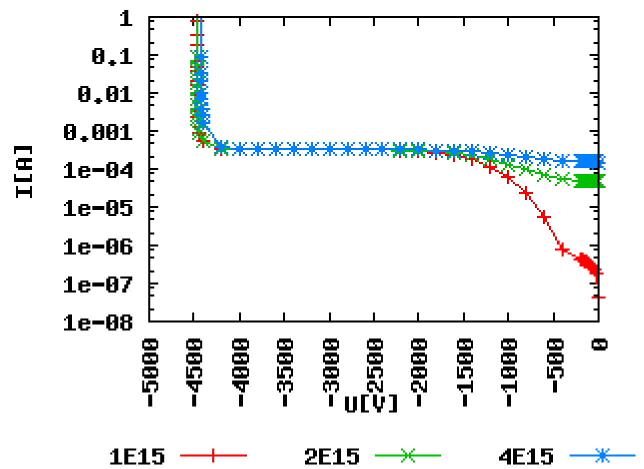

Figure 28: Reverse characteristics dependence on epitaxial layer doping concentration

Electric field strength distribution. Electric field strength distribution has strong dependence on epitaxial layer concentration (Fig. 36). The region where electric field strength distribution is most influenced by epitaxial layer concentration is below the emitter and above highly doped substrate. On higher epitaxial layer doping concentration the slope of electric field strength changing is sharper and on concentration more gentle. As the device has to handle the same voltage, electric field strength integral over the device must be the same. In case of sharper slope the distribution of electric field strength is more uneven causing lower electric field strength region in lower part of epitaxial layer but also higher electrical field strength region near lower part of emitter. The highest strength of electric field is important as device break down depends on it.

Turn-off current characteristics. Turn-off characteristics (Fig. 37) show that lower epitaxial layer doping concentration leads to slower devices. Devices with lower epitaxial layer doping concentration have higher resistance and this results in longer turn-off times.

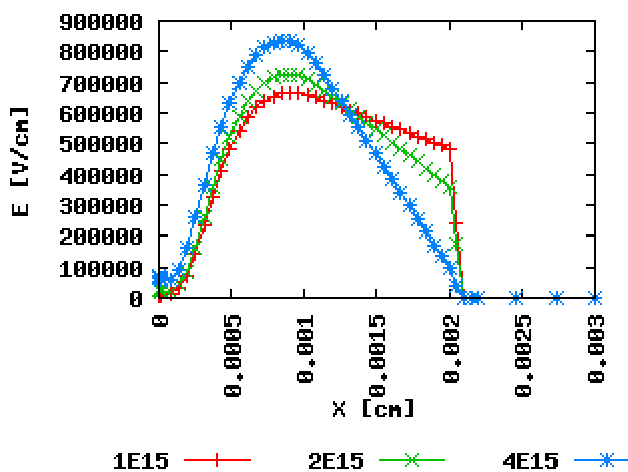

Figure 36: Electric field strength distribution dependence on epitaxial layer doping concentration

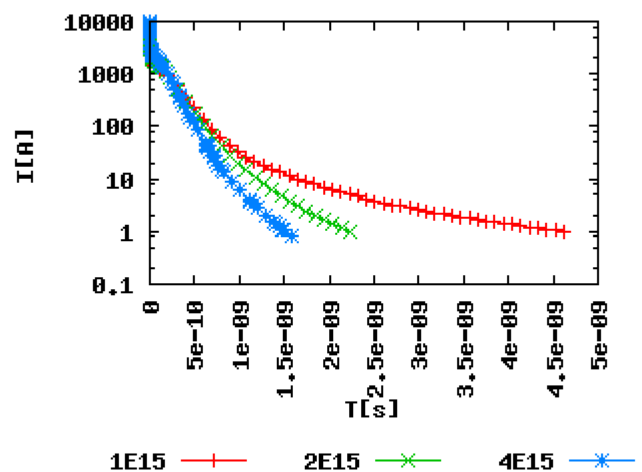

Figure 37: Turn-off I characteristics dependence on epitaxial layer doping concentration

Conclusion. The best doping concentration from three chosen is 2×10^{15} cm^{-3}.

4.4.3. Schottky contact metal work function variations

Forward characteristics. On forward characteristics figures it is seen that metal work function has influence in lower voltage region where characteristics are determined by Schottky part of the device (Fig. 38). Lower Schottky barrier height causes higher currents in low voltage region of characteristic. On higher voltages characteristics of Schottky part of the device are not so important any more and forward I-V characteristics are similar, depending mostly on behaviour of *pn* part of the device.

Reverse characteristics. The reverse characteristics of device depend strongly on contact metal work function, as leakage current of Schottky part of the device determines the whole device current leakage (Fig. 39). Lower Schottky contact metal work function causes higher leakage currents in Schottky part of the device and also in device as a whole.

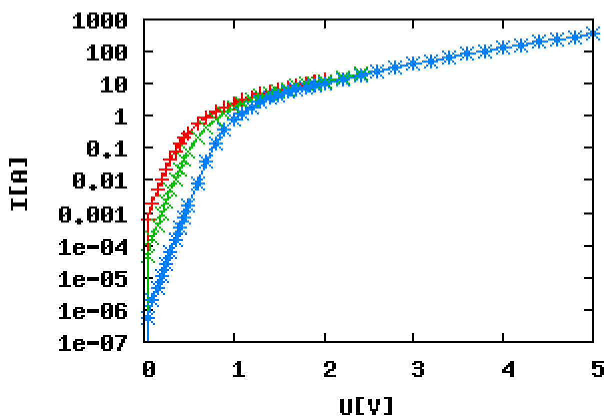

Figure 38: Forward characteristics dependence on contact metal work function

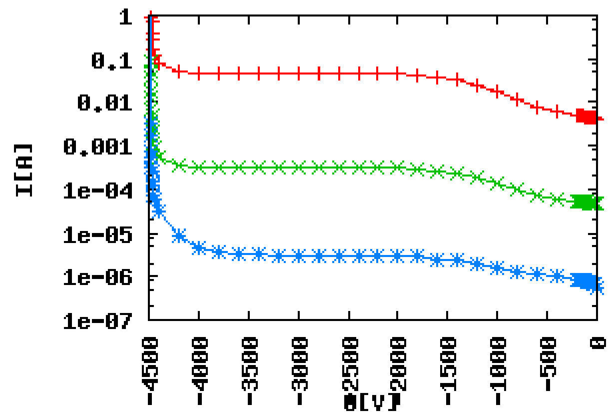

Figure 39: Reverse characteristics dependence on contact metal work function

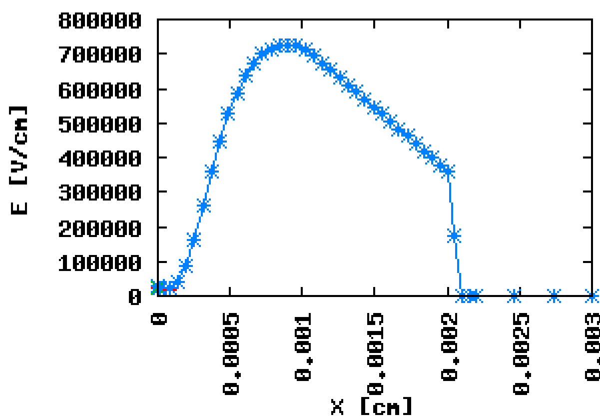

Figure 40: Electric field strength distribution dependence on contact metal work function.

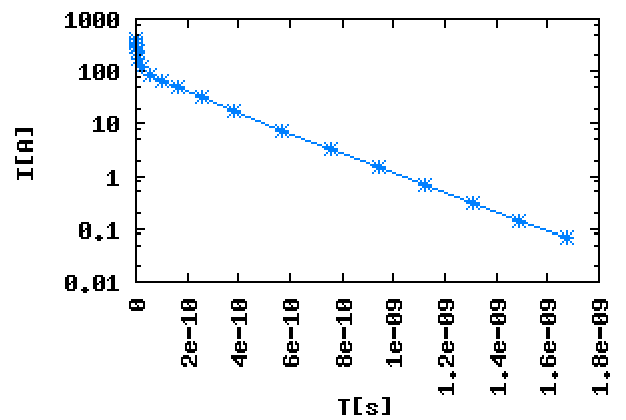

Figure 41: Turn-off I characteristics dependence on contact metal work function.

Electric field strength distribution. Electric field strength (Fig. 40) does not depend on Schottky contact metal work function value. Schottky contact barrier height has only small influence on electric field just below Schottky contact.

Turn-off characteristics. Turn-off characteristics (Fig. 41) do not depend on contact metal work function value. The distribution of currents in reverse voltage situation is the same for all three chosen Schottky barrier work function values. Therefore also turn-off characteristics do not depend on it.

Conclusion. From three chosen metal work function values the best seems to be 5.4 eV. Reverse leakage in case of 5.1 eV is quite high and causes already noticeable device heating at high reverse voltages.

4.4.4. Device dimensions

Forward characteristics. Device characteristics depend not only on relation of *pn* and Schottky part of the device, but also on their absolute dimensions. Here are 4 different *pn* and Schottky dimensions simulated, leaving relation of Schottky to *pn* diode's always the same, 3. On forward characteristics graph (Fig. 42) the device with smallest measure has much lower current. The reason is screening of Schottky part of the device by *pn* part the same way as it happens in reverse voltage situation. This is possible due to small measure of Schottky part (0.66 µm). As a result, *pn* part of the device defines the current at low voltages (Fig. 44).

Reverse characteristics. The reverse characteristics (Fig. 43) are not much different except in case of smallest Schottky+*pn* measure where Schottky area leakage is almost completely blocked under 1000 V and JBS device has leakage of *pn* part. The lower break down voltage in case of 15 µm device is caused by higher electric field strength in semiconductor near emitter bottom region (Fig. 45).

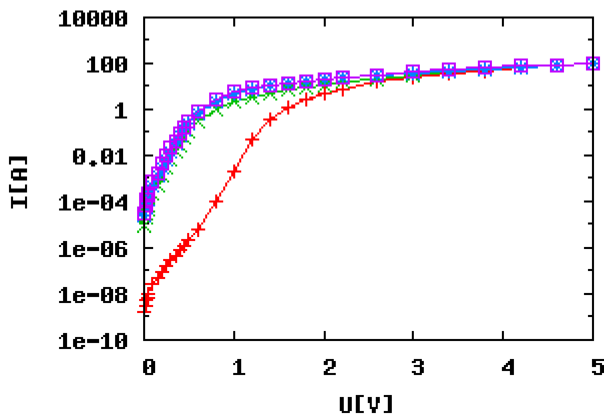

Figure 42: Forward characteristics dependence on device dimensions in µm

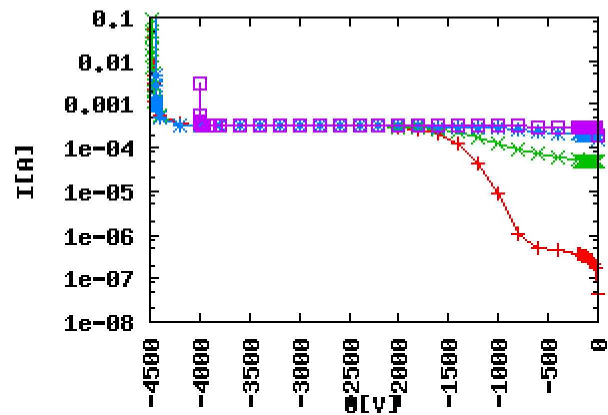

Figure 43: Reverse characteristics dependence on device dimensions in µm

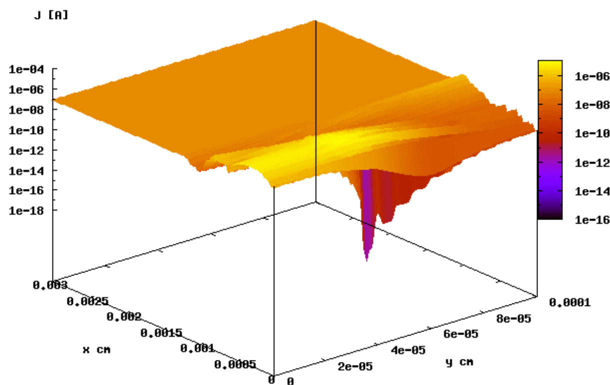

Figure 44: Current crowding to p area at U_F=0.2V, device size 1 μm

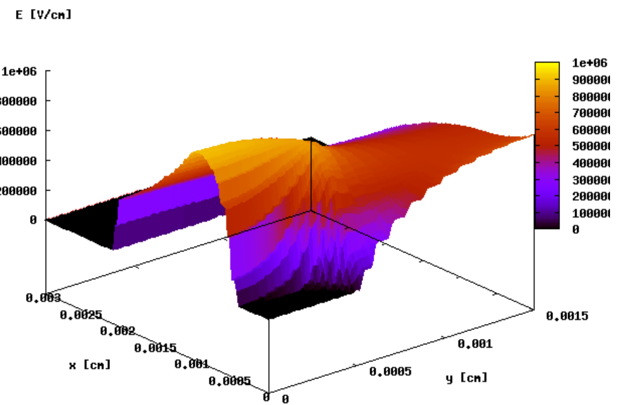

Figure 45: Electric field strength distribution at U_R=1000 V, device size 15 μm

Electric field strength. Electric field strength dependence of device dimensions (Fig. 46) shows clearly, that in case of highest simulated dimensions the effect of lowering electric field strength under Schottky contact is very weak. The effect is also weaker in case of 3 μm device. The reason is limited propagation of depletion region of *pn* junction.

Turn-off characteristics. From turn-off characteristics (Fig. 47) is seen that turn-off time does not depend much on device dimensions. The slight difference of turn-off time is probably caused by relation of depleted region to conducting Schottky area. Depleted region edge around the emitter area is the same for all measures, Schottky area changes. This gives the result where although the Schottky area relation to the whole device is unchangeable, the conducting Schottky area relation to whole device area is larger at larger device dimensions.

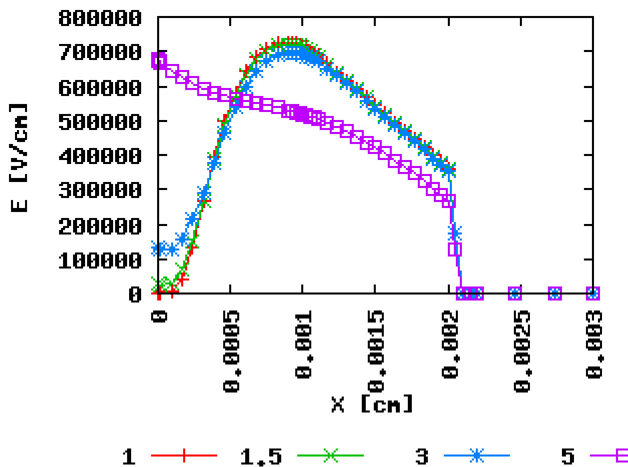

Figure 46: Electric field strength distribution dependence on device dimensions in μm

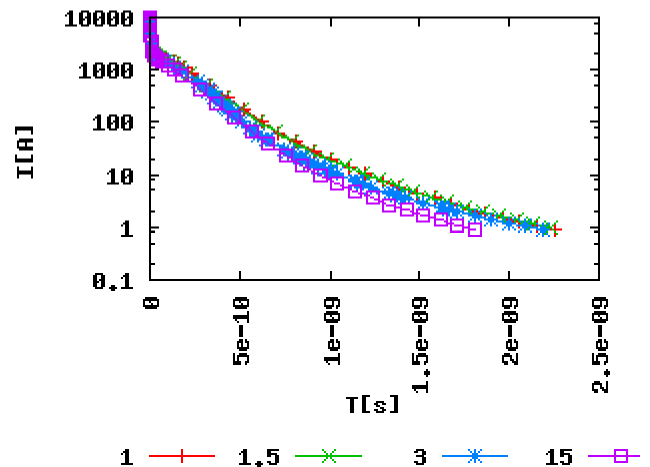

Figure 47: Turn-off I characteristics dependence on device dimensions in μm

Conclusions. From here shown different device dimensions the best is device with 1.5 μm width.

4.4.5. Schottky, JBS, pn diode comparison

Forward characteristics. Forward characteristic of JBS device is between Schottky and *pn* diode, close to Schottky diode (Fig. 48). On lower forward voltages only Schottky part of the device conducts. The JBS device characteristics try to copy the characteristics of best of two. The difference in JBS and best characteristic (Schottky at low voltages and *pn* at high voltages) is only caused by device area, which conducts at the moment. If areas of Schottky and *pn* part of JBS device are equal and majority of current flows through Schottky part as it normally is in region of low voltages. The current density of the whole device is abut two times lower as could be expected because of two times smaller active area.

Reverse characteristics. Reverse characteristic of JBS device is also between Schottky and *pn* diode, close to Schottky diode (Fig. 49). In ideal case the JBS reverse current should be more like in *pn* diode because of depletion region cutting away Schottky leakage current. In current work the best device is not considered to be one with such effect. It seems to author of this work that in case of power devices the low reverse leakage is not so important as high forward current. Reverse currents of chosen best device are small enough not causing noticeable device self-heating. Although both forward and reverse characteristics of chosen best JBS device are close to one of Schottky diode, there are other aspects superior to one. The Schottky barrier height dependence from applied voltage (Schottky effect) is not considered in this work. This effect would probably rise Schottky diodes reverse leakage current considerably, as electric field strength under Schottky contact is very high in case of pure Schottky diode compared to JBS diode (Fig. 50). This means that JBS diode's reverse leakage current is lower than one of pure Schottky diode's on high voltages. Additionally to Schottky effect there is one very important effect more compared to Schottky diode. High electric field strength under surface means very difficult passivation tasks, which still probably will not allow such high electric field strengths as in bulk of semiconductor. This simulation does not consider surface break down effects. The gain from JBS in real life is even more promising because of this fact.

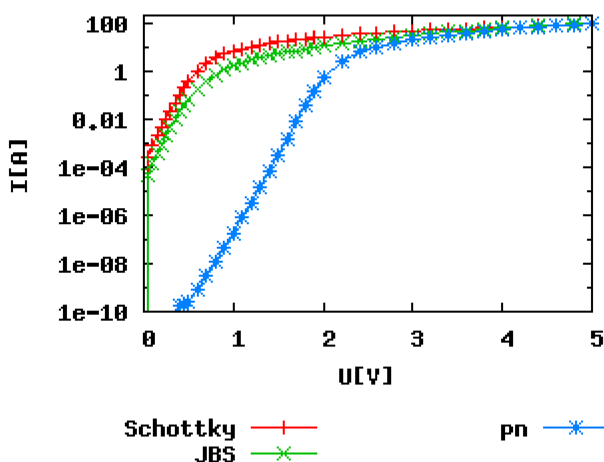

Figure 48: Forward characteristics of Schottky, JBS, pn diode.

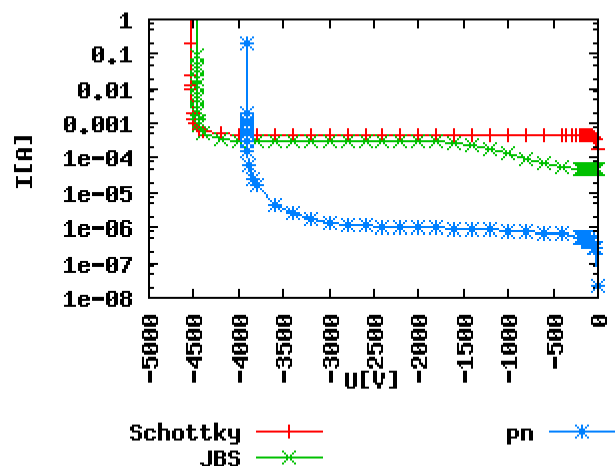

Figure 49: Reverse characteristics of Schottky, JBS, pn diode.

Electric field strength. Electric field strength dependence on device type (Fig. 50) is most important, as here is best seen the effect of lowering electric field strength under Schottky contact compared to pure Schottky device. The lower maximum electric field strength of JBS compared to *pn* diode can not really be compared as unnaturally deep emitter is used compared to normal *pn* diode acceptor implantation. This forces voltage drop of *pn* diode to considerably smaller area of *n*-type lower doped epitaxial layer than in normal *pn* diode. Still, if we consider devices with same measures of *p* area, JBS device has lower maximum electric field strength and can sustain higher reverse voltage.

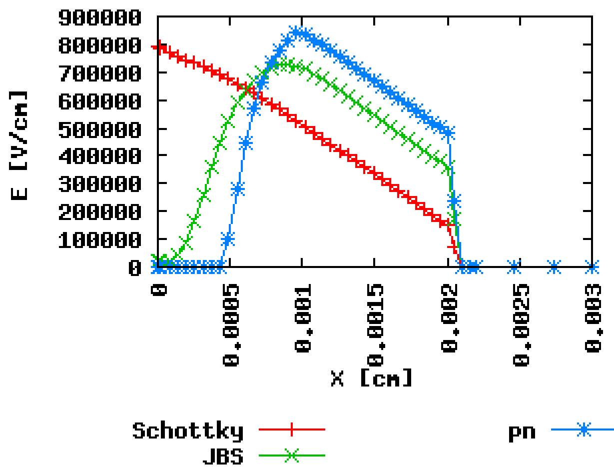

Figure 50: Electric field strength distribution in Schottky, JBS, pn diode

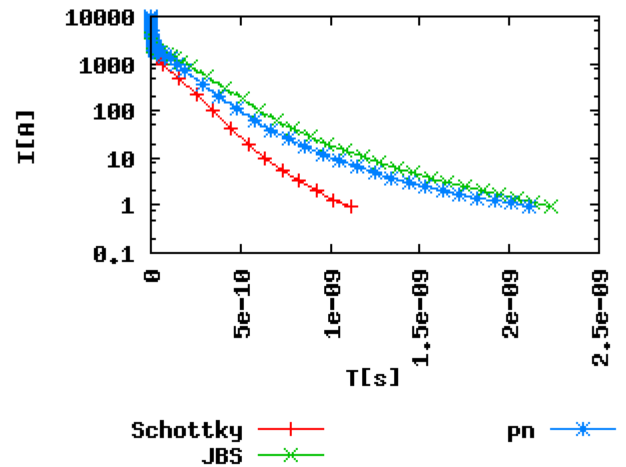

Figure 51: Turn-off I characteristics of Schottky, JBS, pn diode

Turn-off characteristics. The turn-off characteristic of JBS device is close to one of *pn* (Fig. 51). Although there is parallel Schottky structure, high forward currents are still causing minority carrier accumulation in epitaxial layer. Turn-off time of the JBS device is close to Schottky device's then device is switched off from low forward current, then almost all current flows through Schottky device and there is very little minority carrier accumulation in epitaxial layer.

Conclusions. The JBS is the best mainly because of its low electric field strength under Schottky contact compared to pure Schottky device, preserving at the same time Schottky-like forward characteristics.

4.4.6. Conclusions

From all the simulated parameter variations best result seems to have this combination:

4H-SiC with 2×10^{15} cm^{-3} epilayer concentration, metal work function 5.4 eV. The dimensions of the device are: emitter area 0.5 µm wide, 10 µm deep, Schottky area 1 µm wide. As there is never best device for all the solutions it is important to add, that this device has been chosen keeping in mind mainly low power loss in high power applications and goal to reduce need for high quality and complex passivation solutions by keeping electric field strength under surface very low.

The new results concluded from my work are:

1. The best *n* substrate based JBS device for power application is found in means of device dimensions, material type (4H- vs 6H-SiC), epitaxial layer concentration, Schottky contact metal work function values, relation of *pn* and Schottky area.

2. The inner processes of JBS device are shown in 3D. 2D figures do not give complete information about the behaviour of the device. The geometrical slice chosen for 2D figure, let it be current distribution, electric field strength, carrier concentration or something else might not be the most important one.

4.5. Comparison with experimental devices

There have been produced many SiC JBS devices. Still, it is hard to find a manufactured device for comparison with this work simulation results. There is simple explanation. The best device found in this work has very deep emitter area, which is hard to produce in real device with technology we have today. Unfortunately the resulted best device in this work is at the moment just the theoretical

best device. The manufactured device closest to the best device found in this work is one produced in Rutgers University, USA [37]. This device is also the device with best electrical properties produced to day. This device has deepest emitter region (2.3 μm) produced so far. The JBS has been made on 4H-SiC. Its area is 1.4 mm^2 epitaxial layer 30 μm thick with donor doping concentration $2\times10^{15} cm^{-3}$. *pn* diode part p^+ areas are 2 μm wide and 2.3 μm deep as said already. Schottky contacts are 9 μm wide. p^+ areas have acceptor doping concentration of 2×10^{18} cm^{-3}, which is made using Al ion implantation. Lower ohmic contact has been made of Al (0.02 μm) and Ni (0.3 μm). Upper Schottky to *n* and ohmic to *p* area contact has been made of Ti (0.05 μm) covered by thick Au.
This device achieved reverse blocking voltage of 4,308 V. This device has 142 A forward current at 4 V. Its RSP_ON is 20.9 $m\Omega\times cm^2$.

This device is in quite good agreement of simulations made in this work. The presented device has achieved reverse break down voltage of 4,308 V, which is near theoretical limit and limited by SiC avalanche break down electric field strength. The simulations on present work show also reverse break down near 4500 V. It must be taken into account that simulations in this work are for 20 μm epitaxial layer compared to 30 μm of produced device. Thicker epitaxial layer allows wider electrical field distribution and thus bigger voltage drop on same maximum electric field strength.
The on-state characteristics are better than ones achieved in simulations of present work. The reason here can be the simulation temperature, which was quite high: 700 K. Experimental results were probably measured near room temperature.

4.6. Analysis of *p* type semiconductor

4.6.1. Geometric dimensions

The basis of choosing geometrical dimensions is analogous to one in case of *n* substrate. For dimensioning of the JBS device, the width and depth of the emitter of the device are altered simultaneously and different input parameter sets are chosen for simulations. Relevant simulation results are compared to find optimum combination for power application: device with low power losses, high reverse breakdown voltage, fast turn-off characteristic.

Chosen input parameters are:

1. width of the *pn* part of the device (x2 in Fig. 10): 0.25-1 μm (1/6-2/3 of the whole area),
2. depth of the emitter of the *pn* part of the device (x1 in Fig. 10): 1-15 μm.

Other parameters are fixed.

Forward characteristics. Devices with emitter width 2/3 of the device act like *pn* diodes, current through Schottky contact is smaller on whole range of forward voltage. As in case of *n* based JBS devices, the length of Schottky contact area (0.5 μm) is small enough that built-in voltage of *pn* junction forms depletion region under whole Schottky device and eliminates most of free electrons. Devices with emitter depth of 1 μm behave like Schottky diodes. Although on resistance of *pn* diode on higher forward voltages is smaller than one of Schottky diode, those devices don't gain on it. Other devices behave like Schottky diodes below about 2.3 V and like *pn* diodes above that forward voltage. Schottky part of characteristics of those devices is quite alike, but *pn* parts unlike in case of *n* based JBS, differ. In case of *p* based JBS the current through *pn* part of the device dominates at higher forward voltages. Current density distribution at 5 V forward voltage is seen in Fig. 53 (x component) and Fig. 54 (y component). As seen from current density x component figure almost all of the current flows through pn part of the device (lighter area in Fig. 53). The current redistribution to *pn* part of the device takes place in region of lower edge of emitter (lighter area in Fig. 54). In *pn* diode the region defining the voltage drop on the device is mainly low-doped epitaxial layer below the emitter and above the substrate. Thus the difference in region of higher

voltages is caused by length of low-doped epitaxial layer between emitter and substrate. In case of deeper emitter the length of this relatively high resistance region is shorter and device on-resistance consequently lower. The best characteristics have devices with deepest emitter and worst with smallest emitter depth.

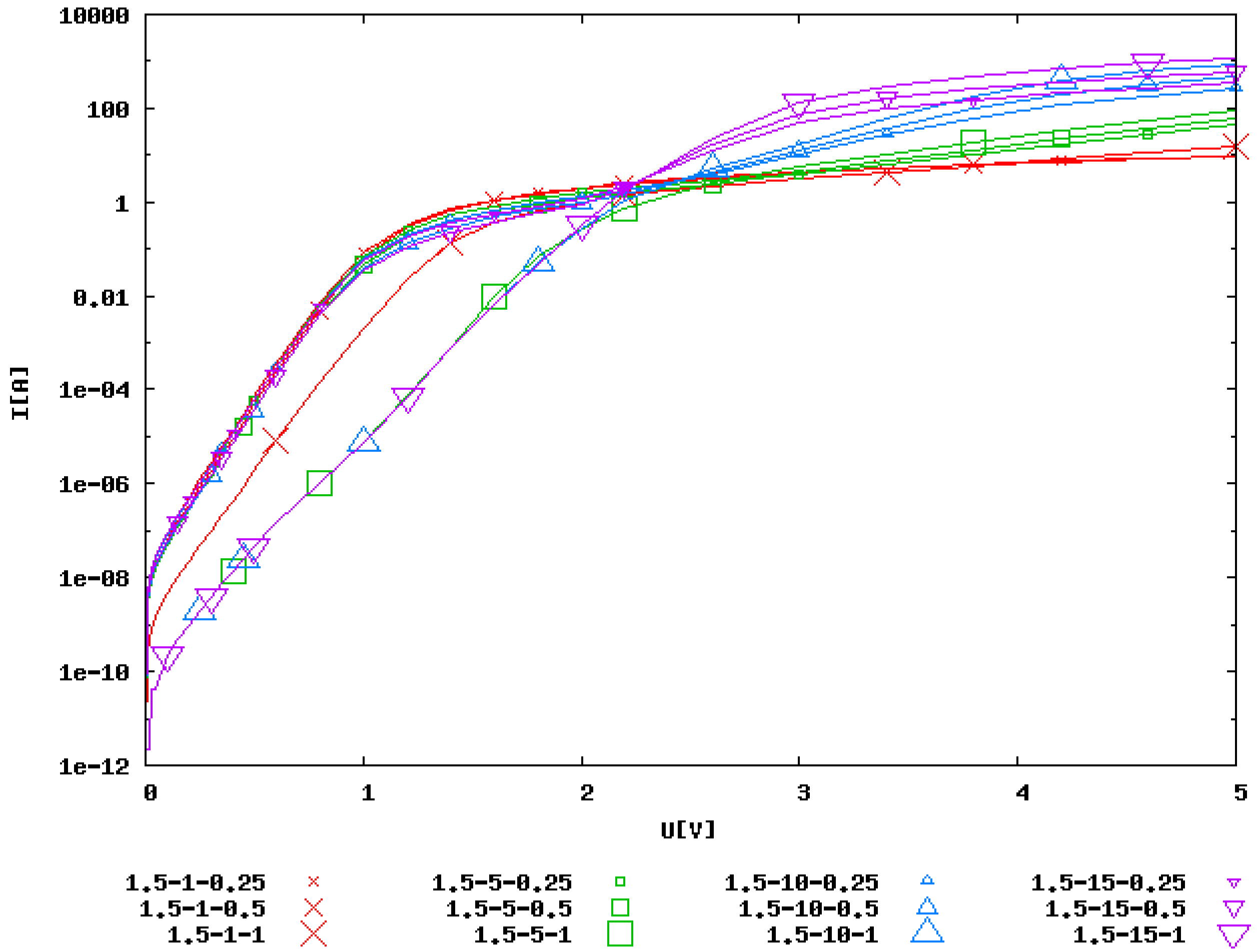

Figure 52: Forward I-V characteristics of JBS devices with different emitter deepness and width. Legend shows width of the whole structure, deepness of the emitter, width of the emitter in μm. p substrate

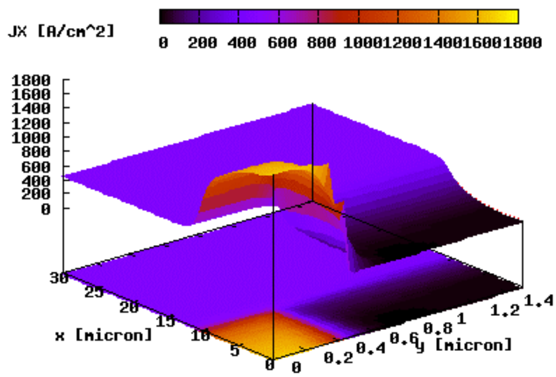

Figure 53: Current density x component in device "1.5-10-0.5" at 5 V forward voltage. Current density direction is opposite to x axis direction. p substrate

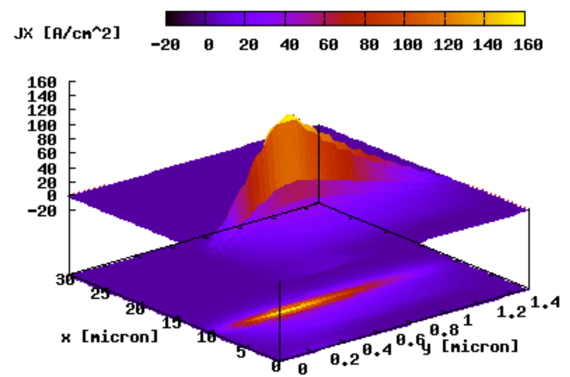

Figure 54: Current density y component in device "1.5-10-0.5" at 5 V forward voltage. Current density direction is opposite to x axis direction. p substrate

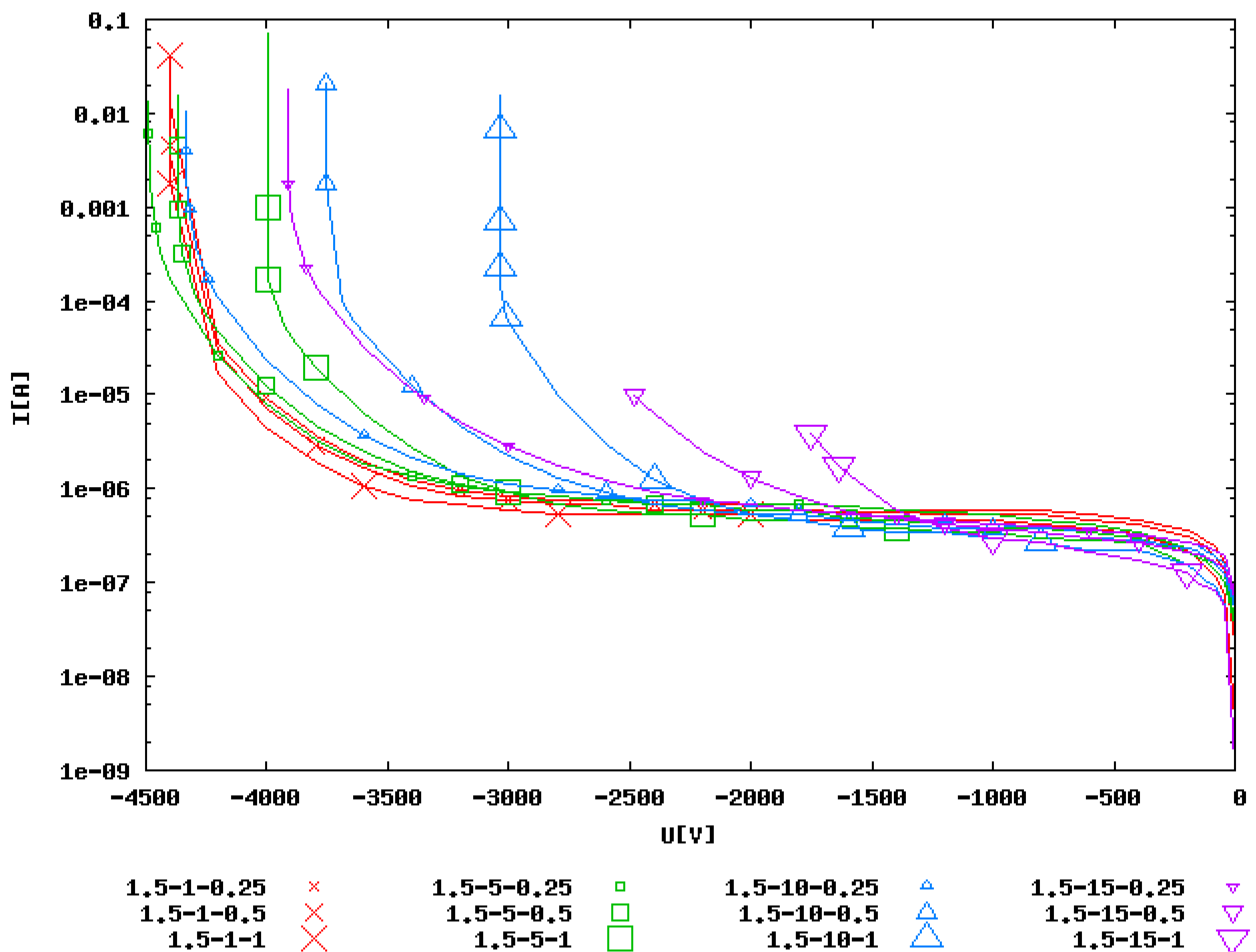

Figure 55: Reverse I-V characteristics of JBS devices with different emitter deepness and width. Legend shows width of the whole structure, deepness of the emitter, width of the emitter in µm. p substrate

Reverse characteristics. Reverse characteristics (Fig. 55) reveal, that JBS device on *p* substrate has very low reverse current, but also in many cases low break down voltage. Lowest break down voltages have devices with deepest emitters. The electric field is forced into narrow region between emitter and substrate in case of deep emitter resulting in low break down voltages. Devices with 10 µm emitter depth have also low break down voltages except of one with 0.25 µm wide emitter, which is too narrow to block effectively Schottky leakage current.

Electric field strength distribution. Electric field strength distribution (Fig. 56) shows that devices with low emitter should be avoided because of high electric field strength under surface. Also devices with deep emitter should be avoided because of very high electric field strength in bulk of semiconductor. Electric field is mainly distributed in region between emitter and substrate. In case of deep emitters the named region is narrow and consequently the maximum electric field strength is high. This very high electric field strength limits device reverse breakdown voltage to be low. Electric field strength distribution along y-axis is relatively even (Fig. 57).

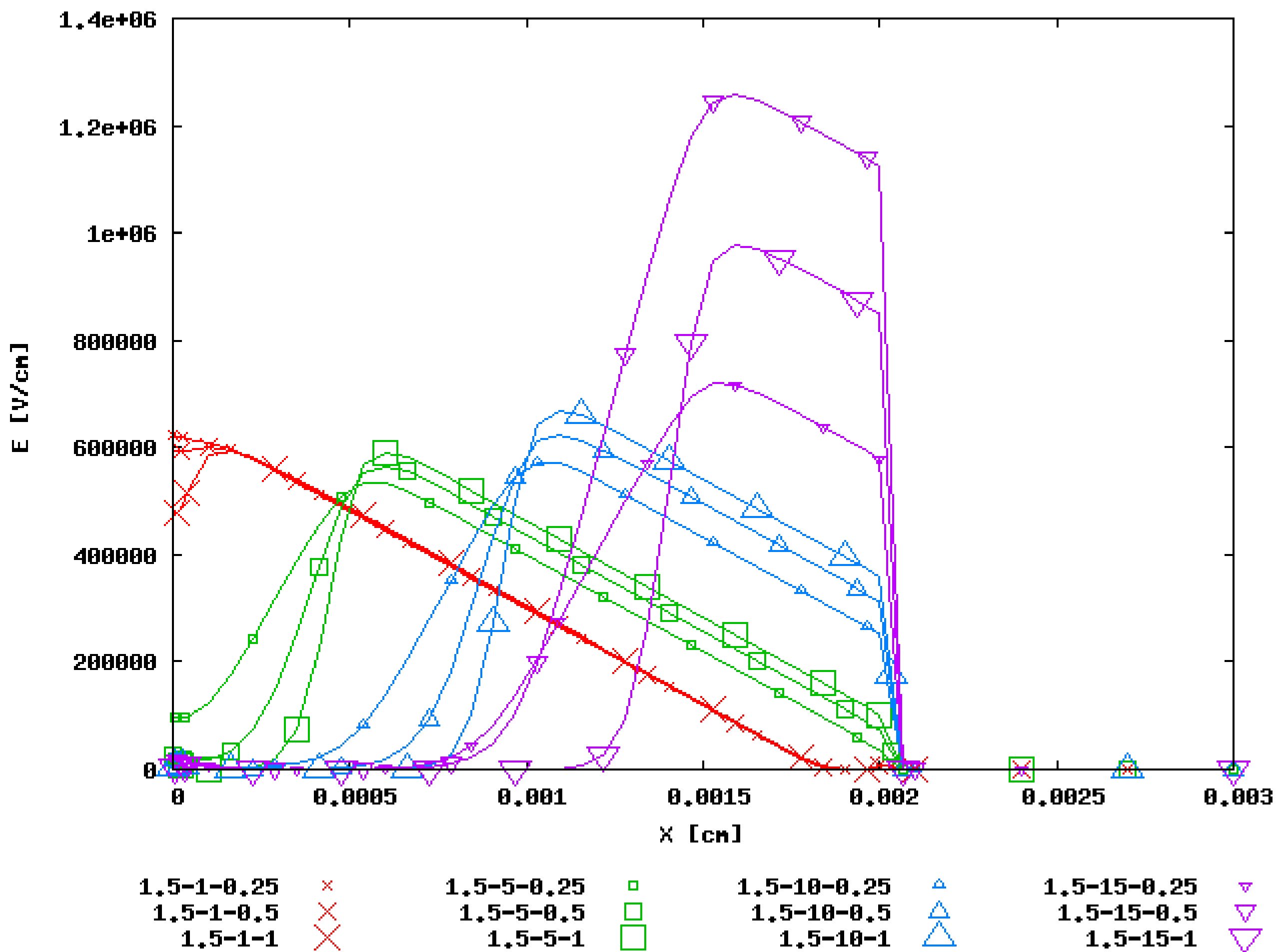

Figure 56: Electric field strength distribution characteristics under Schottky contact of JBS devices with different emitter deepness and width. Legend shows width of the whole structure, deepness of the emitter, width of the emitter in µm. p substrate

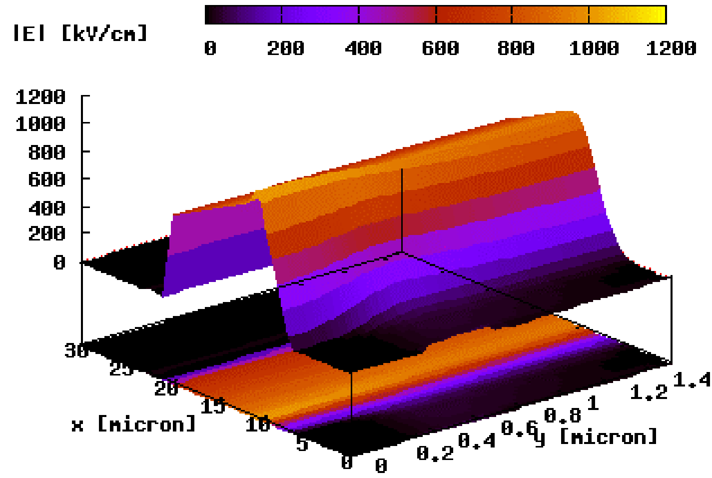

Figure 57: Electric field distribution at reverse voltage 1000 V in case of device "1.5-10-0.5". p substrate

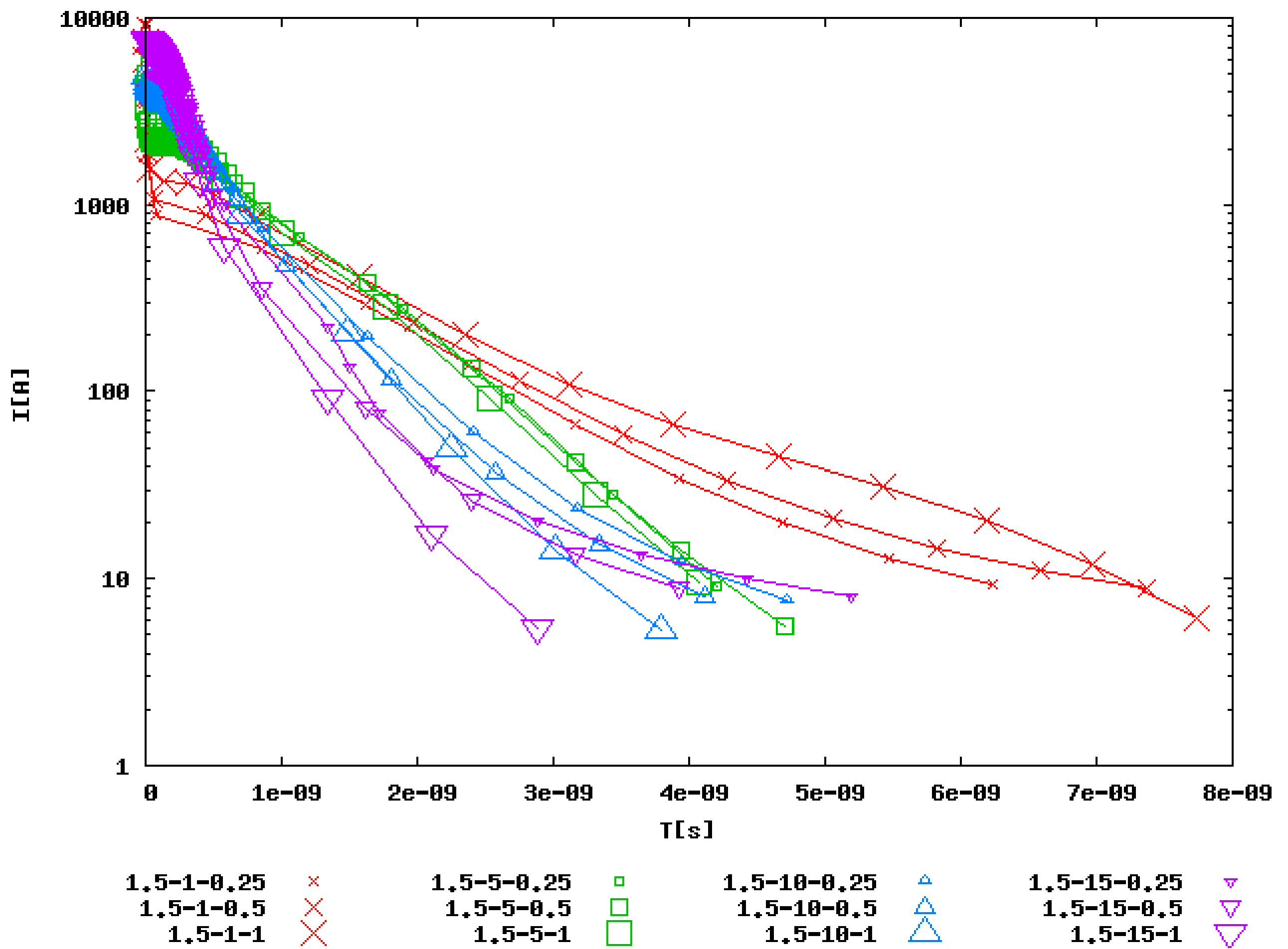

Figure 58: Turn-off current switching JBS from 0V to -5V with different p doping area deepness and width. Legend shows width of the whole structure, deepness of n doping area, width of the n doping area in μm. p substrate

Turn-off characteristics. From turn-off characteristics (Fig. 58) is seen that devices with 1 μm emitter depth are slowest. Although devices with 1 μm emitter depth have smallest amount of minority carriers, it has still longest turn-off time. The reason is probably how minority carriers are transferred out from semiconductor. In case of 1 μm emitter depth the recombination of charge carriers takes place in semiconductor because of majority current flowing through Schottky part of the device. In case of deeper emitter main current flows through emitter and electrons are carried out from semiconductor through emitter metal contact, which is faster.

Conclusions. Best dimensions of emitter for *p* type JBS device are: 10 μm depth and 0.25 μm width. Devices with 1 μm emitter width have bad forward characteristics, devices with low doped epitaxial layer have bad forward characteristics at higher part of forward characteristics. Device with combination of 15 μm deep, 0.5 μm wide emitter has low break down voltage. Device with emitter of 5 μm deep and 0.25 μm width has relatively high electrical field under surface. Only leftover are devices with emitter of 10×0.25 μm and 5×0.5 μm. Device with 10×0.25 μm emitter dimensions has better forward characteristic at higher forward voltages and is thus the best.

4.6.2. 6H-SiC and 4H-SiC comparison

Forward characteristics. 6H-SiC and 4H-SiC comparison reveals that higher voltage part of forward characteristic of 6H-SiC is worse than one of 4H-SiC (Fig. 59). The reason is lower mobility of 6H-SiC. Better characteristics of 6H-SiC in low region of forward voltages is caused by lower Schottky barrier height.

Reverse characteristics. Reverse characteristic of 6H-SiC (Fig. 60) has two orders of magnitude higher reverse current than 4H-SiC. The reason again is Schottky barrier height. Device current is defined by Schottky reverse characteristics and 6H-SiC has lower barrier than 4H-SiC.

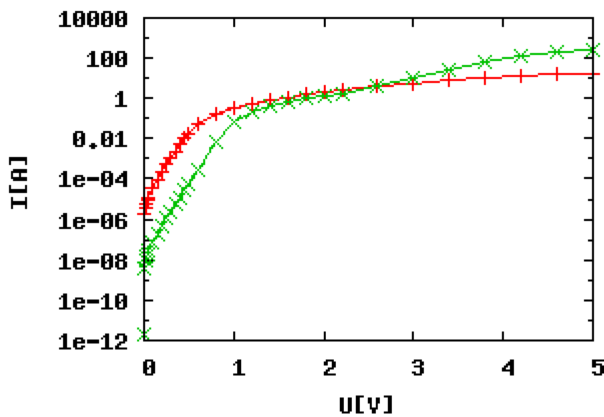

Figure 59: Forward I-V characteristics 6H-SiC vs 4H-SiC. p substrate

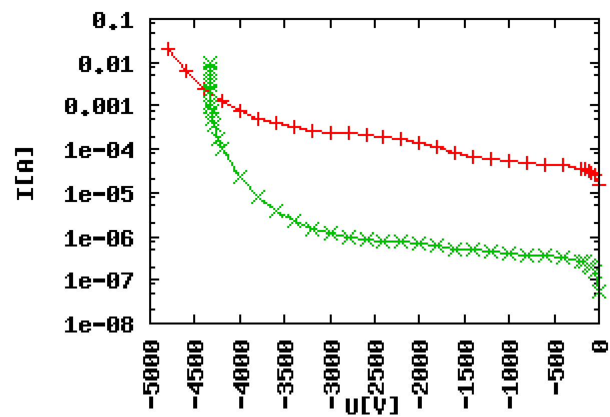

Figure 60: Reverse I-V characteristics 6H-SiC vs 4H-SiC. p substrate

Electric field strength distribution. Electric field strength distribution is same for both materials (Fig. 61). Although the polytype is different, the relative resistance profile of the device for both 6H and 4H-SiC is the same.

Turn-off characteristics. 4H-SiC has also a bit better turn-off characteristic than 6H-SiC (Fig. 62). The reason here is lower charge carrier mobility of 6H-SiC.

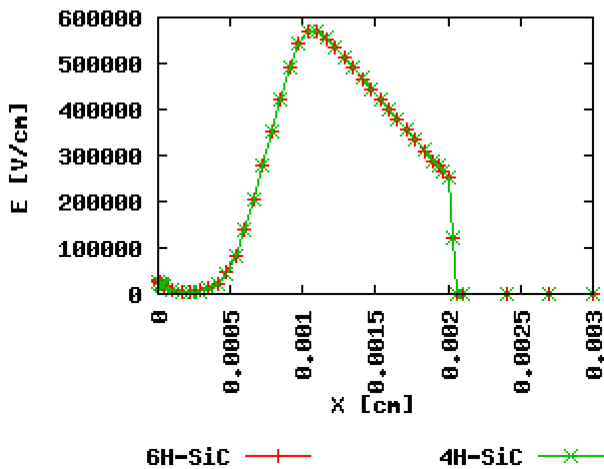

Figure 61: Electric field strength distribution 6H-SiC vs 4H-SiC. p substrate

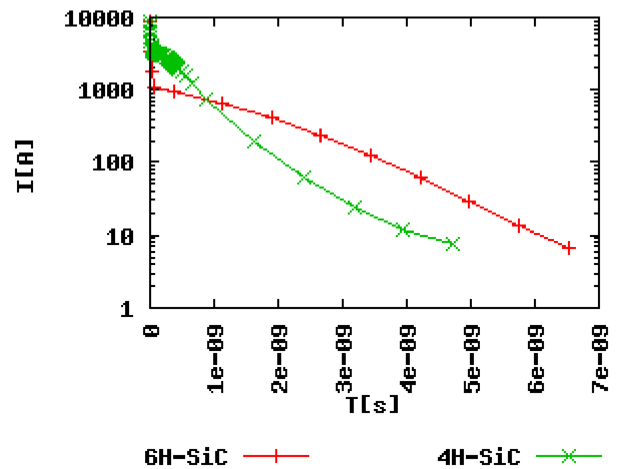

Figure 62: Turn-off I characteristics 6H-SiC vs 4H-SiC. p substrate

Conclusion. In conclusion it can be said that 4H-SiC has better characteristics than 6H-SiC.

4.6.3. Epitaxial layer

Forward characteristics. There is no much difference in forward characteristics (Fig. 63) in case of different epitaxial layer doping concentration. Device with higher epitaxial layer doping concentration has better forward characteristic and bigger reverse current as expected due to lower resistance.

Reverse characteristics. There is no much difference in reverse characteristics (Fig. 64) either.

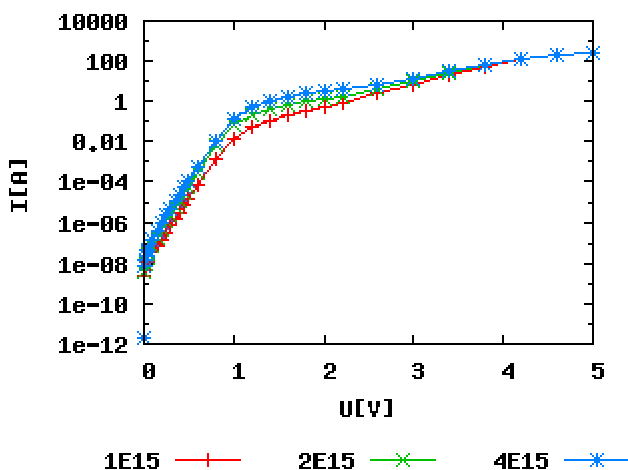

Figure 63: Forward characteristics dependence on epitaxial layer doping concentration. p substrate

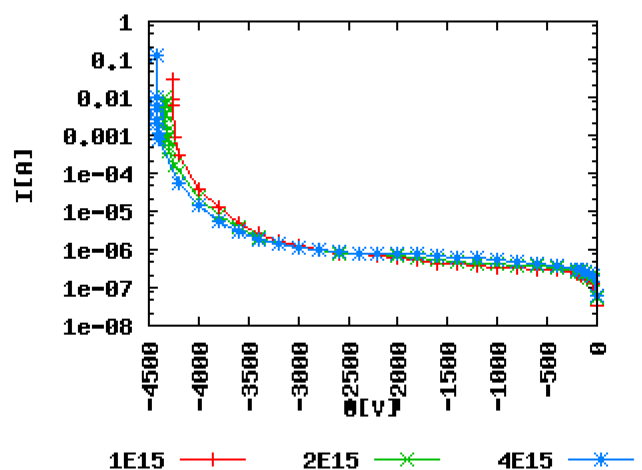

Figure 64: Reverse characteristics dependence on epitaxial layer doping concentration. p substrate

Electric field strength distribution. Electric field strength distribution (Fig. 65) dependence of epitaxial layer doping concentration show that device with higher epitaxial layer doping concentration has higher electric field strength under surface. Lower epitaxial layer doping concentration results in more uniform electric field strength distribution. This allows lower maximum electric field strength peak at the same voltage drop.

Turn-off characteristics. The turn-off time dependence of epitaxial layer doping concentration is also not very big (Fig. 66). The slowest is device with highest doping concentration.

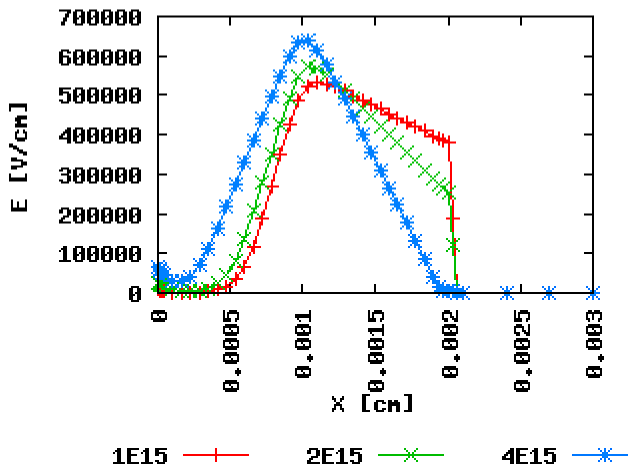

Figure 65: Electric field strength distribution dependence on epitaxial layer doping concentration. p substrate

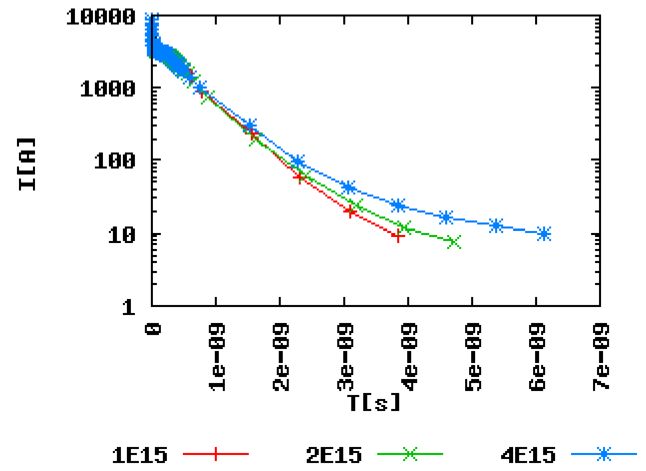

Figure 66: Turn-off I characteristics dependence on epitaxial layer doping concentration. p substrate

Conclusion. As in case of 2×10^{15} is forward characteristic a bit better and electric field strength in 1×10^{15} and 2×10^{15} is almost the same, the doping concentration of 2×10^{15} is considered to be the best.

4.6.4. Schottky contact metal work function value variations

Forward characteristics. The work function has remarkable influence on forward (Fig. 67) characteristics through influence on Schottky barrier. The influence is seen on low voltages because this is the region where Schottky part of the device conducts the main current. On higher voltages most of the current flows through *pn* part of the device and influence of Schottky barrier is not important any more.

Reverse characteristics. Also the influence on reverse characteristics (Fig. 68) is remarkable because of the Schottky barrier height difference. Lower Schottky contact metal work function causes higher leakage currents in Schottky part of the device and also in device as a whole.

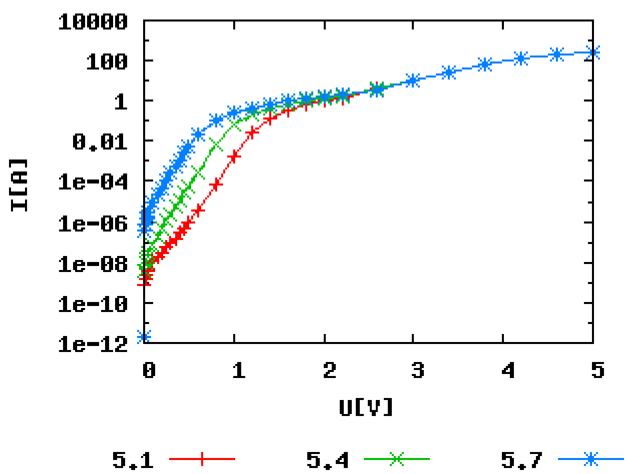

Figure 67: Forward characteristics dependence on contact metal work function. p substrate

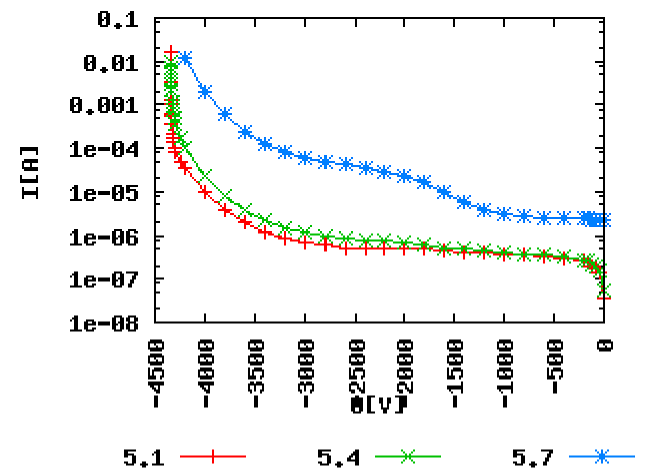

Figure 68: Reverse characteristics dependence on contact metal work function. p substrate

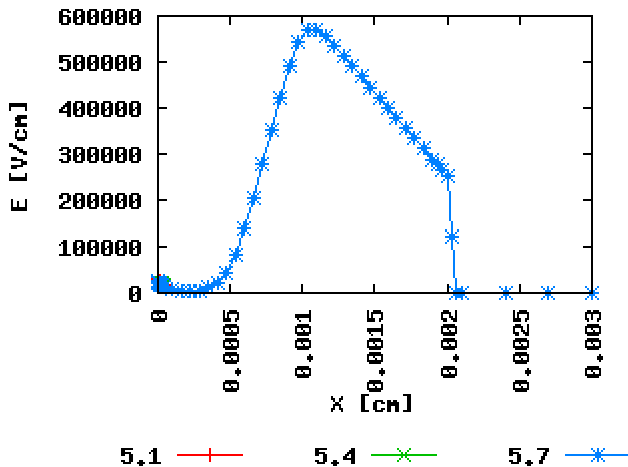

Figure 69: Electric field strength distribution dependence on contact metal work function. p substrate

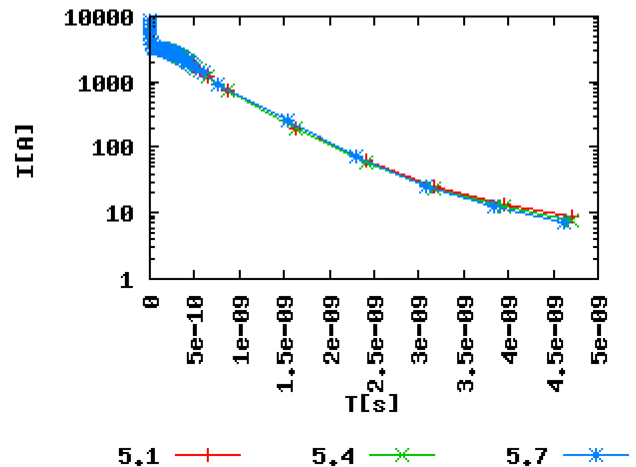

Figure 70: Turn-off I characteristics dependence on contact metal work function. p substrate

Electric field strength distribution. Schottky contact metal work function value has almost no influence on electric field strength distribution (Fig. 69).

Turn-off characteristics. The influence on turn-off characteristics (Fig. 70) is also undetectable.

Conclusions. Work function 5.4 eV seems to be the best because the reverse characteristic of devices with 5.4 eV and 5.1 eV Schottky contact metal work function are close but the difference of forward characteristics is much bigger. The best Schottky contact metal work function is 5.4 eV.

4.6.5. Whole device dimensions

Forward characteristics. Different device measures forward characteristics (Fig. 71) are close to each other except smallest device, as it seems that in case of such a small measures *pn* diode's depletion region starts to influence on Schottky part current.

Reverse characteristics. From reverse characteristics (Fig. 72) it is seen that biggest device has lowest reverse break down voltage. The reason is very high electric field strength near lowest end of emitter. On smaller devices there is no such big electric field strength maximum in this region.

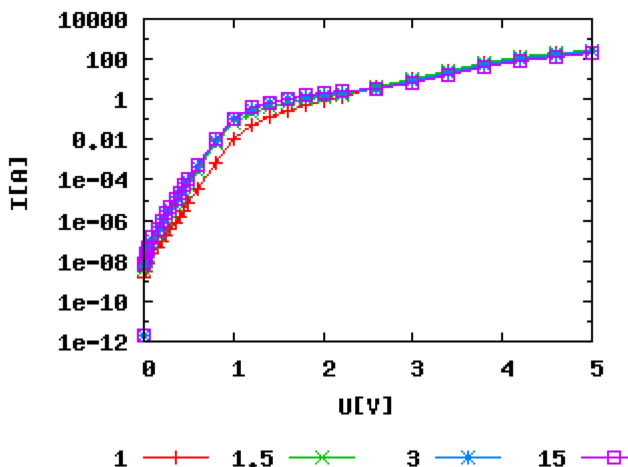

Figure 71: Forward characteristics dependence on device dimensions in μm. p substrate

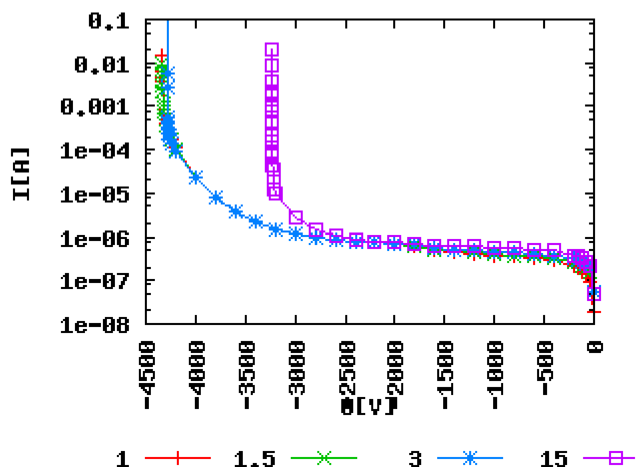

Figure 72: Reverse characteristics dependence on device dimensions in μm. p substrate

Electric field strength distribution. Electric field strength distribution (Fig. 73) maximums on part of Schottky diode are almost equal, but electric field strength under surface of semiconductor is lowest in case of 1 and 1.5 µm devices. In case of highest simulated dimensions the effect of lowering electric field strength under Schottky contact is very weak. The effect is also weaker in case of 3 µm device. The reason is limited propagation of depletion region of *pn* junction.

Turn-off characteristics. Turn-off time has no remarkable dependence on device measures (Fig. 74).

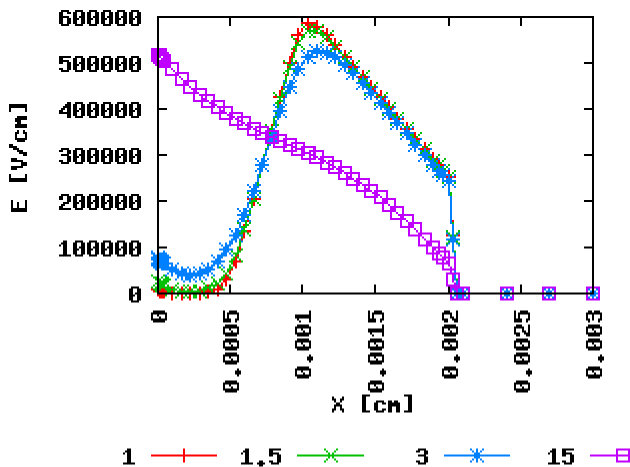

Figure 73: Electric field strength distribution dependence on device dimensions in µm. p substrate

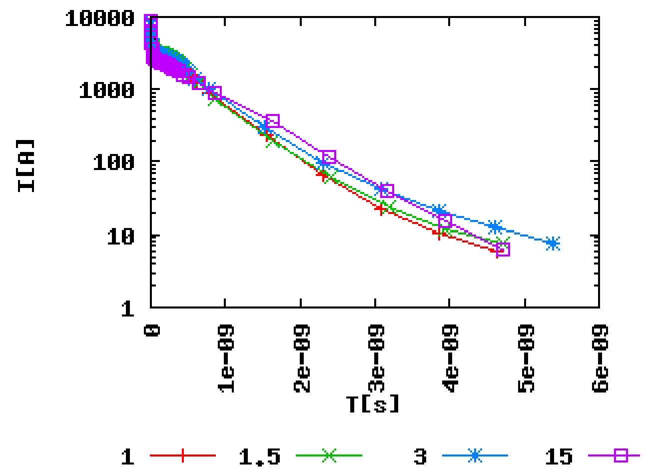

Figure 74: Turn-off I characteristics dependence on device dimensions in µm. p substrate

Conclusions. Best x dimension is 1.5 µm.

4.6.6. Schottky JBS pn comparison

Forward characteristics. Forward characteristics of JBS device is between Schottky and *pn* diode, closer to the best of them (Fig. 75). On lower forward voltages only Schottky part of the device conducts. On higher voltages only pn part of the device conducts.

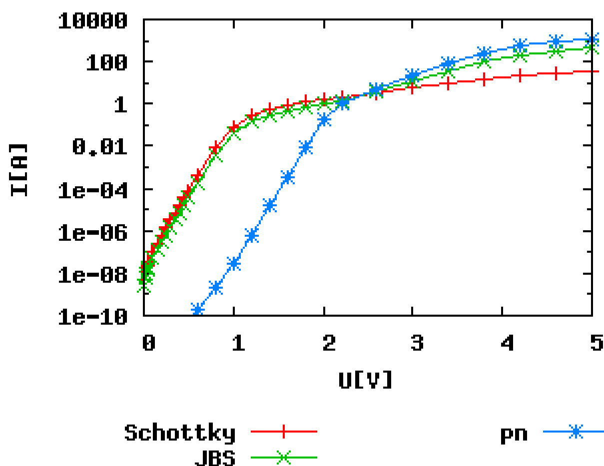

Figure 75: Forward characteristics of Schottky, JBS, pn diode. p substrate

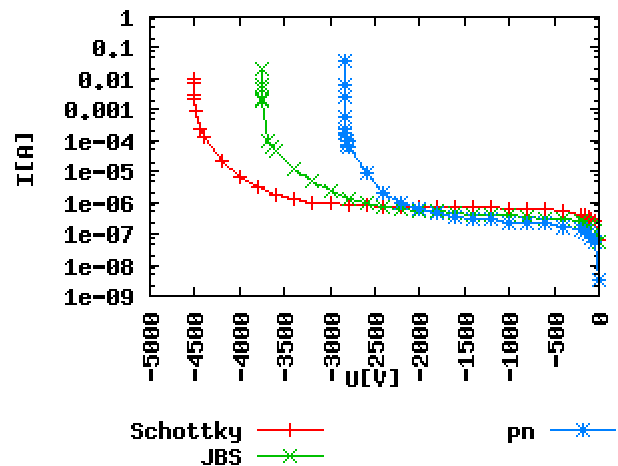

Figure 76: Reverse characteristics of Schottky, JBS, pn diode. p substrate

Reverse characteristics. Reverse characteristics of JBS device is also between Schottky and pn diode (Fig. 76). The reason why pn diode has lower break down voltage than Schottky and JBS, is the dimension of region where electric field strength is distributed. In this case it is only 10 µm.

Electric field strength is distributions. JBS is a compromise between Schottky and pn diodes electric field strength distribution: electric field strength is distributed on wider area than in case of pn diode and it is still low under surface (Fig. 77).

Turn-off characteristics. Turn-off time is slowest in case of JBS (Fig. 78). Closer look at JBS currents shows that Schottky part of the device works against *pn* part of the device for short period of time. Although eventually is turn-off time longer for Schottky than for *pn* diode, it is important to notice that after as short as 30 ps the current of Schottky diode is already about 8 times lower than of *pn* diode. 90% of reverse voltage is achieved in 23 ns in case of Schottky diode and in 600 ns in case of *pn* diode.

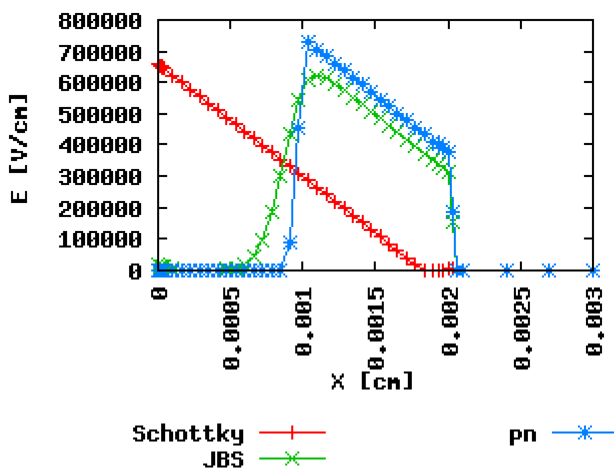

Figure 77: Electric field strength distribution in Schottky, JBS, pn diode. p substrate

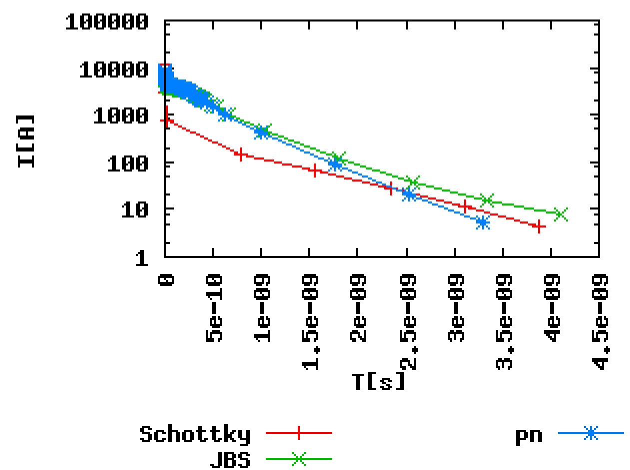

Figure 78: Turn-off I characteristics of Schottky, JBS, pn diode. p substrate

4.6.7. *p* substrate vs *n* substrate best devices

Forward characteristics. *n* and *p* substrate based JBS device forward characteristics (Fig. 79) shows that *n* substrate device has about three orders of magnitude higher current at very low voltages and almost same or a bit lower currents at very high forward voltages compared to *p* substrate. The big current difference at low voltages is explained by lower barrier height of *n* 4H-SiC (about 1.1 eV) compared to *p* 4H-SiC (about 1.4 eV). For both simulations metal work function was the same resulting different barrier heights. On higher voltages most of the current flows through *pn* part of the device causing reverse situation at high voltages.

Reverse characteristics. On reverse characteristics (Fig. 80) is seen that device with *n* substrate has about two and a half orders of magnitude higher leakage current. As in forward bias low voltage situation this is also caused by big difference in barrier heights for *p* and *n*-type material in case of same Schottky contact metal work function.

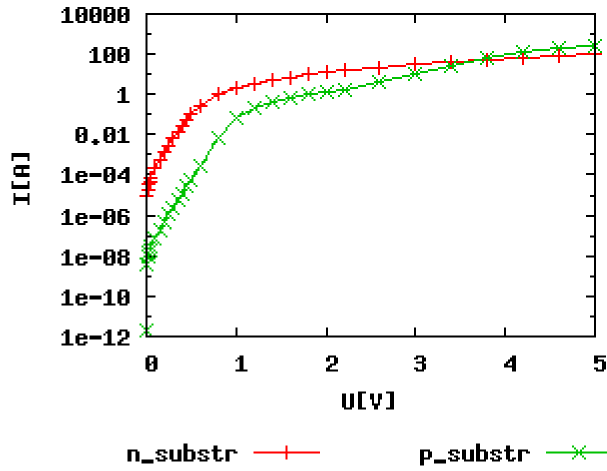

Figure 79: Forward characteristics p vs n substrate

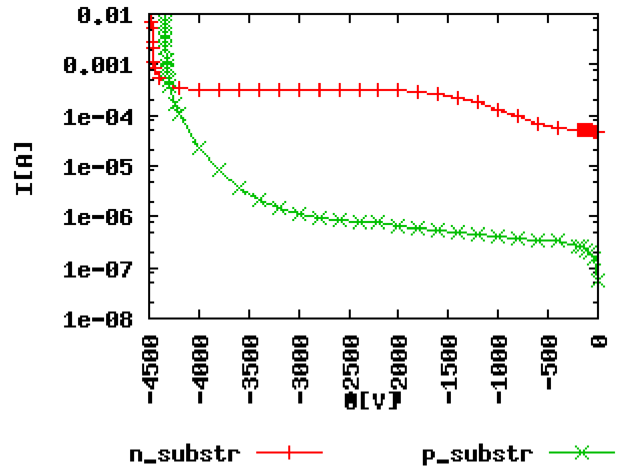

Figure 80: Reverse characteristics p vs n substrate

Electric field strength distribution. Electric field strength distribution maximum is lower in case of *n* substrate (Fig. 81). The reason is the width of emitter, which was chosen to be 1 µm in case of *p* based JBS.

Turn-off characteristic. Turn-off characteristics of *n* semiconductor based device are about 4 times faster than *p* semiconductor based best device (Fig. 82). The reason is the electron mobility, which in case of 4H-SiC is almost 10 times slower than electron mobility.

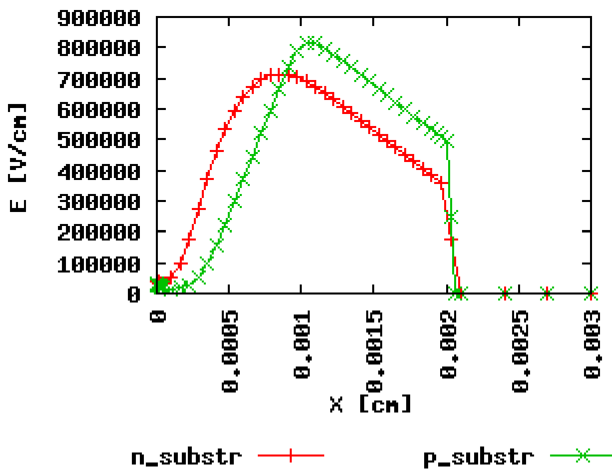

Figure 81: Electric field strength distribution n vs p substrate

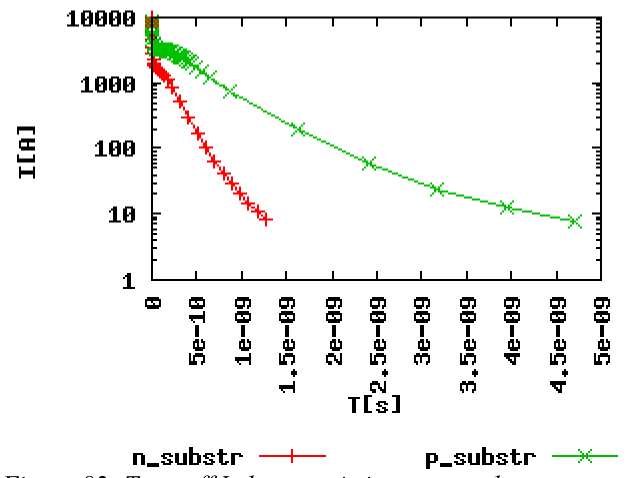

Figure 82: Turn-off I characteristics n vs p substrat

Conclusion. Comparison of complementary *p* and *n* structures shows that *n*-type semiconductor based device has better forward and turn-off characteristics, *p*-type semiconductor based device has lower reverse leakage. If we consider high power devices, most important are low dissipating power and high reverse break down voltage. As break down voltage is same for both *p* and *n* devices, *n*-type device is preferred.

4.6.8. Conclusions

From all the simulated parameter variations best result for *p* based seems to have this combination:

4H-SiC with 2×10^{15} cm^{-3} epilayer concentration, metal work function 5.4 eV. The dimensions of the device are: emitter 1 μm wide, 10 μm deep, Schottky area 0.5 μm wide. As there is never best device for all the solutions it is important to add, that this device has been chosen keeping in mind mainly low power loss in high power applications and goal to reduce need for high quality and complex passivation solutions by keeping electric field strength under surface very low.

The new results concluded from my work are:

1. Simulations for *p* substrate based JBS devices are done. There are no *p* substrate based JBS device simulations published till today. Simulations revealed that *p* substrate based JBS device has no substantial advantages over *n* substrate based device.
2. The best *p* substrate based JBS device for power application is found in means of device dimensions, material type (4H- vs 6H-SiC), epitaxial layer concentration, Schottky contact metal work function values, relation of *pn* and Schottky area.

Summary

As simulations show, best JBS device has *n*-type 4H-SiC with $2\times10^{15}cm^{-3}$ epilayer concentration and metal work function of 5.4 eV. The measures of the device are: *p* area 1 μm wide, 10 μm deep, Schottky area 3 μm wide. The result would be nice, but there is a problem: there is no reasonable means of producing such devices because of deep, 10 μm *p* region. The deepness of *p* region is most important measure in forming the shape of electrical field. Electrical field distribution is important in three aspects:

1. maximum electric field strength determines avalance break down of device,
2. electric field strength under Schottky contact has influence on reverse current through Schottky barrier lowering,
3. electrical field near device surface has great importance on device surface break down.

The new results concluded from my work are:

- The inner processes of JBS device are shown in 3D. 2D figures do not give complete information about the behaviour of the device. The geometrical slice chosen for 2D figure, let it be current distribution, electric field strength, carrier concentration or something else might not be the most important one.
- The best *n* substrate based JBS device for power application is found in means of device dimensions, material type (4H- vs 6H-SiC), epitaxial layer concentration, Schottky contact metal work function values, relation of *pn* and Schottky area.
- The best *p* substrate based JBS device for power application is found in means of device dimensions, material type (4H- vs 6H-SiC), epitaxial layer concentration, Schottky contact metal work function values, relation of *pn* and Schottky area.
- Simulations for *p* substrate based JBS device are done. There are no *p* substrate based JBS device simulations published till today. Simulations revealed that *p* substrate based JBS device has no substantial advantages over *n* substrate based device.

Results achived in this thesis will be used for production of experimental JBS devices in co-operation with Institute of Electronics, TUT and TDI, USA.

The model used in simulations in this work does not include tunneling. Tunneling can influence on device behaviour remarcably in some situations. Therefore additional investigation of JBS device behaviour with inclusions of tunneling model would be interesting subject for continuing the same subject.

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Our Ref SECM05/59641

23 June 2005

Prof T Rang
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ESTONIA

Dear Prof Rang,

Re: Surface/Contact 2005, 5 - 7 September 2005, Bologna, Italy

I am pleased to inform you that the manuscript of your paper "Current crowding phenomenon in JBS structures" by T Rang, R Kurel, G Higelin, I Poirier has been accepted for oral presentation at the conference and has now been passed to the publishers for inclusion in the Conference Proceedings.

Please note that you or one of your co-authors will be expected to attend the Surface/ Contact 2005 conference meeting and present the paper.

The final programme will be completed nearer the time and will be available at the time of registration. Should you wish to know the exact day of your presentation please contact the Conference Secretariat the week prior to the start of the meeting or look on our web page at:
http://www.wessex.ac.uk/conferences/2005/secm05/index.html

I anticipate that you will have 20 minutes for presentation and discussion. LCD projection facilities will be available at the meeting. If you have any other requirements we will do our best to arrange them. Enclosed you will find some guidelines for presentation.

I hope you have a safe and pleasant journey to the conference and look forward to seeing you in Bologna.

Yours sincerely

Rachel Green
Senior Conference Co-ordinator
rgreen@wessex.ac.uk

Encs.

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Copies of selected papers

Selected papers are author’s additional publications not covered in the present thesis.

Proc. Estonian Acad. Sci. Eng., 2004, **10**, 3, 173–178

Comparison of the dynamic behaviour of complementary 6H- and 4H-SiC Schottky structures using numerical simulation

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Abstract. In this paper we compare, using numerical simulation, the dynamic behaviour of complementary Schottky structures based on 6H- and 4H-SiC substrates. Clear differences in the behaviour of these two Schottky structures at different temperatures has been established. The calculations show that the turn-off time is about the same for both Schottky structures, but it varies with the temperature about 1.5 times.

Key words: SiC, Schottky structures, turn-off time, high temperature behaviour, numerical simulation.

1. INTRODUCTION

Silicon carbide (SiC) is an outstanding compound semiconductor material with extremely promising physical properties that makes it an excellent material for high-speed and high-temperature power electronic applications. Metal–semiconductor interfaces play a fundamental role in any semiconductor device. Thus research of different characteristics of the Schottky contact semiconductor structures is very important. Furthermore, some parameters of the 6H- and 4H- polytypes of SiC differ considerably, which influences directly the device characteristics.

In the present paper the turn-off characteristics in complementary SiC Schottky structures with 6H- and 4H- substrates under different temperature conditions are studied using two-dimensional nonisothermal drift-diffusion device simulator DYNAMIT-2DT, developed at TTU Department of Electronics [1,2].

2. DESCRIPTION OF THE MODEL

The simulator solves the Poisson and continuity equations for electrons and holes (holes are negligible in the present case) in semiconductor "electrical solution domain". The boundary conditions at Schottky contact surface are specified in a standard manner, applied in most of the simulators: the boundary potential φ_s (bound with band edge energies E_c and E_v) is shifted from the bulk (neutral) value so that the barrier height for electrons in the metal at the Fermi level equals the effective barrier height and carrier surface concentrations depend slightly on the current density through $j_n = q v_{sn}(n_s - n_{s0})$ -type relations, where j_n is the electron current density, q is the electron charge, v_{sn} is the electron surface velocity, and n_s and n_{s0} are surface concentration of electrons in the actual and thermal equilibrium situations, respectively. The barrier lowering due to the surface electric field (i.e., the Schottky effect) is here not included assuming that the effective (empiric) Φ_{bn} and Φ_{bp} values already include the influence of this effect.

The 100 µm wide structure fragment was selected for simulation, assuming that characteristic lateral scale of the current crowding effect is several times below that limit (Fig. 1). The lateral sides of the fragment are neutral reflecting surfaces (Neumann-type boundary conditions $\partial f / \partial y = 0$). In vertical direction, to reduce the mesh node number, only the $0 \le x \le 100$ µm region was included in "electrical solution". The rest of the 300 µm thick SiC wafer is considered in the

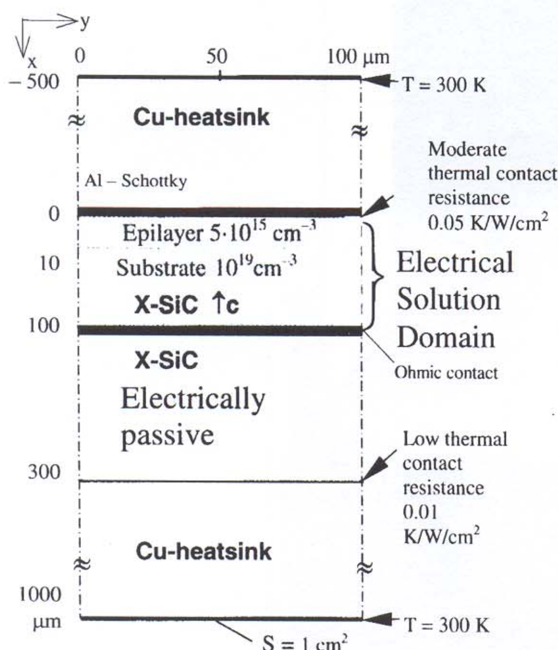

Fig. 1. Description of the electrothermal simulation task (X means either 6H or 4H).

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thermal solution only. The change of the contact metal is assumed to take place exactly at the centre of the 100 μm wide simulation fragment (at $y = 50$ μm). In the present simulation only the abrupt Φ_{bn} (Φ_{bp}) change is analysed considering that this limit case reveals in the clearest way the essential details of the problem. The forward voltage $V < 0$ (n-substrate) and $V > 0$ (p-substrate) is applied to the bottom ohmic contact at $x = 100$ μm, $y =$ 0–100 μm. The Schottky contact is grounded: $V = 0$. The specified Cu heatsink layers model "a nearly ideal cooling package". In contrast to [3,4], part of the cooling is assumed to occur through the upper contact. This choice describes better the reality and also increases temperature changes along the Schottky contact surface.

By default, x-axis is fixed parallel to 6H- or 4H-SiC c-axis and high electron mobility anisotropy is used for 6H-SiC: $\mu_{ny} = 4.8\mu_{nx}$, $\mu_{nx300} = 78.5\ \mathrm{cm^2/Vs}$ (at $T = 300$ K, $N_d = 2.3\times10^{16}\ \mathrm{cm^{-3}}$), $\mu_n(T) \sim T^{-2.07}$ (according to empirical formulae in [5]); here T is the absolute temperature and N_d is the impurity concentration in the semiconductor epilayer. For 4H-SiC, the mobility values were taken as $\mu_{ny} = 0.89\mu_{nx}$, $\mu_{nx300} = 968.0\ \mathrm{cm^2/Vs}$ (at $T = 300$ K, $N_d =$ $2.3\times10^{16}\ \mathrm{cm^{-3}}$) and $\mu_n(T) \sim T^{-1.8}$ [6] (according to empirical formulae in [5]).

3. RESULTS AND DISCUSSIONS

Turn-off processes for complementary 6H- and 4H-Schottky structures were investigated. The stepwise switching process from 5 V forward voltage to 5 V reverse voltage over 0.01 ohm series resistance was assumed to be taking place. The temperature changes have been chosen from 300 up to 900 K. Figure 2 shows the dependence of the switching current on time for the 6H-SiC and Fig. 3 the same function for the 4H-SiC complementary Schottky structures.

Using the 10% rule for determination of the turn-off time (t_{off}), our calculations show that t_{off} for complementary 6H-SiC and n-4H-SiC structures lies between 0.05 and 0.06 ns at room temperature and increases up to the values from 0.07 to 0.08 ns at 900 K. At the same time, the p-4H-SiC has the highest turn-off time (about 0.09 ns) at the room temperature and this value decreases with the temperature increase down to about 0.05 ns. In both cases the temperature influence on the turn-off time has nearly linear character.

It is a clear indication of a different behaviour of p-4H-SiC Schottky structures as compared to other structures. Similar strange behaviour we have observed earlier by the experimental investigations of temperature influence on the U–I characteristics of p-4H-SiC Schottky structures [7].

In the U–I case this strange behaviour can be explained by the mobility of holes in the p-type SiC, which has a relatively weak temperature dependence as compared to electrons, and also by the fact that aluminium doping atoms are not fully ionized. Thus, the increasing temperature influences the turn-off time mainly through the mobility decrease, which in turn causes lower on-state resistance values. The temperature dependence of the barrier height does not play significant role in this process. Due to the fact that the turn-off time can be

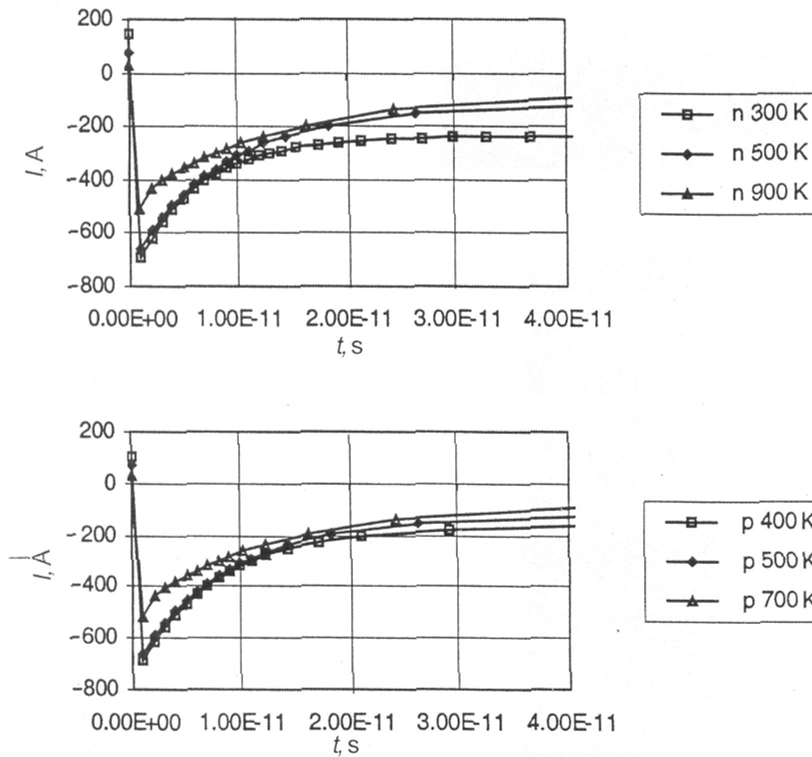

Fig. 2. The current versus time curves for complementary 6H-SiC Schottky structures at different temperatures.

handled as a delay over the Schottky structure, which in first approximation can be described by a simple *RC* chain, we can conclude that the series on-state resistance defines the behaviour of the turn-off time depending on the temperature. Accepting the fact that for all investigated structures the barrier capacity has nearly constant character and there is no charge accumulation of minority carriers in the epilayer, the on-state resistance is the only parameter, which changes the value of the *RC* product and consequently the turn-off time changes in the same way. The decrease of the on-state resistivity is directly defined by the value of mobility of holes over the Schottky structure by increasing temperature.

Our earlier analysis has shown that in p-type silicon Schottky structures the weak, but measurable minority carrier accumulation can be detected in the epilayer near the Schottky depletion layer border [8]. We have not observed such a phenomenon for 6H- and 4H-SiC p-type Schottky structures. The explanation leads back to the quick vanishing of the injected charge of the minority carriers (electrons) in an epilayer outside the Schottky interface for SiC structures. The practically close to zero volume of charge accumulation in the p-type epilayer of the Schottky structure results from the drift-diffusion theory of current transport,

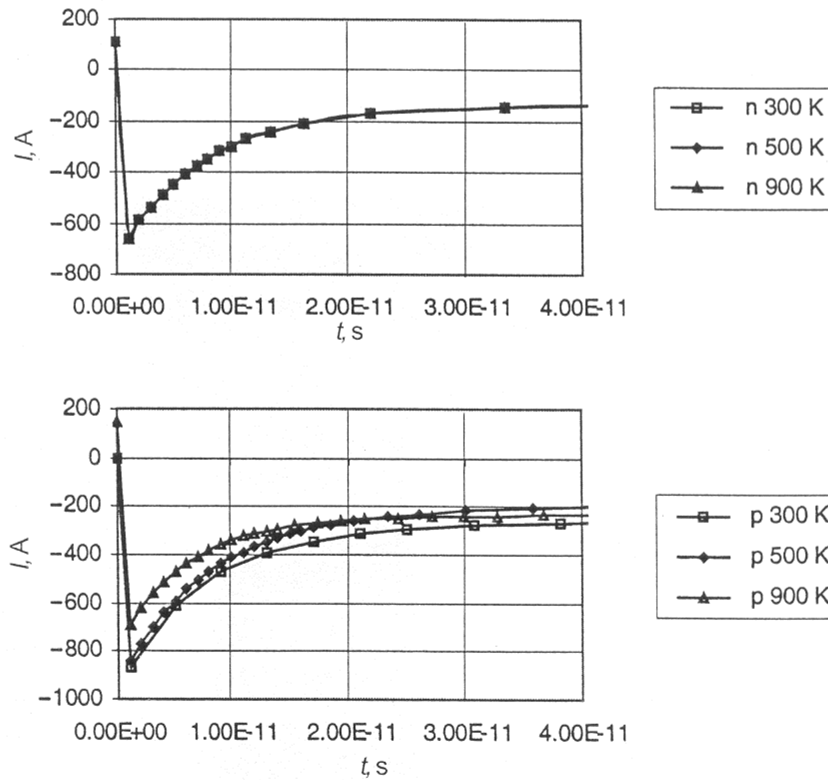

Fig. 3. The current versus time curves for complementary 4H-SiC Schottky structures at different temperatures.

where the minority carriers play significantly smaller role in the SiC epilayer as compared to the Si one and therefore no visible charge accumulation takes place.

4. CONCLUSIONS

A 2D model for the analysis of 6H- and 4H-SiC complementary Schottky structures has been verified. On the basis of our calculations, the turn-off time of the structures has shown nearly linear character under the increase of temperature. The increase of the temperature causes the increase in the turn-off time for 6H-SiC complementary and 4H-SiC n-type Schottky structures. For the 4H-SiC p-type Schottky structures the turn-off time decrease was observed under temperature increase. The reason for such a behaviour can be the decrease of the on-state resistivity under temperature influence. Our calculations show also differences in the behaviour of p-type SiC Schottky structures as compared to similar silicon-based structures. In SiC p-type Schottky structures no minority carrier charge accumulation has been observed in the epilayer outside the Schottky depletion layer.

ACKNOWLEDGEMENTS

The Estonian Science Foundation (grant No. 4869), and the Estonian Academy of Sciences and the Hungarian Academy of Sciences are acknowledged for financial support.

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Komplementaarsete 6H- ja 4H-SiC Schottky struktuuride dünaamilise käitumise uurimine numbrilise mudeli abil

Toomas Rang ja Raido Kurel

On uuritud komplementaarsete 6H- ja 4H-SiC Schottky struktuuride väljalülitusprotsesse erinevatel temperatuuridel. On näidatud, et p-tüüpi epitaksiaalkihiga Schottky struktuuride väljalülitusaeg näitab temperatuuri kasvades kahanemistendentsi, mis erineb oluliselt teiste uuritud struktuuride väljalülitusaegade käitumisest. Tuleb mainida, et vaatamata temperatuuri peaaegu lineaarsele mõjule väljalülitusajale, on selle faktiline muutus siiski suhteliselt suur (ligi 1,5 korda nii suurenemise kui ka vähenemise suunas).

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Numerical Study of Current Crowding Phenomenon in Complementary 4H-SiC JBS Rectifiers

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Keywords: SiC, JBS complementary structures, numerical modeling, current crowding phenomenon.

Abstract. A new type of power semiconductor device – the Junction Barrier Schottky (JBS) diode- has been introduced recently [1]. Our earlier investigations (e.g. [2, 3]) on current crowding effect at Schottky interfaces due to barrier height differences created an idea to investigate the temperature influence on current crowding phenomenon in complementary JBS diodes. The reason for such investigations results from the structure (cross section) of JBS diode, which has three different regions for the current flow through the device under upper metal contact. The MEDICI software package for numerical simulations has been used [4].

The current distribution along the p- and n-4H-SiC structures under different temperatures, epitaxial layer concentrations and barrier heights (work function) conditions have been investigated and the results are presented. The clear differences in current suppressing behavior around the areas, where the arbitrary pn-junction reaches the upper contact of the structures near the edge of Schottky interface can be seen only in some cases. Our simulations show also the weak sides of the p-epilayer SiC JBS, where the temperature influence changes the normal behavior of the device and rearranges the current distribution under higher temperature and barrier height values.

Introduction

Silicon Carbide (SiC) is considered to be a very promising material for high temperature and high power applications due to its high breakdown filed and high thermal conductivity. One possible solution for this approach is the recently introduced new type of power semiconductor device – the Junction Barrier Schottky (JBS) diode [1]. The new type of power devices (JBS) should offer Schottky like on-state and switching characteristics and p-i-n like off-state characteristics. As stated- for example in [1] - the breakdown voltage rating is directly limited by the material and in case of 4H SiC it may reach 3000 V.

Our earlier investigations (e.g. [2, 3]) on current crowding effect at Schottky interfaces due to barrier height differences created an idea to investigate numerically the complementary JBS diodes under different temperatures, epitaxial layer concentrations and barrier heights (work function) conditions. The reason for such investigations results directly from the structure (cross section) of JBS diode, which has three different regions for the current flow through the device under upper metal contact.

This paper presents the comparison of the results of numerical simulations carried out with software package MEDICI for complementary JBS structures for various temperatures, epilayer concentration and Schottky barrier height conditions. The forward characteristics of JBS complementary structures are analyzed.

Description of the Model

The simulated structure is shown in Fig. 1. The upper contact has two different regions. The contact to epilayer is chosen to be a Schottky type and the contacts to p^+ or n^+ side regions are chosen to be Ohmic type. The bottom contact is Ohmic.

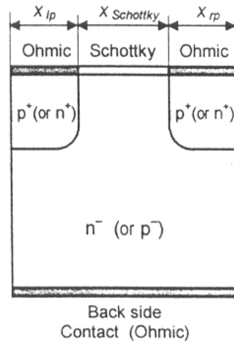

Fig. 1 The cross section of the simulated JBS structure.

The boundary conditions at Schottky contact surface are specified in standard manner, as it appears in MEDICI, e.g. the boundary potential φ_s (bound with band edge energies E_c, E_v) is shifted from bulk (neutral) value so that barrier height for electrons in metal at Fermi level equals to the effective barrier height $E_c - E_{Fm} = q \cdot \Phi_{bn}$ (work function approximation) and carrier surface concentrations are slightly depending on current density via $j_n = q \cdot v_{sn} \cdot (n_s - n_{s0})$ type relations. The lateral sides of simulation fragment are neutral reflecting surfaces (Neumann type boundary conditions $\partial f / \partial y = 0$). The SRH recombination mechanism, avalanche multiplication of charge carriers, barrier lowering at Schottky interface, and band gap narrowing effect has been included.

From physical principles of JBS it is important to keep the Schottky barrier as low as possible to guarantee the low on-state voltage, but at the same time high enough to block the voltage during off-state situation. This requirement has been taken into account for both p- and n-SiC simulations while modeling the Schottky interface and the work function approach gives the best match in that case.

The "work point (WP)" parameters for the structure from Fig. 1 are the following: $N_{epi} = 2 \times 10^{15}$ cm^{-3}, $N_p = 2 \times 10^{19}$ cm^{-3}. For the complementary JBS structure the conductivity types of origin regions have been changed to opposite ones, respectively. The lateral dimensions are $x_{lp} = 1$ µm, $x_{Schottky} = 4$ µm and $x_{rp} = 1$ µm. The depth of the p$^+$-region is 5 µm and the overall thickness of the structure is considered to equal 8 µm. The room temperature is assumed to be equal to 300 K. The mobility temperature dependence is assumed to vary as $T^{-2.3}$ for electrons and $T^{-2.2}$ for holes. The electron-hole scattering is included on base of results from [5]. The values for bandgap narrowing are taken from [6] and the anisotropy phenomenon of mobility is included as foreseen by MEDICI.

The numerical experiments have been defined for temperatures 600 K and 900 K, for epilayer concentrations 6×10^{15} cm^{-3} and 1×10^{16} cm^{-3}, and metal work functions have been chosen on base of assumption that for n-4H-SiC the inequality $\Phi_m > \Phi_s$ has to be fulfilled to realize the Schottky contact. For the p-4H-SiC the opposite inequality $\Phi_m < \Phi_s$ has to be reached.

Results and Discussion

The influence of three important parameters on forward *U-I* characteristics of complementary JBS structures have been investigated.

Fig. 2 shows the behavior of forward current under the influence of ambient temperature. It is clearly seen that forward current of p-SiC JBS structure has a long plateau on low forward voltage values and on temperatures up to 650 K. This is caused by the anisotropic mobility of the majority carriers from the weak accumulation of minority carriers outside the barrier space charge regions as well. Our calculations show also a small increase of leakage current through the side pn-junction at temperatures over 650 K, which can be explained by mobility temperature dependence.

Fig. 3 describes the influence of epilayer concentration on forward current at room temperature. The influence is weak and typical for pure Schottky barriers in case of increasing epilayer concentration. It means that no current redistribution can be observed during the increase of epilayer concentration. The long plateau observed on small forward voltages, has the same reason, as it stated in case of temperature influence on forward characteristic.

Fig. 4 shows the work function (barrier height) influence on forward current at room temperature. In case of p-SiC JBS the unexpected long plateau has been observed on lowest work function value. We believe that the reason for this phenomenon is that the p-SiC Schottky barrier is more close to Ohmic than Schottky interface, and the current flow is defined together by side pn-junction. In case of highest work function values the current distribution has been observed as well. Here the redistribution of the current flow takes place due to side pn-junctions leak, while the high barrier height suppresses the current through the pn-junction.

Summary

An analysis of the behavior of forward characteristics under various ambient (temperature) and technological (epilayer concentration and Schottky barrier height) of complementary JBS rectifiers is presented. Two-dimensional MEDICI analysis gives a clear picture about the advantages and disadvantages of n- and p-4H-SiC JBS complementary structures. From the simulations the following conclusions can be reached:

- Temperature influence is strong and has similar character for both p- and n-SiC JBS structures
- The influence of epilayer doping is weak and the forward current behavior is very close to the one observed in the case of normal Schottky structures without the side pn-junctions inside the device
- The work-function (barrier height) has relatively strong influence on current distribution inside the device. On higher barrier height values the current crowding takes place – the side pn-junction start to conduct the current.

The calculations show also that the influence of mobility anisotropy on forward characteristics can be observed at higher current density conditions (higher temperature or lower barrier height), where the lateral leak starts to be seen and therefore has to be included into model description.

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Numerical Study of Turn-off Phenomenon in Complementary 4H-SiC JBS Rectifiers

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ABSTRACT: A new type of power semiconductor device – the Junction Barrier Schottky (JBS) diode- introduces a current crowding phenomenon at the Schottky interfaces due to barrier height differences. Using the MEDICI numerical software package the turn-off behaviour of complementary JBS structures is investigated. Three different situations along the p- and n-4H-SiC structures under different temperatures, epitaxial layer concentrations and barrier heights (work function) conditions have been investigated and the results are presented.

1 Introduction

Silicon Carbide (SiC) is considered to be a very promising material for high temperature and high power applications due to its high breakdown filed and high thermal conductivity. One possible solution for this approach is the recently introduced new type of power semiconductor device – the Junction Barrier Schottky (JBS) diode [1]. The new type of power devices (JBS) should offer Schottky like on-state and switching characteristics and p-i-n like off-state characteristics. In our previous work [2] from the simulations the following conclusions were reached:

- Temperature influence is strong and has similar character for both p- and n-SiC JBS structures
- The influence of epilayer doping is weak and the forward current behavior is very close to the one observed in the case of normal Schottky structures without the side pn-junctions inside the device
- The work-function (barrier height) has relatively strong influence on current distribution inside the device. On higher barrier height values the current crowding takes place – the side pn-junction start to conduct the current.

This paper presents the comparison of the results of numerical simulations carried out with software package MEDICI [3] for complementary JBS structures for various temperatures, epilayer concentration and Schottky barrier height conditions. The turn-off time of JBS complementary structures is analyzed.

2 Description of the model

The simulated structure is shown in Fig. 1. The upper contact has two different regions. The contact to epilayer is chosen to be a Schottky type and the contacts to p^+ or n^+ side regions are chosen to be Ohmic type. The bottom contact is Ohmic.

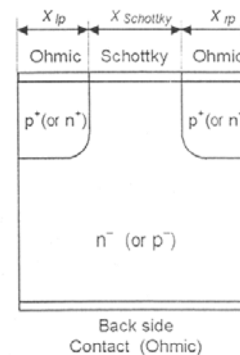


Fig. 1. The cross section of the simulated JBS structure.

The boundary conditions at Schottky contact surface are specified in standard manner, as it appears in MEDICI, e.g. the boundary potential φ_s (bound with band edge energies E_c, E_v) is shifted from bulk (neutral) value so that barrier height for electrons in metal at Fermi level equals to the effective barrier height $E_c - E_{Fm} = q \cdot \Phi_{bn}$ (work function approximation) and carrier surface concentrations are slightly depending on current density via $j_n = q \cdot v_{sn} \cdot (n_s - n_{s0})$ type relations. The lateral sides of simulation fragment are neutral reflecting surfaces (Neumann type boundary conditions $\partial f / \partial y = 0$). The SRH recombination mechanism, avalanche multiplication of charge carriers, barrier lowering at Schottky interface, and band gap narrowing effect has been included.

From physical principles of JBS it is important to keep the Schottky barrier as low as possible to guarantee the low on-state voltage, but at the same time high enough to block the voltage during off-state situation. This requirement has been taken into account for both p- and

n-SiC simulations while modeling the Schottky interface and the work function approach gives the best match in that case.

The "work point (WP)" parameters for the structure from Fig. 1 are the following: $N_{epi} = 2\times10^{15}$ cm^{-3}, $N_S = 2\times10^{19}$ cm^{-3}. For the complementary JBS structure the conductivity types of origin regions have been changed to opposite ones, respectively. The lateral dimensions are $x_{lp} = 1$ µm, $x_{Schottky} = 4$ µm and $x_{rp} = 1$ µm. The depth of the p^+-region is 5 µm and the overall thickness of the structure is considered to equal 8 µm. The room temperature is assumed to be equal to 300 K. The mobility temperature dependence of charge carriers is assumed to vary as $T^{-2.3}$ for electrons and $T^{-2.2}$ for holes. The electron-hole scattering is included on base of results from [4]. The values for bandgap narrowing are taken from [5] and the anisotropy phenomenon of mobility is included as foreseen by MEDICI.

The numerical experiments have been defined for temperatures 600 K and 900 K, for epilayer concentrations 6×10^{15} cm^{-3} and 1×10^{16} cm^{-3}, and metal work functions have been chosen on base of assumption that for n-4H-SiC the inequality $\Phi_m > \Phi_s$ has to be fulfilled to realize the Schottky contact. For the p-4H-SiC the opposite inequality $\Phi_m < \Phi_s$ has to be reached.

3 Results and discussion

We have investigated the influence of three parameters on turn-off time t_{off}. It is well-known that the work function in Schottky barriers plays an important role in forming the barrier height. Not landing in details the barrier height is defined generally as a difference between the work function and electron affinity. Using in our simulations the values for work functions as shown in fig 2, the barrier heights will be in the interval from 1.1 eV up to 1.9 eV for n-SiC JBS structures and in interval from 1.33 eV up to 2.13 eV for p-SiC JBS structures respectively. The electron affinity data used in our calculations is taken from work [6].

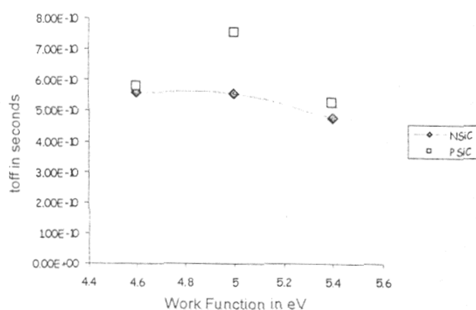


Figure 2. The turn off time versus work function for complementary JBS structures

Fig.2 shows that the t_{off} curve for the JBS structure with p-epilayer has a clearly visible maximum. For the JBS structure with n-epilayer the t_{off} curve differs from this picture. The existence of maximum for JBS structures with p-epilayer has a relatively simple explanation. Due to the lower mobility of majority carriers the current redistribution has the highest level at this particular work function value. From the simulation results it is seen that the current flow redistribution takes place. The surrounding pn-junctions start to inject additional charge carriers into the main current stream area and therefore the total current increases. Consequently the turn-off time is increasing. In case of JBS with n-epilayer the much higher mobility of majority carriers does not lead to such a picture of current crowding around the Schottky junction and therefore the increase of turn-off time is not observed. The decrease of turn-off time at the highest work function values show in both complementary cases the decrease the turn-off time value. The main reason concludes from the barrier height defined by work function. The differences in mobility's of majority charge carriers causing mainly the current crowding in JBS devices does not prevail here by the decrease of the total current defined by the barrier height. The existing current crowding has weak influence on turn-off time.

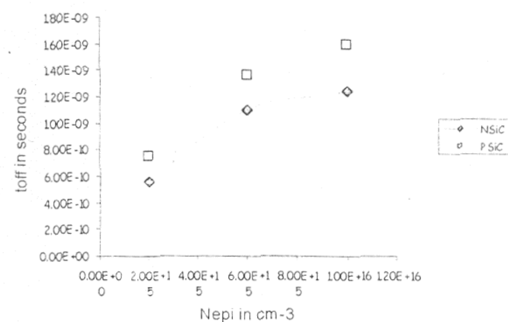


Figure 3. Turn-off time versus epilayer concentration

The epilayer concentration influences similarly both JBS devices with p- or n-epilayer, as it seen on fig.3. The increase in turn-off time concludes from the current behaviour through the whole structure. In case of different epilayer concentrations the simulations show only weak reverse current crowding between the Schottky and pn-junctions, which has the main influence on turn-off time. The higher epilayer concentration influences the duration of turn-off time through the additional charge of minority carriers caused by neighbouring pn-junctions. The extraction of this additional charge introduces a small increase in switch-off time of the JBS devices.

From the fig.4 it is seen that the turn-off time depends on temperature very weakly. And also here the behaviour of the curves has very similar character. The process is mainly explained by the temperature dependence of mobility's of majority carriers and the bandgap thickness.

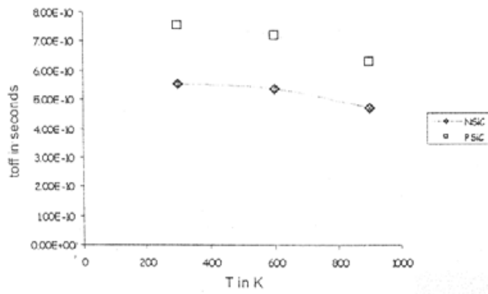
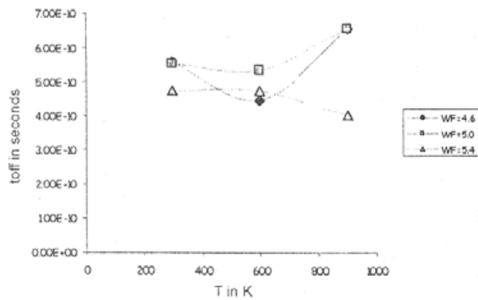
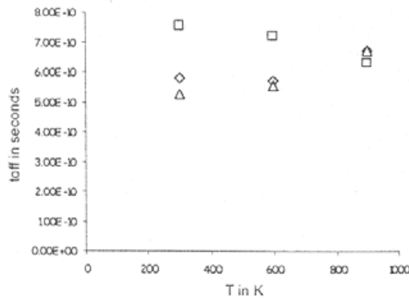


Figure 4. Turn-off time versus ambient temperature



(a)

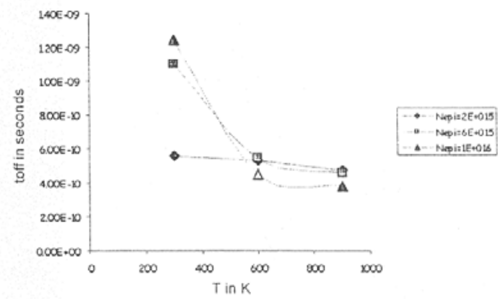


(b)

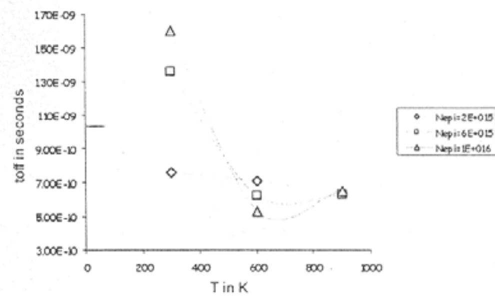
Figure 5. The turn-off time versus temperature at different barrier heights; (a) NSiC JBS device and (b) PSiC JBS device

Our simulations show that it is true for this particular barrier height. which was chosen for the "work point" in our simulations. Analysing the influence of temperature for other values of barrier height the slightly different situation can be observed (fig.5). In case of higher barrier height strong current crowding takes place in both complementary JBS structures. And the total current picture redistribution takes palce in accordance to the values of mobility's of majority carriers. But at higher temperatures (starting from the 600 °K) also the current crowding phenomenon was observed at lower barrier height values. Namely, the additional parallel current component appears through the surrounding pn-junctions. So, the total current adds from two separate components – one through the Schottky interface and another through two pn junctions.

We observed also that in case of low barrier height and at highest temperature the JBS device with p-epilayer does not shot down at all. The additional by electrons induced current was pressed through the neighbouring pn-junctions, which does not allow closing the device. This behaviour was not observed by JBS device with n-epilayer. In that case the holes injection through the pn-junction does not create such a high level additional current, which destroys the shot down mechanism of the device.



(a)



(b)

Figure 6. Turn-off time versus epilayer concentration at various temperatures; (a) NSiC JBS device and (b) PSiC JBS device.

Fig.6 shows the influence of epilayer concentrations on turn-off time under different ambient temperature conditions. For the turn-off process the worst combination is both - the high temperature and the high epilayer concentration. The current flow distribution shows a clear current crowding phenomenon near the

edges, where the Schottky junction transforms to pn-junction. As a result the current is forced to flow through pn- junction and at the highest temperatures the turn-off time starts to increase. The relatively low, and for power devices typical epilayer concentration, forms very regularly behaving curve for turn-off time. The increase of epilayer concentration at higher temperatures decreases the differences for turn-off time values. The JBS structures with highest epilayer concentration do not switch-off at temperatures over 800 °K due to current flowing through the neighbouring pn-junctions.

4 Conclusions

The main conclusions made on base of our calculations are:

- The JBS structures have extremely short turn-off times.
- The change of most important technological parameters (N_{epi} and barrier height) does not have the dramatic influence on turn-off time of complementary JBS structures.
- The influence of temperature in a wide range on turn-off time of complementary JBS structures is also relatively weak.
- Strong redistribution of current flow takes place in case of low barrier height and high epilayer concentration at high temperatures.

Finally we can say that in spite of complicated current flow (current crowding under specific circumstances) in complementary JBS structures the dynamic parameters of the devices are excellent and influenced by current crowding phenomenon only in very specific situations.

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Surface Treatment VI

Computer Methods and Experimental Measurements for Surface Treatment Effects

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Investigation of the combined stress and strain situation in diffusion welded rectifying elements

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Abstract

During the post-bonding cooling process, and due to the differences in the thermal expansion coefficients of the bonded parts, thermal stresses and deformations arise in rectifying elements. The residual stresses and deformations may be the main factor in the subsequent technological treatments and operations. In early papers the regularities of the residual stress and strain situation in general, without examination of the stress distribution along the cross section of the rectifying element during the process of cooling, were observed. The subject of this paper is the use of the finite element method (FEM) and experimental data for investigation of the stress and strain kinetics of rectifying elements during the post-deposition welding cooling process.

1 Introduction

Diffusion welding (DW) is a solid state joining process, which can be utilized to bond "difficult to join" metals or dissimilar material combinations [1].

In the simplest form the DW process includes heating up to a temperature not above the melting point of any of contact materials and compression under a pressure not exceeding the breaking compressive strength of contact materials.

The process of diffusion welding has been known for many years, but only in the last time the application of DW was propagated to power electronics, in particular for metallization of semiconductor structures and bonding of power device heat sink electrodes [2]. The today's power semiconductor rectifying element has traditionally a very thin (250 ÷ 600 μm in thickness) semiconductor wafer bonded with heat sink electrode (tungsten or molybdenium with thickness of 2÷4 mm) over thin (10 ÷ 100 μm) plastic contacting metal (Fig. 1).

The dimensions of modern rectifying elements may be up to 4"diameter. So, the clear view of the stress and strain situation and the ability to control this situation is the essential necessity in the modern semiconductor rectifier production.

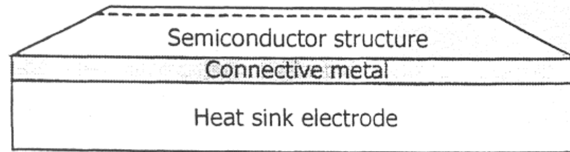

Figure 1: Schematic picture of power semiconductor rectifier.

2 Method

From the standpoint of mechanics, such a structure (Fig. 1) presents the axially symmetric multilayer composite cylinder comprissing layers of elastic and plastic materials. In our case the diffusion welded model for rectifying element has the diameter 40 mm and it is formed on base of 0.6 mm thick silicon semiconductor wafer, bounded with 2 mm thick tungsten disc over 0.1 mm aluminium foil, which is chosen for the basic object in our investigations (Fig. 2).

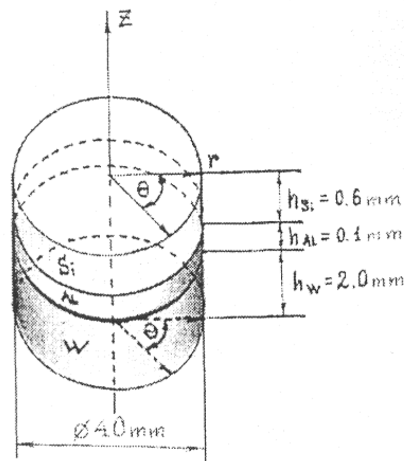

Figure 2: Schematic picture of the basic object in cylindrical coordinates.

For the calculations the Finite Element Method (FEM) was used and the cross-section of rectifying element was broken up into 320 elements with 187 junctions in the way as it is shown in Fig. 3.

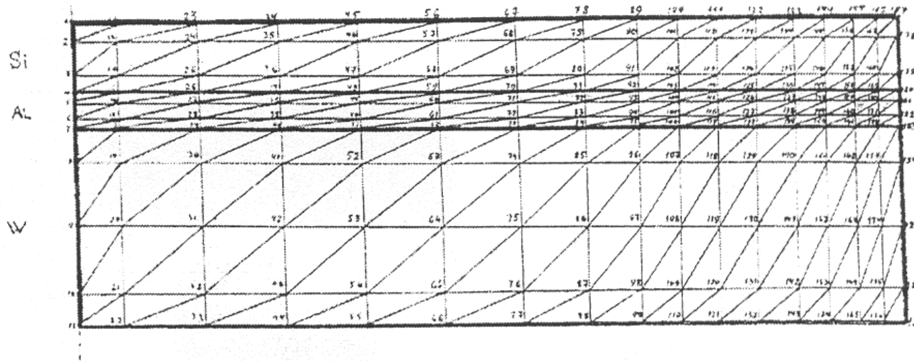

Figure 3: The discretisation picture of the rectifying element.

In the simulations the following assumptions were made. First W and Si were assumed to be elastically deformed over the whole thermo-mechanical stress field and their Young's modulus (E) and the Poisson (ν), factor were assumed to be independent on temperature. Secondly, the aluminium layer was assumed to have only plastio-elastic deformations with negligible linear strengthening in all temperature regions and the creep of the aluminium is not taken into account.

The temperature dependences for main mechanical properties of the materials, going to be welded are shown in Fig. 4.

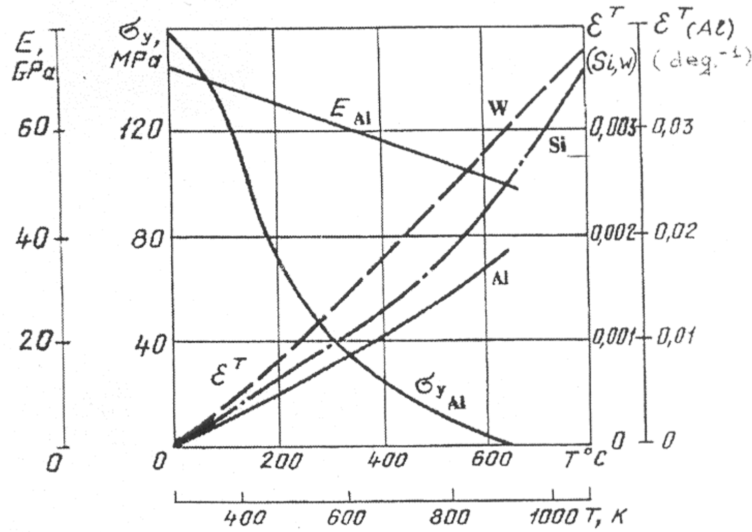

Figure 4: Variation of volume thermal expansion coefficient (ε^T), Young's modulus (E) and yield stress (σ_y) with the temperature.

3 Results

Figure 5 shows the temperature kinetics of radial stress in the cross-section of the rectifying structure.

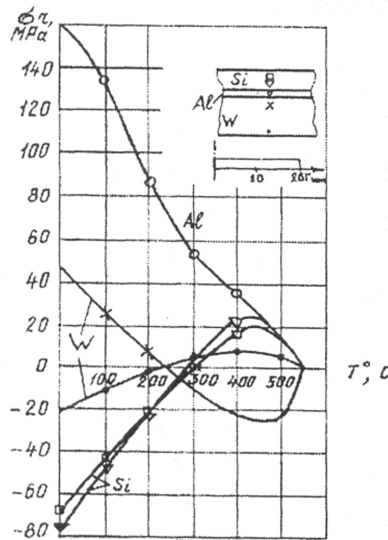

Figure 5: Radial stress (σ_r) kinetics in the section $r = 10$mm.

In the initial cooling stage (from 550° to 300°C) the Si wafer is under tensile radial stress due to higher rate of temperature change compared with W (Fig. 4). Starting from 300°C the compressive radial stresses rise in silicon and they will increase till the temperature reaches the room temperature. In the cooling of tungsten, the bonded face (from 550° to 240°C) stays under the compressive stress, and the opposite (bottom) face will be under tensile stress. At the temperature 240°C the sign of the stresses changes into opposite. In silicon the minimum values of the stress correspond to the temperature close to 300°C. At the temperature 240°C, both tungsten and silicon, loose the stress gradient along the height of the rectifying structure and therefore the rectifying element has not bend deformation at this temperature. The residual stresses have maximum value at the room temperature for all of the layers of the rectifying element. The monotonous increase of tensile stress in aluminium is caused by the increase of its yield stress, when the temperature falls down.

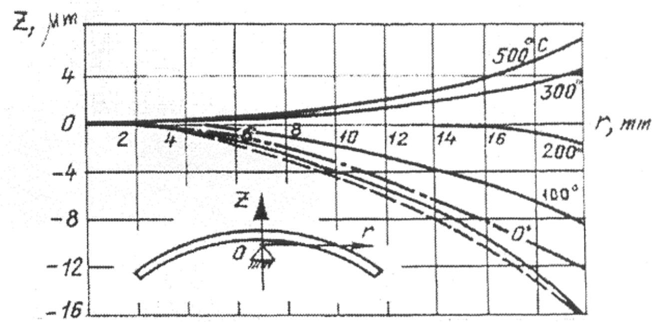

Figure 6: Bending flexure of rectifying element at different temperatures.
_________ FEM solution
_._._._ experimental
- - - - - - - - the ideal spherisity

In the beginning of the cooling process the bend flexure of rectifying element is negative and the changes are in accordance with the kinetic behavior of stresses. At the temperature lower then 240°C the bending flexure becomes a positive sign and at the room temperature the bend flexure has its maximum value (Fig. 6). The calculated and experimental data for bend flexure of rectifying element at room temperature are in a good conformity.

Fig. 7 shows the spread of the residual radial stresses along the height of the rectifying element for different radial cross-sections.

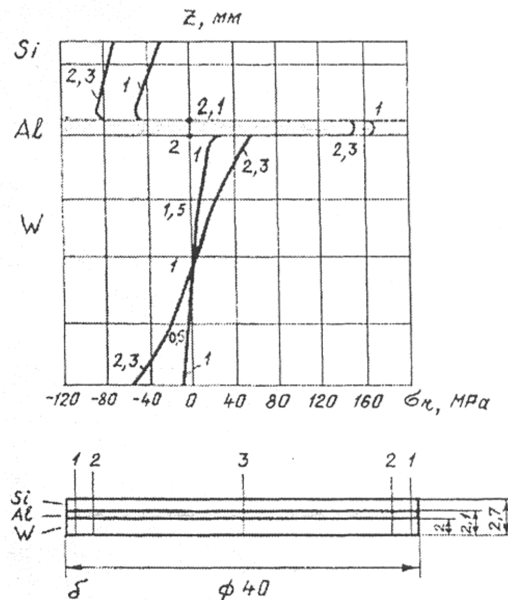

Figure 7: The residual radial stress (σ_r) in different sections of rectifying element.

For silicon the residual stresses across the all sections are compressive character. In tungsten the stresses reverse their sign near the middle of height of the layer, which concludes in the bending of the rectifying element.

As shown in Fig. 8, the radial and circular stresses in silicon on the bonded face are close to constant value along the whole radius, but near the edge side of the rectifier the stress value sharply decreases. The tangential and normal stresses in silicon are negligible along the whole radius with the exception of periphery regions of the rectifier.

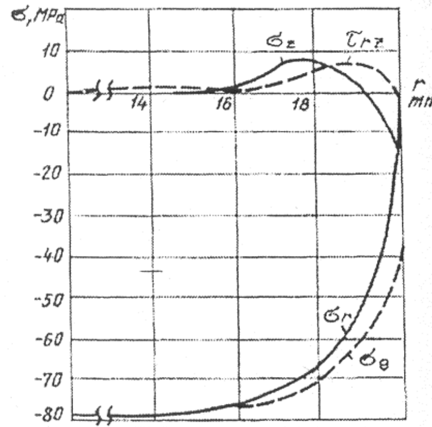

Figure 8: The residual stresses along the radius in bonded face of silicon. (σ_r) – radial, (σ_θ) – circular, (σ_z) – normal, (τ_{rz}) - tangential

The results obtained from FEM simulations form the base of following preliminary conclusions:

- In the after bonding cooling process the values of stresses and bending flexure change the sign.
- The residual stresses and deformation of rectifying element have maximum value.
- Despite the bending deformation of rectifying element, the majority of silicon area is under the plane compressive stress and only in a narrow periphery zone silicon is bulk stressed.
- The stress and strain situation in tungsten is close to classic bend, and deformation behavior of tungsten during the whole after bonding cooling process is dominating for the full construction.

4 Analytical solution

The FEM calculations give reasonably exact and acceptable issues, which are in a good agreement with the experimental results. Nevertheless, the FEM stays to be

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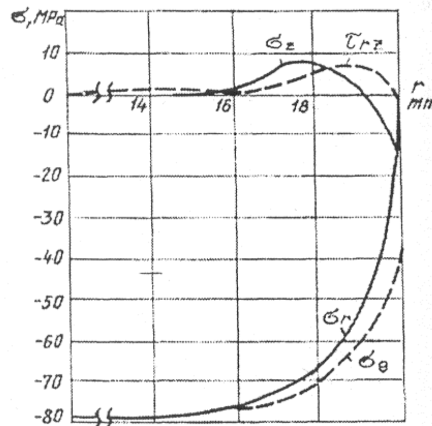

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4 Analytical solution

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comparatively complicated method for first approximation analysis in quick engineering exercises. In paper [3] Karkhin et. al. suggested a simple two equation analytical solution for stress calculations, which bases on theory of thermo-elasticity for plate like cylindrical configurations.

$$\begin{cases} p\tfrac{1}{2}\sum_{i=1}^{n_i} D_i\left(Z_{i+1}^2 - Z_i^2\right) + q\sum_{i=1}^{n_i} D_i\left(Z_{i+1} - Z_i\right) = \sum_{i=1}^{n_i} C_i\varepsilon_i^T\left(Z_{i+1} - Z_i\right) - \sum_{j=1}^{n_j} C_i\sigma_{yj}\left(Z_{j+1} - Z_j\right) \\ p\tfrac{1}{3}\sum_{i=1}^{n_i} D_i\left(Z_{i+1}^3 - Z_i^3\right) = q\tfrac{1}{2}\sum_{i=1}^{n_i} D_i\left(Z_{i+1}^2 - Z_i^2\right) \\ \quad = \tfrac{1}{2}\sum_{i=1}^{n_i} C_i\varepsilon_i^T\left(Z_{i+1}^2 - Z_i^2\right) - \tfrac{1}{2}\sum_{j=1}^{n_j} C_i\sigma_{yj}\left(Z_{j+1}^2 - Z_j^2\right) \end{cases} \quad (1)$$

where p is rotation, q is radial shift, z_i is the coordinate of the elastic layer; z_j is the coordinate of the plastic layer, n_i is the number of elastic layers; n_j is the number of plastic layers, $\varepsilon^T{}_i$ is thermal expansion coefficient of i-th layer, and σ_{yj} is the yield stress of j-th layer.

$$\begin{aligned} D_i &= 2(\mu + \lambda); \quad C_i = 3\lambda + 2\mu \\ \mu &= E/2(1+\nu); \quad \lambda = \nu E/(1+\nu)(1-2\nu) \end{aligned} \quad (2)$$

where E is Young's modulus and ν is the Poisson coefficient.

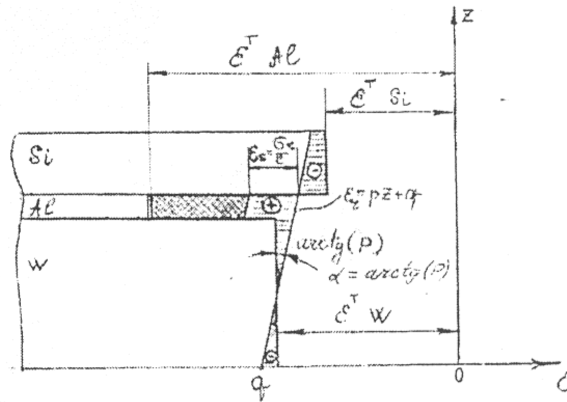

Figure 9: Graphical idea of the analytical solution.

The solution of the equation (1) for p and q determines the deformation ε^T and corresponding ε_{θ}, σ_r, and σ_θ for every part of the rectifying element. The graphic idea of the approximate analytical solution is shown in Fig. 9.

The comparison of the results from FEM and the further described analytical method is shown in Figures 10–13, where the dependences for residual stresses and deformations versus tungsten and aluminium thickness are presented.

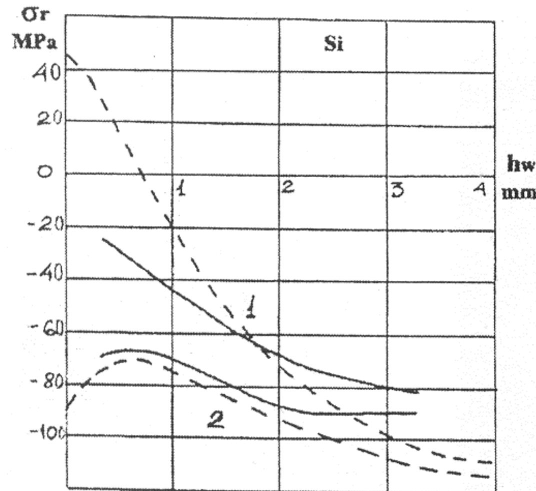

Figure 10: Residual radial stresses on the top (1) and bonded (2) faces of silicon vs. tungsten thickness (h_w)
___________ FEM solution
--------------- analytical solution

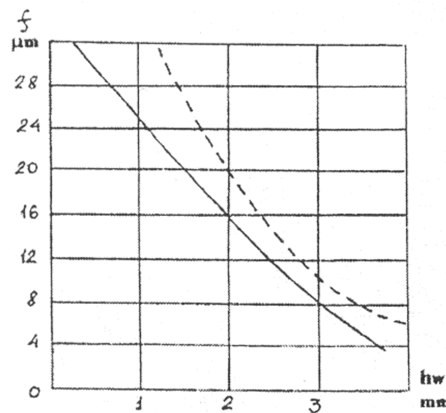

Figure 11: Bending flexure of rectifying element (f) dependence on tungsten thickness (h_w).
___________ FEM solution
--------------- analytical solution

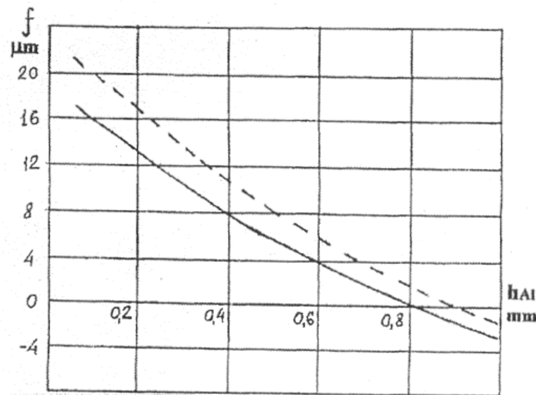

Figure 12: Bending flexure of rectifying element (f) dependence on aluminium thickness (h_{Al}).
__________ FEM solution
-------------- analytical solution

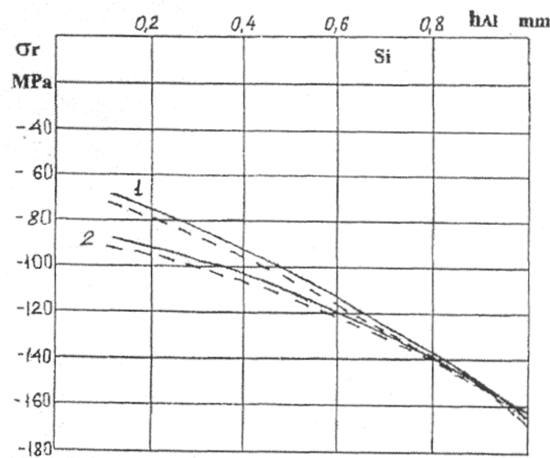

Figure 13: Residual radial stresses on the top (1) and bonded (2) faces of silicon vs. aluminium thickness (h_{Al}).
__________ FEM solution
-------------- analytical solution

5 Conclusion

This paper summarizes how to use FEM and analytical techniques for stress analysis in power semiconductor structures. The conclusions, what we present on the base of our results are:

- During the after bonding cooling process, and due to the difference in the thermal coefficients of bonded materials, the stresses and deformations generally rise in the rectifying element. Over the whole cooling process the stresses and deformations change their sign and value at certain ambient temperature, which concludes after this temperature change point in monotonous increase of their values up to the room temperature. The residual values of stress and deformation are the maximums.
- Changing the thickness of electrode and/or connective metal, the stresses and deformation in rectifying element can be directed into proper relation (stress and strain specific optimal solution).
- The diffusion welding process allows to control completely after bonding cooling stress and strain situation. The unique character of the DW process (solid state bonding, based on the surfaces-chemical reactions) removes a series of technology and physics based limitations, which are typical for traditional metallization methods.

Thus, FEM coupled with analytical solution opens an approved practice for novel designs and improvements as well in power semiconductor rectifier production.

Acknowledgement

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Two-dimensional nonisothermal analysis of the current crowding effect at nonuniform SiC Schottky contacts using device simulator DYNAMIT-2DT

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ABSTRACT: The current crowding at variable barrier SiC Schottky contacts has been earlier investigated using SPICE-based electro-thermal modeling. At that strong current peaks at low-barrier contact edges have been predicted. In present work a precise study for n-6H-SiC–Au/Pt structure on-state and turn-on operation is performed using two-dimensional nonisothermal drift-diffusion device simulator DYNAMIT-2DT. The heat flow in cooling environment surrounding the SiC structure is considered and the direct influence of current density and electron mobility anisotropy on current "push-out" and "peak" region dimensions is shown.

1 Introduction

The problems with current redistribution at nonuniform Schottky contacts were recognized in the beginning of 1980-ies [1,2]. More practical modeling efforts were made in the beginning of 1990-ies [3,4]. At that time intensive research of the silicon carbide, a very promising wide band gap semiconductor material was started and the importance of current crowding effect in SiC was predicted [5,6]. In SiC the barrier height Φ_{bn} differences (1.52/1.04V for 6H-SiC–Au/Pt, 1.72/1.04V for 4H-SiC–Au/Pt [7,8]) are comparable to the Φ_b absolute values for Si. Since Φ_b defines the barrier forward voltage drops, remarkable high-barrier regions will be shunted off from current conductance and correspondingly strong current peaks at the low-barrier contact region edges appear.

In [5,6] this problem was analyzed by SPICE circuit simulator describing the semiconductor 2D-region by the net of resistors and the Schottky barrier by the ideal diodes $j=j_s\cdot[\exp(V/\varphi_T)-1]$ with the saturation currents $j_s\sim\exp(-\Phi_{bn}/\varphi_T)$ strongly depending on the local barrier height according to the traditional Schottky contact theory. In [9,10] the steady-state heat flow quasi-electrical subtask was added to the SPICE-simulator. Despite strong current peaks up to 4-5 times over average level, the considered self-heating caused rather small temperature nonuniformities (typically <1K) at contact. However, this simulation technique remains very restricted by the computational and physical parameters specification.

In the present paper the current concentration and temperature rise precise study for n-6H-SiC-Au/Pt Schottky structure on-state and turn-on operation is performed using two-dimensional nonisothermal drift-diffusion device simulator DYNAMIT-2DT, earlier developed in TTU Department of Electronics [11,12].

2 Model and structure description

The simulator solves Poisson and continuity equations for electrons and holes (holes negligible in the present case) in semiconductor "electrical solution domain" and heat flow equation for the greater "cooling package domain" (see Fig.1). The boundary conditions at Schottky contact surface are specified in standard manner, applied in most of device simulators: the boundary potential φ_s (bound with band edge energies E_c,E_v) is shifted from bulk (neutral) value so that barrier height for electrons in metal at Fermi level equals to the effective barrier height $E_c-E_{Fm}=q\cdot\Phi_{bn}$ and carrier surface concentrations are slightly depending on current density via $j_n=q\cdot v_{sn}\cdot(n_s-n_{s0})$ type relations. The barrier lowering due to the surface electric field (i.e. Schottky effect) is here not included assuming that the effective (empiric) Φ_{bn} values already include influence of this effect.

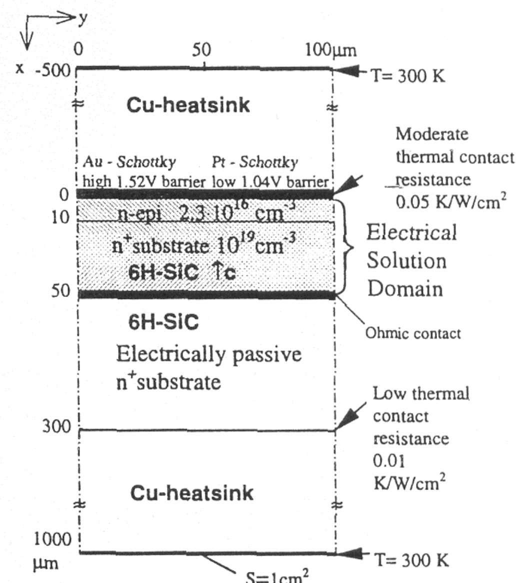

Fig.1 Electrothermal simulation task description

The 100μm wide structure fragment was selected for simulation, assuming that characteristic lateral scale of the current crowding effect is several times below that limit. The lateral sides of simulation fragment are neutral reflecting surfaces (Neumann type boundary conditions

$\partial f/\partial y=0$). In vertical direction, to reduce the meshnodes number, only the $0\leq x \leq 50\mu m$ region was included in "electrical solution". The rest of 300μm thick SiC wafer is considered in thermal solution only. The change of contact metal is assumed to be exactly at 100μm wide simulation fragment center at y=50μm. In present simulation only the abrupt Φ_{bn} change is analyzed considering that this limit case reveals in the clearest way the essential details of the problem. The forward voltage V<0 is applied to the bottom ohmic contact at x=50μm, y=0÷100μm. The both Schottky contacts are grounded: V=0. The specified Cu heatsink layers model "a nearly ideal cooling package". In contrast to [9,10], part of cooling is assumed to occur through the upper contact. This choice describes better the reality and also increases temperature changes along Schottky contact surface.

By default x-axis is fixed parallel to 6H-SiC c-axis and high electron mobility anisotropy is used: $\mu_{ny}= 4.8 \times \mu_{nx}$, μ_{nx300}= 78.5 cm^2/Vs (at T=300K, $N_d=2.3\cdot 10^{16}cm^{-3}$) , $\mu_n(T)\sim T^{-2.07}$, according to empirical formulae from [13].

3 On-state results

Fig.2 shows the calculated I/V curves and corresponding temperature differences rise in semiconductor structure when applied voltage is increased up to 5V (average current density up to 743 A/cm^2). As expected, the threshold voltages of two contacts differ ca 0.5V following the barrier difference. At higher currents the ohmic voltage drops determine the I/V curves.

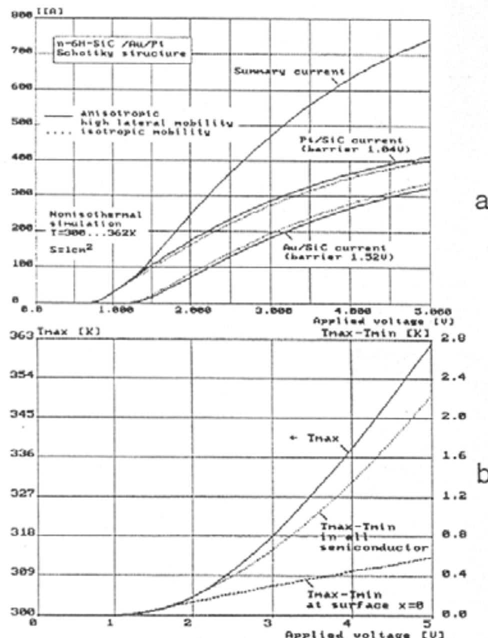

Fig.2 I/V characteristics (a) and increase of temperature differences (b) in active semiconductor structure ($0\leq x \leq 50\mu m$) and at surface of the Schottky contact (x=0) .

At that observed I/V curves nonlinearity is result of mobility decrease as $\mu \sim T^{-2.07}$. In the case of anisotropic high lateral mobility the redistribution of current from Au-contact to Pt-contact is slightly greater than in the case of isotropic mobility. Fig.2b shows that the self-heating of the structure reaches 63K but the temperature difference along contact surface rises only up to 0.6K. The full temperature map is presented in Fig.3 and the temperature distributions through all SiC and Cu layers are shown in Fig.4. Fig.5 reveals that there exists indeed very small area (0.5 × 0.3μm) with high Joule heat generation near the low-barrier contact edge. However, due to high thermal conductivity of SiC this peak is not able to change rather flat temperature-distributions and cause appearance of local temperature maximum.

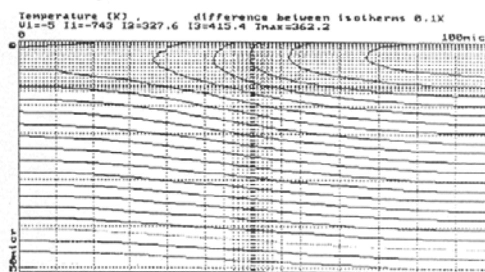

Fig.3 Temperature isotherms map with 0.1K step at maximum forward voltage 5V. In the background meshlines are shown

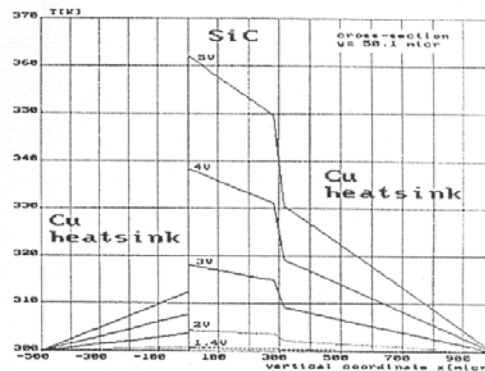

Fig.4 Temperature distributions through all semiconductor and heatsink layers at different forward voltages

Fig.5 Heat generation peak localization (2μm × 1μm zoom)

Figs. 6 and 7 present the important details of the contact current redistribution. Fig.6 shows that the characteristic size of the "peak" region is ≈1μm (≈0.5μm for isotropic μ_n) and this is not depending on current

density. The "push-out" region is 2-3 times wider and increases at lower current densities approximately as $1/\sqrt{j}$. The current peak is actually located inside the low-barrier part, ca 0.1µm from contact metal change. Comparison of anisotropic and isotropic cases showed that the "push-out" and "peak" region sizes increase with lateral mobility as $\sqrt{\mu}$. The extra current in "peak" region is roughly equal to the uncollected current in "push-out" region.

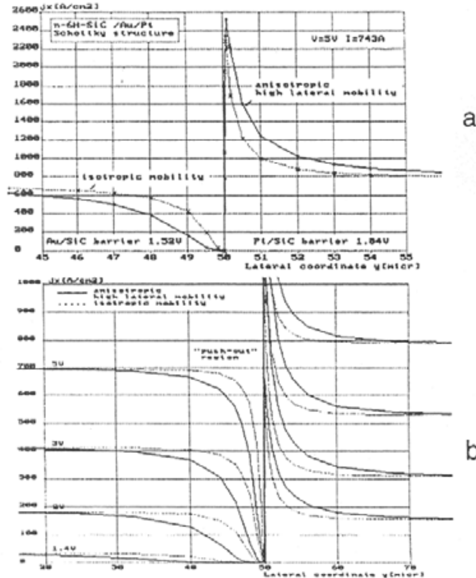

Fig.6 Current density at contact surface: details for forward bias 5V (a) and larger scale comparison for different bias points (b)

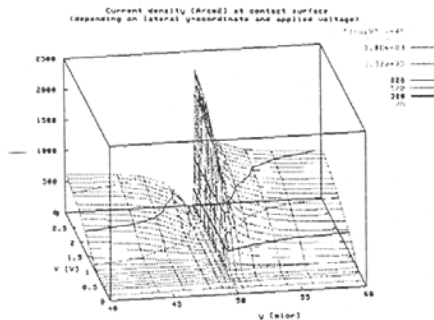

Fig.7 Isometric presentation of the contact surface current density distributions $j_x(y, x=0)$ for all voltage range 0÷5V

Figs. 8 - 10 present details of current density distribution. Fig.8 shows that below the "push-out" region (y≅35÷50µm) at contact, at some depth x>0 the dense current flowlines are positioned parallel to surface indicating strong lateral j_y component. Consequently, despite low j_x, the current density module $j=\sqrt{(j_x^2+j_y^2)}$ remains high. This is confirmed by Fig.9 where at depth x≈0.3µm current density module is not influenced by the presence of the "push-out" region at x=0. This role of j_y component is one additional reason why expected temperature minimum is not appearing near the "push-out" region. Fig.10 illustrates the influence of the lateral conductivity on the form of the high current area.

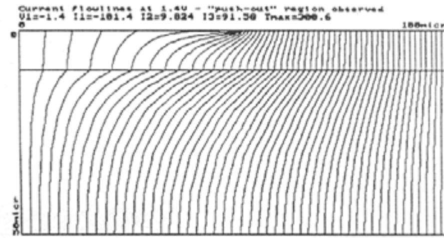

Fig.8 Current flowlines map for the 1.4V voltage point.

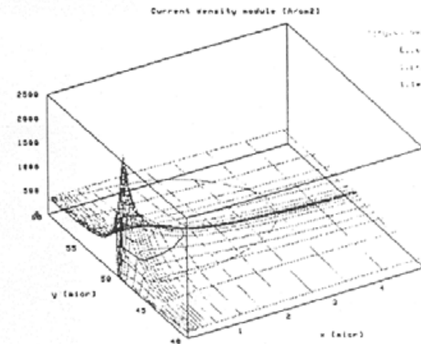

Fig.9 Current density module distribution j(x,y) at forward voltage 2V

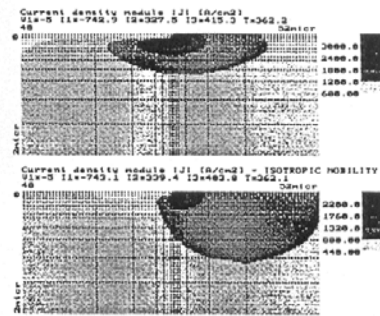

Fig.10 Comparison of the high current density regions for anisotropic and isotropic mobility cases (2µm × 4µm zoom)

3 Turn-on results

As shown above, in spite of strongly nonuniform heat generation, in 100µm distance scale the heat conductivity suppresses any remarkable temperature differences ΔT in steady-state operation mode. Larger ΔT may appear in fast transient processes when local temperature follows local heat generation rate. To confirm this possibility, a turn-on simulation (5V forward voltage pulse, slope 1V/µs) was performed. The results are presented in Fig.11 and 12. The thermal time constant of the investigated structure with heatsink is approximately 1ms (Fig.11b). The

obtained maximum ΔT=3.25K within active semiconductor ($0 \leq x \leq 50\mu m$) is indeed greater than similar steady-state value 2.3K (Fig.2b). However, expected increase of dynamic ΔT at Schottky contact surface is negligible (Fig.11b).

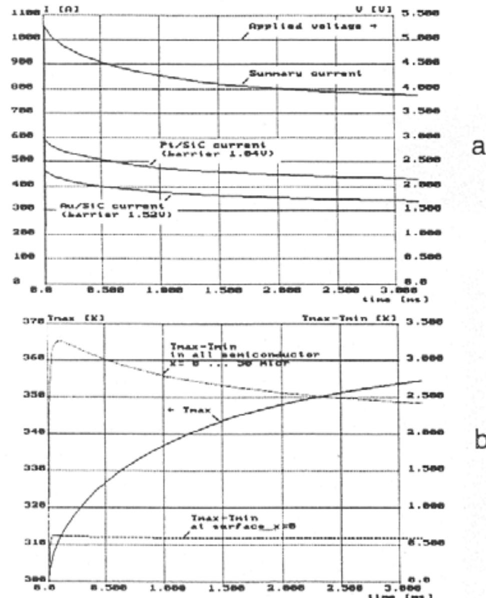

Fig.11 Current transients as response to 5V forward voltage step (a) and dynamics of corresponding temperature differences (b)

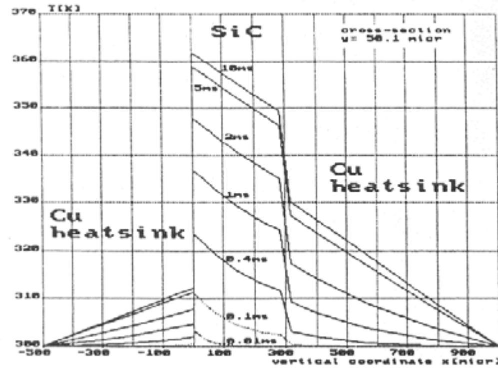

Fig.12 Dynamics of temperature distributions through all heatsink layers in turn-on process

4 Conclusion

The presented exact nonisothermal 2D-simulations confirmed the remarkable current concentration and redistribution at nonuniform Schottky contacts and revealed many important details of those phenomena. The relevant temperature differences within SiC structure were however rather small for steady-state and for transient operation as well.

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