TALLINNA TEHNIKAÜLIKOOL
TALLINN UNIVERSITY OF TECHNOLOGY

Faculty of Information Technology

Thomas Johann Seebeck Department of Electronics

Chair of Communicative Electronics

IEE70LT

Aleksandr Pyatibratov [IAEM105052]

DC regulators

The laboratory work

Master's thesis

Supervisor: Mihhail Pikkov

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Associate professor

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Author's Declaration

I have written the Master's thesis independently. All works and major viewpoints of the other authors, data from other sources of literature and elsewhere used for writing this paper have been referenced.

Master's thesis is completed under associate professor Mihhail Pikkov supervision.

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..... chairman of defence commission

"....."..... 2014.

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Aleksandr Pyatibratov

DC regulators.

The laboratory work.

Abstract.

This work considers matter such as: converter type of voltage regulation, pulse-width adjustment, development of control systems, researching of power units and their different modes. The main objective of this work is to research PWM methods in DC converters and develop a laboratory model. Subsequently work out a manual for a laboratory work.

The developed laboratory model makes it possible to convert unregulated DC input voltage into a controlled DC output voltage at a desired voltage level. Technically the control system that is made on the base of timer circuits and MOSFET driver microcircuit is used to control signals that are transferred to the power unit, based on switch circuits. Thus, PWM regulation has been implemented. Two basic types of DC converters are researched: Buck and Boost to study operation processes of PWM in different conduction modes, that is possible using the oscilloscope. Converters' regulation characteristics are presented in graphs.

The scheme was developed using different types of multivibrators, voltage driver, filters, key-transistors and other electronic components. As a result, there was designed a laboratory layout model that makes possible to study PWM processes in basic DC converters.

In the appendix could be found the results of the accomplished laboratory work .

The Master's thesis is written in English and contains 81 pages, 9 chapters, 57 figures, 3 tables and 5 appendices .

Aleksandr Pjatibratov

Alalispinge regulaatorid.

Laboratoorne töö.

Annotatsioon.

Antud töös käsitletakse selliseid küsimusi nagu muundurite pinge reguleerimine, impulsi-laiuse reguleerimine, kontrollsüsteemi areng, jõuosa uurimine ja erinevate voolurežiimide analüüs. Töö põhieesmärk on uurida pulsilaiusmodulatsiooni (PLM) meetodit alalispinge muundurites ja arendada laboratoorset mudelit ning seejärel välja töötada laboratoorne töö.

Arendatud laboratoorne mudel võimaldab muundada reguleerimata alalispinget reguleeritud pingeks. Tehnilisest vaatepunktist on reguleerimissüsteem koostatud taimeri mikroskeemide ja MOSFET draiveri mikroskeemi põhjal. Reguleeritud signaal saadetakse edasi jõuosasse, mis põhineb lüliti skeemidel. Seega PLM rakendatakse skeemis. Töös on uuritud kahte peamist alalispinge muunduri tüüpi: Buck ja Boost – et uurida kasutades ostsilloskoopi PLM-i tööprotsesse erinevates juhtivusrežiimides.. Muundurite regulatsiooni karakteristikud on esitatud graafikutel.

Skeemi koostamisel olid kasutatuses erinevad multivibraatorid, pinge draiver, filtrid, lüliti-transistorid ja muud elektroonikakomponendid. Tulemusena oli modelleeritud laboratoorsete tööde jaoks makett, mis võimaldab uurida ja aru saada PLM-i protsessidest ja põhilistest alalispinge muunduritest.

Töös on esitatud läbiviidud laboratoorse töö tulemused.

Magistritöö on kirjutatud inglise keeles ning sisaldab 81 lehekülge teksti, 9 peatükki, 57 joonist, 3 tabelit ja 5 lisa.

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Introduction.

Supply issues of modern electronic devices are becoming increasingly important. Creating efficient DC converters (DCC) is an important task in the field of electric power supply for various devices. With the help of such converters engineers are able to solve the problem of creating highly efficient DC electrical drives, controlled power supply, industrial equipment. DC converters are the basis of pulse power supply for computers, audio and video devices, and domestic appliances. One of the most promising areas of converters' application is a rolling stock of suburban, urban and industrial transportation, including also independent supply sources.

Working electromagnetic processes in the different DCC are known with a specific complexity. Appropriate understanding of the construction and application of DCC requires a thorough acquaintance with the principle of work.

The effective learning of DCC during courses of "Power Electronics" is impossible without laboratory work on this topic. Moreover, there should be designed an educational laboratory model that allows to observe and explore the diversity of the flowing electromagnetic processes in DCC. It is also important to get acquainted with the basic properties and measure output characteristics.

Thus, it is obvious that the development of the modern laboratory model "Dc converters" is constructively relevant. This thesis is devoted to designing such training equipment.

1. Short overview of DC converter circuit

1.1 An overall block diagram of DC converter.

DC converters (DCC) are self-contained converters and could be assembled on the base of block diagram Fig.1.1

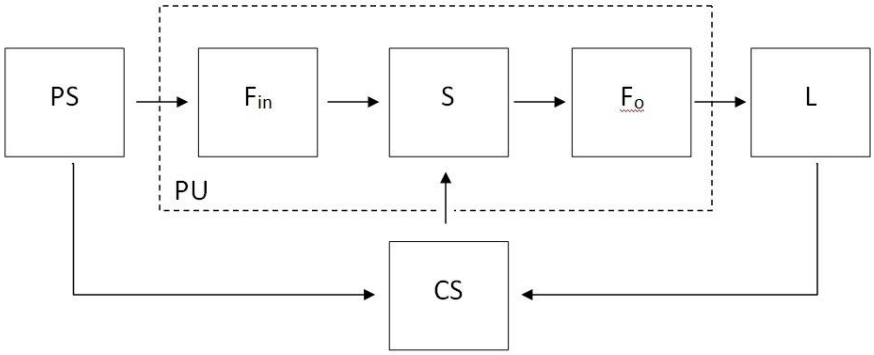

Figure 1.1 Generalized block diagram of DC converter.

A converter is usually consisted of Power Unit (PU) and Control System (CS). PU and CS of a converter get power from Power Supply (PS). Converter's output signal is transferred to Load (L). If the stabilization of output voltage should be implemented in a converter, then the signal of a special type proceeds to CS. Generally PU consists of input filter F_{in} and output filter F_{out} and also key circuit (S) [1÷6].

PS is used in primary and secondary DC electric power sources. Primary power sources are galvanic cells, batteries, DC electromagnetic generators, solar and fuel cells, etc. Secondary power sources include various rectifier units.

The necessity of F_{in} is in reducing the output resistance of PS, smoothing voltage ripple , ensuring the work efficiency of PU in case of rippled consumed current. For the input filter F_{in} there are often used a capacitive or an inductive-capacitive filters, consisted of inductor connected in series with parallel connection of capacitor. There are also used inductive-capacitive filters that have more complex configuration ("LC Ladder filters") consisting of multiple inductors and capacitors.

With the help of Switch (S) pulse voltage conversion is performed in DCC. S usually consists of current interrupter, current-forming inductor, cutting-off diode. During high power usage conventional thyristors with forced commutation nodes are employed as key-schemes. For small and medium power levels S is built on the basis of the totally controlled semiconductor devices. Output filter F_o generally contains an inductor for decreasing current and voltage ripple of a Load (L). For the same purposes output capacitor could be used in the circuit. DC converters act on a Load (L), which could be resistive or resistive-inductive. Quite often a DC-motor is used to be as a Load for converters. Control System (CS) produces operating signals for a switch-circuit S. At the same time voltage converting is implemented by one of the methods described in the next chapter.

1.2 The main methods of DC conversion.

DC (direct voltage) converter in basic state provides a Load with voltage pulses, which have pulse length (t_i) and full period (T) of a signal.

Changing the Duty cycle: $D = t_i / T$, average value of load's voltage could be regulated. It is also possible to regulate Duty cycle, changing t_i or T parameters.

Basically there are 3 common methods of conversion used:

Constant duration of a period.

$$T = K_1 \quad (1.1)$$

Constant duration of a pulse.

$$D \times T = K_2 \text{ or } T = K_2 / D \quad (1.2)$$

Constant duration of a pause.

$$(1- D) \times T = K_3 \text{ or } T = K_3 / (1- D) \quad (1.3)$$

**where K_1, K_2, K_3 – constants

All three methods are shown in the Fig.1.2

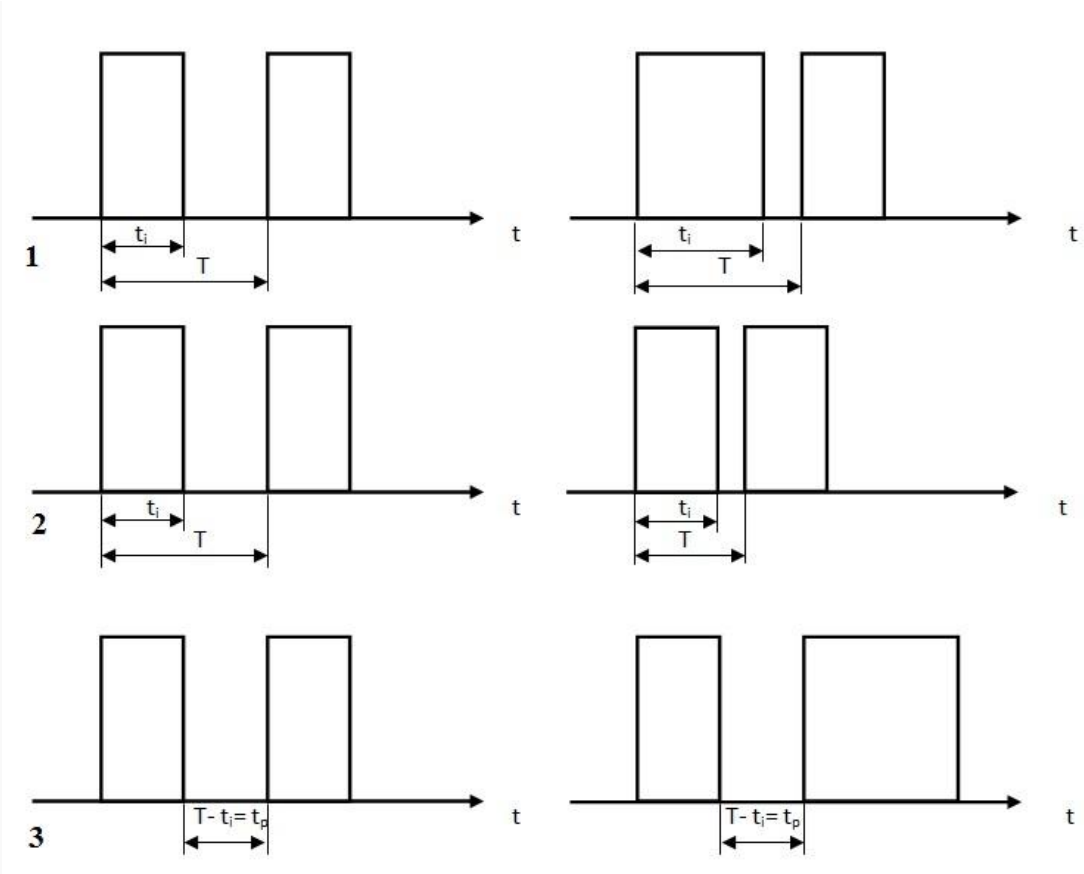

Figure 1.2 Methods of output DC conversion : 1 - constant duration of a period, 2 - constant duration of an impulse, 3 - constant duration of a pause.

Currently, the first of these methods is the most widely used. It is called pulse-width modulation method (PWM). Its advantage compared to the others is in the best smoothing of controlled voltage. The second and third methods of controlling are often used on the base of a thyristor voltage converter switch-circuit that simplifies the modeling of forced commutation thyristor's node. In order to reduce switching losses in a switch-circuit S with a deep regulation of high-power unit loads (for example, in electric drives of urban electric transport) the first method is used in combination with one of the remaining two.

1.3 The main circuits of DC voltage converters.

Nowadays widely used in practice three main types of pulsed DC voltage converters : buck, boost and inverting (DCC1, DCC2 and DCC3) . There are also other voltage converters derived from basic converters: Cuk converter, half-bridge, full-bridge, push-pull, etc. In this work we are going to consider only the basic converters DCC1 and DCC2. By type of energy consumed from the input voltage source and transmitted to the load converters differ as follows:

• pulse energy consumption from the input voltage source and continuous transmission of the energy to the load at DCC1 .

• continuous consumption of the energy from the input voltage source and the pulse transmission of the energy to the load at DCC2 .

• pulse energy consumption from the input voltage source and the pulse transmission of the energy to the load at DCC3 .

By the level of the average value of the output voltage U_o against the input voltage E, converters vary in accordance with the inequalities:

For DCC1 (buck): $U_o = E \times D < E$ (1.1)

For DCC2 (boost): $U_o = E \times D / (1-D) > E$ (1.2)

For DCC3 (inverting): $U_o = E \times D / (1-D) >$ or $< E$ (1.3)

1.3.1 Step-down (buck) converter, DCC1 type.

Basic Step-down converter circuit is shown in Fig.1.3, and timing diagrams illustrate the operation of the converter in the mode of continuous and discontinuous-conduction modes in the inductor's steady state - in Fig. 1.4.[4]

The principle of operation of the circuit: when the A-key switch is on, the diode is closed and is under reverse voltage E. At the time interval $t_i = D \times T$ (impulse width duration) of regulating key energy consumed from the input voltage source is transferred to the load and increases the current in the inductor L. When the control key is off, the EMF generated on inductor's winding, activates the diode VD. During switch off time t_p (pause duration) the energy stored in the inductor, transfers some of its stored energy to the load , that leads to a reduction of current in the inductor. C capacitor smoothes the ripple voltage at the load coming from the ripple current in the inductor, providing low output voltage ripple.

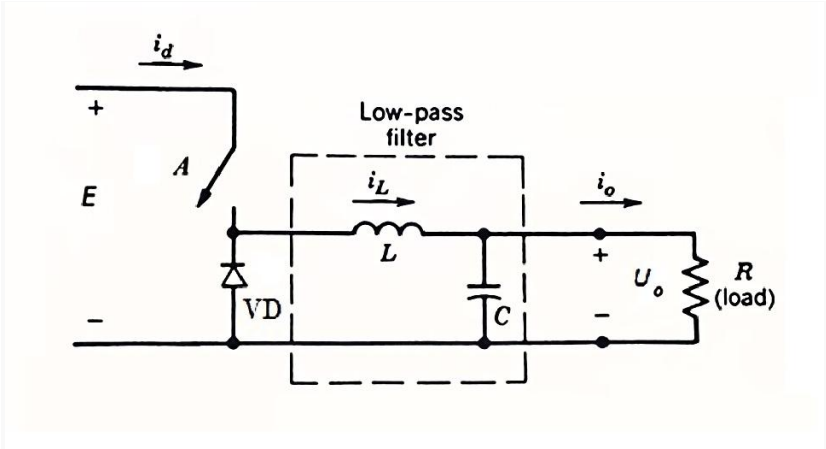

Figure 1.3 Step-down (Buck) converter, DCC1 type.

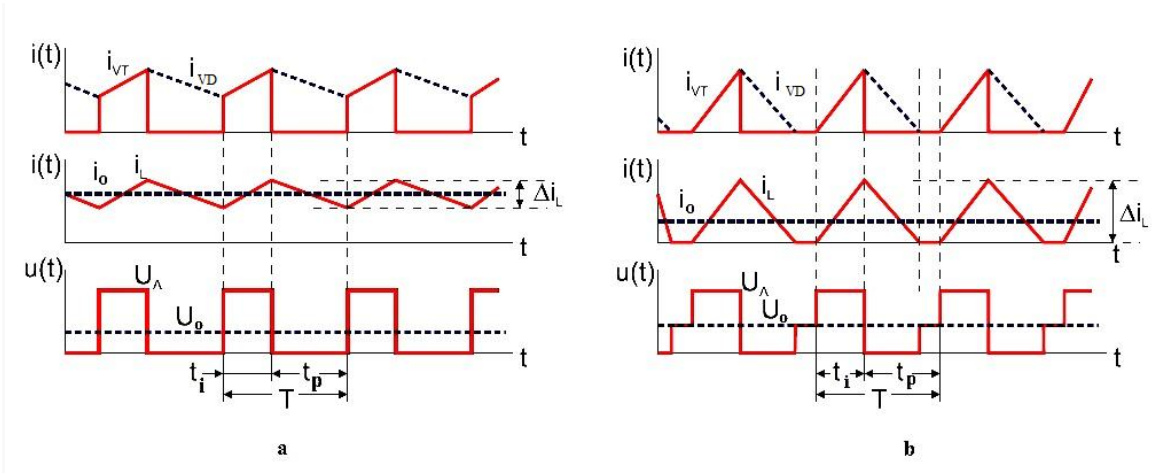

Figure 1.4. Step-down timing diagrams a) continuous-conduction mode b) discontinuous-conduction mode.

Analysis of step-down converter in continuous-conduction mode.

There are assumptions that should be taken into account:

- Input voltage source has zero impedance
- Switching time is negligible compared to the time of their switched on/off state.
- Filter capacitor has zero internal impedance
- Inductor and capacitor are constant for load conditions
- Switches that are used in the converter are ideal
- The output voltage ripple of the converter is negligible in comparison with the average value of the output voltage .
- The resistance of the key elements for the constant current are identical and can be combined with an active resistance of inductor, forming a common resistance r.
- If the following inequality is valid: L / r >> T, where T - switching period

The last assumption allows us to consider as a first approximation that inductor's current alterations are linear in Eq. 1.4. Then currents through the coils of inductor and switches, at time intervals of closed and opened states of regulation key, may vary according to the expressions :

$$I_1(t) = I_{min} + (E - U_o) \times t / L \, , \; 0 < t < t_i = DT \qquad (1.4)$$

$$I_2(t) = I_{max} - (U_o \times t) / L \, , \; 0 < t < t_p = (1- D) / T \qquad (1.5)$$

Considering that $I_1(t_i) = I_{max}$, $I_2(t_p) = I_{min}$, and equations: $t_i + t_p = T = l / f$, $D = t_i \times f$,

where T - period and f - frequency , in formulas (1.4) (1.5) , it is obvious that the converter's characteristic of the inductor is in a continuous-conduction mode.

It could also have the appearance:

$$U_o / E = D \qquad (1.6)$$

Fig. 1.5 shows the graphical view of the adjusting characteristic in relative units.

Using the energy balance equation we can find the minimum and the maximum currents through the keys.

$$I_{min} = I_o - D \times (E - U_o) / (2 \times L \times f) \quad (1.7)$$

$$I_{max} = I_o + D \times (E - U_o) / (2 \times L \times f) \quad (1.8)$$

Now it is possible to find the average current of the inductor for the period of switched on key's state:

$$I_L = (I_{min} + I_{max}) / 2 = I_o \quad (1.9)$$

Average values of the currents through the control key and the bypassing diode:

$$I_{A,av} = I_o \times D \quad (1.10)$$

$$I_{D,av} = I_o \times (1 - D) \quad (1.11)$$

Voltage on the control key and the bypassing diode in the switched off state:

$$U_A = U_{VD} = E \quad (1.12)$$

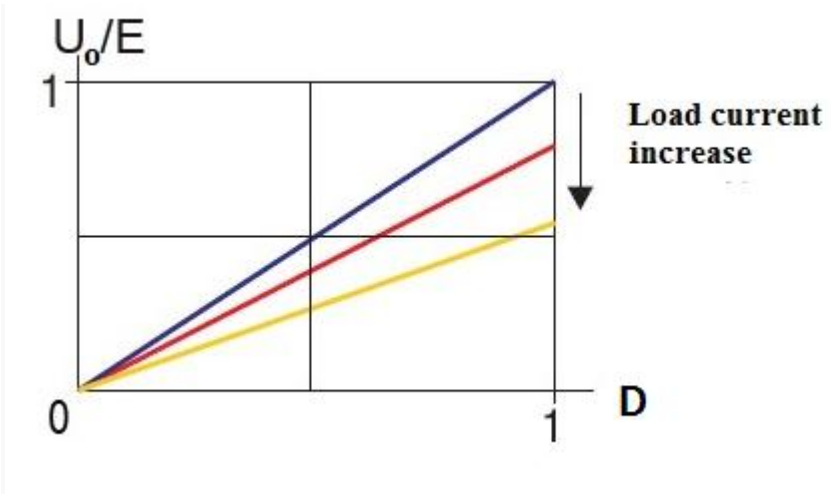

Figure 1.5 Regulation characteristics of DCC1.

Critical current mode of inductor.

The critical value of the load current for a given value of the inductance is determined by (1.7) (1.8) and provided $I_{min} = 0$.

$$I_{o,cr} = ED \times (1 - D) / (2 \times L \times f) \qquad (1.13)$$

Similarly, there is a critical inductance:

$$L_{cr} = ED \times (1 - D) / (2 \times I_o \times f) \qquad (1.14)$$

Discontinuous current conduction mode occurs in the inductor, if $I_o < I_{o,cr}$ for a given inductivity or $L < L_{cr}$ for a given load current .

Regulation characteristic can be obtained from (1.4) (1.5) , assuming that $I_{Lmin} = 0$.

Denoting t'_p duration of opened state for diode D and using in (1.5) that $i_2(t'_p) = 0$, we will find $t'_p = t_i \times (E - U_o) / U_o$. Thus, we can find regulation characteristics in discontinuous-current mode :

$$U_o / E = D^2 \times (\sqrt{1 + 8\tau Lof/D} - 1) / 4\tau L_o f \qquad (1.15)$$

The joint solution (1.6) (1.15) allows to determine D_{cr} for a critical mode.

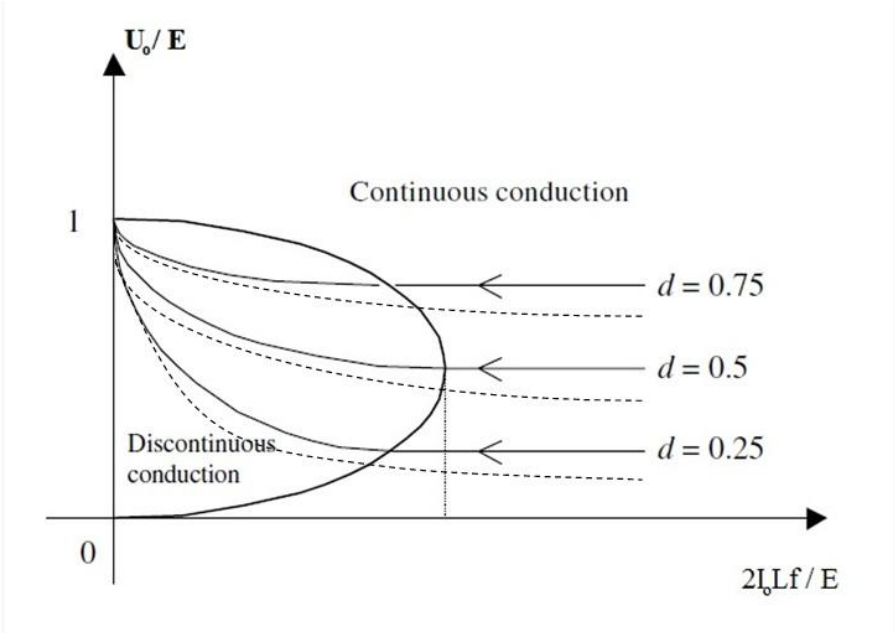

Figure 1.6 External characteristics of DCC1.

$$D_{cr} = 1 - 2 \times \tau L_o \times f \qquad (1.16)$$

Expanding τL_o and replacing $R_o = U_o / I_o$, the expression (1.15) can be transformed to:

$$U_o / E = D^2 / [D^2 – (2 \times L \times I_o \times f) / E] \qquad (1.17)$$

It defines the external characteristic of the ideal DCC1 in discontinuous-conduction mode shown in Fig. 1.6. When $I_o > I_{o,cr}$ external characteristic of the ideal converter doesn't depend on the load current.

However, external characteristics of a real controller depend on the load current due to the nonideality of components and parasitic resistance of inductor. In Fig. 1.6 nonideality is shown with dashed lines.

External characteristic DCC1 has the form:

$$U_o / E = D – (I_o \times r) / E \qquad (1.18)$$

Using (1.18) the output resistance of DCC1 could be found:

$$R_{out} = - (\partial U_o) / (\partial I_o) = r \qquad (1.19)$$

1.3.2 Step-up (boost) converter, DCC2 type.

Basic circuit of step-up converter is shown in Fig . 1.7 , and the timing charts explain its operation in the continuous- and discontinuous-conduction modes of inductor Fig. 1.8 [4]

Principle of operation of the circuit: When the regulating A-key is switched on, diode D that was previously in a conducting state , gets closed and inductor current is switched to the control key. During the time interval DT the bypassed diode is reversed biased (isolating the output stage) and the energy consumed by the input voltage source is

getting stored in the inductor (input current increases) . Load energy is provided by filter capacitor C, which will be subsequently discharged by a load current.

When the regulating key is opened, inductor current is switched to the bypassing diode , and voltage U_o operates on the key. Energy consumed by the input voltage source in this interval of time , recoups for the energy losses in the capacitor C, obtained at the previous stage and supports the load current. The filter capacitor current is equal to the difference of inductor current and load current. In contrast to DCC1, in DCC2 smoothing of output voltage ripple is performed only by filter capacitor.

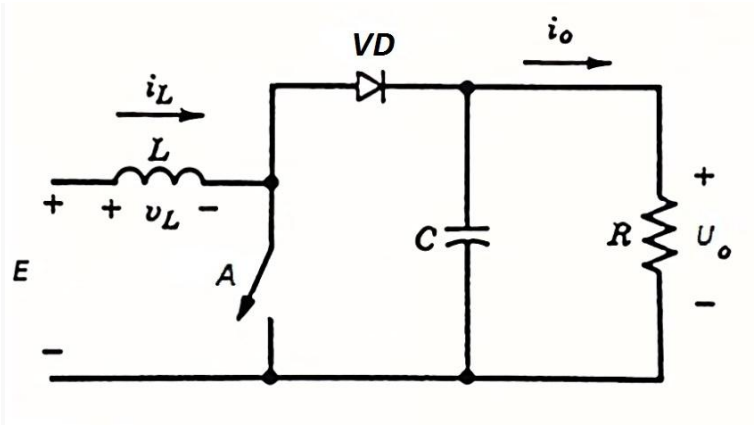

Figure 1.7 Step-up (boost) converter, DCC2 type.

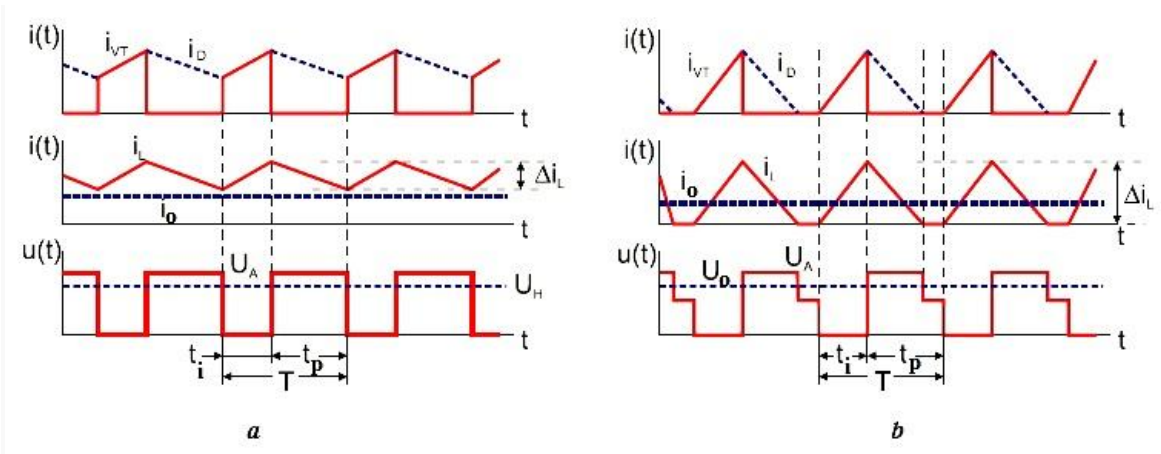

Figure 1.8 Step-up converter timing diagrams a) continuous current b) discontinuous current.

Analysis of the step-up converter in the continuous-conduction mode:

First of all we should remember to use adopted assumptions [1÷3]. Then we could consider that at the intervals of the closed and opened states of the A-key, the current through the inductor, and consequently through the appropriate keys is changed in accordance with the equations:

$$I_1(t) = I_{min} + E \times t / L;\ 0 < t < t_i = DT \qquad (1.20)$$

$$I_2(t) = I_{max} - (U_o - E)\, t / L,\ 0 < t < t_p = (1 - D)\, T \qquad (1.21)$$

Since $I_1(t_i) = I_{max}$, a $I_2(t_p) = I_{min}$, then a joint decision (1.20), (1.21) allows to get regulation characteristics DCC2 in relative units :

$$U_o / E = l / (l - D) \qquad (1.22)$$

Graphic diagrams are shown in Fig. 1.9.

Defining the minimum and maximum currents through the keys could be found using the energy balance equations:

$$I_{max} = I_o / (1 - D) + E \times D / 2 \times L \times f \qquad (1.23)$$

$$I_{min} = I_o / (1 - D) - E \times D / 2 \times L \times f \qquad (1.24)$$

The average inductor current:

$$I_{L,avr} = (I_{max} + I_{min}) / 2 = I_o (1 - D) \qquad (1.25)$$

Average currents of regulation key and bypassed diode are determined by the expressions:

$$I_{A,avr} = I_o \times D / (1 - D) \qquad (1.26)$$

$$I_{D,avr} = I_o \qquad (1.27)$$

Obviously that: $I_{D,avr} + I_{A,avr} = I_{avr}$

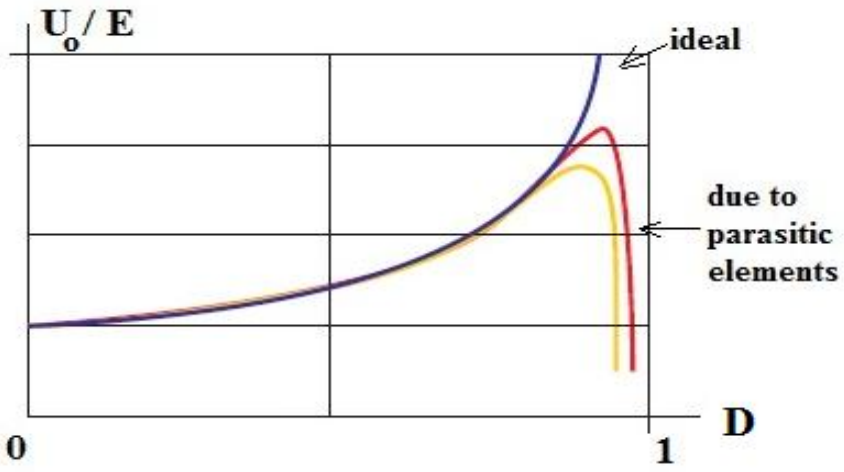

Figure 1.9. Regulation characteristics of DCC2.

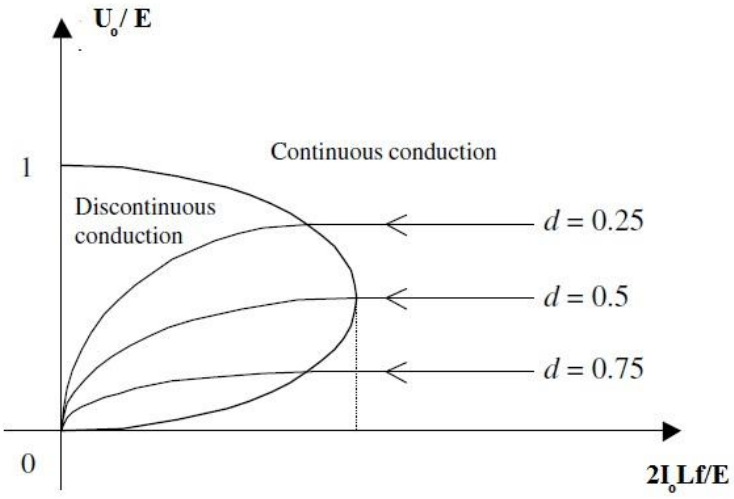

Figure 1.10 External characteristics of DCC2.

Voltage at the opened key and closed bypassing diode is equal.

$$U_A = U_{VD} = E / (1 - D) \qquad (1.28)$$

Critical current mode for the inductor is determined from (1.24) at $I_{min} = 0$. Values of critical load current (at L = const) or critical inductivity (with I_o = const), corresponding to the boundary between continuous mode and discontinuous currents of inductor, are given by equation:

$$I_{o,cr} = E \times D \times (1 - D) / (2 \times L \times f) \quad (1.29)$$

$$L_{cr} = E \times D \times (1 - D) / (2 \times I_o \times f) \quad (1.30)$$

Discontinuous-conduction mode for inductor:

In case if $I_o < I_{o,cr}$ or $L < L_{cr}$, DCC2 turns to a discontinuous current mode in the inductor . Regulation characteristic has the form:

$$U_o / E = 1/2 + \sqrt{\frac{1}{4} + D^2/(2\tau Lof)} \quad , \quad (1.31)$$

where $\tau L_o = L / R_o$

This characteristic is shown in Fig . 1.9 with dashed line. Replacing of $R_o = U_o / I_o$ from (1.31) could be found external characteristic of the ideal DCC2 in discontinuous-conduction mode:

$$U_o /E = 1 + D^2E / (2 \times L \times I_o \times f) \quad (1.32)$$

Ideal DCC2 in continuous-conduction mode does not depend on the load current.

External characteristic of the converter.

External characteristic of the real DCC2 in continuous–conduction mode in relative units:

$$U_o /E = [1/(1 - D)] - (I_o \times r)/ (1 - D)2 \quad (1.33)$$

Graphical representation of the external characteristics of a real DCC2 shown in Fig. 1.10

Output resistance of the converter DCC2 could be found with (1.33)

$$R_{out} = r/(1 - D)^2 \quad (1.34)$$

Replacing $I_o = U_o /R_o$, allows get regulation characteristics of a real DCC2

$$U_o/E = (1 - D) / [(1 - D)^2 + r/R_o] \quad (1.35)$$

Dependence of the output resistance of DCC2 from D determines the appearance of the characteristic's peak at (U_o /E)* and further decrease of U_o down to zero as D $\longrightarrow$ 1.

Differentiation of (1.35) relative to D and equating the derivative to zero determines the coordinates of the maximum:

$$D^* = 1 - \sqrt{\frac{r}{Ro}} \qquad (1.36)$$

$$U_o / E^* = \sqrt{\frac{Ro}{r}} \times 0{,}5 \qquad (1.37)$$

Found values should be considered in designing stabilized DCC2 , because for D > D * feedback is variable , that provides stabilization U_o in a regular mode.

1.4 Assignment clarification.

Besides two main circuits of pulse DC converters there is also third type DCC3 , buck-boost. Common circuit of buck-boost is drawn in Fig.1.11

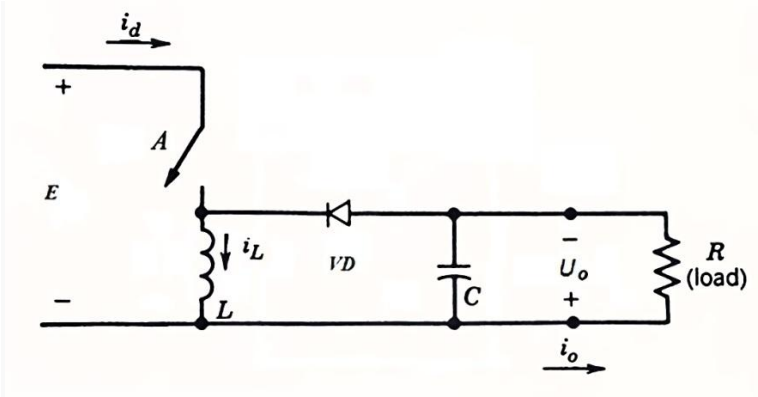

Figure 1.11 Buck-boost converter, DCC3 type.

The feature of this converter is its ability to invert the sign of the output voltage in relation to the input. However, this property of DCC3 is not determinative: it is easy to implement DCC3 also without inverting the sign of the output voltage. As it is shown in [9], all characteristics that are inherent to the DCC3, could be easily implemented using the first two converters . Thereby, DCC1 and DCC2 could be considered the basic circuits of converters. If we assume that elements and input voltage source are ideal , then from the entire set of pulse DC converters could be marked out two types of converters characterized by different features of energy accumulating in the reactive elements :

• Pulse converters with limited ability of energy accumulation in reactive elements (DCC1)

•Pulse converters with unlimited ability of energy accumulation in reactive elements (DCC2)

There is a possibility to implement DCC3 characteristics with basic converters. As follows from [8-10] , regulation characteristic of DCC3 is a composition of regulation characteristics for DCC1 and DCC2. Consequently DCC3 may be implemented by connecting two basic converters. This connection exists if some transformations are done associated with the exception of the intermediate capacitor, due to the average voltage. Combining the two in series connected inductors in one the average currents are the same, shown in Fig. 1.12. As a result, universal converter provides any law of regulation characteristic for DCC1, DCC2 or DCC3 .

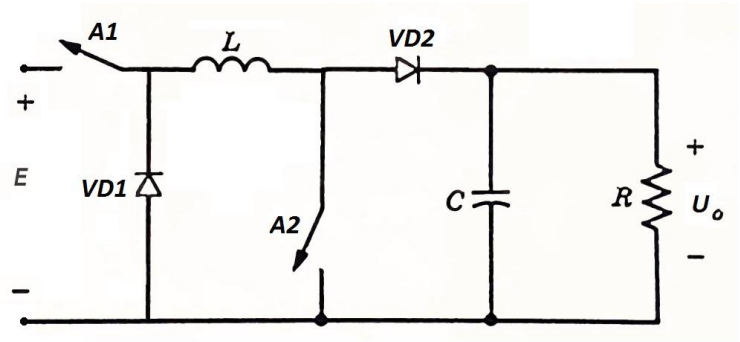

Figure 1.12 Universal circuit of DCC , derived from the combination of basic converter circuits.

As a matter of fact, if the regulation is applied with switch A1, and the switch A2 is opened, then DCC1 is on ; if the switch A1 is closed and regulation is applied with key A2, then we DCC2 is on ; if the regulation is applied with both A1 and A2 , (opening and closing), the DCC3 is on.

In reality to get the general DCC3 circuit Fig. 1.11 some functionally redundant components should be excluded from the circuit of converter depicted in Fig. 1.12, because there is no need to have two regulation keys and two diodes, that are connected in series and working synchronously.

The unofficial statistics shows that the largest part of all DC converters is based on DCC1 type. These are pulse voltage stabilizers in power supply devices, regulators of rotation frequency in DC motors, etc. Considerably smaller part of converters are based on DCC2 type . DCC2 circuit is applied to create pulsed DC voltage stabilizers based on a single-cycle converters with "reversed" switching diodes. DCC2 circuit is indispensable for creating deep regenerative braking DC engines on the base of irreversible restorable converter [6-8]. The same circuit is used in modern LED lamps. It is possible to implement converter in tasks like charging batteries from a generator or solar panels. Application area for DCC3 is very limited. DCC3 is rarely used in devices like power supply, when it is needed to get voltage with opposite polarity sign in the presence of one (usually autonomous) power supply and in situations if there is no possibility to use transformer circuits .

Based on these considerations, it seems reasonable in the developed prototype of the laboratory work, to focus study only on DCC1 and DCC2 circuits. DCC3 circuit and its characteristics is a combination of first two converters' configurations and, hence, from a methodological point of view is not so important.

Developed layout model must meet the following basic requirements:

- The work of the model is limited by possibility to operate in buck or boost mode.
- Power Unit of the model must be implemented on the base of universal converter (Fig.1.12)
- Control system must fulfill conditions of PWM regulation implementation.
- Available in stock component base have to be used for the model design.

2. Block diagram development of DC converter for the laboratory layout model.

Block diagram of layout model is given in Fig. 2.1

The circuit consists of the following basic parts: Power Supply (PS), Control System (CS), Power Unit (PU), Load (L).

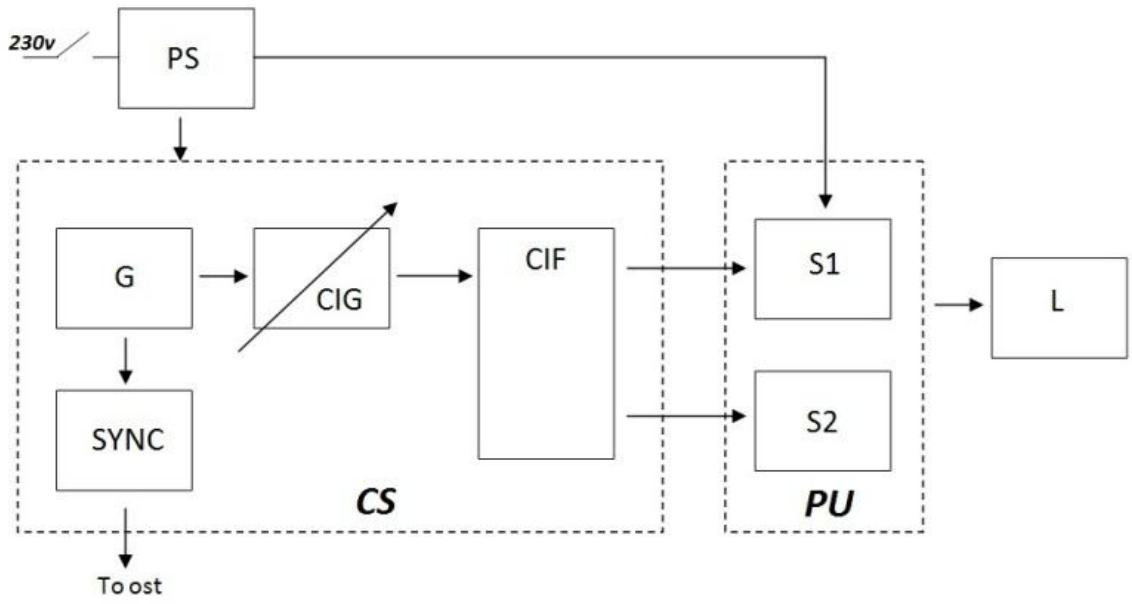

Figure 2.1. Block diagram of layout model.

The objective of CS is to generate pulses with intended frequency and length to regulate switch circuits of PU.

CS consists of :

- Self-contained Generator (G) producing sequence of pulses with stable frequency to activate control impulse generator (CIG) and synchronization impulse generator (SYNC) for oscilloscope.
- Control impulse generator (CIG) providing with intended length pulses and strictly defined repetition frequency, defined by G. These impulses are transfered to the input of Control Impulse Former (CIF). Thereby Duty cycle could be changed.

- Control Impulse Former (CIF) generates impulses with required power to regulate switch circuits S_1,S_2 of PU in the layout model. At the same time required level shift occurs (for the switch circuit S_1).
- Synchronization impulse generator (Sync) produces impulses for oscilloscope activation in external triggering mode.

  In the principle of designing PU switch circuits S_1 and S_2 for current commutation are used. The main task of PU is to implement processes of DC voltage conversion in buck or boost mode. Switching between two modes is implemented by additional commutation elements.

Load (L) allows to implement regulation of consumed current in both conversion modes. The task of PS is to supply CS and PU with rectified, filtered and stabilized required voltages.

3. Development of electrical schematic for the laboratory layout model .

Schematic design of CS is shown in Fig. 3.1 , and diagrams, illustrating the work of CS in Fig.3.2

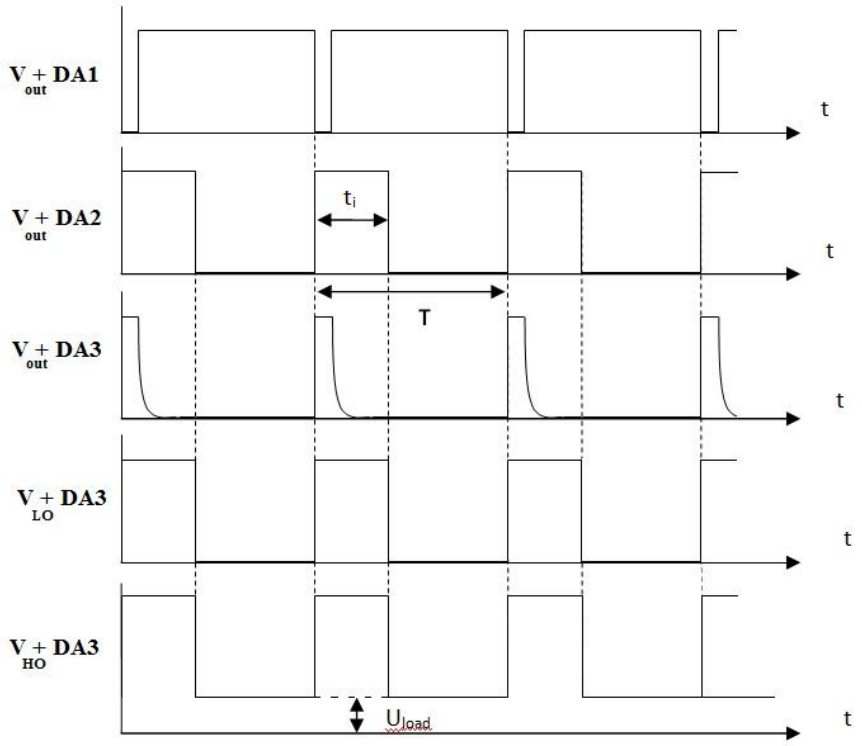

Figure 3.2 Voltage Diagrams of CS.

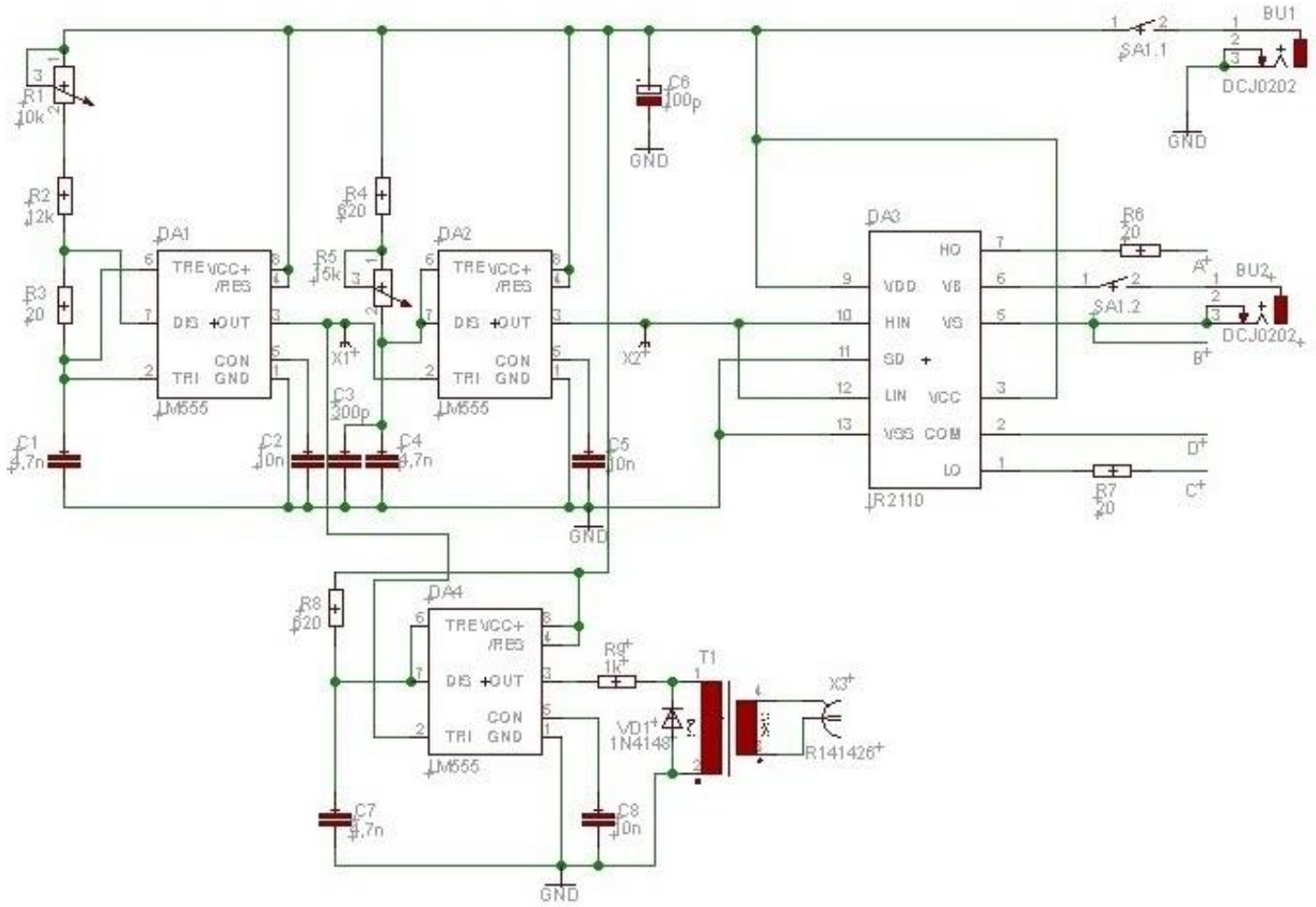

Figure 3.1 Electrical schematic of CS.

3.1 Master Generator.

Master generator is designed on the base of chip DA1. The role of chip DA1 is executed by integral timer LM555. In this circuit timer is working as an astable multivibrator. [11,12]

First of all the frequency of the generator is chosen: 10 kHz. This frequency allows to veiw electromagnetic processes quite well on the screen of oscilloscope. Commutation processes in S switches are quite fast, so they could be neglected. Thereby chosen frequency with its value is approaching to the working frequencies of real DC converters. Moreover, using this frequency, the value of inductor L will have acceptable value.

The capacity value for a timing capacitor C_1 is chosen as 4700 pF. And resistor R3 = 20 Ohm , that is needed to discharge the capacitor, due to the suggested value.[3] Generator (G) produces pulses, that activate CIG and SYNC , therefore pulses have to be with minimum, but sustained generated length. Actually, this time is around 1 μs [12].

To obtain the desired frequency : the total value of the resistors R1,R2,R3 have to be found :[11]:

R_t = R1+R2+R3 = 20+12k+10k = 22,02 kOhm

To have a possibility to accurately adjust the frequency to desired 10kHz, part of the charging line for the capacitor C_1 consists of fixed resistor R2 = 12 kOhm and potentiometer R1 = 10 kOhm. By the adjusting of resistor R1, exact value of frequency is set: f = 10 kHz.

3.2 Control impulse generator.

To implement a chosen law of work in observed converters (PWM) in a range of frequency period G (100 us) it is needed to change width of working impulse : 5 ÷ 95 μs [3,7-10]. It corresponds with the changes of Duty cycle , D = 5÷95%. The easiest way to produce adjustable pulses in such ranges, is to use a deeply regulated monostable multivibrator with activation from G. This kind of multivibrator is designed on the base of integral timer LM555.

Let's choose the capacity of the main timing capacitor C4 = 4700 pF.

During the initial resistance of potentiometer R5 = 0 Ohm , an option for resistor R4 = 620 Ohm gives the value of $t_{i,min}$ [12]:

$$t_{i,min} = 1{,}1 \times R_4 \times C_4 = 1{,}1 \times 620 \times 4{,}7 \times 10^{-9} = 3{,}2\ \mu s$$

If R5 = 17 kOhm, we get maximum value for impulse $t_{i,max}$:

$$t_{i,max} = 1{,}1 \times 17{,}62 \times 10^{3} \times 4{,}7 \times 10^{-9} = 91{,}1\ \mu s$$

In addition to main capacitor, extra capacitor C3 = 300 pF, leads to enhancement of minimum and maximum lengths of pulses:

$$t_{i,min} = 1{,}1 \times R_4 \times (C_3 + C_4) = 3{,}4\ \mu s$$

$$t_{i,max} = 1{,}1 \times R_4 \times (C_3 + C_4) = 96{,}9\ \mu s$$

It corresponds to the changes of D in ranges of 5÷95 % ±2.

3.3 Control impulse former.

As it will be shown below, switch circuits S of the power part PU are designed on the base of field-effect transistor (MOSFET), and configuration of buck circuit has a classical view. The last circumstance requires additional shift for control pulses of S1. Implementation of CIF on the base of discrete elements brings it to the unreasonable complexity of circuit design solution. To avoid this situation, CIF is designed on the base of universal driver microcircuit for MOSFET transistors: IR2110 (DA3).

Originality of using driver IR2110 consists in the controlling of field transistors with a half-bridge inverter. The idea of actual application of circuit IR2110 is in using a transistor's control channel with Low-level for regulating switch circuit S2 in boost-converter and control channel with High-level for regulating switch circuit S1 in buck-converter.At the same time pulses of activation coming from DA2 are transferred to the inputs of both channels HIN and LIN.

During operation of IR2110 in the half-bridge inverter, when transistors in half-bridge work alternately, power supply of control signal generation cascades HO, as a rule, applied by boost mode [check appendix] . In our case boost capacitor charge through the variable wide range load will be difficult. Hence there is implemented an isolated power supply for channel HO from stabilized DC voltage 9V, supplied from PS through the connector Bu2.

Power supply of channel HO proceeds simultaneously with the main power supply (separate dc power supply +9V) of DA1÷DA4 with tumbler SA1. Logical part of driver (Vcc) is supplied by power supply chain of circuits DA1÷DA4. Outputs of channels HO and LO are connected with gates of transistors in switch circuits S1, S2 through resistors R6 = R7 = 20 Ohm, as it is recommended by manufacturer of transistors.

3.4 Synchronization impulse generator

Synchronization impulse generator (SYNC) DA4 is also designed on the base of integral timer(LM555). Timer DA4 works in the mode of monostable multivibrator and activated by generator G (DA1). Implementation of Synchronization impulse source on the base of separate generation circuit , enables if necessary to change synchronization pulse duration without affecting the generator G. By analogy with CIG, timing circuit is applied: R8= 620 Ohm, C7 = 4700 pF. In the first approximation , it provides impulse time:

$t = 1.1 \times R \times C = 3{,}2\ \mu s$

In accordance with the manufacturer's recommendations of 555 circuit, pin #5 (“control”) in DA4 should be blocked by capacitor C8 = 10nF. Similarly should be done in DA1 and DA2.

To implement the possibility of withdrawing the oscillograms of all elements of the PU , galvanic isolation is required for oscilloscope from CP and DA4. This is implemented using a transformer T1. Its role executed by a two-winding input choke of supply-line filter (transformation ratio = 1). To avoid overloading DA4 transformer has a resistor protection: R9 = 1 kOhm. To protect output cascade DA4 primary winding of transformer T1 is shunted with a reverse-biased diode VD1, type 1N4148. A signal from DA4 to the oscilloscope proceeds through the socket X3.

3.5 Power unit .

Power Unit (PU) electrical schematic of the laboratory layout model is brought in Fig. 3.3 It is implemented on the base of scheme in Fig. 1.12

Basis of the circuit are switch circuits S1 and S2 , that are designed on the MOSFET transistors VT1 and VT2. The type of transistors is IRFZ44N. Gate-source chains of transistors (A-B and C-D) are connected to appropriate output pins of DA3.

In the circuit there are used: common inductor L1 , filter capacitor C9, Load R17,R18. Flyback diodes VD2 and VD3(the same as transistors) operate depending on the selected working mode of PU. Output voltage of the load is measured with a built-in pointer-type indicator PA1, type M4200 with scale 0-20V or with digital instruments, located on the laboratory: DMM155 or Protek 506.

Information about currents of switch circuits, flyback diodes and inductor is taken from the measuring resistive shunts R10-R14. The resistance of shunts are 0,1 Ohm. Construction and design is borrowed from [15].

Load (L) consisting of fixed resistor R17 and variable resistor R18 is permanently connected. Power voltage source for PU is given by two DC stabilized voltage sources 2 x 9V, connected to jacks Bu3 and Bu4. The selection of supply voltage depending on the working mode , +9V or +18V is applied by the switch SA2. Turning on of the PU is proceeded by using switch SA3.

The selection of layout model working mode besides switch SA2 is implemented with switches SA4 and SA5, type MT2. On the schematic Fig 3.3 switches SA2 , SA4, SA5 are shown in the corresponding buck mode.

Following conditions should be satisfied for the Buck mode:

- Supply voltage is +18V
- Circuit S1 is switched on with transistor VT1 and flyback diode VD2
- Circuit S2 is switched off with transistor VT2. To reduce losses in the circuit, flyback diode VD3 is shorted.

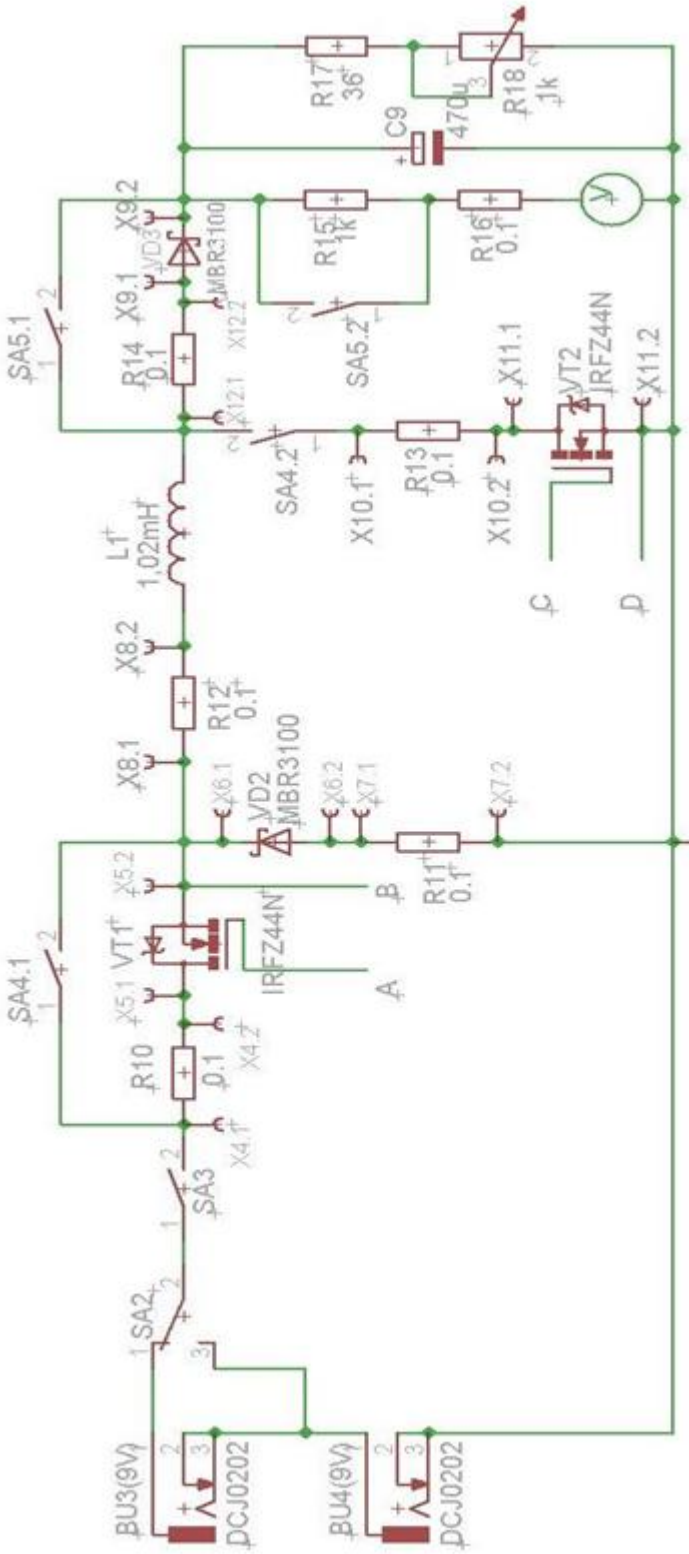

Figure 3.3 PU electrical schematic of the laboratory layout model.

After the the key SA3 is switched on and Buck mode is enabled, the circuit of PU takes form , illustrated on Fig. 3.4.

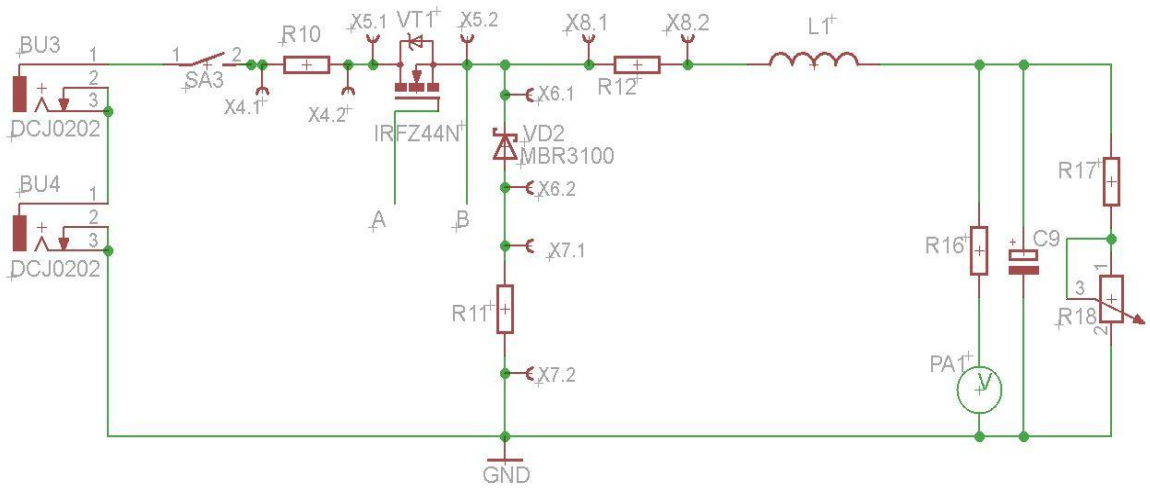

Figure 3.4 Equivalent circuit of PU for Buck mode.

To organize Boost-mode, the switch SA2 has to be flipped to locked position in Fig. 3.3. Now when the SA4 switch is locked and SA5 switch unlocked, the circuit is working in Boost-mode.

Following conditions should be satisfied for the Boost mode:

- Supply voltage is +9V
- Circuit S2 is switched on with transistor VT2 and flyback diode VD3
- Circuit S1 is switched off with transistor VT1.
- Sensitivity of the measuring device PA1 is reduced by connection of an additional resistor R15 (Voltmeter measurement limit is increased to 0-80V)
- Load resistance could be increased by regulation of variable resistor R18.

After the the key SA3 is switched on and Boost mode is enabled, the circuit of PU takes form , illustrated on Fig. 3.5

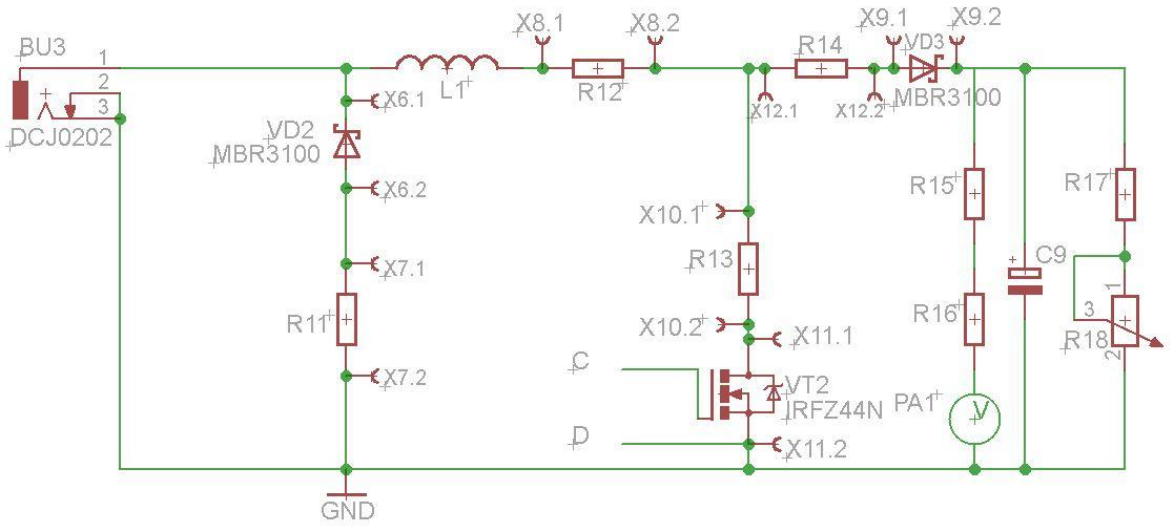

Figure 3.5 Equivalent circuit of PU for Boost mode.

Let's define the most important parameters of the PU circuit for Buck-mode :

$E= 18V$, $I_{load,nom}=0,5A$

Due to the condition of maintaining the continuity of the inductor L_1 current, its minimum inductance L_{min} is [1-3,8-10]:

$$L_{min} \geq E \times D \times (1-D) / 2 \times I_{load} \times f$$

where $E = 2 \times 9 = 18V$ – supply voltage

$f = 10 \times 10^3$ Hz = 10 kHz – switch circuit commutation frequency

Let's find Lmin for D = Dmin = 0,5; that corresponds to:

$$I_{load} = I_{load,nom} \times D_{min} = 0,5 \times 0,5 = 0,25 \text{ A}$$

$$L_{min} = 18 \times 0,5 \times 0,5 / 2 \times 0,25 \times 10 \times 10^3 = 0,9 \times 10^{-3} \text{ H}$$

As an inductor is used a serial connection of 2 multiwinding filter chokes from switching power supplies PC , type PA-4022 204W , Taiwan Liteon Electronic Co., Ltd. All of the windings of each inductor are connected in series and accordantly. Each inductor has the same parameters: L= 0,51mH , R = 0,09 Ohm. Thus, inductance of choke is:

L1 = 0,51×2 =1,02 mH , that satisfies the conditions.

Setting the output load voltage ripple $\Delta U_{load} = 50mV$, filter capacitor C9 could be defined [8-10]:

$$C9 \geq E/32 \times f^2 \times \Delta U_{load} \times L1 = 18 / (32 \times 10^8 \times 50 \times 10^{-3} \times 1{,}02 \times 10^{-3}) = 11{,}03 \times 10^{-5} \text{ F}$$

Mounting C9 = 200 μF x 100V , from Jamicon company.

Operating voltage 100V is selected taking into account the operation of the capacitor C9 [9,10]:

$$I_{c,max} = U_{load} \times (1\text{-}D_{min}) / 2 \times L1 \times f = 3{,}6 \times 0{,}8 / (2 \times 1{,}02 \times 10^{-3} \times 1 \times 10^4) = 0{,}14 \text{ A}$$

Determining the average and maximum values of currents , flowing through the inductor L1:

$$I_{L,av} = I_{load,nom} = 0{,}5 \text{ A}$$

$$I_{L1\ min} = I_{load,nom} - I_{c,max} = 0{,}5 - 0{,}14 = 0{,}36 \text{ A}$$

$$I_{L1\ max} = I_{load,nom} + I_{c,max} = 0{,}5 + 0{,}14 = 0{,}64 \text{ A}$$

Assuming that current value of switch circuit S1 equals:

$$I_{s1} = I_{VT,max} = (1{,}2 \div 2) \times I_{load} = 2 \times 0{,}5 = 1 \text{ A},$$

selecting the transistor VT1 by current and voltage:

$$I_D > I_{L1,max}, \ U_{DS} > E$$

Transistor MOSFET IRFZ44N satisfies the condition. (V_{DS} = 55V, I_D = 49A, P_{tot}= 110W, $R_{DS,on}$= 22 mOhm) [13].

To reduce losses in circuit we choose diode VD2 , type Schottky Barrier Rectifier MBR3100 (I_F =3A, U_R=100V , $U_{F/3A}$ = 0,79V) [14]

Power losses on transistor VT1 and diode VD2 are determined mainly by static losses. Due to the good frequency properties of selected types of transistor VT1 and diode VD2 and also relatively low switching frequency, dynamic (switching) losses could be neglected. Static power losses on the transistor VT1 (D =1,0):

$$P_{stat} = (I_{load,nom})^2 \times R_{DS,on} = 0{,}5^2 \times 22 \times 10^{-3} = 5{,}5 \times 10^{-3} \text{ W}$$

Power losses on diode VD2:

$$P_{VD2} = I_{Load,nom} \times U_{F/0,5} \times (1-D_{min}) = 0,5 \times 0,3 \times (1-0,2) = 0,12 \text{ W}$$

Where $U_{F/0,5}$ = 0,3V – direct fall on the diode MBR3100 with direct current I_F = 0,5A. Thereby power losses in the switch S1(VT1) and reverse diode VD2 are negligible and even a small cooler as a radiator for these elements is not needed.

Next step is determining parameters of PU circuit for boost-mode:
Setting Load current value, corresponding to maximum output voltage, approximately

$$U_{load,\ max} = 50\text{V } [8,9] \text{ and } I_{load,\ max} = 50 \times 10^{-3} \text{ A}$$

Minimum choke inductance , needed to provide current continuous-mode [1-3,8-10] :

$$L_{min2} \geq E2 \times D_{max} \times (1-D_{max}) / 2 \times I_{load,nom2} \times f = 9 \times 0,9 \times 0,1 / 2 \times 50 \times 10^{-3} \times 10^{4} = 8,1 \times 10^{-4} \text{ H}$$

$$L_{min2} \geq 0,81 \text{ mH},$$

Where E_2 = 9V – voltage supply in boost-mode.

D_{max} = 0,9 – the highest value of Duty cycle.

Obviously, that inductor L1= 1,02 mH is suitable for this solution. Let's find an average, min and max currents for inductor L1 for this mode [8,9]:

$$I_{L1,av} = I_{Load,nom2} / (1-D_{max}) = 50 \times 10^{-3} / (1-0,9) = 0,5\text{A}$$

$$I_{L1,min} = I_{L1,av} - (E_2 \times D_{max} / (2 \times L1 \times f)) = 0,5 - (9 \times 0,9 / (2 \times 1,02 \times 10^{-3} \times 10^{4})) = 0,1 \text{ A}$$

$$I_{L1,max} = 2 \times I_{L1,av} - I_{L1,min} = 1,0 - 0,1 = 0,9 \text{ A}$$

Transistor VT2 is selected due to the conditions: [8]

$$I_D > (1,5 \div 2)\, I_{L1,av};\ U_{DS} > U_{load,\ max}$$

These conditions also satisfies MOSFET transistor IRFZ44N. Flyback diode VD3 is selected due to the conditions:

$I_F > I_{L1,max}$; $U_R > U_{Load,max}$ Diode type MBR3100 also satisfies the conditions.

Power losses on the transistor VT2:

$$P_{stat2} = (I_{L1,av})^2 \times R_{DS}, \text{ on} \times D_{max} \times 0{,}5^2 \times 22 \times 10^{-3} \times 0{,}9 = 4{,}95 \times 10^{-3} W$$

Power losses on diode VD3:

$$P_{VD3} = I_{L1,av} \times U_{F/0,5} \times (1-D_{min2}) = 0{,}5 \times 0{,}3(1-0{,}1) = 0{,}135 \text{ W},$$

where Duty cycle for that mode Is $D_{min2} = 0{,}1$

Conclusion: operating in this mode transistor and diode do not need radiators. Let's check level of ripple on the capacitor C9, in boost-mode:

$$\Delta U_{C9} = I_{load,\ nom2} \times D_{max}/(f \times C9) = 50 \times 10^{-3} \times 0{,}9 /(10^4 \times 200 \times 10^{-6}) = 22{,}5 \times 10^{-3} \text{ V}$$

This level of ripple is acceptable.

Load resistors and their values:

$$R17 = E/Iload,nom = 18 \times 0{,}5 = 36 \text{ Ohm}$$

Maximum power dissipation of the R17 resistor:

$$PR17,max = (E \times Dmax)^2 / R17 = (18 \times 0{,}9)^2 / 36 = 7{,}3 \text{ W}$$

In the laboratory layout model is installed R17 = 36 Ohm, type ПЭВ -15.

Total resistance: $R17 + R18 = U_{load,max} / I_{load,nom2} = 50/50 \times 10^{-3} = 1\text{kOhm}$

Maximum power dissipation of the R17, R18 :

$$PR17,R18,max = (Uload,\ max)^2 / (R17+R18) = 50^2 / 10^3 = 2{,}5 \text{ W}$$

In the laboratory layout model is mounted : R18 = 1kOhm, type ППБ-10

3.6. Power Supply.

Power supply must provide the laboratory circuit model with DC voltages 4 x 9V. Voltage of each channel , should be stabilized. Two of power supplies should be intended for currents not less than 0,5A.

The problem is solved using 4 same Switching Adapters models: DSA-01151A-09 A(U) , DVE(China) [look appendix 4], connected to a single-face electrical network 200÷240V. Maximum operating current is 1,5 A.

Connection to the network is carried out by switching all adapters into the power strip for 5 sockets and equipped with a power indicator switch that could display the enabled state. Thus, simultaneous on-off switching is provided for all adapters.

4. Designing and simulation.

When the theoretical part is over and electrical design is finished, it is time to check the design in the virtual space. For that goals there would be used a simulation program NI Multisim 13.0 - a circuit design program developed by National Instruments Electronics Workbench Group. Multisim is widely used in academia and industry for circuits education, electronic schematic design and SPICE simulation.

In spite of the ease of use of the program, it is necessary to remember , that simulation implementation occurs in ideal conditions with ideal components, that could differ from the real model. Moreover some complex simulation components could be not working. However, simulation is very important part of the design, that could reveal defects and help to avoid making a nonfunctioning circuit.

As it was previously mentioned, the circuit consists of the following basic parts:

Power Supply (PS), Control System (CS), Power Unit(PU) and Load (L). There is no need to simulate Power supply or Load. Thus, the main attention will be given to these two parts.

The heart of the CS are astable and monostable multivibrators that are implemented using integral timers 555. Fig.4.1

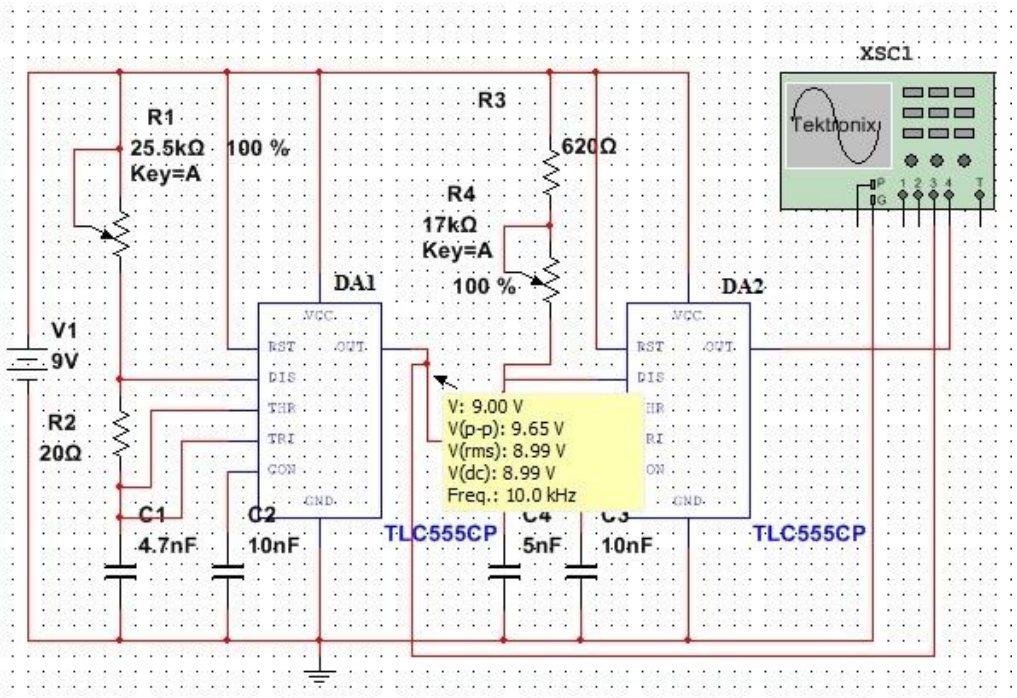

Figure 4.1 Astable Multivibrator DA1 and Monostable DA2.

By the adjusting of the resistor R1 = 25.5k, exact value of frequency is set: f = 10 kHz. Then the signal is transferred to the monostable vibrator, where the Duty cycle could be changed by adusting the resistor R4 = 17k.

We have to check the possibility to change signal in a range of frequency period G (100 us) and make sure that the width of working impulse could be varied : 5 ÷ 95 us [3,7-10], that corresponds with the changes of Duty cycle , D = 5÷95%.

Using the virtual oscilloscope following data has been taken:

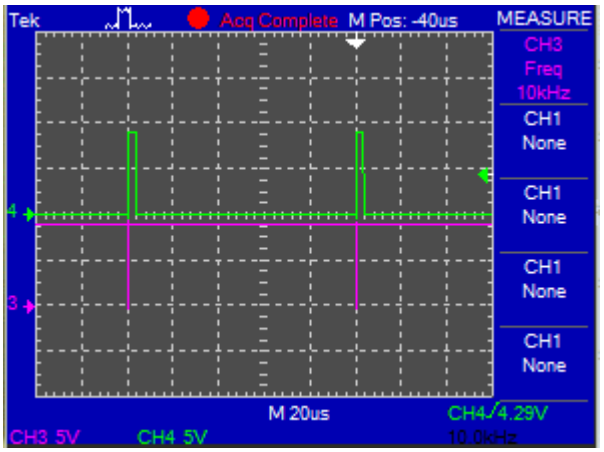

Figure 4.2 Multivibrators, $D_{min.}$

Output signals:

DA1 – astable multivibrator (purple),
DA2 – monostable multivibrator (green)
Duty Cycle – Dmin.(R3 =620 Ω, R4 =0)
T_i(DA1) = 200ns
T_i(DA2) = 4µs

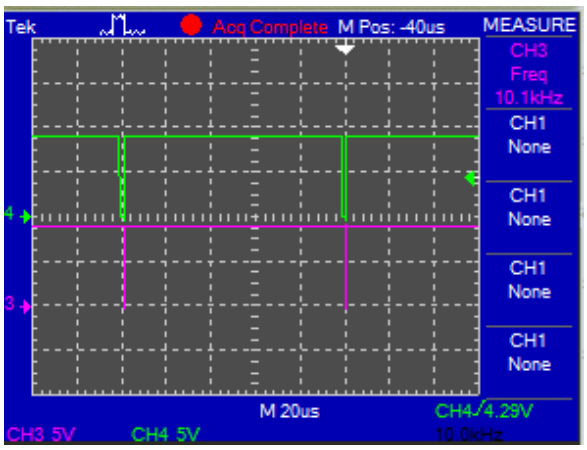

Figure 4.3 Multivibrators, $D_{max.}$

Output signals:

DA1 – astable multivibrator (purple),
DA2 – monostable multivibrator (green),
Duty Cycle – Dmax. (R3 =620 Ohm, R4 = 17K)
T_i(DA1) = 200ns
T_p(DA2) = 2µs

On these diagrams we can see, that Duty cycle regulation is working and adjustable. Considering that DA3 (SYNC) is used only for external triggering, to use oscilloscope, we could leave it without attention, because the circuit will function the same without this part. DA4(CIF) is working as an impulse former and generate pulses with required power, at the same time it makes a level shift for buck converter.

Let’s check the Buck and the Boost converters and get their regulating diagrams in the different conduction modes: continuous and discontinuous:

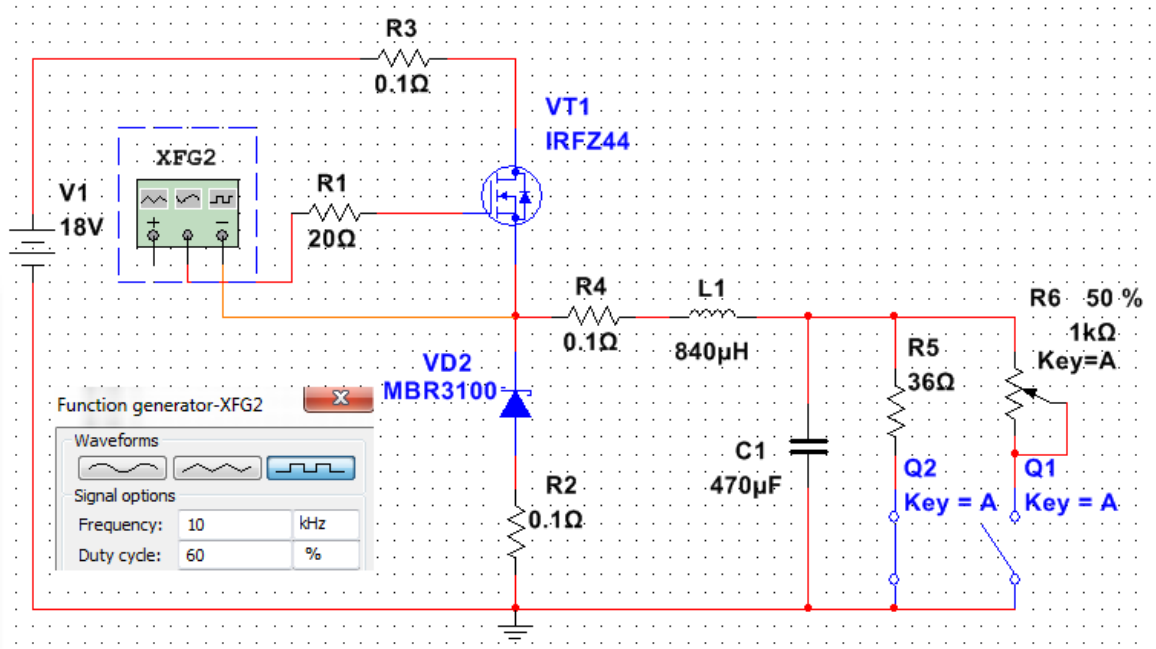

Figure 4.4 Buck-converter simulation.

DCC1 – DC converter 1 type - Buck (step-down) , Fig 4.5-4.11

Continuous-conduction mode, R_L = 36 Ohm.

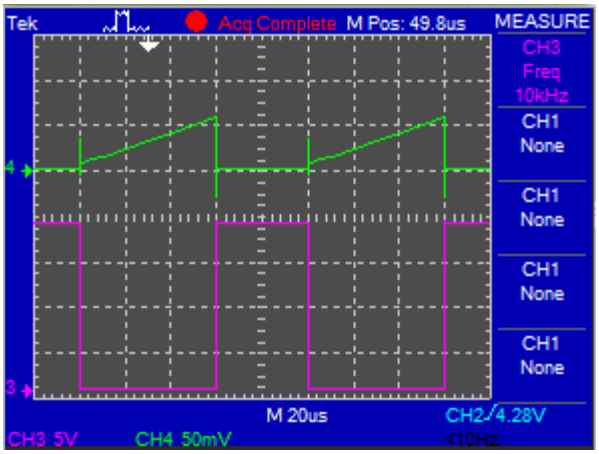

Figure.4.5

Transistor VT1:I_{VT1} (green)

Transistor VT1 U_{ds} (purple)

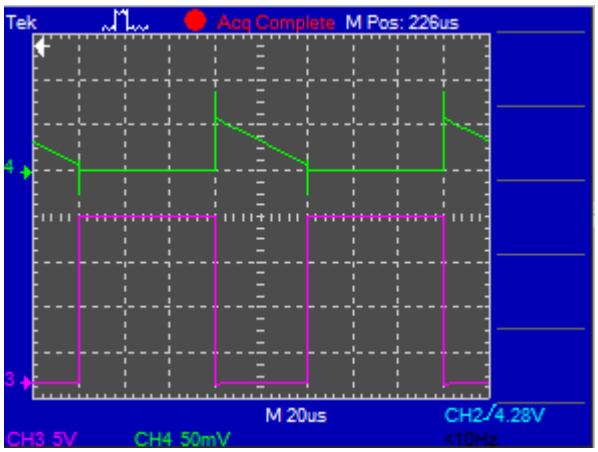

Figure 4.6

Diode I_{VD2} (green)

Diode U_{VD2} (purple),

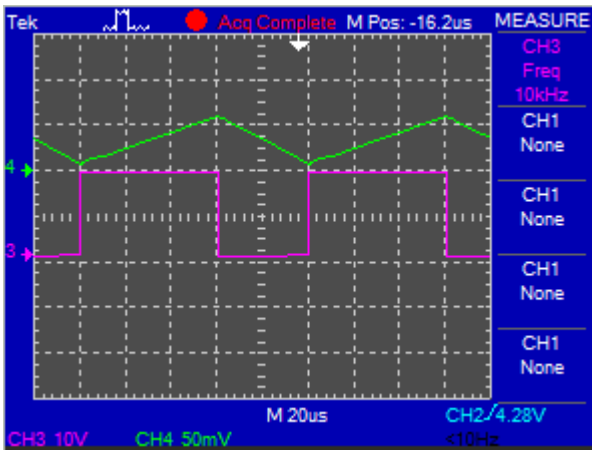

Figure 4.7

Inductor L1: I_L (green)

Diode VD2: U_{VD2} (purple)

DCC1 : Discontinuous-conduction mode, R_L = 470 Ohm. (To see the result 125 Ohm is already enough)

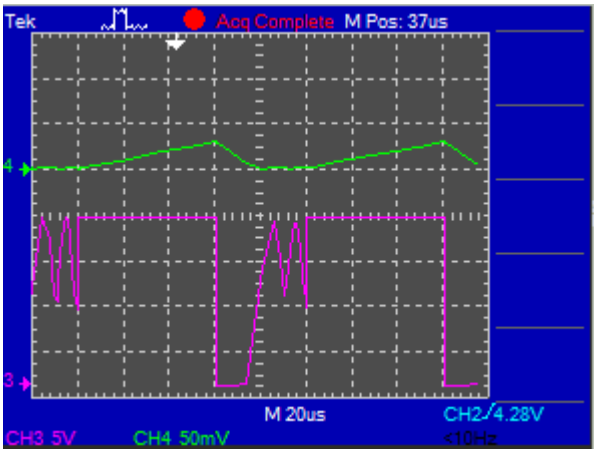

Figure 4.8

Inductor L1: I_L (green)

Diode VD2: U_{VD2} (purple)

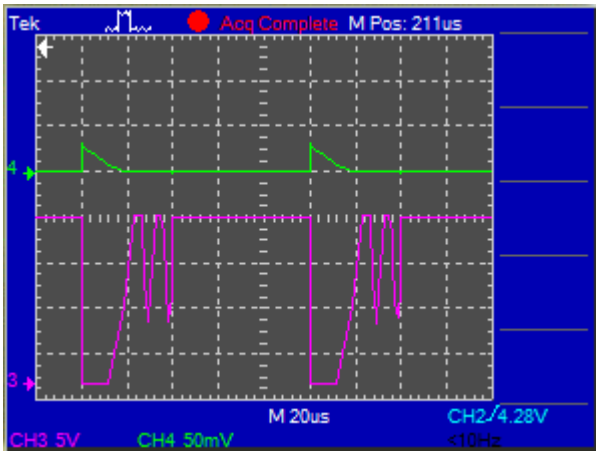

Figure 4.9

Diode VD2: I_{vd2} (green)

Diode:$U_{VD2,AK}$ (purple)

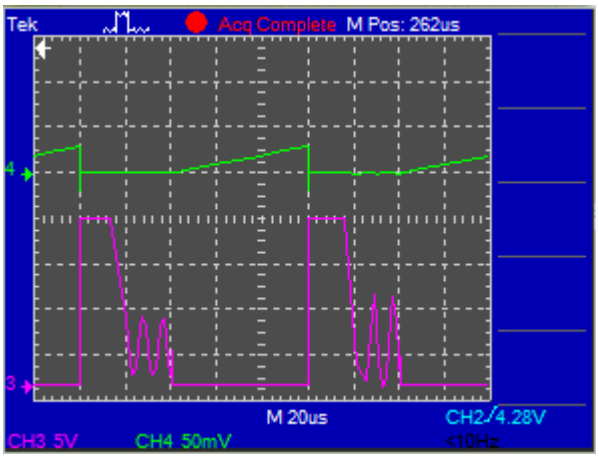

Figure 4.10

Transistor VT2: I_{VT2} (green)

TransistorVT2 : U_{SD} (purple)

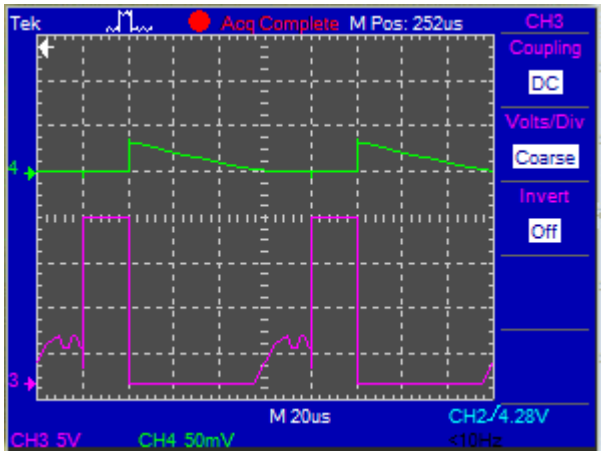

Figure 4.11

R_L =36 Ohm, D =0.2

Diode VD2 : I_{vd2} (green),

Diode VD2 :$U_{vd2,AK}$ (purple)

DCC2 – DC converter type2, boost converter (step-up), Fig.4.13 – Fig 4.18

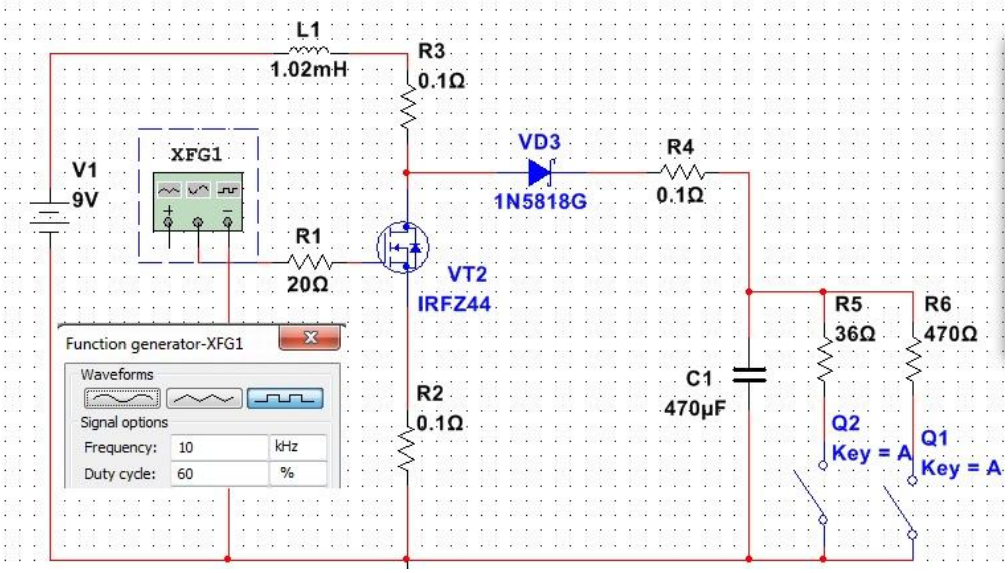

Figure 4.12 Simulation of Boost converter.

Continuous-conduction mode: R_H = 36 Ohm , D =0,6

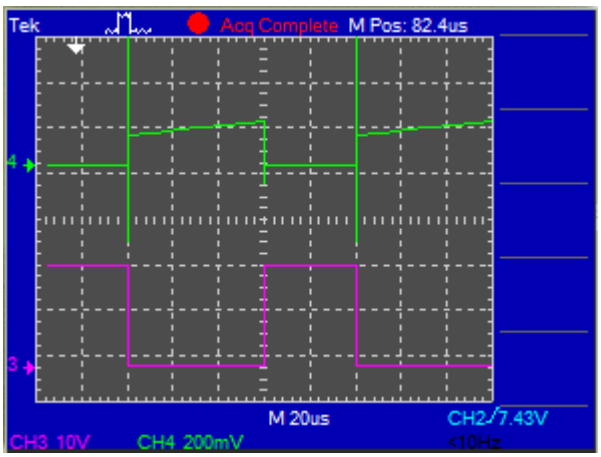

Figure 4.13

Transistor VT2: I_{vt2}(green)

Diode VD3: $U_{VD2,ds}$(purple)

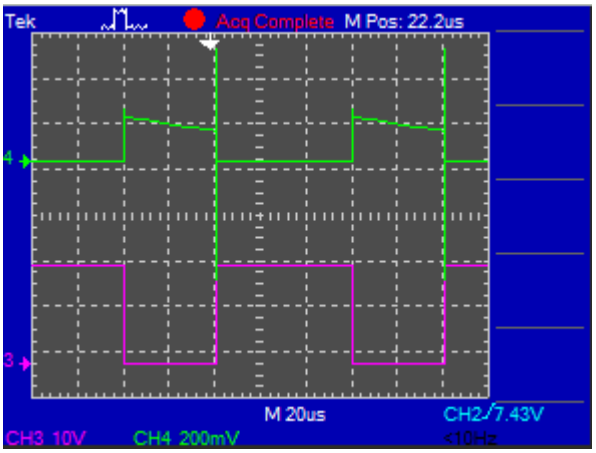

Figure 4.14

Diode VD3: I_{vd3}(green)

Diode VD3: $U_{vd3,ak}$(purple)

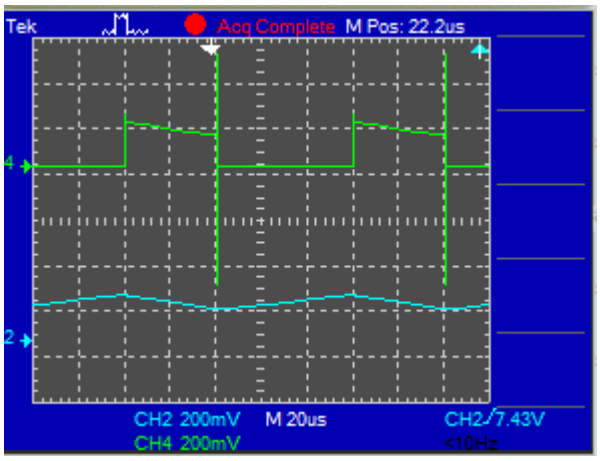

Figure 4.15

Diode VD3: I_{vd3}(green)

Inductor: I_{L1}(purple)

DCC2 : Discontinuous-conduction mode, R_L = 470 Ohm

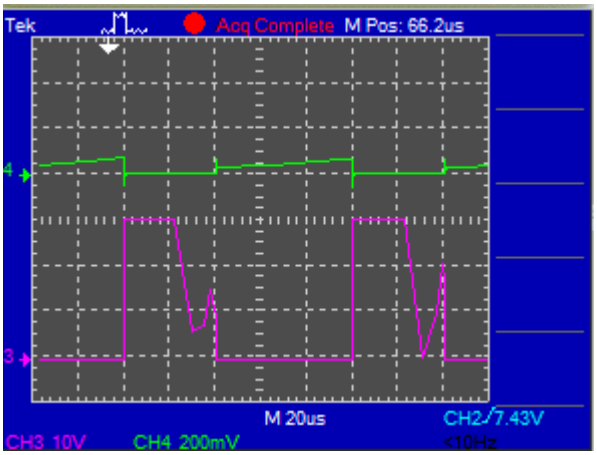

Figure 4.16

Transistor VT2: I_{VT2}, (green)

Transistor VT2:$U_{VT2,DS}$ (purple)

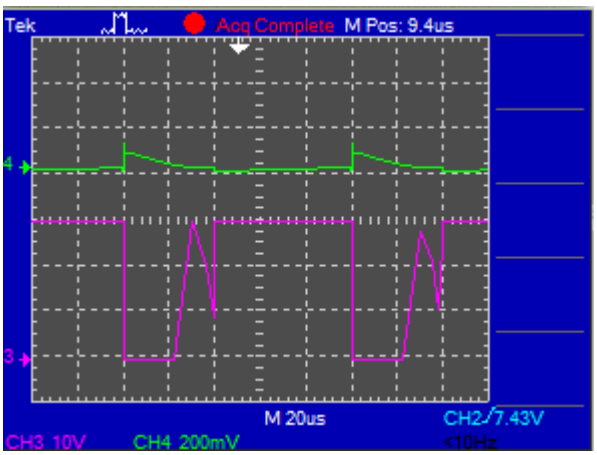

Figure 4.17

Diode VD3: I_{vd3}, (green)

Diode VD3: U_{vd3} (purple)

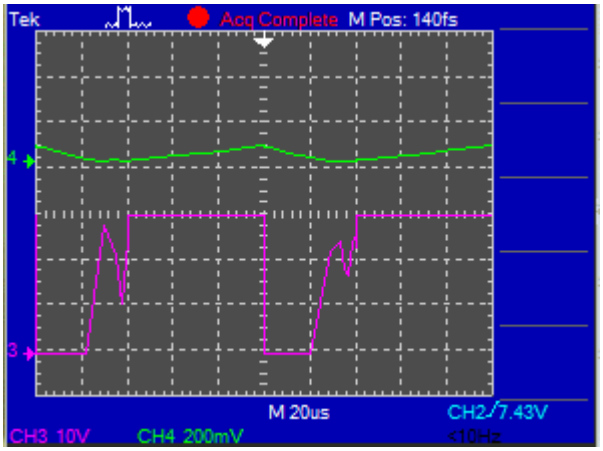

Figure 4.18

Inductor : I_{L1}, (green)

Diode VD3 : U_{vd3}(purple)

These virtually simulated diagrams give the evidence of working layout model and satisfy the required conditions.

5. Construction of the laboratory layout model.

By integrating all previously designed circuits and components there was assembled a fully operating laboratory layout model which is illustrated in [appendix №5].

Blocks and units of the laboratory model are expected to be placed in a box housing , type G317 , that could be found in shop Oomipood, where horizontal board is separately assembled. Load resistors are detached on the form-factors of housing. Above these elements in upper cover and under the board in a bottom part of housing extra holes are made to improve the cooling conditions. On the panel of the device that is mounted over the upper cover of the housing following units of control and regulation are set:

- Power supply switches for CS – SA1.1 and PU – SA3.
- PU operational mode switches SA4 and SA5.
- Potentiometer for changing Duty cycle (D) – R_5
- Small-sized leads of specific points of CS and PU.
- Connectors for adapters
- Connectors for external measuring device M4200 or multimeter.

6. Experimental part.

The most important part of all previous work is to check operational integrity of the designed laboratory layout model in real conditions. The same oscillograms will be taken as in chapter 4 , where were virtually checked continuous and discontinuous -coduction modes of Buck and Boost converters . For these goals will be used two channel USB PC oscilloscope, model PCSU1000 from Welleman instuments company. For synchronization the oscilloscope is connected to the circuit through connection X3, check Fig. 3.1. The oscilloscope is also connected to the PC station to capture the experimental diagrams.

First of all let's check Master Generator and Control Impulse Generator, where Astable Multivibrator DA1 and Monostable Multivibrator DA2 are functioning.

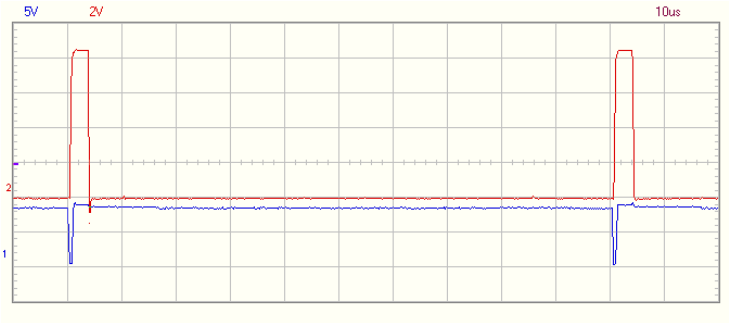

Figure 6.1 Multivibrators, D_{min}

Duty Cycle – D_{min}. (R3 =620 Ω, R4 =0)

T_i(DA1) = 1µs (blue)
T_i(DA2) = 4µs (red)

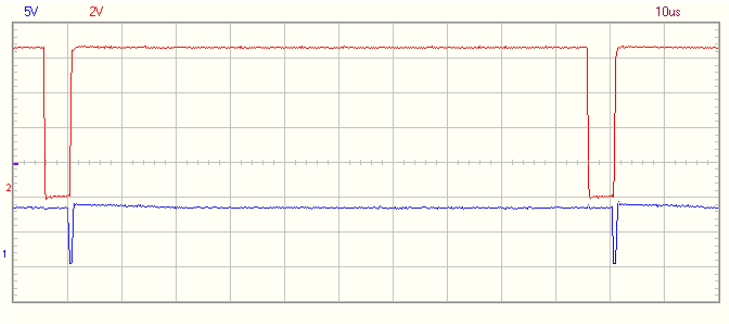

Figure 6.2 Multivibrators, D_{max}

Duty Cycle – D_{max}. (R3 =620 Ohm, R4 = 17K)
T_i(DA1) = 1µs (blue)
T_p(DA2) = 4,1 µs (red)

The result is also very good and this experiment just proved, that PWM circuit is fully functional. Duty cycle is adjustable: D= 4 ÷ 96 % , which was to be shown.

Now let's check Buck and Boost different conduction modes.

DCC1 – DC converter 1st type - Buck (step-down) , Fig 6.3 – 6.9

DD1:Continuous-conduction mode, R_L = 36 Ohm.

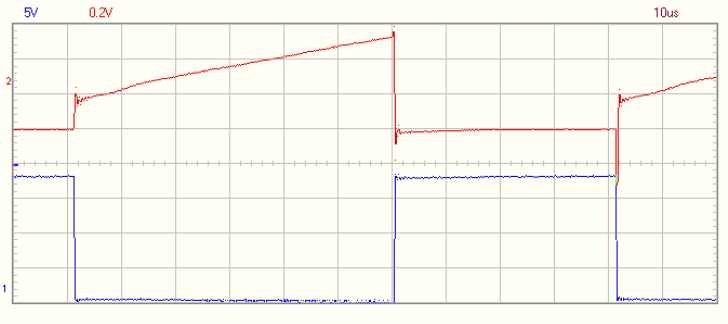

Figure 6.3

Transistor VT1:I_{VT1} (red)

Transistor VT1 U_{ds} (blue)

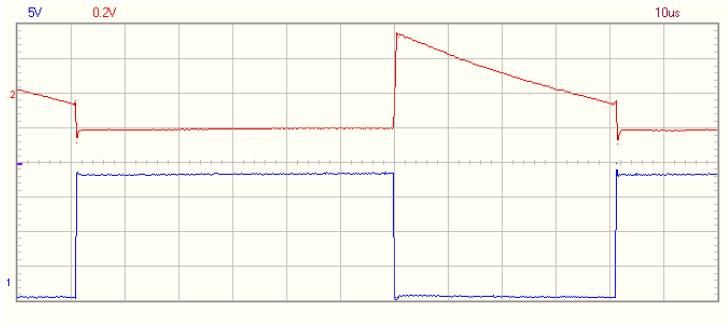

Figure 6.4

Diode I_{VD2} (red)

Diode U_{VD2} (blue),

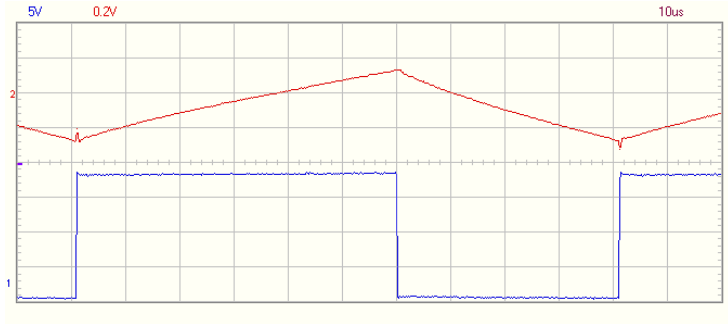

Figure 6.5

Inductor L1: I_L (red)

Diode VD2: U_{VD2} (blue)

DCC1 : Discontinuous-conduction mode, R_L = 470 Ohm

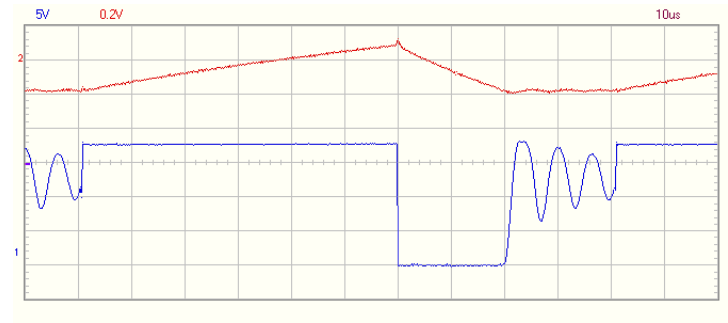

Figure 6.6

Inductor L1: I_L (red)

Diode VD2: U_{VD2} (blue)

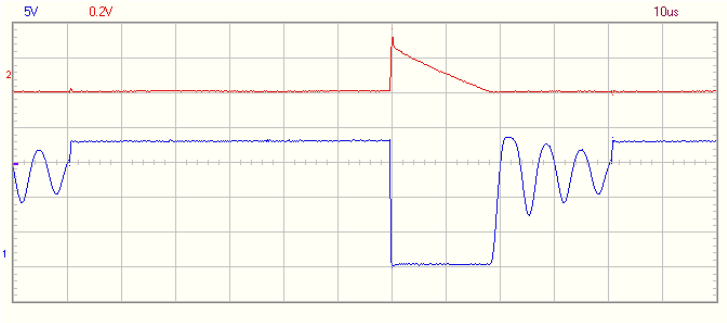

Figure 6.7

Diode VD2: I_{vd2} (red)

Diode:$U_{VD2,AK}$ (blue)

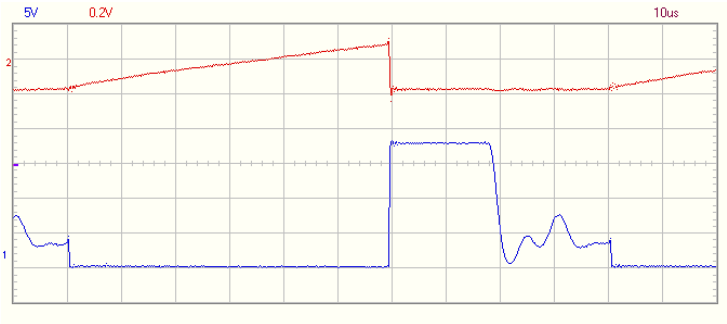

Figure 6.8

Transistor VT2: I_{VT2} (red)

TransistorVT2 : U_{SD} (blue)

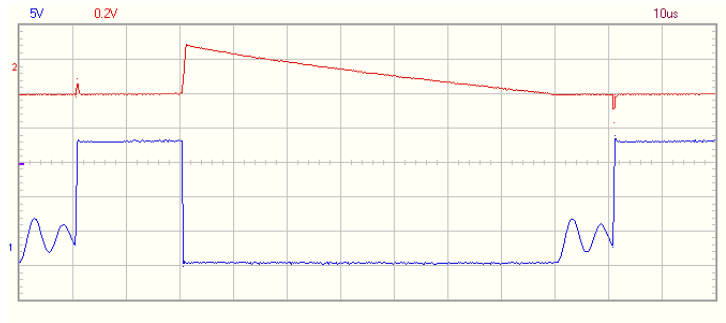

Figure 6.9

R_L =36 Ohm, D = 0.2

Diode VD2 : I_{vd2} (red),

Diode VD2 :$U_{vd2,AK}$ (blue)

DCC2 – DC converter 2nd type, Boost converter (step-up), Fig.6.10 – Fig 6.15

DCC2: Continuous-conduction mode: R_H = 36 Ohm , D =0,6

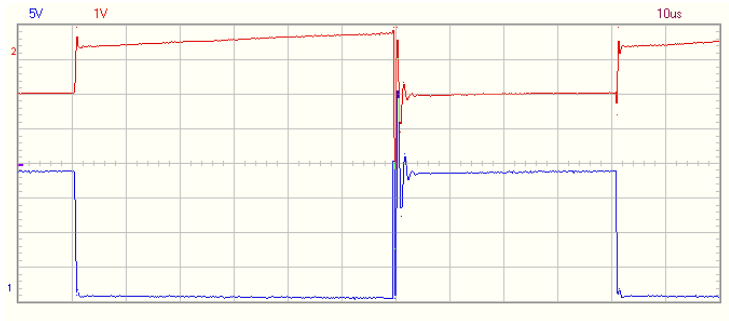

Figure 6.10

Transistor VT2: I_{vt2}(red)

Diode VD3: $U_{VD2,ds}$(blue)

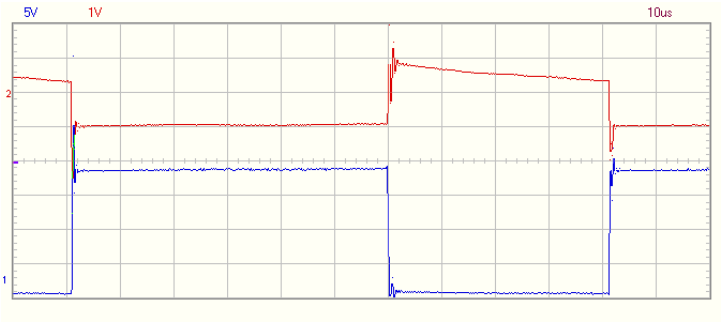

Figure 6.11

Diode VD3: I_{vd3}(red)

Diode VD3: $U_{vd3,ak}$(blue)

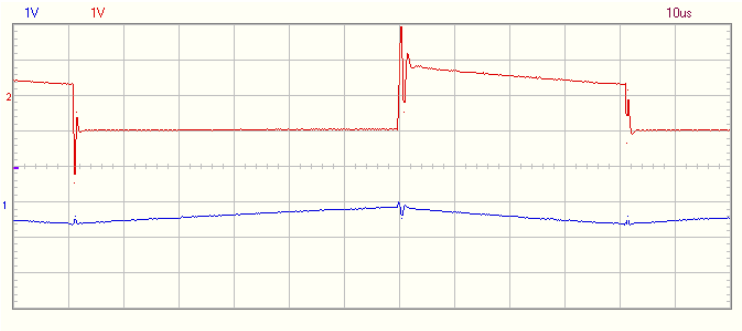

Figure 6.12

Diode VD3: I_{vd3}(red)

Inductor: I_{L1}(blue)

DCC2 : Discontinuous-conduction mode, R_L = 470 Ohm

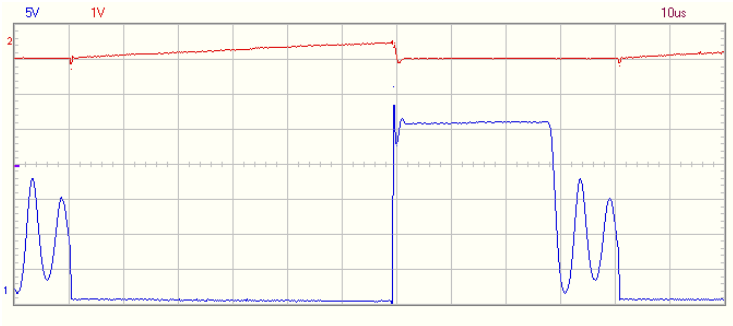

Figure 6.13

Transistor VT2: I_{VT2}, (red)

Transistor VT2:$U_{VT2,DS}$ (blue)

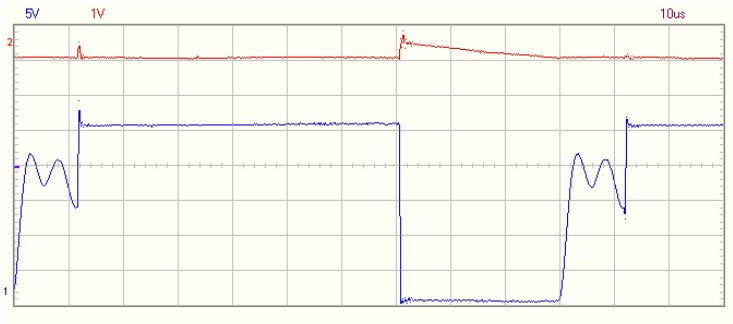

Figure 6.14

Diode VD3: I_{vd3}, (red)

Diode VD3: U_{vd3} (blue)

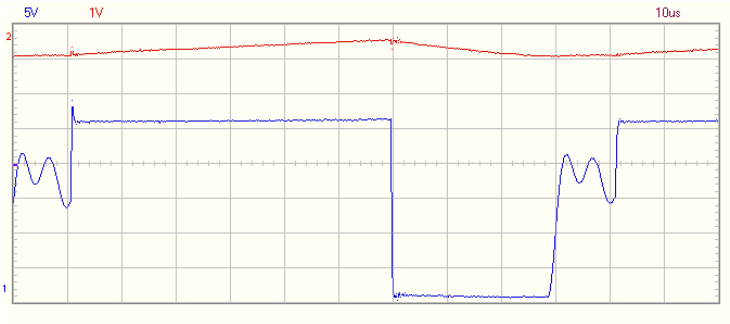

Figure 6.15

Inductor : I_{L1}, (green)

Diode VD3 : U_{vd3}(blue)

If we compare the simulated virtually diagrams to the experimental onces, we will find that they are very similar. A small differences in the oscillograms are due to the fact that components are not ideal. Fluctuations of a signal are caused by the inductor parasitic resistance. However , it still gives us the right to say that the experimental scheme has been assembled correctly and the main goal is reached.

7. Economic part.

Batch production of the laboratory model is not provided, and expected to be used for the laboratory works at the Institute of Electronics. The cost of electronic components is calculated on the base of prices in the internet-shops www.oomipood.ee 29.04.14 and http://ee.mouser.com/ 07.05.14. The components are listed in Tab. 7.1. In case of price abcence, the average price was used, taken from several online resources. The prices are given in euros.

Part Name	Value/ model	Device	Package	.Lib	Cost
PCB		PCB (A4)	PCB/PWB	-	6,5
BU3(9V)	DCJ0202 x 4	connector	DCJ0202 con-jack		1,2(4)
C1	4,7nF	capacitor	C0	rcl	0,02
C2	10nF	capacitor	C0	rcl	0,02
C3	300pF	capacitor	C0	rcl	0,02
C4	4,7nF	capacitor	C0	rcl	0,02
C5	10nF	capacitor	C0	rcl	0,02
C6	100pF	pol_capacitor	CE0	E2rcl	0,1
C7	4,7nF	capacitor	C0	rcl	0,02
C8	10nF	capacitor	C0	rcl	0,02
C9	470µF	pol_capacitor	CE0	E2rcl	0,1
DA1	LM555 x3	timer	DIL-08	st	1,05 (3)
R1	10k	POTENTIOMETER	PT-SPIN	rcl	0,45
R2	12k	resistor	R0	rcl	0,01
R3	20	resistor	R0	rcl	0,01
R4	620	resistor	R0	rcl	0,01
R5	15k	POTENTIOMETER	PT-SPIN	rcl	0,45
R6	20	resistor	R0	rcl	0,01
R7	20	resistor	R0	rcl	0,01
R8	620	resistor	R0	rcl	0,01
R9	1k	resistor	R0	rcl	0,01
R15	1k	resistor	R0	rcl	0,01
R17	36	(ПЭВ-15)	R0	rcl	0,01
R18	1k	POTENT.(ППБ-10)	PT-SPIN	rcl	0,45
SA1.1,1.2;SA4.1,4.2; SA5.1,5.2 = 6		DS01E	DS-01	switch	0,92(6)
SA2	TL36WO	TL36WO	TL3XWO	switch	0,55
SA3	DS01E	DS01E	DS-01	switch	0,7
T1	1:1	VP31	VP31	trafo	1,26
IR2110	IR2110	IR2110	DIL14	st	2,63

Part Name	Value/ model	Device	Package	.Lib	Cost
VD1	1N4148	1N4148	DO35-7	diode	0,05
VD2	MBR3100	MBR3100	MBR3*	diode	1,22
VD3	MBR3100	MBR3100	MBR3*	diode	0,10
VT1,VT2	IRFZ44N	IRFZ44N	TO220BH	tra*	1,59(2)
X1 x 20	MPB1	lug	MPB1	con-	2,0(20)
X3	R141426	R141426	R141*	con-coax	2,6(m)
Housing	G317	housing	-	-	8,58
Total cost approximately					32,73

Table 7.1 Component list.

The approximate price for a laboratory layout model is 33 euros. It should be noted that the measurement of the resistors R10-R14, R16 and inductor L1 are not listed, because these components have been borrowed from the Institute. Also adapters are not included in the price, because the Institute already owns them as a part of the laboratory equipment. The approximate price of the adapter is around 6 euros. Laboratory layout models directly from the manufacturer are very expensive nowadays and could reach several thousand euros. Hence research of a much less expensive model could be very advantageous and beneficial.

8. Safety technique issues.

Operating and electrical installation instructions are applied for the laboratory model. Access to high voltage is excluded during operation of the laboratory model. On the front panel of the model low, safe voltages are laid. Moreover layout is protected against short circuits. All the electrical pins from the specific scheme points are connected through resistors to the last, not distorting the picture of the processes, but at the same time preventing the circuit from damage in case of incorrect connection of measuring devices.

During the laboratory work should be guided by the following rules:

- Students are allowed to start the laboratory work only after studying the instructions of performing the work. After listening a short briefing from the instructor, students must sign the sheet of safety technique.
- Students are not allowed to switch on assembled and prepared for work laboratory model without the permision of the instructor.
- Changing of operating modes on the circuit is allowed to carry out only when the power supply is switched off.
- In case of detection of faults in the measuring devices or in the laboratory model, students must switch off power supply and inform the instructor.
- After the laboratory work is accomplished, laboratory model could be switched off and connections disassembled with the permission of the instructor.

9. Methodological manual for the laboratory work.

Laboratory work №.....

« DC regulators: Converters».

Objective of the work:

The objective of this work is to get acquainted with the main circuits, work processes and characteristics of DC converters.

Description of the laboratory model:

The laboratory layout model consists of the main electric board with the Control System (CS), Power Unit (PU), Load (L) and Power Supply (PS), that is formed of 4 adapters with stabilized output DC voltages 4 x 9V, placed in the panel of power strip.

Block diagram of the laboratory model is shown in the Fig. 9.1

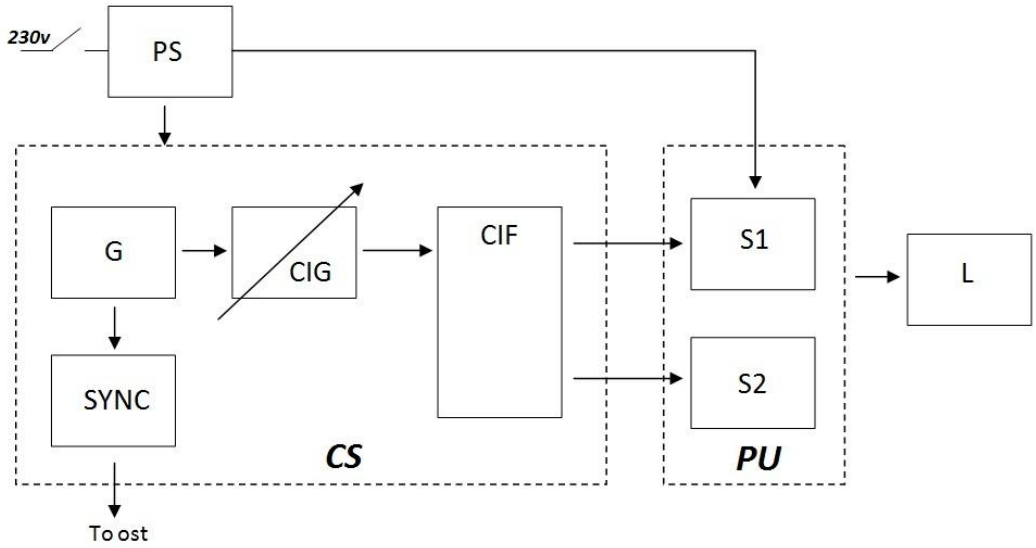

Figure 9.1 Block diagram of the DC converter.

Designations of block diagram parts in Fig 9.2:

PS – Power supply

L - Load

CS – Control System:

- G – Master Generator
- CIG - Control Impulse Generator
- CIF - Control Impulse Former
- Sync – Synchronization impulse generator

PU – Power Unit:

- S – Switch circuit

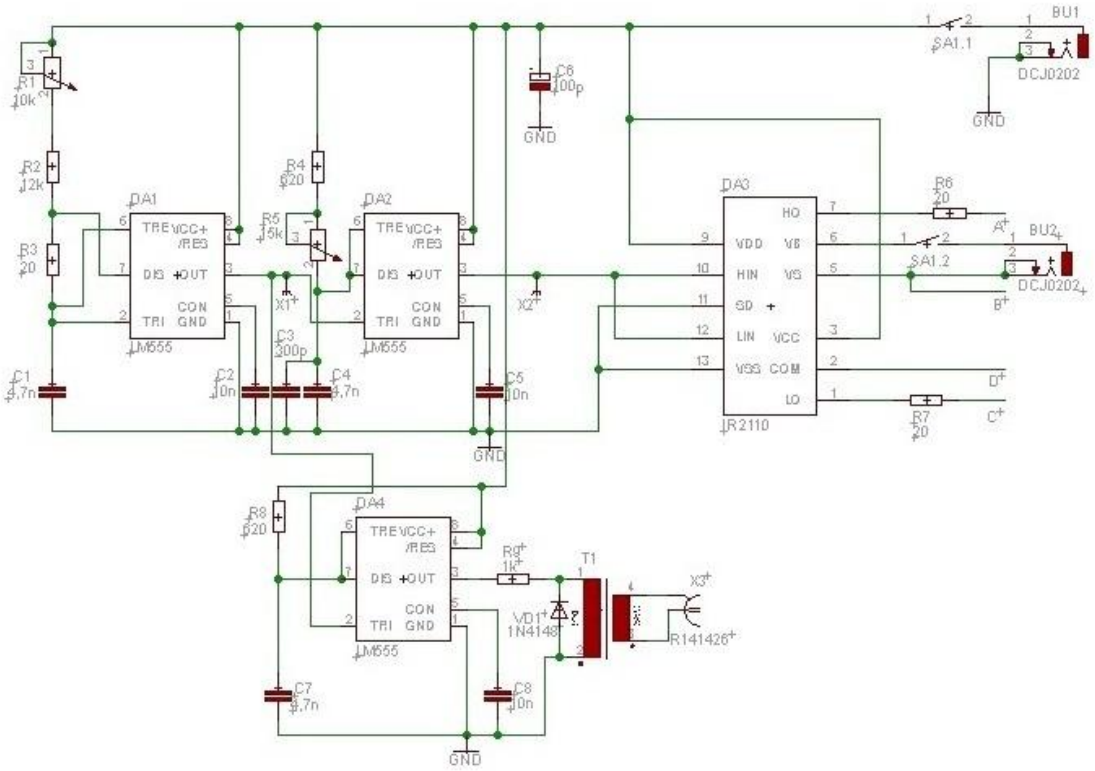

Figure 9.2 Scheme of control systems in DC converter.

Master generator (G) is designed on the base of microcircuit DA1 and works as an astable multivibrator. Its output signal launches Control Impulse Generator (CIG), designed on the base of microcircuit DA2, that as a monostable multivibrator. The length

of the output pulses is possible to change turning the rotary knob of variable resistor (potentiometer) R5. At the same time the Duty Cycle ratio (D) will be changed

$D = t_i/T$ (where t_i –time of impulse, when the switch key is opened) .

Control Impulse Former (CIF) on the base of microcircuit DA3 generates pulses with required power to regulate switch circuits S_1, S_2 of PU in the layout model. The Control System is switching on with switch SA1.

Synchronization pulse generator (SYNC) based on the microcircuit DA4 , produces pulses for oscilloscope activation in external triggering mode.

Power Unit (PU) of the laboratory layout model is designed on the base of a universal DC converter Fig. 9.3. This schematic design allows to implement in one laboratory layout model two different types of converters - buck and boost.

Universal electric schematic of PU part is shown in the Fig. 9.4

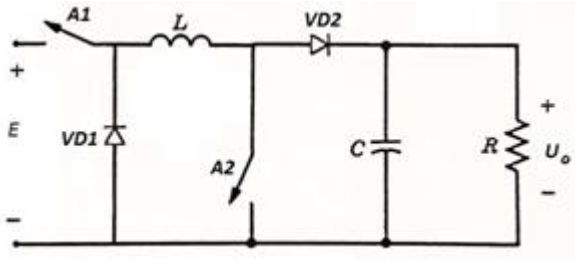

Figure 9.3 Universal circuit of DC converter, derived from the combination of basic converter circuits.

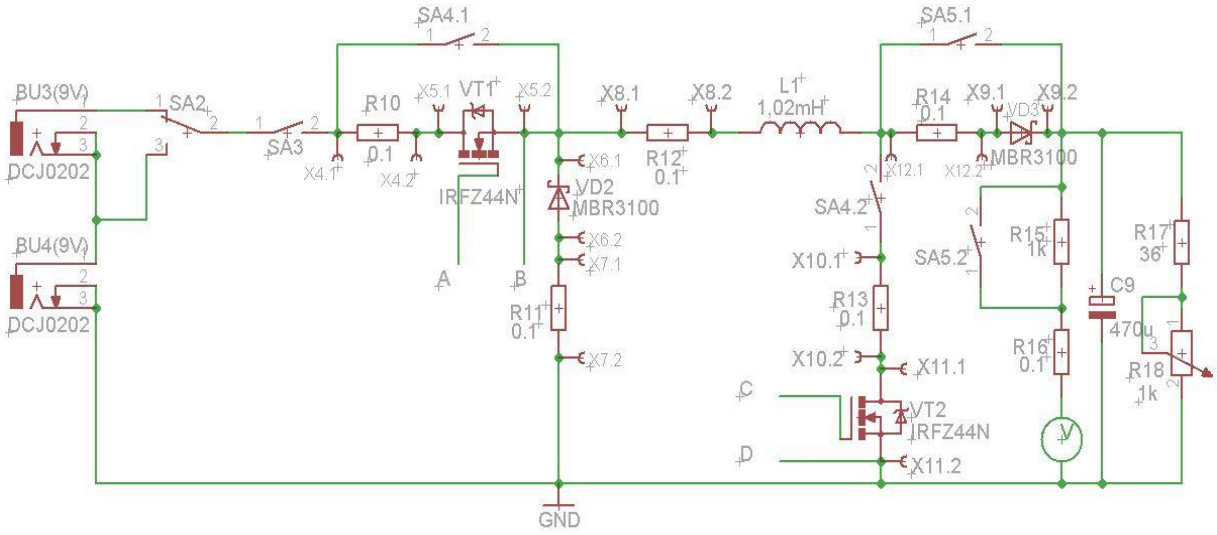

Figure 9.4 Universal PU electrical schematic of laboratory layout model.

Switching of the PU of the laboratory layout model is implemented by switch SA3. Selection of operating mode: Buck/Boost is implemented with switches SA2, SA4, SA5. Output voltage of the load is measured with a built-in pointer-type indicator PA1. Load resistance could be changed by regulating a variable resistor R18, for different operating modes(buck/boost). There are special measurement pins (points) and resistive current sensors are provided to take an oscillogram using oscilloscope.

Work task:

1. To get acquainted with the laboratory layout model, control systems and control points on the panel of the layout.
2. To join 4 adapter plugs to appropriate sockets in the layout. Then adapters could be plugged in to the power strip. Do not switch the power on.
3. Using the appropriate switches, select required operating mode of the layout.
4. Switch on adapters (using indicator button on the power strip)
5. Switch on CS (switch SA1) and PU (switch SA3)
6. Using the oscilloscope take oscillograms of output signals for Master Generator (G) and Control Impulse Former (CIF) for D =5% and D =95%.

Study the work of the layout in Buck-mode:

1. Use switches SA2, SA4 and SA5 to set Buck-mode. Equivalent circuit of PU for Buck-mode is illustrated in Fig. 9.5

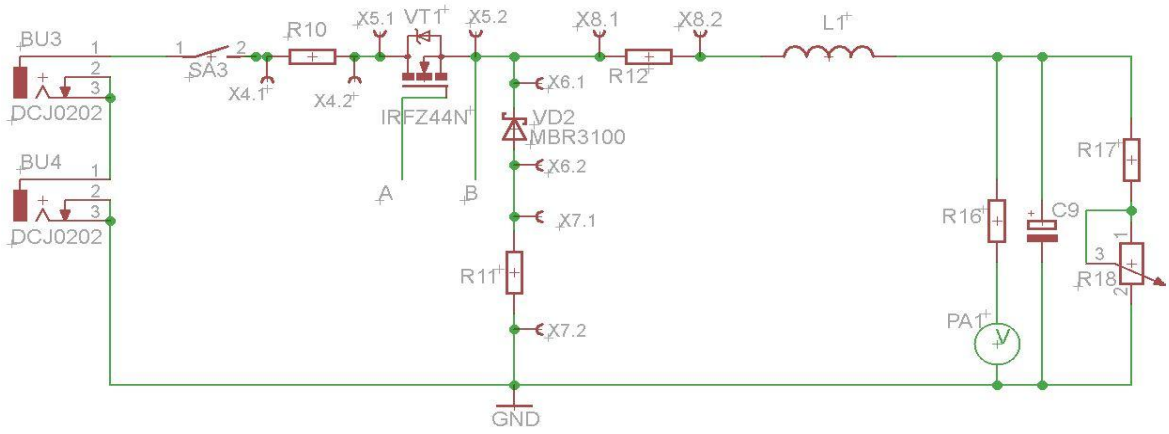

Figure 9.5 Equivalent circuit of PU for Buck-mode.

2. Take oscillograms of voltages and currents of circuit elements, if D = 0,6.

   Continuous-conduction mode: R_{load} = 36 Ohm

Parameter	Signal is taken from:
a) Current $I_{D,VT1}$	X4.1 , X4.2
Voltage $U_{DS,VT1}$	X5.1 , X5.2
b) Current $I_{F,VD2}$	X7.1 , X7.2
Voltage $U_{AK,VD2}$	X6,1 , X6.2
c) Current I_{L1}	X8.1 , X8.2
Voltage $U_{AK,VD2}$	X6.1 , X6.2

Table 9.1 Parameters for measurements.

3. Repeat task #2 for discontinuous conduction-mode, if D = 0,6. For this mode increase load resistance R_{load} ≈500 Ohm, using variable resistor R18.

4. Take regulation characteristic U_{load} = f (D), $R_{load,nom}$= 36 Ohm.

   Mark on the characteristic discontinuous-conduction mode boundary.

Study the work of the layout in Boost-mode:

1. Use switches SA2, SA4 and SA5 to set Boost-mode. Equivalent circuit of PU for Boost-mode is illustrated in Fig. 9.6

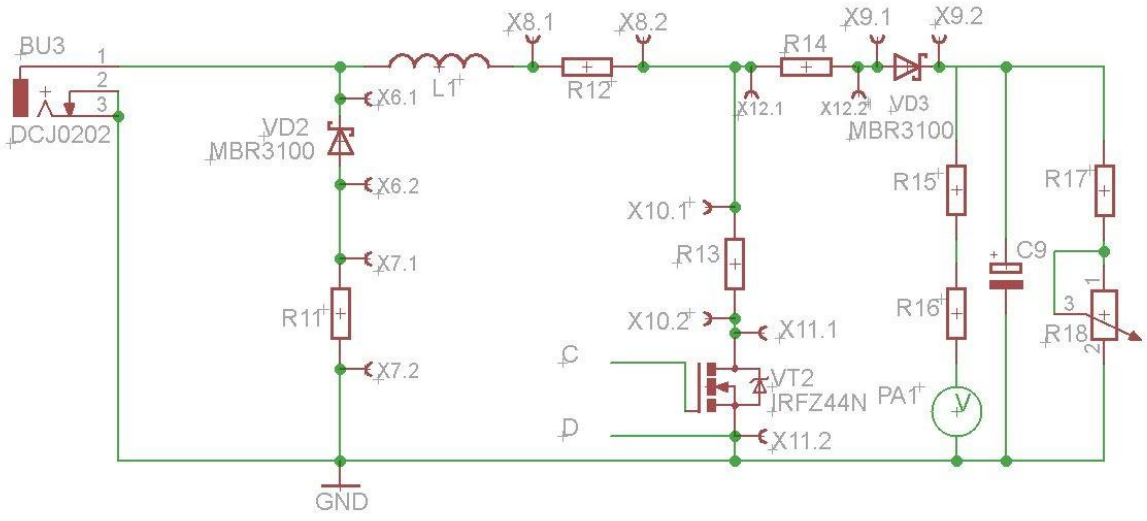

Figure 9.6 Equivalent circuit of PU for Boost-mode.

2. Take oscillograms of voltages and currents of circuit elements, if D = 0,6.
   Continuous-conduction mode: R_{load} = 36 Ohm

Parameter	Signal is taken from:
a) Current $I_{D,VT2}$	X10.1 , X10.2
Voltage $U_{DS,VT2}$	X11.1 , X11.2
b) Current $I_{F,VD3}$	X12.1 , X12.2
Voltage $U_{AK,VD3}$	X9,1 , X9.2
c) Current I_{L1}	X8.1 , X8.2
Current IF,VD3	X12.1 , X12.2

Table 9.2 Parameters for measurements

3. Repeat task #2 for discontinuous conduction-mode, if D = 0,6. For this mode increase load resistance R_{load} ≈500 Ohm, using variable resistor R18.
4. Take regulation characteristic $U_{load} = f(D)$, a) $R_{load,nom}$= 36 Ohm. b) $R_{load,max}$ = 500 Ohm.

   Mark on the characteristic discontinuous-conduction mode boundary.

Methodological guide:

1. Changing of operating mode on the circuit is allowed only when the power supply adapters are switched off.
2. During the exploration of converter circuit use oscilloscope output synchronization.
3. To measure output voltages use embedded(internal) voltmeter . If needed use external voltmeter in DC mode.
4. Regulation characteristic diagrams have to be built in relative units, considering that power supply in Buck mode E =18V , and Boost mode E = 9V.
5. On the diagrams of the measured regulation characteristics mark regulation characteristics of ideal converters.

Control questions:

1. Explain the principal of operation of converters Buck and Boost.
2. Explain features of converters Buck and Boost.
3. Explain the appearance of discontinuous-conduction mode in circuits of converters.
4. Describe the influence of discontinuous-conduction modes on the characteristics of converters.
5. Explain the influence of active resistances of inducter and switch circuits on the characteristics of converters.
6. Indicate the main areas of application for converters: Buck, Boost and Buck-Boost.

References:

1) **Mohan Ned,Tore M. Undeland,William P.Robbins**. Power Electronics, 3d edition, Hamilton Printi Company, USA: John Wiley & Sons , Inc., 2003 , 802 p.
2) **Skvarenina Timothy L.** The power electronics handbook , Boca Raton, Florida, USA : CRC Press LLC, 2002, 664 p.
3) **Marian K. Kazimierczuk** Pulse-width Modulated DC-DC Power Converters. Markono Print Media Pte Ltd., UK: John Wiley & Sons, 2008, 808 p.

Conclusion:

Developed within the bounds of the present thesis laboratory layout model for studying characteristics and operating principle of pulsed DC converters meet modern requirements for educational tutorials and equipment.

During the development there was used quite modern, available and cheap element base, oriented on the resources of TTU Department of Electronics, which affected the cost of the layout model.

The review of regulation methods for DC voltage using PWM is issued in this work, as well as the operational analysis of the main circuits of converters.

Moreover, there was developed the methodological manual for laboratory work “DC converters”. Sample report could be found in the appendices of the laboratory work.

References:

1) **Mohan Ned,Tore M. Undeland,William P.Robbins**. Power Electronics, 3d edition, Hamilton Printi Company, USA: John Wiley & Sons , Inc., 2003 , 802 p.
2) **Skvarenina Timothy L.** The power electronics handbook , Boca Raton, Florida, USA : CRC Press LLC, 2002, 664 p.
3) **Marian K. Kazimierczuk** Pulse-width Modulated DC-DC Power Converters. Markono Print Media Pte Ltd., UK: John Wiley & Sons, 2008, 808 p.
4) **Андрей Образцов, Сергей Образцов** Схемотехника DC/DC преобразователей, http://www.soel.ru/cms/f/?/311582.pdf [10.03.14]
5) **Забродин Ю.С**. Промышленная электроника. Изд: Высшая школа,1982,496 p.
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9) **Поликарпов А.Г., Сергиенко Е.Ф**. Однотактные преобразователи в устройствах питания РЭА, Радио и Связь, 1989, 158 p
10) **Семёнов Б.Ю.** Силовая электроника от простого к сложному , СОЛОН-Пресс, 2005, 416 p.
11) **Männama V.** Elektrogeneraatorid ,Tallinn, 1988, 115 p.
12) Datasheet LM555 : http://www.ti.com.cn/cn/lit/ds/symlink/lm555.pdf [22.02.14]
13) Datasheet IRFZ44N : http://www.irf.com/product-info/datasheets/data/irfz44n.pdf [25.04.14]
14) Datasheet MBR3100: http://www.onsemi.ru.com/pub_link/Collateral/MBR3100-D.PDF [25.04.14]
15) **Lõhmus I.** Ühetaktilised pingemuundurid, Diplomi töö, Tallinn , 1993, 67p

Appendices:

Appendix №1. A Sample report of the laboratory work “DC regulators: Converters”.

TALLINN UNIVERSITY OF TECHNOLOGY

Thomas Johann Seebeck Department of Electronics

<table>
<tr><td>Student: Aleksandr Pjatibratov
Code of register: 105052
Student group: IAEM21</td><td>Work was carried out
25.02.2014</td></tr>
<tr><td>Instructor: M.Pikkov</td><td>Report performed : 11.03.2014</td></tr>
<tr><td colspan="2">POWER ELECTRONICS</td></tr>
<tr><td colspan="2">Practical work № 3 “DC regulators: Converters”</td></tr>
<tr><td>Object of the experiment:
Laboratory layout model.
.....
.....
.....</td><td>The used apparatus:
1) Multimeter DMM-150.
2) Oscilloscope Rigol DS10525S.
.....
.....</td></tr>
</table>

Preparatory task:

Block diagram of the laboratory model is shown in the Fig. 1.

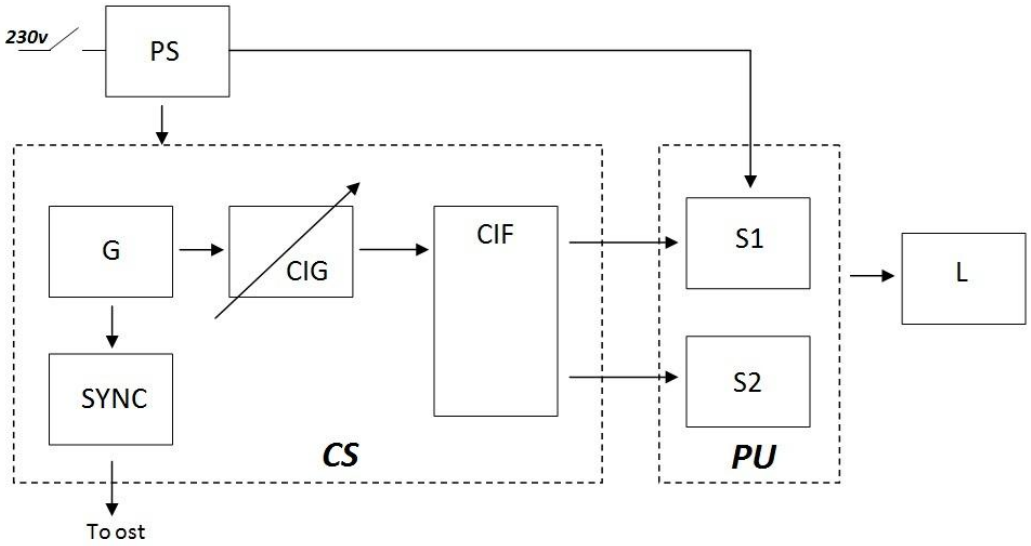


Figure 1 Block diagram of DC converter.

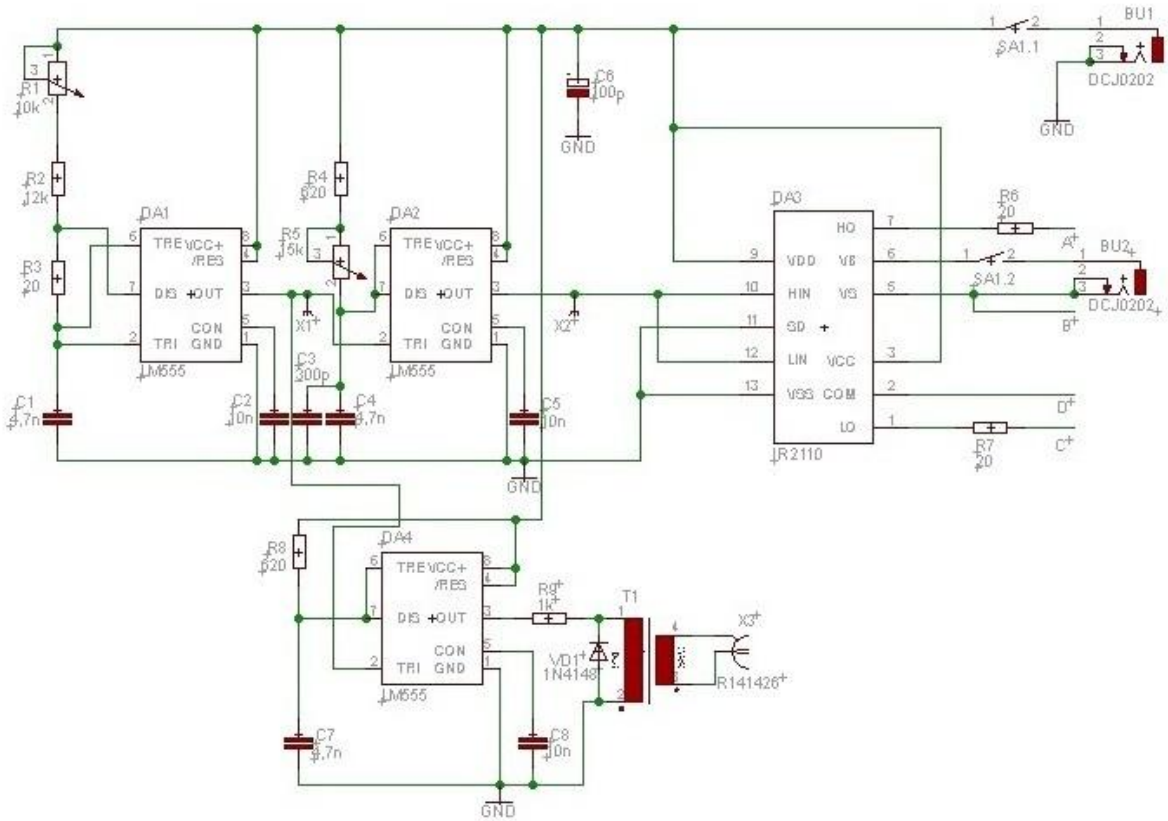


Figure 2 Scheme of Control System in DC converter.

Designations of block diagram parts:

PS – Power supply

L - Load

CS – Control System:

- G – Master Generator
- CIG - Control Impulse Generator
- CIF - Control Impulse Former
- Sync – Synchronization impulse generator

PU – Power Unit:

- S – Switch circuit

To built regulation characteristics of ideal converters we should use equation:

a) For DCC1: Buck converter

$U_L = D \times E$,

where E- power supply , E = 9V , D – Duty Cycle

b) For DCC2 : Boost converter

$U_L = E/(1-D)$,

where E – power supply, E =18 V, D – Duty Cycle

Regulation characteristics of ideal converters are marked together with experimental ones in Fig.8. Theoretical regulation characteristics are marked with dashed lines.

Results of laboratory measurements:

1. Diagrams of voltages in spesific spots of CS are brought in Fig.4,5,6,7

2. CS layout model works the same from internal and external synchronization voltage source. During the experiment Duty Cycle (D) has been changed in ranges 0,1÷0,9 in Fig 3.1-3.3.

3. Research of Buck mode. Oscillograms of PU in continuous-conduction mode of inductor are shown in Fig.4.1-4.3 and in discontinuous-conduction mode in Fig.5.1-5.3 Experimental regulation characteristics are shown in Fig.8 As it was mentioned in the task, characteristics are indicated in relative units.

4. Research of Boost mode. Oscillograms of PU in continuous-conduction mode of inductor are shown in Fig.6.1-6.3 and in discontinuous-conduction mode in Fig.7.1-7.3 Experimental regulation characteristics are shown in Fig.9

Table 1 $U_{load} = f(D)$, Buck, E=18V, R_{load}=36 Ohm.

D	0,1	0,2	0,4	0,6	0,8	0,9
Uload	-	3,6	7,02	10,44	14,04	15,66
U_l/E	-	0,2	0,39	0,58	0,78	0,87

Table 2 $U_{load} = f(D)$, Boost , E=9V, R_{load}=36 Ohm.

D	0,1	0,2	0,3	0,4	0,5	0,6	0,7	0,8	0,9
Uload	9,2	10,5	11,8	14,7	16,1	19,3	17,7	11	4,8
Ul/E	1,02	1,16	1,31	1,63	1,78	2,14	1,97	1,22	0,53

Table 3 U load = f (D), Boost, Boost, E=9V, R_{load}≈500 Ohm.

D	0,1	0,2	0,3	0,4	0,5	0,6	0,7	0,8	0,9	0,95
Uload	9,45	10,8	12,15	14,85	17,1	20,25	23,85	21,6	11,25	4,59
Ul/E	1,05	1,2	1,35	1,65	1,9	2,25	2,65	2,4	1,25	0,51

Duty cycle is changed by potentiometer R5 , that is located in monostable multivibrator circuit. Duty cycle diagrams are shown in Fig 3.1-3.3.

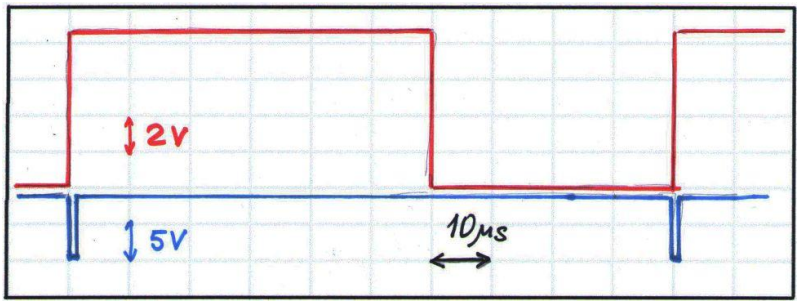


Figure 3.1 D = 0,6.

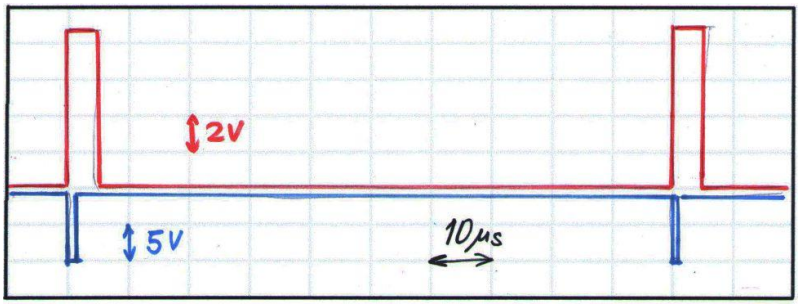


Figure 3.2 D = 0,05 or 5% .

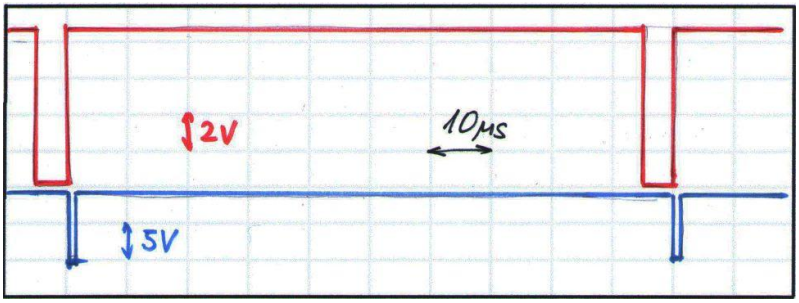


Figure 3.3 D = 0,95 or 95% .

Research of Buck converter, continous-conduction mode:

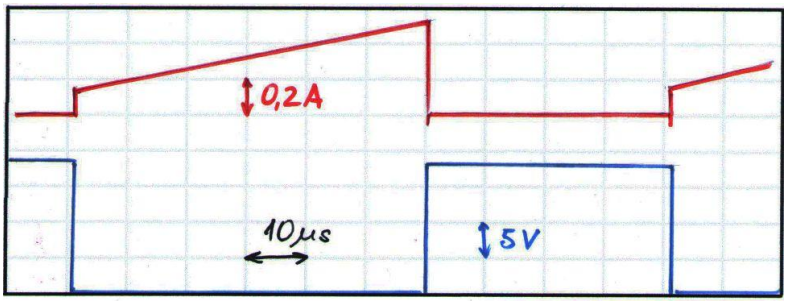


Figure 4. 1 I_{VT1} (red) , $U_{VT1,ds}$ (blue).

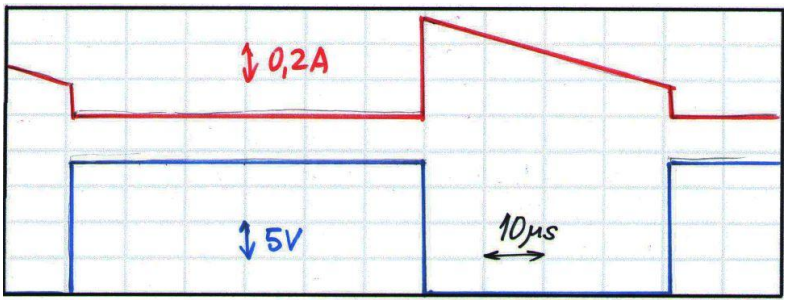


Figure 4.2 Diode: I_{VD2} (red) , U_{VD2} (blue).

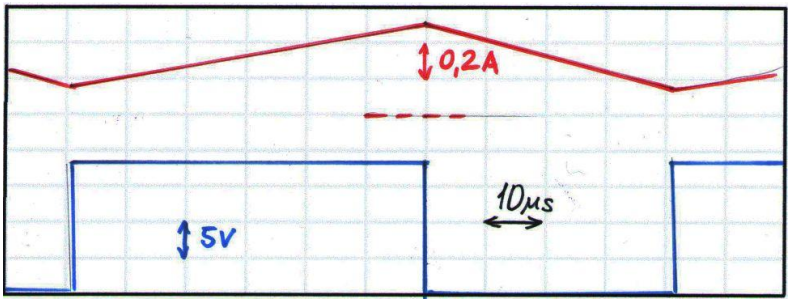


Figure 4.3 Inductor L1: I_L (red), Diode VD2: U_{VD2} (blue).

Research of Buck converter in discontinuos-conduction mode:

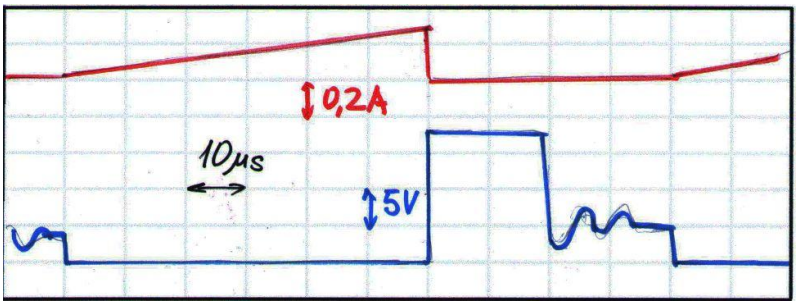


Figure 5.1 Inductor L1: I_L (red), Diode VD2: U_{VD2} (blue).

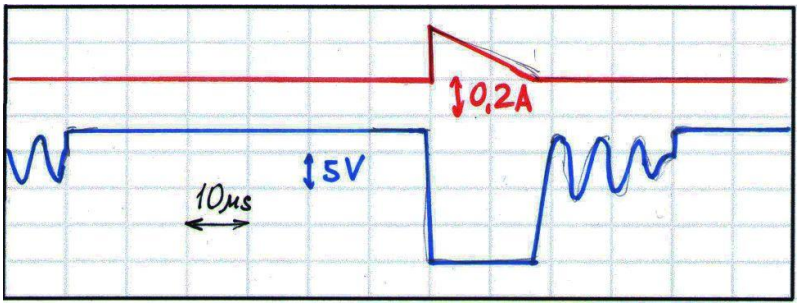


Figure 5.2 Diode VD2: I_{vd2} (red), Diode:$U_{VD2,AK}$ (blue).

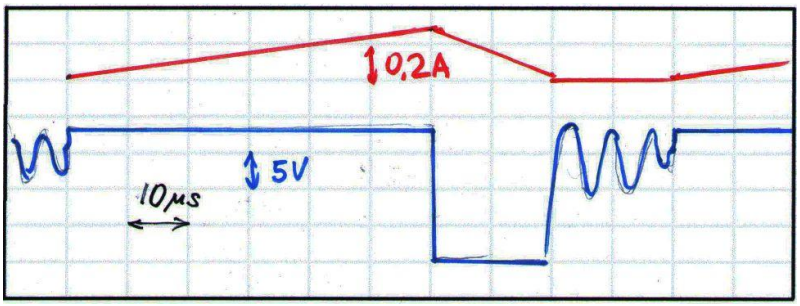


Figure 5.3 Transistor VT2: I_{VT2} (red), Transistor VT2 : U_{SD} (blue).

Research of Boost converter in continous-conduction mode:

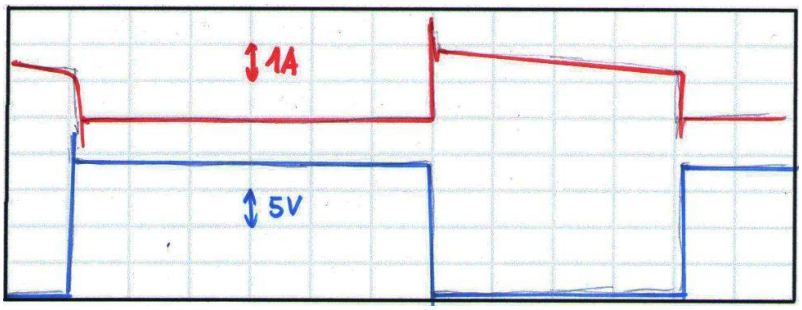


Figure 6.1 Transistor VT2: I_{vt2} (red), Diode VD3: $U_{VD2,ds}$ (blue).

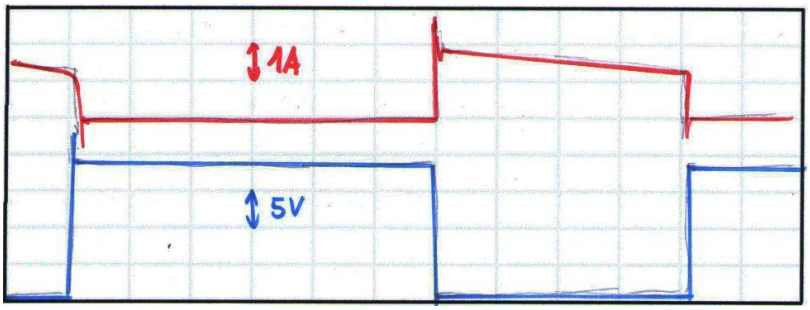


Figure 6.2 Diode VD3: I_{vd3} (red), $U_{vd3,ak}$ (blue).

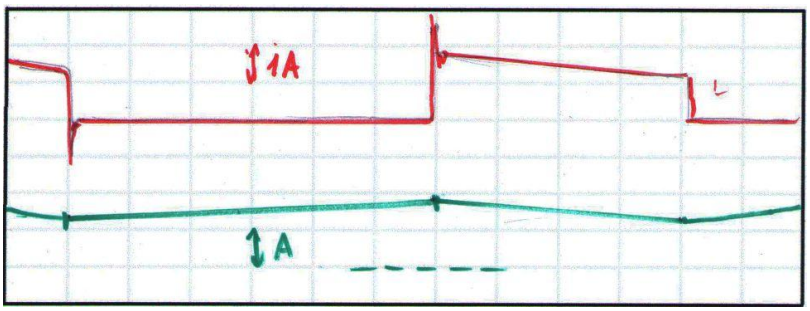


Figure 6.3 Diode VD3: I_{vd3} (red) , Inductor: I_{L1} (blue).

Research of Boost converter in discontinous-conduction mode:

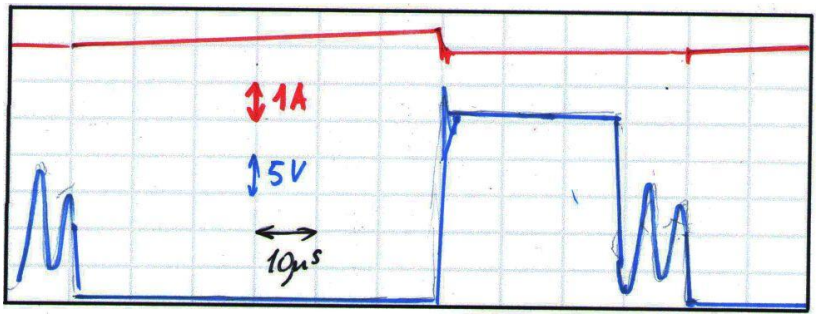


Figure 7.1 Transistor VT2: I_{VT2}, (red), $U_{VT2,DS}$ (blue).

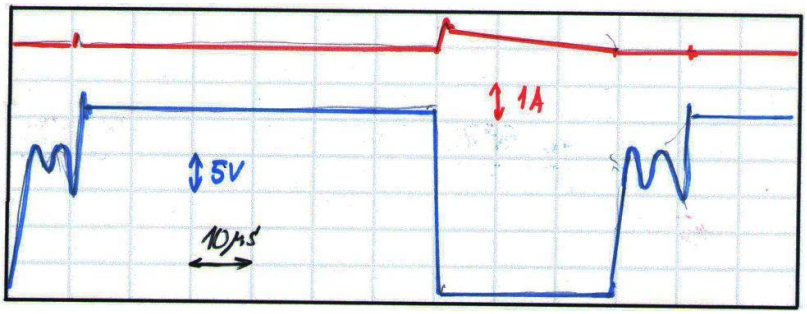


Figure 7.2 Diode VD3: I_{vd3}, (red), Diode VD3: U_{vd3} (blue).

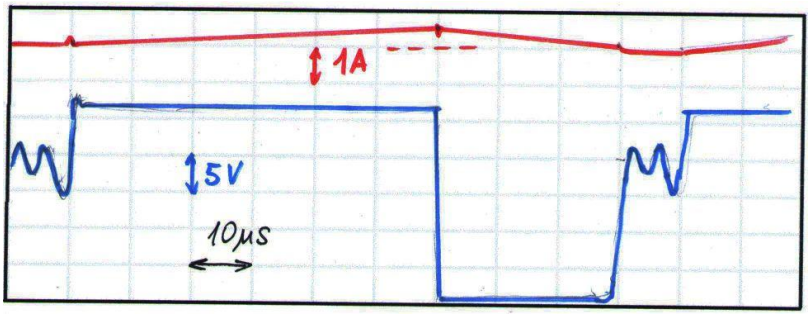


Figure 7.3 Inductor : I_{L1}, (red), Diode VD3: U_{vd3} (blue).

Regulation characteristics of DC converters:

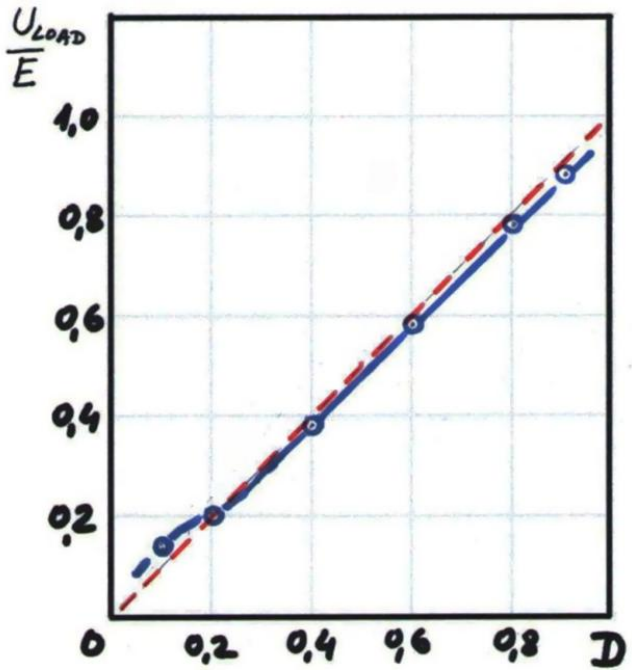


Figure 8. Regulation characteristic of Buck converter.

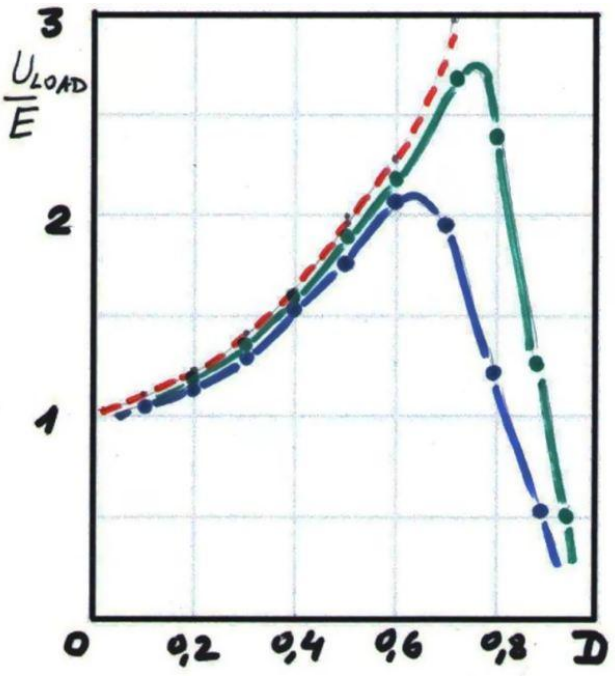


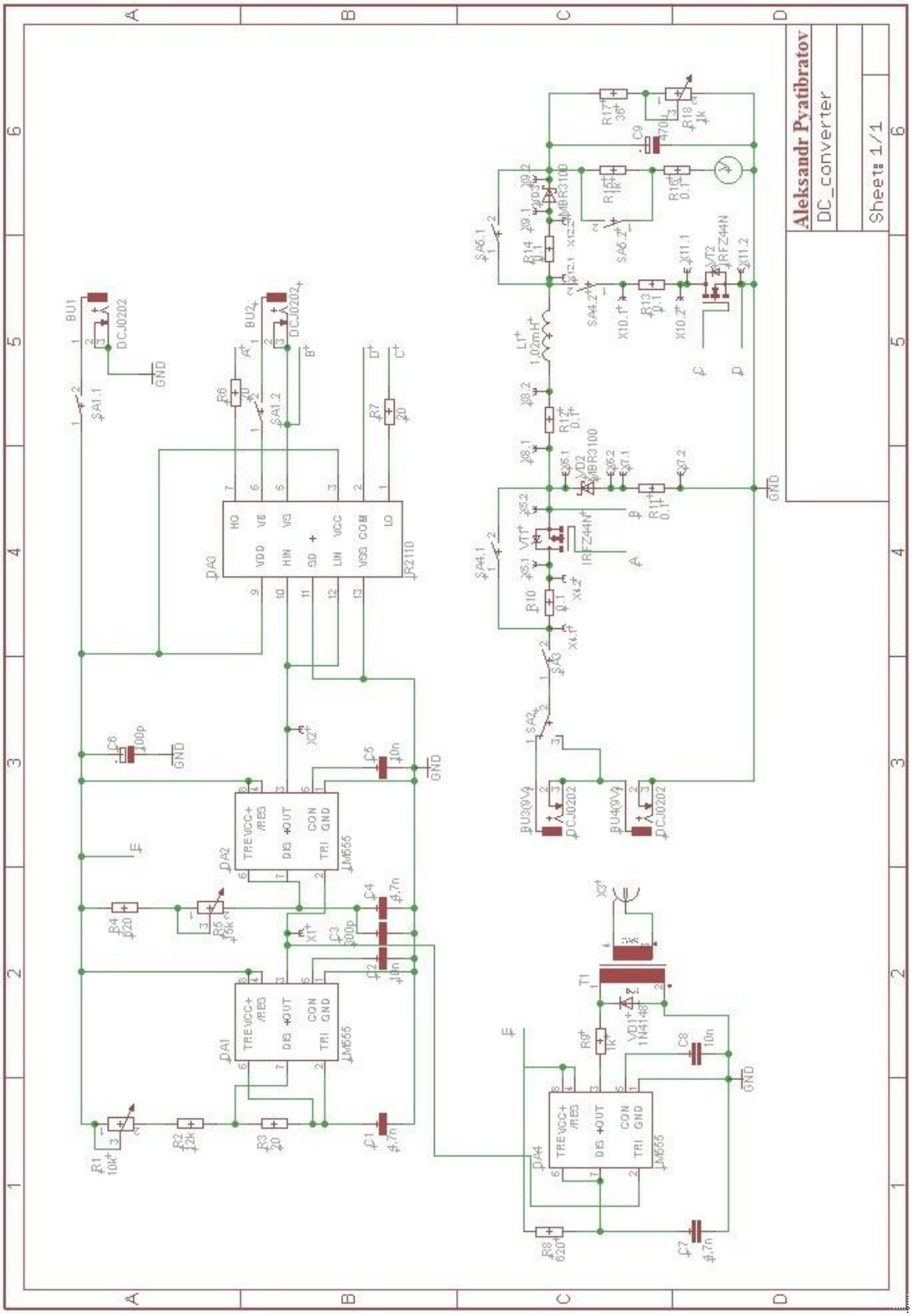
Figure 9. Regulation characteristic of Boost converter.

Conclusion:

Completed work allowed to get sufficiently acquainted with the basic types of DC converters and their operational features. The difference of experimental characteristics from ideal characteristics considerably explained by: comparability of power supply of PU and direct voltage drop of the switch schemes and flyback diodes. Secondly, explained by final value of an active resistance of inductor , internal impedance of power supply and switch schemes (and flyback diodes) relative to Load resistance.

It should be noticed, that observations of discontinuous-conduction mode in both converters are quite useful for understanding the principle of operation.

Appendix №2. Entire electric schematic of the laboratory layout model.



Appendix №3. Data sheet IR2110.

International
IOR Rectifier

Data Sheet No. PD60147 rev.U

IR2110(-1-2)(S)PbF/IR2113(-1-2)(S)PbF

HIGH AND LOW SIDE DRIVER

Features

- Floating channel designed for bootstrap operation
  Fully operational to +500V or +600V
  Tolerant to negative transient voltage
  dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V logic compatible
  Separate logic supply range from 3.3V to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

Product Summary

V_{OFFSET} (IR2110)	500V max.
(IR2113)	600V max.
I_O+/-	2A / 2A
V_{OUT}	10 - 20V
$t_{on/off}$ (typ.)	120 & 94 ns
Delay Matching (IR2110)	10 ns max.
(IR2113)	20ns max.

Packages

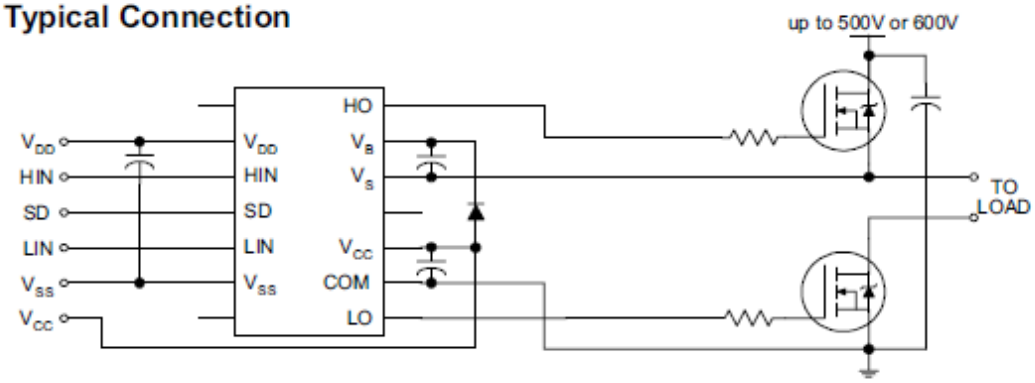
14-Lead PDIP
IR2110/IR2113

16-Lead SOIC
IR2110S/IR2113S

Description

The IR2110/IR2113 are high voltage, high speed power MOSFET and IGBT drivers with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 500 or 600 volts.

Typical Connection



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Additional information is shown in Figures 28 through 35.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply voltage	(IR2110)	-0.3	525	V
		(IR2113)	-0.3	625	
V_S	High side floating supply offset voltage		V_B - 25	V_B + 0.3	
V_{HO}	High side floating output voltage		V_S - 0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage		-0.3	25	
V_{LO}	Low side output voltage		-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage		-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage		V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS} - 0.3	V_{DD} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (figure 2)		—	50	V/ns
P_D	Package power dissipation @ $T_A \leq +25°C$	(14 lead DIP)	—	1.6	W
		(16 lead SOIC)	—	1.25	
R_{THJA}	Thermal resistance, junction to ambient	(14 lead DIP)	—	75	°C/W
		(16 lead SOIC)	—	100	
T_J	Junction temperature		—	150	°C
T_S	Storage temperature		-55	150	
T_L	Lead temperature (soldering, 10 seconds)		—	300	

Recommended Operating Conditions

The input/output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15V differential. Typical ratings at other bias conditions are shown in figures 36 and 37.

Symbol	Definition		Min.	Max.	Units
V_B	High side floating supply absolute voltage		V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	(IR2110)	Note 1	500	
		(IR2113)	Note 1	600	
V_{HO}	High side floating output voltage		V_S	V_B	
V_{CC}	Low side fixed supply voltage		10	20	
V_{LO}	Low side output voltage		0	VCC	
V_{DD}	Logic supply voltage		V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic supply offset voltage		-5 (Note 2)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)		V_{SS}	V_{DD}	
T_A	Ambient temperature		-40	125	°C

Note 1: Logic operational for V_S of -4 to +500V. Logic state held for V_S of -4V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).
Note 2: When $V_{DD} < 5V$, the minimum V_{SS} offset is limited to $-V_{DD}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, C_L = 1000 pF, T_A = 25°C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

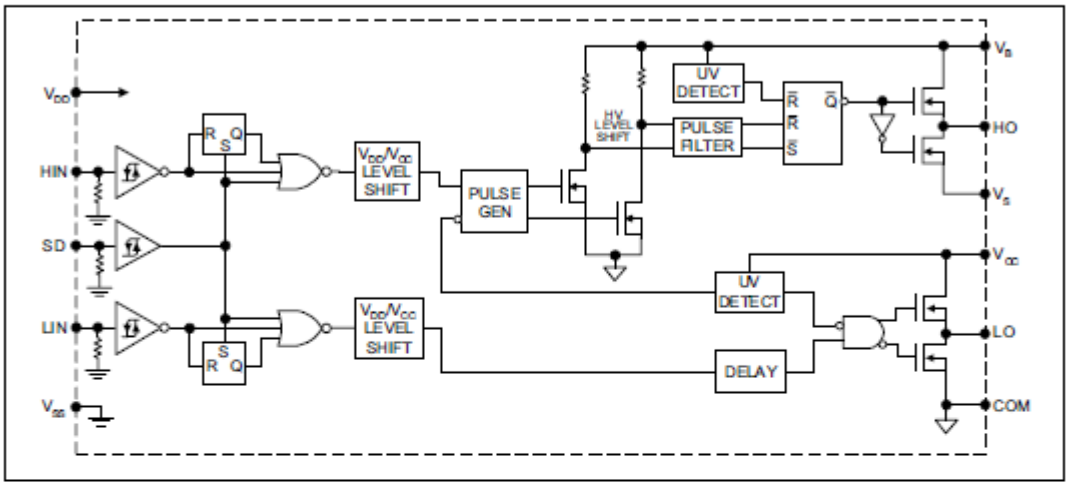
Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	Turn-on propagation delay	7	—	120	150	ns	V_S = 0V
t_{off}	Turn-off propagation delay	8	—	94	125		V_S = 500V/600V
t_{sd}	Shutdown propagation delay	9	—	110	140		V_S = 500V/600V
t_r	Turn-on rise time	10	—	25	35		
t_f	Turn-off fall time	11	—	17	25		
MT	Delay matching, HS & LS turn-on/off (IR2110)	—	—	—	10		
	Delay matching, HS & LS turn-on/off (IR2113)	—	—	—	20		

Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15V, T_A = 25°C and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Figure	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" input voltage	12	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	13	—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O	14	—	—	1.2		I_O = 0A
V_{OL}	Low level output voltage, V_O	15	—	—	0.1		I_O = 0A
I_{LK}	Offset supply leakage current	16	—	—	50	µA	V_B=V_S = 500V/600V
I_{QBS}	Quiescent V_{BS} supply current	17	—	125	230		V_{IN} = 0V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	18	—	180	340		V_{IN} = 0V or V_{DD}
I_{QDD}	Quiescent V_{DD} supply current	19	—	15	30		V_{IN} = 0V or V_{DD}
I_{IN+}	Logic "1" input bias current	20	—	20	40		V_{IN} = V_{DD}
I_{IN-}	Logic "0" input bias current	21	—	—	1.0		V_{IN} = 0V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	22	7.5	8.6	9.7	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	23	7.0	8.2	9.4		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	24	7.4	8.5	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	25	7.0	8.2	9.4		
I_{O+}	Output high short circuit pulsed current	26	2.0	2.5	—	A	V_O = 0V, V_{IN} = V_{DD} PW ≤ 10 µs
I_{O-}	Output low short circuit pulsed current	27	2.0	2.5	—		V_O = 15V, V_{IN} = 0V PW ≤ 10 µs

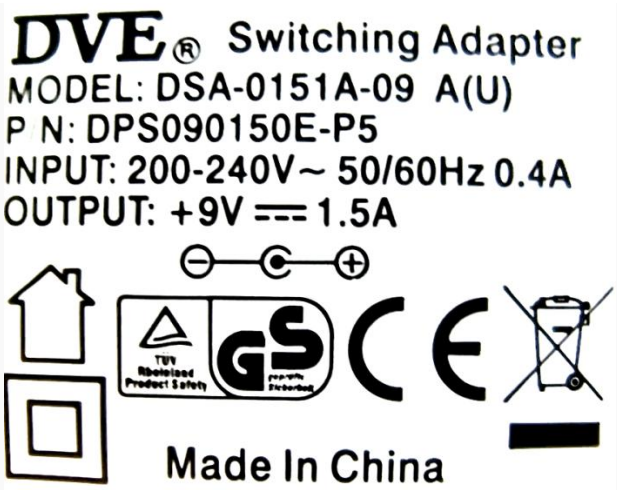
Functional Block Diagram



Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High side floating supply
HO	High side gate drive output
V_S	High side floating supply return
V_{CC}	Low side supply
LO	Low side gate drive output
COM	Low side return

Appendix №4. Adapter DVE as power supply and its parameters.



Appendix №5. The demonstrative model of the laboratory layout circuit.