THESIS ON POWER ENGINEERING,
ELECTRICAL ENGINEERING, MINING ENGINEERING D60

Research and Development of the New Topologies for the Isolation Stage of the Power Electronic Transformer

VIKTOR BELDJAJEV

TUT
PRESS

TALLINN UNIVERSITY OF TECHNOLOGY
Faculty of Power Engineering
Department of Electrical Engineering

Dissertation was accepted for the defence of the degree of Doctor of Philosophy in Engineering on May 20, 2013

Supervisors: Dr. Dipl. Ing. Indrek Roasto, Department of Electrical Engineering, Tallinn University of Technology.

Prof. Tõnu Lehtla, Department of Electrical Engineering, Tallinn University of Technology.

Prof. Dr.-Ing. Marius Klytta, Department of Electrical Engineering and Automation, Technical University of Applied Sciences Mittelhessen, Germany.

Opponents: Prof. D. Sc. (Tech.) Pertti Silventoinen, Laboratory of Applied Electronics, Lappeenranta University of Technology, Finland.

Ph. D. Marek Jasinski, Institute of Control and Industrial Electronics, Warsaw University of Technology, Poland.

Defence of the thesis: June 20, 2013

Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology, has not been submitted for any academic degree.

Viktor Beldjajev.....

ISSN 1406-474X
ISBN 978-9949-23-481-3 (publication)
ISBN 978-9949-23-482-0 (PDF)

ENERGEETIKA. ELEKTROTEHNIKA. MÄENDUS D60

Jõuelektroonilise trafo isolatsioonilüli uudsete topoloogiate uurimine ja arendamine

VIKTOR BELDJAJEV

TTÜ
KIRJASTUS

Contents

Abbreviations

ADN	active distribution network
CCM	continuous conduction mode
CDR	current doubler rectifier
CF-DC/DC	current-fed DC/DC
DAB	dual active bridge
DCM	discontinuous conduction mode
DG	distributed generation
DHB	dual half bridge
FB	full bridge
HB	half bridge
HF	high frequency
HP	high power
HV	high voltage, 100 kV...230 kV (according to ANSI C84.1)
IGBT	Insulated Gate Bipolar Transistor
IMM	improved modulation method
LC	circuit consisting of inductance L and capacitance C
LFT	line frequency transformer
LLC	resonant circuit consisting of two inductors and one capacitor
LLC-HB	HB with and LLC network
LV	low voltage, below 1 kV (according to ANSI C84.1)
MF	medium frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MV	medium voltage, 1 kV…100 kV (according to ANSI C84.1)
PEBB	power electronic building block
PET	power electronic transformer
PFC	power factor correction
PSM	phase shift modulation
PV	photovoltaic
PWM	pulse width modulation
qZSI	quasi-Z source inverter
RCD	resistor-capacitor-diode snubber
TR	transformer
VSI	voltage source inverter
ZCS	zero current switching
ZV	zero voltage
ZVS	zero voltage switching

Symbols

A_e	transformer's core area
b	boost factor
B_{MAX}	maximal flux density of the transformer
C	capacitance
D	duty cycle
D_A	relative duration of the active state
$D_{A,MAX}$	maximal relative duration of the active state
D_S	relative duration of the shoot-through state
$D_{S,MAX}$	maximal relative duration of the shoot-through state
D_Z	relative duration of the zero state
D_φ	relative duration of the phase shift
f_s	switching frequency
$i(t)$	instantaneous current
$I_{aux,AV}$	average current through the auxiliary transformer
I_{AV}	average transformer current during the half switching period
$I_{C,AV}$	average collector current of the IGBT
$I_{C,RMS}$	RMS value of the IGBT's collector current
$I_{D,AV}$	average value of the diode current
I_{IN}	input current
I_{OUT}	output current
$I_{T6,MAX}$	peak current through transistors T_6 (and T_8) of the CDR PEBB
I_{Taux}	average auxiliary switch T_{aux} current of the CDR PEBB
I_{TR}	transformer RMS current
I_{Tx}	switch current
$I_{X,VSI}$	current through the corresponding element in the VSI (in p.u.)
k_I	current ripple factor $\Delta I/I_{AV}$
k_U	voltage ripple factor $\Delta U/U_{DC}$
L	inductance
L_{aux}	leakage inductance of the TR_{aux1} and TR_{aux2} of the CDR PEBB
L_{TR}	equivalent leakage inductance of the transformer
N_{aux}	turn's ratio of the auxiliary transformers
$N_{aux,\mathrm{MIN}}$	minimum auxiliary transformers turn's ratio
N_{TR}	turns ratio of the transformer
N_{LV}	number of turns on the LV side
N_{MV}	number of turns on the MV side
P	active power
P_D	diode conduction losses
P_{IGBT}	IGBT conduction losses
P_{LV}	power on the LV port
$P_{LV,MAX}$	maximal transferred power in the reverse operating mode
P_{MV}	power on the MV port
P_{SW}	switching losses
R	resistance

r_{aux}	active resistance of the auxiliary transformer windings
r_C	on-state resistance of the IGBT
r_D	on-state resistance of the freewheeling diode
r_L	active resistance of the filter inductance
$u(t)$	instantaneous voltage
U_{CE}	collector to emitter voltage drop of the IGBT
U_D	voltage drop on the freewheeling diode of the IGBT
$U_{D,REV,MAX}$	steady state voltage stress on the diodes D_{aux1} and D_{aux2}
U_{DC}	voltage on the LV side terminals of the MF transformer
U_{LV}	low side voltage
$U_{LV,DC}$	low side DC-link voltage
U_{MV}	medium side voltage
$U_{MV,DC}$	medium side DC-link voltage
$U_{S1,MAX}$	blocking voltage over the switch S_1 of the qZSI-PEBB
U_{Tx}	steady state voltage on the switch
$U_{T6,MAX}$	steady state voltage stress on the transistor T_6 and T_8 of the CDR
$U_{Taux,MAX}$	maximum voltage stress on the auxiliary switch T_{aux} of the CDR
$U_{TR,\mathrm{P}}$	voltage on the transformer primary
$U_{TR,S}$	voltage on the transformer secondary
$U_{X,VSI}$	voltage across the corresponding element of VSI (in p.u.)
t	time
t_A	duration of the active state
t_{off}	turn OFF time of the switch
t_{on}	turn ON time of the switch
T_S	PWM period
t_S	duration of the shoot-through state
t_Z	duration of the zero state
t_φ	duration of the phase-shift
TR_{aux1}	auxiliary transformer 1 of the bi-directional current doubler
TR_{aux2}	auxiliary transformer 2 of the bi-directional current doubler
η	efficiency
φ	phase shift angle
Δi	peak-to-peak current ripple
ΔI_L	inductor current ripple
Δi_{TR}	peak-to-peak transformer current ripple
Δu	peak-to-peak voltage ripple

List of Author's Publications

The present doctoral thesis is based on the following publications that are referred to in the text by Roman numbers.

[PAPER-I] **Beldjajev, V**., Roasto, I. State of the Art Trends and Design Challenges of Power Electronic Transformer for Future Distribution Grids. Технічна електродинаміка, Alushta, Ukraine, 17-22 September 2012, pp. 55 – 62.

[PAPER-II] **Beldjajev, V**., Roasto, I., Lehtla, T. Intelligent Transformer: Possibilities and Challenges. Scientific Journal of Riga Technical University: Power and Electrical Engineering, Vol. 4, No. 29, 2011, Latvia, pp. 95 – 100.

[PAPER-III] **Beldjajev, V**., Roasto, I., Vinnikov, D. Analysis of Current Doubler Rectifier Based High Frequency Isolation Stage for Intelligent Transformer. 7th International Conference-Workshop Compatibility and Power Electronics (CPE2011), Tallinn, Estonia, June 01-03, 2011, pp. 336 – 341.

[PAPER-IV] **Beldjajev, V**., Roasto, I. Impact of Component Losses on the Efficiency of the Bi-Directional Current Doubler Rectifier Based Isolation-Stage. The 38th Annual Conference of the IEEE Industrial Electronics Society (IECON2012), Montreal, Canada, 25-28 October 2012, pp. 5209 – 5214.

[PAPER-V] **Beldjajev, V**., Roasto, I. Efficiency and Voltage Characteristics of the Bi-Directional Current Doubler Rectifier. Przeglad Elektrotechniczny, Vol. 88, No. 8, 2012, Poland, pp. 124 – 129.

[PAPER-VI] **Beldjajev, V**., Roasto, I., Zakis, J. Impact of Component Losses on the Efficiency of a New Quasi-Z-Source Based Dual Active Bridge. Doctoral school of Computing, Electrical and Industrial Systems DoCEIS 2013, IFIP AICT 394, Portugal, pp 485 - 492.

[PAPER-VII] **Beldjajev, V**., Rang, T., Zakis, J. Steady State Analysis of the Commutating LC Filter Based Dual Active Bridge for the Isolation Stage of Power Electronic Transformer. 8th International Conference-Workshop Compatibility and Power Electronics (CPE2013), Ljubljana, Slovenia, June 05-07, 2013, pp. 138 – 143.

[PAPER-VIII] **Beldjajev, V**., Lehtla, T., Zakis, J. Impact of Component Losses on the Efficiency of the Commutating LC-Filter Based Dual Active Bridge for the Isolation Stage of the Power Electronic Transformer. 8th International Conference-Workshop Compatibility and Power Electronics (CPE2013), Ljubljana, Slovenia, June 05-07, 2013, pp. 132-137.

The copies of the publications are included in Appendix 1.

Author's own contribution

This section describes the author's contribution to the papers included in the thesis.

[PAPER-I] Viktor Beldjajev is the main author of the paper, responsible for the literature review and data collection. He had a major role in writing. He presented the paper at International Conference „Silovaja Elektronika i Energo-effektivnostj 2012 CEE'2012", Alushta, Ukraine.

[PAPER-II] Viktor Beldjajev is the main author of the paper, responsible for the literature review and data collection. He had a major role in writing. He presented the paper at Riga Technical University 52nd International Conference, Riga, Latvia.

[PAPER-III] Viktor Beldjajev is the main author of the paper, responsible for the literature review, data collection, performed calculations and modeling. He had a major role in writing. He presented the paper at 7th International Conference-Workshop Compatibility and Power Electronics (CPE2011), Tallinn, Estonia.

[PAPER-IV] Viktor Beldjajev is the main author of the paper, responsible for the literature overview, data collection, calculations and modeling. He had a major role in writing.

[PAPER-V] Viktor Beldjajev is the main author of the paper, responsible for the literature review, data collection, calculations and experimental measurements.

[PAPER-VI] Viktor Beldjajev is the main author of the paper, responsible for the literature review, data collection, calculations and experimental measurements. He had a major role in writing. He presented the paper at the Doctoral School of Computing, Electrical and Industrial Systems DoCEIS 2013, Portugal.

[PAPER-VII] Viktor Beldjajev is the main author of the paper, responsible for the literature review, data collection, calculations and modeling. He had a major role in writing. He presented the paper at 8th International Conference-Workshop Compatibility and Power Electronics (CPE2013), Ljubljana, Slovenia.

[PAPER-VIII] Viktor Beldjajev is the main author of the paper, responsible for the literature review, data collection, calculations and modeling. He had a major role in writing. He presented the paper at 8th International Conference-Workshop Compatibility and Power Electronics (CPE2013), Ljubljana, Slovenia.

1 INTRODUCTION

1.1 Background

Modern trends in electrical energy technology are characterized by steadily growing need for renewable energy sources, energy storage, and smart grid technologies. Most widely utilized sources of renewable energy are photovoltaic energy, wind energy, tidal energy and hydrogen based fuel cell energy [1]. Continuous penetration of renewable energy sources into the distribution grid superimposes new challenges to the existing electric power transmission systems. This is due to the unpredictable nature of renewable energy resources in comparison with the conventional energy system, where the energy production and consumption can be predicted and scheduled with tolerable deviations. Conventional power system consists of large centralized generators, passive transformers, transmission lines, substations and consumers, whereas electrical energy flows uni-directionally from the generator's side to the consumers. Today's line frequency (50 Hz and 60 Hz) AC transmission systems use the magnetically coupled transformer concept for voltage elevation, transmission over long distances and voltage reduction for residential use. The traditional line frequency transformer (LFT) has simple construction, high efficiency and reliability and galvanic isolation. In addition, the LFT technology has proven itself during the era of industry. During the last decade, the basic construction of the LFT has remained the same, but the improved material technology allowed higher saturation densities and lower hysteresis losses to be achieved, resulting in very efficient transformers.

However, the growing number of renewable energy sources has resulted in a rising number of distributed power plants that are in principle subject to energy fluctuations. Therefore, it is essential to build energy storages (e.g. batteries, ultra capacitor banks, hydrogen buffer) to the distributed power plants to compensate the power demand during the low production periods (e.g. during the night for PV systems, silent wind periods for wind turbines). In addition, the consumers can supply energy to the grid by means of a local (e.g. roof mounted) power plant, regenerative braking of electrical drives and vehicle-to-grid systems. Thus, future power generation and distribution is likely to involve a substantial amount of the distributed renewable energy sources and micro grids. Many distributed generation (DG) sources cannot be connected directly to the AC systems, hence they require power electronic interface. To easily connect these new energy sources to the grid and improve the power quality by harmonic filtering, voltage sag correction, dynamic control of the power flow, a new power electronic transformer (PET) is required.

Concept of the Power Electronic Transformer

PET, also known as a solid state transformer or intelligent transformer, is a new type of transformer based on the power electronic converter that aims to better voltage regulation, power transmission, isolation and power quality

improvement of the grid. The basic idea behind the PET is to use medium frequency ($f > 1$ kHz) instead of low frequency in order to achieve considerably higher power density of the magnetic core and reduce its size. Moreover, the PET employs "active" control of the electrical energy by continuous monitoring and maintaining the desired network conditions. In comparison with the LFT, the PET has the following advantages:

- **Bi-directional power flow control:** The bi-directional power flow between the sources and the loads can be realized by utilizing the active front end topologies and the proper control of the active switches. In the electrical energy distribution system that incorporates renewable energy sources, storage devices and loads, the bi-directional power flow capability is one of the most important requirements for the PET.
- **Reduced mass and volumes**: As the power throughput density of the transformer is inversely proportional to the frequency, increasing the frequency allows better utilization of the steel magnetic core and reduction in transformer size allowing the high power densities to be achieved in the smaller cores. In comparison with the conventional LFT the size reduction up to three times is possible [2].
- **Power quality**: The control of the reactive power and power factor correction (PFC) has been stated to be one of the most important objectives of the PET. PFC circuits can be implemented on the MV and on the LV terminals that in turn make the additional capacitor banks for compensating reactive power unnecessary [3]. Moreover, the input and output ports of the PET are independent of each other, thus the quality of the output voltage is immune against the harmonics on the input side. The filtering is done by using the energy stored in the DC-link capacitors and active control [4].
- **Protection against distortions**: In order to achieve seamless operation of the network the adaptive control systems that can react on different fault conditions in the network are required. In the PET such voltage distortions like voltage sag, surge on the MV side are not reflected on the low voltage side of the transformer and vice versa. Such ride-through capability is achieved by the active control of the switches and presence of the storage elements (capacitors) in the DC-link of the PET.
- **Environmental safety**: The cooling mineral oil of the LFT poses a risk to the environment due to its toxic contents. The tendency is to avoid the oil in the cooling of the PET, instead the air-cooling can be successfully utilized. Thus the danger of oil pollution will be eliminated and the need for special oil-baths under the substations will be excluded.
- **Smart grid ready**: The PET is mainly aimed to operate first of all in the active distribution networks, where the „passive" control of the energy flow will be improved by adding innovative devices with sophisticated control features to the grid. The PET can be equipped with an advanced communication interface that includes smart metering, diagnostics, fault tracing, protection and distance control features. Advanced measurements are necessary for data acquisition to achieve a higher degree of the network

automation and more deterministic system control [5]. Such features would for example make the PET react on the LV side short circuit by turning off one phase or the whole device and also continue normal operation on the LV side in case of blackout on the MV side.

The PET can replace the LFT in the future active distribution networks (ADN-s), such as smart-grid and microgrid, where the bi-directional power flow and flexible control functions are required. The list of the most important requirements that the PET has to correspond to is presented in [PAPER-I]. The ADN-s operate at the MV level, hence the PET must be adaptable to the existing voltage levels that can range from 0.4 kV to 35 kV worldwide. In addition, the efficiency of the PET must be comparable with the efficiency of the LFT. The US Department of Energy has released the standard for liquid and dry type distribution transformers, effective since 2010 [6]. The standard defines the minimum efficiency of the LFT to be higher than 97 % irrespective of the power rating, however, the standard value approaches 99.5 % for most liquid-immersed power transformers. According to the literature the target efficiency for the PET is 96…98 % depending on the power rating [7].

PET in Future Active Distribution Networks

The aim of the ADN-s is to provide a flexible infrastructure allowing novel distribution and transmission networks to withstand demands that will be placed on them by penetration of the novel generation types, increasing energy demand, harnessing the renewable energy potential and supporting the low-carbon energy systems in an environmentally acceptable manner [5]. A schematic of a semi-autonomous ADN that can separate itself from the main grid and operate in islanding mode is shown in Figure 1.1. In comparison with the traditional passive networks that have limited control of the parameters, low penetration of the renewables and poor monitoring, the ADN-s are aimed to have sophisticated control of power quality and power flow direction between the power plants, loads and DG-s attached to the distribution level, with continuous network condition monitoring. The ADN-s consist of the national grid, distributed power generating units and different loads that are interconnected into one system.

The role of the PET in such systems is to act as an interface between the power grid and loads. It can be regarded as an energy router [8], [9] that can supply the energy during the power down of the main grid (islanding mode) or compensate the power during the higher demand periods. An additional storage that is attached to the PET reduces the influence of the unpredictable power generation on the grid. In such a way, the consumers are protected against the disturbances in the power grid and at the same time the reactive power generated by the loads would not penetrate into the power grid [1]. As a result the operation of the distribution system would be more stable and efficient.

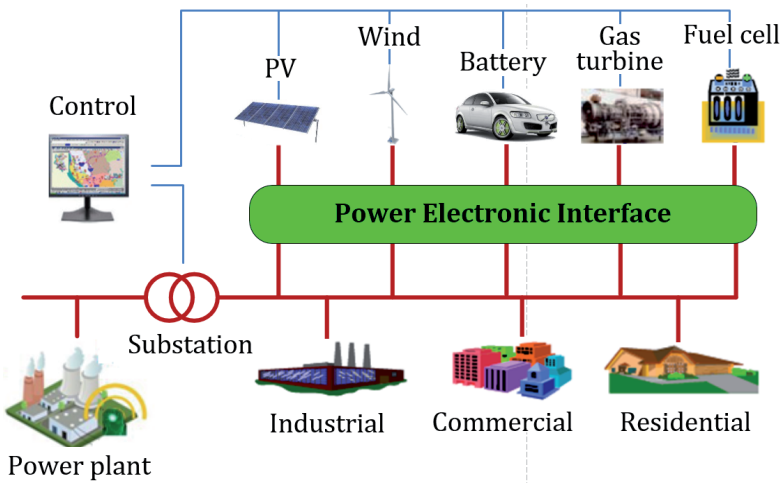


Figure 1.1. A schematic of a semi-autonomous ADN.

Challenges of the Isolation Stage

The topologies of the PET can be classified according to the number of power conversion stages (see chapter 2.1). The three-stage topology, where the isolation stage represents a high frequency isolated DC/DC converter, is the most advantageous among others. The isolation stage provides the voltage conversion and galvanic isolation between the MV and LV ports. The isolation stage can be divided into two logical entities on the MV and on the LV ports of the transformer, which can be seen as power electronic building blocks (PEBB). The PEBB is a standardized module that allows rapid configuration of power converters to meet specific customer needs, including: AC-DC conversion, DC-AC conversion, frequency changers and/or DC-DC voltage changers [10].

Due to the presence of the transformer, the isolation stage has great impact on the weight and the volumes of the PET and eventually on the whole distribution system. In order to achieve high power density (and significant mass reduction compared with the LFT), semiconductors must have the ability to be switched under high switching frequency while maintaining reliable operation under high voltage and high current conditions. The efficiency of the isolation stage depends on the losses in the components. Most crucial of the losses are the conduction, switching and core losses. Research in [1], [11] focused on the analysis of the conduction, the switching and the core losses in the different parts of the PET. According to the research in [11], the losses in the two-level rectifier based isolation stage can comprise 68 % of the total losses.

It can be concluded that the isolation stage will determine the volumes and efficiency of the PET and will play a key role in the power conversion. Thus, investigation of the isolation stage and improvement of the power conversion characteristics are very important and challenging tasks. By investigating the new topologies, such features like the losses, current and voltage stress, the

dynamic behavior and flexibility of the isolation stage can improve the bottlenecks of the existing DC/DC converters. The investigation and development of the DC/DC converter topologies for the performance optimization is the major task of the thesis.

1.2 Main Hypotheses and Objectives of the Thesis

The PET presents a new type of transformer that is based on power electronics. It provides a flexible alternative for the traditional LFT in the future ADN-s, where it acts as an energy router. However, the technology faces numerous challenges that need to be solved before the PET can be integrated into the future ADN. The main purpose of the research is to locate the challenges of the commonly used DC/DC converters and synthesize new medium-frequency isolated DC/DC converter topologies for the isolation stage of the PET. The topologies are to be analyzed mathematically and validated with simulations and experiments.

The Main Hypothesis of the Research

A three-stage topology is considered to be one of the most advantageous topologies for the power electronic transformer. The isolation stage of the three-stage topology is the most critical part of the power electronic transformer considering the wide voltage and power regulation capabilities and the efficiency. By adding new power electronic building blocks to the isolation stage, the power and voltage regulation ranges can be extended. Moreover, the voltage and current stress on the components can be reduced.

The Main Objectives of the Thesis

- to analyze and classify the current state-of-the-art technologies and development trends of the power electronic transformer concept;
- to analyze the current state-of-the-art technologies and development trends of the isolated bi-directional high frequency DC/DC converters;
- to identify weaknesses of conventional topologies of the isolation stage and propose new power electronic building blocks for the LV side of the isolation stage;
- to perform the comparative analysis between the traditional approach and the proposed power electronic building blocks;
- to define directions for the future research based on the challenges obtained from the comparative analysis.

1.3 Contribution of the Thesis and Dissemination

The doctoral thesis is based on the 8 published articles and conference papers composed by the author of the thesis. The study was carried out during the years 2009 – 2013 at Tallinn University of Technology in Tallinn, Estonia. The study was a part of the following projects: Optimal energy conversion and control in smart and microgrids, Intelligent Transformer – Analysis of Operating Modes

(ETF8687), New Converter Topologies and Control Methods for Electronic Power Distribution Networks (SF0140016s11). The originality of the thesis lies in the scientific and practical novelties described further.

Scientific Novelty

Scientific novelty of the doctoral thesis includes:

- classification and analysis of the current state-of-the-art technologies and development trends of the power electronic transformer and bi-directional isolated high frequency DC/DC converters;
- proposal of new power electronic building blocks, such as a current doubler rectifier with bi-directional power flow capability, a quasi-Z source inverter and a current-fed DC/DC converter with an active clamp, for the isolation stage of the power electronic transformer;
- derivation of the mathematical models and assessment of the component losses on the efficiency of the proposed power electronic building blocks.

Practical Novelty

The practical novelty of the doctoral thesis includes:

- improved modulation method for the qZSI and current-fed DC/DC converter with an active clamp to increase the voltage and power regulation range;
- experimental investigation of the proposed power electronic building blocks regarding their impact on the component voltage and current stresses;
- design guidelines for the proposed PEBB-s.

Dissemination of the Results

The results of the doctoral thesis have been presented by the author at 11 international conferences. The author has published 10 international scientific papers directly associated with the thesis. Three of them are available in the *IEEE* database and two have been published in the international peer-reviewed journals.

2 TECHNOLOGICAL OVERVIEW

2.1 Topologies of the PET

A technological overview of the topologies for the PET and their classification is presented in [PAPER-I] and [PAPER-II]. Numerous topologies for the PET have been proposed by different authors. However, many of the proposed topologies do not support the bi-directional power flow that is a major requirement for the PET in the ADN. Other important requirements comprise galvanic isolation and capability of interconnecting renewable energy sources and energy storage devices. The PET topologies can be classified according to the number of power conversion stages [12], [13] as depicted in Figure 2.1.

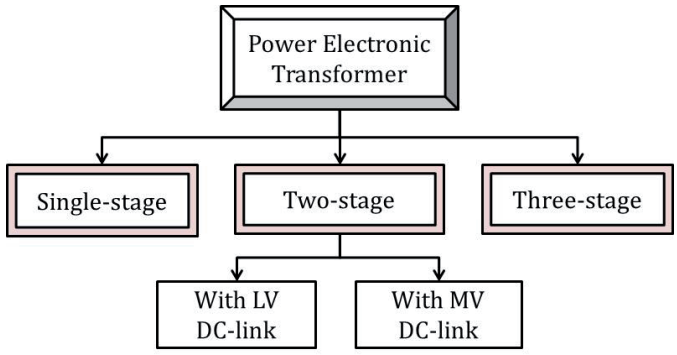


Figure 2.1. Classification of the PET topologies based on the number of stages.

Single-stage PET structure comprises direct AC-AC conversion from low voltage (LV) AC to medium voltage (MV) AC and vice versa [14]. The block diagram of a single stage topology of the PET is shown in Figure 2.2. Typically, such topologies are based on different matrix converter [15]-[17] and cycloconverter [18] topologies. Although this is the most straightforward approach to AC-AC power conversion, including such benefits as low weight and low cost, it is problematic, since each switch must be able to block full primary voltage and also be capable of conducting full secondary current [19]. Lack of the DC-link in the single stage topologies is a major drawback because integration of the storage elements and power factor correction circuit require additional devices that will result in increased complexity, size and cost of the system. In addition, this single-stage topology is sensitive to the distortions, since disturbances on one side of the converter may also reflect to the other side [2].

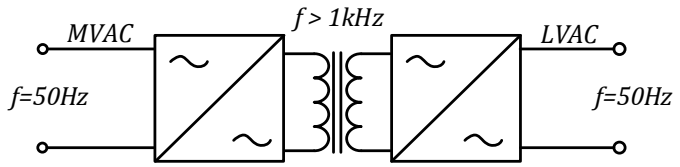


Figure 2.2. Single-stage topology ofthe PET.

The two-stage topologies can be subdivided into topologies with LV DC-link [20] - [23] and MV DC-link [24], [25] as shown in Figure 2.3. Here the low frequency AC is directly converted to the high frequency AC and rectified back to DC on the transformer secondary. Then it is converted to 50 Hz output voltage using a PWM inverter. The switches on the AC-AC side must be four-quadrant to withstand bi-polar voltages and currents. This topology has some notable disadvantages. First, the reactive power compensation feature in the two-stage topology with LV DC-link is complicated on the MV side and requires additional circuitry that results in a higher cost. Moreover, the energy sources cannot be connected directly to the PET due to lack of the MV DC-link. Second, the two-stage topology with MV DC-link lacks the possibility of interconnecting the storage elements directly to the PET.

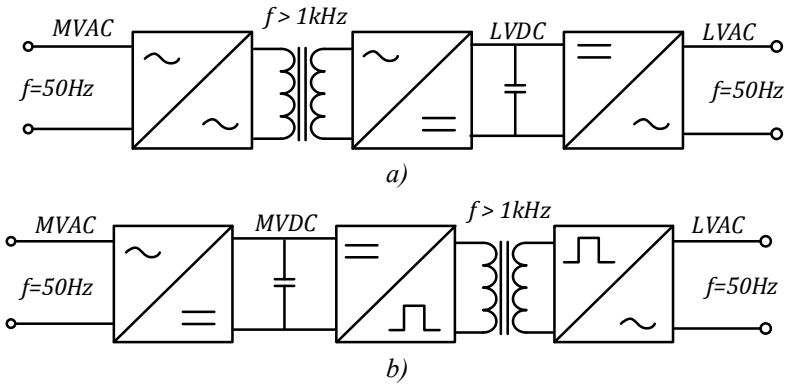


Figure 2.3. Two stage topologies of PET: a) with LV DC-link; b) with MV DC-link.

The three-stage topology is the most preferred and investigated PET topology today, since various converter topologies can be chosen for the different power conversion stages that give a wide playground for the performance optimization of the PET [1], [12], [19], [26] - [35]. The three-stage topology of the PET is shown in Figure 2.4. It consists of three power conversion stages: the input stage, the isolation stage and the output stage. The input stage is an active front end rectifier that rectifies the MV AC to the MV DC voltage. In the isolation stage the DC-DC conversion takes place by converting MV DC voltage into high frequency square-wave AC voltage and is transferred to the MF

transformer, where the voltage level is reduced and rectified again on the LV DC side, forming this way a LV DC-link. Finally, the LV DC is converted back to 50 Hz AC voltage by means of the inverter in the output stage. The three-stage PET topology has a bi-directional power flow capability, thus the power can be transferred from the LV port towards the MV port.

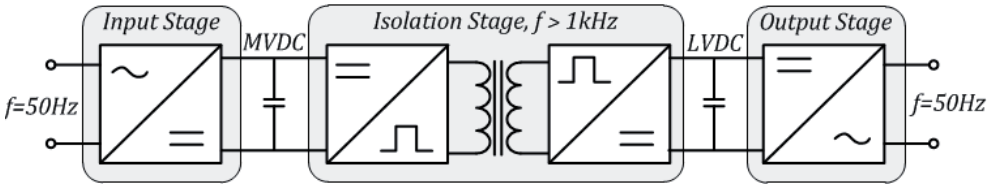


Figure 2.4. Three-stage topology of the PET.

Presence of two different voltage level DC-links allows interconnecting the energy storage devices and the renewable energy sources into one system. Integration of power-factor-correction, sag compensation and isolated DC-DC converters can decrease the losses and consequently improve the efficiency. For these reasons, the three-stage topology seems to be the most advantageous among the other topologies. Though, a high switch count is the major drawback of this topology due to increased conduction and switching losses. However, the losses can be reduced by use of the new-generation *SiC* or *GaN* based switches and different control techniques that enable the zero voltage switching (ZVS) and/or zero current switching (ZCS) to be achieved.

2.2 Topologies for the Isolation Stage

In order to meet the demands of medium voltage and high power capability for the distribution network, two different trends can be seen in the industry and power electronics communities. One way is development of the new semiconductors with higher nominal voltage and current ratings and their integration into existing two-level converter topologies using the series/parallel connections. Second is the development of the new multi-level converter topologies by using the conventional semiconductors [36] - [38].

Series connection of the power switches with high voltage and current ratings can inherit the benefits of well-known control methods. However, these devices are more expensive and they still do not meet the voltage rating requirements set by the future distribution systems. The research in [38] showed that series connection of the MOSFETs and IGBTs may result in unsymmetrical voltage sharing between the switches due to unequal parameters of the switches (leakage current, switching delays, collector-to-emitter capacitance). Therefore additional methods for voltage-balancing are needed to prevent the failures caused by the transients and static phases. The failure in one element will cause a failure of the entire converter that will result in low reliability [39].

Multi-level MV DC/DC topologies

The MV multi-level DC/DC converters use conventional power switches but have a complex structure and control in comparison with the two level converters. They consist of arrays of power switches, diodes and capacitive voltage sources. Correct combination allows the multi-level voltage waveforms to be generated, while maintaining the equal voltage sharing between the switches [39]. Thus a multi-level converter topology is suitable for the MV side to clamp the voltage across each switch that in turn reduces the required switch blocking voltage. Among several multi-level configurations the cascaded, diode clamped and flying capacitors are best known [39] - [44]. The proposed three-level topologies are shown in Figure 2.5. The key components of the diode clamped three-level converter are the diodes D_1 and D_2 that are used to clamp the voltage across each switch to only half the DC bus voltage. The flying capacitor converter works in a similar way as the diode clamped converter, however the voltage across the switches is clamped by clamping capacitor C_3.

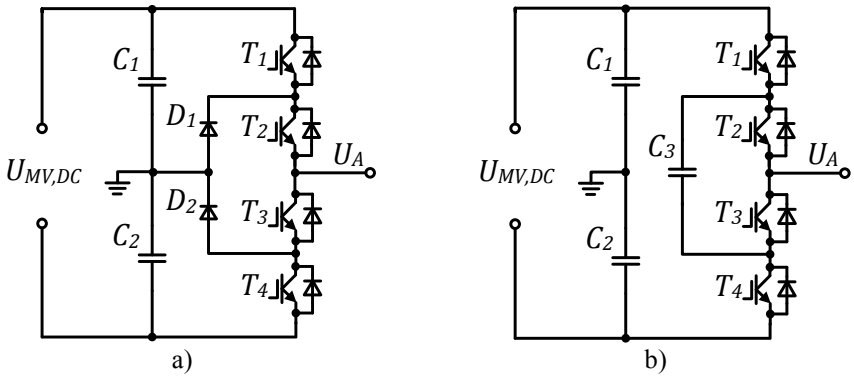


Figure 2.5. Multi-level topologies for the MV side of the isolation stage: a) diode clamped converter; b) capacitor clamped converter.

The multi-level topology combines some serious disadvantages like increased number of components, decreased long-term reliability, increased complexity of control and protection circuits, increased dimensions and weight of the converter [45]. As the reliability is one of the most critical requirements for the PET, the cascaded two-level converter design seems to be a more optimal solution for the PET in comparison with the multi-level converter topologies.

Modular structure based DC/DC converters

The modular structure based DC/DC converters are composed of well-known topologies and available semiconductors. They usually consist of the series connection of the converter cells on the MV side and parallel connection on the LV side as shown in Figure 2.6. The series connection on the MV side allows the voltage to be shared between the switches. Parallel connection on the LV side allows high current to be shared between the switches. As can be seen, each cell handles only part of the total input power. That in turn allows to select the

power switches with lower voltage ratings and thus lower conduction losses and also increase the switching frequency [39], [46]. Lower losses improve the overall efficiency of the converter while increased switching frequency allows the volumes of the MF transformer core to be reduced. Due to higher efficiency, reduced volumes, mass and eventually cost, such type of converters are the optimal for the PET.

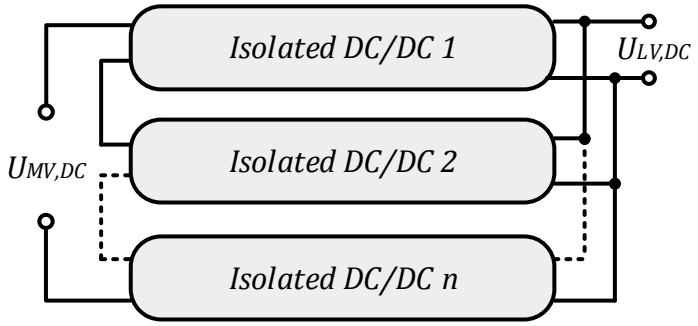


Figure 2.6. Block diagram of the modular series-input-parallel-output design.

Topologies for the Modular Design Based DC/DC Converters

Numerous isolated DC/DC converter topologies have been proposed by different authors [47] - [54], however many of them lack the bi-directional power flow and ZVS capabilities. Among them the phase-shifted dual active half bridge (DHB) and dual active bridge (DAB) meet most of the requirements of the PET concerning the bi-directional power flow and ZVS capabilities, thus making them interesting research objects. Compared to the traditional hard-switched PWM converters, the phase-shift-controlled converters usually have higher circulating current and higher conduction losses. However, as the switching frequency increases, the loss reduction caused by soft-switching overweighs the conduction losses and thus the overall efficiency improves.

A DHB is a widely used converter in the high power applications. For the isolation stage of the PET it was proposed in [39], [55]. The circuit of the DHB shown in Figure 2.7 consists of the two half-bridges (HB) that are connected by means of the HF transformer. Besides small number of the switching devices, simple power stage design and simple control system, a small core loss of the transformer can be achieved. In addition, the DHB results in a more economical implementation than the FB based DC/DC converters. However, the splitting capacitors have to carry all transformer currents and capacitors with higher VA rating are required. Moreover, the total switch conduction losses in the DHB can be twice as high as in the DAB for the same power level due to the higher magnitudes of current (almost double) through the switches [39].

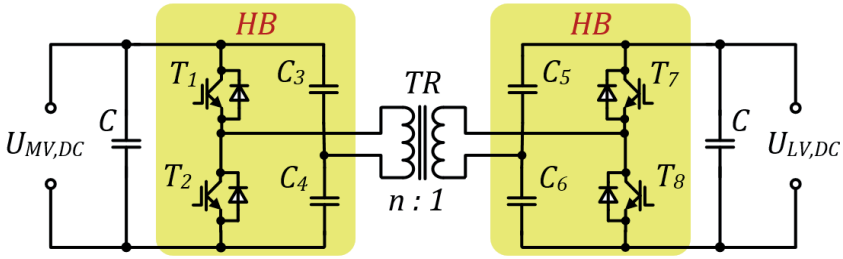


Figure 2.7. Schematic of the dual half bridge circuit.

In [57] the 1.2 MW PET for the traction applications with single phase 15 kV input and 1.5 kV DC output voltages is presented. The isolation stage of the given PET consists of the half bridge LLC isolated resonant circuit topology and a MF transformer as shown in Figure 2.8. By involvement of the magnetizing inductance and the leakage inductance of the MF transformer, the LLC circuit allows the zero voltage turn-on and effective turn-off (with significantly smaller current) of the 6.5kV IGBTs to be achieved.

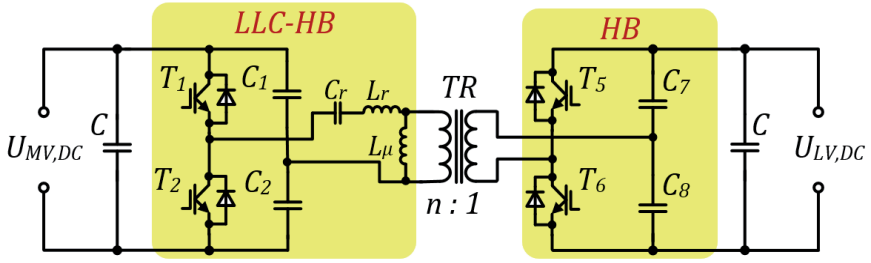


Figure 2.8. Schematic of a half-bridge LLC DC/DC converter topology used in the PET of the traction system.

The most widely proposed topology for the future MV DC-DC converters is the DAB [59] - [64]. A DAB based PET prototypes have already been built for 7.2/0.24 kV and 20 kVA power ratings [65], [66]. Some advantages of the DAB converter are: voltage stress across each switch is limited by the DC bus voltage level, ZVS can be achieved without additional circuitry, simple structure of the transformer, fast dynamic behavior due to lack of passive components, and various possible control algorithms [39]. For these reasons the DAB is selected as a reference topology for the further investigations.

Dual Active Bridge

The circuit of the DAB is shown in the Figure 2.9. It consists of two simultaneously controlled voltage source inverters (VSI) and a HF transformer between them. For proper output power control, the DAB requires a relatively large series inductor L_{TR}, in order to create voltage difference between the voltages on the LV and MV sides of the transformer. As the PET is aimed to be

used in HP and MV applications, the natural stray inductance of the HP transformers is typically sufficient [68].

Research in [68] has analyzed three different modulation methods for the DAB: i) rectangular modulation mode, with duty cycles $D = 0.5$ ii) triangular current mode, iii) trapezoidal current mode. Triangular modulation allows the lowest switching losses to be achieved. Trapezoidal modulation allows higher power to be transferred in comparison with the triangular modulation [68], [69]. With rectangular modulation the highest power transfer can be achieved, thus the rectangular modulation method was selected as a control method of the DAB for the further investigations.

With rectangular modulation method, the magnitude and the direction of power can be controlled by means of the phase shift angle φ between the gate signals of both VSI-s. The value of the phase angle determines the magnitude of the transferred power, whereas the sign of the phase angle determines the power flow direction. In addition, the phase shift technique allows ZVS to be effectively achieved over a wide load range, reducing this way the switching losses. However, using the large phase shift values can result in a high reactive power content that in turn reduces the efficiency of the converter. In [68] the dependency between the phase angle, the active and reactive power is shown. The suggested control range of the phase angle varies between 45°...60° [70]. The gate signals, typical waveforms and operation description of the DAB are presented in [PAPER-VI] and [PAPER-VII].

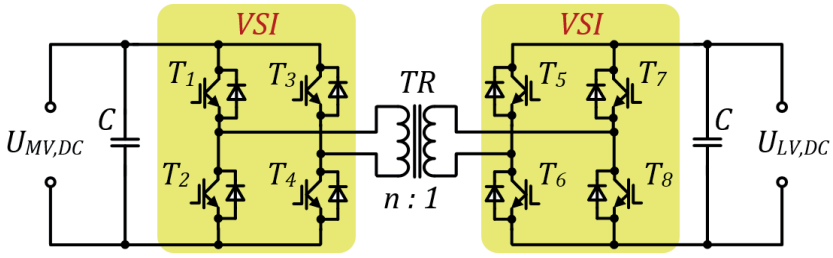


Figure 2.9. Schematic of the DAB.

The power delivered from one port to the other can be determined by knowing the transformer turn's ratio N_{TR}, the voltages on MV and LV side, U_{MV} and U_{LV} respectively, switching frequency f_S and the leakage inductance of the transformer $L_{TR,}$ in the following way:

$$P = \frac{N_{TR} U_{MV} U_{LV} D_\varphi (1 - |D_\varphi|)}{2 f_S L_{TR}}, -1 \le D_\varphi \le 1, \qquad (2.1)$$

where D_φ is the duration of the phase shift t_φ between the gate signals of the corresponding legs of the DAB. The best performance of the DAB is achieved when the voltage on the transformer LV side and the reflected MV side voltages are equal.

$$U_{LV} = N_{TR} \cdot U_{MV}. \tag{2.2}$$

In such case the current stress on the devices is minimal and soft switching can be effectively achieved that results in higher efficiency and reduced component ratings. However, the DAB lacks the voltage boost properties and under realistic conditions the voltages variations on MV and especially on LV cannot be compensated. That in turn results in increased transformer I_{TR} and the capacitor I_{C1}, I_{C2} RMS currents and lower efficiency [60]. These factors have been a serious drawback of the DAB that could be solved by introducing new PEBB-s for the LV side of the DAB.

2.3 Summary

The three-stage topology of the PET is the most advantageous among the single and the two-stage topologies. That is due to the presence of two DC-links with different voltage levels that allow the energy sources and storage devices to be interconnected into one system and power factor correction circuits to be integrated on the MV and LV side. In order for switches to operate on the MV side, the voltage stress on the switches must be reduced by employing the multi-level converter topologies, connecting the switches in series or using the modular design of the converter cells, where total input power is shared between different cells. The DHB and DAB are widely used two port topologies that can be connected into a modular structure to reduce the component ratings. The advantages of the DAB for HP applications overweight the DHB. The phase shift modulation allows to control the power range of the DAB in a wide range in both directions. However, the DAB lacks the voltage regulation capabilities that results in increased component stress values under varying LV side voltage level. These problems can be solved by introducing the new PEBB-s for the isolation stage of the PET.

3 NEW POWER ELECTRONIC BUILDING BLOCKS FOR THE ISOLATION STAGE

Previous chapter reviewed technologies suitable for DC/DC converters for the isolation stage of the three-stage PET. It turned out, that a major drawback of the DAB is lack of voltage compensation capabilities. This chapter focuses on the elimination of this problem. The isolation stage of the PET can be represented by the PEBB-s, as shown in Figure 3.1. The MV side converter consists of the traditional voltage source inverter (VSI) PEBB. Three new PEBB-s for the LV side of the isolation stage are proposed in this section.

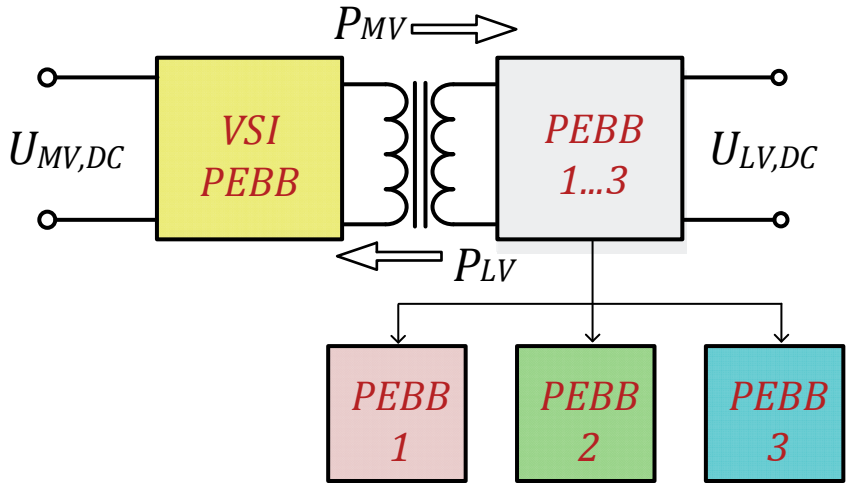


Figure 3.1. Representation of the isolation stage by using the PEBB-s.

The most important requirements for the isolation stage are the bi-directional power flow control and galvanic isolation by means of the MF transformer. The new PEBB-s should have improved shoot-through immunity, reduced current and voltage stress on the components and fairly good efficiency in comparison with the conventional VSI. Following new PEBB-s are proposed for the LV side of the isolation stage:

- CDR PEBB: current doubler rectifier (CDR) with bi-directional power flow capability;
- qZSI PEBB: quasi-Z-source inverter (qZSI);
- CF-DC/DC PEBB: current-fed DC/DC converter with an active clamp.

The isolation stage with the proposed PEBB-s allows the power to be transferred in two directions, in the forward and in the reverse operating mode. In the forward operating mode, the energy is transferred from the MV port

towards the LV port. In the reverse operating mode, the energy is transferred from the LV port towards the MV port.

3.1 Improved Modulation Method

In order to perform comprehensive comparison between the DAB and the proposed PEBB-s the modulation method must provide simultaneous control of the switches on both sides of the transformer. The conventional rectangular modulation can be used in the forward operating mode, however in the reverse operating mode, if voltage regulation is necessary, the improved modulation method (IMM) is used to control the voltage and power level simultaneously [60]. The typical waveforms of the IMM are shown in Figure 3.2*a*, and the equivalent circuit in Figure 3.2*b*.

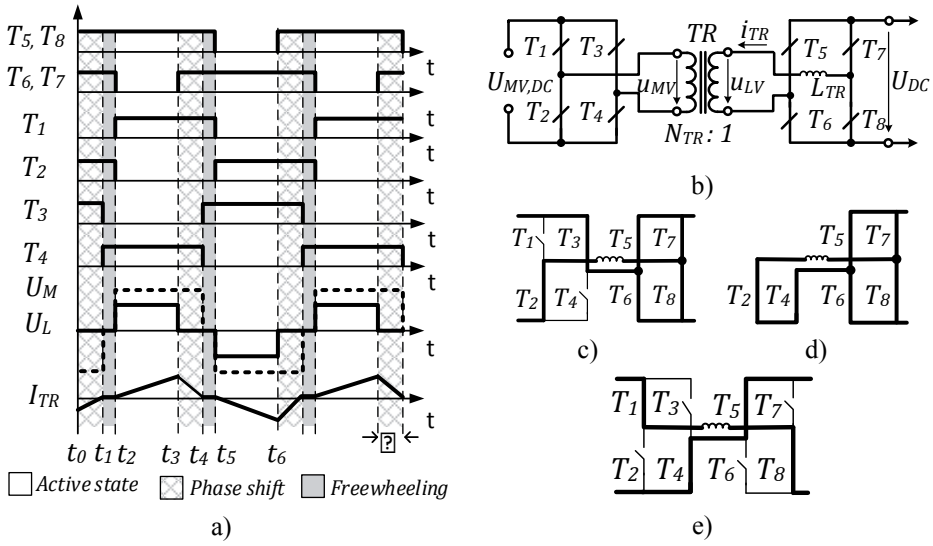


Figure 3.2. Improved modulation method. a) typical waveforms; b) schematic of the circuit; c) phase shift state; d) freewheeling state; e) active state.

The IMM consists of three switching states: active state, phase shift state and the freewheeling state. During the time interval $t_0 \ldots t_1$ the current in the MF transformer is reversed and adjusted to the new level. The equivalent circuit of this switching state is shown in Figure 3.2*c*. The rising slope of the transformer current I_{TR} can be expressed as follows:

$$\Delta i_{TR} = i_{TR,0} + \frac{u_{MV} N_{TR}}{L_{TR}} \cdot \Delta t, t_0 \le t \le t_1, \tag{3.1}$$

where $i_{TR,0}$ is the initial transformer current value at time instance t_0 and L_{TR} designates the leakage inductance of the MF transformer. During the freewheeling time interval $t_1 \ldots t_2$ current slope of the i_{TR} remains constant. The equivalent circuit of the freewheeling state is shown in Figure 3.2*d.* During the

active state $t_2 \ldots t_3$ the energy is transferred from the LV port towards the MV port of the MF transformer. The equivalent circuit of the active state is shown in Figure 3.2*e* and the slope of the current can be determined as follows:

$$\Delta i_{TR} = \frac{U_{LV} - U_{MV} N_{TR}}{L_{TR}} \cdot \Delta t, t_2 \le t \le t_3 . \tag{3.2}$$

The next half switching cycle is symmetrical to the first one. According to a detailed analysis, presented in [PAPER-VII], knowing the switching frequency f_S, the voltages on the MV and the LV ports and considering the leakage inductance of the transformer L_{TR}, the transferred power from the LV port to the MV port can be expressed in the following way:

$$P = U_{LV} \cdot \frac{(2N_{TR}U_{MV} - U_{LV})D_\varphi(1 - D_S)}{4 f_S L_{TR}}, 0 \le D_\varphi \le D_S , \tag{3.3}$$

where D_φ is the relative duration of the phase-shift and D_S designates the relative duration of the shoot-through state. As can be seen, the transferred power is a function of D_S and D_φ, that extends the voltage and power regulation possibilities comparison with conventional rectangular modulation of the DAB. However, the IMM has limited phase angle control range that should be limited to D_S. Increasing D_φ over D_S results in increased component stress and reduced voltage step-up capability.

The following chapters present the proposed PEBB-s, describe their operating principle, their advantages and disadvantages, and recommendations for design.

3.2 Current Doubler Rectifier with Bi-directional Power Flow Capability PEBB

The proposed current doubler rectifier (CDR) PEBB is introduced in [PAPER-III]. The paper describes the operating principle of the converter and presents its typical waveforms. In addition, the paper provides a steady state analysis with the boost factor estimation and the simulation results. The experimental results for the CDR PEBB are presented in [PAPER-V].

A combination of a CDR PEBB and a VSI PEBB results in a topology called CDR-based DAB. A schematic of such combination is shown in Figure 3.3. It consists of the conventional CDR circuit, where the diodes are replaced with controllable switches T_6 and T_8, and inductors are replaced with the transformers TR_{aux1} and TR_{aux2}. An auxiliary circuit is attached to the CDR in order to provide freewheeling path for the energy stored in the auxiliary transformers TR_{aux1} and TR_{aux2}, and mitigate the occurrence of the overvoltage peaks on the switches when operating with the duty cycle $D_A \le 0.5$.

The operating principle of the converter in the forward and the reverse operating modes is described in [PAPER-IV]. When the converter operates in the forward operating mode, the MV side VSI PEBB generates rectangular voltage over the MV side winding of the transformer and the current flows

through the antiparallel diodes of T_6 and T_8 on the LV side. In the reverse operating mode the switches T_6 and T_8 on the LV side are controlled alternately to provide the necessary voltage step-up and power flow to the MV port. In the normal operating mode the switches T_6 and T_8 are controlled with the duty cycle $D > 0.5$ and the boost factor b equals to:

$$b = \frac{u_{MV}}{u_{LV}} = \frac{1}{1 - D_A} \cdot N_{TR}\,, \tag{3.4}$$

where D_A is the duty cycle of the gate signals for T_6 and T_8, and N_{TR} is the turn's ratio of the MF transformer. The switches on the MV side VSI are controlled according to IMM. If the duty cycle of the switches T_6 and T_8 becomes $D_A \leq 0.5$ the path of the transformer's leakage energy gets interrupted. That results in dangerous overvoltage spikes over the switches. Therefore, this energy is redirected back to the LV port by means of the freewheeling path, provided by the auxiliary circuit. A boost factor in that operating mode can be determined as follows:

$$b = \frac{u_{MV}}{u_{LV}} = \frac{N_{TR}}{N_{aux}}\left(2N_{aux} - \frac{1 - 2D_A}{D_A}\right), \tag{3.5}$$

where N_{aux} is the turn's ratio of the auxiliary transformers TR_{aux1} and TR_{aux2}.

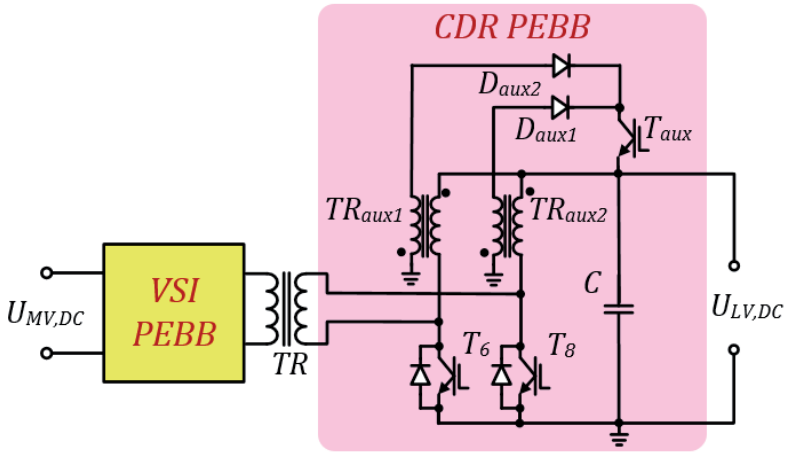


Figure 3.3. Schematic of the CDR PEBB.

The advantages of the CDR PEBB are: i) reduced current ripple, ii) voltage step-up in the reverse operating mode, iii) ZV turn-on can be achieved, iv) improved hoot-through immunity on the LV side, v) simple gate driver design, vi) reduced number of active switches. The major drawbacks of CDR PEBB are: i) increased mass and volumes due to the presence of three transformers, ii) increased voltage stress on the LV side switches, iii) different boost factors in the forward and in the reverse operating modes.

Design considerations for the $D_A > 0.5$

Next, some design guidelines for the CDR PEBB in the reverse operating mode are presented. First of all, the necessary inductance of the auxiliary transformer's should be obtained since it determines the slope and the peak value of the current. Due to the current sharing effect of the CDR PEBB each auxiliary transformer carries half of the input current, thus the average current can be obtained as follows:

$$I_{aux,AV} = \frac{P_{LV}}{2 \cdot U_{LV}}. \tag{3.6}$$

Inductance of the auxiliary transformer depends on the allowed current ripple ΔI_L value. The current through the auxiliary transformer reaches its maximal value at the end of the duty cycle D_A. Thus, considering the maximum duty cycle $D_{A,MAX}$ and the switching frequency f_S, the inductance can be determined according to 3.7

$$L_{aux} = \frac{2 \cdot U_{LV}^2 \cdot D_{A,MAX}}{P_{LV} \cdot f_S \cdot k_I}, \tag{3.7}$$

where k_I represents the ratio of the current ripple and the average current $\Delta I/I_{aux,AV}$. When designing the converter for the bi-directional operating mode, it should be kept in mind that in the forward mode, too low inductance of the auxiliary transformer can bring the converter into the discontinuous conduction mode.

Next, the selection of the filter capacitance is considered. If the CDR-DAB operates in the boost mode, the current ripple is typically very low, thus the LV side capacitor should be dimensioned first of all according to the requirements set in the forward operating mode. If the converter operates in the forward operating mode, the capacitor selection is based on the allowed current on voltage ripples on the LV side and can be selected according to 3.8 as follows:

$$C = \frac{\Delta I}{\Delta U \cdot 2 \cdot f_S}, \tag{3.8}$$

where ΔI is the current ripple, ΔU is the voltage ripple and f_S is the switching frequency. It is advisable to use not more than 1 % voltage ripple during the design. In order to achieve more efficient current ripple cancellation, a capacitor with as small ESR as possible is advisable to be employed.

Transformer turn's ratio

Next, the selection of transformer turns ratio is considered. Different parameters are needed to be considered when designing the MF transformer for the CDR circuit. These are the maximal flux density B_{MAX} (derived from the saturation flux), core area A_e, switching frequency and converter features. The number of turns on the LV side can be obtained according to 3.9

$$N_{LV} = \frac{U_{LV}}{(1-D_A)\cdot B_{MAX}\cdot A_e \cdot f_S}. \quad (3.9)$$

The number of turns on the MV side of the transformer can be obtained according to 3.10 as follows:

$$N_{MV} = \frac{U_{MV}\cdot(1-D_A)\cdot N_{LV}}{U_{LV}}. \quad (3.10)$$

It should be noted, that if the current doubler is phase-shift controlled the effect of the leakage inductance should be carefully considered, as it is needed for the power transfer. If necessary, the number of turns can be made higher than the ones obtained by 3.9 and 3.10, in order to achieve necessary value of the leakage inductance.

Power switches

In order to dimension the power switches, the voltage and current stress values should be determined. Neglecting the voltage spikes that occur during the switching transients, the steady-state voltage stress on the switches T_6 and T_8 can be estimated according to 3.11 in the following way:

$$U_{T6,MAX} = \frac{U_{LV}}{1-D_{A,MAX}}. \quad (3.11)$$

As can be seen, at high D_A values the steady state voltage stress on the switches can be enormous, e.g. for $D_A = 0.8$ a voltage stress 500 % of U_{LV} is applied on the switches. The experimental investigations have determined that high overvoltage peaks occur over the switches during the turn-off, thus the rating of the switches must be even higher. The peak current through the switch T_6 occurs when I_{L8} reaches its maximum level, at the end of the duty cycle $D_{A,\mathrm{MAX}}$. Average current through the switch is half the input current

$$I_{T6,AV} = \frac{1}{2}\cdot I_{LV}. \quad (3.12)$$

The peak current through the switch can be obtained according to 3.13

$$I_{T6,MAX} = \frac{U_{LV}}{L_{aux}\cdot f_S}\cdot\left(\frac{1+D_{A,MAX}}{2}\right). \quad (3.13)$$

When designing the bi-directional CDR, the voltage and current stress values should be considered for both power flow directions. On the LV side the switches with high current rating are feasible. The IGBT-s have lower conduction losses at high current values in comparison with MOSFETs. However, a disadvantage of the IGBT-s is high turn-off losses. Moreover, with the rise of the switching frequency the switching losses of the IGBT-s significantly overweigh the losses in MOSFET-s.

Snubber

The experimental results revealed the problems regarding high overvoltage peaks over the switches in the reverse operating mode of the CDR PEBB. Such feature drastically increases the voltage stress on the switches, increases the turn-off losses and significantly limits the use of this topology in HP applications. However, the overvoltage peaks can be clamped by adding a special diode-capacitor-resistor (RCD) snubber into the circuit, as is shown in section V of [PAPER-IV]. The aim of such snubber is to discharge the energy stored in the leakage inductance of the MF transformer during the turn-off. The design guidelines for calculating the RCD snubber are presented in [77] - [79] and can be used for the RCD snubber design for the CDR PEBB.

Auxiliary circuit

The aim of the auxiliary circuit is to provide a freewheeling path for the energy that is stored in the auxiliary transformers and direct it back to the LV port of the converter. This is needed to prevent the overvoltage peaks on the switches if the duty cycle is $D_A \leq 0.5$. The auxiliary circuit consists of the auxiliary transformers TR_{aux1} and TR_{aux2}, diodes D_{aux1} and D_{aux2}, and one switch T_{aux}. In order to select the turn's ratio of the auxiliary transformers N_{aux}, it should be remembered that it has direct impact on the boost factor of the converter, on the average current and blocking voltage of the auxiliary diodes D_{aux1}, D_{aux2}. The maximum blocking voltage of the auxiliary diodes can be obtained as follows

$$U_{D,REV,MAX} = U_{LV} \cdot \left(1 + N_{aux}\right), \tag{3.14}$$

where N_{aux} designates the turn's ratio of the secondary side and the primary side of the auxiliary transformers. As can be seen, increased turn's ratio of the auxiliary transformer, increases the needed blocking voltage of the diodes. Hence, the turn's ratio of the auxiliary transformers should be taken into account when selecting the appropriate diodes. The average current through the auxiliary diode can be approximately estimated in the following way:

$$I_{D,AV} = I_{LV} \cdot N_{aux}(1 - 2D_A). \tag{3.15}$$

The maximum steady-state voltage on the switch T_6 and T_8 can be evaluated as follows:

$$U_{T6,MAX} = U_{LV} \cdot \frac{\left(1 + N_{aux}\right)}{N_{aux}}. \tag{3.16}$$

As can be seen from 3.14 and 3.16, increasing the N_{aux} decreases the voltage stress on the transistors but on the other hand it increases the voltage stress on the auxiliary diodes. Thus, in order to achieve equal voltage stress on the switches and diodes N_{aux} should be chosen as 1:1 as shown in 3.17

$$U_{D,REV,MAX} = U_{T6,MAX} \rightarrow N_{aux} = 1. \tag{3.17}$$

In order to keep the voltage stress on the switches equal in the both operating modes, with enabled auxiliary circuit and disabled auxiliary circuit, 3.11 and 3.16 should be equal, thus limiting the N_{aux} minimum value to

$$N_{aux,MIN} = \frac{1 - D_A}{D_A}, \tag{3.18}$$

where D_A represents the duty cycle for the operation mode with $D_A \leq 0.5$. The turn's ratio of the auxiliary transformer also determines the boost factor of the CDR if the duty cycle of the control signals is $D_A \leq 0.5$ in the continuous conduction mode. From the steady-state analysis presented in [PAPER-III], the N_{aux} selection can be made according to the required boost factor. The N_{aux} can be selected according to the required voltage boost b in the following way:

$$N_{aux} = \frac{N_{TR} \cdot (2D_A - 1)}{D_A \cdot (b - 2 \cdot N_{TR})}. \tag{3.19}$$

It can be seen that there are several criteria for selecting the turn's ratio of the auxiliary transformers that must be considered during the design.

The last component of the auxiliary circuit is the auxiliary switch T_{aux}. It is needed to detach the auxiliary circuit from the CDR in case the duty cycle $D_A \leq 0.5$, otherwise the system loses its stability due to positive feedback. The switch carries the current that is double times the current through the auxiliary diodes, thus

$$I_{Taux} = 2 \cdot I_{D,AV}. \tag{3.20}$$

The maximal voltage stress on the switch, however, is applied during the operation mode with $D_A > 0.5$, when the auxiliary circuit is disabled. The voltage stress on the switch can be calculated as follows:

$$U_{Taux,MAX} = U_{LV} \cdot \left[N_{aux} \left(\frac{2D_{A,MAX} - 1}{1 - D_{A,MAX}} \right) \right]. \tag{3.21}$$

Although the auxiliary circuit is disabled in the operating mode with $D_A > 0.5$, the voltage stress on the auxiliary switch depends on the turns ratio of the auxiliary transformer.

3.3 Quasi-Z Source Inverter PEBB

The proposed combination of a qZSI PEBB and a VSI PEBB results in a new topology called qZS-based DAB which has been presented in [PAPER-VI]. The paper describes the operating principle of the qZS-DAB and presents its typical waveforms. In addition, paper provides a steady state analysis with boost factor estimation and power flow control and experimental results.

A schematic of the qZS-DAB is shown in Figure 3.4. It consists of two inductors L_1 and L_2, two capacitors C_1 and C_2, a diode D_1, and a switch S_1. The aim of the qZS network is to step-up the voltage on the LV DC-link to match

the criterion 2.2. The step-up of the LV in the reverse operating mode is achieved by simultaneous turn-on (also called shoot-through) of the inverter switches $T_5 \ldots T_8$ of the qZSI PEBB. During the shoot-through state the energy is stored in the inductances of the qZS network while the diode D_1 prevents the short circuit of the capacitors C_1 and C_2. To allow the energy flow in both directions, the diode D_1 is shunted with the switch S_1 in the forward operating mode. In this case, the energy is transferred from the MV side VSI by means of the rectangular modulation of the DAB while qZS network acts as a filter.

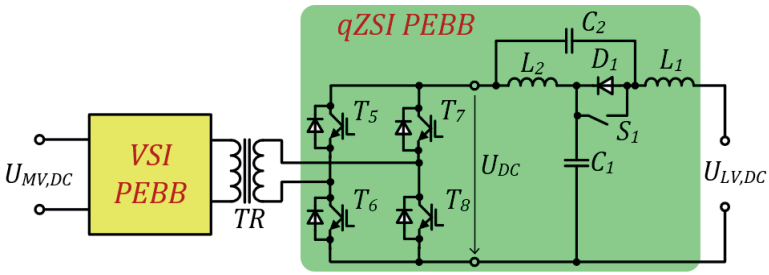


Figure 3.4. Schematic of the qZSI PEBB.

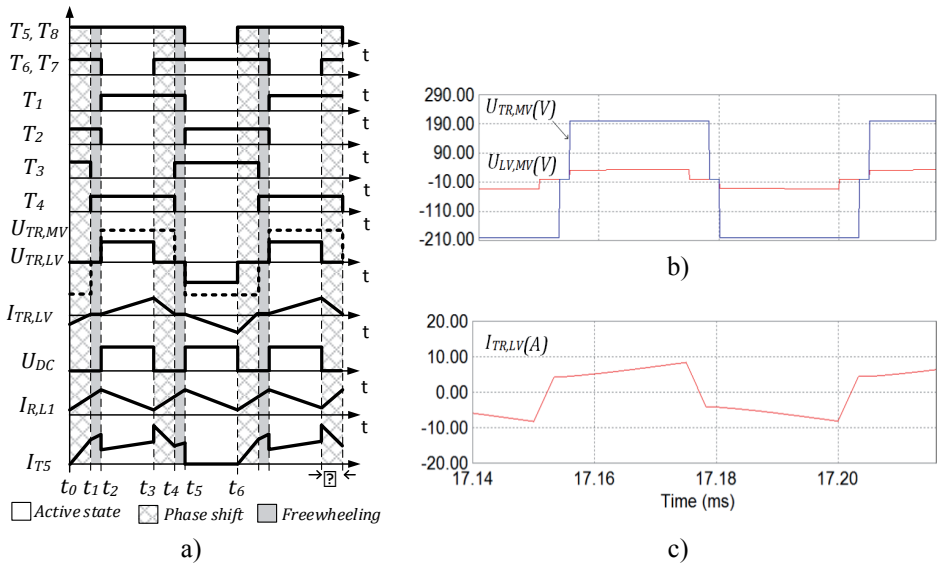


Figure 3.5. Operating principle of the qZS-based DAB: a) typical waveforms; b) simulated transformer voltages; c) simulated transformer current.

The control signals and typical waveforms of the qZS-based DAB in the reverse operating mode are shown in Figure 3.5. It can be seen that during the shoot-through state the current through the switch T_5 rises rapidly during $t_0 \ldots t_1$, and continues to rise with the same slope as the inductor L_1 and L_2 current during

$t_1...t_2$. The voltage on the DC-link of the qZSI PEBB can be obtained in the following way:

$$U_{DC} = U_{LV,DC} \cdot \frac{1}{1-2D_S}, \tag{3.22}$$

where D_S designates the relative duration of the shoot-through state. In order to match the criterion 2.2, the qZSI PEBB must achieve a corresponding voltage level on the LV side DC-link, as shown in 3.23

$$U_{MV,DC} = U_{DC} \cdot N_{TR}. \tag{3.23}$$

The qZS-based DAB can be controlled by using the rectangular modulation technique in both operating modes. In addition, in the reverse operating mode the phase angle control can be used simultaneously with voltage step-up by means of the IMM. The advantages of the qZS-based DAB over the conventional DAB are: i) improved shoot-through immunity, ii) reduced current stress on the switches and capacitors, iii) continuous input current, iv) no need for additional filters on the LV side, v) voltage step-up on the LV side. The major drawbacks of this topology are: i) increased number of passive elements, ii) increased risk of oscillations, iii) poor operation under small-loads and relatively low switching frequency [71], iv) limited ZVS range due to unsymmetrical structure.

Design considerations

When designing the qZS-based DAB for the bi-directional mode, the component values should be dimensioned according to the maximum current and voltage stresses. Some design guidelines of the qZSI are presented in [45]. The maximal stress values on inductances L_1, L_2, capacitors C_1, C_2 and diode D_1 apply in the reverse operating mode. The inductances of the qZSI PEBB limit the current ripple in the switch during the shoot-through. The current reaches its peak value at the end of the shoot-through state. From the steady-state analysis the needed inductance of L_1 and L_2 can be estimated as follows:

$$L = \frac{U_{LV}^2}{P_{LV,MAX} \cdot f_S \cdot k_I} \cdot \frac{D_{S,MAX}\left(1-D_{S,MAX}\right)}{1-2 \cdot D_{S,MAX}}, \tag{3.24}$$

where $P_{LV,MAX}$ is the power at the maximum phase angle and the shoot-through duty cycle $D_{S,MAX}$ value, k_I designates the ratio of the current ripple and the average current $\Delta I_L/I_{L,AV.}$

Next, in order to limit the voltage ripple, the capacitors should be dimensioned accurately. The voltage ripple depends on the maximal shoot-through duration $D_{S,MAX}$. During the shoot-through state the capacitors C_1 and C_2 are connected in series and thus the capacitance of each capacitor, assuming that capacitors are equal, can be obtained in the following way:

$$C = \frac{2 \cdot P_{LV,MAX}}{U_{LV}^2 \cdot f_S \cdot k_U} \cdot D_{S,MAX}\left(1-2 \cdot D_{S,MAX}\right), \tag{3.25}$$

where k_U is the ratio of the voltage ripple and average voltage on the DC-link $k_U = \Delta U/U_{DC}$.

Other elements of the qZSI PEBB are the diode D_1 and the switch S_1. The maximal reverse voltage stress on the diode D_1 and the switch S_1 (open state) applies during the shoot-through state of the inverter switches $T_5 \ldots T_8$, and can be estimated in a similar way as 3.23:

$$U_{D1,REV,MAX} = U_{S1,MAX} = U_{LV} \cdot \frac{1}{1 - 2 \cdot D_{S,MAX}} . \tag{3.26}$$

The average current through the diode can be estimated as follows:

$$I_{D1,AV} = \frac{P_{LV,MAX}}{U_{LV}} . \tag{3.27}$$

The current rating of the switch S_1 should be selected according to the full current rating in the forward operating mode when it is in the conducting state. The steady-state voltage stress on the controllable switches $T_5 \ldots T_8$ applies during the non-conducting state of the switches and is equal to the voltage value on the DC-link

$$U_{Tx} = U_{DC} . \tag{3.28}$$

The average current through the switches in the reverse operating mode at the maximal power level $P_{LV,MAX}$ can be found according to 3.29 in a following way:

$$I_{Tx} = \frac{P_{LV,MAX}}{2 \cdot U_{LV}} . \tag{3.29}$$

In order to reduce the size and the mass of the inductors, they can be wound on the common core forming this way the coupled inductors, as was done in [72].

3.4 Current-Fed DC/DC Converter with an Active Clamp PEBB

The proposed combination of a CF-DC/DC PEBB and a VSI PEBB results in the new topology, the CF-DC/DC based DAB with an active clamp, which is described in [PAPER-VII]. The paper describes the operating principle of the converter and presents its typical waveforms. In addition, paper provides a steady state analysis with boost factor estimation, power flow control and simulation results. The loss analysis and the experimental results are presented in [PAPER-VIII].

A schematic of such combination is shown in Figure 3.6. The CF-DC/DC PEBB consists of an inductor L_1, a capacitor C_1, a controllable switch T_C with an anti-parallel diode and an inverter. In the forward operating mode, the power is transferred from the MV port to the LV port by means of the rectangular modulation of the DAB while CF-DC/DC PEBB acts as a filter. In the reverse operating mode the voltage step-up on the LV side can be used, to match the criterion 2.2. The voltage step-up takes place by means of the simultaneous shoot-through state of the switches on the LV side inverter. During the shoot-

through the energy is stored in the inductor L_1 and redirected to the MV port during the active state. The switch T_C is turned off during the shoot-through state in order to prevent the short circuit of the capacitor C_1.

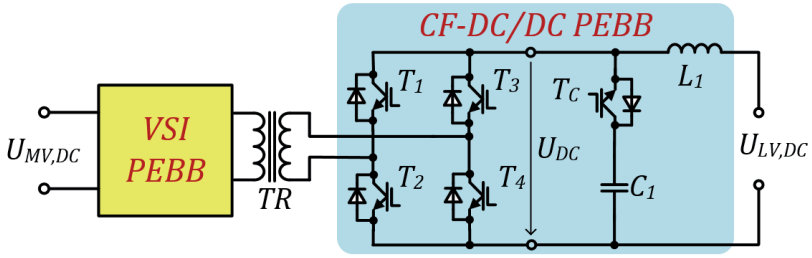


Figure 3.6. Schematic of the CF-DC/DC PEBB.

The boost factor the CF-DC/DC PEBB can be determined by the following equation:

$$U_{DC} = U_{LV,DC} \cdot \frac{1}{1 - D_S}. \tag{3.30}$$

It has the following advantages over the DAB: i) voltage step-up capability, ii) no need for additional filter on the LV side, iii) reduced current and voltage stress on the components. The major drawbacks of this topology are: i) limited ZVS range due to unsymmetrical structure, ii) increased switching and conduction losses due to additional switch T_C.

Design considerations

Detailed design guidelines for the CF-DC/DC PEBB converter are presented in [PAPER-VII] and [73].

3.5 Voltage Regulation Range

Keeping the voltage on the LV side at the constant level is a task that the isolation stage has to fulfill. If the PET operates in the reverse mode, then too low voltage level on the LV side reduces the power transfer performance and increases the voltage and current stress on the components. Compared to the VSI PEBB, the proposed PEBB-s have the voltage step-up properties. Such feature enables to keep the voltage on a stable level and reduce the stress values on the components. The mathematically derived voltage boost factors of the proposed PEBB-s are depicted in Figure 3.7. Here, the PEBB-s are controlled with the active duty cycle is $D_A = 0.6$, shoot-through is $D_S = 0.1$ and the phase shift value is $D_\varphi = 0.1$. The transformer turn's ratio is $N_{TR} = 1$. The VSI PEBB is controlled with the rectangular modulation method and voltages on MV and LV ports are equal. However, the CDR PEBB can regulate the voltage level in a very wide range and reaches $U_{MV} = 300$ V at $U_{LV} = 130$ V. The qZSI PEBB

reaches U_{MV} = 300 V at U_{LV} = 250 V voltage level on the LV side. The LC-filter based DAB reaches U_{MV} = 300 V voltage on the MV side at U_{LV} = 280 V.

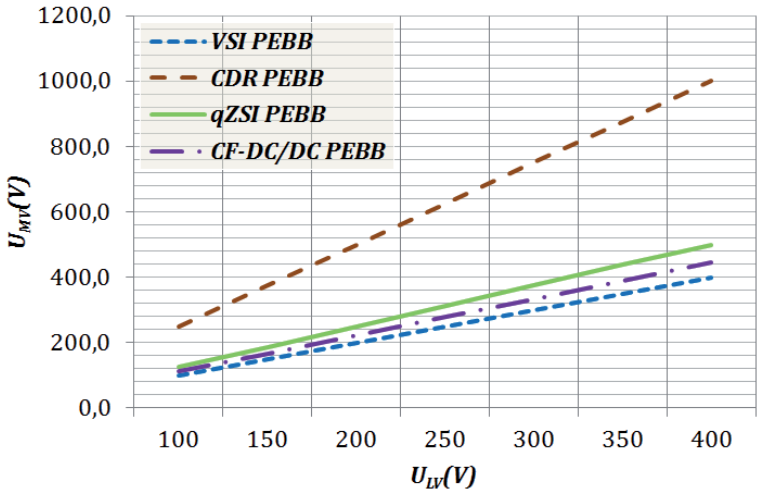


Figure 3.7. Voltage regulation range of the VSI PEBB and proposed PEBB-s.

3.6 Laboratory Test Bench

In order to experimentally analyze the proposed PEBB-s, a flexible prototype was developed. The prototype allows all four topologies to be tested under similar conditions and at the same power level. The test bench consists of the IGBT based VSI on the MV port, the MF transformer and the proposed PEBB-s on the LV port.

Although the final application, the PET, is a high-power device, the prototype was built for the lower voltage and power levels. The IGBT-s *IRG7Ph42ud1pbf* were chosen for the LV port VSI and *IRG4PH50UDPbf* for the MV port VSI. A low voltage side voltage of U_{LV} = 30 V and high voltage side U_{MV} = 200 V are used during the experimental investigation. A *DSPIC33FJ64GS606* microcontroller is used to generate the gating signals for the IGBT driver circuits. The *IR2181* type IGBT drivers are used to control the switches on the MV side VSI PEBB and *MC33153* IGBT drivers were used to control the switches on the LV side VSI PEBB. The main parameters of the test bench and its components are summarized in Table 3.1 and the block diagram of the experimental prototype is shown in Figure 3.8.

Table 3.1. Parameters of the laboratory test bench.

Parameter	Value
Low side voltage U_{LV}	30 V (DC)
Medium side voltage U_{MV}	200 V (DC)
Saturation voltage of IGBT-s (LV) U_{CE}	1.7 V
Saturation voltage of IGBT-s (MV) U_{CE}	2.7 V
Voltage drop of the diodes U_D	1.1 V
Blocking voltage of the IGBT-s	1200 V
Nominal collector current I_C	30 A
Switching frequency f_S	30 kHz

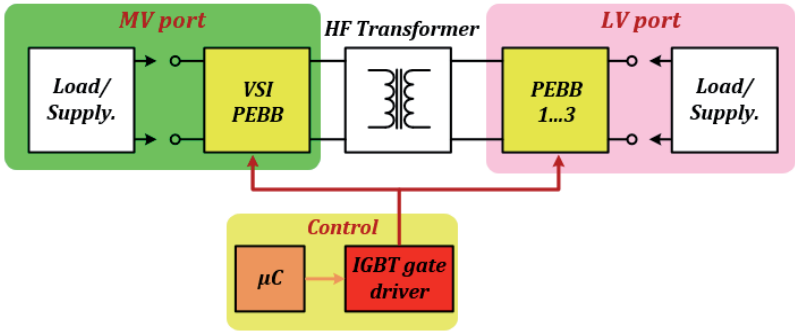


Figure 3.8. Block diagram of the experimental test bench.

3.7 Summary

In order to overcome the challenges of the DAB and extend the control range of the isolation stage, three new PEBB-s were proposed: CDR PEBB, qZSI PEBB and CF-DC/DC PEBB. The combination of the proposed PEBB-s and a VSI PEBB resulted in the new topologies. The comparison of the VSI PEBB and the proposed PEBB-s are presented in Table 3.2. The CDR PEBB has a low number of switches, improved shoot-through immunity, very good voltage step-up properties and equal current sharing. However, the presence of three transformers increases the weight of the converter and causes significant overvoltage peaks (up to 225 %) during the turn-off of the switches that limits the use of this topology without additional snubber circuits. The qZSI PEBB has also improved shoot-through immunity and good voltage step-up properties, with reduced current stress on the capacitors and voltage stress on the switches. However increased number of passive elements increases the size of the converter and the conduction losses. CF-DC/DC PEBB has reduced number of passive elements in comparison with qZSI PEBB, however it has increased switching and conduction losses due to the additional switch and more complex control. The analytically obtained operating principle and waveforms were verified with simulations and tested on the experimental prototype. The experimental results showed the correspondence to the analytically obtained

waveforms. In addition, it was verified that proposed PEBB-s do not cause any instabilities in the forward and in the reverse operating modes. The design guidelines for the proposed PEBB-s were provided. During the design, the components should be selected according to the bi-directional mode of the converters.

Table 3.2. Comparison of the PEBB-s for the isolation stage.

	VSI PEBB	**CDR PEBB**	**qZSI PEBB**	**CF-DC/DC PEBB**
No. of switches	4	3	5	5
No. of diodes	4	4	5	5
No. of passive elements	-	3	4	2
ZV turn-on	Yes	Yes	Yes	Yes
Need for snubber circuit	No	Yes	No	No
Boost factor $b = \frac{U_{MV}}{U_{LV}}$	-	$\frac{1}{1-D_A} \cdot N_{TR}$	$\frac{1}{1-2D_S} \cdot N_{TR}$	$\frac{1}{1-D_S} \cdot N_{TR}$
Voltage regulation range	U_{LV}	$400\% \cdot U_{LV}$ *	$200\% \cdot U_{LV}$ **	$130\% \cdot U_{LV}$ **
On-state switch voltage stress	U_{LV}	$\frac{U_{LV}}{1-D_A}$	$\frac{U_{LV}}{1-2D_S}$	$\frac{U_{LV}}{1-D_S}$
Control complexity	Simple	Medium	Simple	Medium
Short-circuit immunity	No	Yes	Yes	No

* $D_A = 60$ %.

** $D_S = 10$ %.

4 COMPARISON AND ANALYSIS

The aim of this chapter is to compare of the proposed PEBB-s regarding the conduction losses, the switching losses, the component stress values and the efficiency. The results are based on the experimental investigation of all PEBB-s with the parameters shown in Table 3.1. As the aim of the isolation stage is to keep the voltage on the stable level, the operating point was selected such, that 30 V was achieved on the DC-link. Therefore, according to Figure 3.7, the lower voltage was fed to the LV side of the proposed PEBB-s and desired voltage was achieved by the voltage step-up. The proposed PEBB-s were analyzed on the same power level of $P = 500$ W. The active duty cycle was $D_A = 0.6$, (thus shoot-through duration is $D_S = 0.1$) and the phase shift relative duration was $D_\varphi = 0.1$.

4.1 Conduction and Switching Losses

Conduction Losses

The total conduction losses of the converter comprise the conduction losses in the power switches and on the active resistances R of the passive elements and wires. In this section the conduction losses in the power switches, inductors and the transformer are considered, and the conduction losses in the capacitors are neglected. The conduction losses of the IGBT-s P_{IGBT} depend linearly on the collector-to-emitter voltage drop u_{CE} and the current i_c flowing through it. This can be evaluated as follows:

$$P_{IGBT} = \frac{1}{T_s}\int_0^{T_s} u_{CE}(t)\cdot i_C(t)\cdot dt = U_{CE}\cdot I_{C,AV} + r_C \cdot I_{C,RMS}^2, \qquad (4.1)$$

where T_s is the duration of the switching period, $I_{C,AV}$ is the average current that flows through the switch, r_C is the on-state resistance of the switch and $I_{C,\mathrm{RMS}}$ is the RMS value of the current. The conduction losses of the IGBT body diodes can be evaluated in a similar way by multiplying the forward voltage drop u_D of the diode with the forward current i_D

$$P_D = \frac{1}{T_s}\int_0^{T_s} u_D(t)\cdot i_D(t)\cdot dt = U_D\cdot I_{D,AV} + r_D \cdot I_{D,RMS}^2, \qquad (4.2)$$

where U_D is the voltage drop over the diode and $I_{D,AV}$ is the average current of the diode, r_D is the on-state resistance and $I_{D,RMS}$ is the RMS value of the diode current.

Switching losses

The switching losses are caused by non-ideal characteristics of the power switches, when the transition from on-state to off-state or vice versa takes place. Obtaining the switching losses is a more challenging task than that of the

conduction losses, as the switching losses depend on the switch characteristics and on the surrounding parasitic components. The switching losses of the power switches are equal to the sum of turn-on and turn-off losses and can be calculated according to the following equation:

$$P_{SW} = \frac{1}{T_{sw}}\left[\int_{t_1}^{t_2} u_C(t)\cdot i_c(t)\cdot dt + \int_{t_3}^{t_4} u_C(t)\cdot i_c(t)\cdot dt\right] = \frac{1}{2}U_C I_C f_S (t_{on} + t_{off}), \quad (4.3)$$

where U_C is the supply voltage, I_C is the average collector current, f_s is the switching frequency, t_{on} is the turn-on duration, and t_{off} is the turn-off duration. As can be seen, the switching losses are proportional to the switching frequency. During the following analysis the switching frequency was kept on the same level for all topologies. The ZV turn-on of the switches allows the switching losses to be reduced. In order to comprehensively determine the switching losses, considering the circuit parasitic capacitances and the ZV turn-on, the switching losses were obtained experimentally by measuring the current and the voltage waveforms during the switching transient and applying Eq. (4.3).

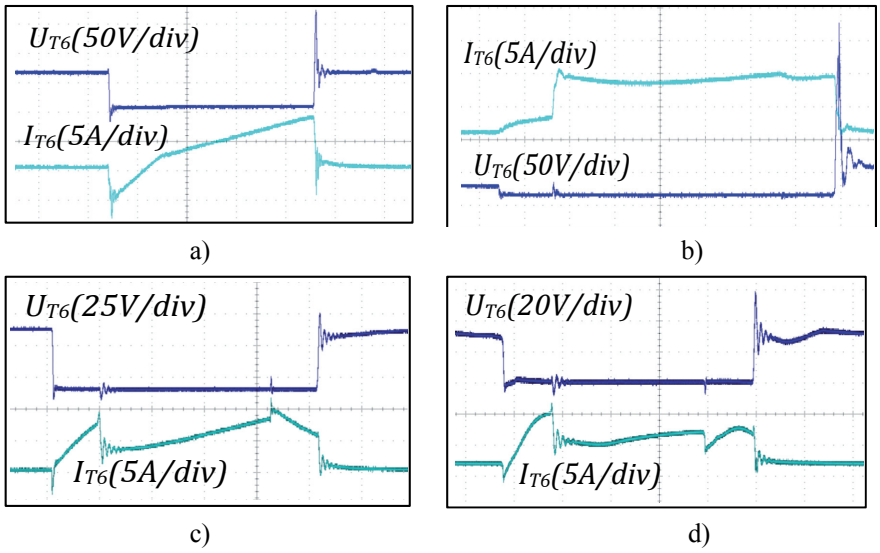


Figure 4.1. Switching sequence of the LV side switch T_6 on the same power level: a) DAB; b) CDR-DAB; c) qZS-DAB; d) CF-DC/DC-DAB.

The switching sequences of the switch T_6 for each PEBB in the boost operating mode (excluding DAB) are shown in Figure 4.1. The experimental results showed that zero voltage turn-on can be achieved in the boost mode of the proposed PEBB-s. It can be seen from Figure 4.1*a* that current rises continuously in case of the VSI PEBB and reaches its peak value at the end of the switching cycle, when hard turn-off takes place. The switching transient of

the CDR PEBB is shown in Figure 4.1*b,* where the high overvoltage peak over the switch can be observed during the turn-off. Thus, it is expected that the CDR PEBB will have significantly higher turn-off losses in comparison with the VSI PEBB. A similar behavior in the switching transients can be seen for the qZSI and CF-DC/DC PEBB-s, shown in Figure 4.1*c,d* respectively. It can be seen that the current has a decreasing slope before the turn-off that results in a lower current peak value and lower instantaneous current at the turn-off. This in turn results in lower turn-off losses.

Experimental results

The experimentally obtained conduction and switching losses in the nominal operating point are shown in Figure 4.2. As can be seen, the conduction losses of the CDR-DAB are the lowest ones in comparison with the other topologies, and are 10 % lower in comparison with the DAB. It is an expected result since CDR PEBB has a lower number of switches on the LV side. A slight rise in the conduction losses of the qZSI and CF-DC/DC PEBB-s was also expected, since additional elements are added to the conventional VSI PEBB. In the case of the qZSI PEBB additional voltage drops occur on the diode D_1 (see Figure 3.4) and on the resistances of the inductors L_1 and L_2. The switch T_C and inductor of the CF-DC/DC-DAB (see Figure 3.6) cause additional conduction losses in comparison with the DAB. Experimental results have shown that the conduction losses of the qZS-DAB and CF-DC/DC-DAB are approximately 7 % higher than those of the conventional DAB.

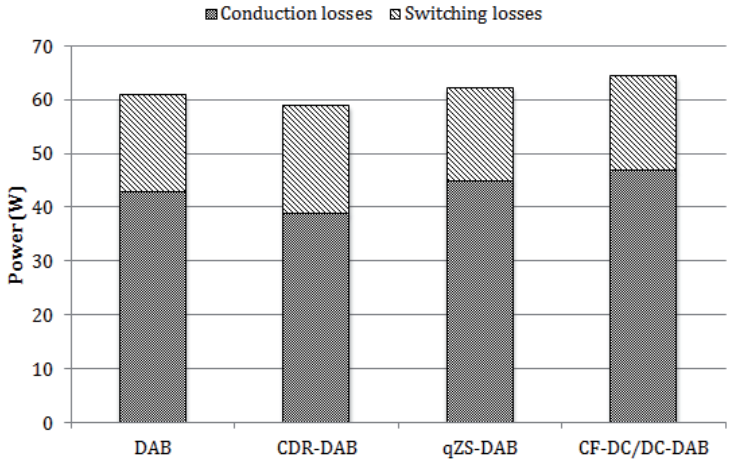


Figure 4.2. Comparison of the conduction and switching losses of the DAB and the new topologies in the reverse operating mode.

As can be seen from Figure 4.2, the switching losses of the CDR-DAB are notably higher than with the other topologies. In the nominal operating point the switching losses of the CDR-DAB are 11 % higher in comparison with the DAB. A reason for that are high overvoltage peaks that occur during the turn-

off (see Figure 4.1*b*). Lower switching losses of the qZS-DAB and the CF-DC/DC-DAB in comparison with the conventional DAB can be observed. That can be explained by the descending switch current slope of these topologies before the turn-off (see Figure 4.1*c,d*) as compared to the DAB. The lowest switching losses were observed in the qZS-DAB. That can be explained by low overvoltage peak over the switch during the turn-off. Additional switching losses in the CF-DC/DC-DAB were caused by the clamping switch T_C. As can be seen from the measurements, the switching losses are most critical for the CDR PEBB. One possible way to reduce the switching losses is to limit the overvoltage peaks by means of the clamping diode-resistor-capacitor snubber (see design guidelines in Chapter 3.2).

4.2 Current and Voltage Stress

The current and voltage stress values on the components have direct impact on the dimensioning and the reliability of the device, since they determine the worst case conditions that the components have to withstand. The current stress is defined as the RMS and the peak current value that flows through the switch, the capacitor or the transformer during the switching period. The voltage stress is defined as the on-state and peak value of the voltage that is applied to the switch, capacitor or other elements during the switching period. Reducing these values enables to increase the efficiency, reduce the component ratings and eventually reduce the cost of the converter.

The on-state stress values on the components can be derived from the steady state analysis of each PEBB. The on-state stress values on the components are presented in the design guidelines for each PEBB in the Chapters 3.2-3.4. However the dynamic stress depends on the circuit configuration and can be obtained experimentally.

The highest dynamic switch overvoltage stress takes place during the turn-off. Such voltage peaks increase the rating of the switches and the switching losses. That in turn increases the need for the switches with higher blocking voltage and higher cost. Although the voltage stress is more important issue on the MV side, reducing the voltage peaks on the LV side results in decreased switching losses. In addition, the RMS current of the capacitor and the switches has direct impact on the thermal performance of the components. The voltage and current stress values on the LV side switches, capacitors and transformer were experimentally obtained at the same power level. The proposed PEBB-s were analyzed in the reverse operating mode using the IMM and compared with the VSI PEBB. The results are shown in Table 4.1. The results are presented in physical units (p.u.) relative to the DAB ($U_{X,VSI}$(p.u.) = 1.0; $I_{X,VSI}$(p.u.) = 1.0).

Table 4.1 shows, that the overvoltage peak on the switch T_6 can be up to 205 % higher in the case of the CDR PEBB. On the other hand it can be seen that the overvoltage peak is reduced in the other PEBB-s. The current RMS values through the switch are increased for all the proposed PEBB-s. It can also be observed that as compared to the VSI PEBB the proposed PEBB-s decrease the peak value of the switch and thus that of the transformer. Reduced current

ripple in turn results in the lower switching losses. As the experimental results have shown, the current stress on the capacitor can be reduced up to 47 % for the CDR PEBB, due to good current ripple cancellation of the CDR circuit.

Table 4.1. The component current and voltage stress in the reverse operating mode in comparison with the DAB.

	CDR-DAB	**qZS-DAB**	**CF-DC/DC-DAB**
Peak voltage over switch T_6 (p.u.)	2.05	0.75	0.9
Switch T_6 RMS current (p.u.)	1.16	1.11	1.11
Peak current of the switch T_6 (p.u.)	0.84	0.88	0.81
Transformer RMS (p.u.)	0.8	0.9	0.92
Transformer peak current (p.u.)	0.72	0.73	0.77
Capacitor RMS current (p.u.)	0.53	0.79	0.89

It should be noted, that the peak values are additionally influenced by the leakage inductance of the MF transformer. Larger leakage inductance will decrease the transformer and switch current ripple, on the other hand it, has direct impact on the power transfer as shown by Eq. (3.3). The necessary leakage inductance value can be reduced, if the converter operates at a higher switching frequency.

4.3 Efficiency

Efficiency is one of the most important criteria in the selection of the suitable and most feasible topology for the isolation stage of the PET. As described in the introduction, the isolation stage will have a major impact on the efficiency of the whole PET.

The DAB is nowadays one of the most used topology in the HP applications where HF isolated DC/DC conversion takes place. The proposed PEBB-s for the LV side of the isolation stage showed a positive impact on the converter regarding the current stress on the components. However, the increase of the conduction losses is obvious if the conventional VSI is replaced with additional circuitry. Thus, it must be ensured that extending the DAB with the new topologies will not significantly reduce the efficiency of the converter in both operating modes.

The effect of the component losses on the efficiency in the reverse operating mode has been analyzed for the CDR PEBB in [PAPER-IV], for the qZS-DAB in [PAPER-VI] and for the CF-DC/DC-DAB in [PAPER-VIII]. The models

considered only the conduction losses in the switches, diodes and on the active resistances of the inductors and transformer.

In order to compare the mathematically obtained efficiencies with those of the real ones, the efficiency of each topology was determined experimentally. Therefore, the power on the MV and LV ports were measured and the efficiency was calculated according to 4.4:

$$\eta = \frac{P_{MV}}{P_{LV}} = \frac{I_{MV} \cdot U_{MV}}{I_{LV} \cdot U_{LV}}, \tag{4.4}$$

where I_{MV}, I_{LV} are the current on the MV and LV ports, and U_{MV}, U_{LV} are the voltages on the MV and LV ports respectively. The measured efficiency values for the DAB and the new topologies are shown in Figure 4.3. It can be seen, that in comparison with the DAB, the other topologies have slightly lower efficiency for the maximal given output power. The efficiency of the DAB for given parameters was 83 %, whereas the lowest efficiency was seen for the CDR-DAB, that comprised 81 %. The efficiencies of the qZS-DAB and the CF-DC/DC-DAB were approximately similar and comprised 82 %.

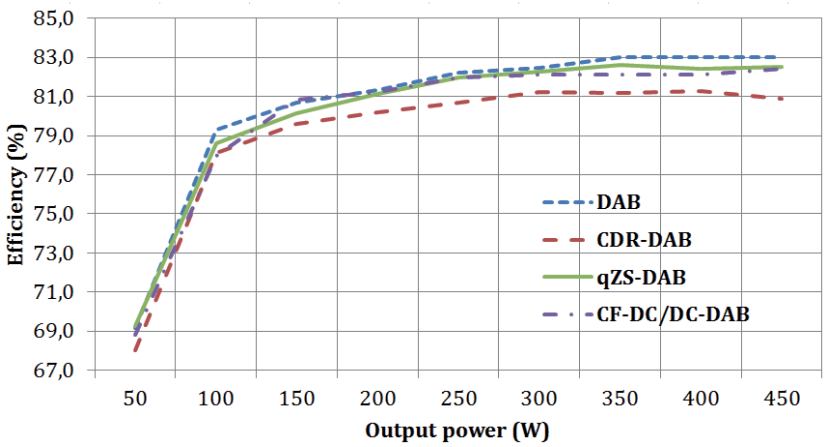


Figure 4.3. Efficiencies of the DAB and new topologies.

Mathematically and experimentally obtained efficiencies for the all topologies are compared in Table 4.2. The similar circuit parameters as in experimental prototype (see Table 3.1) were used in the mathematical models. As can be seen there is a roughly 10 % difference between the analytically derived and measured efficiencies. This is because only conduction losses in the models were analyzed, however the measured values also include the switching and the core losses of each topology.

In practice, the measured efficiency value is relatively low. This is due to the high losses in the power switches, which were not correctly selected for such a low voltage prototype. However, the improvement of the efficiency was outside the scope of the thesis, rather the aim was to compare the proposed PEBB-s

under similar conditions. The achieved results allow to assess the difference in the efficiencies of the proposed PEBB-s also for higher power ratings. In addition, the derived mathematical models allow to rate the impact of the conduction losses on the efficiency in the forward operating mode. In this case the proposed PEBB-s act as filters and affect mostly the conduction losses of the whole isolation stage.

Table 4.2. Estimated and measured efficiencies.

	DAB	CDR-DAB	qZS-DAB	CF-DC/DC-DAB
Estimated	92 %	92 %	89 %	91 %
Measured	83 %	81 %	82 %	82 %

Several solutions can be considered to increase the efficiency of the proposed PEBB-s. First of all, experimental and analytical results have stated that the on-state voltage drop of the IGBT-s affects mostly the efficiency. Thus, for lower currents, switches with lower on-state voltage drop are advisable. Special attention should be paid to the diode of the qZSI PEBB, that carries the whole input current and where a high voltage drop can significantly increase the conduction losses. In addition, to reduce the effect of the active resistance on the efficiency, wires as short as possible should be used.

In order to reduce the switching losses, first of all replacement of the IGBT-s with MOSFET-s that have lower switching losses, should be considered. In addition, the switching loss is affected by the peak value of the current at the turn-off time instance, thus adding additional inductive filters to reduce the current ripple should be considered.

4.4 Dynamic Analysis

In the distribution networks different types of voltage deviations and load transients are typical phenomenon that the transformers have to withstand. Such distortions on the primary side of the LFT are also reflected to the secondary side and vice versa. A controllable PET must ensure the stable voltage on both ports under the realistic conditions with changing line voltage and load. Typically the main functions of the converter's dynamic performance are line regulation and load transient response. Line regulation is the ability of a converter to provide a stable voltage on the output when the input voltage is changing. Load transient shows the reaction of the output to a rapidly changing load.

A comprehensive way to analyze the dynamic behavior of the converter is to perform the transient response analysis. For the isolation stage of the PET the two most common varying values are the voltage and the load on the LV side. Thus the load transient response of the isolation stage can be performed by varying the load on the LV side in the forward operating mode as shown in Figure 4.4*a*. On the other hand, the voltage level on the LV side DC-link must be kept on the stable level and provide stable output on the MV side when the PET operates in the reverse mode. In this way, it is necessary to perform the

line regulation by varying the voltage on the LV side and monitor the changes on the MV side as shown in Figure 4.4*b*. The dynamic performance of the DAB and the proposed topologies under varying voltage and load has been modeled using the open-loop control. The values of the passive elements used for each topology are shown in Table 4.3, where N_{TR} designates the transformer turn's ratio, L is the inductance used in the filters, L_{TR} is the leakage inductance of the MF transformer, C is the capacitance used in the filters. The losses in the switches are neglected.

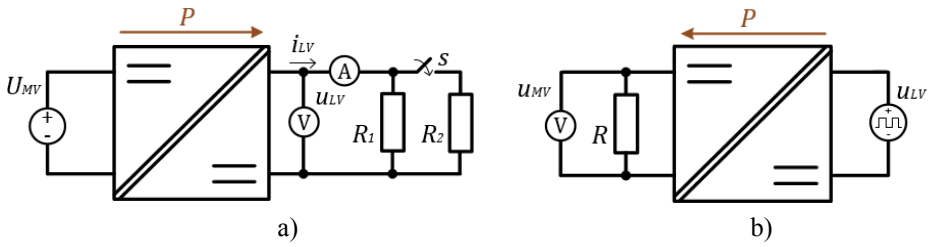


Figure 4.4. Block diagram of the simulation circuit. a) line regulation, b) load transient.

Table 4.3. Simulation parameters.

	DAB	**CDR-DAB**	**qZS-DAB**	**CF-DC/DC DAB**
U_{LV}	20…30 V			
U_{MV}	200 V			
f	20 kHz			
N_{TR}	1:6.6	1:3	1:6.6	1:6.6
L	-	500 µH	150 µH	150 µH
L_{TR}	7 µH	5 µH	7 µH	7 µH
C	100 µF	220 µF	50 µF	50 µF

Open-Loop Response to the Load Transient

In the distribution network the power is mainly transferred from the generator side towards the consumers and the isolation stage will mainly operate in the forward operating mode. Hence, the load variation on the LV side is the phenomenon that the PET will have to deal with most of the time. In order to obtain the load transient on the LV side in the forward operating mode, the load R on the LV side was periodically changing between 100 % and 50 %. For the control of DAB based circuits the rectangular phase shift modulation was used. The CDR PEBB was used as an uncontrollable rectifier. The phase angle and the duty cycle were chosen such that equal output power could be achieved. The voltage on the MV side was kept on the constant level (U_{MV} = 200 V). The simulation results for the load transient in the forward operating mode are presented in Figure 4.5. The voltage and current overshoots with settling times

for each topology are presented in Table 4.4. Settling time is defined as the duration until the voltage reaches 5 % of the final value.

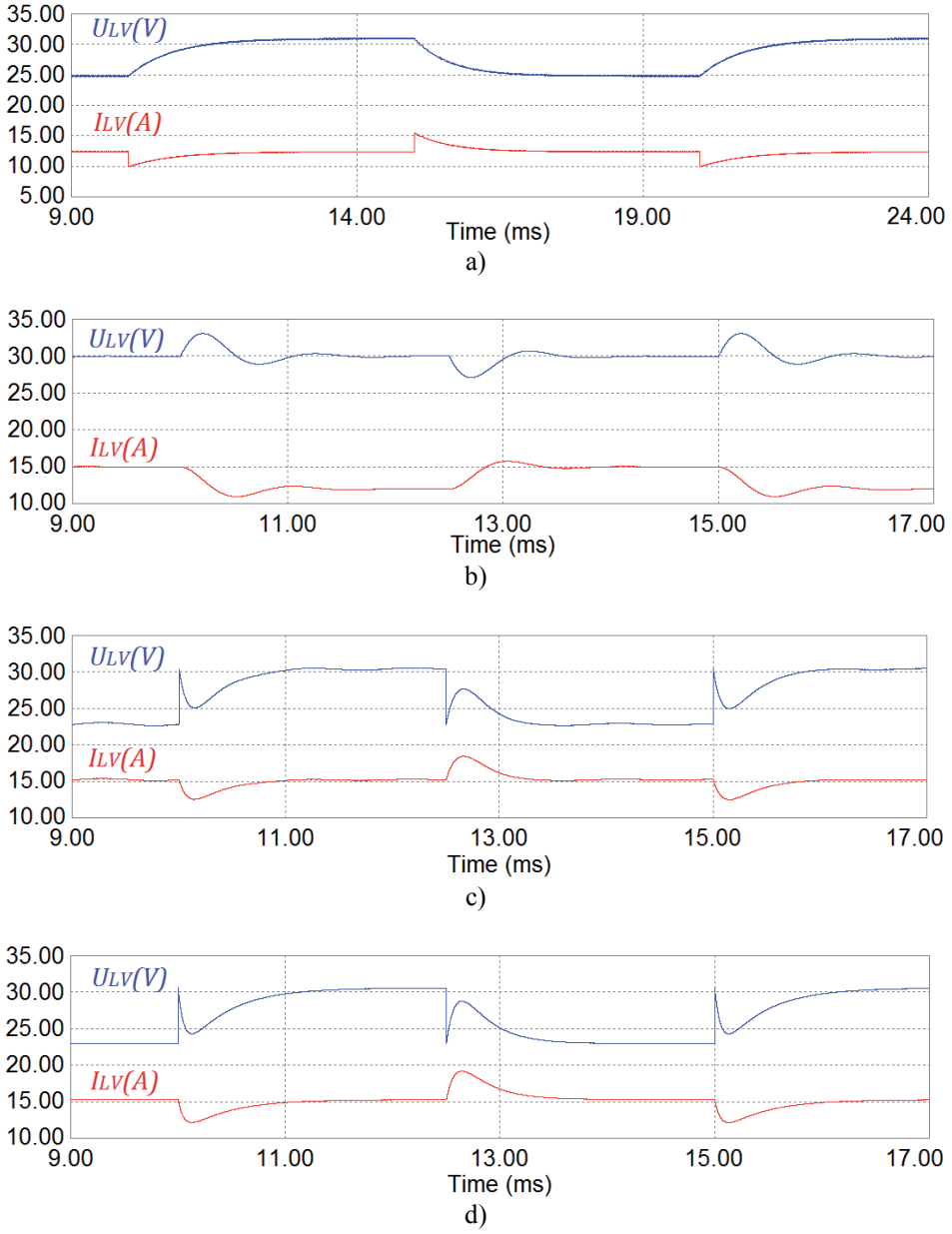


Figure 4.5. Load response on the LV side in the forward operating mode: a) DAB; b) CDR-DAB; c) qZS-DAB; d) CF-DC/DC-DAB.

Table 4.4. Summary of load transient of the different topologies.

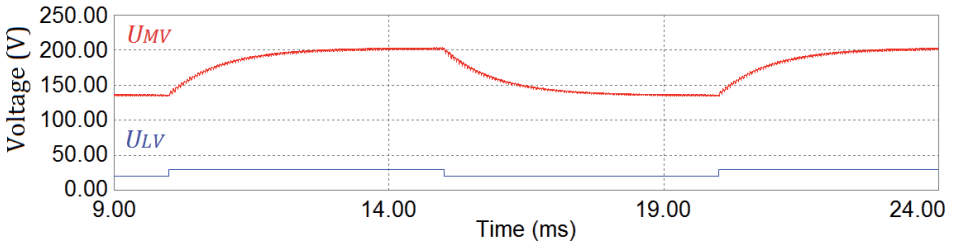
	DAB	CDR-DAB	qZS-DAB	CF-DC/DC-DAB
Settling time (ms)	1.13	0.94	0.73	0.90
Voltage overshoot (p.u.)	1.00	1.10	1.00	1.00
Current overshoot (p.u.)	1.24	1.05	1.20	1.26

From the analysis, it can be seen that all the topologies showed stable responses. The load transient of the DAB is shown in Figure 4.5*a*. It can be seen that the voltage transient has aperiodic behavior with $t = 1.13$ ms settling time. A rapid change in the current with 1.24 p.u. can be observed. In comparison with the DAB, the voltage transient of the CDR-DAB (see Figure 4.5*b*) has 10 % voltage overshoot however the current follows a smooth slope. On the other hand, the current overshoot of the CDR-DAB was the smallest among the others. All the other topologies had a current overshoot of more than 120 % of the final value. The load transient for qZS-DAB (see Figure 4.5*c*) and the CF-DC/DC-DAB (see Figure 4.5*d*) have similar character with an aperiodic behavior of the voltage transient and reduced rate of the current change. The qZS-DAB has shown the fastest settling time of $t = 0.73$ ms.

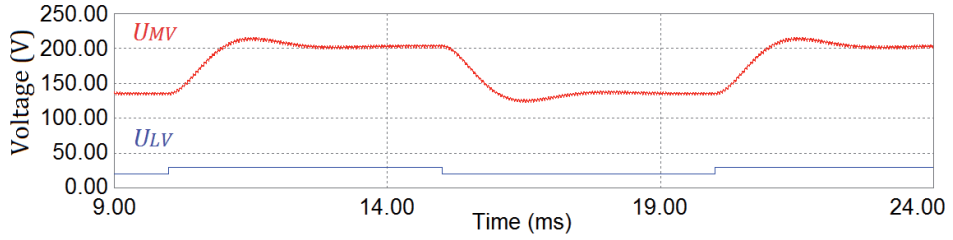
Open-loop response to the LV side voltage transient

In order to obtain the transient response on the MV side, the voltage on the LV side was periodically changing between the 30 V and 20 V and the converter was operating in the reverse operating mode. The duty cycle, phase angle and the load were chosen such that equal power rating could be achieved at the desired voltage level on the MV side ($U_{MV} = 200$ V). The response of the MV side to the LV side transient for each topology is presented in Figure 4.6. The overshoot and settling times for each topology are presented in Table 4.5. Settling time is defined as the duration until the voltage reaches 5 % of its final value.

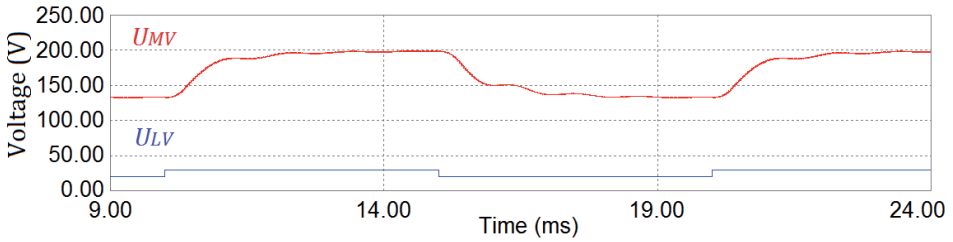
It can be seen that in the open-loop all the topologies show the stable response to the line regulation on the LV side and the desired voltage level on the MV is achieved without any significant deviations or overshoots. Figure 4.6*a* shows the transient response of the DAB. The response has aperiodic behavior with a $t = 1.56$ ms settling time. The longest settling time $t = 1.93$ ms has been observed for the CF-DC/DC-DAB (see Figure 4.6*d*). Moreover, a long settling time $t = 1.85$ ms was observed for the qZS-DAB (see Figure 4.6*c*). The fastest response to the line regulation with settling time $t = 0.87$ ms could be observed for the CDR-DAB as shown in Figure 4.6*b.* The line regulation of the proposed topologies has shown that the voltage overshoot of 10 % occurred only in case of the CDR-DAB.



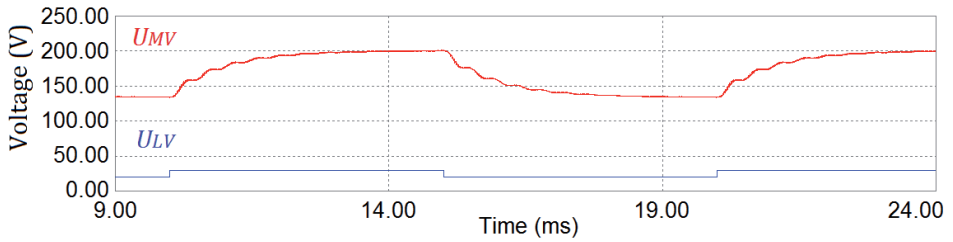
a)



b)



c)



d)

Figure 4.6. Line regulation on the MV side in the reverse operating mode: a) DAB; b) CDR-DAB; c) qZS-DAB; d) CF-DC/DC-DAB.

Table 4.5. Summary of the line regulation.

	DAB	**CDR-DAB**	**qZS-DAB**	**CF-DC/DC-DAB**
Settling time (ms)	1.56	0.87	1.85	1.93
Voltage overshoot (p.u.)	1.00	1.08	1.00	1.00

4.5 Summary

This chapter presented the comparison between the dual active bridge and the new topologies, based on the proposed PEBB-s: CDR-DAB, qZS-DAB and CF-DC/DC-DAB. To perform a comprehensive comparison, the proposed topologies were analyzed on the experimental prototype under similar conditions in the reverse operating mode. The improved modulation method was used for the control the PEBB-s. Focus was on the following features: i) conduction losses in the power switches, diodes and the resistance of the inductors and transformers; ii) switching losses of the switches; iii) current and voltage stress on the different components of the PEBB-s, iv) efficiency; v) line regulation and load transient response.

The analytical and experimental analysis of the conduction losses has shown that the highest conduction losses occur due to collector-to-emitter voltage drop of the IGBT-s in comparison with the active resistance. The converter was tested under relatively low power, however with the increase of the power it is expected that the conduction losses on the active resistances will become more significant. The conduction losses were lowest in the case of the CDR-DAB, and were 10% lower than with the DAB. This can be explained by the smaller number of the power switches of the CDR-DAB. The conduction losses of the qZS-DAB and CF-DC/DC-DAB were both approximately 7 % higher in comparison with the DAB. That can be explained by the additional losses on the diode and active resistances on the inductors of the qZSI PEBB. Additional losses in the CF-DC/DC PEBB occur in the extra clamping switch and the LV side inductor.

The switching losses were also obtained from the experimental prototype for each topology by measuring the voltage and current waveforms during the switching transients. Under the investigated operation range, the ZV turn-on of the switches could be observed for all PEBB-s. However, the switches are hard-switched during the turn-off transition and thus the turn-off losses comprise the major part of the switching losses. The highest switching losses occurred in the CDR-DAB, although this PEBB has the lowest component count, and were 11 % higher than with the switching losses of the DAB. This can be explained by the occurrence of the enormous overvoltage peaks over the switches that were up to 200 % higher than with the DAB. The switching losses were slightly lower (appr. 2 %) in the case of the qZS-DAB and the CF-DC/DC-DAB in comparison with the DAB, even though it was expected that the CF-DC/DC PEBB has an additional switch which is turned-on under two times higher switching frequency. However, it's impact was not significant since the current level through the switch is significantly lower in comparison with inverter switches. Lower switching losses occur due to the lower current peak value of the qZS-DAB and the CF-DC/DC-DAB than of the DAB.

The current and voltage stress analysis has revealed several benefits and challenges of the proposed PEBB-s in comparison with the VSI PEBB. The most important facts are the drastically higher (205 %) overvoltage peaks over the switches of the CDR PEBB. This in turn increases the voltage rating of the

switches and snubber circuit is needed to limit the overvoltage spikes. On the contrary, the overvoltage stress of the qZSI PEBB was 25 % lower in comparison with the VSI PEBB. Another important result was reduced current ripple of the proposed PEBB-s. Reduced current ripple results in reduced switch and transformer peak currents, that in turn results in lower device rating and eventually higher efficiency. In addition, reduced current ripple affects the RMS current of the capacitor. The capacitor current stress value can be reduced up to 47 % in the case of the CDR PEBB in comparison with the VSI PEBB.

The efficiency was analyzed analytically and experimentally for each topology. The mathematical models considered only the impact of the conduction losses on the efficiency, whereas the component values were chosen the same as in the experimental test bench. The mathematical results have shown that for the given parameters and neglecting the core and switching losses, the efficiency over 90 % can be achieved for most of the topologies. However, the experimental results have shown ca 10 % lower efficiency in comparison with the analytical expectations. This is because the mathematical models did not include the switching and core losses. The measured efficiency was highest for the DAB topology (83 %), and the lowest for the CDR-DAB (81 %). The obtained efficiency values are relatively low. This is due to high on-state voltage drop of the IGBT-s in comparison with the low input voltage. However, the aim of the thesis was not to achieve the highest efficiency, but rather to compare the alternative topologies with the DAB under similar condition. Obtained results can provide helpful material in assessment of the feasibility of the proposed PEBB-s for the isolation stage of the PET.

The dynamic analysis, including the line regulation and load transient, for all topologies was performed. In the line regulation, all topologies showed stable response. The CDR-DAB showed the fastest settling time among others, however with a 8 % voltage overshoot. The other topologies showed aperiodic behavior without any voltage overshoots. The longest settling time of $t = 1.93$ ms was shown by the CF-DC/DC-DAB. In the load transient analysis, the qZS-DAB had the fastest settling time among others, that comprised $t = 0.73$ ms. The slowest settling time $t = 1.13$ ms was observed with the DAB. Only the CDR-DAB showed the voltage overshoot of 10 % whereas all other topologies showed aperiodic voltage behavior. On the other hand, load transient has shown the occurrence of the current overshoot, that was more than 20 % for the DAB, the qZS-DAB and the CF-DC/DC-DAB. The smallest current overshoot of 5 % was observed for the CDR-DAB.

5 FUTURE WORK

The thesis proposed three new PEBB-s for the LV side of the isolation stage of the PET: CDR with a bi-directional power flow capability, quasi-Z source inverter and current-fed DC/DC converter based with an active clamp.

Although the proposed PEBB-s may increase the volumes of the PET due to the presence of the passive elements in the circuit, they reduce the current stress on the circuit components, reduce the transient response and have voltage regulation capabilities, while maintaining the advantages of the phase shift controlled DAB. It would be interesting to investigate the influence of the passive elements on the reliability and the lifetime of the PET.

Using the modular design of the isolation stage reduces the voltage stress on the switches and thus, allows switches with lower power ratings and higher switching frequencies to be selected. However, the next generation of silicon carbide (*SiC*) and gallium nitrate (*GaN*) based switches, like IGBT's and JFET's with higher voltage blocking and faster switching capabilities could offer more compact design, improved performance and higher efficiency of the PET.

Moreover, alternative modulation methods for DAB based circuits such as trapezoidal and triangular modulation should be investigated. In such a way, a soft switching capability of the converter could be improved, that would result in increased efficiency of the whole system.

Significant attention should be paid on the design and selection of the magnetic core of the MF transformer. By selecting proper core material, the higher saturation flux density can be achieved that in turn allows the size of the core to be reduced even more. Different materials that are suitable for the transformer core, such as ferrite, amorphous materials and nanocrystalline should be investigated.

Although the new PEBB-s were proposed for the isolation stage of the PET, they can easily be combined into a new multi-port converter with magnetic or DC coupling as shown in Figure 5.1. Such a configuration allows us to integrate the different generating and storage elements into one system and widen the overall performance of the PET.

Finally, it would be interesting to realize the entire concept of the power electronic transformer that would incorporate the new topologies based on the proposed power electronic building blocks. That would allow us to combine the voltage regulation of the isolation stage together with active front-ends on the MV and LV ports.

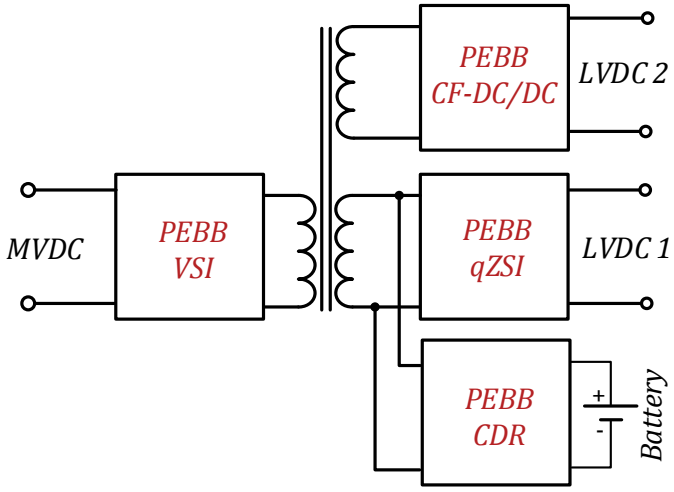


Figure 5.1. Possible use of the new PEBB-s in multiport converters with magnetic coupling.

References

[1] Hengsi Qin; “Dual Active Bridge Converters in Solid State Transformers”, Doctoral dissertation, 2012

[2] T. Zhao, J. Zeng, S. Bhattacharya, M. E. Baran, A.Q. Huang “*An Average Model of Solid State Transformer for Dynamic System Simulation*”. PES 2009, pp. 1-8.

[3] Roasto, I.; Romero-Cadaval, E.; Martins, J.; Smolenski, R., "State of the art of active power electronic transformers for smart grids," *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.5241,5246, 25-28 Oct. 2012

[4] Schietekat, L. M.; “Design and Implementation of the Main Controller of a Solid-State Transformer”, Doctoral dissertation, 2011.

[5] McDonald, J. “Adaptive Intelligent Power Systems: Active Distribution Networks”, Institute for Energy and Environment of University Stratchclyde.

[6] Federal register, 10 CFR Part 431, Energy Conversation Program for Commercial Equipment, Distribution transformers Energy Conversation Standards; Final Rule.

[7] Xu She; Burgos, R.; Gangyao Wang; Fei Wang; Huang, A.Q.; , "Review of solid state transformer in the distribution system: From components to field application," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.4077-4084, 15-20 Sept. 2012.

[8] Xu She; Lukic, S.; Huang, A.Q.; Bhattacharya, S.; Baran, M.; , "Performance evaluation of solid state transformer based microgrid in FREEDM systems," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.182-188, 6-11 March 2011.

[9] Jianhua Zhang; Wenye Wang; Bhattacharya, S.; , "Architecture of solid state transformer-based energy router and models of energy traffic," *Innovative Smart Grid Technologies (ISGT), 2012 IEEE PES*, vol., no., pp.1-8, 16-20 Jan. 2012.

[10] T. Ericsen, “Power ElecVOlua Building Blocks”, The Electric Warship Conference. IMEiEWSEE. London, 1997.

[11] Hengsi Qin; Kimball, J.W.; , "A comparative efficiency study of silicon-based solid state transformers," *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE* , vol., no., pp.1458-1463, 12-16 Sept. 2010.

[12] Falcones, S.; Xiaolin Mao; Ayyanar, R.; , "Topology comparison for Solid State Transformer implementation," *Power and Energy Society General Meeting, 2010 IEEE* , vol., no., pp.1-8, 25-29 July 2010.

[13] Heinemann, L.; Mauthe, G.; , "The universal power electronics based distribution transformer, an unified approach," *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual* , vol.2, no., pp.504-509 vol.2, 2001.

[14] Kang, M.; Enjeti, P.N.; Pitel, I.J.; , "Analysis and design of electronic transformers for electric power distribution system," *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97., Conference Record of the 1997 IEEE* , vol.2, no., pp.1689-1694 vol.2, 5-9 Oct 1997.

[15] Nath, S.; Mohapatra, K.K.; Basu, K.; Mohan, N.; , "Source based commutation in matrix converter fed power electronic transformer for power systems application," *Power Electronics Electrical Drives Automation and Motion (SPEEDAM), 2010 International Symposium on* , vol., no., pp.1682-1686, 14-16 June 2010.

[16] Mirmousa, H.; Zolghadri, M.R.; , "A Novel Circuit Topology for Three-Phase Four-Wire Distribution Electronic Power Transformer," Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on , vol., no., pp.1215-1222, 27-30 Nov. 2007.

[17] Basu, K.; Gupta, R.K.; Nath, S.; Castelino, G.F.; Mohapatra, K.K.; Mohan, N.; , "Research in matrix-converter based three-phase power-electronic transformers," *Power Electronics Conference (IPEC), 2010 International* , vol., no., pp.2799-2803, 21-24 June 2010

[18] Wrede, H.; Staudt, V.; Steimel, A.; , "Design of an electronic power transformer," *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]* , vol.2, no., pp. 1380- 1385 vol.2, 5-8 Nov. 2002

[19] Ronan, E.R.; Sudhoff, S.D.; Glover, S.F.; Galloway, D.L.; , "A power electronic-based distribution transformer," *Power Delivery, IEEE Transactions on* , vol.17, no.2, pp.537-543, Apr 2002

[20] M.Glinka and R.Marquardt, “A new AC/AC multilevel converter family,” *IEEE.Trans.Ind.Electron.*, vol.52, no.3, pp.662-669, June 2005.

[21] P.Drabek, Z.Peroutka, M.Pittermann, and M.Cedl, “New configuration of traction converter with medium frequency transformer using matrix converters,”*IEEE.Trans.Ind.Electron.*, vol.58, no.11, pp. 5041 - 5048, Nov. 2011.

[22] M.Sabahi, A.Y.Goharrizi, S.H.Hosseini, M.B.B.Sharifian, and G.B.Gharehpetian, “Flexible power electronic transformer,” *IEEE.Trans.Power.Electron.*, vol.25, no.8, pp.2159-2169, 2010.

[23] A.J.Jin, H.T.Li, and S.L.Li, “A new matrix type three-phase four-wire power electronic transformer,” in *Proc.IEEE.PESC.,* 2006, pp.1-6.
[24] Banaei, M.R.; Salary, E.; , "Power quality improvement based on novel power electronic transformer," Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2011 2nd , vol., no., pp.286-291, 16-17 Feb. 2011
[25] M.Sabahi, S.H.Hosseini, M.B.Sharifian, A.Y.Goharrizi, and G.B.Gharehpetian, “Zero-voltage switching bi-directional power electronic transformer,” *IET.Power.Electron.*, vol.3, no.5, 2010, pp. 818-828.
[26] G.Ortiz, J.Biela, D.Bortis, and J.W.Kolar, “1 Megawatt, 20 kHz, isolated, bidirectional 12kV to 1.2kV DC-DC converter for renewable energy applications,” in *Proc. Intel. IPEC* 2010., pp. 3212-3219
[27] Beldjajev, V.; Roasto, I.; Vinnikov, D.; , "Analysis of current doubler rectifier based high frequency isolation stage for intelligent transformer," *Compatibility and Power Electronics (CPE), 2011 7th International Conference-Workshop* , vol., no., pp. 336-341, 1-3 June 2011
[28] Manjrekar, M.D.; Kieferndorf, R.; Venkataramanan, G.; , "Power electronic transformers for utility applications," *Industry Applications Conference, 2000. Conference Record of the 2000 IEEE* , vol.4, no., pp. 2496-2502 vol.4, Oct 2000
[29] Iman-Eini, H.; Farhangi, S.; , "Analysis and Design of Power Electronic Transformer for Medium Voltage Levels," *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE* , vol., no., pp.1-5, 18-22 June 2006
[30] Bhattacharya, S.; Tiefu Zhao; Gangyao Wang; Dutta, S.; Seunghun Baek; Yu Du; Parkhideh, B.; Xiaohu Zhou; Huang, A.Q.; , "Design and development of Generation-I silicon based Solid State Transformer," Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE , vol., no., pp.1666-1673, 21-25 Feb. 2010.
[31] Iman-Eini, H.; Schanen, J.; Farhangi, S.; Barbaroux, J.; Keradec, J.; , "A power electronic based transformer for feeding sensitive loads," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* , vol., no., pp. 2549-2555, 15-19 June 2008
[32] Beldjajev, V.; Roasto, I.; Lehtla T.; , “Intelligent Transformer: Possibilities and Challenges” RTU, 2011. , pp. 14 Okt 2011.
[33] G.Brando, A.Dannier, and A.D.Pizzo, “A simple predictive control technique of power electronic transformers with high dynamic features,” in *Proc.IEEE.PEMD.*, 2010, pp.1-6.
[34] D.Grider, M.Das, A.Agarwal, J.Palmour, S.Leslie, J.Ostop, R.Raju, M.Schutten, and A.Hefner, “10kV/120A SiC DMOSFET Half-bridge Power Modules for 1MVA Solid State Power substation,” in *Proc.IEEE.Electric Ship Tech. Symp.*, 2011, pp.131-134.
[35] J.S.Lai, A.Maitra, A.Mansoor, and F.Goodman, “Multilevel intelligent universal transformer for medium voltage application,” in *Proc.IEEE.Ind.Appl.Conf.*, 2005, pp.1893-1899.
[36] N. A. Moguilnaia, K. V. Vershinin, M. R. Sweet, O. I. Spulber, M. M. De Souza, and E. M. S. Narayanan, “Innovation in Power Semiconductor Industry: Past and Future,” *IEEE Trans.Eng. Manage.,* vol. 52, no.4, pp. 429–439, Nov. 2005
[37] C. Gerster, “Fast High-Power/High-Voltage Switch Using Series-Connected IGBTs with Active Gate-Controlled Voltage Balancing,” in *Proc. IEEE Applied Power Electronics Conf.,*1994, pp. 469–472.
[38] D. Aggeler, J. Biela, J. W. Kolar, “Solid-State Transformer based on SiC JFETs for Future Energy Distribution Systems,” in *Proc. the Smart Energy Strategies Conference,* 2008.
[39] H. Fan.”Advanced Medium-Voltage Bi-Directional DC-DC Converter Systems for Future Electric Energy Delivery and Management Systems”, Doctoral dissertation, 2011.
[40] J. Rodr´ıguez, J. Lai, and F. Peng, “Multilevel inverters: A survey of topologies, controls and applications,” IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724–738, Aug. 2002.
[41] J. W. van der Merwe and H. du T. Mouton, “Solid-state transformer topology selection,” in Proceedings of the IEEE International Conference on Industrial Technology, Churchill, Victoria 3842 Australia, Feb 2009.
[42] J.-S. Lai, “Designing the next generation distribution transformers: New power electronicbased hybrid and solid-state design approaches,” in Proceedings of the Lasted International Converence POWER AND ENERGY SYSTEMS, Palm Springs, CA, USA, Feb 2003.
[43] Jih-Sheng Lai; Maitra, A.; Goodman, F.; , "Performance of a Distribution Intelligent Universal Transformer under Source and Load Disturbances," *Industry Applications Conference, 2006. 41st IAS Annual Meeting. Conference Record of the 2006 IEEE* , vol.2, no., pp.719-725, 8-12 Oct. 2006
[44] Chen Ling; Baoming Ge; Daqiang Bi; Qingqing Ma; , "An effective power electronic transformer applied to distribution system," *Electrical Machines and Systems (ICEMS), 2011 International Conference on* , vol., no., pp.1-6, 20-23 Aug. 2011.
[45] Vinnikov, D.; Roasto, I,; Zakis, J., “*New Step-Up DC/DC Converter for Fuel Cell Powered Distributed Generation Systems: Some Design Guidelines*”. Przeglad Elektrotechniczny, vol. 86, no 8. pp. 245 – 252, 2010.

[46] J. W. Kimball, J. T. Mossoba, and P. T. Krein, “A Stabilizing, High Performance Controller for Input-Series-Output-Parallel Converters,” *IEEE Trans. Power Electron.,* vol. 23, no. 3, pp. 1416-1427, May. 2008.
[47] W. Chen, K. Zhuang, and X. Ruan, “A Input-Series- and Output-Parallel-Connected Inverter System for High-Input-Voltage Applications,” *IEEE Trans. Power Electron.,* vol. 24, no. 9, pp. 2127–2137, Sept. 2009.
[48] R. Ayyanar, R. Giri, and N. Mohan, “Active Input-Voltage and Load-Current Sharing in Input-Series and Output-Parallel Connected Modular DC-DC Converters Using Dynamic Input-Voltage Reference Scheme,” *IEEE Trans. Power Electron*., vol.19, no. 6, pp. 1462–1473. Nov. 2004
[49] J. W. Kim, J. S. You, and B. H. Cho, “Modeling, Control, and Design of Input-Series-Output-Parallel-Connected Converter for High-Speed-Train Power System,” *IEEE Trans. Ind.Electron*., vol. 48, no. 3, pp. 534-544, Jun. 2001
[50] J. W. Kimball, J. T. Mossoba, and P. T. Krein, “A Stabilizing, High Performance Controller for Input-Series-Output-Parallel Converters,” *IEEE Trans. Power Electron.,* vol. 23, no. 3, pp. 1416-1427, May. 2008.
[51] Deshang Sha, Zhiqiang Guo, and Xiaozhong Liao, “Cross Feedback Output Current Sharing Control for Input-Series-Output-Parallel Modular DC-DC Converters,” *IEEE Trans. Power Electron*., vol. 25, no. 11, pp. 2762-2771, 2010.
[52] Martinez, C.; Jalakas, T.; Vinnikov, D.; Lazaro, A.; Barrado, A.; , "QZSI DC/DC converters in input-series output-parallel connection for distributed generation," *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012 International Symposium on* , vol., no., pp.952-957, 20-22 June 2012
[53] Jianjiang Shi; Jie Luo; Xiangning He; , "Common-Duty-Ratio Control of Input-Series Output-Parallel Connected Phase-shift Full-Bridge DC–DC Converter Modules," *Power Electronics, IEEE Transactions on* , vol.26, no.11, pp.3318-3329, Nov. 2011
[54] Taotao Jin; Zhang, K.; Kan Zhang; Smedley, K.; , "A New Interleaved Series Input Parallel Output (ISIPO) Forward Converter With Inherent Demagnetizing Features," *Power Electronics, IEEE Transactions on* , vol.23, no.2, pp.888-895, March 2008
[55] Wang Hui; Tan Xing-guo; Li Qing-min; Zhou Fei; Deng Zhan-feng; Li Zhen-he; Lu Nan; , "Development and applicability analysis of intelligent solid state transformer," *Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011 4th International Conference on* , vol., no., pp.1150-1154, 6-9 July 2011
[56] Karshenas, H.R.; Daneshpajooh, H.; Safaee, A.; Bakhshai, A.; Jain, P.; , "Basic families of medium-power soft-switched isolated bidirectional dc-dc converters," *Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2011 2nd* , vol., no., pp.92-97, 16-17 Feb. 2011
[57] Chuanhong Zhao; Weiss, M.; Mester, A.; Lewdeni-Schmid, S.; Dujic, D.; Steinke, J.K.; Chaudhuri, T.; "Power electronic transformer (PET) converter: Design of a 1.2MW demonstrator for traction applications," *Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), 2012 International Symposium on* , vol., no., pp.855-860, 20-22 June 2012
[58] Sixifo Daniel Falcones Zambrano.”A DC-DC Multiport Converter Based Solid State Transformer”. Doctoral dissertation,2011.
[59] Du, S.B.Y.; Gangyao Wang; Bhattacharya, S.; , "Design considerations of high voltage and high frequency transformer for solid state transformer application," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.421-426, 7-10 Nov. 2010
[60] Krismer, Florian. Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies. ETH(2010).
[61] Yang Lijiao; Su Shiping; , "Study of Intelligent Universal Transformer operation model and DSP control," *Advanced Power System Automation and Protection (APAP), 2011 International Conference on* , vol.2, no., pp.1488-1492, 16-20 Oct. 2011
[62] Brooks. P. N.; “Black Start Control of a Solid State Transformer for Emergency Distribution Power Restoration”. Master Thesis, 2012
[63] Khazarei. S. M.;”Stability Challenges and Solutions in Current-Mode Controlled Power Electronic Converter”. Doctoral dissertation, 2012.
[64] Tiefu. Z.;”Design and Control of a Cascaded H-Bridge Converter Based Solid State Transformer”. Doctoral dissertation, 2010.
[65] Gangyao Wang; Seunghun Baek; Elliott, J.; Kadavelugu, A.; Fei Wang; Xu She; Dutta, S.; Yang Liu; Tiefu Zhao; Wenxi Yao; Gould, R.; Bhattacharya, S.; Huang, A.Q.; , "Design and hardware implementation of Gen-1 silicon based solid state transformer," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.1344-1349, 6-11 March 2011
[66] Yu Du; Seunghun Baek; Bhattacharya, S.; Huang, A.Q.; , "High-voltage high-frequency transformer design for a 7.2kV to 120V/240V 20kVA solid state transformer," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.493-498, 7-10 Nov. 2010

[67] K. Wang, F. C. Lee, and J. Lai, “Operation principles of bi-directional full-bridge DC/DC converter with unified soft-switching scheme and soft-starting capability,” *Proc. of the 15th IEEE Annual Applied Power Electronics Conference and Exposition (APEC 2000)*, vol. 1, New Orleans, LA, 6–10 Feb. 2000, pp. 111–118.
[68] N. Schibli, “Symmetrical multilevel converters with two quadrant DC/DC feeding”, EPFL, Thèse Nr. 2220, pp. 99-171, 2000.
[69] Krismer, F.; Biela, J.; Kolar, J.W., "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005* , vol.1, no., pp.599,606 Vol. 1, 2-6 Oct. 2005
[70] D. Aggeler, “Bidirectional galvanically isolated 25 kW 50 kHz 5 kV/700 V Si-SiC Supercascode/ Si-IGBT DC/DC onverter”, Ph. D. dissertation, ETH Zürich, 2010.
[71] Ott, S.; Jalakas, T.; Vinnikov, D.; Roasto, I., "Experimental analysis of extended boost quasi-Z-Source inverters," *Electronics Conference (BEC), 2012 13th Biennial Baltic* , vol., no., pp.259,262, 3-5 Oct. 2012
[72] Andrijanovitš, A, “New Converter Topologies for Integration of Hydrogen Based Long Term Energy Storages To Renewable Energy Systems”. Ph. D. dissertation, Tallinn University of Technology, 2013.
[73] Zakis, J.; Vinnikov, D.; Rankis, I., "Steady state analysis of the galvanically isolated DC/DC converter with a commutating LC filter," *Industrial Technology (ICIT), 2012 IEEE International Conference on* , vol., no., pp.827,832, 19-21 March 2012
[74] Sangtaek Han; Divan, D., "Dual active bridge buck-boost converter," *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE* , vol., no., pp.2905,2911, 20-24 Sept. 2009.
[75] Chen, Y. -T; Jiang, R. -S; Liang, R. -H, "Analysis and design of zero-voltage-switching parallel interleaved current-doubler converters with coupled output inductors," *Power Electronics, IET* , vol.5, no.4, pp.467,476, April 2012
[76] Tsai-Fu Wu; Cheng-Tao Tsai; Yaow-Ming Chen; Chang, Y.-D.; Chang, Y.-D., "Analysis and Implementation of an Improved Current-Doubler Rectifier With Coupled Inductors," *Power Electronics, IEEE Transactions on* , vol.23, no.6, pp.2681,2693, Nov. 2008
[77] Turn-Off Snubber Design for High Frequency Modules. Europe, Application Note APT0404, Advaced Power Technology, December 2004.
[78] Todd, P. C.; Snubber Circuits: Theory, Design and Application. Unitrode Corporation, May 1993.
[79] Design Guidelines for RCD Snubber of Flyback Converters. Application Note AN-4147. Fairchild Semiconductor, 2006.

Acknowledgement

The research for the degree of PhD was conducted at Tallinn University of Technology, the Department of Electrical Drives and Power Electronics during four years of study. First of all I would like to express my appreciation to my supervisors Dr. Indrek Roasto, Prof. Tõnu Lehtla and Prof. Marius Klytta for their helpfulness and encouragement during the years of my research.

Secondly, I would like to express my gratitude to Dr. Sc. techn. Dmitri Vinnikov for helping me to plan research directions and publish the scientific papers in international journals and conference proceedings. Moreover, I am thankful to him for giving me relevant and substantial advice during the work.

In addition, I would like to thank my colleagues Janis Zakis, Oleksandr Husev, Andrii Chub, Andrei Blinov, Alexandr Suzdalenko, Anton Rassõlkin and Tanel Jalakas who helped me with their substantial advice regarding to scientific work and article publishing. Moreover, I am thankful to them for creating favorable atmosphere for my work. Also, I would like to thank Mare-Anne Laane for revising and editing the English texts in my articles.

Also, I would like to express my sincere thanks to all other colleagues from Tallinn University of Technology, Department of Electrical Drives and Power Electronics for their versatile help and support during the four years of research.

I would also like to thank Estonian Ministry of Education and Research (Project SF0140016s11), Estonian Research Council (Grant ETF8687), Doctoral School of Energy and Geotechnology II and Archimedes Foundation for supporting the research with the funding.

My sincere thanks go to my family and my friends for their care and motivation, because it was thanks to them that this thesis became possible.

Thank you all!

Viktor Beldjajev

Abstract

Research and Development of the New Converter Topologies for the Isolation Stage of the Power Electronic Transformer.

Conventional power system consists of large centralized generators, passive transformers, transmission lines, substations and consumers, whereas the electrical energy flows uni-directionally from the generator's side to the consumers. The nowadays low frequency (50 Hz and 60 Hz) AC transmission system uses the magnetically coupled transformer concept for voltage elevation, transmission over long distances and voltage reduction for residential use. However, growing number of renewable energy sources results in rising number of distributed power plants which are principally subject to energy fluctuations. Therefore it is essential to build energy storages (e.g. batteries, ultra capacitor banks, hydrogen buffer) to the distributed power plants for compensating the power demand during the low production periods (e.g. during the night for PV systems, during silent wind periods). In addition, the consumers can supply energy to the grid by means of a local (e.g. roof mounted) power plant, regenerative braking of electrical drives and vehicle-to-grid systems. Many DG sources cannot be connected directly to the AC systems, hence they require power electronic interface. To easily connect these new energy sources to the grid and improve the power quality by harmonic filtering, voltage sag correction, dynamic control of the power flow etc., a new power electronic transformer (PET) is required.

As compared to the conventional line frequency transformer, the PET has lower mass and volumes. This is achieved thanks to the high frequency isolation stage, where the required power density of the magnetic core can be achieved at lower volumes. Isolation stage presents a high-frequency isolated DC/DC converter. The research has shown that isolation stage will mostly determine the volumes, efficiency and overall performance of the PET since the most important power conversion stage takes place in the isolation stage. That makes the isolation stage of the PET an interesting subject of the research.

The aim of the doctoral thesis is to determine the challenges of commonly used high frequency isolated DC/DC converters nowadays and to propose three new power electronic building blocks (PEBB-s) for the low voltage side of the isolation stage in order to optimize the voltage and power regulation. One of the most widely used DC/DC topology nowadays is the dual active bridge (DAB). The DAB has good power control capabilities but it lacks the voltage regulation properties. The proposed PEBB-s allow us to simultaneously regulate the voltage and the power level by means of the improved modulation method. The voltage step-up is achieved by simultaneous turn-on of the inverter switches on the low voltage side. During this state the energy is stored in the filter inductances and later directed to the output.

The proposed PEBB-s are: i) current doubler rectifier with bi-directional power flow capability; ii) quasi-Z source based inverter; iii) current-fed DC/DC converter with active clamp. The combination of the proposed PEBB and the traditional voltage source inverter results in the new topologies, where the switches on both sides of the bridges are controlled simultaneously.

In the thesis the mathematical models of the proposed PEBB-s are presented. The conduction losses, switching losses, component voltage and current stress are analyzed analytically and experimentally. The operating principle of the proposed PEBB-s was verified with the simulations and experimentally. The results have shown that the proposed PEBB-s have good voltage control capabilities, they can reduce the current and voltage stress on the components, that in turn results in smaller switching losses. In addition, the thesis presents the design guidelines for the proposed PEBB-s. These guidelines can be used in the circuit design of the PEBB-s for the applications, where the voltage regulation range is necessary, for example to connect the battery with the electrical bus with a higher voltage.

Kokkuvõte

Jõuelektroonilise trafo isolatsioonilüli uudsete topoloogiate uurimine ja arendamine

Kaasaegne elektrisüsteem koosneb põhivõrgust, jaotusvõrgust ning tarbijatest, kus elektrienergia voog kulgeb tootjatelt tarbijatele. Elektrivõrk täieneb pidevalt uute taastuvenergiaallikatega (nt tuulegeneraatorid, päikesepaneelid jm), aga ka salvestusseadmetega (nt patareid, vesinikpuhvrid, veepumbajaamad jm). Lisaks sellele toodavad kasutajad elektrienergiat lokaalsetest taastuvenergiaallikatest ning suunavad vajadusel toodetud energia võrku tagasi. Sellises süsteemis on energiavoogude liikumine kahesuunaline, nii tootjatelt tarbijatele kui ka vastupidi. See seab kindlad nõudmised elektrivoogude juhtimisele, millega kaasaegne elektrisüsteem hakkama ei saa. Selle probleemi lahendamiseks on välja pakutud jõuelektroonilise trafo kontsept, mis tagaks galvaanilise eralduse erinevate võrguosade vahel ning suudaks korraga teostada nii pinge muundamist, energiavoogude kontrolli kui ka elektrienergia kvaliteedi parendamist.

Võrreldes tänapäeval kasutatavate madalsagedustrafodega omab jõuelektroonniline trafo väiksemaid mõõtmeid ning kaalu, ei vaja muid lisaseadmeid ning isoleerib sisendi- ja väljundipoolseid häiringuid üksteisest. Mõõtmete vähenemine on saavutatud tänu kõrgsagedusliku ($f \geq 1$ kHz) isolatsioonilüli kasutamisele, mis võimaldab saavutada vajaliku võimsustiheduse väiksema trafo südamiku korral. Kõige perspektiivsemaks loetakse tänapäeval kolmeastmelist jõuelektroonilist trafot. See koosneb juhitavatest sisendist ja väljundist, kahest erineva pingega alalispingesiinist ning isolatsioonilülist. Isolatsioonilüli on jõuelektroonilise trafo võtmeelemendiks, kuna seal toimub kõige olulisema tähtsusega pinge muundamise protsess. Siit võib järeldada, et isolatsioonilüli määrab suuremas osas ära kogu jõuelektroonilise trafo gabariidid, kasuteguri ning üleüldise jõudluse. See asjaolu teeb isolatsinoonilülist huvitava uurimisobjekti.

Isolatsioonilüli saab jagada kaheks jõuelektroonika funktsioonplokiks ja kõrgsagedustrafoks. Jõuelektroonika funktsioonploki all mõistetakse jõuelektroonika muundurit. Käesolevas doktoritöös uuritakse isolatsioonilüli topoloogiaid. Välja pakutakse kolm uut jõuelektroonika funktsioonplokki (muundurit), mis võimaldavad optimeerida energia muundust. Väga võimsates muundurites kasutatakse tänapäeval kõige laialdasemalt aktiivset täissilda (*Dual Active Bridge*). Paraku puudub sellel topoloogial pinge reguleerimise võimalus, mistõttu on selle funktsionaalsus pinge kõikumiste korral piiratud. Uued väljapakutud jõuelektroonika funktsioonplokid võimaldavad stabiliseerida toitepinget ning juhtida võimsust kasutades faasinihke modulatsiooni (*phase shift modulation*). Pinge tõstmine käib erilise lühisoleku abil, mis saavutatakse vaheldi lülitite samaaegsel sisselülitamisel, mille tulemusena salvestub energia alalisvooluvahelülis asuvasse filtrisse. Doktoritöö autori poolt väljapakutud

jõuelektroonika funktsioonplokkideks on: i) kahesuunaline voolukordistil baseeruv pinget tõstev muundur, ii) kvaasiimpedants-allikaga pinget tõstev muundur, iii) pinget tõstev alalispingemuundur aktiivse summutusahelaga (*active-clamp*).

Kõigi kolme uudse topoloogia kohta on koostatud matemaatilised mudelid, juhtivus- ja lülituskadude analüüs, komponentide pinge ja voolu taluvuse analüüs. Topoloogiate tööpõhimõte on kontrollitud nii modelleerides kui ka katseliselt. Tulemused näitasid, et väljapakutud uued topoloogiad on heade pinget kordistavate omadustega, nad alandavad komponentide pinge ja voolu taluvuspiiri, mis omakorda vähendab lülituskadusid. Selle tulemusena laieneb muundurite juhtimisvahemik.

Lisaks sellele on koostatud projekteerimismetoodika voolukordisti dimensioneerimiseks ning komponentide valimiseks, samuti arvutusvalemid teiste topoloogiate elementide dimensioneerimiseks. Voolukordisti jaoks koostatud projekteerimis-metoodikat võib kasutada rakendustes, kus väga lai pinge reguleerimise vahemik on vajalik nt. akude ühendamine kõrgepingeliste seadmetega.

Elulookirjeldus

1. Isikuandmed
   Ees- ja perekonnanimi: Viktor Beldjajev
   Sünniaeg ja -koht: 25.12.1985, Tallinn
   Kodakondsus: Eesti

2. Kontaktandmed
   Aadress: Võsa 33-9, Rapla 79514, Eesti.
   Telefon: +37253322442
   E-posti aadress: vbeldjajev@gmail.com

3. Hariduskäik

Õppeasutus (nimetus lõpetamise ajal)	Lõpetamise aeg	Haridus (eriala/kraad)
Tallinn Tehnikaülikool	2009	Elektriajamid ja jõuelektroonika, Tehnikateaduse magistri kraad
Giessen-Friedbergi Rakenduskõrgkool	2009	Automaatika, Diplomeeritud inseneri kraad.
Tallinn Tehnikaülikool	2008	Elektriajamid ja jõuelektroonika, Tehnikateaduste bakalaureuse kraad
Rapla Vesiroosi Gümnaasium	2004	Keskharidus

4. Keelteoskus (alg-, kesk- või kõrgtase)

Keel	Tase
Vene keel	Kõrgtase
Eesti keel	Kõrgtase
Inglise keel	Kõrgtase
Saksa keel	Kõrgtase
Soome keel	Kesktase

5. Täiendusõpe

Õppimise aeg	Täiendusõppe läbiviija nimetus
2009 - 2013	Tallinna Tehnikaülikool, Eesti
2010	RWTH Aachen University, Saksamaa
2009	Stralsund University, Saksamaa

6. Teenistuskäik

Töötamise aeg	Tööandja nimetus	Ametikoht
2010 -...	ABB LV Drives, Jüri, Eesti	Vaneminsener
2008 - 2010	Tallinna Tehnikaülikool	Doktorant
2008	ABB Flexible Automation GmbH, Friedberg, Saksamaa	Praktikant
2007	LUST Antriebstechnik GmbH, Lahnau, Saksamaa	Praktikant
2006	EAAT GmbH, Chemnitz, Saksamaa	Praktikant

7. Teadustegevus
   - Optimaalne energiamuundamine ja juhtimine tark- ja kohtvõrkudes.
   - Intelligentne trafo – talitlusrežiimide analüüs (ETF8687).
   - Aktiivsete elektrijaotusvõrkude muundurite topoloogiad ja juhtimismeetodid (SF0140016s11).
8. Kaitstud lõputööd

   Magistritöö: Robotsüsteem tööstusrobotiga IRB1600, 2009 a. Juhendajad: Prof. Tõnu Lehtla (Tallinna Tehnikaülikool), Prof. Marius Klytta (Giessen-Friedbergi Rakenduskõrgkool, Saksamaa).

Curriculum Vitae

1. Personal data
   Name: Viktor Beldjajev
   Date and place of birth: 25.12.1985, Tallinn.

2. Contact information
   Address: Võsa 33-9, Rapla 79514, Estonia.
   Phone: +37253322442
   E-mail: vbeldjajev@gmail.com

3. Education

Educational institution	Graduation year	Education (field of study/degree)
Tallinn University of Technology	2009	Electrical Drives and Power Electronics Master of Science
University of Applied Sciences Giessen-Friedberg	2009	Automation Diploma-Engineer
Tallinn University of Technology	2008	Electrical Drives and Power Electronics Bachelor of Science
Rapla Vesiroosi Grammar School	2004	Secondary education

4. Language competence/skills (fluent; average, basic skills)

Language	Level
Russian	Fluent
Estonian	Fluent
English	Fluent
German	Fluent
Finnish	Average

5. Special Courses

Period	Educational or other organization
2009 - 2012	Tallinn University of Technology, Estonia
2010	RWTH Aachen University, Germany
2009	Stralsund University, Germany

6. Professional Employment

Period	Organisation	Position
2010 -...	ABB LV Drives, Jüri, Estonia	Senior engineer
2008 - 2010	Tallinn University of Technology	Doctoral student
2008	ABB Flexible Automation GmbH, Friedberg, Germany	Trainee
2007	LUST Antriebstechnik Gmbh, Lahnau, Germany	Trainee
2006	EAAT GmbH, Chemnitz, Germany	Trainee

7. Scientific work
   - Optimal energy conversion and control in smart and microgrids.
   - Intelligent Transformer – Analysis of Operating Modes (ETF8687).
   - New Converter Topologies and Control Methods for Electronic Power Distribution Networks (SF0140016s11).
8. Defended theses

   Master of science thesis: Robot system with industrial robot IRB 1600, 2009, Supervisors: Prof. Tõnu Lehtla (Tallinn University of Technology), Prof. Dipl. Ing. Marius Klytta (Giessen-Friedberg University of Applied Sciences, Germany).

Appendix

[PAPER-I] **Beldjajev, V**., Roasto, I. State of the art trends and design challenges of power electronic transformer for future distribution grids. Технічна електродинаміка, Alushta, Ukraine, 17-22 September 2012, pp. 55 – 62.

STATE OF THE ART TRENDS AND DESIGN CHALLENGES OF POWER ELECTRONIC TRANSFORMER FOR FUTURE DISTRIBUTION GRIDS

V.Beldjajev, I.Roasto
Tallinn University of Technology
Ehitajate Tee 5, 19086, Tallinn, Estonia
E-mail: vbeldjajev@gmail.com, indrek.roasto@ieee.org

Аннотация **– Конструкция традиционного трансформатора отличается крупными габаритами и большим весом. Также, данные трансформаторы обладают повышенной чувствительностью к гармоникам и имеют ряд других недостатков. Альтернативным решением может быть трансформатор на силовой электронике, который имеет управляемые вход и выход, гальваническую развязку, пользовательский интерфейс, а также встроенные функции, позволяющие управлять энергопотоками, отслеживать состояние системы и многое другое.**

Ключевые слова **– силовой трансформатор, силовой преобразователь, качество электроенергии, разпределительная сеть**

INTRODUCTION

The distribution transformers are one of the fundamental and indispensable components in power distribution systems. Their cost is relatively inexpensive, they are highly reliable and fairly efficient. However, heavy weight, large volumes, harmonics sensitivity, voltage drops under load and environemental issues regarding mineral oil, are serious drawbacks of these transformers. Growing number of renewable energy sources results in rising number of distributed power plants and non-linear loads which are principally subject to substantial energy fluctuations [1], [2]. Such sources have negative impact on the power quality in the medium voltage (MV) and low voltage (LV) power distribution network [3]. Many distributed generation sources cannot be connected directly to the AC systems, hence they require power electronic interface. To easily connect these new energy sources to the grid and improve the power quality by harmonic filtering, voltage sag correction, dynamic control of the power flow etc., a new power electronic transformer is required (PET).

PET is a new type of transformer based on the power electronic conversion, that aims to better voltage regulation, power transmission, isolation and power quality improvement of the grid. The basic idea behind the PET is to use medium or high frequency (f > 1 kHz) transformer instead of a traditional low frequency (50 Hz) distribution transformer. As the power throughput density of the transformer is inversly proportional to frequency, hence increasing the frequency allows better utilization of the steel magnetic core and reduction in transformer size [4].

Compared with conventional transformer, the PET is pursuing smart control feature by power electronic (PE) converters, HF transformer and comprehensive controlling technology. It can include built-in functions of diagnostics, protection (overvoltage, undervoltage, short circuit etc), flexible adjustment and convenient communication with the grid. It enables full control of the magnitude and direction of real and reactive power without additional power transformer and frequency conversion equipment [5], [6], [7].

Advantages of PET over the LFT include the fact, that output voltges are sinusoidal regardless of the input power quality or the output current waveshape.

This is because the controls on the output stage actively suppress output voltage harmonics thus preventing their penetration to the input side. In addition, current limiting at the output and input stages is readily used

to prevent secondary faults from propagating through the transformer.

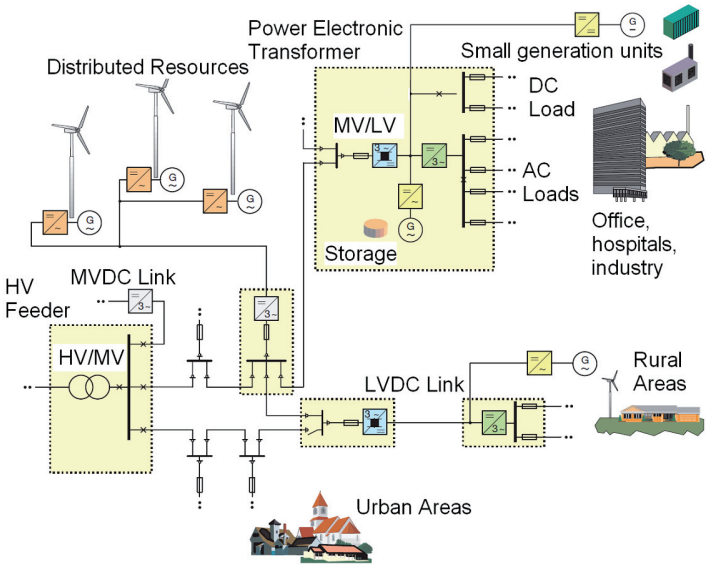


Fig. 1. MV distribution grid with DC subsystems and LV grid [12].

In addition, PET offers a good ride-through capability during the voltage sags on the MV side and equipped with battery it can provide energy during the periods when the main grid is not available (e.g. in islanding mode of microgrid). If connected in parallel with a LFT, PET can provide equal load division between the transformers that results in the elimination of the circulating reactive current between them [8].

Although the idea of PET was already mentioned in the 1980s, the available semiconductors at that time were not able to switch high powers with high switching frequency. During the last decade the highly reliable, low loss SiC based semiconductors with high switching capability and lower cost have been available on the market, thus it is expected that PE based solutions will penetrate the MV distribution network [9], [10].

Although the design of PET is considerably more expensive than that of a conventional LFT and currently less efficient (efficiency of LFT typically > 97 %), falling costs and improved performance of semiconductors will enable the design to be economical in the future [11]. An example of the PET in the distribution grid including distributed energy sources, energy storage devices and different type of loads is shown in Fig. 1.

BASIC REQUIREMENTS

As a complete DC distribution system will not be available in the near future, the PET will operate in the already existing AC MV and LV grid. Thus, the PET has to be adotable to existing MV and LV levels worldwide. The existing MV and LV ratings (based on IEC 60038) in the Europe and North-America are shown Table 1 and Table 2. An overview of the most relevant power ratings with nominal current according to the IEC 60076 is given in [3].

Table 1. Existing medium voltage ratings

Location	**Voltage (kV)**				
Europe	3.6	7.2	12	17.5	24
America	4.75	8.25	15	25.8	

Table 2. Existing low voltage ratings

Rated Low voltages (V)				
100/ 200	120/ 208	110/ 220	127/ 220	120/ 240
230/ 400	277/ 480	347/ 600	400/ 690	

IEC 60038 restricts the tolerance of ± 10 % of the nominal voltage in 230/400 and 400/690 systems must be guaranteed [3].

The transformer provides galvanic isolation between two sides of the grid and suppresses the leakage currents. Accordingly, many standards have been deployed to set maximum allowed leakage current. For instance, the German DIN VDE 0126-1-1 mandates that a leakage current of 30mA necessitates the disconnection of the inverter from the grid within 0.3 second. Other standards, such as IEEE 929-2000, IEC 61727, IEEE 1547, and EN 61000-3-2 have set the maximum DC current injected to the grid to be between 0.5 % and 1%. From the power quality point of view, standards such as the IEC61000-3-2 and the IEEE 519-1992 [13], [14] have set the THD level to less than 5%.

Many standards have been deployed to set allowed deviation ranges of voltage and current parameters from their nominal values to maintain the required power quality in the grid. Table 3 presents the tolerances of the sources and the loads influenced by the voltage parameter. Table 4 presents the range of load current and the susceptibility of the power sources influenced by the current parameter [15].

Typical range of power sources frequency according to [15] is +/- 1 % which also corresponds to the immunity of the electronic loads.

Table 3. Matching load and power source requirements

Voltage parameter	Range of power sources	Immunity of loads
Overvoltage	+ 6 %	+10 %
Undervoltage	-13.3 %	-15 %
Swell/sag	+10 / -15 %	+20 / -30 %
Transients	100 – 6000 V	500 – 1500 V
THD_U	5-50 %	5 – 10 %
Phase unbalance	2 – 10 %	Max 5 %
EMI	10 V up to 200 kHz	3 V

Another important requirement is set for the voltage and current unbalances of the phases that can result in adverse effects on equipment and on the power system. Under such conditions the power system will incur more losses and heating effects and be less stable due to load transfers [16], [17]. The International Electrotechnical Commission (IEC) recommends the maximum voltage unbalance of electrical suppy system to be limited to 2 % [18]. The American National Standards Institute (ANSI) standard C84.1-1995 recommends that electrical supply systems should limit the voltage unbalance to 3 % under no load condition [19].

Table 4. Matching load and power source requirements

Parameter	Load current	Susceptibility of sources
Power factor	0.85 - 0.6	0.8
DC current	Negligible to 5%	< 1 %
Ground current	0 – 10 A rms	> 0.5 A

PET must also be able to withstand such disturbances like voltage transients, load step, inrush current, fault current, voltage regulator interactionsetc.

REVIEW OF TOPOLOGIES

Many existing topologies for do not support the bi-directional power flow, that is a major requirement for replacing the LFT in the distribution grid. Other important requirements comprise galvanic isolation capability, capability of interconnecting renewable energy sources and energy storage devices.

A good approach to classify PET topologies was introduced in [1], [20] and [21]. According to this classification four basic topology principles of the PET can be distinguished:

a) single-stage topology with direct AC-to-AC conversion,

b) two-stage topology with LVDC link,

c) two-stage topology with MVDC link,

d) three-stage topology with MVDC and LVDC links.

The configuration of these topologies is shown in Fig. 2 [20].

Single-stage topologies comprise direct AC-AC conversion. One AC-AC single stage topology with a full bridge converter and a HF transformer was introduced in [21], [22].

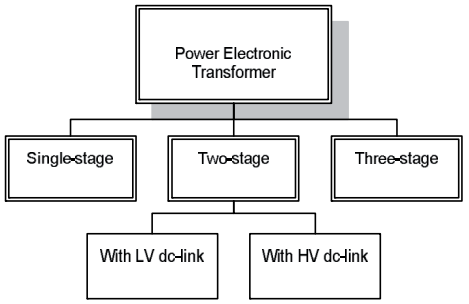


Fig. 2. Classification of PET topologies

A. Single stage topologies

B.

In addition, couple of matrix converter based topologies have been proposed in [23], [24] and research on different matrix converters has been done in [25]. Another cycloconverter based topology with self-commutated switches was proposed in [26]. Although this is the most straightforward approach to AC-AC power conversion, it is problematic, since each switch must be able to block full primary voltage and also be capable of conducting full secondary current [11]. Lack of the DC link in the single stage topologies is a major drawback, thus integration of the storage elements and power factor correction circuit would require additional devices which in turn make the system complicated, increase the size and cost of the overall system.

C. Two-stage topologies

In two-stage topology, the low frequency is directly converted to high frequency AC and rectified back to DC on the transformer secondary. Then it is converted to 50 Hz output voltage using PWM inverter. The switches on the high voltage side must be four-quadrant to withstand bi-polar voltages and currents. A disadvantage of this DC-DC version is the use of two different controls depending on the direction of the power flow [20].

Use of a dual active bridge (DAB) in the two-stage topology would provide seamless control of the power in both direction and zero voltage switching capability for a wide load range. The disadvantages of this topology are high sensitivity of the average active power flow to leakage inductance variation and the large ripple currents [23]. Also, the reactive power compensation feature is complicated on the MV side. Two-stage topologies with MVDC link do not allow interconnecting the storage elements directly to the PET, thus this topology is not suitable for the PET.

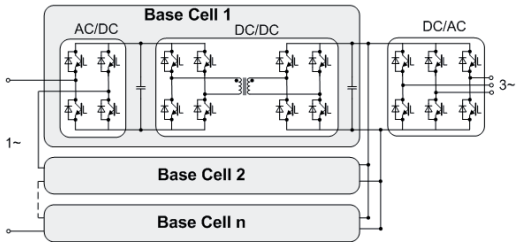


Fig. 3. Three-stage topolgy of PET with series connected base cells and common inverter

D. Three stage topologies

Three stage topologies enable several functions that are desirable to PET [27] - [32]. Three-stage topology consists of the three power conversion stages: the input stage, the isolation stage and the output stage. The input stage rectifies the MV AC forming this way a MV DC-link. In the isolation stage, the DC-DC conversion takes place. The MVDC is converted into high frequency squarewave AC voltage and transferred to the HF transformer, where the voltage level is reduced and rectified again to a LV DC side, forming this way a LV DC-link. LVDC is converted to back 50 Hz AC in the output stage. Schematic of this topology is shown in Fig. 3.

According to research in [1], [20] and [21] the three-stage topology seems to be the most advantageos one among the others. Presence of two different voltage level DC links allows interconnecting the energy storage devices and renewable energy sources into one system without additional converters. Integration of power-factor-correction and isolated DC-DC converters lead to lower losses and consequently improved efficiency

In the high voltage applications the three-level circuit on the MV side can significantly reduce the stress ratings of the components and improve the efficiency,

moreover the harmonics will be reduced either.

DESIGN CHALLENGES

A. Modular design of PET

Based on today's available power levels of PE components two approaches to PET design are considerable. First is to use the multilevel converter with each base cell equipped with standard components (no series connection of semiconductors) and one high frequency transformer per base cell. Such approach results is a high number of series connected base cells on the high voltage side (e.g. 20 series connected converters at a primary AC voltage of 24kV, 3 phases). Second approach consists of utilizing the series connection of the semiconductors inside one base cell (e.g. two or three converters instead of 15-20 with multilevel approach). This in turn results in a lower amount of HF transformers per base cell. The number of series converters depends on the voltage levels and the type of semiconductors [30]. A difficult control of series-tied and parallel tied devices, that must be fully synchronized, is an important drawback, which can result in an inability to correct the power factor and additional voltage oscillations.

B. Input stage

Input stage of the PET consists of an active front-end rectifier with a unity power factor circuit. By controlling the active rectifier the input current and voltage levels can be adjusted accordingy to the specified requirements. The plurality of input stage modules can be used to achieve effective switching frequency, that can reduce the switching losses of the input stage. Another advantage of the multilevel converters (MLC) is the possibility to reduce the switching losses by reducing the switching frequency without increasing the voltage harmonics. Active front-end acts like a static var comensator (SVC) and reduces the reactive power and total harmonic distortion on the grid side. To guarantee a sinusoidal input current and a stabilized MV DC-link voltage for the input stage, a topology with a voltage boost characteristics is necessary. In this case, a low number of MV DC-link levels would be sufficient to cover all MV levels worldwide [3].

C. Isolation stage

Isolation stage is a controllable DC-DC converter where the voltage reduction and galvanic insulation take place. Isolation stage is responsible for providing the required DC voltage levels on the input and output side DC links and managing the bi-directional power flow. Typically the biggest losses occur in the isolation stage, because it comprises, beside conduction and switching losses, core losses of the HF transformer. For this reason the isolation stage determines the overall efficiency of the PET, hence making the isolation stage an interesting research objective.

Different multilevel, dual active bridge, half bridge, current doubler rectifier based topologies have been proposed for the isolation stage [20], [21], [27], [28]. DC link type topologies are the must promising ones, even though the research in [29] shows the transformer core losses are expected to be bigger in the DC-link type converters rather than in the direct ac-ac type converters. To minimize the losses, the duty cycle and switching frequency can be adjusted accordingly to the function of the load. In case of the dual active bridge based topologies the power flow can be controlled by setting the phase shift of the two square wave voltages of the VSC on each side of the HF transformer.

D. Output stage

Output stage is also an active front-end that can control the voltage level of the LVDC link in case of reverse energy flow. Typically on the low voltage side, using the two level topologies can meet all the requirements concerning voltage stress on the semiconductors. In typical applications the output stages are connected in parallel to provide the necessary current to the consumers. In addition, low voltage DC-link enhances the ride-through capability of the PET [30].

E. Semiconductors

Research in [3] states that the usage of fast switching semiconductors with lower voltage blocking capability is more favorable and more future oriented compared to low speed high voltage blocking semiconductors (HV-IGBT, GTO). Such systems require lower number of converter stages what results in lower system costs and higher reliability [1]. Such SiC JFETs can switch several kilovolts in less than 100 ns with operating frequencies of several tens of kilohertz. Research in [1] states that using that type of switches the 97 % efficiency of a 1 MW PET can be achieved..

CONTROL PRINCIPLES

The three different stages of the PET are controlled independently from the others. The main tasks of the input stage are shaping the input current, controlling the power factor, reducing the harmonic content and keeping the DC link voltage at the reference value. It is of high importance to keep the equal voltage distribution among the series connected base cells, as slight differences in switch characteristics and stray capacitances can lead to unwanted scaling effects. An additional expenditure of providing a synchronization of all PWM controlled converters is necessary, because even a small difference in switching frequencies of the modules can cause subharmonic oscillations in the input and output characteristics of the PET.

The primary control objective for the output inverter is to superimpose the required active power to the grid and regulate the voltage on the output. In case when grid is operating autonomously (e.g. islanding mode) the control must also establish the frequency [2].

The controller of the parallel-output stage must control the output voltage and current sharing among the base cells that can be disturbed due to the mismatches between the base cells. The main sources of mismatching are the turn's ratio of the HF transformers, input voltage DC offset, cells equivalent resistance. Such mismatch can cause problems in thermal management and life time of parallel converters. If the two grids are connected through the PET, their operation does not have to be synchronous as it is in case of the LFT.

A feasible control method of the PET was proposed in [32]. It consists of a digital controller for voltage balance monitoring, and an analog controller to regulate the sum of the base cell voltages. In order to achieve highest efficiency the voltages on the DC link need to be hold on constant level with the control of the input stage. The secondary DC-link voltage is controlled by the power flow through the transformer. To realize the constant DC voltage and keep input current sinusoidal, the DC voltage outer loop and AC voltage inner control loops may be used [34].

The power factor correction module is a compulsory feature for the PET, since major of the existing loads in the distribution grid operate with lagging power factor in the range between 40… 90 % [35]. The power factor correction (PFC) module is integrated to the input side of the isolation stage and utilizes the MVDC link capacitor. In case of modular design, each input stage module must consist of a unity power factor active rectifier. The PFC programs the input current waveforms and adjusts the power factor on the MV side to be near one. For performing the power factor correction different methods exist: variable hysteresis control, peak current control and average current control [30]. The main disadvantage of the variable hysteresis control is that it operates at variable switching frequency. Disadvantage of the peak current control generates some distortion in the input current inherently. Thus average current control seems to be most appropriate for the PET.

ACKNOWLEDGMENT

This research and work has been supported by Estonian Ministry of Education and Research (Project SF0140016s11) and Estonian Science Foundation (Grant ETF8687).

SUMMARY

The PET is a new type of transformer that offers various advantages over traditional transformer. In order to replace LFT in the distribution grid, the PET must correspond to the power quality requirements that are nowadays valid for the LFT. Three-stage topology of the PET seems to be the most promising one due to the presence of two DC link and enhanced PFC possibilities. A modular design of PET is necessary to overcome the voltage stress problem on the MV side.

[1] D. Aggeler J. Biela J.W. Kolar , „Solid-State Transformer based on SiC JFETs for Future Energy Distribution Systems“, *Proceedings of the Smart Energy Strategies Conference (SES'08), Zurich, Switzerland, Sep. 8 - 10, 2008* .

[2] Hiskens, I.A.; Fleming, E.M.; , "Control of inverter-connected sources in autonomous microgrids," *American Control Conference, 2008* , vol., no., pp.586-590, 11-13 June 2008

[3] Heinemann, L.; Mauthe, G.; , "The universal power electronics based distribution transformer, an unified approach," Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual , vol.2, no., pp.504-509 vol.2, 2001

[4] E. Ronan, S. D. Sudhoff, S . F. Glover and D. L. Galloway, “Application of Power Electronics to the Distribution Transformer,” Conference Record of APEC 2000, New Orleans, February, 2000, pp. 861-867.

[5] Madhav D. Manjrekar, Rick Kieferndorf, Giri Venkataramanan. Power Electronic Transformers for Utility Applications[C]. Proceedings of the 2000 IEEE-IAS Annual Meeting, 2000, 4:2496 -2502

[6] Edward R. Ronan , Scott D. Sudhoff, Steven F.Glover. A Power Electronic-based Distribution Transformer[J]. IEEE Transactions on Power Delivery, 2002, 17(2):537-543

[7] Wang Hui; Tan Xing-guo; Li Qing-min; Zhou Fei; Deng Zhan-feng; Li Zhen-he; Lu Nan; , "Development and applicability analysis of intelligent solid state transformer," *Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), 2011 4th International Conference on* , vol., no., pp.1150-1154, 6-9 July 2011

[8] Haibo Liu; Chengxiong Mao; Jiming Lu; Dan Wang; , "Parallel operation of electronic power transformer and conventional transformer," *Electric Utility Deregulation and Restructuring and Power Technologies, 2008. DRPT 2008. Third International Conference on* , vol., no., pp.1802-1808, 6-9 April 2008

[9] W. Leonard, “Power Electronics and Control by Microelectronics in Future Energy Systems”, EPE Journal, April 2000

[10] Electric Power Research Institute (EPRI), “Electricity Technology Roadmap, Powering Progress”, July 1999

[11] Ronan, E.R.; Sudhoff, S.D.; Glover, S.F.; Galloway, D.L.; , "A power electronic-based distribution transformer," *Power Delivery, IEEE Transactions on* , vol.17, no.2, pp.537-543, Apr 2002

[12] L. Heinemann, G. Mauthe, J.-J. Maillet, M. Hellum; “Power Quality, The New Paradigm for MV Power Distribution”; ABB Review 03-2000

[13] T. Salmi, M. Bouzguenda, A. Gastli, A. Masmoudi; „A Novel Transformerless Inverter Topology Without Zero Crossing Distortion“. internationa Journal of Renewable energy Reseacrh-IJRER , vol. 2, no. 1, 2012.

[14] "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems," *IEEE Std 519-1992* , vol., no., pp.0_1, 1993

[15] "IEEE Recommended Practice for Powering and Grounding Electronic Equipment," *IEEE Std 1100-1999* , vol., no., pp.0_1, 1999

[16] Kotsopoulos, A.; Heskes, P.J.M.; Jansen, M.J.; , "Zero-crossing distortion in grid-connected PV inverters," *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]* , vol.2, no., pp. 1101- 1106 vol.2, 5-8 Nov. 2002

[17] von Jouanne, A.; Banerjee, B.; , "Assessment of voltage unbalance," *Power Delivery, IEEE Transactions on* , vol.16, no.4, pp.782-790, Oct 2001

[18] EPRI Power Electronics Applications Center, “Input performance of ASDs during supply voltage unbalance,”, Power quality testing network PQTN Brief no. 28, 1996.

[19] *Electric* Power Systems *and Equipment—Voltage Ratings (60 Hertz)*, ANSI Standard Publication no. ANSI C84.1-1995.

[20] Beldjajev, V.; Roasto, I.; Lehtla T.; , “Intelligent Transformer: Possibilities and Challenges” RTU, 2011. , pp . 14 Okt 2011.

[21] Falcones, S.; Xiaolin Mao; Ayyanar, R.; , "Topology comparison for Solid State Transformer implementation," *Power and Energy Society General Meeting, 2010 IEEE* , vol., no., pp.1-8, 25-29 July 2010.

[22] M. Kang, P.N. Enjeti, and I.J. Pitel, “Analysis and design of electronic transformers for electric power distribution systems,” in IEEE Trans. on Power Electronics, vol. 14, no.6, pp. 1133-1141, Nov. 1999.

[23] Mirmousa, H.; Zolghadri, M.R.; , "A Novel Circuit Topology for Three-Phase Four-Wire Distribution Electronic Power Transformer," Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on , vol., no., pp.1215-1222, 27-30 Nov. 2007.

[24] Nath, S.; Mohapatra, K.K.; Basu, K.; Mohan, N.; , "Source based commutation in matrix converter fed power electronic transformer for power systems application," *Power Electronics Electrical Drives Automation and Motion (SPEEDAM), 2010 International Symposium on* , vol., no., pp.1682-1686, 14-16 June 2010

[25] Basu, K.; Gupta, R.K.; Nath, S.; Castelino, G.F.; Mohapatra, K.K.; Mohan, N.; , "Research in matrix-converter based three-phase power-electronic transformers," *Power Electronics Conference (IPEC), 2010 International* , vol., no., pp.2799-2803, 21-24 June 2010

[26] Wrede, H.; Staudt, V.; Steimel, A.; , "Design of an electronic power transformer," *IECON 02 [Industrial Electronics Society, IEEE 2002 28th Annual Conference of the]* , vol.2, no., pp. 1380- 1385 vol.2, 5-8 Nov. 2002

[27] Hengsi Qin; Kimball, J.W.; , "A comparative efficiency study of silicon-based solid state transformers," Energy Conversion Congress and Exposition (ECCE), 2010 IEEE , vol., no., pp.1458-1463, 12-16 Sept. 2010.

[28] Beldjajev, V.; Roasto, I.; Vinnikov, D.; , "Analysis of current doubler rectifier based high frequency isolation stage for intelligent transformer," *Compatibility and Power Electronics (CPE), 2011 7th International Conference-Workshop* , vol., no., pp.336-341, 1-3 June 2011

[29] Manjrekar, M.D.; Kieferndorf, R.; Venkataramanan, G.; , "Power electronic transformers for utility applications," *Industry Applications Conference, 2000. Conference Record of the 2000 IEEE* , vol.4, no., pp.2496-2502 vol.4, Oct 2000

[30] Iman-Eini, H.; Farhangi, S.; , "Analysis and Design of Power Electronic Transformer for Medium Voltage Levels," *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE* , vol., no., pp.1-5, 18-22 June 2006

[31] Bhattacharya, S.; Tiefu Zhao; Gangyao Wang; Dutta, S.; Seunghun Baek; Yu Du; Parkhideh, B.; Xiaohu Zhou; Huang, A.Q.; , "Design and development of Generation-I silicon based Solid State Transformer," Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE , vol., no., pp.1666-1673, 21-25 Feb. 2010.

[32] Iman-Eini, H.; Schanen, J.; Farhangi, S.; Barbaroux, J.; Keradec, J.; , "A power electronic based transformer for feeding sensitive loads," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE* , vol., no., pp.2549-2555, 15-19 June 2008

[33] Banaei, M.R.; Salary, E.; , "Power quality improvement based on novel power electronic transformer," Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2011 2nd , vol., no., pp.286-291, 16-17 Feb. 2011

[34] D. Wang, C. Mao, J. Lu, S. Fan, F.Z. Peng, “Theory and application of distribution electronic power transformer,” Electric. Power Syst. Res, vol. 77, pp. 219–226, March 2007

[35] Tinggren, R.; Yi Hu; Le Tang; Mathews, H.; Tyner, R.; , "Power factor controller-an integrated power quality device," *Transmission and Distribution Conference, 1999 IEEE* , vol.2, no., pp.572-578 vol.2, 11-16 Apr 1999

[PAPER-II] **Beldjajev, V**., Roasto, I., Lehtla, T. Intelligent Transformer: Possibilities and Challenges. Scientific Journal of Riga Techical University: Power and Electrical Engineering, Vol. 4, No. 29, 2011, Latvia, pp. 95 – 100.

Intelligent Transformer: Possibilities and Challenges

Beldjajev Viktor (*Doctoral student, Tallinn University of Technology),*
Roasto Indrek (*Senior researcher, Tallinn University of Technology),*
Lehtla Tõnu *(Professor, Tallinn University of Technology).*

Abstract – This paper covers the concept of an intelligent transformer that is a good candidate to replace a conventional low frequency transformer in the microgrids. As the power production and consumption can vary in a wide range, the new substations have to meet many requirements to guarantee reliable energy management in the autonomous networks. Different topologies of intelligent transformers can be used to meet these requirements. Therefore the advantages and disadvantages of the existing topologies were analyzed. The future trends and challenges are also discussed.

***Keywords* – Intelligent transformer, high-frequency transformer, microgrid, power electronic converter,**

I. Introduction

Initial years of electric distribution have seen heavy discussions between the DC and AC system proponents. The DC system supported by Thomas Edison was attributed considerable advantages over the AC system e.g. easy integration of energy backup devices, no need for reactive power compensation. On the other hand, the voltage in DC systems was hard to control while AC systems provided an easy way for voltage regulation. The AC system uses the magnetically coupled transformer concept for voltage elevation, transmission over long distances and reduction for residential use. Traditional line-frequency-transformer (LFT) has simple construction, high efficiency and reliability. Moreover, it provides galvanic isolation as well. During the last decade, the basic construction has remained the same, but the improved material technology allowed higher saturation densities and lower hysteresis losses to be achieved, which resulted in very efficient transformers. The efficiency of LFT is considered to be 97 %.

However, LFT is very bulky and heavy. It transforms the voltage directly transferring this way also the unwanted voltage sags, dips and frequency variations to the output. LFT has a very limited voltage and power quality regulation and needs additional flexible AC transmission systems (FACTS) for power quality control. Since the optimal performance of the LFT is designed to be near the full-load, it has high losses in under-load or no-load conditions, also under dc-offset unbalances [1]. In nowadays centralized grid, the LFT meets most of the requirements concerning cost, the efficiency and reliability. However, centralized generating facilities are giving way to smaller, more distributed generation. Thus, it is likely that future power generation and distribution will involve numerous distributed renewable energy sources and micro grids. In order to effectively interconnect power generation and energy storage into a grid or micro grid intelligent energy management (IEM) is needed. IEM substations should have bi-directional energy flow control capability, intelligent control and communication interface. Clearly, traditional low frequency (50 Hz) distribution transformers are not suitable for such demanding applications.

To meet the requirements of the future intelligent network management systems a new concept of a distribution transformer is needed. One possibility is to implement an intelligent transformer (ITR). The ITR was proposed already in the 1980's as an alternative to the LFT for voltage transformation [2]. The ITR, also known as a power electronic transformer or a solid state transformer is a new type of transformer that realizes voltage transformation, galvanic isolation and power quality enhancements in a single device. Its role is to enable active management of distributed energy resources, energy storage devices and different types of loads (domestic or industrial) in the distribution grid. The basic idea behind the ITR is to use a high frequency ($f > 1$ kHz) transformer instead of a traditional low frequency (50 Hz) distribution transformer. Increasing the frequency allows higher utilization of the magnetic core and reduction in the size of the transformer.

The advantages of this concept were clear, even though the technology for proper demonstration did not exist at that time. The weight and volumes can be up to three times smaller compared to the corresponding LFT due to the use of high frequency. Bi-directional energy flow capability allows connecting storage elements with renewable energy sources and different loads. Moreover, input and output voltages are adjustable with a reactive power compensation feature. Both AC and DC buses are available. The voltage on the DC link, thus on the output, can be easily controlled with a front-end converter e.g. an active rectifier. In addition, the ITR is environmentally friendly since no liquid dielectrics are used for cooling. ITRs can be equipped with advanced communication interface that includes smart metering, diagnostics and distance control features. Eventually, ITRs are also appropriate to be used in single-wire earth return transmission systems [2].

II. Basic requirements

As a complete DC distribution system will not be available in the near future, the ITR will operate in the already existing AC medium voltage grid. ITRs should be adaptable to different MV and LV levels worldwide. Thus, the ITR will be in the power range of today's power MV/LV distribution LFTs.

TABLE 1

TYPICAL LFT MV/LV DISTRIBUTION TRANSFORMER POWER RATINGS

Apparent power (kVA)	Nominal current (A)	
	237 V	410 V
100	244	141
160	390	225
315	767	444
630	1535	887
1250	3045	1760
1600	3898	2253
2000	4872	2816
2500	7673	4436

TABLE 2

EXISTING MEDIUM VOLTAGE RATINGS

Location	Voltage (kV)				
Europe [1]	3.6	7.2	12	17.5	24
North America [2]	4.75	8.25	15	25.8	
Railway	17.2 [3]	27.5 [4]			

1) 3 phases 50 Hz; 2) 3 phases 60 Hz, 3) 1 phase 16 2/3 Hz, 4) 1 phase 50 or 60 Hz.

TABLE 3

EXISTING LOW VOLTAGE RATINGS

Rated Low voltages (V)				
100/200	120/208	110/220	127/220	120/240
230/400	277/480	347/600	400/690	

2 or 3 phases + neutral, 50 or 60 Hz.

An overview of the most relevant power ratings with nominal current according to the IEC 60076 is given in Table 1. An overview of the most important AC MV- and LV levels in a distribution grid and railway (based on IEC 60038) is given in Table 2 and 3. The standard restricts the use of 3.6 kV and 7.2 kV voltages in public distribution systems. Also, the tolerance of ± 10 % of the nominal voltage in 230/400 and 400/690 systems must be guaranteed.

In addition, ITR must meet the same requirements that are valid for LFT according to the standards. It comprises connection techniques to MV and LV grid, protection against electric shock, sizing and protection of conductors, protection against voltage surges, power factor correction and harmonics filtering, electromagnetic compatibility etc.

III. TOPOLOGIES

Many existing topologies for ITRs as well as for general AC-AC power conversion do not support the bi-directional power flow, which is considered to be a minimum requirement for replacing an LFT. Other important requirements comprise galvanic isolation capability, capability of interconnecting renewable energy sources and energy storage devices.

A good approach to classify ITR topologies and select the appropriate configuration according to the specific needs was introduced in [3] and [4]. According to this classification four basic topology principles can be distinguished:

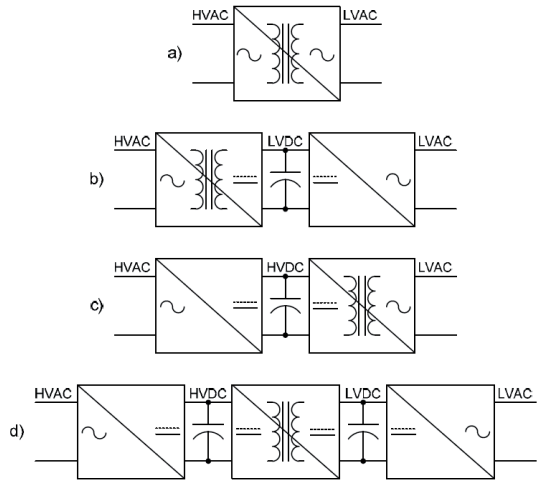


Fig. 1. ITR configurations: a) single-stage AC-AC, b) two-stage with LVDC link, c) two-stage with HVDC link, d) three-stage with HVDC and LVDC links.

a) single-stage topology with direct AC-to-AC conversion,
b) two-stage topology with low voltage DC link (LVDC),
c) two-stage topology with high voltage DC link (HVDC),
d) three-stage topology with both HVDC and LVDC link.

The configuration of these topologies is shown in Fig. 1 [4]. The HVDC link is not suitable for interconnecting the distributed energy storage and distributed renewable energy resource devices since all today's renewable energy resources operate at medium-voltage level. The HV to MV step does not seem to be reasonable due to the need for additional converters that increase the cost and volumes of the whole system. For this reason, topology with the HVDC link is not analyzed further.

A. Single stage topologies

Different single-stage topologies with direct AC-AC conversion exist. Back-to-back VSI is shown in Fig. 2. It is a cascaded connection of a 50 Hz passive transformer and a low-voltage AC-DC-AC converter. It has a bi-directional power flow capability, however it lacks a high frequency transformer and provides no galvanic isolation [5].

Another AC-AC single stage topology with a full bridge converter and a HF transformer was introduced in [4] (see Fig. 3). Here, an input high voltage is turned into a high-frequency square wave and passed through the HF transformer to the low voltage side where it is rectified back to 50 Hz sinusoidal shape voltage. This topology requires simple control, however requires inductive filters on the input and output to allow the buck mode and filter the generated ripple current. Moreover, the lack of the DC link is a major drawback of this topology, thus integration of storage elements and power factor correction would require additional devices which in turn make the system complicated, increase the size and cost of the overall system.

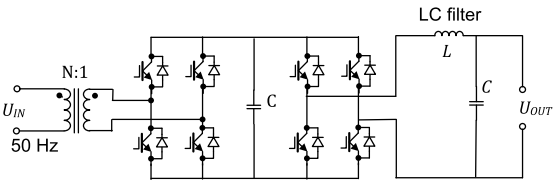


Fig. 2. Single-stage topology with LFT and AC-DC-AC converter.

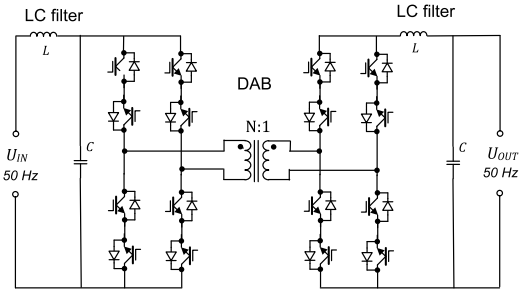


Fig. 3. Single stage topology with full bridge converter and HF transformer.

B. *Two-stage topologies*

A two-stage topology based on an AC-DC converter and a PWM inverter is shown in Fig. 4. The switches on the high side must be four-quadrant to withstand bi-polar voltages and currents. A disadvantage of this DC-DC version is the use of two different controls depending on the direction of the power flow.

Use of a dual active bridge (DAB) in the two-stage topology would provide seamless control of the power in both direction and zero voltage switching capability for a wide load range. The disadvantages of this topology are high sensitivity of the average active power flow to leakage inductance variation and the large ripple currents [5]. Also, the reactive power compensation feature is complicated on the HV side.

C. *Three stage topologies*

Three stage topologies enable several functions that are desirable to ITR [6]-[7]. Three-stage topology comprises rectifying the input AC voltage to a DC voltage, forming this way a MVDC link. Afterwards, the MV is converted into high frequency AC voltage and transferred to the HF transformer, where the voltage level is reduced and rectified again to a low voltage DC level, forming this way a LVDC link. The low DC voltage is converted again into 50 Hz AC voltage. Schematic of this topology is shown in Fig. 5.

The main disadvantage of this topology is the large number of components which results in possibly lower efficiency and reliability. However, the MVDC is suitable for connecting the renewable energy sources to the ITR.

Another three-stage topology with a multilevel-rectifier was proposed in [5]. It uses one flying capacitor multilevel AC-DC converter to provide a HV DC bus for three parallel connected DC-DC DAB converters.

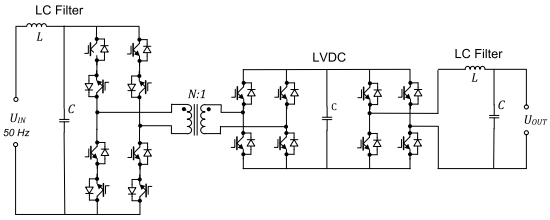


Fig. 4. Two-stage topology with a full bridge converter and a HF transformer.

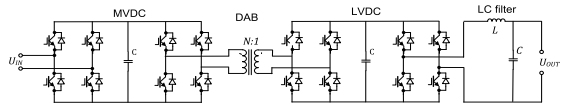


Fig. 5. Three-stage topology system with HVDC/MVDC

DAB converters provide galvanically isolated power conversion to a LVDC bus. An inverter converts low voltage DC to utility AC voltage. This topology is suitable for connecting to the MV side, because it has input-series-output-parallel configuration that allows blocking of the peak voltage on the MV side. This topology uses compact high frequency transformer, has power flow control, power factor correction and a low voltage DC bus for DG generation, however it has a large number of switches and a complicated configuration.

D. *Four wire matrix converter based topologies*

Another suitable topology for the ITR was proposed in [8]. This topology is similar to single-stage topologies and is shown in Fig. 6. Input and output links are matrix converters with six bilateral switches, which convert 50 Hz sinusoidal mains voltage to the medium frequency voltage. The inverse function is carried out in the output link in order to convert medium frequency back to 50 Hz sinusoidal voltage. The transformer middle end of the winding is used as the fourth wire to be used as neutral wire. This topology requires a low number of switches, does not require a capacitor on the MV side, has small losses due to fewer switches and bi-directional power flow control capabilities. However, it needs the zero crossing detection of medium frequency voltage for control scheme implementation. Lack of the DC link makes it unsuitable for interconnecting renewable energy sources and energy storage devices into one system.

The topologies were analyzed in detail on the basis of switch count, switch stress, switch losses, control characteristics and the ability to meet the required and desirable functionalities in FREEDM in [4]. Accordingly, all the analyzed topologies require at least three modules. Single-stage topologies are among others with the least elements count and thus least switching losses. However, there is no difference in the switch count between two-stage and three-stage topologies. Low switch losses in single-stage topologies are at the expense of their limited functionalities. The extra DC link in three-stage topologies improves the LVDC link voltage regulation in comparison to two-stage topologies.

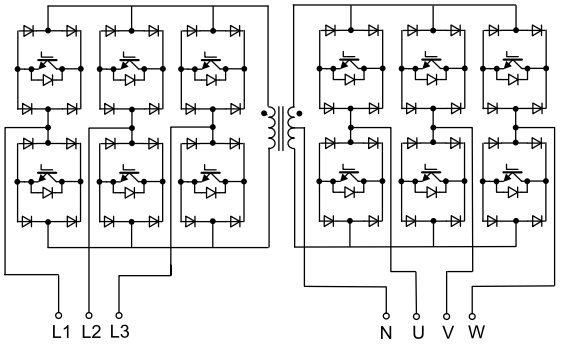


Fig. 6. Direct four-wire matrix converter based ITR topology

Presence of two different voltage level DC links allows interconnecting the energy storage devices and renewable energy sources into one system without additional converters.

According to this comparison three-stage topologies seem to be the most promising due their number of advantages over single- and two-stage topologies. The modular structure based ITR seems to be most advantageous, thus its design and operating principle are described further.

IV. Operating Principle and Design of Modular Structure Based ITR

A. Base module design

The base module consists of three stages: input, isolation, and output stage [8]-[9]. Input stage is a bi-directional controllable rectifier, which regulates the DC- link voltage and can also be used to shape the input current (reactive power compensation feature). Many topologies are suitable for the input stage most commonly an active front-end bridge rectifier is used. The second stage provides galvanic isolation between the primary and the secondary side and reduces the DC-link voltage.

First, the DC voltage is converted to a high frequency (HF) square-wave signal, then transferred through the HF transformer and finally rectified to form the reduced DC-link voltage on the secondary side. Presence of a two-level DC link allows integrating low-voltage energy storage devices and high voltage (or medium voltage) energy generators into one system. The output stage is a sinewave inverter, which converts reduced DC voltage back to low frequency (50 or 60 Hz) alternating grid voltage. Dual active bridges allow the energy flow to be controlled in both directions and use the soft switching technique.

Soft switching is a feasible solution, facilitated either by adding auxiliary devices such as an auxiliary resonant commutated pole (ARCP) or by using leakage inductance of high-frequency transformers (DAB). However it adds circulated energy, trading conduction loss to the switching loss [5]. ARCP adds a bi-directional switch pole between the neutral point of the DC bus and the midpoint of a main switch leg. Auxiliary switches are turned on during the main switching transient and they provide enough inductive energy to resonate with snubber capacitors. In a DAB system, the leakage inductance of the high-frequency transformer resonates with snubber capacitors to achieve ZVS [10]. In the case of DAB no extra switching devices are necessary, however soft switching range becomes narrower with the decrease of the load.

B. Phase module design of ITR

IGBTs and high-frequency transformers with distribution voltage ratings are not yet available. Therefore a modular approach can be used to meet these requirements. A modular design consisting of one or several base modules of the ITR is shown in Fig. 7. The ITR allows connecting energy storage devices or controllable DC/DC converter to the LVDC link as shown in Fig. 8. Fig. 9 presents the possibility of using one common inverter with parallel connected phase modules.

C. Three-phase systems

Three-phase voltage systems are used in electrical transmission today, thus all LFTs have three-phase design. Three-phase transformers have three basic winding connections: star, delta and zigzag. As the windings in the LFT, the phase modules of the ITR can be connected correspondingly to different winding connections. The most common winding configuration in distribution networks is Delta/Star connection. An ITR phase module connection is shown in Fig. 10.

Most distribution networks use isolated neutral configuration, since low earth-fault current guarantees reliable work of the grid. However, earth fault can raise voltage in other phases up to factor √3 times higher, thus a transformer must be designed to cope with these temporary (until couple of hours) overvoltages.

V. Benefits and Challenges

The ITR must have an efficiency profile that is similar to the LFT. The efficiency of the LFT is normally 97% [2], which is higher than the efficiency of the ITR, however an efficiency rate of 98,1% of the ITR without output inverter has been achieved [11]. The efficiency of the LFT is lowered due to the harmonics caused by residential loads. Major losses in power electronic converter are conduction losses, switching losses and core losses. Conduction losses occur due to the voltage drop on each element in the electric circuit. Switching losses comprise IGBT turn-on/turn-off energy and the diode reverse recovery energy. Transformer core losses are caused due to the hysteresis effect in the core that depend on magnetic flux, switching frequency and on the voltage waveform. Besides main losses, also losses in the gate driver, controller and auxiliary circuits are present. The three major losses were analyzed in [5].

It is also important to notice that besides the advantages of high-frequency on a transformer's size, it can significantly affect the winding resistance by introducing dc resistance, skin and proximity effects [12]. Moreover, the high frequency increases EMI emissions, which may require installing an additional filter and thus reduce the efficiency.

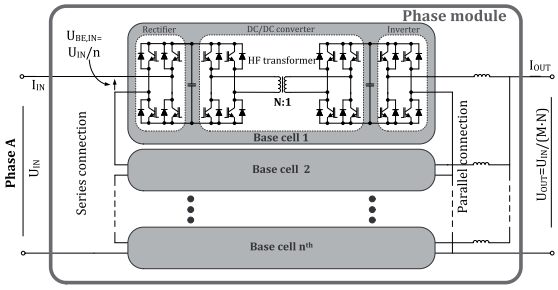


Fig. 7. One Phase module structure of ITR.

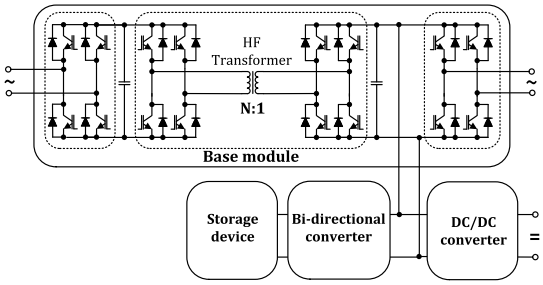


Fig. 8. Connecting an energy storage device and controllable DC source converter to the LVDC link of the ITR.

Efficiency decreases as the power converters become more complex. Efficiency can be improved by lowering the switching frequency using a multilevel front-end rectifier. Moreover, the topology that uses fewer switches has lower energy circulation and fewer power conversion stages.

Reliability of the ITR is the second highest priority after efficiency. In order to increase the reliability, the following steps can be taken: some redundant cells can be included into the ITR to improve the voltage stress handling in case of failure. It is also likely that the reliability will increase together with the progress of technology [2]. Electrolytic capacitors should be avoided due to their relatively short lifetime (12 000 hours).

The cost of the LFT is much lower than that of comparable ITR, which is mainly caused by the high semiconductor cost. LFTs require additional relay protection, additional elements (e.g. FACTS), stable construction with a built-in oil tank and requires higher amounts of copper. The most expensive elements in ITRs are semiconductors and their sophisticated control circuitry. Using modular design with a common inverter (see Fig. 9) would save the cost. However, it is likely, that with an increase of the manufacture, semiconductor costs will be reduced in the future.

Another issue is the maintenance of the transformer. Maintenance costs of the LFT are relatively low since full maintenance is carried out every 10-15 years while the lifetime of the LFT is usually 30 years under nominal load. Thus, although ITRs do not require oil change, it would require more maintenance of the capacitors, cooling fans, semiconductors.

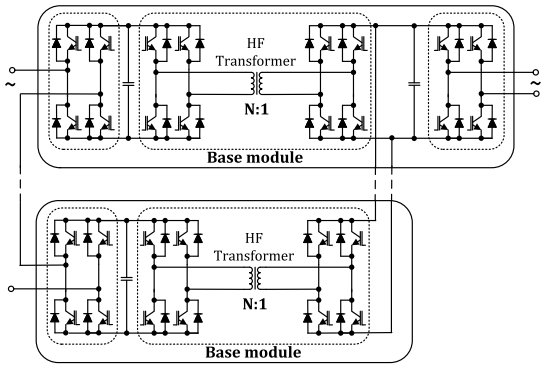


Fig. 9. A modular three-stage design of the ITR with a common inverter

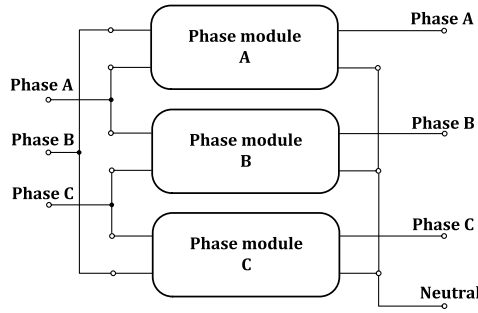


Fig. 10. Delta/Star connection of three phase modules

In order to keep the lifetime of semiconductors as high as possible, keeping the operating temperature in the allowed range is essential.

A. ITR in Microgrid

An ITR is a key element of the ITR-based microgrid systems. A microgrid is a possible solution to realize self-powered residential applications for most houses in the country. Reliability of a microgrid is low due to fluctuating renewable energy sources (wind generators, photovoltaic, fuel cells, supercapacitors, diesel generators, electric vehicles or regenerative drives), so an intelligent management is of high importance in such systems. One example of such ITR-based microgrids is a future renewable electric energy delivery and management (FREEDM) system. This is a revolutionary power grid based on power electronics, high bandwidth digital communication and distributed control. It is radically different from today's grids because it replaces electromagnetic devices such as 50 Hz transformers with the ITR [13]. ITRs will play an important role in the protection of a microgrid, which is very sensitive to faults. That is due to meshed network, where finding a fault might be very complicated. Also, the small impedance of microgrid makes conventional phase and distance relays unsuitable for protection. For that reason ITR must have built in protection to identify the fault.

VI. CONCLUSION

This paper covers the new concept of an intelligent transformer, its design, existing topologies, future benefits and challenges. An ITR is a new power electronic based transformer that is intended to operate in microgrids, where renewable energy sources, storage devices and loads are all interconnected into one system. Basic requirements the ITR has to meet are bi-directional energy flow control capability, power factor correction and galvanic isolation. Moreover, the ITR must have an efficiency, reliability and cost comparable to traditional low frequency transformers. In order to operate in the existing network the transformer must be designed to existing power ratings with existing MV and LV levels.

Different single-stage, two-stage, three-stage and also four-wire topologies exist. The most convenient seem to be three-stage topologies with the introduction of a medium-voltage DC link for connecting the power sources and a low-voltage DC link for connecting energy storage devices into one system.

ACKNOWLEDGEMENT

This research and work has been supported by Estonian Ministry of Education and Research (Project SF0140016s11), Estonian Science Foundations (Grant ETF8687 and Grand G7572) and Estonian Archimedes Foundation (Project "Doctoral school of energy and geotechnology II").

REFERENCES

[1] Iman-Eini, H.; Farhangi, S.; Schanen, J.-L.; Aime, J.; , "Design of Power Electronic Transformer based on Cascaded H-bridge Multilevel Converter," *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium on* , vol., no., pp.877-882, 4-7 June 2007.

[2] van der Merwe, J.W.; du T. Mouton, H.; , "The solid-state transformer concept: A new era in power distribution," *AFRICON, 2009. AFRICON '09.* , vol., no., pp.1-6, 23-25 Sept. 2009.

[3] Heinemann, L.; Mauthe, G.; , "The universal power electronics based distribution transformer, an unified approach," *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual* , vol.2, no., pp.504-509 vol.2, 2001.

[4] Falcones, S.; Xiaolin Mao; Ayyanar, R.; , "Topology comparison for Solid State Transformer implementation," *Power and Energy Society General Meeting, 2010 IEEE* , vol., no., pp.1-8, 25-29 July 2010.

[5] Hengsi Qin; Kimball, J.W.; , "A comparative efficiency study of silicon-based solid state transformers," *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE* , vol., no., pp.1458-1463, 12-16 Sept. 2010.

[6] Bhattacharya, S.; Tiefu Zhao; Gangyao Wang; Dutta, S.; Seunghun Baek; Yu Du; Parkhideh, B.; Xiaohu Zhou; Huang, A.Q.; , "Design and development of Generation-I silicon based Solid State Transformer," *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE* , vol., no., pp.1666-1673, 21-25 Feb. 2010.

[7] Banaei, M.R.; Salary, E.; , "Power quality improvement based on novel power electronic transformer," *Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2011 2nd* , vol., no., pp.286-291, 16-17 Feb. 2011

[8] Mirmousa, H.; Zolghadri, M.R.; , "A Novel Circuit Topology for Three-Phase Four-Wire Distribution Electronic Power Transformer," *Power Electronics and Drive Systems, 2007. PEDS '07. 7th International Conference on* , vol., no., pp.1215-1222, 27-30 Nov. 2007.

[9] Ronan, E.R.; Sudhoff, S.D.; Glover, S.F.; Galloway, D.L.; , "A power electronic-based distribution transformer," *Power Delivery, IEEE Transactions on* , vol.17, no.2, pp.537-543, Apr 2002.

[10] Smith, K.M., Jr.; Smedley, K.M.; , "A comparison of voltage-mode soft-switching methods for PWM converters," *Power Electronics, IEEE Transactions on* , vol.12, no.2, pp.376-386, Mar 1997.

[11] Heinemann, L.; , "Analysis and design of a modular, high power converter with high efficiency for electrical power distribution systems," *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual* , vol.2, no., pp. 713- 718 vol.2, 2002.

[12] Du, S.B.Y.; Gangyao Wang; Bhattacharya, S.; , "Design considerations of high voltage and high frequency transformer for solid state transformer application," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.421-426, 7-10 Nov. 2010.

[13] Xu She; Lukic, S.; Huang, A.Q.; Bhattacharya, S.; Baran, M.; , "Performance evaluation of solid state transformer based microgrid in FREEDM systems," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.182-188, 6-11 March 2011.

[14] Xiaohu Zhou; Yu Liu; Bhattacharya, S.; Huang, A.; , "New inductor current feedback control with active harmonics injection for inverter stage of solid state transformer," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.593-598, 7-10 Nov. 2010.

[15] Escobar, G.; Mattavelli, P.; Stankovic, A.M.; Valdez, A.A.; Leyva-Ramos, J.; , "An Adaptive Control for UPS to Compensate Unbalance and Harmonic Distortion Using a Combined Capacitor/Load Current Sensing," *Industrial Electronics, IEEE Transactions on* , vol.54, no.2, pp.839-847, April 2007.

[16] Mattavelli, P.;"An improved deadbeat control for UPS using disturbance observers," *Industrial Electronics, IEEE Transactions on* , vol.52, no.1, pp. 206- 212, Feb. 2005

Viktor Beldjajev received his B. Sc degree in 2007 and M. Sc. in 2009 in Tallinn University of Technology. In 2009 he also received his Dipl. Ing. degree in the faculty of Automation in the Giessen-Friedberg University of Applied Sciences in Germany. Since 2009 he studies for his PhD at Tallinn University of Technology and his research interests include control of power electronic converters and power quality problems.

He has gained diverse experience working in several companies in Germany in the field of hardware and software development. He has also been teaching industrial robotics in Tallinn University of Technology for several years.

E-mail: vbeldjajev@gmail.com

Ph.D Indrek Roasto received the B.Sc and M.Sc in electrical engineering from Tallinn University of Technology, Tallinn, Estonia, in 2003 and 2005, respectively. At the end of 2009 he defended his PhD Thesis devoted to the research and development of smart control and protection systems for the high voltage high power galvanically isolated DC/DC converters. Currently he is a senior researcher in the Department of Electrical Drives and Power Electronics. He has over 30 publications and owns five Utility Models and one Patent in the field of power electronics. His research interests are in digital control of switching power converters, including modelling, design, and simulation.

E-mail: indrek.roasto@ieee.org

Tõnu Lehtla graduated in Tallinn Technical University in 1970. Engineer of Electrical engineering in the field of electrical drives and industry automation. Received Ph.D. degree in 1976.

He is a Professor and head of the chair of Robotics in the department of electrical drives and power electronics. He has authored over 100 scientific and methodical publications in the field of electrical drive, industry automation and robotics.

E-mail: tlehtla@staff.ttu.ee

[PAPER-III] **Beldjajev, V**., Roasto, I., Vinnikov, D. Analysis of Current Doubler Rectifier Based High Frequency Isolation Stage for Intelligent Transformer. 7th International Conference-Workshop Compatibility and Power Electronics (CPE2011), Tallinn, Estonia, June 01-03, 2011, pp. 336 – 341.

Analysis of Current Doubler Rectifier Based High Frequency Isolation Stage for Intelligent Transformer

Viktor Beldjajev, Indrek Roasto, Dmitri Vinnikov
Tallinn University of Technology, Department of Electrical Drives and Power Electronics
vbeldjajev@gmail.com, indrek.roasto@ieee.org, dmitri.vinnikov@ieee.org

***Abstract* — This paper proposes new topology for high frequency isolation stage of intelligent transformer based on bi-directional current doubler rectifier (CDR). Paper provides complete steady-state analysis of the proposed bi-directional CDR in boost mode. To facilitate the understanding of operation, the converter equivalent circuits for each operating mode with corresponding waveforms are presented. Also, mathematical analysis is done and compared with simulation results.**

I. INTRODUCTION

Modern trends in electrical energy technology are characterized by steadily growing need for renewable energy sources, energy storage, and smart grid technologies. Centralized generating facilities are giving way to smaller, more distributed generation. Thus, it is likely that future power generation and distribution will involve a lot of distributed renewable energy sources and micro grids. In order to effectively interconnect power generation and energy storage into a grid or micro grid intelligent energy management (IEM) is needed. IEM substations should have bi-directional energy flow control capability, intelligent control and communication interface. It becomes clear that traditional low frequency (50 Hz) distribution transformers are not any more suitable for such demanding applications.

Intelligent transformer (also known as solid state or power electronic transformer) is a good candidate for IEM subsystems. Intelligent transformer (ITR) is a new type of transformer that realizes voltage transformation, galvanic isolation and power quality enhancements in a single device.

The basic idea behind the ITR is to use a high frequency ($f > 1$ kHz) transformer instead of traditional low frequency (50 Hz) distribution transformer. Increasing the frequency allows higher utilization of the magnetic core and reduction in the size of the transformer. According to [1] size and weight reduction up to three times is possible. Moreover, ITR uses much less copper that decreases overall costs of the device.

For realization of the ITR, different topologies exist. In [2] an AC/AC buck topology has been proposed. Such converter has variable transformation ratio and the lowest component count. However, it provides no galvanic isolation and causes high voltage (HV) stress for semiconductors. Two stage AC/AC topology with matrix converters is presented in [3]. The benefits of this topology are low number of switches and components, and galvanic isolation. Limited switching frequency that does not allow implementing of high frequency transformer is major drawback of such topology.

A recent approach is the ITR design that has modular structure consisting of one or several base cells, as shown in Fig. 1. The base cell consists of three stages: input, isolation, and output stage [4]-[6]. Input stage is a bi-directional controllable rectifier, which regulates the DC- link voltage and can also be used to shape the input current (reactive power compensation feature). The second stage provides galvanic isolation between the primary and the secondary side and reduces the DC-link voltage. First, the DC voltage is converted to a high frequency (HF) square-wave signal, then transferred through the HF transformer and finally rectified to form the reduced DC-link voltage on the secondary side. The output stage is a sinewave inverter, which converts reduced DC voltage back to low frequency (50 Hz) alternating grid voltage. It becomes clear that high frequency isolation stage is the key for building an optimal and efficient ITR. By selecting the proper inverter and rectifier topologies the efficiency, energy density and volumes of ITR can be improved.

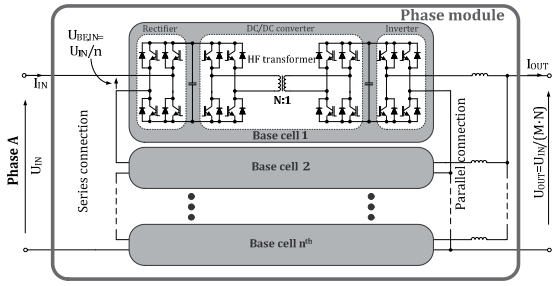


Fig. 1. One phase structure of ITR

II. SURVEY OF ISOLATION STAGE

Two basic topologies are generally suitable for the input side: full-bridge (FB) and half-bridge. Half-bridge topology has a simpler construction and lower number of switches. However, the drawbacks are higher current stress of switches and volt-second unbalance risk. Full-bridge allows to realize phase shift modulation control and zero-voltage switching without additional components, which can reduce switching losses. Due to higher number of switches the volt-second unbalance effect can be prevented and switches have lower

978-1-4244-8807-0/11/$26.00 ©2011 IEEE

current stress when compared to half bridge. Thus, FB seems to be more feasible solution for the input side.

In general, three basic topologies are suitable for output side: full-bridge, centre-tapped rectifier, and current doubler rectifier (CDR). With FB no centre tapped transformer is needed and it has a compact design. However, the transformer secondary and rectifier diodes carry full output current, which increases conduction losses. Centre-tapped rectifier has twice smaller number of rectifying diodes and only one diode is conducting at a time. Thus it has low switching losses. Main drawbacks are complicated design and rectifier diodes have to carry full output current, which increases conduction losses. Use of CDR offers many advantages in comparison with FB and centre-tapped rectifier. Transformers secondary current is half the output current allowing reduction of conduction losses especially in the case of higher currents. Using two transformers in the output provides better heat dissipation, and ripple current cancellation effect which allows to use smaller inductances. Operation of such topology in buck mode has been already presented in [16] - [19], where a detailed analysis can be found. However, using CDR for voltage elevation has been proposed only by few authors [11]-[15], thus needs more detailed analysis.

Several researches [11]-[13] propose to add auxiliary and HF transformer on one magnetic core in series with inductors to eliminate inductor currents at loads close to zero . A push-pull type converter in the input with CDR in the output is proposed in [14]. In addition, each coupled inductor is wound on the same core as input-to output windings, forming this way additional path for excessive energy in inductors. Research in [15] proposes to use two inductors in current-fed push-pull converter, to overcome the drawbacks of single inductor push-pull converter e.g. high output voltage ripple, high voltage across switches, high volt-ampere rating for transformer. However, none of these topologies is suitable for bi-directional energy flow control.

Problems also occur when CDR is working in bi-directional mode. It turns out that traditional CDR cannot provide bi-directional energy flow when duty cycle is smaller than 50 % [7]. A solution was proposed in [8] to overcome this drawback. It uses two auxiliary transformers with two diodes to transfer the leakage energy to the high voltage side. However it has high voltage stress on semiconductors. In the current high voltage application the voltage difference between input and output can be more than 5 times, which would require bulky transformers. Since small weight and volumes are important factors in the ITR design, those auxiliary transformers could be a serious drawback. In this paper a new topology is proposed where the auxiliary transformers can be designed much smaller. Also, the reverse voltage of diodes is lower due to smaller voltage difference.

III. NEW BI-DIRECTIONAL DC/DC CONVERTER

The proposed topology of the high frequency isolation stage is shown in Fig. 2. The proposed bi-directional dc-dc converter consists of a FB inverter, a high frequency transformer and a CDR. The energy can be transferred in both directions. Therefore, the diodes in traditional CDR are replaced with controllable switches T_5 and T_6. The high-frequency step-up isolation transformer TR provides required voltage gain as well as the galvanic isolation between the input and output sides of the converter.

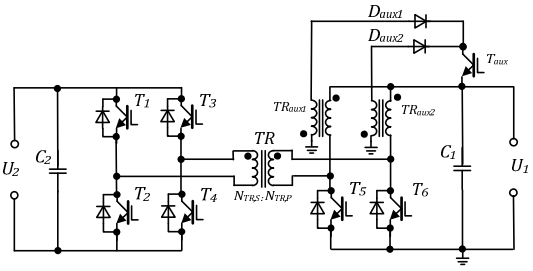


Fig. 2. Power circuit diagram of proposed HF isolation stage

Main benefits of the proposed high frequency isolation stage based on the FB inverter and bi-directional CDR are as follows:

- Zero voltage switching for the primary switches T_1...T_4 in a wide load range, achievable to utilize the energy stored in the output filter inductances [9].
- Bi-directional energy control.
- Use of HF transformer reduces size of the converter.
- Reduced current ripples due to transformers.
- Better thermal performance due to current doubling effect.
- Reduced transient response [10].

The proposed CDR can transfer energy in both directions, operating this way either in buck or boost mode in a wide range of duty cycles. In the buck mode the energy is transferred from high voltage side to low voltage side as shown in Fig. 2. In the boost mode the energy is transferred from low voltage side to high voltage side. Boost mode is also divided into three different states: normal operation with duty cycle D_A value from 50 % to 100 %, start-up operation in continuous conduction mode (with D_A value between 25 % and 50 %) and start-up operation in discontinuous conduction mode (with D_A value between 0 % and 25 %).

However, during start-up operation the freewheeling path of the leakage energy of the inductors is interrupted, which results in dangerous overvoltage. To provide an alternative freewheeling path the inductors are replaced with two auxiliary transformers TR_{aux1}, TR_{aux2}, which redirect leakage energy back to the low voltage side through diodes D_{aux1}, D_{aux2} and controllable switch $T_{aux,}$ which is switched ON only during the start-up operation

IV. STEADY STATE ANALYSIS OF PROPOSED CONVERTER

In steady state analysis, all three operating modes are examined. Mathematical analysis and equivalent circuits for different states are provided.

The analysis of proposed topology is based on the following assumptions: 1) all transistors and switches are ideal, 2) all inductances and capacitors are ideal, 3) auxiliary transformers TR_{aux1} and TR_{aux2} are identical.

A. Operation with duty cycle 50 % ≤ D_A ≤100 %

When duty cycle is between 50% and 100 %, the converter is operating in normal operating mode. Fig. 3 shows the equivalent circuit of proposed converter in the normal mode.

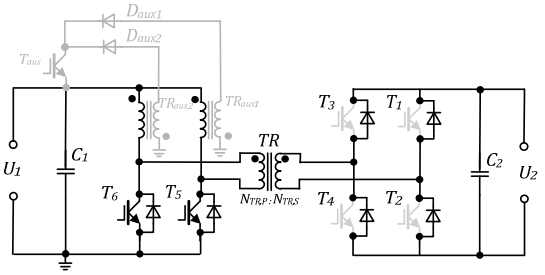


Fig. 3. Equivalent circuit in the boost mode for operation with $D_A \geq 50\%$

The operating period of one switch consists of the active and zero states. During the active state the switch on each branch is switched ON and energy is transferred to the isolation transformer. During the zero state the switch of the branch is switched OFF. The operating period can be written as

$$T = t_A + t_Z , \tag{1}$$

where t_A and t_Z are durations of an active and zero states, correspondingly. For better appearance of equations the state intervals are represented with corresponding duty cycles as

$$\frac{t_A}{T} + \frac{t_Z}{T} = D_A + D_Z = 1 . \tag{2}$$

The turns ratio of transformer is defined as follows

$$N = \frac{N_S}{N_P} , \tag{3}$$

where N_S is the number of turns on the secondary side, and N_P is the number of turns on the primary side of the transformer.

Fig. 4 shows equivalent circuits for both, active and zero state of the switch in the normal operation mode. Typical waveforms for this operation can be found in [8].

Energy can be transferred to the output only during one transistor is switched ON. At the beginning of the active state of transistor T_6 the transistor T_5 is also switched ON and no energy is transferred to the HF transformer. When transistor T_6 switches ON (Fig. 4*a*), the energy is transferred to the output via the HF transformer. Due to the short zero state duration, transistor T_5 switches ON again during transistor T_6 is still ON and the whole process repeats. During the zero state of transistor T_6 and active state of transistor T_5, the energy is transferred to the output.

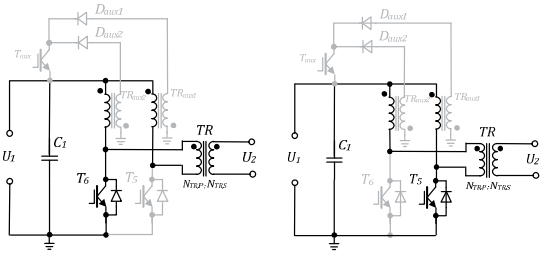


Fig. 4. Equivalent circuits of the transistor's T_6 active state (a) and zero state (b) during normal operation.

For the active state (Fig. 4*a*), it can be obtained that

$$u_{TRaux1} = u_1 . \tag{4}$$

In the zero state (Fig. 4*b*) of transistor T_6 the transformer voltage can be obtained as

$$u_{TRaux1} = u_1 - u_{TR} = u_1 - \frac{u_2}{N_{TR}} , \tag{5}$$

where N_{TR} is turns ratio of the HF transformer.

In the steady state operation, the average voltage over the inductor during one operating period is zero.

$$\frac{u_1 \cdot t_A + \left(u_1 - \frac{u_2}{N_{TR}} \right) \cdot t_Z}{T} = 0 . \tag{6}$$

Equation (6) can be rewritten using duty cycles

$$u_1 \cdot D_A + \left(u_1 - \frac{u_2}{N_{TR}} \right) \cdot D_Z = 0 , \tag{7}$$

where D_A represents the active state of the transistor, and D_Z represents the zero state. From (7) the output voltage can be found as:

$$u_2 = \frac{u_1 \cdot (D_A + D_Z)}{D_Z} \cdot N_{TR} = \frac{u_1 \cdot N_{TR}}{1 - D_A} . \tag{8}$$

Accordingly, the boost factor is:

$$k = \frac{u_2}{u_1} = \frac{1}{1 - D_A} \cdot N_{TR} . \tag{9}$$

B. Operation with 25 % ≤ D_A < 50 %

During the start-up operation the energy stored in transformer TR_{aux1} and TR_{aux2} primaries, is transferred out through secondary windings back into the input. Equivalent circuit for this operation is shown in Fig. 5 and typical waveforms in Fig. 6.

Operating period of the converter consists of one active and three zero states. During the active state the corresponding switch is conducting. The operating period can be defined as:

$$t_A + t_{Z1} + t_{Z2} + t_{Z3} = T . \tag{10}$$

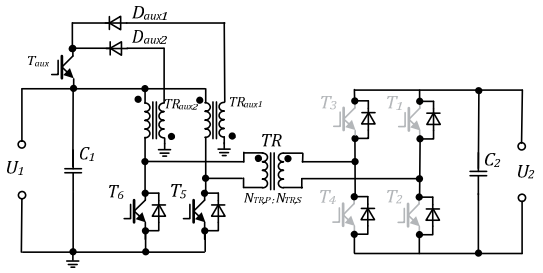


Fig. 5. Equivalent circuit for operation with $D_A < 50$ %.

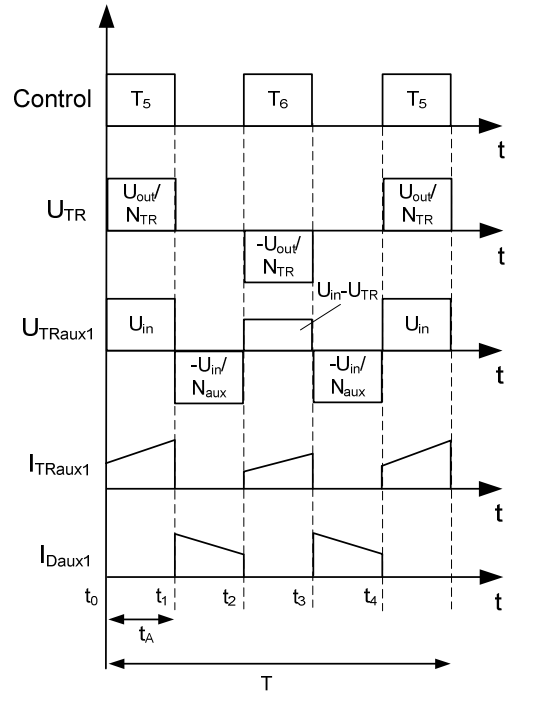


Fig. 6. Waveforms for operation with $D_A < 50$ %.

During active state t_A (**t_0 – t_1**) transistor T_6 is switched ON and energy is transferred to the output via the HF transformer. Current in the auxiliary transformer TR_{aux1} primary increases linearly with input voltage u_1 and stores energy into the transformer. Equivalent circuit for this state is shown in Fig. 4*a*. Voltage over the transformer TR_{aux1} primary is equal to (4).

During zero state t_{Z1} (**t_1 – t_2**), when both transistors are switched OFF, the currents i_{TRaux1} and i_{TRaux2} circulate over auxiliary transformer's secondary back to the input. Magnetizing current of transformer TR circulates on the secondary side [8]. Equivalent circuit for this mode is shown in Fig. 7.

Voltage over the transformer TR_{aux1} primary is equal to input voltage and N_{aux1} ratio.

$$u_{TRaux1} = \frac{u_1}{N_{aux}}. \tag{11}$$

During zero state t_{Z2} (**t_2 – t_3**), transistor T_6 is switched ON and energy is transferred to the output via the HF transformer. At the same time current in the transformer TR_{aux2} primary increases linearly with the input voltage u_1. The voltage applied to TR_{aux1} primary is equal to (5).

Zero state t_{Z3} (**t_3 – t_4**), is identical to the interval t_{Z1}.

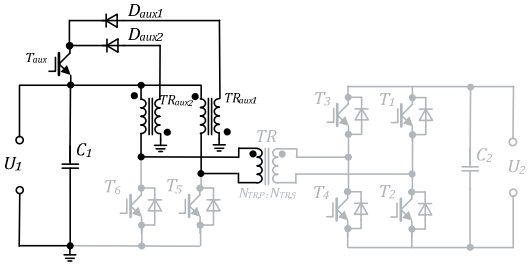


Fig. 7. Equivalent power circuit for intermediate state during start-up.

Equations for steady state analysis in CCM can be written as follows

$$\frac{u_1 \cdot t_A + \left(-\frac{u_1}{N_{aux}}\right)\cdot\left(t_{Z1}+t_{Z3}\right)+\left(u_1-\frac{u_2}{N_{TR}}\right)\cdot t_{Z2}}{T} = 0. \tag{12}$$

Equation (14) can be rewritten using duty cycles

$$u_1 \cdot D_A + \left(-\frac{u_1}{N_{aux}}\right)\cdot\left(D_{Z1}+D_{Z3}\right)+\left(u_1-\frac{u_2}{N_{TR}}\right)\cdot D_{Z2} = 0. \tag{13}$$

Taking into account that in the CCM the zero state duty cycle D_{Z2} is equal to the active state D_A and the zero state D_{Z1} is equal to D_{Z3}. Thus, we can simplify (10)

$$2D_A + 2D_Z = 1, \tag{14}$$

accordingly

$$D_Z = \frac{1-2D_A}{2} \tag{15}$$

Equation (13) can be simplified as follows

$$u_2 = \frac{N_{TR}}{N_{aux}}\left(2N_{aux} - \frac{1-2D_A}{D_A}\right)\cdot u_1, \tag{16}$$

where boost factor for start-up operation is

$$k = \frac{u_2}{u_1} = \frac{N_{TR}}{N_{aux}}\left(2N_{aux} - \frac{1-2D_A}{D_A}\right). \tag{17}$$

C. Operation with 0 % ≤ D_A < 25 %

In case of small loads, relatively low switching frequency and small duty cycle the converter can start to operate in discontinuous conduction mode (DCM), when current

through inductor goes to zero at the end of every operating cycle. As can be seen from (16). In DCM the discontinuous duty cycle D_D must also be taken into account, so that

$$k = \frac{u_2}{u_1} = \frac{N_{TR}}{N_{aux}}\left(2N_{aux} - \frac{1-2D_A-2D_D}{D_A}\right) \quad (18)$$

Boundary condition for DCM can be derived from (17)

$$D_A \geq \frac{1}{2\left(N_{aux}+1\right)}. \quad (19)$$

V. SIMULATION RESULTS

To verify the mathematical model of the bi-directional dc-dc converter, the electric circuit of this topology was simulated in PSIM environment. Moreover, the first experimental prototype was built and tested. Since conventional inductors were used instead of auxiliary transformers the prototype could be only tested in operation mode $D_A \geq 50$ %. The simulation circuit parameters correspond to experimental prototype's parameters, which are set as follows:

TABLE I
CIRCUIT SPECIFICATIONS

Parameter	Value
Low side voltage *(U_1)*	10 V
High side voltage range (U_2)	0…135 V
Power (P)	500 W
Switching frequency *(f_s)*	15 kHz
HF transformer turns ratio *(N_{TR})*	3.3
Auxiliary transformer's turns ratio (N_{aux})	1

Next, the simulation results in steady state operation in three different operating modes are presented. Fig. 8 presents the simulated voltage waveforms on low and high voltage sides in the operating mode with $D_A = 0.6$ in continuous conduction mode. It can be seen that both voltages are pure DC voltages with different layer. According to (8), in case of $U_1 = 10$ V, the $U_2 = 82.5$ V. As can be seen from Fig. 8, simulation results match the mathematical model of the topology.

Fig. 9 presents the experimental results for low and high side voltages, tested with the same parameters as simulation. The values of the voltages correspond to simulation results. Small peaks seen in the experimental results are caused by transistor switching.

Fig. 10 shows the simulated voltage waveforms on low and high voltage sides in the operating mode with $D_A = 0.3$ in continuous conduction mode. Voltage U_2 can be calculated accordingly to (16). In case of $U_1 = 10$ V, the $U_2 = 22$ V. As can be seen from Fig. 10 the simulation results correspond to mathematical model of the topology.

Fig. 11 shows the simulated voltage waveforms on low and high side voltages in the operating mode with $D_A = 0.15$. In this case the converter operates in discontinuous conduction mode and additional discontinuous duty cycle value D_D in (18) must be considered.

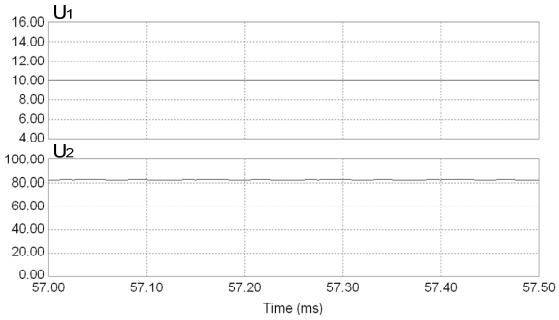


Fig. 8. Simulation results for low voltage side (U_1) as well as for high voltage side (U_2) during operation mode with $D_A = 0.6$.

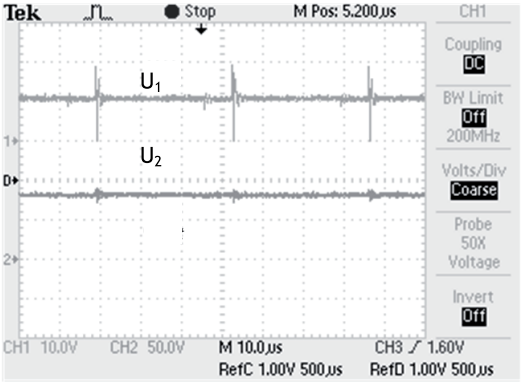


Fig. 9. Experimental results for low voltage side (U_1) as well as for high voltage side (U_2) during operation mode with $D_A = 0.6$.

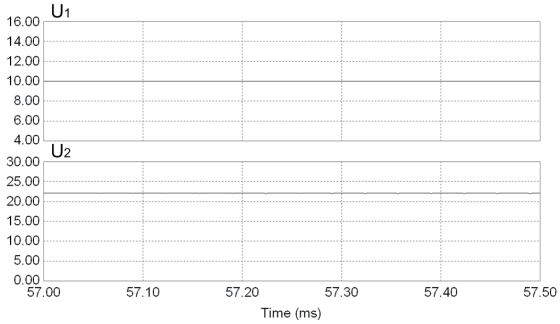


Fig. 10. Simulation results for low voltage side (U_1) as well as for high voltage side (U_2) during operation mode with $D_A = 0.3$.

TABLE II
CALCULATED VS SIMULATED RESULTS

	D_A =0.6	D_A = 0.3	D_A = 0.15
Calculated U_2 [V]	82.5	22	0.2
Simulated U_2 [V]	82.5	22	0.016

Simulation results are compared with mathematically achieved results in Table II. All calculated voltages correspond to the simulation results. Slight difference in operating mode with D_A = 0.15 is caused by uncertainty of D_D.

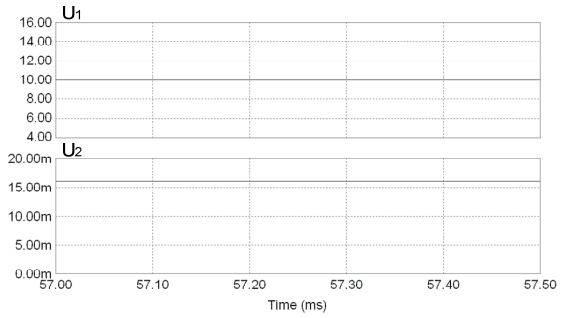


Fig. 11. Simulation results for low voltage side (U_1) as well as for high voltage side (U_2) during operation mode with D_A = 0.15.

CONCLUSION

This paper proposed new topology of HF isolation stage for ITR based on bi-directional CDR. CDR is not widely used for voltage elevation, however this topology is appropriate to ITR because of its bi-directional energy flow capability and operation in buck and boost mode, in a wide range of duty cycles. It has also a compact size, good heat dissipation, reduced danger of overvoltage and low current ripples. The converter is also able to operate in a duty cycle range lower than 50 % in CCM and DCM. Mathematical analysis of converter was done and verified with simulations. One operating mode, with $D_A \geq 0.5$ was also verified experimentally. Simulation results showed that the converter can operate in continuous conduction mode as well as in discontinuous conduction mode. The boundary condition for DCM was also derived. Mathematical models were confirmed by the simulation results, which gives a solid base to move on with real tests. As a next step the experimental prototype should be equipped with auxiliary transformers so that it could be tested in all three operating modes.

ACKNOWLEDGEMENT

This research and work has been supported by Estonian Ministry of Education and Research (Project SF0140016s11), Estonian Science Foundation (Grant ETF8687) and Estonian Archimedes Foundation (Project “Doctoral school of energy and geotechnology II”).

REFERENCES

[1] T. Zhao, J. Zeng, S. Bhattacharya, M. E. Baran, A.Q. Huang “An Average Model of Solid State Transformer for Dynamic System Simulation”. PES 2009, pp. 1-8.

[2] Srinivasan, S.; Venkataramanan, G.; “Comparative evaluation of PWM AC-AC converters”, Power Electronics Specialists Conference, 1995, Atlanta, GA.

[3] Mirmousa, H.; Zolghadri, M.R.; “A Novel Circuit Topology for Three-Phase Four-Wire Distribution Electronic Power Transformer”, 7th International Conference on Power Electronics and Drive Systems 2007. PEDS '07.

[4] Ronan, E.R.; Sudhoff, S.D.; Glover, S.F.; Galloway, D.L.; “A power electronic-based distribution transformer”, Power Delivery, IEEE Transactions on, 2002.

[5] H. Iman-eini and Sh. Farhangi, “Analysis and design of power electronic transformer for medium voltage levels”, in proc. IEEE Power Electronic Specialist Conference, PESC 2006, pp. 1- 5, June 2006.

[6] Jih-Sheng Lai; Maitra, A.; Mansoor, A.; Goodman, F.; “Multilevel intelligent universal transformer for medium voltage applications”, in Proc. IEEE Industry Applications Conf., Vol. 3, October 2005.

[7] Torrico-Bascope, R.P; Torrico-Bascope, G.V.; Branco, C.G.C.; Oliviera Jr, D.S. “A New Current-Doubler Rectifier Based on Three-State Switching Cell for Buck Derived DC-DC Converters”. PESC 2008, pp. 2492 – 2497.

[8] Flores, L.A.; Garcia, O.; Oliver, J.A.; Cobos, J.A. “High Frequency Bi-Directional DC/DC Converter Using Two Inductor Rectifier”. IECON 2006, pp. 2793 – 2798.

[9] Ruan, X.; Li, B.; Wang, J.; Li, J. “Zero-Voltage-Switching PWM Three-Level Converter With Current-Doubler-Rectifier.” IEEE Transactions on Power Electronics, vol. 19, No. 6, November 2004, pp 1523-1532.

[10] Mao, H.; Yao, L.; Deng, S.; Abdel-Rahman, O.; Liu, J.; Batarseh, I. “Inductor Current Sharing of Current Doubler Rectifier in Isolated DC-DC Converters.” IEEE 2006.

[11] Liang, Y.; Lehman, B. Isolated Two-Inductor Boost Converter with One Magnetic Core. APEC ’03. IEEE, pp. 879 – 885.

[12] Yungtaek, Y.; Jovanovic, M. M. New Two-Inductor Boost Converter with Auxiliary Transformer. APEC ’03. IEEE, pp. 654 – 660, vol. 2.

[13] Yungtaek, Y.; Jovanovic, M. M. New Two-Inductor Boost Converter with Auxiliary Transformer. Power Electronics, IEEE Transactions on vol. 19, Issue 1, Jan. 2004, pp. 169 – 175.

[14] Chung-Wook, R.; Seung-Hoon, H.; Myung-Joong, Y. Dual Coupled Inductor Fed Isolated Boost Converter for Low Input Voltage Applications. Electronics Letters, vol. 35, Issue 21. 14 Oct. 1999, pp. 1791 – 1792.

[15] De Arago Filho, W.C.P.; Barbi, I. A Comparison Between Two Current-Fed Push-Pull DC-DC Converter-Analysis, Design and Experimentation. INTELEC ’96. 18th International, 6-10 Oct. 1996, pp. 313 – 320.

[16] Kutkut, N.H.; Luckjiff, G.; "Current mode control of a full bridge DC-DC converter with a two inductor rectifier" PESC '97 Page(s): 203 -209 vol.1

[17] Kutkut, N.H.; "A full bridge soft switched telecom power supply with a current doubler rectifier" INTELEC 97., 19-23 Oct 1997 Page(s):344 -351

[18] Kutkut, N.H.; Divan, D.M.; Gascoigne, R.W.; “An improved full bridge zero-voltage switching PWM DC-DC converter using a two inductor rectifier “Industry Applications Society Annual Meeting, 1993., Conference Record of the1993 IEEE,2-8 Oct1993,Page(s):1065- 1072vol.2

[19] Kutkut, N.H.; Divan, D.M.; Gascoigne, R.W.; "An improved fullbridge zero-voltage switching PWM converter using a two-inductor rectifier", Industry Applications, IEEE Transactions on , Volume: 31 Issue: 1 , Jan/Feb 1995 Page(s): 119 -126.

[PAPER-IV] **Beldjajev, V**., Roasto, I. Impact of Component Losses on the Efficiency of the Bi-Directional Current Doubler Rectifier Based Isolation-Stage. The 38th Annual Conference of the IEEE Industrial Electronics Society (IECON2012), Montreal, Canada, 25-28 October 2012, pp. 5209 – 5214.

Impact of Component Losses on the Efficiency of the Bi-Directional Current Doubler Rectifier Based Isolation-Stage

Viktor Beldjajev
Department of Electrical Drives and Power Electronics,
Tallinn University of Technology,
Tallinn, Estonia
vbeldjajev@gmail.com

Indrek Roasto
Department of Electrical Drives and Power Electronics,
Tallinn University of Technology,
Tallinn, Estonia
indrek.roasto@ieee.org

***Abstract*— This paper presents a detailed analysis of the bi-directional current doubler rectifier (CDR) that is a good candidate for use in a power electronic transformer (PET). Among various advantages the current doubler rectifier offers a bi-directional power flow capability that is the major requirement for the PET. This paper provides the steady state analysis of the CDR in the bi-directional operation. In addition, the impact of the component losses on the efficiency is analyzed. Finally a suitable snubber circuit is proposed to damp the voltage peaks.**

Keywords- power electronic transformer, bi-directional current doubler rectifier, steady state analysis, efficiency.

I. INTRODUCTION

Distribution transformers are fundamental components in power distribution systems. They have relatively simple construction and high efficiency. However, they also have several disadvantages such as heavy weight, large size, complex protection system, high maintenance costs, and environmental concerns regarding mineral oil. These drawbacks are becoming increasingly important as the power quality becomes more of a concern, which is a strong tendency nowadays.

The idea of the power electronic transformer (PET) is already known for over 40 years but the first serious applications are occurring only recently [1][2]. On the one hand, the recent efforts in the field of power electronics semiconductors have brought new high power and high voltage (HV) devices on the market, which increase the voltage blocking capability of components and have made PET concept available for high voltage applications. On the other hand, modern trends in electrical energy technology are characterized by steadily growing need for renewable energy sources, energy storage, and smart grid technologies. Traditional low frequency (50/60 Hz) distribution transformers are not anymore suitable for such demanding application, which forces to find new solutions [3]. The future distribution transformer will not only be a voltage adapter but also a voltage regulator, a power factor corrector, a protective device etc. The most feasible configuration of the PET for active distribution networks is a three-stage configuration that is shown in Fig. 1 [4].

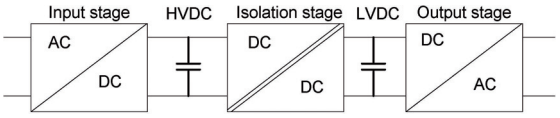


Fig. 1. Three-stage configuration of power electronic transformer.

Three-stage topology consists of an input, isolation- and output-stages. The isolation stage, also known as a dc-dc converter stage, converts HV DC voltage to low voltage (LV) DC voltage. This stage includes a high frequency (4-40 kHz) transformer and two DC-links. The dc-links enhance the ride-through capability of the PET and allow power quality improvement in the input and in the output. Multilevel converter topologies can be implemented in each stage and optimize PET for high voltage or high power applications [5]-[7]. Majority of losses are caused in the isolation stage, which makes it an interesting research object.

Current doubler rectifier (CDR) with the bidirectional energy flow control and reduced output current ripple rates is an attractive candidate for the isolation-stage. However, some serious problems were noticed in the previous research: high voltage peaks and rather low efficiency. In this paper those problems are analyzed in detail and some solutions are proposed. To estimate the efficiency and impact of the component losses on the efficiency the mathematical steady state models were derived. A demonstrator was built to verify the results.

II. CIRCUIT CONFIGURATION

The proposed isolation-stage consists of a controllable full bridge with 4 switches $T_1 \ldots T_4$ with their corresponding anti-parallel diodes $D_1 \ldots D_4$, a high frequency transformer TR and a CDR. To realize the bidirectional energy flow, diodes in a traditional CDR are replaced with the controllable switches T_5 and T_6 and inductors are replaced with the auxiliary transformers TR_{aux1} and TR_{aux2}. Auxiliary transformers secondary windings are connected with the LV port through the diodes. This provides a freewheeling path for the leakage energy in the case of a duty cycle rate lower than 50 %.

978-1-4673-2421-2/12/$31.00 ©2012 IEEE

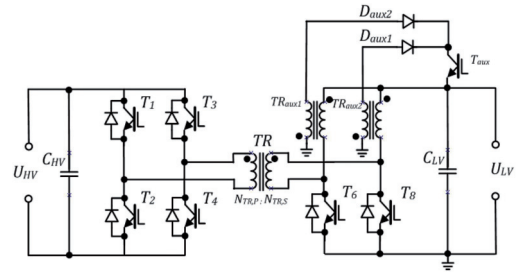


Fig. 2. Electric circuit diagram of the current doubler rectifier with bi-directional energy flow capability.

Two distinct operating modes of the converter are the forward and the reverse operating modes. In the forward operating mode the energy is transferred from the HV side to the LV side. In the reverse operating mode the energy is transferred from the LV side to the HV side.

III. Steady State Analysis with Losses

To model the losses and estimate their effect on the overall efficiency of the converter the steady state analysis was carried out. In the analysis the following losses were taken into account: conduction losses due to collector-to-emitter voltage drop over the IGBT-s (U_{CE}), voltage drop over the freewheeling diodes (U_D), voltage drop due to active resistance of the wires on the HF primary (r_{TR_P}) and secondary (r_{TR_S}) and the auxiliary transformers (r_{aux}). In the steady state analysis both, the forward and the reverse operating modes are handled separately due their different control principles. To simplify the analysis, it is assumed that the auxiliary transformers TR_{aux1} and TR_{aux2}, as well as all transistors $T_1 \ldots T_8$ are identical. For the analysis, the switching losses, the skin and proximity effects in the power switches and in the transformers are neglected. Also, the influence of the leakage inductance in the transformers is neglected.

One operating period T is taken for the basis of the steady state analysis. The operating period of one switch in continuous conduction mode consists of the active state t_A when switch is turned on and the zero state t_Z when the switch is turned off. Such assumption can be expressed as follows:

$$T = t_A + t_Z \tag{1}$$

Equation (1) can also be represented using the duty cycles

$$\frac{t_A}{T} + \frac{t_Z}{T} = D_A + D_Z = 1, \tag{2}$$

where D_A and D_Z are the duty cycles of the active and the zero states of the switch, correspondingly.

In the forward operating mode the effective duty cycle must be used, which is caused by the use of the phase shift modulation strategy. The effective duty cycle D_E is the time when energy is transferred to the HF transformer. The D_E value for the CDR in the forward mode depends on the phase shift value and can roughly be expressed as follows

$$D_E = D_A - \varphi, \tag{3}$$

where φ is the phase shift value in p.u. between the two legs of the FB.

The steady state analysis of both topologies is based on the fact that an average voltage over the auxiliary transformer during one operating period is zero:

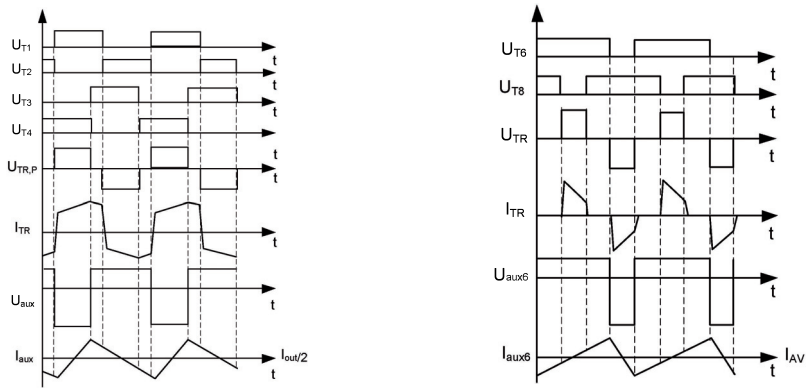
$$U_{TRaux} = \frac{1}{T}\int_{t}^{t+T} u_{TRaux}\,dt = 0 \tag{4}$$

A. Forward operating mode

In the forward operating mode, the energy is transferred from the HV port to the LV port. The typical waveforms and their corresponding gate signals are presented in Fig. 3*a*. The current in the auxiliary transformer is half of the total LV side current, whereas it is determined by the ratio of the LV side voltage and the load resistance. Each diode on the CDR LV side conducts each half cycle. During the effective duty cycle of the transistors T_1 and T_4 the voltage over the auxiliary transformer TR_{aux1} is equal to the difference between the HF transformer's secondary, voltage drop on D_8, r_{TR_S}, r_{aux} and the voltage U_{LV} over the load resistance R (see Fig. 4*a*). During the overlap of the transistors T_1 and T_3 (see Fig. 4*b*) the voltage over the L_{aux1} is equal to the LV side voltage. Next switching cycle is identical with the previous one. The corresponding equivalent circuits are shown in Fig. 4*c*,*d*. It can be seen that voltage over the auxiliary transformer L_{aux1} is equal to the LV side voltage. Thus according to the requirement (4) an equation (5) can be derived considering all the conduction losses in the circuit during one switching period. Eq (6) presents the formulae for estimating the LV side voltage, which is essential in calculating overall efficiency.

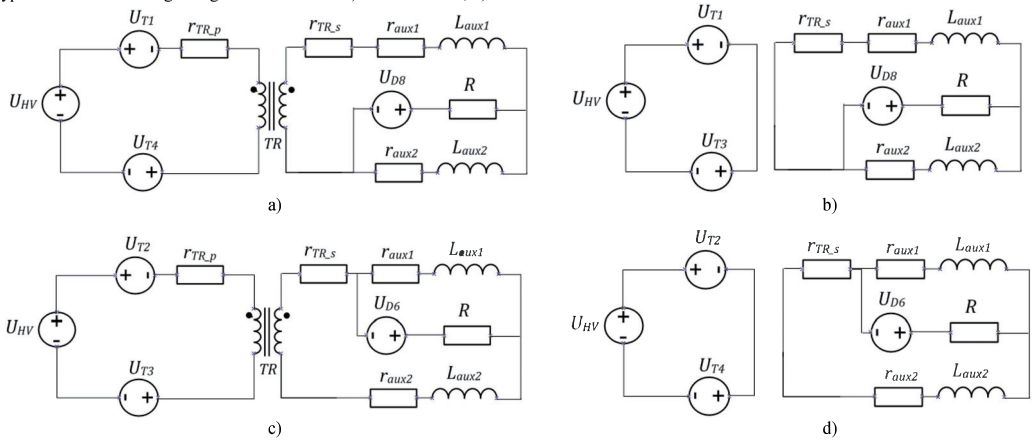
B. Reverse operating mode

In the reverse operating mode the LV side voltage acts like a voltage source and the HV side voltage must be estimated. The lossy model of the CDR in the reverse operating mode is shown in Fig. 3*b*. The voltage over the auxiliary transformer TR_{aux1} is equal to the LV side voltage during the active state of the switch T_6, as shown in Fig. 5*a*. During the overlap of the control signals for T_6 and T_8 the voltage over the auxiliary transformer TR_{aux1} remains the same. During the zero state of switch T_6, the switch T_8 is turned on and the voltage over the auxiliary transformer TR_{aux1} is equal to the difference between the output side voltage and the HF transformer primary voltages. In order to estimate the output power on the HV side the HV side voltage and the current in the auxiliary transformers must be determined. The the amper-second balance of the capacitor current i_C was used for estimation of the current in the auxiliary transformer. According to (4) the equation system for the HV side voltage and the auxiliary current estimation is presented in (7). Eq. (8) presents the solution for the HV side voltage and eq. (9) presents the solution for the current in the auxiliary transformer. Using these two quantities the power on the HV and LV sides can be estimated.



a) b)

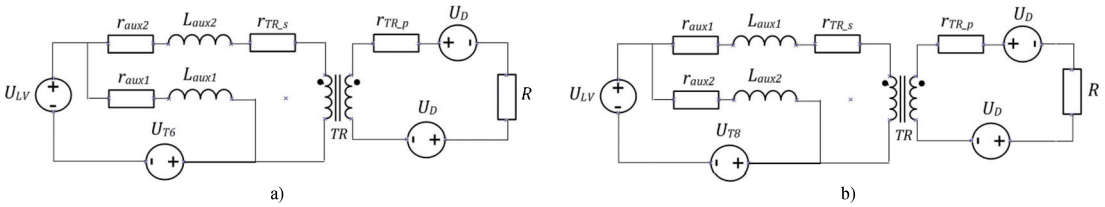
Fig. 3. Typical waveforms and gate signals of the CDR. a) forward mode; b) reverse mode.



a) b)

c) d)

Fig. 4. Switching states of CDR in the forward mode. a) active state of T_1, T_4; b) overlap of T_1, T_3; c) active state of T_2, T_3; d) overlap of T_2, T_4.



a) b)

Fig. 5. Switching states of CDR in reverse mode. a) active state of T_6; b) zero state of T_6.

IV. IMPACT OF COMPONENT LOSSES ON THE EFFICIENCY

In order to facilitate the impact of the component losses on the overall efficiency of the CDR the mathematical models for both operating modes were analyzed in different operating points. The impact of the r_{aux}, U_{CE}, U_D on the overall efficiency was analyzed. Moreover, the analysis was carried out for the different duty cycle D values. To verify the mathematical results on the demonstrator one fixed operating point with determined circuit parameters was selected. The parameters of the circuit as well as the IGBT types and their corresponding drivers are presented in the Table 1. Due to the different control principles of the both operating modes, also different duty cycle values were used. The overall efficiency of the CDR was estimated using the ratio of the output side power P_{OUT} and the input side power P_{IN} (depending on the operating mode of the CDR), that can be written as follows

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{U_{OUT}^{\ 2}}{R \cdot U_{IN} \cdot I_{IN}} \cdot 100\% \qquad (10)$$

$$U_{aux} = \overline{u}_{aux} = -\left[\left(U_{HV} - 2U_{CE} - I_{aux}N_{TR}r_{TR\_P}\right)\cdot N_{TR} - U_{LV} - U_D - I_{aux}\left(r_{aux} + r_{TR\_S}\right)\right]\cdot D_E + \left(U_{LV} + U_D + I_{aux}r_{aux}\right)\cdot\left(1 - D_E\right) = 0 \quad (5)$$

$$U_{LV} = -\frac{2R\cdot\left(U_D + 2N_{TR}U_{CE}D_E - N_{TR}U_{HV}D_E\right)}{D_E\cdot\left(r_{TR\_P}N_{TR}^2 + r_{TR\_S}\right) + 2R + r_{aux}} \quad (6)$$

$$\begin{cases} U_{aux} = \overline{u}_{aux} = \left(U_{LV} - U_{CE} - \dfrac{U_{IHV} - 2U_D + I_{TR\_P}\cdot r_{TR\_P}}{N_{TR}} - I_{aux}\cdot\left(r_{aux} + r_{TR\_S}\right)\right)\cdot\left(1 - D_A\right) + \left(U_{LV} - U_{CE} - I_{aux}r_{aux}\right)\cdot D_A = 0 \\ I_C = \overline{i}_C = \left(\dfrac{I_{aux}}{N_{TR}} - I_{HV}\right)\cdot 2\left(1 - D_A\right) - I_{HV}\cdot\left(2D_A - 1\right) = 0 \end{cases} \quad (7)$$

$$U_{HV} = -\frac{2R(D_A - 1)\cdot(2D_AU_D - 2U_D - N_{TR}\cdot U_{CE} + N_{TR}U_{LV}}{2R + r_{TR\_P} + N_{TR}^2\left[r_{TR\_S}\cdot(1 + D) + r_{aux}\right)\Big] - D\left[2R\cdot(2 + D) + r_{TR\_P}\right]} \quad (8)$$

$$I_{aux} = \frac{N_{TR}\left[2U_D(D - 1) - N_{TR}\left(U_{CE} - U_{LV}\right)\right]}{2R + r_{TR\_P} + N_{TR}^2\left[r_{TR\_S}\cdot(1 + D) + r_{aux}\right)\Big] - D\left[2R\cdot(2 + D) + r_{TR\_P}\right]} \quad (9)$$

TABLE 1.
OPERATING PARAMETERS OF CDR

Parameter	Value	
HV side (U_{HV})	200 V	
LV side (U_{LV})	30 V	
Switching frequency (f_s)	40 kHz	
HF transformer turns ratio (N_{TR})	3	
Inductance of HF transformer (L_m)	1 mH	
Inductance of auxiliary transformer ($L_{трансф}$)	248 μH	
Transformer winding resistances	1 mΩ	
IGBT (IRG7Ph42ud1pbf) saturation voltage (U_{CE})	1.8 V	
Freewheeling diode voltage drop (U_D)	1.1 V	
Duty cycle (D)	0.43 (forw)	0.56 (rev)
IGBT driver type	IR4427 Dual low side driver IR2181 High side driver	

Fig. 6 shows the influence of the winding resistance of the auxiliary transformer r_{aux} on the overall efficiency of the CDR in the forward (see Fig. 6*a*) and in the reverse (see Fig. 6*b*) operating modes. It can be seen that at selected duty cycle rate the efficiency varies in a substantial ranges in both operating modes. In the forward operating mode the efficiency for duty cycle D_E = 0.43 varies between 74…93 % with increase of the resistance from 0…5Ω. In the reverse operating mode at the duty cycle D_A = 0.56 the efficiency varies between 44…92% correspondingly. It can be seen that the resistance of the auxiliary transformer can considerably decrease the efficiency of the CDR, especially in the reverse operating mode. As the CDR is intended to work with high currents on the LV side, then selecting of small winding resistance is of major importance. Difference in the characteristics is caused by the different control principles of the CDR in the both operating modes.

Fig.7 depicts the influence of the collector-to-emitter saturation voltage value on the overall efficiency of the CDR in the forward (see Fig.7*a*) and in the reverse (see Fig.7*b*) operating modes. It can be seen that at the duty cycle D_E = 0.43 the efficiency in the forward operating mode varies from 89…94% with the increase of the U_{CE} value from 0…5 V. In the reverse operating mode at the duty cycle D_A = 0.56 the efficiency varies from 82…98% correspondingly. As converter operates in CCM then the change of the duty cycle value has minor impact on the losses caused by U_{CE}. As expected, the value of the U_{CE} has stronger impact on the efficiency in the reverse mode since these losses occur on the LV side where even the small losses have considerable influence on the power.

Fig.8 depicts the influence of the diode voltage drop on the overall efficiency of the CDR in the forward (see Fig.8*a*) and in the reverse (see Fig.8*b*) operating modes. It can be seen that with the increase of U_D in the range from 0…5 V, the efficiency in the forward operating mode at the duty cycle D_E = 0.43 varies between 81…98 %. In the reverse operating mode at the duty cycle D_A = 0.56 the efficiency varies between 89…94 %. As expected, the diode voltage drop has more significant influence on the efficiency in the forward operating mode since only two diodes conduct on the LV side.

As can be concluded from the previous analysis, the winding resistances r_{aux} reduce the efficiency more considerably than the U_{CE} and U_D values in both operating modes. Moreover, the U_{CE} and U_D values reduced the efficiency more significantly in the reverse operating mode, where higher currents LV side caused higher losses in the power switches.

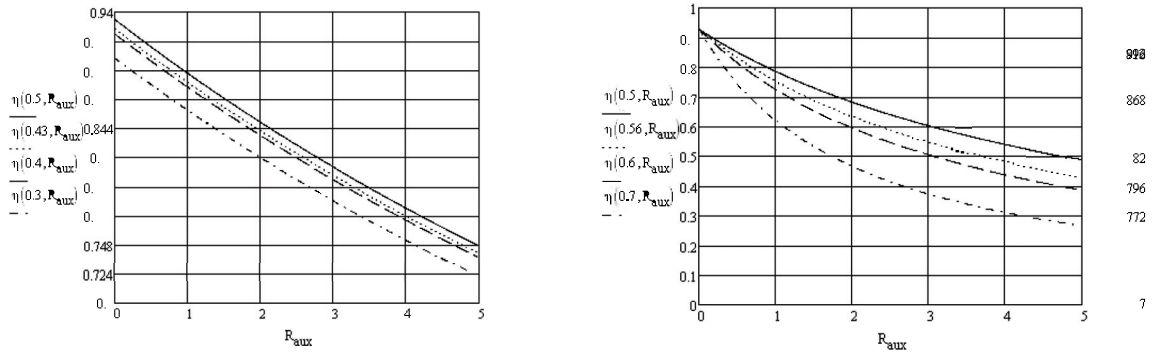


Fig. 6. Impact of the auxiliary transformers winding resistance on the efficiency of CDR with different duty cycle rates. a) forward mode; b) reverse mode.

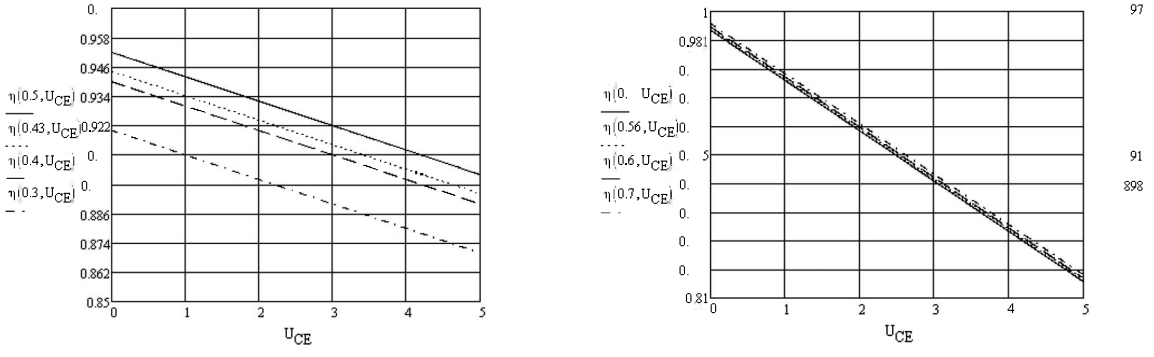


Fig.7. Impact of the collector-emitter voltage drop on the efficiency of CDR with different duty cycle rates. a) forward mode; b) reverse mode.

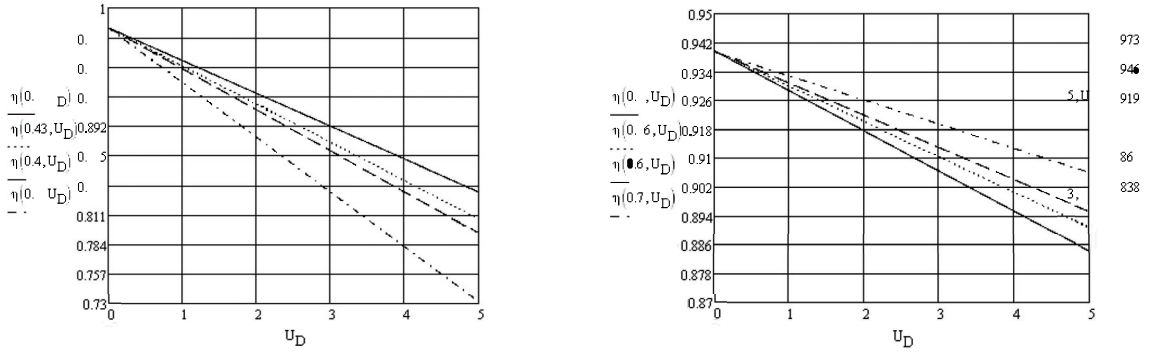


Fig.8. Impact of the diode voltage drop on the efficiency of CDR with different duty cycle rates. a) forward mode; b) reverse mode.

V. SNUBBER CIRCUIT

During the experiments it turned out that selected transformers have significantly high leakage inductance that lead to the occurrence of the high voltage peaks during the turn-off of the switches. These voltage peaks could reach 4 times the voltage over the power switch. Such side effect creates significant constraints in using the bi-directional CDR in the high power applications. Voltage peaks cause additional losses in the converter and increase the voltage stress of the power switches that in turn can lead to their burn-through. One possible approach for minimizing the level of the voltage peaks during the switching transient is to use snubber circuits. The easiest way is to use a passive snubber. A suitable diode-resistor-capacitor (DRC) type snubber for the CDR is shown in Fig. 9 [9].

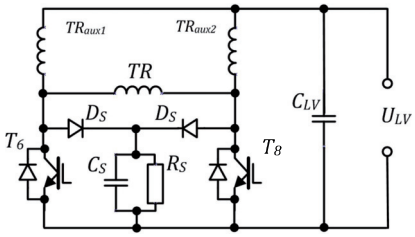


Fig. 9. Simplified schematics of the CDR with DRC snubber circuit.

Such snubber circuit uses two diodes D_S. The anodes are connected to the collector of each IGBT and the cathodes are connected to parallel connected RC circuit. During the voltage peak the energy is transferred from the main circuit to the capacitor bank C_S, afterwards the capacitor is discharged through the resistor R_S. Such snubber was tested on the experimental prototype. Fig. 10*a* depicts the voltage U_{CE} of the transistor T_6 during the switching transient. It can be seen that steady state voltage during the turn off is round 60 V whereas the value of the peak reaches 225 V. The same experiment was carried out with proposed snubber circuit. The switching transient of such circuit is shown in Fig. 10*b*. It can be seen that the value of the peak comprises 125 V in this case which makes it 50 % less than without snubber.

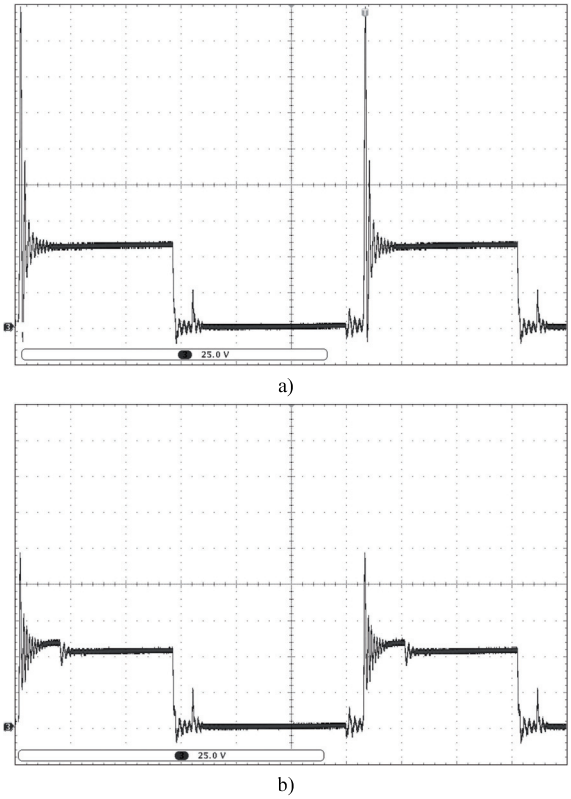


Fig. 10. Voltage over the transistor T_6: a) without snubber; b) with snubber.

VI. Conclusions

In this paper the bi-directional CDR as a candidate topology for the isolation stage of the power electronic transformer was studied. The paper presented the steady state analysis with the lossy model derivation of the CDR in the forward and in the reverse operating modes. The impact of the winding resistance, collector-to-emitter saturation voltage and diode voltage drop on the overall efficiency was analyzed. Mathematical results showed that the value of the r_{aux} has the biggest impact on the overall efficiency in comparison to U_{CE} and U_D. In addition, the higher U_{CE} and U_D values reduced the overall efficiency more significantly in the reverse operating mode rather than in the forward mode. Moreover, the leakage inductance of the auxiliary transformers lead to the occurrence of the high voltage peaks in the transistors that in turn cause voltage stress in the power switches. Therefore a diode-resistor-capacitor type snubber was proposed that reduced the voltage peaks up to 50 %.

The research showed that the efficiency of the bi-directional CDR can be increased up to 92 % in both operating modes. The transistor voltage peaks can be eliminated by proper selection of the snubber parameters. Thus bi-directional CDR can be considered as a suitable topology for the isolation stage of the PET.

Acknowledgment

This research and work has been supported by Estonian Ministry of Education and Research (Project SF0140016s11) and Estonian Science Foundation (Grant ETF8687).

References

[1] W. McMurray, “Power converter circuits having a high-frequency link,” U.S. Patent 3517300, June 23, 1970.

[2] J. L. Brooks, “Solid state transformer concept development,” in Naval MaterialCommand. Port Hueneme, Civil Eng. Lab, Naval Construction Battalion Center, 1980.

[3] T. Zhao, J. Zeng, S. Bhattacharya, M. E. Baran, A.Q. Huang “An Average Model of Solid State Transformer for Dynamic System Simulation”. PES 2009, pp. 1-8.

[4] Merwe, J.W.; du T. Mouton, H.; , "The solid-state transformer concept: A new era in power distribution," AFRICON '09, pp.1-6, 23-25 Sept. 2009

[5] J.-S. Lai, A. Maitra, A. Mansoor, and F. Goodman, “Multilevel intelligent universal transformer for medium voltage applications,” in Proc. IEEE Ind. Appl. Conf., vol. 3, pp. 1893–1899, Oct. 2005

[6] Ronan, E.R., Jr.; Sudhoff, S.D.; Glover, S.F.; Galloway, D.L.; , "Application of power electronics to the distribution transformer" Applied Power Electronics Conference and Exposition, APEC, 15th Annual IEEE, vol. 2, pp.861-867 2000

[7] Haifeng Fan; Hui Li; , "High frequency high efficiency bidirectional dc-dc converter module design for 10 kVA solid state transformer", Applied Power Electronics Conference and Exposition (APEC), 25th Annual IEEE, pp.210-215, 21-25 Feb. 2010

[8] Beldjajev, V.; Roasto, I.; Vinnikov, D.; , "Analysis of current doubler rectifier based high frequency isolation stage for intelligent transformer," Compatibility and Power Electronics (CPE), 2011 7th International Conference-Workshop , vol., no., pp.336-341, 1-3 June

[9] Tolbert, L.M.; Peterson, W.A.; White, C.P.; Theiss, T.J.; Scudiere, M.B.; , "A bi-directional DC-DC converter with minimum energy storage elements," *Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the* , vol.3, no., pp.1572-1577 vol.3, 13-18 Oct. 2002

[PAPER-V] **Beldjajev, V**., Roasto, I. Efficiency and Voltage Characteristics of the Bi-Directional Current Doubler Rectifier. Przeglad Elektrotechniczny, Vol. 88, No. 8, 2012, Poland, pp. 124 – 129.

Viktor BELDJAJEV, Indrek ROASTO

Tallinn University of Technology

Efficiency and Voltage Characteristics of the Bi-Directional Current Doubler Rectifier

Abstract. *This paper presents a detailed analysis of the bi-directional current doubler rectifier (CDR) that is a candidate topology for use in power electronic transformer (PET). Among various advantages the proposed current doubler rectifier offers a bi-directional power flow capability that is the major requirement for the PET. This paper provides the steady state analysis of the CDR in bi-directional operation. Input voltage boost properties of converters are compared for an ideal case. Finally, the impact of losses in the components on the voltage characteristics and efficiency are analysed.*

Streszczenie. *W artykule przedstawiono szczegółową analizę podwajającego prostownika dwukierunkowego (CDR), którego topologia może być użyta do konstrukcji transformatorów energoelektronicznych (PET). Wśród wielu zalet proponowany układ oferuje dwukierunkową możliwości przepływu energii, która jest głównym wymogiem dla PET. Niniejszy dokument przedstawia analizę stanu ustalonego CDR w działaniu dwukierunkowym. Właściwości zwiększania napięcia wejściowego tych przekształtników są porównywane dla przypadku idealnego. W części końcowej przeanalizowano wpływ strat w elementach na charakterystykę napięciową oraz sprawność układu (**Sprawność i charakterystyki napięciowe podwajającego prostownika dwukierunkowego).*

Keywords: bi-directional current doubler rectifier, steady state analysis, loss analysis, efficiency.
Słowa kluczowe: prostownik dwukierunkowy podwajający prąd, analiza stanu ustalonego, analiza strat, sprawność.

Introduction

Switching mode power supplies have been widely used in modern industry products to supply a stable DC voltage. In consideration of cost and efficiency, the conventional hard switching techniques are giving way to more economical topologies where zero voltage switching or zero current switching can be utilized. Typically, the flyback and forward converters are selected for low power applications, and a half bridge converter is used for medium power applications. Half- bridge topology has low cost in comparison to full bridge, however the full-bridge offers better performance in medium and high power applications [1].

Among different soft switching techniques, a full bridge (FB) converter with phase shift was proposed to improve the performance of hard switching converters. The aim of such technique is to achieve soft switching merely by use of only the leakage inductance and output capacitances of the controllable switches. However, the parasitic ringing generated by the large transformer leakage and external inductances and transformers stray capacitance can cause additional EMI problems [2]. One of such topologies, with the full-bridge on the primary side and current doubler rectifier on the secondary side was described in [1], where the ZVS conditions are analysed in a detail. Thorough coverage of the operation of such topology in the forward mode is presented in [3] - [6], where a detailed analysis can be found. However, using CDR in reverse mode has been proposed only by few authors [1], [7] - [9], thus a more detailed analysis is required.

In the current case the main application field is the DC/DC converter of a power electronic transformer (PET). In such application one of the main requirements is the bi-directional power flow capability [10] - [14]. The control task is to keep the voltages on both sides at a constant level. When selecting an appropriate topology it must be kept in mind that different boost factors may become a hindrance to achieving desired functionality. When designing the converter it is also important to take into account that losses in the components reduce the voltage boost and thus converter needs to have sufficient bandwidth to compensate losses. The proposed DC/DC FB converter with the current doubler rectifier (CDR) has a wide voltage regulation capability in a wide duty cycle range. Moreover, it is capable of utilizing the parasitic elements to achieve zero voltage switching.

This paper gives a detailed steady state analysis of the bi-directional CDR considering losses in the elements.

Circuit Configuration

The circuit topology of the proposed DC/DC converter is shown in Fig.1. The circuit consists of the controllable full bridge with 4 switches $T_1 \ldots T_4$ with their corresponding anti-parallel diodes $D_1 \ldots D_4$ and parasitic capacitances, a high frequency transformer TR and a CDR. In order to realize energy flow in two directions the diodes in traditional CDR are replaced with controllable switched T_6 and T_8 and traditional inductors are replaced with auxiliary transformers T_{aux1} and T_{aux2}. Additional auxiliary circuit is added to provide the freewheeling path for the leakage energy of the transformers, in case the duty cycle is lower than 50 % [1]. Auxiliary circuit redirects leakage energy of the transformers back to the low voltage side through the diodes thus preventing dangerous overvoltage to the switches. In addition, the transformers have higher inductance L than inductors used in the traditional CDR. The high frequency isolation transformer provides required voltage gain as well as the galvanic isolation between the input and output sides of the converter.

Two distinct operating modes of the converter are the forward and the reverse operating modes. In forward operating mode the energy is transferred from high voltage FB side to the low voltage side (buck mode). In reverse operating mode the energy is transferred from the low voltage CDR side to the high voltage side (boost mode).

The typical current and voltage waveforms of the converter in forward operating continuous conduction mode are shown in Fig.2. The FB is controlled with phase shifted PWM, with duty cycles near D_A = 0.5, whereas the phase shift determines the effective duty cycle of the converter. Phase shift provides the zero voltage switching capability and desired voltage gain. At the same time, only the diodes and auxiliary transformer primaries conduct on the CDR side. A capacitor is used to smoothen the output voltage.

The typical current and voltage waveforms in reverse operating continuous conduction mode are shown in Fig.3.

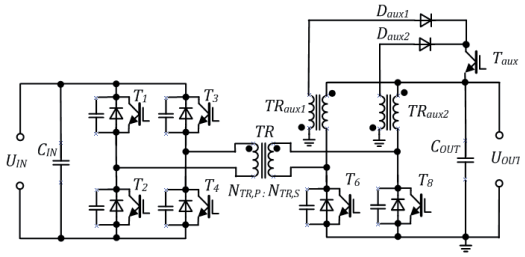


Fig.1. Main circuit of bi-directional current doubler rectifier

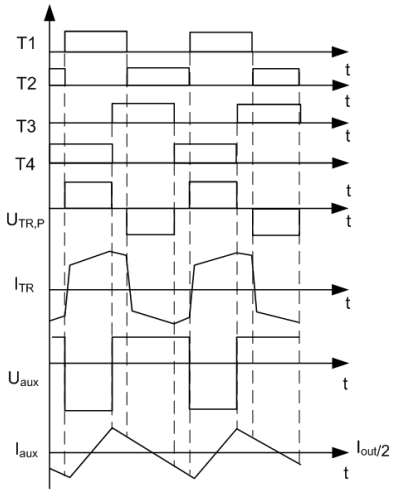


Fig.2. Typical waveforms for CDR in forward operating mode

Switches T_6 and T_8 on the CDR side are controlled with PWM, whereas the duty cycle of the switch can vary from 0…1. If the duty cycle is D_A > 0.5 then auxiliary path is disconnected. The power is transferred to the output during the turn ON of one switch. Energy stored in the auxiliary transformer is redirected into the HF transformer during the overlap of the control signals. At the same time only the diodes conduct on the FB side.

Main benefits of the proposed bi-directional CDR are zero voltage switching capability for the primary switches T_1...T_4 in a wide load range, achievable to utilize the energy stored in the output filter inductances. Moreover, CDR allows bi-directional energy flow control. Using a HF transformer reduces the size of the converter. Reduced current ripples due to the transformers and offer better thermal performance due to the current doubling effect. In addition the CDR has reduced transient response [1].

Steady State Analysis of the CDR

In the steady state analysis both the forward and the reverse operating modes are handled separately due their different control principles. To simplify the analysis, it is assumed that the auxiliary transformers TR_{aux1} and TR_{aux2}, as well as all transistors T_1…T_8 are identical (the same collector-emitter and freewheeling diode voltage drops). For the analysis, the skin and proximity effects in transformers are neglected.

The operating period T of one switch in the continuous conduction mode consists of active state t_A and zero state t_Z:

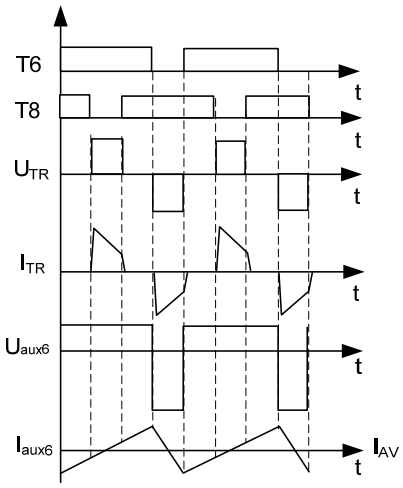


Fig.3. Typical waveforms for CDR in reverse operating mode

(1) $$T = t_A + t_Z$$

Equation (1) can also be represented with duty cycles

(2) $$\frac{t_A}{T} + \frac{t_Z}{T} = D_A + D_Z = 1,$$

where D_A and D_Z are the duty cycles of an active and zero states of a switch, correspondingly.

In the forward mode the effective duty cycle must be used. The effective duty cycle D_E for the CDR in forward mode depends on the phase shift value and can roughly be expressed by

(3) $$D_E = D_A - \varphi\,,$$

where φ is the phase shift value in p.u. between the two legs of FB.

The steady state analysis of both topologies is based on the fact that an average voltage over the auxiliary transformers during one operating period is zero:

(4) $$U_{TRaux} = \frac{1}{T}\int_{t}^{t+T} u_{TRaux}\,dt = 0\,,$$

In the forward operating mode, the current in the auxiliary transformer is half of the output current, whereas the output current is determined by the ratio of the output voltage and the load resistance. Each diode in the CDR conducts each half cycle. The four basic equivalent circuits for forward operating mode are shown in Fig.4. More detailed analysis can be found in [2], [5]. During the effective duty cycle the voltage over the auxiliary transformer TR_{aux1} is equal to the difference between the HF transformer's secondary and output voltages (see Fig.4, a). During this period the transformer secondary voltage is equal to multiplication of the input side voltage and transformer turns ratio.

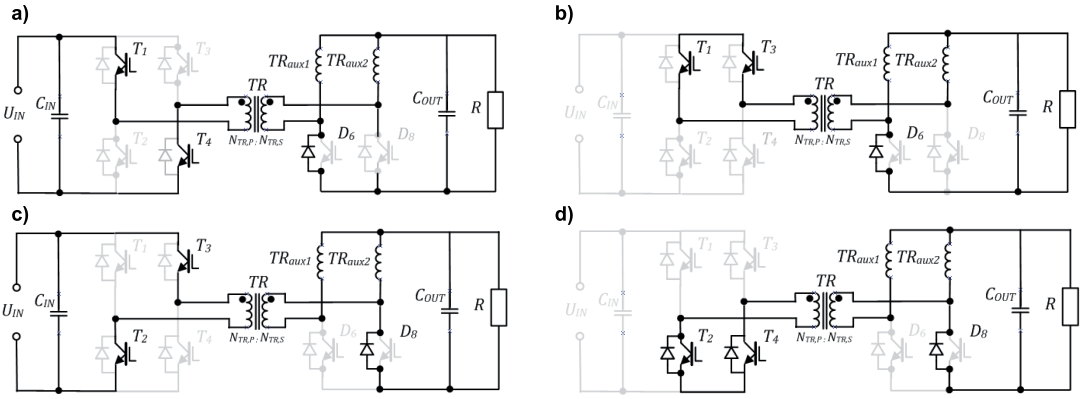


Fig. 4. Switching states of CDR in forward mode. a) active state of T_1, T_4; b) overlap of T_1, T_3; c) active state of T_2, T_3; d) overlap of T_2, T_4

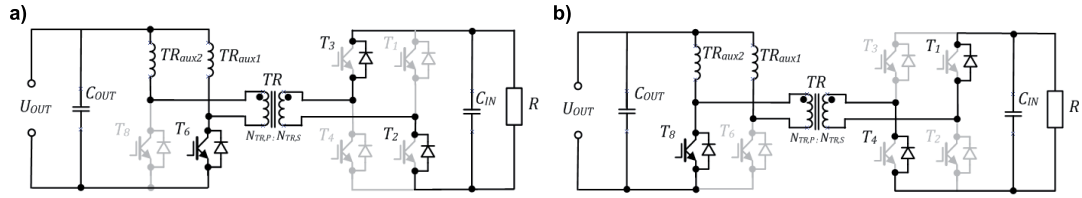


Fig. 5. Switching states of CDR in reverse mode. a) active state of T_6; b) zero state of T_6.

During the overlap of the transistors T_1 and T_3 (see Fig.4, b) the voltage over the TR_{aux1} is equal to the output voltage. Next half switching cycle is similar to previous one, and voltage over the auxiliary transformer TR_{aux1} is equal to the output voltage. During the rest of the period the voltage over the auxiliary transformer is equal to the output voltage. Thus according to the requirement (4) we get

$$(5) \qquad \left(U_{IN} \cdot N_{TR} - U_{OUT}\right) \cdot D_E + U_{OUT} \cdot (1 - D_E) = 0$$

where N_{TR} is the transformers turns ratio, U_{IN} is the voltage on the input side and U_{OUT} voltage on the output side of the converter. From here the output voltage can be evaluated as follows

$$(6) \qquad U_{OUT} = U_{IN} \cdot N_{TR} \cdot D_E$$

In the reverse operating mode the output side voltage acts now like a source and the input side voltage must be estimated. Voltage over the auxiliary transformer is equal to the output side voltage during the active state of the switch T_6, as shown in Fig.5, a. During the overlap of the control signals for T_6 and T_8 the voltage over the auxiliary transformer TR_{aux1} remains the same as can be seen in Fig.3. During the zero state of switch T_6 the voltage over the auxiliary transformer TR_{aux1} is equal to the difference between output side voltage and HF transformer voltage. Equation for the voltage over the auxiliary transformer with $D_A > 0.5$, considering also requirement (4), can be written in a following way

$$(7) \qquad U_{OUT} \cdot D_A + \left(U_{OUT} - \frac{U_{IN}}{N_{TR}}\right) \cdot D_Z = 0\,,$$

from where the input side voltage can be derived:

$$(8) \qquad U_{IN} = \frac{U_{OUT} \cdot \left(D_A + D_Z\right)}{D_Z} \cdot N_{TR} = \frac{U_{OUT} \cdot N_{TR}}{1 - D_A}$$

Impact of Component Losses

In the previous section the lossless models of the CDR were presented. However in practise the voltage boost properties of CDR can be seriously affected by the losses in the components. Moreover, the DC/DC stage of PET comprises the biggest part of overall losses [14]. In the DC/DC stage the following losses are present: conduction losses of the passive and active components, switching losses and core losses. Conduction losses are caused by active resistances in the wires, transformer windings and switches (collector-to-emitter voltage drop, reverse recovery diode voltage drop). Switching losses comprise the turn-on, turn-off and diode reverse recovery losses. The core losses occur in the HF and auxiliary transformers. Previous steady-state analysis included only the analysis of conduction losses.

The conduction losses are more critical on the low voltage and higher current side, where voltage drops over the elements affect the efficiency significantly. For more careful estimation of the operating characteristics of the converter the loss elements, such as winding resistances in the transformers and voltage drops in semiconductors, should be added to the model. In the following analysis the winding losses in auxiliary transformers are represented by the resistance r_{aux}, winding resistance on transformer primary r_{TR_P} and on transformer secondary r_{TR_S}, voltage drop in diodes during the conduction state is U_D. In addition, IGBTs with saturation voltage U_{CE} were used.

As the converter is intended to be used in the isolation stage of power electronic transformer, it is necessary for the converter to keep specified voltage levels on both sides. The specified voltage levels for input and output sides are as follows

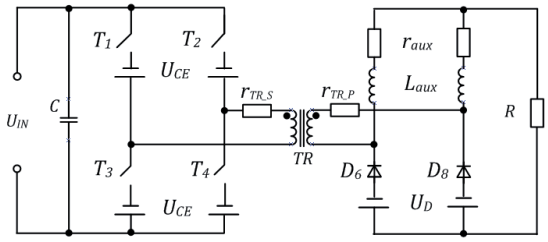


Fig. 6. Equivalent circuit of the lossy model of the CDR. a) forward mode; b) reverse mode

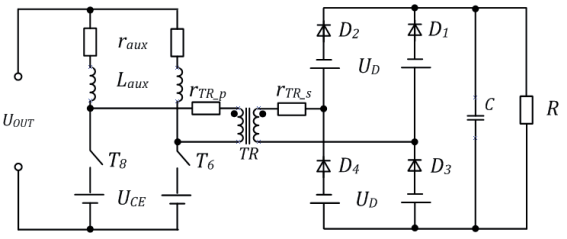


Fig. 7. Equivalent circuit of the lossy model of the CDR. a) forward mode; b) reverse mode

U_{IN} = 200 V; U_{OUT} = 30 V

In the case of reverse operating mode the output side is handled as an input. In further examples the duty cycles for each operating mode are selected so that desired voltage level could be achieved. It must be noticed that the losses can significantly reduce the voltage gain of the converter, thus the required duty cycle must always be bigger than the one obtained with (6) or (8).

Forward Operating Mode

The equivalent circuit considering the losses in components for forward operating mode is shown in Fig.6. On FB side the losses occur due to collector-to-emitter voltage drops U_{CE} of transistors $T_1 \ldots T_4$. On the CDR side the diode voltage drop U_D occurs in diodes D_6, D_8. All transformers have also voltage drop due to winding resistances. The equation (5) can now be extended with adding the losses in the components. And thus we get equation (9), where R designates the load resistance. Output voltage can be thus evaluated according to (10). The current in auxiliary transformer is half the output current.

In order to demonstrate the impact of losses in the components on the voltage characteristics in forward operating mode, then investigated topology is compared mathematically with following parameters:

U_{IN} = 200 V; U_{CE} = 1.8 V; U_D = 1.6 V;

R = 10 Ω; r = 1 mΩ; D_E = 0.45; N_{TR} = 1/3;

where r designates the winding resistance values for auxiliary transformers, and HF transformer resistances on both sides. The corresponding dependency is shown in Fig.8, a. It can be seen that losses become more significant with the increase of the power (duty cycle) and decrease the voltage boost in comparison to the ideal case.

Reverse operating mode

In the reverse operating mode the energy is transferred from the low voltage output side to the high voltage input side. The equivalent circuit considering the losses in the components is shown in Fig.7. In this case, the collector-to-emitter voltage drop U_{CE} occurs in the transistors T_6, T_8 on CDR side and voltage drop U_D occurs in the diodes $D_1 \ldots D_4$ on FB side. As the converter operates with the duty cycle $D_A > 0.5$ then the auxiliary path is disabled and thus not shown in the drawing.

(9) $$U_{aux} = -\left[\left(U_{IN} - 2U_{CE} - I_{aux}N_{TR}r_{TR\_P}\right)\cdot N_{TR} - U_{OUT} - U_D - I_{aux}(r_{aux} + r_{TR\_S})\right]\cdot D_E + \left(U_{OUT} + U_D + I_{aux}r_{aux}\right)\cdot\left(1 - D_E\right) = 0$$

(10) $$U_{OUT} = -\frac{2R\cdot(U_D + 2N_{TR}U_{CE}D_E - N_{TR}U_{IN}D_E)}{D_E\cdot\left(r_{TR\_P}N_{TR}^2 + r_{TR\_S}\right) + 2R + r_{aux}}$$

(11) $$\begin{cases} U_{aux} = \left(U_{OUT} - U_{CE} - \dfrac{U_{IN} - 2U_D + I_{TR\_P}\cdot r_{TR\_P}}{N_{TR}} - I_{aux}\cdot(r_{aux} + r_{TR\_S})\right)\cdot(1 - D_A) + \left(U_{OUT} - U_{CE} - I_{aux}r_{aux}\right)\cdot D_A = 0 \\ I_C = \left(\dfrac{I_{aux}}{N_{TR}} - I_{IN}\right)\cdot 2(1 - D_A) - I_{IN}\cdot(2D_A - 1) = 0 \end{cases}$$

(12) $$U_{IN} = -\frac{2R(D_A - 1)\cdot(2D_AU_D - 2U_D - N_{TR}\cdot U_{CE} + N_{TR}U_{OUT}}{2R + r_{TR\_P} + N_{TR}^2\left[r_{TR\_S}\cdot(1 + D) + r_{aux}\right)\Big] - D\left[2R\cdot(2 + D) + r_{TR\_P}\right]}$$

(13) $$I_{aux} = \frac{N_{TR}\left[2U_D(D - 1) - N_{TR}(U_{CE} - U_{OUT})\right]}{2R + r_{TR\_P} + N_{TR}^2\left[r_{TR\_S}\cdot(1 + D) + r_{aux}\right)\Big] - D\left[2R\cdot(2 + D) + r_{TR\_P}\right]}$$

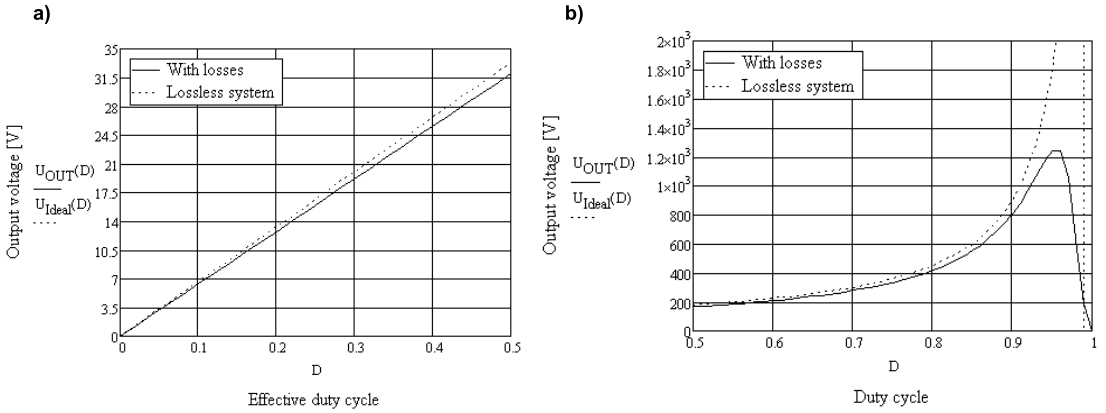


Fig. 8. Comparison of idealized and practical output characteristics of the CDR. a) forward mode; b) reverse mode.

The equation (7) can now be extended to adding the losses of all elements. In order to solve the equation, the current in auxiliary transformer is also needed to be estimated. This can be achieved from the capacitor current, which average is equal to zero over the whole switching period. Eq (11) presents the corresponding equation system. Solving this equation system gives us the solution for the input side voltage which can be estimated according to (12). The current in auxiliary transformer can be obtained with (13). Current on the output side is thus twice the auxiliary current.

In order to demonstrate the impact of losses in the reverse operating mode, then investigated topology is compared mathematically with the following parameters:

U_{IN} = 200 V; U_{CE} = 1,8 V; U_D = 1,6 V;

R = 100 Ω; r = 1 mΩ; D_E = 0.55; N_{TR} = 3;

The corresponding dependency is shown in Fig.8, b. It can be seen that without losses the voltage boost can be infinitely high. However, in the high duty cycle region losses become very significant and thus reduce the voltage boost rapidly to zero.

Efficiency estimation

In the following section the efficiency is estimated using the mathematical model and experimental results. The models were verified on the 1 kW experimental prototype. The 6 IGBTs with switching frequency of 40 kHz are used. The parameters of the experimental prototype are presented in Table 1 and a picture of the prototype is shown in Fig.9. The voltage and current waveforms on the input and output side in forward mode are shown in Fig.10. Same characteristics for reverse mode are shown in Fig.11. It can be seen that specified voltage levels are effectively achieved on both sides of the converter.

The overall efficiency of the CDR can be estimated using the ratio of the output power P_{OUT} and the input power P_{IN},

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{U_{OUT}^{2}}{R \cdot U_{IN} \cdot I_{IN}} \cdot 100\% \quad (14)$$

By inserting the equations (10), (12), (13) into (14), the efficiency of the converter in both operating modes was calculated. The results are presented in the Table 2. In forward mode the efficiency 86.7% was achieved while in the reverse mode this number is only 72.6 %. This difference can be explained with higher conduction losses in the CDR due to higher currents during reverse mode. The difference between mathematical and experimental results can be explained with the fact, that mathematical model did not take switching and core losses of the transformers into account.

Table 1. The parameters of the experimental prototype

Parameter	Value	
Input side voltage (U_{IN})	200 V	
Output side voltage (U_{OUT})	30 V	
Switching frequency (f_s)	40 kHz	
HF transformer turns ratio (N_{TR})	3	
Inductance of HF transformer (L_μ)	1 mH	
Inductance of auxiliary transformer ($L_{\mu aux}$)	248 µH	
Transformer winding resistances	10 mΩ	
IGBT (IRG7Ph42ud1pbf) saturation voltage (U_{CE})	1,8 V	
Freewheeling diode voltage drop (U_D)	1,6 V	
Duty cycle (D)	0.43 (forw)	0.56 (rev)
IGBT driver type	IR4427 Dual low side driver IR2181 High side driver	

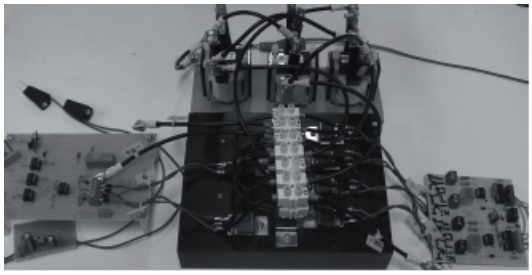


Fig. 9. Experimental prototype of CDR

High voltage peaks were observed in the input and output voltages, as shown in Figs.10 and 11. Those peaks, typical to current doubler rectifier, are caused by the auxiliary transformers T_{aux1}, T_{aux2}. The problem could be solved by implementing proper snubbers.

Table 2. The efficiency of the CDR in defined operating point

Operating mode	Forward	Reverse
Estimated	86.7 %	72.6 %
Experimental	80.7 %	64 %

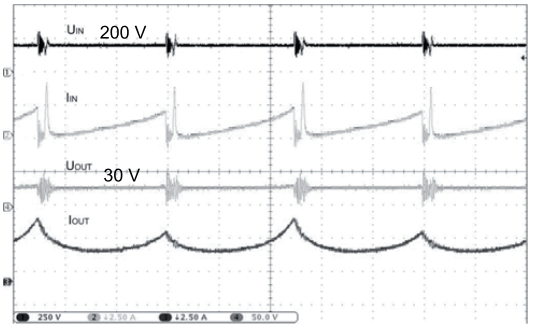


Fig. 10. Input and output side voltage and current waveforms in forward mode

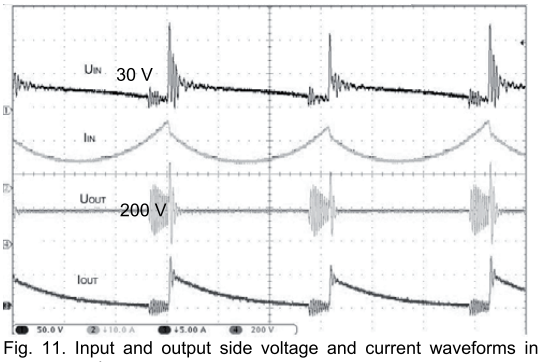


Fig. 11. Input and output side voltage and current waveforms in reverse mode

Conclusion

The paper presented a detailed analysis of the voltage characteristics of the CDR in forward and reverse operating modes. Special attention was paid on the voltage characteristics and efficiency of the investigated topology. Bi-directional CDR as a candidate topology for a DC/DC stage of the power electronic transformer (PET) is the most critical part of the system considering the overall efficiency. In the steady state analysis mathematical models with and without losses were derived and analysed. It was found that for the same operating parameters the converter can operate at the maximum efficiency of 87 % in forward mode and with 72.6 % in reverse mode. The results were verified on the experimental prototype, where the measured efficiencies are 80.7 % and 64 % correspondingly. Voltage characteristics were studied and quite high voltage peaks were observed in the input and output voltage.

In general, relatively low efficiency and high voltage peaks could hinder use of such converter in PET. Future work will include further investigation of CDR to improve its voltage characteristics and efficiency, with proper selection of components and by adding snubber circuits.

Acknowledgement

This research was supported by Estonian Ministry of Education and Research (Project SF0140016s11), Estonian Science Foundation (Grant ETF8687) and European Social Fund´s project Doctoral School of Energy and Geotechnology II.

REFERENCES

[1] Lin, B.-R; Huang, K; Wang, D.; , " Analysis and implementaton of full bridge converter with current doubler rectifier," Proc. IEE Electric Power Appl., vol. 152, no. 5, pp. 1193-1202, 2005.

[2] Chiu, H.J.; Lin, L.W.; Su, Y.C.;Mou, S,C.; , " A phase shfted zero voltage transition full bridge converter with current doubler synchrnous rectification," SICE 2004 Annual Conference, vol. 1, pp. 60-65, 2004.

[3] Beldjajev, V.; Roasto, I.; Vinnikov, D.; , "Analysis of current doubler rectifier based high frequency isolation stage for intelligent transformer," Compatibility and Power Electronics (CPE), 2011 7th International Conference-Workshop , vol., no., pp.336-341, 1-3 June 2011

[4] Kutkut, N.H.; Luckjiff, G.; "Current mode control of a full bridge DC-DC converter with a two inductor rectifier" PESC '97 Page(s): 203 -209 vol.1

[5] Kutkut, N.H.; "A full bridge soft switched telecom power supply with a current doubler rectifier" INTELEC 97., 19-23 Oct 1997 Page(s):344 -351

[6] Kutkut, N.H.; Divan, D.M.; Gascoigne, R.W.; "An improved full bridge zero-voltage switching PWM DC-DC converter using a two inductor rectifier "Industry Applications Society Annual Meeting, 1993., Conference Record of the1993 IEEE,2-8 Oct1993,Page(s):1065- 1072vol.2

[7] Flores, L.A.; Garcia, O.; Oliver, J.A.; Cobos, J.A. "High Frequency Bi-Directional DC/DC Converter Using Two Inductor Rectifier". IECON 2006, pp. 2793 – 2798.

[8] Liang, Y.; Lehman, B. Isolated Two-Inductor Boost Converter with One Magnetic Core. APEC '03. IEEE, pp. 879 – 885.

[9] Yungtaek, Y.; Jovanovic, M. M. New Two-Inductor Boost Converter with Auxiliary Transformer. Power Electronics, IEEE Transactions on vol. 19, Issue 1, Jan. 2004, pp. 169 – 175.

[10] van der Merwe, J.W.; du T. Mouton, H.; , "The solid-state transformer concept: A new era in power distribution," AFRICON, 2009. AFRICON '09. , vol., no., pp.1-6, 23-25 Sept. 2009.

[11] Heinemann, L.; Mauthe, G.; , "The universal power electronics based distribution transformer, an unified approach," Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual , vol.2, no., pp.504-509 vol.2, 2001.

[12] Falcones, S.; Xiaolin Mao; Ayyanar, R.; , "Topology comparison for Solid State Transformer implementation," Power and Energy Society General Meeting, 2010 IEEE , vol., no., pp.1-8, 25-29 July 2010.

[13] Hengsi Qin; Kimball, J.W.; , "A comparative efficiency study of silicon-based solid state transformers," Energy Conversion Congress and Exposition (ECCE), 2010 IEEE , vol., no., pp.1458-1463, 12-16 Sept. 2010.

[14] Beldjajev, V.; Roasto, I.; Lehtla T.; , "Intelligent Transformer: Possibilities and Challenges" RTU, 2011. , pp . 14 Okt 2011.

***Authors**: M. Sc, Dipl. Ing. Viktor Beldjajev, Tallinn University of Technology, Dep. of Electrical Drives and Power Electronics, Ehitajate Tee 5, Tallinn Estonia. E-mail: vbeldjajev@gmail.com; PhD, Dipl. Ing. Indrek Roasto, Tallinn University of Technology, Dep. of Electrical Drives and Power Electronics, Ehitajate Tee 5, Tallinn Estonia. E-mail: indrek.roasto@ieee.org*

[PAPER-VI] **Beldjajev, V**., Roasto, I., Zakis, J. Impact of Component Losses on the Efficiency of a New Quasi-Z-Source Based Dual Active Bridge. Doctoral school of Computing, Electrical and Industrial Systems DoCEIS 2013, IFIP AICT 394, Portugal, pp 485 - 492

Impact of Component Losses on the Efficiency of a New Quasi-Z-Source-Based Dual Active Bridge

Viktor Beldjajev, Indrek Roasto, and Janis Zakis

Tallinn University of Technology, Tallinn, Estonia
vbeldjajev@gmail.com, {Indrek.Roasto,Janis.Zakis}@ieee.org

Abstract. The paper analyzes the impact of the component losses on the efficiency of the novel DC/DC converter. The converter is a combination of the quazi-Z-source (qZS) network and dual active bridge (DAB). In the analysis the mathematical loss models of the proposed DC/DC converter are derived and efficiency is estimated. Eventually the efficiency is verified experimentally.

Keywords: quazi-Z-source inverter, dual active bridge, power electronic transformer.

1 Introduction

During the last decades the bi-directional DC/DC converters have become key components in alternative energy systems. The aim of such converters is to control the electric power flow between the sources and loads, keeping the output voltage on the required level. This paper proposes a novel bi-directional DC/DC converter topology that consists of the quazi-Z-source network, dual active bridge and a high frequency transformer. A possible application of such converter is the isolation stage of the new power electronic transformer (PET) topology where the power flow control capability between two different voltage buses and high efficiency are the major requirements [1-3]. In general, the power flow through the transformer can be controlled by means of voltage elevation on one side or by applying a phase shift control of the inverter bridges on both sides of the transformer. The phase shift control of DAB allows the zero voltage switching to be achieved, that results in reduced switching losses and higher efficiency. In addition, the voltage boost properties of the qZS network allows the voltage on the DC bus to be kept on the constant level that results in lower current stress on the switches. This paper analyzes the converter operation under such conditions when the power flow is controlled only by the phase shift technique. First the loss models are presented according to the waveforms and steady state analysis. Also the impact of the conduction losses of the components on the efficiency characteristics is presented. The obtained efficiency is verified experimentally.

2 Relationship to Internet of Things

Nowadays, the global power system can be described by steadily growing number of renewable energy resources and emerging DC loads on the residential level.

L.M. Camarinha-Matos, S. Tomic, and P. Graça (Eds.): DoCEIS 2013, IFIP AICT 394, pp. 485–492, 2013.

Continuously developing semi-conductor technology and information internet has inspired the idea of the "Energy Internet" concept that may change energy industry from the centralized system to the client-based distributed infrastructure, improving this way the efficiency of the power grid through optimal management of the energy routers. Energy router, a PET-based device that exchanges the energy between the sources, storage devices, DC loads and end-users, is one of the most critical elements of the Energy Internet. The PET is expected to have a bi-directional power flow, high power conversion and power quality enhancement capabilities, plug and play interface and optimal energy management [4]. The paper contributes to the development of the energy router, by analyzing the suitable DC/DC converter for the power conversion.

3 Operating Principle of the Converter

The circuit of the proposed converter, including the conduction losses in the components is shown in Fig.1. Following conduction losses are considered: the collector-to-emitter voltage drop of the IGBT (U_{CE}), diode voltage drop (U_D) and the winding resistance of the inductors L_1 and L_2 (r_L). The converter can operate in both directions, in the forward and in the reverse operating mode. In the forward operating mode the energy is transferred from the HV side towards the LV side. The transistors $T_5 \ldots T_8$ on the HV side and $T_1 \ldots T_4$ on the LV side are switched in pairs using the positive phase shift angle φ. In the forward operating mode the diode Din the qZS network must be shunted with a switch S in order to allow the power flow to the LV side. In the reverse operating mode the energy is transferred from the LV side towards the HV side. The transistors $T_1 \ldots T_4$ on the LV side and transistors $T_5 \ldots T_8$ on the HV side are switched in pairs using the negative phase shift angle φ as shown in Fig.2*a.* The switch S must be in the opened state. The voltage on the LV side DC link can be elevated by the qZS network. Therefore a shoot-through switching state of the inverter switches is introduced, when both switches on one leg (or all 4 switches) conduct simultaneously [5]. During the shoot-through state the energy is stored in the inductors L_1 and L_2 and transferred to the DC link during the active state. The research in [6] stated that adding additional phase shift angle φ to the HV side bridge gate signals during the shoot-through state on LV side allows the power of the converter to be adjusted. Proposed technique is shown inFig.2*b*. Moreover, the additional phase shift can reduce the conduction losses in the transformer that are caused by the circulating current during the shoot through state of the low voltage side inverter (transformer is short circuited).Considering N_{TR} as the transformer's turns ratio, the best performance of the phase shift control and the lowest current stress on the switches is achieved if the converter is designed according to the requirement

$$U_{DC} = N_{TR} U_{HV} \tag{1}$$

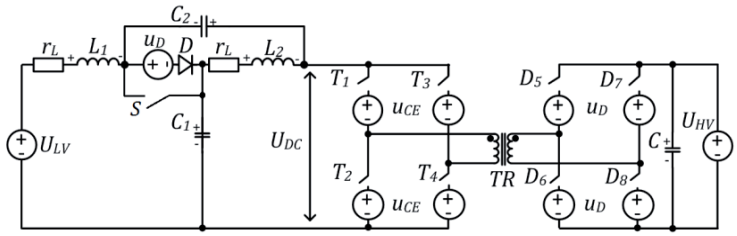
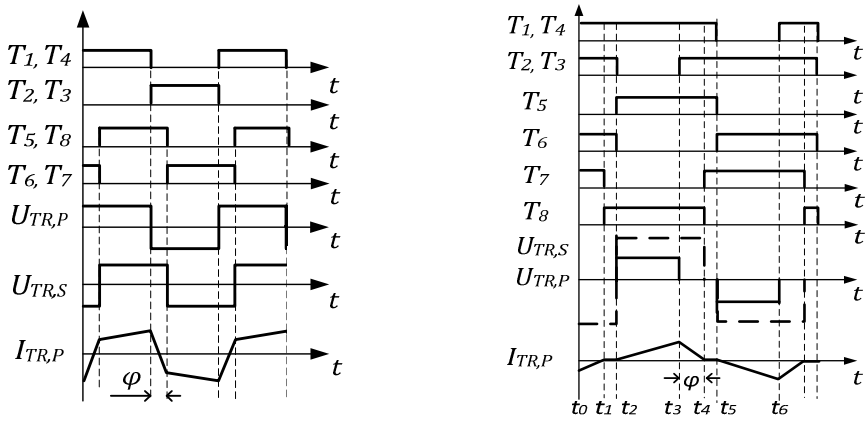


Fig. 1. Circuit of qZS-DAB converter with the losses in the components



a) b)

Fig. 2. Waveforms of the qZS-DAB converter in the reverse operating modes: a) operation under normal conditions, b) voltage boost mode

4 Impact of the Component Losses on the Output Power

In order to facilitate the impact of the component losses on the output power of the qZS based DAB, the mathematical models were derived based on the steady state analysis of the qZS inverter [7] and DAB [8]. Selected circuit parameters are shown in Table 1.

Table 1. The circuit parameters of the qZS-DAB converter

Parameter	Value
HV side voltage U_{HV}	90 V
LV side voltage U_{LV}	30 V
Switching frequency f_s	20 kHz
MF transformer turns ratio N_{TR}	1/3
Leakage inductance of MF transformer L_{TR}	10μH
Resistance of the inductors L_1 and L_2 r_L	150mΩ
IGBT saturation voltage U_{CE}	1.8 V
Diode voltage drop U_D	1.1 V

4.1 Normal Mode

In the normal mode the voltage on the DC link is at the desired level and conventional phase-shift control method is used to transfer the power. The operating period T consist of the active state of the transformer and power transferred from the low voltage side to the high voltage side can be evaluated as follows

$$P_{loss} = \frac{N_{TR}\left(U_{HV} - 2U_D\right)\cdot\left(U_{LV} - 2U_{CE}\right)D_\varphi\left(1-\left|D_\varphi\right|\right)}{2f_S L_{TR}}, -1 \le D_\varphi \le 1. \quad (2)$$

where D_φ is the phase shift duration, f_S is the switching frequency and L_{TR} is the leakage inductance of the medium frequency (MF) transformer.

4.2 Voltage Boost Mode

In the voltage boost mode the voltage on the DC link can be elevated to match the desired level. The operating period T of the MF transformer consists of an active state t_A and a shoot through state t_S that can also be represented with the duty cycles

$$\frac{t_A}{T} + \frac{t_S}{T} = D_A + D_S = 1. \quad (3)$$

A phase shift D_φ is added to gate signals to adjust the power level of the converter as shown in Fig 2*b*.The power transferred from the LV side to the HV side can be evaluated as follows

$$P_{loss} = \frac{\left(U_{DC} - 2U_{CE}\right)\left(2N_{TR}\left(U_{HV} - 2U_D\right) - \left(U_{DC} - 2U_{CE}\right)\right)D_\varphi\left(1 - D_S\right)}{4f_S L_{TR}}. \quad (4)$$

In order to estimate the DC link voltage and thus the output and input power of the converter the equation system (5) can be composed based on the shoot-through (see Fig. 3*a*) and active (see Fig. 3*b*) switching states.

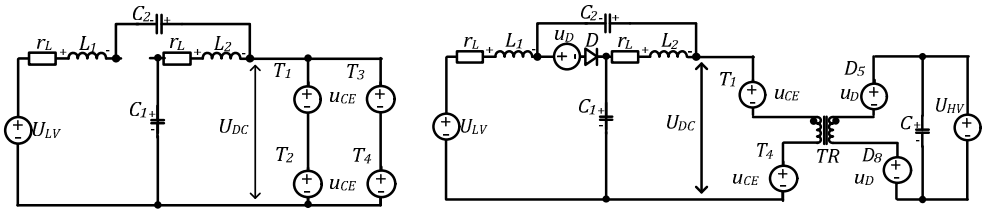


Fig. 3. Switching states of qZS in voltage boost mode: a) shoot through state, b) active state

$$\begin{cases} u_{L1} = (U_{C2} + U_{LV} - U_{CE} - I_L r_L) D_S + (U_{LV} - U_{C1} - U_D - I_L r_L)(1 - D_S) = 0 \\ u_{L2} = (U_{C1} - U_{CE} - I_L r_L) D_S + (-U_{C2} - U_D + I_L r_L)(1 - D_S) = 0 \\ U_{C1} + U_{C2} + U_D - U_{DC} = 0 \\ i_{C2} = I_L D_S + (I_{TR} - I_L)(1 - D_S) = 0 \end{cases} \quad (5)$$

Solving the equation system the DC link voltage can be obtained as follows

$$U_{DC} = \frac{U_{LV} - 2I_{TR} r_L D_S (1 - D_S) - U_D - 2U_{CE} D_S}{1 - 2D_S}, \quad (6)$$

where the I_{TR} is the average transformer current during half-period and it can be obtained from (4) and (5) in a following way

$$I_{TR} = \frac{P_{loss}}{U_{DC} - 2U_{CE}}. \quad (7)$$

As can be seen from (6) the impact of component losses on the U_{DC} depends on the shoot-through duty cycle duration. According to (7) the transformer average current depends on the transferred power and is inversely proportional to the voltage value on the DC link and voltage drop of the IGBT.

Typicallya drawback of the DAB is the increase of the current stress due to the voltage variation on the DC buses, however the DAB extended with the additional qZS network allows the current stress on the switches to be reduced. The current stress on the switchesT_1 and T_5, obtained with the simulation results for determined circuit parameters, is presented in Table 2. According to the simulation results, the current stress on the LV side switches can be reduced from 29 A in case of the DAB to 22 A when the qZS-DAB operates in the voltage boost mode. Moreover, in the voltage boost mode the current on the HV side switches can be reduced from 3A to 0.5A that in turn results in smaller conduction and switching losses.

Table 2. Current stress in the switches

	I(T_1)	**I(T_5)**
Conventional DAB	29.3 A	3.07 A
qZS-DAB (normal mode)	27.6 A	3.4 A
qZS-DAB (boost mode)	22 A	0.5 A

5 Impact of the Component Losses on the Efficiency

In order to facilitate the influence of the component losses on the efficiency of the qZS based DAB the derived mathematical models were analyzed for different component values at varying phase shift duty cycles. The output and input power was estimated and the efficiency was obtained according to the following equation

$$\eta = \frac{P_{OUT}}{P_{IN}} \cdot 100\% \,. \tag{11}$$

The Fig.4 depicts the influence of the U_{CE} on the efficiency of the converter for different phase shift values. It can be seen that the increase of the U_{CE} from 0…3 V decreases the efficiency from 0.95…0.73. Increasing the input voltage would result in a higher efficiency and relatively smaller impact of the U_{CE}. The influence of the active resistance of the inductors is shown in the Fig.5. For the given circuit parameters the increase of the r_L from 0…1 reduces the converter efficiency from 0.85…0.61 for normal mode and from 0.82…0.77 for the voltage boost mode. The influence of the diode voltage drop on the efficiency is shown in the Fig.6. It can be seen that the increasing the diode voltage drop U_D the efficiency decreases from 0.86…0.73.

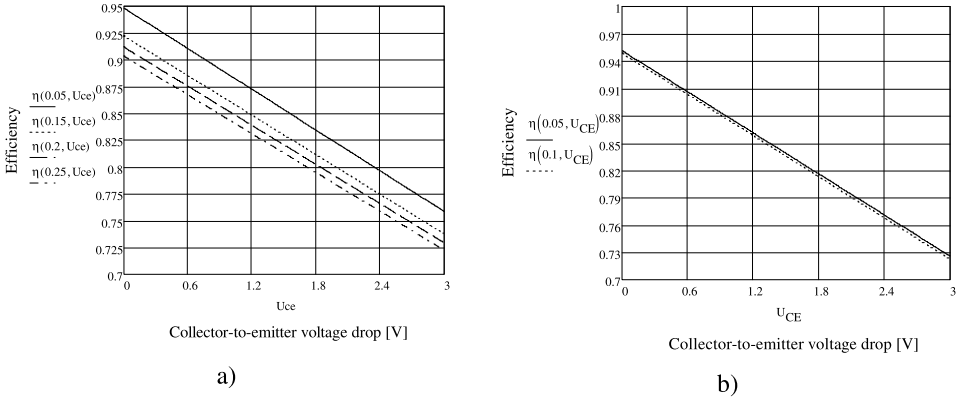


Fig. 4. Impact of the collector-to-emitter voltage drop on the efficiency: a) normal mode; b) voltage boost mode

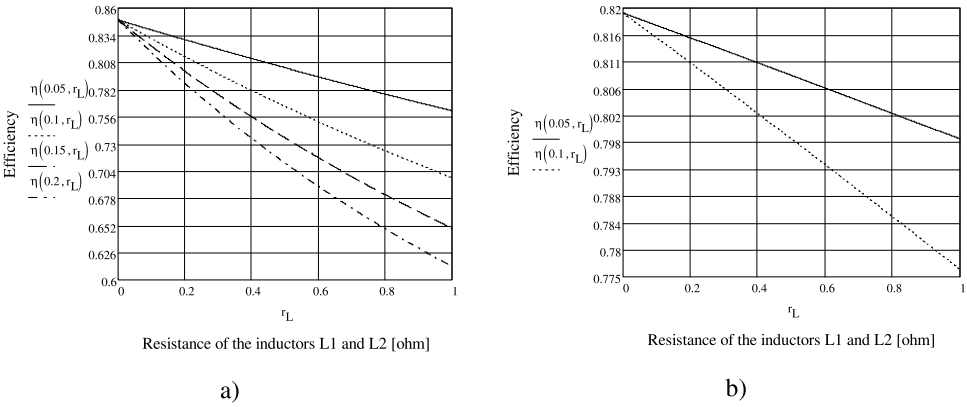


Fig. 5. Impact of the inductor resistance on the efficiency: a) normal mode; b) voltage boost mode

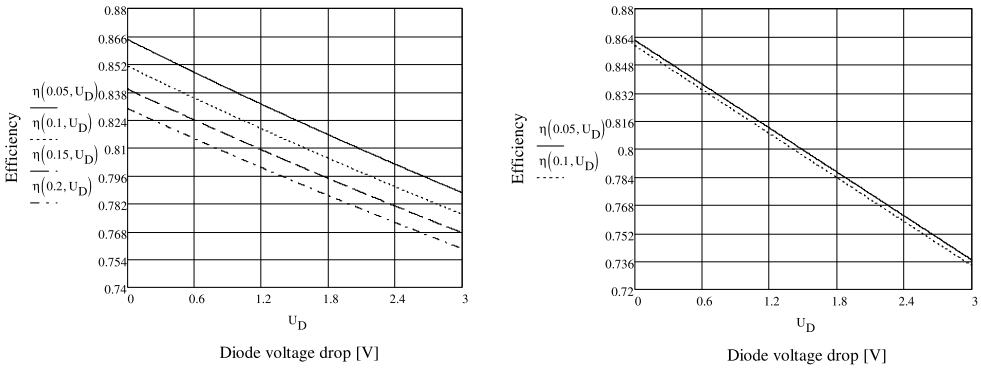


Fig. 6. Impact of the diode voltage drop on the efficiency: a) normal mode; b) voltage boost mode.

6 Experimental Results

The experimental results were carried out on the experimental prototype for the normal and voltage boost modes. The IGBT switches IRG7Ph42ud1pbf were used in the DAB. For the normal mode, the phase shift angle of $\varphi = 10°$ was used. For the voltage boost mode the gate signals with duty cycle $D = 0.6$ were applied on the switches, that resulted in the shoot-through duty cycle $D_S = 0.1$. The phase shift in this case was maximal $D_\varphi = D_S$. The voltage and current measurement results for $P = 250$ W are shown in Fig. 7. According to the parameters listed in Table 1. and the dependency shown in chapter 5, the estimated efficiency of the converter in both modes is roughly 83 %. Measurements have shown 78 % efficiency of the converter with given parameters. Obviously the measured efficiency is lower since the switching losses and core losses were not taken into account in the analysis. Also on the background of the low input voltage the U_{CE} has relatively bigger impact than for the higher voltages.

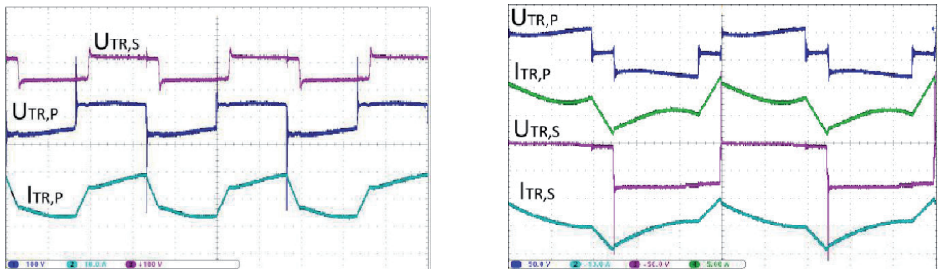


Fig. 7. Waveforms showing input voltage (U_{LV}) and current (I_{LV}) as well as output voltage (U_{HV}) and current (I_{HV}) in normal mode (a) and voltage boost mode (b)

7 Conclusion

The paper presented a loss analysis of the new qZS based DAB. The mathematical loss models of the converter were derived for normal operating mode, using conventional DAB control, and voltage boost mode, when the shoot-through switching state was used to step up the voltage on the DC link. The mathematical models were analyzed for different circuit parameters. The results have shown that U_{CE} and U_D have significant impact on the efficiency of the converter. For this reason the components with as low values should be selected, for example MOSFET switches if the converter operates with low voltage. Moreover, the simulation results verified the decrease of the current stress on the switches. The estimated efficiency for the selected circuit parameters was roughly 83%. The experimental results in the nominal operating point showed the 78% efficiency, which is smaller in comparison with obtained efficiency, since the analysis did not consider the switching and core losses.

Acknowledgment. This research and work has been supported by Estonian Ministry of Education and Research (Project SF0140016s11) and Estonian Science Foundation (Grant ETF8687).

References

1. Beldjajev, V., Roasto, I., Lehtla, T.: Intelligent Transformer: Possibilities and Challenges, RTU, p. 14 (October 2011)
2. Heinemann, L., Mauthe, G.: The universal power electronics based distribution transformer, an unified approach. In: 2001 IEEE 32nd Annual Power Electronics Specialists Conference, PESC, vol. 2, pp. 504–509 (2001)
3. Roasto, I., Romero-Cadaval, E., Martins, J., Smolenski, R.: State of the Art of Active Power Electronic Transformers for Smart Grids. In: 38th Annual Conference of IEEE Industrial Electronics, IECON 2012, October 25-28 (2012)
4. Zhang, J., Wang, W., Bhattacharya, S.: Architecture of solid state transformer-based energy router and models of energy traffic. In: 2012 IEEE PES Innovative Smart Grid Technologies (ISGT), January 16-20, pp. 1–8 (2012)
5. Vinnikov, D., Roasto, I., Strzelecki, R., Adamowicz, M.: Step-Up DC/DC Converters With Cascaded Quasi-Z-Source Network. IEEE Transactions on Industrial Electronics 59(10), 3727–3736 (2012)
6. Krismer, F.: Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies. ETH (2010)
7. Vinnikov, D., Roasto, I.: Impact of component losses on the voltage boost properties and efficiency of the qZS-converter family. In: 2011 7th International Conference-Workshop Compatibility and Power Electronics (CPE), June 1-3, pp. 303–308 (2011)
8. Mi, C., Bai, H., Wang, C., Gargies, S.: Operation, design and control of dual H-bridge-based isolated bidirectional DC-DC converter. IET Power Electronics 1(4), 507–517 (2008)

[PAPER-VII] **Beldjajev, V**., Rang, T., Zakis, J. Steady State Analysis of the Commutating LC Filter Based Dual Active Bridge for the Isolation Stage of Power Electronic Transformer. 8th International Conference-Workshop Compatibility and Power Electronics (CPE2013), Ljubljana, Slovenia, June 05-07, 2013, pp. 138 – 143.

Steady State Analysis of the Commutating LC Filter Based Dual Active Bridge for the Isolation Stage of Power Electronic Transformer

V. Beldjajev*, T. Rang*, J. Zakis**

* Tallinn University of Technology, Tallinn (*Estonia*), ** Riga Technical University, Riga (*Latvia*)
vbeldjajev@gmail.com

***Abstract* — This paper presents a complete steady-state analysis of the novel commutating LC-filter based dual active bridge (DAB). Such converter is aimed to be used in the isolation stage of the power electronics transformer. The topology consists of the LC filter coupled with a DAB. The LC filter allows to boost the input voltage by means of shoot-through state of the inverter switches. The output power of the converter is controlled by means shoot-through and the special phase shift modulation of the DAB. The simulation results of the proposed converter are provided.**

***Keywords* — dual active bridge converter, commutating LC-filter, power electronic transformer, solid state transformer.**

I. INTRODUCTION

Power generation, transmission and distribution are three main parts of the modern power system, in which the power transformers play a significant role [1]. However the traditional transformers cannot meet the set requirements for the future smart grid networks. The power electronics has offered enabling technologies for the power quality enhancements in the transmission and distribution systems. Such systems are for example the flexible AC transmission systems, static VAR compensators, static synchronous compensators, unified power flow controller etc. A new type of the power converter, named power electronic transformer (PET), for the distribution systems was introduced in the 80's [2]. The PET, also called solid state transformer is a new type of transformer that realizes voltage transformation, galvanic isolation and power quality enhancements in a single device. In comparison to the previous century the power ratings of the controllable switches have significantly improved thus enabling the PET to match the voltage and power ratings of the distribution systems [1] – [3]. The bi-directional power flow is the most important requirement that the PET has to fulfil. Additional expected characteristic is the reduction of the volumes by means of increasing the operating frequency. A good state of art concerning different topologies of PET has been presented in [1] – [3]. The research states that the three stage PET topology seems to be the most promising. This topology consists of the controllable input (AC/DC), the isolation (DC/DC) and output (DC/AC) power electronic stages (see Fig. 1). The isolation stage consists of two active rectifiers and a high frequency transformer to separate the high voltage and low voltage ports from each other.

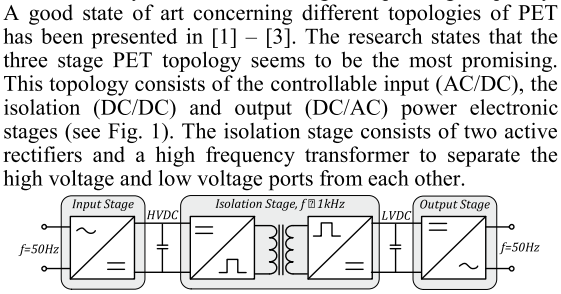


Fig. 1. Three stage topology of PET.

Many different DC/DC converter topologies have already been proposed for the isolation stage of the PET. The research in [3] has proposed a three stage topology based on modular multilevel design. Moreover, the matrix converter based topology has been proposed in [5]. However these topologies require a high number of switches and they lack the voltage step-up properties. A bi-directional current doubler based isolation stage for PET was proposed in [6]. Such converter has good voltage boost and current ripple cancellation properties, however significant number of inductive elements make this circuit hard to use without additional snubber circuit which in turn increases the losses. In particular, the drawback of many conventional DC/DC converters is the growth of switching losses and increase of the undesired effects caused by the parasitic elements, such as stray inductance of the transformer, capacitance of the switches and diode reverse recovery. One of the known topologies that can utilize effectively the circuit parasitics is the dual active bridge (DAB) that varies the phase angle of the control signals to control the output power magnitude and direction [7]. Moreover, DAB based isolation stage for PET has already been built for tens of kilowatts [8]. The best performance of the DAB is achieved when the voltage on the transformer primary and the reflected secondary voltages are equal. In such case the current stress on the devices is minimal and soft switching can be effectively achieved that results in higher efficiency. Under the realistic conditions the voltages on the primary and the secondary can vary in a wide range depending on the load. This results in a DC bus voltage reduction that in turn increases the current stress on the components.

In order to overcome these drawbacks different attempts have been made to achieve the desired voltages on the primary and the secondary sides of the transformer. The research in [9] proposed to extend the DAB with a commutating LC filter for voltage elevation. The topology consists of the two full bridges and one commutating LC filter circuit with an active clamped capacitor. The voltage elevating properties of commutating LC-filter in DC/DC converters have been discussed and analysed by many authors [10]-[14]. Reduced number of passive elements of the LC-filter results in reduced costs, dimensions and increased power density of the whole system [11]. One of the advantages is the ability of active clamped circuit to limit the voltage overshoot of the switches and utilize energy stored in the transformers leakage inductance for achieving ZVS [12]. It has also been shown that this topology is effective in the renewable energy systems [13]. This paper proposes to extend the DAB with the commutating LC filter by utilising the phase shift control technique and employ modulation scheme that was proposed in [9]. The voltage on the DC link

978-1-4673-4913-0/13/$31.00 ©2013 IEEE

is controlled by means of the shoot-through state duration and the output power is additionally controlled by employing the phase shift between the gate signals of the switches on the both HV and LV side bridges.

The paper presents the steady state analysis the actively clamped LC-commutating filter based DAB topology for the isolation stage of PET.

II. COMMUTATING LC-FILTER BASED DAB

The proposed commutating-LC filter based DC/DC converter consists of the two voltage sources U_{LV} and U_{HV}, the inductor L_1, the capacitor C_1 and the clamping power switch T_C, switches $T_1 \ldots T_4$ on the low voltage (LV) side, switches $T_5 \ldots T_8$ on the high voltage (HV) side and a high frequency (HF) transformer as shown in Fig. 2. An additional inductance L_{TR} is added in series with transformer winding. Under the nominal conditions, neglecting all losses in the passive and active components, the voltage on the LV side and the reflected voltage on the HV side must satisfy the condition

$$U_{LV} = U_{DC} = N_{TR} \cdot U_{HV}, \quad (1)$$

where U_{LV} is the voltage on the LV side, U_{DC} is the voltage on the DC link, U_{HV} is the voltage on the HV side and N_{TR} is transformers turns ratio. The transformer turns ratio N_{TR} is defined as follows

$$N_{TR} = \frac{N_P}{N_S}, \quad (2)$$

where N_S is the number of turns on the HV side, and N_P is the number of turns on the LV side of the transformer.

The switches of the DAB are switched in pairs with the duty cycle $D = 50\ \%$ and the power flow of the converter is controlled by means of the phase angle φ between the corresponding legs of the DAB on the LV and HV sides whereas the LC performs the low pass filtering on the LV side. Thus, the switch T_C is turned ON constantly. In particular, the converter operates as a conventional DAB topology where the magnitude of the phase angle determines the output power value and the sign of the phase angle determines the direction of the power flow. If the phase angle is positive then the power is transferred from the LV side to the HV side. Vice versa is valid for the negative sign of the phase angle. The typical waveforms and gating signals of the switches are shown in Fig. 3. If the boost of the input voltage is not needed then LC network provides only the low pass filtering.

However, under the realistic conditions the voltage on the low voltage side may vary in significant ranges that can result in a poor power control, increased current stress on the components and thus lower efficiency. The proposed commutating LC filter topology enables to boost the voltage

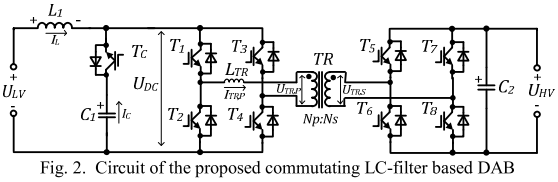


Fig. 2. Circuit of the proposed commutating LC-filter based DAB

on the DC link by means of the shoot-through switching state duration control. During the shoot-through state the switches $T_1 \ldots T_4$ are turned ON simultaneously and the energy is stored in the filter inductance L_1. During the shoot through state the switch T_C is turned OFF in order to prevent short circuiting of the capacitor C_1. Voltage on the DC link U_{DC} during the shoot through is zero. From here it can be seen that the switch T_C switches two times faster than the switching frequency of the DAB transistors. During the active state, the power is transferred from the LV side to the HV side of the converter. The gate signals with both transformer voltages and transformer current waveforms are shown in Fig. 4*a*. During the time interval $t_0 \ldots t_1$, also shown as a phase shift duration t_φ, the transistors $T_1 \ldots T_4$ are in the shoot-through state and $T_6 \ldots T_7$ are switched on the HV side. The voltage U_{HV} is applied to the transformer HV side and the current in the transformer increases linearly. In addition, due to the shoot-through condition the current in the inductor L_1 increases linearly, while the capacitor C_1 is separated from the circuit by means of turning OFF the switch T_C. During the interval $t_1 \ldots t_2$ the switches $T_1 \ldots T_4$ and T_6, T_8 are turned ON and the converter is in the freewheeling state that is used to control the output power of the converter. The capacitor is kept separated from the circuit and current in the inductor keeps rising. During the time interval $t_2 \ldots t_3$ the switches T_1, T_4, T_5 and T_8 are turned ON, however the current flows through the freewheeling diodes of T_5 and T_8 towards the HV side. The transformer current becomes equal to the DC link current and power is transferred from the LV side towards the HV side. As can be seen, considering requirement (1) the output power can thus be adjusted by controlling the duration of time interval $t_0 \ldots t_1$ (phase angle φ). The second half-cycle is symmetrical to the previous one and the transformer current repeats with negative sign during the period $T/2 < t < T$, where T is the duration of the switching period, interval $t_0 \ldots t_6$. In order to illustrate the current and voltage behaviour on the LV side, the inductor current I_{L1}, the voltage on the DC link U_{DC}, capacitor current I_{C1} and current through the active switch I_{T1} are presented in Fig 4*b*.

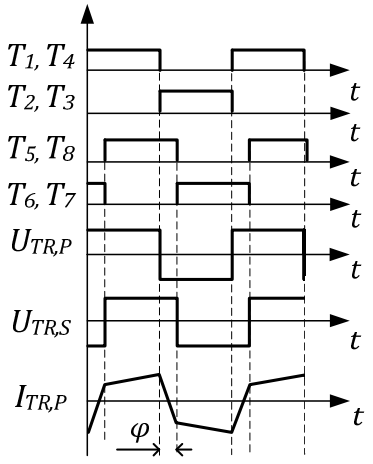


Fig. 3. Gate signals and typical waveforms of conventional DAB

978-1-4673-4913-0/13/$31.00 ©2013 IEEE

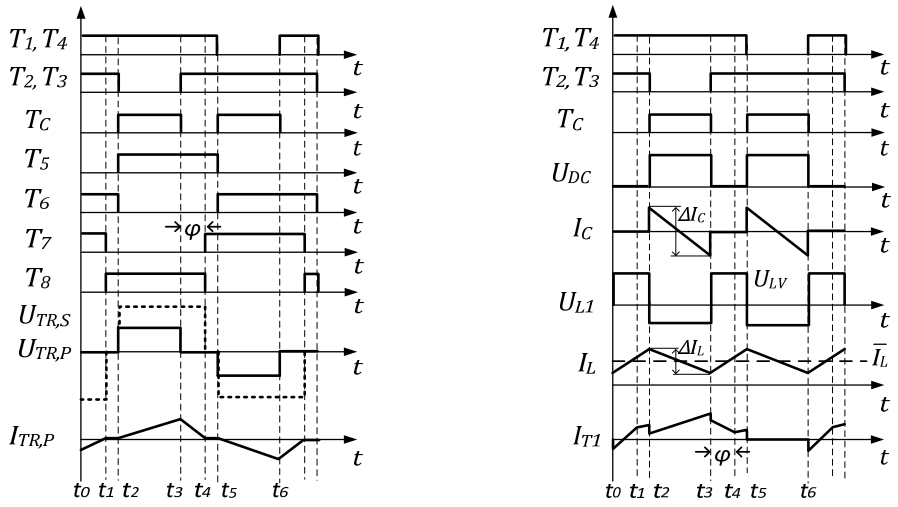


Fig. 4. Gate signals and typical waveforms of the commutating LC filter based DAB

The slope of the transformer current can vary under different load and varying voltage levels on the LV and on the HV sides. The possible shapes of the transformer current are shown in the Fig 5. If the voltage on the LV side is higher than the reflected HV side voltage, then the transformer current has a rising slope on during the non-shoot-through state. If the LV side voltage is lower than the reflected HV side voltage, then current has a decreasing slope. In the ideal case the LV side and reflected HV side voltage are equal, and transformer current has a flat slope. In order to achieve such condition, the boost properties of the commutating LC filter have high importance.

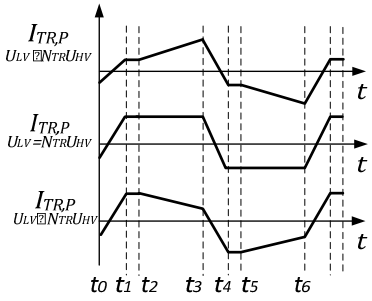


Fig. 5. Typical shapes of the transformer current depending on the LV and HV side voltage levels.

III. STEADY STATE ANALYSIS

For the steady state analysis it is assumed that all switches are ideal, all passive elements are ideal, the transformer is ideal (magnetizing and mutual inductance are equal) however a leakage inductance L_{TR} is added in series. In addition it is assumed that converter operates in the continuous conduction mode. Also, all the switching transients are neglected.

As the transformer current is symmetrical, it is enough to perform the analysis for the half period, so that

$$T_S = \frac{T}{2 f_S}, \tag{3}$$

where f_S designates the switching frequency of the switches $T_1 \ldots T_8$. The operating period T_S of the converter in the voltage boost mode consists of an active state t_A and a shoot-through state t_S

$$T_S = t_A + t_S, \tag{4}$$

For better appearance of the equations the state intervals are represented with corresponding duty cycles as follows

$$\frac{t_A}{T_S} + \frac{t_S}{T_S} = D_A + D_S = 1. \tag{5}$$

Moreover, the time interval $t_0 \ldots t_1$ is duration of the phase angle t_φ thus the corresponding duty cycle can be presented as follows

$$D_\varphi = \frac{t_\varphi}{T_S}. \tag{6}$$

A. Normal mode

In the normal mode, it is assumed that the voltage on the LV and HV sides of the transformer are at the desired level and the condition (1) is satisfied. The output power is controlled by means of adjusting the phase shift between the gate signals of the corresponding legs on both bridges. The transformer current during both intervals can be described as follows

$$\begin{cases} \Delta i_{TR} = i_{TR,0} + \dfrac{U_{LV} - N_{TR} U_{HV}}{L_{TR}} \cdot \Delta t, t_0 < t < t_1. \\ \Delta i_{TR} = \dfrac{U_{LV} - N_{TR} U_{HV}}{L_{TR}} \cdot \Delta t, t_1 < t < t_2. \end{cases} \tag{7}$$

According to the research [9], [10] the output power of the DAB can be obtained in a following way

$$P = \frac{N_{TR} U_{HV} U_{LV} D_\varphi (1 - |D_\varphi|)}{2 f_S L_{TR}}, -1 \le D_\varphi \le 1 \quad (8)$$

As can be seen from (8) the output power depends on the sign and magnitude of the phase angle D_φ. It can also be shown that the maximum power is transferred at the phase angle value $D_\varphi = \pm 0.5$.

B. Voltage boost mode

From the waveforms presented in Fig. 4 it can be seen that current through the transformer is symmetrical and during the first half-cycle $t_0 \ldots t_3$ rising with the different slopes. From the figure it can be seen that the transformer current slopes are linear, hence the transformer current i_{TR} can be described as follows

$$\begin{cases} \Delta i_{TR} = i_{TR,0} + \dfrac{U_{HV} N_{TR}}{L_{TR}} \cdot \Delta t, t_0 \le t \le t_1 = t_\varphi. \\ \Delta i_{TR} = \dfrac{U_{DC} - U_{HV} N_{TR}}{L_{TR}} \cdot \Delta t, t_2 \le t \le t_3 = t_A. \end{cases} \quad (9)$$

Where $i_{TR,0}$ is the initial value of the transformer current at time instance t_0. For the analysis it is assumed that the initial value of the $i_{TR,0}$ is negative. The time period $t_1 \ldots t_2$ is skipped, since the current does not change during this interval $i_{TR}(t_1) = i_{TR}(t_2)$. Due to the symmetry, the i_{TR} at the time instance t_3 has the same value as at the time instance t_0, however with the opposite sign. That can be expressed as follows:

$$i_{TR}(t_3) = -i_{TR,0}. \quad (10)$$

Thus, the transformer current during T_S can be described with the following expression

$$i_{TR,0} + \frac{U_{HV} N_{TR}}{2 f_S L_{TR}} D_\varphi + \frac{U_{DC} - U_{HV} N_{TR}}{2 f_S L_{TR}} (1 - D_S) = -i_{TR,0}, \quad (11)$$

where $(1\text{-}D_S)$ is the active state D_A (5). The solution of (11) gives the following expression for the current term $i_{TR,0}$

$$i_{TR,0} = \frac{1}{4 f_S L_{TR}} \left[N_{TR} U_{HV} (1 - D_\varphi - D_S) - U_{DC} (1 - D_S) \right], \quad (12)$$

Inserting the solution from (12) into (9) allows the current value at the time instance t_1 to be obtained in a following way

$$i(t_1) = \frac{1}{4 f_S L_{TR}} \left[N_{TR} U_{HV} (1 + D_\varphi - D_S) - U_{DC} (1 - D_S) \right] \quad (13)$$

In order to obtain the output power level of the converter, it is necessary to determine the average current of the transformer during the half-cycle. The average current can be obtained by solving the following integral for the half-cycle switching period T_S.

$$I_{TR} = \frac{1}{T_S} \int_{t_0}^{T_S} i_{TR}(t) dt. \quad (14)$$

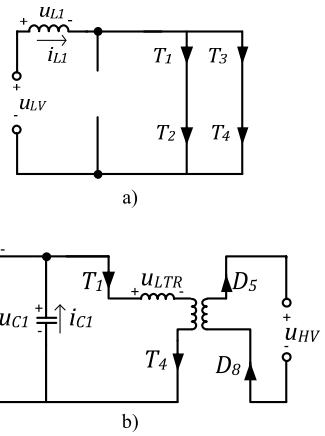


Fig. 6. Equivalent circuit of the converter in shoot-through state (a) and active state (b).

Knowing the average current value determined by (14) allows the transferred power during the half-cycle T_S to be obtained. The instantaneous power can be calculated by multiplying the instantaneous current and voltage values. Assuming that the voltage on the transformer terminals is constantly equal to the DC link voltage U_{DC} and using the expression (14), the output power can be obtained in a following way

$$P = \frac{1}{T_S} \int_{t_0}^{T_S} u(t) \cdot i_{TR}(t) dt = U_{DC} \cdot I_{TR}. \quad (15)$$

Inserting the solutions from (12) and (13) into (14) the average transformer current I_{TR} during the period T_S can be evaluated. I_{TR} is a sum of current terms at different time instances. Considering (9) and (10) the transformer average current during T_S can be expressed as follows

$$I_{TR} = \frac{1}{4 f_S L_{TR}} \left[\left(i(t_0) + i(t_1) \right) \cdot D_\varphi + \left(i(t_1) - i(t_0) \right) \cdot (1 - D_S) \right] \quad (16)$$

And inserting I_{TR} from (16) into (15) the supplied power P can be estimated in a following way

$$P = U_{DC} \cdot \frac{(2 N_{TR} U_{HV} - U_{DC}) D_\varphi (1 - D_S)}{4 f_S L_{TR}}, 0 \le D_\varphi \le D_S. \quad (17)$$

As can be seen from (17) the output power depends proportionally on the phase angle value D_φ, shoot through duty cycle D_S, voltage levels U_{LV} and U_{HV} and inverse proportionally from the switching frequency f_S and the leakage inductance L_{TR} of the HF transformer.

Next it is essential to determine the DC link voltage level and the boost factor of the converter. The estimation of the boost factor is based on the fact that in the steady state operation the average voltage over the inductor during one switching period T_S is zero as can be seen from the Fig. 3.

$$U_{L1} = \frac{1}{T_S} \int_{t_0}^{T_S} u_{L1}(t) dt = 0. \quad (18)$$

The equivalent circuit of the shoot-through state is shown in Fig. 6*a*. It can be seen that the voltage over the inductor L_1 is equal to the LV side voltage

$$u_{L1} = U_{LV} \cdot D_S. \tag{19}$$

The equivalent circuit for the active state is shown in the Fig. 6*b*. The voltage over the inductor is equal to the sum of the voltages on the LV side and capacitor C_1

$$u_{L1} = (U_{LV} - U_{C1}) \cdot (1 - D_S). \tag{20}$$

From (18), (19) and (20) the following expression can be written to describe the inductor voltage

$$u_{L1} = U_{LV} \cdot D_S + (U_{LV} - U_{C1}) \cdot (1 - D_S) = 0. \tag{21}$$

And the capacitor voltage, hence the DC link voltage, can be derived from (21) as follows

$$u_{C1} = \frac{U_{LV}}{1 - D_S}. \tag{22}$$

It can be seen that boost factor of the converter is same as for the traditional boost converter and depends on the shoot-through state duration D_S. Knowing the output power (17) and the DC link voltage (22) the average current through the inductor L_1 can be estimated as follows

$$I_{L1} = \frac{P}{U_{LV}}. \tag{23}$$

The inductor current achieves its maximum value by the end of the shoot-through state. Thus, knowing the inductance L_1 and shoot-through state duration the inductor current ripple can be estimated in a following way

$$\Delta I_{L1} = \frac{U_{LV}}{L_1 f_S} D_S. \tag{24}$$

Moreover, knowing the maximum I_{MAX} value of the transformer current obtained from (13) the peak-to-peak value of the capacitor C_1 can be expressed as follows [12]

$$\Delta I_{C1} = 2(I_{MAX} - I_{L1}). \tag{25}$$

In practise, the parameters necessary for the LC filter inductance are defined by (24). At maximal shoot-through duty cycle $D_{S,MAX}$ the full change of current must be on the accepted level, thus the filter inductance can be selected accordingly

$$L_1 = \frac{U_{LV}^2 D_{S,MAX}}{k f_S P_N}, \tag{26}$$

where P_N designates the desired nominal output power of the converter.

Fig. 7 depicts the influence of the phase angle D_φ and shoot through duty cycle D_S to the output power of the converter. The graphs are obtained analytically using following parameters: f_S = 20 kHz, L_{TR} = 6 µH, U_{HV} = 200 V, N_{TR} = 6.6, U_{DC} = 30 V. It is assumed, that the converter operates at its maximal power level, so that $D_\varphi = D_S$. It can be seen that DC link voltage is kept on the constant level of 30 V when the input voltage is decreasing. The maximal power of the converter is achieved when the shoot-through duty cycle and thus phase angle are D_S = 0.5. Fig. 8 depicts the influence of the phase angle value to the output power, while keeping the shoot-through duty cycle at the constant value D_S = 0.5. It can be seen, when input voltage falls to 15V, the converter keeps the DC link voltage still at required level. The output power depends linearly from the D_φ and achieves its maximal value at $D_\varphi = D_S$.

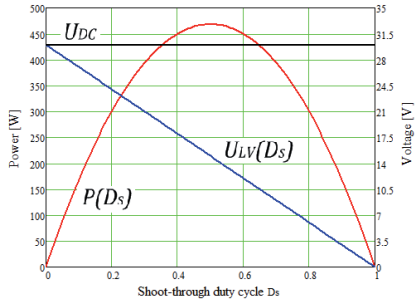


Fig. 7. Output power $P(D_S)$ and DC link voltage U_{DC} dependency of the shoot-through duty cycle by $D_\varphi = D_S$

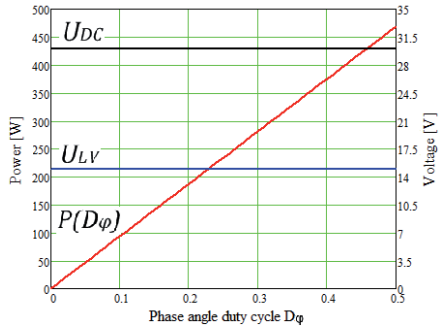


Fig. 8. Output power $P(D_\varphi)$ dependency of the phase angle duty cycle by constant U_{LV}, U_{DC} and the shoot-through duration D_S = 0.5.

IV. Simulation Results

In this chapter the simulation results of the proposed converter are presented. The aim of the simulations is to verify the theoretically obtained results. First the converter is simulated in the normal mode, considering requirement (1). In the normal mode the DAB is controlled using conventional phase shift modulation. During this operating mode the LC network performs low pass filtering. Afterwards the voltage boost mode of the converter is simulated using the modulation shown in Fig. 4. The parameters used in the simulation circuit are presented in Table 1.

Fig. 9 shows the voltages on both sides of the transformer and the current flowing through the transformer primary. The phase shift between the two voltages is clearly seen and current has the waveform that corresponds to theoretical.

Table 1. LC-DAB Circuit Parameters

Parameter	Value
Low side voltage U_{LV}	27/30 V
High side voltage U_{HV}	200 V
Transformer turns ratio N_{TR}	1/6.6
Inductor L_1	100 uH
Capacitor C_1	150 uF
Switching frequency f_S	20 kHz
Output power	1 kW

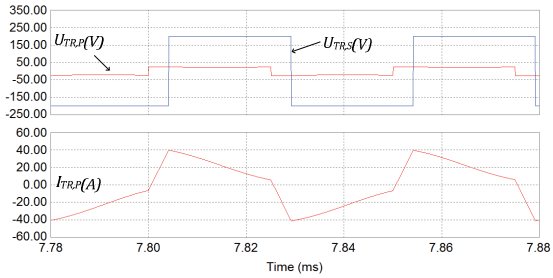


Fig. 9. Transformer LV side ($U_{TR,P}$) and HV ($U_{TR,S}$) voltages with transformer current ($I_{TR,P}$) in the normal operating mode.

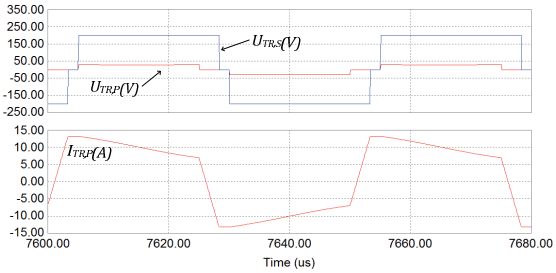


Fig. 10. Transformer LV side ($U_{TR,P}$) and HV ($U_{TR,S}$) voltages with transformer current ($I_{TR,P}$) in the voltage boost mode

Fig. 10 depicts the voltages on both sides of the transformer and the current in the transformer primary in the voltage boost mode. It can be seen that transformer current rises during the phase shift duty cycle, and afterwards stays on the constant level during the freewheeling state described in chapter 2. All waveforms are identical to the theoretical ones.

V. CONCLUSION

The paper presented the steady-state analysis of the commutating LC-filter based DAB DC/DC converter. One possible application for the above-mentioned converter is the isolation stage of the PET. If the voltage levels on the HV-DC link and LV-DC link are at the desired level, the converter operates as a traditional DAB and the phase shift modulation is employed. The LC network provides a low pass filtering of the DC link voltage. However, under the realistic conditions the voltage on the LV DC link may decrease and that in turn would result in increased current stress and lower efficiency. In that case the special modulation state, shoot-through, is used to boost up the voltage on the DC link to the desired value, separating the capacitor from the network by means of an additional switch. In addition a special phase shift modulation is used to control the output power of the converter. The equations for estimating the output power and the boost factor of the LC filter, neglecting the losses, were derived. Also, the power characteristics were presented and the results were verified with the simulations. It can be said that employed modulation scheme for the boost mode allows to additionally control the output power by means of a phase angle. However, a more comprehensive analysis is necessary to assess the feasibility of such topology in practice. The conduction and switching losses in the real switches may have significant impact on the overall efficiency. Moreover, the switching and core losses increase with the switching frequency and need to be paid attention during the design. In addition, due to voltage fed nature, special considerations regarding EMI for this topology.

Next step of the research is to build the prototype of the converter and perform soft-switching and loss analysis in order to estimate the efficiency.

ACKNOWLEDGMENT

The authors would like to thank the Estonian Ministry of Education and Research (Project SF0140016s11), Estonian Research Council (Grant ETF8538, ETF8687) and European Regional Fund´s for the support of this research.

This research work was partially supported by Latvian State Research Programme “LATENERGI” and Latvian Council of Science (Grant 416/2012).

REFERENCES

[1] She, Xu; Burgos, Rolando; Wang, Gangyao; Wang, Fei; Huang, Alex Q.; , "Review of solid state transformer in the distribution system: From components to field application," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.4077-4084, 15-20 Sept. 2012

[2] van der Merwe, J.W.; du T. Mouton, H.; , "The solid-state transformer concept: A new era in power distribution," *AFRICON, 2009. AFRICON '09.* , vol., no., pp.1-6, 23-25 Sept. 2009.

[3] Beldjajev, V.; Roasto, I.; , “State of art trends and design challenges of power electronic transformer for future distribution grids” *Технічна електродинаміка*, vol., no. 3, pp.55-62, 2012.

[4] Zhu Haibin; Li Yaohua; Wang Ping; Li Zixin; Chu Zunfang; , "Design of Power Electronic Transformer Based on Modular Multilevel Converter," *Power and Energy Engineering Conference (APPEEC), 2012 Asia-Pacific* , vol., no., pp.1-4, 27-29 March 2012

[5] Banaei, M.R.; Salary, E.; , "Power quality improvement based on novel power electronic transformer," *Power Electronics, Drive Systems and Technologies Conference (PEDSTC), 2011 2nd* , vol., no., pp.286-291, 16-17 Feb. 2011

[6] Beldjajev, V.; Roasto, I.; Vinnikov, D.; , "Analysis of current doubler rectifier based high frequency isolation stage for intelligent transformer," *Compatibility and Power Electronics (CPE), 2011 7th International Conference-Workshop* , vol., no., pp.336-341, 1-3 June 2011.

[7] Alonso, A.R.; Sebastian, J.; Lamar, D.G.; Hernando, M.M.; Vazquez, A.; , "An overall study of a Dual Active Bridge for bidirectional DC/DC conversion," *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE* , vol., no., pp.1129-1135, 12-16 Sept. 2010

[8] Yu Du; Seunghun Baek; Bhattacharya, S.; Huang, A.Q.; , "High-voltage high-frequency transformer design for a 7.2kV to 120V/240V 20kVA solid state transformer," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.493-498, 7-10 Nov. 2010

[9] Krismer, Florian. “Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies.” ETH(2010).

[10] Sangtaek Han; Divan, D.; , "Dual active bridge buck-boost converter," *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE* , vol., no., pp.2905-2911, 20-24 Sept. 2009

[11] Zakis, J.; Vinnikov, D.; Rankis, I.; , " Analysis of operating modes of the step-up DC/DC converter with a commutating LC-filter," *Технічна електродинаміка*, vol., no.1, pp.87-92, 2011.

[12] Watson, R., Lee, F.C., “A soft-switched, full-bridge boost converter employing an active-clamp circuit,” IEEE PESC, 1996, Volume: 2, Page(s): 1948 -1954 .

[13] Lizhi Zhu; Kunrong Wang; Lee, F.C.; Jih-Sheng Lai, **“**New start-up schemes for isolated full-bridge boost converters,” IEEE APEC 2000, Page(s): 309-313 vol.1

[14] Hanju Cha; Jungwan Choi; Enjeti, P.N., "A Three-Phase Current-Fed DC/DC Converter With Active Clamp for Low-DC Renewable Energy Sources," *Power Electronics, IEEE Transactions on* , vol.23, no.6, pp.2784,2793, Nov. 2008

[PAPER-VIII] **Beldjajev, V**., Lehtla, T., Zakis, J. Impact of Component Losses on the Efficiency of the Commutating LC-Filter Based Dual Active Bridge for the Isolation Stage of the Power Electronic Transformer. 8th International Conference-Workshop Compatibility and Power Electronics (CPE2013), Ljubljana, Slovenia, June 05-07, 2013, pp. 132 – 137.

Impact of Component Losses on the Efficiency of the LC-Filter Based Dual Active Bridge for the Isolation Stage of Power Electronic Transformer

V. Beldjajev*, T. Lehtla*, J. Zakis**

* Tallinn University of Technology, Tallinn (*Estonia*), ** Riga Technical University, Riga (*Latvia*)
vbeldjajev@gmail.com

***Abstract* — This paper presents a steady state analysis of the commutating LC-filter based dual active bridge (DAB) considering the conduction losses in the components. The aim is to use this converter in power electronic transformer (PET). The LC-filter offers the boost properties with a small component count and DAB allows effective power flow control and soft switching capabilities. Such combination allows the voltage on the transformer terminals to be kept at the desired level to enable the best performance of the converter. In order to facilitate the impact of the losses on the power characteristics and efficiency the mathematical loss models are derived and experimental results are presented.**

***Keywords* — dual active bridge converter, commutating LC-filter, power electronic transformer, conduction losses.**

I. INTRODUCTION

Power generation, transmission and distribution are three main parts of the modern power system, in which the power transformers play a significant role [1]. The power electronics has offered enabling technologies for the power quality enhancements in the transmission and distribution systems. Such systems are for example the flexible AC transmission systems, static VAR compensators, static synchronous compensators, unified power flow controller etc. The PET, is a new type of transformer that realizes voltage transformation, galvanic isolation and power quality enhancements in a single device. The PET is suitable for the use in the power systems that comprise renewable energy sources, energy storage devices as well as different type of loads. Thus the bi-directional power flow is the most important requirement that the PET has to fulfil. Additional expected characteristic is the reduction of the volumes by means of increasing the operating frequency. A good state of art concerning different topologies of PET has been presented in [1] – [4]. The research states that the three stage PET topology seems to be the most promising. This topology consists of the controllable input (AC/DC), the isolation (DC/DC) and output (DC/AC) power electronic stages (see Fig. 1). The isolation stage consists of two active rectifiers and a high frequency transformer to separate the high voltage and low voltage ports from each other

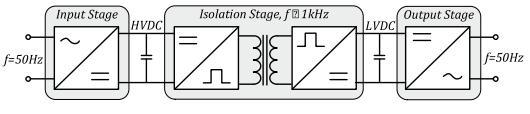


Fig. 1. Three stage topology of PET.

Many different DC/DC converter topologies have already been proposed for the isolation stage of the PET. In particular, the drawback of many conventional DC/DC converters is the growth of switching losses and increase of the undesired effects caused by the parasitic elements, such as stray inductance of the transformer, capacitance of the switches and diode reverse recovery. One of the known topologies that can utilize effectively the circuit parasitics is the dual active bridge (DAB). As a matter of fact, DAB based isolation stage for PET has already been built for tens of kilowatts [5]. The best performance of the DAB is achieved when the voltage on the transformer primary and the reflected secondary voltages are equal. In such case the current stress on the devices is minimal and soft switching can be effectively achieved that results in higher efficiency. Under the realistic conditions the voltages on the primary and the secondary can vary in a wide range depending on the load. This results in a DC bus voltage reduction that in turn increases the current stress on the components. This issue can pose a major drawback of the DAB. In order to overcome this drawback an additional boost circuit can be added to the low voltage side. The commutating LC-filter network has been widely proposed for the DC/DC converters that are used in renewable energy systems [6]-[11]. Reduced number of passive elements of the LC-filter results in reduced costs, dimensions and increased power density of the whole system. One of the advantages is the ability of active clamped circuit to limit the voltage overshoot of the switches and utilize energy stored in the transformers leakage inductance for achieving ZVS [9]. It has also been shown that this topology is effective in the renewable energy systems [10]. If the voltage level on the low voltage (LV) side drops below the desired value, the converter can elevate the voltage on the DC link and thus guarantee the best performance of the DAB. However, additional circuit results in increased conduction losses that in turn decrease the efficiency. For this reason, the impact of the conduction losses is essential and needs to be taken into account when designing the converter.

II. COMMUTATING LC-FILTER BASED DAB

The commutating LC-filter based DAB consists of the two voltage sources U_{LV} and U_{HV}, the inductor L_1, the capacitor C_1, the clamping power switch T_C, switches $T_1 \ldots T_4$ on the low voltage (LV) side, switches $T_5 \ldots T_8$ on the high voltage (HV) side and a high frequency (HF) transformer as shown in Fig. 2. An additional inductance L_{TR} is added in series with transformer winding. Under the nominal conditions, neglecting all losses in the passive and active components, the voltage on the LV side and the reflected voltage on the HV side must satisfy the following condition

978-1-4673-4913-0/13/$31.00 ©2013 IEEE

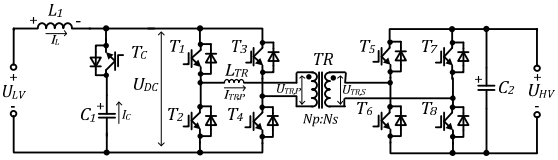


Fig. 2. Circuit of the proposed commutating LC-filter based DAB

$$U_{LV} = U_{DC} = N_{TR} \cdot U_{HV}, \tag{1}$$

where U_{LV} is the voltage on the LV side, U_{DC} is the voltage on the DC link, U_{HV} designates the voltage on the HV side and N_{TR} is transformers turns ratio. The transformer turns ratio N_{TR} is defined as follows

$$N_{TR} = \frac{N_P}{N_S}, \tag{2}$$

where N_S is the number of turns on the HV side, and N_P is the number of turns on the LV side of the transformer. The current stress on the components is minimal when condition (1) is fulfilled.

If the voltage on the LV side drops below nominal value, then it must be elevated by the additional LC extension. The proposed commutating LC-filter topology enables to elevate the input voltage by means of the shoot-through switching state duration control. During the shoot-through state the switches $T_1 \ldots T_4$ are turned ON simultaneously, the energy is stored in the filter inductance L_1. During the shoot through state the switch T_C is turned OFF in order to prevent short circuit of the capacitor C_1. Voltage on the DC link U_{DC} during the shoot through is zero. From here it can be seen that the switch T_C switches two times faster than the switching frequency of the DAB transistors. During the active state, the power is transferred from the LV side to the HV side of the converter. The waveforms of the gate signals, transformer voltages on HV and LV side, and the transformer current are shown in Fig. 3. During the time interval $t_0 \ldots t_1$, also shown as a phase shift duration t_φ, the transistors $T_1 \ldots T_4$ are in the shoot-through state and $T_6 \ldots T_7$ are switched ON the HV side. The voltage U_{HV} is applied to the transformer HV side and the current in the transformer increases linearly. In addition, due to the shoot-through state the current in the inductor L_1 increases linearly, while the capacitor C_1 is separated from the circuit by turning OFF the switch T_C. During the interval $t_1 \ldots t_2$ the switches $T_1 \ldots T_4$ and T_6, T_8 are turned ON. In this case the converter is in the freewheeling state that is used to control the output power of the converter. The capacitor is kept separated from the circuit and current in the inductor keeps rising. During the time interval $t_2 \ldots t_3$ the switches T_1, T_4, T_5 and T_8 are turned ON, however the current flows mainly through the freewheeling diodes of T_5 and T_8 towards the HV side. During the active state, the switch T_C is turned ON. The transformer current becomes equal to the DC link current and power is transferred from the LV side towards the HV side. As can be seen, considering requirement (1) the output power can thus be adjusted by controlling the duration of time interval $t_0 \ldots t_1$ (phase angle φ). The second half-cycle is symmetrical to the previous one and the transformer current repeats with negative sign during the period $T/2 < t < T$, where T is the switching period, interval $t_0 \ldots t_6$. The voltage applied to the leakage inductance L_{TR} is determined by the difference of the input and output voltages

$$U_{LTR} = U_{DC} - N_{TR} \cdot U_{HV}. \tag{3}$$

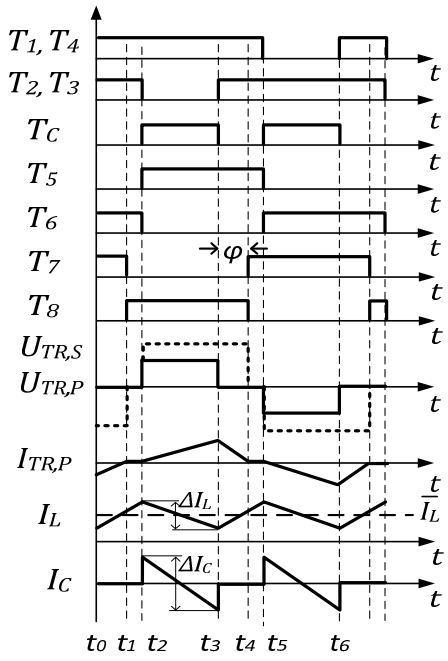


Fig. 3. Gate signals and typical waveforms of the commutating LC filter based DAB

III. STEADY STATE ANALYSIS

For the steady state analysis it is assumed that all switches are ideal, all passive elements are ideal, the transformer is ideal (magnetizing and mutual inductance are equal). In addition it is assumed that voltage sources U_{LV} and U_{HV} are constant and converter operates in the continuous conduction mode. Also, all the switching transients are neglected.

As the transformer is symmetrical, it is enough to perform the analysis for the half period, so that

$$T_S = \frac{T}{2 f_S}, \tag{4}$$

where f_S designates the switching frequency of the switches $T_1 \ldots T_8$. The operating period T_S of the converter in the voltage boost mode consists of an active state t_A ($t_2 \ldots t_3$ and $t_5 \ldots t_6$) and a shoot-through state t_S ($t_0 \ldots t_2$ and $t_3 \ldots t_5$)

$$T_S = t_A + t_S. \tag{5}$$

The state intervals can also be represented with corresponding duty cycles as follows

$$\frac{t_A}{T_S} + \frac{t_S}{T_S} = D_A + D_S = 1. \tag{6}$$

Moreover, the time interval $t_0 \ldots t_1$ is duration of the phase angle t_φ ($t_0 \ldots t_1$ and $t_3 \ldots t_4$) thus the corresponding duty cycle can be presented as follows

$$D_\varphi = \frac{t_\varphi}{T_S}. \tag{7}$$

978-1-4673-4913-0/13/$31.00 ©2013 IEEE

From the waveforms presented in Fig. 3 it can be seen that current through the transformer is symmetrical and during the first half-cycle $t_0...t_3$ rising with the different slopes. From the figure it can be seen that the transformer current slopes are linear, hence the transformer current i_{TR} can be described as follows:

$$\begin{cases} \Delta i_{TR} = i_{TR,0} + \dfrac{U_{HV} N_{TR}}{L_{TR}} \cdot \Delta t, t_0 \le t \le t_1 = t_\varphi. \\ \Delta i_{TR} = \dfrac{U_{DC} - U_{HV} N_{TR}}{L_{TR}} \cdot \Delta t, t_2 \le t \le t_3 = t_A. \end{cases} \quad (8)$$

In (8) $i_{TR,0}$ is the initial value of the transformer current at time instance t_0. For the analysis it is assumed that the initial value of the $i_{TR,0}$ is negative. The time period $t_1 \ldots t_2$ is skipped, since the current does not change during this interval $i_{TR}(t_1) = i_{TR}(t_2)$. Due to the symmetry, the i_{TR} at the time instance t_3 has the same value as at the time instance t_0, however with the opposite sign. That can be expressed as follows:

$$i_{TR}(t_3) = -i_{TR,0}. \quad (9)$$

Thus, the transformer current during T_S can be described with the following expression

$$i_{TR,0} + \frac{U_{HV} N_{TR}}{2 f_S L_{TR}} D_\varphi + \frac{U_{DC} - U_{HV} N_{TR}}{2 f_S L_{TR}} (1 - D_S) = -i_{TR,0}, \quad (10)$$

where $(1\text{-}D_S)$ is the active state D_A duty cycle (5). The solution of (11) gives the following expression for the current term $i_{TR,0}$

$$i_{TR,0} = \frac{1}{4 f_S L_{TR}} \left[N_{TR} U_{HV} (1 - D_\varphi - D_S) - U_{DC} (1 - D_S) \right] \quad (11)$$

Inserting the solution from (10) into (8) allows the current value at the time instance t_1 to be obtained in a following way

$$i(t_1) = \frac{1}{4 f_S L_{TR}} \left[N_{TR} U_{HV} (1 + D_\varphi - D_S) - U_{DC} (1 - D_S) \right] \quad (12)$$

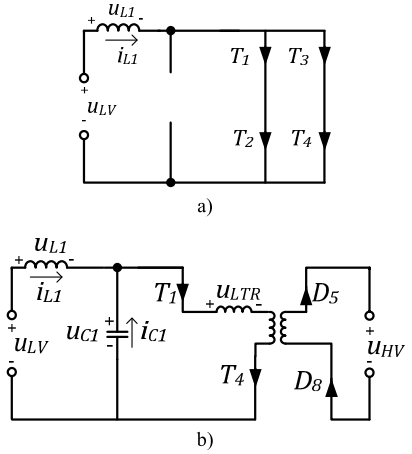


Fig. 4. Equivalent circuit of the converter in shoot-through state (a) and active state (b).

In order to obtain the output power level of the converter, it is necessary to determine the average current of the transformer during the half-cycle. The average current can be obtained by solving the following integral for the half-cycle switching period T_S.

$$I_{TR} = \frac{1}{T_S} \int_{t_0}^{T_S} i_{TR}(t) dt. \quad (13)$$

Knowing the average current value determined from (13) allows the transferred power during the half-cycle T_S to be obtained. The instantaneous power can be calculated by multiplying the instantaneous current and voltage values. Assuming that the voltage on the transformer terminals is constantly equal to the DC link voltage U_{DC} and using the expression (13), the output power can be obtained in a following way

$$P = \frac{1}{T_S} \int_{t_0}^{T_S} u(t) \cdot i_{TR}(t) dt = U_{DC} \cdot I_{TR}. \quad (14)$$

Inserting the solutions from (11) and (12) into (13) the average transformer current I_{TR} during the period T_S can be evaluated. I_{TR} is a sum of current terms at different time instances. Inserting I_{TR} from (13) into (14) the supplied power P can be estimated in a following way

$$P = U_{DC} \cdot \frac{(2 N_{TR} U_{HV} - U_{DC}) D_\varphi (1 - D_S)}{4 f_S L_{TR}}, 0 \le D_\varphi \le D_S. \quad (15)$$

As can be seen from (15) the output power depends proportionally on the phase angle value D_φ, shoot through duty cycle D_S, voltage levels U_{LV} and U_{HV} and inverse proportionally from the switching frequency f_S and the leakage inductance L_{TR} of the HF transformer.

Next it is essential to determine the DC link voltage level and the boost factor of the converter. The estimation of the boost factor is based on the fact that in the steady state operation the average voltage over the inductor during one switching period T_S is zero as can be seen from the Fig. 3.

$$U_{L1} = \frac{1}{T_S} \int_{t_0}^{T_S} u_{L1}(t) dt = 0. \quad (16)$$

The equivalent circuit for the shoot-through state is shown in Fig. 4*a*. It can be seen that the voltage over the inductor L_1 is equal to the LV side voltage

$$u_{L1} = U_{LV} \cdot D_S. \quad (17)$$

The equivalent circuit for the active state is shown in the Fig. 4*b*. The voltage over the inductor is equal to the sum of the voltages on the LV side and capacitor C_1

$$u_{L1} = (U_{LV} - U_{C1}) \cdot (1 - D_S). \quad (18)$$

From (16), (17) and (18) the following expression can be written to describe the inductor voltage

$$u_{L1} = U_{LV} \cdot D_S + (U_{LV} - U_{C1}) \cdot (1 - D_S) = 0. \quad (19)$$

And the capacitor voltage, hence the DC link voltage, can be derived from (19) as follows

$$U_{C1} = U_{DC} = \frac{U_{LV}}{1 - D_S}. \quad (20)$$

It can be seen that boost factor of the converter is same as for the traditional boost converter and depends on the shoot-through state duration D_S. Knowing the output power (15) and the DC link voltage (20) the average current through the inductor L_1 can be estimated as follows

$$I_L = \frac{P}{U_{LV}}. \tag{21}$$

IV. Impact of Component Losses on Power Characteristics

To model the losses and estimate their effect on the overall efficiency of the converter the steady state analysis considering conduction losses was carried out. In the analysis following losses were taken into account: conduction losses due to collector-to-emitter voltage drop over the IGBT-s (U_{CE}), voltage drop over the freewheeling diodes (U_D), voltage drop due to active resistance of the wires on the HF primary winding (r) and on the inductor (r_L). For the analysis it is assumed that converter operates in continuous conduction mode and all transients are neglected. To simplify the analysis, it is assumed that all transistors $T_1 \ldots T_8$ are identical. For the analysis, the skin and proximity effects in the power switches and in the transformers are neglected. In general, the power loss of the switch can be evaluated as

$$P_{IGBT} = \frac{1}{T_s}\int_0^{T_s} u_{CE}(t)\cdot i_C(t)\cdot dt = U_{CE}\cdot I_{CAV}, \tag{22}$$

where U_{CE} designates the voltage drop over the IGBT, I_{CAV} is the average current that flows through the switch. The conduction losses in the freewheeling diodes are evaluated in a similar way

$$P_D = \frac{1}{T_{sw}}\int_0^{T_{sw}} u_D(t)\cdot i_D(t)\cdot dt = U_D\cdot I_{DAV}, \tag{23}$$

where I_{DAV} is the average current and U_D is the forward voltage drop over the freewheeling diode. Conduction losses in the active resistance depend on the resistances value and RMS current flowing through it

$$P_R = r\cdot I_{RMS}^2. \tag{24}$$

The circuit parameters that are used for the analysis are presented in Table 1. The desired voltage on the transformer LV terminals should be held on 30 V. In this case the power magnitude depends only on the phase angle φ value and highest efficiency of DAB is achieved.

Table 1. Circuit Parameters

Parameter	Value
Low side voltage U_{LV}	30 V
High side voltage U_{HV}	200 V
Transformer turns ratio N_{TR}	1/6.6
Inductor L_1	100 uH
Capacitor C_1	150 uF
Leakage inductance L_{TR}	10 uH
Switching frequency f_S	20 kHz
Collector to emitter voltage drop U_{CE}	1.8 V
Diode voltage drop U_D	1.1 V
Inductor and transformer resistance r	0.15 Ω

First of all it is essential to determine the impact of the active resistance r of the transformer on the output power of the DAB. Thus adding r to the (8) and (15) the average transformer current during the T_S can be evaluated accordingly to (25). The influence of r to the power characteristics for different shoot-through duty cycles is depicted in the Fig. 7. In addition, the phase angle duration t_φ is equal to the duration of the shoot-through state t_S (converter operates at maximum power). The influence of the conduction losses on the power characteristic for different shoot-through states is shown in Fig 8. As expected, the output power is lower in comparison with the ideal characteristic and decreases with the increase of the active resistance.

Next, it is necessary to perform the steady state analysis for the loss models of commutating LC filter based DAB, in order to assess the influence of the losses on the boost properties of the LC-filter. Therefore, two equivalent circuits for the shoot-through state and active state are shown in Fig. 6. Considering (16), the voltage over the inductor L_1 and adding the conduction losses of the DC link voltage evaluation into (19) the voltage over the inductor L_1 during T_S can be described according to the equation defined in (26). From (26) the voltage on the DC link considering the losses can be expressed as follows

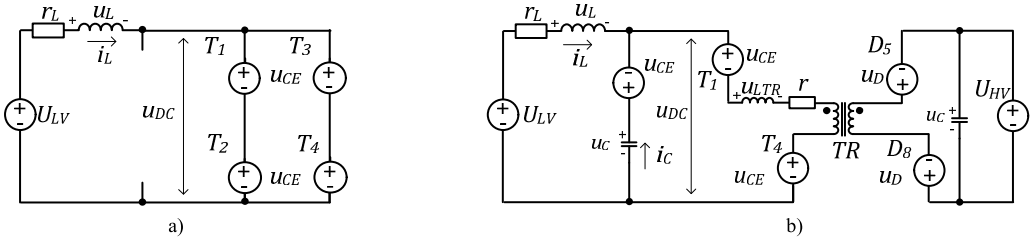


Fig. 5. Switching states of the converter in the shoot-through state (a) and the active state (b).

$$I_{TR} = \frac{D_\varphi(D_S-1)\cdot\left|U_{DC}\cdot r(1-D_\varphi-D_S)+U_{HV}N_{TR}(8L\cdot f+r(1+D_\varphi+D_S))\right|}{2\left[(r(D_S-1)-2L\cdot f)\cdot(4L\cdot f+D_\varphi r)\right]},\ 0\le D_\varphi\le D_S. \tag{25}$$

$$u_{L1} = (U_{LV}-U_{CE}-I_L\cdot r_L)\cdot D_S + (U_{LV}-I_L\cdot r_L-U_{C1})\cdot(1-D_S) = 0. \tag{26}$$

978-1-4673-4913-0/13/$31.00 ©2013 IEEE

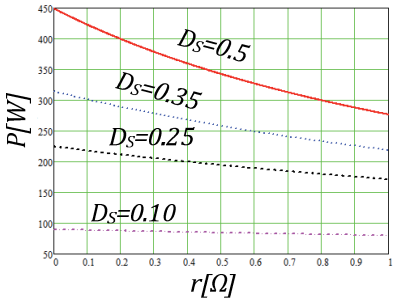


Fig. 6. Impact of r on the output power for different duty cycle values.

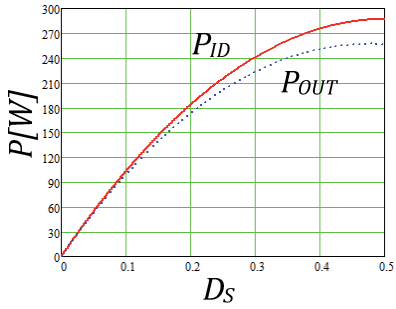


Fig. 7. Impact of the component losses on the output power (P_{OUT}) compared with the ideal output power (P_{ID}).

$$U_{C1} = U_{DC} = \frac{U_{LV} - U_{CE} D_S - I_L r_L}{1 - D_S}. \quad (27)$$

The transferred power of the converter can be evaluated according to (14) and inductor current according to (21). In order to obtain the losses in the capacitor C_1, the maximum value of the I_L has to be determined. The peak of capacitor current depends on the peak value of the inductor current $I_{L,MAX}$ in a following way

$$I_C = \frac{I_{L,MAX} - I_L}{2}, \quad (28)$$

where $I_{L,MAX}$ can be evaluated as follows:

$$I_{L,MAX} = I_L + \frac{\Delta I_L}{2} = I_L + \frac{U_{LV} - U_{CE} - I_L \cdot r_L}{4 f \cdot L_1} D_S. \quad (29)$$

Due to the symmetry of the capacitor current and considering that current changes linearly the loss power in the switch T_C can be described as follows

$$P_C = I_C \left(\frac{1 - D_S}{2} \right) \cdot (U_{CE} + U_D). \quad (30)$$

V. Impact of Component Losses on the Efficiency

In order to facilitate the impact of the component losses on the efficiency of the converter the mathematical models derived in previous chapter are used. In addition, the efficiency was measured on the experimental prototype in the nominal operation point. Considering that the power can flow in both directions the efficiency can be determined using the ratio of the output and input power.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{|P_{OUT}|}{|P_{OUT}| + P_{LOSS}}, \quad (34)$$

where P_{LOSS} is a sum of the conduction losses in the inductor (P_L), transistor T_C (P_C) and in the bridge IGBTs (P_{IGBT}) and active resistance of HF transformer P_r.

$$P_{LOSS} = P_L + P_C + P_r + P_{IGBT}. \quad (35)$$

Fig. 9. shows the impact of the collector-to-emitter voltage drop U_{CE} on the efficiency of the converter for different shoot-through duty cycle values. It can be seen that U_{CE} has a significant impact on the efficiency, and e.g. can decrease the efficiency from 97% (U_{CE} = 0 V) to 83 % (U_{CE} = 3V). For this reason the transistors with as small U_{CE} as possible should be selected. In addition, increasing the input voltage would decrease the impact of U_{CE} on the overall efficiency. For applications with lower currents the MOSFET-s should be considered, in order to achieve higher efficiency.

Fig. 10. depicts the impact of the diode voltage drop U_D on the efficiency of the converter. If power is transferred from LV side towards the HV side then the freewheeling diodes of the transistors carry the major current on the HV side. Due to high voltage, the impact of the U_D is insignificant. However, in high current application the U_D can have remarkable influence on the overall losses.

Fig. 11. shows the influence of the active resistance of the filter inductor L_1 on the efficiency of the converter. As can be seen, the increase of r_L can decrease the efficiency from 91 % (r_L = 0 Ω) even to 61 % (r_L = 3 Ω). Thus the active resistance should be minimized by using wires with as high conductivity as possible. In practice, the active resistance damps the oscillations that are caused by the LC circuit and thus should have reasonable value.

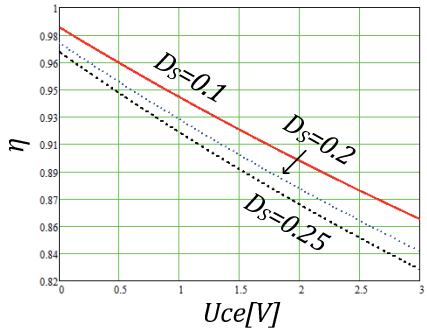


Fig. 8. Impact of the collector-emitter voltage drop on the efficiency of the converter with different duty cycle DS rates

The experimental prototype was used to verify the results. The IGBTs type IRG7Ph42ud1pbf was used to form the DAB and transformer with the turns ratio of 1:1 was used. The voltages and currents on the input and output ports were measured. The measured waveforms are shown in the Fig. 12. The test was carried out using the shoot-through duty cycle of

D_S = 0.1 and with the maximal phase angle value $D_\varphi = D_S$. The measured efficiency comprised 83 %. According to the mathematical models, the expected efficiency is roughly 92 %, without considering the switching losses and core losses and conduction losses caused by the switching transients.

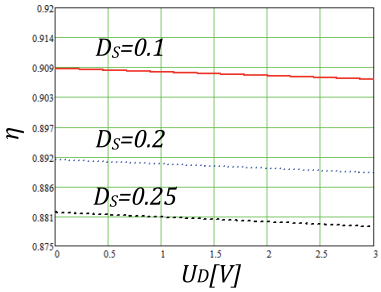


Fig. 9. Impact of the diode voltage drop on the efficiency of the converter with different duty cycle D_S rates

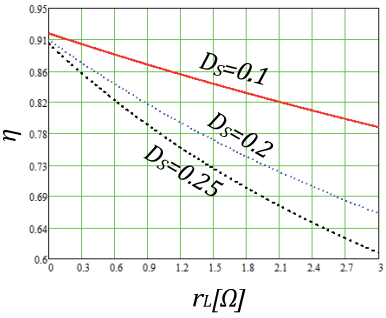


Fig. 10. Impact of the inductor resistance r_L on the efficiency of the converter with different duty cycle D_S rates

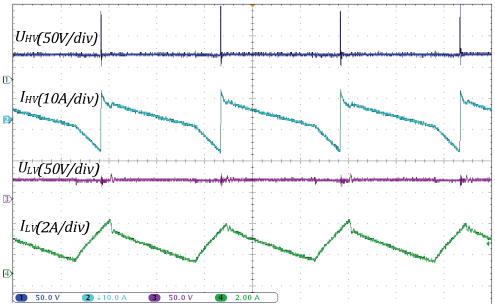


Fig. 11. Experimental waveforms of voltages on the LV side (U_{LV}), HV side (U_{HV}) and current on LV side (I_{LV}) and HV side (I_{HV})

VI. Conclusion

The paper presented a steady state analysis of the commutating LC-based DAB considering the conduction losses in the components. The LC filter offers the input voltage elevation properties that are necessary to keep the voltage on the transformer LV port on the desired level, so that the lowest current stress on the devices is achieved. The derived mathematical models did not consider the switching losses, the switching transients and the core losses. However, the analysis of conduction losses has shown that the active resistance of the transformer decreases the output power of the converter. Moreover, the analysis showed that collector-to-emitter voltage drop and the active resistance of the filter inductor have notable impact on the efficiency of the converter. The experimental result was carried out in one operating point, keeping the DC link voltage on the desired level. The experimental result showed efficiency of 83 %. The 92 % efficiency was expected from the derived mathematical models, however such difference can be explained by the fact, that switching and core losses were not taken into account in the mathematical models. In practise, special considerations regarding EMI are needed for the voltage-fed topologies whose control method includes the shoot-through state of the switches.

Acknowledgment

The authors would like to thank the Estonian Ministry of Education and Research (Project SF0140016s11), Estonian Research Council (Grant ETF8538, ETF8687) and European Regional Fund´s for the support of this research.

This research work was partially supported by Latvian State Research Programme “LATENERGI” and Latvian Council of Science (Grant 416/2012).

References

[1] She, Xu; Burgos, Rolando; Wang, Gangyao; Wang, Fei; Huang, Alex Q.; , "Review of solid state transformer in the distribution system: From components to field application," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.4077-4084, 15-20 Sept. 2012

[2] van der Merwe, J.W.; du T. Mouton, H.; , "The solid-state transformer concept: A new era in power distribution," *AFRICON, 2009. AFRICON '09.* , vol., no., pp.1-6, 23-25 Sept. 2009.

[3] Heinemann, L.; Mauthe, G.; , "The universal power electronics based distribution transformer, an unified approach," Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual , vol.2, no., pp.504-509 vol.2, 2001

[4] Beldjajev, V.; Roasto, I.; , “State of art trends and design challenges of power electronic transformer for future distribution grids” *Технічна електродинаміка*, vol., no. 3, pp.55-62, 2012.

[5] Yu Du; Seunghun Baek; Bhattacharya, S.; Huang, A.Q.; , "High-voltage high-frequency transformer design for a 7.2kV to 120V/240V 20kVA solid state transformer," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.493-498, 7-10 Nov. 2010

[6] Sangtaek Han; Divan, D.; , "Dual active bridge buck-boost converter," *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE* , vol., no., pp.2905-2911, 20-24 Sept. 2009

[7] Zakis, J.; Vinnikov, D.; Rankis, I.; , "Steady state analysis of the galvanically isolated DC/DC converter with a commutating LC filter," *Industrial Technology (ICIT), 2012 IEEE International Conference on* , vol., no., pp.827-832, 19-21 March 2012

[8] Lindroth, I.; Melchert, P.; Sahlstrom, T.; , "Methods of improving efficiency in wide input range boost converters at low input voltages," *Telecommunications Energy Conference, 2000. INTELEC. Twenty-second International* , vol., no., pp.424-431, 2000.

[9] Watson, R., Lee, F.C., “A soft-switched, full-bridge boost converter employing an active-clamp circuit,” IEEE PESC, 1996, Volume: 2, Page(s): 1948 -1954 .

[10] Lizhi Zhu; Kunrong Wang; Lee, F.C.; Jih-Sheng Lai, “New start-up schemes for isolated full-bridge boost converters,” *IEEE APEC 2000*, Page(s): 309-313 vol.1

[11] Hanju Cha; Jungwan Choi; Enjeti, P.N., "A Three-Phase Current-Fed DC/DC Converter With Active Clamp for Low-DC Renewable Energy Sources," *Power Electronics, IEEE Transactions on* , vol.23, no.6, pp.2784,2793, Nov. 2008

DISSERTATIONS DEFENDED AT
TALLINN UNIVERSITY OF TECHNOLOGY ON
POWER ENGINEERING, ELECTRICAL ENGINEERING, MINING ENGINEERING

1. **Jaan Tehver**. Boiling on Porous Surface. 1992.
2. Salastatud.
3. **Endel Risthein.** Electricity Supply of Industrial Plants. 1993.
4. **Tõnu Trump**. Some New Aspects of Digital Filtering. 1993.
5. **Vello Sarv.** Synthesis and Design of Power Converters with Reduced Distortions Using Optimal Energy Exchange Control. 1994.
6. **Ivan Klevtsov**. Strained Condition Diagnosis and Fatigue Life Prediction for Metals under Cyclic Temperature Oscillations. 1994.
7. **Ants Meister**. Some Phase-Sensitive and Spectral Methods in Biomedical Engineering. 1994.
8. **Mati Meldorf**. Steady-State Monitoring of Power System. 1995.
9. **Jüri-Rivaldo Pastarus**. Large Cavern Stability in the Maardu Granite Deposit. 1996.
10. **Enn Velmre**. Modeling and Simulation of Bipolar Semiconductor Devices. 1996.
11. **Kalju Meigas**. Coherent Photodetection with a Laser. 1997.
12. **Andres Udal**. Development of Numerical Semiconductor Device Models and Their Application in Device Theory and Design. 1998.
13. **Kuno Janson**. Paralleel- ja järjestikresonantsi parameetrilise vaheldumisega võrgusageduslik resonantsmuundur ja tema rakendamine. 2001.
14. **Jüri Joller**. Research and Development of Energy Saving Traction Drives for Trams. 2001.
15. **Ingo Valgma**. Geographical Information System for Oil Shale Mining – MGIS. 2002.
16. **Raik Jansikene**. Research, Design and Application of Magnetohydrodynamical (MHD) Devices for Automation of Casting Industry. 2003.
17. **Oleg Nikitin**. Optimization of the Room-and-Pillar Mining Technology for Oil-Shale Mines. 2003.
18. **Viktor Bolgov**. Load Current Stabilization and Suppression of Flicker in AC Arc Furnace Power Supply by Series-Connected Saturable Reactor. 2004.
19. **Raine Pajo**. Power System Stability Monitoring – an Approach of Electrical Load Modelling. 2004.
20. **Jelena Shuvalova**. Optimal Approximation of Input-Output Characteristics of Power Units and Plants. 2004.
21. **Nikolai Dorovatovski**. Thermographic Diagnostics of Electrical Equipment of Eesti Energia Ltd. 2004.
22. **Katrin Erg**. Groundwater Sulphate Content Changes in Estonian Underground Oil Shale Mines. 2005.

23. **Argo Rosin**. Control, Supervision and Operation Diagnostics of Light Rail Electric Transport. 2005.
24. **Dmitri Vinnikov**. Research, Design and Implementation of Auxiliary Power Supplies for the Light Rail Vehicles. 2005.
25. **Madis Lehtla**. Microprocessor Control Systems of Light Rail Vehicle Traction Drives. 2006.
26. **Jevgeni Šklovski**. LC Circuit with Parallel and Series Resonance Alternation in Switch-Mode Converters. 2007.
27. **Sten Suuroja**. Comparative Morphological Analysis of the Early Paleozoic Marine Impact Structures Kärdla and Neugrund, Estonia. 2007.
28. **Sergei Sabanov**. Risk Assessment Methods in Estonian Oil Shale Mining Industry. 2008.
29. **Vitali Boiko**. Development and Research of the Traction Asynchronous Multimotor Drive. 2008.
30. **Tauno Tammeoja**. Economic Model of Oil Shale Flows and Cost. 2008.
31. **Jelena Armas**. Quality Criterion of road Lighting Measurement and Exploring. 2008.
32. **Olavi Tammemäe**. Basics for Geotechnical Engineering Explorations Considering Needed Legal Changes. 2008.
33. **Mart Landsberg**. Long-Term Capacity Planning and Feasibility of Nuclear Power in Estonia under Certain Conditions. 2008.
34. **Hardi Torn**. Engineering-Geological Modelling of the Sillamäe Radioactive Tailings Pond Area. 2008.
35. **Aleksander Kilk**. Paljupooluseline püsimagnetitega sünkroongeneraator tuuleagregaatidele. 2008.
36. **Olga Ruban**. Analysis and Development of the PLC Control System with the Distributed I/Os. 2008.
37. **Jako Kilter**. Monitoring of Electrical Distribution Network Operation. 2009.
38. **Ivo Palu**. Impact of Wind Parks on Power System Containing Thermal Power Plants. 2009.
39. **Hannes Agabus**. Large-Scale Integration of Wind Energy into the Power System Considering the Uncertainty Information. 2009.
40. **Kalle Kilk**. Variations of Power Demand and Wind Power Generation and Their Influence to the Operation of Power Systems. 2009.
41. **Indrek Roasto**. Research and Development of Digital Control Systems and Algorithms for High Power, High Voltage Isolated DC/DC Converters. 2009.
42. **Hardi Hõimoja**. Energiatõhususe hindamise ja energiasalvestite arvutuse metoodika linna elektertranspordile. 2009.
43. **Tanel Jalakas**. Research and Development of High-Power High-Voltage DC/DC Converters. 2010.
44. **Helena Lind**. Groundwater Flow Model of the Western Part of the Estonian Oil Shale Deposit. 2010.
45. **Arvi Hamburg**. Analysis of Energy Development Perspectives. 2010.

46. **Mall Orru**. Dependence of Estonian Peat Deposit Properties on Landscape Types and Feeding Conditions. 2010.
47. **Erik Väli**. Best Available Technology for the Environmentally Friendly Mining with Surface Miner. 2011.
48. **Tarmo Tohver**. Utilization of Waste Rock from Oil Shale Mining. 2011.
49. **Mikhail Egorov**. Research and Development of Control Methods for Low-Loss IGBT Inverter-Fed Induction Motor Drives. 2011.
50. **Toomas Vinnal**. Eesti ettevõtete elektritarbimise uurimine ja soovituste väljatöötamine tarbimise optimeerimiseks. 2011.
51. **Veiko Karu**. Potential Usage of Underground Mined Areas in Estonian Oil Shale Deposit. 2012.
52. **Zoja Raud**. Research and Development of an Active Learning Technology for University-Level Education in the Field of Electronics and Power Electronics. 2012.
53. **Andrei Blinov**. Research of Switching Properties and Performance Improvement Methods of High-Voltage IGBT based DC/DC Converters. 2012.
54. **Paul Taklaja**. 110 kV õhuliinide isolatsiooni töökindluse analüüs ja töökindluse tõstmise meetodid. 2012.
55. **Lauri Kütt**. Analysis and Development of Inductive Current Sensor for Power Line On-Line Measurements of Fast Transients. 2012.
56. **Heigo Mõlder**. Vedelmetalli juhitava segamisvõimaluse uurimine alalisvoolu kaarleekahjus. 2012.
57. **Reeli Kuhi-Thalfeldt**. Distributed Electricity Generation and its Possibilities for Meeting the Targets of Energy and Climate Policies. 2012.
58. **Irena Milaševski**. Research and Development of Electronic Ballasts for Smart Lighting Systems with Light Emitting Diodes. 2012.
59. **Anna Andrijanovitš**. New Converter Topologies for Integration of Hydrogen Based Long-Term Energy Storages to Renewable Energy Systems. 2013.