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Common-Ground Energy Router Structure with Enhanced Reliability and Protection

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TalTech Press

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation, and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for doctoral or equivalent academic degree.

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Ühise nulljuhtmega suurendatud töökindluse ja kaitsega energiaruuter

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Contents

List of Publications

The list of author's publications, on the basis of which the thesis has been prepared:

[PAPER-I] S. Rahimpour, O. Husev and D. Vinnikov, "A Family of Bidirectional Solid-State Circuit Breakers with Increased Safety in DC Microgrids," in IEEE Transactions on Industrial Electronics, doi: 10.1109/TIE.2023.3337493.

[PAPER-II] S. Rahimpour, O. Husev, D. Vinnikov, N. V. Kurdkandi and H. Tarzamni, "Fault Management Techniques to Enhance the Reliability of Power Electronic Converters: An Overview," in IEEE Access, vol. 11, pp. 13432-13446, 2023.

[PAPER-III] S. Rahimpour, H. Tarzamni, N. V. Kurdkandi, O. Husev, D. Vinnikov and F. Tahami, "An Overview of Lifetime Management of Power Electronic Converters," in IEEE Access, vol. 10, pp. 109688-109711, 2022.

[PAPER-IV] S. Rahimpour, O. Husev, and D. Vinnikov, "Design and Analysis of a DC Solid-State Circuit Breaker for Residential Energy Router Application," Energies, vol. 15, no. 24, p. 9434, Dec. 2022.

[PAPER-V] S. Rahimpour, O. Husev and D. Vinnikov, "Impedance-Source DC Solid-State Circuit Breakers: An Overview," 2022 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Sorrento, Italy, 2022, pp. 186-191.

[PAPER-VI] T. Hemmati Shahsavar, S. Rahimpour, N. Vosoughi Kurdkandi, A. Fesenko, O. Matiushkin, O. Husev, D. Vinnikov "Comparative Evaluation of Common-Ground Converters for Dual-Purpose Application," Energies, vol. 16, no. 7, p. 2977, Mar. 2023.

[PAPER-VII] M. R. Azizi, S. Rahimpour, O. Husev, and O. Veligorskyi, "Back-to-Back Energy Router Based on Common-Ground Inverters," CPE-POWERENG 2023 – International Conference on Compatibility, Power Electronics and Power Engineering, Tallinn, Estonia, 2023.

[PAPER-VIII] N. V. Kurdkandi, O. Husev, S. Rahimpour, C. Roncero-Clemente, O. Matiushkin and D. Vinnikov, "A Novel Flying Inductor based Grid-Connected Inverter with Buck-Boost Ability," IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, Brussels, Belgium, 2022, pp. 1-6, doi: 10.1109/IECON49645.2022.9968954.

[PAPER-IX] S. Rahimpour, O. Matiushkin, N. V. Kurdkandi, M. Najafzadeh, O. Husev and D. Vinnikov, "Model Predictive Control of a Single-Stage Flying Inductor Based Buck-Boost Grid-Connected Common-Ground Inverter," 2021 IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia, 2021, pp. 1-6.

Author's Contribution to the Publications

Contribution to the papers in this thesis are:

[PAPER-I] Saeed Rahimpour is the main author of the paper. He proposed and simulated the circuit, calculated the parameters of the circuit, designed the PCB, and prototyped and tested the circuit.

[PAPER-II] Saeed Rahimpour as the main author of the paper, reviewed and investigated the references and authored the paper.

[PAPER-III] Saeed Rahimpour as the main author of the paper, reviewed and investigated the references and authored the paper.

[PAPER-IV] Saeed Rahimpour as the main author of the paper, proposed and simulated the circuit, calculated the parameters of the circuit, designed the PCB, and prototyped and tested the circuit.

[PAPER-V] Saeed Rahimpour as the main author of the paper, reviewed and investigated the references and authored the paper. He presented the paper at 2022 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM).

[PAPER-VI] Saeed Rahimpour as the co-author of the paper, reviewed and investigated the references and authored the paper.

[PAPER-VII] Saeed Rahimpour as the co-author of the paper, was responsible for methodology, surveying, writing and draft preparation.

[PAPER-VIII] Saeed Rahimpour as the co-author of the paper, was responsible for methodology, surveying, writing and draft preparation.

[PAPER-IX] Saeed Rahimpour as the main author of the paper, implemented the control technique and simulated the circuit. He calculated the parameters of the circuit and authored the paper. He presented the paper at 2021 IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON).

Abbreviations

AC (ac)	Alternating Current
ALT	Accelerated Life Testing
ANPC	Active Neutral Point Clamped
CB	Circuit Breaker
CDF	Cumulative Distribution Function
CMC	Cascaded Multilevel Converter
SiC	Silicon Carbide
DC (dc)	Direct Current
DfR	Design for Reliability
EMI	Electromagnetic Interference
EV	Electric Vehicle
FMEA	Failure Mode and Effects Analysis
FTA	Fault-Tree Analysis
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
MC	Markov Chain
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NPS	Neutral Phase Shift
PCB	Printed Circuit Board
PDF	Probability Density Function
PV	Photovoltaic
PWM	Pulse Width Modulation
RBD	Reliability Block Diagram
RMS	Root Mean Square
RUL	Remaining Useful Life
SiC	Silicon Carbide
SSCB	Solid State Circuit Breaker
TalTech	Tallinn University of Technology
THD	Total Harmonic Distortion
TRL	Technology Readiness Level
TSV	Total Standing Voltage

Symbols

μ_V	Voltage utilization rate of the switch
V_{dc}	Input dc Voltage
P	Rated Power
V_{in}	Input Voltage
i_N	Nominal current
S_{i}	MOSFET
D_{i}	Diode
R_S	Snubber Resistor
C_S	Snubber Capacitor
MOV	Snubber MOV
L_{Line}	Input side Inductor
L_{Out}	Output side Inductor
R_{Load}	Load Resistor
R_{i}	Resistor
V_{clamp}	Maximum clamp dc voltage of MOV
E_r	Surge energy on the MOV
I_{Surge}	Maximum surge current of MOV
I_P	Peak short circuit current
v_C	Voltage of capacitor
v_{MOV}	Voltage of MOV
$R_{ds(on)}$	Drain-source on resistance of switch
K_{i}	Relay
D	Duty cycle
i_L	Current of inductor
I_{Limit}	Detection current limit
V_{GS}	Gate-source voltage
$V_{O,max}$	Maximum output voltage
AD	Damage accumulation
λ	Failure rate
π_T	Temperature Factor
π_E	Quality Factor
π_Q	Environment factor
π_J	Junction Temperature
π_S	Voltage stress factor
π_R	Current factor
N	number of power cycles generated by the rainflow counting algorithm
μ_{SSCB}	Efficiency of circuit breaker
$V_{S,max}$	Maximum voltage of the switch

1 Introduction

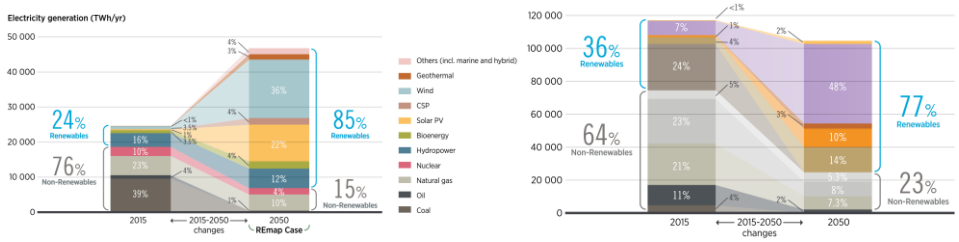
This thesis explores the development of an energy router capable of managing both ac and dc inputs efficiently. This research aims to enhance the reliability and protection mechanisms of energy routers, contributing to a sustainable and efficient energy future.

1.1 Background

The global energy landscape is undergoing a profound transformation marked by an undeniable shift towards sustainable and renewable energy sources [1]. Over the past few decades, there has been a significant increase in the generation of electricity, driven not only by escalating global energy demands but also by a growing awareness of the environmental impact of traditional non-renewable energy sources. This paradigm shift is evident in the increasing prominence of renewable energy technologies, which are gradually overtaking their non-renewable counterparts. Renewable energy technologies, including solar, wind, hydro, and geothermal, have gained momentum as viable alternatives to conventional fossil fuels and nuclear power. These sources are characterized by their inherent sustainability, lower environmental impact, and a reduced carbon footprint compared to traditional non-renewable energy sources. As demonstrated in Fig. 1.1, projections suggest that by 2050, the share of electricity generated from renewable sources will experience a remarkable upswing (from 24% to 85%), marking a transformative departure from the dominance of fossil fuels.

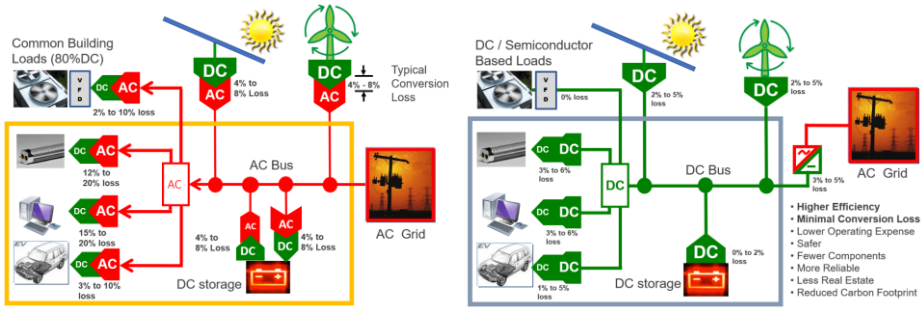
The rising demand for cleaner and sustainable energy sources has led to the proliferation of renewable energy systems, such as solar photovoltaics and wind turbines, which often generate dc power. Simultaneously, traditional power grids predominantly operate on ac. Most of the energy-efficient equipment we use in our homes and businesses now, from lighting to heat pumps and laptops, runs on dc and the ac power coming into our buildings has to be converted to dc. With each conversion, energy is wasted.

As demonstrated in Fig. 1.2, the loss of energy conversion in buildings using ac power is significantly higher than in buildings using dc power. Therefore, integration of ac and dc power necessitates a transformative approach to energy routing, advocating for a unified infrastructure that can efficiently manage both ac and dc inputs.



(a) (b)

Figure 1.1 (a) Electricity generation trend from 2015 till 2050. (b) The trend of the energy consumption of buildings from 2015 till 2050 [2].



(a) (b)

Figure 1.2. (a) Building based on ac input (b) The residential building based on dc input [3].

1.2 Motivation of the Thesis

In the dynamic landscape of modern energy systems, the integration of diverse energy sources and the optimization of energy distribution have become critical imperatives. The coexistence of ac and dc technologies has emerged as a promising solution for achieving greater flexibility, efficiency, and resilience in energy systems. As a solution, the energy router for residential applications has terminals for both ac and dc source and loads.

Furthermore, the integration of advanced protection systems is essential to safeguard the energy router and the connected infrastructure against potential faults, surges, and other adverse events. The thesis will explore innovative protection mechanisms which provide a more reliable and safer performance of the device along with enhanced human safety.

By undertaking this research, the thesis aspires to contribute significantly to the advancement of energy infrastructure, facilitating the seamless integration of diverse energy sources while enhancing the reliability and protection mechanisms of the energy router. The outcomes of this work are expected to catalyze progress towards a more sustainable, efficient, and resilient energy future.

1.3 Aims, Hypothesis and Research Tasks

The main aim of the PhD research is to develop and experimentally confirm a concept of a novel structure of energy router which is applicable for both types of the grids including dc and ac. It is being considered as solution which may speed up transition from conventional ac systems to the hybrid systems for using both ac and dc. The author sets the goal to utilize a smart power management system within the energy router structure along with increasing its safety and reliability.

Hypotheses:

1. Advanced solid-state circuit breakers provide completely safe operation of the energy router in case of a fault.
2. Common-ground interface solves the leakage current issue with no isolation requirements.

3. Fault-tolerant approaches increase reliability of energy router for residential application without significant redundancy.
4. Single-phase power electronic interface with smart internal relays and energy management algorithm is sufficient to balance three-phase single-family house supply system.

Research tasks:

1. Review of the fault-tolerant converters and lifetime management techniques.
2. Development of general structure and requirements for a new configuration of energy routers for residential applications with ac and dc terminals.
3. Evaluating common-ground interfaces suitable for industrial applications.
4. Design of advanced fault-tolerant ac/dc common-ground interface.
5. Design and analysis of reliable advanced solid-state circuit breakers for dc terminals with improved protection capability.
6. Experimental evaluation of the designed energy router prototype with low level control algorithms.

1.4 Research Methods

The research methods used to carry out the thesis are based on mathematical analysis, simulation models and experimental verification. New developed topologies and circuits are mathematically analyzed using the MAPLE software. To study the operating properties of the new topologies and control algorithms, dynamic and static models are developed. Circuit simulations are performed in PSIM software. Altium Designer has been used for designing the circuit. All necessary software licenses have been provided by Tallinn University of Technology. Experimental investigation and validation of theoretically predicted results are performed using laboratory physical models of the new topologies including the energy router and two solid state circuit breakers. The Power Electronics Research Laboratory of TalTech has modern facilities (digital oscilloscopes and function generators, power quality and efficiency analyzers, microprocessor development tools, PCB prototyping, and assembling tools, etc.) for the hardware and software development.

1.5 Contributions and Disseminations

The results of the research are approbated via scientific publications, conferences, symposiums, doctoral schools, and presentations. During the PhD studies the author contributed to 9 publications. Among them, 5 papers were published in peer-reviewed international journals including 4 papers as the first author. In addition, 4 papers were presented at international IEEE conferences. In total, the dissertation is based on 9 main scientific publications, including five journals and four conference papers presented at IEEE international conferences.

Scientific novelties:

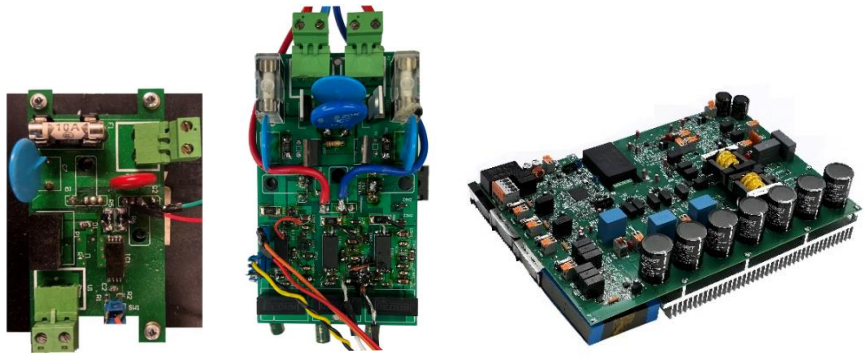
- Innovative classification framework based on a comprehensive review of lifetime management and fault management techniques.
- New configuration of three-phase energy router structure with single-phase power electronic interface.
- Novel solutions for solid-state circuit breakers improved protection capability.
- Novel fault-tolerant five-level common-ground inverter.

Practical contributions:

- Implementation of low-level control algorithms in experimental prototypes.
- Experimental verification of all solid-state circuit breakers.
- Experimental verification of the energy router.

1.6 Experimental Setup and Instruments

The experimental setups were assembled in power electronics laboratory of Taltech including the prototype of the SSCB with soft-reclosing capability as shown in Fig. 1.3(a), the SSCB with enhanced safety as shown in Fig. 1.3(b), and energy router the prototype of the energy router as shown in Fig. 1.3(c). The workspace in the lab and the prototypes are the lab are shown in Figure 1.4. The oscilloscope Tektronix MDO4034B-3 helps to catch the waveforms of voltages and currents of the passive components. The special probes Tektronix P5205A and Tektronix TCP0030A were used for voltage and current measurements correspondently. The Code Composer Studio is used as the environment for writing code for MCU from Texas Instruments, it was used during code development.



(a) (b) (c)

Figure 1.3 Power electronic circuits prototyped in power electronic laboratory of Taltech. (a) the SSCB with soft-reclosing capibility, (b) the SSCB with enhanced safety, (c) the energy router

1.7 Thesis Outline

Chapter 2 describes the review of lifetime management techniques and fault-tolerant converters.

The principles of common-ground structures along with proposing two common-ground inverters including a fault-tolerant inverter are considered in Chapter 3.

In Chapter 4, an SSCB is proposed introducing a soft reclosing approach. In addition, a family of bidirectional SSCBs with increased safety is proposed, and the topologies are analyzed. The experimental results of these structures are included and discussed presenting the validity of the results.

Chapter 5 includes the description of the novel structure of the energy router. This chapter includes the experimental results of the various tests of the energy router.

2 Lifetime management techniques and fault-tolerant converters

Faults in power electronic systems may not only cause unscheduled interruptions, but they may also cause disastrous accidents that cannot be tolerated. Therefore, reliability is a fundamental aspect of power electronics design, ensuring safe, efficient, and consistent operation of electronic systems in various applications. Fig. 2.1. depicts the general guideline for the reliability of power electronic based systems. As shown in this diagram, a power converter's reliability can be discussed from two perspectives, including fault management and lifetime management. Both of these areas are typically considered separate subjects when it comes to research. Fault management is concerned with sudden catastrophic faults in converters, such as shorts and open circuits. It involves diagnosing, isolating, and configuring faults after they have already occurred in order to protect systems from faults. Another aspect of reliability is lifetime management, which involves analyzing, predicting, and extending the lifetime of power electronics.

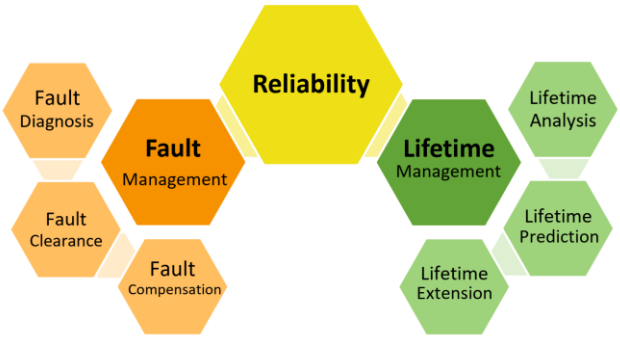


Figure 2.1 Guideline of the reliability of power electronic systems [4].

2.1 Lifetime management techniques

Lifetime management of power electronic systems is significant as it ensures optimal performance, reliability, and sustainability while reducing maintenance costs and extending system longevity. Lifetime management consists of three major categories: lifetime analysis, lifetime prediction and lifetime extension as shown in Fig. 2.2.

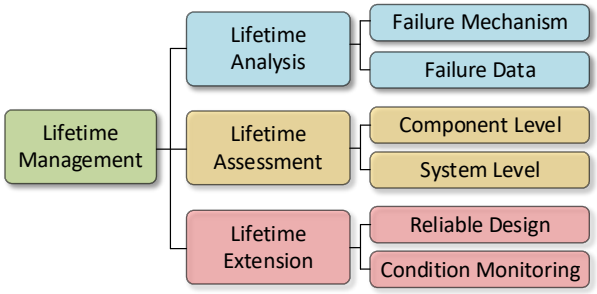


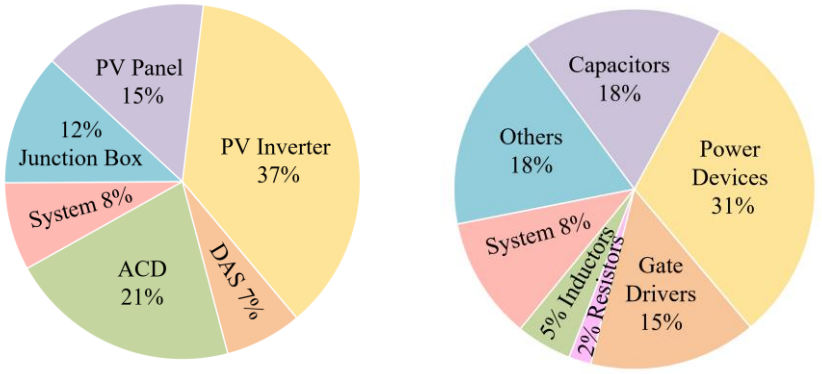
Figure 2.2 Guideline of lifetime management.

2.1.1 Lifetime analysis

Lifetime analysis is the fundamental step of lifetime management that involves identifying the prone-to-failure components along with the failure mechanisms, failure modes, failure causes, and failure indicators.

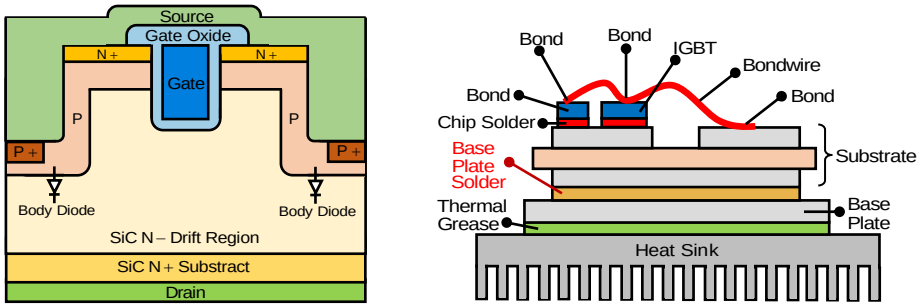
Among various power electronic based products, according to the pie chart shown in Fig. 2.3(a), the reliability of PV systems is severely affected by inverters. In fact, inverters are the most subject to failures with about 37 percent of the whole unscheduled maintenance. Because of their frequent on-off switching and the influence of thermal and electrical overstress, power semiconductors are more prone to failure than those in the rest of the drive system. As demonstrated in Fig. 2.3(b), these power devices such as IGBTs and MOSFETs account for about 31% of an inverter's failures and by considering the fault of the gate drivers, the total failure rate related to the switching devices is approximately 46%. Additionally, the figure shows that capacitors are the second most likely component to fail in power converters. If a converter lacks redundancy or reconfiguration, a failure of one of these components will cause the converter to fail, which is considered catastrophic in mission-critical applications.

Failures in Silicon Carbide (SiC) MOSFETs can be studied at the Chip-level structure (Fig. 2.4(a)) and the package-level structure (Fig. 2.4(b)). Chip-level failures in SiC MOSFETs are primarily due to gate oxide and body diode degradation, with gate oxide failure caused by tunnelling currents, high electric field stress, and high temperature stress, resulting in increased gate leakage current and threshold voltage shifts. Body diode failure is typically due to recombination-induced stacking faults from forward voltage bias stress, leading to higher forward voltage and drain leakage current. At the package level, failures often occur in bond wires and solder layers due to thermomechanical stress from CTE mismatch, humidity-induced corrosion, and high current density stress accelerating electromigration-related degradation [5]. Although various failure mechanisms have been identified, most current lifetime prediction models primarily address package-related failures.



(a) (b)

Figure 2.3 (a) Failure probability share of various parts of a PV plant. (b) Share of each component of a converter in converters' failure.



(a) (b)

Figure 2.4 (a) SiC MOSFET chip-level structure. (b) SiC MOSFET package-level structure.

The failure data is the input for the lifetime prediction process. As demonstrated in Fig. 2.5, this failure data can be classified into three main categories: mission-profile based data, historical data, and data derived from accelerated tests, also known as test data. Mission-profile based data pertains to failure occurrences under actual operating conditions and specific use-cases, providing real-world insights into performance and reliability. Historical data encompasses records of past failures and maintenance logs, offering a comprehensive view of long-term trends and common failure patterns. Accelerated test data is obtained through rigorous testing procedures designed to simulate extended use or extreme conditions in a shorter timeframe, thereby identifying potential failure mechanisms and enhancing predictive accuracy. By integrating these diverse data sources, the lifetime prediction process becomes more robust and capable of providing reliable forecasts of system longevity and maintenance needs. The failure data is the input of the lifetime prediction process.

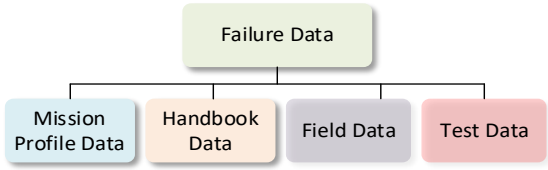
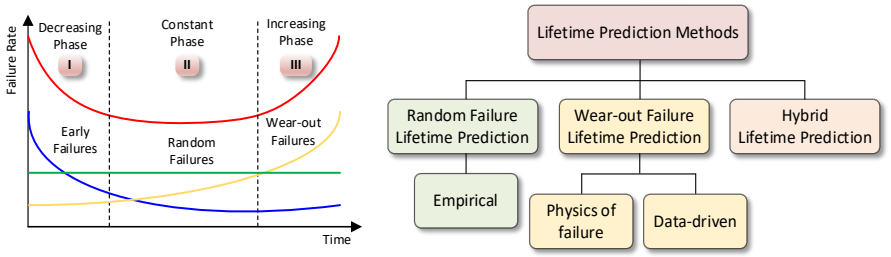


Figure 2.5 Different types of failure data for lifetime prediction process.

2.1.2 Lifetime assessment

The short lifetime of power electronic devices is usually caused by thermal stresses caused by their switching devices, such as IGBTs and MOSFETs. These components may fail due to a catastrophic failure (such as an open-circuit or short-circuit) or a wear-out failure, which affects the system's reliable operation. It is therefore necessary for converter manufacturers and operators to develop an appropriate assessment procedure to improve the reliability of converters, particularly the switching devices. [6].

The lifetime estimation of a power electronic system is first conducted using the component-level models to estimate the failure rate of each component. Afterwards, system-level lifetime estimates are generated based on the summed failure rates.



(a) (b)

Figure 2.6. (a) Bathtub curve of the failure rate. (b) Classification of Lifetime Prediction Methods.

Reliability, unlike other conventional performance indicators for power electronic systems, like power density, efficiency, total harmonic distortion, etc., is hard to measure and quantify. The failure rate $\lambda(t)$ (also called hazard rate $h(t)$) is one of the widely used reliability metrics in reliability engineering. It is defined as the frequency with which a component or a system fails. Based on the conventional life cycle bathtub curve, as demonstrated in Fig. 2.6(a), there are three regions for the failure rate of electronics devices over time including early failures, constant random failures, and wear-out failures. The first part of the curve is dedicated to early failures. During this period, high numbers of failures occur as a result of errors in the design process or manufacturing procedures. The failure rate, however, decreases over time due to the removal of defective and failed products at the beginning of the stage. Early life failures can be addressed through burn-in or screening tests.

As depicted in Fig. 2.6(b), lifetime prediction methods can be classified into three categories: random failure lifetime prediction methods, wear-out failure lifetime prediction methods and hybrid methods which are applied by combination of the random and wear-out failure methods.

Empirical or handbook-based prediction methods are based on models developed from statistical curve fitting of historical failure data, which may have been collected in the field or from manufacturers. Typically, these methods provide reliability estimates for components with similar or slightly modified characteristics.

The most common handbook used for lifetime estimation is the Military Handbook 217. The general formula for calculating the failure rate (λ) in this method is as follows:

$$\lambda = \lambda_a . \pi_E . \pi_T . \pi_Q . \pi_J . \pi_S . \pi_R \qquad (2-1)$$

Where, λ_b is the base failure rate and other parameters are introduced in Fig. 2.7.

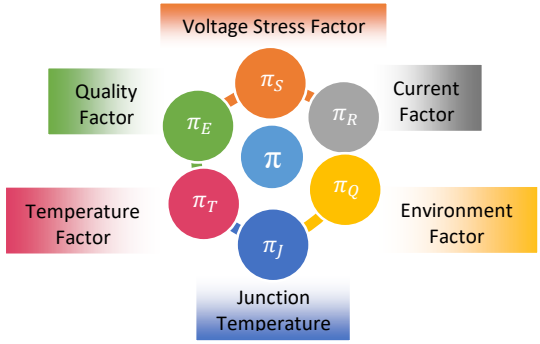


Figure 2.7. Failure parameters diagram.

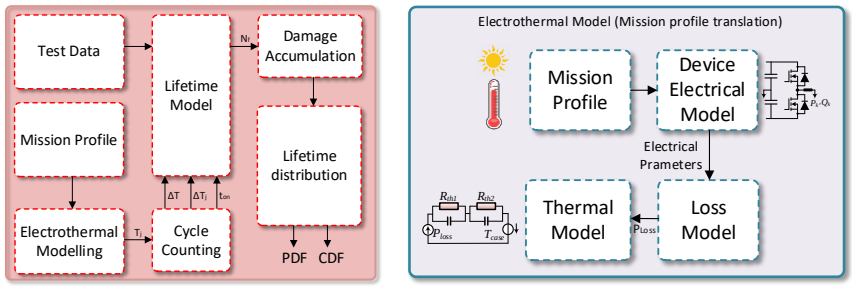
Table 2.1 . Summary of major handbook standards

	MIL-HDBK-217	IEC TR-62380	Telcordia	217plus	FIDES
Last Update	1995	2016	2006	2015	2009
Operation profile	NO	Yes	NO	Yes	Yes
Thermal cycling	NO	Yes	NO	Yes	Yes
Thermal rise in part	Yes	Yes	NO	Yes	Yes
Solder joints failures	NO	Yes	NO	Yes	Yes
Induced failures	NO	NO	NO	Yes	Yes
Failure rate data base for other parts	limited	limited	NO	Yes	Yes
Infant mortality	NO	Yes	NO	Yes	NO
Dormant failure rate	NO	NO	NO	Yes	Yes
Test data integration	Yes	Yes	NO	Yes	NO
Bayesian analysis	NO	NO	NO	Yes	NO

A summary of commonly used handbooks is provided in Table 2.1, and they are explained in detail in the same section that includes the table. Generally, MIL-HDBK-217 failure rate predictions are more pessimistic than other reliability handbook predictions. Some of these handbooks, like FIDES, are still used in some applications, despite the fact that their data is outdated, and their prediction approaches suffer from poor accuracy.

Compared to random failures' lifetime prediction methods, wear-out failures' prediction is often more complex and involves more steps. The diagram in Fig. 2.8(a) This figure illustrates a typical process for predicting wear-out failures. To do so, the first step is to collect failure data from various sources, including mission profiles, testing data, and field data. The next step, if using mission-profile data, would be to translate this data into a thermal profile using electrothermal modelling. Upon completion of the cycle counting process, a suitable lifetime model should be selected in order to calculate the number of failures per cycle. To obtain a precise result, the deviation of the output parameters after the damage accumulation is estimated. Finally, reliability is demonstrated by either Cumulative Distribution Function (CDF) or Probability Density Function (PDF).

The fundamental step in the mission profile-based reliability prediction is translating the converter's mission profile to the corresponding stresses in its prone-to-failure components [7]. Fig. 2.8(b) shows the three steps to translate the mission profile to achieve the junction temperature change.



(a) (b)

Figure 2.8. (a) General diagram of a typical component-level lifetime prediction process. (b) General diagram of a typical electrothermal model.

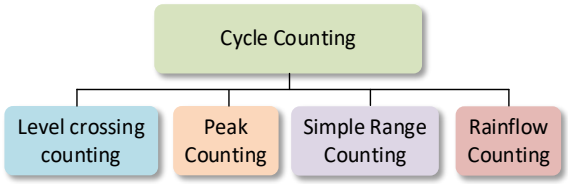


Figure 2.9 Methods of cycle counting.

The next step is cycle counting. A power converter's lifetime is determined by the magnitude and frequency of temperature cycles. Each cycle applies different stresses to the module and results in a particular consumed lifetime. Cycle counting summarizes lengthy irregular load-versus-time histories by providing the number of times cycles of various sizes [8]. The definition of a cycle varies with the method of cycle counting. Several cycle counting methods have been developed for lifetime prediction, three of which are level crossing counting, peak counting, range counting, and rainflow counting.

After cycle counting, it is time to model the lifetime. Fig. 2.10 classifies the wear-out failure lifetime prediction methods and demonstrates the major techniques used in each method. PoF offers better accuracy since the failure rates are calculated based on the actual physics of the components and their failure modes and mechanisms along with the effect of stresses of the product-level on the reliability of the components. There are also data-driven methods in which models are typically “black boxes” with no explicit system knowledge. Data-driven approaches involve learning statistical relationships and patterns from the failure data to provide valuable decision-making information.

Damage accumulation is the next step. Once the damage caused by each thermal cycle has been determined, the total accumulation of damage is calculated, and an estimation of its lifetime can then be obtained using either linear or nonlinear methods. [9]. One of the commonly used methods in damage accumulation evaluation is Palmgren-Miner law [10, 11].

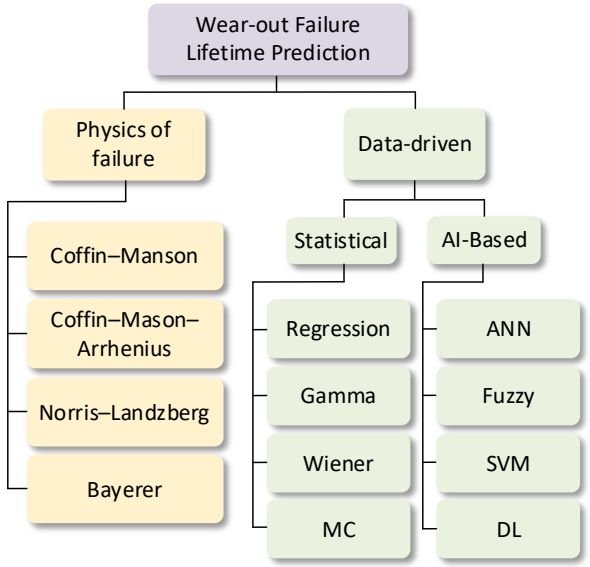


Figure 2.10 Methods of predicting the wear-out failure lifetime.

The formula for calculating the damage accumulation by this method is as follows:

$$AD = \sum_{k=0}^{n} \frac{n_i}{N_i}, \qquad (2-2)$$

where N stands for the total number of power cycles generated by the rainflow counting algorithm, n_i is the number of cycles for i^{th} power cycle, N_i is the number of cycles to failure at the corresponding ΔT_j and T_m in the i^{th} power cycle [12].

The last step of lifetime prediction is parameter estimation and lifetime distribution. The basic idea of parameter estimation is modelling the parameters used in the calculation (e.g., stress parameters in a lifetime model) using a certain distribution function (f(x)), instead fixed parameters [8] with a range of variations (e.g., normal distribution with 5% parameter variation). Thus, uncertainty in practical applications can be represented by parameter variations in the calculation. Monte Carlo simulations are widely used for analyzing the stochastic behavior of model parameters, which represents uncertainty in the prediction [13]. They are based on simulating the model parameters with a certain distribution, representing variation, and randomly selecting them during each simulation.

Afterwards, a set of n samples is carried out to evaluate the lifetime. In this way, the lifetime distribution (e.g., Weibull distribution) of a power electronic component can be constructed based on the lifetime yields of n samples [14].

When the lifetime prediction of all components of a system is determined, one of the system-level lifetime prediction methods is used to map the reliability of the components to the systems. These system-level methods include Reliability Block Diagrams (RBD), Fault-Tree Analysis (FTA), and Markov Chains (MC) [15].

2.1.3 Lifetime extension

Design for Reliability (DfR) and condition monitoring are integral tools in extending the lifetime and enhancing the reliability of power electronic systems, which are critical in applications ranging from renewable energy to industrial automation.

DfR involves incorporating reliability considerations into the design phase, aiming to predict, quantify, and mitigate potential failure modes early in development. This approach includes careful component selection to ensure that only high-quality, durable components are used, capable of withstanding the environmental and operational stresses they will encounter. Effective thermal management strategies, such as employing heat sinks, cooling fans, and advanced materials, are crucial for dissipating heat and maintaining optimal operating temperatures, thereby preventing thermal degradation of components.

Furthermore, DfR emphasizes robust design principles and redundancy. By incorporating redundancy, systems can maintain functionality even if one component fails, enhancing overall resilience. Derating, or operating components below their maximum capacity, along with planning for worst-case scenarios, further bolsters system reliability. Implementing Failure Mode and Effects Analysis (FMEA) systematically identifies potential failure modes, their causes, and their effects on system performance. Addressing these potential issues during the design phase enables engineers to incorporate necessary countermeasures. Accelerated Life Testing (ALT) exposes components to elevated stress conditions, providing valuable data on potential failure

mechanisms and lifespan, which informs design improvements and reliability predictions.

Condition monitoring provides continuous assessment of the system's health and performance during its operational life. This involves using sensors to measure critical parameters such as temperature, voltage, current, and vibration, supplying real-time data essential for monitoring the system's condition. Advanced data analysis and diagnostic algorithms, including machine learning techniques, analyze this data to detect anomalies and diagnose issues early. Predictive analytics can forecast potential failures, allowing for proactive maintenance and timely interventions. Health monitoring systems integrate sensor data and diagnostic tools, offering a comprehensive overview of system health and alerting operators to degrading conditions, thus recommending maintenance actions to prevent failures.

Prognostics further enhances condition monitoring by combining real-time data with models of system behavior to predict the Remaining Useful Life (RUL) of components. This predictive capability facilitates better planning of maintenance schedules, minimizing downtime and extending the system's operational life. The synergy between

DfR and condition monitoring creates a robust framework for managing the lifecycle of power electronic systems. By integrating these methodologies, organizations can significantly reduce unexpected failures, optimize system performance, and lower costs associated with maintenance and downtime. Prioritizing reliability through both design and continuous monitoring leads to more robust and durable power electronic systems, capable of delivering consistent performance over extended lifetimes.

2.2 Fault tolerant converters

Fault tolerant converters are a crucial advancement in the field of power electronics, designed to enhance the resilience and reliability of electrical systems by ensuring continuous operation even in the presence of faults. As the demand for uninterrupted power supply grows in critical applications such as renewable energy systems, electric vehicles, and aerospace technologies, the ability of converters to handle and adapt to failures becomes increasingly vital. These converters incorporate sophisticated design strategies, including redundancy, robust control algorithms, and self-healing mechanisms, to detect, isolate, and mitigate faults without significant interruption. When a fault occurs, the fault management operation is activated which consists of fault diagnosis, fault isolation and fault compensation.

Once a fault occurs, fault diagnosis or fault detection is the first step. A fault diagnostic technique for an inverter can be categorized as model-based or data-driven [16]. The model-based methods are based on the analytical model of the converter [17]. Usually, they need to consider the dynamic properties and operation mechanism of the system before establishing an accurate mathematical model [18]. On the other hand, it is not necessary to know the analytical model of the system to use data-driven fault diagnosis methods as they directly analyze and process the measured data [19]. These techniques include signal processing methods, statistical analysis, and artificial intelligence. In addition to these two methods, the hybrid method uses a combination of these two methods.

Fault isolation is the second step in tackling a fault in a system. When a fault occurs in an inverter, some switching states may be unavailable due to the short-circuit or open

circuit of the faulty switches. These switching states should be avoided or the faulty components themselves should be isolated so that the system continues to function and prevents damage to the entire system. These schemes are performed by adding some extra elements such as fuses and TRIACs and their goal is to isolate the faulty switch(es). Fault isolation usually results in the degradation of the system's performance, especially in the output voltage and Total Harmonic Distortion (THD). Therefore, there have to be solutions to compensate for the effects of the fault which are discussed in section III.

Having isolated the fault, fault compensation schemes are needed to restore the inverter's operation as closely as possible to normal. As shown in Fig. 2.11, fault compensation techniques are classified into three groups: hardware redundancy, switching states redundancy, and unbalance compensation control. An output performance measure such as THD of output voltages and currents, efficiency of the system, and dynamic response should be considered when selecting a fault-tolerant method. Aspects such as cost are also important to consider when comparing fault compensation techniques.

2.2.1 Hardware redundancy

A redundancy scheme is one in which a system feature that is unavailable can simply be replaced with another feature already present [20]. There are two kinds of redundancy in inverters: switching state redundancy, which involves alternative current paths to obtain the same voltage level, or hardware redundancy, which involves extra switches, legs, and modules. The redundant hardware technique involves adding some redundant hardware to the original system. In applications where cost is not a major concern, redundant hardware can be added to the system to provide advantages in post-fault operations [21].

In the switch-redundant topology in Fig. 2.12(a), if one of the upper switches fails open-circuit or short-circuit, it can be replaced by the redundant switch S_{R1} by the correspondent relay. The strategy for the failure of the bottom switches is the same.

As shown in Fig. 2.12(b), some hardware redundant topologies use the redundancy of a whole leg to make the leg replicable when a probable fault occurs. The redundant leg can be connected in parallel or in series.

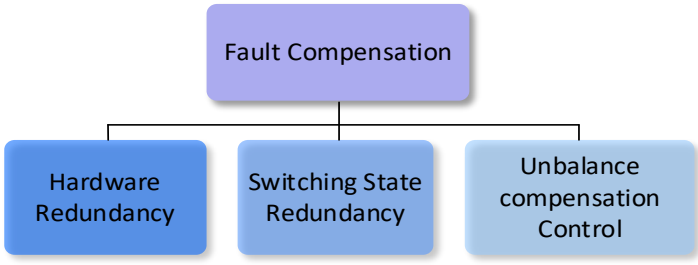


Figure 2.11 Classification of fault Compensation techniques for power converters.

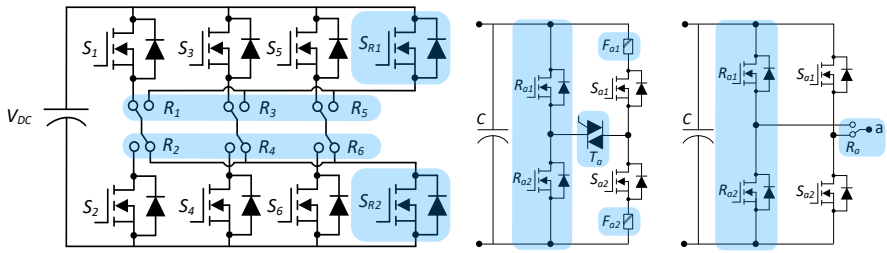


Figure 2.12 (a) Fault-tolerant inverter using parallel switch redundancy proposed in [22]. (b) Fault tolerant topologies using leg redundancy.

2.2.2 Switching States Redundancy

Modulation-based fault clearance includes avoiding the unavailable switching states and minimizing the impact of the fault by a proper switching sequence [23]. In this approach, in case of failure, redundancy in the switching states of the inverter enables the controller to choose an alternate conduction path to retain the same output voltage.

In the three-phase NPC inverter of which the leg "a" and its corresponding phase is shown in Fig. 2.13(a), when one of the switches fail, the faulted state should be avoided because it causes a short-circuit across the bottom or top dc-bus. In the SVM technique, it is enough to exclude the vectors including the faulted phase. With this approach, the fault is cleared, however, the modification of the PWM strategy to avoid unavailable states leads to dc-bus mid-point imbalance, spurious fault detection, and overrating of device voltage to full dc-bus voltage [24].

Active Neutral Point Clamped (ANPC) converter, which is obtained by replacing diodes in NPC with switches, is widely used in high-power medium-voltage applications including distributed generation such as photovoltaic systems, motor control in traction systems, and industrial motor drives [25]. In this converter as shown in Fig. 2.13(b) [26, 27], if an open-circuit fault occurs in the switch S_{a2}, the switches S_{a3} and S_{a6} can be turned on to connect the phase voltage to the dc-bus mid-point which minimizes the impact of the fault by reviving the three-phase system.

In the flying capacitor inverter as shown in Fig. 2.13(c), in the normal mode, the voltage level can be provided by turning on switches S_1, S_3, and S_4 (the current flows through the capacitor C_2 and diode D_2). If for example the switch S_3 fails open, while i_L>0, the same voltage level can be obtained by turning on the switches S_4 and S_1 (the current flows through the capacitor C_3 and diodes D_2 and D_3). On the other hand, in the healthy condition, turning on the switch S_2 (the current flows through capacitors C_1 and C_2, and the diodes D_1, D_3, and D_4) the voltage level is produced. If S_3 fails short, while i_L<0, the same output voltage is obtained when current flows through diodes D_1 to D_4. Therefore, the flying capacitor inverter benefits from the switching state redundancy which makes it retain its output voltage level after an open-circuit or short-circuit fault occurs.

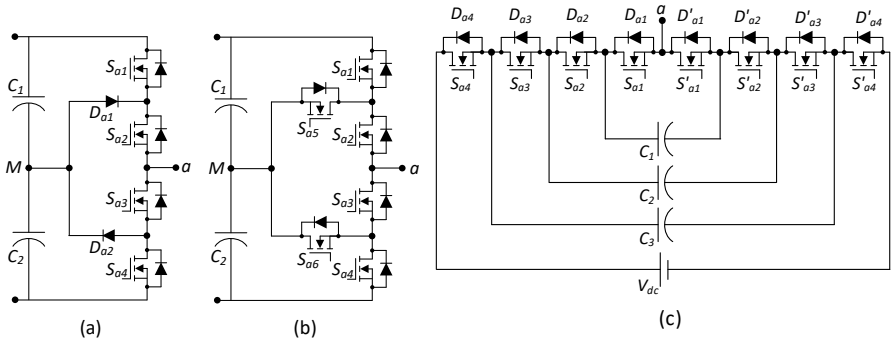


Figure 2.13 (a) One leg of a three-phase NPC inverter, (b) One leg of a three-phase ANPC inverter, (c) Flying capacitor inverter.

2.2.3 Unbalance Compensation Control

Despite the fact that the most important function of an inverter when a fault occurs is to continue servicing as close to normal as possible, other features should also be considered [28]. Imbalance control techniques refer to the altercation of the control strategy to correct the imbalances created by the fault and achieve an optimum operating point concerning the voltage, THD, or any other objective [29]. By using this algorithm, fault-tolerant control can be implemented without changing the inverter's topology. As a result, using them can save hardware costs and simplify topologies [30].

In Neutral Phase Shift (NPS) method, when a fault occurs in a module in a Modular Multilevel Converter (MMC) or Cascaded Multilevel Converter (CMC), one option after isolation of the faulty module is isolating the corresponding modules in the other two phases to keep the output voltage balanced. However, the output voltage is reduced.

By using the NPS method, there is no need to bypass the corresponding healthy modules and have a balanced output at the same time. As shown in Fig. 2.14(a), the line-to-line voltages in normal operation are 8.67 p.u.

When modules W_4, W_5, and V_5 experience a fault, the correspondent healthy modules, which are V_4, U_4, and U_5 are bypassed. The new line-to-line voltages are 5.19 p.u. (Fig. 2.14(b)). By solving the following equations, we can find the angles between phases that make the voltage balanced [31].

$$V_{ab} = {V_a}^2 + {V_b}^2 - 2V_aV_b\cos(\alpha)\,, \qquad (2-3)$$

$$V_{bc} = {V_b}^2 + {V_c}^2 - 2V_bV_c\cos(\beta)\,, \qquad (2-4)$$

$$V_{ca} = {V_c}^2 + {V_a}^2 - 2V_cV_a\cos(\gamma)\,, \qquad (2-5)$$

$$V_{ab} = V_{bc} = V_{ca}, \qquad (2-6)$$

$$\alpha + \beta + \gamma = 360^{\circ}. \qquad (2-7)$$

As shown in Fig. 2.14(b), the output voltage is higher than the conventional method.

This method is similar to the NPS technique with the difference that the output voltage can be sustained at the same level as that in the pre-fault condition [32, 33]. An important drawback of the previous reconfiguration strategy is its effect on the common-mode voltage, which can lead to unbearable stress on the machine bearings [34].

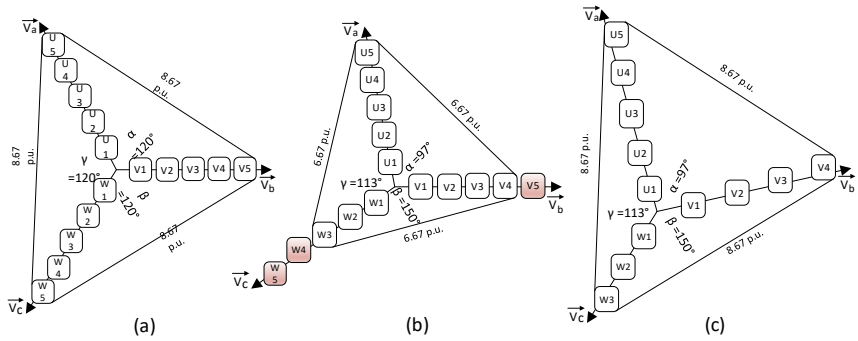


Figure 2.14 The voltage vectors of a modular multilevel inverter (a) Normal Condition, (b) Postfault after implementing NPS approach. (c) Postfault; the overvoltage is shared among three phases.

Voltage extension is another control method for fault management in modular converters. To increase the converter's maximum output range, the average of the maximum and minimum reference phase voltages is injected into the common-mode voltages. When a fault occurs, in order to maintain the output voltage level, the input dc-bus voltage of the faulty phase is increased to keep the total voltage unchanged. As shown in Fig. 2.14(c), the three voltages are balanced, and their value is the same as the normal operation. However, the modules in the phase which had the faulty modules, experience overvoltage. Therefore, to equally share the increased voltage burden among all healthy modules of three phases and optimal angles of the phase voltages are calculated by equations (2-3) to (2-7).

2.3 Summary

The reliability of power electronic systems is crucial to ensure safe and uninterrupted operation in various applications, necessitating comprehensive fault management and lifetime management strategies. Fault management focuses on diagnosing, isolating, and compensating for sudden catastrophic faults, while lifetime management involves analyzing, predicting, and extending the operational life of the systems. Techniques such as DfR and condition monitoring play key roles in enhancing system durability by integrating robust design principles and real-time health assessments. Fault-tolerant converters, which incorporate redundancy and advanced control algorithms, are essential for maintaining continuous operation amidst failures. These converters leverage methods like hardware redundancy, switching state redundancy, and unbalance compensation control to mitigate faults effectively. Voltage extension methods further aid in managing faults by adjusting phase voltages to maintain output levels, thereby ensuring consistent and reliable performance of power electronic systems.

Findings of this section denies the third hypothesis that fault-tolerant approaches increase reliability of energy router for residential application without significant redundancy, since control techniques without redundancy only compensate imbalance in the performance of the converters and cannot fully compensate and clear the fault.

3 Common-ground structure

Despite dc microgrids' advantages, such as flexibility in integrating renewable sources and higher efficiency, they require high protection. Even though dc microgrids have advantages, including higher efficiency, they will be impractical without a reliable protection system. DC system protection is different from that of an ac system. A dc system is protected differently from an ac system. DC systems have many active sources, and each of these sources has a different power level that should be taken into account in comprehensive protection systems. The dc current fault in the dc microgrid increases suddenly during a fault, and since it does not have a zero crossing, it cannot be easily cut; it requires additional equipment to do so [35]. Consequently, there are several aspects to consider from a protection perspective. Only a few studies have been conducted on dc system protection in recent years. [36]. The dc system continues to develop at a slow pace due to a lack of necessary standards and sufficient experience. A dc microgrid can operate independently or in a grid-connected mode, as well as bi-directionally. These operation modes also introduce more challenges to the protection system. It is also important to consider issues related to grounding and the ground current when diagnosing high impedance faults [37].

Capacitive grounding methods (Fig. 3.1(a)) offer advantages such as providing a low-impedance path for common-mode currents to ground, effectively reducing leakage current and enhancing system safety. They are relatively simple to implement and can be cost-effective compared to other grounding techniques. Capacitive grounding methods also do not introduce additional components or losses into the power circuit, which can help maintain system efficiency. However, they may be less effective in high-frequency applications where capacitive coupling with ground can result in increased EMI. Additionally, proper sizing and placement of capacitors are essential to prevent excessive leakage currents and ensure compliance with safety standards. Moreover, capacitive grounding methods may not be suitable for all applications, particularly those with stringent EMC requirements or where galvanic isolation is necessary.

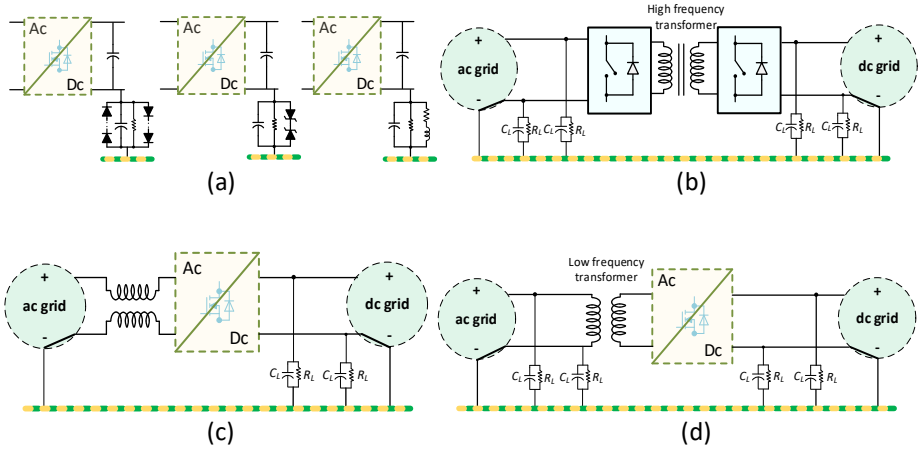


Figure 3.1 Typical solutions to address the leakage current: (a) capacitive grounding methods, (b) high-frequency transformer at the dc side, (c) common-mode choke, (d) a low-frequency transformer at the ac side.

Using a high-frequency transformer at the dc side (Fig. 3.1(b)) to address leakage current in power electronic systems presents advantages such as efficient isolation, which can effectively suppress leakage currents and enhance system safety. High-frequency transformers also offer compact size and reduced weight compared to their low-frequency counterparts, making them suitable for applications with space constraints. Moreover, they allow for higher power density and improved efficiency due to reduced core losses. However, high-frequency transformers may introduce higher Electromagnetic Interference (EMI) and require careful design considerations to minimize losses and maintain high efficiency [38]. Additionally, they may be more expensive and necessitate precise control and protection mechanisms to ensure reliable operation.

Using a common-mode choke at the ac side (Fig. 3.1(c)) to address leakage current in power electronic systems offers advantages such as effective reduction of common-mode noise, which can enhance system reliability and compliance with regulatory standards. Additionally, common-mode chokes can provide protection against ground loops and are relatively simple to implement. However, they come with drawbacks including added cost, size, and weight, as well as potential voltage drop and limited frequency range.

Using a low-frequency transformer at the ac side (Fig. 3.1(d)) to address leakage current in power electronic systems offers advantages such as robust isolation, which effectively suppresses leakage currents and enhances system safety. Low-frequency transformers are known for their reliability and ability to handle high power levels, making them suitable for various industrial applications. Additionally, they typically have lower core losses and produce less EMI compared to high-frequency transformers. However, low-frequency transformers tend to be larger and heavier than their high-frequency counterparts, which may pose challenges in applications with strict space and weight constraints. Moreover, they may exhibit lower efficiency due to higher core losses, necessitating careful design considerations to optimize performance and minimize energy losses.

As demonstrated in Fig. 3.2, a common-ground structure in power electronic systems helps suppress leakage currents primarily by providing a low-impedance path for unwanted currents to return to the power source or ground. By establishing a single reference point for grounding, the common-ground structure ensures that all components share the same ground potential. This reduces the likelihood of voltage differentials between components, which can lead to leakage currents flowing through unintended paths. Additionally, a well-designed common-ground structure minimizes ground loops and reduces electromagnetic interference, further contributing to the suppression of leakage currents. Overall, by promoting a stable and uniform grounding environment, a common-ground structure helps maintain system integrity and safety while mitigating the risks associated with leakage currents.

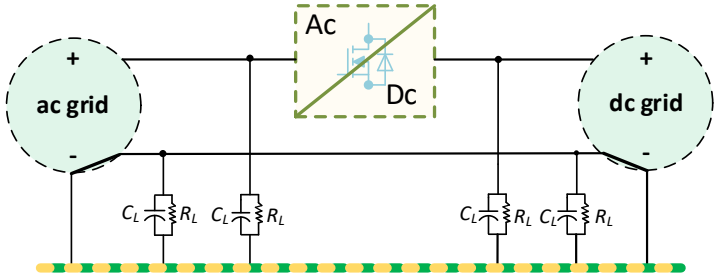


Figure 3.2 Common-ground technique to suppress the leakage current.

3.1 The three-level common-ground inverter

Fig. 3.3 shows the three-level common-ground inverter implemented in the structure of energy router, which consists of five switches, an inductor in series to the input voltage, and a flying capacitor. The converter is common ground as the neutral point of the output side is directly connected to the negative polarity of the input side. The operating states of the inverter are demonstrated in Fig. 3.4. In the first operating state in Fig. 3.4(a) in which the level $+V_O$ is produced, the inductor is in the charging state, while the capacitor is discharged. The operating states in which zero levels are provided are shown in Figs. 3.4(b) and 3.4(c). Once S_1 is turned ON; the current of the inductor ramps up. Once S_2 is triggered to turn ON, the stored energy in the inductor goes down to charge the capacitor. The level $-V_O$ is produced in the operating state in Fig. 3.4(d) in which the capacitor is charging and the inductor discharging. One advantage of this structure is the fixed duty cycle during the boost operation, which simplifies the control strategy. A detailed modulation strategy can be found in [39].

In this converter, the step-up mode works according to the boost converter with a duty cycle of D. Therefore, the ratio of capacitor voltage to the dc input voltage is equal to:

$$V_C = \frac{1}{1-\mathrm{D}} V_{dc}, \qquad (3-1)$$

Where D is the duty cycle of the boost part and corresponds to S_2, which is responsible for the boosting part of the converter. The output ac voltage is also as:

$$V_O = \mathrm{M} V_C \sin(\omega t)\,, \qquad (3-2)$$

where M is the modulation index and corresponds to the amplitude of the sine wave with the same frequency as the output voltage. Also, the peak of fundamental ac output is:

$$V_{O,max} = \mathrm{M} V_C. \qquad (3-3)$$

Finally, the ac to dc gain is expressed as:

$$\mathrm{G} = \frac{V_{O,max}}{V_{dc}} = \frac{\mathrm{M}}{1-\mathrm{D}}. \qquad (3-4)$$

In the modulation of this converter, D is always greater than M. After calculating M and D for the desired output, these values should be the output of the control system to produce PWM Pulses. Having D and M, the four operating states are produced through the modulator.

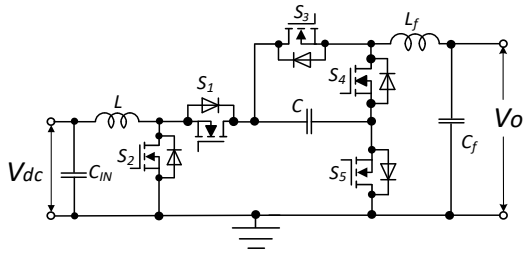


Figure 3.3. Three-level common-ground flying capacitor-based solution to address the leakage current.

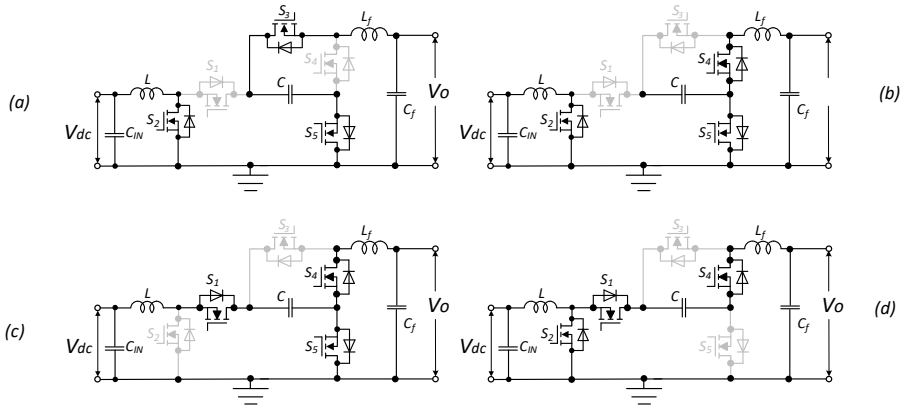


Figure 3.4 Equivalent circuits of the three-level common-ground flying capacitor-based solution. (a) $V_O = +V_C$, (b) $V_O = 0$, (c) $V_O = 0$, (d) $V_O = -V_C$.

The controller of the inverter as shown in Fig. 3.5, includes a Phase-Lock-Loop (PLL) and a Proportional Integral (PI) controller along with a Proportional Resonance (PR) controller are used to produce modulation index (M) and duty cycle (D) required by the inverter. PLL samples grid voltage and provides synchronization to the primary grid. For this PLL, the traditional Second Order Generalized Integrator (SOGI) regulator is used. The grid side reference current (I^*_g) is derived by means of a PI controller using the reference value (V^*_{dc}) and the actual value (V_{dc}) of the dc input voltage. Finally, a conventional PR controller is used for grid current control, producing M and D using the reference ($I^*_g(t)$) and the actual grid current ($I_g(t)$).

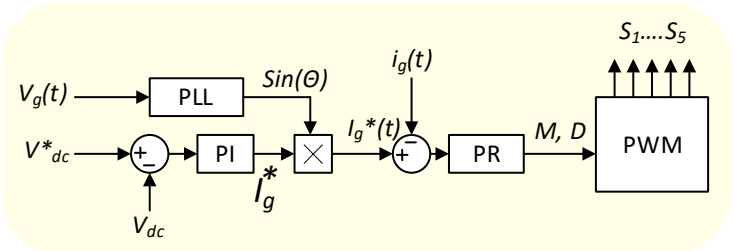


Figure 3.5 The block diagram of the applied control system.

3.2 The proposed five-level fault-tolerant inverter

The proposed fault-tolerant inverter is demonstrated in Fig. 3.6. It comprises of a total of ten power semiconductor switches, an inductor, and two flying capacitors (C_1 & C_2). The proposed topology produces nine-level output voltage waveform across the load terminal with $\pm V_{dc}$, $\pm 2V_{dc}$, and zero voltage levels under healthy conditions.

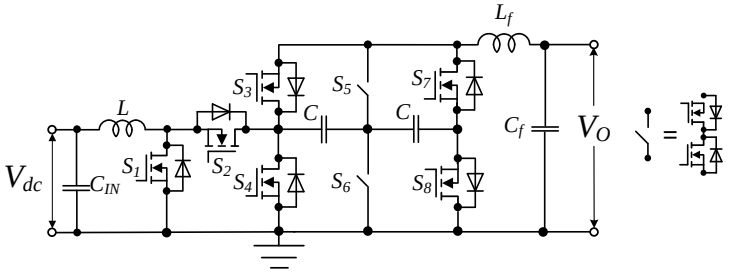


Figure 3.6 The proposed five-level common-ground fault-tolerant inverter.

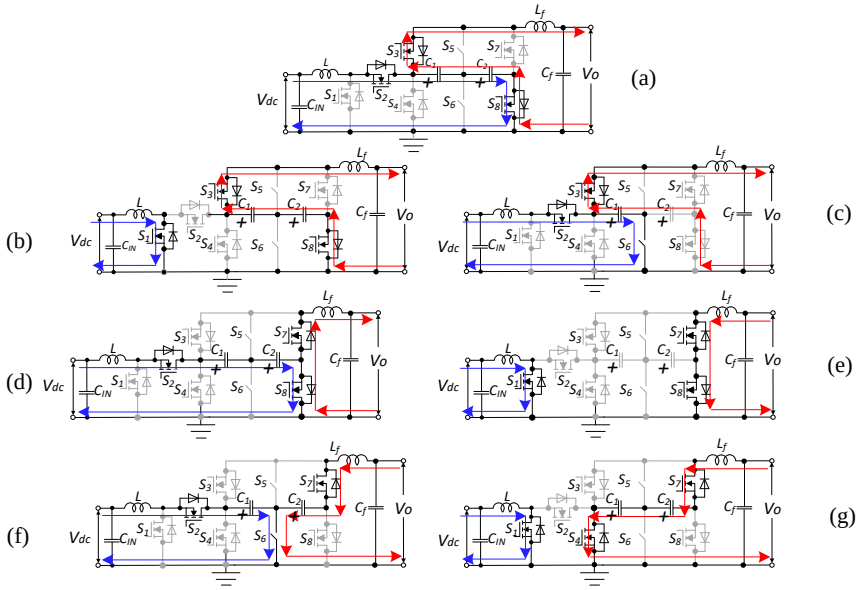


Figure 3.7 Operating states of the proposed fault-tolerant inverter. (a) $V_O = +2V_C$, C_1 & C_2: charging, L: discharging, (b) $V_O = +2V_C$, C_1 & C_2: discharging, L: charging, (c) $V_O = +V_C$, C_1: charging, L: discharging, (d) $V_O = 0$, C_1 & C_2: charging, L: discharging, (e) $V_O = 0$, L: charging, (f) $V_O = -V_C$, C_1: charging, L & C_2: discharging, (g) $V_O = -2V_C$, C_1 & C_2: discharging, L: charging.

There are seven operating states as demonstrated in Fig 3.7. In mode (a) as shown in Fig. 3.7 (a), capacitors C_1 & C_2 are charging while in mode (b) in Fig. 3.7 (b) these capacitors are discharging and, in both modes, the voltage $+2V_C$ is provided in the output. In mode (c), inductor L is transferring its power to the capacitor C through switches S_2 and S_6 to provide the voltage $+V_C$ in output terminals. In modes (d) and (e), zero output voltage is provided by turning on S_7 and S_8 simultaneously. In mode (f), while C_1 is charging, C_2 is discharging in the load and makes the output voltage of $-V_C$. In the last mode in Fig. 3.7 (g), Both capacitors are discharging, and the inductor L is charging and $-2V_C$ is provided in the output.

The fault-tolerant operation of the inverter works such that if any of the three legs of this inverter experiences a fault, or if any of the switches fails, the inverter can be converted into the three-level inverter in Fig. 3.3. Any of the short-circuit faults can be converted to open circuit using fault isolation techniques.

3.3 Comparative analysis

In this section, the aim is to compare the presented inverter in Fig. 3.3 with similar ones in recent literature. These solutions include the unfolding circuit with a buck–boost converter from [40], and the flying inductor power converter in [41], along with the five-level switched capacitor inverter proposed in [42] and the FI-based power converter from [43]. The schematics of these solutions are shown in Figure 3.8. All of these solutions are common ground, except for the buck–boost converter and the unfolding circuit from [40]. While the unfolding circuit can significantly reduce leakage current, it cannot eliminate it entirely.

In the presented inverter, a dual-purpose power converter is introduced. Based on the flying capacitor circuit, it operates as a three-level inverter. A capacitor is used to pump energy into the negative output voltage. On the other hand, the inverter in [42] is based on the switched capacitor circuit and uses two capacitors as voltage sources in the negative half cycle. Despite the fact that virtual voltage sources are used in power converters, their methods of charging capacitors differ. In the presented inverter, the capacitor charges smoothly via a charging inductor, while in [42], the capacitors charge directly from the voltage source at the switching frequency, resulting in spikes in current. In contrast, the unfolding circuit in [40] uses a virtual capacitor that functions as a current source.

Similar to the selected dual-purpose flying inductor converter, the introduced power converters in [41, 43] are based on flying inductor circuits, and the required energy is pumped from the inductors to the output. Among the compared topologies, the switched capacitor power converter in the presented inverter has a fixed double-voltage boosting capability, while other solutions can operate under a wide range of input voltages.

In order to discuss the advantages and disadvantages of each structure, it should be noted that each structure is designed and tested under different conditions; hence, it is not possible to make a fair comparison. However, the fundamental waveforms of a typical converter are independent of the component type and electric parameters (e.g., switching frequency and selected semiconductors). To put it differently, the primary wave forms are produced through the fundamental modulation method, which establishes certain overall requirements for component sizing. These requirements involve estimating passive component values, which can be achieved by considering equal current ripples in the inductors and identical voltage ripples across the capacitors.

In Eqs. (3-5) and (3-6) the maximum accumulated energy inside a capacitor and an inductor are calculated, respectively. According to these equations, the volume of a core of an inductor as well as the volume of a capacitor can be estimated:

The volume of a core of the inductor as well as the volume of the capacitor can be estimated based on its maximum accumulated energy.

$$Vol_C = W_C = \sum_{i=1}^{N_C} C_i {v_{Ci}}^2 , \qquad (3-5)$$

$$Vol_L = W_L = \sum_{i=1}^{N_L} L_i {i_{Li}}^2 , \qquad (3-6)$$

where, L_i and C_i are values of i^{th} inductance and capacitor, N_L is the number of inductors and N_C is the number of capacitors. i_{Li} is the peak inductor current and v_{Ci} is the peak capacitor voltage.

Also, we introduce the relative conduction losses that are independent of the selection of semiconductors. The relative conduction losses are proportional to the square of the switch current. As a result, total conduction losses can be scaled to:

$$P_{CON} = \sum_{i=1}^{N_S} {i_{Si}}^2 . \qquad (3-7)$$

Finally, we can estimate the Total Standing Voltage (TSV) across the semiconductors:

$$TSV = \sum_{i=1}^{N_S} V_{Si} . \qquad (3-8)$$

Based on the above-mentioned points, the same condition is provided for all the selected topologies in PSIM environment under equal condition as the following.

The inductors were selected to have the current ripple equal to 20% of their current ratings. With this assumption, the used charging inductor in [40], are 3.3 mH, the two inductors in the flying inductor power converter in [41] are 1 mH, the inductor in the flying inductor power converter in [43] is 1.1 mH, and the inductor in the selected converter is 1mH.

The capacitors were selected to have the voltage ripple equal to 10% of their voltage ratings. With this assumption, the used capacitor is 10 µF in the flying capacitor based power converter in the presented inverter, is 2 µF in the buck-boost and the unfolding circuit in [40], is 300 µF in the flying inductor based power converter in [41], is 1600 µF for C_1 and 680 uF for C_2 in the switched capacitor based inverter in [42].

The output filter for the selected converter, the flying inductor based converter in [41], the flying inductor based converter in [43], and the buck-boost and the unfolding circuit in [40] is a CL type. The output filter for the flying capacitor based power converter in presented inverter and the switched-capacitor inverter in [42] is a CL type. In all the compared topologies, the output filter capacitor is 3.3 µH. It should be noted that the used capacitor in the unfolding circuit acts as the output filter capacitor and is equal to 2 µF. There is no additional output filter capacitor in this topology. In the selected topology, the inductance of the output filter inductor is 500 µH. It results in 2.53 % THD in the output current. Hence, the output filter inductors are selected to have the same THD. in the output current. Based on this assumption, the output filter inductor is 750 µH for the buck-boost and the unfolding circuit in [40], is 1700 µH for the flying capacitor based power converter in the presented inverter, is 1 µH for the flying inductor based converter in [41], is 700 µH for the flying inductor based converter in [43], is 2000 µH for the switched capacitor based power converter in [42].

The following parameters were considered for all the compared topologies to simulate the same condition: Input voltage (V_{IN}) = 200 V, peak value of the output voltage (V_{out}) = 325 V, switching frequency (f_S) = 25 kHz, average output power (P_{out})= 1 kW.

The on-state resistors of the power switches ($R_{ON,S}$) were considered equal to 0.028 Ω which indicates the internal resistance of NVHL020N120SC1 switch. In contrast, the power switches used in a previous power converter design ([43]) were IGBT power switches without body diodes, which limit the current to flow in only one direction.

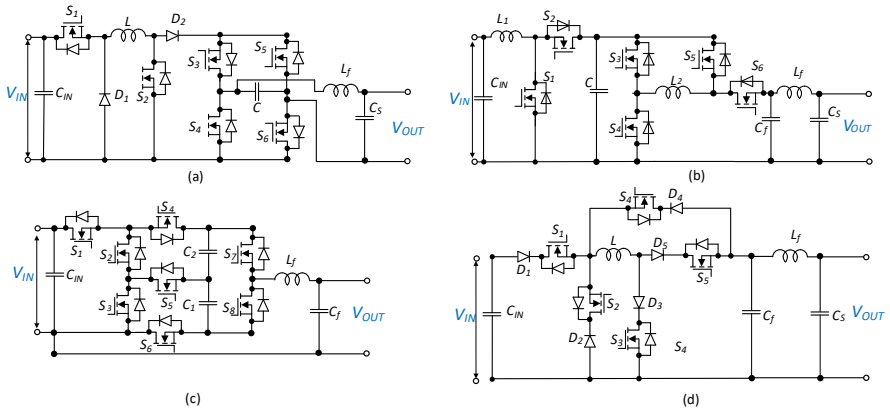


Figure 3.8 Schematics of the compared topologies: (a) buck–boost and the unfolding circuit in [40], (b) flying inductor power converter in [41], (c) switched-capacitor power converter in [42], and (d) flying inductor power converter in [43].

MOSFETs, on the other hand, have bidirectional current flow capability inherently. To account for the unidirectional current flow in the IGBT-based design, a diode was added in series with the power switch in the simulation. For power diodes, the on-state resistance ($R_{ON,D}$) was assumed to be 0.05 Ω, and the forward voltage ($V_{fw,D}$) was assumed to be 0.65 V in the circuit models.

This switch is a N-channel MOSFET power switch with the body diode. In the flying inductor based converter in [43], IGBT power switches without body diodes are used. This causes unidirectional current flowing through the switches, while MOSFETs obtain the inherent bidirectional current flowing capability. Therefore, a diode is connected in series with the power switch in the simulation environment to model the current unidirectional semiconductor for the introduced topology in [43]. The on-state resistors of the power diodes ($R_{ON,D}$) and the forward voltage of power diodes ($V_{fw,D}$) were considered as 0.05 Ω and 0.65 V, respectively for the structures with power diodes.

The comparison between different circuit designs is focused on several key factors, including the accumulated energy of capacitors (WC), the accumulated energy of inductors (WL), the Total Standing Voltage (TSV) of the semiconductors, conduction losses of the semiconductors (PCON), and the number of power switches used (NSW).

Fig. 3.9 presents a radar chart comparing the different circuit topologies based on their calculated parameters shown in per unit values. The inverter introduced in reference [42] uses a switched-capacitor circuit and has the highest capacitor value among the compared designs, resulting in high accumulated energy in the capacitors. However, this topology also has significant conduction losses. Switched-capacitor circuits are susceptible to current spikes that occur when the capacitors are being charged, causing inrush currents to pass through the power switches in the charging path, leading to higher current stress and power losses. As the output power increases, the magnitude of these current spikes becomes higher, potentially damaging the power switches. Therefore, SC-based solutions are not suitable for high-power applications. The flying inductor converter in [43] has the highest value of conduction losses due to power losses across the series-connected power diodes with the power switches. In contrast, the presented inverter, and the buck–boost unfolding circuit in [40] have the lowest accumulated energy in the capacitors. The introduced power converter in [43] use flying

inductor architecture, and the filter capacitor is the only capacitor used in their configuration. The dual-purpose converter in [40] and the presented inverter use a pseudo DC-link approach, which significantly reduces the capacitor size while maintaining good grid current quality. In terms of accumulated energy inside the inductors, the selected dual-purpose power converter stands out among the compared topologies, while the FI-based power converter introduced in [43] ranks highest. Regarding TSV, the introduced flying inductor dual-purpose converter in [41] has the highest voltage stress across its power switches.

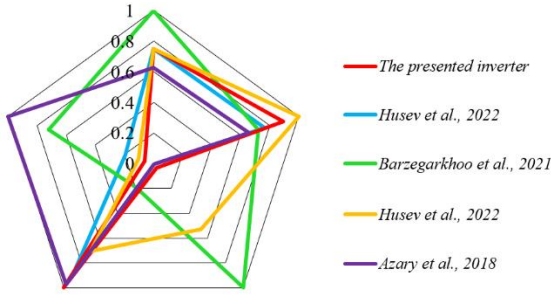


Figure 3.9 Radar chart of the compared topologies.

3.4 Summary

The exploration of various grounding techniques and inverter topologies underscores the critical role of effective leakage current suppression and system safety in power electronic systems, particularly in dc microgrids. Capacitive grounding methods offer simplicity and cost-effectiveness, while high-frequency transformers provide efficient isolation and compactness, albeit with potential EMI concerns. Common-mode chokes offer noise reduction but at the expense of added cost and size. Low-frequency transformers excel in reliability and high-power applications but may pose challenges in space-constrained environments. A common-ground structure emerges as a key strategy to mitigate leakage currents, ensuring stable grounding and minimizing EMI. A common-ground three -level inverter is proposed. A comparative analysis was performed between several common-ground inverters. The comparison methodology was described comprehensively, and the results were shown in the format of a radar chart. It is demonstrated that proposed solution is considered as the best solution among common-ground architectures and is suitable for leakage current suppression in power converters, and in dc system. The presented fault-tolerant inverter continues to work in full power when one of the legs or one of the switches fails. Overall, this section contributes to advancing the understanding of effective grounding techniques and fault-tolerant inverter topologies in dc microgrid systems, paving the way for enhanced efficiency, reliability, and safety in future power electronic applications.

4 Design and analysis of reliable solid-state circuit breakers with increased safety

DC microgrids are becoming increasingly popular due to their high efficiency, universality, and potential application market. However, the reliable protection of these systems still remains a challenge. Circuit breakers as essential components of electrical systems in homes, industrial facilities, and electrical grids ensure the safety of people and electrical equipment. However, fault current interrupting operations in a dc system are significantly more difficult than in an ac system due to the absence of a zero-crossing point in the current as well as the high rate of rise of the fault current. Therefore, the availability of dc circuit breakers becomes crucial, making it a key technology for dc systems.

There are three types of dc circuit breakers: electromechanical, hybrid, and solid-state. Electromechanical breakers do not typically meet the interruption speed requirements for protecting semi-conductor based systems. They also create arcs resulting in the breaker contacts wear out over time, thus increasing the maintenance costs. Using power electronic switches, however, faults can be isolated quickly without creating arcs. As a viable alternative, the hybrid approach combines mechanical and solid-state technologies. Although mechanical disconnectors are employed in these dc circuit breakers, they slow down the current breaking process and increase weight, volume, and investment costs [44]. With the development of power electronic switches in recent years, dc SSCBs have fared much better than mechanical and hybrid circuit breakers due to their high speed and long lifetime. Table 4.1 summarizes the merits and drawbacks of each type of SSCB.

Table 4.1 . Summary of advantages and disadvantages of different circuit breakers [45].

Type		Advantages	Disadvantages
Mechanical circuit breaker		1. Very low power loss 2. Relatively low cost 3. Simple structure	1. Long operating times (30–100 mS) 2. Limited interruption of current capability
Solid-State circuit breaker	Thyristor Based SSCB	1. Automatic tripping for critical fault 2. Lower cost than SSCB with fully controlled switches 3. Reasonable operation speed	1. Fault magnitude needs to be higher for tripping 2. Cannot provide prolonged protection 3. No common ground
	Fully Controlled Switches SSCB	1. Ultra-fast operation (<100 µS) 2. Very long interruption lifetime	1. High power loss 2. Relatively expensive 3. Big size due to heatsink
Hybrid circuit breaker		1. Low power losses 2. No arcing on mechanical contacts 3. Reasonable response time (few mS)	1. Complex technology 2. Current commutation relies on the arc voltage 3. Very expensive

To enhance the fault protection of dc systems, SSCBs have been developed to perform fast protection (<10 µS). However, there are still challenges to address, such as the decoupling of the source and load during operation, the use of switches on the main path, the reliability of MOVs, and the charging of capacitors prior to reclosing. In this section, a soft turn-on auxiliary is first designed to prevent a surge of current due to a capacitance difference between the source and load, and then three bidirectional dc SSCBs are proposed that address the above issues by bypassing the fault current using a third switch. These circuit breakers eliminate the snubber from the power line and do not use the main path switches. These structures also benefit from extra reliability and increased voltage utilization rate of the switches. These features increase both device and human safety.

4.1 Solid-state circuit breaker with soft-reclosing capability

As shown in Fig. 4.1, this topology consists of two MOSFETs back-to-back with an RCD snubber for each MOSFET. As soon as the circuit reaches almost zero current, a mechanical switch turns off the connection between the negative terminals and the input and output terminals. Traditionally, only the positive terminal of a bidirectional SSCB with two switches is disconnected. In addition to increasing safety, the mechanical switch suppresses system disturbances when using more than one SSCB [28].

Fig. 4.1 also represents auxiliary circuitry for the driver of MOSFETs in energy router applications that may encounter voltage differences between the source and load, facilitating the turn-on process. A voltage difference usually occurs between the input and output voltage terminals after the fault is cleared, especially in applications involving energy routers with multiple power sources connected to the dc link. Transient currents can be generated by this voltage difference, which can activate the SSCB. To prevent this, the turn-on process should be as smooth as possible.

An auxiliary circuit for switches is used to resolve the problem mentioned above. As shown in Fig. 4.2(a), it is assumed that there is a voltage difference between V_{dc} and V_O. Considering the gate-source voltage of the MOSFET as shown in Fig. 4.2 (b), an RC circuit is needed for soft turn-on, as demonstrated in Fig. 4.2 (c). By solving the first-order equation of the RC circuit, it is possible to find the gate-source voltage (V_{GS}):

$$V_{GS} = V_K\left(1 - e^{\frac{-t}{RC}}\right), \qquad (4-1)$$

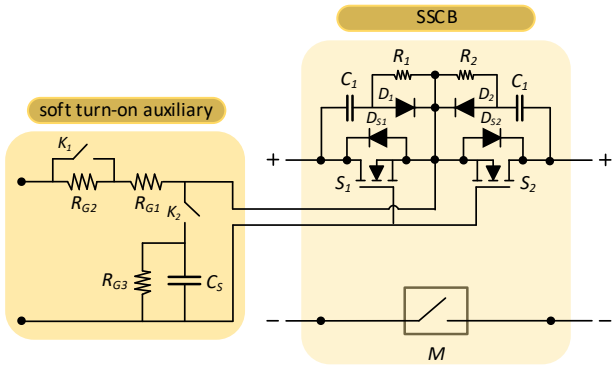


Figure 4.1 Structure of the designed dc SSCB with its soft turn-on auxiliary.

Where, V_K is the voltage of the gate driver. The value of t is the minimum amount of time needed for the circuit voltages to equalize. As a result, it depends on the capacitance of the inputs and outputs and the resistance of the line.

$$t = 5RC. \qquad (4-2)$$

The minimum gate-source voltage (V_{GS}) that can turn on the MOSFET can be obtained by testing a MOSFET or using the datasheet.

The value of *RC* can be calculated by placing V_{GS} and t in Eq. (4-1). For soft turn-on, it seems the easiest solution is to place a capacitor in parallel with the gate-source of the MOSFET and a resistor in series with it. Adding a capacitor, however, will also delay the turn-off process. As a result, it is necessary to place a huge resistor in series with the gate terminal and turn-off resistor R_{G1} and in parallel with a diode so as to not influence the turn-off time (Fig. 4.3(a)). Another structure is to place the diode and resistor in series with each other and in parallel with the turn-off resistor R_{G1} (Fig. 4.3(b)).

However, the aforementioned solution severely affects the gate driver's performance. Therefore, the most complete approach is using the structure in Fig. 4.3(c). In turn-off mode, the mechanical relay K_1 is ON, and relay K_2 is OFF. This means that only the resistor R_{G1} is in the gate auxiliary circuit. On the other hand, in turn-on mode, the state of the relays K_1 and K_2 is reversed and they get OFF and ON respectively which puts the calculated RC in the gate auxiliary circuit. In this circuit, the resistor R_{G3} is in parallel with capacitor to discharge the capacitor for the next turn-on.

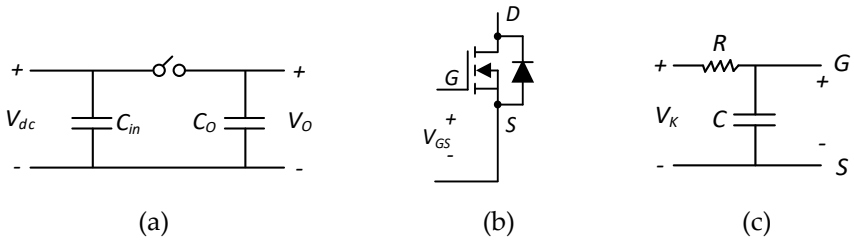


Figure 4.2 Circuits for calculation of the optimized values of R and C: (a) The system with its capacitors of input and output, (b) The gate-source voltage of MOSFET, (c) The auxiliary circuit for the gate of the MOSFET.

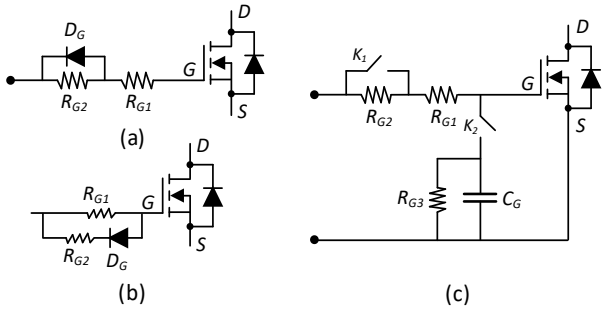


Figure 4.3 The MOSFET and its possible auxiliary circuits: (a) Series approach, (b) Parallel approach, (c) The main and complete approach.

4.2 Solid-state circuit breakers with enhanced safety

The schematics of the proposed SSCBs are shown in Fig. 4.4. These topologies are named according to their shapes like alphabetical letters. Therefore, they are named T-SSCB (Fig. 4.4(a)), Y-SSCB (Fig. 4.4(b)), and H-SSCB Fig. 4.4(c). All three circuits consist of three switches. In addition, T-SSCB is composed of 2 diodes and an RC+MOV snubber, Y-SSCB is composed of 4 diodes and an RC+MOV snubber and Y-SSCB is composed of 4 diodes and two RC+MOV snubbers.

The operating modes of the designed SSCBs are shown in Fig. 4.5. In normal operation, the current flows through both MOSFETs as shown in Figs. 4(a, c, and e). When the short-circuit fault occurs, the third MOSFET S_3 turns on. After a safe delay, the MOSFETs S_1 and S_2 turn off. Therefore, the current of the line inductor is bypassed through the switch S_3 and the snubber as shown in Figs. 4.5(b, d, and f). It should be noted that in T-SSCB, the switches S_1 and S_2 are connected in a different direction from the other two topologies. The MOSFET S_1 is permanently turned off, and the current flows through its diode. It is turned ON when the system works in backward mode.

The proposed SSCBs address the problems of traditional SSCBs making the following contributions:

- Complete decoupling of the primary side with the load side during the interruption ensures the faulty section is quickly and effectively isolated from the fault current to increase safety, reliability and of the load.
- The snubber is removed from the power line, therefore, the MOV's reliability is increased.
- Voltage utilization rate of the switches is increased by 20 %, therefore maximum allowable dc bus voltage on the SSCB is extended.
- Not using switches of the main path which increase reliability.
- Complete and fast discharging of the snubber capacitor before reclosing.
- The SSCB adds the benefits by only adding two diodes and one MOSFET with a low maximum voltage.

The three proposed SSCBs have modularity capabilities that allow them to be easily extended to suit different dc system requirements. The Y-SSCB and H-SSCB, however, would be more suitable for modularization since in T-SSCB, half of the switches are turned ON, decreasing their reliability.

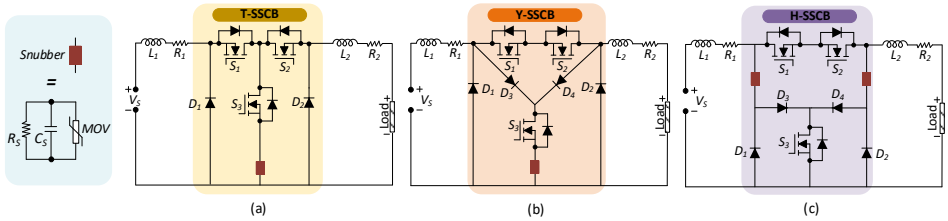


Figure 4.4 The schematics of the proposed SSCBs: (a) T-SSCB (b) Y-SSCB (c) H-SSCB.

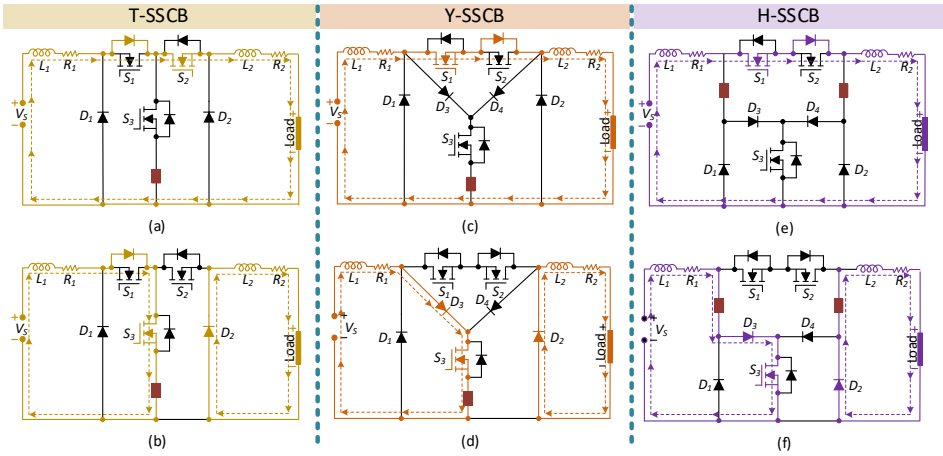


Figure 4.5 Operating modes of the proposed SSCBs: (a) normal operation of T-SSCB, (b) short-circuit operation of T-SSCB, (c) normal operation of Y-SSCB, (d) short-circuit operation of Y-SSCB, (e) normal operation of H-SSCB, (f) short-circuit operation of H-SSCB.

Circuit breakers with high efficiency demonstrate decreased power losses and require less cooling during consistent operating states. One solution to achieve high efficiency in SSCBs is to connect multiple solid-state switches in parallel. This method helps improve overall efficiency by lowering the input switch's equivalent on-state resistance. In accordance with the design parameters of the prototype, the efficiency of the proposed circuit breakers is 99.91 calculated by Eq. (4-3).

$$\mu_{SSCB} = \left(1 - \frac{R_{ds(on)} \cdot I_{dc}}{\mu_V \cdot V_{dc}}\right) \cdot 100\%. \qquad (4-3)$$

As shown in Fig. 4.6, the efficiency of the SSCBs decreases as the nominal current or the on-state resistance of the switches increase. $V_{dc} = 350$ V is used as a reference voltage for the efficiency calculation. When applied in high voltage, the efficiency increases significantly since it is directly proportional to the voltage.

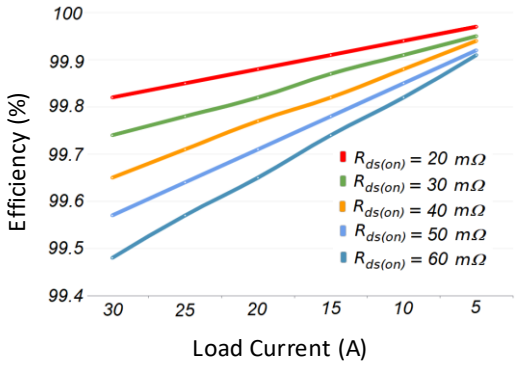


Figure 4.6 The efficiency of the proposed SSCBs for different on-state resistances and currents.

Since solid-state switches are not restricted in terms of their on/off cycles, the lifespan of the breakers is primarily determined by their topology and their operation during the fault isolation procedure. During the isolation process of the proposed SSCBs, no current passes through the switches of the main path which increases their lifetime and reliability reducing their thermal and electrical stress [4].

Since dc systems have low inertia and short circuit fault currents rise rapidly, SSCBs must react quickly to abnormal currents. There are two time intervals included in the response time of an SSCB: detection time and reaction time. The reaction interval is defined as the time between when the fault is detected and when the line current in the system starts to decay.

The proposed SSCBs benefit from high reliability and increased voltage utilization rate of switches of the main path. In most SSCBs with a MOV in parallel with the switches, the voltage of the MOV is equal to the input voltage when the switch is off. As a result, reliability problems arise due to MOV degradation. MOVs suffer degradation as surge currents increase in number and duration, increasing leakage current and decreasing time to failure. Additionally, higher temperatures directly influence the leakage current in MOVs, making it proportional to temperature. MOVs that experience thermal runaway, exceeding their capability, eventually fail due to short circuits [46].

To solve MOV degradation in SSCBs, [47] suggests that V_{dc} should be 20 percent less than the maximum allowable dc voltage on MOV in a steady state. Nevertheless, it gives rise to dimensioning challenges and, more importantly, decreases the main thyristor's voltage utilization rate (μ_V) of the switch which is defined as the following equation.

$$\mu_V = \frac{V_{dc}}{V_{rating,Switch}}.100\%. \qquad (4-4)$$

In the proposed SSCBs, because of the absence of the MOV in the power line, the maximum allowable dc bus voltage on SSCBs and the voltage utilization rate of switches is increased to at least 20%, resulting in improved efficiency due to Eq. (4-3).

Additionally, it increases power density by extending V_{dc} and reducing the number of series-connected switches in MVDC and HVDC applications, as well as enhancing compactness by decreasing cooling systems because it uses lower switches [48].

4.2.1 Operating Zones

Fig. 4.7 presents the electrical waveforms of the proposed SSCBs. There are 10 zones determined by the crucial moments of the interruption process. These zones are discussed independently, and the equations of the currents and voltages are given along with the calculations of time intervals.

Zone I (Before t_0): The first zone includes the normal mode when the switches S_1 and S_2 are turned ON. The current flows from the dc source through the circuit breaker to feed the load as shown in Figs. 4.5 (a, c, and e). As shown in Fig. 4.7, during this interval, the voltages of the capacitor(s) and the main switches are zero and the voltage of the third switch equals the dc voltage. The input side current i_{L1} and the output side current i_{L2} are equal to the nominal value I_N:

$$i_{L1} = i_{L2} = I_N = \frac{V_{dc}}{R_{Load}}. \qquad (4-5)$$

Zone II ($t_0 - t_1$): At t_0 short-circuit fault occurs at the output terminals of the system which makes the current of the circuit increase dramatically making the inductors appear

in the voltage loop as following equation:

$$(L_1{+}L_2)\frac{di_L}{dt} - V_{dc} = 0. \quad (4-6)$$

By solving the above first-order differential equation with initial values: $i_{L1}(t=0) = I_N$, the current is calculated as follows:

$$i_{L1} = i_{L2} = \frac{V_{dc}t}{L_1{+}L_2} + I_N. \quad (4-7)$$

The current at which the fault must be detected is set to I_{limit} in the microcontroller. At t_1 the fault is detected and by approximating the current during T_{0-1} to be linear, the interval $T_{0-1}$is calculated:

$$T_{0-1} = \frac{(L_1{+}L_2)(I_{Limit} - I_N)}{V_{dc}}. \quad (4-8)$$

Zone III ($t_1 - t_2$): Due to the delay of the microcontroller and current sensor, the SSCB acts at t_2 instead of t_1. By considering T_D as the delay time and assuming $t_0 = 0$, the SSCB's action time T_{0-2} is calculated as follows:

$$t_2 = T_{0-2} = T_{0-1} + T_D. \quad (4-9)$$

By calculating T_D and consequently T_{0-2} by Eq. (4-9), the maximum current of the switches is obtained by Eq. (4-7) as follows:

$$I_P = \frac{V_{dc}T_{0-2}}{L_1{+}L_2} + I_N. \quad (4-10)$$

Zone IV ($t_2 - t_3$): A safe delay T_S is considered in the control program to prevent S_1 and S_2 from turn-off before turning ON S_3, since the high voltage resulting from the inductor's decreasing current will burn the switch(s).

$$t_3 = t_2 + T_S. \quad (4-11)$$

Because of the delay T_S, there is a difference between the maximum currents of the input and the output side. However, since it is negligible, we consider this approximation:

$$I_P = i_{L1max} \approx i_{L2max}. \quad (4-12)$$

Zone V ($t_3 - t_4$) (at input side): S_1 and S_2 turn OFF (For T-SSCB, S_1 is already turned OFF) and the current of the input inductor commutates to S_3 and the snubber. This current charges the snubber capacitor till its voltage reaches the clamping voltage of MOV, V_{Clamp}. During this interval, the following equations can be derived:

$$L\frac{di_{L1}}{dt} + +R_1 i_{L1} + v_C - V_{dc} = 0. \quad (4-13)$$

$$i_{L1} = C\frac{dv_C}{dt} + \frac{v_C}{R_S}. \quad (4-14)$$

A portion of the inductor's current flows through the snubber resistor, however, its value (v_C/R_S) is negligible in comparison with the current of the snubber capacitor (Cdv_C/dt). By considering this assumption and the initial values $i_L(0) = I_P$ and $v_C(0) = 0$, the voltage of the capacitor can be obtained:

$$v_C = e^{-\alpha t}\left(\left(\frac{I_P}{C_S} + \alpha V_{dc}\right)\frac{\sin(\omega_d t)}{\omega_d} - V_{dc}\cos(\omega_d t)\right) + V_{dc} \quad (4-15)$$

Where, α, ω_0 and ω_d are defined as follows:

$$\alpha = \frac{R_1}{2L_1}, \omega_0 = \frac{1}{\sqrt{L_1 C_S}}, \omega_d = \sqrt{\alpha^2 - {\omega_0}^2}. \quad (4-16)$$

The interval T_{3-4} can be calculated by placing $v_C = V_{clamp}$ and an approximation by considering t→0:

$$T_{3-4} \approx \frac{V_{clamp} C_S}{I_P}. \quad (4-17)$$

Therefore, the time that the input side current reaches zero is obtained as follows:

$$t_4 = t_3 + T_{3-4}. \quad (4-18)$$

Zone VI ($t_4 - t_6$) (at input side): The current commutates to MOV at t_4. By approximating the current in this interval to be linear, the input current is calculated as follows:

$$i_{L1} = I_P - \frac{V_{Clamp} - V_{dc}}{L_1} t. \quad (4-19)$$

By considering $i_1 = 0$, the time interval T_{4-6} and consequently t_6 are calculated:

$$T_{4-6} = \frac{L_1 I_P}{V_{Clamp} - V_{dc}}. \quad (4-20)$$

$$t_6 = t_4 + T_{4-6}. \quad (4-21)$$

Zone VII ($t_3 - t_5$) (at output side): At the output side, the current of the output inductor flows through the diode D_2 to reach zero at t_5. Considering the initial value $i_{L2}(0) = I_P$, for T-SSCB and Y-SSCB, we have:

$$L_2 \frac{di_{L2}}{dt} + R_2 i_{L2} = 0. \quad (1-22)$$

Therefore, the current of the output side inductor can be obtained as follows:

$$i_{L2} = e^{-\frac{R_2 t}{L_2}} I_P. \quad (4-23)$$

The time that the output current reaches zero is obtained:

$$T_{3-5} = 5\zeta. \quad (4-24)$$

Where $\zeta = \frac{L}{R}$.

In the case of H-SSCB:

$$L_2 \frac{di_{L2}}{dt} + R_2 i_{L2} + v_C = 0. \quad (4-25)$$

$$i_{L2} = C \frac{dv_C}{dt} + \frac{v_C}{R_S}. \quad (4-26)$$

Therefore, the current of the load sideline inductor can be obtained by:

$$i_{L2} = -\alpha e^{-\alpha t} \left(\frac{I_P}{C_S} + \alpha V_{dc}\right) \frac{\sin(\omega_d t)}{\omega_d} + e^{-\alpha t} \left(\frac{I_P}{C_S} + \alpha V_{dc}\right) \cos(\omega_d t). \quad (4-27)$$

By considering i_{L2} =0 and an approximation by considering t→0, the time when the output current reaches zero (T_{3-5}) and consequently t_5 is obtained as follows:

$$T_{3-5} \approx \frac{2L}{R_2}. \quad (4-28)$$

$$t_5 = t_3 + T_{3-5}. \quad (4-29)$$

Zone VIII ($t_6 - t_7$): At t_6, when the current of the input side reaches zero, the voltage on the capacitor equals the input dc voltage as well as the voltage on the switch S_1 (the switch S_2 for T-SSCB).

When both currents of the input side and the output side reach zero, the switch S_3 turns OFF after a safe delay $T_Z = T_{6-7}$.

Zone VII ($t_7 - t_8$): At t_7, S_3 turns OFF and the snubber capacitor starts discharging. As the voltage of the capacitor decays to zero, the voltage of the switch S_3 increases to reach V_{dc}. This is because the resistance value across S_3 at the OFF state (Mega range) is much higher than the resistance value of R_S (KΩ range). During this interval, the voltage of the

capacitor which has been charged to V_{dc}, discharges to R_S during T_{7-8}:

$$T_{7-8} = R_S C_S. \quad (4-30)$$

Zone IX ($After\ t_8$): At t_8, all components and their voltage and current waveforms return to their normal state before the fault and the interruption is completed, and the converter is ready to restart.

$$t_8 = T_{7-8} + t_Z. \quad (4-31)$$

4.2.2 Design Procedure

Table 4.2 summarizes the dependency of each time interval to the value of different parameters of the topologies.

The proper values of snubber capacitance and MOV highly affect the performance of SSCB along with time intervals. Therefore, their appropriate design is of high importance.

Snubber Capacitor, C_S: Considering $v_C(t_4) = V_{clamp}$ in Eq. (4-15), we have:

$$V_{Clamp} = e^{-\alpha T_{3-4}}\left(\left(\frac{I_P}{C_S} + \alpha V_{dc}\right)\frac{\sin(\omega_d T_{3-4})}{\omega_d} - V_{dc}\cos(\omega_d T_{3-4})\right) + V_{dc}. \quad (4-32)$$

By considering t→0, the following approximations can be made to simplify the complex equation:

$e^{-\alpha T_{3-4}} \approx 1$, $\frac{I_p}{C_S} \gg \alpha V_{dc}$, $\sin(\omega_d T_{3-4}) \approx \omega_d T_{3-4}$, $\mathrm{Cos}(\omega_d T_{3-4}) \approx 1$.

Doing so, the value of the snubber capacitor can be derived from Eq. (4-32):

$$C_S \approx \frac{T_{3-4} I_P}{V_{clamp}}. \quad (4-33)$$

By replacing I_P with Eq. (4-10) we obtain the following statement:

$$C_S \approx \frac{T_{3-4}}{V_{clamp}}\left(\frac{T_{0-2} V_{dc}}{L_1 + L_2} + I_N\right). \quad (4-34)$$

Since T_{0-2} has a large dependency on the speed of the microcontroller and the current sensor, $L_1 + L_2$ are line parameters, V_{dc} and I_N are constant and predefined, and also V_{clamp} has its own limit, C_S can be optimized mainly by T_{3-4}.

Snubber Varistor, MOV: The desired MOV can be selected considering three parameters including V_{clamp}, E_r, and I_{Surge}.

The maximum clamp dc voltage V_{clamp} for T-SSCB and Y-SSCB must be 10% lower than the maximum surge voltage of the switches.

$$V_{clamp} < 1.1 V_{S,max}. \quad (4-35)$$

For H-SSCB:

$$V_{clamp} < 2.2 V_{S,max}. \quad (4-36)$$

On the other hand, it also must be 10% higher than $V_{dc,}$;

$$V_{clamp} > 1.1 V_{dc}. \quad (4-37)$$

The maximum surge current must be less than the current of the input side inductor at t_4. Hence, according to (14),

$$I_{Surge} < I_P - \frac{V_{MOV} - V_{dc}}{L_1} t_4. \quad (4-38)$$

The surge energy on the MOV during T_{4-6} can be calculated as follows using the derived i_{L1} from Eq. (4-19):

$$E_{surge} = \int_{t_4}^{t_6} V_{MOV} i_{L1} dt \approx$$

$$\int_{t_4}^{t_6} (\frac{V_{dc} - V_{Clamp}}{\mathrm{t}} + V_{Clamp})(I_P - \frac{V_{Clamp} - V_{dc}}{L_1} t)\,. \qquad (4-39)$$

The obtained result is the minimum value of surge energy of the MOV:

$$E_{MOV} > E_{surge}. \qquad (4-40)$$

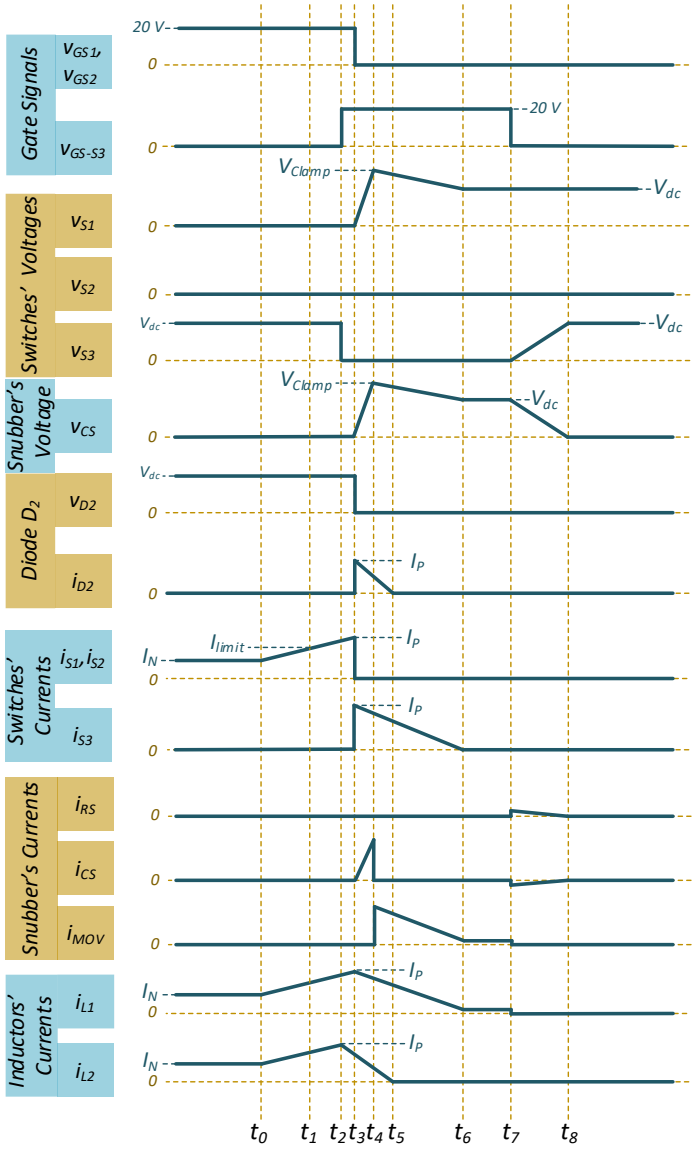


Figure 4.7 Electrical waveforms of the proposed SSCBs.

Table 4.2 . Dependency of Time Intervals to The Value of Different Parameters of The Circuit (▲direct relation, ▼inverse relation)

Time Interval	Key Dependencies
T_{0-1}	L_1 ▲ L_2 ▲, I_{Limit} ▲
T_{1-2} (T_D)	The delay of the microcontroller and ▲ The delay of the current sensor ▲
T_{2-3} (T_S)	Chosen by us
T_{3-4}	C_S ▲,V_{clamp}, ▲ I_P ▼
T_{4-6}	L_1 ▲, I_P ▲, V_{MOV} ▼
T_{3-5}	L_2 ▲, R_2 ▼
T_{6-7} (T_Z)	Chosen by us
T_{7-8}	R_S ▲, C_S ▲

4.3 Experimental Results

4.3.1 Experimental results of SSCBs with soft-reclosing capability

Fig. 4.8 shows the schematic of the circuits used for the experiment along with the prototype. In the first experiment (Fig. 4.8(a)), the short-circuit is created using a mechanical relay K across the load. Fig. 4.8(c) shows the prototype of the laboratory prototype and test operation of the designed SSCB. The voltage of the dc source is 240 V with a 30 A limit for the circuit's current. The result is shown in Fig. 4.9. The SSCB breaks the circuit after 16µS when the current reaches 100 A and the voltage of the switch S_1 reaches 420 V. As discussed before there is a time delay that depends on the current sensor and the speed of the microcontroller programming. The delay time of the current sensor used in this prototype is 14 µS and the delay of the programming equals the sampling period which is 5 µS. These delays do not sum up since they occur simultaneously. This time delay can be reduced using a current sensor with a larger bandwidth.

However, after reducing it to the sampling period, to further decrease the delay, the sampling frequency should be increased. However, as discussed in the previous section it raises the peak voltage of the switch during fault-clearing operation so there should be a lower limit for the delay according to the components' capability.

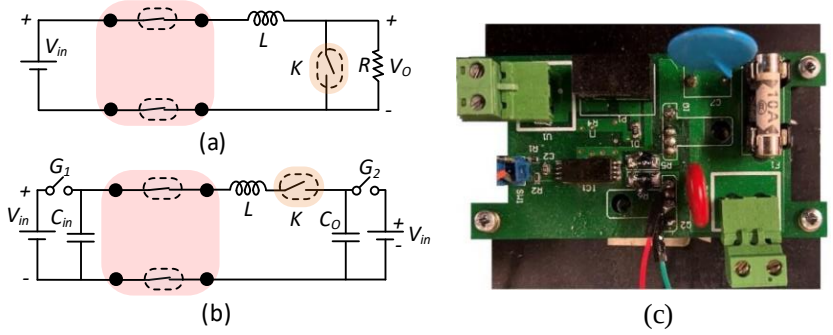


Figure 4.8 Experimental results of the soft turn-on test: V_{dc} =400 V, V_{out} =350 V.

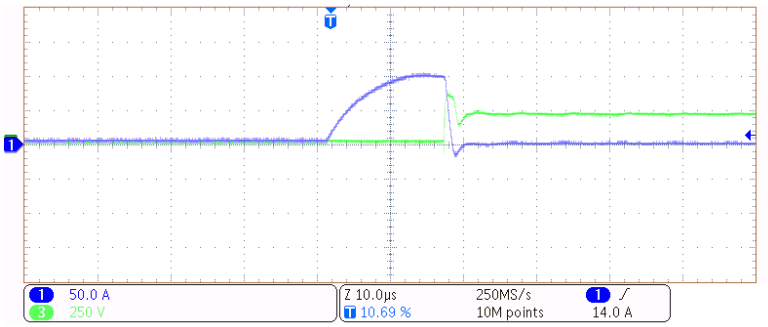


Figure 4.9 Experimental results of the short-circuit test: V_{in} =240 V, I_{limit} =30 A.

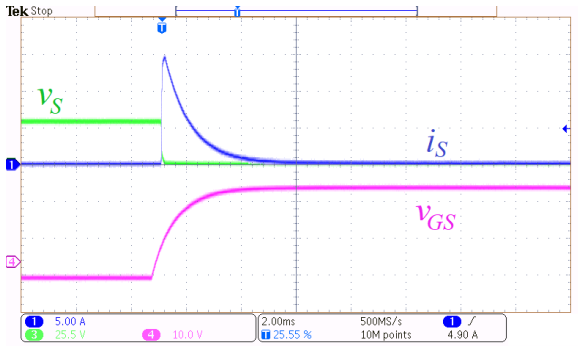


Figure 4.10 Experimental results of the soft turn-on test: V_{dc} =401 V, V_{out} =350 V.

In the second test as shown in Fig. 4.8(b), the main path of the circuit is connected through a mechanical switch. The capacitors are charged to different voltages by turning on the switches G_1 and G_2 temporarily. Then, by disconnecting these switches and connecting switch K, there will be a huge current spike because of the input and output capacitors' voltage difference dropped on the small resistance of the circuit.

As shown in Fig. 4.10, there is a 50 V voltage difference between the input and output capacitors which by the benefit of using a 10 kΩ resistor and a 100 nF capacitor as mentioned before, the peak of the surge current is limited to is 25 A which is very desirable.

4.3.2 Experimental results of SSCBs with increased safety

Fig. 4.11(a) shows the schematic of the test circuit of the prototypes and the laboratory prototype of the designed SSCBs is presented in Fig. 4.11(b). In this test, the short-circuit is created using a mechanical relay K across the load. Two inductors are placed in the input and output terminal of the SSCB as line inductors with values 10µH and 20µH, respectively. The input dc voltage is 500 V, and the output resistor is 50 Ω as the load. The complete list of the design parameters is presented in Table 4.3.

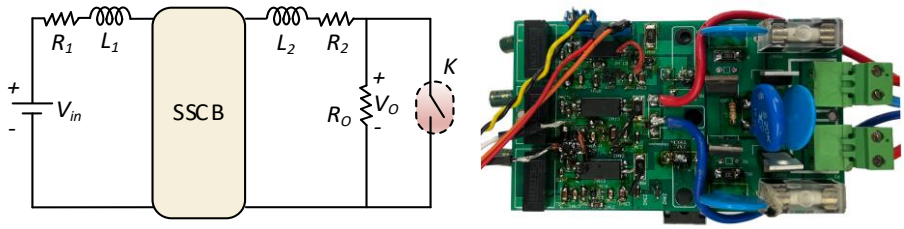


Figure 4.11 (a)Schematic of the test circuit. (b) The prototype of the SSCB.

Table 4.3. Design parameters of the proposed SSCBs.

Parameter	Acronym	Value
Rated Power	P	12.5 kW
Input Voltage	V_{in}	500 V
Nominal current	i_N	25 A
MOSFETs	S_1, S_2, S_3	UF3SC120016K4S
Diodes	D_1, D_2, D_3, D_4	APT30DQ120KG
Snubber Resistor	R_S	3KΩ
Snubber Capacitor	C_S	500nF, 2kV
Snubber MOV	MOV	V_{dc} =505 V, V_{Clamp}: 1000 V
Input side Inductor	L_{Line}	10 µH
Output side Inductor	L_{Out}	20 µH
Load Resistor	R_{Load}	50 Ω
Input side Resistor	R_1	1.5 Ω
Output side Resistor	R_2	1.5 Ω

The input voltage is 500 V, and the nominal current is 25 A. Using a 505 V MOV with clamping voltage of 1000 V, the overvoltage on the switches is 950 as shown in Fig. 4.12(a). Fig. 4.12(b) shows the output side current that reaches its peak at 180 A and decays to zero in 21 µS. The voltage experiences an oscillation when the third switch turns off. This oscillation depends on the safe delay T_S. As shown in Figs. 4.12(c) and 4.12(e), the peak short circuit current in this test in the input side is 195 A while the limit current to be detected is set to 100 A. The overcurrent is detected and reacts in 9 µS. After the detection and reaction, the current reaches 180 A. Following this, the switch S_3 turns on which makes a short circuit across the input side and bypasses the short circuit current into the third leg. To protect the switches, the switch S_2 is turned off after a short time interval T_S which is considered 1 µS here. During this 1 µS, the short current passes through a closer path to the source and sees a lower resistance, therefore the current increases with a sharper pace until it reaches its peak when the input current starts to plummet. In T-SSCB, the maximum voltage peak voltage of the snubber capacitor and therefore the switch S_2 equals the maximum clamping voltage of MOV. It takes 47 µS for i_{L2} and 24 µS for i_{L1} to reach zero. When the input current i_{L1} reaches the MOV's leakage value, after a safe interval of 5 µS the switch S_3 turns off to completely make it zero.

In Y-SSCB, the input current passes through the diode D_3. Also, unlike T-SSCB, the source pins of the switches are connected instead of the drains that places the voltage stress on the switch S_1. The results in this case are similar to T-SSCB, however, the current

does not pass through any of the power line switches.

H-SSCB has an extra snubber in series with its output side diode making it benefit from faster fault clearance in the load side which is about 5 µS in this test (Fig. 4.12(c)). However, since there is a reverse voltage on the output side snubber capacitor, the voltage of the drain pin of MOSFET S_2 is $-V_{Clamp}$. Therefore, the voltage across the switch S_1 will be $2V_{Clamp}$. This structure is suitable in applications where fast fault clearance is needed on both sides and where cost is not a priority and switches with higher voltage can be used.

Figs. 4.12(d) and 4.12(e) show the current of the capacitor rising at the time of breaking operation and commutating to MOV when the voltage of the switch S2 reaches near the clamping voltage.

The 9 µS reaction time depends on the speed of the microcontroller's program along with the delay of the current sensor. The current implemented current sensor is ACS720KLATR-15AB-T, which has an 8 µS delay. By using a high bandwidth current sensor, the detection time can be decreased considerably.

Fig. 4.13 compares the voltage of the snubber capacitor in the steady state in the proposed SSCB and a typical conventional SSCB in Fig. 4.1. Unlike the traditional approach, the capacitor in the proposed SSCB is discharged before reclosing. According to Eq. (4-30), the discharging time depends on the value of the snubber resistor.

By analyzing the voltage of the switches in the proposed SSCB and the conventional one in Fig. 4.14, it is seen that using the same MOV, using a higher dc input voltage is possible in the proposed SSCBs and in general in the SSCBs in which MOV is removed from the power line. In traditional SSCBs with MOV in their power line, the input voltage must be at least 20% higher than MOV's voltage to avoid leakage currents.

It is illustrated from the experimental results that the proposed SSCBs can work properly in different voltage levels below the clamping voltage of the MOV with a safe margin which is attractive for industrial applications.

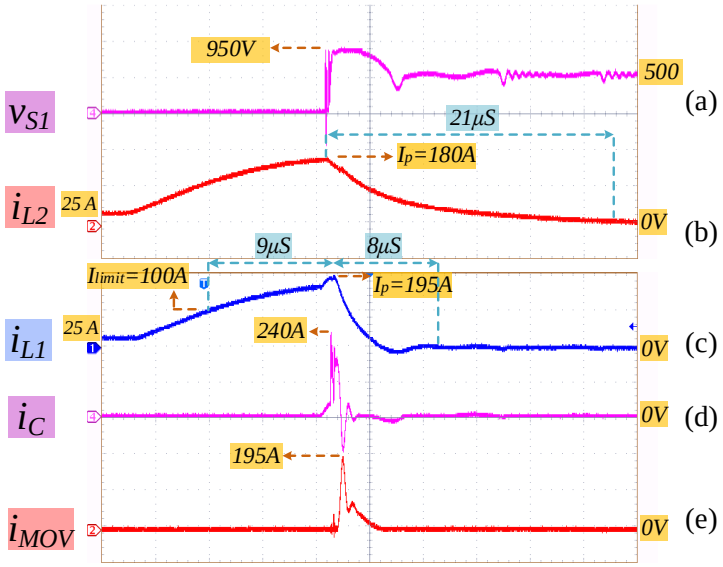


Figure 4.12 The electrical waveforms of Y-SSCB.

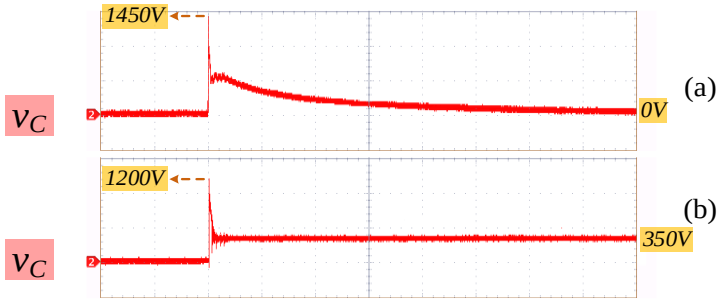


Figure 4.13 The voltage of snubber capacitor in: (a) Proposed SSCBs, (b) Conventional SSCB in Fig. 4.1.

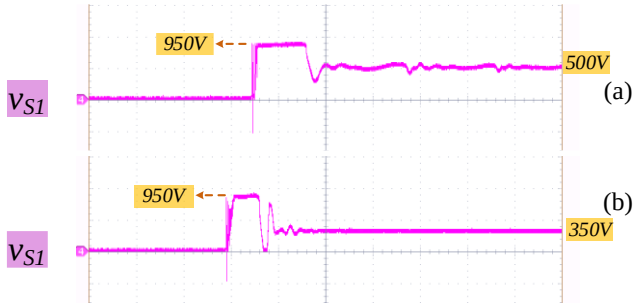


Figure 4.14 The overshot voltage on the switches: (a) Proposed SSCBs, (b) Conventional SSCB in Fig. 4.1.

4.4 Summary

The development and analysis of reliable Solid-State Circuit Breakers (SSCBs) for dc microgrids offer significant advancements in fault protection and safety. The proposed SSCBs, featuring a soft turn-on auxiliary circuit, address key challenges such as decoupling the source and load, enhancing MOV reliability, and managing charged capacitors during reclosing. Three innovative SSCB topologies (T-SSCB, Y-SSCB, and H-SSCB) are designed with a third switch to bypass fault currents, eliminating snubbers from power lines and increasing voltage utilization rates. These designs improve reliability, efficiency, and safety while reducing component count and costs. The optimized auxiliary circuit ensures soft turn-on, preventing high current surges and voltage overshoots, thus extending the lifespan and reliability of the circuit breakers. The experimental results validate the effectiveness of these SSCBs, demonstrating their potential for increased safety and efficiency in dc microgrids.

The findings of this section support the first hypothesis, which states that advanced solid-state circuit breakers provide completely safe operation of the energy router in case of a fault.

5 Energy router for residential applications

The integration of renewable energy sources in buildings and smart houses is pivotal for advancing sustainable living and combating climate change. In addition, the reduction of cost of renewable energy sources has opened new opportunity for the consumers to produce their own electricity [49]. In smart houses, energy routers play a critical role by optimizing the distribution and usage of renewable energy, enhancing energy efficiency, and ensuring that power is utilized where and when it is needed most. This intelligent energy management not only lowers utility costs for homeowners but also contributes to a more resilient and eco-friendly energy grid, making it key for future urban planning and protecting the environment.

The designed energy router is an intelligent power electronic equipment that enables using both ac and dc in residential buildings. It manages the energy transfer between photovoltaic dc sources, energy storage systems, three-phase ac sources, dc, and ac loads [50]. The device also typically includes advanced power management function to ensure stable and reliable energy distribution. Additionally, the power electronic energy router includes communication capabilities for remote monitoring and control, as well as a built-in protection mechanism to safeguard against electrical faults or overloads.

The smart energy router harnesses the power of a three-phase ac source for enhanced stability and avoids overloading, ensuring the longevity of electrical components. It efficiently distributes energy across single-phase structures and intelligently chooses the optimal phase based on time and consumption patterns and maximizes efficiency by aligning energy distribution with demand. It also results in a considerable reduction of the primary cost of the PV and battery systems.

In this chapter, after the description of the energy router's topology along with its power management structure, the Printed Board Circuit (PCB) design considerations of the prototype are explained. The energy router consists of a three-level inverter and two dc-dc converters which are described with experimental results.

5.1 Topology description

The structure of this energy router consists of a bidirectional single-phase inverter to act as interface between the ac grid and the dc link. It also includes a dc-dc converter to use dc power provided by PV panels on the house's rooftops. To store the dc power at moments when PV panels cannot provide enough power, a battery is used by connecting an unfolding dc converter to the dc link.

A standout feature of this energy router lies in its common-grounded structure, meticulously designed to suppress leakage currents, and elevate safety standards. Within this framework, the novel solid-state circuit breaker in this structure exhibits the ability to isolate both the source and load sides entirely. This remarkable characteristic not only enhances device safety but also prioritizes human safety. The PCB layout of the energy router is implemented with high level EMC design.

The contributions of the designed energy router structure are:

- Selection of state-of-the-art power electronic converters and circuit breaker to ensure optimal and reliable performance.
- Merging of conventional smart house functions along with intelligent energy control.

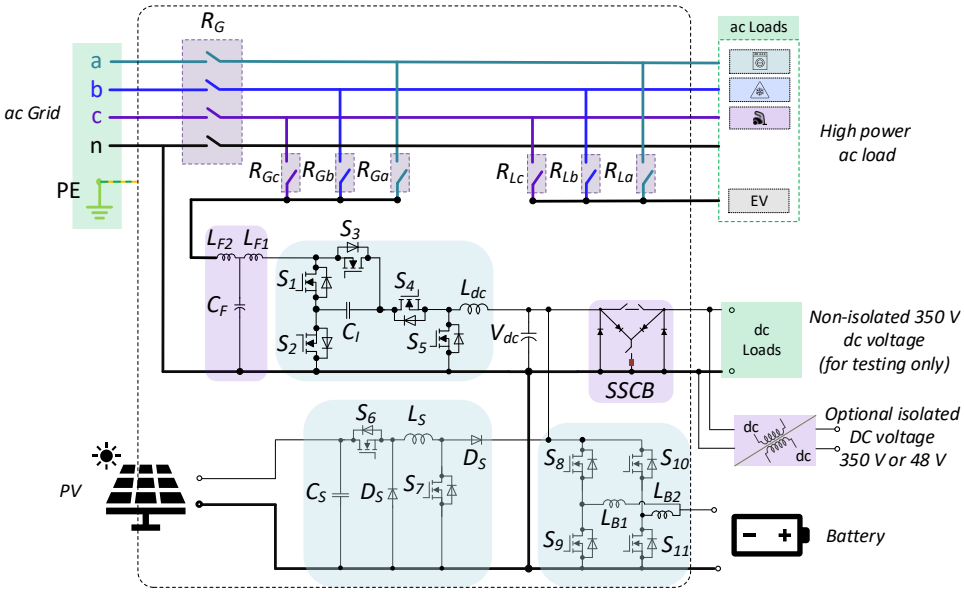


Figure 5.1 Schematic of the energy router.

- Common-grounded structure which eliminates the leakage current and increases the safety.
- High efficiency for dc sources and loads.
- Enhanced Protection functions including a novel SSCB with enhanced safety.
- High scalability for grid extension.
- Active and reactive power control for ac grid.

5.2 Power management structure

The ac port of the energy router features three phases, each intricately connected to an ac load within the house through a dedicated relay for every phase. Within this system, three ac loads operate simultaneously, and at any given moment, the Electric Vehicle (EV) charger port is selectively linked to the ac load with the least power consumption.

To elaborate, each ac load is linked to the ac side of the inverter through a relay. However, only one ac load is actively connected to the inverter at any specific moment, the one exhibiting the highest power consumption among the three ac loads. This entails a dynamic system where the ac load with the highest power demand is supplied by the dc sources through the inverter, facilitated by activating the corresponding relay.

Concurrently, the two remaining ac loads, which exhibit lower power consumption, are supplied by the ac grid. This is achieved by activating the relays corresponding to the respective phases of the ac grid. This intricate arrangement optimizes energy distribution within the household, considering that all three ac loads typically do not operate at their maximum power capacity simultaneously.

Essentially, this method ensures that the dc side, comprising the Photovoltaic system and the battery, only needs to supply one-third of the household's ac loads—the major power consumers at any given time. The remaining power requirement is seamlessly met

by the ac grid. Consequently, the capacity of the dc side, inclusive of the PV system and the battery, is effectively reduced to one-third, promoting an efficient and balanced energy utilization strategy within the household. To govern the operation of the energy router, high-level algorithms are needed to monitor the input from the three-phase source, analyze the power requirements of the connected single-phase loads, and turn on the relays accordingly. This ensures that the single-phase loads receive a consistent and reliable power supply and is out of scope of this work.

5.3 Prototype description

The PCB design of the energy router in both 2D and 3D forms is presented in Figs. 5.2(a) and 5.2(b), respectively. During the design of the four-layer PCB for the energy router, which integrates both the control board and power board, several crucial considerations were implemented to ensure optimal performance and minimize EMI. The forward path and return path were aligned on different layers, with the signal trace placed on the top layer and its corresponding return path directly underneath the adjacent ground plane. This arrangement minimized the loop area, significantly reducing EMI.

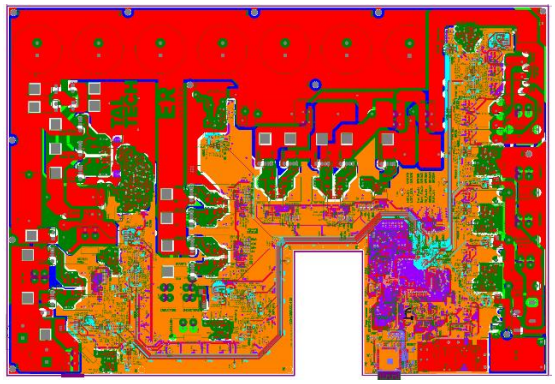


Figure 5.2 PCB design of the energy router in 2D from.

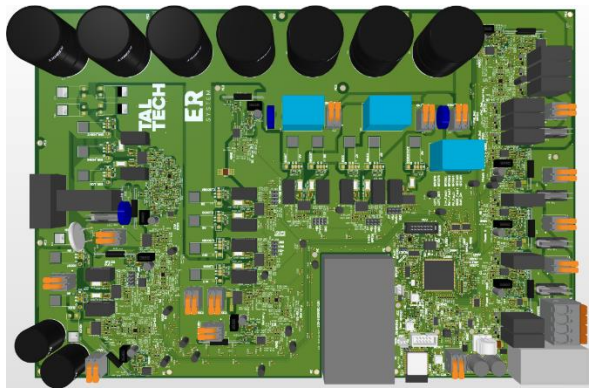


Figure 5.3 PCB design of the energy router in 3D form.

Analog and digital grounds were carefully separated to prevent noise from digital circuits affecting the analogue components. These grounds were connected at a single point using star grounding to avoid ground loops and maintain a common reference point. To maintain power integrity, one inner layer was dedicated as a continuous power plane, providing a stable and clean power supply to all components. Decoupling capacitors were placed close to the power pins of integrated circuits, filtering high-frequency noise, and stabilizing the power supply.

Component layout was meticulously planned to separate high-frequency components from sensitive analogue parts, reducing potential interference. Critical signal traces were kept as short as possible and routed away from noisy areas. Differential pairs were routed together to maintain signal integrity and reduce EMI, with controlled impedance traces designed for high-speed signals to prevent signal degradation.

Thermal management was another key consideration. For the power board section, which handles higher currents, thicker copper layers were used to dissipate heat effectively. Thermal vias were strategically placed to transfer heat from the top layer to the inner and bottom layers, ensuring even thermal distribution. Power components were arranged to avoid heat concentration, promoting efficient thermal management.

Ground fills and copper pours were used extensively around signal traces to provide extra shielding and further reduce EMI. These ground fills also aided in heat dissipation. For high-speed and high-frequency signals, adjacent ground planes were positioned to act as shields, minimizing radiated emissions and improving signal integrity. Through these detailed considerations, the PCB design for the energy router achieved a balance of performance, reliability, and EMI compliance, ensuring robust operation across various conditions.

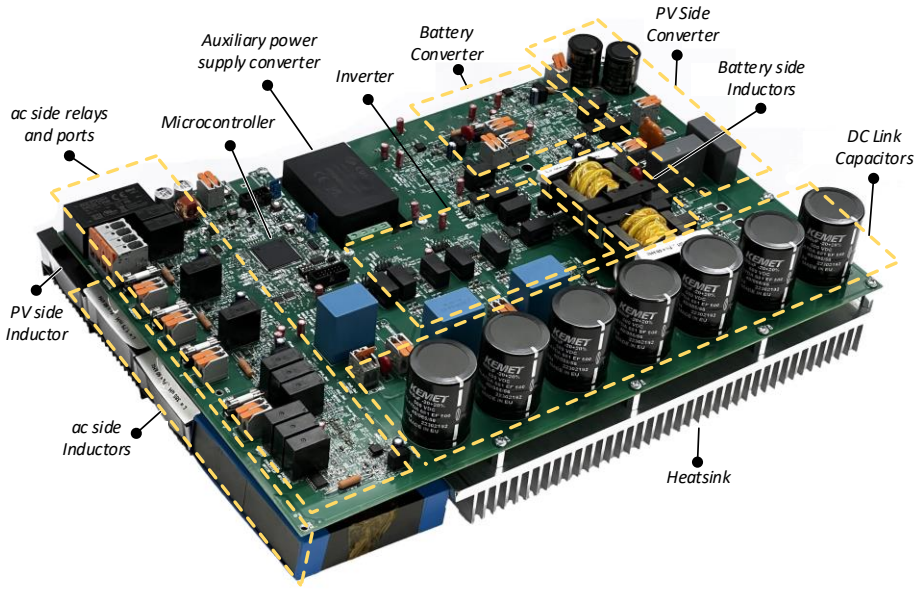


Figure 5.4 The prototype of the energy router assembled in the power electronics lab of TalTech.

Table 5.1. Design parameters of the energy router.

Parameter	Acronym	Value
Rated Power	P	15 kW
Grid and load side ac voltage (RMS)	V_{in}	230 V, 50 Hz
DC link voltage	V_{DC}	350 V
Nominal current of each phase	i_N	25 A
Switching frequency	f_{in}	65 kHz
Solar voltage input range	V_S	150 – 600 V
Battery input voltage range	V_B	150 – 330 V
Power switches of inverter	$S_1 \dots S_5$	C3M0025065K
Power switches of dc-dc converters	$S_6 \dots S_{11}$	C3M0021120K
Dc link capacitor	C_{dc}	3 mF
Inductor of inverter	L_{dc}	1.8 mH
Flying capacitor of inverter	C_I	3 µF
Filter inductors of inverter	L_{F1}, L_{F2}	680 µH, 320 µH
Filter capacitor of inverter	C_F	3.3 µF
Microcontroller	-	TMS320F28379D
Gate Driver	-	UCC21521CDW
Relays	$R_G, R_{Ga}, R_{Gb}, R_{Gc}, R_{La}, R_{Lb}, R_{Lc}$	G5PZ-1A4-E_DC12
Capacitor of buck-boost converter	C_S	100 µF
Inductor of buck-boost converter	L_S	850 µH
Diode of buck-boost converter	D_S	IDH20G120C5XKSA1
Inductors of boost converter	L_{B1}, L_{B2}	500 µH

5.4 Experimental results

The laboratory test prototype of the energy router is demonstrated in Fig. 5.4. The design parameters of the designed energy router are outlined in Table 5-1. The rated power of the device is 15 kW while the ac voltage on both the grid and load sides is 230 volts at 50 Hz. The dc link voltage is set at 350 V and a high switching frequency of 65 kHz ensures efficient energy conversion and control. The solar voltage input range spans from 150 to 600 V, accommodating various photovoltaic panel configurations and environmental conditions. Similarly, the battery input voltage range is specified as 150 V to 330 V, allowing for flexibility in battery selection and integration.

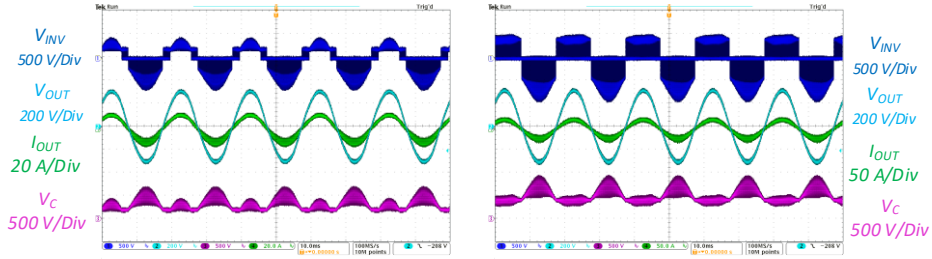


Figure 5.5 Experimental results of the inverter: (a), V_{in} = 200 V, P_{OUT} =2 kW, (b): V_{in} = 400 V, P_{OUT} =3.5 kW.

5.4.1 The three-level Inverter

The operation of the energy router's inverter is described in section 3. Here, the experimental results of the three-level common-ground inverter are demonstrated and explained. Measurements were conducted using Tektronix TPA-BNC voltage probes, TCP0150 current probes, and MDO4034B-3 digital oscilloscopes.

Fig. 5.5 shows the operation of the inverter including the output voltage before filtering (V_{INV}), the output voltage after filtering (V_{OUT}), the output current (I_{OUT}) and the voltage across the capacitor (V_C). 325 V is considered as the nominal peak value of the output voltage.

The results in Fig. 5.5(a) are obtained under 200 V input voltage. It is seen that V_{INV} is a three-level waveform which confirms the successful operation of the power converter in boost mode. Also, it is shown that V_{OUT} is a sinusoidal 50 Hz waveform, and its peak value reaches 325 V. Regarding the 200 V input voltage, this result confirms that the topology steps up the output voltage successfully. In this figure, I_{OUT} is a sinusoidal 50 Hz waveform and its peak value equals to approximately 12 A which corresponds to nearly 2 kW output power. It is also in phase with V_{OUT}, as expected under resistive load. In this figure, the voltage stress across the capacitor is shown.

The indicated results in Fig. 5.5(b) are obtained under 400 V input voltage. It is seen that V_{INV} is a three-level waveform with the highest value of 325 V. It confirms the successful operation of the power converter in buck mode. The peak value of I_{OUT} is approximately 22 A which corresponds to 3.5 kW output power.

Fig. 5.6 is devoted to the efficiency study of the converter without auxiliary power supply losses. Two output power levels are considered including 2 kW under V_{in}=200 V, and 3.6 kW under V_{in}=400 V. It is seen that the efficiency reaches approximately 97.8 % at 0.7 kW when the input voltage is fed by 200 V. The efficiency reaches 97.8 % at 1.5 kW under V_{in}=400 V. It is included from these figures that the highest efficiency is 97.8 %. It is also evident that maximum powers are not the same under V_{in}=200 V and V_{in}=400V. On one hand, the input current is limited by saturation current of the inductor, on the other hand, in case of boost operation, the losses are higher and in order to keep the same maximum dissipative power, the input power has to be cut. It is very common for most industrial converters, in particular in the solar industry.

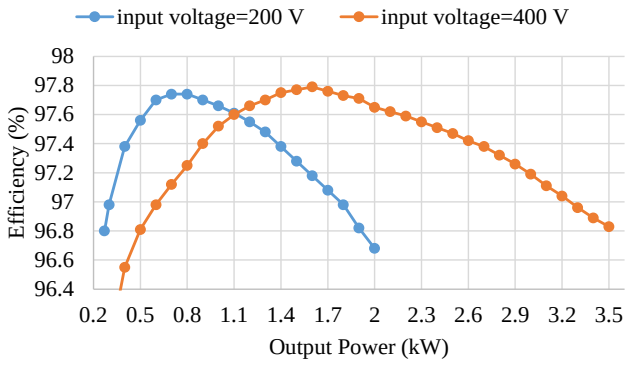


Figure 5.6 Efficiency study of the common-ground converter in different power levels.

5.4.2 The buck-boost dc-dc converter

In the designed energy router, a buck-boost dc-dc converter is used to stabilize and optimize the variable dc voltage generated by the panel, which fluctuates due to changing sunlight conditions. The converter ensures a consistent output voltage suitable for powering devices or charging batteries.

The experimental results for one operation point are demonstrated in Fig. 5.6. As demonstrated in this figure, the input and output currents are approximately 15 A and 8 A, while the voltages of the input and output are 200 V and 350 V respectively. Maximum efficiency approached 99 %.

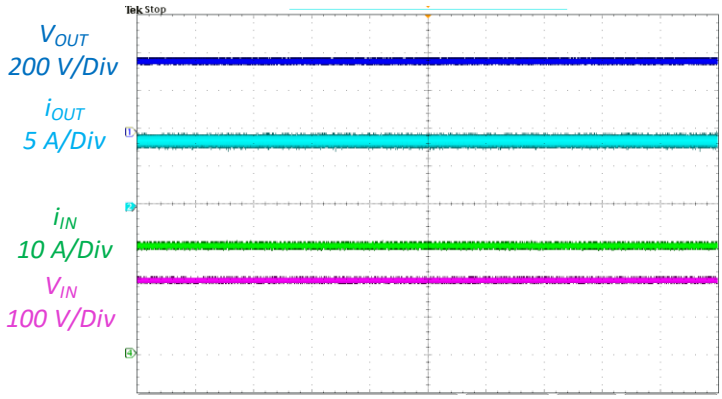


Figure 5.7 Experimental results of the buck-boost dc-dc converter.

5.4.3 The interleaved dc-dc converter

An interleaved boost dc-dc converter is connected directly to a battery in the energy router to precisely manage the charging and discharging processes, ensuring that the battery operates within safe voltage and current limits. It is comprised of four switches and two inductors. By interleaving two phases, the frequency of the output current ripple is effectively doubled. This reduction in the output current ripple is crucial for maintaining the health and longevity of the battery, as lower ripple currents decrease the thermal and electrical stress on the battery cells. Furthermore, the interleaved design allows for current sharing between two phases, reducing conduction losses. This improvement in efficiency is particularly beneficial in battery-connected systems where minimizing power losses is critical to extending battery life and improving overall system performance.

Examples of the experimental results of the interleaved boost converter are demonstrated in Fig. 5.7. As demonstrated in this figure, the input current is approximately 20 A, the output current is half this value at about 12 A. The voltages of the input and output are 200 V and 350 V respectively, which approves the boost capability of the converter. The current ripple is very small on the input side, while it is negligible at the output side. Maximum efficiency was higher than 98 %.

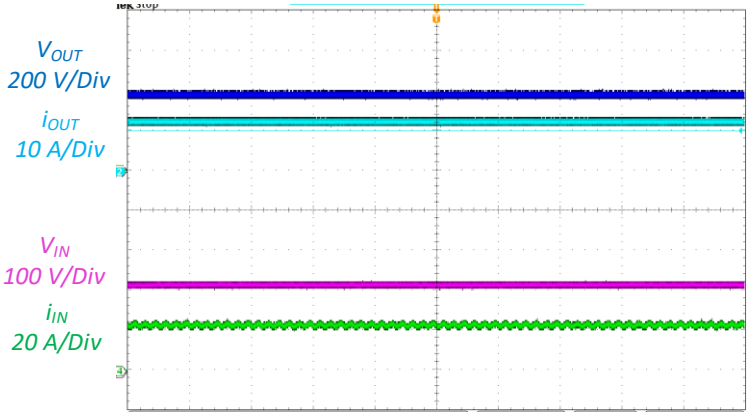


Figure 5.8 Experimental results of the interleaved boost dc-dc converter.

5.5 Summary

The designed energy router facilitates the use of both ac and dc power within a household and enhances energy management within residential buildings. It manages energy flow between PV, dc sources, energy storage systems, three-phase ac grid, and both dc and ac loads. The energy router's common-grounded structure is designed to suppress leakage currents and enhance safety, while the novel solid-state circuit breaker implemented within the structure provides complete decoupling of source and load sides during the fault clearance. The PCB layout is optimized for high-level EMC design. Through meticulous experimentation and analysis, the chapter demonstrates the practical viability of the converters implemented in the proposed energy router, showcasing its ability to manage the power efficiently.

This section approves the second hypothesis that common-ground interface solves the leakage current issue with no isolation requirements. During the experimental verification there is not any leakage current detected thought dc or ac systems.

Also, the context of this section indirectly approves the fourth hypothesis that single-phase power electronic interface with smart internal relays and energy management algorithm is sufficient to balance three-phase single-family house supply system.

6 Conclusions

The research undertaken in this thesis first, explores lifetime management techniques and fault-tolerant converters. By conducting a thorough analysis of lifetime extension methods and fault-tolerant designs, the research highlights the importance of these strategies in enhancing the reliability and longevity of power electronic systems. The proposed techniques, including hardware redundancy and switching state redundancy, provide robust solutions for managing faults and extending the operational life of these systems.

Another significant contribution of this work is the investigation and implementation of common-ground structures. This approach effectively addresses the challenge of leakage current suppression, which is critical for ensuring system safety and stability.

The design and analysis of reliable SSCBs form another part of this thesis. The introduction of SSCBs with soft-reclosing capabilities and enhanced safety features represents an innovative advancement in power protection technology. The experimental results demonstrate that these SSCBs improve the safety of power electronic systems by ensuring fast and reliable fault clearance.

An innovative aspect of this research is the development of an energy router specifically designed for residential applications. The designed energy router with a selection of state-of-the-art power electronic converters and a safety-enhanced circuit breaker ensures optimal and reliable performance. This energy router efficiently manages energy flow between ac and dc grids and loads. By monitoring energy usage across three ac phases and selecting the phase with the highest demand to be supplied by dc sources, the system's costs is reduced by only requiring the PV and battery systems to supply one-third of the total household energy at any given time.

The experimental validations conducted in this thesis provide strong evidence of the practical viability and enhanced performance of the proposed systems. The successful implementation and testing of the energy router prototype demonstrate its capability to manage diverse energy sources efficiently, ensuring a seamless integration of renewable energy into residential applications.

In conclusion, this thesis makes significant strides in the development of advanced energy management systems. By addressing key challenges related to lifetime management, fault tolerance, grounding, and protection mechanisms, the research paves the way for more reliable and efficient energy systems. Future work will focus on scaling these innovations to preindustrial prototypes (TRL6-8) and high-level control implementation, aiming to bring these advancements closer to widespread adoption and real-world application. The findings and contributions of this thesis are poised to play a crucial role in shaping the future of sustainable energy management, ultimately contributing to a more resilient and efficient energy infrastructure.

As a results of thesis, the author **claims** the following:

- Reliable design of power electronic systems requires lifetime management techniques including lifetime analysis, lifetime assessment and condition monitoring along with fault management approaches such as hardware redundancy and imbalance control.

  However, since control techniques without redundancy only compensate imbalance in the performance of the converters and cannot fully compensate and clear the

fault, the third hypothesis is not relevant to this case. Residential application can not tolerate significant cost increasing.

- The proposed soft turn-on auxiliary circuit can be added to the circuit breakers to achieve soft reclosing capability within the systems that may experience input and output voltage imbalances of up to 50 V.
- The proposed family of dc SSCB completely decouples the input and output terminals during the fault clearance and increases the voltage utilization rate of the switches by 20% while providing a fast protection under 10 μS.

  It validates the first hypothesis that advanced solid-state circuit breakers provide completely safe operation of the energy router in case of a fault.
- The energy router is designed with common-ground non-isolated feature to suppress leakage current. It also decreases the required rated power of PV and battery to one-third. It approves the second hypothesis that common-ground interface solves the leakage current issue with no isolation requirements. This confirms the fourth hypothesis that single-phase power electronic interface with smart internal relays and energy management algorithm is sufficient to balance three-phase single-family house supply system.

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Abstract

Common-ground energy router structure with enhanced reliability and protection

This thesis introduces a smart energy router for residential applications, focusing on the advancement of power electronics to enhance its reliability and protection. Investigating lifetime management techniques, including the analysis, assessment, and extension of the lifetime of power electronic systems, helps identify potential failure modes, develop strategies to mitigate risks, and optimize the design and operation of these systems. Methods to suppress leakage current in power electronic converters are studied, and a three-level inverter is implemented in the energy router using a common-ground structure to minimize leakage current. After the classification of fault management techniques to enhance the reliability of power converters, a fault-tolerant structure is proposed, which is common-ground, ensuring continuous operation even in the presence of faults.

The thesis introduces novel SSCBs designed for dc microgrids, which incorporate a soft turn-on auxiliary circuit to solve the voltage imbalance of the input and output terminals of power systems at the time of reclosing. Three innovative SSCB topologies (T-SSCB, Y-SSCB, and H-SSCB) are presented, featuring a third switch that bypasses fault currents, thereby eliminating snubbers from power lines and increasing voltage utilization rates. They also address challenges such as decoupling the source and load, improving MOV reliability, and managing charged capacitors during reclosing. These designs improve system reliability, efficiency, and safety while reducing component count and costs. Experimental results validate the effectiveness of the proposed SSCBs, demonstrating their potential for enhanced fault protection and safety in dc microgrids.

Additionally, the thesis introduces a smart energy router for residential applications. This device enables the integration and management of both ac and dc power sources, including photovoltaic systems, energy storage systems, and various loads. The energy router intelligently distributes power across single-phase structures, optimizes phase selection based on time and consumption patterns, and reduces the rated power of photovoltaic and battery systems. Through these innovations, the thesis contributes to the development of more reliable and efficient solutions for modern electrical systems.

Lühikokkuvõte
Ühise nulljuhtmega suurendatud töökindluse ja kaitsega energiaruuter

See töö tutvustab nutikat energiaruuterit eramutele keskendudes jõuelektroonika edendamisele selle usaldusväärsuse ja kaitse suurendamiseks. Elutsükli haldusmeetodite uurimine, sealhulgas jõuelektroonikasüsteemide eluea analüüs, hindamine ja pikendamine, aitab tuvastada potentsiaalseid rikkeid, arendada riskimaandusstrateegiaid ning optimeerida nende süsteemide projekteerimist ja tööd. Uuritakse lekkevoolu summutusmeetodeid jõuelektroonikamuundurites ning energiaruuteris rakendatakse kolmetasemelist inverterit, mis minimeerib lekkevoolu ühise maandusstruktuuri abil. Lisaks rikkehaldusmeetodite klassifitseerimisele muundurite töökindluse tõstmiseks pakutakse välja ühise maandusega riket taluv struktuur, mis tagab pideva töö ka rikkeolukorras.

Doktoritöö tutvustab uuenduslikke alalisvoolu mikrovõrkudele mõeldud pooljuhtkaitselüliteid (SSCBd), mis rakendavad sujuvkäivitusabiahelat, et tasakaalustada sisend- ja väljundterminalide pinged enne taas sisselülitamist. Esitletakse kolm uudset SSCB topoloogiat (T-SSCB, Y-SSCB ja H-SSCB), millel on kolmas lüliti rikkevoolu möödajuhtimiseks, vältides nõnda summutusahelaid toiteliinides ning suurendades pingekasutusmäära. Need käsitlevad ka alalispinge väljakutseid nagu allika ja koormuse lahutamine, metalloksiidvaristori (MOV) usaldusväärsuse parendamine ja laetud kondensaatorite haldamine ahela taassulgumisel. Sellised kaitselülitid parandavad süsteemi usaldusväärsust, tõhusust ja ohutust, vähendades samal ajal komponentide arvu ja kulusid. Katsetulemused kinnitavad pakutud SSCB-de tõhusust, näidates nende potentsiaali alalisvoolu mikrovõrkudes rikkekaitse tõhustamiseks ja ohutuse tagamiseks.

Lisaks tutvustab doktoritöö nutikat energiaruuterit eramutele. See seade võimaldab nii vahelduv- kui ka alalispingeallikate sh päikesepaneelide, energiasalvestussüsteemide ja erinevate koormuste integreerimist ning haldamist. Energiaruuter jaotab nutikalt võimsust faaside vahel, optimeerides faasivalikut aja ja tarbimismustrite põhjal ning maksimeerides efektiivsust, kohandades energia jaotamist nõudlusega. See lähenemine mitte ainult ei paranda stabiilsust ja väldib ülekoormust, vaid vähendab oluliselt ka päikesepaneelide ja akusüsteemide põhikulusid. Nende uuenduste kaudu panustab doktoritöö usaldusväärsemate, tõhusamate ja odavamate kaasaegsete energiahaldussüsteemide arengusse.