DOCTORAL THESIS

Photovoltaic String Converter with Universal Compatibility with AC and DC Microgrids

Oleksandr Matiushkin

TALLINNA TEHNIKAÜLIKOOL
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TAL TECH PRESS

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology, has not been submitted for a doctoral or equivalent academic degree.

Oleksandr Matiushkin

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OLEKSANDR MATIUSHKIN

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List of Publications

The following is a list of author's publications, on the basis of which the thesis has been prepared:

[PAPER-I] O. Husev, O. Matiushkin, C. Roncero-Clemente, F. Blaabjerg, D. Vinnikov, "Novel Family of Single-Stage Buck–Boost Inverters Based on Unfolding Circuit," *IEEE Trans. on Pow. Electron*., vol. 34, no. 8, Aug. 2019. DOI: 10.1109/TPEL.2018.2879776.

[PAPER-II] O. Husev, O. Matiushkin, D. Vinnikov, C. Roncero-Clemente, S. Kouro, "Novel Concept of Solar Converter with Universal Applicability for DC and AC Microgrids," *IEEE Trans. on Ind. Electron*., vol. 69, no. 5, May 2022. DOI: 10.1109/TIE.2021.3086436.

[PAPER-III] O. Matiushkin, O. Husev, J. Rodriguez, H. Young, I. Roasto, "Feasibility Study of Model Predictive Control for Grid-Connected Twisted Buck-Boost Inverter," *IEEE Trans. on Ind. Electron*., vol. 69, no. 3, Mar. 2022. DOI: 10.1109/TIE.2021.3068663.

[PAPER-IV] A. Fesenko, O. Matiushkin, O. Husev, D. Vinnikov, R. Strzelecki, P. Kołodziejeko, "Design and Experimental Validation of a Single-Stage PV String Inverter with Optimal Number of Interleaved Buck-Boost Cells," *open access Energies*, Apr. 2021. https://doi.org/10.3390/en14092448.

[PAPER-V] O. Husev, O. Matiushkin, C. Roncero-Clemente, D. Vinnikov, V. Chopyk, "Bidirectional Twisted Single-Stage Single-Phase Buck-Boost DC-AC Converter," *open access Energies*, Sep. 2019. https://doi.org/10.3390/en12183505.

[PAPER-VI] O. Matiushkin, O. Husev, D. Vinnikov, C. Roncero-Clemente, "Optimal LCL-filter study for Buck-Boost Inverter Based on Unfolding Circuit," *in proc. of 2020 IEEE 14th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, online event, Setubal, Portugal, Jul. 8-10, 2020. DOI: 10.1109/CPE-POWERENG48600.2020.9161683.

[PAPER-VII] O. Matiushkin, D. Vinnikov, O. Husev, "Performance Evaluation of the Universal Photovoltaic String Converter During the Operation in DC Microgrid Environment," *in proc. of IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, online event, Toronto, ON, Canada, Oct. 13-16, 2021. DOI: 10.1109/IECON48115.2021.9589473.

Author's Contribution to the Publications

The author's contributions to the papers in this thesis are:

[PAPER-I] Oleksandr Matiushkin is co-author of the paper. He was responsible for the simulation, calculation of the passive elements, and development of software for the experimental tests.

[PAPER-II] Oleksandr Matiushkin has co-authored the paper and provided the experimental results of both types of system: open-loop and closed loop based on the Model Predictive Control (MPC). The parts for the control and measurement system of the prototype were developed by him.

[PAPER-III] Oleksandr Matiushkin as main author developed the MPC system within the experimental prototype for a grid-connected system. Oleksandr Matiushkin has provided a literature analysis, calculation processes, and the writing. He was responsible for submission and contact with editors during peer-reviewing rounds.

[PAPER-IV] Oleksandr Matiushkin has co-authored the paper and provided a methodology of calculation and software developing for the experimental prototype. Oleksandr took part in the writing, review and editing of the paper.

[PAPER-V] Oleksandr Matiushkin is co-author of the paper. He was responsible for methodology, software developing, writing and draft preparation and for experimental validation.

[PAPER-VI] Oleksandr Matiushkin as a main author of the paper was responsible for the literature review, the writing, submission, and a calculation process. He has performed validation of the calculation in simulation. Oleksandr Matiushkin presented the paper online in virtual event IEEE 14th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG) 2020.

[PAPER-VII] Oleksandr Matiushkin was a main author of the paper. He has performed a literature review, experimental tests, writing and submission. He has developed a control system for the experimental setup. He presented the paper on virtual conference IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society.

Abbreviations

AC or ac	Alternative Current
ADC	Analog to Digital Converter
BVSI	Voltage Source Inverter with Boost Cell
CB	Circuit Breaker
CEC	California Energy Commission
SiC	Silicon Carbide
DC or dc	Direct Current
DCMG	Direct Current Microgrid
EMI	Electromagnetic Interference
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
MCU	Micro Controller Unit
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MPC	Model Predictive Control
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
PCB	Printed Circuit Board
PLL	Phase Locked Loop
PMC	Phase-Modular Converter
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SSA	Steady State Analysis
SSCB	Solid State Circuit Breaker
SSR	Solid State Relay
TalTech	Tallinn University of Technology
THD	Total Harmonic Distortion
TRL	Technology Readiness Level
VSI	Voltage Source Inverter

Symbols

C_{IN}	Input capacitor for decoupling the input current
C_s	Snubber capacitor of solid-state relay
C_S	Output capacitor of the converter
C_x	Capacitor
D	Duty cycle
D'	Inverted duty cycle and equals 1-D
D_1	Diode of the buck-boost part
D_{BB}	Duty cycle for buck-boost mode for Twisted buck-boost inverter based on Unfolding circuit
D_{BOOST}	Duty cycle for boost mode
D_{BUCK}	Duty cycle for buck mode
D_{Sx}	Duty cycle of the switch
ε	Efficiency of the converter
f	PWM frequency
f_g	Grid frequency
f_{SAMPLE}	Sample frequency
F	Fuse
I_{DC}	Current of dc grid
i_{C1}	Current of the unfolding capacitor
i_{CS}	Current of the output capacitor
i_g	Grid current
i_{IN}	Input current
Δi_L	Current change in the input inductance during PWM period
i_L	Current of the input inductance
I_{LMAX}	Maximum current value of the input inductance in ac mode
Δi_{Lf}	Current change in the output inductance during PWM period
i_{Lf}	Current of the output inductance
I_{LfMAX}	Maximum current value of the output inductance in ac mode
i_{LREF}	Reference signal for input inductor current
i_O	Output current of the off-gird mode
i_{REF}	Reference signal for grid current
K_C	Ripple factor of unfolding capacitor voltage
K_{Cs}	Ripple factor of output capacitor voltage
K_L	Ripple factor of input inductance current
K_{Lf}	Ripple factor of output inductance current
L_f	Output inductor of the converter
L_g	Grid side filter inductances
L_x	Inductance
N_C	Number of capacitors
N_L	Number of inductors

P	Input power of the converter
R_C	Unfolding capacitor's resistance
R_{CIN}	Input capacitor's resistance
R_{Cs}	Output capacitor's resistance
R_g	Grid resistance
R_{IN}	Input line resistance
R_L	Input inductance's resistance
R_{Lf}	Output inductance's resistance
R_s	Snubber resistance of solid-state relay
R_{SWx}	On state resistance of high-frequency transistor
R_{UNFOLD}	On state resistance of switch of unfolding circuit
REL_x	Mechanical relay
$S_{1\text{-}1}$-$S_{1\text{-}2}$	Solid state relay switches
S_{Wx}	Switch based on mechanical relay
S_x	High frequency switch
T_S	PWM period
T_x	Low frequency transistor
ΔV_C	Voltage spike at the grid side
Δv_{C1}	Voltage change of the unfolding capacitor during PWM period
v_{C1}	Voltage across unfolding capacitor
V_{C1MAX}	Maximum voltage value of the unfolding capacitor in ac mode
Δv_{CS}	Voltage change of the output voltage during PWM period
V_{CsMAX}	Maximum voltage value of the output capacitor in ac mode
V_{C_MAX}	Maximum voltage value at the grid side during disconnection from dc grid
V_{DC}	Voltage of dc grid
v_g	Grid voltage
v_{IN}	Input voltage
v_{L1}	Voltage across input inductance
v_{Lf}	Voltage across output inductance
V_M	Amplitude of the grid voltage in ac mode
v_{OUT}	Output voltage of the off-grid mode
v_{REF}	Reference signal
W_{jx}	Weight factor of cost function
Z_g	Grid impedance

1 Introduction

1.1 Background

Most of the electronic devices that we are using every day at home or at the office require a similar approach in terms of the power electronics. For example, in residential buildings with a traditional ac grid most loads have a dc nature, therefore all our devices at home require an additional converter. A traditional laptop's battery voltage is 15 V – 22 V. It is known that the rectified ac grid voltage equals a peak of a one grid phase 310 V – 325 V. Consequently, a laptop battery requires a converter, which rectifies the sinusoidal voltage to a constant 320 V (ac-dc converter: a rectifier diode bridge) and which reduces 320 V to the necessary constant 15 V – 22 V (dc-dc converter). Thus, the main power electronics of traditional electronic devices are intended to rectify the traditional ac grid in a constant voltage level and subsequently convert it to the necessary voltage value (laptop charger, phone charger, TV, light systems, PC, etc.), as shown in Fig. *1.1a*. At the same time, the amount of renewable energy systems which produce a dc voltage and current is increasing each year. The issue thus arises: "Is it reasonable to use devices with a redundant ac part, instead of simple dc-dc converter?".

Although the war between Tesla and Edison has long finished, the modern systems have forced humanity to revive this issue with renewed vigour [1], [2]. Nowadays, dc microgrids attract more attention because many sources and loads have a dc nature. For example, solar panels, fuel cells and energy storage systems generate only dc voltage and current. It would be logical to connect all devices with a common dc bus [3], [4], without redundant ac conversion. Fig. *1.1b* shows an example of the possible DCMG architecture addressed in [5]-[8]. The considered DCMG system is more efficient and reliable. Moreover, the dc grid is free from harmonics and does not provide a reactive power. DCMG systems do not need complex synchronisation and control units.

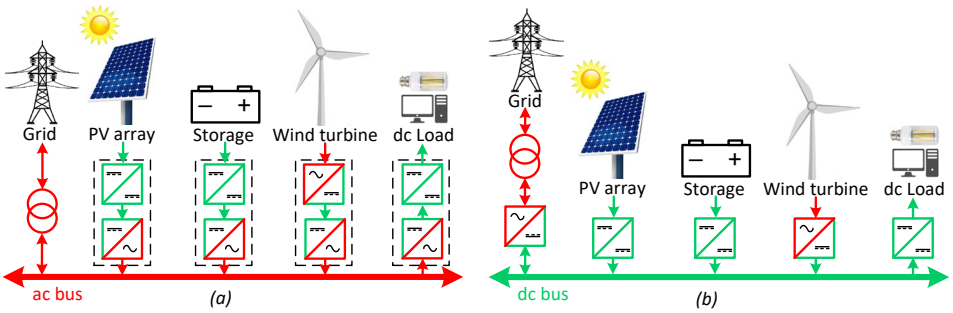


Figure 1.1 Traditional ac distribution system (a), Considered energy transmission system based on common dc bus (b).

However, the ac grid still dominates because there is no clear standard for the dc grid. From an economical point of view the voltage level of 326 V is the most sustainable for the dc grid [9]. This voltage level is applicable to the grid systems using existing cables. However, a company in Netherlands claims that the possible standards are 350 V for low power and 700 V for high-power applications [10]. It is proven in [11] that a high-voltage dc system is more efficient than a traditional ac distribution system. Possible dc distribution systems imply the creation of a different voltage level standard for dc grid types, such as

DCMG, dc nano grid, etc. [12], [13]. The modern base of the power electronics can provide any transformation of the power, however the price for that is still high.

One of the main challenges for dc distribution systems is to develop a circuit breaker for dc grid systems. A conventional ac circuit breaker determines short circuit and works under a zero-crossing point (standardised solutions IEC 61869, IEC 60255, IEC 61850, and IEC 60834). The clearing time in ac grid systems is 80 ms (4 cycles) [14]. Dc grid voltage does not fall to zero, so the conventional protection systems are not suitable. In contrast to conventional relays, it should be a device that keeps the same features as traditional and disconnects the circuit fast. One possible solution is Solid State Relay (SSR) or hybrid mechanical breakers [15]. This type of breaker should offer following features [16]: a fast response, low power losses, high reliability, compact size, long lifetime, and low cost. There are several ideas for the implementation of a dc breaker [17],[18]. Despite the drawbacks of the dc systems, the benefits outweigh the disadvantages. The dc grid will probably appear during the next decade and is already attracting attention as a future electric transmission system.

1.2 Motivation of the Thesis

Since the dc grid appeared as a trend, devices applicable to both types of grids have come into demand. For example, hybrid converters have several terminals for each grid bus [19], [20]. Most of the solar hybrid converters have intended power electronics for each type of electrical distribution system. Moreover, a hybrid converter usually has a dc terminal for a storage element. However, there is a converter that has several terminals for the ac and dc grid. The general term for this type of device is a multiphase or multiport converter [21], [22], [23]. Multiphase converters can be useful for multiphase ac and dc applications. Another possible solution is an energy router for residential applications [24],[25],[26]. They have terminals for each part of the system (dc grid, ac grid, storage, PV panels, etc.). However, all the mentioned converters have a significant drawback as an internal redundancy. This is because these converters require different parts of power electronics to provide transmission energy from/to source to/from the undefined grid. Moreover, these converters will have separate control units and induvial protection systems for each type of grid.

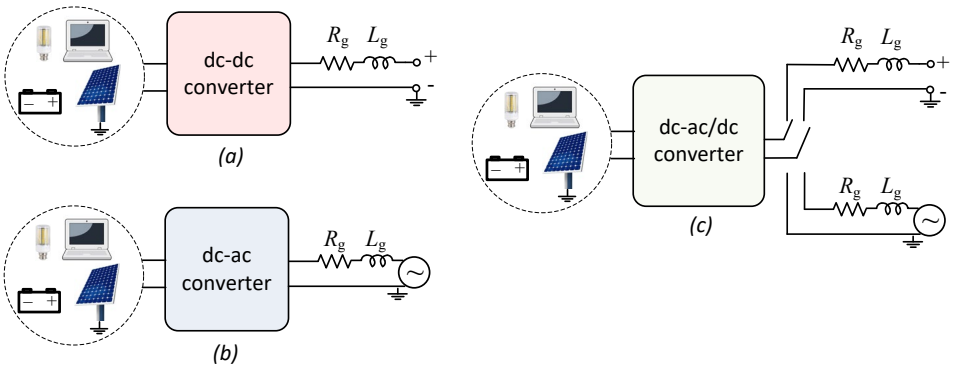


Figure 1.2 Connection of loads, storage systems or solar string to: dc grid with dc-dc converter (a), ac grid with dc-ac converter (b), any type of the grid with universal dc-ac/dc converter (c).

On the other hand, if in the near future the dc grid will be integrated into our residential buildings, a type of converter should also be suitable for the ac grid. For example, the dc grid socket will be integrated in a building and logically a customer will buy a dc-dc charger (Fig. *1.2a*). In the second case, when this customer comes to an old building with a traditional ac grid socket, he will require an ac-dc charger for his laptop, as shown in Fig. *1.2b*. From an economical part of view, a universal solar converter is cheaper and offers the benefits of dc-dc and dc-ac converters. The universal solar converter takes away inconvenience for the customer because the market is limited for dc-dc devices. Such a converter can be connected to both types of grid by the same terminals and at the same time has minimal internal redundancy (Fig *1.2c*). The universal converter with minimum redundancy will use the same protection system and control unit for both types of grid, while the control system will automatically detect a type of connected grid. At the same time the universal converter can be bidirectional and suitable for PV applications or other renewable energy sources.

This thesis was conducted according to one of the research directions of the Power Electronics Group of Tallinn University of Technology. The aim is to gather knowledge and develop the universal solar converter for residential dc and ac grids with minimum redundancy. The current work was supported by PRG675 “New Generation of High-Performance Power Electronic Converters Simultaneously Applicable for dc and ac Grids with Extended Functionalities”, and by EAG122 “Universal dc/ac battery storage interface (UniBSI)”, and by PRG1086 “Future-Proof Power Electronic Systems for Residential Microgrids” from Estonian Research Council, and by TAR16012AT “Zero energy and resource efficient smart buildings and districts” from the Archimedes Foundation and.

1.3 Aims, Hypothesis and Research Tasks

The main aim of the PhD research project is to develop and experimentally confirm a concept of universal dc-dc/ac converter which is applicable for both types of grid. It considers a solution which may speed up transition from conventional ac systems to the hybrid dc/ac systems. The author set a goal to obtain acceptable efficiency in comparison with popular solutions by using the low-frequency unfolding circuit. The outcome of this work is to develop and launch TRL 6 prototype with a real ac grid and virtual dc grid.

Hypotheses:

1. Buck-boost cells with unfolding circuit may provide the universal operation with minimal redundancy.
2. Buck-boost cells with unfolding circuit may provide the reactive current injection in the ac grid-connected mode.
3. Synchronous switches operation reduces zero crossing distortions and improves quality of the grid current.
4. Model Predictive Control (MPC) with modified cost function can be feasible for implementation with low-cost microcontrollers.

Research tasks:

1. To review the existing solutions on the market.
2. Research and design the most suitable power electronic interface for universal application.

3. Research power electronics interface requirements for simultaneous applicability for AC and dc grids.
4. Research and develop a control regulator for a grid-connected system.
5. Design of the experimental setup and experimental verification of the universal converter simultaneously applicable for ac and dc grids.

1.4 Research Methods

The research methods used to carry out the thesis are based on the mathematical analysis, simulation models and experimental verification. New developed topologies and circuits are mathematically analysed using Steady-State Analysis (SSA) [27], [28] as well as transient analysis using functional analysis, including Laplace and Fourier transform techniques. To study the operating properties of the new topologies and control algorithms, dynamic and static models (with and without losses in components) are developed. Computer simulations are generally performed in the MATLAB, Altium Designer and PSIM software packages, which are all available at the Tallinn University of Technology (TalTech). Experimental investigation and validation of theoretically predicted results are performed using small laboratory physical models (≤5 kW) of new topologies, circuits, and unconventional arrangement. The Power Electronics Research Laboratory of TalTech has modern facilities (digital oscilloscopes and function generators, power quality and efficiency analyzers, microprocessor development tools, PCB prototyping, and assembling tools, etc.) for the hardware and software development.

1.5 Contributions and Disseminations

The results of the research are presented via scientific publications, conferences, symposiums, doctoral schools, and presentations. During PhD studies the author contributed to 18 publications. Among them, nine papers were published in peer-reviewed international journals. The remaining papers were reported at international IEEE conferences. The dissertation is based on seven main scientific publications, including five journals and two conference papers presented at two IEEE international conferences.

Scientific novelties:

- Development of novel family of topologies suitable for universal application.
- Definition of requirements for the power electronics interface for universal application.
- Synthesis of novel modulation approach for dc-dc or dc-ac converters.
- Synthesis and control the grid current of the minimum phase system using MPC.
- Comprehensive comparative analysis of buck-boost inverter based on unfolding circuit and conventional solution as a H5, H6 and HERIC topologies.

Practical novelties:

- Reducing zero crossing distortion of the topologies based on the unfolding circuit using synchronous switches instead of diodes and shift methods.
- Developing a new type of device applicable for both types of grid with the same terminals and minimum redundancy.

- Two buck-boost inverters based on the unfolding circuit were assessed and experimentally confirmed with a grid-connected system: single-stage buck-boost inverter based on the unfolding circuit; twisted buck-boost inverter based on the unfolding circuit.

1.6 Experimental Setup and Instruments

The experimental setup was assembled in the power electronics laboratory of Tallinn University of Technology. The workspace in the lab is shown in Fig. *1.3a*. The oscilloscope Tektronix MDO4034B-3 helps to catch the waveforms of voltages and currents of the passive components. The special probes Tektronix P5205A and Tektronix TCP0030A are useful for voltage and current measurements respectively. The Code Composer Studio is an environment for writing a code for MCU from Texas Instruments and was used during code developing.

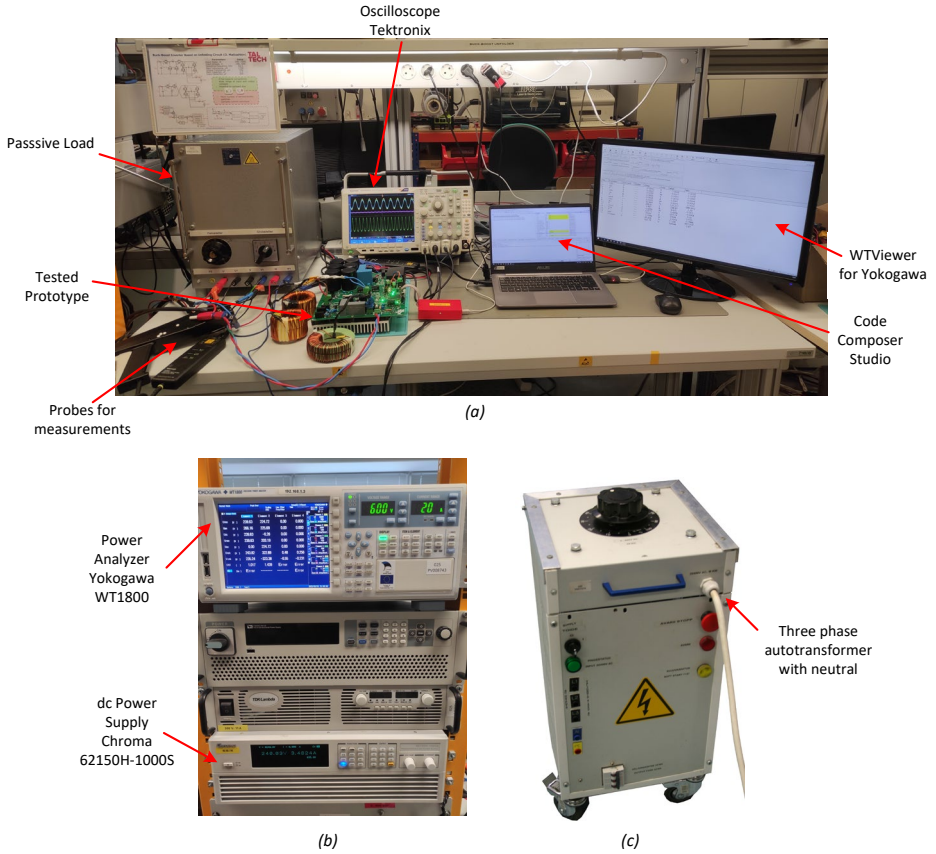


Figure 1.3 Workplace in the laboratory of power electronics (a), Power analyser with a dc source for the experimental setup (b), An autotransformer for a grid connected system (c).

Power Analyzer Yokogawa WT1800 was used for efficiency measurement within software application WTViewer for remote equipment access. The solar simulator equipment Chroma 62150H-1000S was used as an input voltage source for an experimental prototype, as shown in Fig. *1.3b*. The passive load Frizlen BW 20 was used

in the open loop system, while the autotransformer was chosen for the grid-connected system as a grid (Fig. *1.3c*).

1.7 Thesis Outline

Chapter 2 describes the concept of the universal dc-ac/dc converter based on the buck-boost converter with an unfolding circuit. The passive element design is considered in Chapter 2. The experimental results based on the open loop system are presented.

In Chapter 3 control system details are discussed. The non-linear control block based on the MPC is a main regulator, which is considered in Chapter 3. The special control strategy simplifies a calculation and decreases computational time.

The experimental results for the grid-connected system are presented in Chapter 4. The chapter considers all experimental setups that were developed based on the thesis topic.

The last Chapter 5 provides a comparison of the buck-boost inverter based on the unfolding circuit with conventional solution as a H5, H6 and HERIC topologies. The comparison results allowed the possibility to choose the necessary semiconductors.

2 Concept of the Universal dc-dc/ac Converters

The target of dc grid integration of PV plants leads to the appearance of a string dc-dc converter, although conventional dc-ac inverters are still in demand. The market for the solar microinverters concluded the same statement. The isolated dc-dc solar converters are useful for customers. Currently companies [10], [29], [30] consider dc-dc solar optimizers and string dc-dc converters as a future target market. However, the universal dc-dc/ac converter can be useful as an alternative solution. This alternative solution provides flexibility and the possibility of a connection to dc grid or to ac grid. The same features can be found in any of the renewable energy converters.

The simplified structure of the universal dc-dc/ac solar converter is shown in Fig. *2.1*. The structure contains a semiconductor stage depending on topology, an output filter along with an Electromagnetic Interference (EMI) filter, protection hardware circuit and grid side with an impedance. Such a structure can be considered as an interface between dc input voltage source and any residential grid (dc or ac). Moreover, a similar system is suitable for an ac voltage source as well. This solution can be generalized for any application with a grid connection.

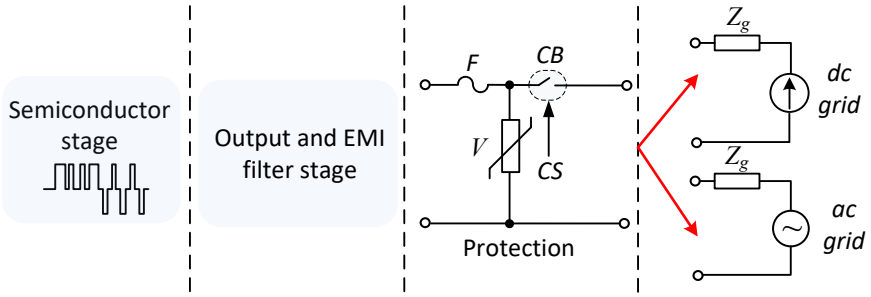


Figure 2.1 Simplified structure of the universal dc-dc/ac solar converter.

One of the main aims of this chapter is to define the requirements for power electronics converters and a possible internal structure for a universal solar converter for dc and ac operation modes.

Fig. *2.2* shows several possible topologies for a semiconductor stage of the single-phase universal string solar converter. The conventional Voltage Source Inverter (VSI) with an intermediate dc-dc boost cell can be connected to the dc grid (Fig. *2.2a*). A simple full-bridge inverter with a boost dc-link has a wide range of the input voltage regulation, a simple control strategy and freewheeling states. Some good overviews of the conventional solar inverters are provided in [31], [32]. At the same time many inverters can work in the dc-dc mode. High step-up inverters [33], [34], [35] or common ground inverters can also be competitive solutions [36], [37]. However, they may have inherited limited power range or lower efficiency from dc-ac mode.

On the other hand, Fig. *2.2b* shows one more possible solution for a universal single-phase dc-dc/ac solar converter. The structure of such a topology is similar to an interleaved synchronous buck-boost converter. The similar approach for boost converter and common input voltage source was discussed in [38].

The third option as a possible universal solar converter is an inverter based on the unfolding circuit [39], [40], [41]. Fig. *2.2c* shows a buck-boost inverter as part of the family of inverters based on unfolding circuit [42]. Such a solution can easily be adapted for the

dc-dc operation mode by the control system without any impact on redundancy. Moreover, the high number of semiconductors does not produce an excessive amount of switching losses, because the system has the minimal number of simultaneously switching semiconductors. At the same time, a buck-boost inverter based on the unfolding circuit does not have problems with leakage current, because it does not have a high-frequency component in the common-mode voltage.

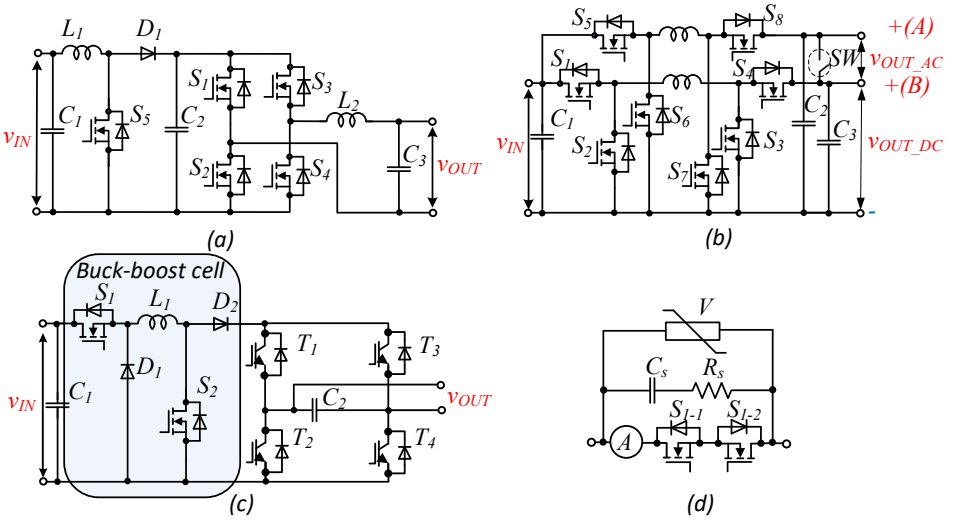


Figure 2.2 Conventional VSI as a universal dc-dc/ac solution (a), Buck-boost derived universal dc-dc/ac converter (b), Buck-boost inverter based on unfolding circuit as universal dc–dc/ac converter (c), Solid-state relay based on four-quadrant switch (d).

2.1 Protection Issue

The protection circuit is a usual tool for disconnecting the converter from the grid line. Such instruments are a standardised solution (IEC 61869, IEC 60255, IEC 61850, and IEC 60834). The important part of protection is a circuit breaker for a fast system break from the grid side. The main internal structure of ac CB is electromechanical components, which allows the possibility to disconnect the circuit during the zero-crossing point, which is a traditional principle of fault isolation. EMI filter is needed for avoiding higher harmonics propagation. As mentioned in Chapter 1, the time of CB in ac system equals around 80 ms, which corresponds to 4 cycles. An additional protection tool such as a fuse can prevent burning out all switches and unnecessary system activation after a fault. A varistor saves the system from overvoltage of the grid side.

However, a traditional CB became an unusual tool with the appearance of the dc grid concept, because dc voltage does not fall to zero value. Thus, designing a good protection system for the dc microgrid has been a challenge over the past few years [16]. A target fault clearing time in dc transmission system is considered as 2.5 ms.

The structure of the possible protection circuit between the power electronic converter and the low voltage dc grid can be the same. However, the main problem is the nature of the dc fault current because it can rapidly rise to more than a hundred times the nominal current. The dc microgrid has a low line impedance Zg. As a result, the fault current deviation is so big, and during a couple of milliseconds the current

increases to hundreds of amps. It means that ac protection instruments cannot be useful for dc grid protection. Dc grid protection should include high communication speed and good breaker functionalities [43]. As mentioned, one of the possible solutions for CB is a solid-state relay. These solutions offer such key features as fast response, high reliability, low conduction loss, long lifetime, and low cost. On the other hand, if CB is suitable for dc grid protection, it can be applied to the ac grid as well. Fig. *2.2d* shows the possible solid-state relay for a dc grid CB. The SSR is based on a four-quadrant switch and a current sensor. An additional snubber in parallel provides smooth switching, while a varistor save CB from overvoltage.

2.1.1 Grounding Issue

Grounding is another issue which relates to safety and protection. The traditional ac system ground has or may have the same potential as a neutral ground. However, the potential between ac and dc ground is undefined if ac and dc grids coexist together in the future. The main reason is that the dc bus line will be derived by rectification of the ac voltage. There are several options that can be utilized for grounding. The first solution is to use galvanic isolation between the dc and ac sides via using a transformer. The other options are to set low or high resistance grounding or without grounding [44], [45]. None of these solutions have an impact on the discussed universal solutions. If a universal converter works with an ac system, where the impedance between ground and neutral wires are low, then it can work with the dc grounded system as well.

Another important issue is a leakage current, which appears in all transformerless no-common-ground converters. In most cases it can be solved by common-mode filters [46], [47], that can be easily integrated into a circuit. Another way is to apply special modulation techniques to reduce a leakage current [48], [49]. The universal solar converters based on the unfolding circuit have a very small high-frequency common-mode voltage component. Thus, the EMI filter is not needed for universal dc-dc/ac converters. The negative output terminal of buck-boost inverter based on the unfolding will be connected to common ground in the case of dc mode and a leakage current will be absent.

2.1.2 Output Filter Selection in Terms of Protection

Another important parameter is the grid current quality. Filters with inductors at the grid side are the most suitable to control the grid current. In many cases the grid side inductance is assumed as an internal grid impedance. The calculation guidelines are well-known and have been widely studied [50]. The topic of the dc grid systems along with converters connected to the dc grid has become popular. However, the grid filter design is not so widely studied. Usually, the capacitor is used at the grid side, but the specific value of grid capacitor is not defined.

A simple filter can be integrated into a simple boost converter where the input inductor is not connected to the output capacitor. The same LC-filter can be suitable for a conventional buck converter, see Fig. *2.3a*. In both cases the grid capacitor should be small in order to prevent high spikes during connection to the grid, because there can be a voltage difference. On the other hand, Steady State Analysis does not require an additional capacitor for grid current quality. At the same time, a sudden disconnection from the grid can be accompanied by a voltage spike due to the presence of the output inductor. Thus, this capacitor can be considered as a suppressor to limit possible voltage spike.

The CLC-filter in Fig. *2.3b* can be considered as a further derivation of a C-filter suitable for boost converters. The capacitor C_1 along with the inductor L_1 are the main filtering elements, while the grid side capacitor C_2 is a suppressor. Fig. *2.3d* shows a simplified equivalent circuit of a sudden dc grid disconnection process in the case of a grid side LC-filter. The control system has to perform a short circuit at the output side of the converter to minimise the voltage spike ΔV_C across the capacitor C_1 after detecting a sudden dc grid disconnection.

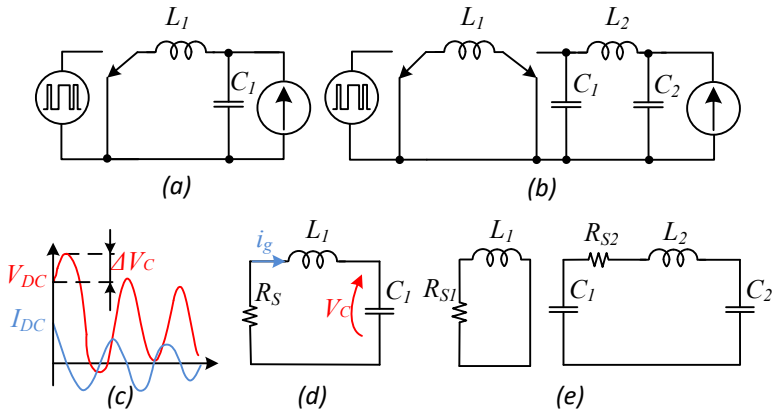


Figure 2.3 Switching process during sudden dc-grid disconnection: disconnection schematic for LC-filter (a), disconnection schematic for the LCLC-filter (b), transient process of the output voltage and output inductor current (c), equivalent circuit of the LC-filter (d), equivalent circuit of the LCLC-filter (e).

The perfect transient waveforms are shown in Fig. *2.3c*. As usual the waveform of transient process is oscillation. The above process describes the equivalent circuit in Fig. *2.3d*, and it is possible to derive differential equations:

$$L_1 \cdot \frac{di_g}{dt} = -i_g \cdot R_S - v_C \,,\; C_1 \cdot \frac{dv_C}{dt} = i_g \;. \tag{2.1}$$

If the disconnection from the dc grid occurred, the initial conditions will be as follows:

$$i_g(0) = I_{DC} \,,\; v_C(0) = V_{DC} \,, \tag{2.2}$$

where V_{DC} is a dc grid voltage at the moment of disconnection, while the I_{DC} is a grid current at the moment of disconnection.

The voltage across the output capacitor is starting to grow up to maximum value V_{C_MAX} after disconnection from dc grid due to the accumulated energy in the inductor. The solution of eq. (2.1) is simple, but it is massive. The series resistance defines the damping ratio of this oscillation but does not have a significant influence on the maximum value V_{C_MAX}.

If to neglect parasitic resistance Rs, it is possible to find a simplified expression of the maximum voltage across the capacitor. The entire accumulated energy in the inductor is flowing to the capacitor:

$$\frac{L_1 \cdot I_{DC}^2}{2} = \frac{C_1 \cdot \left(V_{C\_MAX}^2 - V_{DC}^2\right)}{2}. \tag{2.3}$$

Finally, the expression for the voltage spike ΔV_C across the capacitor C_1 can be calculated:

$$\Delta V_C = V_{C\_MAX} - V_{DC} = \sqrt{\frac{L_1}{C_1} \cdot I_{DC}^2 + V_{DC}^2} - V_{DC}. \tag{2.4}$$

The value of the voltage spike is proportional to the initial current and filtering inductance, while it is opposite to the value of the suppressing capacitor. As a result, design guidelines must consider a maximum voltage spike across the capacitor and maximum power of the converter.

Fig. *2.3e* shows the equivalent circuit in the case of CLC- and LCLC-filters after dc grid disconnection. Based on this circuit, the expression of the suppression capacitor can be obtained in a similar way to solving differential equations. In the case of the CLC-filter, one more differential equation is needed:

$$L_1 \cdot \frac{di_g}{dt} = -i_g \cdot R_S,\ C_1 \cdot \frac{dv_{C1}}{dt} = -i_g,\ C_2 \cdot \frac{dv_{C2}}{dt} = i_g. \tag{2.5}$$

The initial values are the same as before and correspond to grid voltage and current:

$$i_g(0) = I_{DC},\ v_{C1}(0) = V_{DC},\ v_{C2}(0) = V_{DC}. \tag{2.6}$$

In the same way it is possible to identify energy between capacitors and inductor after disconnecting from the dc grid. It is possible to write a system of equation to get the suppressor voltage spike:

$$\begin{cases} C_1 \cdot \dfrac{V_{DC} - V_{C\_MAX1}}{t_0} = C_2 \cdot \dfrac{V_{C\_MAX} - V_{DC}}{t_0} \\ \dfrac{L_2 \cdot I_{DC}^2}{2} = C_1 \cdot \dfrac{V_{C\_MAX1}^2 - V_{DC}^2}{2} + C_2 \cdot \dfrac{V_{C\_MAX}^2 - V_{DC}^2}{2} \end{cases}. \tag{2.7}$$

Finally, solving equation system 2.7 gives a result for the voltage spike across the suppression capacitor:

$$\Delta V_C = \frac{I_{DC}\sqrt{C_1 C_2 L_2 \left(C_1 + C_2\right)}}{2C_2\left(C_1 + C_2\right)}. \tag{2.8}$$

All other passive components of the universal converter part can be calculated similarly to the classical approach [PAPER-VI], [51] keeping the ripple in the current as a main parameter to be reduced.

2.2 Summary

The converter based on unfolding stage can naturally provide dc or ac output voltage without additional redundancy. The power electronics converter that was initially designed for dc-ac application with an output filter stage for dc grid and fast protection relay can be considered as a universal solution. The CB must cover all demands of dc grid protection, while the output filter can be chosen as a filter for conventional ac application with an additional output capacitor (suppressor) to eliminate voltage spike at a sudden grid disconnection. The considered approach can be used as an industrial solution for low-voltage dc and ac systems.

3 Application Oriented Design

The fundamental waveforms of a converter are independent of the selection of components and electric parameters (e.g. switching frequency, selected semiconductors) and result from the basic modulation scheme and yield some general requirements for the dimensioning of the components. General requirements include passive components' estimation taking into account the same current ripple in the inductors and the same voltage ripple across capacitors.

The volume of a core of the inductor as well as the volume of capacitor can be estimated based on its maximum accumulated energy:

$$Vol_L \cong \sum_{i=1}^{N_L} L_i \cdot \hat{i}_{Li}^2, \;\; Vol_C \cong \sum_{i=1}^{N_C} C_i \cdot \hat{v}_{Ci}^2, \tag{3.1}$$

where L_i and C_i are values of i inductance and capacitor, N_L is number of inductors and N_C is number of capacitors. $\hat{i}_{Li}$ is a peak inductor current and $\hat{v}_{Ci}$ is a peak of capacitor voltage.

Moreover, the relative switching and conduction losses that are independent from the selection of semiconductors can be introduced. First of all, the relative conduction losses are proportional to the square of the switch current. As a result, total conduction losses can be scaled to the following scale:

$$CL \cong \sum_{i=1}^{N_S} \tilde{i}_{Si}^2, \tag{3.2}$$

where $\tilde{i}_{Si}$ is RMS switch current, N_S is a number of switches.

Neglecting the current ripple, both the semiconductor voltage v_{Si} and semiconductor current i_{Si} influence the hard switching losses [56]. The average value of the product v_{Si} ·and i_{Si} over a fundamental period *T* express a good measure to indicate switching losses:

$$SL \cong \sum_{i=1}^{N_S} \left\langle \hat{i}_{Si} \cdot \hat{v}_{Si} \right\rangle_T . \tag{3.3}$$

Table 3.1 Target parameters of the universal interface converter.

Parameters	Value
RMS grid voltage V_{grid}, V	230 ac/350 dc
Output power range P, W	100-3600/100-5000
Input voltage range, V	100-500
Maximum input current, A	10/18
Maximum input current ripple, %	40
THD of the output current in the ac mode, %	5
Maximum output current ripple in the dc mode, %	5
Maximum switching frequency	62 kHz

Obviously, unfolding transistors do not contribute to the switching losses, as no switching transitions occur. Taking into account the size and price optimisation, it is necessary to calculate the minimal values of passive components that are able to provide acceptable input and output power quality. At the same time, due to the

non-conventional utilisation, it has to take into account both dc and ac modes. Table 3.1 summarises the parameters of the universal interface converter including target demands for passive components.

3.1 Design of the Filters

Steady state analysis is considered as the main tool for calculations. SSA allows to obtain the expressions of the passive components with sufficient tolerance. The calculation of inverters based on the infolding circuit has a difference to a simple SSA because the system is the 4th order type in buck mode and the 3d order type in boost mode. The calculation is too bulky, which is why only a buck-boost inverter with an unfolding circuit which operates in a buck mode was considered. The same approach was applied to all selected topologies for all modes: buck and boost.

Basically, the calculation of the passive components with using SSA relates to the dc-dc converter. On the other hand, the ac grid-connected system also operates with a high switching frequency. It is possible to underline that, during several PWM periods, any power parameter is in a steady state. The output voltage is a sinusoidal power signal, while the output current directly depends on the output voltage and the load:

$$v_{OUT} = V_M \cdot \sin(\varphi),\ i_O = {v_{OUT}}/{R_L},\ \quad (3.4)$$

where V_M is the peak of the output voltage, R_L is a resistance load.

Fig. *3.1* shows the topologies of the buck-boost inverters based on the unfolding circuit that were proposed as the inverter's family in [42].

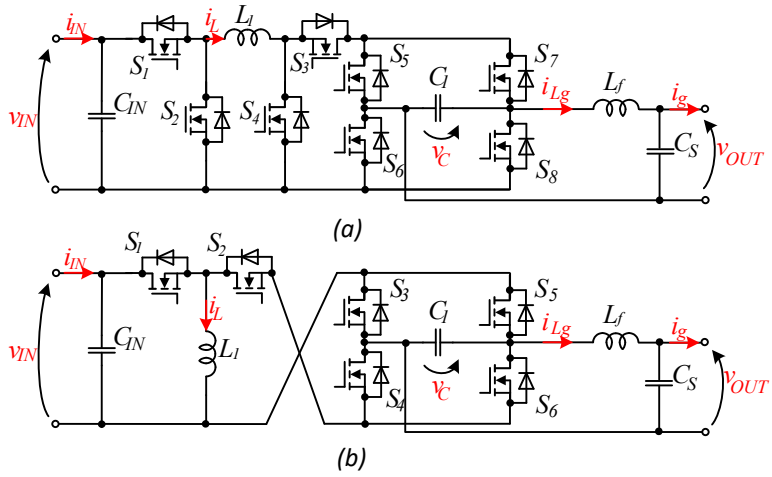


Figure 3.1 Family of the single-phase buck-boost inverters based on the unfolding circuit: Buck boost inverter with unfolding circuit (a), Twisted buck-boost inverter based on unfolding circuit (b).

The first topology of the inverter's family is a single buck-boost inverter based on the unfolding circuit with two inductors (Fig. 3.*1a*): the input inductor is a main part of converter and the second is a grid filter inductor. The circuit consists of an input inductance L_1, a small capacitor C_1 instead of a big dc-link capacitor, the output LC-filter for protection and current quality and eight switches S_1–S_8. In part, the principle of

operation is described in [52], which selects the mode of operation based on the ratio between the input and the output voltage.

The unfolding circuit is operating with a low frequency of switching, while the buck-boost part is working with high frequency. Despite a high number of switches that generally decrease reliability, it provides a very flexible modulation strategy. Switches S_1 and S_2 correspond to buck mode and S_3, S_4 are working in boost operational mode. At the same time, transistors S_1 and S_3 are the main switches of the basic operation modes of the converter.

The transistors S_2 and S_4 can be replaced by diodes in case unidirectional operation is required. In the case of bidirectional power flow, the switches S_2 and S_4 should be selected as transistors. A bidirectional power flow allows the possibility to work as a rectification converter, which may be useful in another application. Transistors S_5-S_8 work as a simple unfolding circuit in accordance to the classical unfolding circuit. Potentially, the unfolding switches can also be used with a high-frequency modulation.

The buck mode will be applied when the input voltage v_{IN} will be higher than the instantaneous value of the output voltage. The buck mode operates using a traditional duty cycle dependence:

$$v_{OUT} = D_{S1} \cdot v_{IN} . \tag{3.5}$$

where D_{S1} is a duty cycle for the transistor S_1. The converter works in two states: active state corresponds to conduct switch S_1 and zero state, where S_2 is conducting.

Otherwise, if the input voltage is smaller than the output instantaneous value of the output voltage v_{OUT}, the boost mode will be chosen. During boost mode transistor S_1 is conducting, complementary switches S_3 and S_4 are responsible for boost function:

$$v_{OUT} = \frac{v_{IN}}{1 - D_{S3}}, \tag{3.6}$$

where D_{S3} is duty cycle of the switch S_3. Therefore, the buck or boost functionality is selected based on the ratio between the input and output levels.

The second topology is the twisted buck-boost inverter based on the unfolding circuit, which is shown in Fig. *3.1b.* The details regarding a twisted inverter based on the unfolding circuit are presented in [PAPER-V].The operational principle of this converter is slightly different to the first topology. The main difference is the number of switches and one operational mode. The converter works only with a buck-boost mode and does not require tracking the ratio between input and output voltages. The twisted inverter is based on the conventional buck-boost dc-dc converter with known gain factor:

$$v_{OUT} = \frac{D_{S1}}{1 - D_{S1}} \cdot v_{IN} . \tag{3.7}$$

Switch S_1 is responsible for generating necessary value of the output voltage, while S_2 can be replaced by a diode for unidirectional power flow. The unfolding circuit is realized by transistors S_3-S_6 with low switching frequency.

A significant number of the semiconductors does not cause a significant switching loss, because only two transistors are switching in any operation point. The common mode voltage of any of these solutions does not have high-switching harmonic, as a result small size of the common mode filter is required.

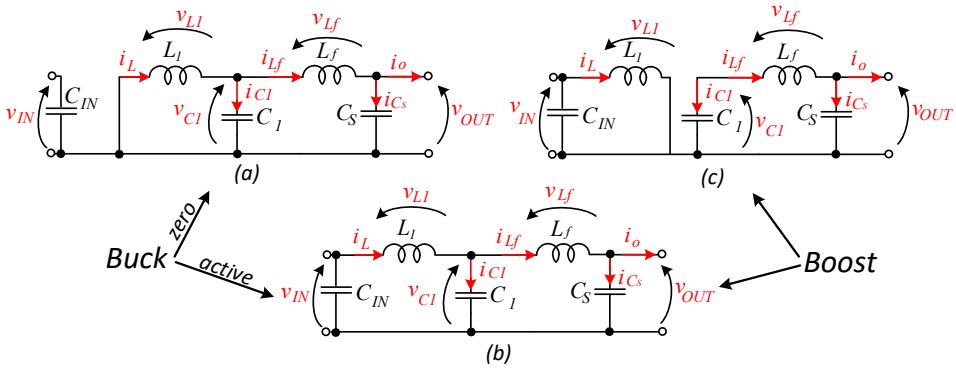


Figure 3.2 Equivalent circuits of buck-boost inverter based on unfolding circuit: buck mode (a)-(b), boost mode (b)-(c).

Then the buck-boost inverter based on the unfolding circuit operates in buck mode, and two states are used: active and zero. The equivalent circuits of the buck operation are shown in Figs. *3.2a* and *3.2b.* Two LC-filters provide small ripples at the output side during buck mode. Figs. *3.2b* and *3.2c* show the equivalent circuits of the boost mode. The purpose of the boost case is to store energy in the input coil and to transfer accumulated energy immediately to the load via the CLC-filter.

As a first action, the Kirchhoff rules should be considered to obtain the basic equations of each equivalent circuit:

$$\begin{cases} v_{L1} = v_{IN} - v_{C1} \\ i_{C1} = i_L - i_{Lf} \\ v_{Lf} = v_{IN} - v_{L1} - v_{OUT} \\ i_{Cs} = i_{Lf} - i_o \end{cases}_{Fig.\ 3.2a}, \quad \begin{cases} v_{L1} = -v_{C1} \\ i_{C1} = i_L - i_{Lf} \\ v_{Lf} = -v_{L1} - v_{OUT} \\ i_{Cs} = i_{Lf} - i_o \end{cases}_{Fig.\ 3.2b}, \tag{3.8}$$

where v_{L1} is the voltage on the input inductance, v_{Lf} is the voltage across the output inductor, i_{C1} is the current of the unfolding circuit capacitor, i_{Cs} is the current of the output capacitor, v_{IN} is the input voltage, v_{OUT} is the output voltage.

Fig. *3.3* shows the waveforms of the inductor currents and the voltages across the capacitors. A singularity of the buck mode is that all high-switching pulsations depend on the ripple of the input inductor current. Furthermore, the pulsation of the unfolding capacitor voltage depends on the current of the output inductor. The ripples of inductor L_f current depend on the capacitor voltages. Finally, the output capacitor fluctuation depends on the output inductor current. Thus, the filled areas of calculation in Fig. *3.3* are needed to obtain each high-frequency ripple:

$$L_1 \Delta i_L = DT_S \cdot v_{IN} - \int_0^{DT_S} \left[v_{C1}(t) \right] dt \,, \; L_f \Delta i_{Lf} = \int_0^{DT_S} \left[v_{C1}(t) - v_{Cs}(t) \right] dt \,, \tag{3.9}$$

$$C_1 \Delta v_{C1} = \int_{\frac{DT_S}{2}}^{DT_S} \left[i_L(t) - i_{Lf}(t) \right] dt + \int_0^{\frac{D'T_S}{2}} \left[i'_L(t) - i'_{Lf}(t) \right] dt \,, \tag{3.10}$$

$$C_s \Delta v_{Cs} = \int_{-\frac{DT_S}{2}}^{\frac{DT_S}{2}} \left[i_{Lf}(t) \right] dt + \int_{0}^{\frac{D'T_S}{2}} \left[i'_{Lf}(t) \right] dt , \qquad (3.11)$$

where Δi_L is a high-frequency ripple of the input inductor current, T_S equals the PWM period, D is a duty cycle, D' is an inverted duty cycle and equals 1-D, Δv_{C1} is a high-frequency ripple of the unfolding circuit voltage (across capacitor C_1), Δi_{Lf} is a ripple of the grid inductance current, L_1, L_f, C_1, C_s are nominal values of the passive elements.

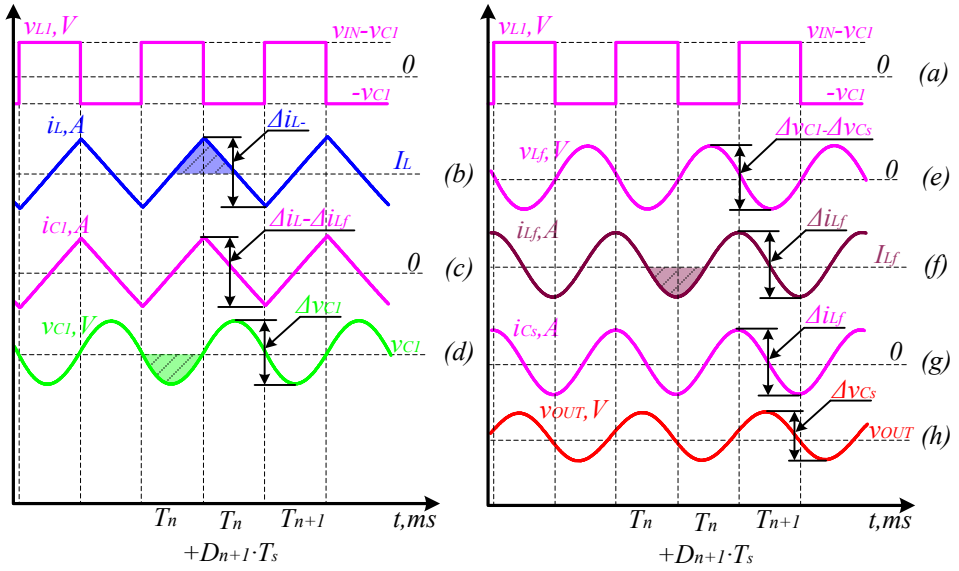


Figure 3.3 High-frequency waveforms of ripples in the passive components: a voltage across the input inductor L_1 (a), a triangular input inductor current (b), capacitor current i_{C1} (c), 2nd order shape voltage of the unfolding capacitor C_1 (d), the voltage across output inductance Lf (e), 3d order shape of the output inductor current (f), the output capacitor current (g), 4th order shape of the output voltage (h).

The ripple of the input inductor current is a triangular waveform (Fig. *3.3b*). The inductor current depends on the high-frequency ripple and the steady state value:

$$i_L(t) = \frac{\Delta i_L \cdot t}{D \cdot T_S} - \frac{\Delta i_L}{2} + i_o , \; i'_L(t) = \frac{\Delta i_L \cdot t}{D' \cdot T_S} + \frac{\Delta i_L}{2} + i_o . \qquad (3.12)$$

As mentioned, the buck mode has two LC-filters; they are working continuously during the buck mode. Therefore, the capacitor of the first LC-filter has the second order high-frequency pulsation. It corresponds to a parabola shape, as shown in Fig. *3.3d*. The voltage expression of the capacitor C_1 during active state is as follows:

$$v_{C1}(t) = \frac{2 \cdot \Delta v_{C1} \cdot t^2}{(D \cdot T_S)^2} - \frac{2 \cdot \Delta v_{C1} \cdot t}{D \cdot T_S} + v_{OUT} . \qquad (3.13)$$

The grid inductance current has the third order shape of ripple (Fig. *3.3f*). The equations of the inductor current with an active and a zero state are shown below:

$$i_{Lf}(t)=\frac{2\Delta i_{Lf}\cdot t^3}{(D\cdot T_S)^3}-\frac{3\Delta i_{Lf}\cdot t^2}{(D\cdot T_S)^2}+\frac{\Delta i_{Lf}}{2}+i_o\,, \tag{3.14}$$

$$i'_{Lf}(t)=\frac{2\Delta i_{Lf}\cdot t^3}{(D'\cdot T_S)^3}+\frac{3\Delta i_{Lf}\cdot t^2}{(D'\cdot T_S)^2}-\frac{\Delta i_{Lf}}{2}+i_o\,. \tag{3.15}$$

The voltage across the grid capacitor has the fourth order shape pulsation (Fig. *3.3h*), which depends on the steady state value and the pulsations across the grid capacitor in the active state:

$$v_{Cs}(t)=\frac{8\Delta v_{Cs}\cdot t^4}{5(D\cdot T_S)^4}-\frac{16\Delta v_{Cs}\cdot t^3}{5(D\cdot T_S)^3}+\frac{8\Delta v_{Cs}\cdot t}{5D\cdot T_S}+v_{OUT}\,. \tag{3.16}$$

Based on eq. (3.8)-(3.16) it is possible to obtain a linear system with 4 unknown variables. These unknown variables are ripples in passive components and the mathematical system has the following format:

$$\begin{cases}\Delta i_L=\dfrac{(v_{IN}-v_{OUT})\cdot v_{IN}}{L_1\cdot v_{OUT}\cdot f},\Delta i_{Lf}=\dfrac{(\Delta v_C+\Delta v_{Cs})\cdot v_{OUT}}{3\cdot L_f\cdot v_{IN}\cdot f}\\ \Delta v_{C1}=\dfrac{4\cdot\Delta i_L+5\cdot\Delta i_{Lf}}{32\cdot C_1\cdot f},\Delta v_{Cs}=\dfrac{5\cdot\Delta i_{Lf}}{32\cdot C_s\cdot f}\end{cases}, \tag{3.17}$$

where f is the PWM frequency. Solving of the system (3.17) gives the equations of the ripple in each passive component.

Table 3.2 Expressions of passive components and duty cycle for buck and boost modes.

Topology	Buck-boost inverter based on unfolding circuit (Fig. *3.1a*)		Twisted buck-boost inverter based on unfolding circuit (Fig. *3.1b*)
Mode	Buck	Boost	Buck-Boost
Duty cycle	$\frlvert v_{REF}\frrvert / v_{IN}$	$\frlvert v_{REF}\frrvert - v_{IN} / \frlvert v_{REF}\frrvert$	$\frlvert v_{REF}\frrvert / \frlvert v_{REF}\frrvert + v_{IN}$
Inductance L_1	$\frac{v_{OUT}\cdot V_M\cdot(v_{IN}-v_{OUT})}{2\cdot K_L\cdot P\cdot v_{IN}\cdot f}$	$\frac{v_{IN}^2\cdot(v_{OUT}-v_{IN})}{2\cdot K_L\cdot P\cdot v_{OUT}\cdot f}$	$\frac{v_{OUT}\cdot V_M\cdot v_{IN}^2}{2\cdot K_L\cdot P\cdot(v_{OUT}+v_{IN})\cdot(V_M+v_{IN})\cdot f}$
Inductance L_f	$\frac{v_{OUT}\cdot V_M^2\cdot(K_C+K_{Cs})}{6\cdot K_{Lf}\cdot P\cdot v_{IN}\cdot f}$	$\frac{V_M^2\cdot(4\cdot K_C+5\cdot K_{Cs})}{64\cdot K_{Lf}\cdot P\cdot f}$	$\frac{V_M^2\cdot(4\cdot K_C+5\cdot K_{Cs})}{64\cdot K_{Lf}\cdot P\cdot f}$
Capacitor C_1	$\frac{P\cdot(4\cdot K_L+5\cdot K_{Lf})}{16\cdot K_C\cdot V_M^2\cdot f}$	$\frac{2\cdot P\cdot(v_{OUT}-v_{IN})}{K_C\cdot V_M\cdot v_{OUT}^2\cdot f}$	$\frac{2\cdot P\cdot v_{OUT}^2}{K_C\cdot V_M^3(v_{OUT}+v_{IN})\cdot f}$
Capacitor C_s	$\frac{5\cdot K_{Lf}\cdot P}{16\cdot K_{Cs}\cdot V_M^2\cdot f}$	$\frac{2\cdot P\cdot K_{Lf}\cdot(v_{OUT}-v_{IN})}{3\cdot K_{Cs}\cdot V_M^2\cdot v_{OUT}\cdot f}$	$\frac{2\cdot P\cdot K_{Lf}\cdot v_{OUT}}{3\cdot K_{Cs}\cdot V_M^2(v_{OUT}+v_{IN})\cdot f}$
Point of maximum	$v_{OUT}=v_{IN}/2$	$v_{OUT}=V_M$	$v_{OUT}=V_M$

Usually, the ripple factor is used for the calculation of the passive elements:

$$K_L=\Delta i_L/I_{LMAX}\,,\ K_{Lf}=\Delta i_{Lf}/I_{LfMAX}\,, \tag{3.18}$$

$$K_C = \Delta v_{C1} / V_{C1MAX}\ ,\ K_{Cs} = \Delta v_{Cs} / V_{CsMAX}\ , \tag{3.19}$$

where I_{LMAX}, I_{LfMAX} are the maximum current values in inductances, V_{C1MAX}, V_{CsMAX} are the peaks of the capacitor voltages.

The next step of the calculation is to find the maximum ripple during the grid period because each expression depends on the phase of the output voltage. Taking the derivative reveals the maximum of the ripple.

Tables *3.2* and *3.3* contain the expressions with the values of passive components for the considered family of topologies. The maximum pulsation in the buck mode corresponds the point when the output voltage equals half of the input voltage. The point of maximum of the twisted buck-boost inverter coincides with boost mode points in another topology. The presented calculation approach allows to obtain values of the passive components with the predefined ripples.

Table 3.3 Values of passive components as a function of converter parameters.

Topology	Conventional VSI with boost cell (Fig. *2.2a*)		Phase-integrated solution based on buck-boost cell (Fig. *2.2b*) $v_{AN} = \left(v_{OUT} + V_M\right)/2$	
Mode	Buck	Boost	Buck	Boost
Inductance L_1	$\frac{v_{IN}^2 \cdot K_C}{16 \cdot K_L \cdot P \cdot f}$	$\frac{v_{IN}^2 \cdot \left(v_{OUT} - v_{IN}\right)}{2 \cdot K_L \cdot P \cdot v_{OUT} \cdot f}$	$\frac{v_{AN} \cdot V_M \cdot \left(v_{IN} - v_{AN}\right)}{2 \cdot K_L \cdot P \cdot v_{IN} \cdot f}$	$\frac{v_{IN}^2 \cdot \left(v_{AN} - v_{IN}\right)}{2 \cdot K_L \cdot P \cdot v_{AN} \cdot f}$
Inductance L_f (L_{f1}, L_{f2})	$\frac{V_M \cdot v_{OUT} \cdot \left(v_{IN} - v_{OUT}\right)}{4 \cdot K_{Lf} \cdot P \cdot v_{IN} \cdot f}$	$\frac{V_M^2 \cdot \left(4 \cdot K_C + 5 \cdot K_{Cs}\right)}{64 \cdot K_{Lf} \cdot P \cdot f}$	$\frac{v_{AN} \cdot V_M^2 \cdot \left(K_C + K_{Cs}\right)}{6 \cdot K_{Lf} \cdot P \cdot v_{IN} \cdot f}$	$\frac{V_M^2 \cdot \left(4 \cdot K_C + 5 \cdot K_{Cs}\right)}{64 \cdot K_{Lf} \cdot P \cdot f}$
`Capacitor C_1	$\frac{2 \cdot P \cdot \left(v_{IN} - v_{OUT}\right)}{K_C \cdot v_{IN}^3 \cdot f}$	$\frac{2 \cdot P \cdot \left(v_{OUT} - v_{IN}\right)}{K_C \cdot V_M \cdot v_{OUT}^2 \cdot f}$	$\frac{P \cdot \left(4 \cdot K_L + 5 \cdot K_{Lf}\right)}{16 \cdot K_C \cdot V_M^2 \cdot f}$	$\frac{2 \cdot P \cdot \left(v_{AN} - v_{IN}\right)}{K_C \cdot V_M \cdot v_{AN}^2 \cdot f}$
Capacitor C_S	$\frac{P \cdot K_{Lg}}{4 \cdot K_{Cg} \cdot V_M^2 \cdot f}$	$\frac{2 \cdot P \cdot K_{Lg} \cdot \left(v_{OUT} - v_{IN}\right)}{3 \cdot KCg \cdot V_M^2 \cdot v_{OUT} \cdot f}$	$\frac{5 \cdot K_{Lf} \cdot P}{32 \cdot K_{Cs} \cdot V_M^2 \cdot f}$	$\frac{P \cdot K_{Lf} \cdot \left(v_{AN} - v_{IN}\right)}{3 \cdot K_{Cs} \cdot V_M^2 \cdot v_{AN} \cdot f}$
Point of maximum	$v_{OUT} = v_{IN}/2$	$v_{OUT} = V_M$	$v_{OUT} = v_{IN}/2$	$v_{OUT} = V_M$

Table 3.4 Current and voltage stress across passive components as a function of converter parameters.

Topology	Buck-boost inverter based on unfolding circuit (Fig. *3.1a*)		Twisted buck-boost inverter based on unfolding circuit (Fig. 3.*1b*)	Conventional VSI with boost cell (Fig. *2.2a*)		Phase-integrated solution based on buck-boost cell (Fig. *2.2b*)	
Mode	Buck	Boost	Buck-boost	Buck	Boost	Buck	Boost
Maximum current Inductance L_1	$\frac{2 \cdot P}{V_M}$	$\frac{2 \cdot P}{v_{IN}}$	$\frac{2 \cdot P}{v_{IN}} + \frac{2 \cdot P}{V_M}$	$\frac{2 \cdot P}{v_{IN}}$		$\frac{2 \cdot P}{V_M}$	$\frac{2 \cdot P}{V_M}$
Maximum current Inductance L_f (L_{f1}, L_{f2})	$\frac{2 \cdot P}{V_M}$						
Maximum voltage Capacitor C_1, Cs	V_M						
Total voltage stress across high-switching transistors	$2 \cdot V_M + 2 \cdot V_{IN}$		$2 \cdot V_M + 2 \cdot V_{IN}$	$4 \cdot V_M$		$4 \cdot V_M + 4 \cdot V_{IN}$	
Total voltage stress across low-switching transistors	$4 \cdot V_M$		$4 \cdot V_M$	$2 \cdot V_M$		0	

In advance, Table 3.4 shows the current and voltage stress across passive components as a function of converter parameters for all compared topologies. It will be used for further comparative evaluation. Equations contain input power P, maximum output voltage V_M and input voltage v_{IN} and output voltage v_{OUT}. The output voltage corresponds to the general case of ac and dc modes. If the dc mode is considered, this value is equal to the maximum output voltage V_M, while in ac mode it is the absolute value of sinusoidal voltage waveform.

Output filter (L_f) in the case of buck operation of BVSI is calculated according to the classical approach that takes into account the THD of the output current rated for 75% of maximum output power. This design approach does not differ from any other conventional inverter. It includes V_{INV} output high-frequency component of the inverter voltage before filter.

3.2 Verification of the Filter Design

3.2.1 Special Modulation Techniques

Several modulation techniques can be used for the proposed topologies. In general, the modulation method can lead to different conduction and switching loss, computational time, and quality of the output current and voltage. During calculation of the duty cycle for an open-loop system some reference signal such as v_{REF} should be used. Basically, the reference signal corresponds to the expected output voltage. In the case of a grid connected closed-loop system the control block uses MPC for a generating reference signal. It is possible to highlight two main cases: the input voltage is less than the amplitude of the reference voltage v_{REF} and when the input voltage is higher than the

peak of v_{REF}. In the first case, the converter will operate in buck and boost mode, depending on the comparison between input voltage and instantaneous reference value, as shown in Fig. 3.*4a*. If input voltage is higher than the reference signal, the buck mode with buck duty cycle is chosen:

$$D_{BUCK} = \frac{|v_{REF}|}{v_{IN}}. \tag{3.20}$$

where reference signal v_{REF} is taken as absolute value because the output side is kept as positive for the input side during a negative half cycle.
Otherwise, the converter will enter boost mode with a corresponding duty cycle:

$$D_{BOOST} = \frac{|v_{REF}| - v_{IN}}{|v_{REF}|}. \tag{3.21}$$

where D_{BOOST} is a duty cycle of the switch S_3, while the main buck switch S_1 is always turned on.

These duty cycles are compared with high-frequency carrier signals to generate gate signals for each corresponding switch. At the same time, the unfolding signals can be derived by comparing the reference signal v_{REF} with zero. The frequency of the unfolding circuit is the same as industrial grid frequency and equals 50 Hz. Fig. 3.*4b* shows the principle of signal generation for buck, boost and unfolding circuit switches. This case corresponds to a situation where the input voltage is lower than a peak of the reference signal. The modulation technique discussed is valid for a buck-boost inverter based on the unfolding circuit.

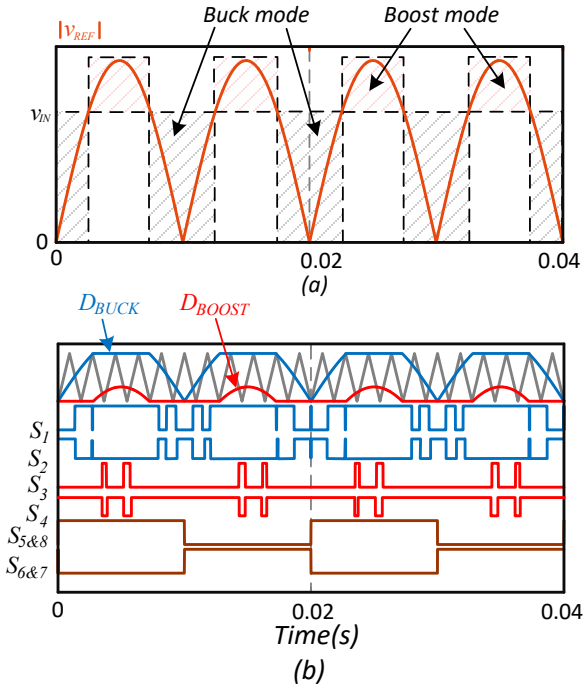


Figure 3.4 Switching signals generation for the buck-boost inverter based on unfolding: the case when v_{IN} is lower than the peak value of v_{REF} (a) and PWM signals of each transistor (b).

The same approach is used for a twisted buck-boost inverter based on the unfolding circuit, but this circuit only works with one operational mode for the buck and boost feature. This regime can be called the buck-boost mode.

The duty cycle similarly depends on the absolute value of the reference signal, and is calculated as follows:

$$D_{BB} = \frac{|v_{REF}|}{|v_{REF}| + v_{IN}}, \tag{3.22}$$

where D_{BB} represents the duty cycle of buck-boost mode for switch S_1. The unfolding signals are generated in the same way as in the first circuit. Fig *3.5* shows the principle of signal generation for the twisted buck-boost inverter based on the unfolding circuit. If apply duty cycle more than 0.5 the boost mode will be chosen, otherwise the system will work in buck mode.

Fig. *3.6a* describes the operation principle of the conventional solution for universal PV application. A non-conventional modulation approach is considered for implementation. In some research studies it was called a time-sharing dual mode control scheme [53], [54]. A very similar control approach is called cooperative control [55]. The shape of the voltage across capacitor C_1 follows the modulation voltage in the boost mode. In this case only boost transistors are working in the high-switching mode, while VSI transistors perform an unfolding function.

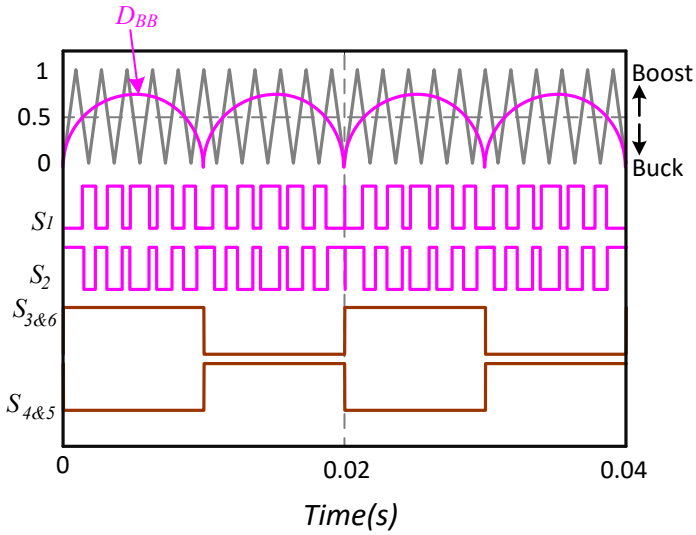


Figure 3.5 Switching signals generation for twisted buck-boost inverter based on the unfolding inverter in a case when v_{IN} is lower than the peak value of reference signal.

Figs. *3.6b* and *3.6c* illustrate the concept of universal applicability of the Phase-Modular Converter (PMC). In the first case, internal commutators (switches) SW_1-SW_3 are configured to provide sinusoidal output voltage (Fig. *3.6b*). SW_{12} is conducting, while other commutators are switched off. In the second case, the commutators (switches) SW_1 and SW_3 are conducting, which leads to the connections of the positive output's terminals of each cell providing only the dc component. The interleaved mode that is activated in this case reduces the output and input current ripple.

A simple open-loop system was chosen as verification. The values of the ripple factors should be such that they avoid discontinuous current mode in inductances. For example, the ripple factor of input inductance was set at 20%. The unfolding voltage factor was also 20%, while only 5% was set for the output LC-filter ripple factors. The output inductance ripple factor is 10%. The lower power causes significant current pulsations in the inductances, which is why it was decided to calculate passive elements under 1 kW. Moreover, the highest possible boost according to announced voltage range is 3.2. If the minimum input voltage equals 100 V, the maximum possible input power is 1 kW.

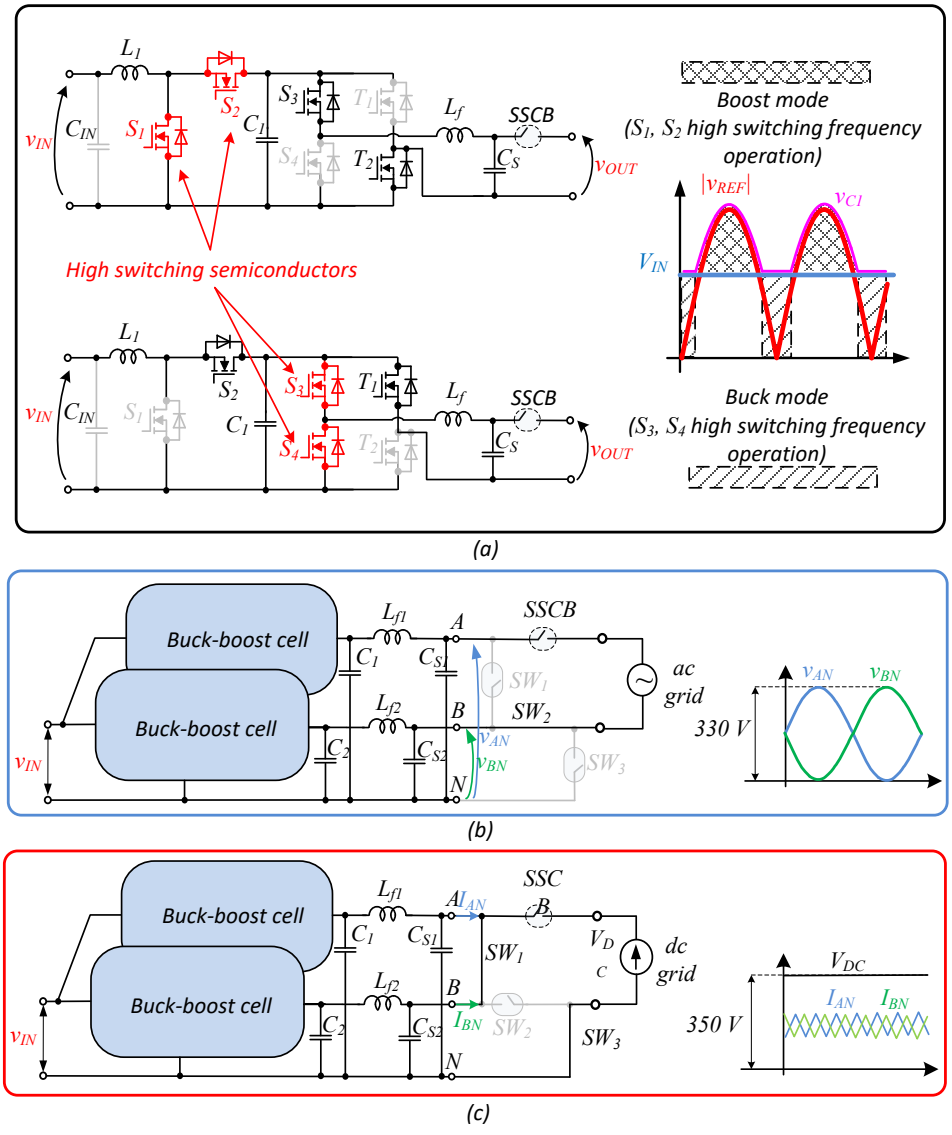


Figure 3.6 General operation illustration of the operation principle: boost and buck operations for conventional inverter with boost cell(a), phase-integrated solution based on buck-boost cell (b), dc-dc mode interleaved buck-boost cells (c).

Fig. *3.7* shows the simulation results from a software tool, PowerSim. The buck mode is shown in Figs. *3.7a, 3.7b* and *3.7c.* The input voltage was 500 V, and the output voltage was a traditional grid shape, which equalled 220 V of Root Mean Square (RMS). Based on the simulation results, it was found that the theoretical statements are only right in the phase of the maximum ripple, because a combination of two LC-filters or one CLC-filter with a resistance load causes phase shifting between currents and voltages. As the peak of the output voltage is 320 V, the phase of maximum ripple is 51 degrees in the buck mode. The unfolding capacitor ripple, which equals 21.1%. The ripple factor of the inductance L_1 is 21.1% when the output inductance factor is 9.8 %. The output ripple factor is 4.3%.

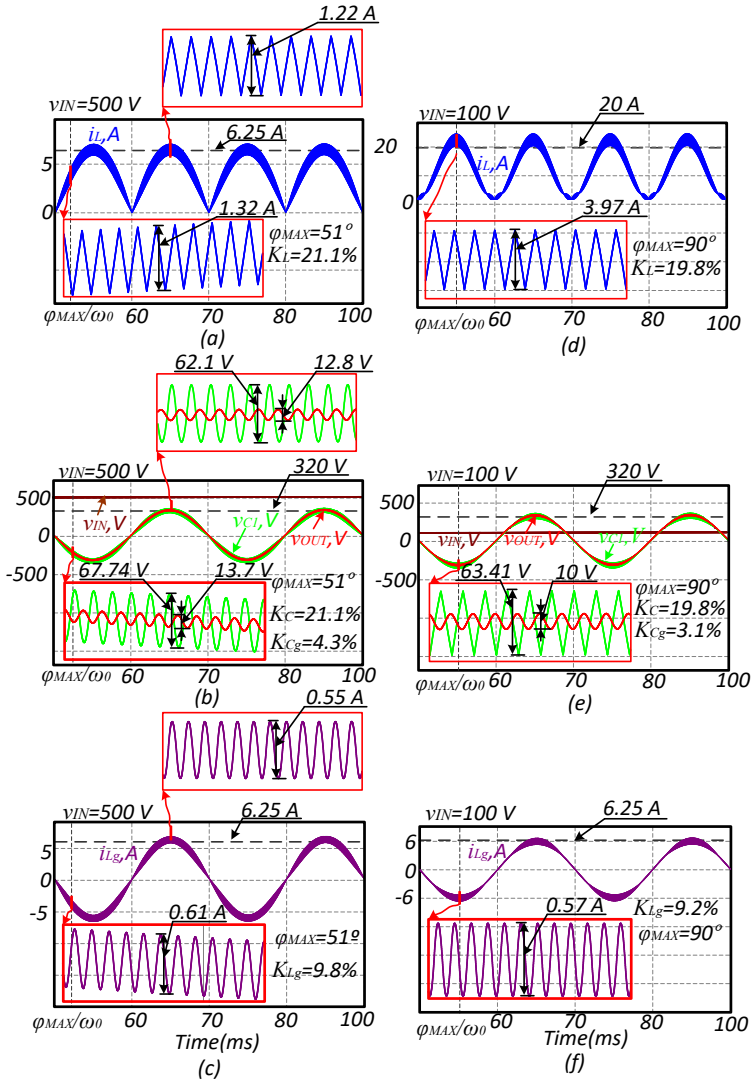


Figure 3.7 Simulation verification of the component design for the buck-boost inverter based on the unfolding circuit: the inductor current within 500 V of the input voltage (a), capacitor voltages in the buck case (b), the grid inductor current in buck case (c), the inductor current in the buck-boost case (d), the output voltage along with the capacitor voltage under 100 V of the input voltage (e), the grid inductor current in buck-boost case (f).

Figs. *3.7d*, *3.7e* and *3.7f* correspond to the boost mode when the input voltage is 100 V. The point of the maximum ripple matches the peak of ac voltage and equals 90 degrees. The maximum input ripple factor is 19.8%. The voltage factors are 19.8% and 3.1%. The output inductor pulsation equals 9.2% while the theoretical factor is 10%. As a result, the simulation results show a precise conformation the theoretical calculation. The maximum discrepancy with a setpoint ripple factor is 1.9% in the output voltage.

3.2.2 Comparative Evaluations

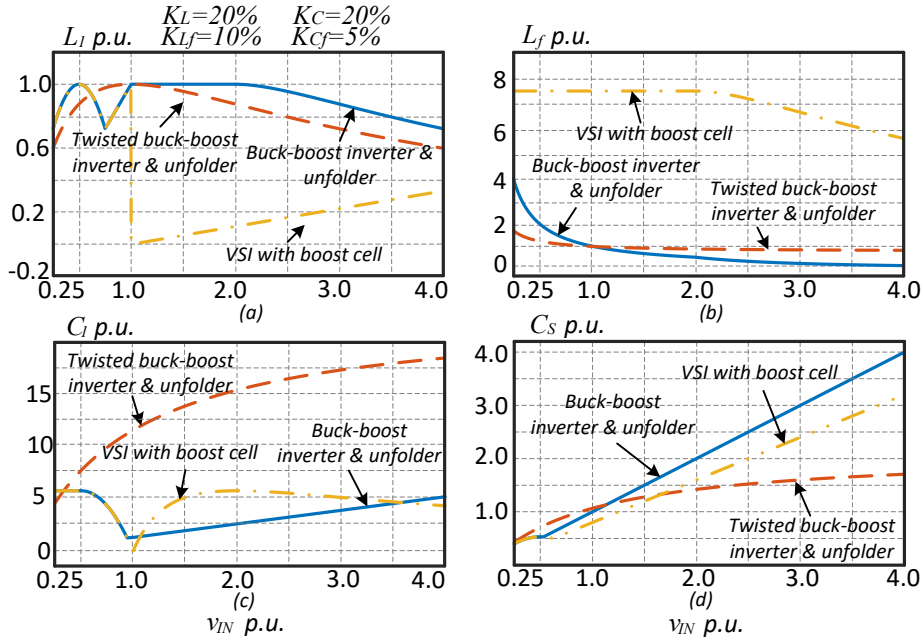


Figure 3.8 Calculation results of normalized passive elements in a range from boost 4 to buck 4: the input inductance values L_1 (a), dependence of the grid inductance L_f (b), the unfolding capacitor C_1 (c), and the grid capacitance C_S (d).

Fig. *3.8* shows a comparison of passive elements for all topologies under a constant input current instead of a phase-integrated solution based on buck-boost cell. All passive components were designed according to the biggest ripple. Each parameter is normalized to the value of a single buck ratio (v_{IN} p.u.= 1). The comparison considers a range from 4 boost to 4 buck ratios between the input voltage and the output peak. The x axis contains the input voltage, which is normalized on the peak of the output voltage. All theoretical ripples were the same as considered during the verification. Fig. *3.8a* shows the comparison of the inductance L_1. If we pay attention to all input voltage ranges, the inductance should be selected with the same value for all topologies. The capacitor C_1 should be chosen higher in the twisted buck-boost inverter based on the unfolding circuit, as shown in Fig. *3.8b*. Conventional VSI with boost cell requires a bigger nominal value for the inductor L_f, as demonstrated in Fig. *3.8c*. Finally, the single buck-boost inverter based on the unfolding circuit needs the highest value of the grid capacitor C_S (Fig. *3.8d*).

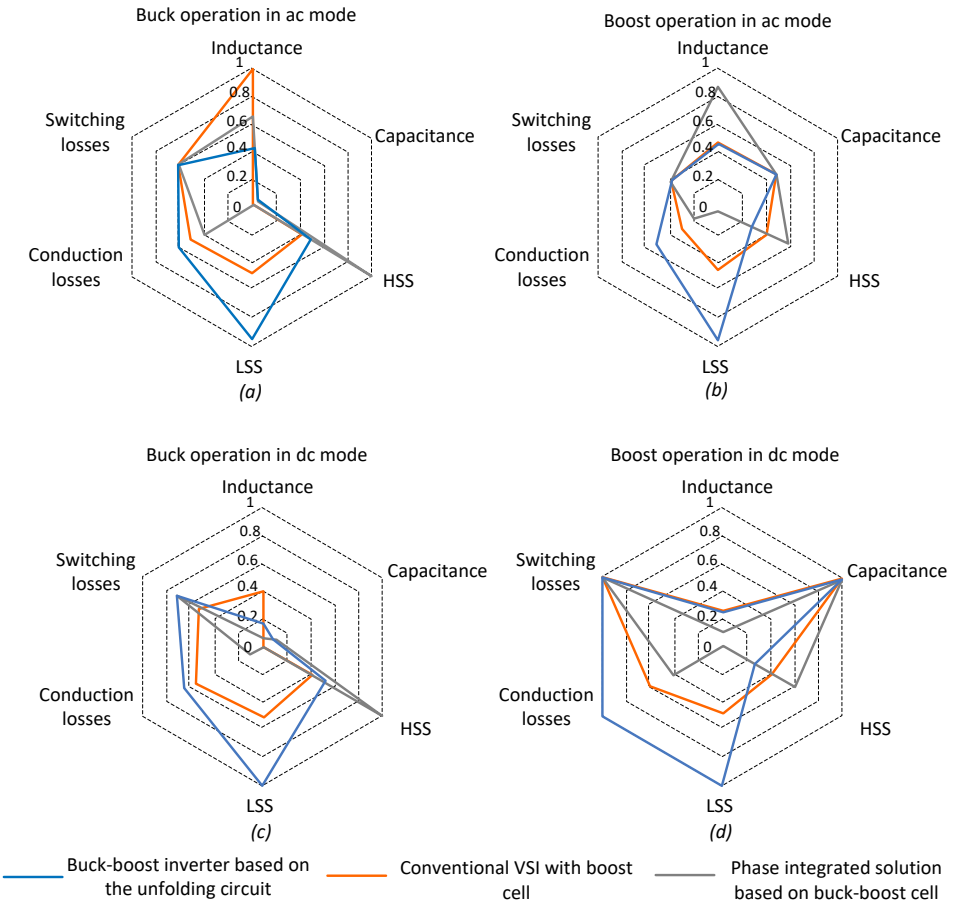


Figure 3.9 Comparative spider diagrams: buck operation in ac mode (a), Boost operation in ac mode (b), Buck operation in dc mode (c), Boost operation in dc mode (d).

Fig. *3.9* shows a comparison of the results between three topologies: buck-boost inverter based on the unfolding circuit, conventional VSI with boost cell and a phase-integrated solution based on buck-boost cell. Capacitance energy is approximately the same in all topologies. However, the buck-boost inverter based on the unfolding circuit has lower inductance energy. The maximum voltage stress across high-frequency switches is the phase-integrated solution based on the buck-boost cell, while other solutions have approximately the same lower values. Of course, the maximum stress on low-frequency switches is found in the first solution, because it has an unfolding circuit. The conventional VSI with boost cell is the better solution in terms of switching and conduction losses in comparison with other solutions. However, modern semiconductors on the market allow the possibility to significantly decrease power losses. That is why the buck-boost inverter based on the unfolding circuit can be considered the best solution for a universal concept for residential ac and dc grid application.

As a result, the final values of the passive elements were chosen. Table 3.5 contains the parameters of the passive elements and a model of switches for buck-boost inverter based on the unfolding circuit. The values of inductors were chosen for 1 kW input power

for the buck case. The capacitor values were selected from the boost case. As unfolding circuit switches are low-frequency switches and do not generate switching losses, the switches should have a good drain source resistance but bad dynamic characteristics.

Table 3.5 Components used for further simulations and experimental setup.

Topology	Buck-boost inverter based on unfolding circuit	Twisted buck-boost inverter based on unfolding circuit
Inductance L_1, L_2	1.6 mH	1.6 mH
Inductance L_f (L_{f1}, L_{f2})	0.33 mH	0.68 mH
Capacitor C_1 (C_2)	1.3 µF	1 µF
Capacitor C_S (C_{S1}, C_{S2})	1 µF	1 µF

Research project [PAPER-IV] studies the interleaved features of the buck-boost inverter based on the unfolding circuit. The interleaved buck-boost inverter means using several buck-boost cells in parallel and a common unfolding circuit. As a result, the optimal number is two buck-boost cells, because with the second case the efficiency goes up, despite the cost. The third buck-boost cell will lead to a significant cost increase, but the efficiency does not go up significantly.

3.3 Summary

Several solutions were selected as a universal converter that is applicable for the ac and dc grid. A comparative analysis based on several criteria was performed for choosing the most suitable solution. One of the main parameters is a volume of the passive elements that corresponds to energies in passive components. SSA allows to get a maximum high-frequency ripple in each component. The buck-boost inverter based on the unfolding circuit was chosen as an optimal solution for a universal converter.

4 Model Predictive Control as a Feasible Solution for Industrial Application

Many circuits in power electronics use different existing techniques for control. The integral-based techniques are used in most cases for power electronic converters. For example, a Proportional Resonant (PR) controller provides high quality of the grid current [57], [58], [59]. Usually, a PR controller is the base for an inverter control system. Despite fundamental harmonics, the PR block can suppress unnecessary frequency of the grid current. On the other hand, to avoid additional harmonics a combination of different techniques can be applied in a single system [60]. Integrated control techniques eliminate the steady-state error [61]. Such methods work slowly and do not require a high sample rate. Delay is also an issue for the integral methods. The repetitive controller (RC) is one of the solutions to overcome the delay problems [62]. Another issue of integral methods is zero-crossing distortions under low input power, especially in unfolding circuit-based inverters. Fig. *4.1* shows the zero crossing distortions of the grid current. However, the integral control techniques do not provide high accuracy during a wide range of the input power.

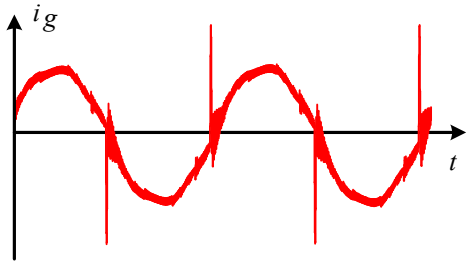


Figure 4.1 Zero-crossing distortion of the grid current in a twisted buck–boost inverter with unfolding circuit based a PR controller.

Another possible solution is a non-linear method, Model Predictive Control (MPC), which has become a popular algorithm in power electronics [63]. The MPC can be classified as a continuous control set (CCS-MPC) or as a finite control set (FCS-MPC) type. The continuous control MPC has a fixed switching frequency with modulator, while the FCS-MPC allows online optimisation and has a variable frequency. FCS-MPC requires a faster control unit, as shown in [64]. MPC solves several issues of the integral methods. The MPC cost function observes different parameters, such as power, voltage, current, and duty cycle. The MPC selects the exact variant of the suitable current value, which consequently improves accuracy.

4.1 MPC for Twisted Buck-Boost Inverter Based on the Unfolding Circuit

The initial idea of the MPC strategy for inverters based on the unfolding circuit was presented in [65]. This chapter describes the implementation of CCS-MPC control block for a grid-connected twisted buck-boost inverter with the unfolding circuit. One of the main purposes is to reduce a zero-crossing distortion by using the MPC. Fig. *4.2a* shows the functional structure of the control system with a pulse width modulator. Fig. *4.2b* presents the general block diagram of the different gate signals by calculating the duty cycles. The MPC is a certain block of the control system. An indirect CCS-MPC permits

calculation of the high-frequency ripple in the passive elements. High frequency sampling increases stability, because each PWM period is considered. However, the accuracy can be reduced because of limited opportunities for changing the power signals.

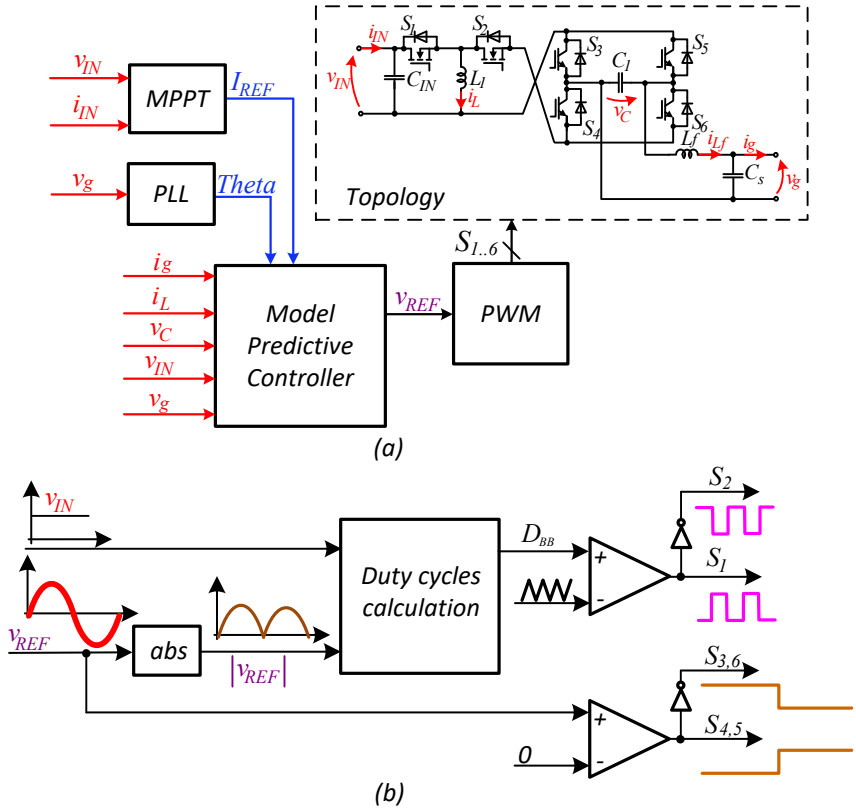


Figure 4.2 Structure of the control system based on MPC (a), Modulator structure for the twisted inverter based on the unfolding circuit (b).

The sample frequency is the same as the PWM frequency. The measurement delay is one cycle of the PWM. Accordingly, the system should also calculate power states during the previous period. The CCS-MPC provides control of the low-frequency unfolding circuit. The unfolding part signals are changed with regard to the sign of the predictive output capacitor voltage.

Fig. *4.3* shows the shapes of the power states due to the switching of the main buck-boost transistor S_1 [See Fig. *3.1b*]. Regarding the signal shapes, some simplifications can be applied. The high-frequency ripple of the input inductor current has a triangular view as the output capacitor voltage. However, the shape of the grid current is a nonlinear signal. Thus, it is not easy to calculate values of the grid current for the next period of the PWM. The instant power signals create a shift for the higher harmonic of the grid current.

The computational time is an important parameter when the MPC is used as a control block. Usually, the integral techniques calculate reference voltage faster than the MPC [66]. Thus, systems that provide an MPC with high horizon require expensive chips with a high computational burden [67]. As a possible option, the parallel working of DSP within FPGA chips allows to decrease the computational time of the MPC [68].

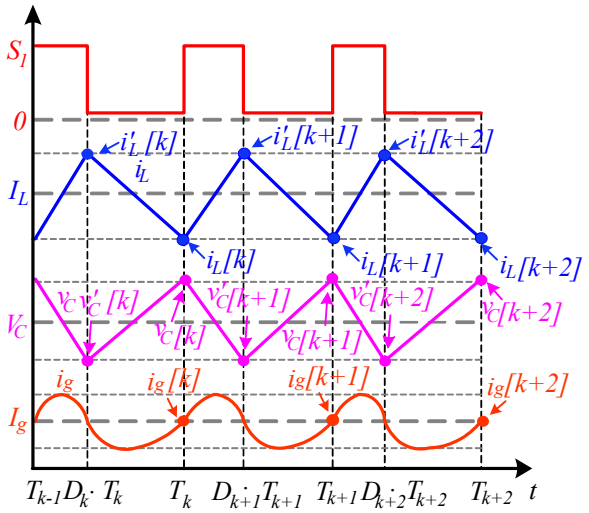


Figure 4.3 High-frequency waveforms of the states.

Fig. *4.4a* shows the equivalent circuit that relates to the input energy storage. Fig. *4.4b* depicts the second equivalent circuit, where the storage energy transfers to the grid. The resistances of inductances and switches were considered in the calculation. The voltage of the input capacitor C_{IN} was equal to the input voltage, therefore input capacitor was ignored during the calculation. The differential equations were obtained for each equivalent circuit.

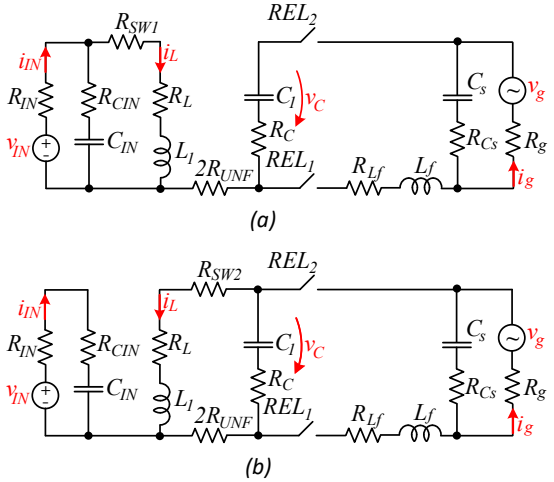


Figure 4.4 Equivalent circuits: The first state when the input inductor is accumulating the input energy (a), the case of the storage energy transferring to the grid (b).

The equation for the first equivalent circuit is as follows:

$$L_1 \cdot \frac{di_L(t)}{dt} = v_{IN}(t) - i_L(t) \cdot (R_{IN} + R_{SW1} + R_L), \tag{4.1}$$

$$L_f \cdot \frac{di_g(t)}{dt} = v_C(t) - v_g(t) - i_g(t) \cdot (R_g + R_{Lf}),\ C_1 \cdot \frac{dv_C(t)}{dt} = -i_g(t), \tag{4.2}$$

where R_L is the input inductor resistance, R_{IN} is the input side resistor, R_{SW1} is the resistance of the switch S_1, C_1 is the unfolding circuit capacitor, L_1 is the input inductance. The second equivalent circuit is the third order equation. The differential equations are the following:

$$L_1 \cdot \frac{di_L(t)}{dt} = v_C(t) - i_L(t) \cdot (2 \cdot R_{UNFOLD} + R_{SW2} + R_L), \tag{4.3}$$

$$L_f \cdot \frac{di_g(t)}{dt} = v_C(t) - v_g(t) - i_g(t) \cdot (R_g + R_{Lf}),\ C_1 \cdot \frac{dv_C(t)}{dt} = i_L(t) - i_g(t), \tag{4.4}$$

where R_{SW2} is the resistance of the transistor S_2, R_{UNF} is the resistor of the unfolding switch.

4.1.1 Cost Function Based on the Grid Current

As a classical cost function, the grid current is a main parameter for regulation. For this, simple differential equations are useful for predictive values. A special assignment of the duty cycle is defined. The new value of the duty cycle may be chosen in 0.5-3% near the open loop voltage ratio. The expression of duty cycle has the next view:

$$D[k+1] = \frac{v_g[k+1]}{v_g[k+1] + v_{IN}[k]} \pm 0.01,\ D'[k+1] = (1 - D[k+1]) \cdot T_S, \tag{4.5}$$

$$t_0 = D[k+1] \cdot T_S,\ t_1 = 1 - D[k+1] \cdot T_S, \tag{4.6}$$

where $v_{IN}[k]$ is the input voltage level, $v_g[k+1]$ is the value of the grid voltage at the next PWM period.

The simple differential equations allow to obtain the predictive values for the next periods. The parameters of the input capacitance R_{IN} and C_{IN} have a small effect on the main inductor current. That is why these parameters were neglected. The predictive values are as follows:

$$i'_L[k+1] = \frac{v_{IN}[k] \cdot t_0 + L_1 \cdot i_L[k]}{L_1},\ v'_C[k+1] = v_C[k] - \frac{i_g[k]}{C_1} \cdot t_0, \tag{4.7}$$

$$i'_g[k+1] = i_g[k] + \frac{(v'_C[k+1] + v_C[k] - 2 \cdot v_g[k])}{2 \cdot L_f} \cdot t_0, \tag{4.8}$$

where $i_L[k]$, $v_C[k]$, $i_g[k]$, $v_g[k]$ are the initial values of the sample.

In the second case the differential equation is more complicated, because the equivalent circuit is 3rd order system:

$$i_L[k+1] = i'_L[k+1] - \frac{(v_C[k] + v'_C[k+1])}{2 \cdot L_1} \cdot t_1, \tag{4.9}$$

$$v_C[k+1] = v'_C[k+1] - \frac{i_L[k+1] + i'_L[k+1] + 2i'_g[k+1]}{2 \cdot C_1} \cdot t_1, \tag{4.10}$$

$$i_g[k+1] = i'_g[k+1] + \frac{(i'_L[k+1] + i_L[k+1]) \cdot L_1 - v_g[k+1] \cdot t_1}{2 \cdot L_f}, \tag{4.11}$$

Finally, the cost function of the system can be expressed as follows:

$$J = \min\left\{\sum_{j=1}^{3}\left(\left|i'_g\left[k+j\right]-i_{gREF}\left[k+j\right]\right|\cdot W_{j1}+\left|i'_g\left[k+j\right]-i_{gREF}\left[k+j\right]\right|\cdot W_{j2}\right)\right\}, \qquad (4.12)$$

where W_{j1}: W_{11}, W_{12}, W_{13}, W_{j2}: W_{21}, W_{22}, W_{23} are fixed weight factors. The choice of weighting factors is an open problem in MPC applications. The conventional design approach is to determine the weighting factors heuristically [69].

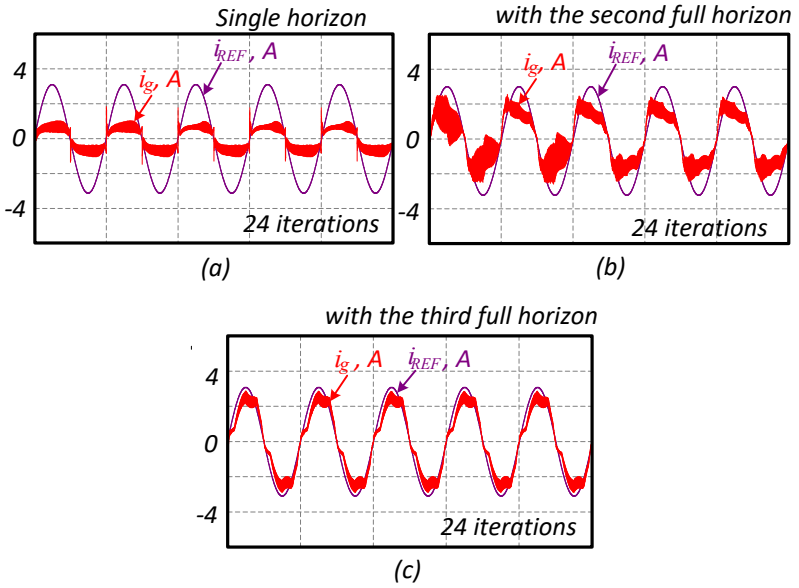


Figure 4.5 Simulation results of the grid-connected inverter with MPC based on the grid current: with a single horizon (a), with the second horizon (b) and with third horizon (c).

Fig. *4.5* shows the simulation results of the closed-loop system based on the MPC along with the traditional cost function. The twisted buck-boost inverter based on the unfolding circuit is used for simulation. The input voltage equals 350 V and a peak of the grid current reference signal is 3A. The grid voltage is a traditional 220 V of RMS. The simulation results were performed for different depths of predictive horizon. As a result, one horizon level of MPC cannot provide a necessary grid current and creates a zero-crossing distortion, as shown in Fig. *4.5a*. The second level of horizon allows to eliminate zero crossing distorting, but the grid current is still not sinusoidal shape (Fig. *4.5b*). The simulation results with the third horizon level showed the best regulator performance, because the grid current was significantly better and similar to a reference grid signal (Fig. *4.5c*). But THD value is still not acceptable in the third case. Moreover, a large number of incrementation steps for duty cycle (iteration) require fast computation and good performance chips. The iteration number is 24 for each level of predictive horizon. If calculating a number of iterations for the third horizon level, it will be 24^3=13824. Of course, the further horizon level will increase quality of the grid current, but the number of computational efforts is unacceptable for practical implementation.

4.1.2 Cost Function Based on the Input Inductor Current

The traditional cost function is not sufficient for ensuring a good grid current, as shown in the previous subchapter. The main reason is that the system is a non-minimum phase system, especially in boost mode [70], [71]. Therefore, another approach for a cost function should be applied. Often, the system goes over the stability, because the input inductor current is not under control when it is controlling the grid current. Thus, the input inductor current should be added in the final cost function. Based on the hypothesis let consider the input inductor current as a main parameter for control.

The first condition that is needed is that the grid current has very low high-frequency ripple, because of an output filter. That is why the next predictive values of the grid current can be considered as similar during several samples:

$$i_g\left[k+3\right] = i_g\left[k+2\right] = i_g\left[k+1\right] = i_g\left[k\right], \tag{4.13}$$

where $i_g[k+3]$, $i_g[k+2]$, $i_g[k+1]$ are predictive values of the grid current for the next PWM periods.

The second important assumption is that the duty cycle should change slowly, because it should not be a sharp current step in the nominal operation. This approach allows to decrease computational time, because instead of range: from 0 to 100%, the system will choose the next duty cycle value across a previous value. The previous value of the duty cycle must be kept in the memory of the microcontroller. The new value of the duty cycle can be found, for example, at 5-10% near the previous value:

$$D\left[k+1\right] = D\left[k\right] \pm 0.1, \tag{4.14}$$

where $D[k]$ is the previous value of the duty cycle.

As mentioned in the previous subchapter, the deeper predictive horizon increases the quality of the grid current. Thus, the second horizon was chosen. The cost function of the MPC in this case has the next view:

$$J = \min\left\{\sum_{j=1}^{2}\left(\left|i'_L\left[k+j\right] - i_{LREF}\left[k+j\right]\right|\cdot W_{j1} + \left|i_L\left[k+j\right] - i_{LREF}\left[k+j\right]\right|\cdot W_{j2}\right)\right\}, \tag{4.15}$$

where $i`_L[k+j]$: $i`_L[k+1]$, $i`_L[k+2]$, $i_L[k+j]$: $i_L[k+1]$, $i_L[k+2]$ are predictive values of the inductor current during the next PWM periods, $i_{LREF}[k+j]$: $i_{LREF}[k+1]$, $i_{LREF}[k+2]$ – reference values of the inductor current. The system should calculate only 2 equations instead of 6, as it was in a traditional cost function.

Fig. *4.6* depicts the simulation results of grid-connected system for special cost function based on the inductor current. The boost case is shown in Fig. *4.6a*, when the input voltage is 160 V. The input power equals 650 W and the grid current peak is 4 A. Fig. *4.6b* shows the simulation results for buck mode with a single voltage ratio. The input voltage equals the peak of traditional grid voltage, i.e. 320 V. The grid current peak is 7 A, which corresponds to 1.1 kW of the output power. Fig. *4.6c* shows the simulation result under 450 V of the input voltage. So, the simulation results confirm the hypothesis regarding non-minimum phase system. The number of iterations equalled 5, which simplified the computation process. The second approximated horizon was used in addition. The overall number iteration is 10.

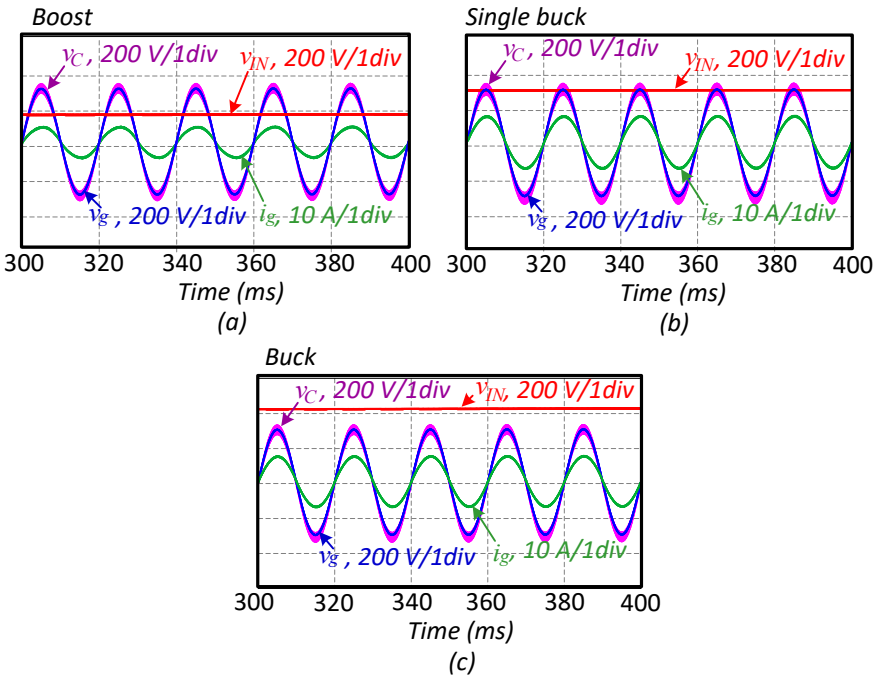


Figure 4.6 Simulation results of the main operation mode. The waveforms of the output capacitor voltage, the grid voltage and the grid current at the input voltage 160 V (a), the input voltage equals 320 V (b), and the input voltage is 450 V (c).

4.2 Summary

This chapter demonstrated the main principle of the CCS-MPC block for a grid-connected system. It considered two ways for implementation of the MPC: with traditional cost function based on the grid current, and a special cost function based on input inductor current. It defined that the boost mode can be considered as a non-minimum phase system. The number of iterations for traditional approach was 24^3=13824, while the special approach needed only 10 iterations for low THD of the grid current.

5 Technology Demonstrator of the Universal Converter

Two buck-boost inverters based on the unfolding circuit were designed for the universal solar concept. Altium Designer was the main hardware designer for all PCBs. The further text explains the experimental results with real prototypes. The grid-connected system based on the MPC was considered. Two power boards and a control board were designed for experimental verification. All inductances are connected by external terminals. The auxiliary supply of the control and measurement board was 12V and corresponds to 10 W of the power losses during converter operation.

5.1 Control and Measurement System

The control board is shown in Fig. *5.1.* The board has 5 isolated voltage and 3 isolated current sensors. The voltage sensor contains a power resistance divider with an isolated opto-element. The item ACS720 is used as a current sensor. The current sensor generates a hardware protection signal, which is overcurrent detection with the digital output. Moreover, the slow and fast overcurrent detection exists in the current sensor to determine what the type of fault is: simple overcurrent value without burned switches or something has burned out and it is now a short circuit. Hardware protection emits a signal to the microcontroller to stop the system as soon as possible. So, all sensors are isolated from the low-voltage control part. Finally, the useful signal goes to the Analog to Digital Converter (ADC) of microcontroller. The differential signals are used for avoiding the common mode interference. Every voltage sensor has a varistor for safety at the overvoltage. The board contains two mechanical relays. The relays are placed in a grid measurement side. The relays allow to connect or disconnect the grid side of the converter.

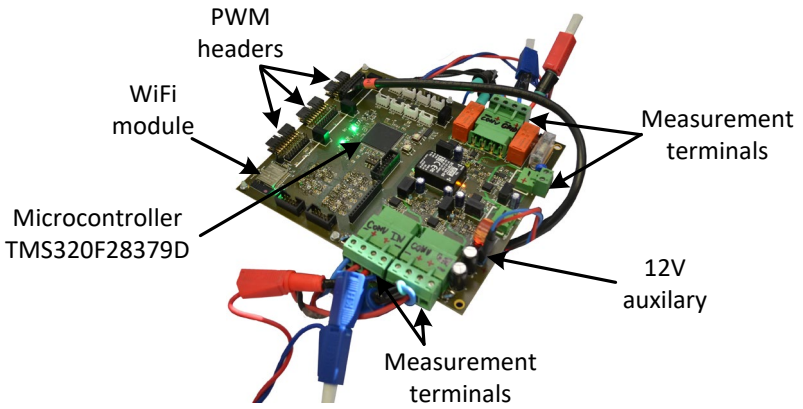


Figure 5.1 Control and measurement board for experimental verification.

Texas Instruments microcontroller TMS320F280379D is one of the best chips for power electronic application. This model of microcontroller is used as the 'brain' of the control board. External crystal frequency is 10 MHZ for MCU. However, internal Phase Locked Loop (PLL) multiplies the crystal frequency 20 times to get a clock frequency of 200 MHz. MCU TMS320F280379D has 2 independent cores. Both have additional low core with low computational capability, as can be seen in Fig. *5.2.* The MCU contains 12 complementary PWM blocks. Every complementary PWM block has A and B channels.

Code Composer Studio from Texas Instruments is an environment for the coding and programming of the microcontroller. Besides hardware safety elements and signals, the software safety system also has a place in the control system. The software protection system takes measured values and compares them with safe limits. In the case of a fault, the system stops and creates a free-wheeling state by switching the necessary transistors. The control system stops relays as well if a fault has occurred. The MCU has a trigonometrical hardware unit that can quickly calculate sinus, cosine or tangent rapidly. All control registers have a duplicate register for shadowing mode. The shadow mode loads data at a clear time.

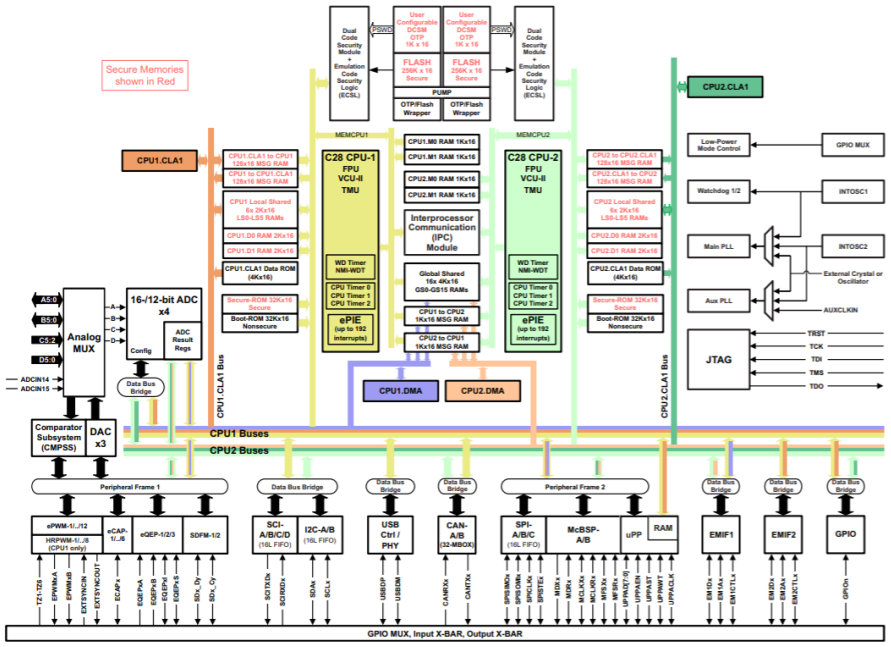


Figure 5.2 Functional Block Diagram of Microcontroller TMS320F280379D.

When talking about MPC implementation, the deeper prediction level increases the quality of the grid current. However, the time of conversion is limited by the sample period and the number of iterations is consequently bounded. The system delay is one sample period due to the shadow mode. A new duty cycle value is set at the start of the next PWM period.

Fig. *5.3* shows the block flowchart of the MPC algorithm of each sample. The sample starts with the emitted signal from the ending of ADC conversions. The next step is to check measured values and identify a fault if it has occurred. If every power signal is fine, the algorithm goes to PLL for continue a grid voltage synchronisation (Fig. *5.3a*). The next important act is to distribute the MPC cycle between the cores (Figs. *5.3b and 5.3c*). For example, the first core is a master core, that enables another core. Each core has its own MPC cycle range. Each core operates independently and parallel to other cores. All results of minimum cost function and the corresponding duty cycles are gathered together in the master core after calculation. The master core compares all results and finds the minimum cost function with a suitable duty cycle. Finally, the duty cycle will be

applied in the PWM block. Approach to distribution of the MPC task increases the amount of iteration and a deeper prediction level can be used.

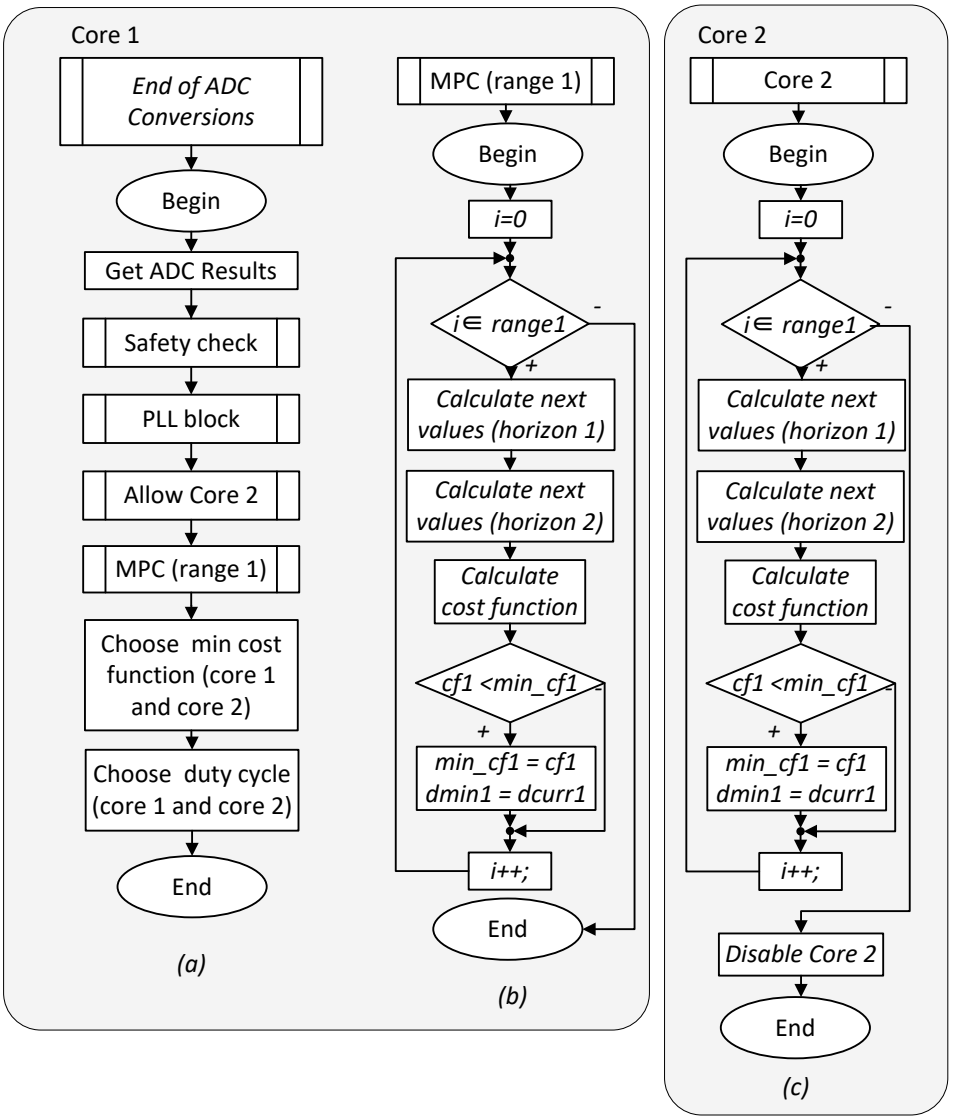


Figure 5.3 Block diagram of the nominal mode with the multicore's distribution: the main core flow of system (a), MPC cycle algorithm (b), the second core flow diagram (c).

5.2 Twisted Buck-Boost Inverter Based on Unfolding Circuit

Fig. *5.4* depicts the experimental prototype of twisted buck-boost inverter based on the unfolding circuit. The experimental prototype consists of power board and a control board. The filters were chosen in according to Chapter III. The rating of the passive elements, transistor limits and other parameters are listed in Table 5.1. The high-frequency transistors S_1, S_2, are executed on the SiC MOSFET C2M0080120D. An alternative unidirectional option is to use a diode instead of transistor S_2. A SiC diode D_1 C3D10012A

is suitable for that topology. The unfolding circuit does not require a transistor with a good dynamic characteristic but needs switches with low static losses. Transistor IPB60R060P7ATMA1 is used for unfolding circuit switches.

Table 5.1 Experimental prototype specifications.

Parameter	Value
Unfolder Capacitor C_1	1.3 µF, 600 V
Input Capacitor C_{IN}	150 µF, 500 V
Grid Capacitor CS	1 µF, 600 V
Input Inductor L_1	1.7 mH, 15A
Output Inductor Lf	0.7 mH, 10 A
Switch S_1, S_2	C2M0080120D, 1200 V
Switches S_3-S_6	IPB60R060P7ATMA1, 650 V
Input Resistance R_{IN}	0.1 Ω
Grid Resistance R_g	0.1 Ω
Input Inductor Resistance R_L	1.0 Ω
Ouput Capacitor Resistance R_C	0.1 Ω
Ouput Inductor Resistance R_{Lf}	0.5 Ω
Resistance of S_1, S_2	0.08 Ω
Resistance of S_3-S_6	0.06 Ω
Sample Frequency $fsample$	62.5 kHz
PWM Frequency f_{PWM}	62.5 kHz
Grid Frequency fg	50.0 Hz
Grid Voltage Amplitude V_M	320 V

Digital oscilloscope Tektronix MD04034B-3 helps to determine power signal shapes along with using current probes Tektronix TCP0150 and voltage probes Tektronix TPA-BNC. Power Analyzer Yokogawa WT1800 measures the efficiency with high tolerance and allows to estimate the performance of any converter.

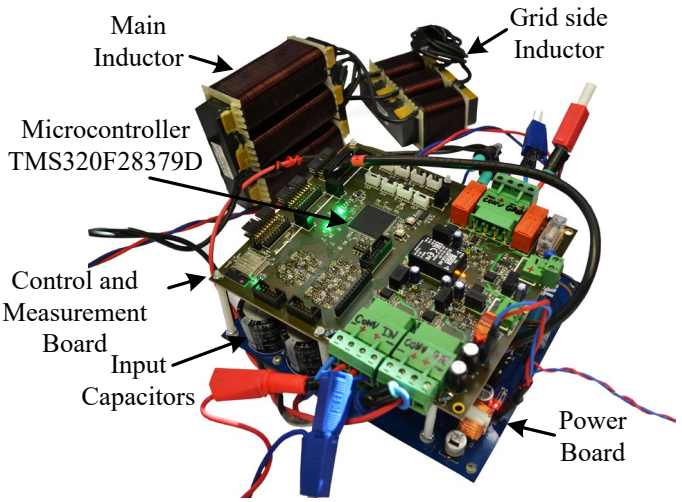


Figure 5.4 The experimental prototype of the buck-boost twisted inverter based on unfolding circuit with the control board.

5.2.1 Solving of Zero Crossing Distortion

One of the hypotheses is that the zero-crossing distortion can be reduced by synchronous switches. One possible option is to analyse the influence of shifting between the buck-boost cell and unfolding circuit in terms of the zero-crossing distortion. A second way focuses on the influences of synchronous switch S_2 on the zero-crossing distortion.

Fig. *5.5* shows the experimental results of the open loop system with resistance load for different cases of zero-crossing distortion. The input voltage equals 250 V and the input power is 250 W. The experimental results without additional control for zero-crossing distortion are shown in Fig. *5.5a*. It is possible to see significant zero-crossing distortion in the output voltage. The input current and input inductor currents are the same as considered in theoretical part and do not fall to negative values. The voltage before unfolding circuit is a green line and corresponds to v_{AB}.

The second scenario is to make a shift between buck-boost cell and the unfolding part by control. Fig. *5.5b* shows the experimental results of the second approach. The zero-crossing distortion was reduced but not eliminated. However, for each point of input voltage and power it requires re-tuning each time. That is why this approach works but requires an additional autotuning each time.

The third approach is to use synchronous switch $S2$ instead of a simple diode. The main principle of operation in the third case is to discharge unfolding capacitor through the input inductance. That is why the input inductor current goes to a negative value across output zero. This method increases the quality of the output voltage at any point of the input voltage and power as it is shown in Figs. *5.5c* and *5.5d*. So, the zero-crossing distortion is eliminated by synchronous switch, which reduces THD of the output voltage.

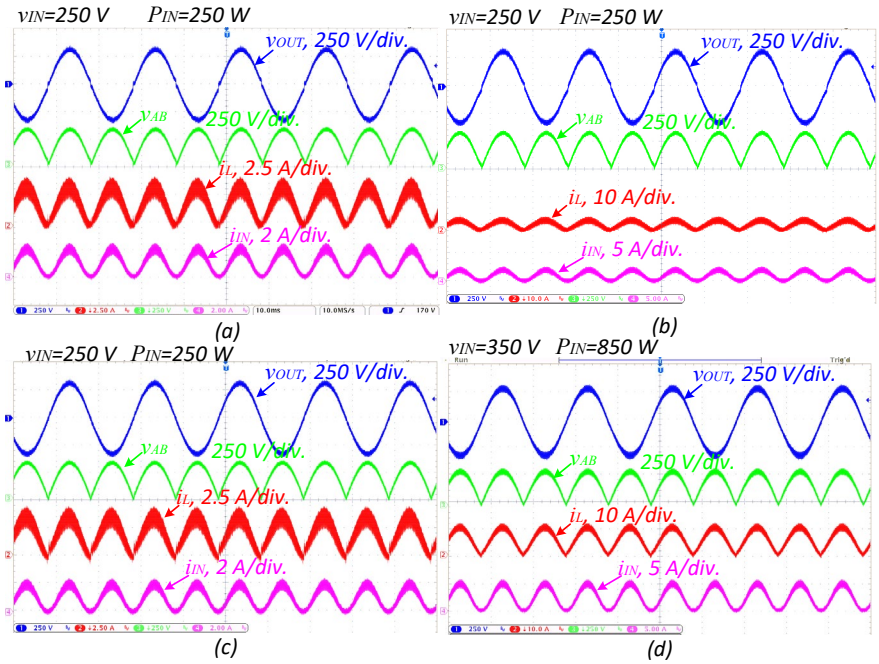


Figure 5.5 Experimental results in off-grid mode without synchronous switching and separate control (a), without synchronous switching and with separate control (b), with synchronous switching and with separate control (c)-(d).

5.2.2 Efficiency Estimation

The efficiency profile is shown in Fig. *5.6.* The efficiency was estimated based on diode and synchronous switch. The auxiliary power loss was 10 W and was not taken into account during an efficiency estimation.

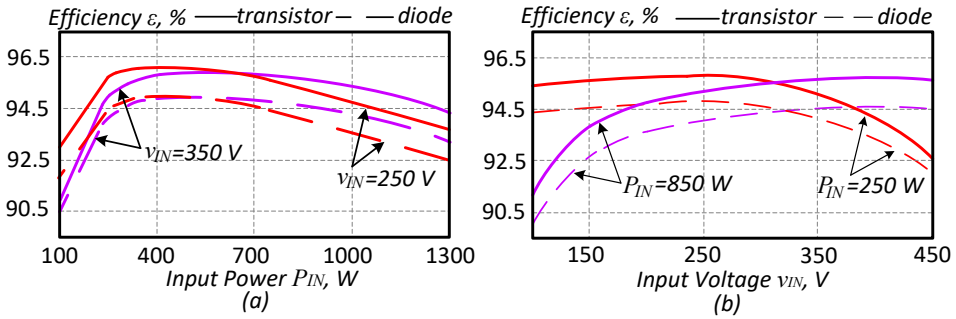


Figure 5.6 Efficiency versus input power in with constant input voltage (a), Efficiency versus input voltage with constant input power (b).

The peak value of efficiency is around 95%. The point of maximum efficiency is different under different input voltages. The solid curve corresponds to efficiency based on synchronous switch, while the spilt line is for efficiency based on diode. The peak of efficiency belongs to the input power 300 W, under a lower input voltage (Fig. *5.6a*). When increasing an input voltage, the currents decrease, and efficiency rises.

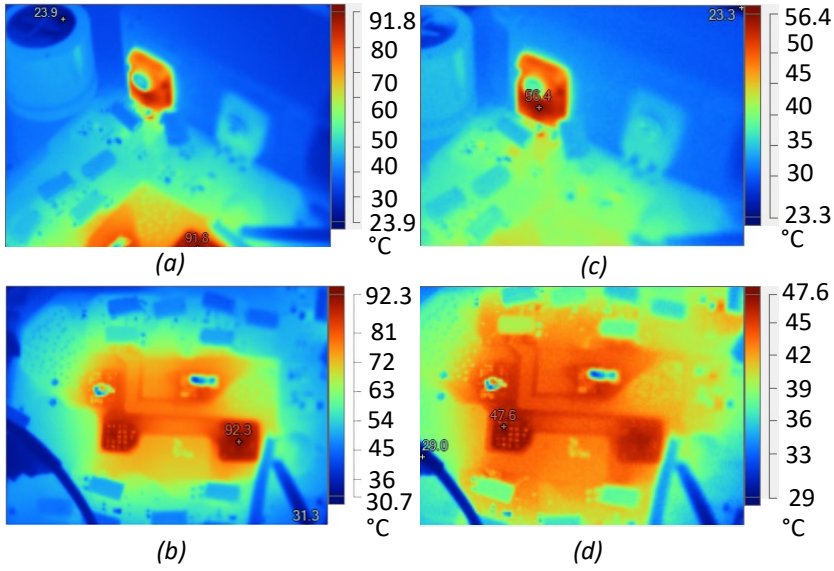


Figure 5.7 Efficiency study of the twisted buck-boost inverter based on the unfolding circuit solution: thermal picture for 350 V and 1150 W (a)-(b), and for 250 V and 550 W (c)-(d).

Fig. *5.6b* shows the dependences of the efficiency versus the input voltage. The input power was measured in a range from 100 W to 1300 W, but only two cases are depicted. The first pair of lines correspond to 250 W of the input power. The peak of efficiency is located at low values of input voltage. Further increasing in the input voltage will

decrease efficiency. In the second case, the power is 850 W. The peak efficiency belongs to the higher value of the input voltage.

Fig. *5.7* demonstrates photos from the thermal camera for two cases of the input voltage and power. The first case corresponds to 250 V of the input voltage and 550 W of the input power in ac mode. The efficiency at this point is 96%. In the second case the efficiency is 95%. This point belongs to 350 V of the input voltage and 1150 W of the input power.

The temperature of the semiconductors is significantly higher in the case of higher input power. Figs. *5.7a* and *5.7c* show the high frequency switches, while Figs. *5.7b* and *5.7d* correspond to the unfolding transistors. All transistors have an acceptable temperature and do not go over 90 °C. From the thermal pictures it is possible to conclude that the switch S_1 generate larger power losses in comparison with another high switching transistor S_2. Also, the efficiency of inverter based on synchronous switch S_2 is higher than in a case based on diode D_1.

5.2.3 Experimental Results of Grid-Connected System

The grid-connected system was tested based on the MPC. The load of the converter is autotransformer, which is connected to the ac grid.

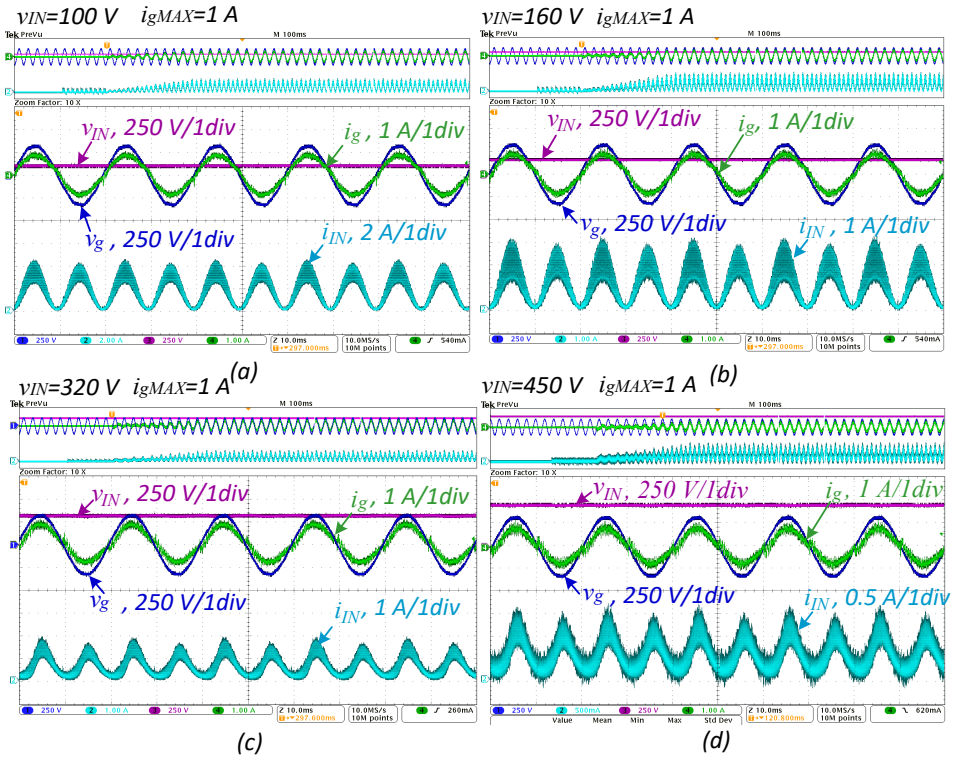


Figure 5.8 Experimental results of grid-connected system for low input power: the waveforms of the input and output voltages and currents for the lower input power in the case of high boost (a), double boost (b), only buck (c) and with higher buck ratio (d).

Firstly, the system was tested for low grid current. Figure *5.8* shows the experimental results of the twisted buck-boost inverter based on the unfolding circuit connected to the grid for 1 A of the grid current. The low power has a significant ripple and complicates the task for a regulator. However, the MPC provides good quality of the grid current even under low power. The main advantages of the twisted buck-boost inverter based on the unfolding circuit are only one mode existing for boost and buck functionalities and the low number of switches. Figs. *5.8a* and *5.8b* show the experimental results for boost cases. At the same time, the buck cases are shown in Figs. *5.8c* and *5.8d*, the input voltage is 320 V and 450 V respectively. THD of grid current was 3.15% in a boost case and was no more than 3% in buck cases. The higher buck case belongs to 450 V of the input voltage. The higher boost case causes the high ripple in the input current.

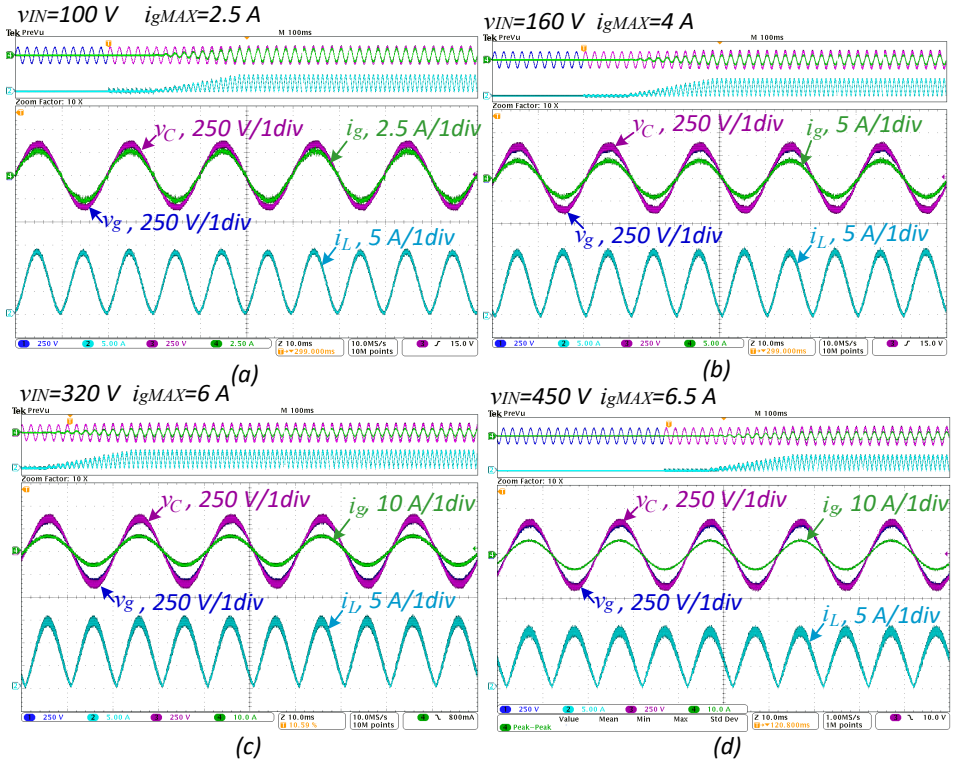


Figure 5.9 Experimental results of twisted buck-boost inverter connected to the ac grid: the waveforms of the input and the output voltages and currents for the higher input power at the input voltage 100 V (a), 160 V (b), 320 V (c) and 450 V (d)

On the other hand, the main drawbacks are the high stress on the semiconductor and high current in input inductor current. The switch stress equals the sum of input and output voltage values. It is similar for the inductor current: it equals the sum of input and output current values. The maximum rate current for input inductor is 15 A and going over this current makes no sense, because the value of inductance will drop. However, the MPC should consider the exact value of the inductance, and, if it is changing in real time, the system can become unstable. A higher buck case corresponds to the most voltage stress on high switching transistors.

Fig. *5.9* shows the experimental results of a grid-connected system for a higher input power. The inductor current reaches 14 A in a peak. For example, when the input voltage equals 100 V and input power equals 550 W, the inductor current reaches 14 A (Fig. *5.9a*). The second boost point is shown in Fig. *5.9b*. The input voltage is 160 V and input power equals 800 W. The grid current peak is 4 A. THD value was less than 5% in boost range. The buck cases are shown in Figs. *5.9c* and *5.9d*. The maximum power was 1.1 kW. THD values of the grid current were less than 3%. The voltage stress reaches 850 V when input voltage is 450 V. The results show that a zero-crossing distortion appeared in the higher buck ratio, but it is not significant. The reason lies in synchronisation.

Another interesting test is the behaviour of the system under dynamic changing of the input voltage. Fig. *5.10* demonstrated the experimental results under the input voltage variations. The input voltage change is changed by spinning of the power supply. Fig. *5.10a* shows the fine changing of the input voltage. It is possible to see that the grid current is stable and does not have any spikes. The input voltage was changed from 360 V down to 260 V. The grid current peak is 3.5A. Figs. *5.10b* and *5.10c* depict the experimental results under a sharp input voltage change. The programmable dc supply provides a fast voltage step. The time of the step is 4-5 periods of the grid. The grid current is stable and does not have any distortions or transients. THD value of the grid current is shown in Fig. *5.10d* and is 3.63%. In summary, the system is stable under input voltage variations.

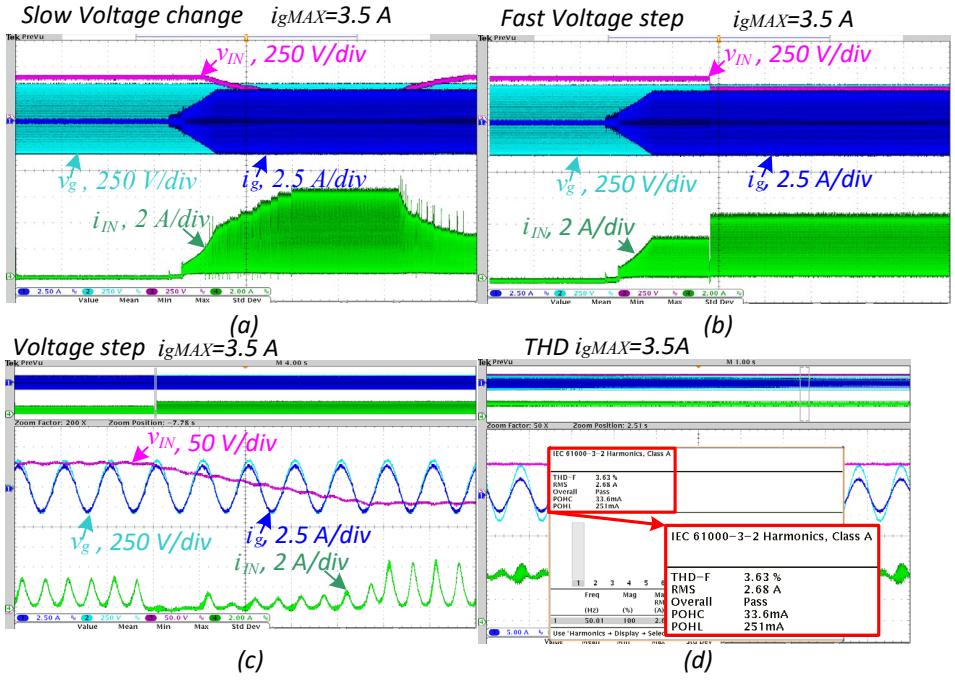


Figure 5.10 Experimental results under the input voltage variation from 360 V to 260 V (a)-(c); THD value estimation of the grid current (d).

5.3 Buck-Boost Inverter Based on Unfolding Circuit

The interleaving of the high-switching cell is a common approach for industrial solutions (Fig. *5.11*). The high efficiency and compact size of inductors are features of the interleaved approach [PAPER-IV]. The grid voltage of ac is 230 V, while the dc grid voltage can be considered in the range of 350 V to 400 V.

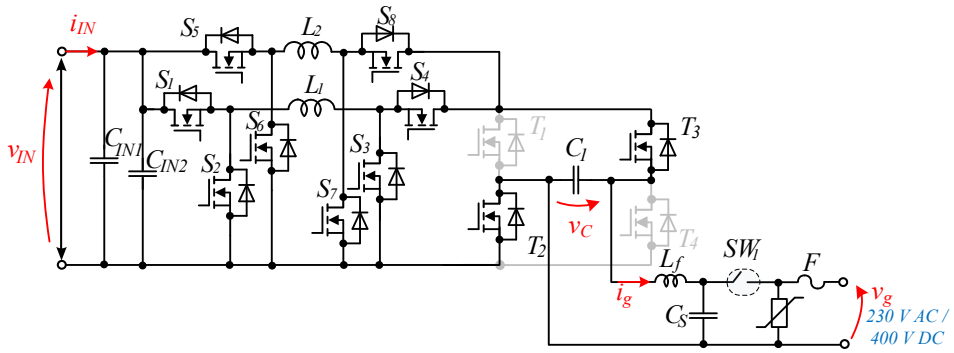


Figure 5.11 Buck-boost 3.6 kW ac (5 kW dc) dc-dc/ac solar converter based on the unfolding circuit with interleaved function.

Converter specifications along with the output filters are shown in Table 5.2. The values of the passive elements correspond to the presented design guidelines from Chapter 3. Table 5.2 contains semiconductor models, that were selected for the experimental prototype. The unfolding circuit does not require a semiconductor with good dynamic characteristics but needs a low resistance. MOSFET FCH060N80 was chosen for unfolding circuit. On the other hand, the SiC transistor C3M0021120K was chosen for high-frequency switches S_1, S_4, S_5, S_8. At the same time, the transistor IMZ120R030M1H was selected for other high-frequency transistors S_2, S_3, S_6, S_7. All selected semiconductors have significant voltage breaking value.

Table 5.2 Prototype parameters and components.

Parameter	Value (Size)
Capacitors $C_{01} = C_{02}$	2.1 mF (0.57 dm^3)
Capacitor C_1	1.3 µF (0.009 dm^3)
Inductors L_1, L_2	1.6 mH (0.55 dm^3)
Output inductor L_f	330 µH (0.27 dm^3)
Grid side capacitance C_S	1 µF (0.008 dm^3)
Switching frequency f	62 kHz
High switching frequency transistors S_2, S_3, S_6, S_7	IMZ120R030M1H
High switching frequency transistors S_1, S_4, S_5, S_8	C3M0021120K
Unfolding circuit transistors T_1-T_4	FCH060N80

Fig. *5.12* shows the laboratory experimental prototype of the universal 3.6 kW ac (5 kW dc) dc-dc/ac converter. All switches have a common heatsink. At the same time, the converter has two boards: power board and control board. There are several aims that were targeted to achieve. The first purpose is to evaluate operation of the buck-boost inverter based on the unfolding circuit during dc and ac grid connections. The second goal is an efficiency study in the dc and ac grid modes. The different PV profiles can be connected to the universal solar converter. Moreover, another task is to connect different types of loads to the converter: resistor, capacitor, inductive, active and grid loads.

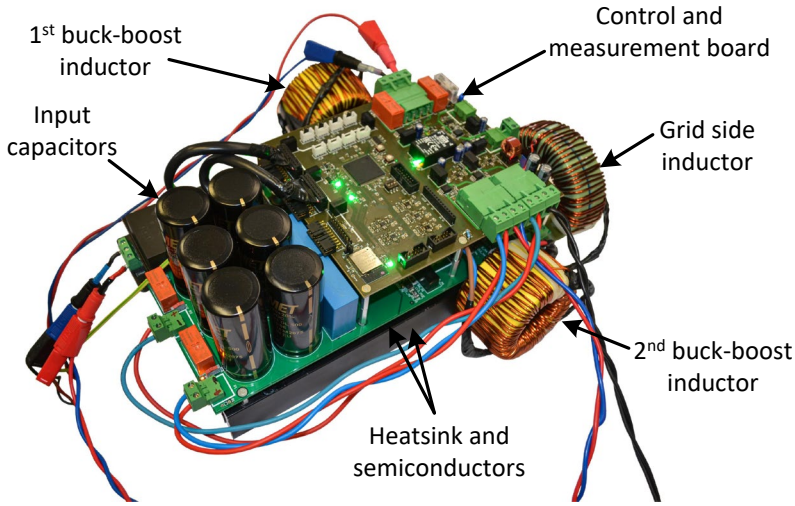


Figure 5.12 Experimental laboratory 3.6 kW ac (5 kW dc) prototype of the universal single-phase dc-dc/ac solar converter based on buck-boost inverter with unfolding circuit.

5.3.1 Dc-ac Mode

Ac operational mode was tested with the grid-connected and open-loop system (grid-off mode). Fig. *5.13* refers to the experimental results of steady-state operation of grid-connected system based on MPC and the grid-off mode. The operation of the universal solar converter in the off-grid mode is presented in Fig. *5.13a*. The input power is 3.3 kW. The converter is working as expected. The second case is capacitive load, which is shown in Fig. *5.13b*. The input power was reduced two times and set a 15 µF in parallel to the resistance load. The phase shifting between output current and voltage in a case of the capacitive load. The third case is shown in Fig. *5.13c*, which corresponds to the inductive load. The additional 2 mH inductance was added in series to the load. The phase shift between the output voltage and current is low. The last off-grid test is an experiment with a nonlinear load. A simple half-bridge rectifier with a large electrolytic capacitor and resister was used. The output voltage is slightly distorted but has a good THD value. The THD_V of the output voltage is 4%, while output current THD_I is around 30%. However, at the present time commercial uninterruptible power supply (UPS) does not provide and ideal output sinusoidal voltage.

The experimental results for the ac grid-connected system are depicted in Fig. *5.13e* and *5.13f*. The active power result is illustrated in Fig. *5.13e* with the half of the maximum input power. The current THD value is less than 3%. Higher input power leads to the higher quality of the grid current. The last interesting test is a pure reactive power injection possibility (Fig. *5.13f*). This feature is useful in some actual applications. Despite the fact that the results have distortions in the reactive mode it is not significant. The distortion appears because the unfolding circuit is working as a hard switching part. The unfolding circuit switching leads to appearing current fall or spike, which can be eliminated by control. However, the control system should be tuned each time for different input voltage and power values.

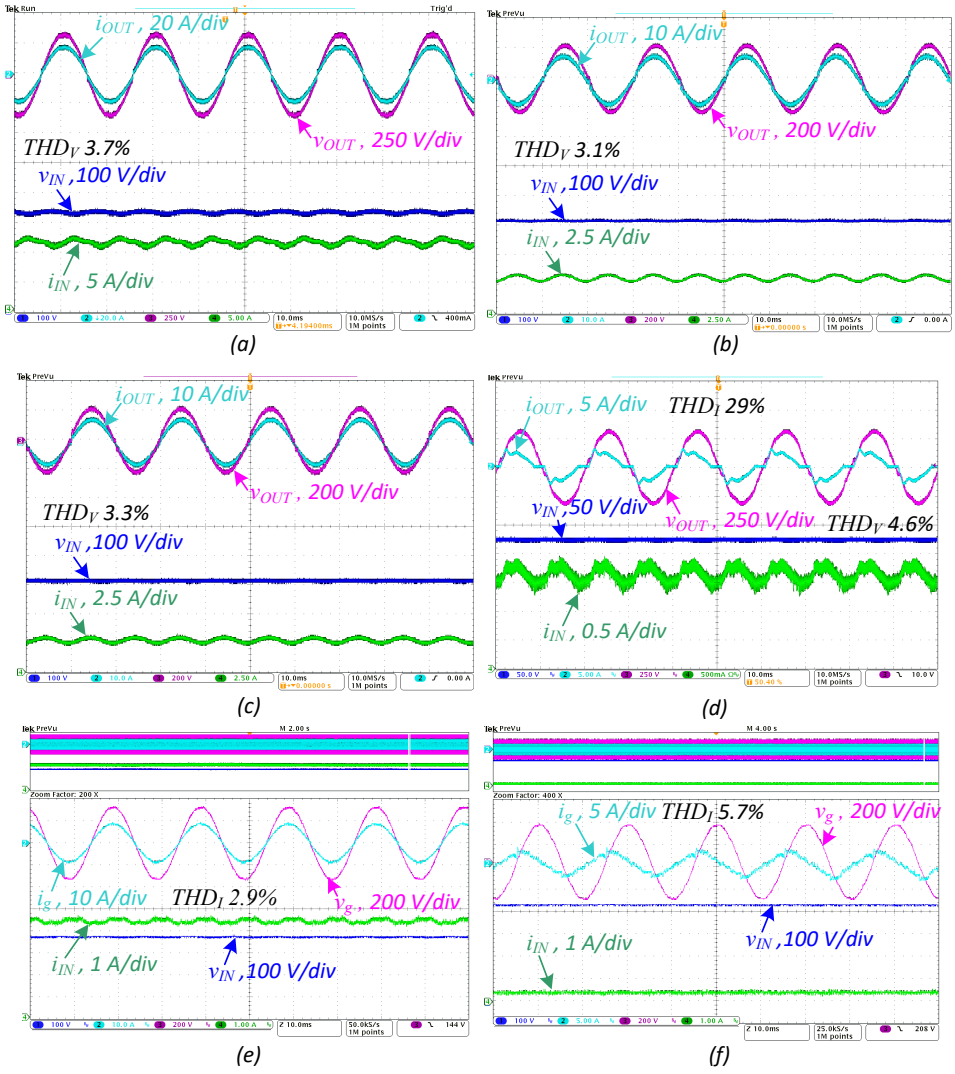
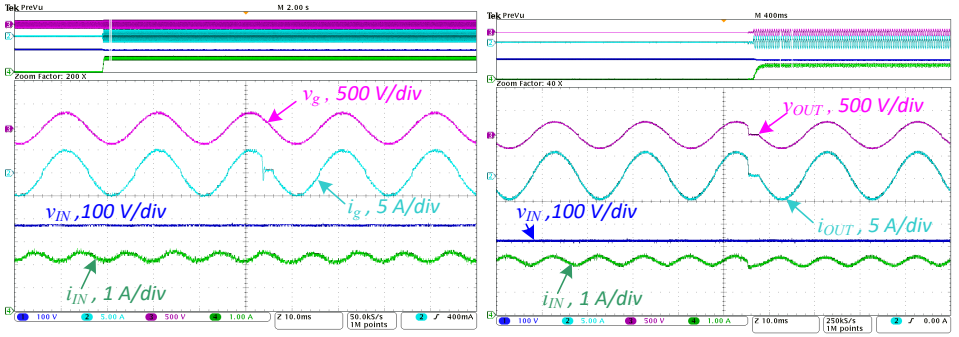


Figure 5.13 Experimental results of the ac operation modes: open-loop system with resistance load (a), capacitive load of the closed-loop system (b), inductive load of closed loop system (c), nonlinear load with a closed loop system for voltage control(d), grid-connected mode with active power (e), reactive power injection in the grid-connected mode (f).

Fig. *5.14* shows the experimental results for current jump cases of the off-grid mode and the grid-connected system. Fig. *5.14a* shows the possibility to inject distorted current into the grid, while the grid voltage is a traditional 220 V. This feature can be used for utility grid and islanding detection. The good dynamic characteristics of the converter by using the MPC is presented. In the second case, the off-grid mode is used (Fig. *5.14b*). The grid current reference also has the same distortion. However, the voltage replays the grid current reference in the off-grid mode. Thus, the type of load can be detected by such an approach. Moreover, a nonlinear MPC control offers fast reacts on any distorted current reference and provides low THD value of the grid current in a grid-connected case.



(a) *(b)*

Figure 5.14 Experimental results in transient conditions: distorted reference current in the ac grid-connected system (a), distorted reference current with a resistance load (b).

5.3.2 Dc-dc Mode

The dc-dc mode was tested for different PV profiles. Benchmarking considers ideal operation conditions without shading and high temperature. The experimental tests considered photovoltaic panels available on the market. Several solar panels were considered: CSM300-60, CSM340-120 and JHM4/72BH445. These modules can be connected in series for increasing the input power and voltage values. The maximum possible voltage of the PV string is limited and equals 1.5 kV. Consequently, 36 panels can be connected in series by PV string. For example, the first profile considered a PV string of 12 solar panels of CSM300-60. The second PV array profile consists of 11 panels of CSM340-120. The last profile comprises in PV string 8 panels of JHM4/72BH445. Table 5.3 lists the parameters of the considered PV profiles.

Table 5.3 PV array profiles considered during experimental evaluations.

Profile	Type of PV	N of panels	V_{OC}, V	V_{MPP}, V	I_{SC}, A	I_{MPP}, A	P_{MPP}, kW
1	CSM300-60	12	478	391	9.8	9.2	3.6
2	CSM340-120	11	455	375	10.1	9.8	3.68
3	JHM4/72BH445	8	394	329	11.3	10.8	3.55

Fig. *5.15a* shows the converter input voltage and power range, MPPT operational range and the selected profiles characteristics. The Maximum Power Point (MPP) value is 3.6 kW for all considered profiles. The maximum dc current is 10 A. The input voltage is changing from 100 V to 500 V. The Maximum Power Point Tracking (MPPT) is working from 150 V to 490 V. The nominal voltage of the dc grid is chosen as 380 V. The maximum input current of converter is considered as 15 A. The power of the solar panel depends on the solar irradiance, which effects voltage and current of the panel. That is why the efficiency was measured under different solar irradiances for selected solution. Different irradiance values make a shift of the MPP, while the voltage falls a little. The solar simulator equipment Chroma 62150H-1000S was used as an input voltage source for the experimental prototype. The same irradiance values were applied for all considered profiles.

The short circuit of the first profile is around 9.2 A, while the open circuit voltage is around 480 V (Fig. *5.15b*). The second profile is selected for higher short circuit current 10 A and a lower open circuit voltage, which is near 450 V. For the third profile the short circuit current is chosen as 11.3 A ad open circuit voltage is 390 V.

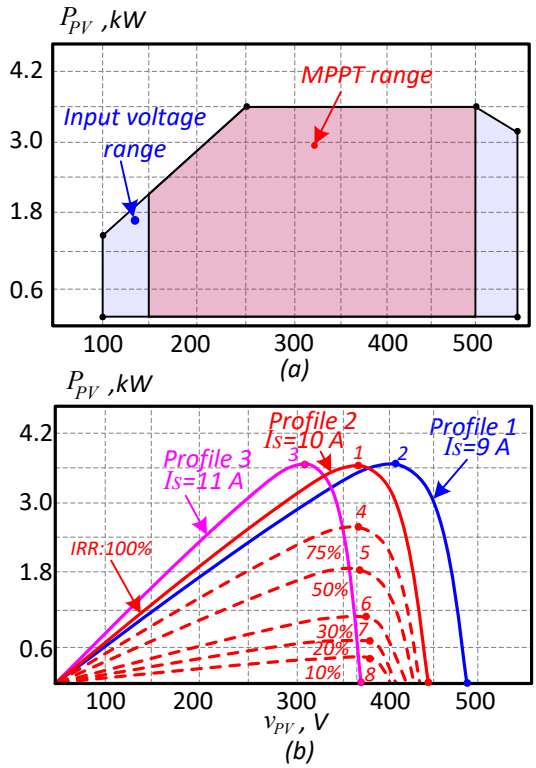


Figure 5.15 The input voltage and power range of universal converter (a), Characteristics of different PV profiles at different solar irradiance levels for universal single-phase dc-dc/ac converter (b).

Fig. *5.16* shows the experimental results for dc grid operation. The experimental pictures contain results for different profiles. For example, Figs. *5.16a* and *5.16b* are devoted to the second profile. These pictures show the MPPT transient process and a pre-charging of the output capacitor C_S. The pre-charging process is needed in the grid to avoid current spikes during the relay switching. The steady-state waveforms are shown in Figs. *5.16c* and *5.16d*, which correspond to profile 3. The ripple of the grid current is 0.15A, while the ripple of the input current is 0.97 A. Such ripple values are acceptable for PV applications. The last two pictures (Figs. *5.16e* and *5.16d*) show the experimental results for profile 1. These pictures contain transient responses when the universal solar converter is disconnecting from the dc grid by the relay. The rapid reference current value does not create a huge spike in the grid current and voltage. The suppressor capacitor provides a soft transient process during stopping of the system and relay disconnection. The input inductors are short circuited by control for safety path of the inductance's currents. The converter showed good performance in dc mode. The MPC control block also was used for the dc-dc operational mode, which also provides a stable operation of the converter under different input voltage and power values.

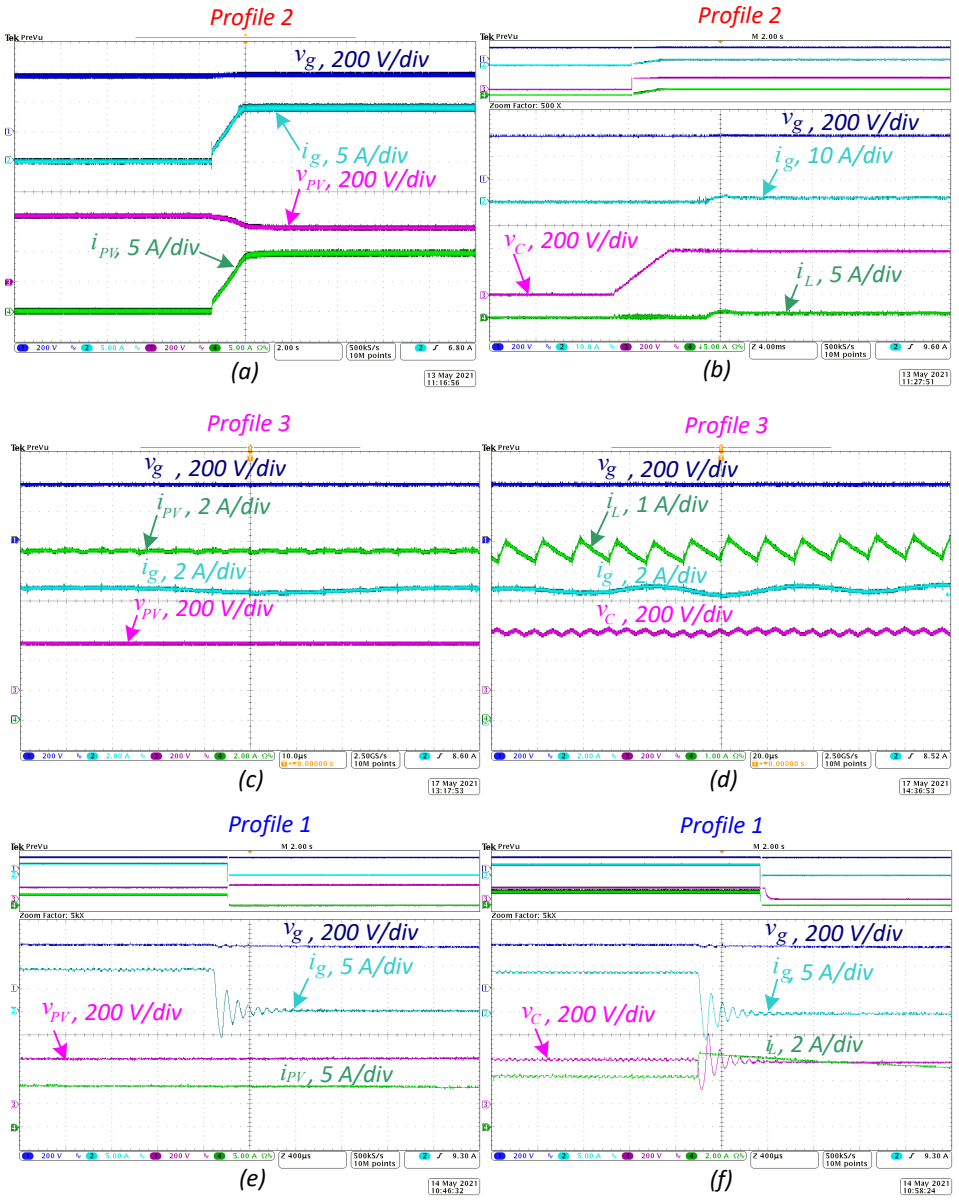


Figure 5.16 Experimental results of a universal solar converter in the dc-dc mode, PV and grid voltage and current: during MPPT operation for profile 2 (a), high ripples in profile 3 (c), switch-off waveforms in profile 1 (e). The waveforms of the input inductor current and output capacitor voltage along with the grid side: during MPPT operation for profile 2 (b), ripple with profile 3 (d), switch-off waveforms for profile 2 (f).

5.3.3 Efficiency Study

The efficiency was estimated in the dc and ac modes of an off-grid system. At the same time, the efficiency of the converter was estimated for a closed-loop system and for different PV profiles in dc mode. Fig. *5.17a* shows the efficiency lines for different PV profiles based on the different irradiation values. The maximum efficiency is 98.8%. The California Energy Commission's (CEC) efficiency is used for an efficiency study. The first PV profile showed better performance, while other two profiles correspond to a boost operation. CEC efficiency of profile 1 is 98.37%, and for the second and the third profiles CEC efficiency is 97.64% and 97.13% correspondingly.

On the other hand, the universal solar converter has an unfolding circuit as a redundancy for dc-dc operational mode. However, the unfolding circuit creates only conduction losses. It is easy to calculate the efficiency of the converter without contribution of the unfolding switches. Fig. *5.17b* shows the efficiency curves for PV profiles without the unfolding circuit. The maximum efficiency value is increased to 99.02%. However, the maximum CEC efficiency was increased by just 0.14%. Similarly, the CEC efficiency of other profiles is less than first profile performance.

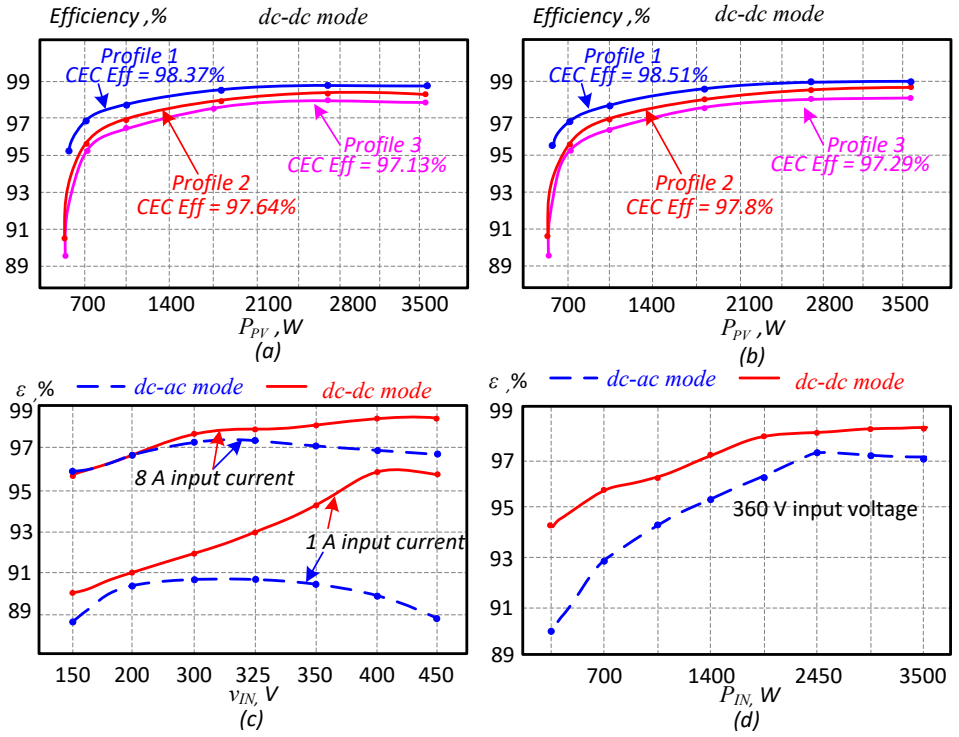
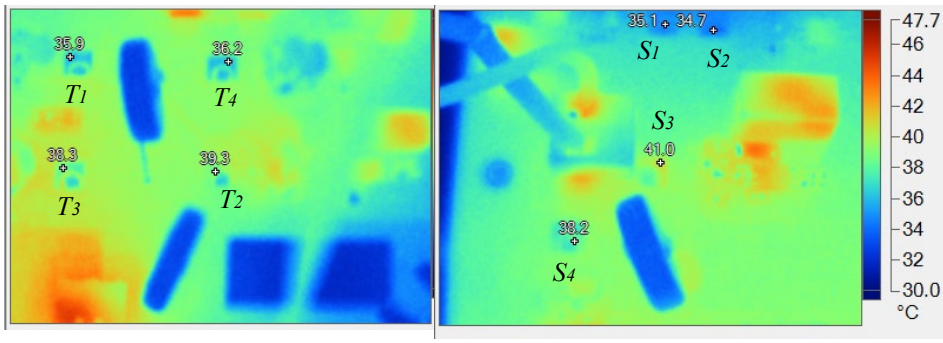


Figure 5.17 Experimental efficiency of the prototype under different PV profiles and with different solar irradiations: with unfolding circuit (a), without unfolding part (b), efficiency versus input voltage with constant input current with ac and dc mode (c), efficiency versus input power with constant input voltage with ac and dc mode (d).

At the same time, the efficiency study was performed for off-grid dc-dc operational mode. The input power was changed from 150 W to 5 kW. The peak efficiency again was more than 98%. The main reason of this performance is a minimum number of semiconductors switching. Figs. *5.17c* and *5.17d* shows the comparison results of the

efficiency measuring between dc and ac mode and with different constant values of the input current. The blue lines correspond to dc-ac mode, when the red lines belong to dc-dc mode. The first value of the input current is 1 A (Fig. *5.17c*). The efficiency is low during the whole input voltage range. The reason for this is auxiliary power supply consumption that is constant and equals 12 W. The efficiency fall in a case of input voltage drop is explained by the lower level of the input power. In the second case the input current value is 8 A. The efficiency is significantly higher. However, the curves kept the same features as were seen with a lower input current value. Efficiency drops and rises in the same way. The last picture with efficiency curves is Fig. *5.17d*. The peak of the efficiency corresponds to the maximum input power. The difference in the efficiency between dc and ac modes is around 1% in the nominal input power. Due to a higher efficiency in dc-dc mode, the input power was increased up to 5 kW.

Fig. *5.18* shows the thermal pictures of the universal converter under an operation in dc. The temperature of the switches does not reach more than 50 °C under the maximum input power value (Fig. *5.18b*). The maximum temperature of the unfolding switches was around 40 °C (Fig. *5.18a*). The heatsink temperature was around 42 °C.



(a) *(b)*

Figure 5.18 Thermal pictures of the solar converter under a maximum power point operation: unfolding transistors (a), buck-boost cell switches (b).

5.4 Summary

Two laboratory experimental prototypes were shown in this chapter. These experimental prototypes were implemented based on the control and measurement board, which have 5 voltage and 3 current sensors. The brain of the control board is the multicore MCU that can split the MPC task between cores and decrease computational time. It was found that the synchronous switches should be used instead of a simple diode for reducing a zero-crossing distortion in topologies based on the unfolding circuit. A twisted buck-boost converter was investigated in terms of closed-loop system based on MPC, while the single-phase buck-boost inverter was studied in terms of dc and ac functionality. Finally, the efficiency study was performed for all prototypes. As a result, the buck-boost dc-dc/ac converter showed better performance. If compare dc and ac modes, the dc-dc mode is more efficient at any point.

6 Conclusions

The novel concept of the universal solar dc-dc/ac converter is suitable for dc and ac single-phase applications. A great deal of inverter topologies can be considered as a universal solar converter. For example, the power electronics converter that was initially designed for dc-ac application with an output filter stage for dc grid and fast protection circuit breaker can be considered as a universal solution. The converter based on the unfolding stage can naturally provide dc or ac output voltage without additional redundancy. The universal concept of the solar dc-dc/ac converter can be used as an industrial solution for low-voltage dc and ac systems. The comparative analysis based on several criteria was performed to find the most suitable solution. The buck-boost inverter based on the unfolding circuit was chosen as an optimal solution for universal converter.

The grid-connected system was implemented based on the CCS-MPC block. A boost mode of the selected topologies ca be considered as non-minimum phase system. That is why a non-traditional cost function is required for control.

Two laboratory experimental prototypes were designed along with a control and measurement board, which have 5 voltage and 3 current sensors. The brain of the control board is the multicore MCU that can split MPC tasks between cores and decrease computational time. The efficiency study was conducted for the family of the buck-boost inverter based on the unfolding circuit. As a result, the buck-boost dc-dc/ac converter showed better performance. The dc-dc mode is more efficient in any point.

The additional capacitor as a suppressor should be set at the grid side to control a voltage spike during a grid disconnection.

As the results of thesis, the author can claim the following:

- The family of the buck-boost inverter based on the unfolding circuit provides the universal capability with minimum redundancy.
- The interleaved approach with two buck-boost cell is the optimal solution.
- Zero-crossing distortion in topologies based on the unfolding circuit can be eliminated by using synchronous switches.
- A traditional cost function for a grid-connected system is not suitable for the family of the buck-boost inverter, which is why some special cost function should be applied. Using a multicore chip can distribute the MPC cycle task between cores and decrease the computational time by 2-3 times.
- A family of the buck-boost inverters based on the unfolding circuit provides bidirectional energy flow. Such types of inverters can generate a reactive power.

Future work relates to designing the preindustrial TRL-6 experimental prototype. The future task is thus to design the control, measurement, and power parts on one PCB.

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I want to dedicate this thesis in memory of grandmother Valentina and my cat Mars, Love you.

Abstract

Photovoltaic String Converter with Universal Compatibility with AC and DC Microgrids

This PhD thesis is dedicated to the development of the novel concept of the universal solar dc-dc/ac converter suitable for dc and ac single-phase applications. The power electronics converter that initially was designed for dc-ac application with an output filter stage for dc grid and fast protection circuit breaker can be considered as a universal solution. The CB must cover all demands of dc grid protection, while the output filter can be chosen as a filter for conventional ac application with an additional output capacitor (suppressor) to eliminate voltage spike at a sudden grid disconnection. The considered approach can be used as an industrial solution for low voltage dc and ac systems.

Several solutions were selected as a universal converter that is applicable for ac and dc grid. The comparative analysis based on several criteria was done for chosen the most suitable solution. The buck-boost inverter based on the unfolding circuit was chosen as an optimal solution for universal converter.

A family of the buck-boost inverters based on the unfolding circuit were proposed as a universal solar converter applicable for dc and ac grids. Two laboratory experimental prototypes were developed. Twisted buck- boost converter was investigated in terms of closed-loop system based on MPC, while the single-phase buck-boost inverter was learned in terms of dc and ac functionality. The efficiency study was done for all prototypes, where the buck-boost dc-dc/ac converter showed better performance than twisted inverter with unfolding circuit. The dc-dc mode is more efficient in any point because it does not have double power pulsation.

The main principle of the CCS-MPC block for grid-connected system was considered. A special cost function based on input inductor current has a better performance because the buck-boost inverter based on the unfolding circuit is non-minimum phase system. Computational burden was reduced by using multicores MCU with 2 independent cores and 2 extra sub-cores, which is suitable for parallel computation, for example for deeper prediction horizon of MPC.

This work has also a substantial practical value:

- Developing new type of devices applicable for both types of the grid with the same terminals and minimum redundancy.
- Two buck-boost inverters based on the unfolding circuit as the most optimal solution for universal application: single stage buck-boost inverter based on the unfolding circuit, twisted buck-boost inverter based on the unfolding circuit.

The theoretical and practical results can be used for further developments for universal solar converter, particularly for developing TRL-6. The proposed cost function and approach of MPC technique make this attractive for the industry.

Lühikokkuvõte
Alalis- ja vahelduvvoolu mikrovõrkudega ühilduv universaalne muundur päikese-elektrijaamadele

Antud doktoritöö on pühendatud uudse alalis-alalis-vahelduv tüüpi jõupooljuhtmuunduri arendusele, mis mõeldud nii alalisvoolu kui ka ühefaasilist vahelduvvoolu kasutavatele rakendustele. Tegu on universaalse jõupooljuhtmuunduriga, mis algselt loodi alalis- ja vahelduvvoolu rakendustele sisaldades nii alalisvoolu poolset filtrit kui ka kiireid kaitseahelaid. Kaitseahel peab vastama alalisvooluvõrgu kaitsenõuetele samas kui väljundfilter töötab vaheluvvoolu poolses osas tavalise filtrina, millele on lisatud üks kondensaator, vältimaks ülepingeimpulssi võrgu lahutamisel. Sellist lahendust saab kasutada nii madalapingelistes, tööstuslikes alalis- kui ka vahelduvvoolusüsteemides.

Valiti välja mitu universaalmuunduri põhimõttelist lahendust, mis sobiks vahelduv- ja alalisvooluvõrkudele. Mitmele kriteeriumile toetuv võrdlev analüüs aitas valida parima lahendusena vaheldava ahelaga pinget tõstva ja langetava skeemilahendus.

Vaheldava ahela baasil pakuti välja terve seeria pinget tõstvaid ja langetavaid skeemilahendusi alalis- ja vaheluvvoolurakendustele. Loodi kaks eksperimentaalset prototüüpi. Antud rakenduses uuriti nii pööratud topoloogiaga kui ka ühefaasilist pinget tõstavat ja langetavat muundurit. Kõigi prototüüpidega viidi läbi põhjalik kasuteguri uuring, mille põhjal näitas ühefaasiline topoloogia olulist eelist pööratud topoloogiaga vaheldava ahelaga muunduri ees. Kõige energiatõhusamaks osutus alalis-alalis režiim tänu võimsuspulsatsiooni puudumisele.

Töötati välja mudelipõhise juhtimisega võrguühendusega süsteemi põhimõtteline lahendus. Spetsiaalne drosselivoolul põhinev kulufunktsioon näitas parimaid tulemusi, kuna vaheldava ahelaga pinget tõstev ja langetav muundur on mitte-miinimumfaasilise käitumisega süsteem. Arvutusjõudluse tõstmiseks kasutati mitmetuumalist (kahe sõltumatu ning kahe alamtuumaga) mikrokontrollerit, mis on sobiv paralleelarvutusteks, mida vajavad kiired mudelipõhised ennustavad juhtalgoritmid.

Antud tööl on ka arvestatav praktiline väärtus:

- Uut tüüpi minimaalsete lisakomponentide ja minimaalse arvu viikudega universaalsete jõupooljuhtmuundurite arendamine nii alalis- kui ka vahelduvvooluvõrkudele.
- Kaks vaheldava ahelaga pinget tõstva ja langetava muunduri lahendust universaalseks rakenduseks: üheastmeline muundur ning pööratud topoloogiaga muundur.

Töö teoreetilisi ja praktilisi tulemusi saab kasutada universaalsete päikesepaneele teenindavate muundurite edasiseks arendamiseks tehnilise valmisoleku tasemeni 6. Loodud väärtuspõhine funktsioon koos mudelipõhise ennustava juhtimisalgoritmiga muudavad antud seadmed eriti huvipakkuvaks jõuelektroonikat tootvatele ettevõtetele.

Appendix

[PAPER-I] O. Husev, O. Matiushkin, C. Roncero-Clemente, F. Blaabjerg, D. Vinnikov, “Novel Family of Single-Stage Buck–Boost Inverters Based on Unfolding Circuit,” *IEEE Trans. on Pow. Electron*., vol. 34, no. 8, Aug. 2019. DOI: 10.1109/TPEL.2018.2879776.

Novel Family of Single-Stage Buck–Boost Inverters Based on Unfolding Circuit

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***Abstract*—This paper describes a novel family of single-phase single-stage buck–boost inverters using output unfolding circuits. Operation principles and component design guidelines along with modulation techniques are presented and discussed. The simulation results confirm all theoretical statements. Experimental setup of the most promising solution is assembled and tested, where the efficiency for different operation modes is analyzed. Finally, the pros and cons along with applications of the proposed solutions are discussed in the conclusions.**

***Index Terms*—Buck-boost, dc-ac converter, unfolding circuit.**

I. Introduction

THE Google Little Box Challenge (GLBC) has shown a close relation with the topic of high-power density inverters for photovoltaic (PV) applications and that have demonstrated extremely high-power density of power electronics converters achievable [1]–[3]. One of the GLBC project outcomes is the concept of a very high-power density converter. The finalists demonstrated a similar approach. It includes the basic full-bridge interleaved inverter, an active decoupling circuit, and also using widebandgap (WBG) semiconductors.

WBGs market has an upward trend in today's power electronics due to their high electron mobility and high-voltage breakdown field [4]–[6]. As a result, fast-switching high-voltage semiconductor devices are already available on the power electronics market. The challenge is still the cost of those devices, which, however, is decreasing year by year.

At the same time, in PV systems, several configurations may be used [7], [8]. Single PV panel is available for low-power applications. It suffers from voltage drop at the temperature increasing. In the serial or string connections, one of the major drawbacks is its significant voltage drop at partial shadowing. Both of them lead to a wide range input voltage variations during the energy utilization time. The GLBC solution is intended for narrow input voltage regulation, and it cannot provide a high and efficient PV energy conversion in heating or shadowing conditions. Also, dual-back inverters [9], [10] or the boost inverter reported in [11] and [12] cannot be considered as a solution with a wide range of regulation. Intermediate voltage boost dc–dc converters are used to overcome this drawback. At the same time, this solution is more complex and more expensive in price.

Several alternatives have already been presented. Inverters with an active boost cell are described in [13]–[16]. They can provide very high boost of input voltage but suffer from high-current spikes in the semiconductors and passive elements. The buck–boost solutions based on an active boost cell are rarely seen in industrial applications.

An impedance-source (IS) network was proposed in [17] as a novel single-stage solution. Since that time, many solutions based on the IS networks have been extended for various fields of application. Z-source inverters and quasi-Z-source inverters (qZSIs) were proposed for grid integration. They overcome the limitation of the conventional grid-connected inverters: they have a buck; a boost mode; and do not suffer from shoot-through (ST) states. This boosting technique enhances the inverter reliability. Also, many other derivations of IS networks have been proposed. All of them can be subdivided into the following groups: those including separated inductors; coupled inductors; with and without a transformer; and discontinuous and continuous input current. Siwakoti *et al.* [18]–[21] present a good overview of the existing solutions.

At the same time, recent research reveals evident drawbacks of the IS-based converters in terms of power density and efficiency. The control system is quite complex as well [22]–[24]. Split-source inverters [25], [26] have been proposed as an alternative solution to inverters with IS networks. Improved performance in terms of passive component counts accompanied by higher voltage and current stresses at lower voltage gains is obtained, and no ST immunity is present anymore. The

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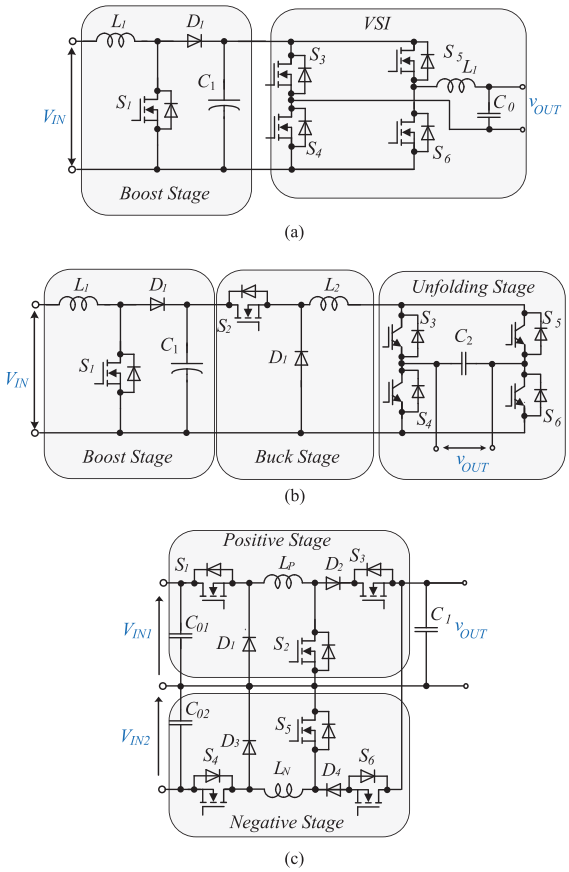

Fig. 1. (a) Conventional boost dc–dc converter along with VSI. (b) DC–AC converter based on unfolding circuit. (c) Aalborg inverter.

necessity of the inverter with wide input voltage regulation along with high power density and acceptable efficiency pushes the industry and the academia to search for new and better solutions. Several interesting single-stage buck–boost inverters are proposed in [27]–[31].

The solution based on the input boost and buck converters along with a line-frequency unfolding circuit seem to be interesting for practical applications [31], [32]. Fig. 1 shows the initial solutions. The operation principle consists in the boosting input voltage to the dc-link voltage, which is maintained constant. Buck stage performs further modulation, which is unfolding to the sinusoidal voltage.

A very interesting solution is proposed in [33], which is further developed in [34]–[38]. An Aalborg inverter [see Fig. 1(c)] is proposed as an inverter that combines buck and boost functionalities. It is achieved by utilizing two independent buck–boost stages that are in response to the output sinusoidal voltage generation. The first stage is in response to the positive output voltage generation, the other is to negative output voltage generation. One of the main advantages of the proposed solution is in the minimum voltage drop of the filtering inductors in the power loop at any time. At the same time, this solution uses a double number of semiconductors and an inductor in the buck and boost stages, which is an obvious drawback. Also, two power sources are required. Quite similar idea with double components is discussed in [39]. The dual-buck-structured inverter is working in similar way, but has single-input voltage source.

This paper discusses further modification of the solution based on the combination of the buck and boost functionalities without evident dc-link stage with the output unfolding circuit. The next sections are organized as follows. Section II describes the proposed solution in general terms. Section III focuses on the detailed study of the modulation technique for the novel solutions. Guidelines for component selection are provided in Section IV, and Section V covers the simulation study of the proposed solutions. Experimental verifications are presented in Section VI. Finally, Section VII contains discussions and conclusions.

II. Proposed Novel Single-Phase Single-Stage Inverters With Unfolding Circuits

The first proposed single-phase unfolding circuit with only one inductor is depicted in Fig. 2(a). This circuit consists of an input inductance L_1, a capacitor C_1, and eight switches S_1–S_8. Partially, the principle of operation is described in [40], which has selection of the stage, using the ratio between the input voltage and the required output voltage.

It is obvious that a high amount of switches provides a very flexible modulation strategy and many approaches can be applied. In any case, switches S_1 and S_3 define the basic operation modes of the converter. The transistors S_2 and S_4 are optional and they can be replaced by diodes if only unidirectional operation is required or used for conduction losses reduction. However, the use of transistors S_2 and S_4 allows a bidirectional power flow or the rectification mode in the converter, which may be helpful in some applications.

According to the classical definition of the unfolding circuit, transistors S_5–S_8 provide a simple unfolding circuit. At the same time, it should be noted that in the general case, these switches can be used for high-frequency modulation.

If the input voltage $V_{\rm IN}$ is higher than the desired instantaneous output voltage $v_{\rm OUT}$, the buck mode will be applied with the corresponding buck factor B_{11}

$$B_{11} = D_{S1} \tag{1}$$

where D_{S1} is the transistor S_1 duty cycle. In this mode, the converter has two possible states: transistor S_1 is conducting or not conducting.

If the input voltage $V_{\rm IN}$ is lower than the desired instantaneous output voltage $v_{\rm OUT}$, the transistor S_1 is constantly conducting, while transistor S_3 is switching, performing the classical boost function

$$B_{12} = \frac{1}{1 - D_{S3}} \tag{2}$$

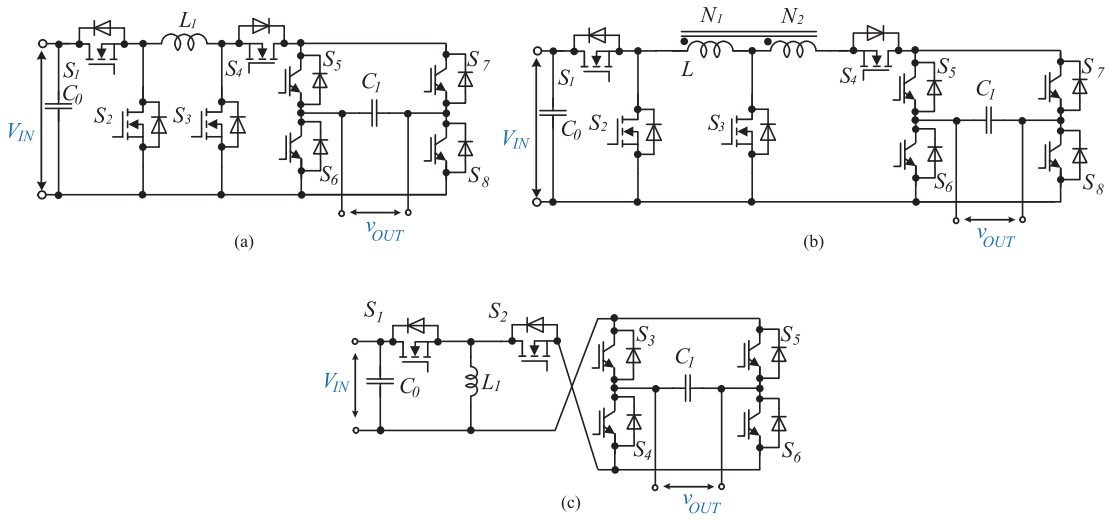

Fig. 2. Family of the single-phase single-stage buck–boost inverters with unfolding circuits: (a) Single-inductor unfolding buck–boost inverter. (b) Tapped-inductor unfolding buck–boost inverter. (c) Single-inductor twisted unfolding buck–boost inverter.

where D_{S3} is the transistor S_3 duty cycle. It means that buck–boost functionality is optionally selected, depending on the ratio between the input and output voltages.

The second solution is the tapped-inductor unfolding buck–boost inverter shown in Fig. 2(b). It is evident that the operation principle of this converter is very similar to the first solution. The main difference lies in the tapped inductor. Due to the different turns ratio of the tapped inductor, a higher input voltage range can be achieved.

Finally, Fig. 2(c) shows a single-inductor twisted unfolding buck–boost inverter. It is derived from the conventional buck–boost dc–dc converter with the well-known gain factor

$$B_2 = \frac{D_{S1}}{1 - D_{S1}}. \tag{3}$$

It means that the instantaneous value of the output voltage is defined by switch S_1, while the unfolding circuit is realized by means of transistors S_3-S_6. Similar to the first solution, the transistor S_2 is optional and it can be replaced by a diode or used for conduction losses reduction. This solution is different from the other ones because it uses the same operation mode for the buck and boost cases.

A detailed description of a possible modulation strategy is presented in Section III. Despite an increased amount of semiconductors, only two of them have high-switching frequency in any particular operation point. It means that very low-switching losses along with electromagnetic interferences (EMI) are expected. In addition, none of these solutions have high-switching harmonics in the common-mode voltage, which in turn, means reduced size of the common-mode filters.

III. Special Modulation Techniques

Because of the possibilities in variety of the switching states, several modulation techniques can be applied for the proposed circuits. Depending on the modulation method, different conduction and switching losses, quality of the output voltage, and computational burden can be derived. In general, during the operation of each proposed inverter, it is possible to distinguish two main situations: the input voltage ($v_{\rm in}$) is lower than the peak value of the reference voltage ($v_{\rm ref}$ (t)) or $v_{\rm in}$ is higher than the peak value of $v_{\rm ref}$ (t). In the first case, the converter will switch from the buck mode to the boost mode accordingly [see Fig. 3(a)], while just the buck mode is present in the second situation.

When $v_{\rm in}$ is lower than the peak value of $v_{\rm ref}$ (t), we can also distinguish if $v_{\rm in}$ is lower or higher than the instantaneous value of $v_{\rm ref}$ (t). If $v_{\rm in}$ is higher, the converter will operate in the buck mode with a duty cycle obtained as

$$D_{\rm Buck} = \frac{|v_{\rm ref}(t)|}{v_{\rm in}} \tag{4}$$

which, in fact, represents the duty cycle of switch S_1, while S_3 is always turned OFF. However, if $v_{\rm in}$ is lower than the instantaneous value of $v_{\rm ref}$ (t), the power converter runs at the boost mode, and the duty cycle is represented as

$$D_{\rm Boost} = 1 - \frac{v_{\rm in}}{|v_{\rm ref}(t)|} \tag{5}$$

where $D_{\rm Boost}$ is the duty cycle of switch S_3, meanwhile S_1 will be turned ON in this mode. These two modulating signals are compared with a carrier signal to trigger the different switching states at high frequency in either buck or boost modes. The generation of the gate signals for switches that compose the

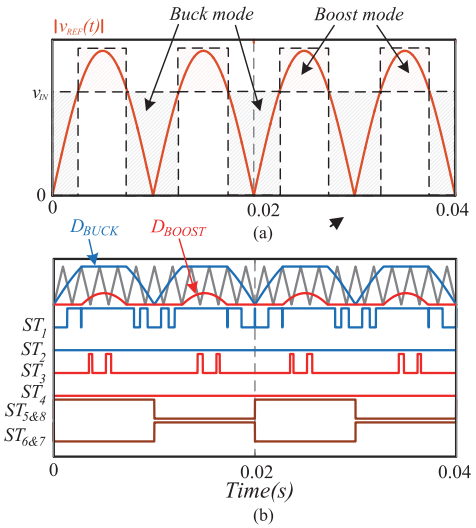

Fig. 3. Switching signals generation for the single-inductor unfolding buck–boost inverter and the tapped-inductor unfolding buck–boost inverter: Illustration of the case when $V_{\rm IN}$ is lower than the peak value of $v_{\rm ref}$ (t) (a) and pulsewidth modulated signals (b).

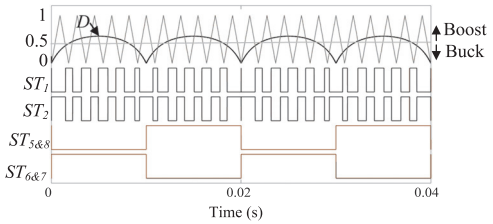

Fig. 4. Switching signals generation for single-inductor twisted unfolding buck–boost inverter when $V_{\rm IN}$ is lower than the peak value of $v_{\rm ref}$ (t).

unfolding inverter can be obtained by comparing the $v_{\rm ref}$ (t) with zero. These last switches operate at the nominal frequency (50 Hz). Fig. 3(b) depicts the switching signal generation if $v_{\rm in}$ is lower than the peak value of $v_{\rm ref}$ (t) with a modulation frequency index equal to 11 for a better representation. The described modulation method is valid for the single-inductor unfolding buck–boost inverter (first circuit) and the tapped-inductor unfolding buck–boost inverter [see Fig. 2(a)].

The same situations to the value of $v_{\rm in}$ in comparison with $v_{\rm ref}$ (t) are possible with the proposed single-inductor twisted unfolding buck–boost inverter but, in this case, the duty cycle is calculated as

$$D = \frac{|v_{\rm ref}(t)|/v_{\rm in}}{1+|v_{\rm ref}(t)|/v_{\rm in}} \tag{6}$$

where D represents the duty cycle of switch S_1, and meanwhile, S_3 has the complementary switching state. Fig. 4 shows how to generate the pulsewidth modulation (PWM) signals for this inverter. It is observed that if D is higher than 0.5, it works in the

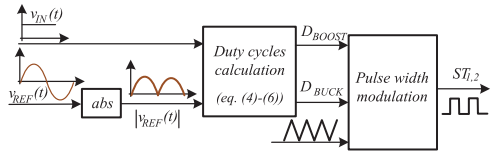

Fig. 5. General block diagram for switching signal generation.

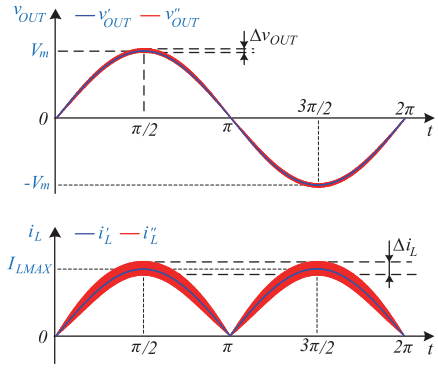

Fig. 6. Waveforms of the output voltage and the inductance current per one fundamental period.

boost mode, otherwise it will work in the buck mode. Finally, Fig. 5 presents the general block diagram in order to obtain the different gate signals by calculating the duty cycles with the aforementioned principle.

IV. Component Design Guidelines

This section provides guidelines for the passive component design taking into account the predefined parameters. Any single-phase inverter has low-frequency current ripple because of the power fluctuation. All high-frequency and low-frequency current and voltage ripples should be taken into account.

Fig. 6 shows the waveform of the output voltage in the unfolding capacitor and current across the inductor. It relates to any of the proposed circuits and has low frequency and high-switching frequency components that are defined as

$$i_L = i'_L + i''_L, v'_{\rm OUT} = v'_{\rm OUT} + v''_{\rm OUT} \tag{7}$$

where i'_L is the fundamental component of the inductor current, i''_L is the high-frequency component of the inductor current, $v'_{\rm OUT}$ is the fundamental component of the output voltage, and $v''_{\rm OUT}$ is the high-frequency component of the output voltage.

These components can be expressed as follows:

$$i'_L = I_{LMAX}\,|\sin(\varphi)|\,,\ i''_L = i_{\rm RIPPLE}(\varphi) \tag{8}$$

$$v'_{\rm OUT} = V_M \sin(\varphi),\ v''_{\rm OUT} = V_{\rm RIPPLE}(\varphi). \tag{9}$$

Fundamental and high-frequency ripple components are changing according to some function, depending on the phase of the output sine. It can be seen that the maximum value of the current ripple is denoted as Δi_L, and the voltage as $\Delta v_{\rm OUT}$.

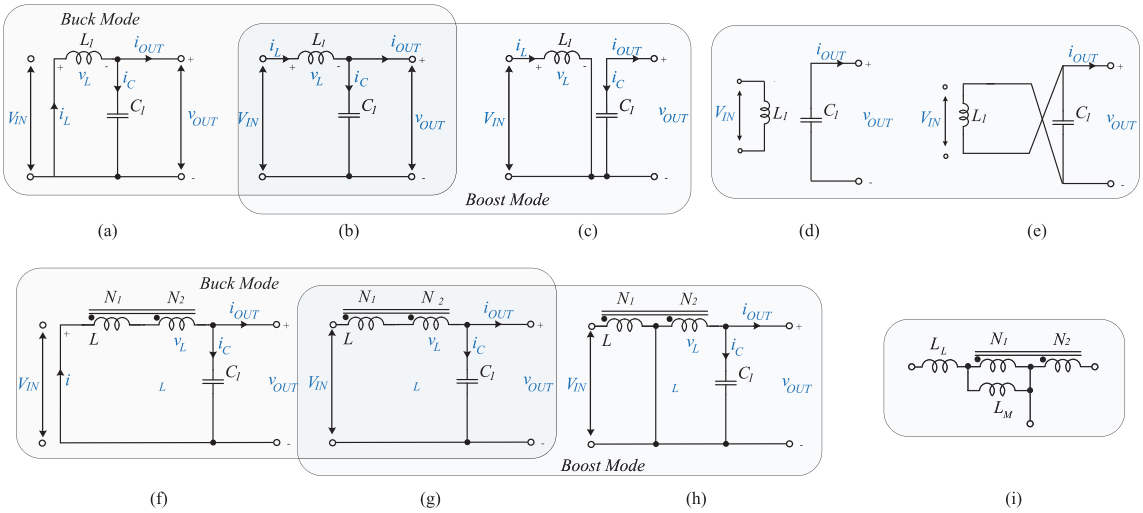

Fig. 7. Equivalent circuits. (a)–(c) Single-inductor unfolding buck–boost inverter. (d)–(f) Tapped-inductor unfolding buck–boost inverter. (g) Equivalent circuit of tapped-inductor. (h), (i) Single-inductor twisted unfolding buck–boost inverter.

In order to find these functions and maximum values, the steady-state modes for all solutions are analyzed.

Any power electronics converter can be represented by means of equivalent circuits. The first [see Fig. 2(a)] and the second [see Fig. 2(b)] solution have a common feature and two different modes, as it was described above. Fig. 7 shows equivalent circuits of the proposed solutions.

Fig. 7(a)–(c) shows the equivalent circuits of the single-inductor unfolding buck–boost inverter. In the case of buck mode, circuits (a) and (b) are involved. Boost mode requires the use of circuits (b) and (c).

Before the passive elements calculation, it should be mentioned that a lossless system is considered

$$P_{\mathrm{OUT}} = P_{\mathrm{IN}} = P. \tag{10}$$

Assuming that the switching frequency is very high and the average value of the inductor current from one switching interval to another is changing, a negligible volt–second balance across the inductor can be applied. It means that the current ripple in the buck mode can be expressed as follows:

$$\Delta i_L = \frac{V_{\mathrm{IN}} - v_{\mathrm{OUT}}}{2L_1} \cdot D_{S1} \cdot T_S \tag{11}$$

where T_S is the switching period and D_{S1} is the duty cycle of the conducting transistor S_1

$$D_{S1} = \frac{v_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \frac{V_M \sin(\varphi)}{V_{\mathrm{IN}}}. \tag{12}$$

It corresponds to the equivalent circuit in Fig. 7(b). Taking into account the value of the duty cycle and the output voltage [see Eq. (4)], it is possible to claim that the ripple value of the current in the inductor depends on the output voltage phase.

As a result, the value of the inductance can be expressed as

$$L_1 = \frac{(V_{\mathrm{IN}} - V_M \cdot \sin(\varphi))}{2P \cdot V_{\mathrm{IN}} \cdot K_L \cdot f} \cdot V_M^2 \cdot \sin(\varphi) \tag{13}$$

where K_L is the high-frequency current ripple factor

$$K_L = \frac{2\Delta i_L}{I_{L\mathrm{MAX}}}. \tag{14}$$

In order to estimate the voltage ripple across a capacitor, the current flow through the capacitor is analyzed. Assuming that the output current is proportional to the capacitor voltage, it is evident that the voltage ripple across the capacitor is caused by the high-frequency current ripple in the inductor

$$\Delta v_{\mathrm{OUT}} = \frac{1}{C_1} \int i_c dt = \frac{\Delta i_L}{8 \cdot C_1} T_S. \tag{15}$$

As a result, the value of the capacitor can be expressed as

$$C_1 = \frac{K_L \cdot P}{4 \cdot V_M^2 \cdot K_C \cdot f} \tag{16}$$

where K_C is the voltage ripple factor.

It can be seen that the current ripple factor K_L has direct impact on the voltage ripple across the capacitor.

The current and voltage ripple can be expressed in a similar way in the boost mode. The only difference lies in the equivalent circuits involved in the boost mode. In particular, the circuits in Fig. 7(b) and (c) are used.

During the state depicted in Fig. 7(c), the output load is fed only by the capacitor, while the inductor is disconnected. It leads to a significant voltage ripple increase.

TABLE I
EXPRESSIONS OF PASSIVE COMPONENTS AND DUTY CYCLE FOR BUCK AND BOOST MODES

	Single-inductor unfolding buck-boost inverter (Fig 2*a*)		Tapped-inductor unfolding buck-boost inverter (Fig 2*b*)		Single-inductor twisted unfolding buck-boost inverter ((Fig 2*c*))
Mode	Buck	Boost	Buck	Boost	Buck-Boost
Inductance	$\frac{(V_{IN}-V_M\cdot\sin(\varphi))}{2P\cdot V_{IN}\cdot K_L\cdot f}\cdot V_M^2\cdot\sin(\varphi)$	$\frac{(V_M\cdot\sin(\varphi)-V_{IN})\cdot V_{IN}^2}{2P\cdot K_L\cdot f\cdot V_M\cdot\sin(\varphi)}$	$\frac{n_1^2\cdot V_M^2\cdot(V_{IN}-V_M\cdot\sin(\varphi))\cdot\sin(\varphi)}{2P\cdot K_L\cdot f\cdot V_{IN}\cdot(n_1+n_2)^2}$	$\frac{1}{2P\cdot K_L\cdot f}\times$ $\times\frac{n_1^2\cdot V_{IN}^2\cdot(V_M\cdot\sin(\varphi)-V_{IN})\cdot(V_M\cdot n_1+V_{IN}\cdot n_2)}{(V_M\cdot\sin(\varphi)\cdot n_1+V_{IN}\cdot n_2)\cdot(V_M\cdot n_1^2+V_{IN}\cdot n_2(2n_1+n_2))}$	$\frac{V_{IN}^2\cdot V_M^2\cdot\sin(\varphi)}{2P\cdot f\cdot K_L\cdot(V_M\cdot\sin(\varphi)+V_{IN})\cdot(V_M+V_{IN})}$
Capacitance	$\frac{K_L\cdot P}{4V_M^2\cdot K_C\cdot f}$	$\frac{2(V_M\cdot\sin(\varphi)-V_{IN})\cdot P}{V_M^3\cdot K_C\cdot f}$	$\frac{K_L\cdot P}{4V_M^2\cdot K_C\cdot f}$	$\frac{2P\cdot n_1\cdot(V_M\cdot\sin(\varphi)-V_{IN})\cdot\sin(\varphi)}{K_C\cdot f\cdot V_M^2\cdot(V_M\cdot\sin(\varphi)\cdot n_1+V_{IN}\cdot n_2)}$	$\frac{2P\cdot\sin^2(\varphi)}{f\cdot K_C\cdot V_M\cdot(V_M\cdot\sin(\varphi)+V_{IN})}$
Duty cycle	$\frac{V_M}{V_{IN}}\sin(\varphi)$	$\frac{V_M\cdot\sin(\varphi)-V_{IN}}{V_M\cdot\sin(\varphi)}$	$\frac{V_M}{V_{IN}}\sin(\varphi)$	$\frac{n_1\cdot(V_M\cdot\sin(\varphi)-V_{IN})}{V_M\cdot\sin(\varphi)\cdot n_1+V_{IN}\cdot n_2}$	$\frac{V_M\cdot\sin(\varphi)}{V_M\cdot\sin(\varphi)+V_{IN}}$
Inductor current ripple	$\frac{(V_{IN}-V_M\cdot\sin(\varphi))}{2L_1\cdot V_{IN}\cdot f}\cdot V_M\cdot\sin(\varphi)$	$\frac{(V_M\cdot\sin(\varphi)-V_{IN})\cdot V_{IN}}{2L_1\cdot f\cdot V_M\cdot\sin(\varphi)}$	$\frac{n_1\cdot V_M\cdot(V_{IN}-V_M\cdot\sin(\varphi))\cdot\sin(\varphi)}{2f\cdot V_{IN}\cdot L_1(n_1+n_2)}$	$\frac{n_1\cdot V_{IN}\cdot(V_M\cdot\sin(\varphi)-V_{IN})}{2L_1\cdot f\cdot(V_M\cdot\sin(\varphi)\cdot n_1+V_{IN}\cdot n_2)}$	$\frac{V_{IN}\cdot V_M\cdot\sin(\varphi)}{2L_1\cdot f\cdot(V_M\cdot\sin(\varphi)+V_{IN})}$
Output voltage ripple	$\frac{K_L\cdot P}{8C_1\cdot V_M\cdot f}$	$\frac{(V_M\cdot\sin(\varphi)-V_{IN})\cdot P}{C_1\cdot V_M^2\cdot f}$	$\frac{K_L\cdot P}{8C_1\cdot V_M\cdot f}$	$\frac{P\cdot n_1\cdot(V_M\cdot\sin(\varphi)-V_{IN})\cdot\sin(\varphi)}{C_1\cdot f\cdot V_M\cdot(V_M\cdot\sin(\varphi)\cdot n_1+V_{IN}\cdot n_2)}$	$\frac{P\cdot\sin^2(\varphi)}{C_1\cdot f\cdot(V_M\cdot\sin(\varphi)+V_{IN})}$

Finally, using similar analysis, the equations for inductance and capacitor definitions are as follows:

$$L_1=\frac{(V_M\cdot\sin(\varphi)-V_{\rm IN})\cdot V_{\rm IN}^2}{2P\cdot K_L\cdot f\cdot V_M\cdot\sin(\varphi)}. \tag{17}$$

$$C_1=\frac{2(V_M\sin(\varphi)-V_{\rm IN})\cdot P}{V_M^3\cdot K_C\cdot f}. \tag{18}$$

It can be seen that both current and voltage ripples depend on the phase of the output voltage. Also, coming from the analysis of the equations obtained, it can be concluded that the boost mode requires larger passive components in order to keep the ripples in a predefined range.

The same analysis was performed for the other two topologies. Fig. 7(d)–(f) shows the equivalent circuits of the tapped-inductor unfolding buck–boost inverter. The operation principle corresponds to the single-inductor solution. The only difference is in the turns ratio of the inductor windings that leads to a wider regulation range of the input voltage. The equivalent circuit of the tapped inductor is illustrated in Fig. 7(g). It consists of the leakage inductance, magnetizing inductance, and ideal transformer with the turns ratio m as being

$$m=\frac{N_2}{N_1}. \tag{19}$$

Such solution may provide a higher step-up ratio. The resulting equations are summarized in Table I.

It should be noticed that the leakage inductance is not desirable in the presented solution because of voltage and current spikes in the semiconductors that it may evoke. The analysis performed is idealized and the leakage inductance is omitted.

Finally, a similar analysis was performed for the twisted unfolding buck–boost inverter, where the equivalent circuits of which are shown in Fig. 7(h) and (i). As it was mentioned above, this solution is different from other ones because it uses the same operation mode for buck and boost cases. As a result, the single equations for inductance and capacitance are presented.

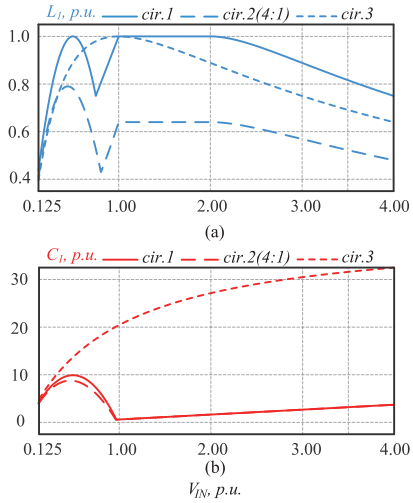

Fig. 8. Capacitor and inductance values as a function of input voltage with constant average input current, constant input current ripple, and constant output voltage ripple for single-inductor unfolding buck–boost inverter and single-inductor twisted unfolding buck–boost inverter. (a) Inductance. (b) Capacitance.

Such representation is convenient because the peak output voltage V_M is a constant value that can be used like a reference. In this case, one unit of input voltage corresponds to the boundary level between the buck and boost modes.

The main idea of Fig. 8 is to show the required value of the passive component for maintaining the same current ripple over the inductor and voltage ripples over the capacitor in a certain operating point.

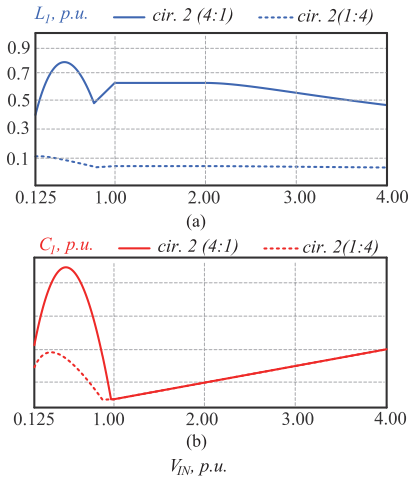

Fig. 9. Capacitor and inductance values as a function of input voltage under different turns ratio with constant average input current, constant ripples, and constant output voltage for tapped-inductor unfolding buck–boost inverter. (a) Magnetizing inductance. (b) Capacitance.

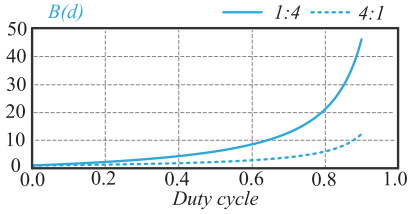

Fig. 10. Gain factor of the boost converter based on a tapped inductor.

Also, it should be mentioned that the average input current is considered as a constant value. These considerations were taken into account due to the PV energy behavior. The PV voltage may change rapidly due to the environmental conditions. The PV system is regarded as the main application of the proposed solution.

The main conclusion from Fig. 8 is that the third solution requires much higher capacitance in value the whole range of the input voltage, while the inductance values are very close, the buck mode demands higher value of the capacitance for all solutions.

Also, an interesting conclusion here is that the largest value of the inductance corresponds to the boundary input voltage between the buck and boost operations.

The second solution is very similar to the first one. The first solution can be considered as a particular case of the second one. To emphasize the difference, Fig. 9 shows the dependencies of the passive elements value versus the input voltage for the second solution under different turns ratios of the tapped inductor. At the same time, Fig. 10 shows the gain factor of the boost converter based on the tapped inductor.

It can be seen that the turns ratio of the tapped inductor gives more freedom in terms of input voltage regulation function. Also, it is possible to achieve the reduction of capacitance and inductance values. Due to the presence of a transformer, a wider range of input regulation can be achieved. At the same time, the overall size of the converter cannot be smaller due to the presence of an ideal transformer in the model.

In summary, to select proper values of passive components, the engineer should define the value of the desired voltage and current ripples in a certain operating point. The operating point is defined by the input voltage and the output power.

Also, switching frequency should be predefined. The value of passive components can be derived by introducing these predefined data into equations in Table I.

V. Simulation Verification of the Proposed Solutions

In order to verify the theoretical statements, simulations were performed for all proposed solutions. Since the PV is announced as possible application field for this type of inverters, the wide range of input voltage is considered with constant average input current. The thin-film PV panels are selected as a case study system. This is novel and growing trend in PV market.

Fig. 11 shows the simulation results for all proposed circuits in the boost mode.

Fig. 11(a)–(c) demonstrates the simulation results for the single-inductor unfolding buck–boost inverter [see Fig. 2(a)].

The input voltage is equal to 100 V, RMS output voltage is 230 V, and output power is about 250 W. High-frequency and low-frequency ripples are shown. It can be seen that the continuous input current is achieved by means of a simple input capacitor. The purpose of the input capacitor is to mitigate high-frequency current ripple. At the same time, its value is relatively small and it can be even smaller. With the present value, a high-switching input current ripple is very minor.

Fig. 11(d)–(f) demonstrates the simulation results for the tapped-inductor unfolding buck–boost inverter [see Fig. 2(b)]. Input voltage is equal to 40 V, the other parameters are the same. Input voltage is reduced in order to demonstrate the possibility of extending the input voltage regulation range. Due to the increased amplitude of input current, the absolute value of the current ripple can be increased as well, and as a result, the value of the magnetizing inductance of a tapped inductor can be decreased compared to the first solution.

Fig. 11(g)–(i) shows similar results for the single-inductor twisted unfolding buck–boost inverter. The input and output parameters are the same as in the first case. Also, the current and voltage ripples are very similar. The main difference lies in the different values of passive components that are summarized in Table II. Such approach of results representation demonstrates how to achieve the same input and output waveforms using different circuits and passive elements.

Finally, Fig. 12 demonstrates similar simulation results for the case when the input voltage is higher than the peak output voltage (450 V). It can be seen that the quality of the input

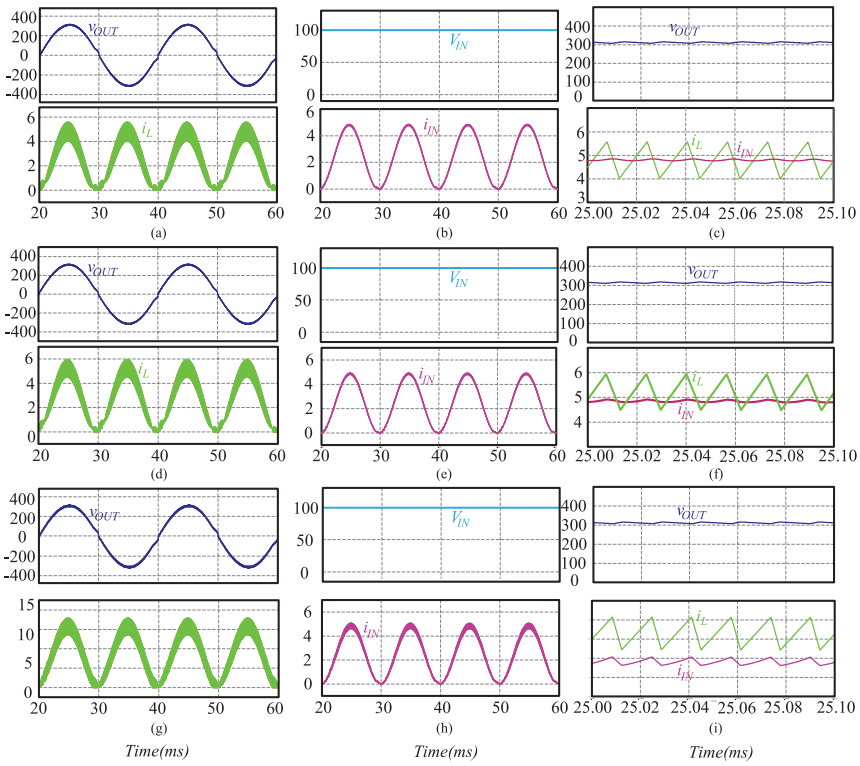

Fig. 11. Simulation results of the proposed circuits for boost case: The output voltage and the inductor's current [(a) for circuit in Fig. 2(a), (d) for circuit in Fig. 2(b), and (g) for circuit in Fig. 2(c)]; the input voltage and the input current [(b) for circuit in Fig. 2(a), (e) for circuit in Fig. 2(b), and (h) for circuit in Fig. 2(c)]; and ripples of the output voltage and of the inductor's current [(c) for circuit in Fig. 2(a), (f) for circuit in Fig. 2(b), and (e) for circuit in Fig. 2(c)].

TABLE II
PASSIVE COMPONENTS VALUES OF PROPOSED SOLUTIONS FOR SIMULATION AND EXPERIMENTAL VERIFICATIONS

Parameter	Single-inductor unfolding buck-boost inverter	Tapped-inductor unfolding buck-boost inverter(4:1)	Single-inductor twisted unfolding buck-boost inverter
Input current ripple	32 %	28%	28 %
Output voltage ripple	2.5 %	2.4%	2.8 %
Input filter inductor, L_0	1 uH		
Input capacitor filter, C_0	60 uF		
Boost inductor (magnetazing inductor), L_1	700 uH		
Unfolding capacitor, C_1	2.1 uF		

current and the output voltage is slightly different. At the same time, the relative value of ripples does not exceed the predefined value. The average input current remains the same. The output power is increased to 1000 W in this case.

The passive components were selected according to the equation presented in Table I. The maximum input current ripple is defined as 20%, while the maximum output voltage ripple is defined as 3%.

VI. COMPARATIVE ANALYSIS OF THE PROPOSED SOLUTIONS

To demonstrate the difference between the proposed solutions and different conventional solutions, a comparative analysis was made. Table III presents several important parameters, such as the number of semiconductors, the number of passive elements, as well as the number of required input power sources. It should be noticed that for a fair comparison, an additional input capacitor is introduced in the solutions with discontinuous input current. Also, the output stage is considered for a simple resistive load; thus, the output capacitor is considered as a filter. Additional inductance is required for all solutions in the grid-connected system.

The reason for the use of the common-mode filter was analyzed as well. It is very important in PV applications. A substantial common filter is not required in all the solutions based on an unfolding circuit because of very small high-frequency component in the common-mode voltage. An intermediate

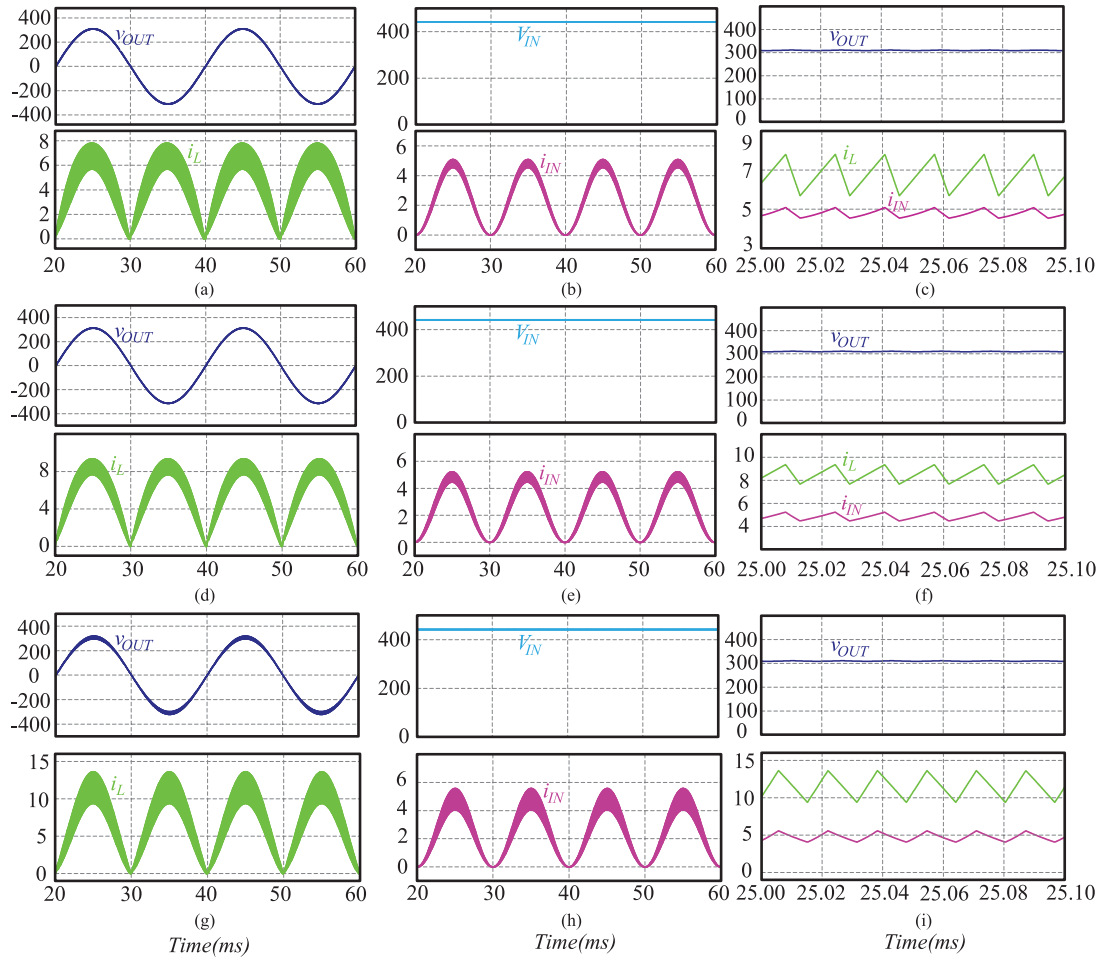

Fig. 12. Simulation results of the proposed circuits for buck case: The output voltage and the inductor's current [(a) for circuit in Fig. 2(a), (d) for circuit in Fig. 2(b), and (g) for circuit in Fig. 2(c)]; the input voltage and the input current [(b) for circuit in Fig. 2(a), (e) for circuit in Fig. 2(b), and (h) for circuit in Fig. 2(c)]; and ripples of the output voltage and of the inductor's current [(c) for circuit in Fig. 2(a), (f) for circuit in Fig. 2(b), and (e) for circuit in Fig. 2(c)].

TABLE III
PARAMETERS OF THE COMPARED SOLUTIONS WITH BUCK AND BOOST PERFORMANCES

Topology	Semiconductors	High Switching Semiconductors	Capacitors	Inductors	Dc-links	Common Mode Filter	Input Power Sources
Boost+VSI	6	6	2	2	yes	yes	1
qZSI	5	5	3	3		yes	1
dc-ac converter based on unfolding circuit	8	2	2	2	yes		1
Aalborg Inverter	10	2	3	2		yes	2
Dual-buck-structured inverter	8	4	3	6			1
Single-inductor unfolding buck-boost inverter	8	2	2	1			1
Tapped-inductor unfolding buck-boost inverter	8	2	2	1 (tapped-inductor)			1
Single-inductor twisted unfolding buck-boost inverter	6	2	2	1			1

dc-link stage is also taken into account. On the one hand, usually it requires a larger capacitor, but may simplify the control system.

Finally, in order to underline absence of high-switching semiconductors in the unfolding stage, an additional column was introduced with a number of active (high switching) semiconductors. For example, despite the large number of semiconductors, an Aalborg inverter may be added that utilizes only two of them during any switching stage. It means lower switching losses. In addition, this is a very important parameter for the EMC design of industrial prototypes.

Several competitive solutions were taken into account in the comparative analysis. The main goal was to cover the main types of converters with different and similar structures. First, the conventional solution with boost and VSI stages was analyzed, followed by a solution with the qZSI inverter that is a typical representative of IS inverters. Detailed comparative analysis of IS inverters is reported in [22]–[24]. As it was mentioned in Section I, the main drawback of the IS-based converters is the large size of passive components as compared to conventional solutions.

Comparative analysis included the dc–ac converter based on an unfolding circuit [see Fig. 1(b)] along with an Aalborg inverter [see Fig. 1(c)] because of the presence of similar features. Also, the dual-buck-structured inverter is represented in Table III.

Table III reveals that the proposed solutions have evident advantages in terms of the number of passive components and high-switching semiconductors. Neither do the solutions suffer from the leakage current problem. The main drawback lies in the four consecutive conducting semiconductors that may lead to increased conduction losses. At the same time, due to the substantially reduced switching losses, this drawback can be balanced.

Comparison of the presented solutions with that in Fig. 1(b) shows that the main difference lies in the changed sequence of the buck and boost stages. The main drawback of such solution is in two inductors. In the first section, L_1 is working in the boost mode, and in the second, L_2 is in the buck mode. In order to provide the converter operation in a wide range of input voltage, both inductors should be large enough, while the proposed solutions have a single inductor utilized in a back and boost cases. Also, proposed solutions give more freedom in the further topology deviation [see Fig. 2(b) and (c)].

Comparison of the proposed solutions with an Aalborg inverter reveals that the main advantage of the proposed solutions lies in the reduced number of semiconductors and passive components. The same is valid for dual-buck-structured inverters, where the number of inductors and high-switching devices are higher.

At the same time, it should be noticed that in the engineering practice, to compare only the number of passive components or semiconductors appears not to be a mature approach. A single inductor can be much larger and more expensive than several smaller inductors. In order to validate the hypothesis of the reduced size of the passive components, our focus in the analysis will be on the stored energy.

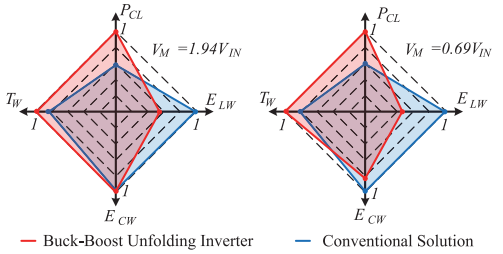

Fig. 13. Comparative analysis of the proposed solution vs. conventional solution based on the boost dc–dc converter and VSI both in the boost and buck modes.

The main assumption is that the volume of the magnetics $\underline{Vol}_{\underline{\mathrm{L}}}$ is proportional to the stored energy

$$E_{\mathrm{LW}} = \sum_{i=1}^{N} \frac{L_i \cdot I_{\mathrm{MAX}_i}^2}{2} \tag{20}$$

which is estimated by means of the inductance L and the maximum inductor current I_{MAX}; and N is the number of inductances. Such parameter allows the estimation and comparison of the required number of magnetic elements, their sizes, and cost for a certain topology. Similar parameters can be introduced for the capacitors

$$\mathrm{E_{CW}} = \sum_{i=1}^{N} \frac{C_i \cdot V_{\mathrm{MAX}i}^2}{2} \tag{21}$$

where E_{CW} is the total energy stored in the capacitors.

It is well known that the size, volume, and cost of the capacitors strictly depend on the maximum voltage and capacitance. The size of the passive elements depends strongly on the material and switching frequency, but these parameters can be assumed to be the same for all compared solutions.

In order to make the analysis more comprehensive, the conduction losses along with the voltage stress on the semiconductors are also considered.

To estimate the contribution of semiconductors to the topologies above, their number and blocking voltage was also taken into account

$$T_W = \sum_{i=1}^{N} V_{BTi}. \tag{22}$$

To compare the conduction losses P_{CL}, the same MOSFETs transistors were taken into account. In this case, conduction losses of semiconductors are proportional to the RMS value of the current that can be accurately estimated by a simulation tool.

Fig. 13 shows the diagram that illustrates the results of the comparison. Axes illustrate the parameters described above. This diagram corresponds to the case with a minimum size of passive components for the conventional boost and VSI solution [see Fig. 1(a)] and one of the proposed solutions [see Fig. 2(a)]. These two solutions were selected as the most promising among compared solutions.

The first case [see Fig. 13(a)] corresponds to the boost mode, where the input voltage $V_{\rm IN}$ is much smaller than the peak output voltage V_M. In the opposite case [see Fig. 13(b)], the input voltage is higher than the peak output voltage.

In both cases, the predefined 20% input current and the 1% output voltage ripple are provided by means of proper passive components. Double-frequency ripple was not eliminated and only high-frequency ripple was considered.

It should be mentioned that in the proposed solution, the front-end input filter is used to mitigate high-switching input current ripple in correspondence with the conventional solution. The filter consists of very minor series resistance and inductance that usually is present in the wires and an additional capacitor C_0. This filter is included in the summarized results.

The main conclusion from the diagrams above is that the proposed buck–boost inverter with the unfolding circuit has a lower value of inductance and energy stored in the inductor in any mode. The overall size of the capacitors in the proposed solution is significantly smaller in the buck case [see Fig. 13(b)]. All the parameters are represented in relative units, while the switching frequency is the same.

It is evident that the conduction losses as well as the overall number of semiconductors are higher. At the same time, as it was mentioned above, the expected switching losses are much lower.

Also, it should be taken into account that transistors with a very low open drain-source resistance can be selected for unfolding circuits. Usually, such type of MOSFETs has an internal diode with very poor dynamic performance that is neglectable in this solution. It means that despite a higher number of semiconductors, higher overall efficiency is expected. Another possible alternative is the commercially available low-voltage thyristors that are a very good option from the cost point of view.

In addition, in the comparison, the continuous open-loop control system for the dc-link voltage was implemented in the simulation. It means that the minimum value of dc-link capacitance in the conventional solution will not be sufficient for experimental realization, which has limited switching frequency and computational delay. The same is not valid for the proposed solution where the dc-link control is not required.

VII. Experimental Study

Taking into account the results presented above, the single-stage buck–boost inverter with an unfolding circuit [see Fig. 2(a)] is selected for experimental study as an optimal solution in terms of passive component size. Also, compare to the solution in Fig. 2(c), it has reduced voltage across semiconductors.

Fig. 14 shows the experimental setup for the studied solution. The passive elements correspond to the simulation study. It consists of the inverter printed circuit board (PCB) board, the control board, and inductor. The small input film capacitor is used. The inductor is based on the serial connection of the coupled inductor with inductance 700 μH and saturation current 20 A (size is 30, 60, 65 mm). All the diagrams are derived by the digital oscilloscope Tektronix MDO4034B-3, current probes

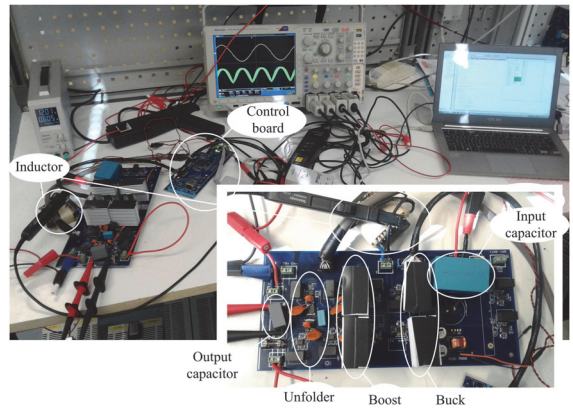

Fig. 14. Experimental setup of the single-stage buck–boost inverter with unfolding circuit.

Tektronix TCP0150, and voltage probes Tektronix TPA-BNC. The control system is based on the low-cost field-programmable gate array, which allows realization of any PWM technique with high-resolution and high-switching frequencies.

The high-switching part of the prototype is based on the MOSFET transistors IPW65R041CFD along with SiC diodes C3D10065A. The unfolding circuit is based on the MOSFET transistors IPB60R060P7ATMA1 with poor dynamic characteristics but very low static losses. The buck and boost cases, in correspondence with simulation results, are shown in Fig. 15. Fig. 15(a)–(c) demonstrates experimental results for the single-inductor unfolding buck–boost inverter [see Fig. 2(a)] when the boost mode is required. It is fully corresponding to the simulation results. The input voltage in this case is equal to 100 V, the RMS output voltage is 230 V, and the output power is about 250 W. Inductor current i_L along with output voltage $V_{\rm OUT}$ is illustrated as measured in Fig. 15(a).

Fig. 15(b) shows the input voltage $V_{\rm IN}$ along with the input current $i_{\rm IN}$. It can be seen that due to the input capacitance, input current has smaller high-frequency ripples compare to the inductor current. High-frequency ripple of the input current, inductor current, and output voltage are shown in Fig. 15(c). The average value of the input current is about 2.5 A.

In order to show the maximum possible power for this input voltage, Fig. 15(d)–(f) demonstrates similar diagrams for 1000 W. It can be seen that due to the high average value of the input current, the ripple seems very small. The input voltage has some ripple also because it corresponds to the maximum possible current.

The case when only the buck operation mode is used is shown in Fig. 14(g)–(i), and in this case, the input voltage is equal to 450 V. Input current remains the same as in the first case, while the output power increased to 1100 W. Due to higher input voltage, the high-switching current and voltage ripples are increased.

At the same time, the value of the ripples corresponds to the theoretical estimation. This point corresponds to the nominal operation point and was verified by simulation as well.

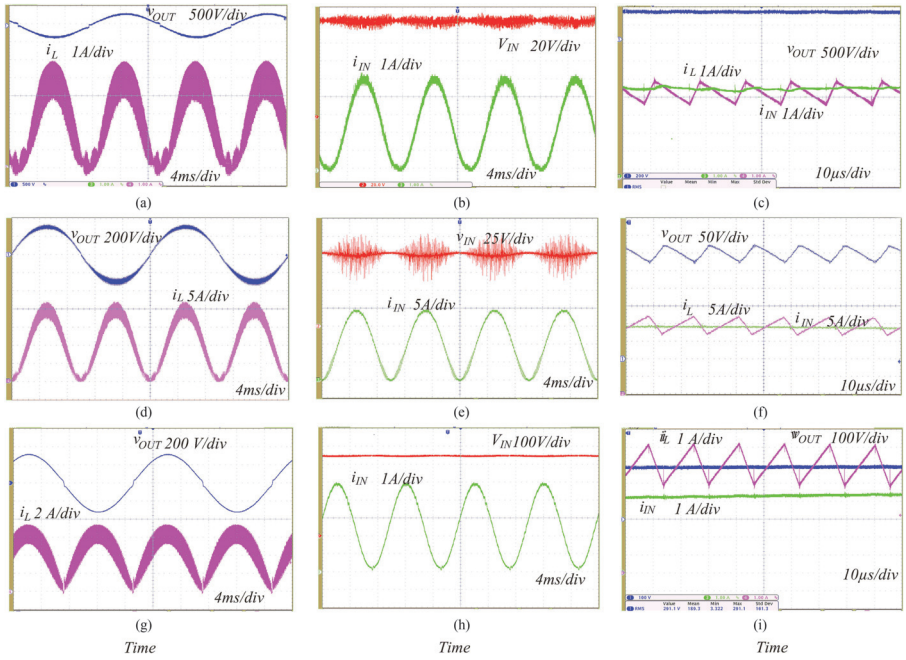

Fig. 15. Experimental results for the first proposed circuit: Boost case (a)–(c) with 250 W, boost case (d)–(f) with 1000 W, and buck case (g)–(i) with 1100 W.

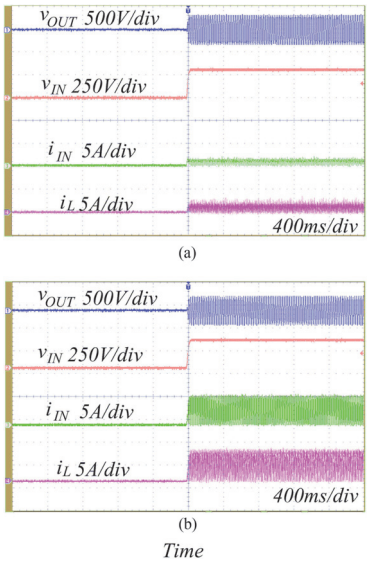

Fig. 16. Dynamic response on the input voltage step from 0 to 300 V.

Finally, Fig. 16 shows the dynamic response of the converter. Input voltage is changed from 0 to 300 V. There is no any significant current and output voltage oscillation. Fig. 16(a) corresponds to the 200 W, while Fig. 16(b) corresponds to the 1000-W input power.

The efficiency of the converter was also estimated. The very precise four wire measurement method by means of Yokogawa WT1800 was used. Fig. 17(a)–(c) shows pictures from the thermal camera.

In the first case of reduced input voltage, the boost mode is activated. In this particular case, the boost mode prevails over the buck mode due to the very low-input voltage and the losses are mostly caused by transistors S_1, S_3, and diode S_4, which is confirmed by Fig. 17(a), where the thermal picture of these transistors is illustrated. The total efficiency in this case is more than 96%.

At maximum possible current [see Fig. 17(b)], which corresponds to the experimental results in Fig. 15(d)–(f), the total efficiency decreased to 92.5%. The relatively lower efficiency is explained by the low-input voltage while the current is very high. Also, Fig. 17(b) shows that unfolding transistors have high temperature. At the same time, the losses are not very high because there is no heatsink. The thermal dissipation is going through the printed circuit design board.

Fig. 17(c) shows the inverter board during the buck mode. It can be seen that in this case, transistor S_1 has higher temperature than the other ones. This transistor works with maximum current and switching losses. In this case, the efficiency is almost 98%. This is achieved due to the MOSFET transistors with low drain-source resistance and a minimum number of switching semiconductors is used.

The efficiency profile as the function of input voltage with constant current is illustrated in Fig. 17(c). The reduction in the efficiency with a voltage drop is explained by the decreased level of the input power. At the same time, Fig. 17(e) shows the

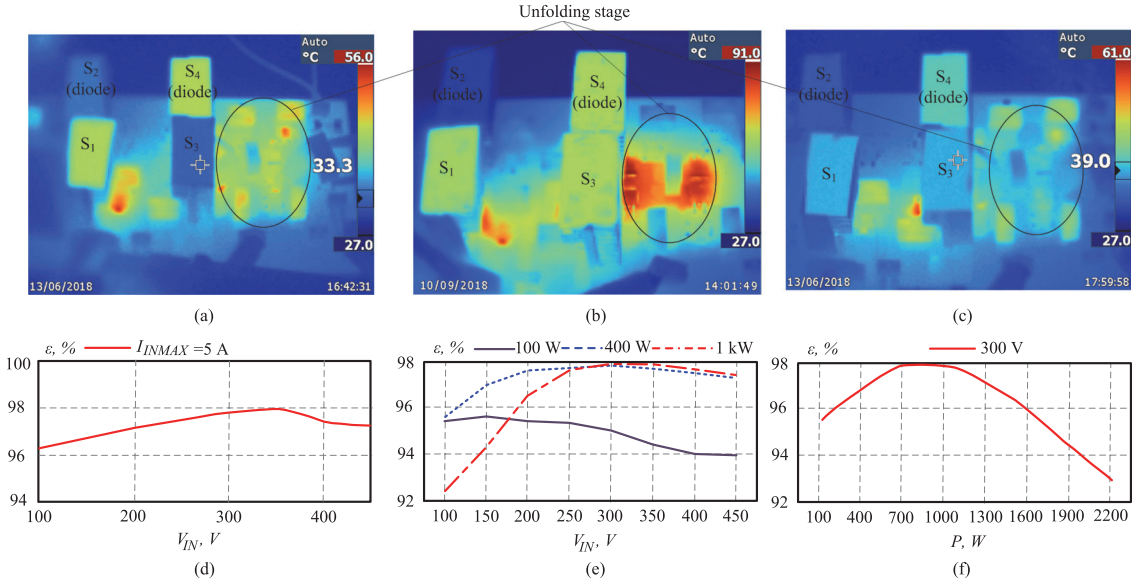

Fig. 17. Efficiency study of the proposed solution: (a) Thermal picture in the boost case with 250 W. (b) Thermal picture in the boost mode with 1000 W. (c) Thermal picture in the buck mode with 1000 W. (d) Efficiency vs. input voltage with constant input current. (e) Efficiency vs. input voltage with constant input power. (f) Efficiency vs. input power with constant input voltage.

dependence of the efficiency as the function of the input voltage with constant power. The power was investigated in a range from 100 to 1000 W. The main conclusion is that the converter may work with high current and low voltage. At the same time, the PV profile with high voltage and low current is preferable. It is evident, that the maximum possible power is different for different input voltage. For example, only 800 W was possible to get with 80-V input voltage, but 2200 W was provided to the output when input voltage was 300 V. The efficiency curve as a function of input power with constant input voltage is shown in Fig. 17(f).

It should be noted that each of the high-switching semiconductors has the same separate heatsink (5.3 C/W). It is done on purpose in order to estimate losses in each semiconductor. However, the selected approach of heatsink design is not optimal. In industrial terms, common heatsink for all high-switching semiconductors will be better. In this case, the losses will be more equally distributed and maximum temperature of the semiconductors will be lower. It means lower drain-source resistance and higher efficiency. Finally, Fig. 18 shows the losses distribution for 1000 W at 450 V [see Fig. 18(a)] and 100-V [see Fig. 18(b)] input voltage. Due to the separated heatsinks, it is possible to estimate total losses in each semiconductor. The current in the semiconductor along with the case and heatsink temperature can be measured. Taking into account datasheet parameters, and current in semiconductors, the conduction losses can be estimated separately. It can be seen that conduction losses have major contribution in both cases. Also, it is evident that conduction losses are increasing during the input current increase.

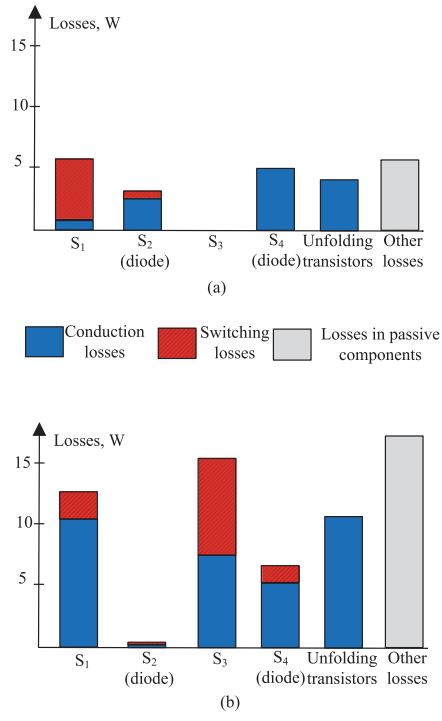

Fig. 18. Losses distribution for 1000 W at 450 V [see Fig. 18(a)] and 100 V [see Fig. 18(b)] input voltage.

At the same time, it can be seen that losses in the passive components are present as well. It means that this issue can be optimized as well.

The main conclusion from the thermal pictures and the efficiency study is that a converter may have high efficiency in a wide range of input voltage. At the same time, in any period of operation, only two transistors are involved in the high-switching performance that, in turn, lead to reduced switching losses and EMI compared to the conventional solutions. Due to dominant conduction losses, the application at higher input voltage and lower input current can be recommended. It means that the proposed solutions can be recommended for PV applications where higher power corresponds to higher voltage.

VIII. Conclusion

This paper has presented a novel family of buck–boost inverters using output unfolding circuit. Component design guidelines along with modulation techniques are given. Simulation and experimental results confirmed the theoretical analysis.

It is demonstrated that the main advantage of these solutions is the reduced size of passive elements in a wide range of input voltage regulation. It is achieved due to the direct dc to ac energy conversion without any dc-link stage.

Despite the increased amount of semiconductors, the overall efficiency can be very high because only two semiconductors are involved in high-switching performance in any period of operation. The solutions proposed can be recommended for PV applications where high power corresponds to high voltage. In advance, it gives reduced EMI compared to any other competitive solutions. At the same time, a continuous input current is achieved.

The proposed modifications of the buck–boost inverters provide high selection flexibility. The buck–boost inverter with a tap-inductor and output unfolding circuit may provide very high step-up solutions. Another valuable advantage is the common voltage shape, which contains no high-switching frequency components. As a result, leakage current problem does not exist for PV application.

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Novel Concept of Solar Converter With Universal Applicability for DC and AC Microgrids

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***Abstract*—This article presents a novel concept of a universal solar converter suitable for application in both in the dc or single-phase ac grids using the same terminals. The idea lies in the utilization of the same semiconductors in the dc–dc and in the dc–ac configuration, resulting in minimal redundancy. Possible semiconductor stages are considered. The particular attention is focused on the output filter design along with proper protection circuit selection for dc and ac grids. The design example and comparative analysis between dc–dc, dc–ac, and universal solutions are given. The experimental prototype of the universal solar converter that is rated for 3.6 kVA power in the ac mode and 5 kW in the dc mode is presented. The experimental results demonstrate the ability of operation in ac or dc grids with main correspondent modes. Possible fields of application along with main benefits are addressed in conclusions.**

***Index Terms*—DC–AC converter, dc–dc converter, solar converter, universal converter.**

I. Introduction

THE constant growing energy demand of humanity exacerbates the development of sustainable energy such as solar power, wind power, and other forms of renewable energy sources (RESs) that can replace fossil fuels. At the same time, it becomes obvious that storage elements are required to balance the grid that contains high penetration level of RESs.

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Many years have passed since the Tesla-Edison war of the currents. However, because most of the RESs and battery storages are dc-based, the topic of using dc devices is reviving with renewed vigor [1], [2]. Hence, dc microgrids are becoming a modern trend [3], [4]. It is well known that ac voltage level can be easily stepped up or down by means of a transformer. Effective electrical energy distribution systems can be constructed. According to some reports, it is already proved that a high-voltage dc (HVdc) distribution system is more efficient than a high voltage ac system in several cases [5]. In particular, it was demonstrated bringing offshore wind power to shore [6]. Due to the latest research efforts in power electronics, the HVdc transmission system may replace an ac system in the coming decades. Power electronics facilities can provide step up or step down performance [7]. The cost of such solution is still a challenge.

The dc low-voltage distributed system may become a reality even sooner [8]–[10]. From both the technical and the economical point of view, the most suitable dc voltage level seems to be 326 V [9]. It has been shown that this voltage is readily applicable to existing systems, which makes it possible to use the existing cables. Some other preliminary research shows that the dc voltage level from 350 to 380 V is considering to be like a future standard [11]. Due to the simplicity of storage systems or renewable energy integration, reduction of power electronics stages in many devices connected to the conventional ac grid, this solution is attracting researchers' efforts targeted to implementation. At the same time, it is evident that immediate transition from the ac to the dc grid is infeasible. In the nearest decade, we will observe a merge of the dc and the ac systems.

There is a trend to consider future power electronics converter solutions simultaneously suitable for dc and ac applications [12]. For example, so-called hybrid converters have dc and ac terminals and correspondent internal power electronics. In the most cases, it relates to the hybrid solar converters where an additional dc terminal is intended for battery storage connection. There are few examples when the converter has dc-link terminals for dc grid connection along with ac grid. In a very general case, these converters are called multiport converters [13]. The idea of universal multiphase converters is presented in [14]. Due to the high number of input/output terminals, these solutions can be used in single-phase ac, multiphase ac, and dc applications. Another option is power electronics facilities for power flow control between residential dc and ac grid. These types of

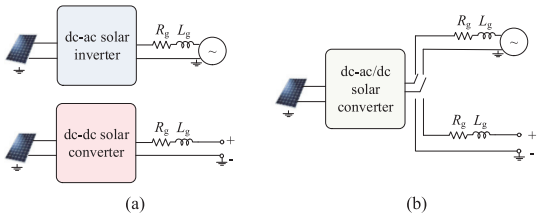

Fig. 1. Motivation and concept demonstration of the universal solar converter. (a) DC–DC and dc–ac string solar converters as independent solutions. (b) Universal single-phase string solar dc–dc/ac converter.

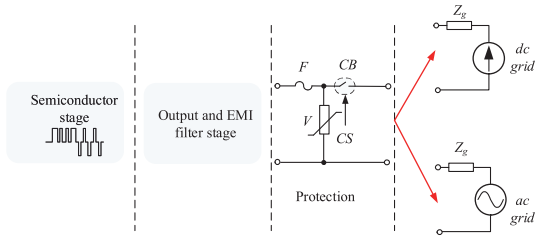

Fig. 2. Simplified structure of the universal dc–dc/ac converter that contains semiconductor part, output filter, protective circuits and dc or ac grid with impedance.

converters can be called energy routers. They have terminals for dc and ac grids [15]–[17]. They can be applied for the energy distribution system and residential applications.

At the same time, all above-mentioned converters have significant redundancy if it is necessary to provide energy from/to power source to/from the grid, but type of the grid is not defined. We predict that some universal converters that accept both dc or ac grid by the same converter terminals with minimal internal redundancy will be required. This work is devoted to the novel concept of a universal solar converter that is applicable for both the dc and the ac grid. This article is organized as follows. Section II describes the concept of universal converters. Section III analyzes and discusses the possible semiconductor stages. Section IV is devoted to the output filter selection and protection issues. Section V shows a design example of the universal solar converter and comparison with conventional solutions. Finally, experimental results are presented in Sections VI. Section VII concludes this article.

II. Concept of the Universal DC–DC/AC Converter

The motivation of the universal solar converter solution is illustrated in Fig. 1. Fig. 1(a) shows solutions for string solar applications expected to be available on the market in the nearest decade. Along with conventional string solar dc–ac inverters, we can expect the appearance of string dc–dc converters targeted for the dc grid integration of PV plants. The same conclusion belongs to the market of solar microinverters. The isolated dc–dc solar optimizers are available for customers. There are several companies that target market of the future dc–dc solar optimizers and string dc–dc converters [18].

At the same time, as an alternative solution, the universal dc–dc/ac converter illustrated in Fig. 1(b) can be proposed for customers. Such solution will provide flexibility and independence of the type of available residential grid. The same features belong to any renewable energy converters.

Fig. 2 shows a simplified structure of the universal solar (dc–dc/ac) converter that contains a semiconductor part, an output filter along with an electromagnetic interference (EMI) filter, protection circuits and the dc or the ac grid with corresponding impedance. This is an example of the universal solution, which is considered as interface between the dc input voltage source and ac or dc residential grid. It is evident that similar structure can be considered for ac voltage source as well. In a very general case, if assume that semiconductor stage may have high-frequency isolated stage, this solution can be generalized for any application.

The main goal of this work is to define the demands for power electronics converters and their possible internal structure in case of capability of the universal dc or ac operation and pits feasibility for application.

III. Possible Semiconductor Stage of the Universal Solar Converter

Fig. 3 shows several solutions as possible semiconductor stage for the single-phase universal string solar converter. First of all, Fig. 3(a) shows that even the conventional voltage source inverter (VSI) with an intermediate boost dc–dc converter can be connected to the dc grid. A good overview of the conventional single-phase solar inverters is presented in [19]–[23]. Many of the existing dc–ac converters can work in the dc–dc mode. More complex solutions, like high step-up inverters [24] or common-ground inverters [25] also can be considered as competitive solutions. At the same time, they may have inherited limitations from dc–ac mode like limited power range or lower efficiency.

In this particular case [see Fig. 3(a)] in order to provide dc output voltage the transistor S_2 have to be in a conductive state while transistors S_3 and S_4 are in synchronous mode providing buck operation. Fig. 3(b) shows another possible example of the proposed universal single-phase solar converter. In fact, this is an interleaved synchronous buck-boost converter. A similar solution based on a boost converter with common input voltage source was disclosed in [26] for the dc to the ac application, which can work in the bidirectional mode. A similar approach recently proposed for a three-phase rectifier in [27] is a phase-integrated converter (PIC).

The third example as a solution for a universal single-phase solar converter is a buck-boost inverter with unfolding circuit [see Fig. 3(c)]. This solution is shown as part of the family of inverters with unfolding circuit [28]. At the same time, it is evident that this solution can be easily adapted for the dc–dc operation simply by changing the control strategy and without any impact on redundancy. Despite the relatively high number of the series semiconductors, this solution has the minimal number of simultaneously switching semiconductors, which leads to the significant reduction of the switching losses. Also, it does not have a high-frequency component in the common-mode voltage

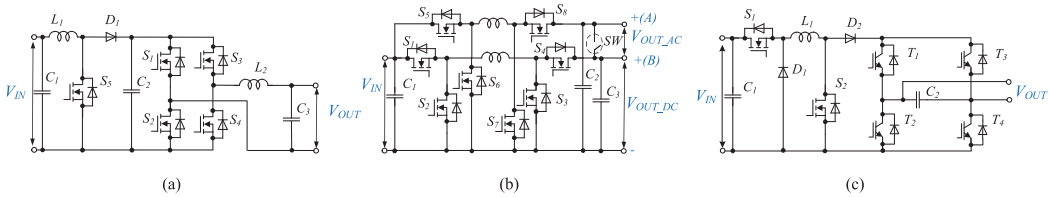

Fig. 3. Possible solutions of the universal nonisolated single-phase solar converter. (a) VSI derived universal dc–dc/ac converter. (b) Buck-boost derived universal dc-dc/ac converter. (c) Buck-boost converter with unfolding circuit as universal dc–dc/ac converter.

that eliminates problems with leakage current in case of solar application.

Finally, it is the single stage energy conversion solution that provides wide input voltage range regulation without dc-link capacitor [28]. As a conclusion from Fig. 3, it can be stated that the semiconductor stage for universal application can be derived from the different types of converters. Fig. 3(a) represents VSI (or dc–ac) derived semiconductor stage, while Fig. 3(b) shows how to derive a dc–ac operation in case of initial dc–dc configuration. Finally, converter with unfolding stage can naturally provide dc or ac output voltage without any redundancy.

IV. Protection Circuits and Output Filter Selection for AC- and DC-Grid Integration

Any semiconductor stage can not be separately considered without output filter and protection stages in any power electronics converters. This section is devoted to the selection of the output filter along with a proper protection circuit. The main goal is to provide a desired power quality and a safety level in both the dc and the ac operation mode.

A. Protection and Grounding Issues

First of all, the single-phase ac protection circuit is a well-known and standardized solution (IEC 61869, IEC 60255, IEC 61850, and IEC 60834). Usually, it contains Circuit Breaker (CB), fuse *F* as overcurrent protection and varistor *V* as overvoltage protection. Also, EMI is required to cancel higher harmonics propagation. In case of a sudden fault, most of the ac electromechanical CBs disconnect appliances during the zero-crossing point, which is the principal mechanism of fault isolation. A typical fault clearing time in ac transmission systems is 80 ms (4 cycles for 50 Hz system), including 2 cycles relay tripping time and 2 cycles circuit breaker operating time [29]. DC grid has numerous advantages and is already considered as a future electric transmission system [30], [31]. However, designing an appropriate protection system for dc microgrids has been a serious challenge over the past years [32]–[36]. A target fault clearing time in dc transmission systems can be 2.5 ms [11].

The structure of the possible protection circuit between the power electronic converter and the low voltage dc grid can be the same. The main problem lies in the nature of the dc fault current, which can rapidly increase to more than a hundred times the nominal current during sudden fault inception. In the dc microgrid, the line impedance Z_g is very low. As a result, fault current deviation is too high, and the fault current reaches hundreds of amps in less than a couple of milliseconds. It means that ac protection technologies cannot be fully transferred to dc grid protection. DC grid protection requires higher bandwidth, higher communication speed, and sophisticated relay coordination and breaker functionalities [35]. Possible CB solutions like solid-state relays are presented in [33]–[36]. These solutions require such key features as fast response, high reliability, low conduction loss, long lifetime, and low cost. At the same time, if a CB solution can satisfy demands for dc grid protection, it is certain to suit for the ac grid as well.

Grounding is another issue, which belongs to the safety and protection. The grounding approach of ac systems is well known while the grounding issue of dc systems is still under discussion. It is evident that dc and ac systems will be coexisting in the future distributed grid. The main problem can be in a potential difference between ac and dc grounds. In case of ac system, the ground may have the same potential as neutral ground while the dc bus lines derived by rectification of the ac voltage can not be directly connected to the ac ground. There are several solutions already discussed in the literature [37]–[39]. The first solution consists of the galvanic isolation of ac and dc systems by transformers. Another solution consists of the grounding through high impedance. At the same time, all grounding approaches belong to the dc grid side and do not have a direct impact on the discussed universal solutions. If the discussed converter is adopted for the conventional ac system, where the impedance between ground and neutral wires are low, it will be definitely working with dc grounded system.

Leakage current is another important issue that is interconnected with grounding. It is particularly important for all transformerless converters connected to the grid. Despite the grounding solution, in the most cases, it is solved by simple common-mode filters [40] that can be easily integrated into above-discussed filters. Also, leakage current can be mitigated by modulation techniques [41]. Also, it should be mentioned that topological solutions based on unfolding circuits have very small high-frequency common-mode voltage component and do not require any additional common-mode filters [28] in ac mode. At the same time, in case of dc grid connection, it will have a common ground wire with a grid that eliminates the problem with a leakage current.

B. Output Filter Selection

Another parameter to conform to both of the requirements is the output current quality. In the ac grid, filters with inductors

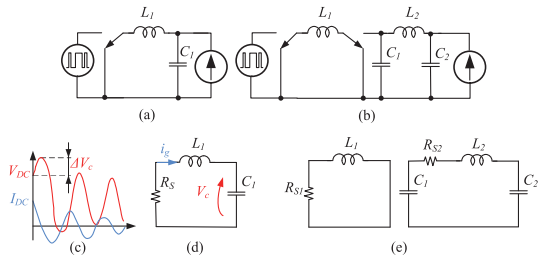

Fig. 4. Illustration of the switching process during sudden dc-grid disconnection. (a) Disconnection schematic for *LC*-filter. (b) Disconnection schematic for the *LCLC*-filter. (c) Transient process of the output voltage and inductor current. (d) Equivalent circuit of the *LC*-filter. (e) Equivalent circuit of the *LCLC*-filter.

from the grid side are preferable due to the controllability of the grid current. In most cases of the *LC*-filter application, the grid side inductance is assumed to be present like internal grid impedance. The design process is well-known and widely studied [42]–[45].

The dc grid as well as the converters connected to the dc grid is an emerging topic [46], [47]. However, output filter design is not addressed. In all cases, the capacitor is used from the dc grid side, but its value is not specified. In a first approximation, a simple grid side capacitor can be considered as an output filter. This simple filter can be used in the boost-derived converters where the internal inductor is not directly connected to the output capacitor. Also, simple *LC* filter can be considered for a conventional buck converter [see Fig. 4(a)]. In both cases, the grid side capacitor C_1 has to be small enough in order to smooth grid connection with the minimal current spike in case of any voltage difference before connection. In the steady-state grid connected mode, this capacitor does not have a direct impact on the grid current quality, but at the same time, it should be mentioned that the grid side capacitor C_1 is very important to eliminate the output voltage spike in the case of sudden dc grid disconnection. It means that this capacitor is a suppressor capacitor required to limit possible voltage spike.

The *CLC*-filter [see Fig. 4(b)] can be considered as a further derivation of a *C*-filter suitable for boost-derived converters. In this case, the first capacitor C_1 along with the inductor L_1 are main filtering elements, while the output grid side capacitor C_2 is a suppressor. Fig. 4(d) shows the simplified equivalent circuit of a sudden dc grid disconnection process in case of *LC* filter. Straight after detecting a sudden dc grid disconnection, the control system has to short circuit the output side of the converter in order to minimize the voltage spike ΔV_C across the capacitor C_1.

The idealized transient waveforms are shown in Fig. 4(c). It will be accompanied by oscillation. In the analysis of the above process that describes the equivalent circuit in Fig. 4(d), we can derive a set of differential equations

$$L_1\frac{di_g(t)}{dt} = -i_g(t)R_S - v_C(t),\ C_1\frac{dv_C(t)}{dt} = i_g(t). \quad (1)$$

The initial conditions are defined as follows:

$$v_C(0) = V_{DC},\ i_g(0) = I_{DC} \quad (2)$$

where V_{DC} is a dc grid voltage at the moment of disconnection, while the I_{DC} is a grid current at the moment of disconnection. It is evident that straight after disconnection due to the energy accumulated in the inductor the voltage across output capacitor is starting to grow up to reaching maximum value $V_{C\cdot MAX}$. The solution of (1) is simple but is very bulky. The series resistance defines the damping ratio of this oscillation but does not have a significant influence on the maximum value $V_{C\cdot MAX}$. Neglecting this resistance R_s, it is possible to derive a simplified expression of the maximum voltage maximum across capacitor. It can be assumed that all energy accumulated in the inductor is flowing to the capacitor

$$\frac{C_1\cdot(V_{C\_MAX}^2 - V_{DC}^2)}{2} = \frac{L_1\cdot I_{DC}^2}{2}. \quad (3)$$

Finally, the expression for the voltage spike ΔV_C across the capacitor C_1 can be obtained

$$\Delta V_C = (V_{C\_MAX} - V_{DC}) = \cdot\sqrt{\frac{L_1}{C_1}I_{DC}^2 + V_{DC}^2} - V_{DC}. \quad (4)$$

The value of the voltage spike is proportional to the initial current and filtering inductance, while it is opposite to the value of the suppressing capacitor. As a result, design guidelines have to take into account maximum acceptable voltage spike across the capacitor and maximum power of the converter. In the case of *CLC*- and *LCLC*-filters, Fig. 4(e) shows the equivalent circuit for the estimation of the voltage spike across the suppression capacitor at a sudden dc grid disconnection. Based on this circuit, the expression for the suppression capacitor can be derived in a similar way of solving differential equations. Using the same approach demonstrated in (3) and (4), we can show that voltage spike across suppression capacitor can be defined as follows:

All other passive components of the converter side part of the filter can be calculated similar to the classical approach [42]–[46], [48] keeping the ripple in the current as a main parameter to be reduced.

In summary, to provide universality of the protection circuit and the output filter, the CB has to satisfy the demands for dc grid protection, while the output filter can be designed as a filter for conventional ac application with an additional small output capacitor (suppressor) to eliminate voltage spike at a sudden grid disconnection.

V. Design Example of the Universal Solar DC/AC Converter and Comparison With Conventional Solutions

In this section, the design example of the conventional solar inverter, dc–dc solar converter and universal solar converters are given. The same dc-dc buck-boost cell is selected as the semiconductor stage for all solutions in order to analyze the redundancy of the discussed solutions. Fig. 5 shows the selected solutions. They will be compared in terms of size of passive

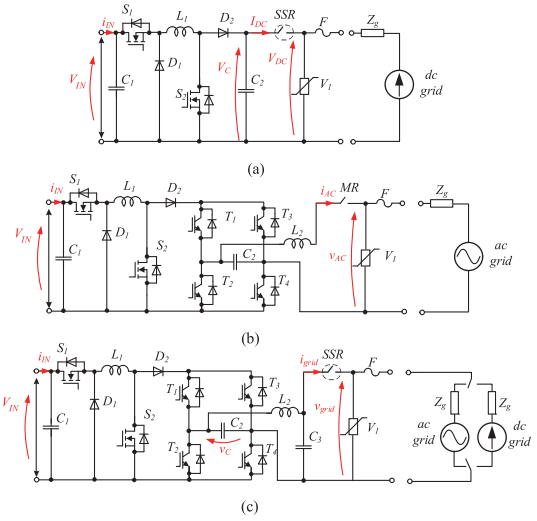

Fig. 5. Competitive solutions rated for 3.6 kW. (a) Solar dc–dc converter. (b) String solar inverter. (c) Universal single-phase solar converter.

TABLE I
TARGET PARAMETERS OF THE SOLAR CONVERTER

Parameters	Value
RMS grid voltage V_{grid}, V	230 AC/400 DC
Output power range P, W	100-3600/100-500
Input voltage range, V	100-600
MPPT voltage range, V	150 – 450
Maximum input current, A	10
Switching frequency	62 kHz

components, semiconductors, number of voltage and current sensors, and protection circuit's requirements.

Table I shows the target parameters of the solar converter. On the one hand, it corresponds to the typical market representative of the single-phase solar inverter [49]. On the other hand, it has a double type output voltage specification: 230 V ac grid and 400 V dc grid.

All solutions are designed for the same input voltage range, maximum input current, and nominal output power. First, we assume that the same high-switching semiconductors are considered for all solutions. It is explained by the same voltage stress across semiconductors and the same switching frequency. The maximum voltage stress is defined by maximum input voltage. The difference between efficiency in the different modes is discussed in the experimental section.

In order to estimate the contribution of the semiconductors to the discussed solutions, their number and maximum blocking voltage are also taken into account

$$S = \sum_{i=1}^{N_S} V_{BS}. \tag{6}$$

The switching frequency range has to be in agreement with electromagnetic compatibility (EMC) standards that define 150 kHz as a minimum frequency of the conducted emissions (EN61000-6-3). As a result, in most commercial solar converters, 65 kHz is recommended as a maximum switching frequency in order to satisfy EMC requirements. The ac grid has a slightly smaller peak voltage compare to the dc grid. It means that unfolding transistors in the universal solution have to be rated to the slightly higher output dc voltage that will be taking into account in (6).

The next step is to select passive components. In case of dc–dc converter, the capacitor C_1 is selected to provide a high-frequency current mitigation.

Its value can be neglected compare to the capacitor C_1 for ac application. In this case, large electrolyte capacitor is required in order to provide the PV panel's voltage ripple $\Delta V_{PV}/V_{PV}$ not higher than 3–4%. It is assumed that PV current ripple has to be limited to 10%. These numbers are enough to provide maximum power point tracking (MPPT) efficiency not less than 99% that is industrial standard [50]. In our case 4 mF capacitor is required in order to provide double-frequency power decoupling. All other passive components have to be calculated taking into account requirements to the output capacitor value that is discussed above. In case of dc–dc converter C_2 is a suppressor capacitor and does not have direct influence on the quality of injected current. It means that inductance L_1 defines the current ripple and can be calculated for the buck and boost modes

$$L_1 \geq \frac{V_{DC}}{K_L \cdot I_{DC} \cdot f_{SW}}\left(1 - \frac{V_{DC}}{V_{IN\_MAX}}\right)$$
$$L_1 \geq \frac{V_{IN}}{K_L \cdot I_{DC} \cdot f_{SW}}\left(1 - \frac{V_{IN}}{V_{DC}}\right) \tag{7}$$

where K_I is the output current ripple coefficient and $V_{IN\cdot MAX}$ is a maximum input voltage. Similar analysis can be found here [51].

There is no any significant voltage spike expected in case of grid disconnection in the dc–dc converter illustrated in Fig. 5(a). It is explained by the possibility of the inductor decoupling. Thus, the upper value of the capacitor C_2 is limited only by possible current spike during the grid-connection process. According to (7) setting, the output current ripple not higher than 5% the inductance L_1 has to be equal to 4.2 mH.

Guidelines for the design of an output filter for an inverter based on unfolding circuit are given in [52]. It belongs to the dc–ac operation mode [see Fig. 5(b)]. Taking into account the same output current ripple coefficient, we can obtain very similar values for L_1, C_2, and L_2. These and other values are summarized

$$\Delta V_{C2} = \frac{2C_1C_2V_{DC} + 2C_2^2V_{DC} + I_{DC}\sqrt{(C_1^2C_2 + C_2^2C_1)\cdot L_2}}{2\cdot(C_1C_2 + C_2^2)} - V_{DC}. \tag{5}$$

TABLE II
RESULTS OF COMPARISON

Parameter	Operation mode		
	dc-dc	dc-ac	dc-dc/ac
Decoupling capacitor, μF	5	4000	4000
Capacitor C_2, μF	1	1.3	1.3
Capacitor C_3, μF			1
Inductor L_1, mH	4.2	1.6	1.6
Inductor L_2, mH		0.33	0.33
Number of high-switching semiconductors	4	4	4
Number of low-switching semiconductors	0	4	4
Speed of relay disconnection, 1/sec	400	12.5	12.5
Number of sensors	5	4	5

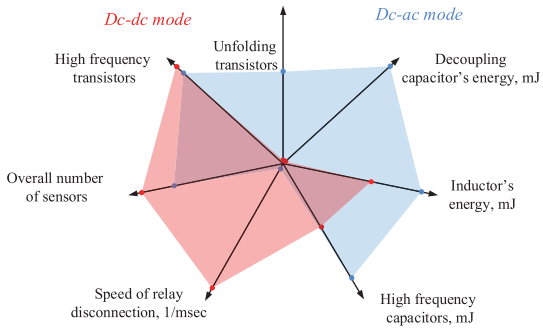

Fig. 6. DC–DC and dc-ac mode comparison.

in Table II. The same components can be used for universal solution [see Fig. 5(c)] along with additional suppression capacitor C_3. In this case, the suppression capacitor has to be calculated taking into account the already defined value of inductors L_1, L_2, and capacitor C_2. From (5), in order to keep voltage spike not higher than 20% of the nominal dc-link voltage, the suppression capacitor has to be not smaller than 0.9 μF. It corresponds to the nominal 9 A output dc current. Also, it should be noted that configuration of the output filter selected for universal solution requires a larger suppression capacitor value, but significantly smaller overall size of inductors.

Finally, the results of comparison are illustrated in Fig. 6. There are many specific parameters that are taken into account. In the above-presented analysis, the values of passive components were defined. However, it is well known that the size and cost of the passive components are defined by the maximum accumulated energy and technology of manufacturing [53].

Assuming the same technology for the same types of components, we can analyze the accumulated energy

$$\mathrm{E}_L = \sum_{i=1}^{N_L} \frac{L_i \cdot I_{MAXi}^2}{2}, \mathrm{E}_C = \sum_{i=1}^{N_C} \frac{C_i \cdot V_{MAXi}^2}{2} \qquad (8)$$

where L and C are estimated inductances and capacitances, I_{MAX} and V_{MAX} are the maximum inductor current and maximum capacitor voltage. For convenience and generalization of the analysis, N_L and N_C are number of components. The most important conclusion that despite on the higher required inductance value in the dc-dc mode, the size of the inductor is slightly smaller due to the absence of low-frequency ripple. As it was pointed out, the fast relay is required in the dc–dc grid. In order to count this parameter into the comparative diagram, we introduced the speed of relay disconnection, which is the reciprocal value.

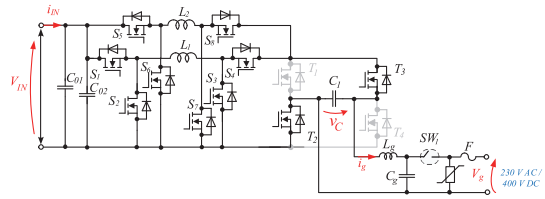

Fig. 7. Universal single-phase 3.6 kW (5 kW) dc–dc/ac solar converter selected for experimental verification.

TABLE III
PROTOTYPE PARAMETERS AND COMPONENTS

Parameter	Value (Size)
Capacitors $C_{01} = C_{02}$	2.1 mF (0.57 dm^3)
Capacitor C_1	1.3 μF (0.009 dm^3)
Inductors L_1, L_2	1.6 mH (0.55 dm^3)
Grid side inductance L_g	330 μH (0.27 dm^3)
Grid side capacitance C_g	1 μF (0.008 dm^3)
Switching frequency	62 kHz
High switching frequency transistors S_2, S_3, S_6, S_7	IMZ120R030M1H
High switching frequency transistors S_1, S_4, S_5, S_8	C3M0021120K
Unfolding circuit transistors T_1-T_4	FCH060N80

Finally, the number of sensors in order to implement the stable operation of the converter is taking into account. In case of dc–ac operation, usually the grid voltage is measuring only, while dc–dc mode requires control of the output voltage from the converter side in order to provide output capacitor precharging. In order to generalize the results of the comparison, all values are given in relative scaled units. Low values of the parameters demonstrated in the diagram correspond to the best case. Such approach allows demonstrating redundancy of the universal solution. At the same time, it can be seen that the most significant redundancy lies in the requirements to the relay and the necessity of output suppression capacitor. If dc–ac converter will be accompanied by these features and proper control it can be adapted to the universal application.

VI. EXPERIMENTAL VERIFICATION

Due to the lower passive component count, finally, the solution based on unfolding circuit was selected as the most promising for experimental verification. Fig. 7 shows the realized experimental prototype of the universal dc–dc/ac converter rated for 3.6 kVA power in the dc–ac mode and 5 kW in the dc–dc mode. Converter specifications are listed in Table I.

Provision of high efficiency and smaller size of inductors is enabled by the interleaving approach of the high-switching cell, which is a common approach for industrial solutions. The parameters of the output filter along with other components are shown in Table II. Their values correspond to the above-presented design of the converter. Table III summarizes the passive components along with semiconductors that are selected

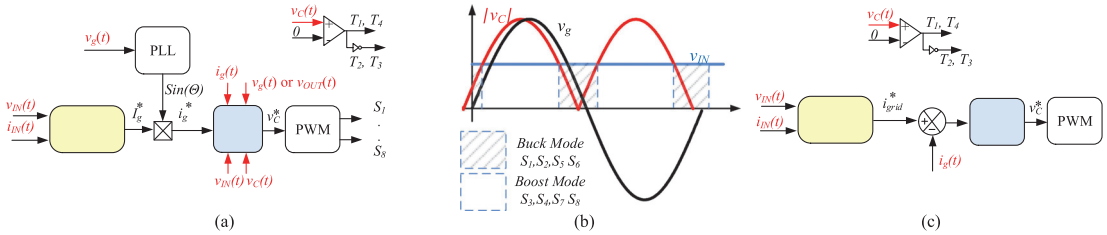

Fig. 8. Control system illustration and prototype. (a) DC–AC mode. (b) Diagrams of the control approach in the dc–ac mode. (c) Sketch of the dc–dc mode.

to provide reference efficiency. MOSFETs FCH060N80 are used as power switches in unfolding circuit. These are conventional Si transistors with poor dynamic but good static characteristics. The SiC transistors C3M0021120K were selected as high-frequency switching transistors for S_1, S_4, S_5, S_8. It was shown in [28] that these switches have a significant contribution in terms of conduction losses and have to be optimized. At the same time, IMZ120R030M1H were selected as high-frequency switching transistors for S_2, S_3, S_6, S_7. They have slightly worse static characteristics but lower price. All the semiconductors have significant voltage blocking value that corresponds to industrial solutions and provides reliable operation.

A. Control System Description

Fig. 8 shows the control system that was realized in order to provide both modes of operation. It discloses dc–ac mode [see Fig. 8(a)], diagrams of the control approach in the dc–ac mode [see Fig. 8(b)] and dc–dc mode [see Fig. 8(c)]. The proportional resonant controller belongs to the PI-based linear regulators that were first proposed in [54]. This controller is often found in inverter applications [55]–[57]. At the same time, our preliminary research demonstrated that this approach may have a zero-crossing distortion and nonlinear control can be applied in order to solve this problem [58]. It was shown that the model predictive control (MPC) is a suitable technique to provide desired output current. Fig. 8(b) shows the sketch of the grid voltage and absolute value of the unfolding capacitor voltage. The absolute value of the unfolding capacitor voltage defines the common-mode voltage waveform. It demonstrates the control system approach. MPC block defines the reference value of the unfolding capacitor voltage v_C^*, which is given to pulsewidth modulation (PWM) block as a modulation signal. The PWM block defines the high-switching transistor states, while simple comparator defines the state of the unfolding circuit.

The phase shift between unfolding capacitor voltage and grid voltage defines the grid current amplitude and phase. As any other solar inverter, it can inject active and reactive power. Such an approach provides very good dynamics and robustness of the control system. In advance, it can provide off-grid operation. In this case, the grid current is replaced by output voltage in the cost function calculation.

Fig. 8(c) shows the sketch of the dc-grid control system. It is quite similar to the ac system in terms of unfolding the control

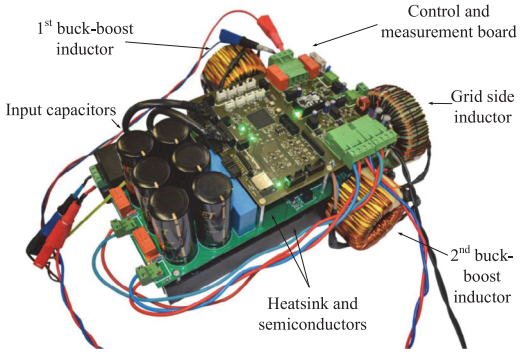

Fig. 9. General view of the 3.6 kW (5 kW) laboratory prototype of the universal single-phase dc–dc/ac converter.

circuit. Depending on the polarity of the output terminals, the corresponding switches are conducting. In this case, the converter is the conventional buck-boost dc–dc converter and does not suffer from zero-crossing distortion. As a result, the MPC block can be replaced by the conventional PID controller. It provides a reference value of the unfolding capacitor voltage which in turns defines the grid current value. The reference grid current is defined by the MPPT block that is designed based on well-known incremental conductance method with output integrator [59], [60].

B. Experimental Setup Description

Further, we describe the experimental verification of the proposed solution. All the measurement results were obtained by voltage probes Tektronix TPA-BNC, current probes Tektronix TCP0150 and by the digital oscilloscope Tektronix MDO4034B-3. For testing different PV profiles and operating points, Chroma 62150H-1000S power supply (PV simulator) was used. Precision power analyzer YOKOGAWA WT1800 was used to estimate the efficiency. The dc voltage source along with the dc electronic load were used to emulate the dc grid.

The experimental setup is shown in Fig. 9. It has a common heatsink for all semiconductors, which helps to dissipate the power losses and equalize the temperature of semiconductors. It has two printed circuit boards (PCB); the top PCB contains measurement circuits and the control system realized on

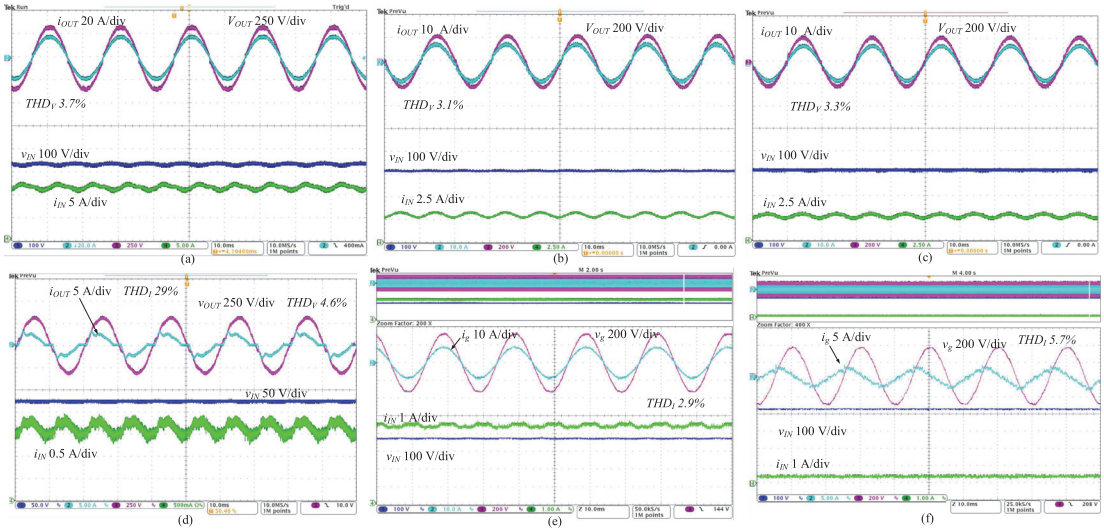

Fig. 10. Experimental results of the steady-state ac operation modes.(a) Only active component in the off-grid mode. (b) Capacitive load in the off-grid mode. (c) Inductive load in the off-grid mode. (d) Nonlinear load in the off-grid mode. (e) Grid-connected mode with pure active power. (f) Reactive power injection in the grid-connected mode.

TMS32028379DPTPT. This is a μC with two cores and two subcores specially designed for power electronics application and allows realizing any complex control algorithm. The bottom PCB contains capacitors, semiconductors, and relays.

The experimental study was targeted to achieve several aims. The first aim was to evaluate the operation of the universal converter in the dc and the ac modes. Detailed efficiency study of the solutions in different operating points was a second goal. The different PV profiles that correspond to Table I can be connected to the designed converter.

C. Operation Evaluations

In the case of ac operation, the grid-connected and off-grid mode along with different load impacts were evaluated. Fig. 10 is devoted to the demonstration of steady-state operation in the grid-connected and off-grid modes. The steady-state operation in the off-grid mode under maximum power is presented in Fig. 10(a). It can be seen that the performance of the converter corresponds to the expectation. Also, the operation with capacitive and inductive loads are shown in Fig. 10(b) and (c) correspondently. In these cases, the active component was two times reduced, while reactive component was introduced. In the first case, a 15-μF capacitor was added in parallel, in the second case, a 2-mH inductance added in series. Phase shift between the output voltage V_{OUT} and current i_{OUT} is recognizable in case of capacitive load, and very small in the case of an inductive load.

Fig. 10(d) shows the converter performance in the off-grid mode in the case of a nonlinear load. The simple half-bridge rectifier with electrolytic capacitor and resistive load was connected. Compared to the previous cases, the output voltage waveform is slightly distorted but acceptable. If in case of linear load, the voltage THD_V was about 3–4%, in case of nonlinear load it was about 5% while current THD_I was about 30%. Commercial uninterruptible power supply inverters cannot provide ideal output sinusoidal voltage V_{OUT} [61] in such load condition.

The ac grid-connected mode is illustrated in Fig. 10(e). It shows the half of the maximum power. Even in this case the THD_I of the grid current i_g is less than 3%. Further power increase leads to the power quality improvement. The pure reactive power injection capability is illustrated in Fig. 10(f). Due to the nonlinear nature of the converter, a slight distortion is observed, but not significant. This feature can be demanded in some modern applications.

Fig. 11 is devoted to the different transient modes. Fig. 11(a) shows the capability to inject distorted current to the grid. Such feature can be used in applications capable of providing ancillary services (e.g., in active filtering) to the utility grid and in islanding detection. Also, it demonstrates good dynamic characteristics of the converter. Fig. 11(b) shows the same reference current generation in the islanding mode. In this case, the correspondent voltage shape changes is observed and it can be used for islanding mode detection. Finally, the load step change is shown in Fig. 11(c). It demonstrates capability of the grid-forming operation. The MPC control recognizes a load change and reacts correspondently.

Fig. 12(a) shows the steady-state diagrams for the dc grid operation. It can be seen that in this case almost ideal ripple-free input and output currents can be observed in the steady-state mode. The rapid changing of the reference current does not evoke any problems. The grid-connection process is very smooth and has no specific features in ac operation mode. Fig. 12(b) shows

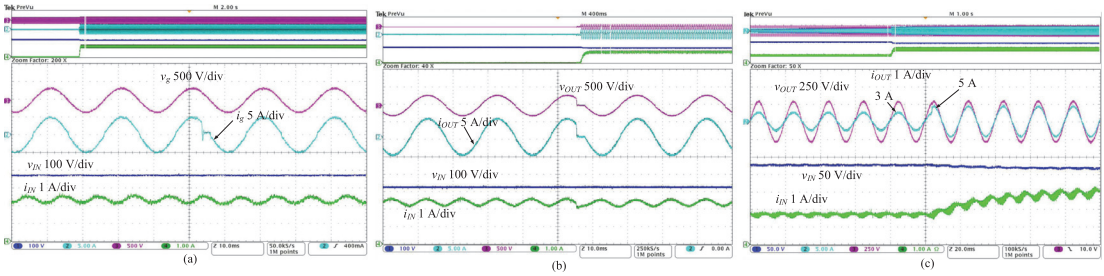

Fig. 11. Experimental results in transient conditions. (a) Distorted reference current in the grid-connected ac mode. (b) Distorted reference current in the off-grid ac mode. (c) Load step change in the off-grid ac mode.

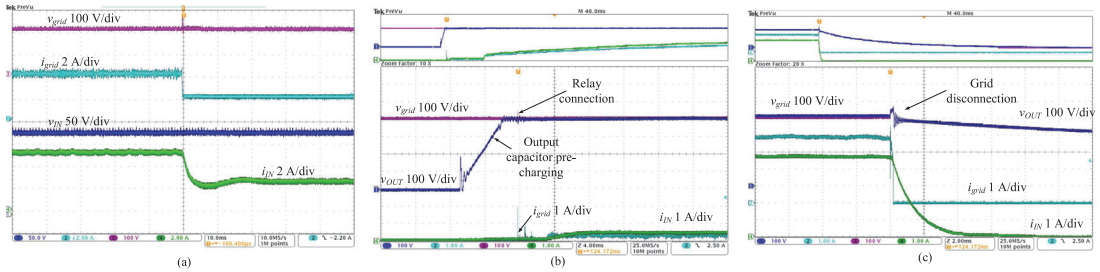

Fig. 12. Experimental results. (a) Waveforms of the universal single-phase dc–dc/ac converter in the dc operation: steady-state mode. (b) During connection to the dc grid. (c) Disconnection of dc grid.

a start-up process in the case of dc residential grid. It can be seen that at the very beginning the output voltage v_{OUT} across output capacitor C_g is equal to zero. Due to the initial precharging of the suppression capacitor, there is no significant current spike during grid connection, nor is there any voltage spike during the load step.

A sudden grid disconnection case is more complex and is shown in detail in Fig. 12(c). It can be seen that at some moment of time, the grid current falls to zero, which means that the grid was disconnected. Straight after that, the voltage across the output capacitor is starting to grow. The control system that detects this process immediately stops high switching transistors operation and sets transistors S_2, S_6, S_7, S_3 in the conducting mode. It is only for a few seconds when the output capacitors are fully discharged that the converter operation can be stopped. It helps to discharge the unfolding capacitor and mitigates the voltage spike across the output capacitor and the energy that is accumulated in the buck-boost inductors is dissipating through the drain-source resistance of transistors. It means that this energy does not create any voltage spikes across capacitors. From another side, the energy that is accumulated in the grid side inductor L_g is dissipating in the circuit created by grid side inductor, unfolding capacitor C_1, and grid side capacitor C_g. It means that both capacitors are involved in the voltage spike mitigation. As a result, the spike across output capacitors does not exceed 25% of the nominal voltage. This is one of the features that provide competitive advantage to the solutions with unfolding circuits in terms of safe margin operation.

The above presented experimental results show that the proposed solution can work as a conventional solar inverter with ancillary services like reactive power injection or islanding operation and solar dc–dc converter. The detection of islanding operation can be implemented based on conventional algorithms for ac [62] and dc operation modes [63].

A. Efficiency Study

The very precise four wire measurement method by means of Yokogawa WT1800 was used. The power was investigated in a range from 150 to 5 kW. In both the ac and the dc cases, the peak efficiency ε is higher than 98%. This is achieved due to the use of minimum number of switching semiconductors. The efficiency profile as the function of the input voltage with constant input current is illustrated in Fig. 13(a). The blue dotted line corresponds to the ac output mode study while the solid red line corresponds to the dc output mode study. A wide range of current was considered. The first case corresponds to the input current 8 A. Another diagrams are shown for 1 A input current.

It can be seen that, in case of reduced current, the efficiency is lower, which is normal and partially explained by auxiliary power supply consumption, which is constant and does not depend on the operating power. The reduction in efficiency with a voltage drop is explained by the decreased level of the input power. A similar effect can be observed with the current increase.

Fig. 13(b) shows the efficiency dependence as a function of input power under constant input voltage. It can be seen that peak of the efficiency curve in the dc–ac mode corresponds to

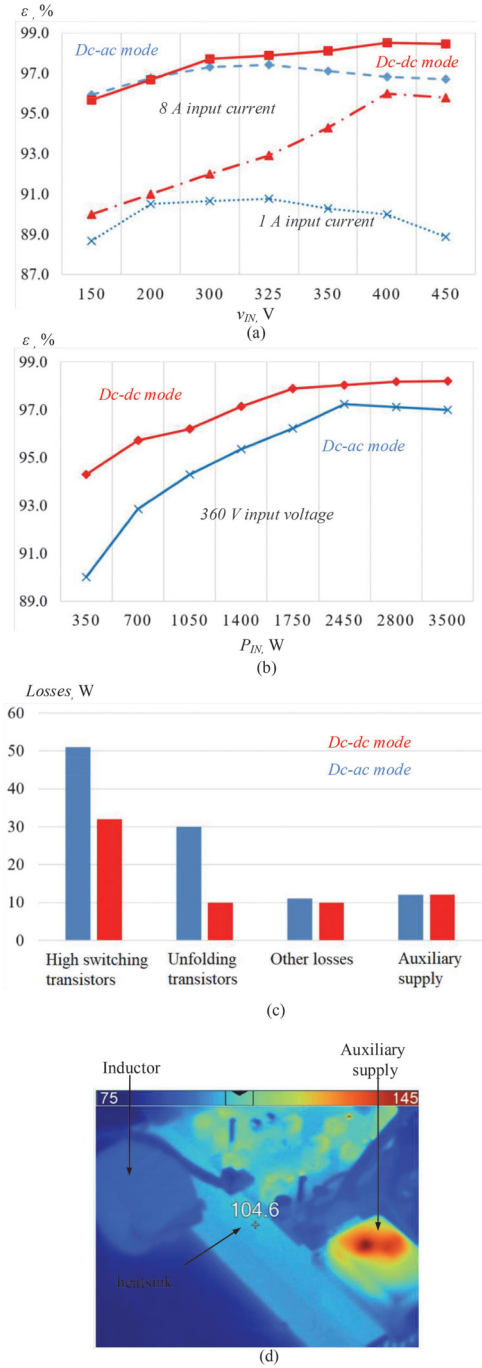

Fig. 13. Efficiency study of the proposed solution. (a) Efficiency versus input voltage with constant input current with ac and dc mode. (b) Efficiency versus input power with constant input voltage with ac and dc mode. (c) Losses distribution in the ac and dc modes. (d) Thermal image of the converter in the ac mode.

nominal power, while there is no decline in the efficiency curve in the dc–dc mode. Due to the higher efficiency in the dc–dc mode, the input power can be increased up to 5 kW.

An important conclusion from the efficiency study is that dc–dc mode is more efficient almost at any point. The dc mode operation does not have any double frequency ripple that leads to more efficient operation. Some superior performance of ac mode can be observed in the points with low input voltage where dc mode requires a slightly higher boost. In most of the other points, the difference in the efficiency between the dc and the ac application is around 1%.

Fig. 13(c) shows the losses distribution that corresponds to 360 V input voltage and nominal power 3.6 kW. The losses in semiconductors were estimated by temperature measuring. Only two simultaneously switching semiconductors explain relatively low losses in the high-switching stage at any moment of time. It can be seen that auxiliary supply circuits create some losses contribution that are significant in case of low power operation. It is also interesting to note that losses in the unfolding circuit in the dc mode are three times smaller than in the ac mode. It is explained by a smaller output current RMS value for the same power. Other losses belong to losses in the inductors, capacitors, and wires and are calculated by means of subtraction of the overall losses and defined losses in the semiconductors and auxiliary supply. In advance, Fig. 13(d) shows the thermal picture of the converter in the ac mode at nominal power 3.6 kW. It can be seen that the heatsink temperature is about 42 °C (104.6 °F) that corresponds to the expectations. In addition, it can be seen that the hottest point corresponds to the auxiliary supply.

The main conclusion from this section is that the highest efficiency about 98.6% corresponds to 400 V input voltage operation point with the output dc grid. This operation point has minor dynamic losses of semiconductors. Almost in all other points the dc mode is more efficient as well. It means that converter designed for 3.6 kW power in ac mode can handle more power in the dc mode due to the absence of double frequency ripple. At the same time, the efficiency of the converter in dc–ac mode is not inferior to commercial solutions.

VII. Conclusion

This article presented a novel concept of the universal solar converter suitable for the dc and the single-phase ac application. The main goal was to elaborate converter featuring minimal redundancy.

Different semiconductor stages, output filter design along with proper protection circuit selection for dc and ac grids were considered. All possible modes were verified by means of experimental prototype. Based on the results of the research, it was possible to underline that the main redundancy of the proposed universal solar converter compared to the dc–ac application consists in the CB requirements to be adopted for the dc grid application and generalized for all types of solutions.

The design process had to take into account that dc application required a grid side capacitor to fix the converter voltage before connection to the grid and store energy at sudden disconnection.

At the same time, it had to be quite small to avoid significant current spike during grid connection. Other passive components designed for ac grid utilization will be definitely suitable for dc applications.

If to summarize the power electronics converter initially designed for dc–ac application with modification of the output filter stage and fast relay can be considered as a universal solution. This approach can be recommended for industrial solutions for low voltage dc and ac grids. DC–DC mode was more efficient in the most of operating points due to the absence of the double-frequency power ripple. It means that the dc mode can be rated for higher power.

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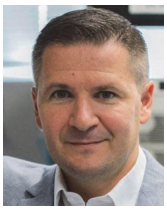

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Feasibility Study of Model Predictive Control for Grid-Connected Twisted Buck–Boost Inverter

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***Abstract*—This article studies the model predictive control (MPC) for a twisted buck–boost inverter based on unfolding circuit. The focus is on the practical implementation of the MPC algorithm for the microcontroller designed for application in power electronics. Selection of proper cost function parameters along with a continuous control set reduced prediction horizon, at the same time keeping good quality of the grid current. The results showed that simplified differential equations and a multicore microcontroller contribute to the sample time reduction, which in turn increases the sampling frequency with the corresponding increase in the output current quality. The simulation and experimental results confirmed theoretical predictions. In conclusion, the MPC technique suits for reducing zero-crossing distortion and in applications based on unfolding circuit.**

***Index Terms*—Boost, buck, inverter, multicore systems, power electronics, predictive control.**

I. Introduction

NUMEROUS topologies and relevant techniques exist in the field of power electronics. In the most common case, the integral-based techniques are used for power electronic converters. For example, the proportional resonant (PR) controller is often found in inverter applications [1]–[3]. PR controllers allow the fundamental harmonic with rather high accuracy of the grid current to be supplied. Besides, an additional resonant is used to suppress unnecessary frequency.

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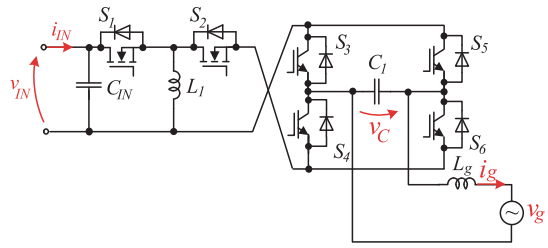

Fig. 1. Buck–boost twisted dc–ac converter based on unfolding circuit.

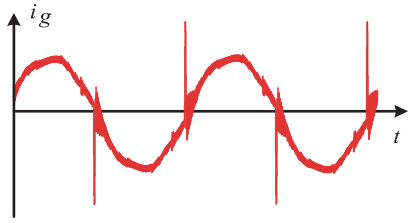

Fig. 2. Zero-crossing distortion of the grid current in a buck–boost inverter with unfolding circuit based a PR controller.

A combination of various techniques in a single system can be applied [4]. Integrated control methods allow one to eliminate the steady-state error [5]–[7]. Such techniques do not require faster sample rate in many cases.

Another auxiliary technique allows to overcome the delay problems. The repetitive controller (RC) with phase-lead compensation mutually with proportional integral (PI) is shown in [8]. The bidirectional grid-connected inverter reported in [9] showed precise tracking for the periodic reference signal based on RC.

However, the integral control methods do not provide high accuracy during the whole set range of the input power. This issue is especially evident in nonlinear circuits. The family of the buck–boost inverters based on unfolding circuits is presented in [10]. The twisted buck–boost inverter based on unfolding circuit described in [11], [12] is shown in Fig. 1.

The topologies based on unfolding circuit may have spikes near grid voltage zero-crossing [13], [14]. Fig. 2 shows the zero-crossing distortion of the grid current based on a PR controller.

The hybrid method for soft-switching of the inverter with unfolding circuit based on a PR controller is described in [15]. Several other inverters based on unfolding circuit have similar benefits and shortcomings [16]–[18].

Model predictive control (MPC) has become a frequently used algorithm in power electronics [19]. Basically, MPC can be as a continuous control set (CCS–MPC) as a finite control set (FCS–MPC) type. The continuous control MPC has a fixed switching frequency and needs a modulator. Otherwise, the FCS–MPC allows online optimization and has a variable frequency. FCS–MPC sets out the chief parameter faster, but it requires a faster control unit, as reported in [20].

MPC has several advantages over integral methods. The main instrument of MPC is the cost function that can observe different parameters, such as power, voltage, current, and duty cycle. The MPC selects the exact variant of the suitable current value, which consequently improves accuracy. As a rule, a greater prediction horizon decreases the total harmonic distortion (THD) value of the grid current [21]. MPC is found in dc–dc converters with different nominal powers as well [22], [23]. Some interesting results obtained with grid-connected systems are reported in [23]–[26].

The initial idea of the selected MPC strategy was presented in [27], but only for simulation. The aim of this article was to provide practical implementation, which includes significant algorithm modifications and a feasibility study.

This article describes the implementation of the unfolding circuit based grid-connected buck–boost twisted inverter to the grid. The main purpose is to reduce the zero-crossing distortion by using MPC as a main functional block in the control system and to implement computational reduction of each sample.

The article is organized as follows. Section II describes the case study system. Section III is devoted to the optimal MPC description. Section IV shows the experimental confirmation. Finally, Section V concludes this article.

II. Case Study System

The twisted buck–boost inverter based on unfolding circuit has several benefits. The design of the passive components showed that the total energy of the passive elements is less in comparison with the conventional solution [10]. The twisted inverter has two parts: the high-frequency buck–boost part (S_1, S_2) and the low-frequency unfolding circuit (S_3–S_6). The phase shifting between the buck–boost and the unfolding parts leads to reducing the zero-switching distortion discussed in [12]. Due to the low number of high-switching semiconductors, lower switching losses are expected. Also, its high-switching component of the common mode voltage is insignificant, which leads to the absence of problem with leakage current for solar application. In addition, the twisted buck–boost inverter can operate in a wide range of the input voltage and the input power. Switches S_1 and S_2 are related both to the buck mode and the boost mode. Switch S_1 is considered the primary switch and switch S_2 is the complementary transistor to the primary switch. The expression of the duty cycle can be obtained through the

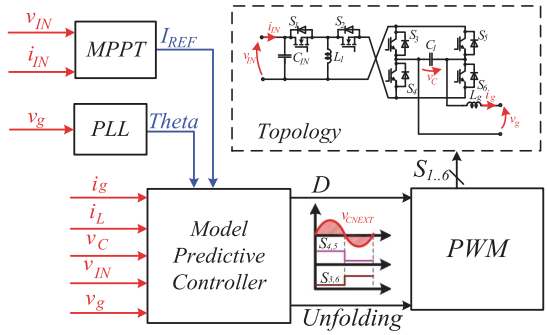

Fig. 3. Structure of the control system based on MPC.

input and the grid voltages:

$$D = \frac{v_C}{v_C + v_{\text{IN}}}, v_C = v_g + i_g \cdot (R_g + R_{Lg}) + L_g \cdot \frac{\Delta i_g}{T_S} \quad (1)$$

where *Rg* is a grid side resistance, *RLg* is the resistance of the grid inductance, *TS* is a switching period, and *Lg* is a grid inductance.

Despite benefits, a twisted inverter based on unfolding circuit has a few significant drawbacks. The voltage drops of the buck–boost semiconductors equal the sum of the input and the output voltages. Thus, in (2), it is required to select transistors with a higher drain-source broken voltage:

$$v_{\text{SW1}} = v_{\text{SW2}} = v_{\text{IN}} + v_C. \quad (2)$$

Also, it assumes the maximum current in the coil. It is possible to express the inductor current using the dependence of the duty cycle:

$$i_g = (1 - D) \cdot i_L \quad (3)$$

where *iL* is the instantaneous value of the inductor coil.

As a result, the inductor current represents the sum of the input and output currents. The maximum values in both cases relate to the phase π; thus, the peak value of the inductor current is the sum of the maximum currents:

$$i_L = i_{\text{IN}} + i_g, I_{L\text{MAX}} = I_{\text{INMAX}} + I_{g\text{MAX}} \quad (4)$$

where *I*INMAX is the maximum value of the input current and *Ig*MAX is the amplitude of the grid current.

In summary, this section has addressed the analysis of the shape of the power signals. As a result, necessary ratings of the capacitor voltage, inductor currents, and transistor drain-source broken voltages have been selected.

Fig. 3 shows the functional structure of the control system that consists of four blocks. Each of them helps to determine or to regulate the power parameters. MPC is a certain block of the control system. It should be noted that an indirect MPC (CCS–MPC) was implemented in the control because MPC permits calculation of the high-frequency ripple in the passive elements. Thus, the stability of the system is increasing with high-frequency sampling. On the other hand, the accuracy might be reducing because of limited opportunities for changing the power signals.

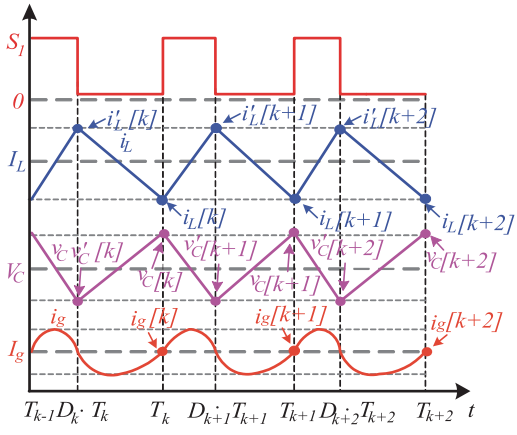

Fig. 4. High-frequency waveforms of the states.

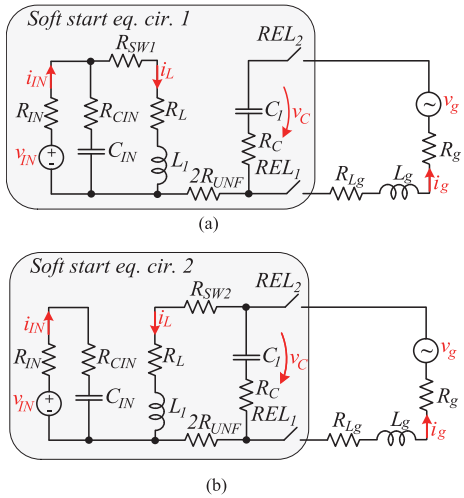

Fig. 5. Case of the input energy storage (a). Case of the storage energy transferring to the grid (b).

However, the direct MPC typically requires a higher possibility of the microcontroller performance because it should observe both turning ON and turning OFF the switch. Therefore, the sample frequency is the same as the pulsewidth modulation (PWM) frequency. The measurement delay is one cycle of the PWM. Hence, the system should analyze power states during the previous period. The CCS–MPC also provides control of the low-frequency part (unfolding circuit). The unfolding part signals are changed with regard to the sign of the predictive output capacitor voltage.

Regarding to the signal shapes, some simplifications are required. As a rule, the states are the currents in the inductors and the voltages across the capacitors. All the values of the power states are added to the cost function, even for each switch of the main transistor during the future periods. Fig. 4 shows the shapes of the power states due to the switching of the main buck–boost transistor S_1. The high-frequency ripple of the input inductor current has a triangle view as the output capacitor voltage. However, the shape of the grid current is a significant nonlinear signal. Thus, it is not easy to get values during the next period of the PWM. Besides, the instant power signals create a shift for the higher harmonic of the grid current.

III. Optimal MPC Description

The computational time is a mandatory parameter when the MPC is used as a control block. Usually, the integral techniques operate faster than MPC and require short computation time. The study in [28] confirmed it by a comparison between the PI and a moving discrete control set MPC. Thus, systems that provide MPC, in particular those with high horizon, require expensive chips with high computational burden, as shown in [29], [30]. The DSP within FPGA chips allows complex parallel computations of the MPC [31], [32]. The design of weighting factors is an open problem in MPC applications. Although some automated design procedures based on artificial intelligence have been proposed recently [33], the conventional design approach is to employ computer simulations to determine the weighting factors heuristically [34].

The major instrument of the MPC is the cost function. As a rule, the cost function should contain the parameter that is considered as a parameter of the regulator. Logically, the grid current is the suitable parameter in the grid-connected systems. However, in some systems, it is required to take into account other parameters because they have special features. This section studies the behavior of the system with different MPC approaches.

Fig. 5 shows equivalent circuits during the switching of the main buck–boost key. The Relays REL_1 and REL_2 provide the connection inverter to the grid. Fig. 5(a) shows the equivalent circuit that relates to the input energy storage. Fig. 5(b) describes the transfer of the storage energy to the grid. The resistor of each element was considered in the design. The voltage of the input capacitor was equal to the input.

The differential equations were obtained for each equivalent circuit. The expressions for the first equivalent circuit are as follows:

$$L_1 \cdot \frac{di_L(t)}{dt} = v_{\mathrm{IN}}(t) - i_L(t) \cdot (R_{\mathrm{IN}} + R_{\mathrm{SW1}} + R_L) \quad (5)$$

$$L_g \cdot \frac{di_g(t)}{dt} = v_C(t) - v_g(t) - i_g(t) \cdot (R_g + R_{Lg}) \quad (6)$$

$$C_1 \cdot \frac{dv_C(t)}{dt} = -i_g(t) \quad (7)$$

where RL is the inductor resistance, RIN is the input side resistor, RSW1 is the resistance of the switch $S1$, $C1$ is the output capacitor, $L1$ is the input inductance.

The second equivalent circuit is the third-order system. The calculated equations are the following:

$$L_1 \cdot \frac{di_L(t)}{dt} = v_C(t) - i_L(t) \cdot (2 \cdot R_{\mathrm{UNFOLD}} + R_{\mathrm{SW2}} + R_L) \tag{8}$$

$$L_g \cdot \frac{di_g(t)}{dt} = v_C(t) - v_g(t) - i_g(t) \cdot (R_g + R_{Lg}) \tag{9}$$

$$C_1 \cdot \frac{dv_C(t)}{dt} = i_L(t) - i_g(t) \tag{10}$$

where *R*SW2 is the resistance of the switch *S*2 and *R*UNF is the resistor of the unfolding switch.

A. Cost Function Based on the Grid Current

The classical approach of the MPC is to predict the grid current. This section explains the strategy of the grid current prediction. The simple differential equations are used for predictive values. First, a definition of the duty cycle is considered. The new value of the duty cycle may be found in 0.5–3% near the voltage ratio. The range of the duty cycle depends on the initial values of the sample:

$$D[k+1] = \frac{v_g[k+1]}{v_g[k+1] + v_{IN}[k]} \pm 0.01 \tag{11}$$

$$t_0 = D[k+1] \cdot T_S, t_1 = 1 - D[k+1] \cdot T_S \tag{12}$$

$$D'[k+1] = (1 - D[k+1]) \cdot T_S \tag{13}$$

where *v*IN*[k]* is the initial value of the input voltage, *vg*[*k*+1] is the value of the grid voltage at the next PWM period.

The classical differential equations were used to obtain the predictive values during the next samples. The control system is fitting and smoothing each predictive value to determine the states on the next sample. The parameters of the input capacitance *R*IN and *C*IN have low effect on the main inductor current. Thus, the equations do not include the input capacitor branch in the nominal mode. The value of the input inductor current is obtained by differential equations in the case of the input energy storage:

$$i'_L[k+1] = \frac{v_{\mathrm{IN}}[k] \cdot t_0 + L_1 \cdot i_L[k]}{L_1} \tag{14}$$

$$v'_C[k+1] = v_C[k] - \frac{i_g[k]}{C_1} \cdot t_0 \tag{15}$$

$$i'_g[k+1] = i_g[k] + \frac{(v'_C[k+1] + v_C[k] - 2 \cdot v_g[k])}{2 \cdot L_g} \cdot t_0 \tag{16}$$

where *iL*[*k*], *vC*[*k*], *ig*[*k*], and *vg*[*k*] are the initial values of the current sample.

The differential equation is more complicated in the second case that corresponds to transferring the storage energy to the grid side:

$$i_L[k+1] = i'_L[k+1] - \frac{(v_C[k] + v'_C[k+1])}{2 \cdot L_1} \cdot t_1 \tag{17}$$

$$v_C[k+1] = v'_C[k+1] - \frac{i_L[k+1] + i'_L[k+1] + 2i'_g[k+1]}{2 \cdot C_1} \cdot t_1 \tag{18}$$

$$i_g[k+1] = i'_g[k+1] + \frac{(i'_L[k+1] + i_L[k+1]) \cdot L_1 - v_g[k+1] \cdot t_1}{2 \cdot L_g}. \tag{19}$$

The predictive values of the grid current can be derived based on (14)–(19). So it requires six equations with different operations, like divide, multiply, add, and subtract. The cost function of the system can be expressed as follows:

$$J = \min \left\{ \sum_{j=1}^{3} \left(\begin{array}{l} |i'_g[k+j] - i_{g\mathrm{REF}}[k+j]| \cdot W_{j1} + \\ + |i'_g[k+j] - i_{g\mathrm{REF}}[k+j]| \cdot W_{j2} \end{array} \right) \right\} \tag{20}$$

where *Wj*1*: W*11, *W*12, *W*13, *Wj*2*: W*21, *W*22, *W*23 are fixed weight factors.

B. Cost Function Based on the Inductor Current

All the issues around the grid current create distortion on the real signal, whereas the input inductor current does not participate in the cost function at all. Frequently, the system goes beyond stability because the current in the main inductor reaches huge values. Therefore, adding the input inductor current to the cost function as a main parameter increases the stability and quality of the grid current.

So under the hypothesis of this article that the input inductor current is the main parameter, the quality of the grid current should be increased.

A taking into account that the inductor at the grid side reduces high-frequency ripple and the grid current does not change abruptly, the next predictive values of the grid current can be applied similar to the previous sample:

$$i_g[k+3] = i_g[k+2] = i_g[k+1] = i_g[k] \tag{21}$$

where *ig*[*k*+3], *ig*[*k*+2], and *ig*[*k*+1] are predictive values of the grid current for the next PWM periods.

The duty cycle should change slowly rather than sharply in the nominal mode. Thus, it is not required to consider the range of the full possible range of the duty cycle that is from 0% to 100%. Thereby, the duty cycle selected previously must be kept in the memory of the microcontroller. The new value of the duty cycle may be found in 5%–10% near the previous value. All recent arguments lead to greater reliability and to lower computational requirements. The range of the duty cycle depends on the previous value:

$$D[k+1] = D[k] \pm 0.1 \tag{22}$$

where *D*[*k*] is the previous value of the duty cycle.

Logically, the accuracy of the grid current should be higher if the horizon of the prediction is greater. The reason is that the higher horizon finds the most suitable point at a deeper analysis of a prediction. The cost function of the MPC in the nominal

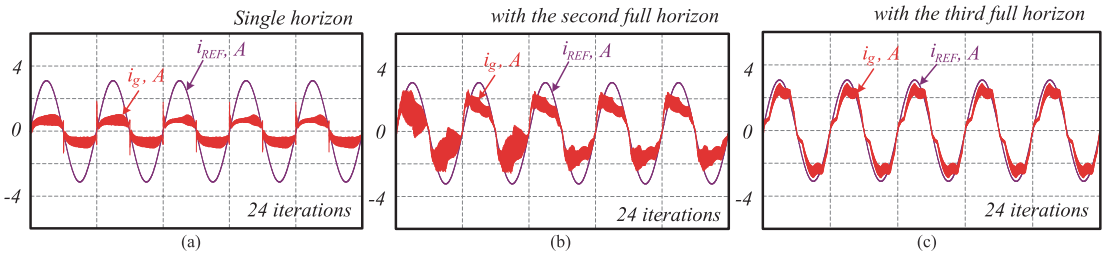

Fig. 6. Simulation results of the grid-connected inverter with MPC based on the grid current: with a single horizon (a), with the second horizon (b), and with third horizon (c).

TABLE I
PARAMETERS OF THE SYSTEM DURING THE SIMULATION AND THE EXPERIMENT

Parameter	Value
Output Capacitor C_1	1.0 μF
Input Capacitor C_{IN}	150.0 μF
Input Inductor L_1	1680.0 μH
Grid Inductor L_g	680.0 μH
Input Resistance R_{IN}	0.1 Ω
Grid Resistance R_g	0.1 Ω
Input Inductor Resistance R_L	1.0 Ω
Ouput Capacitor Resistance R_C	0.1 Ω
Ouput Inductor Resistance R_{Lg}	0.5 Ω
Resistance of S_1	0.5 Ω
Resistance of S_2	0.5 Ω
Resistance of S_3-S_6	0.3 Ω
Sample Frequency f_{sample}	62.5 kHz
PWM Frequency f_{PWM}	62.5 kHz
Grid Frequency f_g	50.0 Hz
Grid Voltage Amplitude V_M	320 V

mode is as follows:

$$J = \min\left\{\sum_{j=1}^{2}\left(\begin{array}{l}|i'_L[k+j] - i_{LREF}[k+j]| \cdot W_{j1} + \\ +|i_L[k+j] - i_{LREF}[k+j]| \cdot W_{j2}\end{array}\right)\right\} \quad (23)$$

where $i'L[k+j]$: $i'L[k+1]$, $i'L[k+2]$, $iL[k+j]$: $iL[k+1]$, $iL[k+2]$ are predictive values of the inductor current during the next PWM periods, $iL\mathrm{REF}[k+j]$: $iL\mathrm{REF}[k+1]$, $iL\mathrm{REF}[k+2]$—reference values of the inductor current.

C. Simulation Verification

The simulation tool allows one to increase the horizon of the prediction and to obtain almost ideal shapes during all power ranges, but the real control system always has timing and hardware limits. Thus, the simulation was done for the real implementation and possibility of the microcontroller. The selected system was simulated in PSim11. The parameters of the system are listed in Table I.

First of all, Fig. 6 shows the simulation results for the MPC approach based on the grid current in the cost function with different horizons. The input voltage is equal to 350 V. The peak of the reference signal for the grid current is 3 A. The single horizon cannot provide a good quality of the grid current, as shown in Fig. 6(a). The amplitude is smaller than it is needed. An appearance of zero-crossing distortion is an indicator for instability. The second horizon allows avoiding zero-crossing distortions [Fig. 6(b)]. However, the amplitude is still a deficiency. Only the third horizon allowed to get a suitable peak of the grid current, as it is seen from Fig. 6(c). Although the third horizon was applied, the THD value is quite significant. The iteration number was 24 per each full horizon. Thus, considering three horizons, the total amount of iteration is $24^3 = 13\,824$. Further horizon increase may lead to the THD improvement, but the number of computational efforts is unacceptable for practical implementation.

The simulation results described above can be explained by a nonminimum phase system, as it was mentioned in [35]–[36]. These types of systems are complex to control. They require complex algorithms to provide a desired output current.

Fig. 7 displays the simulation results of the nominal mode after the grid connection for the different buck and boost ratios with the inductor current in the cost function. The results of the high boost ratio are shown in Fig. 7(a). The input voltage was 160 V. The input power equals 650 W, whereas the grid current peak reaches 4 A. The inductance current attains 12 A in those conditions. Fig. 7(b) demonstrates the simulation results with only buck mode with a single ratio. The input voltage equals 320 V. The input power is 1.1 kW, with 7 A of the grid current. As in a single buck case, the input power within the grid current amplitude was the same for a higher buck case [Fig. 7(c)].

A no-load (no grid) case requires the grid voltage generation on the output capacitor. The same voltage of the output capacitor and the grid side eliminates the sharp spike of the grid current. Fig. 8 shows the simulation results of the soft-start mode with different depths of the predictive horizon and different increments of the duty cycle. The input voltage equals 100 V that relates to 3.2 of the boost ratio. The reduced step changes of the duty cycle provide an unsatisfactory capacitor voltage [Fig. 8(a)]. A higher number of the duty cycle step changes does not improve the performance, as shown in Fig. 8(b). Finally, an increase of the predictive horizon excludes any unstable occurrences, as shown in Fig. 8(c).

Simulation results showed that monitoring of the input inductor current as a main parameter improves the performance, as it was supposed. The CCS–MPC system supplies a fundamental harmonic even with four iterations for one horizon of the

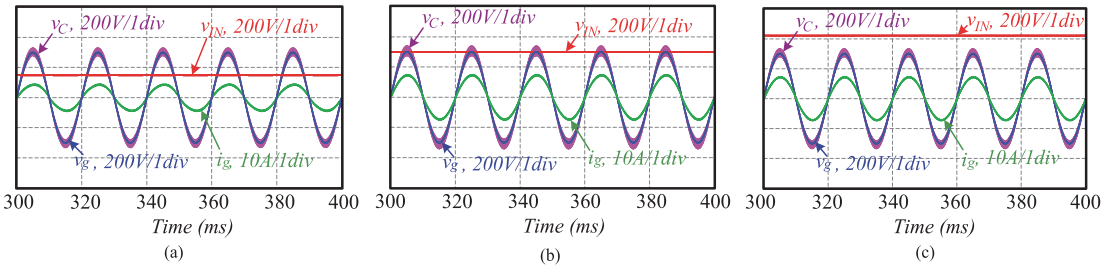

Fig. 7. Simulation results of the main operation mode. The waveforms of the output capacitor voltage, the grid voltage, and the grid current at the input voltage 160 V (a), the input voltage equals 320 V (b), and the input voltage is 450 V (c).

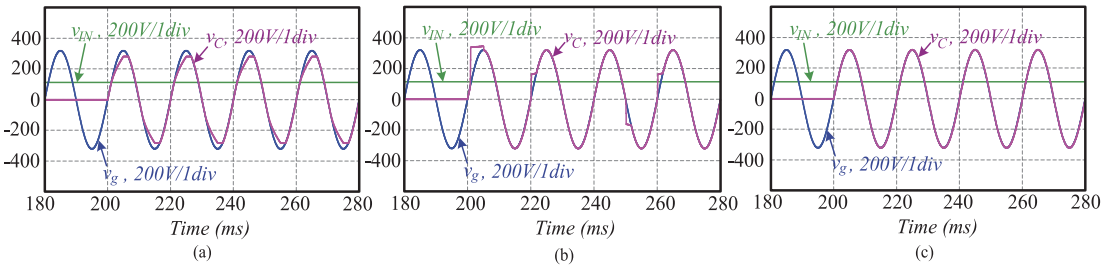

Fig. 8. Simulation results of the precharging: waveforms of the output capacitor voltage and grid voltage with a reduced value of the duty cycle step (a), with a higher increment of the duty cycle of a single predictive horizon (b), and with a higher increment of the duty cycle along with second predictive horizon (c).

prediction. Figs. 7 and 8 show the model with two-step horizon of MPC, but the second horizon is with the approximation. During the first horizon calculation, 5 iterations and only 10 iterations with the second approximated horizon calculation were used, while 25 required without approximation. The MPC reduced a zero-crossing distortion significantly, as was assumed in the theory. The simulation results confirm theoretical statements.

The key points of the simulation verification allow obtaining an optimal MPC horizon and factors of the tuning. The quality of the grid current and the computational opportunity of the microcontrollers are regarded as the main factors of the tuning. The second horizon had a higher priority in the system; therefore, the weight factors have ratio 2:1, which corresponds to the second horizon versus the first one. The heuristic methodology [34] was applied to obtain the following set of weighting factors: $W11$, $W12$, $W21$, and $W22$.

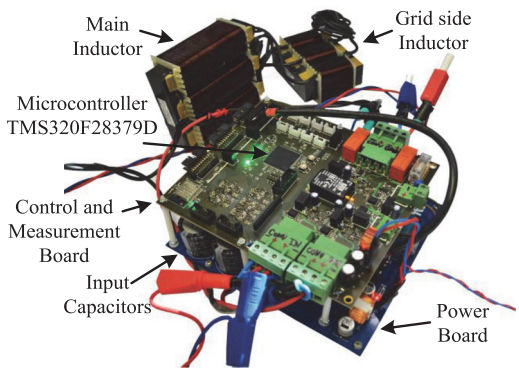

Fig. 9. Experimental prototype of the buck–boost twisted inverter based on unfolding circuit with the control board.

IV. Experimental Confirmation

A. Setup of the Twisted Buck–Boost Inverter

Two boards (control and power) were designed for the experimental setup. Fig. 9 shows the experimental prototype of the twisted buck–boost inverter based on unfolding circuit. The inductances are connected by external terminals. The auxiliary supply of the control and measurement board was 12 V and corresponds to 10 W of the power losses.

The control board includes the measurement channels: five voltage and three current sensors. The current sensor ACS720 enables the overcurrent detection with the digital output. It has fast and slow overcurrent detection that allows the system to be stopped as quickly as possible. All the sensors are isolated from the control part. The analog digital converter (ADC) receives the differential signal that avoids the common mode interference. The rating of the switches limits and passive limits are collected in Table II.

TABLE II
RATING OF ELEMENTS LIMITS

Parameter	Value
Output Capacitor C_1	600 V
Input Capacitor C_{IN}	500 V
Input Inductor L_1	15A
Grid Inductor L_g	10 A
Switch S_1	1200 V
Switch S_2	1200 V
Switches S_3-S_6	650 V

Multicore microcontroller of the Texas Instruments TMS320F280379D is the main brain of the prototype. MCU operates at 200 MHz of the input frequency. The safety system consists of the software and hardware protection. The software protection estimates the measured parameters according to the safe limits. The hardware protection emits digital signals from the current sensors to the microcontroller. The microcontroller stops the PWM directly because it has the corresponding opportunity. Each channel of voltage measurement has a varistor for safety at the overvoltage.

The control and measurement board includes two relays that allow connecting or disconnecting the grid side from the inverter. Thus, if some parameter is exceeding the hardware or software limits, the system starts to turn OFF all PWM channels, relays and buffers, but it leaves the unfolding working for energy discharging through the grid.

B. MPC Task Distribution

The simulation results showed high stability even for a single horizon, but the soft-start was stable only with the second horizon, as described in Section III. It is necessary to take into account that the time of data conversion is limited by the sample period when MPC is a main control block. Due to the previous facts, the amount of the iterations is bound as well. Many microcontrollers cannot provide the second horizon even with fast arithmetic operations. The microcontroller TMS320F280379D has four parallel cores. Each of them allows quick calculating, multiplying, and dividing. The MCU has a hardware trigonometric unit that calculates sinuses, cosines, and tangents in a few ticks. All registers are operating with the shadow mode. The shadow mode is intended for a clear time of data loading. The system delay is one sample period due to the shadow mode. A new duty cycle value will be set to the start of the next PWM period; thus, when the algorithm comes to MPC, it needs to take into account the previous duty cycle value.

Fig. 10 shows the block diagram of the principle of data handling. The end of ADC conversions launches the data checking. If the error does not occur, the code is going into MPC to calculate the predictive values. The idea is to distribute the MPC iterations between the cores. The first core is a master for all other structures. When the algorithm comes to the MPC part, it emits a signal to the other cores to start the MPC as well. Each core corresponds to the own iteration range of the MPC. The results from all cores are compared between each other and the most suitable variant is applied to the duty cycle.

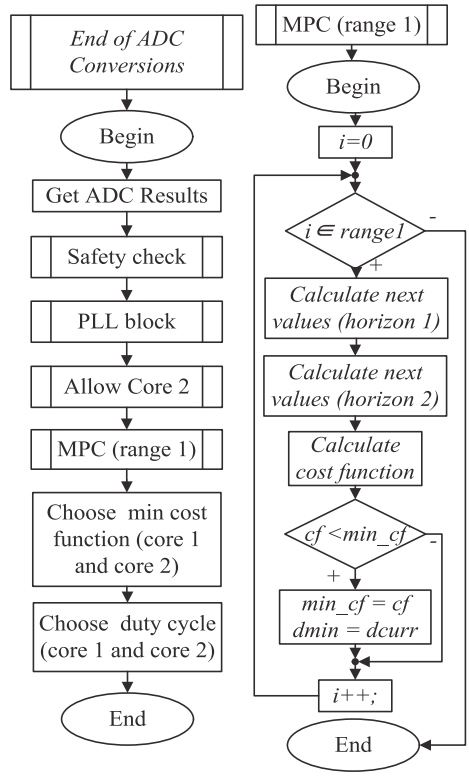

Fig. 10. Block diagram of the nominal mode with the multicores distribution.

Finally, the distribution of the MPC task allows a double increase in the amount of the iteration with the second cores. The working of both cores decreases the computational time twice in comparison with only one operating core.

C. Experimental Results

The experiment with the grid connection confirmed the theoretical hypothesis and repeated the simulation results. The monitoring of the inductor current proved the best way to stabilize the system and to obtain high accuracy of the grid current. Zero-crossing distortions were reduced or even eliminated in some cases of the input power. It is necessary to inject a delay for entering the nominal mode after the inverter connection to the grid. The reason is that if the system is going to the normal amplitude sharply, it can damage the elements. Thus, a slow increase of the grid current was implemented at the beginning of the nominal mode.

The case of the lower input power had a small spike near the sine zero. The synchronous transistor $S2$ allows both reduction of the static loss and fast discharge of the capacitor voltage near zero. The shift between the buck–boost part and unfolding circuit helps to avoid zero-crossing distortion as well.

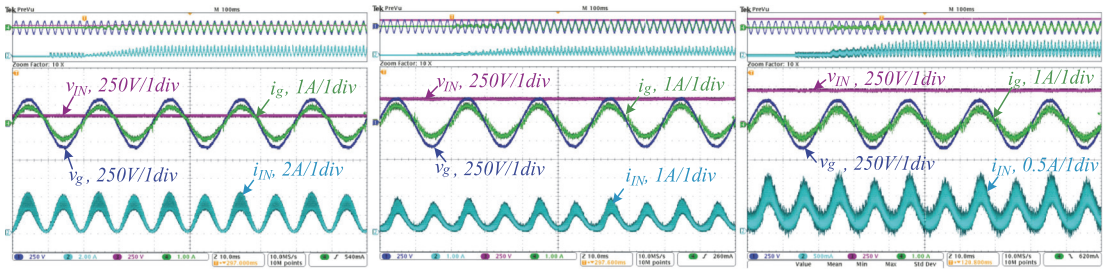

Fig. 11. Experimental results of the steady-state operation: the waveforms of the input and output voltages and currents for the lower input power in the case of boost (a), only buck (b) and with higher buck ratio (c).

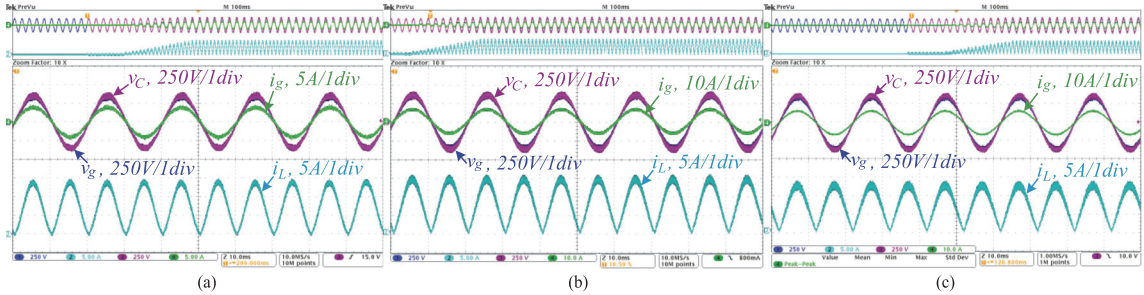

Fig. 12. Experimental results of the steady-state operation: the waveforms of the input and the output voltages and currents for the higher input power at the input voltage 160 V (a), 320 V (b) and 450 V (c).

Fig. 11 displays the experimental results with the amplitude 1 A of the grid current that confirms a reduced distortion. The case of the triple boost ratio showed that the grid current is of a sine shape while the current in the input inductance is reaching up to 5 A. Fig. 11(a) shows the input and the grid voltages and currents. THD of the grid current was 3.15% in the boost case. The single and higher buck cases are shown respectively in Fig. 11(b) and (c). THD was no more than 3% in both buck cases. The higher buck case corresponds to 450 V of the input voltage. A bigger ripple of the input current occurred in the higher boost case.

On the other hand, Fig. 12 displays the results for the double boost ratio with 650 W of the input power. The inductor current reaches 14 A due to the high-frequency ripple. The input power equals 1.1 kW in the buck cases [Fig. 12(b) and (c)]. THD value was less than 3% in all cases. A high-frequency ripple confirmed the previous theoretical design [Fig. 12(b)] reported in [15]–[16]. A higher buck case is the most critical point for semiconductor voltage stresses. Voltage spike during switching was not significant at 450 V of the input voltage. Though the voltage stress reached 850 V, the transistor worked correctly. Hence, the experiment was done at 150 W of the minimum input power. The results showed that greater zero- crossing distortion appeared in the higher buck case. The maximum tested power was around 1.1 kW.

When any emergency is recognized, the unfolding part is still working for some time while the buck–boost circuit is stopped immediately. The equivalent circuit corresponds to three parallel branches: the main inductor branch, the output capacitor branch, and the grid side branch. As a result, the storage energy of the passive components is flowing to the grid. The transient process corresponds to the damped harmonic transient type. Thus, it is possible to observe some fluctuations on the capacitor voltage and in the inductor's currents, but they are not significant.

The dynamic behavior of the system demonstrated good execution. Fig. 13 confirms the good performance of the control system under the input voltage variations. The knob spinning of the power supply influenced the input voltage change [Fig. 13(a)]. The input voltage was changed from 360 to 260 V, while the grid current was stable during each period. At the same time, the system mode is changing from buck to boost mode. Usually, the PV voltage is changing slowly, which corresponds to several dozen periods. Thus, it was decided to generate a fast voltage step by using the programmable dc supply.

Fig. 13(b) and (c) is responsible for the case of the input voltage step. The time of the step equals 4–5 periods of the grid,

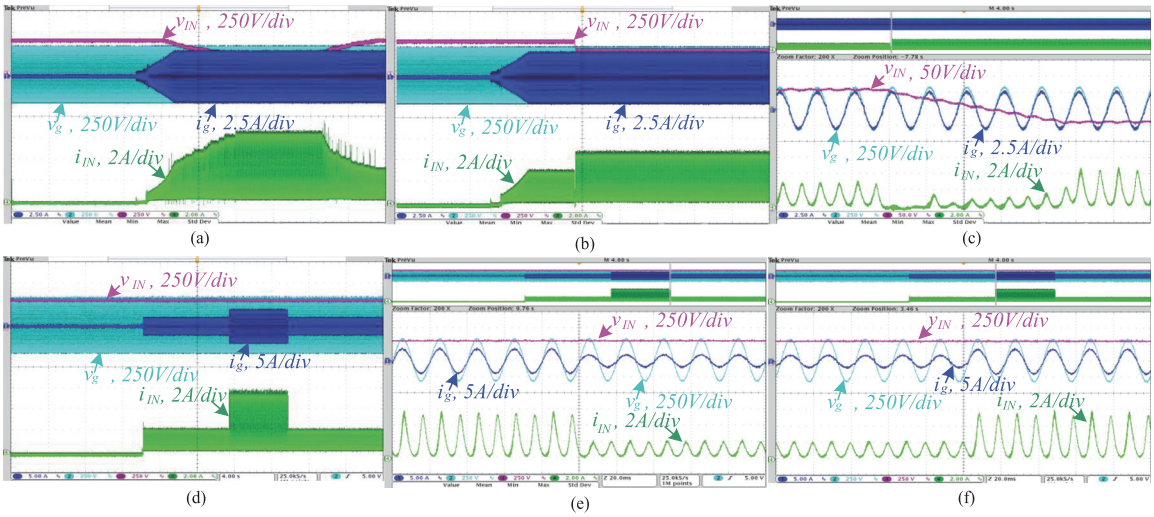

Fig. 13. Experimental results under the input voltage variation from 360 to 260 V (a)–(c); experimental result under the grid power values: the transient process (d), transient from 4 to 2 A of the grid current (e), transient from 2 to 4 A of the grid current (c).

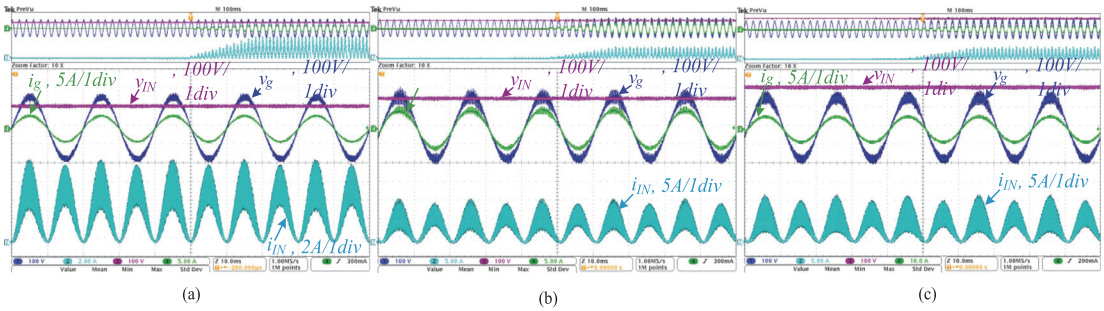

Fig. 14. Experimental results for 50% of the grid voltage: boost case vIN (t) = 100 V, I_gMAX = 4 A (a), buck case vIN (t) = 160 V, I_gMAX = 6 A (b), buck case vIN (t) = 240 V, I_gMAX = 8 A (c).

while the grid current is the same and has not any transients or distortions. Thus, we can underline that the system is stable under input voltage variations.

In advance of the input voltage step change test, the system was tested under the step change of the reference grid power. The power was changed by using a software debug window. Fig. 13(d)–(f) show the experimental results at the change of the grid power from 320 to 640 W. The amplitude of the grid current is moving from 2 to 4 A [Fig. 13(e)] and thereafter is coming back to 2 A [Fig. 13(f)]. The test showed superior performance of the MPC over the integral techniques due to the immediate response without any oscillations.

It should be noted that the values of the passive elements and of the transistors were measured or taken from the datasheets. However, the real values are not the same as those measured because each equipment like a tester or an RLC analyzer has an error of measurement. If the values are correct, other conditions influence the transistor and the passive elements, such as temperature, switching frequency, power level, etc. Thus, one of the good results is the operation of the converter with wrong or approximately the same values of the passive elements. Fig. 14 shows the experimental results with 50% of the grid voltage. The autotransformer was used for reducing the peak value of the grid voltage down to 160 V. The serial grid inductance that is not taken

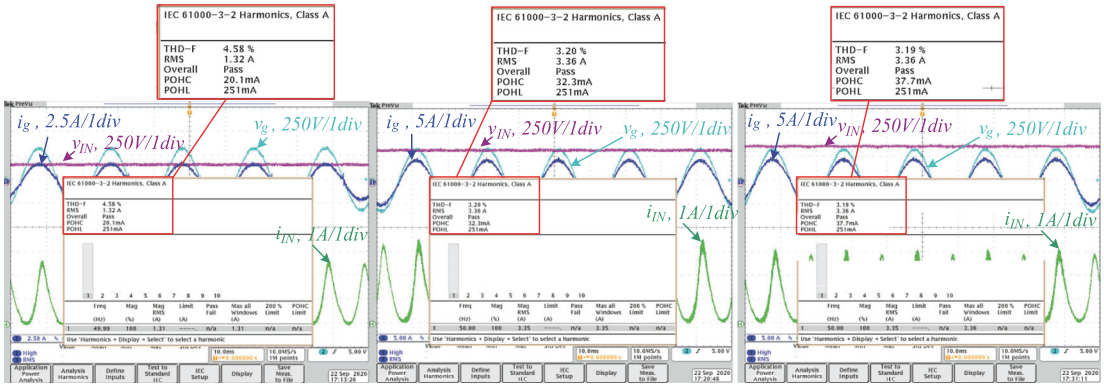

Fig. 15. THD estimation of the converter under different input voltages: boost case with 160 V of the input stress (a), buck case with 300 V of the input voltage (b), higher buck ratio *v*IN = 360 V (c).

into account was injected in the system by the autotransformer. As it is seen, the system behavior is stable, but high-frequency ripples were increased. The inverter performance is good in the boost case [Fig. 14(a)]. The input power was 320 W. The buck case is accompanied by high ripples of the inductor current, as shown in Fig. 14 (b) and (c). The maximum showed power is 650 W [Fig. 14 (c)].

The last experimental tests correspond to the THD estimation. The used oscilloscope Tektronix MSO 4034B has a feature of a harmonic analyzer. The standard IEC 61000-3-2 is the requirement for THD estimation. The experimental prototype was tested for THD determination with the input voltage range from 100 to 450 V and with different input powers. Fig. 15 shows three tested points of THD estimation for boost and buck cases. Fig. 15(a) presents THD value in the boost mode. The input voltage was 160 V along with 320 W of the input power. The single buck case that corresponds to 300 V is presented in Fig. 15(b). THD value less than 4%. The input power is 800 W. The third picture regards to 360 V of the input voltage with the same 800 W of the input power. The THD value is approximately the same as that in a single buck case. All measured results passed the standard even in the low power mode.

V. Conclusion

Features associated with the experimental implementation of the twisted buck–boost inverter based on the unfolding circuit were presented. The hypothesis that MPC should set the inductor current as the main parameter in the cost function was found to be reasonably supported.

Predictive values were obtained by differential equations, which simplified the calculation process. No trigonometric functions (TF) were used in the equations, which enabled reduced calculation time. However, the computational time goes beyond the PWM period at the higher horizon or the greater amount of iterations because the PWM frequency is 62 kHz. One iteration without TF takes 1.5–2 μs.

Simulation results showed that the soft start was stable only with the second horizon that increased the requirement for the microcontroller performance. The horizon of the nominal mode was a single horizon, while the amount for the iteration did not go beyond 10. The simulation confirmed the hypothesis about the reduction of the zero-crossing distortions as well.

The experimental prototype was presented within the control and measurement board: five voltage and three current sensors provided all necessary measurements for the stable work of the MPC. The brain of the control board is the multicore microcontroller that contributes to the MPC task between the cores and makes the calculation process faster. The experiment revealed reduced zero-crossing distortion. The operation range of the input voltage was from 100 to 450 V. The minimum input power was 150 W, whereas the maximum equals 1.1 kW. The operation of the system is stable under different input stresses and under different grid powers without any transient processes and distortion in the grid current observed.

Finally, MPC is suitable for topologies based on unfolding circuit within the performance of the multicore microcontroller for decreasing zero-crossing distortion. At the same time, the multicore controller allows reduction of the computation time.

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Design and Experimental Validation of a Single-Stage PV String Inverter with Optimal Number of Interleaved Buck-Boost Cells

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Abstract: Increasing converter power density is a problem of topical interest. This paper discusses an interleaved approach of the efficiency increase in the buck-boost stage of an inverter with unfolding circuit in terms of losses in semiconductors, output voltage ripples and power density. Main trends in the power converter development are reviewed. A losses model was designed and used for the proposed solution to find an optimal number of interleaved cells. It describes static and dynamic losses in semiconductor switches for buck and boost mode. The presented calculation results demonstrate the efficiency of the interleaved approach for photovoltaic system. 1 kW power converter prototype was designed with two parallel dc-dc cells for experimental verification of obtained theoretical results. The experimental results confirm theoretical statements.

Keywords: buck-boost cell; unfolding circuit; interleaved approach

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1. Introduction

The Google Little Box Challenge (GLBC) has shown a close relation with the topic of high-power density inverters for Photovoltaic (PV) applications that have demonstrated extremely high-power density of power electronics converters achievable [1–3]. One of the GLBC project outcomes is the concept of a very high-power density converter. The finalists demonstrated a similar approach. It includes the basic full-bridge interleaved inverter, an active decoupling circuit and use of Wide Band-Gap (WBG) semiconductors.

WBGs market has an upward trend in today's power electronics due to their high electron mobility and high voltage breakdown field [4–6]. As a result, fast switching high voltage semiconductor devices are already available on the power electronics market. The challenge is still the cost of those devices, which, however, is decreasing year by year.

At the same time, several configurations may be used in the PV systems [7,8]. Single PV panels are available for low power applications. They suffer from the voltage drop when the temperature is increasing. In the serial or string connection, one of the major drawbacks is a significant voltage drop at partial shadowing. Both connections lead to a wide range of input voltage variation during the energy utilization time. The GLBC solution is intended for narrow input voltage regulation, and it cannot provide a high and efficient PV energy conversion in heating or shadowing conditions. Neither can dual-back inverters [9,10] or boost inverters reported in [11,12] be considered as a solution at a wide range of regulation. Intermediate voltage boost dc-dc converters are used to overcome this drawback. At the same time, this solution is more complex and more expensive.

An alternative is to use single-stage buck-boost for a single input dc source. In this solution, inverters with an active boost cell are used [13–16]. They can provide very

high boost of the input voltage but suffer from high current spikes in semiconductors and passive elements. The buck-boost solutions based on an active boost cell are rare in industrial applications.

New solutions are required to design an inverter with wide input voltage regulation along with high-power density and acceptable efficiency. For almost a decade, the impedance-source converters have attracted attention of the researchers [17–22]. But only a few attempts of industrial design can be found [23,24].

Several interesting single-stage buck-boost inverters are proposed in [25–29]. The solution based on the input boost and buck converter along with a line frequency unfolding circuit seems to be interesting for practical applications [29–31].

Another perspective method to decrease the size of passive components is using an interleaved approach [32–38]. In a general case, this method assumes use of two parallel circuits with the phase shift of control signals. The main advantage of such approach is reducing current through each single component, which allows reducing energy in the passive component and switch conduction losses that are proportional to the current and sizes.

Interleaved approach has been applied to different topologies, such as boost interleaved inverters with coupled inductors [33], two-phase interleaved inverters [35], three-phase grid-connected interleaved inverters [36], buck-boost interleaved inverters [37], and the three-level interleaved topology [38]. The advantages of the interleaved approach in terms of power density, cost and total converter efficiency have resulted in the improvement of the boost and buck stage in the power factor corrected rectifier system [39–41].

The main disadvantages of this topology are greater number of passive and active components, higher voltage drop on active components, and more complicated control technique.

This paper focuses on further modifications of the buck-boost inverter with unfolding circuit using the interleaving approach. Figure 1 shows the inverter structure with the N-cell dc-dc stage. This approach allows for the reduction of losses in semiconductor components, in inductor energy and output voltage ripples. The main goal of this work is to find an optimal number of the interleaved cells.

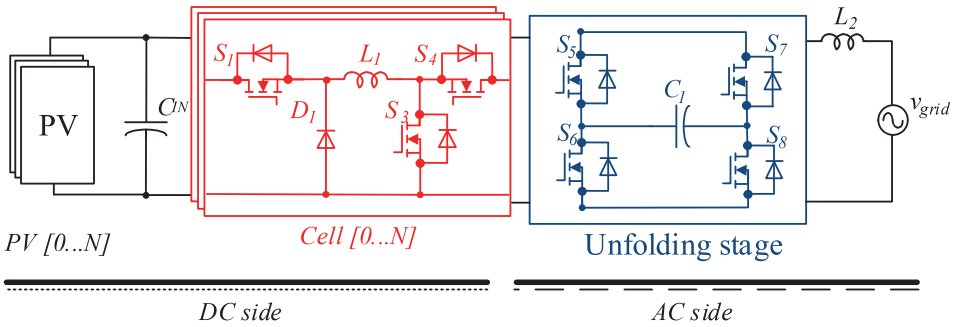

Figure 1. The inverter structure with the buck-boost N-cells.

2. Description of the Case Study System

First, the selected system is intended for PV application. Thus, the PV panel (PV string) is the input source for this topology. As a rule, a PV station has several solar panels, which can be reconfigured as parallel or serial connections to obtain the higher current or voltage, respectively. This section explains the characteristics of the real PV string applied along with brief topology features.

The set of HNS-SD140 solar panels was used as the PV string. Figure 2a shows the real PV string on the roof of the Chernihiv Polytechnic National University. The string consists of seven panels connected in series. The single panel generates around 140 W with a full panel lighting. The open circuit voltage equals 75 V with the single panel and 525 V

with the PV string, while the short circuit current is 2.5 A. The total output power reaches up to 1 kW. The PV string parameters from the datasheet are listed in Table 1. Figure 2b demonstrates the real power characteristic of the PV string in the middle of the day.

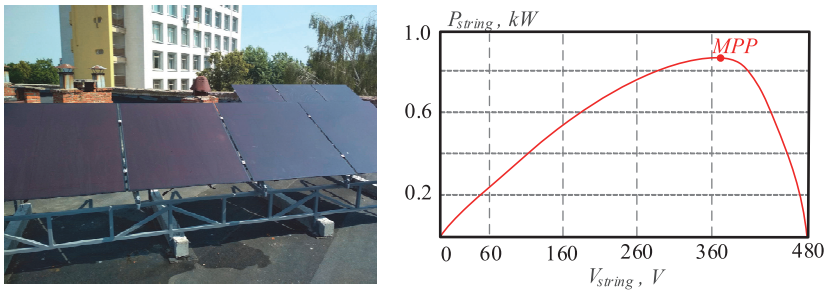

Figure 2. (**a**) PV string on the roof, (**b**) real power performance of the 7 serial-connected panels in one PV string.

Table 1. PV string parameters from the datasheet.

№	Parameter	Value
1	Input power, W	up to 1000
2	Open circuit voltage, V	525
3	Short circuit current, A	2.5
4	Maximum Power Voltage, V	413
5	Maximum Power Current, A	2.17

Topology Description

The aim of the inverter is to convert the PV string power into the ac power and to deliver it into the grid. The buck-boost inverter has two parts of circuits. The buck-boost part is the high-switching circuit that generates the unipolar sine shape at the output side using PWM. The unfolding circuit changes the sign of the output signal. The unfolding part is a low-switching part. Besides, the unfolding circuit commutes under zero voltage and zero current; thus, the dynamic losses equal zero. One of the advantages of the inverter is a wide range of the input voltage regulation. The input voltage can vary from 100 V to 500 V, while the peak of the output voltage is 320 V. Thus, the converter might be operating in a buck or in a boost mode. If the value of the grid voltage is less than the input voltage, the system operates in the buck mode, otherwise the boost mode is chosen. Figure 3 shows the principle of mode selection based on the grid voltage value.

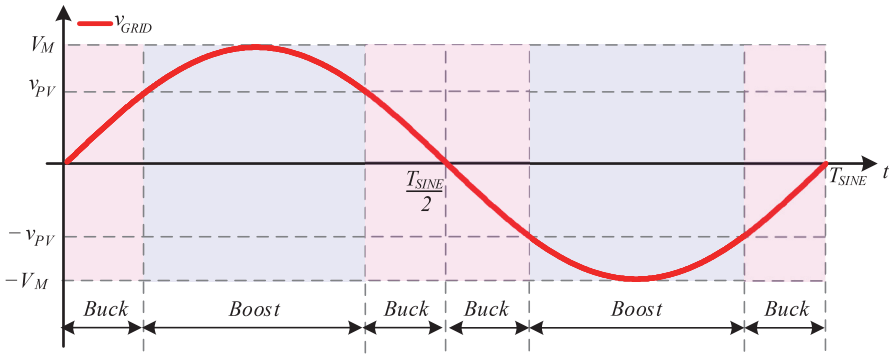

Figure 3. The principle of the buck or the boost mode selection for the buck-boost inverter based on unfolding circuit.

Figure 4 shows the commutation principle of both modes for a single buck-boost cell. Only two switches are operating during the PWM period. The principle of the buck mode is to connect or disconnect the PV side from the inverter. The boost mode is operating with energy storage by the input inductor and is giving the storage energy instant to the grid.

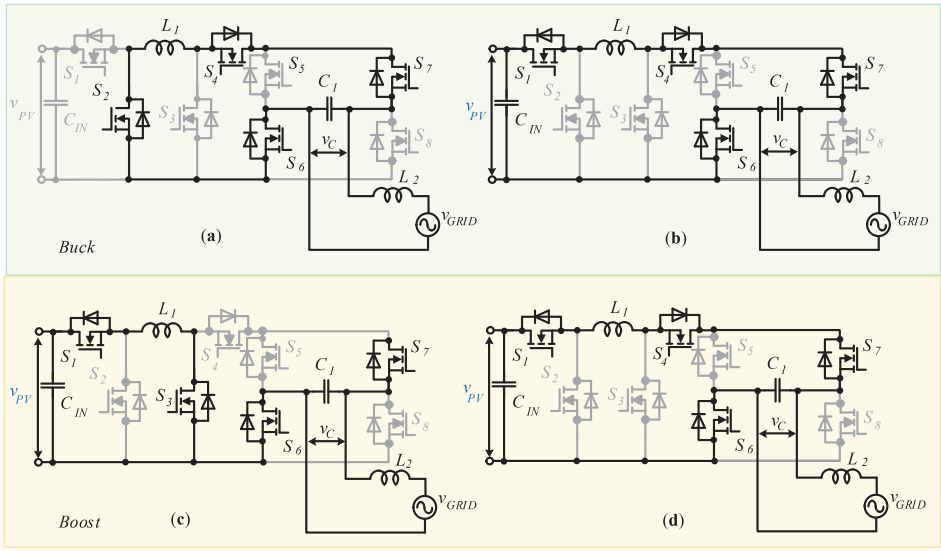

Figure 4. Switching principle of the inverter based on unfolding circuit with a single buck-boost cell: (**a**,**b**) for the buck mode, (**c**,**d**) for the boost mode.

If the buck-boost cell is not a single cell, the PWM channels are shifted between each other. The shifted phase is calculated as follows:

$$\varphi_i = \frac{360^\circ}{N} \cdot i \tag{1}$$

where N is the number of buck-boost cells, i is the current cell number.

3. Losses Model for the Buck-Boost Cell and Unfolding Circuit

It is known that the results of the calculations and those of the experiment cannot be absolutely the same because experimental parameters depend on different factors, such as the environment conditions, quality design, and other factors. Thus, the following calculation regards the power loss under ideal external conditions.

The designed model includes both types of the power losses: dynamic and static. The power signals were analyzed in detail during the model design. Figure 5 explains the high-frequency ripples of the semiconductor currents during the operation of the buck-boost case. Moreover, the buck and the boost modes require separate calculation of the power losses. Therefore, it is required to have correspondence of transistors with the modes:

$$S_1 \equiv S_{BUCK},\ S_2 \equiv S_{NBUCK}, S_3 \equiv S_{BOOST},\ S_4 \equiv S_{NBOOST},\ S_6 \equiv S_7 \equiv S_{UNFOLD}, S_5 \equiv S_8 \equiv S_{NUNFOLD}. \tag{2}$$

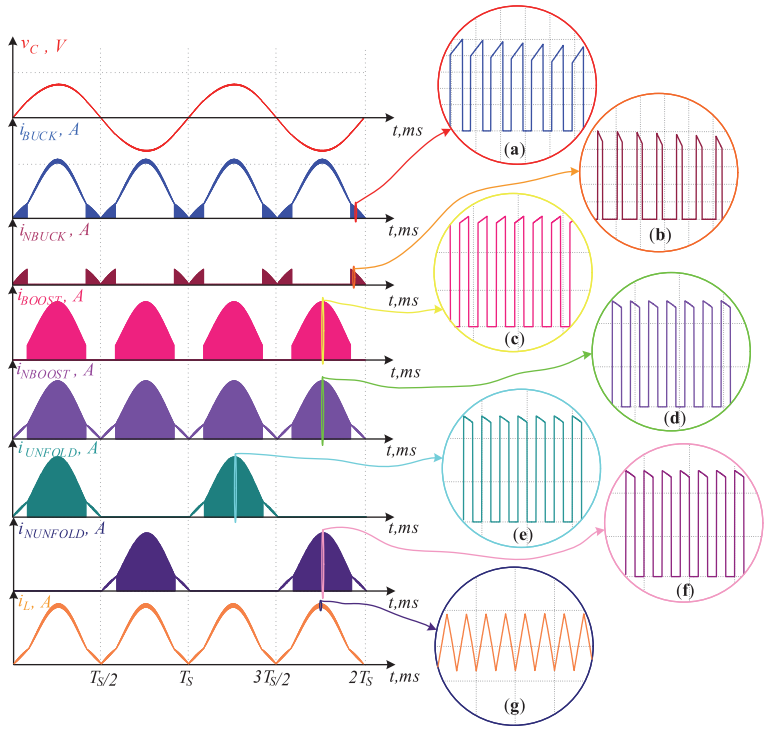

Figure 5. The high-switching current ripples of the semiconductor: (**a**) the input buck switch S_{BUCK}, (**b**) the complementary buck switch S_{NBUCK}, (**c**) the boost transistor S_{BOOST}, (**d**) the complementary boost transistor S_{NBOOST}, (**e**) the forward polarity unfolder switch S_{UNFOLD}, (**f**) the reverse polarity unfolder transistor $S_{NUNFOLD}$, (**g**) and the inductor current.

So, it is necessary to take into account dependences of the duty cycle for each mode. The expressions of the duty cycle are the same as in the case of a simple buck and boost dc-dc converter, but the output voltage is considered as a sine shape signal:

$$D_{BUCK} = \frac{|v_{GRID}|}{v_{PV}},\ D_{BOOST} = \frac{|v_{GRID}| - v_{PV}}{|v_{GRID}|},\ v_{GRID} = V_M \cdot \sin(\varphi), \tag{3}$$

where v_{GRID} is the grid voltage, v_{PV} is the PV voltage, V_M is an amplitude of the grid voltage, φ is the current phase of the grid voltage, v_C output capacitor voltage.

In the context of the steady state analysis, the currents depend on the input power and on the duty cycle. It is worth nothing that the inductor current is inversely proportional to the number of the buck-boost cells. The expressions are as follows:

$$i_{PV} = \frac{2 \cdot P}{v_{PV}} \cdot \sin^2(\varphi),\ i_{L\_BUCK} = \frac{i_{PV}}{N \cdot D_{BUCK}},\ i_{L\_BOOST} = \frac{i_{PV}}{N}, \tag{4}$$

where P is an average value of the input power, N is the number of buck-boost cells.

The steady state analysis allows obtaining the expression of the ripples in the passive elements. The pulsations of rising and falling states are considered the same. Figure 5g shows the high frequency ripple of the inductance current. The expressions of the inductor current ripples for the different modes are given below:

$$\Delta i_{L\_BUCK} = \frac{v_{PV} - |v_{GRID}|}{2 \cdot f_{SW} \cdot L_1 \cdot N} \cdot D_{BUCK},\ \Delta i_{L\_BOOST} = \frac{v_{PV}}{2 \cdot f_{SW} \cdot L_1 \cdot N} \cdot D_{BOOST}, \tag{5}$$

where f_{SW} is the switching frequency, L_1 is the value of the inductance.

Further calculations take into account each high-switching period. The dependences of the rising and falling of the inductor current are obtained using a canonical equation of the line. The inductor current depends on the time and on the current switching period. The expressions of the buck mode are as follows:

$$i_{L\_BUCK\_RISE} = i_{L\_BUCK} - \Delta i_{L\_BUCK} + 2 \cdot \Delta i_{L\_BUCK} \cdot \frac{t - i \cdot T_{SW}}{D_{BUCK} \cdot T_{SW}}, \quad (6)$$

$$i_{L\_BUCK\_FALL} = i_{L\_BUCK} + \Delta i_{L\_BUCK} - 2 \cdot \Delta i_{L\_BUCK} \cdot \frac{t - (i + D_{BUCK}) \cdot T_{SW}}{(1 - D_{BUCK}) \cdot T_{SW}}, \quad (7)$$

where T_{SW} is the switching period, "i" is the current number of the high-switching period.

The same equations are used for the boost mode. Moreover, any power signal or other variables are presented as the function of the current switching period:

$$\varphi \to \varphi(i) = \omega_0 \cdot i \cdot T_{SW}\ , i_{L\_BUCK\_RISE} \to i_{L\_BUCK\_RISE}(i),\ i_{L\_BUCK\_FALL} \to i_{L\_BUCK\_FALL}(i), \quad (8)$$

$$D_{BUCK} \to D_{BUCK}(i)\ ,\ D_{BOOST} \to D_{BOOST}(i). \quad (9)$$

However, the currents of the transistors are not continuous, so it is required to consider a different time span for each semiconductor.

3.1. Static Losses Model

The static model corresponds to the law of Joule-Lenz. Thus, the overall static losses are equal to the sum of each semiconductor power loss. The general static losses are derived with the next expression:

$$P_{CLOSS} = \sum_{i=1}^{M} \left(I_{i\_RMS}^2 \cdot R_{DSON} \right), \quad (10)$$

where M is the number of transistors, I_{i_RMS} is the RMS value of the transistor current, R_{DSON} equals the ON-state resistor declared in the document of the element.

On the other hand, the current ripples through the semiconductor element were taken into account during the RMS calculation. Certainly, each high-switching period is considered. So, the square RMS values of the semiconductor currents are expressed as:

$$I_{T\_BUCK\_RMS}^2 = \frac{1}{T_{SINE}} \cdot \sum_{i=0}^{Q} \left[\int_{i \cdot T_{SW}}^{(i + D_{BUCK}(i)) \cdot T_{SW}} \left(i_{L\_BUCK\_RISE}^2(i) \cdot dt \right) \right], \quad (11)$$

$$I_{T\_NBUCK\_RMS}^2 = \frac{1}{T_{SINE}} \cdot \sum_{i=0}^{Q} \left[\int_{(i + D_{BUCK}(i)) \cdot T_{SW}}^{(i+1) \cdot T_{SW}} \left(i_{L\_BUCK\_FALL}^2(i) \cdot dt \right) \right], \quad (12)$$

$$I_{T\_BOOST\_RMS}^2 = \frac{1}{T_{SINE}} \cdot \sum_{i=0}^{Q} \left[\int_{i \cdot T_{SW}}^{(i + D_{BOOST}(i)) \cdot T_{SW}} \left(i_{L\_BOOST\_RISE}^2(i) \cdot dt \right) \right], \quad (13)$$

$$I_{T\_NBOOST\_RMS}^2 = \frac{1}{T_{SINE}} \cdot \sum_{i=0}^{Q} \left[\int_{(i + D_{BOOST}(i)) \cdot T_{SW}}^{(i+1) \cdot T_{SW}} \left(i_{L\_BOOST\_FALL}^2(i) \cdot dt \right) \right], \quad (14)$$

$$I^2_{T\_UNFOLD\_BUCK\_RMS} = \frac{1}{T_{SINE}} \cdot \sum_{i=0}^{Q} \left[\begin{array}{l} \int\limits_{i \cdot T_{SW}}^{(i+D_{BUCK}(i)) \cdot T_{SW}} \left(i^2_{L\_BUCK\_RISE}(i) \cdot dt \right) + \\ + \int\limits_{(i+D_{BUCK}(i)) \cdot T_{SW}}^{(i+1) \cdot T_{SW}} \left(i^2_{L\_BUCK\_FALL}(i) \cdot dt \right) \end{array} \right], \quad (15)$$

$$I^2_{T\_UNFOLD\_BOOST\_RMS} = \frac{1}{T_{SINE}} \cdot \sum_{i=0}^{Q} \left[\int\limits_{(i+D_{BOOST}(i)) \cdot T_{SW}}^{(i+1) \cdot T_{SW}} \left(i^2_{L\_BOOST\_FALL}(i) \cdot dt \right) \right], \quad (16)$$

where T_{SINE} is the sine period, Q is the amount of the high-switching periods per one sine period.

3.2. Dynamic Losses Model

The dynamic losses can be obtained using the same principle: consider each high-switching period. The next expression allows the calculation of the switching loss during the sine period:

$$P_{DLOSS} = \frac{1}{T_{SW}} \cdot \left(\frac{t_{dON} + t_r + t_{dOFF} + t_f}{2} \cdot I_{P\_AVG} \cdot V_{P\_AVG} + \frac{5}{4} \cdot Q_{rr} \cdot V_{P\_AVG} \right), \quad (17)$$

where t_{dON} is the turn on the delay time, t_r is the rise time of the transistor, t_{dOFF} is the turn-off delay time, t_f is the fall time, I_{P_AVG} equals an average value of transistor current spikes during the grid period, V_{P_AVG} is the average value of the transistor drain source stress during the sine period, Q_{rr} is the reverse recovery charge of the reverse diode.

The average current spikes during the grid period can be obtained from previous Equations (3)–(15) for each switch. As is known, they correspond to the maximum ripple of the inductor current at each moment of the transistor conduction (one high-switching period):

$$I_{T\_BUCK}(i) = i_{L\_BUCK}(i),\ I_{T\_NBUCK}(i) = i_{L\_BUCK}(i), \quad (18)$$

$$I_{T\_BOOST}(i) = i_{L\_BOOST}(i),\ I_{T\_NBOOST}(i) = i_{L\_BOOST}(i), \quad (19)$$

The average voltage spikes can be derived from a simple differential equation of equivalent circuits. The values of the peak of one high-switching period are as follows:

$$v_{DS\_BUCK}(i) = v_{PV}(i),\ v_{DS\_NBUCK}(i) = v_{PV}(i), \quad (20)$$

$$v_{DS\_BOOST}(i) = v_{PV}(i),\ v_{DS\_NBOOST}(i) = v_{PV}(i). \quad (21)$$

4. Study of the Optimal Number of the Buck-Boost Cells

An interleaved approach for the buck-boost stage of the inverter has some advantages and disadvantages. Parallel connection of dc-dc cells increases the number of semiconductor switches, and as a result, it increases the number of high-frequency commutations, and even may increase the total converter volume and the size. On the other hand, an interleaved feature allows the distribution of the input current between the cells, which leads to the reduction of conduction losses in the semiconductors. At the same time, the input inductances can be redesigned for lower current. This section is devoted to finding an optimal number of cells.

4.1. Conclusions from the Calculations

Section 3 described the calculation based on the real semiconductor parameters. The transistor UJC0650K was chosen for the buck-boost part, while IPP60R060P7 is embedded in the unfolding part. The parameters of the switches are listed in Table 2.

Table 2. Parameters of the semiconductors.

Parameter	UJC0650K	IPP60R060P7
V_{DS}, V	650	650
R_{DS_on}, Ω	34	60
I_{D_max}, A	36.5	38
t_{d_on}, ns	29	23
t_r, ns	10	12
t_{d_off},ns	70	79
t_f, ns	15	4
Q_{rr}, µC	0.95	2.9

Note that the semiconductor parameters from the datasheet are given under some conditions: constant drain current, environment temperature, case temperature and other conditions. Thus, it is impossible to acquire the same efficiency obtained in the experiment tests. Besides, the parasitic parameters of the board also influence the dynamic characteristics of the switches. Therefore, the calculation has some errors and expresses an approximate shape of efficiency as compared with that of a real case.

First, the static loss will be considered. Logically, to increase the number of cells, the static losses should be decreased because the current is evenly split between the cells. The last statement is an advantage. Figure 6 presents dependences for the static loss. The boost case causes significant differences in the static losses with different amounts of cells. However, a big difference can be seen with the higher input power, for example, from 1 kW, as shown in Figure 6a. On the other hand, the lower input power does not affect static losses considerably, even with a great boost ratio (Figure 6b).

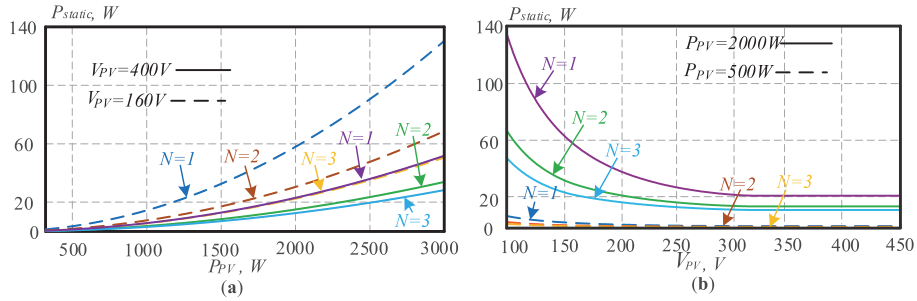

Figure 6. (**a**) Dependence of static losses on the input power at constant PV voltage, (**b**) dependence of static losses on the PV voltage at constant input power.

Despite the static losses decreasing under greater number of cells, the dynamic losses are increasing. The reason is the number of commutations, because four semiconductors are added with each additional cell. However, the current distribution in the case of several buck-boost cells provides fewer dynamic losses for a single component, but the number of components is increasing. Figure 7 shows dependences of dynamic losses based on the PV voltage and the input power. The dynamic losses are rising linearly with a higher input power, while the PV voltage is constant, as shown in Figure 7a. The dynamic losses with three buck-boost cells are greater than with one or two cells during a wide range of the input power and voltages. Thus, when an engineer designs an interleaved approach, the weight of static advantages versus the weight of dynamic drawbacks must be estimated.

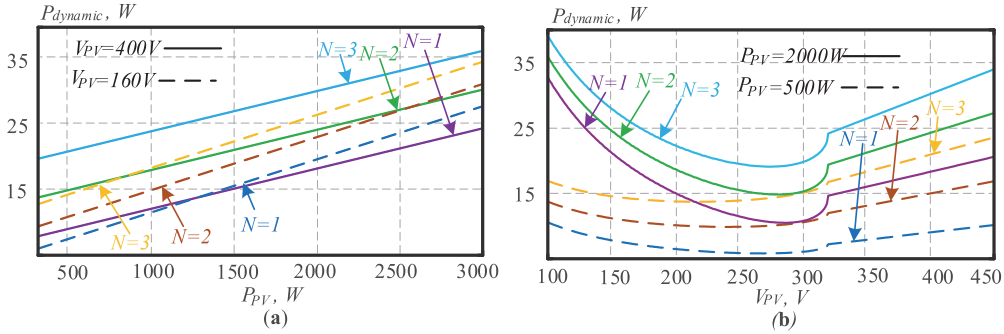

Figure 7. (**a**) Dependence of dynamic losses on the input power at constant PV voltage, (**b**) dependence of dynamic losses on the PV voltage at constant input power.

Finally, the dependences of the efficiency based on the input voltage and the input power were built. Figure 8 shows that the interleaved approach is more effective with higher input power. The inverter with two or three cells has better efficiency at the input power over 800 W in the case of boost (Figure 8a). The buck mode is more effective at the input power over 2 kW, as shown in Figure 8b. However, the results of the efficiency depend on the switches that were chosen, i.e., this efficiency dependence is in correspondence only for an inverter with selected transistors (Table 2).

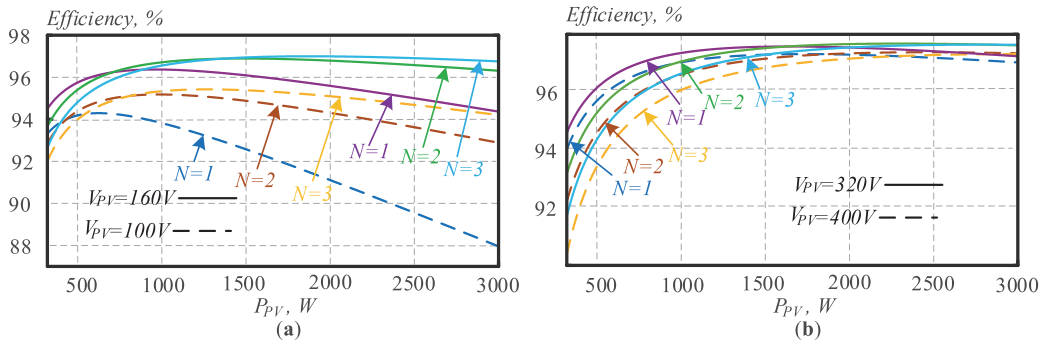

Figure 8. The results of the switch efficiency calculation for different number of buck-boost cells: (**a**) in the case of buck-boost, (**b**) in the case of only buck.

Switch S_2 can be changed by diode. In Section 3 equations for transistor were presented. Comparative study of system with transistor and diode reviled small influence of this factor on efficiency in general. Transistor instead of diode allows for a more flexible control strategy. On the other hand, it should be mention that transistor in boost mode has bigger static losses then dynamic. And in buck mode dynamic losses prevail on static losses. Figure 9 demonstrate insignificant influence of component type on efficiency in buck-boost and buck mode for a different number of parallel cells. For these reasons, diode was chosen for experimental study.

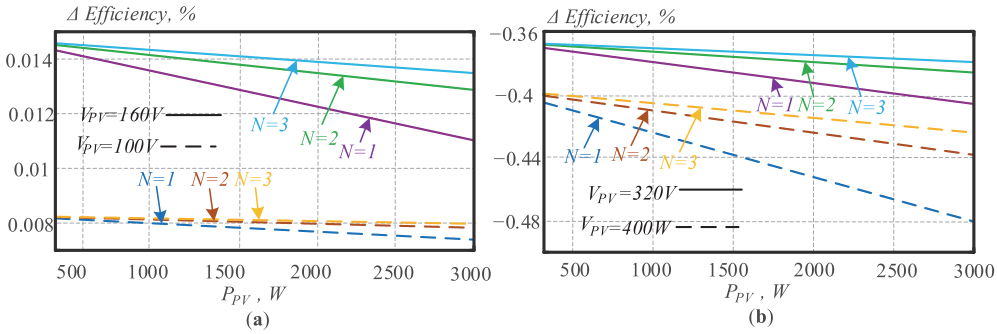

Figure 9. The results of the switch efficiency comparison of buck-boost cells: (**a**) in the case of buck-boost, (**b**) in the case of only buck.

4.2. Qualitative Assessment of the Interleaved Approach

Based on the results obtained, theoretical assumption about the efficiency of the interleaved approach for the buck-boost cell in terms of active component losses was verified. On the other hand, there are other parameters that should be taken into account during designing, such as size of the power converter because it requires a greater number of switches and more driver circuits; the cost of element base; the passive elements. This section presents the qualitative comparison between the single-, two- and tree cells by a square of the power board, overall energy of inductances, efficiency and cost of semiconductors.

The influence of the interleaved approach on the linear size of the converter was analyzed. This parameter establishes relationship between the number of active components, their control circuits and PCB size. The area for the one buck-boost cell S_{BB_cell} consists of the area of inductors S_L, the area of the active switch S_{SW}, which is multiplied on the number of active components and the area of the driver S_{Driver} for each semiconductor. The area for unfolding circuit was calculated by the same method for different types of switches and is presented as a constant parameter S_{UNF}. The overall area of the inverter can be obtained by the next expression:

$$S = N \cdot (S_L + 4 \cdot (S_{SW} + S_{Driver})) + 4 \cdot (S_{UNF} + S_{Driver}). \quad (22)$$

The second parameter compared is an overall inductance energy of the inverter. This parameter contains the sum of the energy of all inductances. The energy of the inductor allows indirect estimation of the size of the inductor because it depends on the inductor value and the maximum current. The overall energy of inductances is as follows:

$$E_L = N \cdot \frac{I_L^2 \cdot L_1}{2} + \frac{I_{GRID}^2 \cdot L_{GRID}}{2}. \quad (23)$$

The third parameter is the cost. With regard to the interleaved approach, it is necessary to consider the cost of all semiconductors C_{BB_SW}, C_{UNFOLD_SW} and their drivers C_{Driver}. Besides, the cost of the inverter depends on the board size C_{PCB}. The cost of the inverter based on the number of cells is obtained by the next expression:

$$C = 4 \cdot N \cdot (C_{BB\_SW} + C_{Driver}) + 4 \cdot (C_{UNFOLD\_SW} + C_{Driver}) + C_{PCB}. \quad (24)$$

The last parameter mentioned in Section 4.1 is the efficiency. All the parameters were normalized on the single cell, except for the efficiency. However, some aspects were missing. For example, with the number of parallel cells increasing, the control system complexity also increases. This trend leads to extremely expensive MCU or even FPGA for three and more parallel cells. But many chips contain a sufficient number of PWM channels that cover single-, two-, or three cells.

Figure 10 shows the diagrams that compare the buck-boost cells in relative units. The condition of the comparison was that the efficiency of several buck-boost cells is higher or the same with a single cell. The overall inductance energy is 2 times lower in the case of two buck-boost cells and 3 times lower in the case of three cells, respectively. However, the cost and the area are increasing linearly with the higher cells, as shown in Figure 10a. The efficiency of the inverter is the same for all sets of cells in the case of the buck mode. The boost mode is more effective for higher sets of cells (Figure 10b).

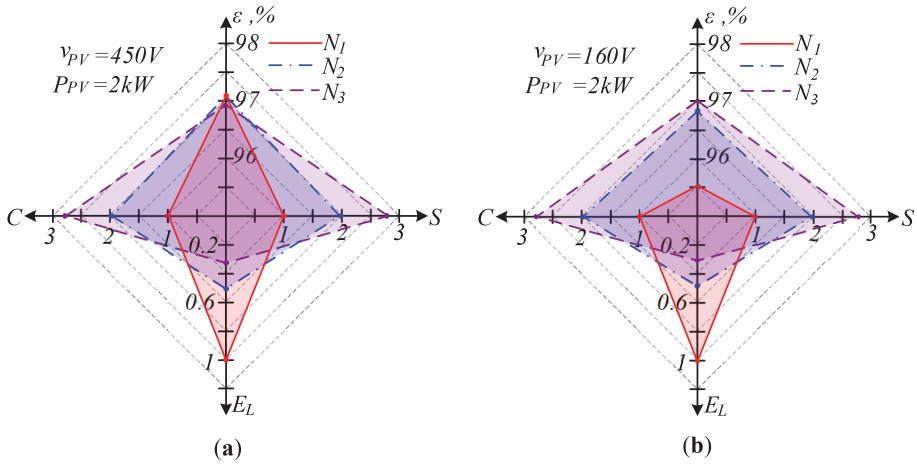

Figure 10. Comparison diagrams for the cost, the area on board, the inductor energy and the efficiency: (**a**) for the buck case, (**b**) for the boost case.

Finally, the optimal number of buck-boost cells can be obtained from the previous calculation and estimation. In the case of the current case study system, the optimal number is single-, or two- buck-boost cells because with the second cell, the efficiency is growing up in the boost mode, while it is the same during the buck mode. Further cell number increase will lead to a significant cost increase without a significant efficiency increase.

5. Control System Description

For the efficiency measurement, the open-loop system was chosen. Figure 11 shows the strategy of the modulator with Pulse Width Modulation (PWM). The principle is as follows: the sine signal is generated by the control unit; the reference signal is compared with the input voltage and with zero; the result of the comparison with the input voltage leads to choosing a suitable mode, while the comparison with zero changes unfolding circuit signals; all the results are going to PWM, as shown in Figure 11a. The principle of PWM is demonstrated in Figure 11b.

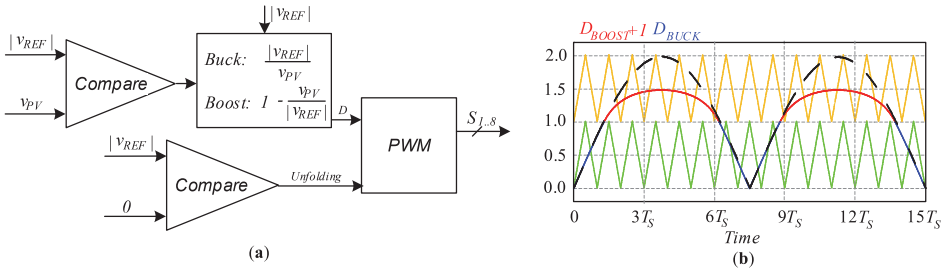

Figure 11. The modulator inside strategy: (**a**) generation reference signals for PWM, (**b**) the PWM principle.

The closed-loop system provides stable operation with a grid connection. The control system consists of the next blocks: Phase-Locked-Loop block (PLL), Maximum Power Point Tracking (MPPT), Model Predictive control (MPC) and Modulator, as shown in Figure 12 [42].

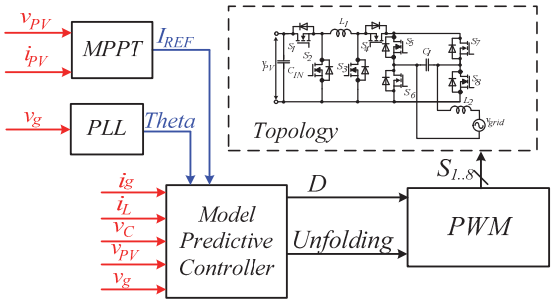

Figure 12. Closed-loop control system structure based on Model predictive control.

There are three current and voltage sensors in the system. These sensors provide measurement of the input and the output voltages and currents. Measurements of the current in the inductances and the voltage of the capacitor are necessary to achieve the required accuracy.

The system is synchronized with the network voltage by using a PLL block. The MPPT calculates the amplitude of the PV output current to produce the reference signal. The system selects the operation mode and calculates the optimal value of the duty cycles for the converter based on the weather conditions, solar irradiation, and other parameters. The MPC block predicts the next values of the currents and voltages and selects the necessary duty cycle for the next high-switching period. MPC also defines the state of the unfolding circuit. Finally, the new duty cycle and the unfolding states are sent to PWM.

6. Experimental Verification

Results of experimental verification were obtained from the designed converter prototype (Figure 13). The prototype consists of the power PCB with all active and passive components, filters, driver circuits, control and measurement PCB based on the microcontroller unit (MCU) TMS320F28379 of the Texas Instruments, which provides the MPPT and MPC control algorithm. Selected MCU contains four independent cores that provide sufficient computing resources to implement a complex control system. In addition, MCU includes a fast 16-bit differential Analog to Digital Converter (ADC) block.

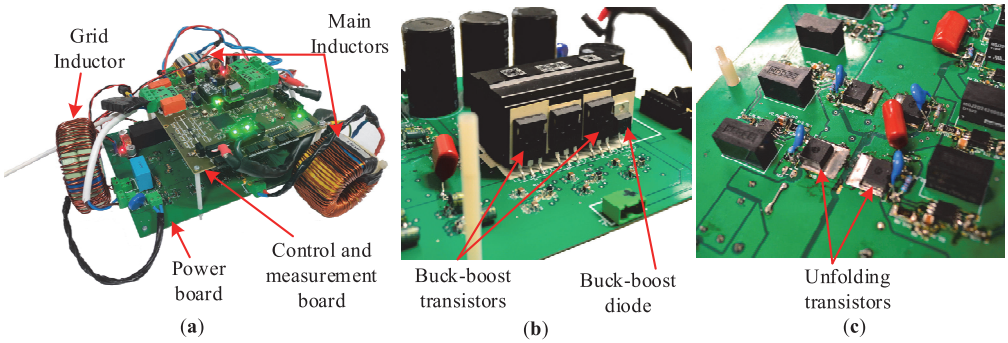

Figure 13. (**a**) Experimental prototype of the converter, (**b**) buck-boost transistors, (**c**) unfolding transistors.

The control and measurement PCB contains five voltage sensor channels. Two of them provide AC voltage measurement in the range from 0 V up to 500 V. The other three sensors were designed for DC voltage measurement. The whole control circuit is galvanically isolated from the power part. The control system has the hardware and software protection items, such as a fuse, varistors, relays galvanic isolated buffers, and some software predefined limits for the measured parameters.

The inverter power PCB was designed for two parallel DC/DC cells with individual inductors, one unfolding circuit, input and output filters, and switch driver circuits. All the inductors were designed manually. Two inductances for the DC/DC stage have current limit of 10 A and the grid inductor current limit is up to 15 A. The input filter consists of three electrolytic capacitances, which are equal to 100 µF. The output filter includes an inductance of 0.3 mH.

Two different models of transistors were used for the high frequency DC stage and low frequency unfolding circuit. The main parameters of all the used active components are presented in Section 4, Table 2. DC/DC stage contains six switches UJC0650K in two parallel cells. Unfolding stage includes four transistors IPP60R060P7 (Figure 13c). The transistor S2 of the buck-boost cell is replaced by a SiC diode CREE C3D10065. All buck-boost semiconductors are placed on a common heatsink (Figure 13b). The unfolding switches have only static losses, they were placed on the power board without any heatsink.

Figure 14 demonstrates a particular case of the experimental results for the open-loop system of the buck-boost inverter based on unfolding circuit with two cells. Diagrams for the boost case are presented in Figure 14a–d and for the buck case in Figure 14e,f. The input voltage equals 190 V or 250 V for boost cases and 320 V for the buck case. The output voltage satisfies the main requirements for the grid voltage. Figure 14b,d,f shows the high-frequency ripples of the input inductor current.

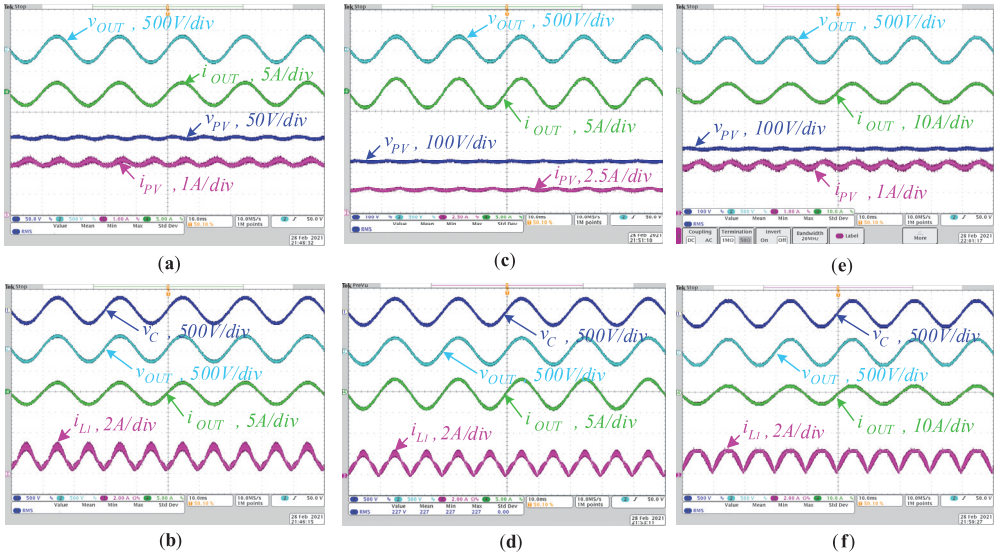

Figure 14. The input and output currents and voltages along with the high-frequency ripples of the input inductor currents of the buck-boost inverter based on unfolding circuit with two cells: (**a**,**b**) three panels VIN = 190 V, (**c**,**d**) four panels VIN = 250 V, (**e**,**f**) five panels VIN = 320 V.

The efficiency diagram is presented in Figure 15. The results for the efficiency are approximately similar to those calculated, as it was explained in Section 4. In the determination of the differences between the mathematical expressions and the experimental results, as established in the losses model, thermal changing of the parameters of the

switches, such as revers recovery charge Q_{rr} and measurements error, were not taken into account. Consequently, theoretical assumptions were confirmed by experimental results. The efficiency was measured with the analyzer YOKOGAVA WT1800. Figure 15a shows the real efficiency along with theoretical in the boost mode. The buck case lines are shown in Figure 15b.

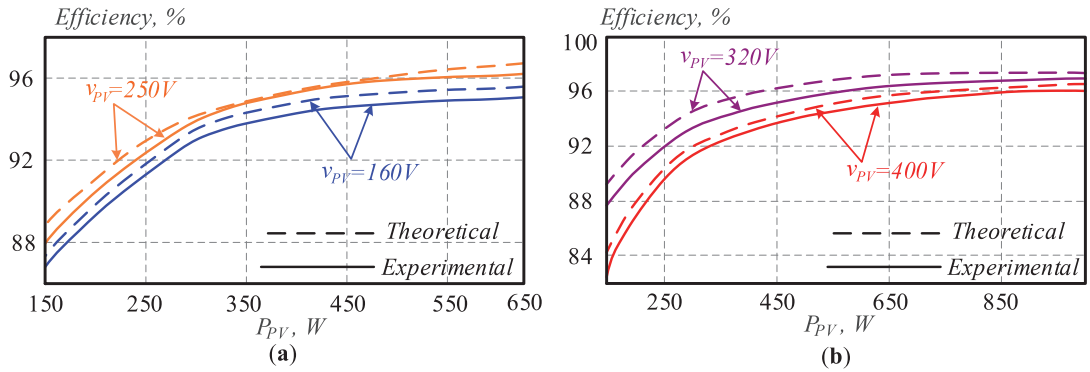

Figure 15. Experimental efficiency of the buck-boost inverter based on unfolding circuit along with the calculated curve: (**a**) boost case, (**b**) buck case.

The results of the closed-loop system based on MPC are shown in Figure 16. The integral MPPT algorithm is used. The PV string contains five serial panels. The open-circuit voltage was around 410 V. The MPP voltage equaled 350 V, while the MPP current reached 2 A, as seen in Figure 16b. The system is stabilized with the THD of the grid current less than 5% (Figure 16c). The sine shape of the grid current is so good that it allowed us to tune the MPPT with no problems. As a result, the experimental results confirmed the control strategy within the efficiency theory.

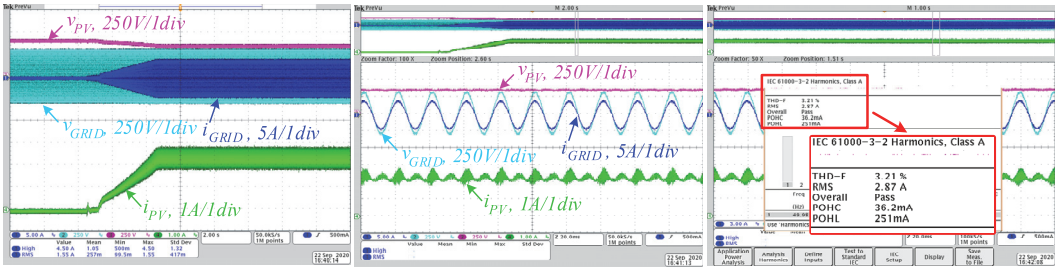

Figure 16. Experimental results of the closed-loop system: (**a**) MPPT operation, (**b**) the grid and input currents and voltages, (**c**) THD estimation.

7. Conclusions

The design and experimental validation of a single-stage PV string inverter with an optimal number of interleaved buck-boost cells are presented. The inverter can provide stable operation under the range of the input voltage from 100 V up to 500 V. Moreover, different PV strings can be applied for this solution. Thus, the selected topology of the inverter is suitable for PV application.

The theoretical calculation allows the estimation of real efficiency and finding the optimal number of the buck-boost cells. The theoretical dependences of the efficiency were obtained based on the parameters of the transistors UJC0650K and IPP60R060P7.

The optimal number of cells depends on the cost of the inverter, on the area of the power board, on the overall energy of the inductances, and on the efficiency. The results showed that the cost and the area of the power board are increasing linearly when the additional buck-boost cell is added. The energy of inductances is also decreasing linear, so it is possible to reduce the size of the inductances with the larger number of cells. Besides, the efficiency is increasing with the higher input power. Thus, two cells were obtained as the optimal number for this research.

The real PV string characteristics with the real PV string were used in theoretical and experimental parts. The set of the 7 serial HNS-SD140 panels provided 1 kW of the input power. The real prototype was designed for the theoretical verification. The simple open-loop system was used for the efficiency measurements. The closed-loop system based on MPC provides reliable operation of the inverter in the grid-connected system.

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Bidirectional Twisted Single-Stage Single-Phase Buck-Boost DC-AC Converter

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Abstract: This paper describes a bidirectional twisted single-phase single-stage buck-boost dc-ac converter based on an output unfolding circuit. This solution is derived by the combination of an inverting buck-boost dc-dc converter and an unfolding circuit. The operation principle, component design guidelines, along with the control approach are presented. The zero-crossing distortion problem is discussed and solved by a simple approach. The simulation and experimental results confirm all theoretical statements. Loss distribution and achievable efficiency are analyzed. Finally, the pros and cons of the proposed solution, along with the most promising application field, are analyzed and discussed in the conclusion.

Keywords: unfolding circuit; bidirectional dc-ac converter; buck-boost converter

1. Introduction

Renewable energy sources require advanced technologies. A photovoltaic (PV) system stands out among the present and future energy systems. The concept of a near zero energy building requires the presence of additional storage elements, which raises the cost of the overall system.

A solar inverter, as part of the PV system, contributes substantially to the overall price and efficiency of the system. System optimization, in terms of price, efficiency, input voltage range operation, and power density, is the priority task in power electronics research. The Google Little Box Challenge (GLBC) demonstrated a close relation with the topic of high-power density inverters for PV applications [1–3]. The main GLBC project outcome is the concept of a very high-power density converter. The finalists demonstrated that a basic full-bridge interleaved inverter with an active decoupling circuit, along with wide band-gap semiconductors utilization, may give the best result in terms of power density. At the same time, the mass production market demands simple and cheap solutions. Usually, power density optimization is not a first level priority.

In PV systems, several configurations can be used [4,5]. Single PV panels are available for low power applications. A partial shadowing in the serial or string connection leads to a significant voltage drop, which in turns leads to a wide range of input voltage variations during the energy utilization time. An intermediate voltage boost dc-dc converter can be used to overcome this drawback. It is shown in Figure 1a.

Another application field of the dc-ac converter with wide input voltage regulation is battery storage. Lithium-ion batteries are targeted to become the most popular choice for on-grid and grid-off solar battery storage in the foreseeable future. Such types of batteries have a wide range of input voltage. A converter that accepts different storage elements is preferable.

Several single-stage alternatives were presented as alternative solutions. Inverters with an active boost cell were described in [6–9]. These inverters provide very high boost of the input voltage but suffer from high current spikes in the semiconductors and passive elements. Impedance-source networks have been reported in many research papers as a promising single-stage solution. Z-source inverters (ZSIs) and quasi-Z-source inverters (qZSIs) were proposed for different applications. Existing solutions were reviewed in [10–14], and different relevant issues are addressed in [15–20]. However, recent research revealed evident drawbacks of the IS-based converters in terms of power density and efficiency [21–23].

Split-source inverters (SPIs) [24,25] were proposed as another alternative solution. According to the literature, SPIs have less passive component counts accompanied by higher voltage and current stresses at lower voltage gains, and they do not have short circuit immunity.

Several interesting single-stage buck-boost inverters were proposed in [26–29]. At the same time all of them did not find industrial application. For example, the solution [26] requires reverse-blocking IGBTs, while others are quite complex solutions.

An Aalborg inverter (Figure 1b) is proposed as an inverter that combines buck and boost functionality [30–35]. These solutions have two independent buck-boost stages that are responsible for output sinusoidal voltage generation. The main advantage of the proposed solution is in the minimum voltage drop of the filtering inductors in the power loop at any time. At the same time, this solution uses a double number of semiconductors and an inductor in the buck and boost stage, which is an obvious drawback. Another drawback consists in the two power sources utilization. A similar idea with double components is discussed in [36].

The solution based on the input boost and buck converter along with a line frequency unfolding circuit was proposed in [37,38]. The input voltage is boosting to the constant dc-link voltage. The Buck stage performs further modulation, which is unfolding to the sinusoidal voltage.

A modified solution based on the inverting buck-boost dc-dc converter that allows reducing count of inductors is proposed in [39,40]. This paper discusses a grid-connected application of the proposed above discussed solution along with its bidirectional application which extends its application. The objective includes designing a closed-loop control along passive component design with efficiency estimation.

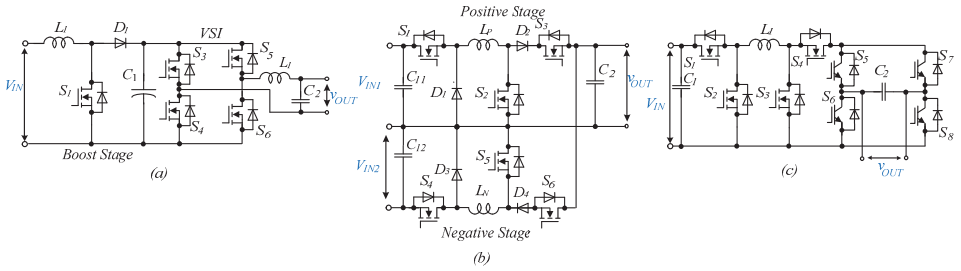


Figure 1. Conventional boost dc-dc converter along with voltage source inverter (**a**), Aalborg inverter (**b**), buck-boost inverter with unfolding circuit (**c**).

2. Control System of Twisted Single-Phase Single-Stage Inverter based on Unfolding Circuit

The discussed single-phase single-stage buck-boost dc-ac converter based on the unfolding circuit is depicted in Figure 2. This circuit consists of inductances L_1, L_2 capacitors C_1 and C_2, switches S_1, S_2, and low frequency switches T_1–T_4. The switch S_2 can be replaced by a diode D_1 in the case of unidirectional operation.

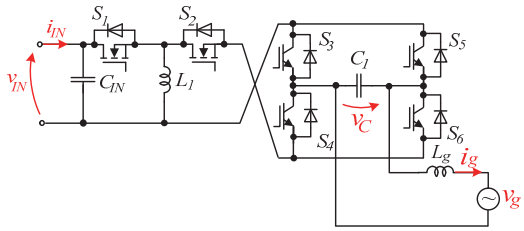


Figure 2. Single-phase twisted single-stage bidirectional buck-boost dc-ac converter based on unfolding circuit.

According to the classical definition of the unfolding circuit, transistors T_1–T_4 realize a simple unfolding circuit. However, these switches can also be used for high frequency modulation.

The proposed solution is derived from the conventional buck-boost dc-dc converter that has a following gain factor B:

$$B = \frac{D}{1-D}, \tag{1}$$

where D represents the duty cycle of the switch S_1. Taking into account the instantaneous reference output voltage $v_{c2}(t)$, the instantaneous value of the duty cycle $D(t)$ can be expressed as follows:

$$D(t) = \frac{|v_C(t)|}{v_{IN} + |v_C(t)|}, \tag{2}$$

Figure 3a shows a general control system approach along with the modulation technique. It should be mentioned that the main task of a high-level control system depends on the particular application. Using an output current as a feedback signal, the modulation signal V_{MOD} can be derived by different control approaches including a resonant controller, DQ control, model predictive control, etc. A well-known Second Order Generalized Integrator (SOGI) phase-locked loop (PLL) algorithm for grid synchronization is used in [41].

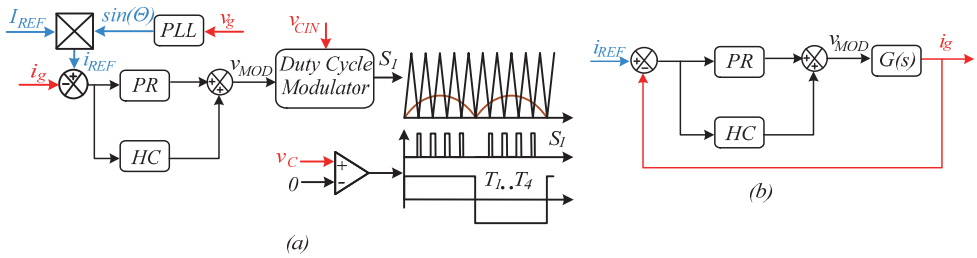


Figure 3. Control system structure for the proposed solution (**a**) and closed-loop control equivalent circuit (**b**).

The duty cycle modulator defines the duty cycle value according to Equation (2). This value defines the switching signal of the transistor S_1 by means of a very simple modulation technique. The unfolder's transistors are controlled by a simple comparison of the capacitor voltage with the zero level.

The modulation signal V_{MOD} is derived from the output current controller. In this case, a simple proportional-resonant (PR) controller with Harmonic Compensation (HC) was used. The control system tuning is based on the transfer function of the proposed solution, which is derived from a small signal model [42]. The transfer function is shown in Figure 3b.

The PR-controller factors were determined based on the transfer function, which takes into account the input stress as the changing of the duty cycle:

$$G(s)\Big|_{\hat{u}=0} = \frac{\hat{i}_g}{\hat{d}} = \frac{N(s)}{sM(s)} \tag{3}$$

The small signal designing is a suitable approach for explaining the topology by analytic expressions. The equivalent circuits include the parasitic resistance of each passive element (Figure 4). These parasitic parts include resistors of on-state semiconductor switches. The presence of three passive elements leads to polynomials with third order in the denominator:

$$\begin{aligned} N(s) = {} & \tfrac{(C_1Rs+1)}{R(1+D')} \cdot \Big[L_1 s\Big(v_g + V_D - \Big(v_g + v_{IN} + V_D\Big)D\Big) + \\ & \Big(2v_{IN} + 3v_g + 3V_D - \Big(v_g + v_{IN} + V_D\Big)(3 + D') \cdot D\Big) \cdot R\Big], \end{aligned} \tag{4}$$

$$\begin{aligned} M(s) = {} & \Big[C_1L_1L_g s^3 + C_1Rs^2 \cdot \Big(L_g \cdot (1 + D') + 2L_1\Big) + \\ & s \cdot \Big(C_1R^2 \cdot (1 + D' \cdot (2 + D')) + L_g \cdot (D')^2 + L_1\Big) + \\ & R \cdot (1 + D')\Big] \cdot s, \end{aligned} \tag{5}$$

where D' is a reverse value of the duty cycle, and each parasitic resistance is replaced by R.

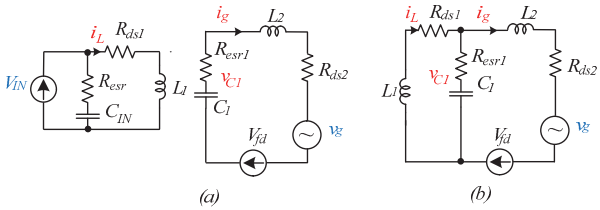


Figure 4. Equivalent circuits of a twisted buck-boost converter-based unfolding: on-state of forward transfer (**a**), on-state of reverse transfer (**b**).

The tuning approach described in many research papers does not contain any novelty. Reference current I_{REF} can be derived from a high-level algorithm that depends on a particular application, which is out of scope of this paper. If the power flows from the dc to the ac side, it can be derived from the high-level maximum power point tracking algorithm or the battery discharging algorithm. In an opposite power flow, it can be derived by the battery charging algorithm or an additional capacitor voltage v_{c2} control loop.

3. Component Design Guidelines for Bidirectional Operation

This section describes guidelines for the design of passive and active components taking into account predefined parameters and target losses level in the system.

The main approach of passive element design has relevance to the steady-state analysis. Each period occurs with the processing of energy storage by the input inductance (Figure 4a) and is immediately transferred to the load (Figure 4b). It should be noted that the parasitic parameters are not taken into account in the calculation.

As a rule, the expression of the pulsations of the output capacitor voltage depends on the capacitor current, the switching frequency, and the value of the capacitance. However, the change of the output current depends directly on the ac-part of the capacitor voltage. The area of the capacitor voltage ac-part is proportional to the ripples of the output current.

The values of passive components are expressed as:

$$L_1(\varphi) = \frac{V_{IN}^2 \cdot V_M^2 \cdot \left|\sin(\varphi)\right|}{2K_L P f\left(V_{IN} + V_M \cdot \left|\sin(\varphi)\right|\right) \cdot (V_{IN} + V_M)} \tag{6}$$

$$C_1(\varphi) = \frac{2P \cdot \sin^2(\varphi)}{2K_C V_M f\left(V_{IN} + V_M \cdot \left|\sin(\varphi)\right|\right)} \tag{7}$$

$$L_g(\varphi) = \frac{K_C V_M^2}{16 K_g P f} \tag{8}$$

where φ is a current phase of the grid voltage, V_M is the amplitude of the grid voltage and K_L, K_C, K_g are coefficients of corresponding element ripple. The ripples of elements are defined as follows:

$$K_L = \frac{2\Delta i_L}{I_{LMAX}}, K_C = \frac{2\Delta v_C}{V_M}, K_g = \frac{2\Delta i_g}{I_{gMAX}}, V_{INp.u.} = \frac{v_{IN}}{V_M}. \tag{9}$$

The obtained expressions show the dependence between the optimal values of the passive components and the phase of the grid voltage. Also, the high-switching side of the topology allows obtaining a current with only positive values.

Figure 5 shows the influences of the passive component values on the ratio between the input stress and the amplitude of the grid voltage (Equation (9)) at constant input power and input current.

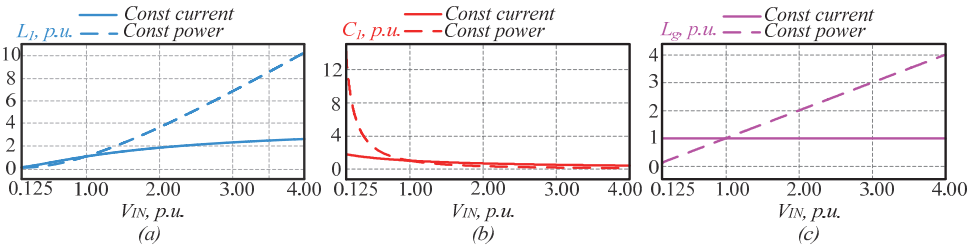


Figure 5. Influences of the buck-boost on the passive elements at constant input power and current: the main inductance (**a**), the output capacitance (**b**), the output inductor filter (**c**).

The ripple factor is constant for each element. All the values of inductances or the capacitor are normalized to their value at a point when the input voltage equals the grid voltage maximum:

$$L_{1p.u.} = \frac{L_1}{L_0}, C_{1p.u.} = \frac{C_1}{C_0}, L_{gp.u.} = \frac{L_g}{L_{g0}}, \tag{10}$$

where L_0, L_{g0}, C_0 represent values of the passive elements when the ratio $V_{INp.u.}$ is equal to one unit.

To select a semiconductor, the losses model of the proposed solution is proposed and analyzed. The switching and conduction losses of the MOSFET transistors are taken into account [43]. The conduction losses model is illustrated in Figure 4—it includes the drain-source resistance R_{ds} of transistors, the equivalent series resistance R_{esr} of capacitors and voltage drop on the diode V_{fd}.

Figure 6 demonstrates the power losses of the topology as the function of the power and the input voltage.

The switching losses at the constant input current and the constant input power are shown in Figure 6b. Figure 6c shows the overall expected efficiency of the converter as a function of the input voltage. In this case, different distributions between the conduction and the switching losses are considered. In the first case (dotted line), semiconductors with a good static characteristic are

considered, while in the second case, the conduction losses dominate. The main idea of this quality analysis is to show the possibility of the maximum efficiency point tuning and optimization.

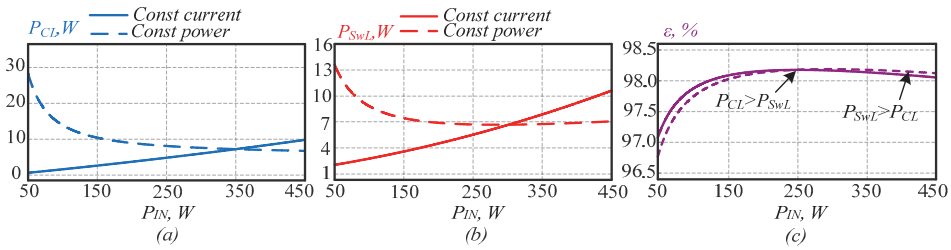


Figure 6. Power losses estimation of the inverter: conduction losses of semiconductor switches (**a**), switching losses of transistors (**b**), efficiency estimation (**c**).

As a conclusion of this section, the values of the passive elements determine the pulsations of current in transistors. The proper selection of the passive components can avoid discontinues current mode, that could lead to unstable behavior. At the same time, the selected topology does not have a dc-link stage, thus no dc-link electrolytic capacitors are required.

4. Simulation Verification of Bidirectional Operation Capability

To verify the theoretical statements and basic operation modes, simulations were performed for proposed solutions in PSCAD simulation tool (Figures 7 and 8). Since the PV or different storage batteries are considered as possible application scenario, a wide range of the input voltage is defined. The values of passive components are illustrated in Table 1.

Table 1. Passive components used for simulation verification.

Passive Components	Value
Input capacitor, C_1	330 uF
Inductor, L_1	1800 uH
Unfolding capacitor, C_2	2.1 uF
Grid side inductor, L_2	670 uH
Switching frequency	60 kHz
Sampling frequency	15 kHz

Figure 7 shows the simulation diagrams for low input voltage and low input power operation mode. Figure 7a shows the rectifier mode, while Figure 7b shows the inverter mode. An ideal sinusoidal grid is considered. In the inverting operation, the average dc input voltage is equal to 250 V, while RMS output voltage is equal to 230 V, and input power is about 250 W. It can be seen that the input current has a continuous mode which is achieved by means of a simple input capacitor.

At the same time, its value is relatively small. In the reverse operation, the sign of reference PR controller current is changed, while the control structure remains the same.

Figure 8 demonstrates very similar simulation results for an increased input voltage (350 V) and power (850 W).

The main outcome from these figures is that simulation results correspond to the theoretical expectation. A very simple control system can provide bidirectional operation with acceptable grid current quality.

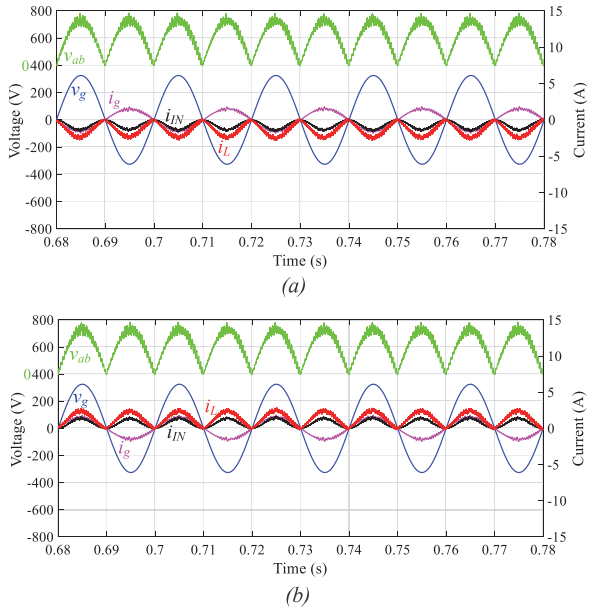


Figure 7. Simulation results for Vout = 250 V, Pin = 250 W in rectifier mode (**a**) and inverter mode with Vin = 250 V (**b**).

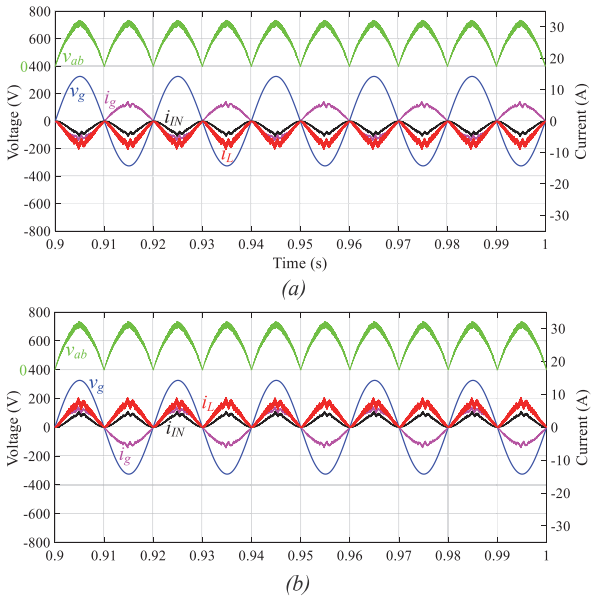


Figure 8. Simulation results for Vin = 350 V, Pin = 850 W in rectifier mode (**a**) and inverter mode (**b**).

5. Experimental Verification

Figure 9 shows the experimental setup for the studied solution. It consists of an inverter PCB board, a control board and an inductor. The passive elements correspond to the simulation study.

The high switching transistors S_1, S_2 are realized on the MOSFET SiC transistor C2M0080120D along with SiC diode D_1 C3D10012A. The diode was used as an alternative solution for unidirectional operation. The unfolding circuit is based on the MOSFET transistors IPB60R060P7ATMA1. These transistors have the poor dynamic characteristics but low static losses.

All the diagrams were derived by current probes Tektronix TCP0150, and voltage probes Tektronix TPA-BNC along with the digital oscilloscope Tektronix MDO4034B-3. A general approach to the experimental verification is shown in Figure 4. A high performance power analyzer YOKOGAVA WT1800 was used for efficiency measurement.

The control system is based on a digital signal processing (DSP) controller and a low-cost field-programmable gate array (FPGA). External ADC converters were implemented to provide high accuracy. This approach is justified by the very high switching frequency of the transistors and the high-level demand of the calculation resources. As a result, the functionality is detached between the FPGA and the DSP. This test bench allows the realization of any PWM technique with a high switching frequency and high resolution. At all operation points, the switching frequency was 60 kHz.

Our experimental study was targeted to achieve several aims. First, the aim was to analyze the influence of the separate control of high switching and unfolding transistors on the zero crossing distortion. Second, the focus was on the influence of synchronous switching of transistors S_1 and S_2 on the zero crossing distortion. Finally, a detailed efficiency study was conducted.

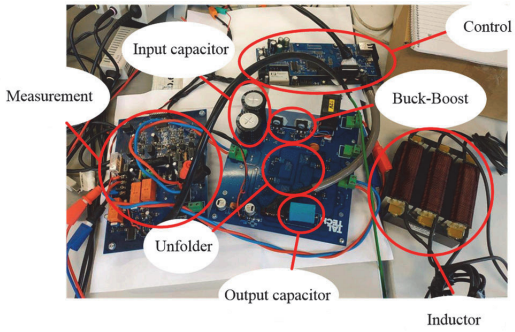
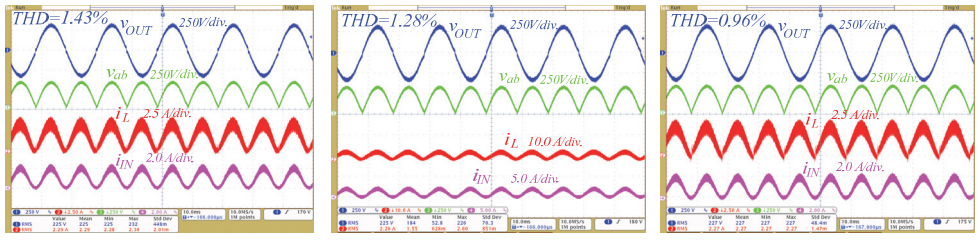


Figure 9. Experimental setup of the twisted buck boost converter with unfolding circuit.

Figure 10 shows the experimental results at low input voltage V_{in} = 250 V, and at low power P_{in} = 250 W in the inverter mode. In this case, several scenarios were tested. The first scenario (Figure 10a) corresponds to the case without synchronous switching of transistors S_1 and S_2 and without separate control of the unfolding transistors.



(a) *(b)* *(c)*

Figure 10. Experimental results for V_{in} = 250 V, P_{in} = 250 W in the inverter mode without synchronous switching and separate control (**a**), without synchronous switching and with separate control (**b**), with synchronous switching and with separate control (**c**).

Figure 10a shows the output voltage in the grid-off mode, v_{ab} voltage before unfolding circuit, inductor i_L and input i_{IN} currents. As can be seen, zero crossing distortion is present. Figure 10b shows the same diagrams without synchronous switching of transistors S_1 and S_2 but with separate control; zero crossing distortion is slightly reduced but not completely eliminated.

Finally, the influence of synchronous switching was estimated. Figure 10c shows that an ideal output voltage shape is achievable in this case. It is explained by an additional discharge circuit that helps to keep the output voltage across the unfolding capacitor very close to sinusoidal shape. The THD value was estimated for all cases and confirms that the last case corresponds to the lowest value <1%.

Similar experimental results are shown in Figure 11 with increased output current. First of all, it should be underlined that an increase in power leads to a decrease in distortion, even in the worst case. Both of these figures show the open loop operation with a simple passive load.

To confirm the grid-connection operation capability, Figure 12 shows the diagrams in the grid-connected mode. It can be seen that despite current distortion, the experimental results are very similar to the simulation results. Slight distortion is caused by non-ideal laboratory grid voltage that can be improved by more sophisticated control, which is beyond the scope of this work. In this working point, THD values in all cases were less than 1%.

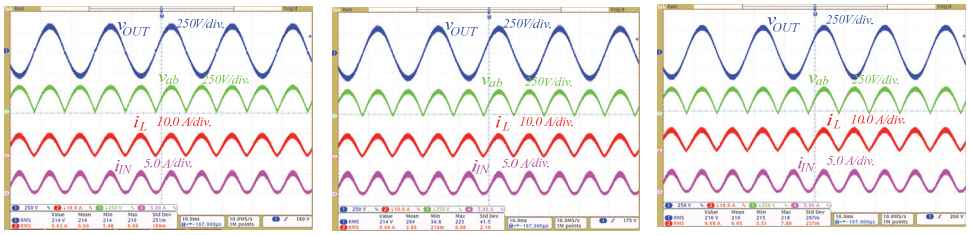


Figure 11. Experimental results for V_{in} = 350 V, P_{in} = 850 W in the inverter mode without synchronous switching and separate control (**a**), without synchronous switching and with separate control (**b**), with synchronous switching and with separate control (**c**).

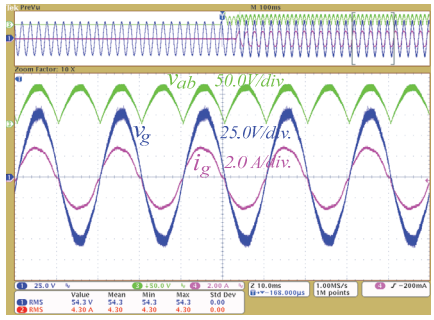


Figure 12. Experimental results of the grid-connected converter in the inverter mode.

6. Efficiency Estimation

The efficiency profile as the function of the input power with constant input voltage is shown in Figure 13a. The open loop unidirectional mode was utilized when the transistor S_2 was replaced by a diode.

It can be seen that the characteristic has the peak value of efficiency at about 95%. The point of maximum efficiency is different at different input voltages. The solid line corresponds to 250 V, while

the split line corresponds to the input voltage of 350 V. At a lower input voltage, the peak efficiency belongs to the input power of 300 W. At an increased input voltage, the maximum efficiency can be achieved with an increased input power as well.

At the same time, Figure 13b shows the dependence of the efficiency as the function of the input voltage with constant power. The power was investigated in a range from 100 W to 1000 W. The two cases are shown. In the first case, the reduced input power is 250 W. It can be seen that the peak efficiency occurs at a relatively low input voltage. A further increase in the input voltage in the constant power mode will lead to the overall efficiency decreasing. In the second case, illustrated by a split line, the power was increased to 850 W. In this case, the peak efficiency point is evidently shifted to the higher voltage.

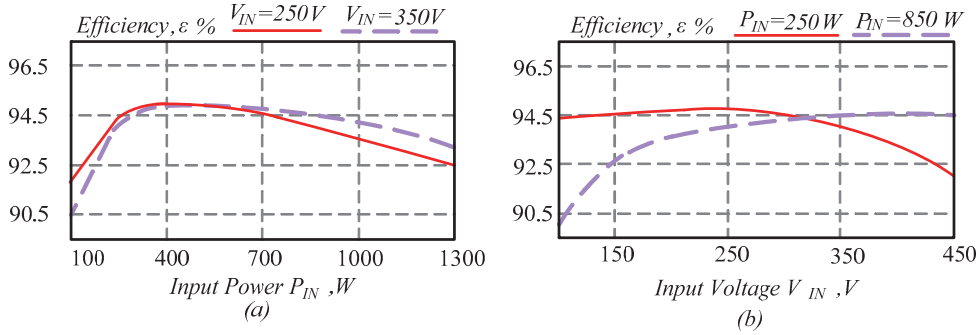


Figure 13. Efficiency versus input power in unidirectional mode with constant input voltage (**a**), efficiency versus input voltage with constant input power (**b**).

The main conclusion is that the converter has some optimal operation point that depends on the input voltage and power level. This conclusion correlates with the theoretical losses model described above. The overall efficiency mostly depends on the conduction losses in the high-switching semiconductors and unfolding transistors. At the same time, it can be optimized for a certain operation point by means of selecting different semiconductors for high switching and unfolding circuit.

Figure 14 shows the next set of experimental tests devoted to the efficiency study in the bidirectional operation mode.

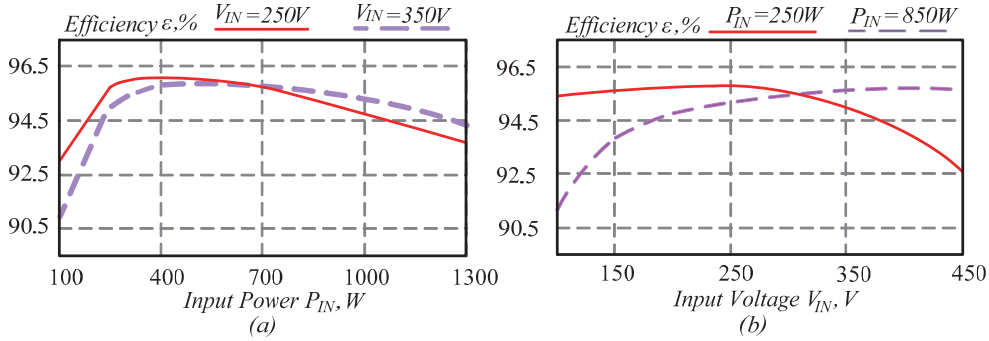


Figure 14. Efficiency versus input power in the bidirectional mode with constant input voltage (**a**), efficiency versus input voltage with constant input power (**b**).

In this case, the diode was replaced by the transistor S_2. The diagrams in Figure 14 are similar to those in Figure 13. It can be seen that the efficiency profile behaves very similar to the unidirectional

mode. The main difference lies in the significant efficiency increase, which in turn, is explained by the reduction of conduction losses. The maximum 96.2% efficiency is observed in this case.

Figure 15 shows pictures from the thermal camera. In the first case (Figure 15a,b) the input voltage and power were reduced, the total efficiency was about 96%. In the second case, the input power increases along with the input voltage. Figure 15c,d shows the corresponding thermal picture. The efficiency in this case was about 95%. Due to the lower efficiency and higher power, the temperature of the semiconductors was significantly higher as well. Figure 15a,c corresponds to the high switching semiconductors, while Figure 15b,d corresponds to the unfolding transistors. At the same time, it can be seen that all semiconductors have an acceptable temperature up to 90 °C.

Another important conclusion is that losses across the high switching transistor S_1 are larger than losses across the high switching transistor S_2. It directly confirms that efficiency increases in case a diode is replaced by a transistor for a bidirectional operation. It is especially evident for the first case when the boost mode is applied and the conduction time of the transistor S_1 is significantly larger.

The losses can be split and estimated separately taking into account datasheet parameters and current in semiconductors. Figure 16 shows the loss distribution for the operation point discussed above.

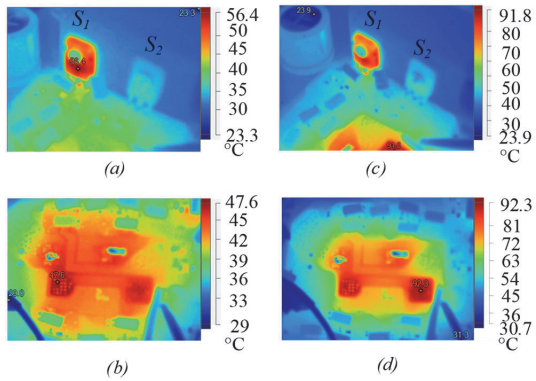


Figure 15. Efficiency study of the proposed solution in the unidirectional mode: thermal picture for 250 V and 550 W (**a**,**b**), and 350 V, 1150 W (**c**,**d**).

Conduction losses have a major contribution in both cases. It is evident that conduction losses increase as the input current increases.

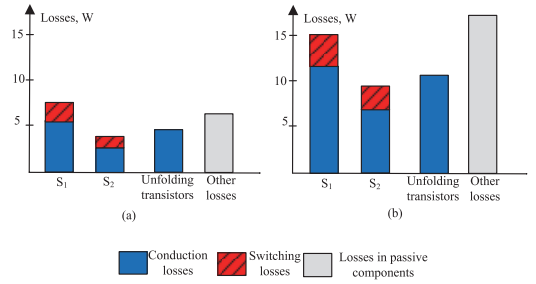


Figure 16. Losses distribution for 550 W at 250 V input voltage (**a**) and 1150 W at 350 V (**b**) input voltage.

The main conclusion from the efficiency study and the thermal pictures is that a converter may have high efficiency in a wide range of input voltage. The efficiency of 96% can be achieved without any extraordinary semiconductors or an interleaving approach. At a constant input current profile, the maximum efficiency does not correspond to the maximum voltage, which perfectly suits the

PV profile. At the same time, this solution can be optimized for a certain input voltage level and bidirectional operation that in turn, means good applicability for battery storage interfacing.

In contrast to conventional solutions, reduced switching losses and EMI are expected since only two semiconductors are involved in the high switching performance.

7. Conclusions

This paper has presented a novel bidirectional twisted buck-boost converter based on the inverting buck-boost circuit and output unfolding circuit in the grid-connected mode. Component design guidelines, along with possible control strategies are given. Simulation and experimental results are confirmed by the theoretical analysis.

The overall efficiency can be very high because only two transistors are involved in high switching performance in any period of operation. Also, it may give benefits in reduced EMI compared to any other competitive solution.

It is demonstrated that a typical problem encountered in an unfolding circuit-based solution that consists in zero voltage distortion can be solved by a simple approach. Synchronous switching of the transistors along with proper control of unfolding transistors enables elimination of the zero crossing distortion. At the same time, synchronous switching leads to higher efficiency.

Also, it is demonstrated that the main advantage of this solution is simplicity, in the ability to work in a wide range of input voltages with high efficiency and high flexibility of the optimal operation point tuning. On the one hand, the maximum input voltage is limited by the maximum voltage stress across high-switching semiconductors. On the other hand, the high-voltage high-switching MOSFET transistor is a verified technology that enables reduction of price and removal of any serious challenges.

As a result, taking into account that efficiency for higher boost is not decreasing, it can be recommended for applications with PV arrays or storage batteries.

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Optimal LCL-filter study for Buck-Boost Inverter Based on Unfolding Circuit

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Abstract— LCL-filter design for a buck-boost inverter based on unfolding circuit is addressed. Our aim is to find the dependencies between the passive components of the smallest size and the stable mode of the system. Guidelines for the design of passive components are provided for both modes. The simulation results confirmed the design and helped to estimate a stable option in different sets of passive elements. In conclusion, the LCL-type can be replaced by the LC-filter based on the correct selection of the output capacitor.

Keywords — inverter, unfolding, buck, boost, filter.

I. Introduction

Today's power electronic converters comprise novel topologies that require an additional analysis to gain the right control and the stable condition tuning. The math approaches [1]-[2] are often used when a question of the dynamic characteristics of the system appears. The ratio between the passive elements should be taken into account as well.

The task of selecting a dc-ac converter topology is a hard exercise, because it depends on pros and cons of the structure. For instance, the grid-connected converters [7]-[8] require algorithms for supplying the stable mode.

One of the methods frequently used is the Proportional-Resonant (PR) controller. The control system based on a PR block can provide high accuracy of the main harmonic of the output current, as it is shown in [9]-[10]. However, a PR controller has a transient process at the start of grid connection, and can lead to unstable mode with different input powers.

On the other hand, many new studies are using the non-linear predictive management technique. The Model Predictive Control (MPC) [11] employs one of the non-linear algorithms. Previously, this method was excluded from the field of power electronics because the resources of the processors did not allow many calculations to be performed quickly. Presently, the existing FPGAs and microcontrollers enable many calculations to be made in a very short period of time. The main benefit of MPC is a creative approach to the cost function of every system. The cost function can comprise both the next predictive values of current and voltages and power loss. Thus, the method of predicting becomes feasible in industry [12]-[13]. Many research papers are devoted to the grid-connected systems based on MPC, such as in [14]-[15].

The implementation of non-linear predictive technique is challenging even for a simple topology in power electronics. The reason is that different math approaches are available to obtain the next predictive values of current and voltages, but the question is - which is a better approach. The State-Space model is a suitable method to obtain the states of a system. Many studies are using the State-Space model for the model predictive control [16]-[18].

The dc-ac converters usually include one of the known filters, such as L-, LC-, LCL- and LLCL- filters. A convention L-filter has an excellent value of inductance, which affects the size of the inverter. The grid-connected inverters traditionally have a L-filter at the output side [19]-[20]. A LC-filter is used in topologies when the control of the output voltage is required. The traditional filter for grid-connection is a LCL-filter, which has a small size and a reduced cost [21]-[26]. Another LLCL-filter was proposed in [27]-[28].

This article describes guidelines for the components design and energy estimation in the coils for the buck and boost modes for a buck-boost inverter based on unfolding circuit.

The main aim is to conduct theoretical analysis and select the passive components of the buck-boost inverter based on unfolding circuit. The objective is to obtain stability of the selected system in according to the LCL-filter resonance frequency.

Section II addresses the design of the passive elements for buck and boost modes. The control system is described in section III. Section IV presents the results of the simulation, the results of the design and component selection. The final section summarizes the main conclusions of this research.

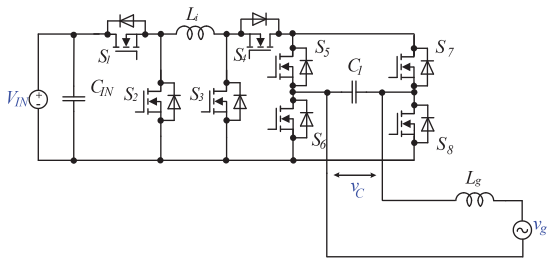

Fig. 1. Buck-Boost inverter based on unfolding circuit.

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II. Design of Passive Components

The selected topology is a combination of the buck-boost dc-dc converter with an additional unfolding circuit, which provides the necessary sign of the voltage on the output terminals. One of the objectives is to study the shape of the power. It is because the average power in case of ac is not the same as with the dc bus application. The resulting average power is half the maximum power:

$$P = \frac{1}{\pi} \cdot \int_0^{\pi} P_{MAX} \cdot \sin^2(\varphi) d\varphi \,,\; P_{MAX} = 2 \cdot P \,, \tag{1}$$

where P_{MAX} - the maximum power, φ - the phase instantaneous value of the output voltage.

A. Definition of Passive Components in the Buck Case

Buck case is related to the higher input voltage versus the output voltage. The buck mode keeps the all-in-one LCL-filter during the switching period. This feature complicates the process of passive component design. Thus, the closed-loop with the grid-connected inverter was considered.

In the design of a LCL-filter only the high switching harmonic is taken into account. A perfect network with just the main harmonic is considered. Figure 2 shows the equivalent circuit for a non-fundamental harmonic definition.

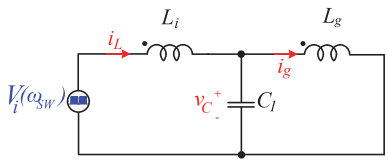

Fig. 2. The equivalent circuit of a non-fundamental harmonic definition.

As is known, the Laplace domain is a powerful tool in the math for the spectrum analyzer. Hence, the definition of a high harmonic of the grid current requires movement in the Laplace domain. The gain of the grid-connected inverter is calculated by the following expression:

$$G_{LCL}(s) = \frac{I_g(s)}{V_i(s)} = \frac{1}{C_1 \cdot L_i \cdot L_g \cdot s^3 + (L_i + L_g) \cdot s} \,, \tag{2}$$

where $I_g(s)$, $V_i(s)$ - the grid current and the input impact in the Laplace domain, C_1, L_g, L_i - passive components.

The stability of the system is an important condition in the filter design. The resonance frequency is one of the key parameters, which depends on the passive elements and can be derived from the denominator of Eq. (2):

$$f_{RES} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{L_1 + L_g}{C_1 \cdot L_1 \cdot L_g}} \,. \tag{3}$$

Moreover, in the design, it is required to define and refer to the resonance frequency. The LCL-filter should consider the whole structure because each of the passive elements depends on the resonance frequency.

The Bode plots of the LCL-filter transfer function are shown in Fig. 3. As is known, the switching frequency along with the sample frequency should be as a minimum two times higher than the resonance frequency (Fig. 3(a)).

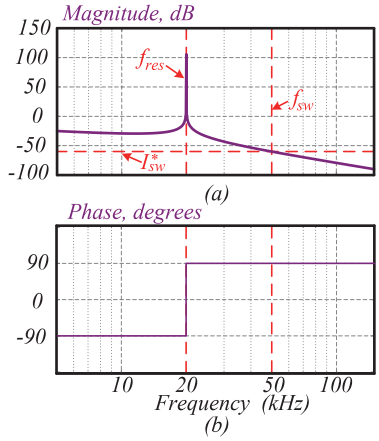

Fig. 3. The Bode plots of a LCL-filter: the magnitude spectrum (a), the phase specturm (b).

The next step is entering the auxiliary relationship between the coils, as shown in Eqs. (4)-(5):

$$L_g = r \cdot L_i \,,\; L = \frac{1}{4 \cdot \pi^2 \cdot C_1 \cdot f_{RES}^2} \,, \tag{4}$$

$$L_g = (r+1) \cdot L \,,\; L_i = \frac{(r+1)}{r} \cdot L \,, \tag{5}$$

where r is the inductances coefficient.

The spectrum of the grid current has different values of the high harmonics. The switching harmonic that brings also some minor frequencies is a significant part. However, only the switching frequency was taken into account.

The Total Harmonic Distortion (THD) of the grid current depends on the inductor factor r; thus, the final task is to solve Eq. (13) with the unknown variable r:

$$THD_I = \frac{I_{SW}}{I_G} = \frac{G^{*SW} \cdot V_i^{*SW}}{I_G} = f(r) \,, \tag{6}$$

The capacitor value was determined previously in [28], as in a simple LCL-filter:

$$C = \frac{\Delta \cdot 2 \cdot P}{V_M^2 \cdot \omega_{SINE}} \,, \tag{7}$$

where Δ - the relative value of the reactive power. It is used in the conventional approach for a LCL-filter in conventional voltage source inverters.

B. Definition of Passive Components in the Boost Case

In the non-linear condition, there are shapes in the boost case, but most of the shapes of the power signals can be distributed in two linear cases. Both equivalent circuits in the boost case provide different passive component connections. Figure 3 shows the equivalent circuit of the buck-boost inverter based on unfolding circuit in the boost mode.

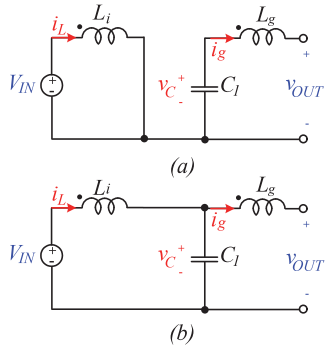

Fig. 4. Equivalent circuit: storage energy by the input inductance (a), energy given to the load (b).

The simple boost converter has the well known gain factor, but the gain of the buck-boost inverter based on unfolding circuit depends on the phase's instantaneous value of the output voltage:

$$D(\varphi)=\frac{\left|V_M\cdot\sin(\varphi)\right|-V_{IN}}{\left|V_M\cdot\sin(\varphi)\right|}, \tag{8}$$

where V_{IN} is the input voltage,

The design of the input inductor and the output capacitor are the same as in a simple boost converter based on a LC-filter. The difference is that there is an additional output inductance as a filter. Thus, the steady state analysis allows us to find the values of the passive components based on the predefined ripples. The differential equations of the first circuit and the change of the inductor current within the change of the output capacitor are given below:

$$L_1\cdot\frac{di_L}{dt}=V_{IN},\quad C_1\cdot\frac{dv_C}{dt}=-i_g, \tag{9}$$

$$\Delta i_L=\frac{V_{IN}}{2\cdot L_1}\cdot D(\varphi)\cdot T_{SW},\ \Delta v_C=\frac{v_{OUT}}{2\cdot R\cdot C_1}\cdot D(\varphi)\cdot T_{SW}, \tag{10}$$

where i_g - the output current, v_{OUT} - an instantaneous value of the output voltage, R - the load resistance, T_{SW} - the switching period.

On the other hand, in the design of the output inductance, it is required to study ripple shapes in detail. The reason is that a ripple in the output current depends only on the ripple across the capacitor. Therefore, it is possible to obtain the inductance value by using the equation with the coil flow, because the flow equals the integral of the inductor voltage. The change of the output current can be obtained by taking a square of the capacitor voltage ripple:

$$L_g\cdot\left(2\cdot\Delta i_g\right)=\Delta\Psi,\quad \Delta i_g=\frac{\Delta v_C}{8\cdot L_g}\cdot T_{SW}, \tag{11}$$

where $\Delta\Psi$ - changing of the coil flow.

The ripple factors for each passive element were considered for convenience. The maximum values of the currents in inductances are shown below:

$$I_{LMAX}=\frac{2\cdot P}{V_{IN}},\ I_{gMAX}=\frac{2\cdot P}{V_M}, \tag{12}$$

$$K_L=\frac{2\cdot\Delta i_L}{I_{LMAX}},\ K_C=\frac{2\cdot\Delta v_C}{V_M},\ K_g=\frac{2\cdot\Delta i_g}{I_{gMAX}}. \tag{13}$$

Thus, the ripples in the passive components depend on the instantaneous value of the output voltage. As a result, the previous statement leads to the dependences of the inductances and the capacitor on different parameters:

$$L_i=\frac{V_{IN}^2\cdot\left(\left|V_M\cdot\sin(\varphi)\right|-V_{IN}\right)}{2\cdot P\cdot K_L\cdot f_{SW}\cdot\left|V_M\cdot\sin(\varphi)\right|}, \tag{14}$$

$$C_1=\frac{2\cdot P\cdot\left(V_M\cdot\sin(\varphi)-V_{IN}\right)}{V_M^3\cdot K_C\cdot f_{SW}}, \tag{15}$$

$$L_g=\frac{V_M^2\cdot K_C}{16\cdot P\cdot K_g\cdot f}, \tag{16}$$

where f - the switching frequency.

III. Control System Description

The control system is used as an instrument to confirm the theory. It requires an open loop system in the boost case, but the ideal tuned control system based on the Model Predictive Control was chosen in the buck mode. Figure 5 shows the structure of the managing system based on MPC for the buck-boost inverter based on unfolding circuit.

The control system consists of four main blocks. The Maximum Power Point Tracker allows the determination of a suitable peak of the grid current.

One of the important issues is fast and correct synchronization with the network voltage in the inverter. The phase locked loop provides good phase managing of the grid

current in the network connection system. The necessary reference signal is generated by the previous two blocks. The MPC structure takes into account the instantaneous value of the reference signal. Certainly, the control system should obtain the measure values of the input voltage and the input current. Nevertheless, it is required to manage the grid current, the control system manages the output side by controlling the current in the input inductor. It is difficult to obtain an expression of the grid current with an explicit view because the high switching harmonic is non-linear. Thus, the main states in the system are measurements based on the other parameter.

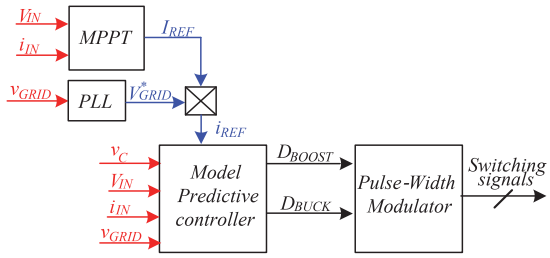

Fig. 5. The control system structure based on MPC for a buck-boost inverter based on unfolding circuit.

The input inductance current is calculated from the input current value. The output capacitor voltage should also be taken into account because this parameter is a state. Based on the states and the value of the input and grid voltages, the MPC is used to find a suitable duty cycle. The depth of the predictive is two. The cost function of the MPC is as follows:

$$J = \left|\left(i_L^{DTs} - i_{REF}\right) + \left(i_{REF} - i_L^{Ts}\right)\right| \cdot W_1 + \left|D_{prev} - D_{curr}\right| \cdot W_2 , \qquad (17)$$

where i_{REF} - the reference current, i_L^{Ts} and i_L^{DTs} - the values of the input inductor current during the switching period, W_1 and W_2 - weight factors, D_{prev}, D_{curr} - the duty cycle during the previous and the current periods respectively.

IV. Estimation of Optimal LCL-filter Values

A. Buck case

The LCL-filter is a non-split structure; thus, all the filter parameters depend on the resonance frequency. Therefore, the main points that were considered during the simulation are listed in Table I.

The main idea is to decrease the size of the overall filter by enlarging the capacitor. In the filter, inductances occupy the largest area because, as a rule, the converters have inductors with the ferrite coil. The size of the coils depends on the maximum current rating as well. Thus, the size of the filter depends on the energies in the passive components.

Figure 6 shows the dependence of the coil values on the value of the capacitor with the constant values of the output ripples, the power and the frequencies. Figure 6 (a) demonstrates that the input coil is increasing with a rise in the capacitor value because the resonance frequency does not change. On the other hand, the value of the grid coil is decreasing in the same way as the input inductor is growing. However, the ripple in the coils should be several percent, while the ripple in the input inductor can be up to 20%. Thus, the overall energy of the coils remains the same, it can even be reduced.

TABLE I. Parameters of the Buck Case.

Parameter	C_1 = 0.42 µF		C_1 = 0.84 µF		C_1 = 1.26 µF	
	LCL	*LC*	*LCL*	*LC*	*LCL*	*LC*
Current change of the grid inductor Δi_g, A	0.2	-	0.19	-	0.21	-
Current change of the input inductor Δi_L, A	1.55	1.39	1.3	1.25	1.25	1.21
Voltage change of the output capacitor Δv_C, V	8.5	8.27	4	3.72	2.9	2.4
Grid inductance L_g, µH	137.58		61.75		40	
Input inductance L_i, µH	665.48		741.31		763.06	
Frequency of switching f_{SW}, kHz	50					
Sample frequency, kHz	50					
Input voltage V_{IN}, V	450					
Grid Amplitude voltage V_M, V	320					
Grid Frequency voltage f_{SINE}, Hz	50					
Input Power P, W	1600					

The value of the input coil can be reduced and the output ripples still will be the same, but the resonance frequency will grow. Otherwise, higher values of the capacitor cause additional distortions across zero of the grid current.

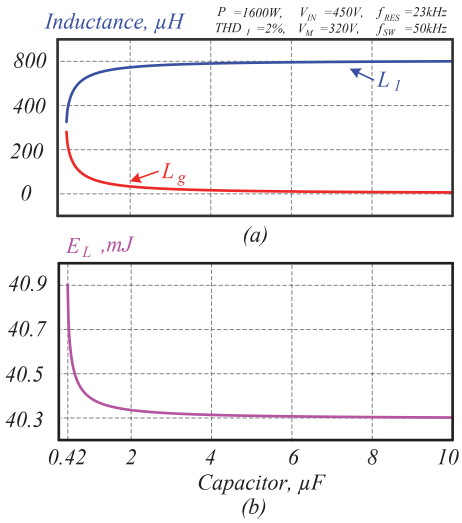

Fig. 6. Estimation of the passive components: dependences of the coils on the capacitor value (a), energy dependence on the capacitor value (b).

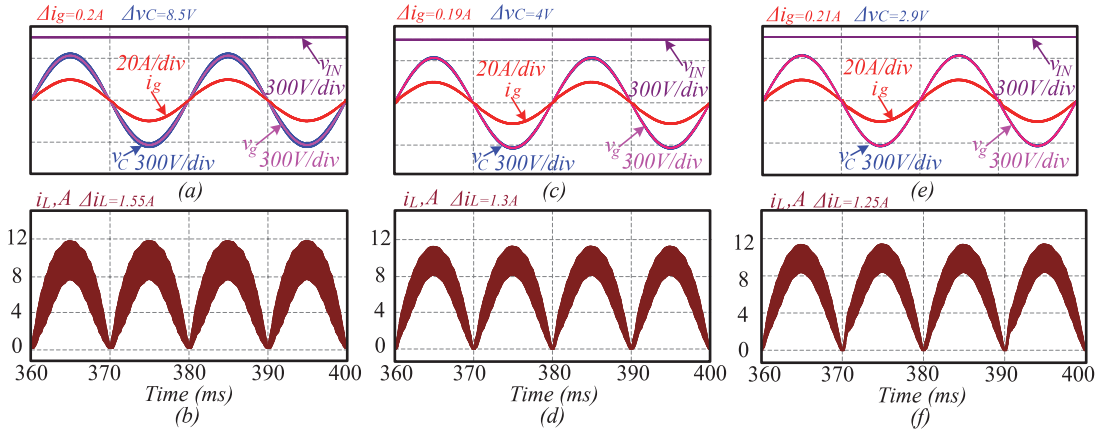

Fig. 7. Simulation results for the buck case: the output voltage and current within the grid voltage (a), the inductor current (b), the output pararmeters with a double capacitor (c), the inductor current with a double capacitor (d), the output parameters with a triple capacitor (e), the inductor current with a triple capacitor(f).

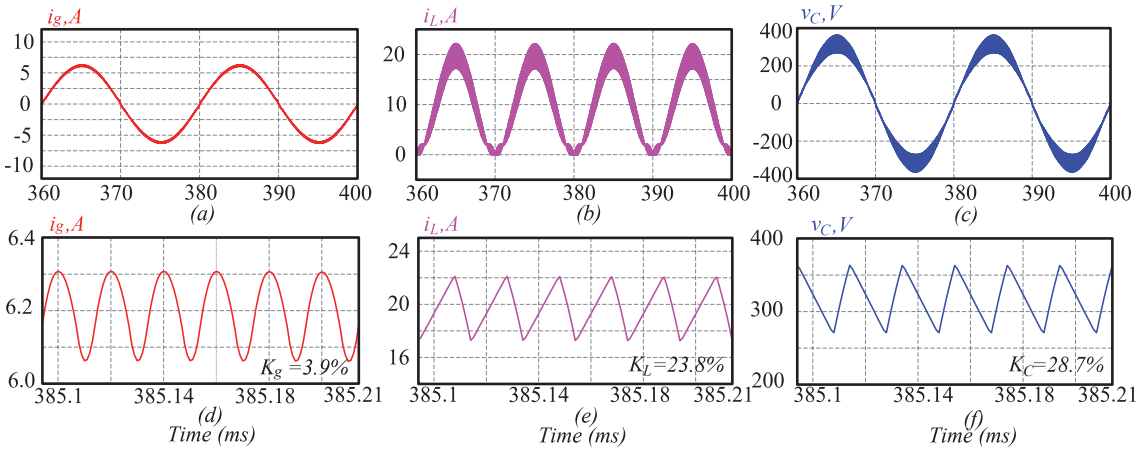

Fig. 8. Simulation results of the boost case: the ouput current (a), the main inductor current (b), the output voltage (c), the ripple in the ouput current (d), the ripple in the input inductor (e), the ripple in the output voltage (f).

Another interesting result is obtained by reducing the grid filter to the value less than 50 μH. The latter indicates that it is unnecessary to use the output coil. The reason is that the line of the grid has small inductance up to 40 μH. Thus, it is possible to replace a LCL-filter by a simple LC-filter. The comparisons of the voltage ripples of the currents between the LCL- and LC- filters are shown in Table I. Figures 7(a)-(f) demonstrate the simulation results for the buck mode with different output capacitors.

B. Boost case

In the boost case, the LCL-filter does not function for the whole structure. The ripples of the output current depend only on the pulsations of the output capacitor. Here a greater value of the capacitor according to Eq. (17) is required for the same pulsation of the output capacitor system. The main simulation parameters are shown in Table II. Figure 8 shows simulation results for the boost case.

TABLE II. PARAMETERS OF THE BOOST CASE.

Parameter	Value
Output current ripple factor K_g,%	4
Ouptut voltage ripple factor K_C,%	30
Input current ripple factor K_L,%	24
Output inductance L_g, μH	960
Input inductance L_i, μH	286.46
Output capacitor C_1, μF	0.9
Input voltage V_{IN}, V	100
Input power P, W	1000
Frequency of switching f_{SW}, kHz	50
Grid amplitude voltage V_M, V	320

V. Conclusions

The design of a LCL-filter for a buck-boost inverter based on unfolding circuit for both cases was studied. Our results showed that the LCL filter can be improved in size by increasing the capacitor in the buck mode. However, the resonance frequency should be in a range for stable conditions.

On the other hand, the system requires a larger capacitor to reduce the ripples of the output current in the boost mode. As result, a compromise between the capacitor of the buck and boost modes is required, while the LCL-filter structure must be kept. The LCL-filter can be replaced by a simple LC-filter at an increase of the capacitor at least three times. A large capacitor can cause imbalance in the stability of the system, but the MPC can provide a stable mode of operation.

ACKNOWLEDGMENT

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Performance Evaluation of the Universal Photovoltaic String Converter During the Operation in DC Microgrid Environment

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***Abstract* — Photovoltaic (PV) string converter for residential dc microgrids is presented. The concept of the converter is based on the interleaved buck-boost dc-dc converter with a wide input voltage range operation capability. The main control unit is a continuous control set model predictive control. The control system uses a simple droop control unit based on a proportional-integral regulator to ensure stability of the grid voltage. An experimental prototype based on a universal solar dc-dc/ac converter with the unfolding circuit was designed, featuring the MPPT voltage window from 150 V to 490 V and the nominal power of 3.6 kW. The efficiency benchmarking of a universal solar dc-dc/ac with connection to the dc microgrid is considered. Three real-world PV string profiles were considered during the experimental verification of the proposed approach. Based on the California Energy Commission (CEC) standard, the efficiency of the approach was well over 97 % in all selected case study scenarios.**

Keywords—droop control, buck, boost, microgrid.

I. INTRODUCTION

Demand for electrical energy is increasing each year. Modern power distribution systems require different types of power electronic converters. Although the ac grid is traditional, the DC Microgrid (DCMG) is attracting more attention since many generation systems and loads have a dc nature. Also, as the number of renewable energy systems is increasing, higher attention is attached to DCMG. Conventional grid requires many energy conversions between the source and the consumer, which leads to power losses. The DCMG is free from harmonics, reactive power, and synchronization issues. Moreover, the DCMG systems are more reliable, more efficient and require simple control strategies [1]. Fig. 1 shows the DCMG architecture addressed in [2] -[3]. Photovoltaic panels, fuel cells and battery energy storage systems provide only dc output, wherein large amounts of loads also consume dc power. A wind turbine may require an additional ac-dc or ac-ac converter for the correct nominal operation.

Dc-dc converters can be evaluated by several parameters, such as power density, cost, efficiency, reliability, and control complexity [4]. Also, dc-dc converters can be used for full and partial power conversions [5]. The full power conversion directly transfers electrical energy from a PV panel to the output while the partial power conversion is used to compensate the mismatch between the PV panels by processing only a fraction of the full power [6]. Usually, a deep boost ratio leads to lower efficiency because of high input current. Despite that, different converters have been reported to provide good efficiency performance even at high boost operation points [7]. All of the high step-up non-isolated converters are built on series boost cells, coupled inductors or switched capacitors. At the same time, all of them have significant drawbacks and have not found industrial application. For example, solutions based on a coupled inductor give flexibility to propose versatility of new solutions, but magnetic components are very large and require particular attention to the leakage inductance problem. Switched capacitor cells usually have problems with inrush current and require particular attention in the switching cell design.

Thus, if a high step-up feature is required, a transformer-based solution is a preferable choice [8]. Galvanically isolated converters based on the transformer are simpler to design and have high step-up ratio with lower losses. There are many derivatives of the isolated dc-dc converters with extended voltage regulation. An isolated impedance dc-dc converter is one of the solutions for distributed generation systems [9]. The quasi-Z-Source converter (qZS) [10]-[11] has small component stress and operates with continuous input current. The qZS based converter has more advantages than other impedance-sources [9]. The dc-dc Series-Resonant Converter (SRC) has many benefits over other solutions, one of which is zero-voltage switching [12]-[13]. As a result, SRC has minimum dynamic losses. All the considered dc-dc converters can be used in distributed generation systems, partial in PV applications.

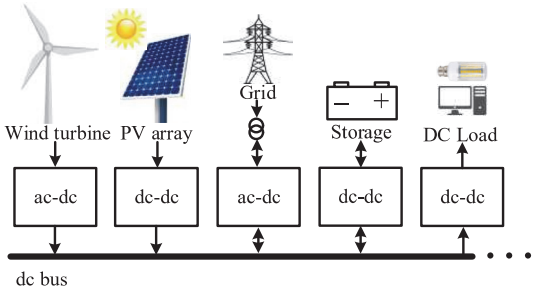


Fig. 1. DCMG architecture.

TABLE I. COMMERCIAL PHOTOVOLTAIC MODULES (UNDER STC).

Type of PV	Model and manufacturer	Open circuit voltage, V	Short circuit current, A	MPP voltage, V	MPP current, A	Number of cells/ output	Efficiency, %	Cost, EUR/W
1	CSM300-60 (Cell Solar Energy Co.)	39.82	9.84	32.55	9.23	60/300	18.44	0.141
2	CSM340-120 (Cell Solar Energy Co.)	41.34	10.16	34.12	9.83	60/345	20.45	0.141
3	JHM4/72BH445 (Yangzhou Jinghua New Energy Technology Co.)	49.2	11.36	41.1	10.83	144/445	20.14	0.207

At the same time, we want to underline that PV systems do not require high step-up solutions, but rather a wide input voltage range regulation that needs a different approach. It was demonstrated that a conventional non-inverting buck-boost converter is one of the most suitable solutions for solar application [14], [15]. This article discusses the PV string converter for DCMG applications. The approach is based on the interleaved buck-boost non-isolated dc-dc converters, which are the core parts of the universal solar dc-dc/ac converter earlier presented by a team in [16]. In this paper, the focus is on the efficiency benchmarking of the universal solar dc-dc/ac converter with an interleaved feature during the operation in the DCMG environment.

II. DESCRIPTION OF THE CONVERTER

A. Topology and Specifications

A generalized power circuit topology of the universal solar dc-dc/ac converter is presented in Fig. 2. The solar converter includes the unfolding circuit for ac grid connection, while the dc-dc mode requires no switching of the unfolding part. The universal converter [16] features interleaved control for decreasing the values of the inductances and reducing the power losses because two buck-boost cells divide into two times the input current in.

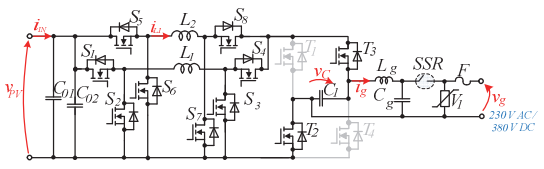


Fig. 2. Universal solar converter based on the unfolding circuit with two buck-boost cells.

It was confirmed in [17] that an interleaved feature with two buck-boost cells increases the efficiency with a higher input power. In contrast to the ac mode, the dc grid requires a fast relay. Solid State Relay (SSR) is a suitable element for fast disconnection from the dc grid side. The topology in Fig. 2 has an additional LC filter on the output for reducing the grid spikes under the grid disconnection. The output filter reduces the high switching ripples of the grid current. The fuse and the varistor are the elements for hardware protection. Besides, the software protection should also exist for detecting the overcurrent or the overvoltage conditions. When the fault appears, the system stops generation of control signals and allows current discharging in the inductances. For safety reasons, the inductances current should be lost not through the grid, thus the transistors S_2, S_3, S_6, S_7 help to do short circuits on the input inductances. The grid current is charging the output capacitor at the grid disconnecting.

Available photovoltaic modules should be taken into account. Table I presents the parameters of three commercial photovoltaic modules with Standard Test Conditions (STC). In the PV string, these modules are connected in series for increasing the input voltage and the power of the PV system. The maximum voltage of the PV system is typically limited by 1.5 kV, which means that the maximum number of series connected PV modules CSM300-60 and CSM340-120) is up to 36. Three profiles were considered in this paper. The MPP equals approximately 3.6 kW in all cases. Table II shows the parameters of the profiles. The idea is to demonstrate the performance of the converter under different input voltage and different input power variations. The first profile corresponds only to the buck mode with lower input current around 9 A and composes 12 solar panels of CSM300-60. The second profile has 11 CSM340-120 PV panels. The converter operates almost in the buck mode with MPP current 10A. Finally, the last profile is for the boost mode and for higher PV current (11 A). The MPP voltage is 329 V in the last case.

TABLE II. PV ARRAY PROFILES CONSIDERED DURING EXPERIMENTAL EVALUATIONS.

Profile	Type of PV	N of panels	V_{OC}, V	V_{MPP}, V	I_{SC}, A	I_{MPP}, A	P_{MPP}, kW
1	1	12	478	391	9.8	9.2	3.6
2	2	11	455	375	10.1	9.8	3.68
3	3	8	394	329	11.3	10.8	3.55

Fig. 3 shows the input power and the input voltage ranges of the converter. The nominal input power of the converter is 3.6 kW. The maximum output dc current is 10 A. The converter operates with an input voltage range from 100 V to 500 V. MPPT range is from 150 V to 490 V. The nominal voltage of the dc grid was considered as 380 V. Boost case is accompanied by a high level of the input current. Considering maximum input current of the solar converter is 15 A, the boost case has a negative slope according to the input power. For example, the maximum input power is around 2.2 kW at 150 V of the input voltage. The maximum power point depends on the panel temperature and on the solar irradiance. It is known that irradiance has impact on both PV parameters: voltage and current. Thus, the efficiency of the converter was measured under different solar irradiances. Fig. 4 shows the PV characteristics of the chosen profiles. The ideal operating conditions without shading and high ambient temperatures were considered for the benchmarking. Profile 2 is demonstrated at

different solar irradiance levels. Fig. 4 shows that the solar irradiance shifts the MPP down, while the open circuit voltage drops but not significantly. The same approach was applied for profile 1 and profile 3.

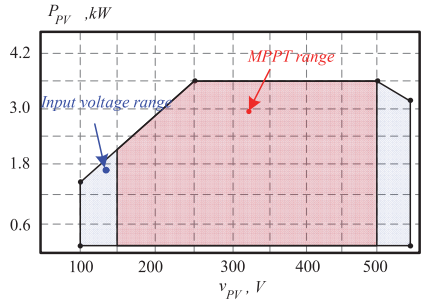


Fig. 3. Converter input voltage range along with MPPT range.

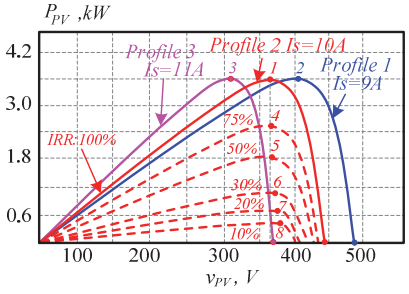


Fig. 4. Characteristics of different PV profiles at different solar irradiance levels.

B. Control System Description

The main regulator in the control system is the Model Predictive Control. In [18], the details of the MPC for a twisted buck-boost inverter based on the unfolding circuit are described. The main statements about the control system are summarized below. Fig. 5 explains the structure of the control system for the dc-dc buck-boost solar converter. Model predictive control is of continuous control set type because Pulse Width Modulation (PWM) is used. The control system contains the Maximum Power Point Tracking (MPPT) and droop control blocks for keeping stable grid voltage. The topology in Fig. 2 can be considered as a non-minimum phase system. Therefore, the traditional cost function is not suitable. The cost function based on the internal inductor current is more appropriate for the grid connected system:

$$J = \min\left\{\sum_{j=1}^{2}\left(\begin{matrix}\left|i'_{L1}[k+j]-i_{L1REF}[k+j]\right|\cdot W_{j1}+\\ +\left|i_{L1}[k+j]-i_{L1REF}[k+j]\right|\cdot W_{j2}\end{matrix}\right)\right\}, \quad (1)$$

where $i'_{L1}[k+j]$: $i'_{L1}[k+1]$, $i'_{L1}[k+2]$, $i_{L1}[k+j]$: $i_{L1}[k+1]$, $i_{L1}[k+2]$ are predictive values of the inductor current during the next PWM periods, $i_{L1REF}[k+j]$: $i_{L1REF}[k+1]$, $i_{L1REF}[k+2]$ - reference values of the inductor current. W_{11}, W_{21}, W_{12}, W_{22} are weight factors.

The MPC predicts the two next samples of the system, which means using two horizons. However, the second horizon was cut and used with approximation for faster computation actions. The overall number of cycles iterations is 10. The amount of the duty cycle step is also reduced due to the limitation of the microcontroller unit. This approach increases the reliability and allows a decrease in the time of computations. The system predicts the next duty cycle value across the previous value, considering a range of 10%:

$$D[k+1] = D[k] \pm 0.1, \quad (2)$$

where $D[k]$ is the previous value of the duty cycle.

The heuristic methodology allowed to find the most optimal weight factors W_{11}, W_{12}, W_{21}, W_{22}. The second horizon is considered with a higher priority, the ratio between the second horizon weight factors and the first one is 2:1.

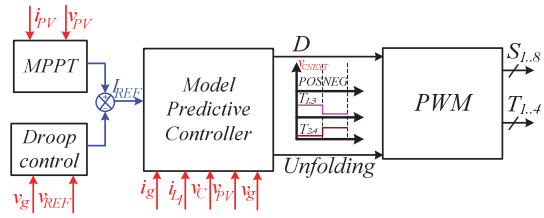


Fig. 5. Structure of the control system based on MPC.

Finally, the grid current cannot change sharply in the nominal mode. The next values of the grid current are the same during several PWM periods, because the inverter has an additional L-filter that decreases the high-frequency ripple and prevents a rapid increase in the grid current:

$$i_g[k+3] = i_g[k+2] = i_g[k+1] = i_g[k], \quad (3)$$

where $i_g[k+3]$, $i_g[k+2]$, $i_g[k+1]$ are predictive values of the grid current for the next PWM periods.

C. Droop Control and Power Clipping/Curtailment

The droop control is a basic technique for a stable dc grid voltage. Despite the lower efficiency of MPPT, the droop control allows considering resistance of the grid line and eliminating the voltage change of the grid [19]. Fig. 6 shows the principle of the grid behavior under an injection current process. *Rgd* is a resistance of the grid line. This resistor can be calculated taking into account the slope of the voltage change.

Several interesting methods for the droop control are described in [20]-[22]. Droop control can be implemented with MPC, integral methods and in other cases. Fig. 7 describes a simple Proportional-Integral (PI) regulator for the droop control. The main strategy is to decrease the reference current at the grid voltage hike. Reference voltage for the grid is 380 V. It is worth emphasizing that the maximum power of PV is not used with the droop control, but the stability of the grid and the system is increasing.

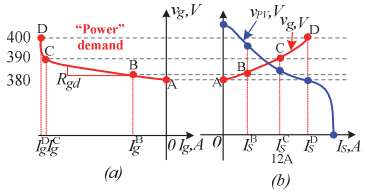


Fig. 6. Grid voltage changing under current injection (a), PV characteristics depend on the droop action (b).

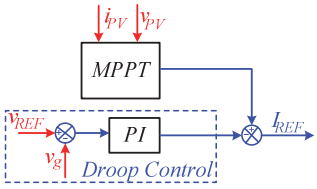


Fig. 7. Structure of generation of the grid current reference within the droop control and MPPT.

D. Selected Design Guidelines

In the design of the PV string converter, it is required to calculate the filter, choose the semiconductors, sensors, and protection systems. The protection system was explained above. The number of sensors can be counted easily from the control system structure. The proposed approach requires 6 sensors: 3 for currents and 3 for voltages. The converter has 12 transistors that should be chosen according to the voltage stress across them. In an ideal case, the maximum stress on the semiconductor corresponds to the input voltage; however, factors such as design of board, inductances and dead time configuration create voltage spikes at the moment of switching. Thus, it should be considered during transistor choice. The passive components of the buck mode can be obtained in the same way as shown in [23]. Design of passive elements requires a steady state analysis for an open loop system. Equations (4)-(5) help to calculate the values of the passive components in the boost mode:

$$C_1 = \frac{P_{PV} \cdot \left(v_g - v_{PV}\right)}{v_g^3 \cdot K_C \cdot f_{SW}}, \tag{4}$$

$$L_1 = L_2 = \frac{2 \cdot v_{PV}^2 \cdot \left(v_g - v_{PV}\right)}{P_{PV} \cdot K_L \cdot f_{SW} \cdot v_g}, \; L_g = \frac{v_g^2 \cdot K_C}{4 \cdot P_{PV} \cdot K_g \cdot f_{SW}}, \tag{5}$$

where f_{SW} - switching frequency, K_C, K_L, K_g are ripple factors for every passive component.

III. Performance Evaluation

A. Converter specifications

This section discusses the experimental verification of the universal photovoltaic string converter during the operation in the dc microgrid environment. The experimental prototype is shown in Fig. 8. Its control board contains 3 current sensors and 5 voltage sensors. The model of the microcontroller used in the project is TMS320f28379d from Texas Instruments. It contains 12 complementary PWM blocks and 10 differential ADC channels. All high-frequency switching transistors are SiC MOSFETs. S_2, S_3, S_6, S_7 are IMZ120R030M1H 1200 V SiC transistors with R_{DSON} of 30 mOhm. The transistors S_1, S_4, S_5, S_8 are C3M0021120K SiC 1200 V with 21 mOhm of R_{DSON} under normal conditions. The unfolding part contains superfet transistors FCH060N80 800 V with 60 mOhm of R_{DSON}. Table III lists the specifications of the developed PV string converter. The switching frequency is 62 kHz.

TABLE III. Main Specifications of the PV String Converter.

Parameters	Value
Input voltage range of converter, V	100 – 500
MPPT voltage range, V	150 – 490
Maximum MPP current, A	12
Rated DC input power, kW	3.6
Nominal output DC voltage, V	380
Output DC voltage range, V	380 – 390
Maximum output DC current, A	10
Switching frequency, kHz	62
Max. efficiency, %	98.8
CEC efficiency, %	98.34
Output DC voltage during fault, shut down or disconnected from DC-bus, V	380
Input inductances, mH	1.6
Input capacitance, mF	4
Output capacitance, uF	1
Grid inductances, mH	0.33
Grid capacitance, uF	1

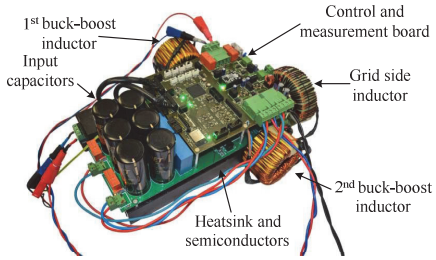


Fig. 8. Experimental prototype of a universal photovoltaic string converter.

B. Peak and CEC efficiency, efficiency map at different input/output voltages

Fig. 9 shows experimental results for the buck-boost universal converter with different profiles. Fig. 9*a* shows the MPPT transient process for the second profile. Universal solar converter requires pre-charging of the output capacitor to remove current spikes during the relay switching (Fig. 9*d*). The second set of the pictures in Fig. 9*b* and 9*e* demonstrates high switching ripples of the PV side, the grid side, the input inductor current and the output capacitor for profile 3 (boost profile). In the boost case, the input inductor ripples reach higher values than in the buck case. The pulsations of the grid current were 0.15 A, when the ripple of the input current was 0.07 A, which is acceptable for PV applications. The first profile is shown in Fig. 9*c*, 9*f*. The grid suppressor capacitor about 1 uF is sufficient to provide a soft transient process.

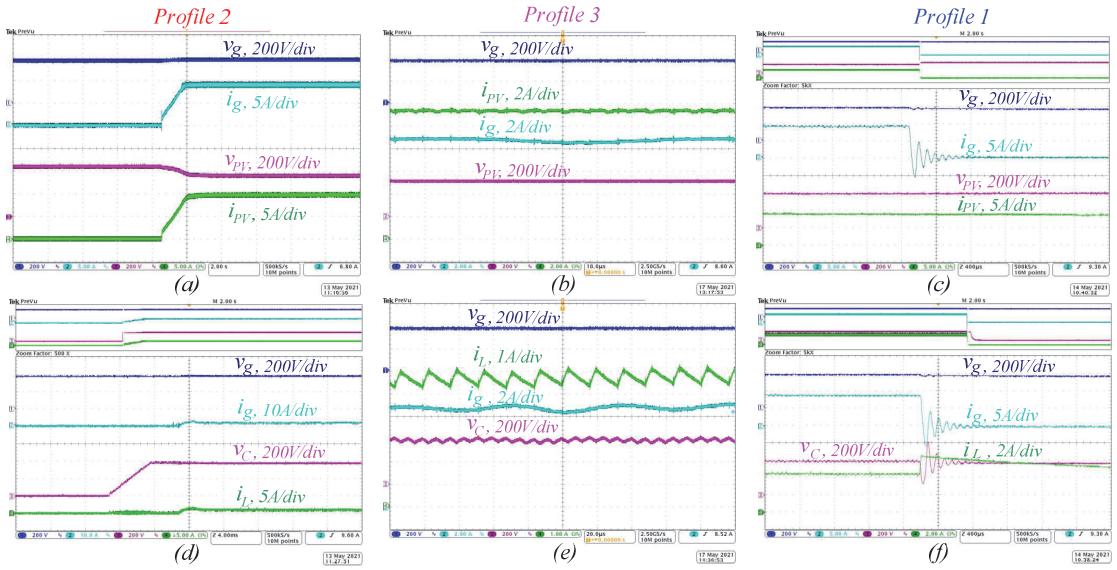


Fig. 9. Experimental results of a universal solar converter in the dc-dc mode, PV and grid voltage and current: during MPPT operation for profile 2 (a), high ripples in profile 3 (b), switch-off waveforms in profile 1 (c). The waveforms of the input inductor current and output capacitor voltage along with the grid side: during MPPT operation for profile 2 (d), high switching pulsations with profile 3 (e), during stop of the system with profile 2 (f).

As it was discussed earlier, some spike is appearing during the disconnecting process or during stop of the system. The input inductances are shorted circuit for current loss through a transistor, hence it is possible to see some current increasing (Fig. 9*f* green line). The converter was working stable under each profile. Fig. 9 shows a waveform at the full profile input power.

The efficiency estimation is the main objective to show the operation of the converter with different profiles. The precision power analyzer Yokogawa WT1800 was used to measure the efficiency. Fig. 10 shows the efficiency curves based on the PV power. The maximum measured efficiency was 98.8 % at the PV voltage of 390 V. CEC efficiency was used for the performance estimation. The most used profile corresponded to a higher buck case (profile 1 with CEC efficiency 98.34 %). Two profiles have lower efficiency under low input power. In small buck and in small boost profiles, CEC efficiencies are slightly different (97.64 % with profile 2 and 97.14 % with profile 3). Though those unfolding transistors are present, their contribution is not significant in terms of the power losses. Unfolding switches dissipate only static losses. Hence, it is possible to calculate an efficiency without the unfolding circuit because it is required only to know R_{DSON} of the transistor and an average value of the grid current. Fig. 10*b* shows the results of the efficiency calculation without the unfolding circuit. The maximum efficiency value is 99.02 % at the same point 390 V of the input voltage. The maximum CEC efficiency was increased by 0.14 % and equaled 98.51 %. The efficiency in the low power is approximately the same in all cases, the difference is seen under higher PV power points (>2 kW).

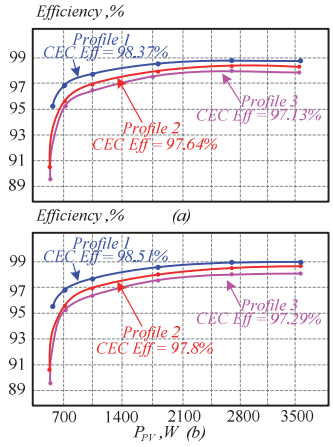
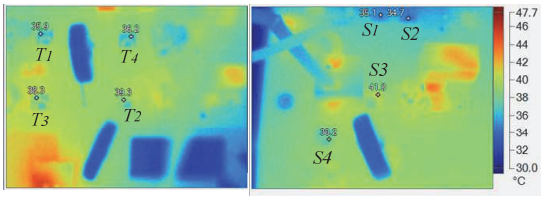


Fig. 10. Experimental efficiency of the prototype under different PV profiles and with different solar irradiations: with unfolding circuit (a), without unfolding part (b).

Despite the declared nominal power, the maximum temperature of the transistors reaches 50 ºC. Fig. 11 presents the temperatures of the transistors. The unfolding part (Fig. 11*a*) has no switching and contains only static losses. The maximum temperature of the unfolding transistor was around 40 ºC. The buck-boost cell operated as a hard switching part. Therefore, the temperature of the buck-boost transistors did not exceed 50 ºC.



(a) (b)

Fig. 11. Thermal pictures of the solar converter under a maximum power point operation: unfolding transistors (a), buck-boost cell switches (b).

IV. Conclusions and Future Work

This paper presented the performance evaluation of a universal photovoltaic string converter during the operation in the dc microgrid environment. A pre-industrial prototype is discussed within the control and the measurement systems. Such type of a converter requires different types of protection: software and hardware; the concept of protection was shown along with the switch-off process. The control system includes MPC as the main regulator. The MPC provides stable levels of the grid current due to the second horizon and a special cost function. In addition, the control system has a droop control block for the stable level of the grid voltage, as it can be in real system with many converters connected to the same grid. The droop control consists of a simple PI regulator, which is enough for the current application. Three real PV string profiles were chosen for an experimental verification. A pre-industrial converter was implemented based on a universal solar dc-dc/ac converter with the unfolding circuit that can operate under 3.6 kW of the input power. The temperature of the switches did not exceed 50 ºC. The efficiency was estimated for the considered profiles with the CEC standard. The maximum obtained CEC efficiency is 98.37 % at a higher buck ratio, while the efficiency without the unfolding circuit loss is 98.51 %. However, the efficiency can still be improved, taking into account the variable switching frequency approach.

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