TALLINN UNIVERSITY OF TECHNOLOGY
School of Information Technologies

Anna Navolotskaia 214598IVEM

Circuit-level and Device-level Measurements of the Threshold Voltage Instability in p-GaN HEMTs

Master's thesis

Supervisor: Yannick Le Moullec
PhD
Co-Supervisor: Tian-Li Wu
PhD

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Infotehnoloogia teaduskond

Anna Navolotskaia 214598IVEM

P-GAN HEMT-TÜÜPI TRANSISTORIDE LÄVIPINGE MÕÕTMINE VOOLURINGIS JA ERALDISEISVA SEADISENA

Magistritöö

Juhendaja: Yannick Le Moullec
PhD
Kaasjuhendaja: Tian-Li Wu
PhD

Tallinn 2024

Author’s declaration of originality

I hereby certify that I am the sole author of this thesis. All the used materials, references to the literature and the work of others have been referred to. This thesis has not been presented for examination anywhere else.

Author: Anna Navolotskaia

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Abstract

Gallium nitride high electron mobility transistors (GaN HEMTs) are increasingly popular in the semiconductor market; GaN HEMTs offer the widest energy gap, highest critical field, and highest saturation velocity, making them well-suited for power systems and communication systems. However, the reliability of these new devices needs to be established, as they face challenges such as on-resistance and gate material degradations, gate stress and bias temperature instability, and threshold voltage shift.

This master's thesis is related to ongoing research conducted by the International College of Semiconductors Technology of National Yang Ming Chiao Tung University. A comprehensive review of GaN material properties, GaN HEMTs, and their reliability issues, particularly threshold voltage instability, was conducted. The state-of-the-art threshold voltage methods and techniques were reviewed, and an existing circuit-level board was analysed. The experimental work involved obtaining Id-Vg curves of the device under 12, 24 and 32 V stress voltages with stress pulse duration of 100 μs, 1 ms, 10 ms, 100 ms, 1s and 10 s. Three threshold voltage extraction methods (constant current, linear extrapolation, transconductance change) were applied to the data; the constant current method proved to be the most consistent (i.e. increasing threshold voltage values with increasing stress time, and threshold voltage closest to the expected typical value (deviation between +0.130 V and +0.547 V)), and time-effective. The device-level threshold voltage measurements were compared with circuit-level measurements, showing valid but less accurate results. The advantages and limitations of device-level measurements using a probe station were discussed and a procedure for probe-station measurements was proposed to address these practical limitations.

Overall, the objectives of this master's thesis were successfully achieved, providing valuable insights into threshold voltage measurements for GaN HEMTs. The results obtained serve as a foundation for future research in this field.

This thesis is written in English and is 64 pages long, including 6 chapters, 28 figures and 5 tables.

Annotatsioon

P-GaN HEMT-de Lävipinge Ebastabiilsuse Mõõtmised Vooluringi Tasemal ja Seadme Tasemal

Galliumnitriidi-põhised suure elektronide liikuvusega transistorid (GaN HEMTid) on pooljuhtide turul üha suuremat populaarsust saavutamas; GaN HEMTide eeliseks on nende lai energiavahe, kõrgeim kriitiline välja ja kõrgeim küllastunud kiirus, mistõttu on need eriti sobivad elektri- ja sidesüsteemide jaoks. Vaatamata oma muljetavaldavale jõudlusele on GaN HEMT-ide töökindlus endiselt kriitiline murekoht, kuna need on vastuvõtlikud sisselülitustakistuste ja paismaterjalide halvenemisele, paispingele ja eelpingetemperatuuri ebastabiilsusele, mis põhjustab lävepinge ebastabiilsust.

See magistritöö on seotud Rahvusliku Yang Ming Chiao Tung Ülikooli Rahvusvahelise Pooljuhtide Tehnoloogia Kolledži poolt läbiviidava pideva uurimistööga. Viidi läbi põhjalik ülevaade GaN materjalide omadustest, GaN HEMT-idest ja nende usaldusväärsuse küsimustest, eriti lävendi pinge ebastabiilsuse kohta. Arvustati lävendi pinge mõõtmise meetodeid ja tehnikaid, ning analüüsiti olemasolevat trükkplaati. Katsetöö hõlmas seadme Id-Vg kõverate leidmist pingetel 12V, 24V ja 32 V, impulsi kestusega 100 μs, 1 ms, 10 ms, 100 ms, 1 s ja 10 s. Andmetele rakendati kolme lävipinge eraldamise meetodit (pidevvool, lineaarne ekstrapolatsioon, transkonduktiivsuse muutus); pidevvoolu meetod osutus kõige järjekindlamaks (s.o. suurenevad lävipinge väärtused koos pingeaja suurenemisega ja lävipinge, mis on lähim eeldatavale tüüpilisele väärtusele (hälve vahemikus +0,130 V ja +0,547 V)) ja ajaliselt efektiivseim. Seadme-tasandi lävipinge mõõtmisi võrreldi vooluringi-tasandi mõõtmistega, mis näitas valiidseid, kuid väiksema täpsusega tulemusi. Arutati sondi abil seadme tasandil mõõtmise eeliseid ja piiranguid ning nende praktiliste piirangute käsitlemiseks pakuti välja sondiga mõõtmise protseduur.

Üldiselt saavutati selle magistritöö eesmärgid edukalt, pakkudes väärtuslikku teavet GaN HEMT-de lävipinge mõõtmise kohta. Saadud tulemused on aluseks antud valdkonna edasisele uurimistööle.

Lõputöö on kirjutatud Inglise keeles ning sisaldab teksti 64 leheküljel, 6 peatükki, 28 joonist, 5 tabelit.

List of abbreviations and terms

2DEG	Two-Dimensional Electron Gas
AlGaN	Aluminium Gallium Nitride
BTI	Bias-Temperature Instability
CC	Constant Current
DUT	Device Under Test
Dia	Diamond
EPO	European Patent Office
GaN	Gallium Nitride
GIT	Gate-Injection Transistor
HD-GIT	Hybrid-Drain Gate-Injection Transistor
HEMT	High Electron Mobility Transistor
ICST	International College of Semiconductors Technology
JEDEC	Joint Electron Device Engineering Council
LE	Linear Extrapolation
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NYCU	National Yang Ming Chiao Tung University
SD	Second Derivative
Si	Silicon
SiC	Silicon Carbide
USPTO	United States Patent and Trademark Office

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1 Introduction

Gallium nitride high electron mobility transistors (GaN HEMTs) – of which a schematised diagram is represented in Figure 1 – are gaining in popularity. As reported by Spherical Insights & Consulting, the global high electron mobility transistor market size is to grow from 7.51 billion USD to 16.82 billion USD by 2032 [1]. This is due to the GaN material's properties including the widest energy gap, largest critical field, and highest saturation velocity when compared to other currently commercially available semiconductors [2]. These properties make GaN-based power devices good candidates for high-efficiency and high-switching applications, such as in power systems and communication systems. Yet, this new technology needs to prove its reliability to replace older semiconductor devices. Reliability issues in HEMTs include on-resistance degradation and instability, gate material degradation, gate stress and bias temperature instability, and threshold voltage shift. Threshold voltage is one of the important reliability characteristics; under several conditions including temperature influence, gate stress, or OFF-state drain stress, the threshold voltage may shift causing limited control of the transistor operation as device starts to conduct with increased/decreased gate voltage provided.

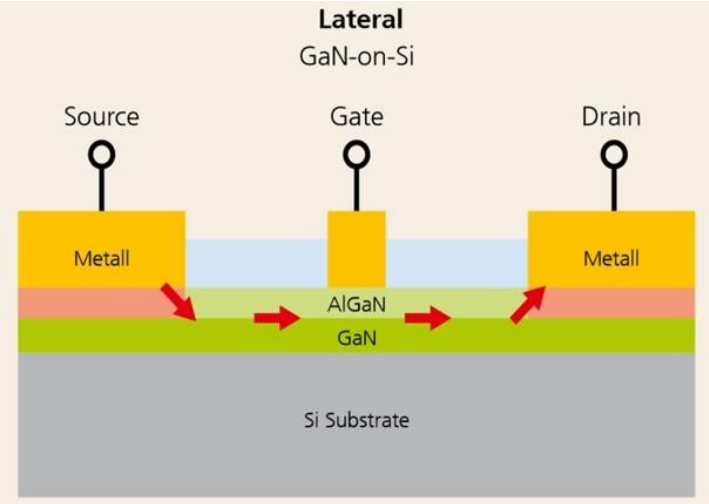


Figure 1. Schematised diagram of a lateral GaN HEMT device with red arrows showing the current path [3].

A common approach to analyse the threshold voltage shift is to use power device analysers (curve tracers) with a probe station (example of a typical setup shown in Figure 2 [4]); however, this approach has some limitations including high cost of the probe station and of the curve tracers themselves, as well as the need for using extra modules for different devices, parameter measured, or measurement conditions (high current, voltage, temperature, etc). Moreover, the measurement process is time and power-consuming and several conditions may be hard to achieve; one of these conditions is a short stress pulse. Curve tracers typically can go down to 100-500 μs [5], [6], while even shorter signals are required for testing of the devices for high-frequency applications.

Figure 2. A probe measurement setup including Keithley 4200 SCS semiconductor parameter analyzer and a Janis ST-500 cryogenic probe station [4].

1.1 Problem Statement

Custom circuits have been developed to overcome the above-listed limitations, providing solutions requiring less power and time needed to perform the measurement, and at the same time allowing to reach shorter stress pulse duration. In a work previously conducted by the ICST at NYCU, a threshold voltage measurement circuit allowing decreased OFF-state stress time duration was proposed ([7]). However, an extensive analysis of the threshold voltage shift of the device under test is still missing. Further investigation is required, and results obtained using the probe station measurement should be compared

with the results from the custom circuit. This analysis can validate the past results and/or lead to further suggestions for improving the circuit. At the same time, this work aims to define the advantages and disadvantages of using a probe station for device characterisation and explore threshold voltage extraction techniques to define the optimal one. Thus, the following issues need to be investigated throughout this thesis:

- Explore the state-of-the-art methods to measure threshold voltage as well as explore threshold voltage extraction techniques and choose the one most suitable for the experiment at hand.
- Carry out measurements of the same device characterised in the previously published work ([7]) using a curve tracer and a probe station. Compare the results obtained from the probe station with the ones from the custom circuit.
- Define advantages and limitations of using the probe station and curve tracer compared to the circuit-level measurement and propose a procedure for the threshold voltage extraction of the packaged device.

1.2 Workflow

In order to investigate the above-listed issues, i.e. to understand the different threshold voltage (Vth) instability from the two different set-ups, further analysing the degradation mechanisms, and proposing improvements to the measuring procedure or custom circuit to enhance the current result, the workflow below has been followed:

1. Analyse the background theory and state of the art of GaN HEMTs properties and reliability issues.
2. Conduct research on GaN HEMTs' threshold voltage instability nature after applying a drain OFF-state stress.
3. Explore ways to obtain threshold voltage of a GaN device.
4. Define the limitations of the existing method.

5. Analyse the previously published custom circuit board performance.
6. Obtain the Vth values under various OFF-state stress conditions with the help of a probe station and a curve tracer.
7. Analyse the obtained results and compare them with the results from the custom circuit.
8. Propose solutions for improvement of a measurement procedure.

1.3 Thesis organisation

The rest of this thesis is organised as follows.

Chapter 2 presents the theoretical background of the GaN HEMT technology, focusing on the material properties of gallium nitride, presenting high electron mobility technology including its benefits and limitations, presenting reliability issues, and defining threshold voltage instability.

Chapter 3 gives an overview of threshold voltage measurement, including the procedure for finding the threshold voltage with a probe station and the state of the art of existing threshold voltage measurement circuits, and finally presenting the previously published measurement circuit to be analysed in this work.

The practical part of this work starts with Chapter 4 where the threshold voltage measurement setup and results are represented, starting with the measurement procedure and the probe station description, illustrating the obtained measurement results.

Chapter 5 presents and discuss the comparison between the circuit-level and device-level results, advantages and limitations of Vth measurement using a probe station, and the proposed procedure.

Chapter 6 concludes the thesis by summarizing the conducted work and achieved results and by providing some suggestions for future work.

2 Background of GaN HEMT Technology

Having reached the theoretical limits of silicon semiconductor power devices effectiveness has provoked an interest in alternative materials. Such limitations as ones connected to operational temperature and frequency, as well as breakdown voltage, do not satisfy the requirements for power devices. Wide bandgap semiconductor devices outperform the traditional Si devices, offering greater performance with reduced dimensions and being able to work in harsher environments [8]. Wide bandgap materials offer large band gap and superior thermal properties. Over the past two decades, wide bandgap materials such as silicon carbide (SiC), gallium nitride (GaN) and diamond (Dia) have become widely available in the commercial market. A timeline of key milestones in SiC and GaN transistors technology development is illustrated in Figure 3 [9]. In particular, GaN presents several advantages, i.e. faster switching, smaller size, increased efficiency and reduced costs, allowing it to be used for lasers and RF applications (while for high-power applications it is still in the early stage) [10]. As introduced earlier, this master thesis focuses on the threshold voltage instability of GaN HEMTs; thus, the following section cover the main properties of GaN, operating principles of transistors built with GaN, reliability in GaN HEMTs, and finally the specific issue of threshold voltage instability.

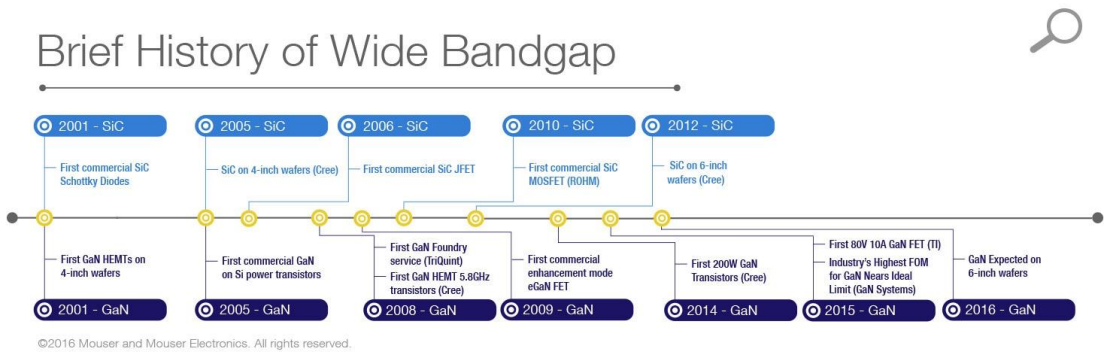


Figure 3. Milestones in SiC and GaN transistors technology development [9].

2.1 GaN properties

The properties of GaN make it an efficient and versatile semiconductor for high-power, high-frequency, and high-temperature applications. This section briefly introduces the physical properties of this material. The paragraph below is focused on GaN material properties and is mostly based on [11].

The first important property of GaN is that it has three times higher bandgap E_g $(unit: electronvolt\ (eV))$ compared to silicon, which makes the amount of energy required to pull the electron away from the atom in the crystal to be three times higher. This property allows GaN devices to operate at higher temperatures (e.g. aluminium gallium nitride/gallium nitride (AlGaN/GaN) high-electron mobility transistors up to 500 ˚C [12]), and to tolerate higher electron field before breakdown.

The second important property of GaN is its high critical breakdown electric field E_{crit} $(unit: megavolt\ per\ centimeter\ (\frac{MV}{cm}))$ which is ten times higher than for silicon. This comes from the strong chemical bond causing the wider band gap. E_{crit} determines how close the terminals of the device can be brought together before they arch. A smaller distance between the source and drain gates allows a faster switching rate. Additionally, ten times the amount of electrons can be packed between the terminals, theoretically allowing the device to be a thousand times smaller and still having the same on-resistance and threshold voltage.

A third important property of GaN is its 10% higher electron mobility μ_n $(unit: square\ centimeters\ over\ volts\ seconds\ (\frac{cm^2}{V \cdot s})$ which determines how sticky the electrons are. This is inversely proportional to resistivity, making GaN suitable candidate material for power transistors. A comparison chart of GaN vs. Si and SiC properties is shown in Figure 4 [13].

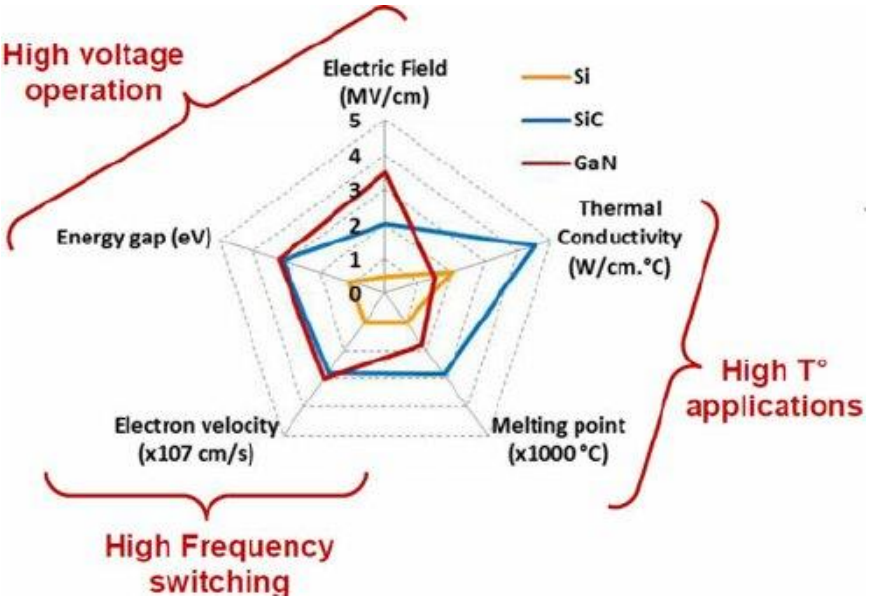


Figure 4. Gallium nitride (GaN), silicon (Si) and silicon carbide (Sic) properties chart [13]. GaN has higher critical electric field but lower thermal conductivity and melting point when compared to SiC, and has superior properties to Si in every shown characteristic except for thermal conductivity.

2.2 GaN high electron mobility transistors

GaN is a natural piezoelectric. When a AlGaN layer is added on top of GaN, significant strain over a very short distance can be created. This results in an electric field that attracts a large amount of electrons to the surface, creating a highly conductive two-dimensional electron gas (2DEG).

GaN high electron mobility transistors are based on this 2DEG. The introduction of the AlGaN layer creates a heterojunction structure, which enhances electron confinement and mobility within the channel, contributing to the transistor's high-speed and high-power capabilities. The typical lateral structure of GaN HEMT in comparison with the vertical structure of Si/SiC metal-oxide-semiconductor field-effect transistor is represented in Figure 5 [14].

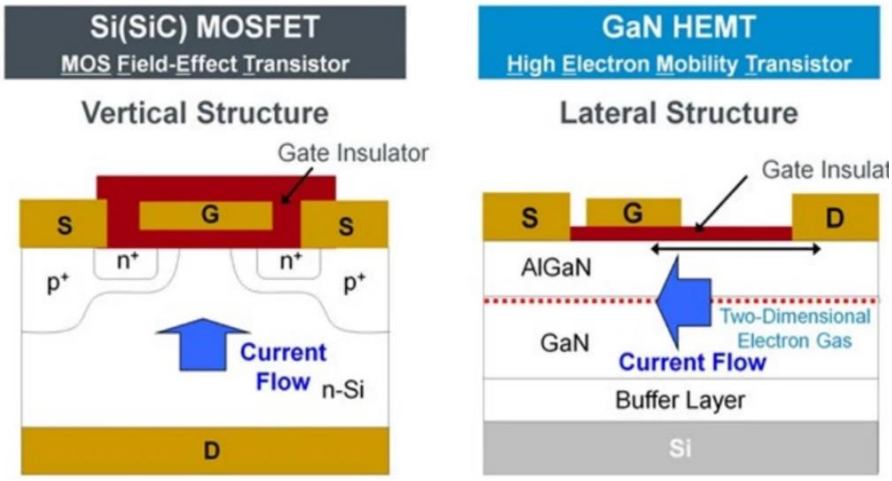


Figure 5. Structure comparison for Si/SiC and GaN HEMT devices [14]. The main carriers in MOSFETs are electrons or holes conducting in the presence of a metal gate, while HEMTs use a heterostructure and the high electron mobility in 2DEG created at the AlGaN/GaN junction.

GaN HEMTs are typically in a normally-ON state due to the spontaneous polarization at the bandgap interface in the AlGaN/GaN heterojunction. These transistors are also called depletion GaN HEMTs. However, they can be transformed into a normally-OFF state by incorporating several technologies such as i) a cascode device, ii) a gate-injection transistor (GIT) with a Schottky contact for the gate, or iii) an hybrid-drain gate-injection transistor (HD-GIT) with an ohmic contact for the gate [15]; these three options are briefly discussed in what follows.

A cascode structure is the straightforward way to achieve the normally-OFF behaviour; it lays in introducing the additional Silicon metal–oxide–semiconductor field-effect transistor (MOSFET) controls for the turn-on and turn-off of depletion GaN HEMT (see Figure 6(a) [16]).

Another approach to design a normally-OFF device resulted in the GIT, where an additional p-GaN or p-AlGaN layer on the gate increases the potential at the 2DEG channel (see Figure 6(b)). The injection of holes from the doped layer to the channel lifts the electron density, allowing modulation of the drain current with gate to source voltage, finely tuning the device output current based on the voltage applied to the gate terminal. The GIT is also referred to as p-GaN gate HEMT.

Finally, a HD-GIT transistor has a parallel connection between p-GaN layer and a metallic contact and is controlled with the gate current instead of voltage. An additional p-GaN region is introduced to release electrons trapped during switching operation of the device (see Figure 6(c)). This technology contributes to stabilising dynamic on-resistance and preventing the phenomena of current collapse that occurs with the increase of the on-resistance.

These two latest technologies (GIT and HD-GIT) are now the most widely available in the market with different processing approaches described in [10]. The device characterised in this work (Efficient Power Conversion Corporation EPC2014C) is a p-GaN gate HEMT also called enhancement mode (e-mode) GaN by the manufacturer.

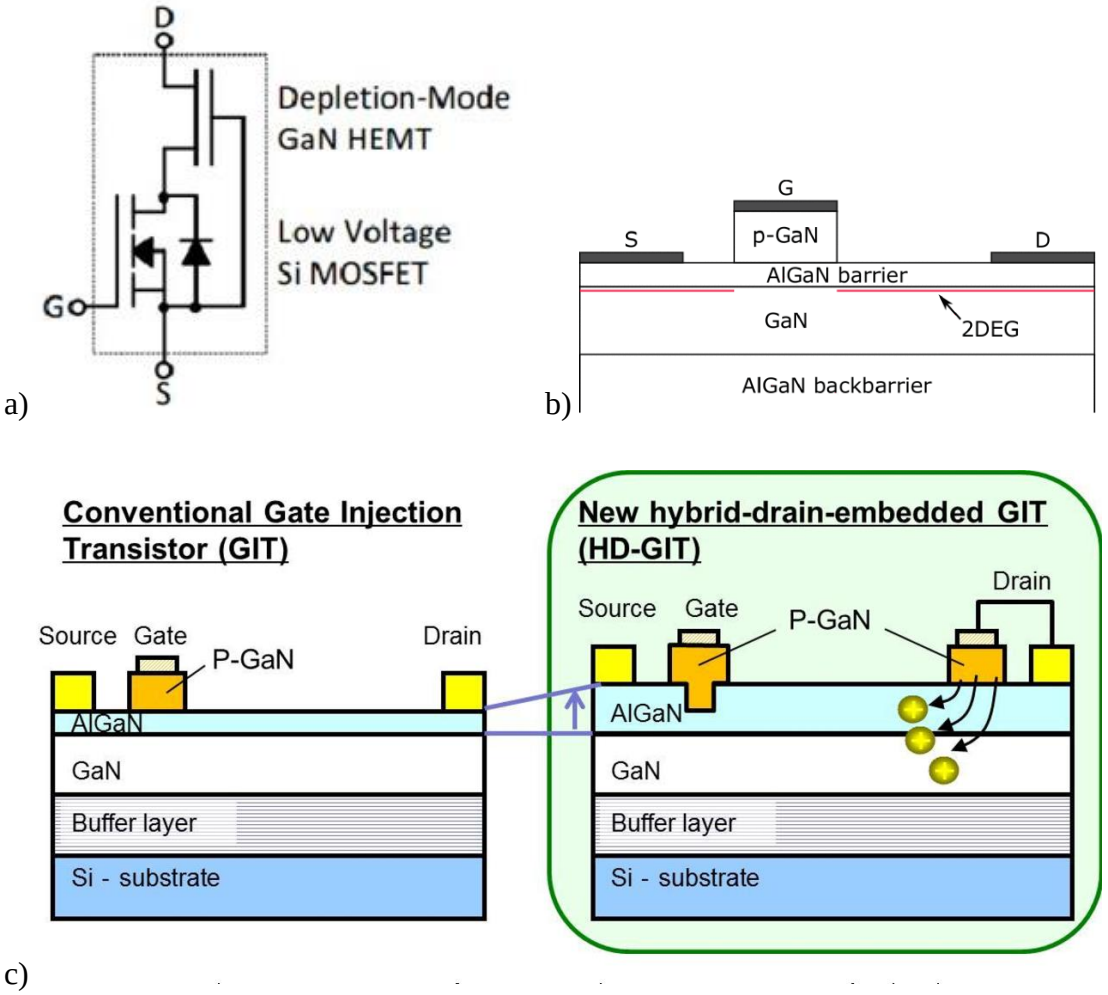


Figure 6. GaN HEMT schematised structure: a) GaN HEMT cascode structure [16], b) GIT HEMT structure [17], c) HD-GIT HEMT structure compared to GIT HEMT structure [18]. While a) uses additional device, b) relies on electron depletion caused by presence of a doped layer, and c) introduces p-GaN region near drain terminal.

Introducing a p-GaN doped layer (commonly achieved using magnesium doping) creates a new gate structure different from the one adopted from Si based technologies. This new gate structure means that an extensive gate reliability characterisation is required for understanding the degradation problems in such structures [19], as discussed in the next section.

2.3 GaN HEMTs degradation mechanisms

To replace traditional Si devices, GaN power devices need to not only showcase superior energy conversion capabilities when compared to traditional Si devices but also meet, or even exceed, the reliability standards of Si devices. Typical failure mechanisms appearing in AlGaN/GaN HEMTs are displayed in Figure 7 [20] on the cross-section of a schematised device.

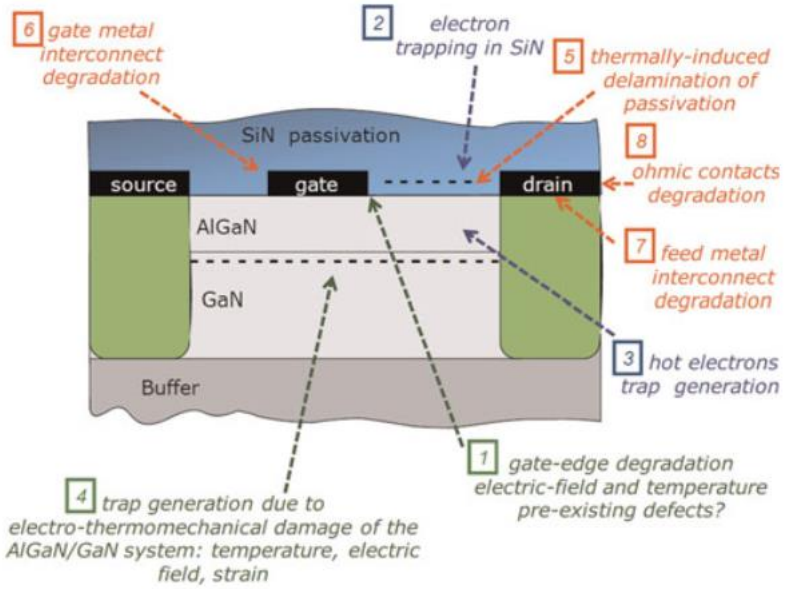


Figure 7. Degrading problems affect AlGaN/GAN HEMTs and their sources [20]. Thermally activated processes are listed in orange (5, 6, 7, 8), hot electrons in blue (2, 3), and polar and piezoelectric related mechanisms peculiar to GaN in green (1, 4).

In Figure 7, the mechanisms listed in orange relate to thermally activated degradation processes: thermally induced delamination of passivation (5), gate metal interconnect degradation (6), feed metal interconnect degradation (7), ohmic metal degradation (8).

These mechanisms have been observed in other semiconductors systems (Si, SiC, GaAs, etc.) and so they are related to the metallization scheme rather than to AlGaN/GaN materials themselves.

Degradation mechanisms listed in blue refer to the presence of hot electrons: electron trapping in SiN (2), hot electron trap generation (3). This type of degradation has occurred in other semiconductor devices such as in Si and SiC devices and is common to all high-voltage field-effect transistors. Hence, these mechanisms are related to hot electrons effects themselves rather than GaN material properties.

Finally, mechanisms marked in green are gate-edge degradation due to electric field and temperature or preexisting defects (1), trap generation due to electro-thermomechanical damage of AlGaN/GaN system: temperature, electric field, strain (4) related to polar and piezoelectric nature of GaN material and is peculiar to GaN semiconductor devices.
The above-mentioned degradation mechanisms contribute the threshold voltage shift of the device making it less reliable, moreover, it was observed that when devices are biased in the OFF-state, significant degradation effects appear leading to decrease of the critical voltage [21].

2.4 Threshold voltage instability

Threshold voltage is a gate to source voltage below which the device is turned off. It depends on the voltage created by the piezoelectric strain and the built-in voltage. Since the strain within the AlGaN barrier, as well as the voltages generated by the inner metallurgy, are relatively constant with the temperature, the threshold voltage is also relatively constant with the temperature [11]. The graph of the normalized threshold voltage versus temperature of the device used in this work (Efficient Power Conversion Corporation EPC2014C) is shown in Figure 8 [22].

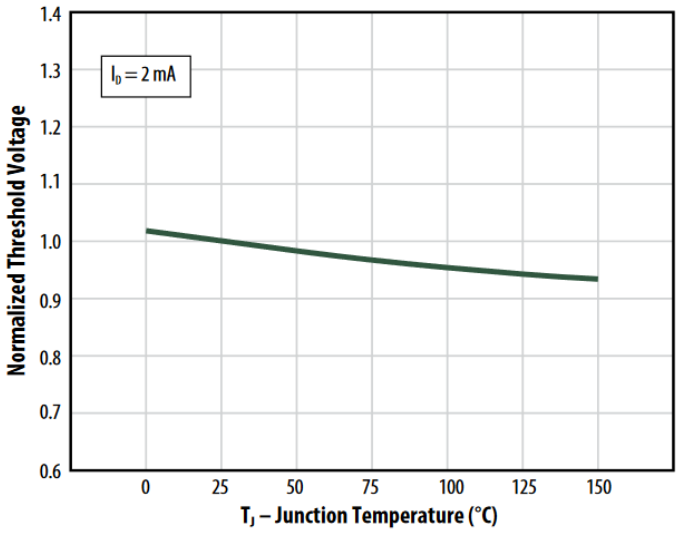


Figure 8. Normalized threshold voltage vs temperature graph of the EPC2014C [22] used in this work.

The schematised cross-section of a p-GaN HEMT is shown in Figure 9 [23], illustrating a device in two states: OFF state with zero gate voltage and depleted region marked, as well as ON state with gate voltage applied and carrier channel formed. Figure 10 [24] depicts the threshold voltage shift caused by increasing temperature; Vth is marked on each graph by pointing out the start of the conducting region.

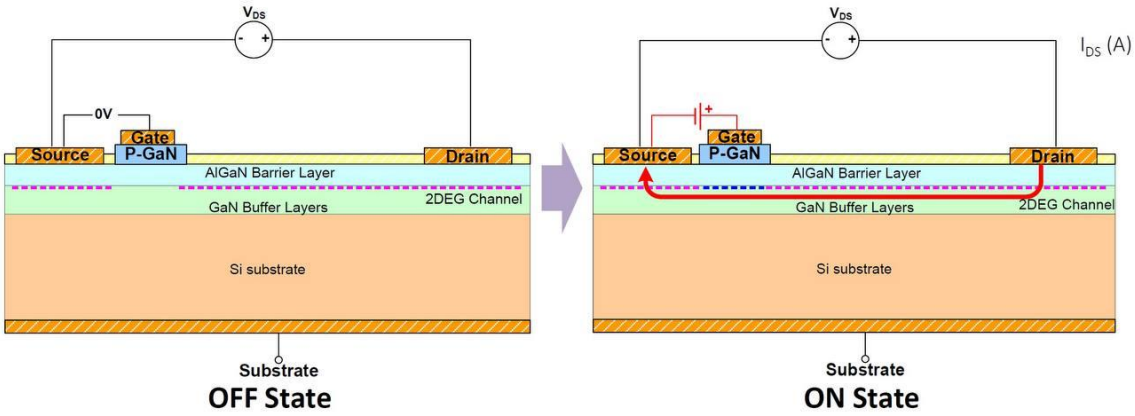


Figure 9. Schematised cross-section of a GaN HEMT in OFF and ON states with 2DEG marked with the pink colour dotted line and carrier region that is formed in the ON state shown with the blue dotted line. Current flow from drain to source is shown with a red arrow [23].

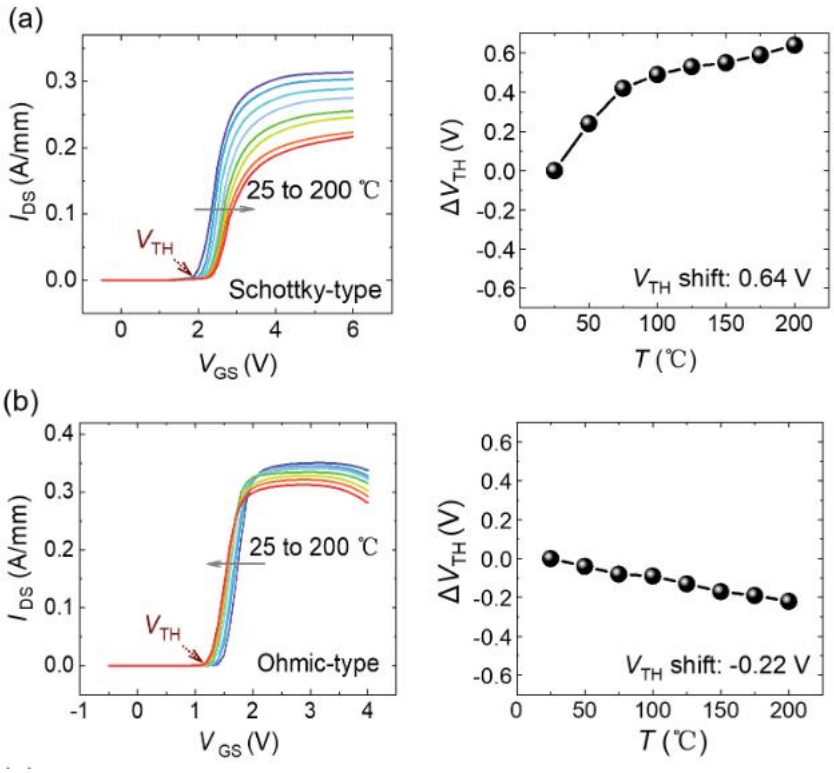


Figure 10. Threshold voltage shift visible on the Id-Vg curve of GaN HEMT under increasing temperature: a) positive shift, b) negative shift [24].

However, there are several factors causing threshold voltage shift in addition to temperature, i.e. gate stress and OFF-state drain stress.

A positive drain OFF-state stress leads to the increase of the threshold voltage. Indeed, a positive threshold shifts in p-GaN gate HEMTs due to OFF-state drain bias stress has been demonstrated in [6]. The phenomenon is shown to be caused by the ionization of acceptor traps leading to hole depletion in the AlGaN layer at the drain edge of the gate.

The ability of GaN HEMTs to replace traditional silicon devices depends on their reliability [25], [26]. In many applications, especially those in which GaN HEMTs are used in critical roles such as power amplifiers, radar systems, and communications infrastructure, device reliability is of critical importance. Threshold voltage instability can lead to device failures and reduced operational lifetimes. In high-frequency and high-power applications, circuit designs are often optimized for specific threshold voltage values. Instability can necessitate more complex design and calibration procedures. Demonstrating stability in threshold voltage is crucial for the widespread adoption of GaN

technology. Thus, it is important to develop precise and reliable techniques helping to analyse threshold voltage shift under various circumstances.

2.5 Threshold voltage shift under the drain bias

High OFF-state drain bias can cause p-GaN HEMTs threshold voltage instability. 2DEG below the gate is cut-off since Vgs is shorted during the OFF-state. When a high drain voltage stress is introduced, the p-GaN to gate contact pn junction is forward biased; at the same time AlGaN to p-GaN is reverse biased. As a result, the junction capacitance of this junction is charged to the drain voltage, negative charges accumulate under the gate (Figure 11(a)). When the device is turned on p-GaN/AlGaN junction is forward biased by the gate voltage, trapped negative charges are removed by the gate current [27], [28] (Figure 11(b)) This process, however, is limited by the fact that p-GaN junction is reverse biased and not all traps can be released. Thus, negative charges are accumulated under the gate leading to the positive voltage shift.

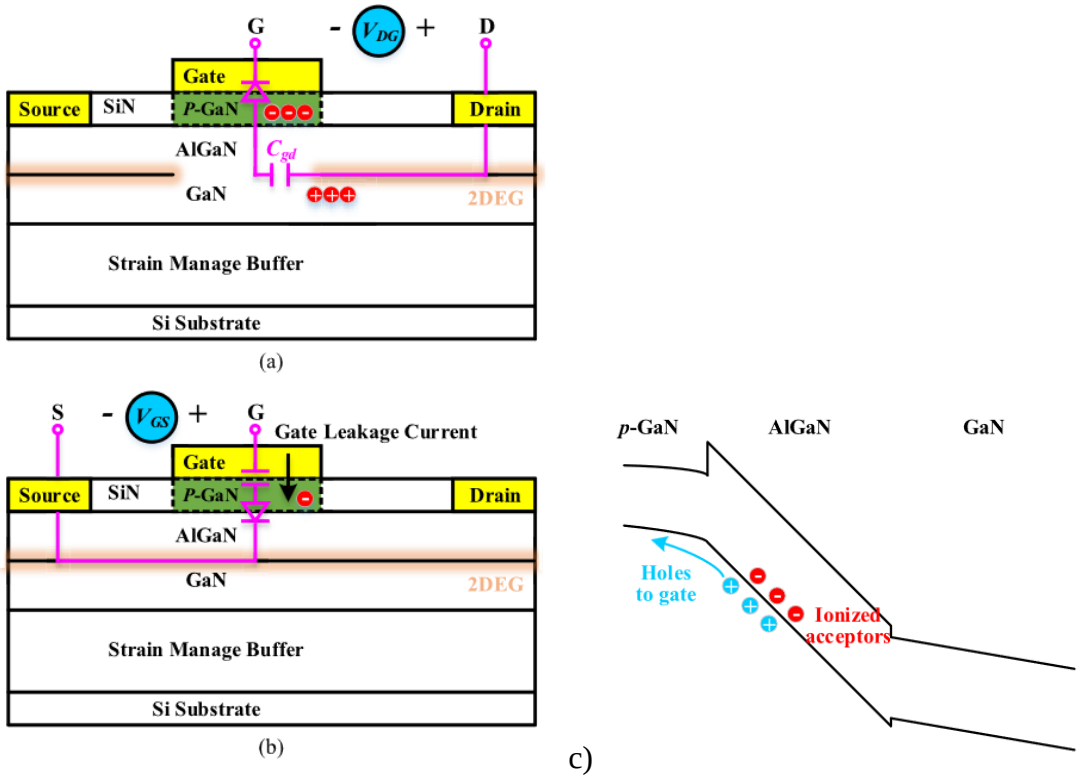


Figure 11. a) Schematised of GaN HEMT during charge and discharge process in the ON-state, b) in the Off-state, c) band diagram of ionized acceptors in the OFF-state [29].

Another explanation for this voltage shift is based on the band diagram analysis according to which the reason for the shift is ionization of acceptor traps in the AlGaN layer under the p-GaN gate. According to [6], hole de-trapping is increased under the high drain stress and the acceptors in the AlGaN region are fully ionized (Figure 11(c)). When the device is in the ON-state the heterojunction barrier at p-GaN/AlGaN junction prevents holes from detrapping. This leads to accumulation of the negative charge below the gate thus positively shifting threshold voltage.

Positive threshold voltage shift can enhance the degradation of dynamic ON-resistance. A larger gate voltage is required to turn on the device resulting in a safe operation gate bias range. In a reverse conduction mode positive Vth shift is causing a larger reverse turn-on voltage leading to higher reverse conduction energy loss during the dead time.

Thus, positive threshold voltage shift is expected to be observed after the introduction of the drain OFF-state stress. Moreover, the shift is expected to increase with the increased duration of a stress pulse as traps will have more time to accumulate yet charge trapping saturation is not expected to occur due to not long enough stress.

This chapter introduced the main properties of GaN which include high bandgap, high critical electrical breakdown field and high electron mobility making GaN semiconductor devices good candidates for high-power and high-switching applications. It also introduced the reliability issues focusing on degradation mechanisms occurring in GaN devices. It also gave a brief overview of threshold voltage instabilities nature, importance and factors affecting it paying special attention to the OFF-state drain stress. The state of the art in threshold voltage measurement techniques and circuits is presented in the next chapter.

3 Overview of Threshold Voltage Measurement

This chapter presents common ways of threshold voltage measurement including 1) the basic procedure of using a probe station and a corresponding curve tracer, 2) the state of the art of threshold voltage measurement circuits, 3) the existing measurement circuit used in this work, and 4) the threshold voltage extraction techniques.

3.1 Procedure for finding the threshold voltage with a probe station and curve tracer

The most straightforward way to find the threshold voltage bias is using a probe station and a curve trace analyser; the measurements are performed directly on the device. The base procedure of finding the threshold voltage shift can be summarized as follows:

1. Preparation: calibrate the curve tracer, connect the device as per user manual.
2. Obtain the Id-Vg graph of the device under test (DUT) by recording the drain current as a respond to a linearly increasing gate voltage from zero to above the threshold value.
3. Apply stress voltage onto the gate of the transistor while keeping the drain to source voltage equal to zero.
4. Obtain the Id-Vg graph of the transistor directly after the stress.
5. Extract the threshold voltage values from the obtained graphs.

The Joint Electron Device Engineering Council (JEDEC) has not yet developed a standardised protocol for GaN HEMTs threshold voltage shift measurement. However, in [30] it was experimentally verified that using the triple sense protocol established by JEDEC (i.e. JEDEC JEP184 [31]) increased the stability of the threshold voltage measurement; the measurements remained stable, despite the degrading voltage stress on the drain and the gate.

3.2 State of the art of threshold voltage measurement circuits

One of the limitations of using a curve tracer and a probe station to find the threshold voltage shift of the device due to OFF-state drain stress is the inability to test the device

under short pulses of a few μs which are most likely to appear in high frequency applications of GaN HEMTs. While investigating the OFF-state trapping phenomena in [32], researchers used an OFF-state stress of 40 ms. In [33], researchers analysed long-term and short-term stress impact on the device, the shortest signal achieved is just 0.5 ms. The shortest pulse duration that the curve tracer can provide is only 100 μs [5].

There exist some circuit-level solutions proposed for threshold voltage measurement i.e. [6], [29], and [34]; however, they still require using of a curve trace analyser used with pulse duration of 500 μs. This value is far too large for the actual switching frequencies. In [6] the researchers managed to decrease the pulse duration to 20 μs, which, however, is still not short enough. At the same time, their solution requires an additional costly setup. The pulse duration is further reduced in [34], achieving 1-2 μs; yet the measuring setup remains expensive. In [29] a characterisation circuit using a half-bridge is presented. The introduction of this circuit allows to reduce the cost and at the same time to achieve the minimum duration of the OFF-state pulse of 2 μs. The limitation of this circuit is that it is only able to measure the threshold voltage shift due to the OFF-state, ignoring the switching transient current effect. Circuit schematic diagrams of [29] and [34] and set-up photo of [34] are shown in Figure 12((a), (b), (c)) ([29], [34]).

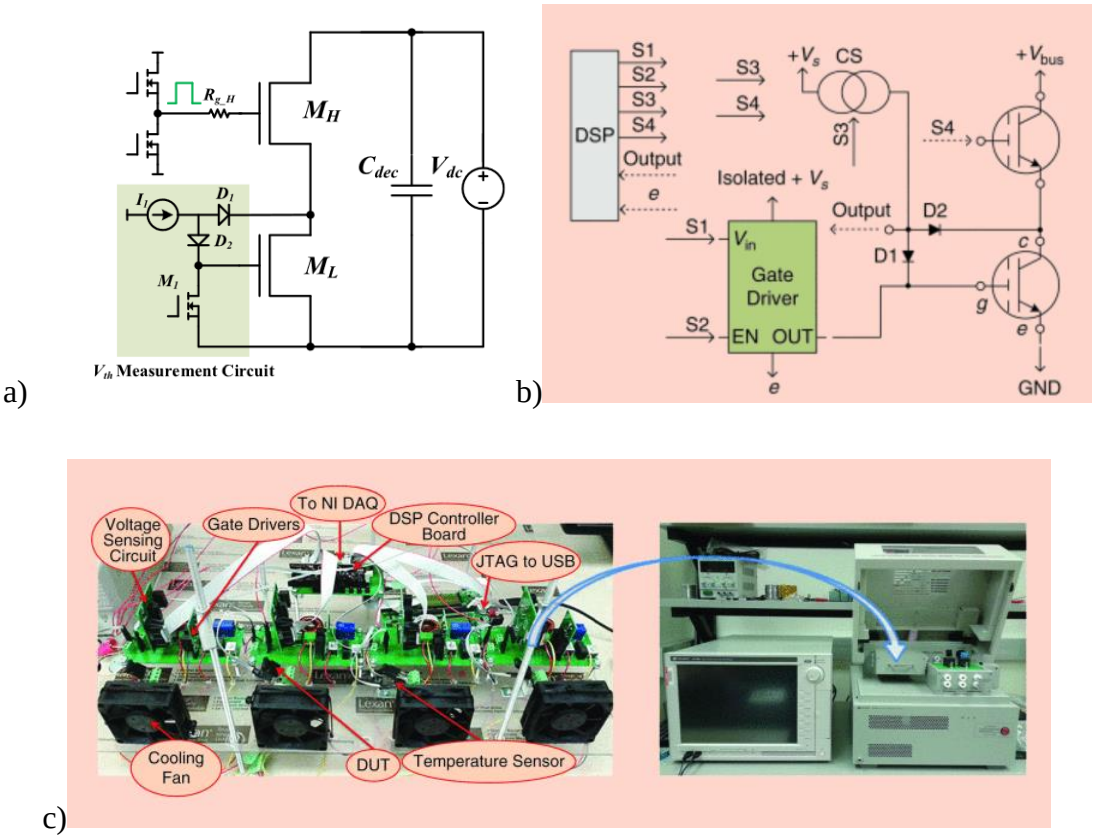


Figure 12. Illustration of the threshold voltage measurement circuits: a) schematic circuit diagram of [29], b) schematic circuit diagram of [34], c) set-up photo of [34].

No patents exactly meant for the threshold voltage measurement of GaN HEMTs circuits could be found in European Patent Office (EPO) and United States Patent and Trademark Office (USPTO) databases. However, some patents propose solutions for the dynamics on-resistance measurement ([35], [36]). Moreover, [37] presents a circuit and measurement technology of a threshold voltage measurement, but it is related to memory devices. Finally, a voltage detection circuit presented in [38] can be used to obtain the threshold voltage, but indirectly as it aims to compare voltage across the other part of the circuit with the voltage across the transistor. These patents are not suitable for this work since they do not focus on GaN HEMT threshold voltage measurement which may lead to a lack of reliability of these method as they either do not consider specific reliability issues such as trapping or devices material properties or do not allow applying short pulsed OFF-state stress onto the device.

3.3 The previously published measurement circuit used in this work

The circuit introduced in this section was created at ICST of NYCU to further reduce the cost of the circuit and overcome the limitations of too long pulse duration and of disregarding the impact of transient current fluctuations; this half-bridge circuit with a series-connected capacitor was developed in [7]. This circuit brings about many advantages such as providing decreased pulse time duration for the OFF-state stress (measurements were conducted starting from 7.6 μs stress pulse), low power consumption, and no need for additional setup apart from the oscilloscope. However, the extensive analysis of the threshold voltage shift results is still needed to be carried out to prove that the obtained data is consistent with the transistor DUT datasheets.

Given its reduced OFF-state stress pulse duration and simplicity to use advantage, this circuit is further analysed in this work and the obtained results of the threshold voltage shift using the measuring circuit and the results of the curve analyser are compared taking into consideration the manufacturer's data.

3.3.1 Operation principle of the previously published circuit

The previously published circuit consists of a half-bridge and a capacitor connected in series at source of the device under test (C) and decoupling capacitor connected in parallel to the device and in-series capacitor (C_{decap}). The circuit diagram is shown schematically in Figure 13(a) and the experimental setup in Figure 13(b) [7].

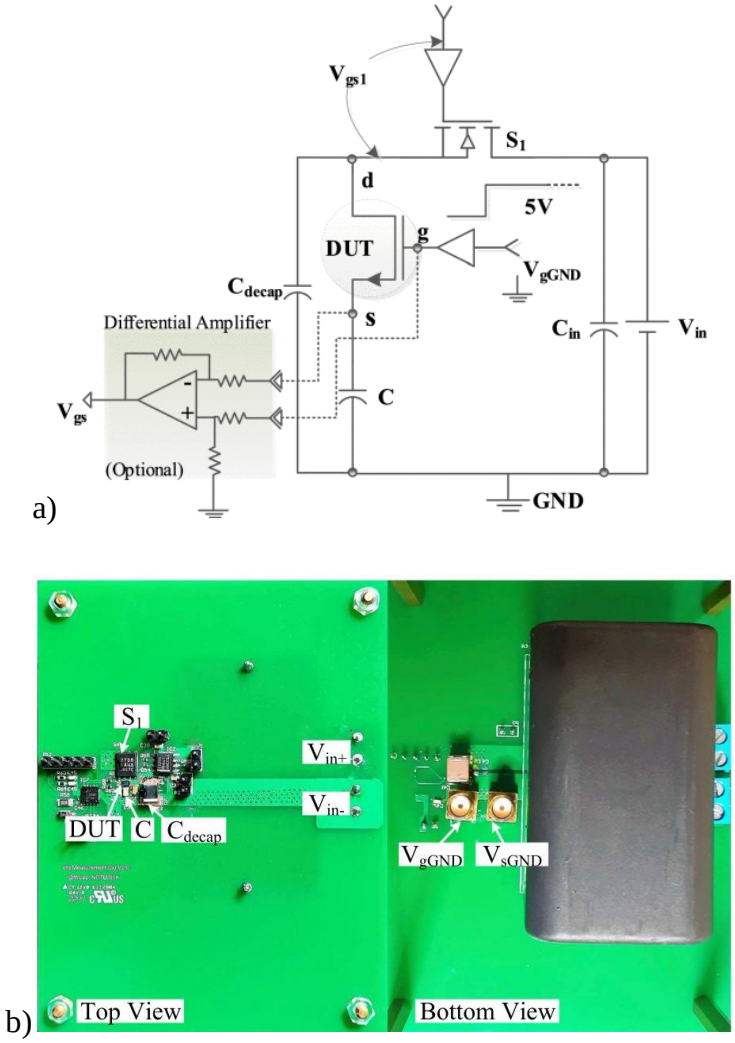


Figure 13. a) Circuit for threshold voltage characterisation [7]; high V_{gS1} produces OFF-state stress of the DUT, and b) experimental set-up of the circuit [7].

The circuit operation consists of three parts, the corresponding operational key waveform can be seen in Figure 14 [7] and are described below:

- Before OFF-state stress, $[t_0 - t_s]$: switch S_1 and DUT are kept in the OFF state by applying zero voltage at gate and source terminals. This step ensures unwanted OFF-state stress to be avoided.

- OFF-state stress mode, $[t_s - t_m]$: V_{gS1} is high and V_{gGND} is low. This generates OFF-state stress across drain and source terminals of the device.

- Measurement mode, $[t_m - t]$: V_{gGND} is high, causing current to flow through the C and $V_{sGND}$to rise. This reduces the V_{gs} across the DUT initiating decrement in the DUT current I_{d_sat}. As I_{d_sat} reaches I_{th} the V_{gs} is equal to V_{th}.

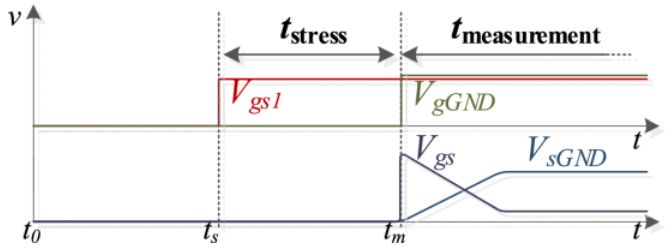


Figure 14. Operational key waveform of the circuit [7].

The results of threshold voltage shift obtained using this circuit are presented in Chapter 5 and compared with the results of Vth from the probe station measurements presented in Chapter 4.

3.4 Threshold voltage extraction techniques

The Id-Vg curve is obtained by providing a gate voltage to the device in small increasing steps. There are several techniques used to extract the threshold voltage from the Id-Vg curve of the device. Commonly-used linear region extraction methods are reviewed in this section and are applied in Chapter 4 to obtain the V_{th} value from the measured data to observe the advantages and limitations of each one for the test configurations.

The methods are described by the semiconductor engineering trade organization and standardisation body JEDEC in various references mentioned in the following subsections.

3.4.1 Constant current method

A first and simple way to extract the threshold voltage from the Id-Vg curve commonly used in the industry is the constant current method [39], [40]. According to JEDEC [41], the constant current method states that threshold voltage ($V_{th(ci)}$) of a transistor is a gate to source voltage (V_{gs}) corresponding to a drain current value (I_d) of a constant current

(I_{d0}), which is appropriate for a certain technology multiplied by the ratio of gate width (W) to gate length (L):

$$V_{th(ci)} = V_{gs}\ at\ I_d = I_{d0} \cdot W/L \quad (1)$$

The constant current value is defined such that $V_{th(ci)}$ is in the subthreshold region of the device. The values are defined by JEDEC for MOSFET devices; however, it should be noted that the characterisation value for GaN HEMT is still not standardised. Moreover, gate width and length of a packaged device are usually not provided by manufacturers; thus, values of I_d are chosen empirically in the sub-threshold region. There is no hard rule on choosing the exact value and it depends on the measurement set-up limitations targeting the transition region on the graph of Id-Vg curve.

Advantage: the method is simple to use since it requires very little to no calculation and can be used for estimation of the threshold value. It is useful for industrial application because the result can be obtained with a single voltage measurement.

Limitation: the result is dependent on the drain current value chosen to define the threshold voltage; thus, inconsistent results are likely to occur.

3.4.2 Linear extrapolation threshold voltage method

A second way to extract threshold voltage from the Id-Vg curve is extrapolating it from measurements of the maximum slope $g_{m(max)}$. It is calculated by subtracting the drain current at the point of the maximum slope of the curve $I_{d(gm(max))}$ divided by the maximum slope of this curve in the linear region from the gate voltage value at the point of this slope $V_{gs(gm(max))}$ [42].

$$V_{th(ext)} = V_{gs(gm(max))} - I_{d(gm(max))}/g_{m(max)} \quad (2)$$

Advantage: The result is more grounded compared to the above-described constant current method while still being simple to use.

Limitation: the result can be strongly influenced in case of significant presence of drain series parasitic resistances and mobility degradation.

3.4.3 Transconductance change/second derivative method

A third way to extract threshold voltage from the Id-Vg curve is by means of the transconductance change method, also called the second-derivative method; it is one of the commonly-used threshold voltage extraction methods that was developed to avoid dependence on series resistance [43]. According to this method, the V_{th} value is determined as the gate voltage value at which the derivative of the transconductance is maximum. The maximum linear transconductance is equal to the maximum slope of the Id-Vg curve in the linear region. According to JEDEC, the gate voltage is incremented no greater than 20 mV per step from below the turn-on voltage to a value great enough to make sure the $g_{m(max)}$ has been reached [44].

$$\frac{dg_m}{dV_g} = \frac{d^2 I_d}{d^2 V_g^2}, V_{th(tc)} = V_g \; at \; \frac{dg_m}{dV_g}(max) \qquad (3)$$

Advantage: Eliminates the effect of the mobility degradation and parasitic resistance [45].

Limitation: This method is sensitive to measurement error and noise, since the second derivative is similar to applying a high-pass filter to the measurement.

This chapter has presented an overview on threshold voltage measurement including a procedure used on a curve tracer and probe station and state-of-art alternative methods using custom developed measurements circuits. It introduced the circuit that are further analysed in this work and also presented threshold voltage extraction methods that are applied to the data obtained by the curve tracer later in this work.

The following chapter includes the experimental part where threshold voltage measurements procedure and results are presented, and the extraction techniques are applied to the new data to determine the most suitable method.

4 Threshold Voltage Measurement with the Probe and Curve Tracer and Extraction

4.1 Measurements procedure on the probe station

For this master thesis, the measurements were performed according to the procedure presented earlier in Section 3.1. The measurement setup consisted of a Keysight B1505A curve tracer connected to a N1258A module (connection diagram shown in Figure 15); the probe station (see Figure 16) is a commercial product of Apolloware, it was provided by NYCU.

The probe station setup with the DUT is presented in Figure 16 and a connection example diagram is provided in Figure 15 [46]. In the connection diagram, the DUT is delimited by the dashed orange box. The connection setup used for the device characterisation was based on this diagram and consists of two types of source measurement units (SMU) and one type of ground unit.

- High Current Source Measurement Unit (HCSMU) was chosen to be used on the drain because the drain current is expected to be in the range between 10 to 20 A;
- Medium Current Source Measurement Unit (MCMSU) was used for the gate terminal;
- Finally, Ground Unit (GNDU) was used for grounding.

Five probes were used for performing the measurements:

- A pair of High Force (noted High F in the figure) and High Sense (High S) probes for the drain (D);
- A pair of Low Force (Low F) and Low Sense (Low S) probes for the source (S);
- And a single probe for the gate (G). Force source provided voltage source and sense port detected voltage of the corresponding terminal.

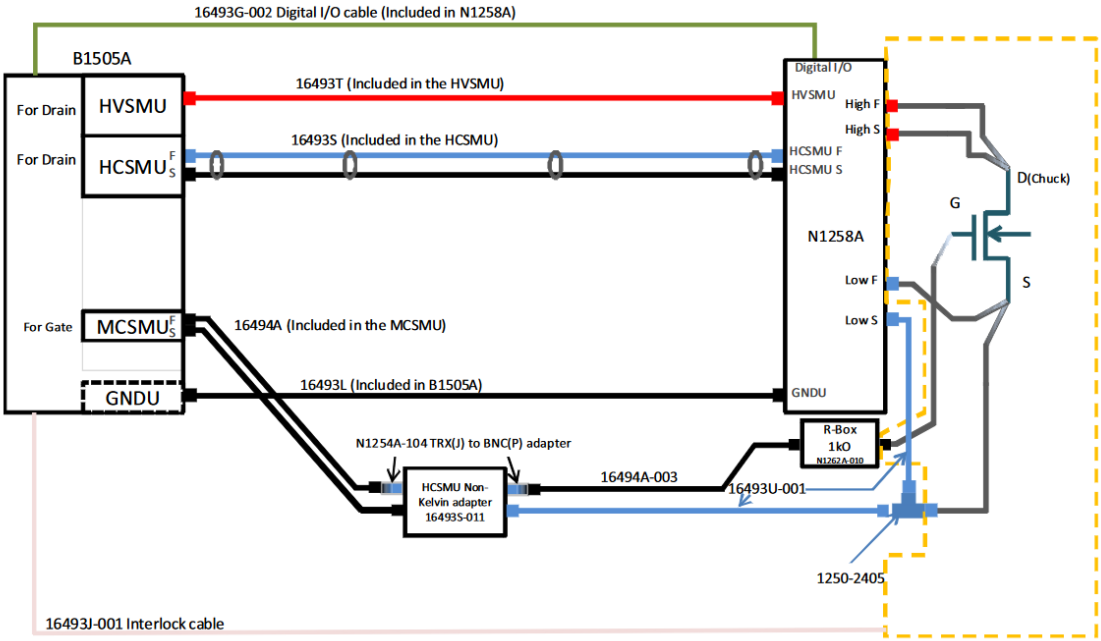
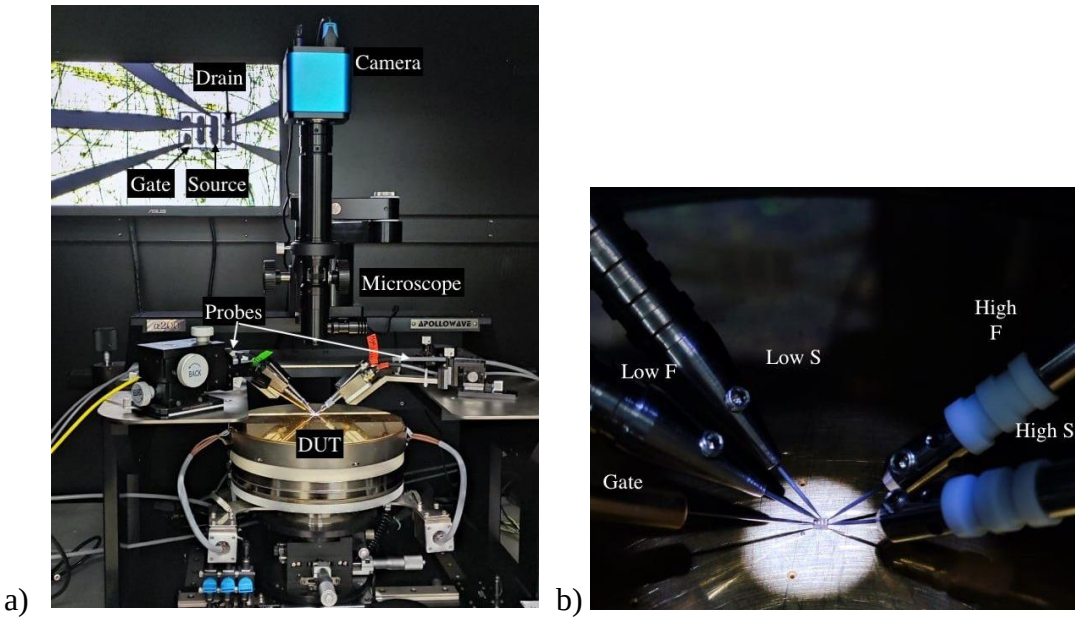


Figure 15. Connection example for 3 kV/20 A automated measurement with N1258A Module [46].



a) b)

Figure 16. a) Probe station with DUT (with microscopic view shown on the LCD display in the background), b) DUT and needles close-up.

The DUT was forced under drain OFF-state stress for durations of 100 µs, 1 ms, 10 ms, 100 ms, 1 s, and 10 s, each with 12 V, 24 V and 32 V constant stress pulses. The drain current versus gate voltage values were obtained from a fresh device (i.e. freshly manufactured or rested for a long time after the previous measurement), immediately after

each stress application by sweeping Vg from 0 to 6 volts. All experiments were conducted under room temperature (23 to 25 ℃).

4.2 Measurements results with the probe and curve tracer

The waveform obtained with the help of the EasyEXPERT curve tracer software is shown in Figure 17. The graph represents the device characteristics after the 32 V OFF-state stress voltage was applied for a varying duration of time (from 100 µs to 10 s). The Y-axis of the graph shows the drain current on a logarithmic scale. A positive threshold voltage shift can already be visually recognised from the raw data, i.e. the shift increases correspondingly to the pulse duration and is visible in the region where VG is between 1 and 2.5 V.

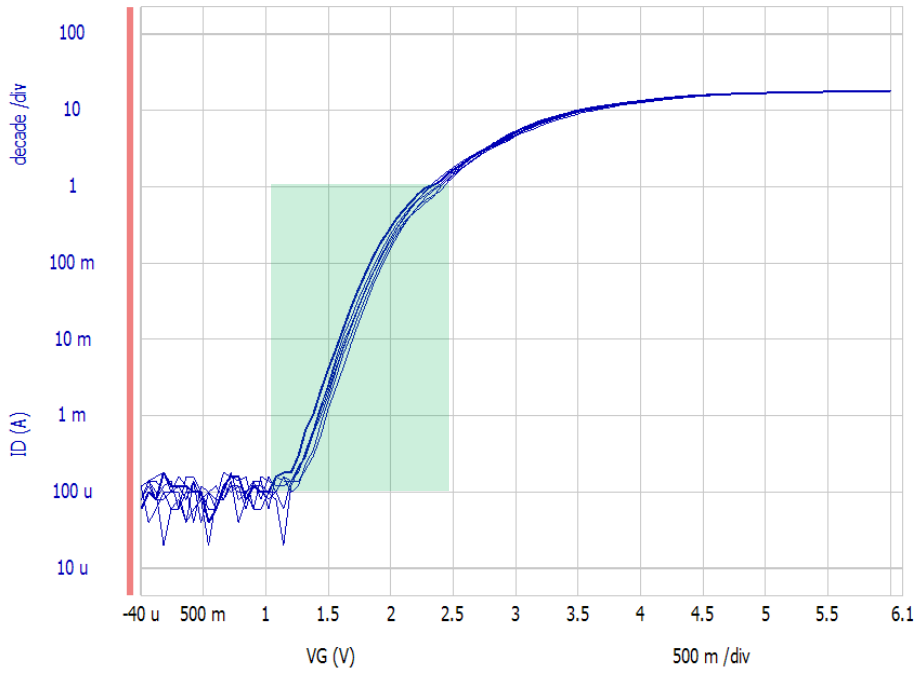


Figure 17. Id-Vg curves positive shift obtained by the curve tracer on a logarithmic scale with visible shift in the region where VG is between 1 and 2.5 volts (within the green rectangle).

4.3 Applying the threshold voltage extraction techniques

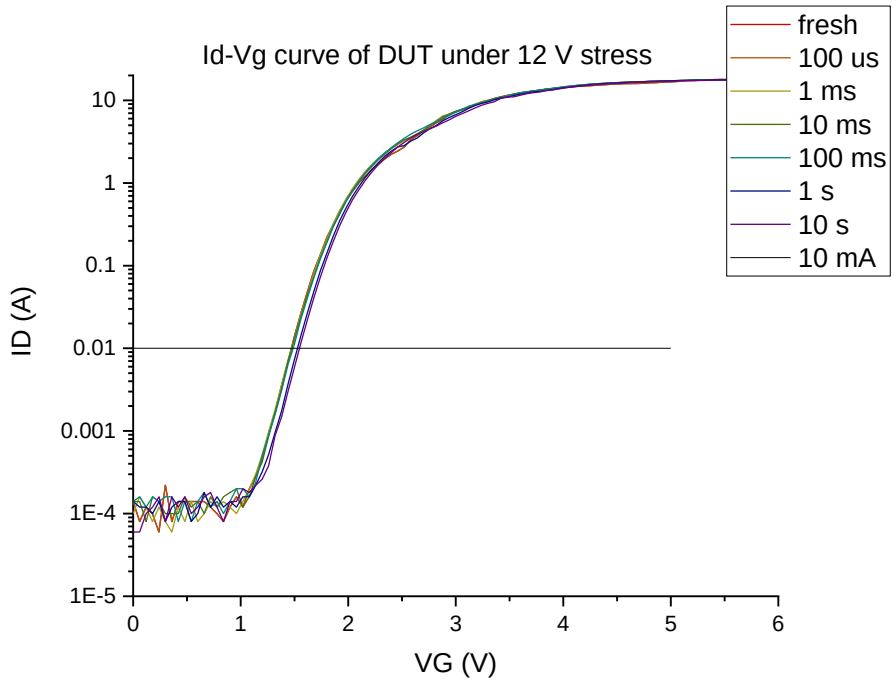
The threshold voltage extraction methods presented in Chapter 3 are applied to the obtained data set for 12 V, 100 µs to 10 s stress of the DUT as this result was the most successful, showing an increased slope of the I-V curve with an increased stress pulse

duration. The results obtained with these methods are compared and evaluated to find an optimal threshold voltage extraction technique that is then used to analyse the rest of obtained measurement data sets.

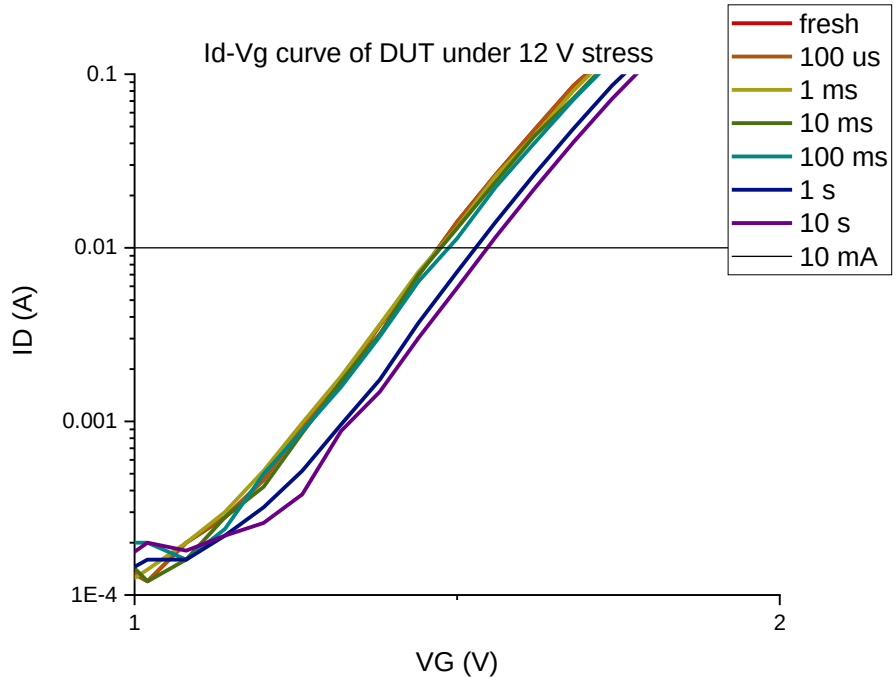
4.3.1 Applying the constant current method

Since gate dimensions are unknown for the EPC2014C device [22] characterised in this work, the I_d value can only be used instead of I_{d0}. The general rule is to aim for the lowest reliable drain current value. This value should be, in the beginning of the conducting region above the noise level, high enough to yield a stabilized and relatively noise-free plot. In [32], [33], values were taken two orders of magnitude above the noise level and were 100 mA and 1 mA, respectively. In this work, considering the DUT, the I_d value chosen to find the threshold values is set to 10 mA.

Threshold voltage extraction includes finding gate voltage value at the intersection with the chosen drain current constant value. The extraction process plot is shown in Figure 18, both on a full scale and zoomed-in on the intersect region. The Vth results are presented in Table 1.



a)



b)

Figure 18. Illustration of Vth extraction using the constant current method: a) on a full scale, b) zoomed-in on the conducting region.

Table 1. Threshold voltage extraction results using constant current method.

Stress time	Vth (Constant current method)
Fresh (0 s)	1.471 V
100 μs	1.471 V
1 ms	1.472 V
10 ms	1.475 V
100 ms	1.487 V
1 s	1.529 V
10 s	1.547 V

The measurement results appear accurate as the threshold voltage value is within the expected range (0.8 to 2.5 V) and is close to the typical value of 1.4 V (deviation between +0.071 V and +0.147 V) mentioned in the datasheet [22]; moreover, the Vth values increase with the pulse duration increasing, as expected.

4.3.2 Applying the linear extrapolation method

The first step for performing the linear extrapolation method is finding the values of the first derivative of the drain current with respect to the gate voltage. The results are shown on the graph in Figure 20. Next, after determining the maximum values of the derivatives $g_{m(max)}$, for each plot, the corresponding drain current value $I_{d(gm(max))}$ was found from the graph. Then, a tangent line was plotted at the same point to find the intersection point of this line with x axis, $V_{gs(gm(max))}$; the extrapolation results are shown in Figure 19 Finally, the threshold voltage value was calculated using Equation (2) from Section 3.4.2; the calculation results and parameters values are presented in Table 2

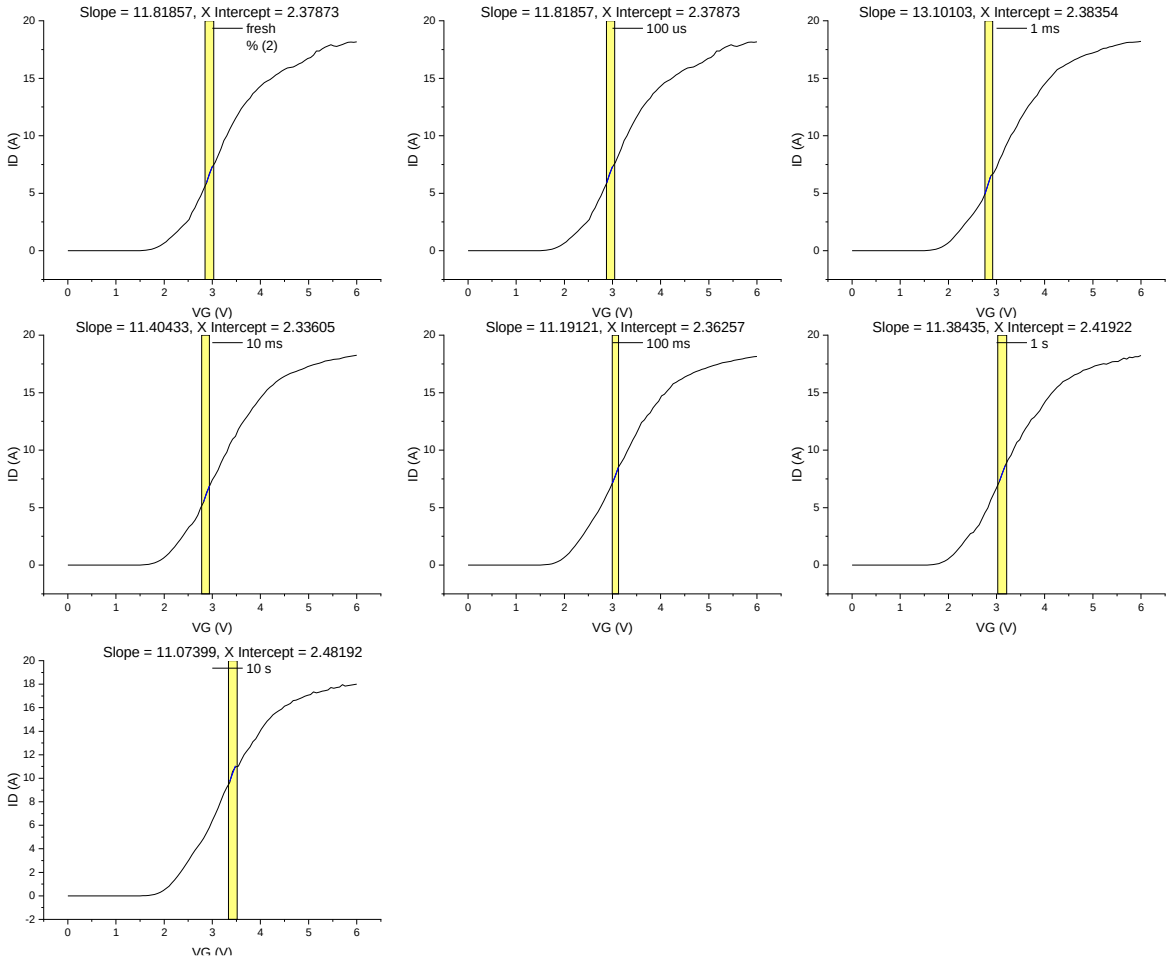


Figure 19. Tangent line (in yellow) at the maximum slope for each stress time (fresh (i.e. 0 s) , 100 μs, 1 ms, 10 ms, 100 ms, 1 s, and 10 s) Id-Vg graphs.

Table 2. Threshold voltage extraction using linear extrapolation method results (taking the values from Figure 19 and applying Equation (2) from Section 3.4.2.

Stress time	$g_{m(max)}$	$I_{d(gm(max))}$	$V_{gs(gm(max))}$	$V_{th(ext)}$ (linear regression method)
Fresh (0 s)	11.818 V	6.725 V	2.379 V	1.810 V
100 μs	11.818 V	6.725 V	2.379 V	1.810 V
1 ms	13.101 V	5.715 V	2.384 V	1.947 V
10 ms	11.402 V	6.299 V	2.336 V	1.784 V
100 ms	11.196 V	7.740 V	2.363 V	1.671 V
1 s	11.384 V	7.999 V	2.419 V	1.717 V

10 s	11.095 V	10.566 V	2.482 V	1.530 V

The extracted V_{th} values remain within the expected 0.8 – 2.5 V range; however, they are all greater than the typical 1.4 V value (deviation between +0.130 V and +0.547 V). There is also a lack of consistency as Vth does not show an increasing trend as the stress time is increasing.

4.3.3 Applying the transconductance change method

According to transconductance change method, it is needed to take the second derivative $\frac{dg_m}{dV_g}$ of the drain current with respect to the gate-source voltage to find the threshold voltage value. The threshold voltage is a gate voltage at the maximum second derivative value $\frac{dg_m}{dV_g}(max)$. The graph of second derivatives for each Id-Vg curve of 12 V stress data set is shown in Figure 20. The resulting values of the threshold voltages extracted using this method are presented in Table 3.

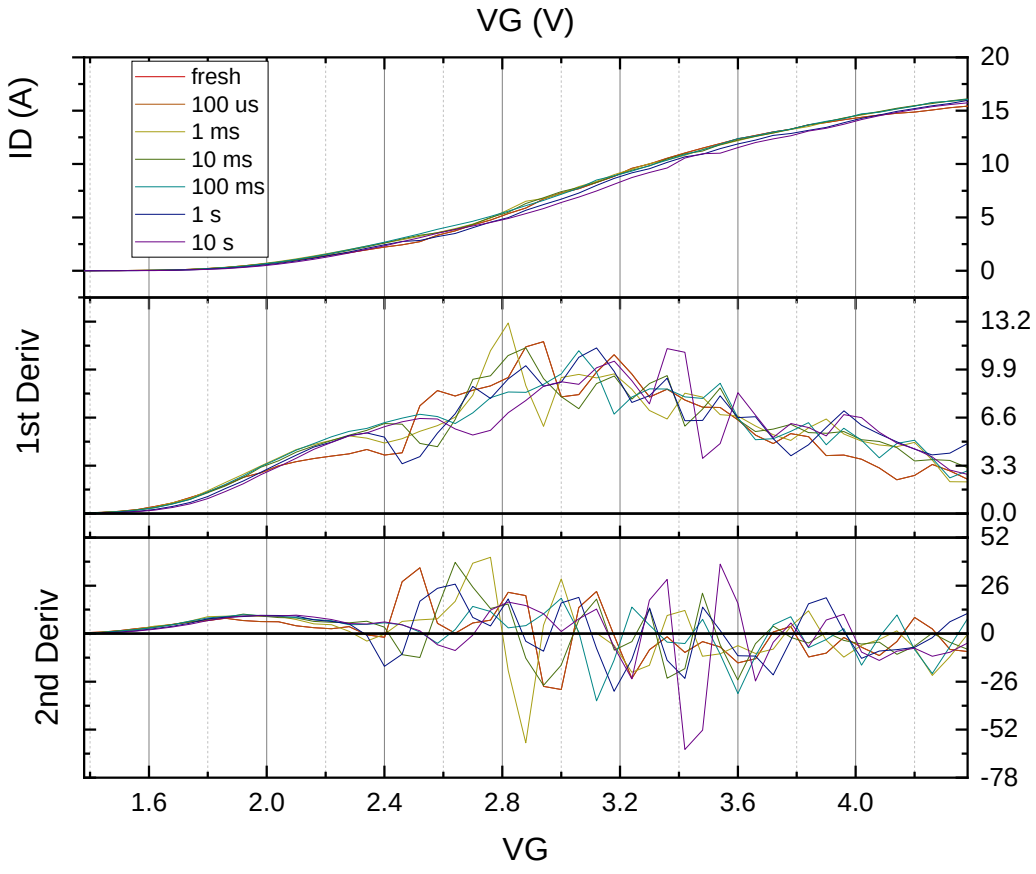


Figure 20. Graph of Id-Vg curve of the device under 12V stress, its first and second derivatives.

Table 3. Results of threshold voltage extraction using transconductance change method.

Stress time	Vth (Transconductance/second derivative method)	Max second derivative $\frac{dg_m}{dV_g}(max)$
Fresh (0 s)	2.520 V	35.665
100 μs	2.520 V	35.665
1 ms	2.760 V	41.324
10 ms	2.640 V	38.614
100 ms	2.700 V	14.700
1 s	2.640 V	26.817
10 s	3.540 V	37.694

As can be seen from Table 3, Vth results extracted with the second derivative method fall outside the expected range (0.8 – 2.5 V) as they are all higher than 2.5 V; they all significantly differ from the typical 1.4 V value (deviation between +1.120 V and +2.140 V). Moreover, there is also no clear increase in threshold voltage with increasing stress time.

4.3.4 Comparison of the extracted values of threshold voltage by the three methods

All the results are summarized in Table 4 and plotted on a graph (Figure 21) and are discussed below.

Starting from the second method, the linear extrapolation method: this was the most time consuming to perform and showed not consistent results, i.e. although the extracted Vth values were within the expected range (0.8-2.5 V), they were far from the expected 1.4 V value (deviation between +0.12958V and +0.54732V) and were mostly decreasing (instead of increasing) with rising pulse duration. This result is most probably caused by the presence of noise in the data and also by the fact that the obtained data goes through integration by the curve tracer software.

The third method, i.e. transconductance change (second derivative) method, was relatively simple to perform. On the one hand, the results obtained using the second derivative method mostly showed increasing Vth with increasing stress time as expected; however, the values were outside of the expected range (i.e. above 0.8-2.5 V) and well above the expected 1.4 V value (deviation between +1.120 V to +2.140 V). This error could be due to the sensibility to noise of this method.

Coming back to the first method, i.e. constant current method: it was the easiest one to perform. Moreover, the results obtained using this constant current method are the most consistent (increasing threshold voltage values with increasing stress time) and are the closest to the expected value of 1.4 V (deviation between +0.129.58V and +0.54732V) of the typical threshold voltage provided in the datasheet.

Therefore, the constant current method was selected to be used for further threshold voltage extractions.

Table 4. Threshold voltage extracted using different techniques results.

Stress time	Vth (transconductance change/second derivative (SD))	Vth (Linear extrapolation (LE))	Vth , V
Fresh (0 s)	2.520 V	1.810 V	1.471 V
100 μs	2.520 V	1.810 V	1.471 V
1 ms	2.760 V	1.947 V	1.472 V
10 ms	2.640 V	1.784 V	1.475 V
100 ms	2.700 V	1.671 V	1.487 V
1 s	2.640 V	1.717 V	1.529 V
10 s	3.540 V	1.530 V	1.547 V

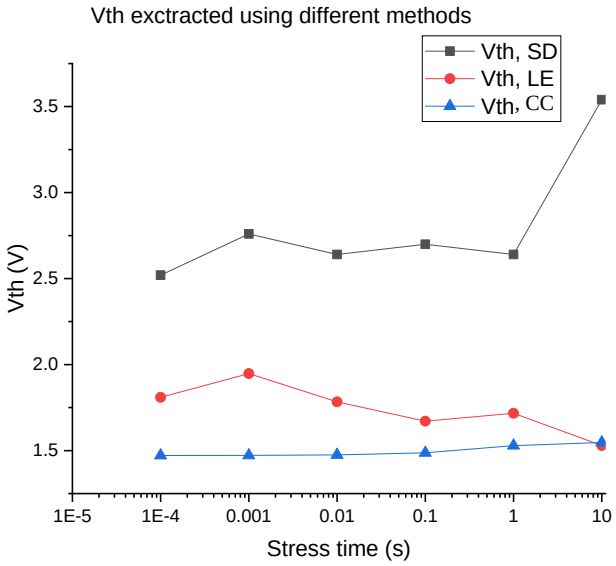


Figure 21. Threshold voltage of the DUT under 12V OFF-state stress extracted using transconductance change/second derivative (SD), linear extrapolation (LE) and constant current (CC) methods. The constant current method shows the most consistent results, closest to the expected voltage threshold value.

4.4 Threshold voltage results for 12, 24 and 32 V OFF-state stress

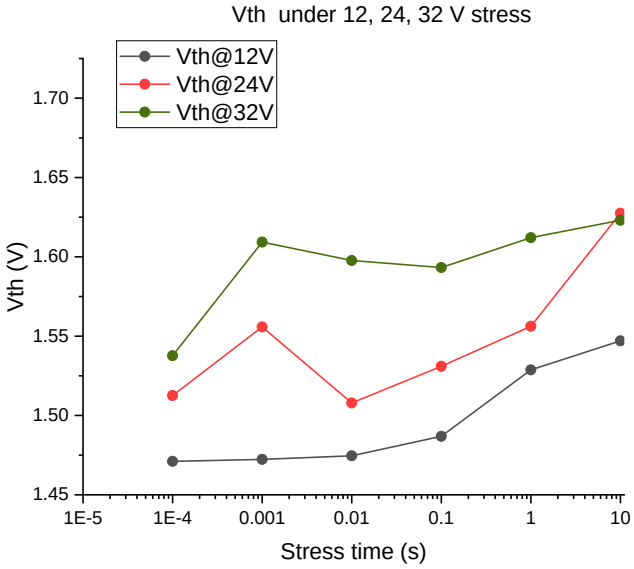
The results of the extracted threshold voltage using the previously selected method (constant current method) are summarised below. The values of the threshold voltage as well as the threshold voltage shifts are presented in Table 5 and are plotted on the graph shown in Figure 22.

As can be seen, with the selected constant current method, all the results fall within the expected 0.8 - 2.5 V range and, generally, the threshold voltage values increase together with the increasing OFF-state stress pulse duration.

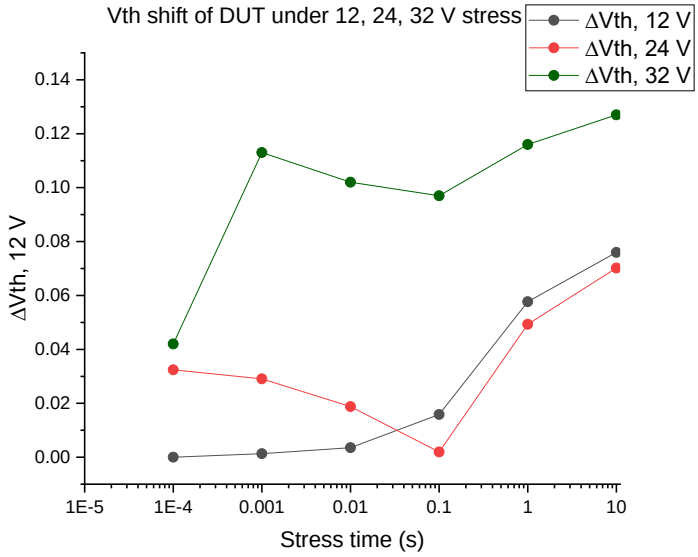
Table 5. Threshold voltage and threshold voltage shift (Δ Vth) of DUT under 12, 24 and 32 V stress.

Stress time	Vth at 12 V stress voltage	Vth at 24 V stress voltage	Vth at 32 V stress voltage	Δ Vth at 12V stress voltage	Δ Vth at 12 V stress voltage	Δ Vth at 12 V stress voltage
Fresh (0 s)	1.471 V	1.489 V	1.588 V	0.000 V	0.000 V	0.000 V
100 µs	1.471 V	1.513 V	1.610 V	0.000 V	0.032 V	0.024 V

1 ms	1.472 V	1.556 V	1.644 V	0.001 V	0.029 V	0.067 V
10 ms	1.475 V	1.508 V	1.631 V	0.004 V	0.019 V	0.019 V
100 ms	1.487 V	1.531 V	1.668 V	0.016 V	0.002 V	0.042 V
1 s	1.529 V	1.556 V	1.646 V	0.058 V	0.049 V	0.067 V
10 s	1.547 V	1.627 V	1.694 V	0.076 V	0.070 V	0.139 V



a)



b)

Figure 22. A) threshold voltage and b) threshold voltage shift (Δ Vth) under 12, 24 and 32 V stress voltages, applied for 100 µs, 1 ms, 10 ms, 100 ms, 1 s and 10 s.

This chapter has introduced the probe station and curve tracer setup used for the device characterisation as well as raw data example. Then, threshold voltage extraction methods previously discussed in Chapter 3 were applied to the obtained dataset to figure out the most suitable extraction method to be used in this work; this method is the constant current one. Finally, the results of threshold voltage shift of the device under 12, 24 and 32 V stress were presented and plotted.

The next chapter compares the obtained results with the results from the previously published paper and discuss advantages and limitations of the probe-station threshold voltage shift measurement and proposes a threshold voltage extraction method to deal with those limitations.

5 Comparison of the Results, Discussion, and Proposed Procedure

This chapter presents and discuss the comparison between the results obtained with the circuit-level and device-level approaches, the advantages and limitations of Vth measurement using a probe station, and the steps of the proposed measurement procedure.

5.1 Comparison of circuit-level and device-level results

At the circuit-level, the obtained threshold voltage values of the device under 32 V stress were found to be 1.32 V, 1.36 V, 1.42 V and 1.6 V for OFF-state stress times of 7.6 µs, 76 µs, 700 µs and 7.2 ms, respectively. For comparison purposes, normalized threshold voltage shift obtained using both circuit measurements and probe station measurements are shown in Figures 23 [7] and 24.

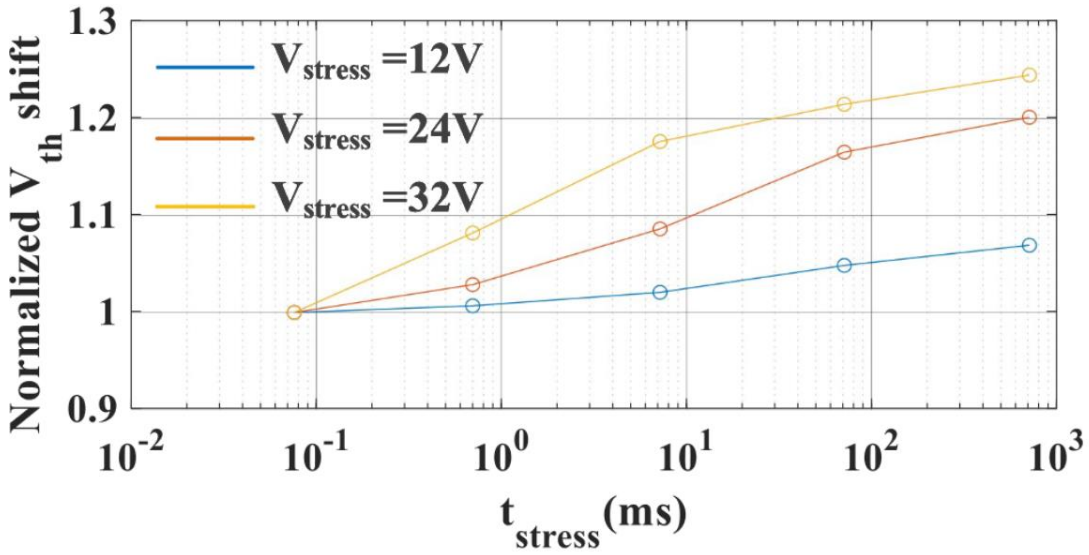


Figure 23. Circuit-level normalized Vth shift at 12, 24, and 32 V stress voltages over time [7]. A comparison of these existing results and those of Figure 24 are discussed in this section.

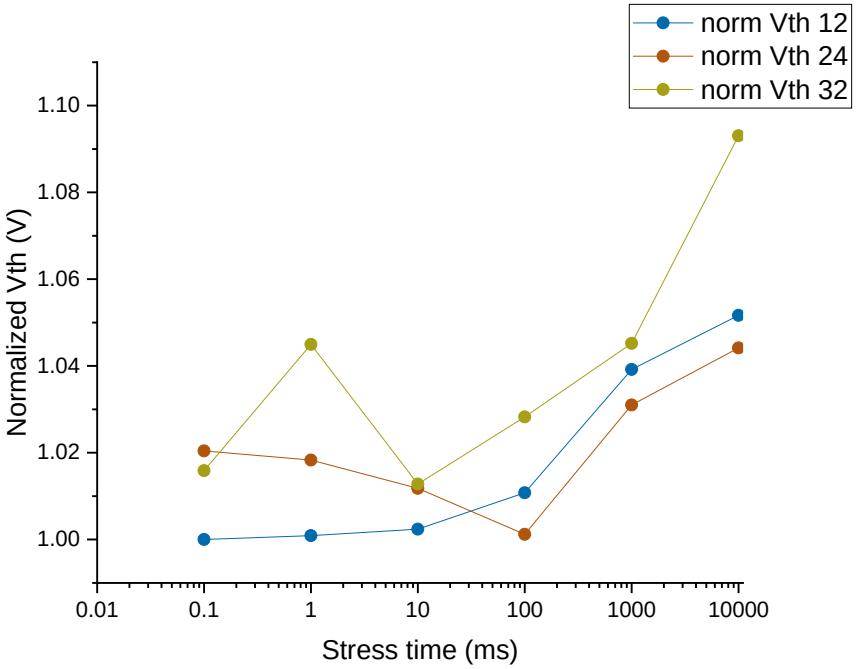


Figure 24. Device-level normalized Vth shift values at 12, 24 and 32 V stress voltages over time. A comparison of these new results and the existing results of Figure 23 are discussed in this section.

Comparing Figure 23 and Figure 24, it can be observed that the existing circuit-level results are more consistent and show increased Vth shift with increased pulse duration and voltage. The new device-level results are less consistent and include errors (deviation between +0.130 V and +0.547 V), but still show the increasing trend of Vth. While this method at the device-level can help to estimate the value by showing the increasing trend, it is less reliable if an exact Vth value for a certain stress voltage level and pulse duration is required. When compared to the typical value provided by manufacturer, device-level result shows deviation of at least 10% and circuit-level result – roughly 5% deviation.

Both sets of results were extracted from Id-Vg curves using the constant current method. While it was only possible to use 10 mA intersect values for the probe station due to the lower resolution, the measurement circuit Id-Vg curve resolution allowed to take Vth values at 2 mA.

5.2 Advantages of Vth measurement using a probe station

If the required modules are available, the probe station measurement approach can be used on various devices including wafer measurement (it is not possible to measure those on the circuit, obviously).

Using a probe station for voltage threshold measurement allows applying different types of stress tests to the DUT, simulating the operating conditions, and revealing its reliability and stability. It is possible to stress the gate or the drain of the device and use either switching or constant voltage or current.

5.3 Limitations of Vth measurement using a probe station

This section reflects the insights gained during the laboratory work conducted as part of this master thesis; it highlights the practical challenges and limitations of using a probe for threshold voltage measurement. The lessons learned presented in this section can be useful to students and researchers working in this field.

A limitation of using a probe station for voltage threshold measurement is that it requires multiple modules and a complex setup, which can increase the cost, time, and complexity of the measurement. The probe station needs e.g. specific needles, a power supply, current source, voltmeter, probe array, microscope, chuck, and a stage, as well as cables and connectors to link them together. The probe station also needs a software interface to control and monitor the measurement, which can have limitations in terms of functionality, compatibility, and integration, e.g. the software may not support the required measurement frequency, resolution, or range, or it may not be compatible with other software or hardware components.

5.3.1 Connection issues

Set-up preparation is time-consuming since it requires establishing a proper connection between the modules, calibration of the device, connecting the probes to the DUT and changing the needles. Moreover, the software is not perfectly optimised and all the parameters have to be entered manually and creating a program for more complex measurement takes additional time.

Needs to be injected deep enough yet not damaging the device. This depends on the device structure, namely on the thickness of the top layer, the needle should not go through this layer completely. On the other hand, if an oxide layer has formed on top of the device, needle has to be inserted deeper that this oxide layer. This range often falls within 10 to 100 µm.

The probes need to penetrate the package and reach the terminals of the device. This requires special needles that are sharp enough to pierce the package and make a good electrical contact with the device. A seemingly simple task of connecting the probes to the DUT can cause extra complications, too. Probe needles need to be properly attached with device's channels providing a stable connection; in practice this means that the DUT needs to be scratched during every measurement. Changing the needles is not a simple task, as it involves removing the old needles, inserting the new ones, aligning them with the microscope, and calibrating them. It takes time and practice to perform this task without damaging the needle or the device, which is treachery taking into account the very small physical dimensions of the transistors.

Imperfect connection leads to inconsistent results, creating voltage and current peaks or other deviations during the measurement. No such problem occurs when the DUT is soldered directly onto a test board.

5.3.2 Software configuration

One of the additional tasks in obtaining Id-Vg curves using a curve tracer is fine tuning the results with the software. Among other parameters affecting the results is the integration time of the data. The default value of 2 µs gives a noisy outcome, as shown in Figure 25 where small peaks are visible at many data points.

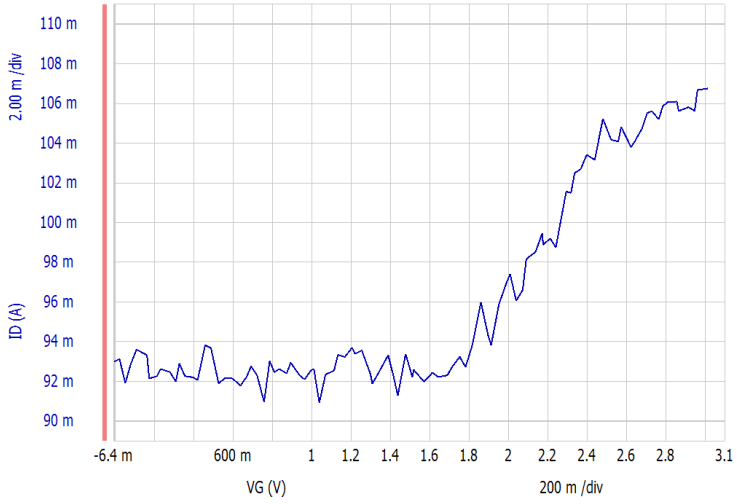
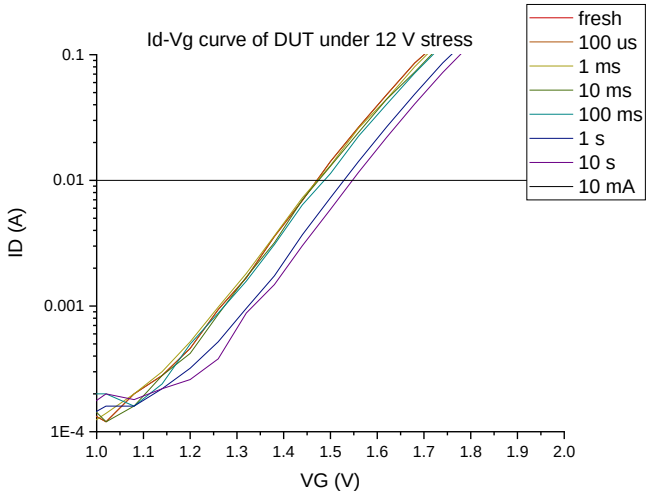


Figure 25. Id-Vg curve using the default 2 µs integration time. With this default value, the results are noisy (i.e. subject to small peaks at many data points).

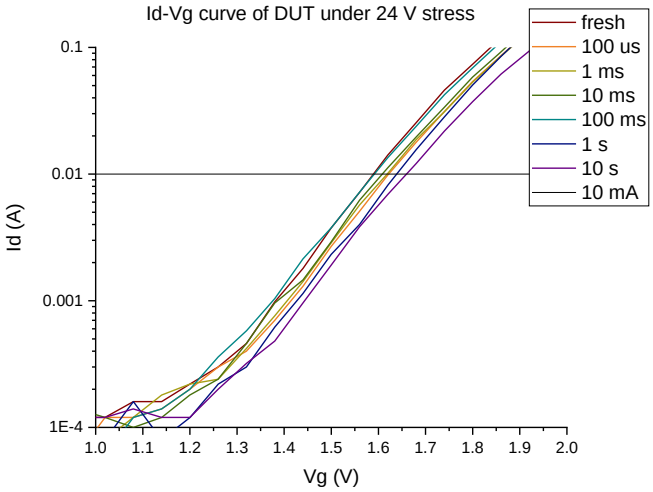
To improve the results integration, the time was increased up to 100 µs which enabled to get a smooth curve. Note, however, that selecting the integration time is a trade-off and increasing it too much may affect the results' precision and accuracy by approximating the value. Increasing the integration time too much might lead to a loss of precision. If the integration time is excessively long, the measured values may become less consistent or reproducible. At the same time, if the integration time is set too high, it could potentially impact the accuracy of the measurements. Excessive integration time might lead to an averaging effect, causing the measured values to deviate from the true characteristics of the device.

5.3.3 Effect of the order in which the measurements are taken

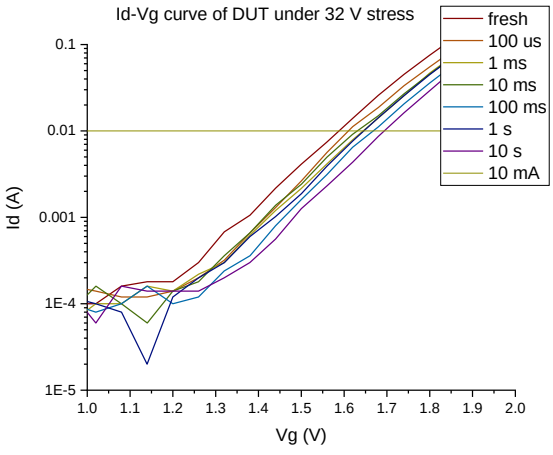
When the DUT was forced under the OFF-state and drain stress voltage sequences of 12, 24 and 32 V with relatively short rest period (5 to 10 minutes) between the measurements were applied, the initial threshold voltage shift occurred. This can be seen in Figure 26, i.e. the first test was performed on a freshly manufactured device with 12 V stress voltage and the threshold voltage value is below 1.5 V. During the next measurement that was conducted shortly after its "fresh" value, the threshold voltage has already shifted and is now above 1.5 V. The threshold voltage shifts even further during the 32 V stress measurement. It was empirically found that the DUT needs to rest for 15-20 minutes after a 12 V measurement and for 30 minutes after a 24 V measurement.



a)



b)



c)

Figure 26. Id-Vg curves of the DUT with 10 mA intersect zoomed-in in the conduction region with stress voltages of a) 12 V, b) 24 v, and c) 32 V. Although the measurements with different pulses durations are conducted with short rest period (5 to 10 minutes) in between, threshold voltage shift is clearly visible.

Threshold voltage results from the first data set when the device was forced under increasing OFF-state stress voltage is shown in Figure 27. There is an obvious positive shift for 24 and 32 V stress voltage results as compared to 12 V stress voltage.

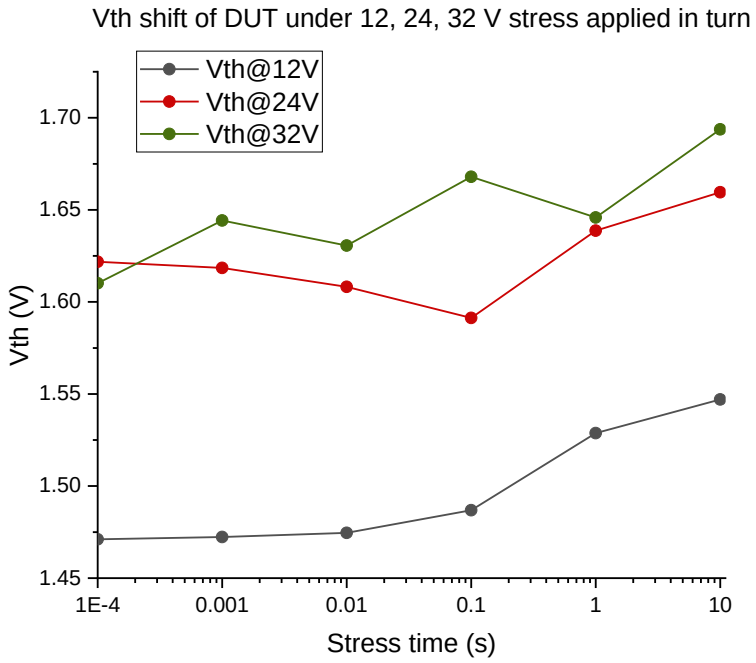


Figure 27. Vth shift results when increasing stress voltage levels are applied (12 V, 24 V, 32 V), with visible shift of a fresh value.

This problem of threshold voltage shift is overcome in the circuit-level measurement by pulling the transistor's drain to zero.

5.4 Proposed procedure for device-level measurement

The proposed procedure described below is based on the procedure for finding the threshold voltage with a probe station presented in Chapter 3 and aims to deal with the limitations discovered during the work on obtaining data for this thesis.

5.4.1 Preparation

1. Select source monitor units based on current or voltage ratings is needed to use based on the data provided by the manufacturer (Figure 28 [47]). The use of an appropriate module ensures reproducibility of the measurement.

Assemble the curve tracer and additional modules set-up as shown in Figure 15 (see Chapter 4).

Part number	Description	Slots occupied	Range of operation	Measure resolution
B1510A	High Power Source Monitor Unit (HPSMU)	2	-200 V to 200 V, -1 A to 1 A	2 µV, 10 fA
B1511B	Medium Power Source Monitor Unit (MPSMU)	1	-100 V to 100 V, -100 mA to 100 mA	0.5 µV, 10 fA
B1512A	High Current Source Monitor Unit (HCSMU)	2	-40 V to 40 V, -1 A to 1 A -20 V to 20 V, -20 A to 20 A (Pulse only)	200 nV, 10 pA
B1513C	High Voltage Source Monitor Unit (HVSMU)	2	-3000 V to 3000 V, -4 mA to 4 mA -1500 V to 1500 V, -8 mA to 8 mA	200 µV, 10 fA
B1514A	Medium Current Source Monitor Unit (MCSMU)	1	-30 V to 30 V, -100 mA to 100 mA -30 V to 30 V, -1 A to 1 A (Pulse only)	200 nV, 10 pA
B1520A [1]	Multi Frequency Capacitance Measurement Unit (MFCMU)	1	1 kHz to 5 MHz	

1. N1300A-100 SMU CMU Unify Unit (SCUU) is not supported for the B1505A.

Figure 28. Range of operation for SMUs for the B1505A [47].

2. Attach the needles to each probe; for packaged device characterisation use thicker needles (at least 20 µm thickness at the tip).
3. Calibrate the curve tracer using EasyExpert software. This ensures the measurement is consistent across the experiment.
4. Connect the needles with the DUT by slightly inserting them into the solder bar or into the channels' surface directly. High Force and High Source probe tips should be connected to the same drain terminal and Low Force and Low Source – to the same source terminal, and the single Gate probe should be connected to the gate.

   Note that this step is critical for the outcome of the measurements, make sure the device is slightly scratched to ensure proper needle-device connection but do not push the needle too strong to avoid the needle to bend or break or to damage the device.
5. Configure the software. Create a measurement setup for I-V measurement, make sure to choose proper SMUs for assigned channels and select whether you want to manipulate voltage or current, choose Vd to be constant value and Vg to vary from zero till saturation value. And a setup of the OFF-state stress with Vd kept constant for the time duration of stress and Vg kept at zero.

5.4.2 Experiment

6. Make test I-V measurement of the rested or freshly manufactured device, use log scale for the plot, adjust the integration time if needed so that the graph is as smooth as possible (this may take several iterations).
7. Run the stress-measurement sequence and record the data.
8. Make sure to let the DUT rest for a long enough time between the different measurement sets; this rest time has to be determined experimentally by observing and recording how much rest time is needed between initial measurements so that the threshold voltage shift is no longer visible.

5.4.3 Data processing

9. Use the software of your choice to display all graphs on the same plot, find intersect with the chosen constant value. To choose the intersect value, aim for the lowest possible Id value in the transition region of the device. Generally, this value should be 1 or 2 orders of magnitude above the OFF state noise level.

This chapter has presented a comparison of the device-level and circuit-level threshold voltage measurements results. The device-level results are valid; however, the data obtained by using the previously published circuit are shown to be more consistent when compared to the new data obtained at the device-level. Then, probe-station measurement's advantages and limitations were discussed, highlighting that its main limitations are the high cost of the setup, limitations in pulse duration of the stress voltage signal, and lack of ease of use. Finally, a procedure was proposed to decrease the effects of these limitations.

The next chapter summarizes the work presented in this thesis and presents suggestions for the future work.

6 Conclusion

6.1 Summary

The main goals of this master's thesis work were 1) to conduct extensive threshold voltage measurements at the device-level to verify and compare the results with those obtained at the circuit-level via the board designed by the ICST at NYCU; 2) identify the practical advantages and limitations of using a probe station and curve tracer to analyse packaged device threshold voltage instability, and 3) to propose a procedure for conducting threshold voltage measurement at the device-level.

The first step to achieve the above-mentioned goals was to conduct a background review in GaN material properties and GaN HEMTs themselves. Benefits and reliability issues of GaN semiconductor technology were studied with a special attention paid to threshold voltage instability of devices, especially the voltage shift caused by OFF-state drain stress.

Then, the state of the art of threshold voltage methods and techniques were reviewed and the circuit-level board presented and demonstrated to overcome existing limitations in threshold voltage measurements such as not short enough stress pulse, high cost of the setup, and complexity of use.

The next step was to review the state of the art threshold voltage extraction techniques that were further applied to the data obtained by the probe station measurements in order to increase the outcome results quality.

The experimental part of the work started with obtaining the Id-Vg curves of the device under 12, 24 and 32 V stress voltages with stress pulse duration of 100 μs, 1 ms, 10 ms, 100 ms, 1s and 10 s. The results were then processed and the threshold voltage values were extracted using the three previously presented methods and compared. The results obtained using the constant current method showed to be the most consistent (i.e. increasing threshold voltage values with increasing stress time, and threshold voltage closest to the expected typical value (deviation between +0.130 V and +0.547 V), and at the same time the least time consuming; it was therefore selected for the next measurements.

The device-level results were then compared with the results obtained by the measurement circuit-level board and it was shown that the device-level values were valid albeit at the same time showing to have more errors (fresh device threshold voltage deviation starting from 10%) when compared to the circuit-level values (deviation of a Vth of a fresh device from the typical value is around 5%).

The next step provided a detailed discussion of the device-level measurements advantages and limitations, showing that using the probe-station to get threshold voltage shift of the packaged device is a complex and time-consuming task requiring costly setup and the peculiarities of using a probe station and a curve tracer such as data processing and need to use the needles to probe the device leads to errors in the data and to introducing mechanical damages to the device. Finally, a procedure for probe-station measurements was proposed to deal with the discovered practical limitations.

All in all, it is deemed that the goals of this master thesis have been reached. The results achieved in this thesis pave the way for further work, as discussed in what follows.

6.2 Future work

For the probe-station measurement approach: continue to further refine and improve the procedure to improve the consistency and reliability of the results and contribute towards the standardization of the measurement procedure, making sure that experiment is both repeatable and reproducible. Another step can be made towards standardization of the Vth extraction using constant current method and defining the proper I_d value for GaN HEMTs.

For the circuit: the circuit can be further improved by adding the dynamic on-resistance measurement features since it is another instability in GaN HEMTs affecting their reliability; circuit can be adopted to perform the measurements on high voltage DUTs contributing to GaN development in power electronics.

Regarding the Vth properties, several issues could be further investigated, including studying how the threshold voltage changes at different temperature levels and under different stress conditions, as well as estimating the recovery time of the device after the stress is removed and the trap density of the defects that cause the threshold voltage instability.

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