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# Quasi-Z-Source Based String Inverter for Residential Photovoltaic Application

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**Declaration:**
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for doctoral or equivalent academic degree.

Elena Santasheva
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# Kvaasi-impedants tüüpi allikaga muundur kodumajapidamistes kasutatavatele päikesepaneelidele

ELENA SANTASHEVA

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# Contents

## List of Publications

The list of author's publications, on the basis of which the thesis has been prepared:

[PAPER-I] J. Zakis, E. Makovenko, H. Zeng, O. Husev, L. Kutt, "qZSI as Synchronverter in Small Scaled Mico-Grid", *Elektronika ir Elektrotechnika (IF-1.088)*, pp. 58-62, 2017.

[PAPER-II] E. Makovenko, O. Husev, D. Vinnikov, K. Tytelmaier, C. Roncero-Clemente, E. Romero-Cadaval, S. Bayhan, Y. Liu, "Novel quasi-Z-source derived inverter with unfolding circuit and battery storage", IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), pp. 1-6, 2018.

[PAPER-III] E. Makovenko, O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, F. Blaabjerg, "Single-phase 3L PR controlled qZS inverter connected to the distorted grid", 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2016), pp. 234-239, 2016.

[PAPER-IV] E. Makovenko, O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, "Three-level single-phase quasi-Z source inverter with active power decoupling circuit", 18th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM), pp. 497-502, 2017.

[PAPER-V] E. Makovenko, O. Husev, J. Zakis, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, "Passive power decoupling approach for three-level single-phase impedance Source Inverter based on resonant and PID controllers", 11th IEEE International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2017), pp. 516-521, 2017.

[PAPER-VI] E. Makovenko, O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, "A Single-Phase 3L qZS Inverter Connected to the Distorted Grid with Battery Storage and Active Power Decoupling Function", IEEE 59th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), pp. x-x, 2018.

[PAPER-VII] O. Husev, E. Makovenko, D. Vinnikov, T. Jalakas, C. Roncero-Clemente, E.Romero-Cadaval, J. F. Martins, V. Delgado-Gomes, V. Fernão Pires, "Single-phase qZS-based PV inverter with integrated battery storage for distributed energy generation", IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), pp. 1-6, 2018.

[PAPER-VIII] O. Husev, C. Roncero-Clemente, E. Makovenko, E. Romero-Cadaval, D. Vinnikov, "Optimization and Digital Implementation of the Proportional-Resonant Controller for Grid-Connected Inverter", *Transactions in Industrial Electronics (IF-7.05), pp. 1-10, 2019.*

## Author's Contribution to the Publications

[PAPER-I] Elena Makovenko is co-author of the paper, responsible for the simulation study of the converter in PSCAD, for the literature review.

[PAPER-II] Elena Makovenko is the first author of the paper, synthesized for converter algorithm, responsible for literature review, for simulation study of the converter in PSCAD. She presented the paper at 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Doha, Qatar.

[PAPER-III] Elena Makovenko is the first author of the paper, responsible for the mathematical tune up process of the controllers in Maple, for the simulation results in PSIM, for literature review. She presented the paper at 2016 IEEE 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Bydgoszcz, Poland.

[PAPER-IV] Elena Makovenko is the first author of the paper, responsible for the developed control system, for the mathematical calculations, for the simulation study of the converter in PSCAD, for literature review. She presented the paper at 2017 IEEE 18th International Conference of Young Specialists on Micro/Nanotechnologies and Electron Devices (EDM), Altai, Russia.

[PAPER-V] Elena Makovenko is co-author of the paper, responsible for the developed control system, for the mathematical calculations, for the simulation study of the converter in PSCAD, for literature review.

[PAPER-VI] Elena Makovenko is a first author of the paper, responsible for the tune up process of the control system in Maple, for the simulation study of the converter in PSCAD, for literature review. She presented the paper at 2018 IEEE 59th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), Riga, Latvia.

[PAPER-VII] Elena Makovenko is co-author of the paper, responsible for control system tuning and preliminary simulation verification.

[PAPER-VIII] Elena Makovenko is co-author of the paper, responsible for for mathematical analysis and the simulation study of the converter in PSCAD.

## Abbreviations

| | |
|---|---|
| VSI | Voltage - Source Inverter |
| CSI | Current - Source Inverter |
| PV | Photovoltaic |
| PVs | Photovoltaic Systems |
| PEC | Power Electronic Converter |
| NPC | Neutral - Point Clamped |
| qZSI | quasi - Z Source Inverter |
| RES | Renewable Energy Source |
| DFR | Double Frequency Ripple |
| APD | Active Power Decoupling |
| PPD | Passive Power Decoupling |
| DDFR | Double Damped Frequency Ripple |
| PDN | Passive Distribution Network |
| ADN | Active Distribution Network |
| CCM | Continuous Current Mode |
| DCM | Discontinuous Current Mode |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| PWM | Pulse Width Modulation |
| AC | Alternative Current |
| DC | Direct Current |
| EMI | Electromagnetic Interference |
| DGS | Distribution Generation System |
| IEEE | Institute of Electrical and Electronics Engineers |
| IEC | International Electrotechnical Commission |
| IS | Impedance Source |
| ISN | Impedance Source Network |
| ISNs | Impedance Source Networks |
| MPPT | Maximum Power Point Tracking |
| qZSN | quasi – Z - Source Network |
| ST | Shoot - Through |
| CIC | Continuous Input Current |
| DIC | Discontinuous Input Current |
| PF | Power Factor |
| FOC | Field Oriented Control |
| VOC | Voltage Oriented Control |
| DTC | Direct Torque Control |
| DPC | Direct Power Control |
| SVM | Space Vector Modulation |
| SPVWM | Space Vector Pulse Width Modulation |
| PI | Proportional Integer |
| PR | Proportional Resonant |
| dPR | damped Proportional Resonant |
| HC | Harmonic Compensation |
| MPC | Model Predictive Control |
| qZS | quasi - Z - Source |
| RESs | Renewable Energy Source system |
| PID | Proportional Integer Derivative |
| E-cap | Electrolytic capacitor |
| ESRs | Equivalent Series Resistors |

| | |
|---|---|
| dPR | damped Proportional Resonant |
| MPP | Maximum Power Point |
| AD | Analog Digital |
| FPGA | Field-Programmable Gate Array |
| DSP | Digital Signal Processor |
| PLL | Phase Locked Loop |
| SOGI | Second Order Generalized Integrator |
| LPF | Low Pass Filter |
| BIC | Battery Interface Converter |
| SPI | Serial Peripheral Interface |

## Symbols

| | |
|---|---|
| *C1- C4* | capacitors of the qZSN |
| *L1- L4* | inductors of the qZSN |
| $C_B$ | buffer capacitor |
| $L_B$ | buffer inductor |
| *Bat* | battery of the battery interface converter |
| $D_{01}$-$D_{04}$ | blocking diodes |
| $D_1$, $D_2$ | diodes of the qZSN |
| *Li* | inductor of the inverter side filter |
| *Lg* | inductor of the grid side filter |
| *Cf* | filter capacitor |
| *Rfi, Rfg, Rd* | parasitic resistances |
| *Ds* | shoot-through duty cycle |
| *Da* | active state duty cycle |
| *S1-S8* | inverter switches |
| *T1, T2* | switches of the battery interface converter |
| *Cout* | output capacitor in unfolding circuit |
| *Lout* | output inductor in unfolding circuit |
| *Rout* | output resistor in unfolding circuit |
| *Pin* | input power |
| *Pg* | grid power |
| *Vin* | input voltage |
| *Vg* | grid voltage |
| *Iin* | input current |
| *Ig* | grid current |
| *Ibat* | battery current |
| *Ib* | current across active power decoupling circuit |
| *Ds* | shoot - through duty cycle |
| *Da* | active duty cycle |
| *Vdc* | dc-link voltage |
| *Vc* | voltage across capacitors C2+C3 |
| *T* | line period |
| *tsw* | switching period |
| *ton* | ON - state time duration |
| *toff* | OFF - state time duration |
| *fsw* | switching frequency |
| $T_{sw}$ | switching period |
| $E_{LW}$ | energy stored in the inductors |
| $E_{CW}$ | energy stored in the capacitors |
| $T_W$ | total voltage stress on the switching devices |
| *Vmax* | maximum voltage across capacitors |
| *Iave* | average current across inductors |
| $v_L$ | instantaneous voltage across inductor |
| $v_C$ | instantaneous voltage across capacitor |
| $V_T$ | reverse voltage on the semiconductor devices |
| $i_L$ | instantaneous current across inductor |
| $i_C$ | instantaneous current across capacitor |

| | |
|---|---|
| $i_{S0}$ | instantaneous current across intermediate switch |
| $i_{out}$ | instantaneous output current |
| $v_{out}$ | instantaneous output voltage |
| $K_{C1}$, $K_{C2}$, $K_{CB}$ | ripple coefficient of voltage across capacitors $C_1$, $C_2$, $C_B$ |
| $K_{L1}$, $K_{L2}$, $K_{LB}$ | ripple coefficient of current across inductors $L_1$, $L_2$, $L_B$ |
| *Cu* | capacitor in an equivalent unit |
| *Lu* | inductance in an equivalent unit |
| *L* | output inductor |
| *C* | output capacitor |
| *R* | load resistance |
| $\omega$ | line frequency |
| $\omega c$ | cut-off frequency |
| $\varphi$ | phase shift |
| *TrF* | transfer function |
| *G* | transfer function |
| *Isc* | shoot-through current |
| *Immp* | current at the MPP |
| *Voc* | open circuit voltage |
| *Vmpp* | voltage at the MPP |
| *Empp* | efficiency of the MPPT block |
| *Econv* | efficiency of the converter |
| *E%* | solar irradiance in percentage from nominal value |

# 1 Introduction

## 1.1 Definitions of the residential PV Inverter

Today we can observe how the power plants are shifting from being centralized power grid to becoming decentralized power grid/micro-grid due to the rising interest in the Renewable Energy Sources (RES), where the Photovoltaic Systems (PVs) are the most promising among RESs. A typical centralized power grid consists of:

- centralized generator (powerful synchronous generator) that sets the frequency of the grid and equals 50 Hz or 60 Hz, and the voltage of the grid, rms value equals 230 V. It is characterized as steady and dispatchable, including inertia, speed governing, excitation control [1],[2];
- transmission network that transfers the electricity from the centralized generator to a substation where the voltage of the electricity is decreased;
- distribution network delivers the electricity to the consumers/load;
- distribution generator is an additional power plant that produces power; it is usually located near the consumers/load. It can be connected to the distribution network or to the load in stand-alone mode. It could be the synchronous generator of smaller in size than the centralized generator or RES. The RES is characterized as variable, non-dispatchable, inverter-based, distributed;
- consumers/load.

The shift from being centralized to becoming a decentralized power grid is motivated by the fact that the electricity power socket is overloaded with too many plugs and in order to sustain the power supply, making just some upgrades could be more expensive than the creation of a new, independent from the fuel cell, a decentralized power grid, which can also be more cost effective [3].

The string technology is a demanded solution where high power/voltage of the PVs is required, such as residential application. But since the PVs are characterized as a time-varying source due to their intermittent nature of the power production, this common Photovoltaic (PV) issue is crucial, because it depends on the temperature, solar irradiance, and the PVs do not produce the power during the night period. One of the major drawbacks of the string technology lies in its poor energy utilization at partial shadowing, where it can lead to the power fluctuation in the Distributed Generation System (DGS). Earlier when the penetration level of the RES into the DGS was not so high, its effect on the stability of the parameters of the grid was not critical because their capacities were significantly lower than the capacity of the central generator. So the shift is motivated also by the fact that the increasing level of the penetration of the RESs into DGS was starting to cause the instability of the grid, and the centralized generator was incapable of providing the stability of the system anymore. The decentralized power grid can consist of:

- distribution generator (micro turbine generator and RES);
- distribution network;
- energy storage;
- consumers/load.

The residential micro-grid may consist of one house, where the power produced by the PVs would be spent for its own needs, or of few houses in which case the community may share the produced power between each other or transfer the surplus of power to the main grid. One of the examples of such grids was built in the Netherlands, “The Aardehuizen: a neighbourhood microgrid” [3].

In order to connect the DC power produced by PVs and the ac sources or ac load, it is necessary to use a Power Electronic Converter (PEC), a residential PV inverter, as an interface inverter in a residential micro-grid. Earlier the PEC operated as a Passive Distributor Network (PDN) that could not provide the support of the grid. It only could inject the current into the grid with THD lower than 5%, which had to be synchronized with the grid voltage. However, high penetration level of the RES into DGS in the centralized power grid and the creation of the decentralized power grid led to the necessity to expand the functions of the PEC. In 2013, the Institute of Electrical and Electronics Engineering (IEEE) 1547 and International Electrotechnical Commission (IEC) 50438 were revised and the interface inverter was considered as an Active Distributor Network (ADN). The ADN with a wider function can provide the frequency/voltage support of the grid. The review of the updated standards is presented in Chapter 2.

As stated earlier, the PVs produce unstable voltage, which forces to use the boost stage. In the industry, the traditional DC-DC boost converter was used. The Voltage Source Inverter (VSI) or Current Source Inverter (CSI) with a boost DC-DC converter cannot provide more than twice higher input voltage regulation ratio and this solution is topologically more complex and harder to control, because of the two-stage power conversion. One of the alternative approaches is based on an intermediate Impedance-Source Network (ISN) [1]-[3]. The ISN provides Shoot-Through (ST) immunity that makes the control strategy simpler, since there is no need to introduce dead-time and it can operate in a buck, and in a boost mode. These inverters based on the ISN are capable of performing Maximum Power Point Tracking (MPPT) with no need for using an auxiliary or extra DC-DC converter. Different types of the ISN have been proposed, such as the Trans-source[4],[5], Y-source [6],[7], EZ-source containing the coupled inductors within[8], [9] and the LCCT-Z-source[10]-[12], Γ-Z-source that contains the transformer within[13],[14] in the literature so far. In [15] authors present the brief review of the different configurations of the impedance networks. Not all of the proposed ISN are suitable for PV application because they provide Discontinuous Input Current (DIC) such as: Z –source [16], Trans-Z –source, LCCT-Z - source, Y-source, Γ-Z-source. Among the ISN which provides the Continuous Input Current (CIC) the quasi-Z-Source Network (qZSN) looks more attractive for PV application because it provides lower input current ripple in comparison to the: EZ – source, Trans-quasi-Z – source[17], and it contains a lower number of the passive elements than LCCT-quasi-Z source network [18].

One of the possible decentralized power grids is presented in [PAPER-I] where the decentralized system contains a small synchronous generator and a few different types of the RES, but the grid fault had occurred and the rest part of the decentralized power grid started to operate in a stand-alone mode. In this system, the PECs were connected in parallel and at the grid fault, one of the PEC that had higher capacity than others was able to change its operation mode from the CSI to the VSI and mimic the behavior of the absent synchronous generator, and started to set the frequency and voltage of the grid based on the load demands. Other PECs in the stand-alone mode kept operating in a normal mode; moreover, they could provide the support of the virtual synchronous

generator in the case of a change in the load demand by means of the droop control that is a new available function accepted by updated standards. The droop control is a function that allows us to maintain the voltage and frequency of the grid parameters by changing the active and reactive power production.

Since the load power can fluctuate during the day in a residential micro-grid, and the PV system produces non-stable power value during the day, it is mandatory to use the battery as part of the whole system in order to achieve the power balance.

The residential PV inverter is a small scale power generator which has the power capacity of up to 5 kW [18]. It should be able to regulate input voltage in a wide range which means that it should consist of some boost stage. It should provide CIC and the required quality of the produced current. In order to improve the efficiency of the MPPT block, it should be able to reduce the DFR of the input power and provide power balance between the produced power and the required power by the load by means of the battery integration.

Currently, the research of quasi-Z-source inverters (qZSI) showing their application for residential application is very limited.

The main goal of this work is to optimize the performance of the novel solar inverter based on the quasi-Z-source network with energy storage utilization making it suitable for residential application. The optimization is concerned with optimal control strategies along with passive components size and volume reduction keeping predefined power quality and level of MPPT performance.

## 1.2 Hypothesis and Tasks

The aim of the PhD research is to design and experimentally validate a single-phase qZSI with storage integration to be applied for residential application.

**Hypothesis:**

- The usage of the three-level NPC inverter allows us to improve the quality of the power at the PCC, whereas reducing the voltage stress on the semiconductor devices allows the use of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) transistors with increased frequency;
- The qZS network allows an increase of the input voltage up to the required level on the dc-link and maintain it in a wide range of the input voltage;
- The interface storage converter allows us to provide the power balance between the input and the output sides and even to feed the consumers/load in the case of the absence of the power produced by PV panels;
- To mitigate the double-frequency ripple of the input power the Active Power Decoupling (APD) approach is a better solution in comparison with the Passive Power Decoupling (PPD) approach.

**Tasks:**

- To overview and select the topology of a DC-AC converter that is able to provide a wide range of input voltage regulation along with the capability of battery storage integration;
- To estimate the best decouping approach which ables to mitigate double-frequency ripple of input power taking into account overall power density, overall efficiency and cost;

- To design and improve the grid-connection and battery control strategies for an DC-AC converter with battery storage utilization, a wide range of power and input voltage regulation in terms of stability and power quality at the PCC;
- To verify the developed solution of a solar inverter with battery storage utilization for residential application.

## 1.3 Scientific Novelties

- New quasi-Z-source based inverter with storage energy integration and unfolding circuit;
- New modified three-level NPC quasi-Z-source inverter with combined storage integration and active decoupling capability;
- Novel tuning approach of the proportional-resonant controller for grid current control strategy with optimized start up transient;
- Comparative analysis of the passive and active power decoupling approach for double-frequency ripple elimination in ISN based converters.

## 1.4 Practical Outcomes

- Design guidelines for the decoupling approach, its goal is to reduce the DFR of input power and improve the MPPT performance;
- Mathematical guidelines to tune up the applied controllers;
- Design guidelines to optimize the damped Proportional Resonant (dPR);
- Experimental prototype of a single-phase ISN based solar inverter.

## 1.5 Confirmation and Dissemination of Results

The results of the doctoral thesis have been disseminated at 6 international conferences, at 7 doctoral schools and 2 scientific journals.

The author has published 12 international scientific papers indexed by IEEE Explore, 8 of them associated with the doctoral thesis. The most important papers directly connected to the topic of the dissertation are listed in the Appendix.

# 2 State-of-the-art of residential string inverters

This chapter gives an overview of the standards of the residential grid-connected PV inverters, which change over time, new functions added due to the high penetration level of the RES into DGS. Also, it reviews different control strategies of the grid connected inverters where the main tasks are to provide the required quality of the grid current even if the grid voltage is distorted, provide fast dynamic response and zero steady-state error. Final goal is to describe power electronics topologies that can be applied for residential PV application, where the most important issue is to provide the regulation of the input voltage in a wide range and to provide CIC.

## 2.1 Overview of existed standards and requirements

Different countries are applying different standards. The IEC 50438[19] standard is being applied in European countries such as Estonia and Spain, while the IEEE 1547 standards and Rule 21 [1], [2] were designed for the USA. The main differences between these two territories are the parameters of the grid. The reference voltage is 240 V and the frequency is 60 Hz in the USA, while in Europe it is 230 V and 50 Hz correspondingly.

The IEC 50438 standard dates back to 2013, since that time, it has been revised and some changes have been introduced in order to improve the reliability, safety, stability of the grid, the power quality, and control over generation, and storage capabilities, taking into account more specific features of the cooperation between the RES and the DGS. For instance, the tests for verification of interface protection, islanding detection have been modified; the test of the direct current injection has been added [1] and new functions were added, such as:

- Voltage/Frequency Ride Through. The mentioned standards set clearing time and voltage/frequency deviation from the nominal value in the DGS; during that time, the inverter may stay connected to the grid, but if the anomaly exceeds the clearing time or available voltage/frequency deviation, the inverter should be disconnected. The available voltage/frequency deviation and clearing time are presented in TABLE 1.
- Dynamic Volt/VAr control regulates the voltage fluctuation by injecting or absorbing the reactive power into DGS, Figure 1 between points 1 and 4. The PVs or/and load change can cause the voltage fluctuation in the DGS. If the voltage fluctuations are higher than it is set in Table 1 (Points 1 and 4 in the Figure 2.1), the RES should be disconnected. The Volta/VAr curve can include the deadband or not.

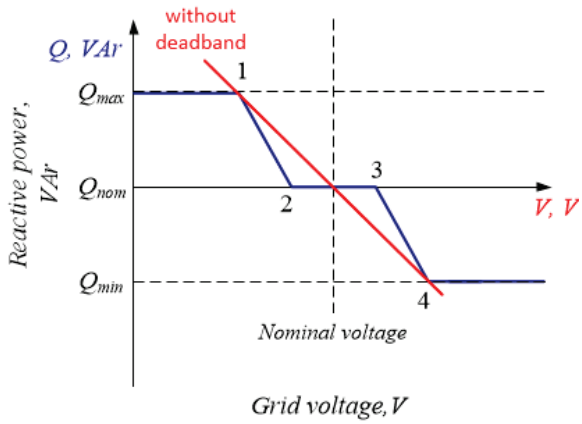



*Figure 2.1 Volt/VAr curves.*

- Dynamic Freq/Watt control regulates the frequency deviation. The load change may cause the frequency deviation in the DGS. The PEC can provide the frequency support of the DGS by regulating the active power production, between points 1-4 Figure 2. If the frequency fluctuations are higher than it is set in Table 2.1 (Points 1 and 4 in Figure 2.2), the RES should be disconnected. If the frequency deviation exceeds points 2 or 3, then the active power change rate should be equal to 10%/Hz. Without this control and at the over frequency, the inverter increases active power production that may deteriorate the parameters of the grid [20].

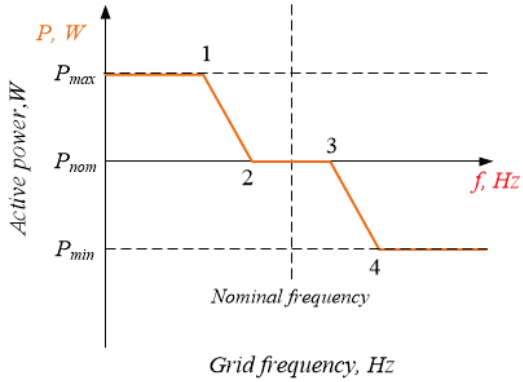



*Figure 2.2 Freq/Watt curve.*

- Ramp-up power rates. After disconnection when it comes to reconnect the RES to the DGS and if the reconnection is done simultaneously (Curve 1 in Figure 2.3), it may cause the large spike of the active power in the grid and the instability of the system or the frequency deviation. The suitable power rate slope should be set in order to smooth the transition process (Curve 2 in Figure 2.3). There is also another method that allows avoiding any negative subsequences of the reconnection of the RES into the DGS, which is to separate their reconnection time. This method is named as the ”Soft Start“. As a result, the reconnection process can be divided based on two types: ramp-up power rates and random switch within a time window. According to the IEC 50438 standard, in Estonia the RES may start the

reconnection process if during 1 minute the voltage range is between 85%-110% and the frequency range is between 47.5 Hz-50.05 Hz.

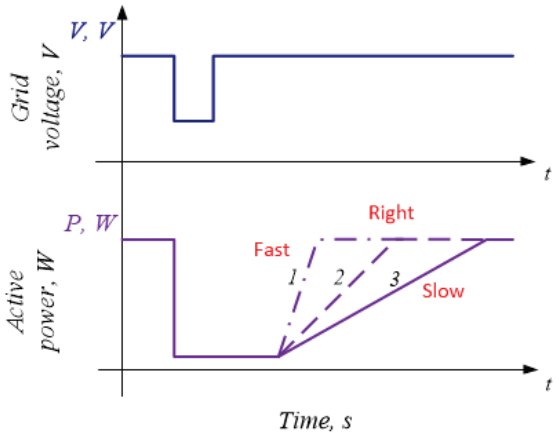



*Figure 2.3 Ramp-up power rates.*

- Non-Unity Power Factor (PF). Recent PV inverters operated with unity PF, which is unsuitable today because of different types of load that can introduce reactive power into the DGS and other various RES types that can change PF in DGS as well, and some shift may occur due to the large scale of feeder especially in the case of the high penetration level of RES into the DGS. To compensate their influence and improve the stability of DGS, it is required to vary the PF of the PV inverter to regulate voltage by injecting/absorbing the reactive power. Different studies have focused on the influence of different values of the PF [21]. In [22] authors performed an experimental comparison with lead and lag PF. Non-unity PF increased the losses across semiconductor devices of the PV inverter that reduced their lifetime. According to their results, it was more preferable to set the lag PF since it caused lower energy losses compared to lead PF. The approach proposed in [23] allows control of the flow of the reactive power into the system; their method was named the ”Q at Night“. In [24] authors report their experimental results where they changed the PF between 80% leading and 80% lagging, which caused a change in the reactive power without influencing the active power.

It is expected that wider functionalities allow more accurate response to a voltage and a frequency deviation of the grid. The islanding mode is not permitted nowadays due to the different interconnection challenges. In the future, this attractive function is expected to be integrated. Different studies are dedicated to this mode [25],[26],[PAPER-I]. The main idea is to connect few interface inverters in parallel that operate normally in the grid connected mode, for instance a CSI. But in the case of the islanding mode, one of the inverters starts to operate as a synchronous generator (VSI) and sets frequency and voltage based on the load demand. The droop control seems a reasonable solution for such systems.

As a conclusion, the residential PV inverter should be able to perform the following tasks [1]:

- Provide the Volt/Freq control;
- Correct work at the grid disturbance;
- Provide protection function;
- Provide the stability of the system;
- Provide the continuity of the service;
- Provide the interaction with the system [27].

From Table 2.1 it is clear that the PECs have different critical points in different countries. This means that the industrial PEC should be able to adapt for different countries by changing its critical points.

*Table 2.1 – Measured efficiencies and duty cycle values*

| Country/Standard | Parameter | tmin | tmax | Trip value |
|---|---|---|---|---|
| Estonia (IEC 50438) | Over voltage | -<br>0.1 s | 3 s<br>0.2 s | 230 V+10%<br>230 V+15% |
| Spain (IEC 50438) | | -<br>- | 1.5 s<br>0.2 s | 230 V+10%<br>230 V+15% |
| Denmark (IEC 50438) | | 0.1 s<br>39 s | 0.2 s<br>40 s | 230 V+13%<br>230 V+10% |
| IEEE 1547 | | -<br>- | 1 s<br>0.16 s | 240 V+10%<br>240 V+20% |
| Estonia (IEC 50438) | Under voltage | 1.2 s | 1.5 s | 230 V-15% |
| Spain (IEC 50438) | | - | 1.5 s | 230 V-15% |
| Denmark (IEC 50438) | | 9 s | 10 s | 230 V-10% |
| IEEE 1547 | | -<br>- | 0.16 s<br>2 s | 240 V-50%<br>240 V-12% |
| Estonia (IEC 50438) | Over frequency | 0.3 s | 0.5 s | 52 Hz |
| Spain (IEC 50438) | | - | 0.5 s | 50.5 Hz |
| Denmark | | 0.1 s | 0.2 s | 52 Hz |
| IEEE 1547 | | - | 0.16 s | 60.5 Hz |
| Estonia (IEC 50438) | Under frequency | 0.3 s | 0.5 s | 47.5 Hz |
| Spain (IEC 50438) | | - | 3 s | 48 Hz |
| Denmark (IEC 50438) | | 0.1 s | 0.2 s | 47.5 Hz |
| IEEE 1547 | | - | 0.16 s | 57 Hz |

## 2.2 Overview of different control strategies

Originally, most of the control techniques were developed for motor drives [28]-[31] and have been applied for grid-connected inverters with minor change of the names: Field Oriented Control (FOC) became Voltage Oriented Control (VOC), Direct Torque Control (DTC) became Direct Power Control (DPC), where the torque and the stator flux were replaced with an active and a reactive power of the grid-connected inverter [32], [28]. The main features of both control methods remained the same. Namely, the VOC is tightly related to the use of coordinate transformations for grid currents and voltages (abc to αβ, αβ to dq) and additional current control loop that provides fast transient

response and high static performance [32] - [34]. The block diagrams of the different control methods are presented in Figures 2.4, 2.5.

The DPC eliminates the current control loop, the conducting state of the converter's switches is defined based on the instantaneous values of the grid voltage space vector and the active and reactive power demand. This control method requires the higher sampling frequency and inherits the variable switching frequency, contrary to the VOC. As a result, DPC requires higher inductances and has a potential problem of the LCL filter resonance [35], [4].

The structure of the common inverter control scheme usually consists of two loops – the outer voltage control loop with slow dynamics responsible for the energy flow between the dc-link and the grid by generating the reference value for the current loop; and the inner current control loop with a fast dynamic responsible for the quality of the current waveform, the current protection. The implementation of the particular control structure depends on the reference frame that is divided into three groups: natural frame (abc), rotating frame (αβ) and synchronous reference frame (dq). The DPC performs the control of the active and reactive power directly and it has no Pulse Width Modulation (PWM) blocks opposite to the VOC methods. Typically, the DPC includes the Hysteresis control or Space Vector Modulation (SVM) or Space Vector Pulse Width Modulation (SPVWM) block with a voltage look up table. Table 2.2 presents the classification of the main current controllers. The PR controller provides theoretically infinite gain at the tuning frequency, which means that the steady state error is minimized. It can operate in the abc reference frame or in the $\alpha\beta$ reference frame, which means that there is no need to perform the transformation in comparison to the Proportional Integer (PI)[36] controller that requires the transformation of the reference frame, because it operates in the dq reference frame and it is more suitable to control the dc quantities. Proportional Resonant (PR) controller has a fixed switching frequency that makes this controller more attractive for application than the hysteresis controller although there are hysteresis controllers with fixed switching frequency [37]-[39]. The predictive deadbeat controller [40]-[42] has the following disadvantage: it is a delay that occurs due to the reference value of the next sample that will be known at the end of the modulation period. The MPD [43]-[47] inherits the unpredictable THD of the produced current that makes it complicated to design an output filter. The application of the PR controllers connected in parallel or Harmonic Compensation (HC) circuit [48]-[50] allows the control of the undesired order harmonics in the produced current even if the grid is distorted. The negative aspect of the PR controller can be related to its operating frequency, i.e., if the frequency of the grid is distorted, the performance of the PR controller could be significantly deteriorated. Different types of modulation techniques are described in [51].

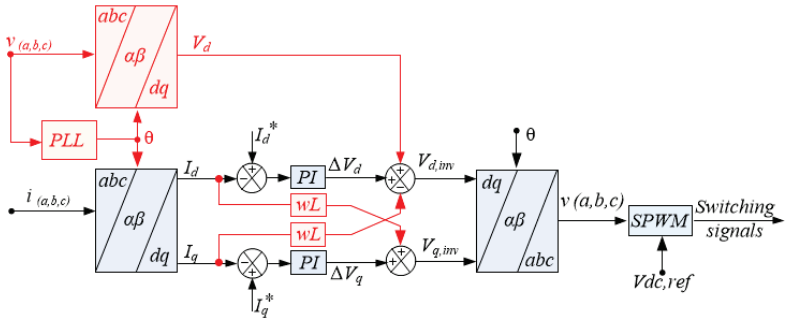



*Figure 2.4 Voltage oriented control based on the PI controller.*

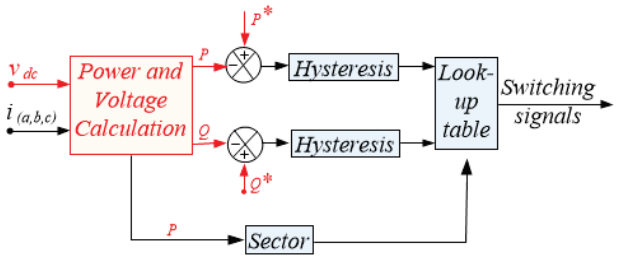



*Figure 2.5 Direct power control.*

*Table 2.2 – Classification of the control methods*

| **Control methods** | | **Type of the controller** | | | | | |
|---|---|---|---|---|---|---|---|
| | | PR | PID | RC | Hysteresis | MPC | DBC |
| Method | VOC | * | * | * | * | * | * |
| | DPC | | | | * | * | * |
| Reference frame | abc | * | | * | * | * | * |
| | αβ | * | | * | * | * | * |
| | dq | | * | | * | * | * |
| Linearity | Linear | * | * | * | | * | * |
| | Non-linear | | | | * | * | * |
| Number of loops | Single loop | * | | * | * | * | * |
| | Multi-loops | | * | | | * | * |
| Sensor | Sensor | * | * | * | * | * | * |
| | sensorless | | | | | | * |

## 2.3 Overview of power electronics transformer-less topologies

In [52], different configurations of PEC topologies for PV application are reviewed. The differences of the topology configurations depend on the following: with or without isolation step, internal or external MPPT block, power range, efficiency, with or without transformer, complexity of the design, with or without DC-DC converter.

The transformer-less PV inverters with the DC-DC converter are described in [53], [54] and without DC-DC converter in [55]-[57].

All the proposed transformer-less topologies, in general, can be expressed through two block diagrams, Figure 2.6*a,b*.

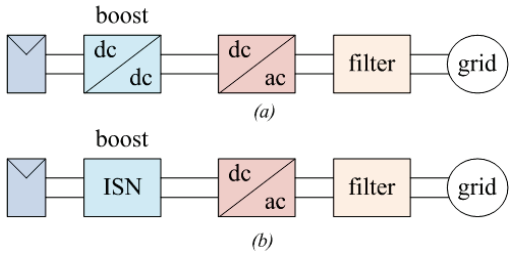



*Figure 2.6 Block diagram of the grid connected inverters; traditional approach (a), novel approach (b).*

The traditional approach, with the DC-DC converter, is widely used in the industry, Figure 2.6*a*. The DC-DC boost converter is used there to increase the PV voltage and to convert a Direct Current (DC) power into Alternative Current (AC), the full-bridge inverter is used. In 2002, Peng was the first to propose ISN, Z-source network, which allows regulation of the input voltage in a wide range, provides shoot-through (ST) immunity and allows combining two power conversation steps into one.

Figures 2.7*a,b* show two topologies of the PEC. The first topology, Figure 2.7*a*, shows the traditional concept with some modification and the second, Figure 2.7*b*, shows the novel concept that is based on the Z-source network.

The topology in Figure 2.7*a* looks attractive due to the three-level voltage *Vab* that leads to the improved quality of the produced current. This topology provides low input voltage regulation range due to the low boost factor B=1/(1-Ds) [58] in comparison to the ISN based converters. The topology in Figure 2.7*b* presents a novel approach based on the Z-source network. Since this topology consists of the Z-source network, it changes the input current discontinuous, i.e., the efficiency of the PVs is worse than that of the ISN, which provides CIC.

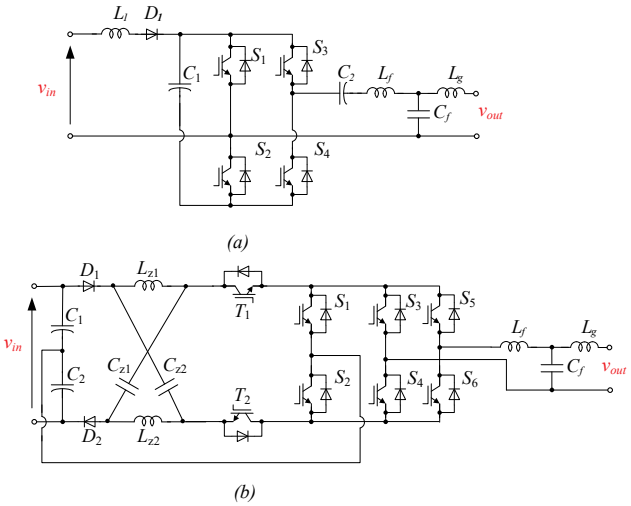



*Figure 2.7 A single-phase boost inverter with common ground for photovoltaic application [58] (a), single-phase Z-source three-level inverter [59] (b).*

## 2.4 Summary of Chapter 2

High penetration level of the RES to the DGS led to the revision of the standards for the grid-connected converters. Based on the new accepted functions the PEC now is considered as ADN. The same standard has different critical points for different High penetration level of the RES to the DGS led to the revision of the standards for the grid-connected converters. Based on the new accepted functions, now the PEC is considered as ADN. The same standard has different critical points for different countries, which means that the industrial converter should be able to integrate to the country where it is going to be located.

The control methods were introduced to power electronics from the motor drive theory with minor modification. The decision about the applied controllers is usually based on the power capacity of the control system, reference frame and the precision, knowing of the behavior of the system.

Researchers today show high interest in the opportunity to apply the PEC based on the ISN in the industry. The reason is that the ISN allows overcoming a set of limitations that the traditional DC-DC boost converter has, such as: ST duty cycle intolerance, low input voltage regulation range. The ISN allows combining two power conversion steps into one. At the same time, not all of the proposed ISN are suitable for residential PV applications due to the DIC that they provide.

# 3 Impedance-source based inverter with storage integration

This chapter addresses the string PV inverter topology. In the analysis, two new possible topologies of the string PV inverter for residential application will be considered. The traditional VSI requires an additional boost stage, the DC-DC boost converter, which would increase the time varying input voltage up to the required level in order to ensure the right direction of the power flow. Moreover, the traditional VSI requires integrating the dead time between switching of the transistor switches; in the opposite case, the ST state may occur, which is dangerous for the traditional VSI because unlimited currents start to flow through the ST circuit [16].

Chapter 1 presented a novel approach based on the ISN, which allows preventing some limitations of the traditional VSI. As stated above, not all ISNs are suitable for PV application while some ISN are. The Quasi-Z-Source Network (qZSN) is one of them. It provides CIC and is able to regulate the input voltage in a wide range; qZSN provides ST immunity that makes the control strategy simpler because there is no need to introduce dead-time.

For further consideration, the topologies based on the qZSN were selected.

## 3.1 Novel quazi-z-source derived inverter with unfolding circuit and battery storage integration

Firstly, a novel Quasi-Z-Source (qZS) derived inverter with unfolding circuit and battery storage integration was designed and investigated [PAPER-I] (Figure 3.1). The topology consists of the following components:

- qZS network *($L_1$, $L_2$, $C_1$, $C_2$)* to boost the input voltage;
- BIC*($T_1$, $T_2$, $L_b$, $C_b$, Bat)* to maintain the virtual dc-link voltage and to control the battery power flow;
- intermediate switching device $S_0$, which commutates under a non-fixed and a high switching frequency; the $S_0$ forms positive half-waves of the output signal;
- inverter circuit *($S_1$-$S_4$)* commutates under a low switching frequency and it forms the positive/negative waveforms of a sinusoidal output current;
- output circuit (*Cout, Lout, Rout*).

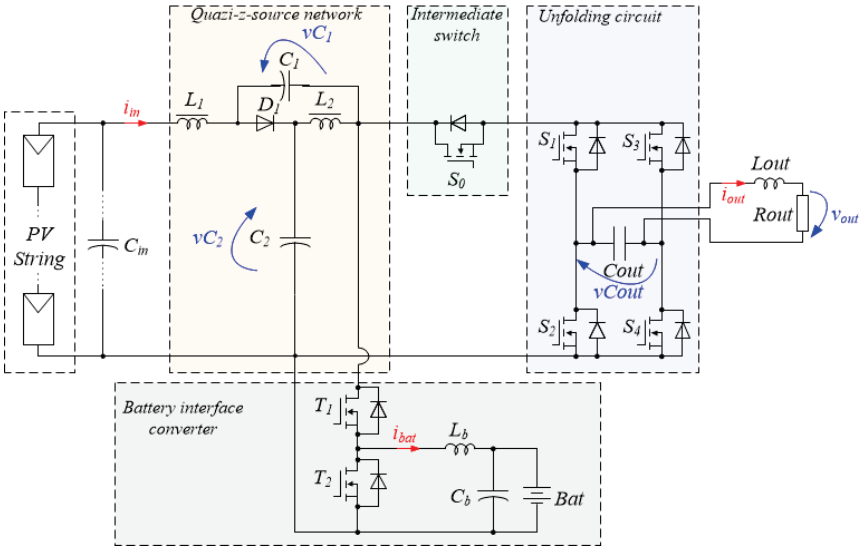



*Figure 3.1 Quasi-z-source derived inverter with unfolding circuit and battery storage integration [PAPER-I].*

Inverters based on the unfolding circuit[61]-[64] are attractive for their switching frequency of the inverter switches that equals to the line frequency, as a result, the switching losses of the inverter switches are negligible. At the same time, the unfolding circuits are known well to their produced shape of the voltage and current, which have some distortion near zero. It is caused by the uncertain state of the inverter's switches when the voltage reaches zero voltage.

### 3.1.1 Operation principle and steady state analysis

The operation principle basically can be divided into two operation modes: the formation of the positive half wave of the output signal and the negative. The difference between these two modes is in the switching states of the inverter switches, which commutate each half period. The time intervals within the modes are symmetrical and for that reason the consideration of only one of the operation modes is enough. Figure 3.2 shows the operation principle of the formation of the positive half wave of the output signal of the qZS derived inverter with unfolding circuit and battery storage integration.

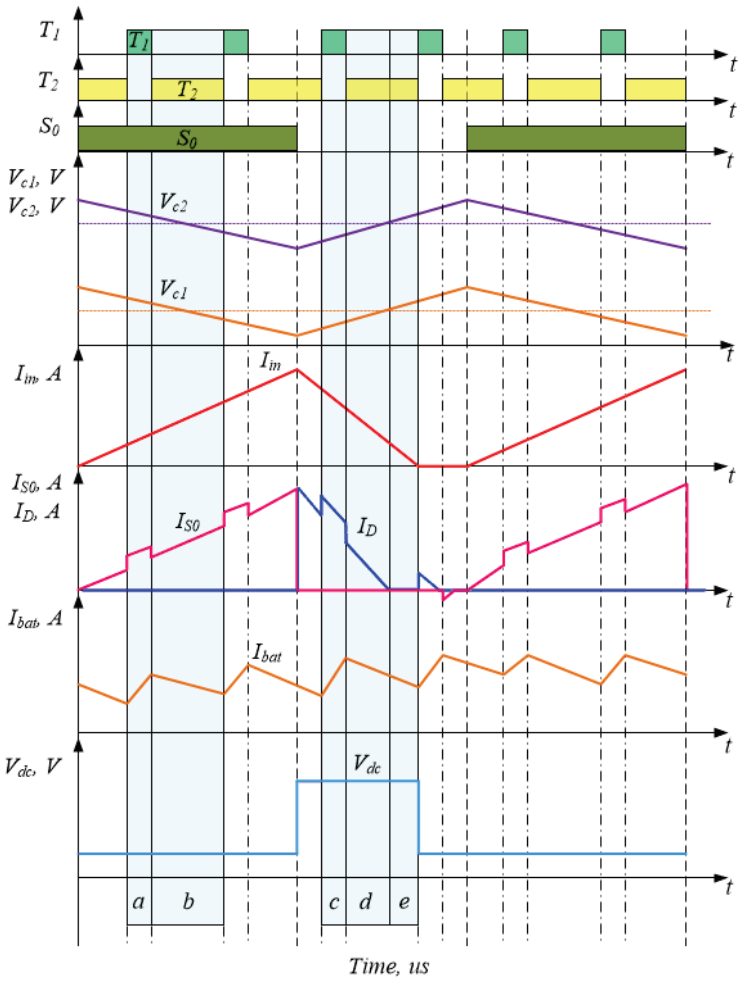



*Figure 3.2 Control principles and idealized operating waveforms of the proposed converter in steady state mode.*

The switches $S_1$, $S_4$ are conducting within the whole half part of the grid period to form the positive half wave of the output signal. The intermediate switch $S_0$ is responsible for the formation of the sinusoidal shape of the grid current.

The interval *a* in Figure 3.2 shows the time when the switch $S_0$ is conducting, the impedance capacitors are discharging and transferring their energy the impedances' coupled inductors, and as a result, the dc-link voltage is increasing. The switch $T_1$ is turned on and the battery is charging, the current's spike across the intermediate switch is due to the battery's current being added. For this mode, equations of voltages and currents can be presented as follows:

$$v_{L1} = v_{Cout} - v_{C1} - V_{in},\ v_{L2} = v_{Cout} - v_{C2}. \tag{3.1}$$

$$i_{in} + i_{C2} = i_{bat} + i_{S0},\ i_{Cout} + i_{out} = i_{S0}. \tag{3.2}$$

The interval *b* in Figure 3.2 shows the time when the instantaneous voltage across capacitor $C_2$ is becoming lower than the predefined value; the battery starts to discharge, which means that $T_2$ is turned on, and $T_1$ is turned off.

The interval *c* in Figure 3.2 shows the interval when the switch $S_0$ is turned off. The impedance diode starts to conduct, and the impedance capacitors and the battery are charging. The current across the output capacitor *C* changes its direction, while keeping the direction across the output circuit *L, R*. Although the switches *S1, S4* are turned on, the current across them equals zero.

$$v_{L1} = v_{C2} - V_{in},\ v_{L2} = v_{C1}. \tag{3.3}$$

$$i_{in} + i_{C1} = i_{C2},\ i_{Cout} = i_{out}. \tag{3.4}$$

The interval *d* in Figure 3.2 shows the time when the switch $S_0$ is turned off, and the impedance diode keeps operating, and the battery is discharging.

The interval *e* in Figure 3.2 shows the time when neither of the switching devices $S_0$ nor $D_1$ are conducting and the current flows across the output circuit in the same direction as in the previous operation mode. In the Continuous Current Mode (CCM), the last mode is absent.

In a steady state mode, the average voltage across the inductors is equal to zero. Equations (5-7) 'minus' correspond to the positive part of the output voltage and 'plus' to the negative. The average voltage across the capacitors can be expressed as follows:

$$V_{C1} = \frac{Da(V_{in} \pm V_{Cout})}{1 - 2Da}, \tag{3.5}$$

$$V_{C2} = \frac{V_{in} - Da(V_{in} \pm V_{Cout})}{1 - 2Da}. \tag{3.6}$$

Where $Da=ta/T$ is a relative time when the intermediate switch is being turned on, T is a switching frequency, ta is a time interval when the intermediate switch is being turned on.

The required duty cycle of the switching state of the switch $S_0$ can be calculated as:

$$Da = \frac{V_{dc} - V_{in}}{2V_{dc} \pm 2V_{Cout}}. \tag{3.7}$$

Where $Vdc=V_{C1}+V_{C2}$is the desired level of the dc-link voltage.

### 3.1.2 Closed loop system description

Different types of the control strategies are applied in order to control the whole system, Figure 3.3*a-d*. To control the dc-link voltage the voltage across impedance capacitors $C_2$, $C_3$ is controlled by buffer circuit, Figure 3.3*a*. To control the buffer circuit the SPWM block is applied, Figure 3.3*b*.

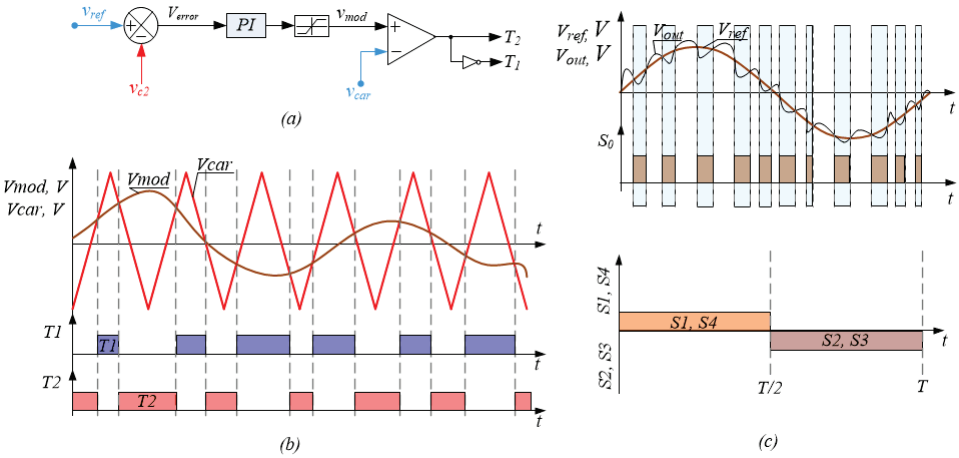



*Figure 3.3 The control strategy applied (a); control signals of the modulation techniques applied to the buffer circuit (b); hysteresis control approach for an intermediate modulation switch (c); control signals of the unfolding circuit (d).*

To control the output voltage, the hysteresis controller is selected, where the reference output voltage is compared with the measured output voltage and on the basis of that error, the intermediate switch is controlled, Figure 3.3*c*. To control the unfolding circuit a simplified PWM block is applied, Figure 3.3*d*.

## 3.2 Single-phase three-level quasi-z-source neutral-point-clamped inverter with battery storage integration

Another topology is a single-phase three-level quasi-z-source neutral-point-clamped inverter proposed in 2012 by Power Electronics Group from Tallinn University of Technology [65] (Figure 3.4), ), but only open loop mode was investigated.

The circuit consists of the following components:

- symmetrical quazi-z-source network *($L_1$, $L_2$, $C_1$, $C_2$, $D_1$, $L_3$, $L_4$, $C_4$, $C_3$, $D_2$)* to boost the input voltage;
- three-level inverter circuit, each leg consisting of two complementary switching pairs and four anti-parallel diodes *($S_1$-$S_8$. $D_{01}$-$D_{04}$)*.

The advantages of this topology are: continuous input current, ST immunity, reduced switching losses, and balanced neutral-point voltage in contrast to the traditional two-level VSI.

According to studies in [65], the proposed topology can operate in eight operation modes, some of which are repeated and only the switching state of the transistors or diodes is changed; therefore, in general, the proposed topology can operate in three operation modes: active state, zero state and ST state. The modulation technique is described in [66].

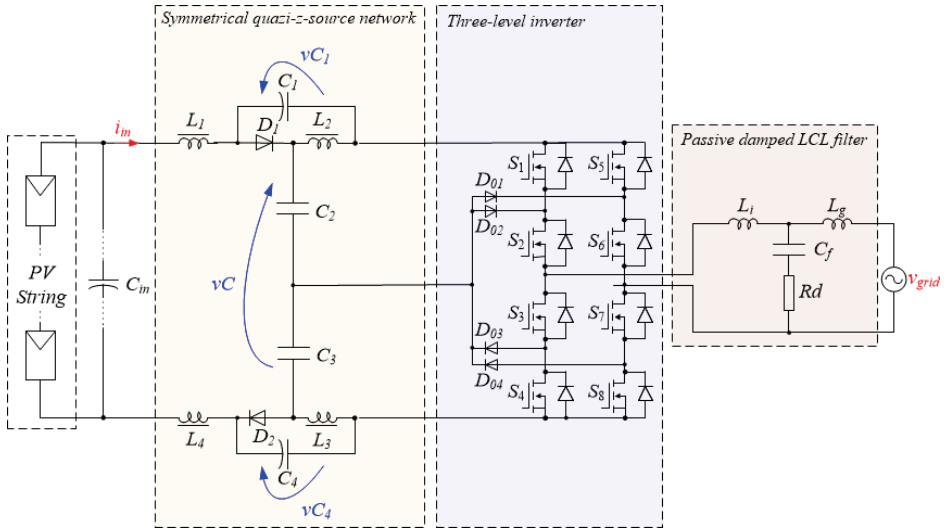



*Figure 3.4 Single-phase three-level quazi-z-source neutral-point-clamped inverter.*

### 3.2.1 Operation principle of 3L NPC qZSI

The combination of the active states, zero states and ST states allows us to control the dc-link voltage by increasing the input voltage up to a desired level of the dc-link when it is required.

The link between the anti-parallel diodes and two impedance capacitors $C_2C_3$ denoted as NPC allows reduction of the voltage stress on the switching devices twice. The reduction of the required blocking voltage capability of the inverter switches allows us to use the switching devices with an increased switching frequency. The combination of the produced three-level voltage and the increased switching frequency allows reduction of the size of the output filter and improvement of the THD of the grid current. Also, NPC allows us to use either the separate or single source in the input side. The single source is simpler to use because then the problems that may occur in the case of non-identical input sources are removed.

The CCM of the input current is the desired mode especially for PV applications, but this mode depends on the balance between the input and the output power. In order to ensure the CCM of the input current, all possible scenarios of the operation modes should be taken into consideration at the designing step.

Figure 3.5 shows the equivalent schemes in the different time intervals.

The modes *a,b,c* operate during the formation of the positive grid current and *d,e,c* during the negative. The idealized operating waveforms of the proposed converter in the steady state mode and during the CCM of the input current are presented in Figure 3.6.

The interval *a* corresponds to the conventional active state. The energy flows from the input to the grid.

$$v_{L1} = v_{L3} = \frac{V_{in} - v_C}{2};\ v_{L2} = v_{L4} = -v_{C1} = -v_{C4};\ v_{C2} = v_{C3}, \tag{3.7}$$

$$i_{L1} + i_{C1} - i_{L2} - i_{C2} = 0;\ i_{C3} - i_{L3} - i_{C4} + i_{L4} = 0;\ i_{L2} - i_{C1} - i_{ab} = 0. \tag{3.8}$$

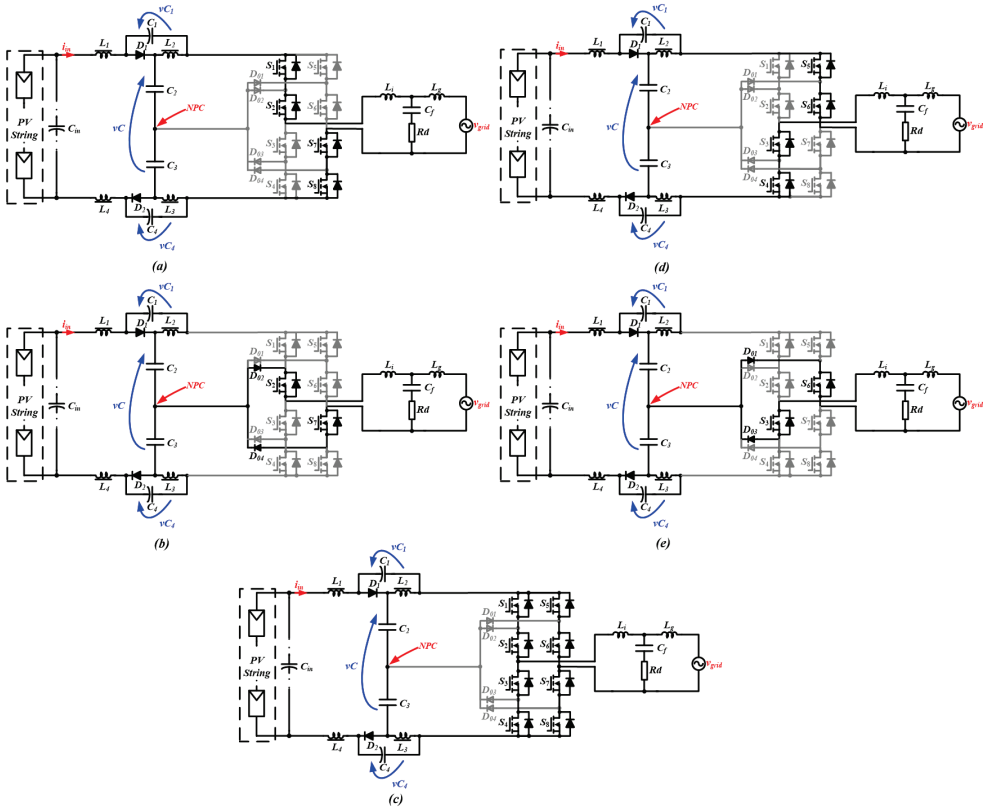



*Figure 3.5 Equivalent schemes: active states (a,d), zero states (b,e) and ST state (c).*

The interval *b* is a zero state; during this interval, the impedance capacitors are storing energy.

$$v_{L1} = v_{L3} = \frac{V_{in} - v_C}{2};\ v_{L2} = v_{L4} = -v_{C1} = -v_{C4};\ v_{C2} = v_{C3}, \tag{3.9}$$

$$i_{L1} + i_{C1} - i_{L2} - i_{C2} = 0;\ i_{L4} + i_{C3} - i_{L3} - i_{C4} = 0. \tag{3.10}$$

The interval *c* is ST state. During this mode, the energy that has been stored in the impedance capacitors at the previous step is transfered to the impedance inductors. In the next time interval *a*, the energy stored in the inductors will accumulate with the input energy and as a result, the voltage after impedance networks, virtual dc-link voltage, will be increased.

$$v_{L1} = v_{L3} = \frac{V_{in} + v_{C1} + v_{C4}}{2};\ v_{L2} = v_{L4} = v_{C2} = v_{C3}, \tag{3.11}$$

$$i_{L1} + i_{C1} = i_{L3} + i_{C4} = 0;\ i_{L4} + i_{C3} = i_{L2} + i_{C2} = 0. \tag{3.12}$$

The simulation results presented in [PAPER-III] show that the investigated topology is able to operate in a wide operation range of the input power; it can operate in a buck and in a boost mode and it is able to produce a grid current of the required quality.

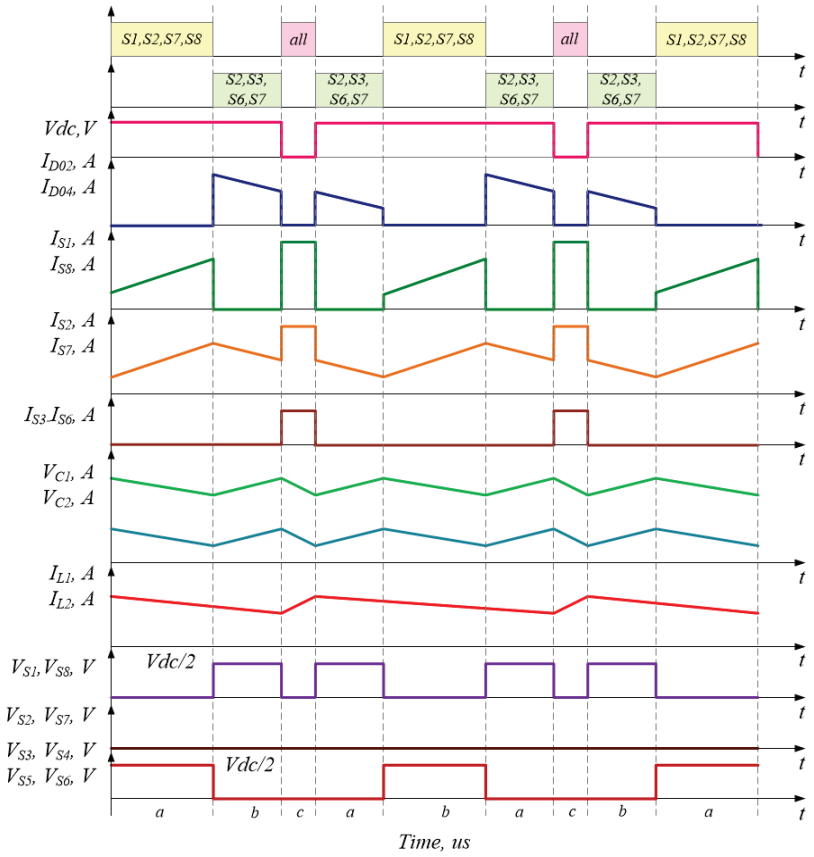



*Figure 3.6 Control principle and idealized operating waveforms of the proposed converter in steady state mode.*

**3.2.2 Selected battery storage integration scenario in a quasi-Z-source inverter.**

The decentralized power plants require integration of the battery storage into the RESs in order to support the RES such as a PV system during low production period or even to provide the power if the input source is absent.

Two ways of connecting the battery to the impedance network are presented in [67] and [68]. In [69], a brief review of both of them and their negative aspects are discussed, and possible scenarios for solving some drawbacks are pointed out. The main drawback is that the battery can only provide the power balance between the input and the output side in a limitation input voltage range, otherwise the operation mode moves from the CCM to the Discontinuous Current Mode (DCM). If the input voltage is absent, none of the discussed methods is able to provide the power to the load because of absence of a possibility to increase the battery power up to required level.

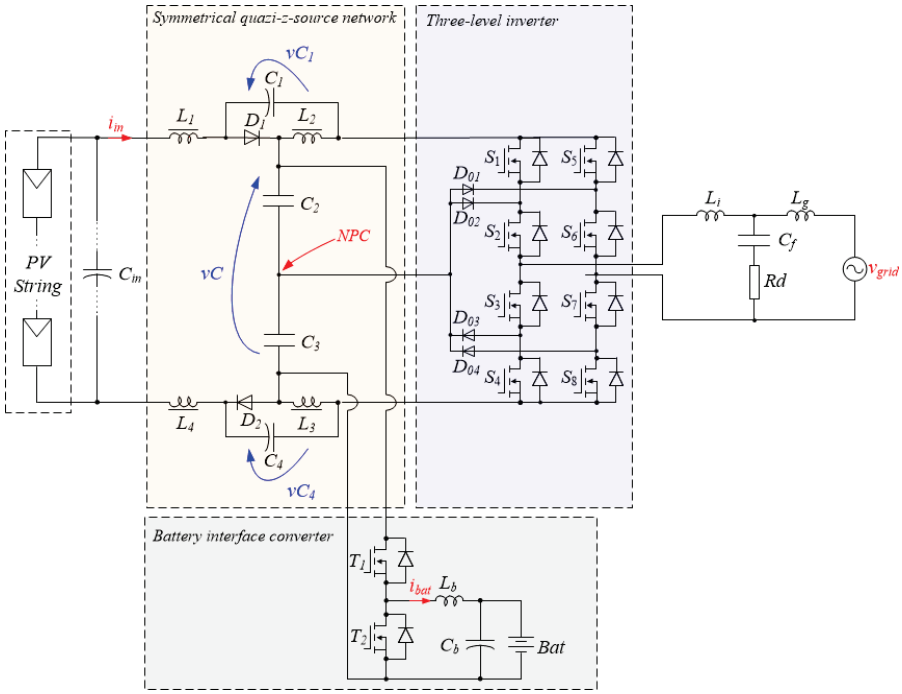



*Figure 3.7 Single-phase three-level quasi-z-source neutral-point-clamped inverter with BIC.*

In order to overcome the discussed limitation, the storage interface converter was chosen to integrate the battery into the studied topology in Figure 3.7. Because this configuration allows utilizing of the battery even if the input source is absent. In this case, the topology can be represented (Figure 3.8), where the PVs are presented as a diode. On the left side, the DC-DC boost converter is connected to the battery. Thanks to the transistors T1 and T2, the battery power can be increased up to required level, while the ST immunity of the system is kept.

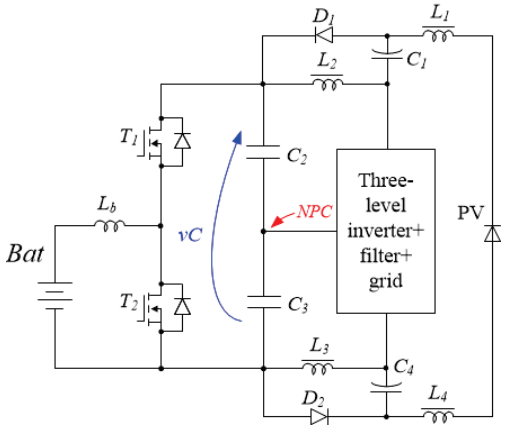



*Figure 3.8 The single-phase three-level NPC qZSI with interface storage integration during the absence of the input source.*

## 3.3 Simulation verification of the considered solutions

Figure 3.9 shows the simulation results of two considered topologies. The $P_{grid}$ was 3 kVA in both cases. In [PAPER-I] it is shown that the qZSI based on the unfolding circuit and battery storage integration can operate only in a boost mode.

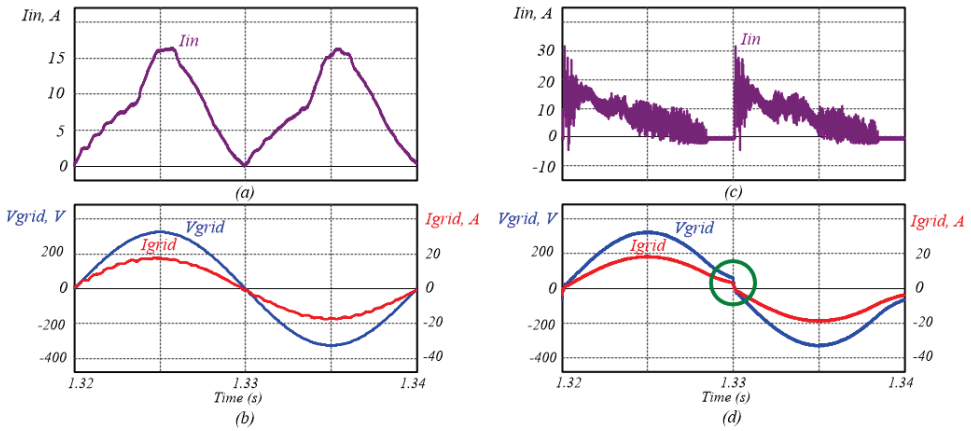



*Figure 3.9 Simulation results: single-phase three-level quasi-z-source neutral-point-clamped inverter with BIC (a,b); quasi-z-source derived inverter with unfolding circuit and BIC(c,d).*

The simulation results were performed when the $V_{IN}$ was equal to 360 V for the three-level NPC qZSI and 100 V for the qZSI based on the unfolding circuit and battery storage integration. Those values were considered as nominal values for the topologies. All the others parameters were the same for both topologies.

Figure 3.9*a,b* shows that the produced grid current and input current have better waveforms. The grid current in Figure 3.9*d* has some distortion near zero, which is a common problem of any unfolding circuit due to the uncertain state of the intermediate switch when the voltage before the unfolding circuit and the voltage across the unfolding capacitor are crossing zero point. The waveform of the grid current in Figure 3.9*c* is worse than that in Figure 3.9*a*, which results in a deteriorated performance of the MPPT, and it probably would be more complex to mitigate the ripple of the current in an unfolding circuit application.

Taking into account all the points discussed above, the three-level NPC qZSI looks more suitable for PV applications. The advantages of this topology are: it can operate without battery storage; it provides better results of the grid current and the input current; it can operate in a buck and in a boost mode. The control strategy of the energy storage circuit in this topology is independent of the control strategy of the main circuit that improves the reliability of the system. For those reasons, the three-level NPC qZSI was selected for future consideration.

## 3.4 Summary of Chapter 3

In this chapter, two topologies of PEC were considered in order to define the final topology for further consideration. The main requirements to the topology are: CIC, wide regulation of input voltage, quality of the produced current. The first topology, the qZSI inverter with unfolding circuit, was proposed by the author during her PhD study program. The second topology, single-phase three-level NPC qZSI, was proposed by Power Electronics Group from Tallinn University of Technology. The comparison between these two topologies has shown that the second topology is more suitable for residential PV applications because in terms of the main requirements, it provides better results than the first topology.

Since this work focuses on the PEC for residential PV applications, it is required to integrate the energy storage into the system. In this chapter, the storage interface converter was proposed. The proposed storage interface converter is able to provide the power balance between the input and output sides; moreover, it is able to provide the power even when the input source is absent during the night period.

# 4 Hardware and software design of the grid-connected qZSI with battery storage integration

This chapter is dedicated to the hardware and software design of the grid-connected qZSI with battery storage integration. In particular, two power decoupling approaches used to filter the DFR component of input power are addressed. The tuning up process of the dPR controller with the HC circuit used to control the grid current along with the tuning up process of the Proportional Integer Derivative (PID) controller used to control the voltage across impedance capacitors $C_2$ and $C_3$ are presented. Finally, the battery interface conversion will be considered to provide both the power balance and filtering of the DFR component of input power.

The main task of any regulator is to ensure the stability of the system along with providing quality parameters. The residential PV inverters should inject into the grid the current of the required quality, based on the standard EN61000-3-2, the THD should be lower than 5%. In order to control the output current, different types of controllers can be applied. In Chapter 2, it was shown that it is a good solution to regulate ac quantity by the PR with HC circuit due to the ability to control the undesired low order harmonics that can be present in a grid voltage. Since the input voltage is a time-varying component, it is required to use a voltage controller to regulate the voltage across capacitors $C_2$ and $C_3$. Since we are dealing with a single-phase inverter, the input power has a DFR component, which affects the MPPT performance. In order to improve the efficiency the MPPT, different filtering methods can be applied.

## 4.1 Double-frequency ripple elimination strategy for qZSI

The common problem of single-phase inverters is the DFR of the input power. The grid power consists of two components: the grid voltage and the grid current, which change according to the sinusoidal law with the line frequency. As a result, the grid power has not only an average value, but also the DFR. The grid voltage and grid current are assumed to be in phase:

$$V_g(t) = V_{g\_max}\, sin(\omega t)\text{,}\quad I_g(t) = I_{g\_max}\, sin(\omega t)\text{,} \tag{4.1}$$

$$P_g(t) = V_g(t)I_g(t) = \frac{1}{2}V_g(t)I_g(t) - \frac{1}{2}V_g(t)I_g(t)\,cos(2\omega t)\cdot \tag{4.2}$$

These DFRs are transferred into the input side from the output side [70], [71], deteriorating the efficiency of the PV system. In order to mitigate the DFR of the input power, the filtering systems of the DFR are applied where the ripple component of the power flows across the storage element by passing the input side of the main circuit. As a result, the input power has minimum power pulsation that allows using the storage battery in the input side. Traditionally, to reduce the DFR, the input capacitor is applied. This decision needs no auxiliary components, nor changes in the control strategy [72]. But the required capacitance and voltage are high enough, therefore, for this purpose, an Electrolytic Capacitor (E-cap) is applied. The E-cap is a weak part of the system despite the highest energy density and the lowest price per Joule because of the low ratings of ripple current and the high value of the Equivalent Series Resistors (ESRs), which leads to the heating up of the E-cap, therefore its size is limited.

The leakage current due to the electromechanical reaction of the oxide layer reduces the lifetime of the E-cap [73]-[75].

There are two types of filtering methods: APD [76]-[87] that has an additional active component(s) and PPD [88] that has an additional passive component(s) or can be realized just by means of the modified control strategy.

The integration of one of these methods allows attenuation of the DFR of the input power and reduction of the capacitance of the capacitor(s) used as a storage element; as a result, the metallized polypropylene film capacitor or the multi-layer ceramic capacitor can be used instead of the E-cap. Today's markets are offering these types of capacitors with lower energy density, lower field strength and higher price than the E-cap, but their size is smaller and they have better immunity to the leakage current, which improves the reliability of the system in general [74]-[91]. Naturally, every type of a capacitor has its own specific advantages and disadvantages that should be taken into consideration at the design step, such as the operation mode, the environment, the voltage stress, the current ripple, the operation frequency.

Further, the APD and the PPD will be compared.

#### 4.1.1 Comparison of the active and passive decoupling approach for double-frequency power ripple cancellation.

In order to compare the two approaches: active power decoupling and passive power decoupling the following parameters can be applied. All energy is being stored in capacitors [92] and inductors [93], because these parameters reflect the required dimension size of the corresponding components:

$$E_{LW} = \sum_{i=1}^{N_L} \frac{L_i I_{ave(i)}^2}{2}, \tag{4.3}$$

$$E_{CW} = \sum_{i=1}^{N_C} \frac{C_i V_{\max(i)}^2}{2}, \tag{4.4}$$

where $E_{LW}$ is energy stored in indictor, $E_{CW}$ is energy stored in capacitor, $N_L$ is number of inductors, $N_C$ is number of capacitors, $L$ is inductor, $C$ is capacitor, $I_{ave}$ is average current across inductor, $V_{max}$ is maximum value of voltage across capacitor:

Secondly, voltage stress on the transistors dictates the type of a switch to be selected from among those available on the market:

$$T_W = \sum_{i=1}^{N_T} V_{T(i)}, \tag{4.5}$$

where $N_T$ is number of transistors, $V_T$ is voltage stress across transistors.

It should be mentioned that all semiconductor devices are assumed to be of the same type for both cases. Also, switching losses will not be analyzed in detail because of its complexity. The switching losses are assumed to be proportional to the conduction losses. This assumption is quite realistic because switching frequency is the same for all semiconductors in both cases.

The size of the passive components is represented in the relative units (p.u.) in order to neglect the effect of input/output parameters on the final comparison, where

$$C_u = \frac{P_g T}{2\pi V_g^2},\ L_u = \frac{V_C V_g T_{sw}}{12\pi P_g}. \tag{4.6}$$

**Passive elements estimation in PPD approach**

Figure 4.1*a* shows the linear-ripple approximated waveforms of the inductor current and capacitor voltage where *D* is the shoot through duty cycle.

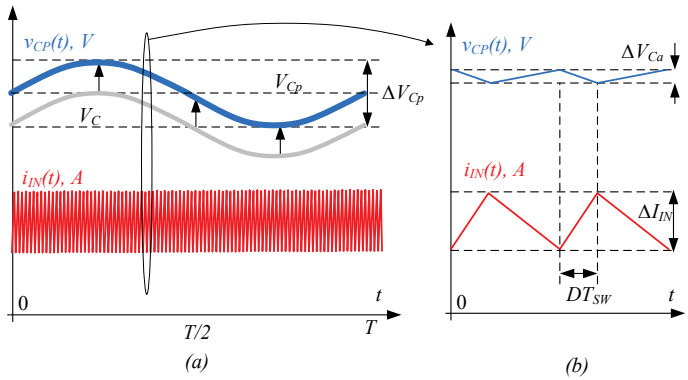



*Figure 4.1 Capacitor voltage and inductor current waveforms: low frequency ripple (a) and high frequency ripple (b).*

We assume here that the system operates in the CCM. To ensure the right power flow from the input side to the output, the value of the dc-link voltage should be higher than the maximum value of the grid voltage. Therefore, the average value across the impedance capacitors should be higher by half the voltage ripple across them (Figure 4.1*b,c*). The dependences between the input $V_{IN}$, dc-link and capacitors voltages are well known [65]:

$$V_{dc} = \frac{V_{in}}{1-2D}. \tag{4.7}$$

$$V_{C2} = V_{C3} = \frac{1-D}{1-2D} \cdot \frac{V_{in}}{2}, \tag{4.8}$$

$$V_{C1} = V_{C4} = \frac{D}{1-2D} \cdot \frac{V_{in}}{2}. \tag{4.9}$$

Due to the symmetrical two quasi-Z source networks, the voltage across the capacitors is $V_{C1} = V_{C4}$, $V_{C2} = V_{C3}$.

The capacitors are being applied as storage elements to mitigate the DFR. The value of the inductances of the impedance network inductors can be calculated by taking into account the high-frequency ripple of the current across them.

On the other hand, by taking into account (4.8) and (4.9), the ST duty cycle can be expressed as:

$$D = \frac{V_C - V_{in}}{2V_C - V_{in}}. \tag{4.10}$$

By assuming that the converter is ideal, i.e., the energy conversion efficiency $\eta = 100\%$, an average input current can be expressed as:

$$P_{in} = P_g;\ I_{in} = \frac{P_g}{V_{in}}. \tag{4.11}$$

Voltages across the capacitors have Low Frequency Ripple (LPF) that can be calculated as:

$$\Delta V_{C1p} = \frac{1}{C_{1p}} \int_0^{T/4} \frac{P_g}{V_{dc}} sin(2\omega t) d\omega t = \frac{P_g T}{2\pi V_{dc} C_{1p}}, \tag{4.12}$$

$$\Delta V_{C2p} = \frac{1}{C_{2p}} \int_0^{T/4} \frac{P_g}{V_{dc}} sin(2\omega t) d\omega t = \frac{P_g T}{2\pi V_{dc} C_{2p}}, \tag{4.13}$$

where $V_{dc} = V_{C1p} + V_{C2p} + V_{C3p} + V_{C4p}$.

It should be taken into account that in the PPD approach, significant voltage ripples are present across the capacitors. The control system should be able to increase an average voltage level, to ensure that the minimum value of the dc-link voltage is not less than the predefined nominal level at any moment of time (Figure 4b,c). The average voltages across the impedance capacitors in the PPD approach can be expressed as:

$$V_{C1p} = V_{C1} + \frac{\Delta V_{C1p}}{2} = \frac{V_{Cp} - V_{in}}{2} + \frac{P_g T}{4\pi C_{1p} V_{dc}}, \tag{4.14}$$

$$V_{C2p} = V_{C2} + \frac{\Delta V_{C2p}}{2} = \frac{V_{Cp}}{2} + \frac{P_g T}{4\pi V_{dc} C_{2p}}. \tag{4.15}$$

At the same time, the voltage ripple factor across the capacitor is defined as:

$$K_{C1p} = \frac{\Delta V_{C1p}}{V_{C1p}};\ K_{C2p} = \frac{\Delta V_{C2p}}{V_{C2p}}. \tag{4.16}$$

The value of the capacitors through the relative unit (4.6) as a function of ripple factors is expressed as:

$$C_{1p} = C_{4p} = C_u \frac{2V_g^2}{K_{C1p}(2V_{Cp}^2 - 3V_{Cp}V_{in} + V_{in}^2)}. \tag{4.18}$$

$$C_{2p} = C_{3p} = C_u \frac{2V_g^2}{K_{C2p}V_{Cp}(2V_{Cp} - V_{in})}. \tag{4.19}$$

By assuming that two impedance networks are equally loaded, the average current in each inductor is:

$$I_{L1p} = I_{L2p} = I_{L3p} = I_{L4p} = \frac{P_g}{V_{in}}. \tag{4.20}$$

Considering that low frequency ripples are being filtered by the LPF in the input current, the inductance can be calculated by taking into account the High Frequency Ripple (HFR) only:

$$\Delta I_{L1p} = \int_0^{DT_{sw}} \frac{di_{L1}}{dt} dt = \frac{V_{Cp} DT_{sw}}{L_{1p}}, \tag{4.21}$$

$$\Delta I_{L2p} = \int_0^{DT_{sw}} \frac{di_{L2}}{dt} dt = \frac{V_{Cp} DT_{sw}}{2L_{2p}}. \tag{4.22}$$

where $T_{sw}$ is the switching period.

Inductances $L_{1p}$, $L_{2p}$ can be expressed through the current ripple factor as:

$$K_{L1p} = \frac{\Delta I_{L1p}}{I_{L1}}; \qquad K_{L2p} = \frac{\Delta I_{L2p}}{I_{L2}}. \tag{4.23}$$

By assuming that $K_{L1p} = K_{L2p} = K_{Lp}$ and based on (4.20)-(4.24),(4.6) the value of inductances through the relative unit can be expressed as:

$$L_{1p} = L_{2p} = L_{3p} = L_{4p} = L_u \frac{6\pi V_{in}(V_{Cp} - V_{in})}{K_L V_g (2V_{Cp} - V_{in})}. \tag{4.24}$$

The total voltage stress on the semiconductor devices can be estimated by summarizing the voltage stress across the semiconductor devices. In the PPD, all the transistors are in similar conditions; thus, the total voltage stress can be expressed as:

$$T_{wp} = 8V_{S1} = 8\left(\frac{(V_{Cp\_max} - V_{in})}{2} + \frac{V_{Cp\_max}}{2}\right). \tag{4.25}$$

Finally, the total energy stored in the capacitors and inductors is expressed as follows:

$$E_{LWp} = 2\frac{L_{1p} I_{in}^2}{2} + 2\frac{L_{2p} I_{in}^2}{2} = L_{1p}\left(\frac{P_g}{V_{in}}\right)^2 + L_{2p}\left(\frac{P_g}{V_{in}}\right)^2, \tag{4.26}$$

$$E_{CW14p} = 2\frac{C_{1p}(\frac{V_{Cp\_max} - V_{in}}{2})^2}{2} = C_{1p}(\frac{V_{Cp\_max} - V_{in}}{2})^2, \quad (4.27)$$

$$E_{CW23p} = 2\frac{C_{2p}(\frac{V_{Cp\_max}}{2})^2}{2} = C_{2p}(\frac{V_{Cp\_max}}{2})^2, \quad (4.28)$$

$$E_{CWp} = E_{CW14p} + E_{CW23p} = C_{1p}(\frac{V_{Cp\_max} - V_{in}}{2})^2 + C_{2p}(\frac{V_{Cp\_max}}{2})^2. \quad (4.29)$$

**Passive elements estimation in APD approach**

In the APD approach, it is assumed that the fluctuating component of the power is directed to the auxiliary circuit and does not influence the impedance network components.

The control system predefines the average voltage across the buffer capacitor as:

$$V_{C_B} = kV_{Ca}, \quad (4.30)$$

where *k* is a coefficient introduced to demonstrate a ratio between the voltage across inner capacitors and buffer capacitor. It can be chosen in the following range $0.5 < k < 1$. It is important to notice that the voltage across the buffer capacitor should be less than the dc-link voltage.

The average value of the voltages across the capacitors $C_1, C_2, C_3$ and $C_4$ is maintained at the constant level according to (4.8) and (4.9); thus, their capacitance can be calculated by taking into account only the HFR:

$$\Delta V_{C1a} = \frac{1}{C_{1a}}\int_0^{DT_{sw}} \frac{P_g}{V_{dc}}dt = \frac{P_g T_{sw}(V_{Ca} - V_{in})}{C_{1a}(2V_{Ca} - V_{in})V_{dc}}, \quad (4.31)$$

$$\Delta V_{C2a} = \frac{1}{C_{2a}}\int_0^{DT_{sw}} \frac{P_g}{V_{dc}}dt = \frac{P_g T_{sw}(V_{Ca} - V_{in})}{C_{2a}(2V_{Ca} - V_{in})V_{dc}}. \quad (4.32)$$

Power ripple factors for the HFR components are defined as:

$$K_{C1a} = \frac{\Delta V_{C1a}}{V_{C1a}}, K_{C2a} = \frac{\Delta V_{C2a}}{V_{C2a}}. \quad (4.33)$$

The value of the capacitors is expressed as:

$$C_{1a} = C_{4a} = \frac{2P_g T_{sw}}{K_{C1a}(4V_{Ca}^2 - 4V_{Ca}V_{in} + V_{in}^2)}, \quad (4.34)$$

$$C_{2a} = C_{3a} = \frac{2P_g T_{sw}(V_{Ca} - V_{in})}{K_{C2a} V_{Ca}(4V_{Ca}^2 - 4V_{Ca}V_{in} + V_{in}^2)}. \quad (4.35)$$

Voltage across the buffer capacitor has the DFR. By assuming that the whole power ripple circulates in the auxiliary circuit, the voltage ripple across the buffer capacitor can be calculated as:

$$\Delta V_{C_B} = \frac{1}{C_B} \int_0^{T/4} i_{C_B}(t) \sin 2\omega t dt = \frac{P_g T}{2\pi V_{C_B} C_B}. \quad (4.36)$$

The voltage ripple factor through the buffer capacitor is defined as:

$$K_{C_B} = \frac{\Delta V_{C_B}}{V_{C_B}}. \quad (4.37)$$

Finally, by taking into account Eqs. (4.36), (4.37) and (4.6), the value of the buffer capacitor through the relative unit can be expressed as:

$$C_B = C \frac{V_g^2}{V_{Ca}^2 k^2 K_{C_B}}. \quad (4.38)$$

The average current in the impedance inductors is equal to the input current:

$$I_{L1a} = I_{L3a} = \frac{P_g}{V_{in}}, \; I_{L2a} = I_{L4a} = \frac{2P_g}{V_{in}} \quad (4.39)$$

HFR of the inductor current can be estimated as:

$$\Delta I_{L1a} = \int_0^{DT_{sw}} \frac{di_{L1a}}{dt} dt = \frac{V_{Ca} D T_{sw}}{2L_{1a}}, \quad (4.40)$$

$$\Delta I_{L2a} = \int_0^{DT_{sw}} \frac{di_{L2a}}{dt} dt = \frac{V_{Ca} D T_{sw}}{2L_{2a}}. \quad (4.41)$$

The average value of the current in the buffer inductor is zero, but the maximum value can be found from the maximum value of the reactive power:

$$I_{L_B} = \frac{P_g}{kV_{Ca}}. \quad (4.42)$$

At the same time, the buffer inductor current has the HFR component that can be expressed as:

$$\Delta I_{L_B} = \int_0^{D_b T_{sw}} \frac{di_{L_B}}{dt} dt = \frac{V_{Ca} D_b T_{sw} (1-k)}{L_B}. \quad (4.43)$$

where $D_b$ is the time duty when the upper switch is conducting.

Current ripple factors are defined as follows:

$$K_{L_B} = \frac{\Delta I_{L_B}}{I_{L_B}}, \; K_{L1a} = \frac{\Delta I_{L1a}}{I_{L1}}. \quad (4.44)$$

The value of inductances can be expressed through the relative unit (25) as:

$$L_{1a} = L_{3a} = L_u \frac{6\pi V_{in}(V_{Ca} - V_{in})}{K_{L1} V_g (2V_{Ca} - V_{in})} \quad (4.45)$$

$$L_{2a} = L_{4a} = L_u \frac{3\pi V_{in}(V_{Ca} - V_{in})}{K_{L2} V_g (2V_{Ca} - V_{in})} \quad (4.46)$$

$$L_B = L_u \frac{12\pi k D_b V_{Ca}(k-1)}{K_{L_B} V_g}. \quad (4.47)$$

In the APD approach, the total voltage stress on the semiconductor devices can be expressed by taking into account 8 inverter switches and 2 buffer switches:

$$T_{wa} = 8V_{S1} + 2V_{T1} = 4(2V_{Ca} - V_{in}) + 2V_{Ca}. \quad (4.48)$$

The total energy storage in the capacitors and inductors is:

$$E_{LWa} = 2\frac{L_{1a} I_{in}^2}{2} + 2\frac{L_{2a} I_{in}^2}{2} + \frac{L_B I_{L_B}^2}{2} = \frac{L_B I_B^2}{2} + L_{1a}\left(\frac{P_g}{V_{in}}\right)^2 + \left(\frac{2P_g}{V_{in}}\right)^2 L_{2a}. \quad (4.49)$$

$$E_{CWa} = \frac{2C_{1a}V_{C1}^2}{2} + \frac{2C_{2a}V_{C2}^2}{2} + \frac{C_B V_{C_{B\_max}}^2}{2} = C_{1a}\left(\frac{V_{Ca} - V_{in}}{2}\right)^2 + C_{2a}\left(\frac{V_{Ca}}{2}\right)^2 + \frac{C_B(1+K_{CB})^2 V_{CB}^2}{2}. \quad (4.50)$$

*Table 4.1 – Main equations*

| | APD | PPD |
|---|---|---|
| $C_1$,$C_4$ | $\frac{2P_gT_{sw}}{K_{C1a}(4V_{Ca}^2-4V_{Ca}V_{in}+V_{in}^2)}$ | $C_u\frac{2V_g^2}{K_{C1p}(2V_{Cp}^2-3V_{Cp}V_{in}+V_{in}^2)}$ |
| $C_2$,$C_3$ | $\frac{2P_gT_{sw}(V_{Ca}-V_{in})}{K_{C2a}V_{Ca}(4V_{Ca}^2-4V_{Ca}V_{in}+V_{in}^2)}$ | $C_u\frac{2V_g^2}{K_{C2p}V_{Cp}(2V_{Cp}-V_{in})}$ |
| $C_B$ | $C_B=C\frac{V_g^2}{V_{Ca}^2k^2K_{C_B}}$ | - |
| $L_1$,$L_3$ | $L_u\frac{6\pi V_{in}(V_{Ca}-V_{in})}{K_{L1}V_g(2V_{Ca}-V_{in})}$ | $L_u\frac{6\pi V_{in}(V_{Cp}-V_{in})}{K_LV_g(2V_{Cp}-V_{in})}$ |
| $L_2$,$L_4$ | $L_u\frac{3\pi V_{in}(V_{Ca}-V_{in})}{K_{L2}V_g(2V_{Ca}-V_{in})}$ | $L_u\frac{6\pi V_{in}(V_{Cp}-V_{in})}{K_LV_g(2V_{Cp}V_{in})}$ |
| $L_B$ | $L_u\frac{12\pi kD_bV_{Ca}(k-1)}{K_{L_B}V_g}$ | - |
| $T_W$ | $10V_{Ca}-4V_{in}$ | $4(2V_{Cp\_max}-V_{in})$ |
| $E_{LW}$ | $\frac{L_BI_B^2}{2}+L_{1a}\left(\frac{P_g}{V_{in}}\right)^2+\left(\frac{2P_g}{V_{in}}\right)^2L_{2a}$ | $L_{1p}(\frac{P_g}{V_{in}})^2+L_{2p}(\frac{P_g}{V_{in}})^2$ |
| $E_{CW}$ | $C_{1a}(\frac{V_{Ca}-V_{in}}{2})^2+C_{2a}(\frac{V_{Ca}}{2})^2+$ $+\frac{C_B(1+K_{CB})^2V_{CB}^2}{2}$ | $C_{1p}(\frac{V_{Cp\_max}-V_{in}}{2})^2+C_{2p}(\frac{V_{Cp\_max}}{2})^2$ |

Altogether the above parameters reflect the quality of the discussed approaches and give useful information for engineers at the stage of the selection and system design.

Figure 4.2 shows the diagrams of the energy stored in capacitors and inductors and total voltage stress on the semiconductor devices under different decoupling approaches, different input voltage and different voltage ripple coefficients.

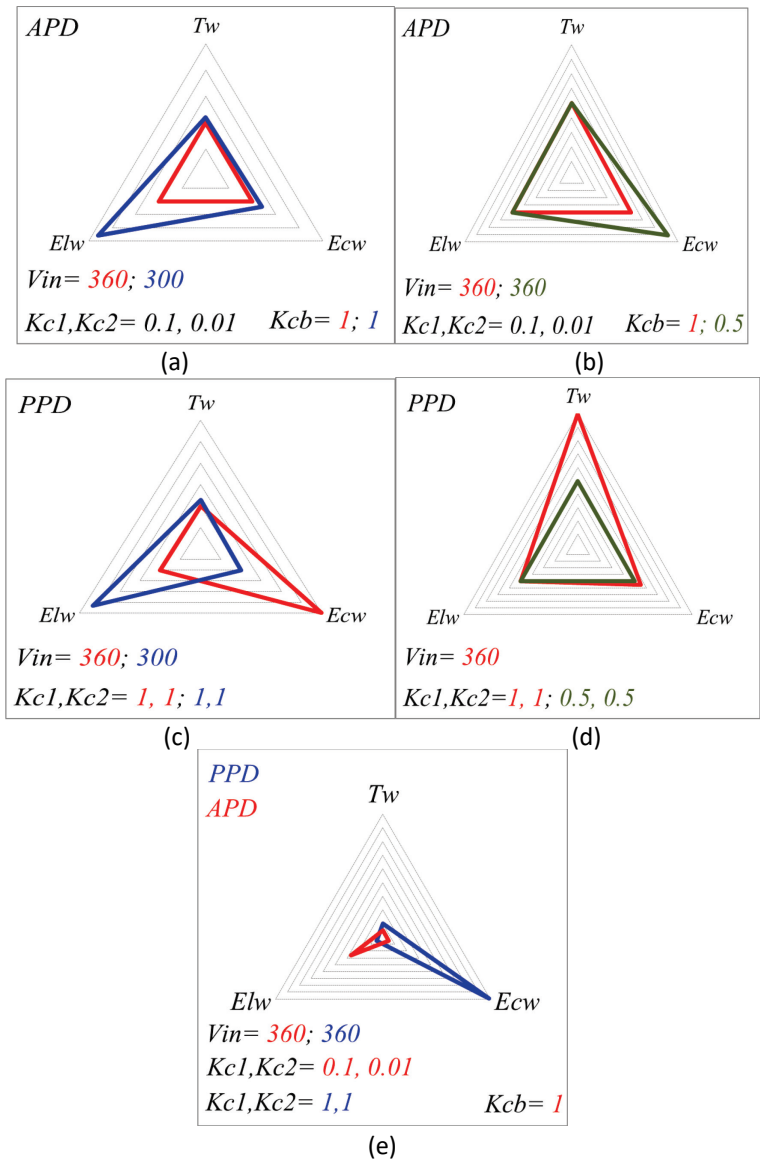



*Figure 4.2 Diagrams for comparison.*

Figure 4.2*a* shows the calculated parameters in the case of the APD approach with different input voltages. It can be seen that with the increase of the input voltage, the energy stored in capacitors and inductors is decreasing, and the total voltage stress on the semiconductor devices is decreasing as well. Figure 4.1*b* shows the calculated parameters in the case of the APD approach with different predefined voltage ripple factors of the buffer capacitor. The evident conclusion is that the energy stored in the capacitor is decreasing with the voltage ripple increasing.

Figure 4.2*c* shows the calculated parameters in the case of the PPD approach with different input voltages. It can be seen that with the increase of the input voltage, the energy stored in the capacitors is increasing, the energy stored in the inductors is

decreasing, and the total voltage stress on the semiconductor devices is decreasing as well. Figure 4.2*d* shows the calculated parameters in the case of of the PPD approach with different predefined voltage ripple factors of the impedance capacitors. The conclusion is: the energy stored in the capacitors and the total voltage stress on the semiconductor devices are increasing with the voltage ripple increase.

Finally, Figure 4.2*e* shows the comparison of the results between the application of the APD and the PPD. According to the results, the energy stored in the capacitors and the total voltage stress on the semiconductor devices are higher in the case of the PPD while the energy stored in the inductors is lower.

### 4.1.2 Implementation of the active power decoupling approach for qZSI

The APD approach was implemented and investigated in PSCAD simulation program tools. Figure 4.3 shows the case study system [PAPER-IV].

Figure 4.4 shows the block diagram of the control strategy of the investigated topology. To control the DFR of the input power, the dc-link voltage and/or input current can be under control. In the proposed control strategy, the dc-link voltage is maintained at the constant level by means of the PID controller. Therefore, to mitigate the DFR of the input power, the DFR of the input current should be under control.

In order to circulate the DFR of the input power through the auxiliary circuit, it is necessary to generate the reference decoupling current $i_B^*$. In the proposed configuration, it cannot be derived directly from the measured output power because of an additional phase shift that will be present due to the passive components of the qZSN. For that reason, the input current is used to obtain the $i_B^*$ by means of the Damped Double Frequency Resonance (DDFR) controller, which highlights the ripples of the double frequency.

In order to keep the predefined voltage across the capacitor $C_B$, it is necessary to form the constant current across the decoupling circuit $i_{B\_const}^*$; for that purpose, the PI controller is used.

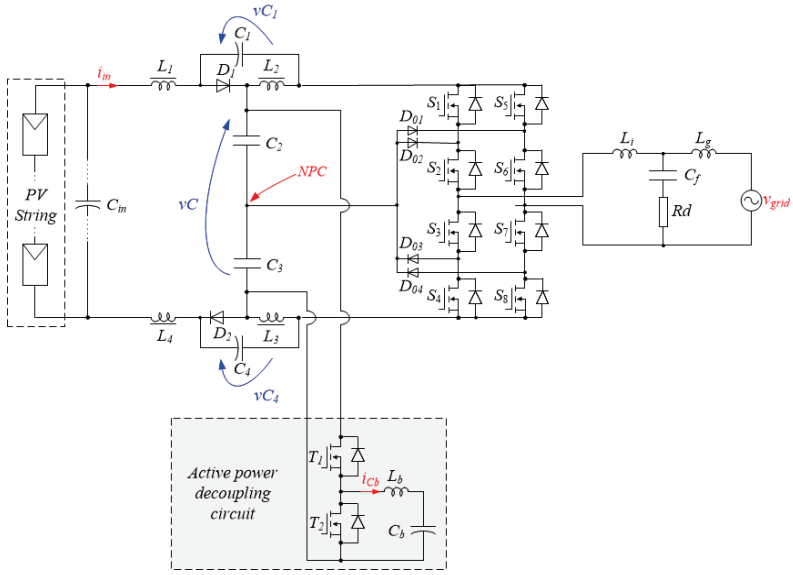



*Figure 4.3 The single-phase three-level neutral-point clamped inverter with the active power decoupling circuit.*

Finally, the very simple hysteresis approach of the constant switching frequency is used in order to provide the reference value of the current. The error $\Delta i_B$ between the reference value and the measured value of the current is applied to its input.

The strategy proposed is quite simple and requires no complex tuning. The Low Pass Filter (LPF) used for filtering the input current has 25 Hz cut-off frequency and can be easily realized in any digital system.

Figure 4.5 shows the input power ripples before and after the launch of the APD approach. The APD starts to operate at the time that equals 1.2 s. The input power ripples are equal to 100% without APD and 12.5% with APD.

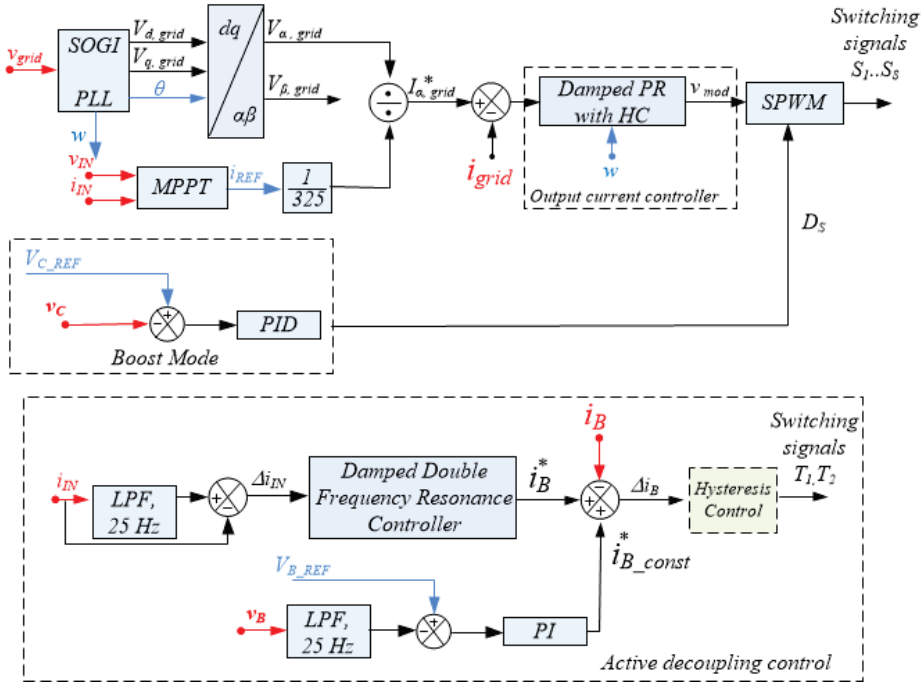



*Figure 4.4 Block diagram of the control strategy of the single-phase three-level neutral-point-clamped inverter with the active power decoupling approach.*

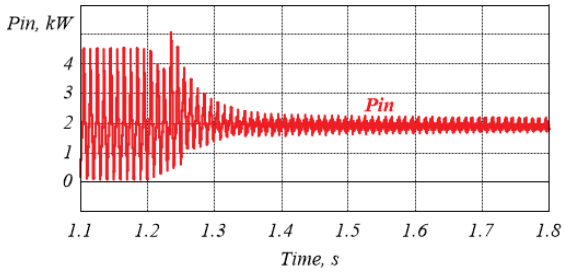



*Figure 4.5 Simulation result: input power in the APD approach.*

### 4.1.3 Implementation of the passive power decoupling approach for qZSI

The PPD approach was also implemented and investigated in PSCAD simulation program tool. The considered PPD approach is in the modified control strategy. The main topology is depicted in Figure 4.3, but without buck type active power decoupling circuit.

The modified control strategy forms the time-varying ST signal to mitigate the DFR of the input power. The time-varying ST signal causes voltage change in the dc-link; thus, one of the aims is to limit the change in the dc-link voltage in the acceptable range [PAPER-V]. Figure 4.6 shows the block diagram of the PPD control strategy.

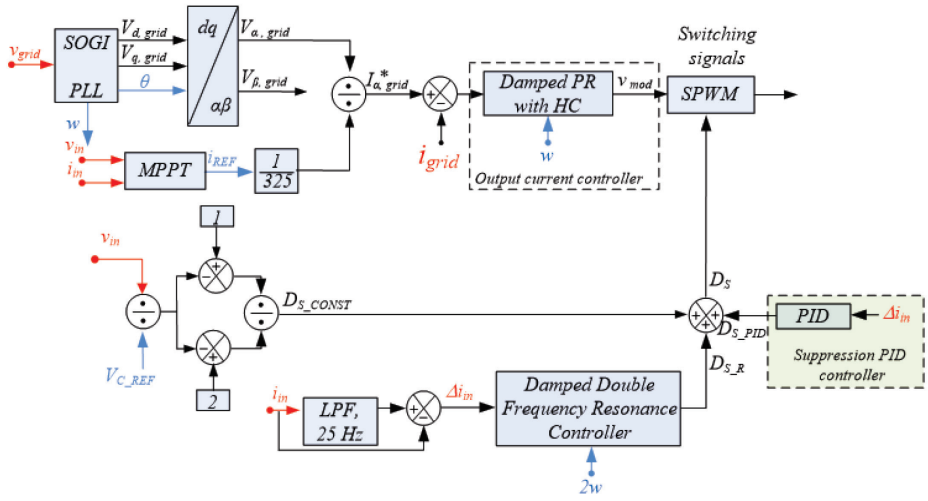



*Figure 4.6 Block diagram of the single-phase three-level neutral-point-clamped inverter with the passive power decoupling approach.*

The full ST duty cycle *Ds* consists of three components: the constant ST duty cycle *Ds_cons*, which depends on the input voltage and the desired average level of the dc-link voltage; the ST duty cycle which is changed accordingly to the sinusoidal law with the double frequency relative to the grid frequency; and $Ds_{PID}$ which is used to mitigate the high-frequency ripples of the input power.

Figure 4.7 shows the input power ripples before and after the launch of the PPD approach. The PPD starts to operate at the time when it equals 1.2 s. The input power ripples are equal to 100% without APD and 5.5% with PPD.

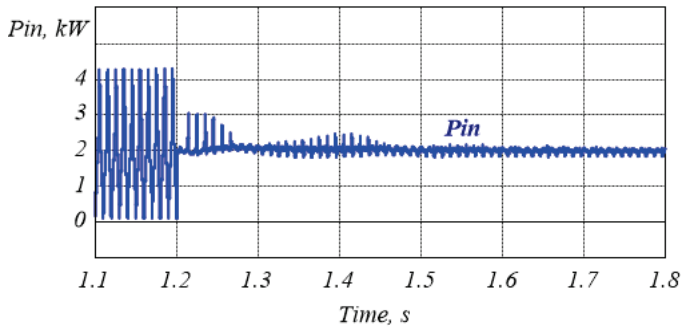



*Figure 4.7 Simulation result: input power in the PPD approach.*

## 4.2 Grid-connected control strategy for qZSI with battery storage

The control strategy of the whole system can be divided into two main parts: first, a high speed current control loop that controls the quality of grid current, and second, a low speed voltage control loop that controls the dc-link voltage. Below, the output current control loop is discussed.

To control the quality of the output current in the application of the three-level neutral-point-clamped inverter, which allows an increase of the switching frequency of inverter's switches, thus improving the quality of the grid current, we apply a passive *dLCL* output filter with dPR output controller.

Passive damped variant of an *LCL* filter was chosen because of the resistor, which is series connected to the filter capacitor and helps to smoothen the possible resonance oscillation, which may occur between *L* and *C* components; thus, it improves the stable-state of the system in comparison to a conventional *LCL* filter [96]. Passive *dLCL* filter was also chosen because of its third order filter, which attenuates the switching order harmonics in the grid current better than an *L* or *LC* filter and also an *dLCL* filter has smaller size than the other two [94], [95]. The main drawback of the application of the *LLCL* filter [97]-[99] is that this type of a filter attenuates the harmonics in a smaller range, near the switching frequency as compared to the *dLCL* filter. The design process of the *LCL* filter is presented in [100].

The dPR controller with phase compensation was selected since it has a wider frequency range under controlling in comparison to the PR controller [50], and provides the phase compensation caused by digital delay [101], [102].

### 4.2.1 Proportional-resonant controller design for grid-connected qZSI

In order to tune up the dPR transfer function of the output part which consists of the dPR, HC circuit and dLCL were calculated [PAPER-VIII]. Figure 4.8 shows the block diagram of the output part. The main object is to achieve the stable state of the system in digital realization where the digital delay is:

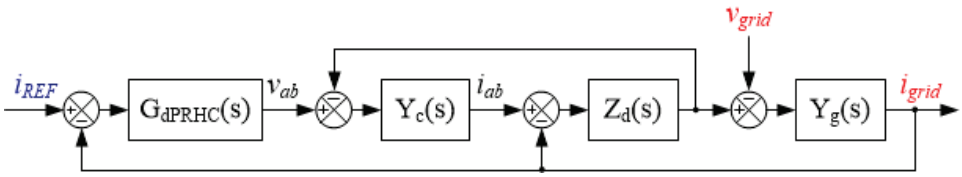



*Figure 4.8 Control diagram of the grid current.*

where $Y_c(s) = \frac{1}{sL_{fc} + R_{fc}}$ is impedance from converter side, $Y_g(s) = \frac{1}{sL_{fg} + R_{fg}}$ is impedance from grid side, $Z_d(s) = \frac{1}{sC_f} + R_d$ is impedance of the filter capacitor, $G_{dPRHC(s)}$ is a transfer function of the dPR controller with *HC* circuit. The components of the *dLCL* filter are: $R_{fc}$ and $R_{fg}$ - parasitic resistance, $R_d$ is a damped resistance, $L_{fc}$ is a filter inductor from inverter side, $L_{fg}$ is a filter inductor from grid side, $C_f$ is a capacitor filter.

The transfer function of *dLCL* was calculated by Mason's Gain Rule:

$$G_{dLCL}(s) = \frac{Y_c(s) Z_d(s) Y_g(s)}{1 + Y_c(s) Z_d(s) + Y_g(s) Z_d(s)}. \tag{4.51}$$

Figure 4.9 shows the *dPR* controller with phase compensation, where *Kp* is the proportional coefficient, Ki is the integer coefficient, h is order harmonic, $\omega_c$ is the cut-off frequency, $\omega$ is the angular frequency.

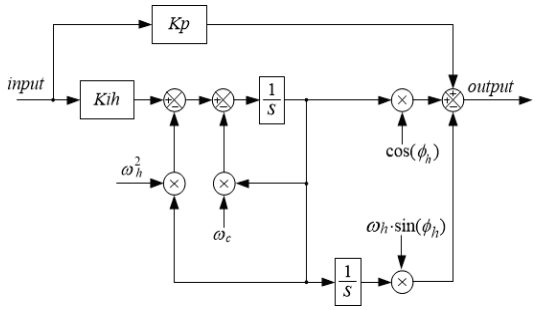



*Figure 4.9 dPR controller with phase compensation.*

The transfer function of the *dPR* controller with *the HC* circuit and phase compensation is:

$$G_{dPR}(s) = K_p + \sum_{h=1,3,5,7,9} K_{rh} \frac{s \cdot cos(\varphi_h) - \varphi_h \cdot sin(\varphi_h)}{s^2 + 2\omega_{ch} s + \omega_h^2}, \tag{4.52}$$

$$\varphi_h = N \cdot 360^0 \cdot \frac{\varphi_h}{2\pi} \cdot \frac{1}{f_s}, \tag{4.53}$$

where *N* is computational delay, *fs* is a switching frequency.

Full closed loop transfer function is:

$$G_{dPRHCdLCL}(s) = \frac{dPRHC(s)\, dLCL(s)}{1 + dPRHC(s)\, dLCL(s)}. \tag{4.54}$$

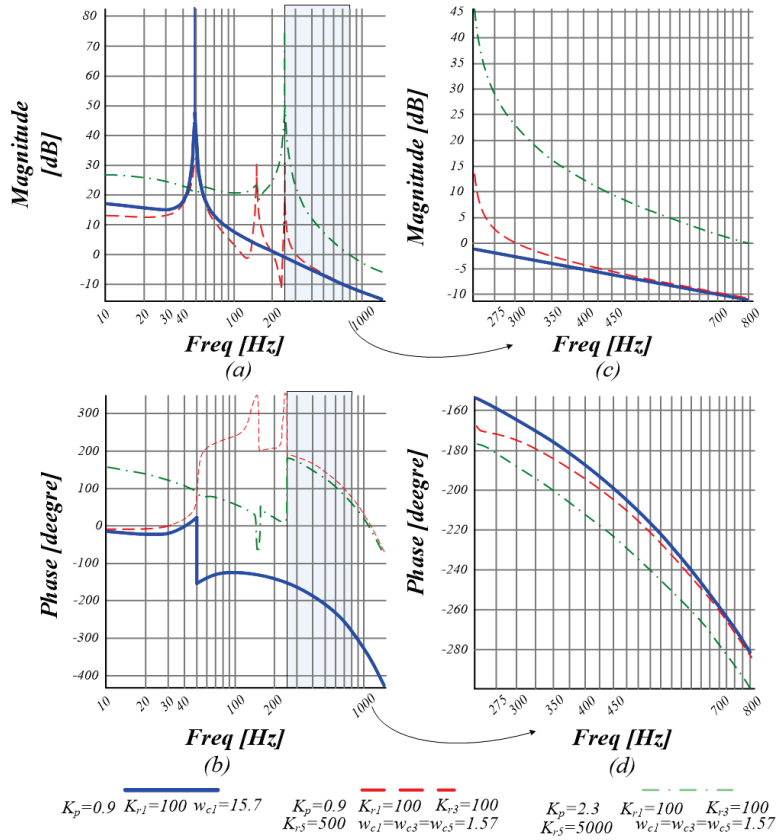



*Figure 4.10 Bode plot diagrams of $G_{dPRdHCLCL}(z)$.*

Figure 4.10 shows the Bode plot diagrams of $G_{dPRHCdLCL}(z)$. The transformation from s domain to z domain was performed by means of the Tustin with pre-wrapping discretization method.

Figure 4.11 shows the simulation results of the single-phase three-level NPC qZSI connected to the grid. Figure 4.11*a* shows the simulation results with stable parameters of the dPR with HC circuit, which is marked as the red line in Figure 4.10. During startup, the grid current has some spikes that can launch the current protection function, which disconnects the PEC from the grid. Figure 4.11*b* shows the simulation results with unstable parameters, which are marked as the green line in Figure 4.10. During startup, the grid current has lower current spike compared to the stable parameters. The optimization of the dPR with the HC circuit based on the combination of the unstable parameters and the stable parameter could allow smoothing the startup grid current value.

Figure 4.11*c* shows the results of the optimized dPR controller with the HC circuit. In the beginning the parameters of the current controller were unstable and they were changed until the parameter became stable during 5 fundamental periods. It can be noticed that the startup grid current was smoothened, while the stability of the system remained the same.

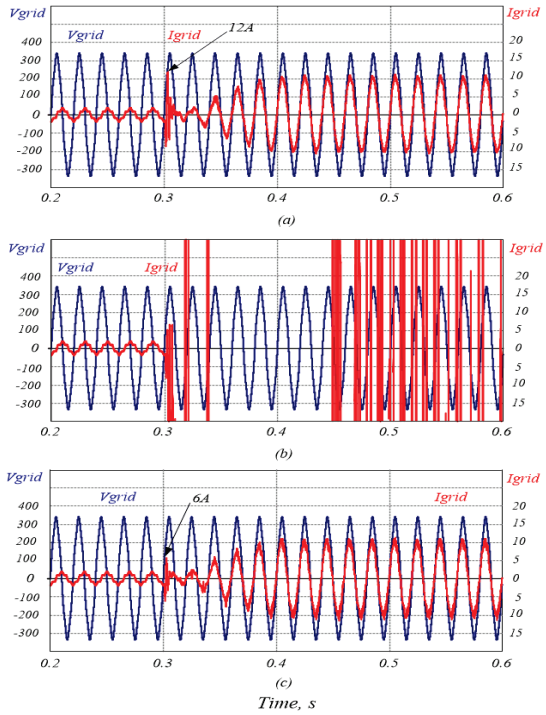



*Figure 4.11 Simulation results: nominal PR controller parameters (a), increased PR controller parameters (b), increased controller parameters during starting up along with nominal parameters in steady state mode (c).*

### 4.2.2 PID controller design for qZS capacitors voltage control

As it was mentioned above, the control system of the main topology has two control loops. The tune up process of the PID controller that controls the dc-link voltage, the low speed loop, is presented here. Figure 4.12 shows the equivalent circuits of the qZSI with battery storage integration during the active and ST states.

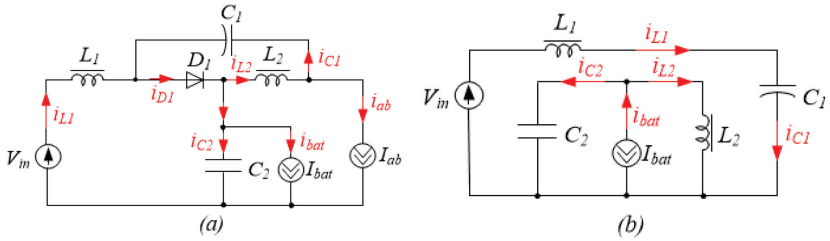



*Figure 4.12 Equivalent circuits: active state (a); ST state (b).*

To tune up the PID controller the small signal models, commonly used to analyze the dynamic behavior of the system, of the qZSI were calculated, Figure 4.12.

In a steady-state mode, it is assumed that the *Vin* and *Vab* variables are constant. The state equation of a system:

$$K\frac{dx(t)}{dt} = Ax(t) + Bu(t)\ ; \tag{4.55}$$

$$y(t) = Cx(t) + Eu(t)\ . \tag{4.56}$$

where,
1) All of the state variables *x(t)* in the considered case are:

$$x(t) = [i_{in}; i_{L2}; i_{L4}; v_{C1}; v_C; v_{C4}] \tag{4.57}$$

2) The inductor winding voltage and capacitor currents:

$$K = \begin{bmatrix} 2L & 0 & 0 & 0 & 0 & 0 \\ 0 & L & 0 & 0 & 0 & 0 \\ 0 & 0 & L & 0 & 0 & 0 \\ 0 & 0 & 0 & C & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{C}{2} & 0 \\ 0 & 0 & 0 & 0 & 0 & C \end{bmatrix} \tag{4.58}$$

3) The independent inputs of the system are:

$$u(t) = \begin{bmatrix} Vin(t) \\ Vab(t) \end{bmatrix} \tag{4.59}$$

4) Linear combination of the elements of the *x(t)* and *u(t)* are expressed as *y(t)*.

5) The constant of the proportionality is expressed through A,B,C,E.

The small signal state equations of the qZSI in the active state *($D_a$)*, Figure 4.13*a,* are:

$$\begin{cases} L\dfrac{di_{in}}{dt} = V_{in}(t) - 2R\cdot i_{in}(t); \\ L\dfrac{di_2}{dt} = \dfrac{vC(t)}{2} - R\cdot i_2(t); \\ L\dfrac{di_4}{dt} = \dfrac{vC(t)}{2} - R\cdot i_4(t); \\ C\dfrac{dvC_1}{dt} = -i_{in}(t); \\ C\dfrac{dvC}{2dt} = -i_2(t); \\ C\dfrac{dvC_4}{dt} = -i_{in}(t). \end{cases} \rightarrow A1 = \begin{bmatrix} -2R & 0 & 0 & 0 & 0 & 0 \\ 0 & -R & 0 & 0 & 1/2 & 0 \\ 0 & 0 & -R & 0 & 1/2 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}; \quad (4.60)$$

The constant of the proportionality C consists of the inputs $\begin{bmatrix} i_{in} \\ v_c \end{bmatrix}$, *B1* and *B2* consist of the $\begin{bmatrix} V_{in} & i_{ab} \end{bmatrix}$.

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}; \; B1 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}. \quad (4.61)$$

The small signal state Eqs. of the qZSI in the ST state (Ds), Figure 4.13b, are:

$$\begin{cases} L\dfrac{di_{in}}{dt} = V_{in}(t) - vC(t) + 2R\cdot i_{in}(t); \\ L\dfrac{di_2}{dt} = R\cdot i_2(t) - \dfrac{vC_1(t)}{2}; \\ L\dfrac{di_4}{dt} = R\cdot i_4(t) - vC_4(t); \\ C\dfrac{dvC_1}{dt} = i_2(t) - i_{ab}(t); \\ C\dfrac{dvC}{2dt} = i_{in}(t) - i_{ab}(t); \\ C\dfrac{dvC_4}{dt} = i_4(t) - i_{ab}(t). \end{cases} \rightarrow A2 = \begin{bmatrix} 2R & 0 & 0 & 0 & -1 & 0 \\ 0 & R & 0 & -1 & 0 & 0 \\ 0 & 0 & R & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix}; \quad (4.62)$$

$$B2 = \begin{bmatrix} 1 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -1 \\ 0 & -1 \\ 0 & -1 \end{bmatrix}. \tag{4.63}$$

The average signal state equations are xpressed as:

$$\begin{cases} A_{av} = \dfrac{d_s(t)\big|_T}{2}(K^{-1}A_1) + \dfrac{d_a(t)\big|_T}{2}(K^{-1}A_2); \\ B_{av} = \dfrac{d_s(t)\big|_T}{2}(K^{-1}B_1) + \dfrac{d_a(t)\big|_T}{2}(K^{-1}B_2); \\ C_{av} = C. \end{cases} \tag{4.64}$$

where the sum $d_s(t)+d_a(t)$ *was assumed equaled to 1.*

The average state consists of the constant component and variable component:

$$\begin{cases} x(t)\big|_T = X + \tilde{x}(t); u(t)\big|_T = U + \tilde{u}(t); y(t)\big|_T = Y + \tilde{y}(t); \\ d_s(t)\big|_T = D_s + \tilde{d}(t); d_a(t)\big|_T = 1 - D_s - \tilde{d}(t). \end{cases} \tag{4.65}$$

Based on Eqs. (4.59)-(4.65), Eq. (4.55) can be rewritten as:

$$K\frac{d}{dt}\tilde{X} = A\tilde{x} + B\tilde{u} + [(K^{-1}A_1 - K^{-1}A_2)X + (K^{-1}B_1 - K^{-1}B_2)U]\cdot\tilde{d}\,. \tag{4.66}$$

By applying the Laplace transformation to Eq. (4.23) the small signal model is derived:

$$\begin{cases} x(s) = (s\cdot I - A)^{-1}\cdot B\cdot\tilde{u}(s) + (s\cdot I - A)^{-1}\cdot M\cdot\tilde{d}(s); \\ M = (K^{-1}A_1 - K^{-1}A_2)X + (K^{-1}B_1 - K^{-1}B_2)U; \\ y(s) = C\cdot\tilde{x}(s) = C(s\cdot I - A)^{-1}\cdot B\cdot\tilde{u}(s) + C(s\cdot I - A)^{-1}\cdot M\cdot\tilde{d}(s). \end{cases} \tag{4.67}$$

where *I* is - diagonal matrix.

Finally, we obtain four transfer functions. The first couple of transfer functions express the dependence of the controlled parameters on the ST duty cycle variation. The second couple of the transfer functions express the dependence of the controlled parameters on the voltage variation.

$$\left[\begin{matrix} G_{id}(s) \\ G_{vd}(s) \end{matrix}\right]_{\tilde{u}(s)=0} = C(s\cdot I - A)^{-1}\cdot M\,;\ \left[\begin{matrix} G_{iu}(s) \\ G_{vu}(s) \end{matrix}\right]_{\tilde{d}(s)=0} = C(s\cdot I - A)^{-1}\cdot B. \quad (4.68)$$

The PID controller is used to control the dc-link voltage by changing the ST duty cycle; therefore, in order to tune up the PID controller the following transfer function is considered:

$$G_{vd}(s) = C(s\cdot I - A)^{-1}\cdot M. \quad (4.69)$$

The transfer function of the PID controller is:

$$TrF_{PID} = K_p + \frac{1}{sK_i} + sK_d. \quad (4.70)$$

And the total transfer function of the whole system is:

$$TrF_{voltage} = G_{vd}(s)\cdot TrF_{PID}. \quad (4.71)$$

The transformation from the s domain to the z domain was performed by means of the backward discretization method.

Figure 4.12 shows the Bode plot diagram of the $TrF_{voltage}(z)$. Figure 4.13 shows the Bode plot diagram of the PID controller with selected stable parameters.

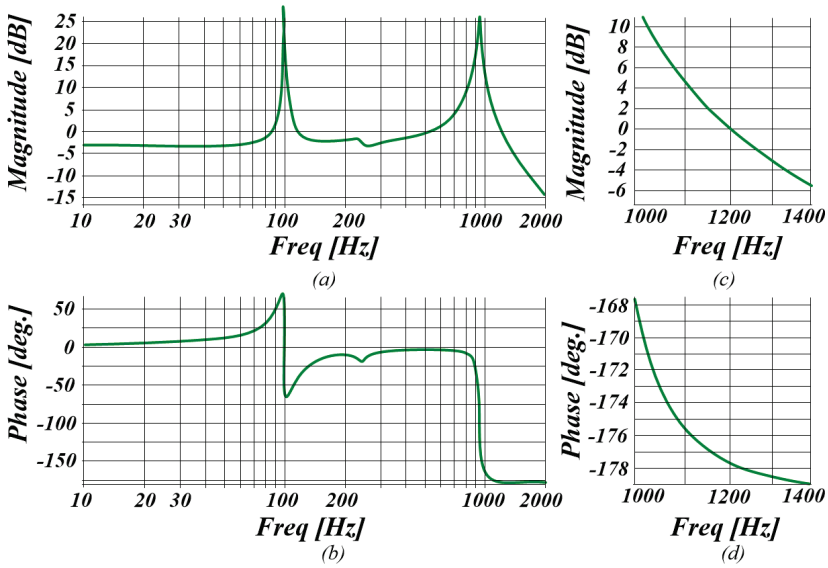



*Figure 4.13 Bode plot diagram of the $TrF_{voltage}(z)$.*

### 4.2.3 Battery storage control system design combined with the active decoupling approach

High penetration level of RES into DGS leads to energy fluctuation. For that reason, the integration of the energy storage into RES is a common requirement, which allows control of the power balance between the input and the output sides. In Section 3.2.3 it was shown that the integrating of the interface energy storage circuit into the

considered topology is a good solution, because the system is able to provide power even if the input source is absent. Moreover, it is possible to combine the performance of two desired functions - the power balance and the APD - into one circuit, Chapter 3, Figure 3.9. The same idea is reported in [103] but their solution cannot provide power if the power of the input source is twice smaller from that of the nominal.

The proposed solution is presented in [PAPER-VI] where the investigated topology was considered under three different output power demands and it was shown that the active power decoupling circuit was able to provide the power balance and the mitigation of the DFR under different mentioned cases. Also, it is shown in [PAPER-VI] that the sampling frequency and digital delay could cause critical influence on the stability of the system.Figure 4.14 shows the topology of the single-phase three-level NPC qZSI with battery storage and Figure 4.15 presents the control strategy.

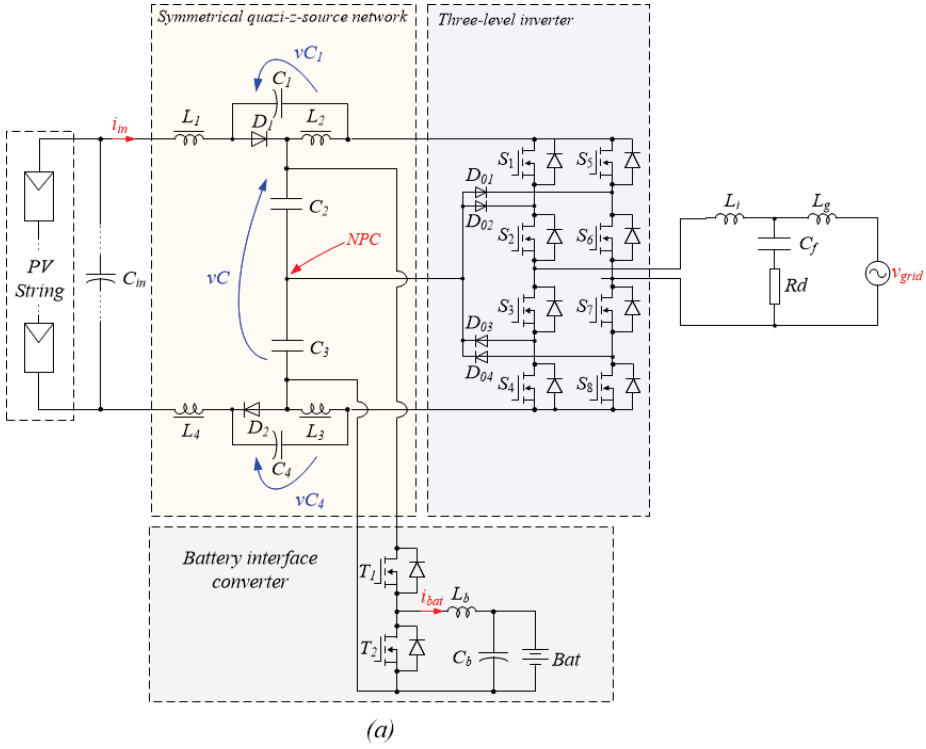



*Figure 4.14 Single-phase three-level NPC qZSI with BIC.*

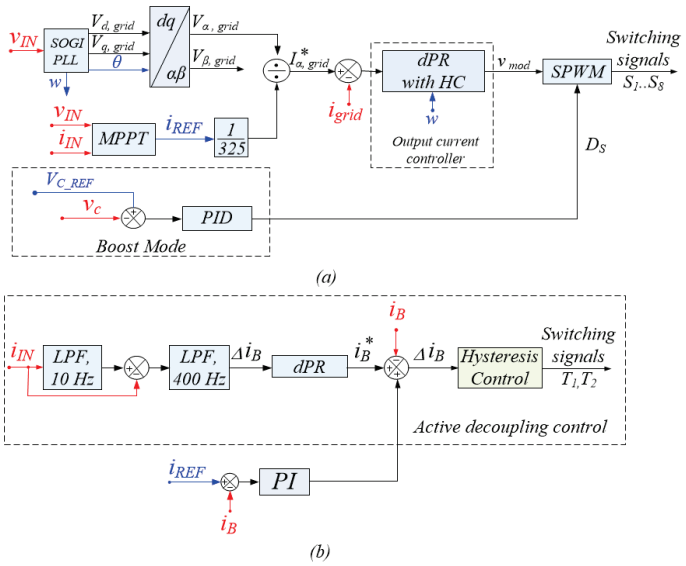



*Figure 4.15 Control strategy.*

## 4.3 Summary of Chapter 4

This chapter has addressed hardware and software design approaches. First of all, two possible approaches how to mitigate the DFR of the input power were considered. Simulation results revealed that both approaches are able to cope with this task. Based on the comparative analyses, the APD is more preferable since it has two benefits: lower energy stored in capacitors and lower total voltage stress on the semiconductor devices, in comparison to the considered PPD. The APD circuit improves the efficiency the MPPT block along the reduction of the efficiency of the system by adding extra power losses caused in its circuit. The integration of the APD function into BIC allows compensation of the power losses caused by the operation of the battery circuit. At the same time, using an auxiliary circuit just for the APD function is not recommended. It may improve the overall power density, but deteriorate the efficiency and increase the cost. Such conclusions are in correlation with industrial string solar inverters where power decoupling is mostly realized by passive components.

Software optimization consists of the grid-connection and the dc-link control. The tuning up process of a current controller was presented. Based on the simulation results, the optimization of the start-up transients was proposed, which allows reduction of a current spike during start-up and avoiding the launch of the current protection function. Also, the tuning up process of the PID controller is presented based on the small signal model of the qZSI.

# 5 Application example of qZSI with battery storage integration

In this chapter, the experimental prototype of the single-phase three-level NPC qZSI with BIC will be tested under different conditions. The aim is to obtain the experimental results of the battery utilization, to test the different operation modes of the system (with MPPT, without MPPT) and to determine the CEC of the tested inverter.

## 5.1 Generalizations of the software and hardware design

The experimental prototype was built based on the scheme in Figure 5.1. Since one PV panel cannot produce the required level of power, there are different ways how to connect them for achieving the desired level of power. For residential application, the string PV system, which allows an increase of the voltage production, is widely used. For the selected topology, a PV installation of 11 series connected PV panels (HSPV185Wp) is sufficient [104]. The voltage at the Maximum Power Point (MPP) under maximum solar irradiance is about 397.1 V in ideal conditions, which corresponds to the back mode of the converter. The boost mode is required during lower solar irradiance (bad weather, a fog etc.) and during partial shadowing. The partial shadowing mostly affects the current production but the reduction of current generation will affect the shifting of MPP and as a result, the voltage production. At low power production, the implementation of battery storage allows supporting the power grid by discharging it, or in an opposite case, by charging battery storage. In the considered case, the lead acid battery storage unit was used with nominal voltage 96 V and capacity about 7 Ahour.

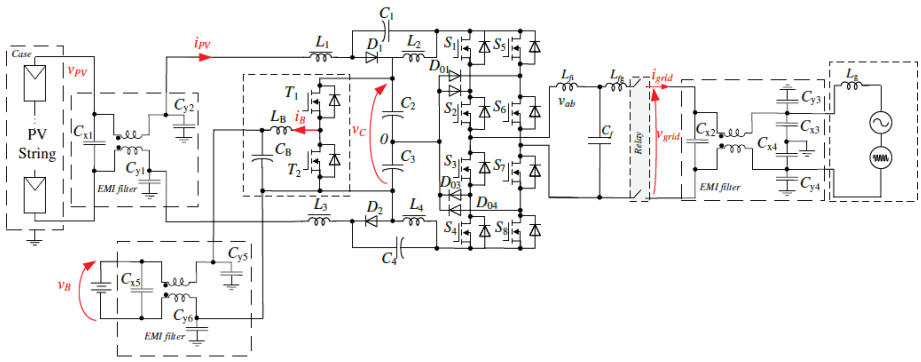



*Figure 5.1 Single-phase three-level NPC qZSI with BIC.*

This choice is not an optimal solution because lead acid battery is sensitive to the current ripple, the LiFePO4 battery or Li4Ti5O12 would be more reasonable to use but their cost is much higher than that of the lead acid battery. To disconnect the PEC from the grid, two relays were integrated to the output side.

In order to suppress the leakage current, two filtering approaches were used. To suppress common mode noise, the y capacitors were used. To suppress the differential mode noise, the x capacitors and coupled inductors were used.

Figure 5.2 shows the structure of the assembled prototype in a 3U box.

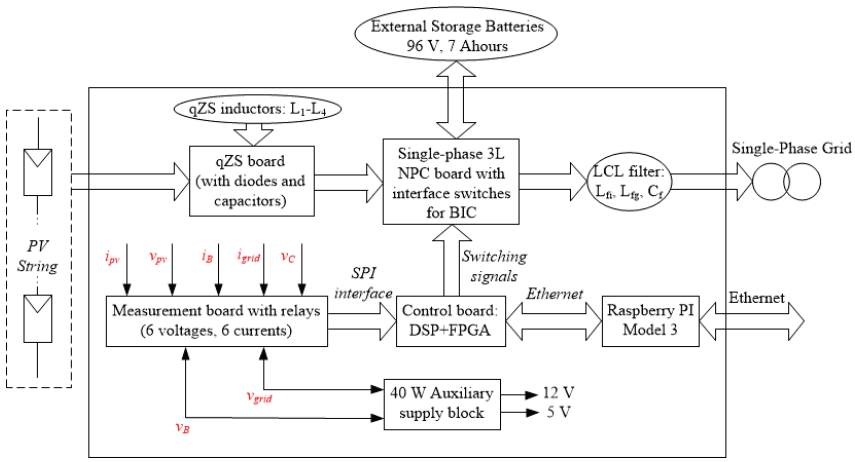



*Figure 5.2 The block structure of the study prototype.*

It consists of four main PCB boards: power board, measurement board, control board (bottom board, top board) and external qZS inductors, storage inductors, inductors of output filters, and a battery. There is a possibility for intercommunication with other similar devices connected to the same grid through Ethernet connection. To provide remote control and energy management, the RPI3 board was used.

The measurement board consists of current sensors TLI4970 with digital output from Infineon and with simple resistor dividers as voltage sensors. For galvanic isolation, operational amplifiers ACPL-C87A and Analog-to-Digital Converters ADC LTC1864CS8 from Linear Technologies were used, which send data to the bottom control board through the SPI interface.

The Field Programmable Filed Array (FPGA) from Altera Cyclone IV EP4CE6E22C8 located on the bottom board was responsible for the communication between the measurement board and the top control board. The FPGA was also responsible for the formation of the switching signals for transistors. To provide the power immunity, the buffer SN74LVCC was used. It converted the voltage from 3.3 V on the FPGA side to 5 V on the outside.

The Digital Signal Processor (DSP) – STM32F417VG is located on the top board. This type of the DSP was selected because it has a 32 bit processor and a MAC controller that allows the implementation of Ethernet communication, SPI and one I2C interface and FPU. To provide the compatibility between MAC and Ethernet, the DP83848 was used.

The computational process was divided between DSP and FPGA in order to avoid additional outlay and fasten the computational process. Due to the FPGA a very high switching frequency of semiconductor devices is achievable. At the same time, computational frequency is limited, especially in a low cost control system applied for low power devices.

The remote control was realized by means of the RPI3 microcomputer with a standard micro - USB connector and Ethernet connection.

Each of these parts can work independently and communicate through SPI. Such combination provides an effective performance of any complex control.

## 5.2 Description of the experimental setup

Figure 5.3 shows the experimental prototype and Table 5.1 presents its parameters.

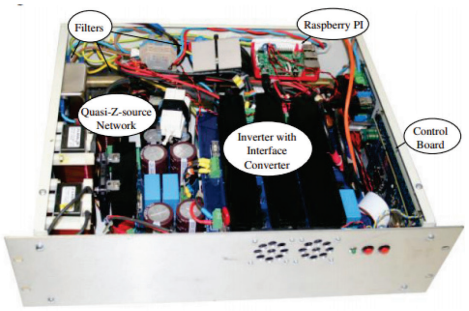



*Figure 5.3 Experimental prototype.*

*Table 5.1 – Parameters of the prototype*

| Parameter | Value |
|---|---|
| Capacitances from capacitors $C_1$ and $C_4$ | 2.70 mF |
| Capacitances from capacitors $C_2$ and $C_3$ | 1.47 mF |
| Inductances from inductors $L_1$ and $L_3$ | 400 µH |
| Inductances from inductors $L_2$ and $L_4$ | 200 µH |
| 1st filter inductance Li (inverter) – LCL | 440 µH |
| Filter capacitance $C_f$ – LCL | 15.47 µF |
| 2nd filter inductance Lg (grid) – LCL | 220 µH |
| Switching frequency (MOSFET devices) | 100 kHz |
| Sampling frequency (DAC and ADC converters) | 8 kHz |
| Inverter transistors S1,…,S8 | IPW65R041CFD |
| Storage interface transistors T1,...,T2 | CMF20120D |
| NPC diodes and qZS diodes | C2M0080120D |
| MOSFETS drivers | ACPL-H342 |
| AD converters | LTC1864CS8 |

## 5.3 qZSI with remote control for residential application

The qZSI with remote control was tested in the Laboratory of Power Electronics Group in Tallinn University of Technology and in Antwerp for the project horizon 2020 in cooperation with Ubik Solution.

Further, the results obtained will be described.

### 5.3.1 Classical grid-connected mode with MPPT

The solar irradiance influences the MPP, Figure 5.4. With the reduction of solar irradiance, the MPP is reducing as well.

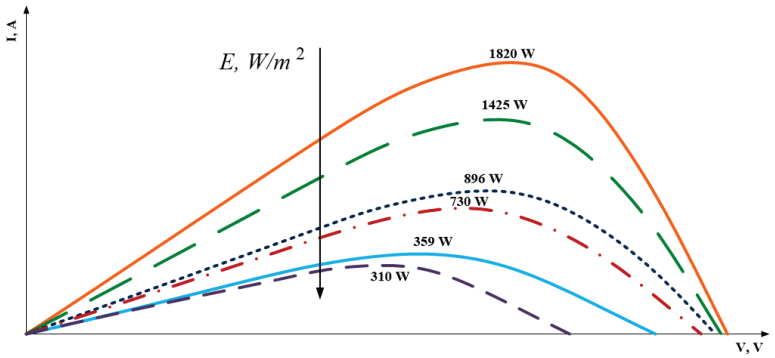



*Figure 5.4 MPP under different solar irradiances.*

Table 5.2 presents the experimental results of the efficiency of the PV system and the converter under different solar irradiations in %.

*Table 5.2 – The experimental parameters under different solar irradiations*

| № | $I_{SC}$ | $I_{MMP}$ | $V_{OC}$ | $V_{MMP}$ | $E_{MMP}$ | $E_{ff}$ | E,% |
|---|---|---|---|---|---|---|---|
| **1** | 1.2 | 1.1 | 350 | 280 | 94 | 90 | 10 |
| **2** | 1.25 | 1.15 | 390 | 310 | 95 | 92 | 20 |
| **3** | 2.2 | 2.1 | 440 | 340 | 92 | 96 | 30 |
| **4** | 2.6 | 2.5 | 450 | 350 | 97 | 96.2 | 50 |
| **5** | 4 | 3.9 | 455 | 355 | 98 | 96.4 | 75 |
| **6** | 5 | 4.9 | 460 | 360 | 99 | 96.5 | 100 |

Table 5.2 shows that the efficiency of the MPPT is increasing with the increase of the solar irradiance. The reason is that the investigated system was tuned up to track the MPP at the maximum solar irradiance curve by means of P&O method [105]. Solar irradiance decreasing leads to smoother slope of the curve; therefore, it is more difficult to detect the MPP.

The efficiency of the tested converter was increasing with an increase of the solar irradiance. The parameters of the system were chosen to achieve the maximum efficiency at the maximum solar irradiance; therefore, at the reduction of the power, the power losses stay at the same value, which leads to the reduction of the efficiency of the converter.

CEC coefficient of the PEC was calculated by the following equation [106]:

$$CEC = 0.04 \cdot Eff\,10\% + 0.05 \cdot Eff\,20\% + 0.12 \cdot Eff\,30\% + 0.21 \cdot Eff\,50\% + \\ +0.53 \cdot Eff\,75\% + 0.05 \cdot Eff\,100\% \quad (5.1)$$

The full efficiency of the tested converter under different solar irradiances based on Eq. (5.1) is:

$$FullEffConv = 96\% \tag{5.2}$$

In order to estimate the CEC of the designed converter it was tested at the nominal input power point under changing power load Table 5.3 presents the experimental results.

The CEC coefficient was calculated based on Eq. (5.1). The CEC of the tested PEC was 97.6%.

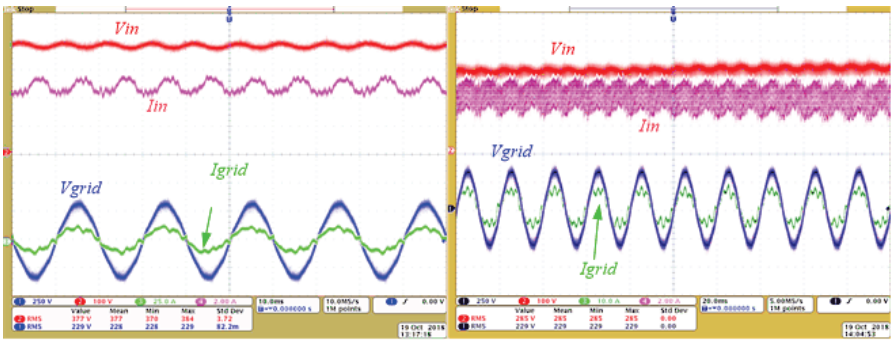
Figures 5.5*a,b* show the experimental results of the output power equal to 1800 W and 900 W correspondingly. It can be noticed that the quality of the grid current was deteriorated because the low current is harder to control, especially when the current controller was tuned up to control the nominal grid current.

Figure 5.6*a* shows that the heat distribution during the operation time corresponds to Figure 5.5.

*Table 5.3 Experimental parameters under different load power*

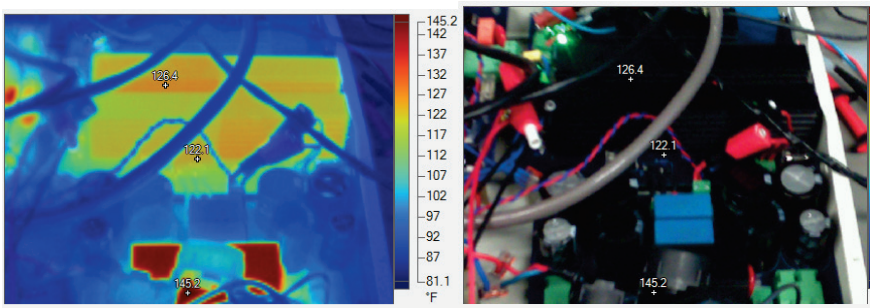
| № | $V_{in}$ | $P_{load}$ | $E_{conv}$ | P,% |
|---|---|---|---|---|
| **1** | 360 | 360 | 96.4 | 10 |
| **2** | 360 | 720 | 96.9 | 20 |
| **3** | 360 | 1080 | 97.2 | 30 |
| **4** | 360 | 1800 | 97.6 | 50 |
| **5** | 360 | 2700 | 98 | 75 |
| **6** | 360 | 3600 | 97.2 | 100 |

Figure 5.6*b* shows that most of the hot parts of the system were inverter switches and impedance diodes.




*(a)* *(b)*

*Figure 5.5 Experimental results: input voltage and current, grid voltage and current.*




*(a)* *(b)*

*Figure 5.6 Experimental results of the thermos camera.*

### 5.3.2 Reference active power supporting

Figure 5.7 shows the experimental results of the tested prototype to provide the opportunity for supporting the active power.

During the time intervals *a* and *b*, the system operated in the MPPT mode. During that time, the PV system was producing maximum of the possible power.

During the interval *b,* the battery was charging; as a result, the active power was reduced for the part that was equal to the charging power of battery.

During the interval *c*, the system was not working. At 16:18:40, the power production by the PV system was set 1750 W while the grid power demand was equal to 1500 VA, interval *e*. Since the power produced by the PV system had some slope in order to fasten the transient process of transferring power to the grid, the battery was discharging during the time interval *d*. After that, the battery was charging. At time 16:21:32, the reference power produced by the PV system was changed to 2100 W while the grid power demand was 1750 VA, interval.

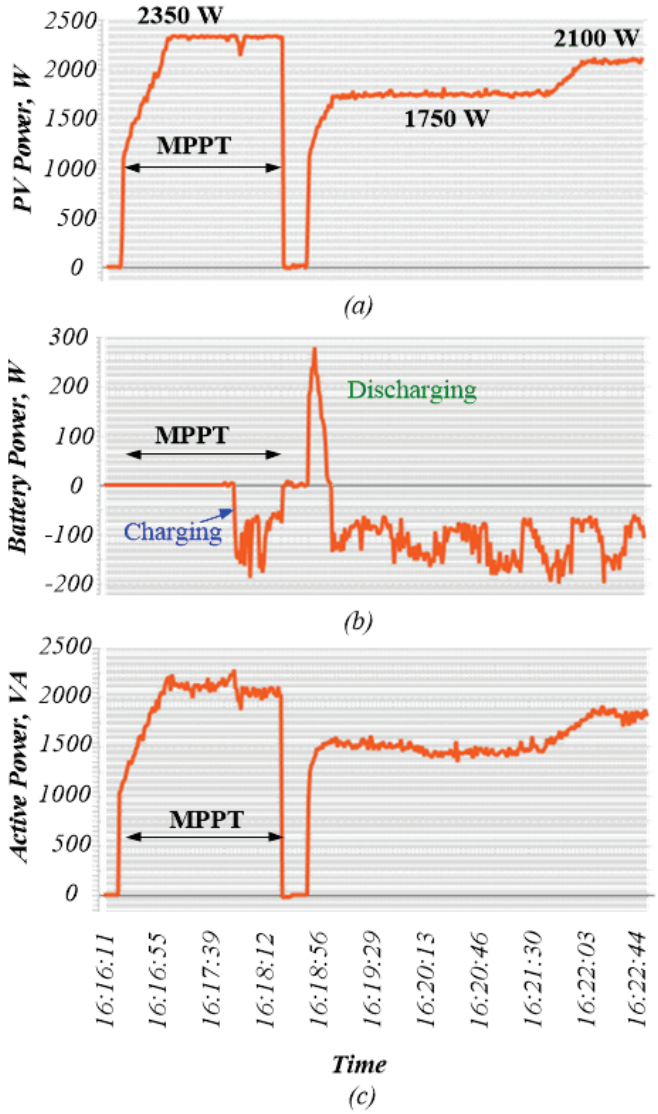



*Figure 5.7 Experimental results: PV power (a), battery power (b), active power (c).*

### 5.3.3 Battery storage utilization for reference grid power supporting

The experimental prototype was tested for provision of power balance by utilization of the battery storage.

Figure 5.8 shows that during the time interval emphasized in circle *1*, the whole active power was received from the PV system and the battery, which means that the battery helps to achieve the power balance during the time when the PV power is insufficient for the grid. The time interval *2* shows the case when only the battery fed the power to the grid, the PV system produced no power. This finding confirms the theoretical and simulation results that the proposed BIC was able to provide power at the absence of the input source.

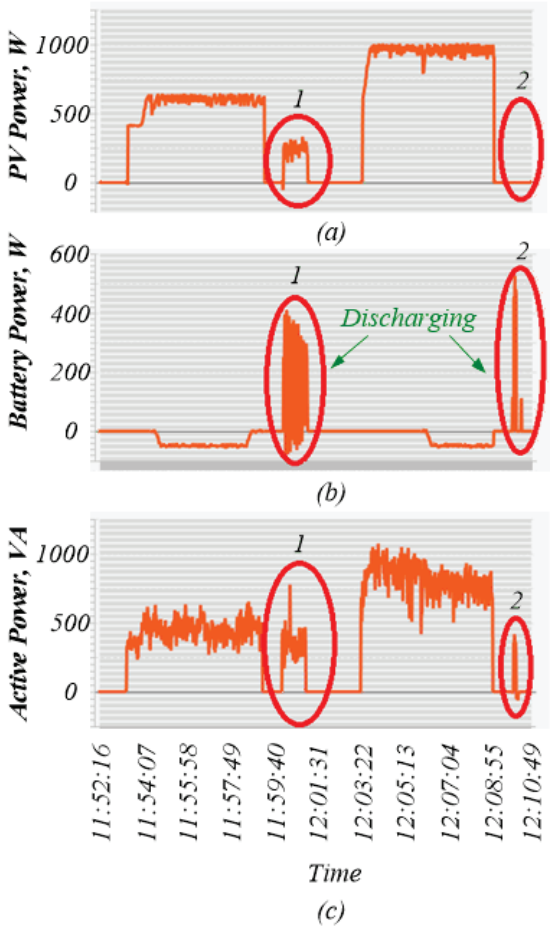



*Figure 5.8 Experimental results: PV power (a), battery power (b), active power (c).*

## 5.4 Summary of Chapter 5

In this chapter presented the description of the built prototype of the qZSI with BIC and remote control. The full efficiency of the tested qZSI with BIC under different solar irradiances was 96%. The CEC was 97.6%. The experimental results showed that qZSI with BIC was able to operate in different modes (with MPPT and without MPPT) and it was capable of providing the power even if the input source (during night period) is absent. Based on the experimental results, the proposed topology can be applied for residential PV application.

# 6 Conclusions and Future work

## 6.1 Conclusions

The main aim of the PhD thesis was to design the residential PV inverter with storage integration. The topologies based on ISN allowed to combine two power conversion steps into one and to regulate the input voltage in a wide range. Due to the ST immunity those topologies improve the reliability of the system.

The battery integration is a demanded part of the residential PV inverter. The comparison between the APD and PPD approaches along with novel BIC were presented in this PhD thesis. The optimal solution was selected for industrial implementation.

As the main results of this thesis, the author claims the following:

- The single-phase three-level NPC qZSI with BIC was proven as a better solution among inverters with ISN networks. This solution provides CIC along with the low input current ripple and the required lower size of the passive components among other ISNs. Moreover, the three-level NPC inverter allowed the reduction of the voltage stress on the inverter's switching devices twice and as a result, using conventional Si MOSFET transistors with increased switching frequency; therefore, three-level output voltage and high switching frequency resulted in the improved quality of the power at the PCC and increased reliability due to the ST immunity.
- The comparison of APD and PPD approaches revealed that the considered APD required lower value of the capacitance; provide lower total voltage stress on the semiconductor devices, but required higher value of the inductance. At the same time integration of APD method was not recommended for industrial application due to the increased cost and additional power losses caused by the APD circuit. It was shown that for industrial application it would be more reasonable to apply a simple PPD approach based on the capacitor.
- The proposed novel topology with BIC allowed combining the performance of two different functions at the same time: power balance and mitigation of the DFR of the input power. Moreover the proposed BIC was able to provide power even when the input source was absent.
- The control system for solar inverter with storage battery integration was designed and tuned. The novel tuning approach of the optimized dPR that allows avoiding triggering the current protection during start-up and providing stable operation despite on significant latency caused by control system was proposed.
- Finally, the qZSI with the BIC and the remote control was built, and tested in the Laboratory of the Power Electronic Group in Tallinn University of Technology and in Antwerp for the project horizon 2020 in cooperation with Ubik Solution Company.

The experimental results of the built inverter demonstrated an efficiency of 96%, and the CEC that of 97.6% under different irradiances. The prototype could operate in different modes (with MPPT and without). The experimental results demonstrated that the built up qZSI with BIC can be applied for residential PV application.

## 6.2 Future work

Future work consists in using theoretical and practicl thesis outcomes for further industrial implementation. Advanced research work must be conducted in the cost optimization and reliability assestmant.

# 7 Conclusiones y Trabajos futuros

## 7.1 Conclusiones

El principal objetivo de esta tesis doctoral es diseñar un inversor PV residencial con almacenamiento integrado. El inversor basado en el ISN fue seleccionado como una solución adecuada para aplicaciones residenciales con integración de almacenamiento en baterías. Las topologías basadas en ISN permitieron combinar dos etapas de conversión de potencia en una sola y regular la tensión de entrada en una amplia gama de valores. Esta topología mejora la estabilidad del sistema debido a la inmunidad de ST. También se concluye que la integración de la batería es una parte imprescindible para el inversor PV residencial. Además, se ha propuesto la solución óptima para ser implementada en el sector industrial. También se expone una comparación entre APD y los nuevos enfoques de PPD.

Los principales resultados de esta tesis son los siguientes:

- El inversor de tres niveles NPC qZSI con BIC es la mejor solución de entre los inversores con redes ISN. Esta solución proporciona CIC junto con una baja corriente en alterna y una reducción del tamaño de los componentes pasivos de la red del ISN. Además, la topología de tres niveles permite utilizar transistores MOSFET de silicio con una mayor frecuencia de conmutación, con la consiguiente mejora de la calidad de la potencia en el PCC y el aumento de la fiabilidad debido a la inmunidad ST.

- La comparación de APD y de PPD reveló que APD requiere el menor valor de la capacidad posible: proporciona tensiones inferiores en los elementos semiconductores, en contraposición requiere el valor más alto de la inductancia. Al mismo tiempo la integración del método APD no se recomienda para la aplicación industrial debido al elevado coste y las pérdidas de potencia adicionales causadas por el recorrido APD. Se demostró que para la aplicación industrial sería más razonable aplicar un enfoque de PPD simple basado en condensadores.

- La nueva topología propuesta con BIC permite combinar dos funciones diferentes al mismo tiempo: equilibrio de potencia y mitigación del DFR de potencia en la entrada. Además, el BIC propuesto es capaz de proporcionar potencia aun cuando la fuente de energía no está disponible.

- El sistema de control del inversor solar con acumulador integrado se ha diseñado y calibrado correctamente. El nuevo proceso de sintonización optimizado de dPR evita la actuación de la protección de corriente durante el arranque y proporciona una operación estable a pesar de los tiempos de latencia del control.

- Finalmente, el qZSI con BIC se construyó y se provó en el laboratorio de Power Electronic Group en la universidad de Tallin de Tecnología y en Antwerp para el proyecto H2020 en cooperación con Ubik Solutions.

Los resultados experimentales del inversor construido demostraron que bajo diferentes niveles de irradiancia solar su eficacia es iguala al 96% y el CEC al 97,6%. Además, el prototipo podría funcionar en diferentes modos (con MPPT y sin MPPT). Los resultados

experimentales demostraron que el qZSI con BIC propuesto se puede aplicar en instalaciones PV residenciales.

## 7.2 Trabajos futuros

Como trabajos futuros se propone utilizar los resultados teóricos y prácticos de la tesis para su aplicación industrial. Otra línea de investigación consistiría en optimizar el tamaño de los componentes pasivos. Además, se podría investigar como optimizar los costes y mejora de la fiabilidad de los dispositivos desarrollados.

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# Abstract

## Quasi-Z-Source Based String Inverter for Residential Photovoltaic Application

Nowadays the industrial PEC for residential PV application is based on the wellknown DC-DC boost converter and DC-AC inverter. In such topologies, the power goes through two conversion steps (DC-DC and DC-AC), therefore it is necessary to prevent the ST state by introducing the dead-time between the switching of the inverter switches that complicates the control system.

The solar PEC has the PV system in the input side, which leads to the following: the PEC should be able to regulate the input voltage in a wide range, provide CIC and have battery storage especially for residential application. The main task of the battery is to provide the power balance between the input and the output power in case of power misbalance that can occur between them. It can be caused by changing of the operation point of the PV system that could be affected by different reasons (solar irradiance/temperature variation) or load variation. Also, the battery storage should be able to provide the power when the input power is absent, for instance, during dark periods.

High DFR of the input power in single-phase inverters deteriorates the efficiency of the MPPT. In order to reduce the DFR of the input power, usually the E-cap with high value of capacitance in the input side is used. This solution has some drawbacks, the E-cap is the weakest part of the whole system; it is very sensitive to the current ripple and the capacity of the E-cap is reducing with time. As a result, generally it should be replaced every five years. In order to use other types of the capacitor such as film or ceramic, it is necessary (based on the market supply capabilities) to reduce the required value of capacitance of the decoupling capacitor. In order to achieve this goal, different approaches of the power decoupling (which in general can be divided into two types: the PPD and the APD approaches) have been proposed in the literature.

All the points above allow us to improve the efficiency, the reliability of the system, but the main task of the solar PEC is to provide the required quality of the power at the PCC with all discussed features.

This work was dedicated to the novel concept of the PEC based on the ISN. The PEC has benefited from qZSN through such positive properties as ST immunity, CIC. To provide the required power to the grid the BIC was proposed, which is able to provide the power even without the input source. To achieve the required quality of the grid current, the dPR controller with the HC circuit was selected; to avoid the current spike during the start-up period, which may cause the current trigger protection, the optimization process of the dPR controller was proposed. To stabilize the dc-link voltage during the boost mode, the PID controller was used. To compensate the additional power losses caused by BIC, the APD approach realized by means of the specific control strategy of the BIC was proposed.

The theoretical results were confirmed by experimental results that were achieved by building up the qZSI with a BIC prototype. The tests showed that the designed qZSI with BIC can be applied for residential PV application.

# Kokkuvõte

## Kvaasi-impedants tüüpi allikaga muundur kodumajapidamistes kasutatavatele päikesepaneelidele

Kaasaegsed tööstuslikud päikesepaneele teenindavad muundurid põhinevad hästi tuntud pinget tõstval alalispingemuunduril ja vaheldil. Selliste skeemilahenduste korral muundatakse elektrienergiat kaks korda (alalis/alalis ja alalis/vahelduv) ning lühiste vältimiseks kasutatakse juhtalgoritmides erinevate transistoride lülituste vahel nõndanimetatud "keelatud perioodi" (dead time), mis muudab antud seadmete juhtimise keerukamaks.

Kuna päikesepaneele teenindav jõupooljuhtmuunduril on päikesepaneelid sisendpoolel, siis tingib see vajaduse reguleerida laias ulatuses sisendpinget ja salvestada elektrienergiat. Akusalvesti põhiline ülesanne on sisend- ja väljundvõimsuse balansi tagamine. Võimsusbalanss võib rikutud saada näiteks päikese-energiasüsteemi tööpunkti muutmisest päikesekiirguse intensiivsuse, temperatuuri või koormuse muutumise tagajärjel. Salvesti tagab energiavarustuse ka päikesevalguse puudumise korral.

Kõrge sisendvoolu pulsatsioon vähendab ühefaasiliste vaheldite maksimaalse võimsuspunkti jälgimise tõhusust. Pulsatsiooni vähendamiseks kasutatakse tavapäraselt suure mahtuvusega elektrolüütkondensaatoreid seadme sisendis. Samas on selle lahenduse puuduseks see, et elektrlüütkondensaator on kogu süsteemi nõrgim lüli, kuna ta on väga tundlik suure voolupulsatsiooni suhtes. Elektrolüütkondensaatorite mahtuvus väheneb kiiresti ning neid tuleks vahetada iga viie aasta tagant. Vahetamaks elektrolüütkondensaatoreid film- või keraamiliste kondensaatorite vastu on vaja vähendada vajaminevat mahtuvust. Selle saavutamiseks on mitmeid võimalusi, millest põhilised on passiivne ja aktiivne võimsuseraldus (passive and active power decoupling). Need meetodid võimaldavad tõsta süsteemi kasutegurit, töökindlust ja energiakvaliteeti.

Käesolev töö on käsitleb uudset impedantsallikaga päikesepaneele teenindava muunduri skeemilahendust. Antud skeemilahendus kätkeb endas mitmeid eeliseid nagu näiteks lühisekindlus ja katkematu sisendvool. Nõutava võimsuse saatmiseks võrku lisati süsteemile ka energiasalvesti, mis võimaldab katkematut toidet ka sisendvoolu puudumisel. Võrguvoolu kvaliteedi tagamiseks kasutati dPR-tüüpi regulaatorit koos spetsiaalse skeemilahendusega. Lsaks loodi töö käigus ka dPR-regulaatori parameetrite optimeerimisprotsess vältimaks käivitamisel tekkivat vooluimpulssi, mis võib omakorda aktiveerida ülevoolu kaitse. Alalispingesiini pinge stabliliseerimiseks pingetõstmisrežiimi korral kasutati PID-tüüpi kontrollerit. Akusalvesti poolt tekitatud energiakao minimeerimiseks kasutati spetsiifilist juhtalgoritmi.

Töö teoreetilisi tulemusi kontrolliti eksperimentaalselt, milleks ehitati kvaasi-impedants tüüpi allika ning energiasalvestiga muundur päikesepaneeelide sidumiseks elektrivõrguga. Katsed näitasid loodud seadmete sobivust kasutamiseks kodumajapidamiste päikeseenergiasüsteemides.

# Abstracto

Actualmente el PEC usado en las instalaciones fotovoltaicas del ámbito residencial, está basado en el convertidor DC-DC y el inversor DC-AC. En estas topologías la potencia pasa por dos etapas de conversión (DC-DC y DC-AC) y existe la necesidad de prevenir el estado ST, introduciendo un tiempo muerto entre la conmutación de los interruptores,
El hecho de que el PEC en cuestión esté conectado a un sistema fotovoltaico conduce a lo siguiente: el PEC debe ser capaz de regular la tensión de entrada en un amplio abanico de posibilidades, proporcionar CIC y tener almacenamiento de baterías, especialmente en su aplicación en el ámbito residencial. La tarea principal de la batería es subsanar el problema de desequilibrio de potencia entre la entrada y la salida. El desequilibrio suele producirse debido al cambio del punto de funcionamiento del sistema fotovoltaico o debido a variaciones de carga. El punto de funcionamiento puede variar por diferentes razones: irradiancia solar o variación de la temperatura. En cuanto, a la batería debe ser capaz de proporcionar la potencia necesaria cuando el sistema fotovoltaico no pueda por si solo, por ejemplo, durante la noche o durante el transcurso de las inclemencias meteorológicas.

El alto DFR en la potencia de entrada en inversores monofásicos empeora la eficiencia del MPPT. Para reducir el DFR de la potencia de entrada se utilizan generalmente E-cap con alto valor de capacidad en el lado de entrada. La solución basada en E-cap presenta ciertos inconvenientes que lo convierten en la parte más débil del sistema, ya que es muy sensible a las pulsaciones y además su capacidad se reduce con el tiempo (con un tiempo de reemplazo de unos 5 años). Existe una necesidad del mercado de reducir la capacidad del condensador de desacoplamiento, por lo que se está sustituyendo por otro tipo de condensadores como pueden ser los films o los cerámicos. Para lograr este objetivo en la literatura se propusieron diferentes enfoques de desacoplamiento de potencia (que en general se pueden dividir en dos tipos: los enfoques PPD y APD).

Todos los puntos mencionados anteriormente permiten mejorar la eficiencia y la fiabilidad del sistema, pero la principal tarea del PEC fotovoltaico es proporcionar una potencia en el PCC con niveles adecuados de calidad.

Este trabajo presenta un novedoso concepto de PEC basado en ISN o qZSN, que permite introducir mejoras en cuanto a la inmunidad en ST y CIC. Para proporcionar la energía necesaria a la red se propuso el BIC, que es capaz de proporcionar energía incluso sin fuente de entrada. Para lograr la calidad requerida en la corriente de red se elige el controlador dPR con circuito HC, el cual permite además evitar los picos de corriente producidos durante el período de arranque, evitando así la actuación de la protección de corriente. A la hora de abordar el problema de estabilizar el pico de la tensión del bus de continua durante el proceso de arranque, se propone un controlador PID, mientras que para compensar las pérdidas de energía adicionales causadas por el BIC se propone el enfoque de APD.

Los resultados teóricos han sidos confirmados por los resultados experimentales obtenidos mediante la construcción del prototipo qZSI con BIC. La realización de los ensayos experimentales demostró que el qZSI diseñado con BIC se puede aplicar en instalaciones PV residencial.

# Appendix

[PAPER-I] J. Zakis, E. Makovenko, H. Zeng, O. Husev, L. Kutt, “qZSI as Synchronverter in Small Scaled Mico-Grid”, *Elektronika ir Elektrotechnika (IF-1.088)*, pp. 58-62, 2017.

# qZS Inverter as Synchronverter in Small-Scale Micro-Grid

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***Abstract*—Focus is on the case study of a synchronveter model use in the qZS inverter working in an islanding operation mode. Main tasks and control principles of a sychronverter in the microgrid are explained.**

**Theoretical assumptions are tested and verified with Psim simulation model with different types and powers of microinverter loads. General waveforms are presented and discussed. Also, the effectiveness of synchronverter implementation is verified by means of grid regulation capability.**

**Additionally, we address the most challenging tasks for further developments and improvements of the qZS inverter based synchronverter in microgrids.**

***Index Terms*—DC-AC power converters; Voltage-source converters; Static power converters; Power quality.**

## I. INTRODUCTION

Introduction of Grid Connected Distributed Power Generation Sources (DEGSs) in modern power systems is increasing [1]. This makes the power electronics interface converter a key element for adjusting power parameters (voltage level, frequency) before injecting it in the grid. For many years, keeping injected power parameters under established standards was not considered critical, because large synchronous generators (typically in hydro power plants or combined heat and power stations) in the system were able to keep stability and constant parameters. Such systems are called centralized.

In recent years, power systems have become decentralized because the number of DEGS in the supply network is dramatically growing and synchronous generator cannot keep the stability of the system and parameters at rated values any more. As a result, new tasks and challenges have been set to grid connected inverters. Inverters should play a more serious role in the power system by keeping constant and improving grid parameters and increasing supply reliability if a synchronous generator failed. The synchronverter that mimics a synchronous machine and inherits its properties in the system has been proposed for solution. The idea of the synchronverter and the implementation of the mathematical model of a synchronous machine in the conventional inverter was proposed in [2]–[13].

DEGSs usually do not provide constant output voltage because primary sources like sun, wind, etc. are changing. A common approach of introducing an intermediate step-up dc-dc converter can be used here to provide rated dc bus voltage. Recent high interest among researchers has resulted in impedance source based inverters in various applications due to their unique properties (shoot-through immunity, high input voltage gain etc.) [14]–[16].

In addition, there is a difference in controlling an inverter in the grid connected mode and in the islanding mode. In the first case, the output controller is a current controller, i.e. PR; PID; Deadbeat; Predictive; Fuzzy Logic, hysteresis. While in the islanding mode, an inverter starts operating as a voltage source, thus the output controller should be a voltage controller. In both modes, the system for synchronization such as phase-locked loop (PLL) should be applied; in the grid-connected mode, to synchronize produced current with grid voltage and in the islanding mode, to generate the desired frequency. In [17] the digital hysteresis controller with PI controller and state feedback was proposed. In [18]–[20] a PI controller was selected to control the output voltage since it showed good performance in *dq* reference frame. The good dynamic behaviour of the whole system during the transient time from the islanding mode to the grid-connected mode was shown in all those papers.

Our aim is to combine the benefits of a synchronverter with an impedance source and more particular quasi-Z-source (qZS) network [21], [22] in the input side. This solution may provide a wide input voltage regulation range along with short circuit immunity, which means enhanced

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reliability.

## II. CASE STUDY SYSTEM DESCRIPTION

This section describes the case study system. Fig. 1 shows the schematic diagram of the micro-grid cell that is disconnected from the central grid. The single-phase quazi-Z Source Inverter (qZSI) in the islanding mode operates as a synchronous generator, which sets frequency and voltage based on the load demand. The microinverter can be connected in parallel to the synchronverter with a different load. It operates in the normal grid-connected mode. The Photovoltaic (PV) string can be considered a power source. In this case, the battery is connected to the dc-link voltage and allows expanding the capabilities of the whole system by charging and discharging in power production at any time.

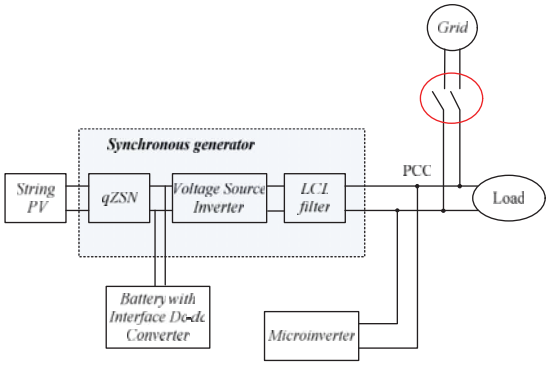


Fig. 1. Schematic diagram of the case study micro-grid.

In case the synchronverter can mimic the behaviour of the synchronous generator, the implementation of the droop control in the microinverter becomes reasonable. The reason is that several microinverters along with the synchronverter can maintain grid balanced and stable.

In this particular case, a scaled small power system is under consideration. A microinverter means an inverter that has much lower power than the synchronverter. Table I shows the parameters of this particular system.

TABLE I. SYSTEM PARAMETERS.

| Parameter | Value |
|---|---|
| Input voltage range of synchronverter | 220 V–400 V |
| Input voltage of microinverter | 400 V |
| Refernce power of microinverter | 325 VA |
| Nominal power of synchronverter | 1 KVA–10 KVA |
| LCL filter of synchronverter | 560 uH; 0.47uF; 200 uH |
| qZS networks parameters | 0.45 mH; 1 mF |
| LCL filter of microinverter | 2.2 mH; 0.47 mF, 1 mH |

## III. CONTROL SYSTEM STRUCTURE AND DESCRIPTION OF IMPLEMENTATION

Figure 2 presents a general circuit diagram of the proposed system which consists of a qZSI and an LCL filter with passive load. $I_a$ is the output current of the qZS inverter, $I_g$ is grid current; in which case it is Voltage Source Generator (VSG) current.

Figure 3(a) and Fig. 3(b) present second order generalized integrators used to extract real ($\alpha$) and imaginary ($\beta$) components to obtain single phase instantaneous active and reactive power. $v_g$ is the grid voltage. Steady state $v_{g\_\alpha}$ is regulated to be the same with $v_g$ because of the negative feedback.

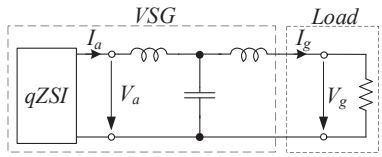


Fig. 2. General circuit diagram of the system.

Steady state $v_{g\_\beta}$ is regulated to be 90° phase shifted compared to $v_{g\_\alpha}$. So $v_{g\_\alpha}$ and $v_{g\_\beta}$ are real and imaginary axis power generated by SOGI. $\omega_0$ is used to determine the resonant frequency.

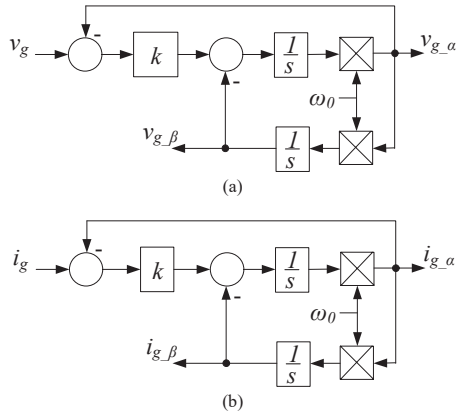


Fig. 3. Second order generalized integrator.

Based on the generated real and complex components as discussed above, single-phase instantaneous power can be calculated by (1) and (2).

Power references $p^*_0$ and $q^*_0$ are obtained from the nominal power:

$$d = \frac{1}{2}\left(v_{g\alpha} \times i_{g\alpha} + v_{g\beta} \times i_{g\beta}\right), \quad (1)$$

$$q = \frac{1}{2}\left(v_{g\beta} \times i_{g\alpha} + v_{g\alpha} \times i_{g\beta}\right), \quad (2)$$

where $v_{g\alpha}$ – $\alpha$ component of grid voltage, $v_{g\beta}$ – $\beta$ component of grid voltage, $i_{g\alpha}$ – $\alpha$ component of grid current, $i_{g\beta}$ – $\beta$ component of grid current. Second order mechanical model is used to emulate the feature of synchronous generator (Fig. 4), where $k_i$, $k_p$ – coefficients of PI regulator, $k_f$ – droop forming coefficient (dependent on real system).

The active inertia $J_a$ is used to emulate the physical inertia [23] of the rotor and active viscous damping coefficient $b_a$ is used to emulate the physical friction of the system. This mechanical emulation is the key benefit of a synchronous generator to build up a stiff and stable grid. Field winding emulation is not implemented since it does not provide the key feature that is mentioned above.

Figure 4 shows the reference voltage generation according to the f-p droop characteristics. It is used to enable primary frequency control such that a system can

have frequency deviation and frequency can be stable with steady state error if the load has been changed. This frequency deviation is sensed by other grid connected inverters so that power should be balanced from those inverters.

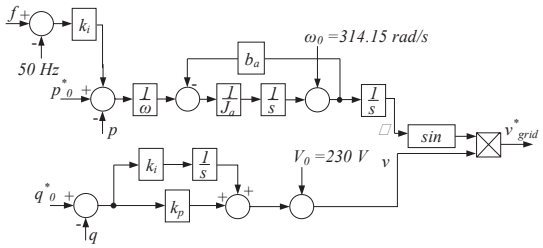


Fig. 4. State block diagram of reference voltage generation with f-P droop characteristics.

Table II summarizes the parameters of the selected f-P droop characteristics.

TABLE II. PARAMETERS OF SELECTED F-P DROOP CHARACTERISTICS.

| Parameter | Value |
|---|---|
| Integral term of PI regulator, $k_i$ | 0 |
| Proportional term of PI regulator, $k_p$ | 0.001 |
| Droop forming coefficient (dependent on real system), $k_f$ | -20000 |
| Active inertia, $J_a$ | 0.05 |
| Active viscous damping coefficient, $b_a$ | 0 |

## IV. CONTROL SYSTEM TURNING OF VSG IN THE SYNCHRONVERTER

Since an inverter in the standalone mode starts to operate as VSG, it means that the output controller should control the quality of output voltage's form and frequency in the first place. Therefore, in order to control the main inverter that is a virtual synchronverter, a Proportional-Resonant (PR) controller was applied.

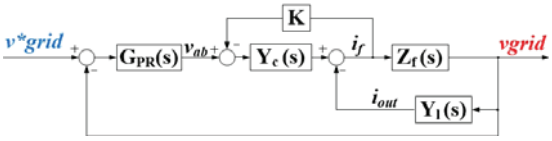


Fig. 5. Equivalent block diagram of VSG.

The transfer function of LCL filter can be expressed through *Vout* = *Vc* and *Vinv*

$$G_{LCL}(s)=\frac{V_C}{V_{inv}}=\frac{Y_iZ_c}{1+Y_iZ_c+Z_cY_n}, \tag{3}$$

where:

$$\begin{cases} Y_i(s)=\dfrac{1}{sL_1}, \\ Y_n(s)=\dfrac{1}{sL_2+R_n}, \\ Z_c(s)=\dfrac{1}{sC}+R_d. \end{cases} \tag{4}$$

The output PR controller's transfer function is

$$G_{PR}(s)=K_{pr}+\frac{sK_{ir}}{s^2+\omega^2}, \tag{5}$$

where $K_{pr}$ is a proportional gain of the controller, selected equal to 1 and $K_{ir}$ is an integral gain of the resonant component selected equal to 600, $\omega$ is fundamental angular frequency. The closed loop transfer function is expressed as follows

$$G_{PRLCL}(s)=\frac{G_{PR}G_{LCL}}{1+G_{PR}G_{LCL}}, \tag{6}$$

Figure 6 presents the zero pole maps of the output transfer function under the condition of a time-varying load.

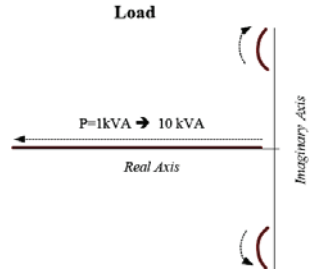


Fig. 6. Map of poles of the transfer function of the output PR controller and LCL filter.

Figure 6 shows that the selected parameters of the PR controller provide stable operation of the system in the whole range of predefined output power.

## V. SIMULATION RESULTS

First of all, the single-phase qZSI is simulated under time-varied load conditions (Fig. 7). The simulation results are shown in Fig. 8.

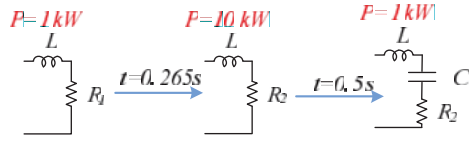


Fig. 7. Different types of load.

Figure 8 shows the load changing during simulation time, the following parameters were selected for simulation: *R1* = 92.7 *Ohm, R2* = 10.6 *Ohm, L* = 0.2 *mH, C* = 0.1 *mF*. Up to 0.265 s – $t_1$ the inverter's output power was 1 kW, the load was active-inductive. At 0.265 s, the demand of power by load was changed to 10 kW – $t_2$. At time 0.5 s, the load demand was changed again up to previous power demand and capacitive character of load – $t_3$ was added.

The simulation results show that inverter is able to produce the current and voltage of the required quality even when the load is varying with time. A problem is encountered with a non- active load when the inverter should be able to synchronize the produced voltage and current in order to reduce the reactive power production that affects the load and increases the energy cost.

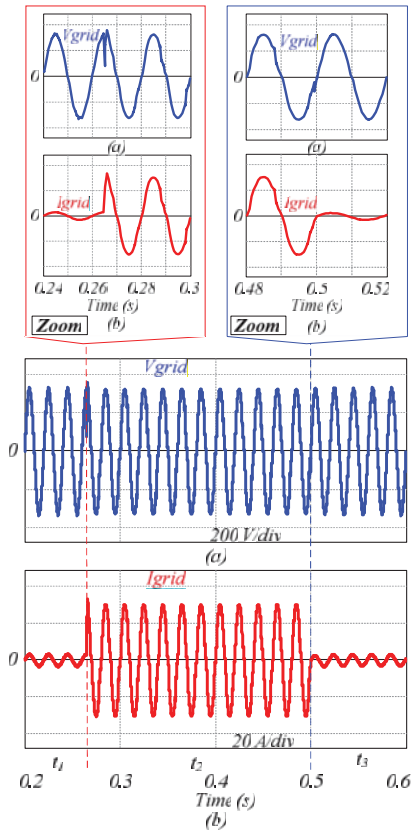


Fig. 8. The simulation results: a) grid voltage; b) grid current.

Figure 9 presents the simulation results under different load conditions and connection of microinverter. The load is only active till the moment of time 0.4 s. At the time 0.4 s, the microinverter is connecting to the whole system.

Figure 9 from top to bottom: grid voltage; grid current; output current of microinverter; output current of synchronous generator (qZS inverter). From the beginning, the synchronous generator is operating only.

At the moment of time 0.265 s, the load demand is changed from 1 kW to 10 kW. The transient time is very fast, the inverter is able to react fast to the load changing.

At the time 0.4 s, the microinverter is connecting to the system and the produced current for the load is shared between the two inverters based on their power production capacity. The transient time in the microinverter is not so good, but it does not affect the total output current-grid current.

At the moment of time 0.5 s, the load demand is changing the whole system from 10 kW to 1 kW to cope with this task very fast. The power is correctly shared between the inverters. At the same time, it can be seen that the transient process is complicated.

The next step was the verification of the function of the synchronverter. Figure 10 presents three loading steps implemented in the model. As the frequency curve shows, there is no load at the very beginning. The grid is not built up by qZSI since there is no reference voltage. In the next stage, voltage reference is applied, the load has nearly step change and power reference is also set to have the same step to balance the load.

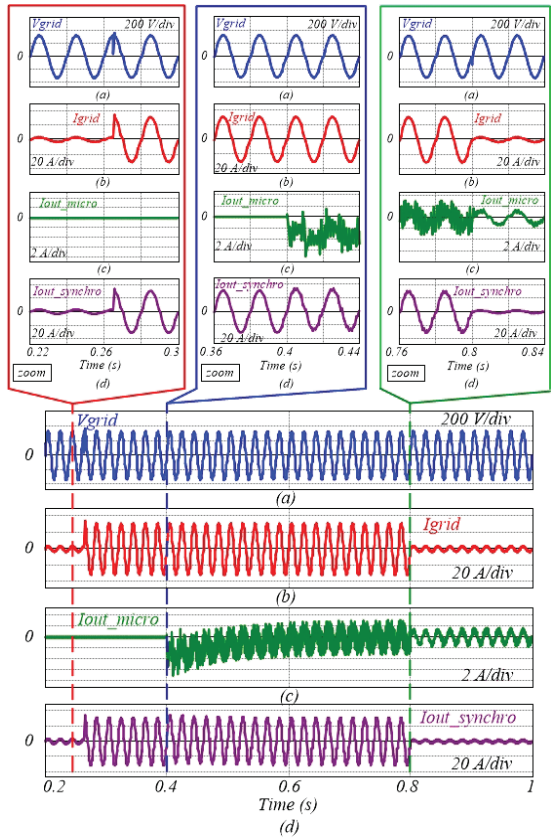


Fig. 9. Simulation results of the qZSN inverter with the microinverter in the islanding mode.

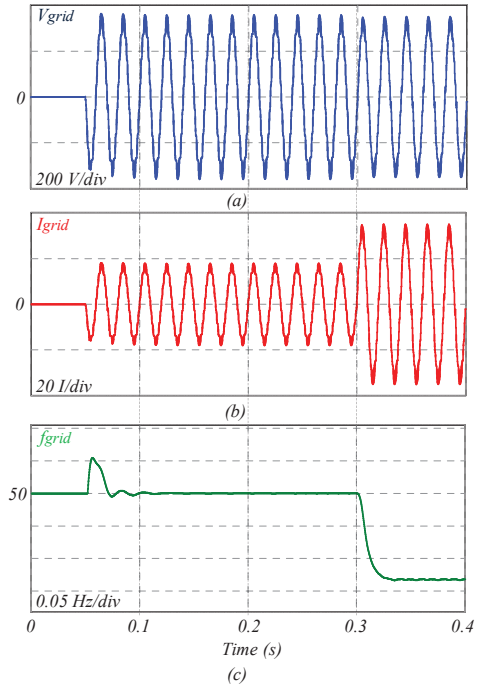


Fig. 10. Simulation waveforms of the proposed VSG.

Although the frequency will be deviated during the transient, it goes back to 50 Hz due to the effect of the droop control. In the last stage, the load has been increased but the power reference is kept unchanged. Due to the effect of VSG, the frequency will be decreased due to power mismatch and a new steady state point will be reached due to the droop control. Despite the implemented changes, the grid voltage has remained at its rated value.

## VI. CONCLUSIONS

The paper discusses the possibility of implementation of the syncrhonverter concept in a small-scaled microgrid. In this grid, the synchronous machine is absent and the inverter was used to replace it by means of operation as the synchronverter while other less powerful inverters can be connected to such grid.

The functionality of VSG by providing load dependent frequency and voltage were verified. As a result, the other inverters could be involved in the same voltage and frequency regulation.

It is shown that the concept of the synchronverter, which means frequency and peak voltage setting, is not difficult to implement. The qZS network, which is reasonable due to the extended voltage regulation along with improved reliability defines the dynamic behaviour of the inverter.

At the same time, the most complex part consists in the reference power generation. It depends on many factors.

The output voltage control as well as harmonic compensation of the current control of the syncroinverter defines the quality of the output voltage in steady state mode. At the same time, internal microinverter control systems mostly define the quality of the transient process during its connection/disconnection.

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# Novel Quasi-Z-Source Derived Inverter with Unfolding Circuit and Battery Storage

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***Abstract* — This paper presents a novel solution for the single-stage buck-boost inverter with unfolding and buffer circuit intended for photovoltaic applications. The general operation principle is demonstrated by means of simulation. The advantages of the proposed solution and its limitations are discussed in conclusions.**

***Keywords— quasi-Z-source network, unfolding circuit, storage batteries.***

## I. INTRODUCTION

Present technologies and innovations have led to the expansion of Photovoltaic (PV) energy generation systems worldwide [1]-[4]. PV energy sources are characterized by wide output voltages and power variations.

The Google Little Box Challenge (GLBC) has shown close association with the topic of high-power density inverters for PV applications that have made extremely high power density of power electronics converters achievable [5], [6]. One of the main GLBC project outcomes is the concept of an extremely high-power density converter. The finalists have demonstrated a similar approach. It includes the basic full-bridge interleaved inverter, active decoupling circuit and Wide Band-Gap (WBG) semiconductors.

At the same time, the GLBC solution is intended for narrow input voltage regulation and cannot provide a high efficiency PV system in the heating or shadowing conditions.

Intermediate voltage boost dc-dc converters are used in order to overcome this drawback. At the same time, this solution is more complex and more expensive.

To extend the input voltage regulation range, solutions based on Impedance-Source (IS) networks have been proposed [7]-[12]. In contrast to the conventional converters, they have a buck mode, a boost mode and do not suffer from the Shoot-Through (ST) states. In advance, the quasi-Z-Source Inverter (qZSI) drives Continuous Input Current (CIC) from the source and shares a common ground with a dc-source suitable for renewable energy applications, in particular for the PV systems. These inverters are also capable of performing Maximum Power Point Tracking (MPPT) without an extra dc-dc converter.

At the same time, IS based converter applications for various areas are discussed in many research papers [13]-[16].

Another trend and demand in PV systems is the application of storage batteries. It makes a system independent and feasible as an autonomous power supply. Several solutions with qZSI and battery integration are presented and discussed in [17]-[20]. At the same time, it does not seem feasible for practical applications [21] Where a separate interface circuit for storage battery control is more reliable.

Several single-stage buck-boost inverters are proposed in [22]-[26]. The solution based on the input boost and buck converter along with a line frequency unfolding circuit seems to be interesting for practical applications [26], [27].

This paper discusses further modification of this solution based on the combination of the unfolding circuit, interface storage converter along with the qZS network for buck and boost functionalities (Fig. 1).

The next sections are organized as follows. Section II covers a detailed study of the operation of the proposed topology. The steady state analysis is presented.

Section III describes the simple control strategy. Section IV presents the simulation results along with previous estimation of the efficiency. Finally, the pros and cons of the proposed solution and future research directions are discussed in the conclusions.

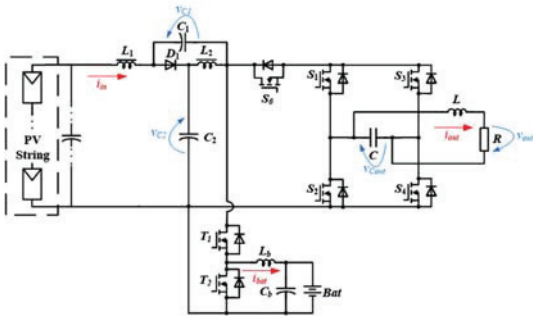


Fig. 1. Proposed buck-boost qZS derived inverter with unfolding and buffer circuits.

## II. Generalized Operation Principle

Fig. 2 demonstrates the control principle and idealized operating waveforms of the proposed converter. The operation modes of the topology are shown in Fig. 3.

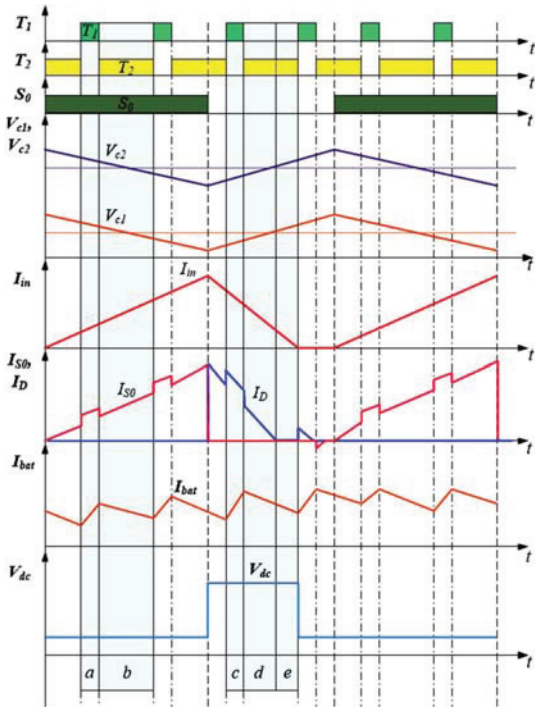


Fig. 2. Control principle and idealized operating waveforms of the proposed converter in steady state mode.

The circuit consists of the following: the qZS network ($L_1$, $L_2$, $C_1$, $C_2$) for boosting the input voltage; the buffer circuit ($T_1$, $T_2$, $L_b$, $C_b$, *Bat*) to maintain the virtual dc-link voltage and to control the battery power flow; interconnection switching device $S_0$; inverter circuit ($S_1$-$S_4$) that commutates under low frequency and forms positive/negative waveforms of sinusoidal output current; and output circuit (*C, L, R*).

We consider several operation modes here. The operation configurations can be divided into five types based on the switching states of the switching devices. Configurations that correspond only to the positive part of the output current are considered to reduce the overall description. The main difference between the positive and the negative lies in the waveforms in the output circuit, and they have no specific conditions, thus will not be considered.

During the operation mode presented in Fig. 3*a*, switches $S_0$, $S_1$, $S_4$ are conducting and forming the positive part of the sinusoidal output current. The impedance capacitors are discharging and transferring their energy to impedances' coupled inductors, and as a result, the dc-link voltage is increasing. During this mode, the switch $T_1$ is turned on and the battery is charging, the current's spike across the intermediate switch is due to the battery's current being added and due to the mode *(Fig. 2c)*. For this mode, equations of voltages and currents can be presented as follows:

$$v_{L1} = v_C - v_{C1} - V_{in}, \quad v_{L2} = v_C - v_{C2}. \tag{1}$$

$$i_{in} + i_2 = i_{bat} + i_{S0}, \quad i_C + i_{out} = i_{S0}. \tag{2}$$

During the following mode shown in Fig. 3*b,* at the time when the instantaneous voltage across capacitor $C_2$ is becoming lower than the predefined value, the battery starts to discharge, which means that $T_2$ is turned on, and $T_1$ is turned off.

During the operation mode presented in Fig. 3*c,* the switch $S_0$ is turned off. The impedance's diode starts to conduct, and the impedance's capacitors and battery are charging. The current across the output capacitor *C* changes its direction, while keeping the direction across the output circuit *L, R*. Although the switches *S1, S4* are turned on, the current across them is equal to zero.

$$v_{L1} = v_{C2} - V_{in}, \quad v_{L2} = v_{C1}. \tag{3}$$

$$i_{in} + i_1 = i_2, \quad i_C = i_{out}. \tag{4}$$

Fig. 3*d* presents the mode where the switch $S_0$ is turned off, and the impedance's diode keeps operating, and the battery is discharging.

Fig. 3*e* presents the last mode when neither the switching device $S_0$ nor $D_1$ is conducting and the current flows across the output circuit in the same direction as in the previous operation mode. In the case of CCM, the last mode is absent.

In a steady state mode, the average voltage across the inductors is equal to zero. Equations (5-7) 'minus' corresponds to the positive part of the output voltage and 'plus' to the negative. The average voltage across the capacitors can be expressed as follows:

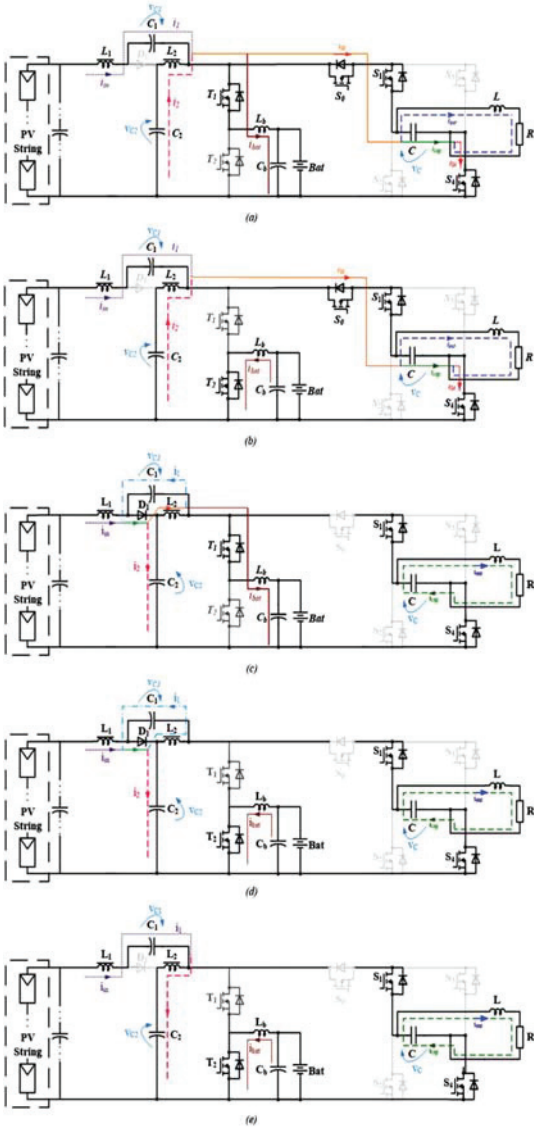


Fig. 3. Equivalent circuits to form positive waveforms. S0, T1-is conducting *(a),* S0, T2-is conducting *(b),* D1,T1-is conducting *(c),* D1, T2-is conducting *(d),* T2- is conducting *(e).*

$$V_{C1} = \frac{Da(V_{in} \pm V_C)}{1-2Da}, \tag{5}$$

$$V_{C2} = \frac{Vin - Da(V_{in} \pm V_C)}{1-2Da} \tag{6}$$

where $Da = \frac{t_a}{T}$ is a relative time when the intermediate switch is being turned on.

The required duty cycle of the switching state of the switch $S_0$ can be calculated as:

$$Da = \frac{V_{dc} - V_{in}}{2V_{dc} \pm 2V_C}, \tag{7}$$

where $V_{dc} = V_{C1} + V_{C2}$ is the desired level of the dc-link voltage.

Fig. 4 presents the dependence of the active duty cycle from the level (phase) of the output voltage, which corresponds to the input voltage of 300 V. The higher the level of the output voltage, the longer the active state duty cycle will be.

The dependence of a non-sinusoidal character is shown in Fig.4. In the case of PWM, an application recalculation block is required.

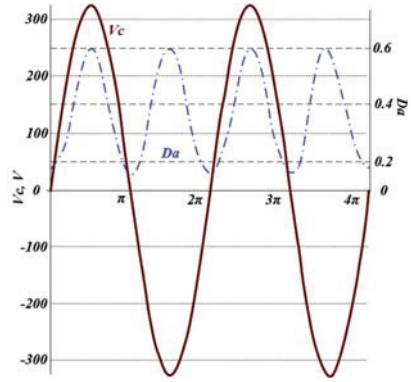


Fig. 4. The dependence of the active state duty cycle on the output voltage.

## III. PROPOSED CONTROL APPROACH

The sketch of the proposed control approach is illustrated in Fig. 5.

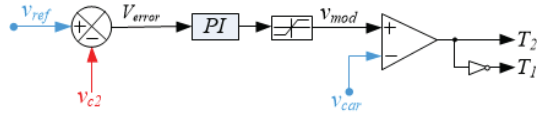


Fig. 5. Block diagram of the applied control strategy.

To control the dc-link voltage, we decided to maintain the average voltage across the internal impedance capacitor $C_2$. The desired value of the voltage is compared with the measured voltage and the error enters the PI controller. The output signal of the PI control is a modulation signal, which is compared with a triangular carrier signal, and based on that comparison, the T1 or T2 switch is switched on alternately.

Fig. 6 presents the principle of the modulation technique applied to the battery circuit control.

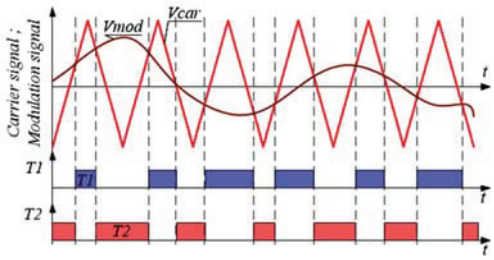


Fig. 6. Control signals of the modulation techniques applied to the buffer circuit.

To control the buffer circuit, the SPWM is applied with one bipolar triangle carrier signal and the modulation signal is formed by the PI controller based on the error between the reference dc-link voltage and the measured value.

Fig. 7*a* presents a sketch of the control technique applied for a modulation transistor. To control the output voltage, the hysteresis controller is selected, where the reference output voltage is compared with the measured output voltage and on the basis of that error, the intermediate switch is controlled. As a result, the frequency of the interconnection switch $S_0$ is not fixed, and the frequency is much higher than in the inverter's switching devices.

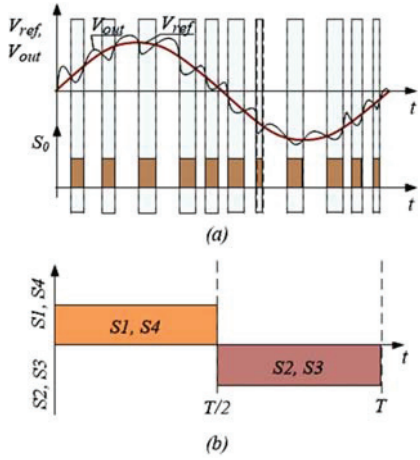


Fig. 7. Hysteresis control approach for an intermediate modulation switch *(a);* Control signals of the unfolding circuit *(b).*

Since the switching devices of the inverter commutate under low frequency (50 Hz), the switching and conduction losses across them are decreased. Fig. 7*b* shows a simple diagram. To control the unfolding circuit, a simplified PWM block is applied. During one half of the period, one of the diagonals is turned on, i.e., *S1, S4,* and it forms the positive waveform of the output current, in another one – an opposite diagonal is turned on and it forms a negative waveform of the output current.

## IV. Simulation Results

Fig. 9 presents the simulation results obtained by the PSIM simulation tool. From the top to the bottom: input current; voltage across capacitors $V_{C1}$ and $V_{C2}$; current across buffer capacitor; output current and voltage across output capacitor. From left to right: *Vin=400 V; 200 V; 50 V* – all of them correspond to the boost mode. Table I shows the the values of the components used during the simulation of the system.

TABLE I. Parameters used for simulation

| Parameter | Value |
|---|---|
| *Vin* | *400 V; 200 V; 50 V* |
| *Vout* | *325 V* |
| $VC_2$ | *450 V* |
| *Pout* | *3 kW* |
| *L1, L2* | *0.25 mH* |
| *C1,C2* | *2.5 mF* |
| *L* | *0.5 mH* |
| *C* | *0.1 mF* |
| *Lb* | *1 mH* |
| *Cb* | *1 mF* |
| *Vbat* | *96 V* |
| *f_buf;* | *50 kHz* |
| *f_inv* | *50 Hz* |

Fig. 9*a, e, i* present the input current. In the first case, the CCM's input voltage equals 400 V, but the maximum value of the input current in this mode is higher than in any other considered case - about *78 A,* while in other cases about *50 A*. As a result, the input power in the first case is up to *14 kW,* while the demand for the output power is – *3 kW* in all cases, and the remaining power flows through the buffer circuit.

Fig. 9*b, f, j* shows voltage across the impedance capacitors *C1, C2*. The applied control strategy is able to maintain the predefined voltage across the capacitor C2 in all cases and the simulation results confirm the validity of the equations (5,6,7).

Fig. 9*c, g, k* shows the battery current. It should be noted that in the first case, the battery current is approximately equal to 150 A, which is a very high value and in practice, this mode should be avoided. The buffer circuit could theoretically also operate as an active power decoupling circuit and maintain the CCM of the input current.

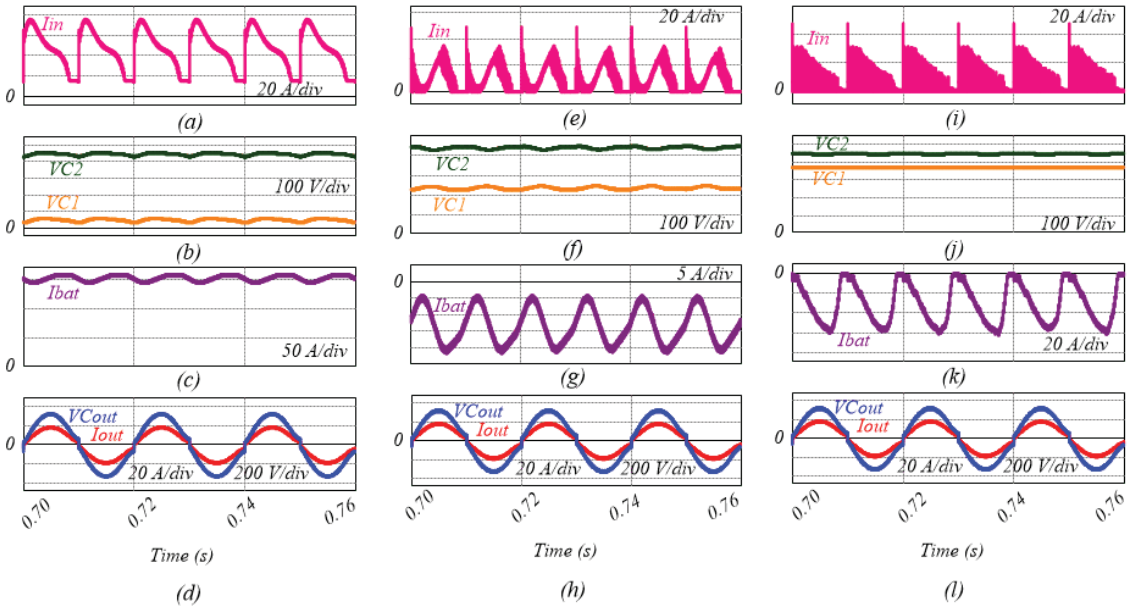


Fig. 9. Waveforms of input current; voltage across capacitors $V_{C1}$ and $V_{C2}$; current across buffer capacitor, output voltage and current, *(a-d)* – Vin=400 V; *(e-h)*-Vin=200 V, (i-l)-Vin=50 V.

Finally, Fig. 9*d, h, l* show the output current and voltage across the output capacitor. As can be seen, the proposed topology provides a solution to the task despite the value of the input voltage in all the cases. At the same time, a problem appears near zero, which is a common problem of an unfolding circuit.

## V. Conclusions

This paper presented a novel solution of the single-stage inverter with an unfolding and buffer circuit that are able to operate in several modes. Its advantages are a minimum number of passive elements, a very flexible control algorithm and reduced high switching frequency harmonics in the common mode voltage. The simulation results confirmed all the theoretical statements. Despite the buck mode demonstrated, it is able to operate only with the decoupling circuit. Thus, the topology is more suitable under the conditions when the input voltage is significantly lower than the output voltage.

It can be recommended for applications where wide input voltage regulation ranges along with storage battery facilities are required. Despite the high number of active switches, only few of them might have significant switching losses. The control strategy proposed in this paper is simplified and used for topology demonstration.

## Acknowledgments

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# Single-Phase 3L PR Controlled qZS Inverter Connected to the Distorted Grid

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***Abstract*—This paper presents a single-phase three-level NPC qZS inverter connected to a distorted grid using PID and PR regulators. A case study system along with the control strategy are described. Tuning approaches for PID and PR regulators are addressed and validated by means of simulation results. The stability domain and limitations of the regulator parameters are also discussed.**

## I. INTRODUCTION

Recently, Z-Source Inverters (ZSIs) and quasi-Z-Source Inverters (qZSIs) were proposed**Error! Reference source not found.-Error! Reference source not found.**and extended for various fields of application**Error! Reference source not found.**-[9]. ZSIs and qZSIs overcome the limitation of the conventional inverters: they have both buck and boost operation modes and do not suffer from Shoot-Through (ST) states. In advance, the qZSI drives Continuous Input Current (CIC) from the source and shares a common ground with a dc-source suitable for renewable energy applications, in particular for the Photovoltaic (PV) systems. These inverters are also capable of performing Maximum Power Point Tracking (MPPT) without an extra dc-dc converter.

Another trend in power electronics consists in the modular and multilevel converter applications. The Neutral-Point-Clamped (NPC) inverter is the most attractive solution for industrial applications [10]. Within other multilevel solutions, the NPC is popular because of low capacitor count, especially for the Three-level (3L) case. The qZSI was extended to the 3L application as well[11]-[17]. It has traditional advantages that lie in the output voltage quality improvement, reduced voltage stress on the semiconductors that allows using fast MOSFETs among other industrially verified Si technologies and a larger nominal power that converter can handle. Moreover, the 3L NPC qZSI has a very wide input voltage operation range.

At the same time, there are few papers devoted to the study of the grid-connected qZSI[18]-[21],especially for single-phase applications[22]-[25]. Along with well-known problems related to voltage harmonics mitigation in the distorted grid, the grid-connected inverter based on the qZS network faces hidden problems connected with the stability. It is well known that idle mode in the load of any boost converter type leads to the discontinuous conduction mode and over-boost performance. Resonance phenomena inherited from the qZS network result in complications. Further, low frequency power fluctuations caused by a single-phase ac system leads to the input voltage and current fluctuation identical to the variable dc load.

The problem is that most of the papers study only part of the problems. The main goal of this work is to achieve stable performance of the single-phase 3L NPC qZSI connected to the distorted grid in the full load profile along with a wide input voltage range which can be applied in the range of applications.

## II. CASE STUDY SYSTEM DESCRIPTION

The case study system is depicted in Fig. 1. The 3L NPC qZSI is the string PV inverter connected to a distorted grid.

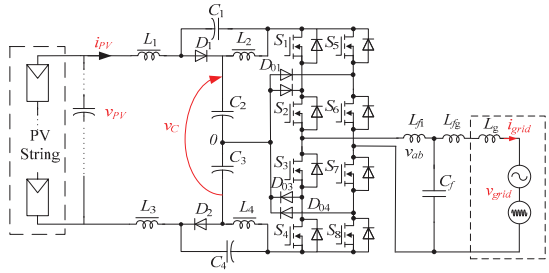


Fig. 1. Single-phase PV system using 3L qZSI.

A PV installation of 10 serial modules is a voltage source for the selected topology. It is well known that solar panels provide limited voltage (V) and current (I) that follow an exponential I-V curve. The main specifications of a commercial solar module (LDK 185D-24(s)) are detailed in [26]. Even low but equally distributed solar irradiation does not require extremely high boost performance. High boost capabilities are demanded in a partially shaded mode where only some of the modules in the array have lower irradiation. The MPP with maximum irradiation over all the modules corresponds to the 390 V input voltage that requires no voltage boost feature from the converter.

The general concept of the single-phase 3L NPC qZSI is described in [14] and experimentally verified in[4]. It is intended for applications that require a wide operation range of the input voltage along with the CIC.The types and values of the passive components used in the simulation model were selected according to the approach in[15]and it is presented in Table I.

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The overall control system of the qZSI contains a few independent blocks as shown in Fig. 2: MPPT algorithm, Phase-Locked-Loop (PLL), a grid-connected control strategy to generate the reference, a current controller to track such reference and a dc-link voltage control loop.

TABLE I. PASSIVE COMPONENTS USED FOR SIMULATION

| Parameter or component | Value |
|---|---|
| Capacitors $C_1$ and $C_4$ | *0.2 mF* |
| Capacitors $C_2$ and $C_3$ | *1mF* |
| Inductors $L_1$... $L_4$ | *900 µH* |
| Filter inductor on the inverter side $L_{fi}$ | *0.7mH* |
| Filter capacitor $C_f$ | *0.47 µF* |
| Filter inductor on the grid side $L_{fg}$ | *0.5mH* |
| Switching frequency | *100 kHz* |

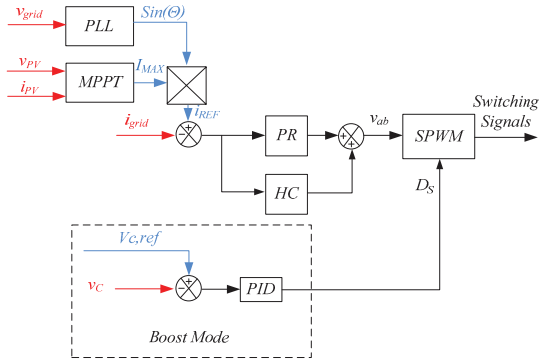


Fig. 2.Grid connected control system based on PR controller.

Several grid-current controllers are possible: a Proportional-Resonance (PR) controller based on the stationary reference frame and the rotating reference frame. In this case, the grid-connected control system is based on the PR controller, which is an accepted solution for single-phase systems [27]. Also, a traditional control system based on the rotating reference frame can be used for a similar case[24]. The main drawback of any control system based on the rotating reference frame lies in the complexity of the control system for a distorted grid. It requires a multi-reference control system and more calculation resources. Moreover, a multi-resonance PR controller is much simpler in real implementation.

Fig. 2 shows that the control signal after the PR controller moves to the Sinusoidal-Pulse-Width-Modulation (SPWM) block with equally distributed ST states in each switching period[12]. Where the $D_S$ is a ST duty cycle.

The PLL-Second Order Generalized Integrator (SOGI) algorithm was selected for grid synchronization because of the pure and stable sinusoidal output signal despite the distorted grid voltage waveform[28]. The derived sinusoidal waveform is in phase with the fundamental harmonic of the grid voltage and it is used for the reference current signal. At the same time, the MPPT block gives the peak value of the reference current. There are many review papers devoted to a proper selection of the MPPT algorithm. Papers[30] and[31]have shown that the Perturb and Observe (P&O) method is most attractive for the discussed topology. The PLL design and the MPPT algorithms are outside the scope of this paper.

## III. CONTROL SYSTEM TUNING

Operational stability of the selected control system depends on the selected coefficients of the regulators, which in turn, depend on the passive elements and dynamic features of the converter.

### *A. PR controller tuning*

The quality of the injected grid current depends on several parameters. First of all, the output filter must be properly designed. An *LCL* filter possesses a set of advantages. First, the third order filters lead to better attenuation of the switching harmonics and reduced Electromagnetic Interference (EMI). The disadvantages of these filters lie in a more complex power circuit where resonance may lead to undesired oscillations or instability of the system.

The single-phase power fluctuation may result in a fluctuation of the dc-link voltage, which in turn causes output current distortions.

When imbalance and distortion occur in the grid voltage, the PR controller performs control to reduce the power ripple, suppressing the most significant undesirable harmonics by means Harmonic Compensation (HC). Thus, the PR controller and the *LCL* filter have to provide acceptable output current quality.

Fig. 3*a* shows the dynamic model of the PR controller. The input source is assumed to be constant for a simple tuning.

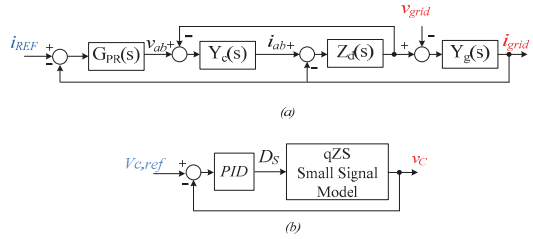


Fig.3.Dynamic model of the current controller (a) and dynamic model of the dc-link controller (b).

The PR controller's transfer function is given by

$$G_{PR}(s) = \frac{v_{ab}(s)}{i_{ref}(s) - i_{grid}(s)} = Kp + Ki\frac{s}{s^2 + \omega^2}, \quad (1)$$

where $v_{ab}$ is an output inverter voltage before filter. *Kp* is a proportional gain of the controller and *Ki* is an integral gain of the resonance component. Reference grid current $i_{ref}$ normally is derived from MPPT that is compared with real grid current $i_{grid}$.

The closed loop transfer function $G_{PRLCL}$ according to Fig. 3*a* is derived as:

$$G_{PRLCL}(s) = \frac{G_{PR}G_{LCL}}{1 + G_{PR}G_{LCL}}. \quad (2)$$

Taking into account the mathematical model of the *LCL* filter, the closed loop transfer function of the *LCL* filter $G_{LCL}$ is derived as:

$$G_{LCL}(s) = \frac{Y_c(s)Z_d(s)Y_g(s)}{1 + Y_c(s)Z_d(s) + Z_d(s)Y_g(s)}, \quad (3)$$

where

$$Y_c(s) = \frac{1}{sL_{fi}},\ Y_g(s) = \frac{1}{sL_{fg} + R_L},\ Z_d(s) = \frac{1}{C_f s}. \quad (4)$$

A damping resistor $R_L$ is presented in the model like a series resistor to the grid side inductor. Fig. 4 shows the map of poles of the closed loop transfer function of the current controller and the *LCL* filter that contains poles of the closed loop transfer function.

The proportional gain (Fig. 4*a*) has the most significant influence on the stability of the grid side control system. It should be smaller than 1. At the same time, higher resonance gain (Fig. 4*b*) accelerates the system but does not lead to the instability of the system. Finally, the proportional gain of the controller was selected as *Kp=0.6* and the integral gain of the resonance part *Ki =6000*.

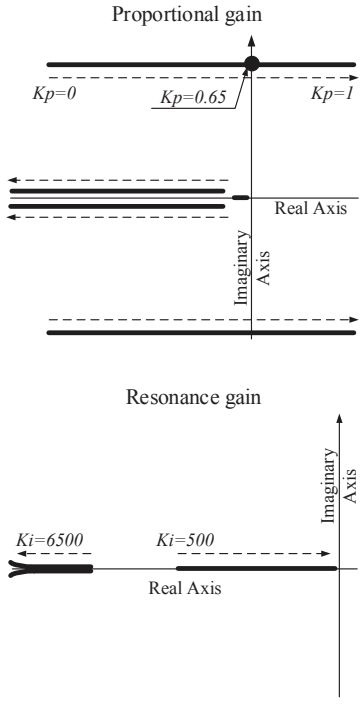


Fig.4. Map of poles of the transfer function of the grid side controller and filter.

The HC transfer function is expressed as

$$G_{HC}(s) = \sum_{h=1} Ki_h \frac{s}{s^2 + h^2\omega^2}. \quad (5)$$

The fundamental harmonic is 50 Hz. The HC is used to compensate other undesired harmonics. In this case it is the third, fifth and seventh harmonics. These harmonics are most prominent in a typical current spectrum at the low voltage distribution level. Similar to the above described approach the integral gains of the resonance harmonics were estimated.

### *B. PID controller tuning*

In order to provide the demanded quality of the grid current with a selected modulation technique, a constant dc input voltage ($V_{IN}$) is needed. In the case of qZSI, the average value of dc-link voltage must be constant:

$$V_{C2} + V_{C3} = V_C = \frac{(1 - D_S)}{(1 - 2 \cdot D_S)} \cdot V_{IN}\ . \quad (6)$$

In this case, the PV voltage can drop and rise. To stabilize the average dc-link voltage, a PID regulator was implemented. The output signal of this regulator varies with the ST duty cycle ($D_S$)of the impedance network and at a voltage sag in $V_{IN}$, the $D_s$ increases. Thus, the capacitors' ($C_2$ and $C_3$) voltage remains constant, independent of the input voltage from the PV system. In Fig. 3*b*,a simplified dynamic qZSI model with a PID regulator is shown. This model is based on a small signal model and allows tuning at accurateoperation points.

The PID regulator transfer function is given as:

$$G_{PID}(s) = K_{PROP} + \frac{1}{T_i s} + T_d s\ , \quad (7)$$

where $K_{PROP}$, $T_i$,, $T_d$ are proportional gain, integral and derivative time constants, respectively.

The closed loop transfer function can be obtained as:

$$G_{PIDqZS}(s) = \frac{G_{PID}(s)G_{qZS}(s)}{1 + G_{PID}(s)G_{qZS}(s)}\ . \quad (8)$$

The small signal model allows estimation of the transfer function and as a result, it is possible to select proper values of the PID regulator parameters. Fig. 5 shows the map of poles of the closed loop transfer function that contains only poles changing. The left side of the map of poles corresponds to the stable region. It can be seen that the system with a PID regulator has a limited but a predicted stability domain. The most significant influence is the proportional gain (Fig. 5*a*). Its increase leads to an unstable behavior. At the same time, an increase in the integral (Fig. 5*b*) and derivative (Fig. 5*c*) time constants leads to the stability domain is increasing.

It should also be mentioned that the small signal model includes a resistor *R* located in series with each inductor and represents losses in the system. It can be seen from Fig. 5 that *R=0* is a theoretical assumption that completely changes the map of poles.According to the developed model, the following parameters of the PID regulator were selected: $Ti=2$, $K_{PROP}=0.02$, $Td=5\cdot10^{-6}$.

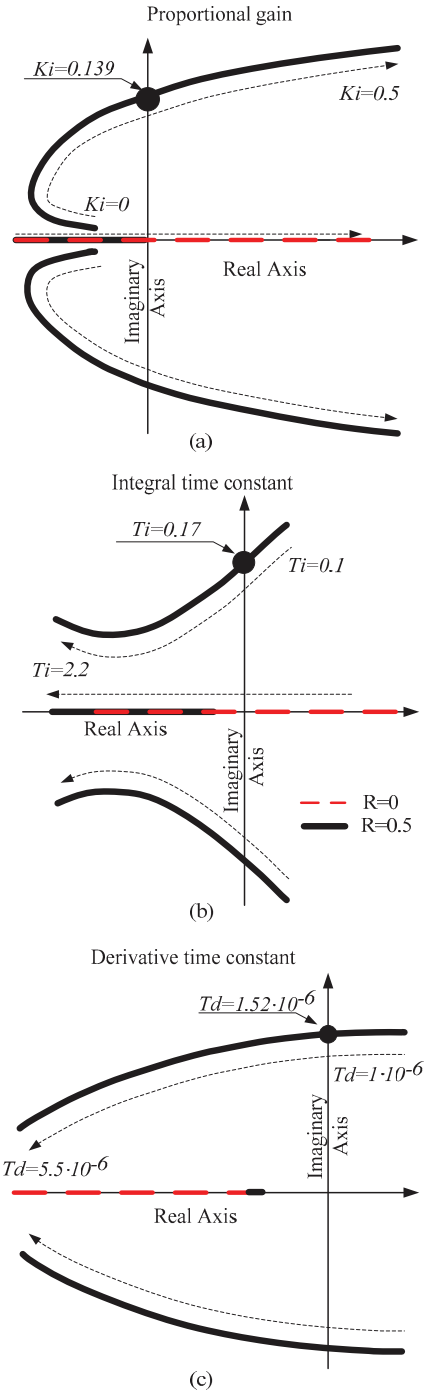


Fig. 5. Map of poles of the closed loop transfer function of the qZSI small signal model along with the PID regulator: proportional gain changing (a), integral gain changing (b), derivative gain changing (c).

## IV. Simulation Results

In order to verify the theoretical predictions, using a PSIM tool, simulations were performed. Table II summarizes parameters used for the simulations. It should be noticed that the issue of MMPT is ignored in this paper and an ideal voltage source is used in the simulation model. This assumption will not influence the converter behavior because of the very slow dynamic characteristics of the PV modules.

TABLE II. Values Used for Simulation Study

| Parameter | Unit | Value |
|---|---|---|
| Nominal Power | (W) | 1800 |
| Grid RMS voltage | (V) | 230 |
| Input voltage range | (V) | 200 - 440 |
| $PID(K_{PROP})$ | | 0.002 |
| $PID(T_I)$ | (s) | 2 |
| $PID(T_D)$ | (µs) | 5 |
| $PR\ (K_P)$ | | 0.6 |
| $PR\ (K_{i1})$ | | 6000 |
| $PR\ (K_{i3})$ | | 60000 |
| $PR\ (K_{i5})$ | | 60000 |
| $PR\ (K_{i7})$ | 0987 | 60000 |
| Switching frequency | (kHz) | 100 |
| Simulation step | (µs) | 0.2 |

The average input current was about 5 A. It corresponds to nominal power 1.8 kW. It can be seen that the average dc-link voltage is very stable and the quality of the grid currents satisfies all standards. $THD_{(I)}$ is less than 5 %.

Fig. 6 presents the THD spectrum of the grid current with and without HC. Obviously, the harmonic spectrum of the grid current without HC contains a significant value of the fifth harmonic, which deteriorates the quality of the grid current.

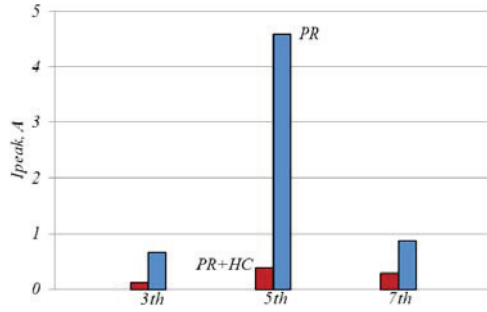


Fig. 6 .THD spectrum of the output current with and without HC loop in the PR regulator.

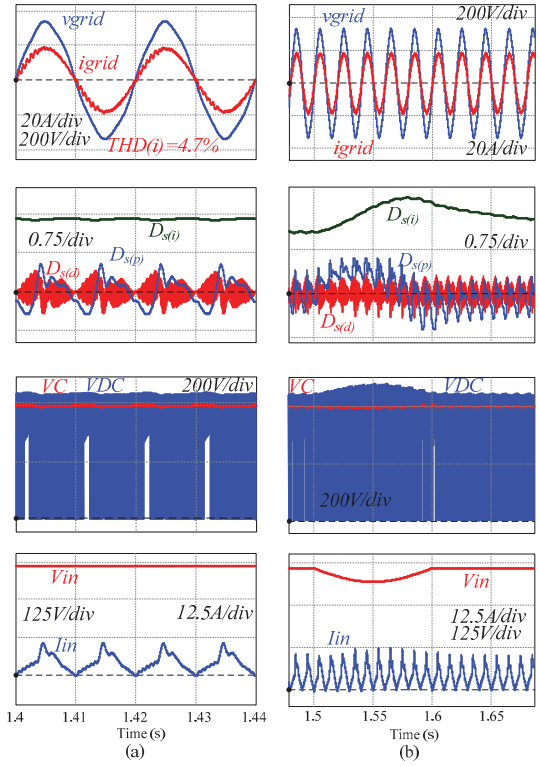


Fig. 7 .Simulation results: Steady state mode (a), transient response during input voltage disturbance (b).

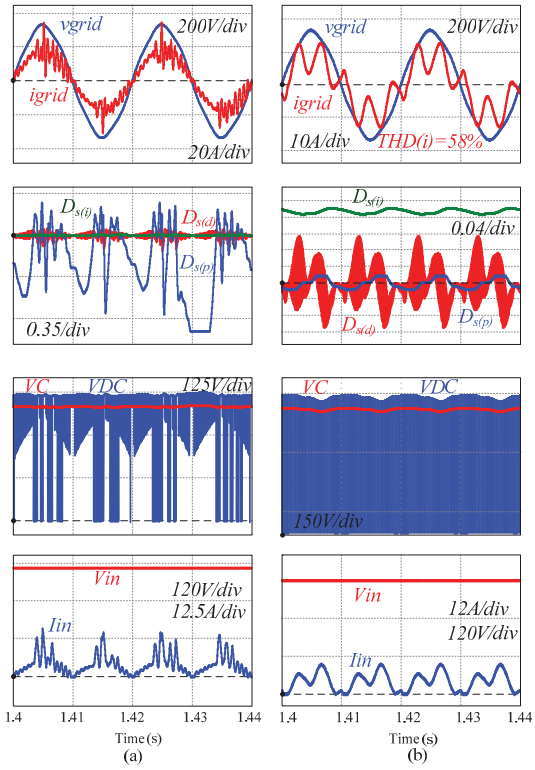


Fig. 8 .Simulation results: Steady state mode with unstable PID regulator parameters (a), steady state mode without HC circuits (b).

Fig. 7, Fig. 8 show the main simulation results. Fig.7*a* shows steady state waveforms in the nominal power point: grid voltage $v_{grid}$, grid current $i_{grid}$, output signals of *PID* regulator, capacitors voltage $V_c$ and dc-link voltage $V_{DC}$, input voltage $V_{in}$, and input current $I_{in}$. In particular Fig. 8*a* shows steady state waveforms in the nominal power point: grid voltage $v_{grid}$, grid current $i_{grid}$, capacitors voltage $V_C$ and dc-link voltage $V_{DC}$, input voltage $V_{IN}$, and input current $I_{IN}$. The output signals of the PID regulator have three control actions: the proportional *Ds(p)*, integral *Ds(i)*, and derivative *Ds(d)* components. The input voltage is about 360 V, the reference capacitors' voltage that defines an average dc-link voltage is 400 V.

Fig. 7*b* shows the waveforms during input voltage disturbance. During that time, the input voltage drops from 360 V to 320 V. Fig. 9*b* shows correspondent PID regulator parameters variation. It can be seen that the PID regulator provides a stable average dc-link voltage while the PR regulator maintains a stable RMS value of the grid current.

Fig. 8*a* shows the performance of the converter with the PID regulator parameters that are out of the stability domain: $Ti=0.1$ *s*, $Kp=0.2$, $Td=5\cdot10^{-6}$ *s*.

That, in turn, evokes fluctuation of the grid current, which cannot be mitigated by the PR regulator.

Unstable operation means fluctuation of the capacitors' voltage $V_C$. This leads also to the fluctuation of the dc-link voltage.

Finally Fig 8*b* shows that using the PR controller without HC, the waveform of the output current is significantly distorted and the $THD_{(i)}$= 58 % increased.

## V. CONCLUSIONS

This paper presents the single-phase three-level qZS inverter connected to the PR controller-based distorted grid. The case study system along with the control strategy are described.

A PR controller is a good solution for a distorted grid and provides sinusoidal grid current. At the same time, the quality of the injected current depends on the voltage across the qZS capacitors. In order to provide stable capacitor voltage values, the small signal model of the qZS inverter was created. It was used to select proper values of a PID regulator. Selected coefficients allow provision of a fast response without leaving the stability domain. It was shown that a system with a PID regulator has a limited but a predicted stability domain. The most significant influence is the proportional gain. Its increase leads to an unstable behavior.

The most significant influence on the stability of the grid side PR regulator based control is the proportional gain. It should be smaller than one.

The theoretical claims have been validated by means of simulation results and can be used for preliminary guidelines in the practical realization of the grid-connected qZSI.

## ACKNOWLEDGMENT

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# Three-Level Single-Phase Quasi-Z Source Inverter With Active Power Decoupling Circuit

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***Abstract*— Single-phase inverters suffer from double-frequency ripple of the input power. For mitigation, an input capacitor is applied but the fluctuation range of power across it is limited according the desired fluctuation in the dc-link voltage. To realize power decoupling without changes in the main circuit and in the control strategy of it, an additional independent power decoupling circuit can be applied, where the buffer capacitor works mainly as a storage element that operates with a part of the ripple of the input power. This paper proposes a three-level neutral-point-clamped impedance source based converter with active decoupling circuit connected to the internal capacitors. Our simulation results validate the proposed solution. Its advantages are very simple control strategy and the possibility of storage battery connection.**

***Index Terms* — active decoupling; single-phase inverter; PR controller; double-frequency ripple; quasi-Z source.**

## I. INTRODUCTION

Photovoltaic (PV) interface single-phase inverters suffer from Double-Frequency Ripple (DFR) of input power that deteriorates the maximum power point tracking efficiency and reduces the lifetime of the input electrolytic capacitor and PV panels. In order to reduce the DFR of input power, different methods can be applied [1]-[3].

There are two types of power decoupling approaches: passive and active. The passive power decoupling is realized by means of passive components and modified control strategy. An inductor or a capacitor can be used as storage element. A capacitor is a more attractive solution due to the higher power density as compared to the inductor.

In the active power decoupling approach, the DFR of power is created by auxiliary circuits with additional storage elements [2]. This additional circuit can be connected to the main circuit in parallel, series or by other methods.

Recent research and Google Little Box Challenge show that active decoupling approach allows achieving very high power density [4]. Though Google Little Box challenge has attracted much attention, all of those solutions have narrow input voltage regulation range.

At the same time, the string configuration of PV panels is a demanding solution where high efficiency of the PV system is required [5], [6]. One of the major drawbacks of the string technology is its poor energy utilization at partial shading conditions. It leads to wide range input voltage variations. Single stage Voltage Source Inverters (VSI) or Current Source Inverters (CSI) cannot provide more than twice higher input voltage regulation ratio. The main practical limitation lies in the low modulation index, which in turn leads to poor output current quality. Intermediate voltage boost dc-dc converters are used in order to overcome that drawback. Recent solutions based on intermediate Impedance-Source (IS) networks have attracted much attention [7]-[10]. IS based inverters overcome the limitation of the conventional grid-connected inverters: they have a buck and a boost mode, and do not suffer from Shoot-Through (ST) states. In addition, most of them have continuous input current.

Another trend in power electronics is the modular and multilevel converter applications. Multilevel inverters have advantages over the conventional and very well-known two-level inverters: improved output quality and larger nominal power in the converter [11]-[13]. Multilevel converters are a good solution for low power and low voltage applications as well. Reduced voltage stress allows using fast MOSFET semiconductors among industrially verified Si or novel GaN technologies.

As a result, several publications have proposed the Three-Level (3L) Neutral-Point-Clamped quasi-Z-Source Inverter (NPC qZSI) [14], [15]. It combines advantages of the qZS network and the NPC inverter.

At the same time, several papers have revealed that IS based inverters have similar or higher volume of passive components as compared to the conventional two-stage solution with the dc-dc boost converter and VSI [16], [17]. In order to mitigate the DFR of power in a single-phase system, even larger components are required [14], [18], [19].

Passive decoupling approach can be considered a solution for input current ripple mitigation [20]. It is proven in the paper that the capacitance value of the qZS capacitors tends to decrease. But it should be mentioned that the size of capacitors maybe even increase due to higher voltage across the capacitors. As a result, better power density is unattainable.

In conclusion, the active power decoupling approach maybe only the way to improve the power density of the single-phase 3L NPC qZSI.

Several papers have reported the use of the active filtering approach in order to decouple the DFR on the ac side [21]-[23]. On the one hand, such solutions require ac capacitors

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and complex control due to the ST states. On the other hand, buck circuit has been found to be the best solution as active circuit in terms of achievable power density [24], [25].

This paper proposes the 3L NPC qZSI with active power decoupling circuit connected in parallel to the internal capacitors. One of the features of our solution is the possibility to integrate storage elements with full controllability.

Next sections describe the study of control strategies and our simulation results.

## II. INVESTIGATED TOPOLOGY

Fig. 1 shows the topology under our study. The main topology is described in [14]. The buck converter, a well known solution, is used as an active decoupling circuit.

Here an active circuit is connected to the internal capacitors of the qZS network. In the constant boost control approach the voltage across internal capacitors remains constant and lower than the dc-link voltage. It means that a two-level active decoupling circuit can be used. Transistors will be the same as in the 3L NPC circuit.

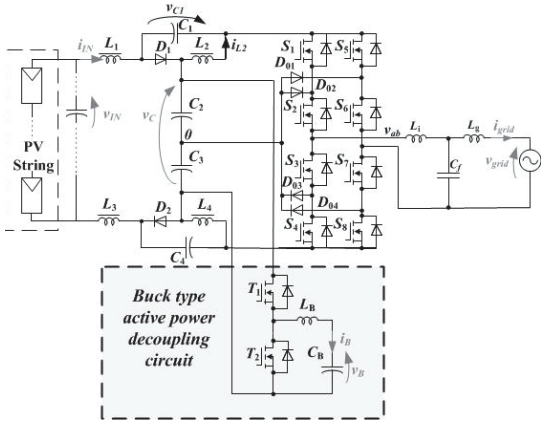


Fig. 1. Single-phase PV system using 3L NPC qZSI along with active decoupling circuit.

### A. Estimation of passive elements of the qZS network

Passive elements in the presented topology have been estimated in [14], [18], [19]. In the single-phase system, the size and value of the passive components are defined by the high frequency switching ripple along with DFR. Since the active power decoupling circuit is used, the passive elements of the qZSI can be reduced and only high switching ripples are taken into account.

### B. Passive elements estimation of active power decoupling circuit

The instantaneous power of the grid has an average value and the DFR of line frequency that is transferred into the input side and should flow across the capacitor of the active power decoupling circuit are described as:

$$p_{grid} = v_{grid} \cdot i_{grid} = \frac{VI}{2}\cos(\phi) + \frac{VI}{2}\cos(2\omega t + \phi), \quad (1)$$

where the average power and double-frequency power are presented in (2), (3) respectively.

$$P_{ave} = \frac{VI}{2}\cos(\phi), \quad (2)$$

$$P_R = \frac{VI}{2}\cos(2\omega t + \phi). \quad (3)$$

This power ripple $P_R$ should charge the capacitor when the input power is larger than the average value; in the opposite case, the capacitor should return that power and as a result, the input power is maintained with minimum pulsation. Therefore, the energy that must be stored in the buffer capacitor $C_B$ is defined as:

$$\Delta E = \frac{P_R T}{2\pi} = \frac{C_B (V_{\max} - V_{\min})^2}{2}, \quad (4)$$

where $T$ is the fundamental period, $V_{max}$, $V_{min}$ are the desired maximum and minimum values of voltage across the buffer capacitor.

From equation (4), the value of buffer capacitor can be found:

$$C_B = \frac{2\Delta E}{(V_{\max} - V_{\min})^2}. \quad (5)$$

However, the voltage across the buffer capacitor $C_B$ should be lower than the dc-link voltage that limits the peak voltage of this capacitor.

The current across the inductor $L_B$ is the current across the capacitor $C_B$ and can be calculated as:

$$i_L = C_B \frac{dv_{C_B}}{dt} = \frac{P_{R(\max)}}{V_{C_B(\max)}}. \quad (6)$$

The value of the buffer inductor $L_B$ is

$$L_B = \frac{V_{dc}}{4\Delta i_{L_B} f_{sw(buf)}} \quad (7)$$

where $\Delta i_{L_B}$ is assumed to be about 20% from $i_L$, $f_{sw(buf)}$ is switching frequency of switching devices of the active power decoupling circuit.

Such approach allows selecting passive elements of the desired value of the active decoupling circuit.

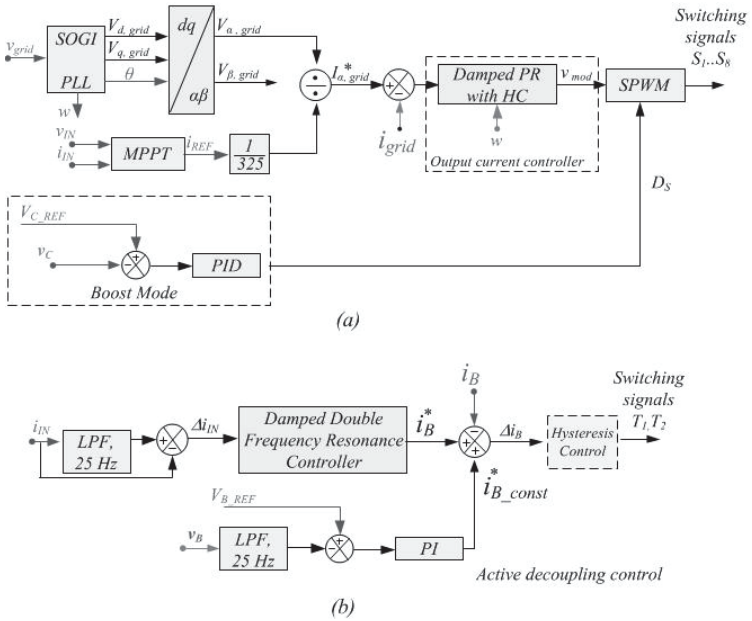


Fig 2. Block diagram of the proposed control strategy: 3L NPC qZS inverter control (a), active decoupling circuit control (b).

## III. CONTROL SYSTEM DESCRIPTION

Fig. 2 shows the proposed control strategy. The control system can be divided into two main parts. The first part provides the desirable operation of the single-phase 3L NPC qZSI (Fig. 2*a*), the other part provides active power decoupling (Fig. 2*b*).

### *A. qZSI control structure*

The overall control system of the qZSI contains some independent blocks, as shown in Fig. 2: MPPT algorithm, Phase-Locked-Loop (PLL), a grid-connected control strategy to generate the reference, a current Proportional-Resonant (PR) controller to track such reference and a dc-link voltage control loop.

MPPT block provides the maximum value of the reference current. Papers [26] and [27] have shown that the Perturb and Observe (P&O) method is most attractive for the discussed topology.

Despite the distortion in the grid voltage the PLL-Second Order Generalized Integrator (SOGI) algorithm was selected for grid synchronization because of stable sinusoidal output signal [28]. The derived sinusoidal waveform was used for the reference current signal.

In order to produce the output current injected into the grid, the *LCL* output filter and damped PR controller with Harmonic Compensation (HC) approach are used. The detailed tuning of the PR controller for the 3L NPC qZSI is discussed in [29]. The damped PR controller was selected because it provides the high gain at the tuning frequency over a wider band in comparison with the conventional PR controller. In [30] the conventional PR controller and the damped PR controller are compared.

The applied control strategy of the SPWM is described in [31]. It has constant ST states distribution and allows maintaining constant voltage across capacitors.

The value of the shoot-through duty cycle ($D_S$) provides an average value of the ST required to maintain the average voltage in the inner capacitors $V_C$. It should be emphasized that tuning of the PID controller that is used to provide $D_S$ generation is a very important issue studied in detail in [29].

### *B. Active power decoupling controller*

In order to circulate output power ripple in the auxiliary circuit, it is necessary to generate the reference decoupling current $i_B^*$. In the proposed configuration, it cannot be derived directly from the measured output power because of additional phase shift that will be present due to the passive components of the qZS network.

The Damped Double Frequency Resonant Controller depicted in Fig. 2 is an ideal solution. The input current ripple is the input signal. The output of the controller is becoming stable when the input current ripple decreases.

Also, the constant component of the current of the auxiliary circuit $i_{B\_const}^*$ is derived by means of a simple PI controller. It is necessary for maintaining predefined average voltage across the capacitor $C_B$.

Finally, the very simple hysteresis approach of constant switching frequency is used in order to provide the reference value of the current. The error $\Delta i_{B\_const}$ between the reference value and the measured value of the current is applied to its input.

The strategy proposed is quite simple and requires no complex tuning. The Low Pass Filter (LPF) used for filtering

the input current has 25 Hz cutoff frequency and can be easily realized in any digital system.

## IV. SIMULATION RESULTS

Table I presents the parameters of the case study system used in our simulation. It includes all the parameters necessary to reproduce the proposed control strategy.

Fig. 3 shows the simulation results of the transient process with and without active decoupling strategy. From 1.0 s to 1.2 s, the active power decoupling circuit is not working and the ripple of the input power is maximum.

At the time 1.2 s, the proposed strategy starts to work and the ripple of the input power is reduced, which confirms the validity of the proposed control strategy, the transients time is about 0.125 s.

TABLE I
PARAMETERS OF THE STUDIED TOPOLOGY

| Parameters | Value |
|---|---|
| General parameters | |
| $V_{in}$ | 200-400 V |
| $V_{Grid}$ | 230 V ac |
| $f_{switching}$ | *50 kHz (100 kHz)* |
| $f_{switching(buffer)}$ | *100 kHz* |
| $f_{line}$ | *50 Hz* |
| *Passive components* | |
| $C_2, C_3$ | *0.39 mF* |
| $C_1$, $C_4$ | *0.42 mF* |
| $L_1, L_2, L_3, L_4$ | *0.240 mH* |
| $R_{qZS}$ | *0.1* Ω |
| $L_{fi}$ | *0.44mH* |
| $L_{fg}$ | *0.22mH* |
| $C_f$ | *15, 47 uF* |
| $R_f$ | *0.1* Ω |
| $L_B$ | *0.7 mH* |
| $C_B$ | *2 mF* |
| *Input current controller: PID with Resonant controller* | |
| *PID(P)* | *0.002* |
| *PID(I)* | *2 S* |
| *PID(D)* | *0.5 us* |
| *Active decoupling Resonant controller* | |
| $K_{RES1}$, | *50* |
| *Active decoupling PI controller* | |
| *PI(P)* | *0.01* |
| *PI(I)* | *50 s* |
| *Output current Proportional-Resonant controller* | |
| $K_P$ | *0.5* |
| $K_{RES2}$, | *100* |
| $w_C$ | *0.314* |

Fig. 4 shows the simulation results at the steady-state mode. Fig. 4b and c demonstrate that the voltage ripple across the buffer capacitor and current ripple across the buffer inductor correspond to the predefined values. Fig. dd presents the current across the input inductor that is the input current of continuous value and the ripple is about 2 A. Fig. 4h shows the input power, the ripple is about 400 W that corresponds to 22% from the nominal value of the input power, which confirms the validity of the proposed control strategy.

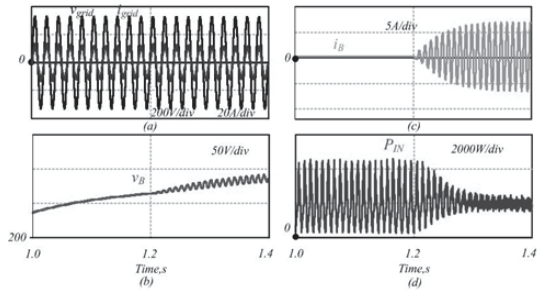


Fig. 3. Simulation results of the transient process without and with active decoupling strategy: grid voltage and current (a); voltage across buffer capacitor (b); current across buffer inductor (c); input power (d).

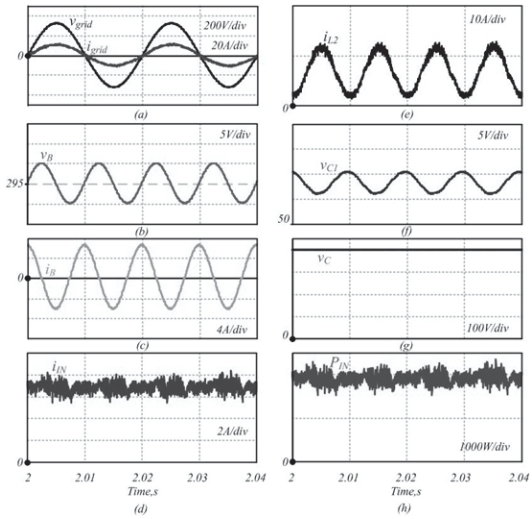


Fig. 4. Simulation results at steady state mode of the system with active decoupling: voltage grid and current (a); voltage across buffer capacitor (b); current across buffer inductor (c); current across impedance inductor $L_1$ (d); current across impedance inductor $L_2$ (e) voltage across impedance capacitor $C_1$ (f); voltage across impedance capacitors $C_2$ and $C_3$ (g); input power (h)

## V. CONCLUSIONS

This paper presents the active power decoupling approach realized by means of the modified control strategy based on a

resonant controller. It was shown that the resonant controller can provide double-frequency current ripple that is sufficient to compensate the input current ripple.

The system proposed is very easy to realize. Except for mitigated input current ripple, it has positive influence on the dc-link control strategy, which in turn leads to better output current quality.

The proposed solution of auxiliary active decoupling circuit has low number of switches, simple control strategy and can be combined with a storage system.

## ACKNOWLEDGMENT

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# Passive Power Decoupling Approach for Three-Level Single-Phase Impedance Source Inverter Based on Resonant and PID Controllers

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***Abstract*— Single-phase inverter suffers from double-frequency power ripples in the input side transferred there from the ac-side. To mitigate this ripple, two types of power decoupling approaches can be applied: passive power decoupling and active power decoupling. We present a technique of passive power decoupling realized by modifying the control strategy. The main idea is to produce the time-varying shoot-through duty cycle to charge and discharge impedance capacitors when needed in the desired sequence for mitigating input power ripple without deteriorating the output power quality. The main contribution of the paper is in the determination of the parameters of a regulator taking into account the dynamic feature of the quasi-Z-source network. The validity of the proposed control strategy was confirmed by simulation results in PSCAD. The results show that this strategy can be applied for practical applications.**

***Keywords — passive decoupling; single-phase inverter; PR controller; double-frequency ripple; distorted grid; quasi-Z source.***

## I. INTRODUCTION

During the two last decades, the integration of impedance networks in different fields of application, in particular in Photovoltaic (PV) systems, has been under wide discussion. Different configurations of impedance networks proposed in [1]-[8] allow preventing limitations of the Voltage Source Inverters (VSIs). The Shoot-Through (ST) state is introduced in the system in order to provide boost function without an additional conversion stage. The ST improves the reliability of the system because of absence of any forbidden states.

The qZ-source Neutral-Point-Clamped (NPC) inverter presented in [9] allows use of the single or separated input source(s) to reduce the voltage stress across the switching devices, thus increasing the switching frequency.

Another important feature of the inverter is the capability of injecting current into the distorted LV grid with the required quality set by international standards such as IEEE-519 [10]. Different types of controllers are used to control the quality of the output current injected [11], [12]-[14]. The PR controller looks most promising since it can provide stable fundamental current injection along with Harmonic Compensation (HC) [15].

At the same time, the single-phase system suffers from such drawback as Double-Frequency Ripple (DFR) of input power. Several strategies are reported in the literature to reduce the DFR [16], [17]. These strategies are divided into two types: passive decoupling [18] that means the system has no additional switching devices and active decoupling [19], [20] containing additional switching devices. This paper focuses on passive power decoupling. The purpose of passive power decoupling is to maintain the average voltage of the dc-link with limited second-order fluctuations across it to reduce the same in the input power. Most of the approaches are based on a modified control strategy without configuration changes[18].

Also, the mitigation of input power pulsation can be achieved by means of increasing the values of the passive components [21], [22]. At the same time, it is evident that the size of these components will be larger.

The main problem here is in the oversized passive components used for simulation and experimental verification of the proposed algorithms [16], [18], [21].

The aim is to develop a novel approach based on resonant and PID controllers for passive decoupling. It is clearly demonstrated that such approach is capable of mitigating DFR in the case of optimized passive elements.

## II. CASE STUDY SYSTEM DESCRIPTION

The case study system is depicted in Fig. 1*a*. It consists of the Three-Level (3L) single-phase Neutral-Point-Clamped (NPC) quasi-Z-Source Inverter (qZSI) connected to the distorted grid through an LCL-filter. This topology is described in [23]. Grid voltage contains 5$^{th}$ harmonic that is about 3% from the fundamental one. A PV installation of 10 serial modules is a voltage source for the selected topology. The calculation of passive components is presented below, with summarized values given in Table I.

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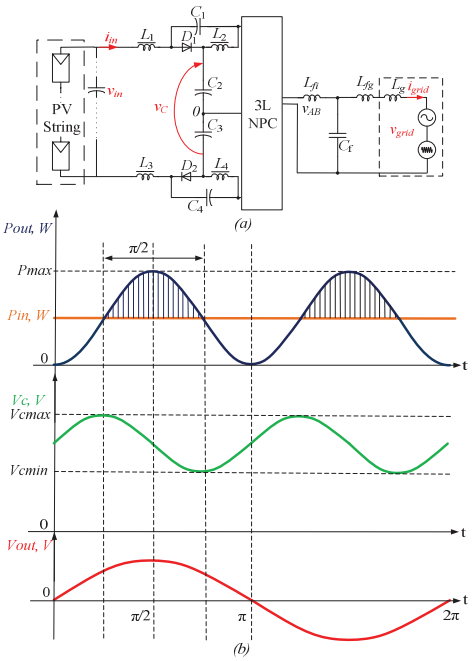


Fig. 1. Single-phase PV system using 3L NPC qZSI *(a)*; idealized waveforms of the output power along with desirable input power, voltage across impedance source capacitors and grid voltage over one line cycle *(b)*.

### A. *Passive elements estimation*

The following assumptions were accepted for the topology studied: $C_1=C_2=C_3=C_4=C$; $L_1=L_2=L_3=L_4$; in the steady state mode, the inductors current is equal; therefore, the capacitors current is equal as well. It will be valid under proper control strategy discussed in the next section. The minimum value of the ST duty cycle ($D_{min}$) depends on the value of the input voltage ($V_{in}$) and the desired minimum value of the output voltage ($V_{dc\_min}$):

$$D_{min} = 0.5 \cdot (1 - \frac{V_{in}}{V_{dc\_min}}). \quad (1)$$

This value should exceed zero to ensure that PR controller operates in linear range.

The average voltage across the capacitors of the qZS network depends on the average value of ST duty cycle ($D$). The average voltage across the capacitors $C_1$, $C_2$, $C_3$, $C_4$ is expressed as [23]:

$$V_{C2} = V_{C3} = \frac{1-D}{1-2D} \cdot \frac{V_{in}}{2}, \quad (2)$$

$$V_{C1} = V_{C4} = \frac{D}{1-2D} \cdot \frac{V_{in}}{2}. \quad (3)$$

Fig. 1*b* shows the idealized waveforms of the output power along with desirable input power, voltage across impedance capacitors and grid voltage over one line cycle ($f_{line}=50$ *Hz*).

The time $\pi/4<t<3\pi/2$ corresponds to the realizing energy mode. During that time, capacitors are discharging to maintain the input power at the average value. The time $3\pi/2<t<5\pi/4$ corresponds to the storage energy mode. During that time, capacitors are charging for the same reason.

According to Fig. 1*b*, the frequency is fixed at the double line frequency and the amplitude is $\pm 100\%$ of the output average power (neglecting losses). It is assumed that the voltage ripple across the capacitors will be distributed evenly.

$$\Delta V_{C1} = \Delta V_{C2} = \Delta V_{C3} = \Delta V_{C4} = \frac{\Delta V_{dc}}{4}, \quad (4)$$

where $\Delta V_{dc}$ is available pulsation in the dc-link.

The maximum and minimum voltages across the capacitors are:

$$V_{C1\_max} = V_{C1} + \frac{\Delta V_{C1}}{2}; \; V_{C2\_max} = V_{C2} + \frac{\Delta V_{C2}}{2}, \quad (5)$$

$$V_{C1\_min} = V_{C1} - \frac{\Delta V_{C1}}{2}; \; V_{C2\_min} = V_{C2} - \frac{\Delta V_{C2}}{2}. \quad (6)$$

The input power ripple is calculated according to the following equation:

$$\Delta P = \frac{2}{\pi} \int_0^{\pi/2} (P_{max} - P_{in}) \sin(2\omega t) d\omega t. \quad (7)$$

The energy that must be stored in the impedance capacitors in order to mitigate the ripple is defined as:

$$\Delta E = \Delta P \cdot \frac{T}{4} = \frac{P_{in} T}{2\pi}, \quad (8)$$

where $T$ is the fundamental period.

This energy is distributed between capacitors $C_1$ and $C_2$ according to the voltage variation:

$$\Delta E_1 = \frac{C(V_{C1\_max}^2 - V_{C1\_min}^2)}{2} = C \cdot V_{C1} \cdot \Delta V_C, \quad (9)$$

$$\Delta E_2 = \frac{C(V_{C2\_max}^2 - V_{C2\_min}^2)}{2} = C \cdot V_{C2} \cdot \Delta V_C. \quad (10)$$

Finally, the total energy can be expressed as:

$$\Delta E = 2\Delta E_1 + 2\Delta E_2 = 2C \cdot V_{C1} \cdot \Delta V_C + 2C \cdot V_{C2} \cdot \Delta V_C. \quad (11)$$

From (11), the value of the capacitor can be calculated:

$$C = \frac{P_{in} \cdot T}{4\pi \cdot \Delta V_{dc} (V_{C1} + V_{C2})}. \quad (12)$$

Considering that DFR is compensated by the control system and capacitors, the inductor of the impedance network can be selected taking into account high frequency current ripple only. The following expression is presented in many papers:

$$L_1 = L_2 = L_3 = L_4 \geq \frac{V_{in}^2 \cdot (1-D) \cdot D}{2 \cdot P_{in} \cdot f_S \cdot K_I \cdot (1-2 \cdot D)}, \quad (13)$$

where $K_I$ is a current ripple factor and $f_S$ is switching frequency.

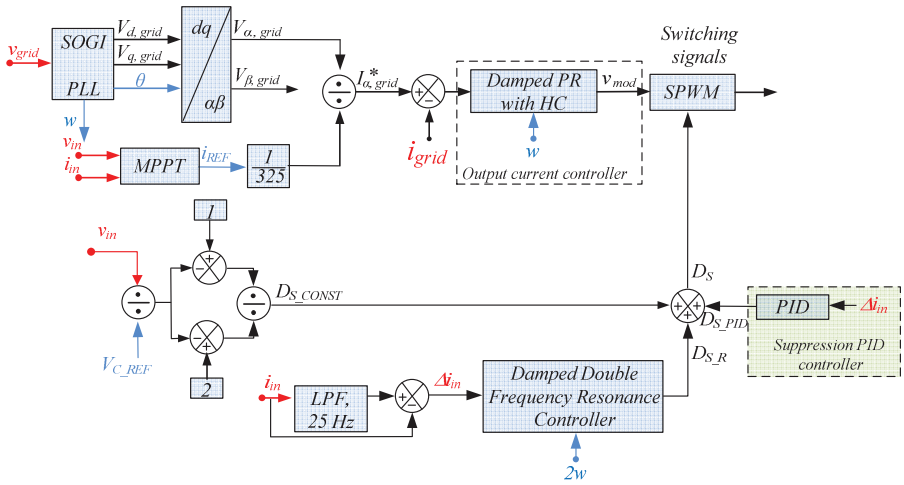


Fig. 2. Block diagram of the proposed control strategy.

## III. CONTROL SYSTEM DESCRIPTION

The proposed control strategy is presented in Fig. 2. The control system can be divided into two parts. The first part provides the desirable value of the dc-link voltage, the other one controls the quality of the output current, which will be injected into the distorted grid.

### A. Output current controller

In order to produce the output current that will be injected into the distorted grid with THD that satisfies the international standards (it should be less than 5%), the LCL output filter and damped PR controller with the Harmonic Compensation (HC) approach were applied. HC was applied to attenuate the value of the 3rd, 5th, 7th, 9th order harmonics. Detailed tuning of the PR controller for 3L NPC qZSI is discussed in [12]. The damped PR controller was selected because it provides high gain at the tuning frequency over a wider band in comparison with the conventional PR controller. Comparison of a conventional PR controller and a damped PR controller is presented in [15]. The damped PR controller with the HC transfer function is:

$$G_{dPR\_HC} = K_p + \Sigma \frac{K_H s}{s^2 + 2\omega_{CH} s + \omega_H^2}, \qquad (14)$$

where $H$ is the harmonic order, $w_{CH}$ is cut-off frequency that is defined for each harmonic separately.

The applied control strategy of the SPWM is described in [24]. It is reported that the carrier signal of the ST state has double frequency that relates to the carrier signals of the active state. Thus, in the proposed case, we obtain: $f_{sw}=50\ kHz$ when $Ds=0$, and $f_{sw}=100\ kHz$ when $Ds>0$.

The value of the $D_{S\_CONST}$ provides an average value of the ST required to maintain the average voltage in the inner capacitors $V_C$.

### B. Resonant suppression controller

The function of the suppression controller is to acquire the desirable voltage fluctuation in the dc-link that should provide the corresponding voltage fluctuation across impedance capacitors, which allows reducing the power fluctuation in the input side by means of the time-varying of the ST duty cycle. Detailed description is provided in [18] and a resonant controller is proposed in order to suppress the DFR.

The same structure is used in this paper. It has been shown that qZSI may have right half-hand plane zero that limits the system dynamic response. It is a typical non-minimum system. At the same time, the study above has overlooked the possible problems with fluctuations of the input current due to the resonance in the qZS network.

Fig. 3 shows a dynamic model of the input current control loop. It is based on the qZSI small signal model presented in several papers [25]-[27]. It has been shown before that the dynamic behavior of the qZS network strictly depends on the value of the passive components. In the studied case, the value of passive components was selected in order to provide the demanded input and output current quality. At the same time, it cannot be oversized because of practical reasons. As a result, the control system should be tuned for optimal passive component values.

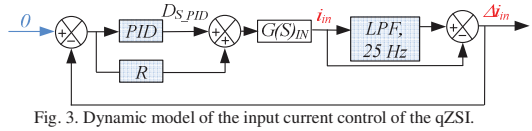


Fig. 3. Dynamic model of the input current control of the qZSI.

The $G(S)_{IN}$ transfer function is derived from the small signal model of qZSI and defines the link between the ST duty cycle and the input current variation. The main purpose of this loop is to suppress possible input current fluctuations connected with the resonance feature of the qZS network.

## IV. Comparative Analysis of the Proposed Control System

This section describes the proposed modification of the control strategy in detail and presents a comparative analysis of our approach and other approaches proposed before.

Fig. 4 shows the root locus diagrams of the dynamic model depicted in Fig. 3. Fig. 4*a* shows the diagram of the system without a PID controller; Fig. 4*b* shows the diagram of the system with a PID controller. As can be seen, the qZ-source inverter with a resonant controller and without a PID controller has roots and zeros that are very close to the axes center. As a result, the system is very sensitive and has complex dynamic behavior.

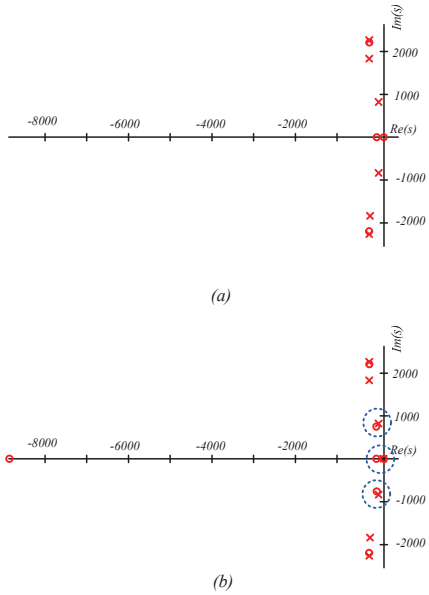


Fig. 4. Root locus diagram of the input current control transfer function without (a) and with (b) PID controller.

Fig. 4*b* shows that adding of a PID controller leads to additional poles and zeros that compensate already existing roots and zeros. As a result, better dynamic performance is expected.

Theoretically, it is possible to tune a PID controller in order to completely eliminate some poles and zeros. But in practical applications it is not possible because of limited passive elements tolerance.

Fig. 5 shows the Bode diagram of the input current control transfer function with a resonant controller but without a PID controller. The system has several resonance peaks, the left one corresponds to the resonant controller, while the right one corresponds to the qZS network resonance frequency.

The main point is that phase shift approaches 180 degrees in the high frequency domain. To shift zeros and poles deeper in the left half-plane, an additional PID controller was applied. The Bode diagram of PID controllers is shown in Fig. 6 and the body diagram of the open loop full transfer function is shown in Fig. 7.

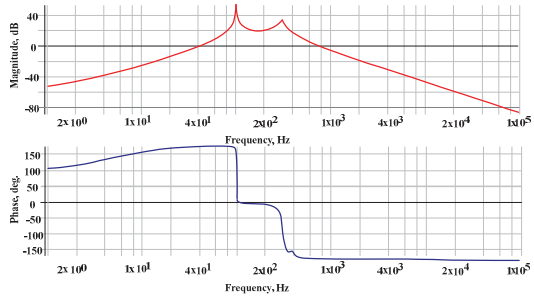


Fig. 5. Bode diagram of the open loop input current control transfer function with a resonant controller.

It can be seen that the PID controller introduces an additional phase lead and the summarized phase shift is closer to 0 degrees, as depicted in Fig. 7. The PID controller corrects phase shifting along with the smoothest gain in the whole range of the frequency domain. As a result, the system is more stable and predicted.

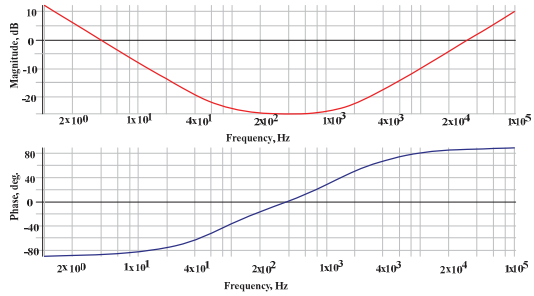


Fig. 6. Bode diagram of the PID controller.

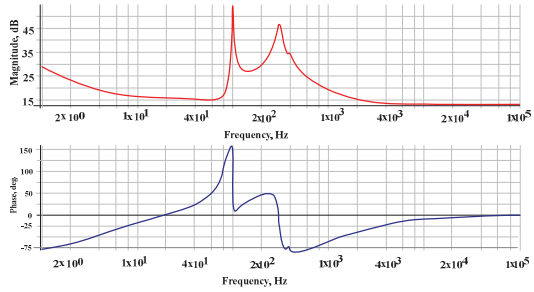


Fig. 7. Bode diagram of the open loop input current control transfer function with resonant and PID controllers.

## V. Simulation Results

Table 1 presents the parameters of the study system that was used in the simulation. Fig. 8 shows the simulation results by using the R term *(a)*; by using the R term with the PID controller *(b)*; transient time by using the R term with the PID controller *(c)*. From top to bottom: input power; summarized voltage across the impedance capacitors and voltage across impedance capacitors separately; ST duty-cycle; grid voltage and current.

TABLE 1. PARAMETERS OF THE 3L SINGLE PHASE QZSI UNDER STUDY

| Parameters | Value |
|---|---|
| *General parameters* | |
| $V_{in}$ | 360 V |
| $V_{Grid}$ | 230 V ac |
| $V_{dc\_ave}$ | 474V |
| $V_{dc\_peak\ to\ peak}$ | 68 V |
| $f_{switching}$ | 50 kHz (100 kHz) |
| $f_{line}$ | 50 Hz |
| *Passive components* | |
| $C_1$, $C_2$,$C_3$,$C_4$ | 0.7 mF |
| $L_1$,$L_2$,$L_3$,$L_4$ | 0.240 mH |
| $R_{qZS}$ | 0.1 Ohm |
| $L_{fi}$ | 0.44mH |
| $L_{fg}$ | 0.22mH |
| $C_f$ | 15, 47 uF |
| $R_f$ | 0.1 Ohm |
| *Input current controller: PID with Resonant controller* | |
| *PID(P)* | 0.05 |
| *PID(I)* | 0.04 |
| *PID(D)* | 5 us |
| *R* | 10 |
| *Output current Proportional-Resonant controller* | |
| $K_P$ | 0.5 |
| $K_1$, $K_3$, $K_5$, $K_7$, $K_9$ | 100; 100, 150, 10, 20 |
| $w_{C1}$, $w_{C3}$, $w_{C5}$, $w_{C7}$, $w_{C9}$ | 0.314, 3.14, 3.14, 3.14, 3.14 |

In Fig. 8*b*, the ripple of the input power is 533 W while the average input power is 1800 W, the ripple across impedance capacitors is 68 V and 17 V across each capacitor separately, which corresponds to the calculation results; the ST duty cycle has high frequency ripple to mitigate fast dynamic pulsation in the input power, the THD of the grid current is about 5%. Fig. 8*a* shows that obviously the R term is not enough to achieve the desired purpose. The ripple of the input power is significant. The quality of the output power was deteriorated. Fig. 8*c* presents the transient time from zero to 0.8 sec. at the moment of time the relay connects the inverter to the grid. At the moment of time 0.2 sec, the inverter starts to operate without the input current mitigation algorithm. Finally, at the moment of time 0.5 sec, the proposed control strategy starts to work.

## VI. CONCLUSIONS

This paper presents the technique of passive power decoupling realized by the modified control strategy based on the resonant with PID controllers. It was shown that the resonant controller cannot provide the satisfied operation mode of the passive decoupling approach due to the possible resonance in the qZS network while the application of the PID controller allows elimination of some zeros and poles, resulting in the stable system.

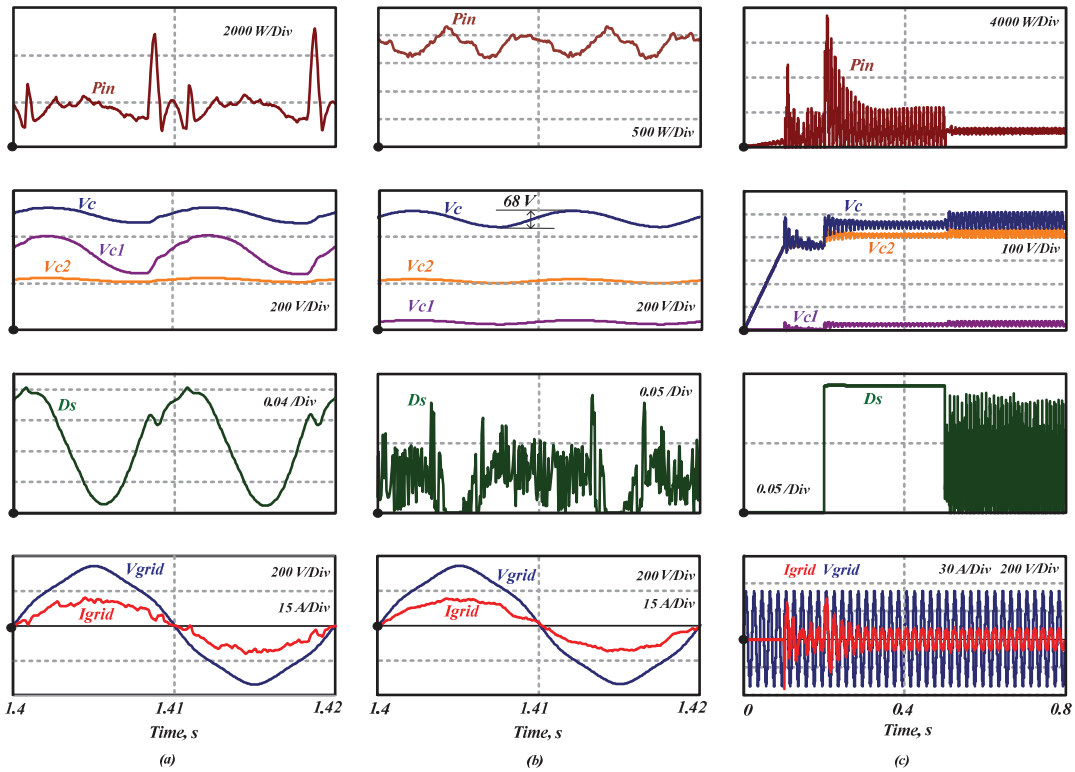


Fig. 8. Simulation results with a resonant controller (a); simulation results with a resonant and a PID controller (b); simulation results of transient time with a resonant and a PID controller (c).

The main idea of passive decoupling is to charge and discharge the impedance capacitors when it is needed. The capacitors of the impedance network should be able to absorb the required ripple energy. Based on this statement, the passive components of the impedance network were calculated. When the grid reduces the consumption of power, the capacitors are discharging and return that energy when the demand of power by the grid is increasing; as a result, the fluctuation of the input power is minimized. For proper work of the resonant term, the ST should exceed zero in all operation modes. Thus, the dc-link voltage is non-fixed, the voltage stress of the switching devices is increasing as compared to the control strategy without the decoupling approach but for low voltage applications and for the 3L converter, this value is not critical. The simulation results confirm the validity of the studied work. The ripple of the input power is 30% at nominal power while the fluctuation confirmed theoretical predictions.

## ACKNOWLEDGMENT

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[PAPER-VI] E. Makovenko, O. Husev, C. Roncero-Clemente, E. Romero-Cadaval, D. Vinnikov, “A Single-Phase 3L qZS Inverter Connected to the Distorted Grid with Battery Storage and Active Power Decoupling Function”, IEEE 59th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON), pp. x-x, 2018.

# Single-Phase Three-Level qZ-Source Inverter Connected to the Grid with Battery Storage and Active Power Decoupling Function

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***Abstract*— This paper introduces a single-phase three-level neutral-point clamped quasi-Z-source inverter with battery storage and active power decoupling (APD) function. Main focus is on the tuning process of the digital control system of the investigated topology by taking into account digital delay caused by digital realization. The results of our approach are validated by simulation.**

***Keywords — active power decoupling; single-phase inverter; digital delay; quasi-Z source.***

## I. INTRODUCTION

Photovoltaic (PV) based energy generation systems have expanded worldwide [1]-[4]. To extend the input voltage regulation range, solutions based on Impedance-Source (IS) networks have been proposed [5]-[12]. As compared to conventional voltage source converters, the buck-boost mode presented does not suffer from the Shoot-Through (ST) states. The quasi-Z-Source Inverter (qZSI) draws continuous input current from the source. These inverters are also capable of performing Maximum Power Point Tracking (MPPT) without an extra dc-dc converter.

The Three-Level (3L) Neutral Point Clamped (NPC) qZSI concept proposed in [13] combines advantages of 3L topology with an impedance source (IS) network. Further development of this topology with storage battery integration described in [14] is shown in Fig. 1.

To improve the use of PV modules, the APD circuit is used to attenuate double frequency ripple of the input power. A possible scenario is described in [15]-[17]. At the same time, the scenario proposed in [17] does not allow for the combination with battery storage integration, while the scenario proposed in [15] can use the storage battery instead of a decoupling capacitor.

The proposed solution combines battery storage integration with the APD of the single-phase power ripple.

This paper presents the tuning process of a single-phase 3L qZSI connected to the grid with battery storage and APD. The tuning process takes into account the sampling frequency and digital delay that consists of a measurement sample delay and computational delay.

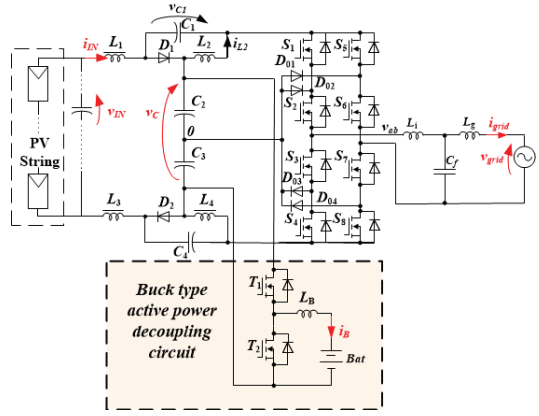


Fig. 1. Single-phase PV system using 3L NPC qZSI along with battery storage integration and APD.

## II. DIGITAL CONTROL SYSTEM TUNING

Fig. 2 shows the proposed control strategy. The control system can be divided into two main parts. Fig. 2a presents the control system for the main circuit where Maximum Power Point Tracking (MPPT) algorithm operates based on the Perturb and Observe (P&O) method to extract maximum power from solar panels, Phase-Locked-Loop (PLL) block to synchronize grid voltage and damped Proportional-Resonant (dPR) controller with Harmonic Compensation (HC) circuit to control the grid current. Also, a Proportional-Integer-Derivative (PID) controller is used to control virtual dc-link voltage. This part of the control system is described in [18].

Fig. 2b presents the control system for battery storage interfacing and APD. The reference current is formed by the dPR controller with HC circuit. The difference between the reference current and measurement buffer current gives an error that goes to the hysteresis controller with constant switching frequency. If the error is positive, the battery is charging by absorbing extra power from the input side; if the error is negative, the battery is discharging by giving back power into the input side; therefore, input power ripples are being attenuated. This control system is partially described in [15].

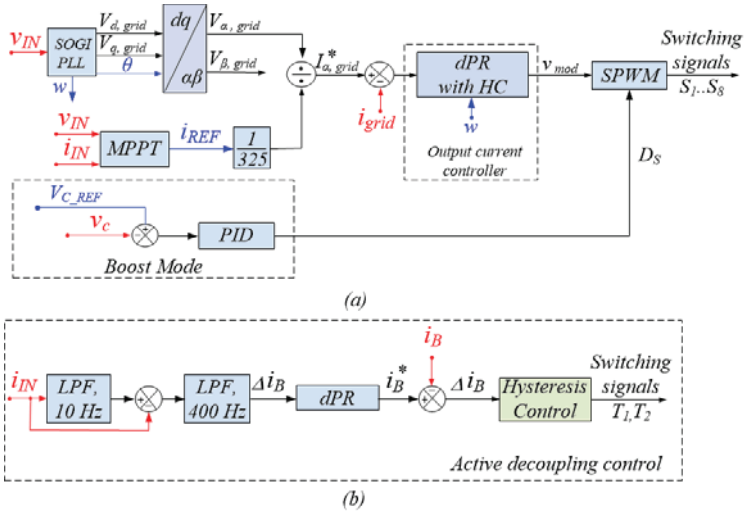


Fig 2. Block diagram of the proposed control strategy: 3L NPC qZS inverter control (a), APD circuit control (b).

The control algorithm of the battery storage interface is added. The system may produce active and reactive power from the battery. The digital realization of the system, which gives digital delay causing the instability of the system, is reported in [19], [20]. It should be taken into account during the tuning process. Also, sampling frequency should be considered.

There are a few compensation delay methods that can be used to reduce the influence of digital delay; however, they are suitable for simple control systems, for instance, in cases with a sinusoidal signal where a SOGI-based time delay compensator could be applied [21], [22]. But if the applied system is complex and consists of a few control subcircuits, it is difficult to achieve the desired results by means of one compensation method.

Today's semiconductors can achieve very high switching frequency. At the same time, computational frequency is limited, in particular, in low cost control systems applied for low power devices. In order to avoid additional outlay and fasten the computational process, one of the possible solutions is to separate functionality between Field Programmable Gate Array (FPGA) and Digital Signal Processor (DSP).

Fig. 3 presents the process where the desired modulation signal is compared with the triangle signal, but due to the sampling period, the delay occurs as a result of the difference between the measured, processed signal and the real signal at the current moment, which can lead to the instability of the system. It is required then to start the retuning process of the control system, namely the controller's coefficients change in order to achieve stable state of the system or integrate some of the compensation methods.

In this particular case, the measurement signal goes through three steps before the resulting signal will be obtained. Fig. 4 presents the processing steps.

The delay of the measurement takes one step. The delay caused by information processing from Analog to Digital Converter (ADC) to DSP and between DSP and FPGA is composed of two steps. In sum, the total delay takes three steps. The sampling frequency is 20 kHz, which means that the delay caused by one step is 50μs and the total delay of three steps is 150 μs.

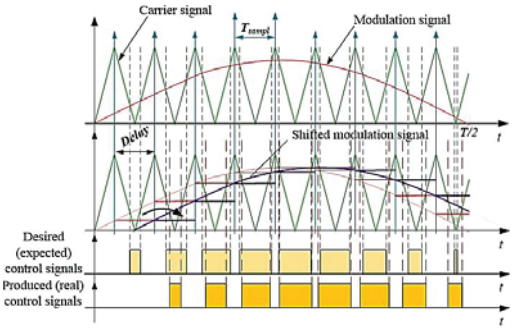


Fig.3 Processes in the digital part.

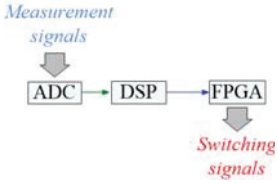


Fig 4 Block diagram of the signal processing.

For the case study system, two resonant controllers were used. The first dPR controller with the HC circuit was used to attenuate 3rd,5th,7th,9th order harmonics of the grid current.

In order to speed up the transient process, the feed forward sinusoidal signal from the PLL block was added. Another dPR controller was used to create the Double-Frequency Ripple (DFR) of the current across the buffer circuit.

The digital system operates in the *Z*-domain. There are different discretization methods to transfer the system from the S-domain to the *Z*-domain. Different studies have compared methods to be applied for higher accuracy in different applications [23]. The aim is to select a discretization method that would provide the best converge of characteristics over the considered frequency range of the processed signal in the *Z*-domain with itself in the S-domain. In this work, the backward discretization method was applied for a PID controller and pre-warpping discretization method for dPR controllers (with HC circuit). Fig. 5 illustrates the difference between the S- and the Z-domain realization of the PID controller.

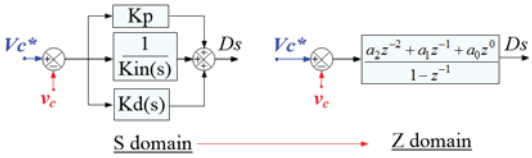


Fig. 5 Block diagram of a PID controller in the S- and Z-domains.

Also, it is needed to take into account the phase shift of each order harmonic which are caused by the three steps after the measurement process and compensate them. The phase shift can be expressed as:

$$\varphi_h = h\frac{2\pi N T_{sample}}{T_{fund}} \ (rad). \qquad (1)$$

where $T_{sapmle}$*=20 kHz* $T_{fund}$*=0.02 s* is a fundamental period, *N* is full delay *=3, h* is order harmonic.

Fig. 6 presents the dynamic model of the input current control of the qZSI with a battery interface circuit. In this work, the 3L NPC configuration with a symmetrical qZ-source network can be simplified, as shown in Fig. 6. The simplification does not affect the dynamic behavior of the system.

The principle of calculation of the small signal model of the qZSI is described in [24]. The guidelines presented for the design of the qZSI use the calculation of its small signal models. For that reason, the basic calculation of the small signal model is not described in this paper. The final equations of the transfer function of the qZSI are:

$$\left[\frac{G_{id}(s)}{G_{vd}(s)}\right]_{\Delta u(s)=0} = C\cdot(s\cdot I - A)^{-1}\cdot M\,, \qquad (2)$$

$$\left[\frac{G_{iu}(s)}{G_{vu}(s)}\right]_{\Delta d(s)=0} = C\cdot(s\cdot I - A)^{-1}\cdot B\,. \qquad (3)$$

where Eq. (2) gives two transfer functions, current and voltage, which depend on the duty cycle. Eq. (3) gives also two transfer functions but they depend on the voltage changing.

In this work, two out of four transfer function are applied to tune the system:

$$G_{vd}(s) = C\cdot(s\cdot I - A)^{-1}\cdot M\,, \qquad (4)$$

$$G_{vu}(s) = C\cdot(s\cdot I - A)^{-1}\cdot B\,. \qquad (5)$$

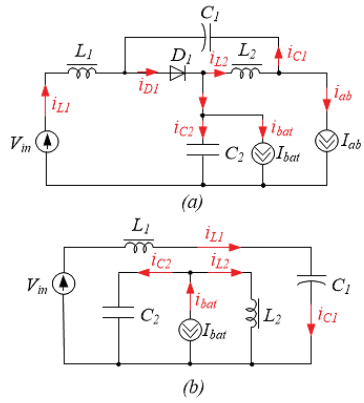


Fig. 6 Equivalent schemes (a) active state; (b) shoot-through state

The first transfer function is applied to tune the PID controller since the dc-link voltage is controlled by the shoot-through duty cycle.

The second transfer function is applied to tune the dPR controller. The input current depends on the dc-link voltage because of the buffer's current, which under control, causes the changing of the dc-link voltage.

Figs. 7 and 8 show the bode diagrams of the system controlled by the dPR controller with two sets of different parameters: first when the system is stable only in the S-domain *(Kp=0.6; Ki=50)*, second, when it is stable on both domains *(Kp=0.5; Ki=50)*.

The transfer function is expressed as:

$$TrF_{dPR}(z) = G_{vu}(z)\cdot dPR(z)\,. \qquad (6)$$

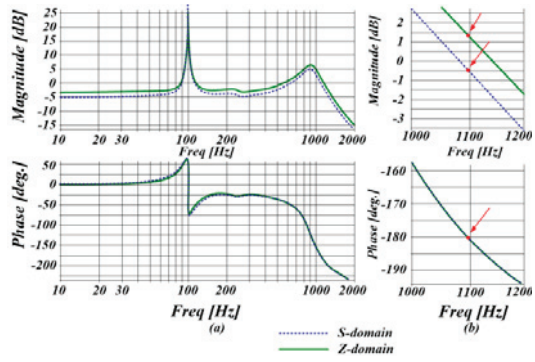


Fig. 7 Bode diagram of the qZSI with an unstable dPR controller.

In Fig. 7*b*, red dots show that even if the system is stable in the S-domain, it does not mean that it would be stable in the Z-domain, because the digital delay causes the positive amplitude shift at the phase that equals 180 degrees and that

leads to the instability of the system. Fig. 8 presents the case when the system keeps stability in both domains. In order to achieve the stability of the system in the Z-domain, the proportional coefficients of dPR were increased.

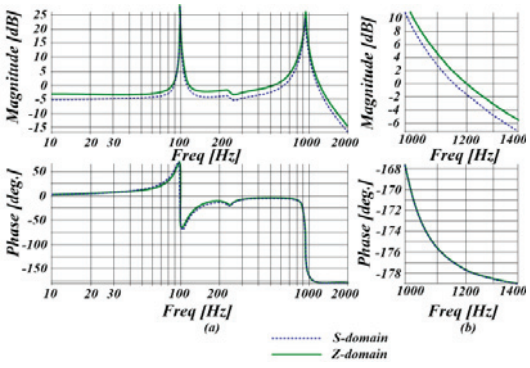


Fig. 8 Bode diagram of the qZSI with a stable dPR controller.

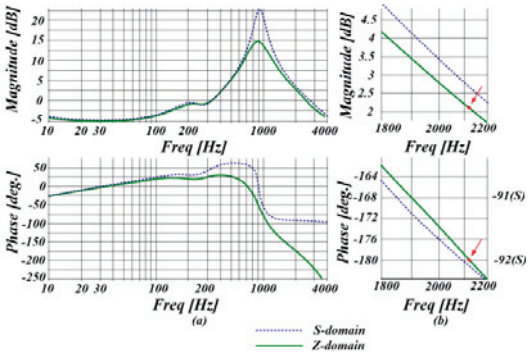


Fig.9 Bode diagram of the qZSI with an unstable PID controller.

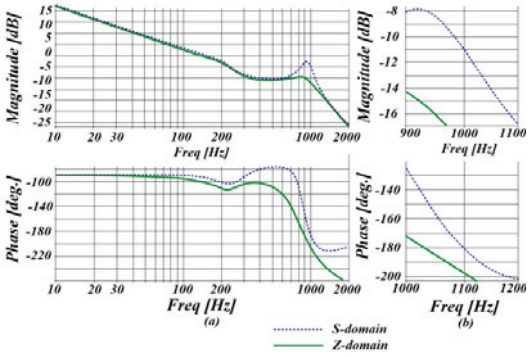


Fig.10 Bode diagram of the qZSI with a stable PID controller.

Figs. 9 and 10 show the bode diagrams of the system controlled by the PID controller with two sets of different parameters: first, when the system is stable only in the S-domain *(Kp=0.001; Ki=30; Kd=1e-6)*, second, when it is stable on both domains *(Kp=0.0001; Ki=1.2; Kd=1e-8)*. The transfer function is expressed as:

$$TrF_{PID}(z) = G_{vd}(z) \cdot PID(z)\,. \tag{7}$$

Figs. 9 and 10 show that the behavior of the system is the same as in Figs. 7 and 8. Fig. 9 presents the case when the system is stable only in the S-domain and it is not stable in the Z-domain due to the presence of digital delay, because it causes the critical phase shift and magnitude shift. Fig. 10 shows the case when the system keeps stability in both domains. In order to achieve the stability of the system in the Z-domain, all the coefficients of the PID controller were increased.

## III. SIMULATION RESULTS

To verify the presented theoretic statements, PSCAD program tools were used for the simulation results.

Table 1 presents the parameters of the case study system that were used for simulation.

Table 1. Parameters of the studied topology

| *Parameters* | *Value* |
|---|---|
| *General parameters* | |
| $V_{in}$ | *360 V* |
| $V_{Grid}$ | *230 V ac* |
| $P_{grid}$ | *900 W;1400 W; 800 W* |
| $f_{switching}$ | *50 kHz (100 kHz)* |
| $f_{switching(buffer)}$ | *100 kHz* |
| $f_{line}$ | *50 Hz* |
| $f_{sample}$ | *20 000 Hz* |
| $T_{full\ delay}$ | *0.00015* |
| *Passive components* | |
| $C_2, C_3$ | *0.05 mF* |
| $C_1, C_4$ | *1.39 mF* |
| $L_1, L_2, L_3, L_4$ | *0.240 mH* |
| $R_{qZS}$ | *0.1 Ohm* |
| $L_{fi}$ | *0.44mH* |
| $L_{fg}$ | *0.22mH* |
| $C_f$ | *15, 47 uF* |
| $R_f$ | *0.1 Ohm* |
| $L_B$ | *2 mH* |
| *Bat* | *96 V* |
| *PID controller* | |
| *a0, a1, a2* | *0.000162; -0.00014; 0.00002* |
| *b0, b1* | *1; -1* |
| *dPR controller* | |
| $Kp, K_h, w_C$ | *-1; -100; 3.14* |
| *Output current dPR controller with HC circuit* | |
| $K_P, K_{RES1}, w_{C1}$ | *0.9, 100, 0.314* |
| $K_{RES3}, K_{RES5}, K_{RES7}, K_{RES9}$ | *100,150,10,20* |
| $w_{C3}, w_{C5}, w_{C7}, w_{C9}$ | *3.14, 3.14, 3.14, 3.14* |

An important aspect is that the capacitance of capacitors C2 and C3 is reduced, which allows us to create voltage ripple across them; therefore, in the dc-link as well and finally to perform APD.

Fig. 11 shows the simulation results of the investigated topology with digital delay at the steady-state mode; the output power is 900 W. The battery is not used as a storage element, but only as a source to provide power decoupling.

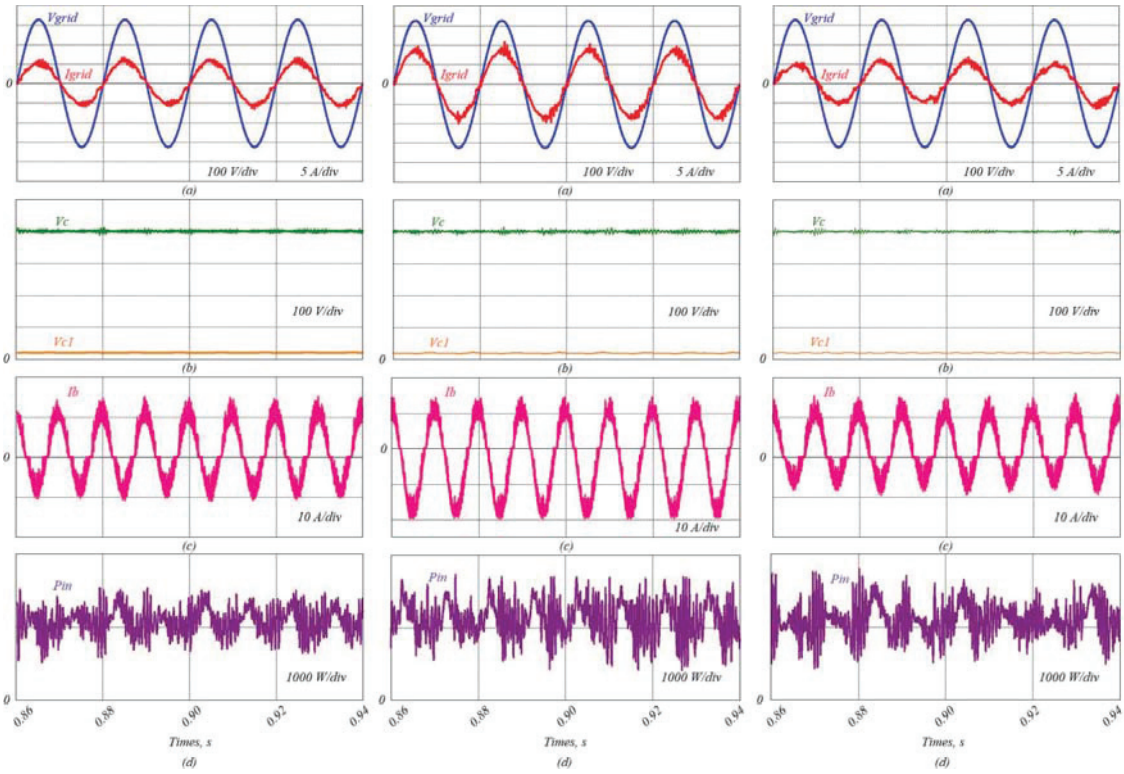


Fig. 11. Simulation results at the steady state mode of the investigated system with digital delay and without additional support of grid demand: voltage grid and current (a); voltage across impedance capacitors (b); current across buffer circuit (c); input power (d).

Fig. 12. Simulation results at the steady state mode of the investigated system performed with digital delay while the battery extra power was produced by the PV system: voltage grid and current (a); voltage across impedance capacitors (b); current across buffer circuit (c); input power (d).

Fig. 13. Simulation results at the steady state mode of the investigated system performed with digital delay while the battery transfers some power to the grid: voltage grid and current (a); voltage across impedance capacitors (b); current across buffer circuit (c); input power (d).

From top to bottom: *(a)* voltage grid, current grid; *(b)* voltage across two impedance capacitors $C_2$,$C_3$ – *Vc*, *(c)* voltage across impedance capacitor $C_1$; *(d)* current across buffer circuit; input power.

Figs. 11*a-d* show that the system is at the steady-state mode and it is stable, which means that the system is tuned correctly.

Fig. 11*a* shows that the produced current is synchronized with the grid voltage and the THD of the current is 4%, which means that the output dPR controller with HC and with phase compensation are tuned properly and the system is able to provide required quality of the grid current despite the presence of digital delay.

Fig. 11*b* shows that the PID controller is tuned correctly and the voltage across the impedance capacitor *Vc* is retained at the predefined voltage level 400 V with minimum ripples.

Fig. 11*d* shows that the input power ripples are reduced up to 39% from full regions of pulsation, thus the APD copes with the task.

Figs. 12*a-d* show the simulation results of the investigated topology with digital delay at the steady-state mode with increased output power up to 1400 W. The battery is used as a storage element that feeds the load by transferring the absent power value produced by the input side.

Fig. 12*a* shows that the produced current is synchronized with the grid voltage and the THD of the current is 3.3%.

Fig. 12*b* shows the voltage across impedance capacitors, its value is not changed, which means that the PID controller copes with its task.

Fig. 12*d* shows that the input power ripples are reduced, thus the APD copes with the task even if the output power is increased and the battery does not only provide the power decoupling but also feeds the grid.

The input power ripples are reduced up to 35.7% from nominal power ripples.

Fig. 13*a-d* show the simulation results of the investigated topology with digital delay at the steady-state mode, the output power is reduced up to 800 W. The battery is used as a storage element which absorbs extra power from the input side.

Fig. 13*a* shows that the produced current is synchronized with the grid voltage and the THD of the current is 3.3%.

Fig. 13*b* shows that the voltage across impedance capacitors stays at the same level as in previous two cases; the PID controller copes with its task even in this situation.

Fig. 13*d* shows that the input power ripples are reduced up to 62.5% from nominal power ripples, thus the proposed topology and control strategy provide the APD even if the output power is reduced and the battery along with power decoupling also absorbs extra power from the input side.

## IV. CONCLUSIONS

Focus in this paper is on the practical implementation of the APD system taking into account the digital delay, sampling and switching frequency.

Typically, it is difficult to achieve the stability of the system with all mentioned parameters and it may be necessary to reduce some of them in order to stabilize it.

The simulation results of a single-phase 3L NPC qZSI connected to the grid with battery storage and APD under different output power requirements confirmed that the system was tuned correctly in the Z-domain where digital delay and sampling frequency were taken into account. The system is able to keep stability and provide required quality of produced current and mitigated DFR of the input power even if the required output power is changed and in that case, the battery provided the support to keep power balance between the input-output. To verify the selected parameters of the controllers in the Z-domain, the plotted bode diagrams confirmed all the results obtained.

## ACKNOWLEDGMENT

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# Single-Phase qZS-based PV Inverter with Integrated Battery Storage for Distributed Energy Generation

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***Abstract*—This paper presents an experimental setup of quasi-Z-source-based inverter for photovoltaic application solution with storage integration. It fully describes the industrial prototype experimental setup considering its complete functionalities. The specifications of this system were made taking into consideration the context of smart-grids and the support of low voltage networks. Experimental results are presented. The main pros and cons are discussed.**

***Keywords— quasi-Z-source network, unfolding circuit, storage batteries.***

## I. INTRODUCTION

Present technologies and innovations have led to the worldwide expansion of Photovoltaic based (PV) energy generation systems [1]-[4]. PV energy sources are characterized by a wide output voltage and power variation. Therefore, the PV system power electronics converters should have a wide input voltage and load regulation range. To extend the input voltage regulation range, solutions based on Impedance-Source (IS) networks have been proposed [5]-[10]. They present a buck mode, a boost mode and do not suffer from the Shoot-Through (ST) states, when compared with conventional voltage source converters. In advance, the quasi-Z-Source Inverter (qZSI) draws Continuous Input Current (CIC) from the source and shares a common ground with a dc-source suitable for renewable energy applications, in particular for the PV systems. These inverters are also capable of performing Maximum Power Point Tracking (MPPT) without an extra dc-dc converter. The application of IS based converters for various fields of application are discussed in many research papers [11]-[14].

At the same time, inverters used for the grid integration of PV system can be based on two-level or multilevel topologies. Multilevel inverters offer preferable solutions not only for medium-voltage but also for low-voltage applications. One of the most important benefits of the multilevel inverter is the reduced voltage stress on the semiconductors [15]. The increased number of the output voltage levels leads to an output voltage quality improvement and to the reduction of bulky output filters. The Three-Level (3L) Neutral Point Clamped (NPC) inverter is one of the most popular solutions among the multilevel topologies. The 3L NPC qZSI concept is proposed in [16] which combine advantages of 3L topology along with IS network.

It has traditional advantages that lie on the output voltage quality improvement, reduced voltage stress on the semiconductors allowing the use of fast MOSFETs among other industrially verified Si technologies and a larger nominal power that converter can handle. Moreover, the 3L NPC qZSI has a very wide input voltage operation range.

It should be noticed that some drawbacks are discussed in several papers [17]-[19]. But in opposite there are many papers that demonstrate possible further improvements in many ways [20]-[23]. Another trend and demand in PV systems is application battery storage. It makes the system independent and feasible as autonomous power supply or distributed generation. Several solutions with qZSI and battery integration are presented and discussed in the literature [24]-[27]. At the same time its feasibility for practical application is doubtful [28], being a separate interface circuit for storage battery control more reliable from the practical point of view.

Despite of many research papers there is no feedback from industry reporting about any commercial or industrial prototypes.

The goal of this paper is demonstration of the first industrial prototype designed for residential PV power system which has integrated energy storage. This paper includes detailed description of the hardware setup, accomplished functionalities and experimental results. Possible problems and solutions toward possible commercialization are also discussed in conclusions.

## II. CASE STUDY SYSTEM DESCRIPTION

The case study system is depicted in Fig. 1. The 3L NPC qZSI is the string PV inverter connected to a distorted grid. A PV installation of 10 series connected PV modules is a voltage source for the selected topology. It is well known that solar panels provide limited voltage (V) and current (I) that follow an exponential I-V curve. The main specifications of a commercial solar module (Bisol BMU-255) are detailed in [29].

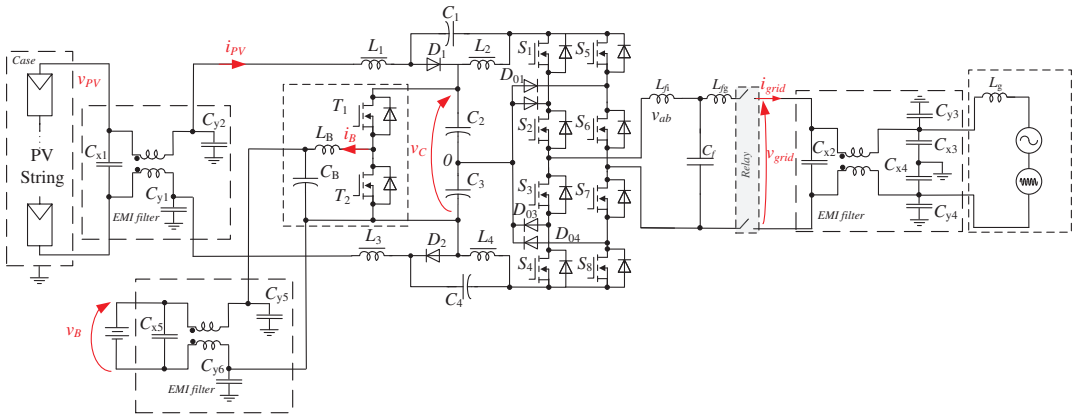



Fig. 1. Single-phase PV system using 3L qZSI.

Even low but equally distributed solar irradiation does not require extremely high boost performance. High boost capabilities are demanded in a partially shaded mode where only some of the modules in the array have lower irradiation The MPP with maximum irradiation over all the modules corresponds to the 390 V input voltage that requires no voltage boost feature from the converter. Fig. 2 shows power-voltage curve of the case study PV string.

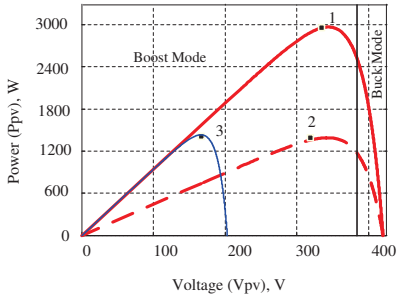



Fig. 2. Power-voltage curve of the case study PV string

From another side it has a battery storage unit with nominal voltage 96 V and capacity about 7Ahour.

The general concept of the single-phase 3L NPC qZSI is described and verified in [16]. It is intended for applications that require a wide operation range of the input voltage along with the CIC.

3L NPC topology allows utilizing high switching frequency conventional Si MOSFETs.

The storage unit is connected to the inner capacitors $C_2$ and $C_3$ of qZS network through the interface converter. The sum of capacitors voltage has voltage not less than 380 V in grid connected mode. At the same time this voltage is smaller than voltage applied to the output filter of inverter, that's why the simple two-level bidirectional dc-dc converter based on transistors $T_1$ and $T_2$ is utilized.

In standby mode the inverter is disconnected from the grid through relay.

The types and values of the passive components used in prototype are selected according to the approach in [15] and presented in Table I.

TABLE I. PASSIVE COMPONENTS OF THE PROTOTYPE

| Parameter or component | Value |
|---|---|
| Capacitors $C_1$ and $C_4$ | *2 mF* |
| Capacitors $C_2$ and $C_3$ | *2.4mF* |
| Inductors $L_1$... $L_4$ | *240 μH* |
| Filter inductor on the inverter side $L_{fi}$ | *0.44mH* |
| Filter capacitor $C_f$ | *15.47 μF* |
| Filter inductor on the grid side $L_{fg}$ | *0.22mH* |
| Battery inductor $L_B$ | *2mH* |
| Switching frequency | *100 kHz* |

Fig. 3 shows the structure of the assembled prototype in a 3U box. It consists of the four main PCB boards and external qZS inductors, storage inductors and inductors of output filters. The control system allows communication with other similar devices through Ethernet connection. In this particular case, a RaspberryPi 3 (RPI3) board is used as intermediate control unit. Its purpose consists in providing remote control and energy management. This communication was introduced in order to integrate the system in a smart-grid with the support of low voltage networks.

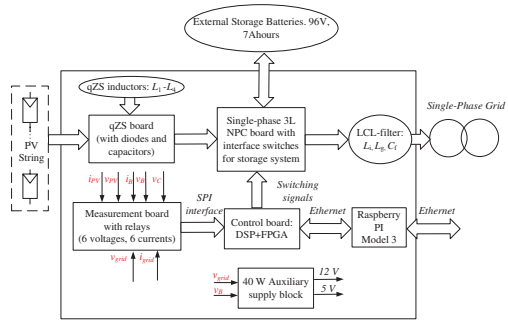



Fig. 3. Structure of the assembled prototype of the 3L NPC qZSI

The measurement board consists of new current sensors TLI4970 with digital output from Infineon and with simple resistor dividers as voltage sensors. For galvanic isolation operational amplifiers ACPL-C87A, and AD converters LTC1864CS8 from Linear Technologies are used, which send data to the control board through the SPI interface. All together this is cost-effective solution. Finally, key active components are summarized in Table II.

TABLE II. ACTIVE COMPONENTS OF THE PROTOTYPE

| Parameter or component | Type |
|---|---|
| Inverter transistors $S_1,\ldots,S_8$ | IPW65R041CFD |
| Storage interface transistors $T_1,..,T_2$ | CMF20120D |
| NPC diodes and qZS diodes | C2M0080120D |
| MOSFETS drivers | ACPL-H342 |
| AD converters | LTC1864CS8 |

## III. CONTROL SYSTEM STRUCTURE AND MODES OF OPERATION

The overall control system of the qZSI contains a few independent blocks, as shown in Fig. 4: MPPT algorithm, Phase-Locked-Loop (PLL), a grid-connected control strategy which is aimed to generate a reference current, a current controller to track the reference and a dc-link voltage control loop.

Several grid-current controllers are possible. In this case, the grid-connected control system is based on the damped PR controller, which is an accepted solution for single-phase systems [30], [31]. This type of controller has been selected because of its relative simplicity and its ability to track sinusoidal references. Moreover, a multi-resonance PR controller is much simpler in real implementation.

A schematic diagram of control system is depicted in Fig. 4. It can be seen that it is represented by two different structures. In particular, Fig.4*a* shows the control approach in case of buck mode, while Fig.4*b* belongs to the boost mode of the qZSI. The main difference is defined by the need of ST control along with MPPT performance. In any mode specially designed algorithm for grid connection is applied. It consists in output filter capacitor pre-charging before relay switched on.

### A. Buck mode

In buck mode the input voltage is higher than required dc-link voltage. It means that ST states are not activated as well as dc-link control. In this case MPPT block generates the peak value of the reference power that provides reference current for the grid or power for battery. There are many review papers devoted to a proper selection of the MPPT algorithm [33]. The incremental conductance method is most attractive for the discussed topology.

The PLL-Second Order Generalized Integrator (SOGI) algorithm was selected for grid synchronization because of the pure and stable sinusoidal output signal despite the distorted grid voltage waveform. The derived sinusoidal waveform is in phase with the fundamental harmonic of the grid voltage and it is used for the reference current signal.

The quality of the injected grid current depends on several parameters. Among them are output filter, switching and sampling frequency. The output filter must be properly designed [34]. An *LCL*-filter possesses a set of advantages. First, the third order filters lead to better attenuation of the switching harmonics and reduced Electromagnetic Interference (EMI). The disadvantages of these filters lie in a more complex power circuit where resonance may lead to undesired oscillations or instability of the system.

When imbalance and distortion occur in the grid voltage, the PR controller performs control to reduce the power ripple, suppressing the most significant undesirable harmonics by means of Harmonic Compensation (HC).Thus, the PR controller and the *LCL*-filter have to provide acceptable output current quality.

Fig. 4 shows that the control signal after the PR controller moves to the Sinusoidal-Pulse-Width-Modulation (SPWM) block with equally distributed ST states in each switching period. Where the $D_S$ is a ST duty cycle and set to 0 in this mode.

The buck mode is always activated at the beginning of power generation process till the moment of time when input voltage is crossing the dc-link reference voltage.

### B. Boost mode

In boost mode ST states are activated in order keep dc-link voltage not less than the nominal value. It should be noted that in qZSI the dc-link voltage has zero states due to the ST implementation and as a result it is difficult to control the average value. At the same time, in case of constant boost control the average voltage of dc-link is equal to the voltage $V_C$ across inner capacitors $C_2$ and $C_3$. To stabilize the average dc-link voltage, a simple PI controller is implemented.

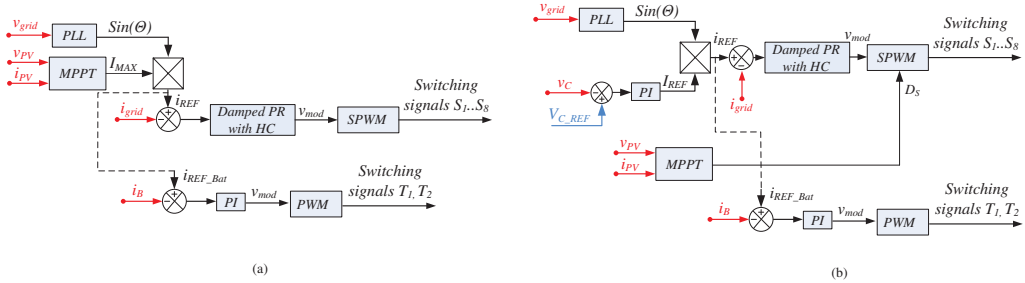



Fig.4. Dynamic model of the current controller (a) and dynamic model of the dc-link controller (b).

The output signal of this controller provides the peak value of the reference current. Thus, the voltage of inner capacitors' ($C_2$ and $C_3$) remains constant due to the power balance control. At the same time MPPT block provides value of ST duty cycle.

As it can be seen the MPPT block is switching between generation of reference power in the buck mode and ST duty cycle in the boost mode. It is explained by better stability in the boost mode. The MPPT control is much slower than dc-link control or output current control and is considering like a disturbance for them. In order to provide smooth transient between modes the value of $D_S$ and reference power are exchanged between correspondent blocks. Also, the hysteresis band is added in order to avoid high frequency oscillation at the boundary of the modes.

Battery power control is realized by means of simple PI controller which output value is given to the PWM block. The input of PI controller is battery current error. The reference current of the battery is defined by complex algorithm which description is out of this paper. It includes information about reference power from MPPT, external information about required power to the grid and the state of charge of the battery.

## IV. Experimental Results

This chapter is devoted to the detailed description of experimental results. Fig. 5 shows the industrial prototype of the converter. It corresponds to the block diagram presented in Fig. 3.

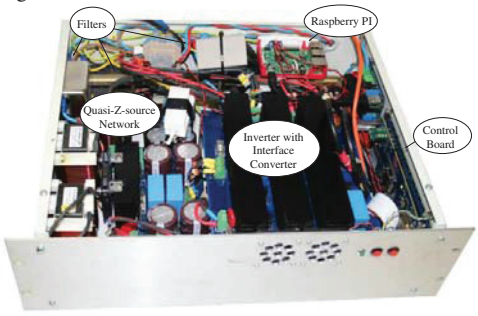



Fig.5. Industrial prototype of 3L NPC qZSI with interface converter for storage integration.

The nominal input and output grid power is 3.3 (kVA). The interface converter designed for 10A maximum current of the battery and tested in a voltage range from 64V to 380V. In the case study system, the simple battery set with 96 V nominal voltage is utilized. The real discharge and charge current depends on the state of charge of the battery.

Fig. 6 shows the experimental waveforms in one of the typical operation modes. All the measurements were made by the oscilloscope Tektronix MSO4043B with voltage and current probes Tektronix TCP0030A with bandwidth no less than 100 MHz. Obtained results were verified with the help of temperature analysis performed by the help of a thermal imaging camera Fluke Ti10.

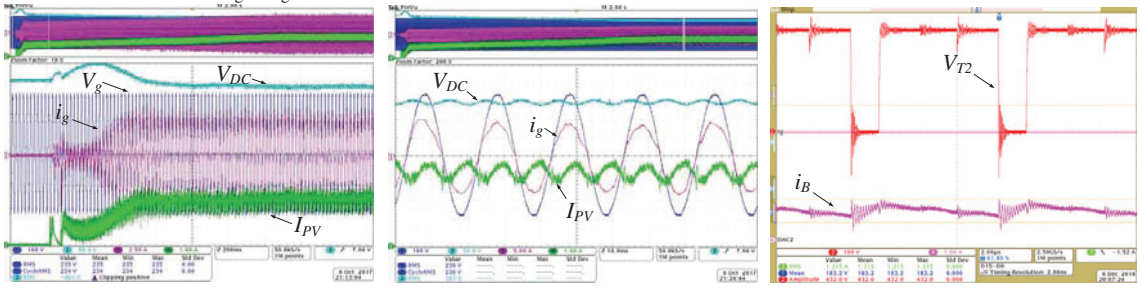
Fig. 6a shows the start up process and MPPT performance. Fig. 6b shows the same diagrams in a steady-state mode. Finally, the steady-state diagrams of battery current along with voltage across transistor of interface converter are depicted in Fig. 6c.

The main conclusion from these figures is that battery and PV currents are continuous. Also, it can be noticed that, the grid voltage contains a significant value of the fifth harmonic, but the quality of grid current corresponds to the standards and THD does not exceed 5% at the nominal power point.

Fig. 7 shows the experimental efficiency of the converter. First of all the Fig. 7*a* shows the losses distribution at the operation point close to the nominal power about 2.8 kW including auxiliary power supply. The overall efficiency is about 95%. It can be seen that losses in transistors give the major losses contribution. In this particular case battery are not involved in power exchange.

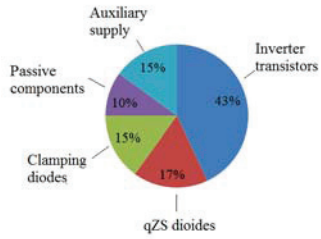
Fig. 7b shows the case study when storage batteries are activated. Also, the voltage from PV panels is much lower, ST states are activated. In this operating point the output power is about 1.2 kW while power from PV 900 W. In this case only 2 qZS diodes make the same contribution to power losses as all inverter transistors. The absolute value of auxiliary power supply losses remains the same. As a result, the overall efficiency drops to 92%.

Finally, the Fig. 7c shows the efficiency of only inverter as a function of input voltage under constant power. It is expected result which is explained by increasing ST and current while voltage decreasing.



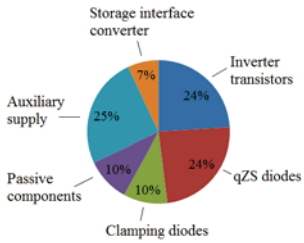

*(a)* *(b)* *(c)*

Fig.6. Experimental results: transient process of PV current, dc-link voltage, grid voltage and current (a), : steady-state curves of PV current, dc-link voltage, grid voltage and current (b), curves of battery current and voltage across transistors (c).



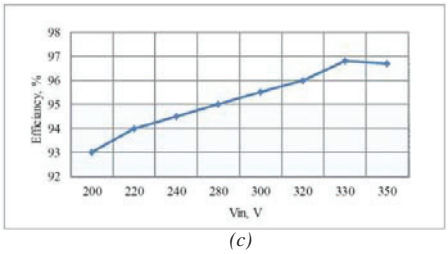

140 W losses distribution

*(a)*




100 W losses distribution

*(b)*




*(c)*

Fig. 7. Efficiency investigation: losses distribution at the nominal power point (a), high-boost point with reduced power (b) and inverter efficiency as a function of input voltage (c).

The high-level energy management is performed by means of special application designed for RPI3 control board which allows realizing remote control. The control signals from RPI3 are coming to the main control board. The main control board consists of two boards based on a combination of the low cost Field-Programmable Gate Array (FPGA) and Microcontroller (µC) with Floating-point Unit (FPU). The bottom side board has a low cost FPGA from Altera Cyclone IV EP4CE6E22C8. The upper side board has µC STM32F417ZET correspondingly. Each of these parts can work independently and communicate through Serial Peripheral Interface (SPI). Such combination provides an effective performance of any complex control.

Fig. 8 shows a screenshot of the remote-control interface. It shows that active and reactive power from the grid, battery power can be controlled separately. Also, it shows power derived from PV panels.

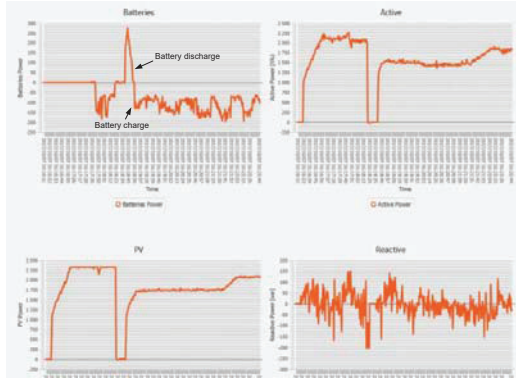



Fig. 8. Remote control interface.

## V. CONCLUSIONS

This paper presents an industrial prototype of qZSI for PV application solution with storage integration. There are many research papers presented similar approach for theoretical study, but none of them discussed industrial implementation, real pros and cons and feasibility of such approach. The team can underline several conclusions:

1. The overall size of magnetic elements is comparable to the conventional solutions. From the one side the qZS network inductors lead to the additional size and cost increasing. From another side, this solution has reduced common mode voltage and reduced EMI filters correspondently.
2. The most feasible and reliable solution for storage integration is additional interface converter. Despite that other solutions based on qZS capacitors are proposed, only additional interface converter may propose full battery current control possibility.
3. The real advantage of ST immunity consists in driver's circuit simplification. Inverter does not suffer from short-circuit problem. It means that only unipolar voltage drivers can be used.
4. Overall voltage stress across semiconductors is higher than in conventional solution. In case of multilevel approach this difference can be mitigated, but should be kept in mind anyway.
5. qZS network has more complex dynamic behaviour compare to conventional boost converter coupled with inverter. It should be taken into account during control system design.

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# Optimization and Implementation of the Proportional-Resonant Controller for Grid-Connected Inverter with Significant Computation Delay

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***Abstract*— The paper describes the tuning process of the proportional-resonant controller taking into account the significant computational delay from the digital control system. Different structures of the controller and related contradicting results are discussed. Particular attention is paid to the stability domain and its dependence on different parameters of the proportional-resonant controller. The main outcome of the paper consists in the tuning approach guidelines for selection of controller parameters in case of significant digital system delay. An optimal controller structure and start-up current optimization are proposed. All results are confirmed by simulation and experimental setup.**

***Index Terms*— dc-ac inverter, proportional-resonant controller, digital control.**

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## I. Introduction

RENEWABLE Energy Sources (RESs) are increasingly important in today's electrical system. European Commission set up a target to raise the share of renewable energy to 20% before 2020 [1], [2]. Denmark expects to reach 70% of energy production from renewable sources by 2020 and 100% by 2050 [3]. Power electronic converters, being the interface between the different RESs and the loads/grid, are of high interest since stricter interconnection requirements and technical standards have been proposed by several utilities.

As the amount of the power electronic converters for renewable applications is growing, the interest in their control systems and associated suitable tuning methods is also increasing. In particular, grid-connected inverters attract much attention because their specifications, both in steady and transient operation, require higher accuracy and fast response.

Different structures of control systems have been proposed for grid-connected inverters [4]-[6]. One of the most used grid-side inverter control is the dual-loop: the outer loop with slower dynamics in the time domain and the inner loop with very fast response to control the current. Regarding this inner current control loop, its controller can be classified as nonlinear and linear. Hysteresis, predictive and dead beat controller types belong to the first controller's group presenting high robustness and fast dynamic response. As a drawback, they require a high sampling rate to achieve better performance. On the other hand, linear current controllers such as Proportional-Integral (PI) based, Proportional-Resonant (PR) based or Repetitive Controller (RC) based have been successful with wide usage. At the same time, such controllers can be implemented in the *dq*-rotational, $\alpha\beta$-stationary or *abc*-natural reference frames. Stationary and natural reference frames are a very popular solution in the case of single-phase systems. The PR controller, first proposed in [7], is a quite simple and attractive solution in the case of *abc*-naturally or $\alpha\beta$-stationary reference implementation frames because, in comparison with the conventional PI controller, it can overcome two well-known drawbacks of the latter: inability to track a sinusoidal reference with zero steady-state error and poor disturbance rejection capability. A similar idea

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of integrating the sinusoidal current in the reference frame has been introduced in [8]. Many detailed studies addressing this type of controllers have been reported. Several papers have demonstrated that PR controllers cover a very wide stability domain [9]-[13], being most of them based on simulation results. In general, it may be concluded that the resonance term has a direct impact on the transient process but does not shift the root loci diagram, while the proportional term has a direct impact on the stability domain.

Several modifications of the PR controller's structure have also been presented. The adaptive PR controller was introduced in [14]-[16], where improvements in the PR controller are proposed for the case of grid frequency deviations. Usually, the nominal value of the grid frequency is set and used inside the PR controller. This solution uses the output value of the Phase-Locked-Loop (PLL) block as a reference value inside the PR controller. As a result, the inverter operation becomes more stable during grid frequency deviations. A similar approach with repetitive controller is also implemented in [17].

On the other side, to increase the stability domain of the PR controller, the damped PR controller was proposed in [18] and discussed with different modifications in [19]-[22]. It was shown that the cut off frequency of the damping term increases the stability domain but can be a reason for the steady-state error.

Opinions and experiences from different research groups present distinct views on this issue. Some researchers do not recommend the damping approach and suggest that the phase compensation approach compensates the time delay of the control system [23]-[27]. However, a not significant computational delay was considered.

This paper provides a generalized tuning process of the PR controller taking into account the digital control system implementation with a significant delay and several parameters available for tuning. The optimization process is discussed, taking into account previous literature results.

The paper is organized as follows. Section II describes the case study. Section III analyzes and discusses the discretization methods for digital implementation. Section IV demonstrates the influence of the computational delay on the stability of the control system. Sections IV and V are devoted to the enhancing of the stability domain and optimizing of the transient process correspondingly. Finally, experimental results and conclusions are presented and discussed.

## II. PR Controller General Design and Implementation

Fig.1 shows the structure of a system and a case study which includes a grid-connected single-phase full-bridge Three-Level (3L) Neutral Point Clamped (NPC) Voltage Source Inverter (VSI) along with its control system. Single-phase full-bridge 3L NPC VSI gives 5 level of output voltage [28]. In this case, the digital control system is composed by a Field-Programmable Gate Array (FPGA) and a Digital Signal Processing (DSP) controller. Furthermore, external ADC converters are implemented to provide the maximum accuracy. Such complex approach is justified by the transistors' very high switching frequency and the calculation resources high-level demand, resulting in relatively low computational frequency. The functionality is detached between the FPGA and the DSP. Moreover, it gives flexibility in Pulse-Width Modulation (PWM) design. As a result, this approach is often used for power electronics application [29], [30]. Since the power electronic converters' switching frequency is increasing much faster related to the computation frequency, this solution is becoming more common. The main drawback of such approach lies on the significant additional time delay from the closed loop control system. However, even in a simple system based on the DSP, that time delay would be insignificant. Nevertheless, it should be taken into account.

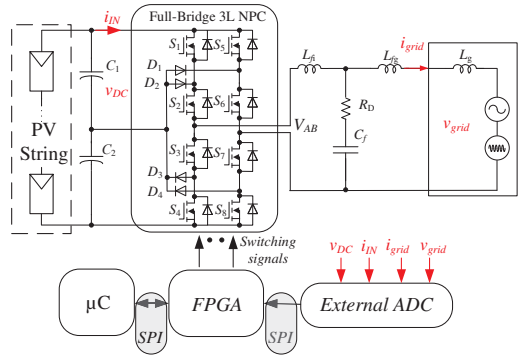


Fig. 1. Case study control system.

Fig. 2 shows the implementation of the digital control system of the PR controller. It has a PLL block, which is one of the traditional Second Order Generalized Integrator (SOGI) regulators. The main purpose of the PLL block is to provide the reference sinusoidal signal that is synchronized with a grid voltage $V_{grid}(t)$.

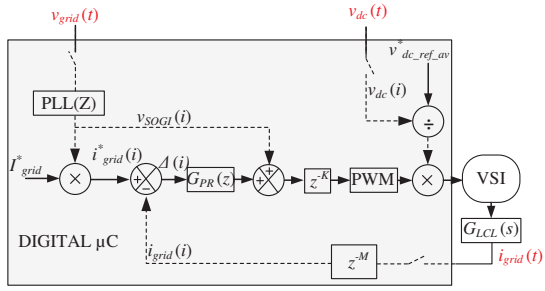


Fig. 2. Digital structure of the control facilities.

The output signal of the PLL block is multiplied by the peak reference grid current $I^*_{grid}$, which is an external value for the PR controller. This signal is then compared with the measured grid current $i_{grid}(t)$. $M$ denotes the measurement sampling delay. In this particular case, two samples are considered. The first sample delay is caused by sending data from ADC to FPGA, and the second is due to the data transmission from FPGA to DSP. $K$ denotes the computational delay, which includes the delay for data exchange between the

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FPGA and DSP and is equal to 3. Therefore, for further analysis, an overall delay $N$ was introduced, which is equal to $N=K+M$.

$G_{PR}(z)$ is the PR controller transfer function in the $z$-domain, being its output a modulation signal for the PWM block. Along with the output transfer function signal, the feed forward sinusoidal signal from the PLL block is added in advance to speed up the transient process.

Fig. 2 presents the digital current control loop and the VSI with the output filter. The behavior of a first-order inductive filter $L$ (1) or third-order filter ($LCL$) (2) can be modeled by their transfer functions (second-order $LC$ filter is just a particular case of $LCL$ filter in which the third inductance is considered to be negligible):

$$G_L(s)=\frac{I_{grid}(s)}{V_{AB}(s)}=\frac{1}{sL_{Fi}+R_{Fi}}, \tag{1}$$

$$\begin{cases}\dfrac{I_i(s)}{V_{AB}(s)-V_D(s)}=\dfrac{1}{sL_{fi}+R_{fi}}=Y^i(s)\\ \dfrac{I_{grid}(s)}{V_D(s)-V_{grid}(s)}=\dfrac{1}{sL_{fg}+R_{fg}}=Y^g(s)\\ \dfrac{V_D(s)}{I_i(s)-I_{grid}(s)}=\dfrac{1}{sC_f}+1=Z^D(s)\end{cases}, \tag{2}$$

According to the desirable feedback current signal ($i_i$ or $i_{grid}$), the corresponding transfer functions $G_{LCL}(s)$ are presented in (3) and (4), respectively.

$$G^i{}_{LCL}(s)=\frac{I_i(s)}{V_{AB}(s)}=\frac{Y^i(s)\left[1+Y^g(s)Z^D(s)\right]}{1+Y^i(s)Z^D(s)+Y^g(s)Z^D(s)}, \tag{3}$$

$$G^g{}_{LCL}(s)=\frac{I_g(s)}{V_{AB}(s)}=\frac{Y^i(s)Y^g(s)Z^D(s)}{1+Y^i(s)Z^D(s)+Y^g(s)Z^D(s)}. \tag{4}$$

To obtain the discrete-time function equivalent to the plant without neglecting computational delays, the $z^{-N}$ block is added through the direct path and the PWM block is replaced by a zero-order hold (ZOH). The ZOH model is a very good approximation in the case of the triangular carrier signal [25]. Thus, the red dotted line in Fig. 3 represents the Bode diagram of $G_{LD}(z)$ and the blue one the diagram of $G_{LCLD}(z)$

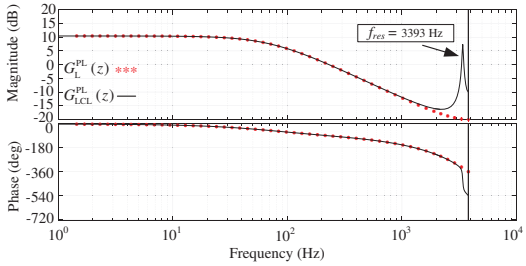


Fig. 3. Bode diagrams of $G_{LD}(z)$ and $G_{LCLD}(z)$, with equivalent parameters at low frequencies ($L_F=L_{Fi}+L_{Fg}$ and $R_F=R_{Fi}+R_{Fg}$). Parameters: $L_{Fi}$ = 0.44 mH, $R_{Fi}$ = 0.2 Ω, $L_{Fg}$= 0.22 mH, $R_{Fg}$ = 0.1 Ω, $C_f$ = 15μF, $R_D$ = 0.8 Ω).

It is important to note that for frequencies below the $LCL$ resonance (3393 Hz in this case), the $LCL$ can be modeled as $L$ filter [27]. Notice that this value must be higher than the chosen resonant controller frequencies according to the application. The digital current control loop scheme presented in Fig. 2 can be simplified by the one in Fig. 4*a*, where $G_{PR}(z)$ represents the controller and $G_{LCL}(z)$ the discretized plant.

There are several types of PR controllers. An ideal PR controller form with an infinite gain at $\omega_h$ is given as:

$$G_{PR}^{id}(s)=K_p+\sum_{h=1,3,5,7}K_{rh}\frac{s}{s^2+\omega_h^2}. \tag{5}$$

This equation (5) is presented in Fig. 4*b*, comprising a fundamental component along with high frequency harmonics compensation. $K_p$ defines the dynamic response in terms of gain, phase margin and bandwidth.

The resonant part of the PR controller can be implemented by two simple integrators as depicted in Fig. 4*c*, for the case of single frequency control at $\omega_0$ [31].

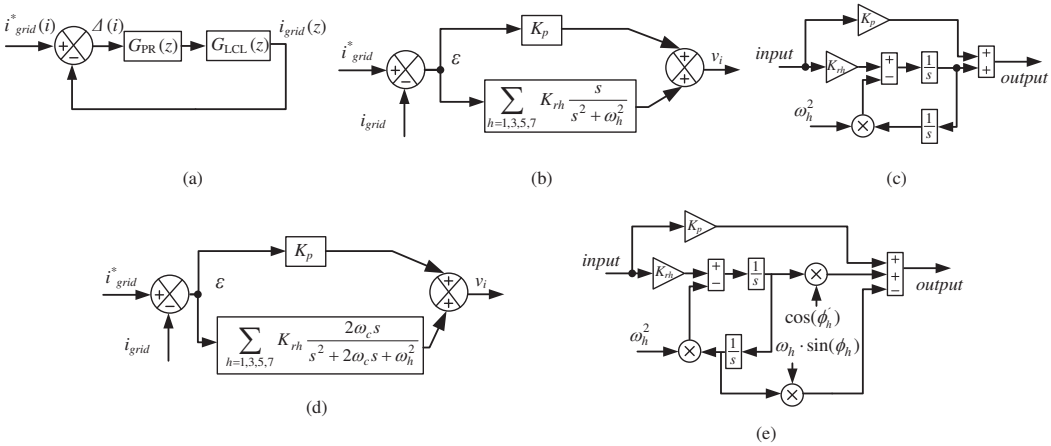


Fig. 4. Bode diagrams of $G_{LD}(z)$ and $G_{LCLD}(z)$, with equivalent parameters at low frequencies ($L_F=L_{Fi}+L_{Fg}$ and $R_F=R_{Fi}+R_{Fg}$). Parameters: $L_{Fi}$ = 0.44 mH, $R_{Fi}$ = 0.2 Ω, $L_{Fg}$= 0.22 mH, $R_{Fg}$ = 0.1 Ω, $C_f$ = 15μF, $R_D$ = 0.8 Ω).

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To avoid stability problems, the real form is commonly used, with a finite gain (however still high) to minimize the steady-state error and widened bandwidth by a proper setting of the cut-off frequency $\omega_C$ [18]-[21]. This feature is helpful in scenarios with grid frequency grid variation as it reduces the sensitivity.

The implementation sketch is shown in Fig. 4*d* and is expressed as follows [30], [31] in (6):

$$G_{PR}^{id}(s) = K_p + \sum_{h=1,3,5,7} K_{rh} \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_h^2} \tag{6}$$

Fig. 5 shows the Bode diagrams of $G^{id}_{PR}(s)$ and $G^{re}_{PR}(s)$ where their particular aforementioned features can be graphically observed.

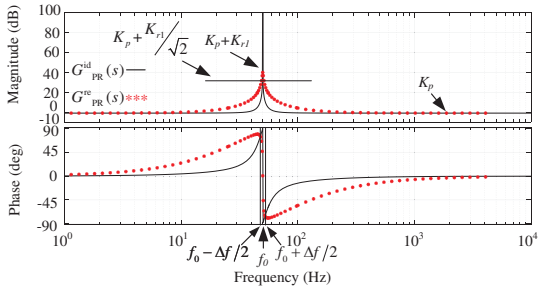


Fig. 5. Bode diagrams of $G_{PR}(s)$ in their ideal and real forms. Parameters: $K_p$ = 5, $K_{r1}$ = $K_{r3}$ = $K_{r5}$ = $K_{r7}$ = 50, $\omega_C$ = 10 rad./sec and $f_0$ = 50 Hz.

According to Fig. 5, the amplitude of the real form of the PR controller is equal to the sum of $K_p$ and $K_r$ at $\omega_h$ frequency [34]. Its bandwidth equals the difference between the two frequencies whose amplitudes equal $K_p+K_r/\sqrt{2}$. This can be described as:

$$G^{re}_{PR}(j\omega) = K_p + K_r/\sqrt{2}. \tag{7}$$

And the bandwidth as:

$$\Delta f = \frac{\omega_C}{2\pi}. \tag{8}$$

Finally, several papers describe the phase compensation approach in order to eliminate the influence of the computational delay [26], [34]:

$$G_{PR}^{id}(s) = K_p + \sum_{h=1,3,5,7} K_{rh} \frac{s\cdot\cos(\phi_h) - \omega_h \cdot \sin(\phi_h)}{s^2 + \omega_h^2}. \tag{9}$$

where the angle is a phase delay for each harmonic is calculated as follows:

$$\phi_h = N \cdot 360^0 \cdot \frac{\omega_h}{2\pi} \cdot \frac{1}{f_s}. \tag{10}$$

It can be seen that additional terms are implemented for each harmonic separately. The implementation scheme is shown in Fig. 4*e*. It is demonstrated that such approach may significantly improve the dynamic performance [26]-[28].

## III. Selection of Function Discretization Methods

A critical step in the practical implementation of a resonant digital controller is the discretization process. Only a few studies have analyzed how the existing discretization techniques affect the performance of a PR controller. Reference [36] presents a deep analysis of different consequences of discretization (pole and zero deviation, effect on delay compensation and in terms of computational burden) on the PR controller. As this study is focused on the ideal form, the conclusions cannot be directly extended to the real one. As examples, in [9] the discretization method based on Tustin with pre-wrapping ($T_{pw}$) was chosen, in [34] the Tustin ($T$) or Bilinear form were considered and in [27] the impulse invariant method (*Imp*) without detailed explanations were used. Among the well-known discretization methods *Imp*, ZOH and $T_{pw}$ are often used for the output current control.

The frequency responses of the real form of the PR controller (with 1st, 3rd, 5th and 7th terms), discretized with such methods, are presented in Fig. 6*a*.

The method based on the $T_{pw}$ approach is the most accurate one since its plot is closer to the continuous model. The introduced phase shift is smaller, which helps with stability issues and allows for a larger phase margin. These effects are related to zero displacement continuous transfer function caused by the discretization method, and they cannot be neglected in frequencies $\omega \approx \omega_h$ where the gain is very high. $T_{pw}$ leads to the maximum stability domain among the compared methods.

Another important criterion to be analyzed is the effect on pole displacement produced by the discretization method. The poles must be placed in the unit circumference since resonant components result in undamped (natural) oscillation responses on the time domain. Fig. 6*b* represents the root-locus of the PR controller, in its real form, discretized by means of $T$ and $T_{pw}$ methods. The poles are located in different positions of the unit circumference.

This situation means that there is a difference between the reference resonant frequency and the real one. For this reason, even the high gain cannot match the frequency of the controller references, causing steady-state errors. The Tustin transformation exhibits 2 Hz deviation in the resonant frequency of the 7th harmonic while the $T_{PW}$ method provides a perfect similarity. This difference can be observed by the highlighted points presented in Fig. 6*b* over the unit circumference.

The same conclusion can be derived from the frequency response (Fig. 6*c*) of the PR controller discretized with the $T$ and $T_{pw}$ methods. The frequency response of the $T_{pw}$ discretization method matches with the tuned frequency of the controller (the 7th harmonic band is represented) and the error with the $T$ method is higher for higher sampling frequencies or resonant frequencies.

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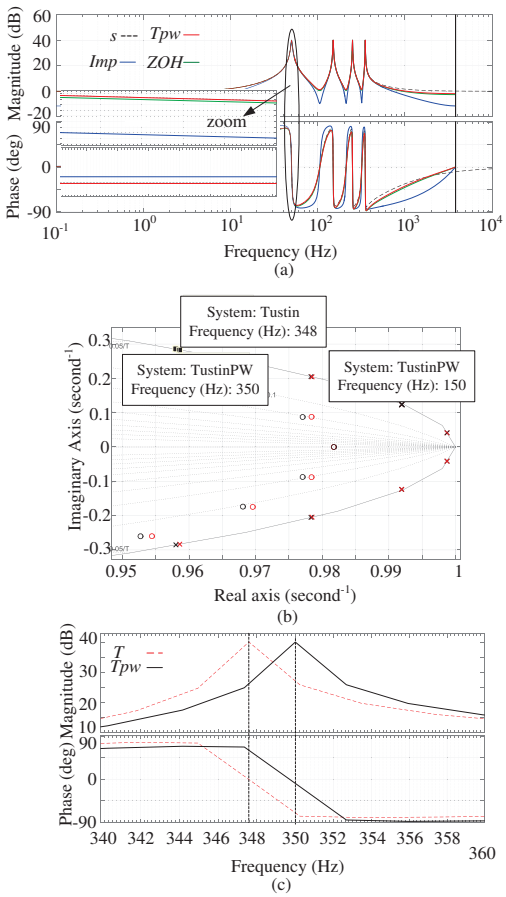


Fig. 6. Bode diagrams of $G_{PR}(s)$ in their real form with different discretization methods ( $K_p$ = 0.9, $K_{r1}$ = $K_{r3}$ = $K_{r5}$ = $K_{r7}$ = 100, $f_h$ = 50 Hz, $T_s$ = 1/7600 sec., and $\omega_C$ = 2 rad./sec) (a), pole locus of the discretized resonant controllers (with 1*st*, 3*rd*, 5*th* and 7*th* terms, $K_p$ = 0.9, $K_{r1}$ = $K_{r3}$ = $K_{r5}$ = $K_{r7}$ = 100, $f_h$ = 50 Hz, $T_s$ = 1/7600 sec., and $\omega_C$ = 2 rad./sec) (b), deviation of the resonance frequency of the discretized controller with the $T$ and $T_{pw}$ method ( $K_p$ = 0.9, $K_{r1}$ = $K_{r3}$ = $K_{r5}$ = $K_{r7}$ = 100, $f_h$ = 50 Hz, $T_s$ = 1/7600 sec., and $\omega_C$ = 2 rad./sec) (c).

From this analysis it is possible to assure that the discrete transfer function obtained by the $T_{pw}$ method is the most optimal among those discussed in applications where high frequencies should be tracked. The reasons are that its zero distribution causes less phase-shift and it presents the most accurate location of the resonant peaks. These features lead to a higher stability domain and reduced steady-state error.

## IV. Influence of the Computational Delay on the Stability Domain and Its Extending

Resulting from the above discussion, the discretization method has a very significant impact and Tustin with pre-wrapping can be considered most suitable for the PR controller. A further step is the study of the influence of the computational delay $N$ on the stability domain of the PR controller.

Fig. 7 shows the Bode diagram of the open loop transfer function which includes the PR controller along with the *LCL*-filter. The parameters of the PR controllers are the same for three cases: $K_p$=0.5, $K_r$=1500,. Only the fundamental harmonic is considered without damping. The *LCL*-filter has the following parameters: $L_{Fi}$ = 0.56 mH, $R_{Fi}$ = 0.2 Ω, $L_{Fg}$= 0.24 mH, $R_{Fg}$ = 0.1 Ω, $R_D$ = 0.7 Ω, $C_f$ = 15 μF. The sampling frequency $f_S$ is 7.6 kHz. It demonstrates the influence of the delay on the stability domain. It can be seen that in the case of delay absence, the system is stable. This corresponds to the blue solid line.

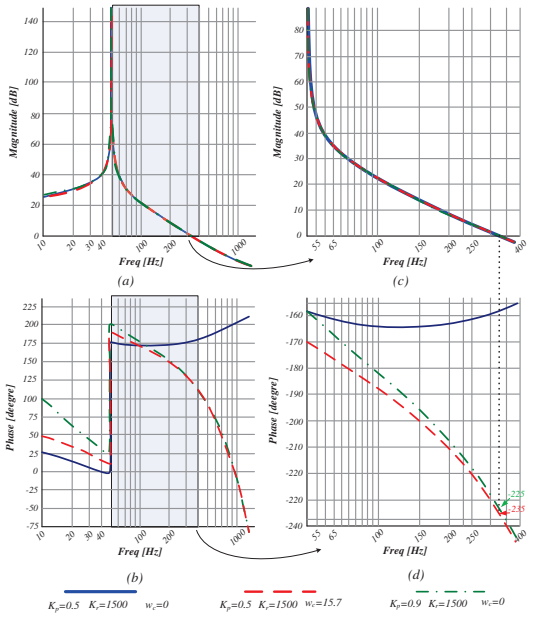


Fig. 7. Influence of the computational delay on the stability region: without delay (blue solid line), with delay and without compensation (red broken line), with delay and with compensation (green dotted line).

The red dotted line corresponds to the same system but with a delay that is equal to five samples. It can be seen that a significant delay leads to a significant phase shifting. The right side Bode diagram (Figs. 7*c* and 7*d*) shows the frequency domain when the magnitude is higher than 1. The red dotted line crosses the -180° phase shift, which in turn leads to the unstable behavior.

According to several studies [35], [36] the phase shifting can be eliminated by introducing additional components (9).

It can be seen that, in comparison with the red broken line, the phase shift in the domain of fundamental harmonic is decreased. At the same time, it is observed that this is not sufficient to keep the system stable. The effect of phase compensation becomes negligible at higher frequencies.

To verify the theoretical study, a comprehensive simulation was performed using the PSCAD® tool. Fig. 8 presents the simulation results. The sampling frequency and the parameters

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of the discretized PR controller along with *LCL*-filter correspond to those in Fig. 7.

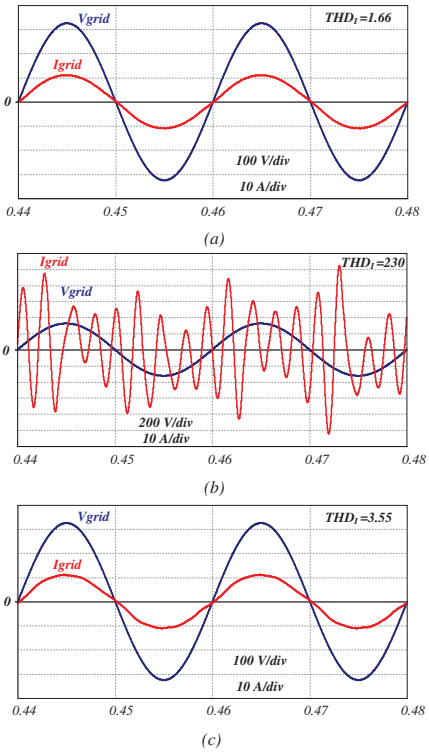


Fig. 8. Simulation results: without delay (a), with delay and with compensation (b), with delay, with compensation, decreased resonance gain and increased proportional gain (c).

The single-phase 3L NPC VSI topology, with an ideal grid, was considered. The dc-link voltage was equal to 380 V. It should be noted that the switching frequency was quite high and equal to 100 kHz.

Fig. 8a shows simulation results in the case of delay absence. The grid voltage and current are stable. The peak value of the grid current corresponds to the reference grid current. The steady state error is absent.

Fig. 8*b* represents the simulation results in the case of delay presence with compensation respectively. It can be seen that the grid current is uncontrollable. It confirms that the computation time delay may lead to stability problems. The phase compensation may help only in the case of non-significant delay. It is obvious that a natural improvement could be achieved just by increasing the sampling frequency, which would result in computational delay decrease. However, this is not always possible and there is a trade-off between the output current quality and the cost of the control system.

A further step is to extend stability by keeping the same parameters of the control system. Fig. 9 shows several root locus diagrams of the system. The main idea of these diagrams is to demonstrate influence of computational delay and other parameters on the system stability. It confirms that system is losing stability with significant delay (Fig. 9*a* and Fig. 9*b*). Increasing of the proportional coefficient and decreasing of the resonance can improve stability domain (Fig. 9*c* and Fig. 9*d*).

Correspondent Bode diagrams of the system are shown in Fig. 10. The first case, with the blue solid line, corresponds to $K_p=0.5$, $K_r=500$ and the phase compensation is obtained according to Eq. (9). The right side Bode diagram (Figs. 10*c* and 10*d*) shows the frequency domain when the magnitude is higher than 1. It can be seen that the system is unstable and the implemented phase compensation it is not enough to avoid phase delay in the full frequency range. The red dotted line corresponds to the same system but with additional damping. The equation in the continuous domain can be expressed as follows [26]:

$$G_{PR}^{id}(s) = K_p + \sum_{h=1,3,5,7} K_{rh} \frac{s\cdot\cos(\phi_h) - \omega_h \cdot \sin(\phi_h)}{s^2 + 2\omega_{ch}s + \omega_h^2}. \quad (11)$$

It can be noticed that it reduces the phase compensation delay in the range of nominal frequencies, but the red dotted line crosses the -180° phase shift while the magnitude is higher than 1, which means that the system remains unstable.

A very interesting phenomenon is observed in the third case (dotted green line). In this case, the proportional coefficient is increased to $K_p=0.9$, which in turn increases the gain but significantly decreases the phase shift of the plant. As a result, a stable behavior is expected.

Fig. 8*c* shows the corresponding simulation results where current in the grid is stable. It should be noted that it is a borderline case and the quality of the current is worth.

It demonstrates that the phase compensation, damping and proportional coefficient increase lead to the elimination of the computational delay effect and extending of the stability domain of the system.

In conclusion, Eq. (11) can be recommended as the most flexible solution. In the case of Tustin with pre-wrapping discretization method, the final equation (12) in the discrete-time domain will be as follows:

$$G_{PR}^{id}(z) = \sum_{h=1,3,5,7} \frac{a_{0h} - a_{1h}\cdot z^{-1} - a_{2h}\cdot z^{-2}}{b_{0h} - b_{1h}\cdot z^{-1} - b_{2h}\cdot z^{-2}},$$
$$K_{Sh} = \frac{\omega_h}{\tan(\omega_h \cdot T_S/2)}, \quad (12)$$

where $T_S$ is the sampling time.

Coefficients are following:

$$a_{0h} = 2K_{rh}(K_S\cos(\phi_h) - \omega_h \sin(\phi_h)),\ a_{1h} = 4K_{rh}\omega_h \sin(\phi_h),$$
$$a_{2h} = 2K_{rh}(K_{Sh}\cos(\phi_h) + \omega_h \sin(\phi_h)),$$
$$b_{0h} = K_{Sh}^2 + \omega_{ch}K_{Sh} + \omega_h^2,\ b_{1h} = 2K_{Sh}^2 - 2\omega_h^2,$$
$$b_{2h} = K_{Sh}^2 - \omega_{ch}K_{Sh} + \omega_h^2. \quad (13)$$

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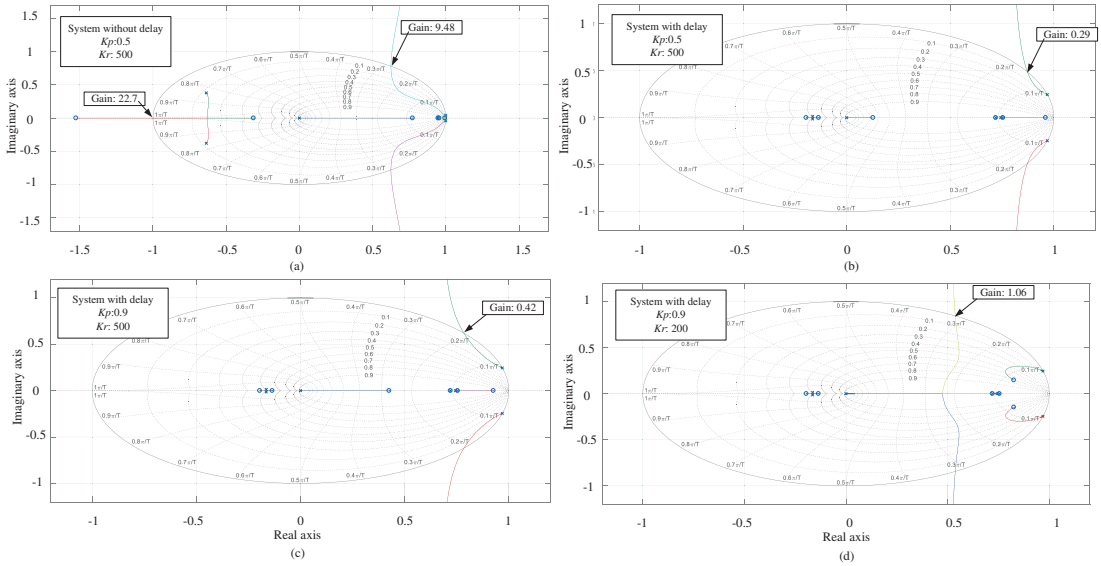


Fig. 9. Root locus diagrams: without delay (a), with delay (b), with delay and increased proportional gain (c), with delay, increased proportional gain and decreased resonant gain (c)

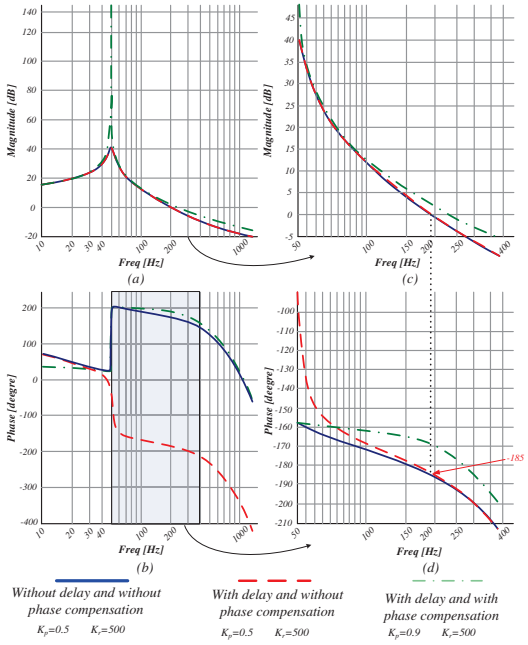


Fig. 10. Influence of the cut-off frequency and proportional coefficient on the stability domain.

The final tuning consists in a trade-off selection between different coefficients that should keep the system stable with a minimum steady-state error.

## V. Startup Current Optimization

In the previous sections, it was shown that under significant computational delay, the coefficients of the PR parameters should be carefully selected. At the same time, it is obvious that keeping a system stable in the steady-state mode leads to the damping and slowing down of the transient response.

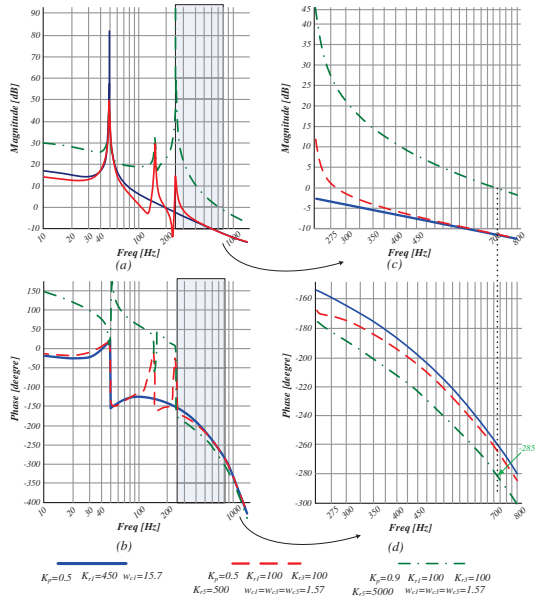


Fig. 11. Bode diagram of the PR+LCL filter with different coefficients.

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Fig. 11 shows three different cases of PR controller parameters. Blue solid line corresponds to the nominal parameters without harmonic compensation. Similar to previous cases, the right side Bode diagram (Figs. 11*c* and 11*d*) shows the frequency domain when the magnitude is higher than 1. The red dotted line corresponds to the nominal parameters with harmonic compensation.

Its additional harmonics influence the phase delay in the high frequency domain and should be selected carefully.

The green dotted line corresponds to the very fast performance of the PR controller with all coefficients increased. It can be seen that the system becomes unstable. Fig. 12 shows the corresponding simulation results where Fig. 12*a* results from the nominal parameters along with harmonic compensation. It can be seen that the system is stable but the current spike is present during the start-up of the PR controller performance.

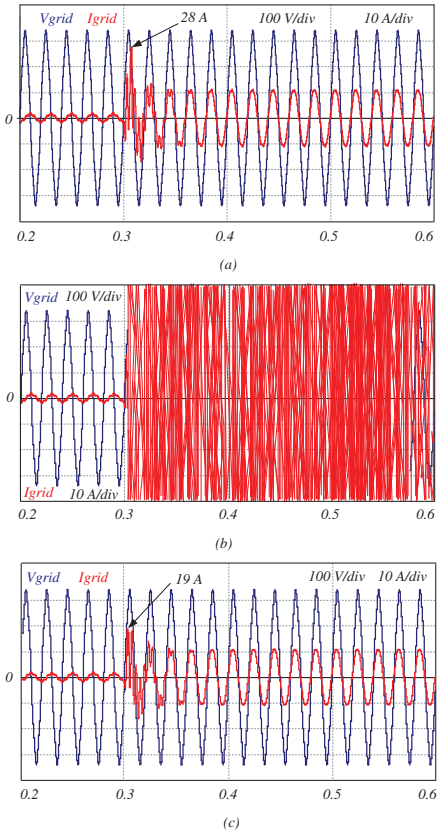


Fig. 12. Simulation results: nominal PR controller parameters (a), increased PR controller parameters (b), increased controller parameters during starting up along with nominal parameters in steady state mode (c).

The core idea is to speed up the regulator during the first transient process. This is achieved by increasing the PR controller parameters only during the first few transient cycles.

The transient process with very fast and constant PR controller parameters is illustrated in Fig. 12*b* where it is evident that the system is unstable. At the same time, Fig. 12*c* demonstrates a transient which has a very high resonant and proportional coefficient during the start-up and nominal parameters during the steady-state mode.

In comparison with Fig. 12*a* it can be seen that such approach provides a current spike decrease from 28 A to 12 A. Such approach can be recommended for start-up current spike decrease which is very suitable for practical applications.

## VI. Experimental Verifications

This section describes the experimental verification in order to validate the theoretical statements. Fig. 13*a* shows the experimental setup. It consists of the 3L NPC VSI and output filters. The values of the passive components are shown in Table I. All the measurements were made by Tektronix MDO4034B-3digital oscilloscope, Tektronix TCP0150 current probes, and Tektronix TPA-BNC voltage probes. Fig. 13*a* also shows a zoomed picture of the control board, specially designed for this application.

The control system consists of two boards based on a combination of a low cost FPGA and DSP with Floating-point Unit (FPU). The bottom side board holds the low cost FPGA from Altera Cyclone IV EP4CE6E22C8, while the upper side board holds the DSP STM32F417ZET. Each of these parts can work independently communicating through Serial Peripheral Interface (SPI). Such combination provides an effective performance of any complex control.

TABLE I
Components and Parameters of 3L NPC VSI used for Experiments

| Parameter | Value |
|---|---|
| Input dc voltage $V_{IN}$ | 380 V |
| Output ac RMS voltage $V_{OUT}$ | 230 V |
| Output power | 1.8 kW |
| Capacitance value of the dc-link capacitors $C_1$, $C_2$ | 2 mF |
| Inverter side inductor filter $L_I$ | 0.56 mH |
| Output side inductor filter $L_g$ | 0.24 mH |
| Capacitor filter $C_f$ | 15 μF |
| Switching frequency $f$ | 100 kHz |
| Control Unit (FPGA) | Cyclone IV EP4CE6E22C8 |
| Control Unit (MC) | STM32F417ZET |
| Transistors Driver Chip | ACPL-H312 |
| Transistors $S_1$... $S_4$ | IPW65R041CFD |
| PR: $K_p$, $K_r$, $K_{r3}$, $K_{r5}$, $K_{r7}$, $K_{r9}$ | 0.9, 100, 100, 100, 10, 10 |
| PR: $w_{c1}$, $w_{c3}$, $w_{c5}$, $w_{c7}$, $w_{c9}$ | 0.0314, 3.14, 3.14, 3.14, 3.14 |

Final experimental waveforms are shown in Fig. 13 as well. In this case, all above theoretical hypotheses have been verified. Safe connection to the grid is mandatory for grid-connected inverters. The converter is connected to the grid, by means of a relay, at the moment of time when the grid voltage is crossing zero. Fig. 13*b* shows this procedure. Very soft charging of the filter capacitor is achieved. After some pause, the transistors and the PR controller are activated and the transient process is launched.

To provide minimum current spike, the parameters of the PR controller during the start-up are selected beyond the stability region: $K_p$=*3.0*, $K_r$=*2000*. This will provide a fast time response of the controller. After start-up, the parameters of the PR controller approach the nominal values reaching them in 5 ms. Full transient is illustrated in Fig. 13*c*.

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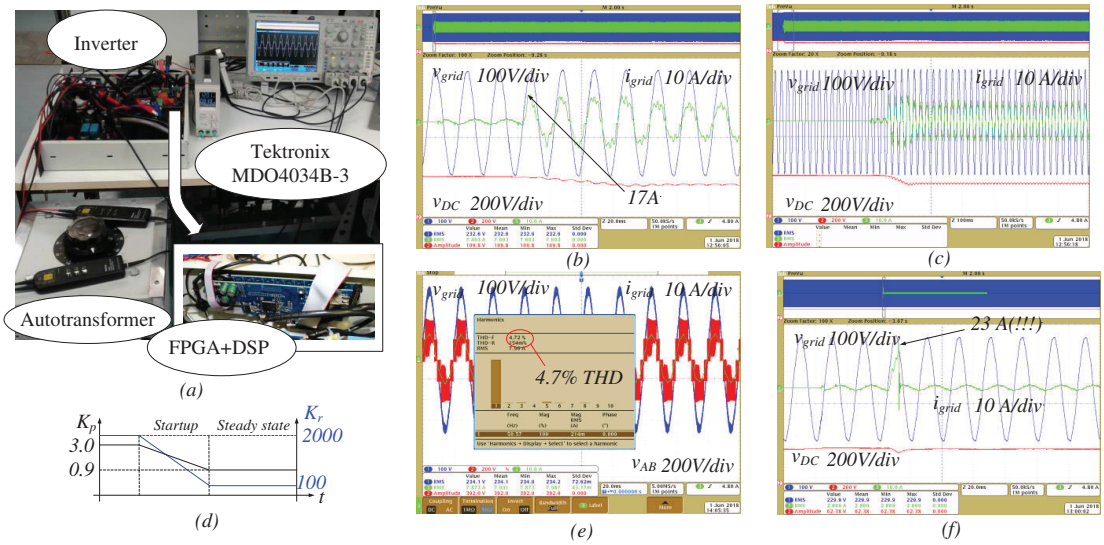


Fig. 13. Experimental verification: experimental setup (a), waveforms: relay connection and adaptive start up process (b), transient process (c), changing of $K_p$ and $K_r$ parameters during startup (d), steady state mode (e) and startup without adaptive approach (f).

Fig. 13*d* schematically illustrates the coefficient changing during startup process. Nominal values of the PR controller were selected as: $K_p$=*0.9*, $K_r$=*100*. It was observed a high quality undistorted grid current waveform is achieved during the steady-state mode. It should be noted that the 3rd, 5th 7th and 9th harmonic compensation were activated. As a result, the grid current quality in the steady-state mode satisfies standards being the THD about 5% (Fig. 13*e*). Parameters of the PR controller in the steady state mode are given in Table I.

At the same time, the case without startup optimization is demonstrated in Fig. 13*f*. It can be seen, that with the same reference peak current (11 A), the peak value of the current during first fundamental cycles reaches value of 23 A. Because of security reason the control system blocks further operation. Similar diagrams can be derived in case of unstable operation.

## VII. Conclusions

This paper described in detail the implementation and the tuning process of the PR controller for grid connected inverters. The optimal coefficients that provide a minimum steady state error and also keep the converter stable were found. Computational time delay resulting from digital control system leads to a significant phase delay in the frequency domain, which makes it difficult to control high order frequency harmonics in particular. It was demonstrated that phase-compensation is not enough and a damping approach is required. It is evident that sampling frequency increase and computational delay decrease lead to the improved quality of the control but this is not always possible. Finally, the trade-off tuning approach that keeps valid initial control system parameters is proposed.

The following guidelines can be underlined:

1. The discretization method based on Tustin with pre-wrapping is the optimal.
2. Phase compensation approach is not sufficient in order to keep the system stable in the case of significant computational delay.
3. Increase in the proportional coefficient along with a decrease in the resonance coefficient lead to the extension of the stability domain and increase in the steady-state error.
4. Implementation of the damping cut-off frequency leads to the extension of the stability domain but the steady-state error increases.
5. The adaptive approach that consists in the resonance coefficients increase during the step response is proposed in order to decrease the steady-state error and avoid overcurrent during start-up interval.

All the results have been verified by simulation and experimental analysis. By that, the presented proposal can be used for tuning the PR controllers applied to grid-connected inverters.

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