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Post Regulation Low Drop Out (LDO) Regulator

Master's thesis

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Author’s declaration

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IED40LT

Eelreguleeritud madala pingelanguga pingeregulaator

Magistri lõputöö

Annotatsioon

Antud töö keskendub eelreguleeritud madala pingelanguga pingeregulaatori väiksema võimaliku sisendpinge leidmisele, säilitades seejuures mõistlikult väikest pingelangu väljundtransistoril. Regulaatorit uuritakse erinevate konfiguratsioonidega, valides välja sealt parima. Vastavalt simulatsioonidele muudetakse regulaatori skeemi. Leitakse regulaatori peamised parameetrid ning disainitakse kiibi pinnalaotus.

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Post regulation Low Dropout Regulator (LDO)

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Annotation

This work is focused on finding how low can go with post regulation LDO input voltage and same time maintaining reasonable dropout voltage. LDO is examined with different configurations and then selecting best one. According to simulations the circuit is improved. LDO main parameters are found and layout designed.

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INTRODUCTION

Post regulation low-dropout(LDO) regulator is linear voltage regulator. Post regulation means that LDOs input voltage is regulated before by another regulator which regulation from higher voltage to lower is more efficient than LDOs.

Power management has increasing role in the present electronic industry[2]. The explosive proliferation of battery-operated equipment such as cellular phones, notebook computers in the past decade have accelerated the development and usage of LDOs with better regulating performance, higher efficiency and lower voltages. Many modern electronic devices have multiple internal voltages and sources of external power. Common voltages for electronics are 5 V, 3.3 V, 1.8 V, etc. Advanced handheld and battery powered applications require the power management techniques to extend the battery life and consequently the operating life of the device.

In recent years the trend is towards lower supply voltages. This is partially due to the processes used to manufacture integrated circuits. Circuit speeds have increased. One of the enabling technologies of this increase is the reduction of size of the transistors used in the process. These smaller feature sizes imply lower breakdown voltages, which, in turn, indicate lower supply voltages. LDO voltage regulators play a very important role in the modern power management units because LDO regulator can provide a good regulation and a fast transient response while providing clean and ripple-free output voltage. Compared with the switching regulators, linear regulators are less noisy, less complex, and cheaper.

In this paper, is studied how low we can go with LDO input voltage to maintain reasonable dropout voltage. Technology in simulation circuits is used National's CMOS7-5V process technology. In focus is to examine different LDO configurations where is used PMOS and NMOS transistors as pass elements and error amplifier with NMOS and PMOS input transistors. Target is to supply 100 mA current from LDO and dropout voltage under 200 mV. Best theoretically found solution circuit is designed in cadence and afterward different simulations are simulated. On the basis of simulations, the circuit design is improved. Specification for LDO are taken from simulations. If circuit design and simulations are given satisfied results then layout of LDO is made in cadence.

1. DC VOLTAGE REGULTORS

Every electronic circuit is designed to operate off of some supply voltage, which is usually assumed to be constant [1]. A voltage regulator provides this constant DC output voltage and contains circuitry that continuously holds the output voltage at the design value regardless of changes in load current or input voltage (this assumes that the load current and input voltage are within the specified operating range for the part).

Several methods exist to achieve DC-DC voltage conversion. Each of these methods has its specific benefits and disadvantages, depending on a number of operating conditions and specifications. Examples of such specifications are the voltage conversion ratio range, the maximal output power, power conversion efficiency, number of components, power density, galvanic separation of in- and output, etc. When designing fully-integrated DC-DC converters these specifications generally remain relevant, nevertheless some of them will gain weight, as more restrictions emerge. For instance the used IC technology, the IC technology options and the available chip area will be dominant for the production cost, limiting the value and quality factor of the passive components. These limited values will in-turn have a significant impact upon the choice of the conversion method.

1.1 Linear voltage regulator

The most elementary DC-DC converters are linear voltage regulator [2]. They achieve DC-DC voltage regulation by dissipating the excess power into a variable resistor, making them resistive dividers. Modern designs use one or more transistors which operate in their linear region. Clearly, this is not quite ideal for the power conversion efficiency, which formula is:

$$\eta_{lin} = \frac{P_{out}}{P_{in}}, \tag{1.1}$$

Another implication of their operating principle is the fact that they can only regulate a certain input voltage V_{in} into a lower output voltage V_{out}, having the same polarity. In other words, the value of their voltage conversion ratio is:

$$k_{lin} = \frac{V_{out}}{V_{in}}, \tag{1.2}$$

It is always between zero and one. If the input voltage approaches the desired output voltage, the regulator will "drop out". The input to output voltage differential at which this occurs is known as the regulator's drop-out voltage.

Linear designs have the advantage of very "clean" output with little noise introduced into their DC output, but are most often much less efficient and unable to step-up or invert the input voltage like switched supplies. The another advantage of linear voltage converters is that they are fairly simple to implement. Moreover, they generally do not need large, and space consuming, inductors or capacitors, making them an attractive option for monolithic integration. Two types of linear voltage regulators, namely the series and the shunt regulator, are discussed in sections 1.1.1 and 1.1.2.

1.1.1 Series pass voltage regulator

The operating principle of a linear series voltage regulator is shown in figure 1.1. A variable resistor R_{series} is placed in series with the load R_{load}, lowering V_{in} to V_{out}. The resistance of

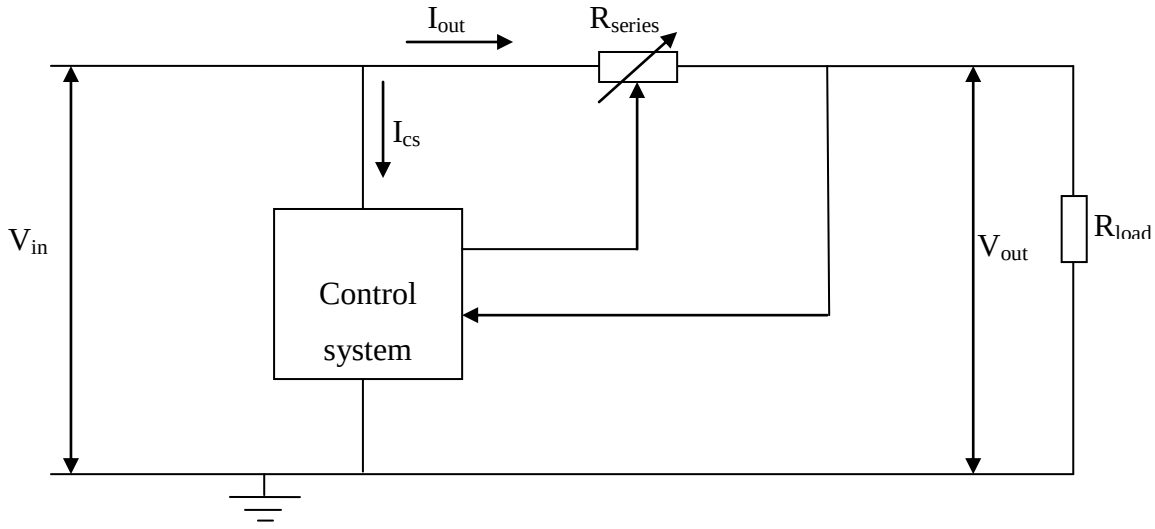

Fig. 1.1 The principle of a linear series voltage regulator

R_{series} is controlled by the control system, which keeps V_{out} constant under varying values of by its supply current I_{cs}. In this case the control system uses V_{in} as supply voltage, which can also be provided by V_{out}.

A practical implementation example for a linear series voltage regulator is shown in figure 1.2. In this example R_{series} is implemented as an transistor M and the control system as

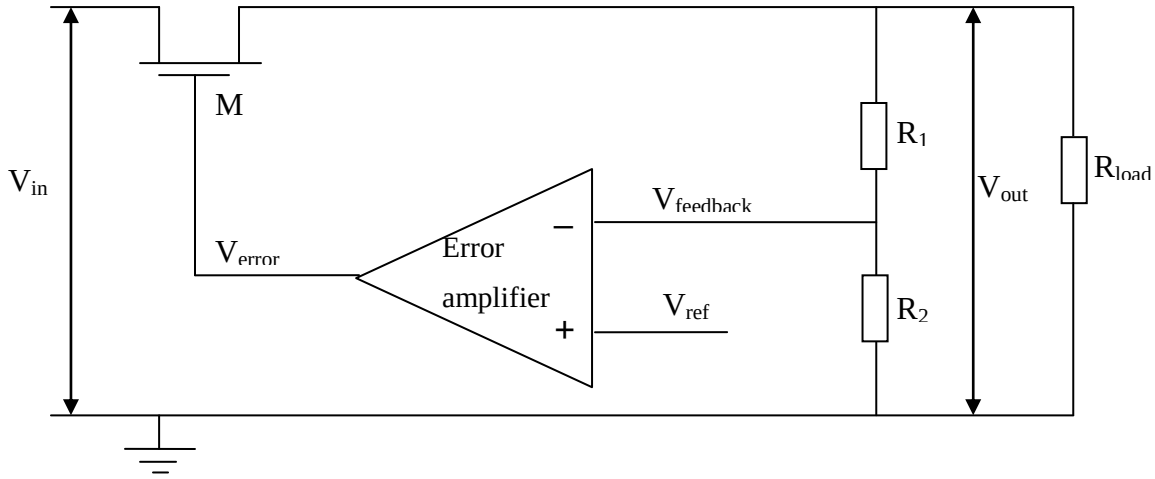

Fig. 1.2 A simple practical series pass regulator implementation

an operational amplifier, which performs the task of an error amplifier. Control of the series pass transistor M is accomplished by the negative feedback loop consisting of the resistor sampling network and the error amplifier. The sampled output voltage equation is:

$$V_{feedback} = V_{out}\left(\frac{R_2}{R_1 + R_2}\right), \tag{1.3}$$

This is compared with the constant reference voltage V_{ref}. An error is generated by the error amplifier that is proportional to the difference between the sampled output voltage and V_{ref}. This error voltage drives the series pass transistor. A small increase in output voltage causes an increase in the series pass element impedance to maintain a constant output voltage. Likewise, a small decrease in output voltage will cause the impedance of the series pass transistor to decrease. The negative feedback loop always maintains the sampled output

voltage very nearly equal to V_{ref} :

$$V_{feedback} \approx V_{ref}\,, \tag{1.4}$$

By doing so, V_{out} is determined by

$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right), \tag{1.5}$$

By examining the operating principle of figure 1.2, η_{lin} can be calculated through equation (1.7).

$$I_{in} = I_{out} + I_{cs}\,, \tag{1.6}$$

$$\eta_{lin} = \frac{P_{out}}{P_{in}} = \frac{V_{out} \bullet I_{out}}{V_{in} \bullet I_{in}} = \frac{V_{out} \bullet I_{out}}{V_{in} \bullet (I_{out} + I_{cs})}\bigg|_{I_{cs}=0} = \frac{V_{out}}{V_{in}} = k_{lin}\,, \tag{1.7}$$

When I_{cs} is neglected and assumed to be zero, η_{lin} is equal to k_{lin} and thus independent of R_{load}. This is graphically illustrated by the black curve in figure 1.3(a) [3]. The gray curve illustrates the more realistic situation, where I_{cs} has a finite positive value. It can be seen that η_{lin} will tend to decrease when P_{out} decreases. Clearly, linear series voltage converters have an intrinsic advantage, in terms of power conversion efficiency, at high voltage conversion ratios. This is illustrated by figure 1.3(b) [3], where the black curve is valid for I_{cs} = 0 and the gray curve for a finite, non-zero I_{cs}. The gray curve shows that the impact of the power consumption of the control system on η_{lin} becomes more dominant when k_{lin} approaches unity.

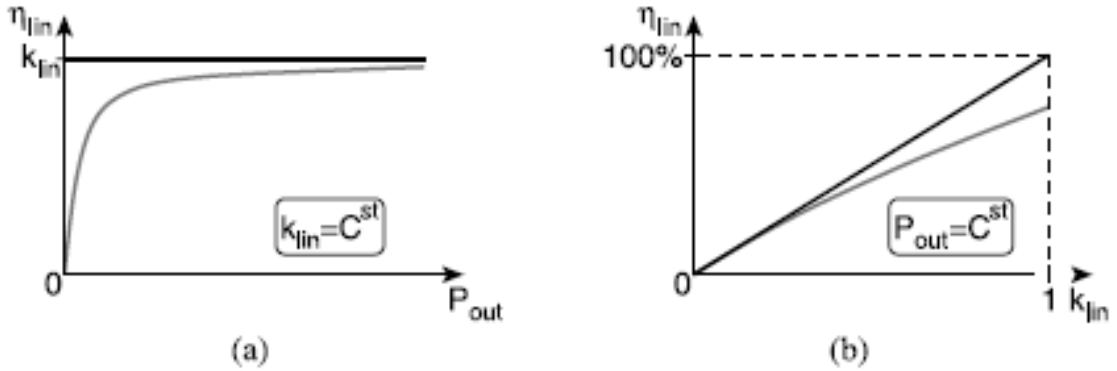

Fig. 1.3 (a) The power conversion efficiency η_{lin} as a function of the output power P_{out} for a linear series voltage converter, at a constant voltage conversion ratio k_{lin}. The black curve is valid for a zero control system supply current I_{cs} and the gray curve is valid for a non-zero I_{cs}. **(b)** The power conversion efficiency η_{lin} as a function of the voltage conversion ratio k_{lin} for a linear series voltage converter, at a constant output power P_{out}. The black curve is valid for a zero control system supply current I_{cs} and the gray curve is valid for a non-zero I_{cs}

1.1.2 Shunt voltage regulator

The alternative for a linear series voltage converter is a linear shunt voltage converter [2]. The principle of operation for this type of DC-DC converter is shown in figure 1.4. V_{in} is

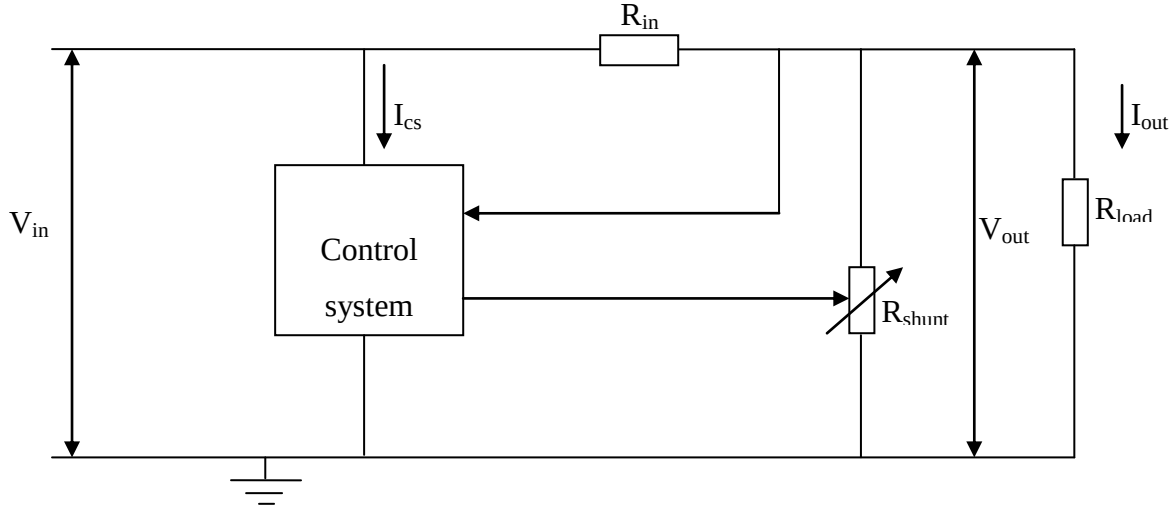

Fig. 1.4 The principle of a shunt voltage regulator

lowered to V_{out} by means of the resistive division between the fixed input resistor R_{in} and both

the load R_{load} and the variable shunt resistor R_{shunt}, where V_{out} is calculated by:

$$V_{out} = V_{in} \frac{R_{load} // R_{shunt}}{R_{in} + R_{load} // R_{shunt}}, \tag{1.8}$$

R_{in} can either be the intrinsic output resistance of V_{in}, an added resistor or the combination of both. V_{out} is kept constant under varying R_{load} and V_{in} conditions by adapting the value of R_{shunt}. This operation can be performed by a control system, providing feedback from V_{out}. The control system consumes a certain amount of power by drawing a current I_{cs} from V_{in} or V_{out}. Feedback of V_{out} is however not always required. The shunt resistor could be replaced by a reverse-biased zener diode. In this way a quasi constant V_{out} can be achieved, if the current through zener diode is kept large enough for it to operate in the zener-region.

A practical implementation example for a linear series voltage regulator is shown in figure 1.5. In this example R_{shunt} is implemented as an transistor M and the control system as an operational amplifier, which performs the task of an error amplifier. Control of the transistor is accomplished same way as it was in section 1.1.1.

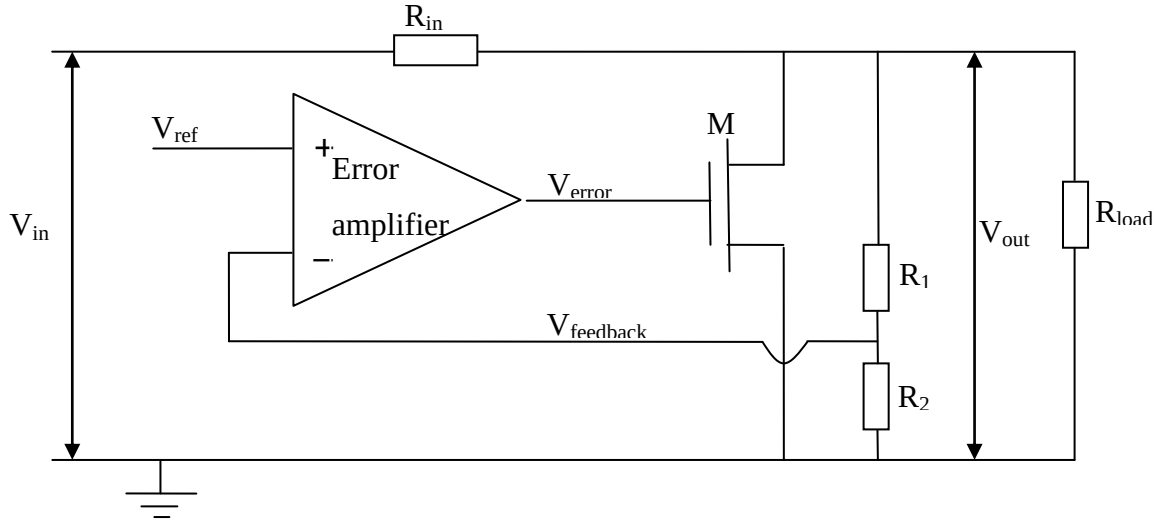

Fig. 1.5 A simple practical shunt regulator implementation

For a shunt converter η_{lin} is calculated by

$$\eta_{lin} = \frac{P_{out}}{P_{in}} = \frac{\frac{V_{out}^2}{R_{load}}}{\frac{V_{in}^2}{R_{in} + R_{load}//R_{shunt}} + V_{in} \bullet I_{cs}}, \tag{1.9}$$

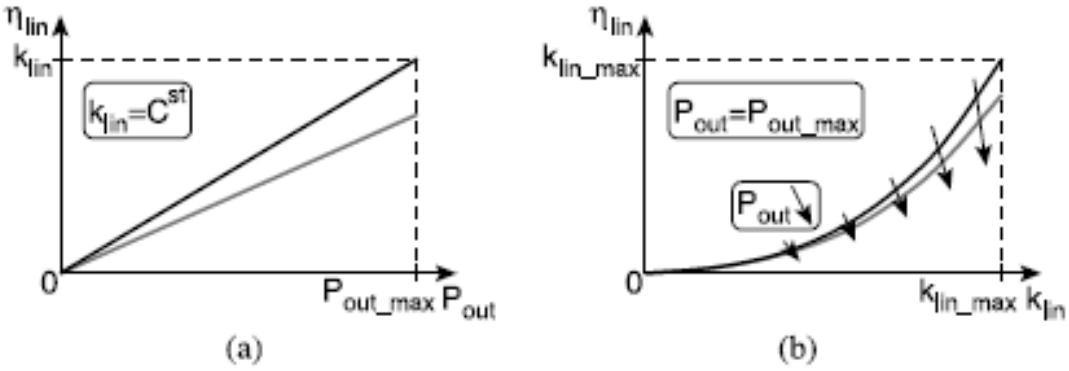

Fig. 1.6 (a) The power conversion efficiency η_{lin} as a function of the output power P_{out} for a linear shunt voltage converter, at a constant voltage conversion ratio k_{lin}. The black curve is valid for a zero control system supply current I_{cs} and the gray curve is valid for a non-zero I_{cs}. **(b)** The power conversion efficiency η_{lin} as a function of the voltage conversion ratio *klin* for a linear shunt voltage converter, for a constant value of $P_{out} = P_{out\_max}$. The black curve is valid for a zero control system supply current I_{cs} and the gray curve is valid for a non-zero I_{cs}

Figure 1.6(a) [3] graphically illustrates η_{lin} as a function of the output power P_{out}, for a constant voltage conversion ratio k_{lin}. The black curve is valid for the ideal case where I_{cs} is zero and the gray curve is valid for a finite non-zero I_{cs}. As opposed to a linear series converter, η_{lin} is intrinsically linear dependent on P_{out}. It can be seen that η_{lin} is zero for $P_{out} = 0$ and that it has a maximal value equal to k_{lin}, occurring at the maximal output power P_{out_max} which is given by (1.10). For a given V_{in} and V_{out}, P_{out_max} is determined by the inverse of the value of R_{in}.

$$P_{out\_max} = \frac{V_{out}(V_{in} - V_{out})}{R_{in}}, \tag{1.10}$$

The dependency of η_{lin} on k_{lin} is illustrated in figure 1.6(b) [3], for a constant $P_{out} = P_{out\_max}$. The black curve is valid when I_{cs} is zero and the gray curve is valid for a finite, non-zero value of I_{cs}. As explained for figure 1.6(a), η_{lin} is maximal for P_{out_max}. Therefore, the

curves will become lower upon decreasing P_{out}, eventually congregating with the X-axis. The maximal achievable voltage conversion ratio k_{lin_max} is calculated by (1.11) and is for a given U_{out} inversely proportional to P_{out} and R_{in}.

$$k_{lin\_max} = \frac{V_{out}^2}{V_{out}^2 + P_{out\_max} \bullet R_{in}}, \tag{1.11}$$

Unlike a linear series converter, where η_{lin} is ideally independent of P_{out}, a linear shunt converter only achieves its maximal η_{lin} at P_{out_max}. This behavior makes a linear shunt converter inferior compared to a series converter, in terms of η_{lin}. However, its simple practical implementation makes it suitable for applications that require a small and quasi constant P_{out}. Furthermore, a linear shunt converter can prove to be more practical than a linear series converter in applications that have a low value for k_{lin} and P_{out}. In such a case the voltage difference $V_{in} - V_{out}$ will only be present over the passive resistor R_{in} rather than over an active device, of which the maximal voltage is limited. The simple nature of a linear shunt voltage converter, and its lack of large passives, makes it suitable for monolithic integration in non-critical applications. Obviously, the problem of on-chip power dissipation remains and becomes more limiting than for linear series voltage converters.

1.2 Switching voltage regulator

Switching regulators are used where large input-to-output differential voltages may exist, or where high load current requirements are necessary [2]. Their use is particularly suited for high power applications and systems where efficiency is important.

Switching regulators rapidly switch a series device on and off. The duty cycle of the switch sets how much charge is transferred to the load. This is controlled by a similar feedback mechanism as in a linear regulator. Because the series element is either fully conducting, or switched off, it dissipates almost no power; this is what gives the switching design its efficiency. Switching regulators are also able to generate output voltages which are higher than the input, or of opposite polarity — something not possible with a linear design. Unlike linear regulators, these usually require external components: an inductor or capacitor that acts as the energy storage element. Two basic switching regulators are shown in figure 1.7 [6] and discussed in sections 1.2.1 and 1.2.2.

Fig 1.7 Two basic switching voltage regulators

1.2.1 Step-down switching voltage regulator

The switching operation of a basic step-down converter is shown in figure 1.7. A low impedance transistor is opened and closed periodically between the input and the output. The voltage drop of the transistor when it is in the saturated "on" state (normally closed) is V_{sat}. Then the out will periodically vary between zero volts and almost the input voltage, with the average value of this being by equation:

$$V_{out} = (V_{in} - V_{sat}) \bullet \frac{T_{on}}{T}, \tag{1.12}$$

where T_{on} is the time that the transistor switch is "on" and T is the switching period. The ripple voltage still has a peak-to-peak value of nearly less than *Vin*. However, adding the *LC* (Fig 1.8) filter reduces the ripple to an acceptable level.

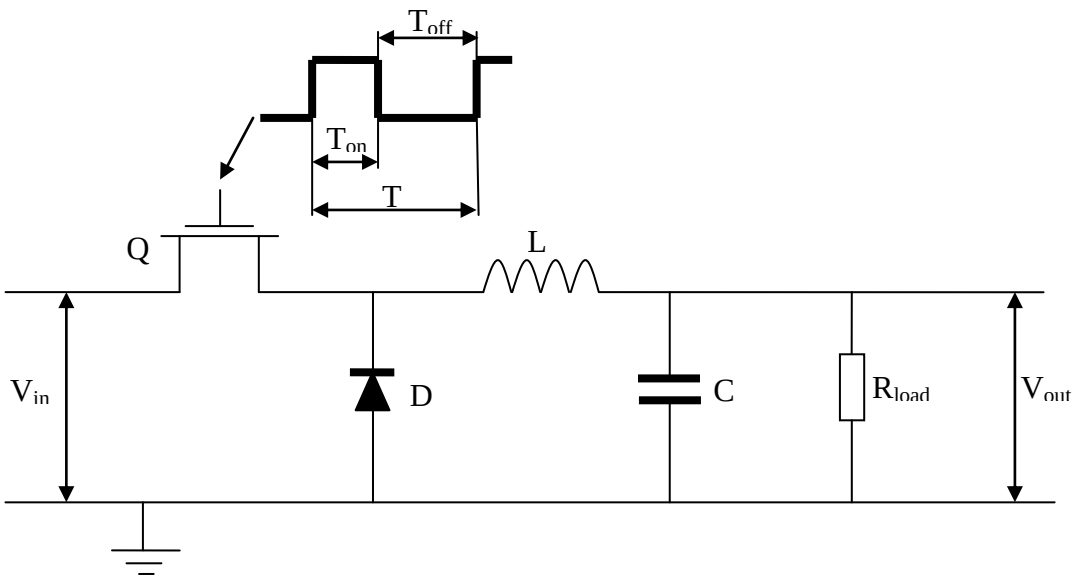

Fig. 1.8 Simple step-down switching converter

The switching duty cycle, defined as T_{on}/T, means that by varying the duty cycle any output voltage lower than the input can be obtained. Efficiency is high, since the only losses in the converter occur in the switching transistor when it is “on”. These losses are insignificant because the voltage drop across the transistor when it is "on" is low. There is no power dissipation when the transistor is "off" because no current flows through it.

When the transistor switch turns "off”, the input side of *L* goes negative because current cannot change instantaneously through an inductor. Diode *D* starts conducting when its cathode potential becomes sufficiently negative to cause the diode to become forward biased. When the transistor is “off”, load current is supplied by both *L* and *Q* in parallel. If *L* is made large enough, then the current in *L* will change very little from the transistor "on" to "off" time and will be equal to the DC output current V_{out}/R_{load}. When the transistor turns “on" again, diode *D* is reverse biased and stops conducting. Load current is then supplied by the source through the transistor.

The converter of figure 1.8 can be transformed into a switching voltage regulator by adding an output voltage sampling resistor network, a error amplifier, a stable voltage reference, and a DC voltage controlled pulse-width modulator.

The negative feedback circuit changes the pulse width or duty cycle to maintain a constant output. Changes in the load or input voltage are compensated by varying the duty cycle of the transistor switch without increasing the interval power dissipated in the switching regulator.

The higher switching frequencies result in smaller filter inductors and capacitors which in turn reduces the size and weight of the regulator for the same power output. Higher frequencies also result in larger switching losses and hence lower efficiencies.

1.2.2 Step-up switching voltage regulator

Unlike the step-down switching regulator which can only produce a voltage less than the input voltage, the step-up switching regulator is capable of producing a higher voltage than the input. It can be used wherever a higher voltage than the existing source is required. There is no DC isolation, however, from the negative terminal of the source .

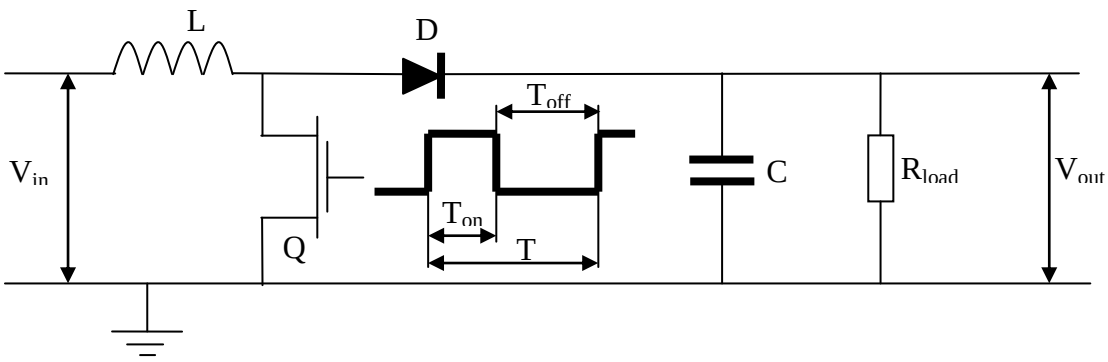

Fig. 1.9 Simple step-up switching converter

The operating principle of a switching voltage regulator with high conversion efficiency can be understood by analyzing the basic configuration of the step-up switching regulator shown in figure 1.9. [4] The duty cycle of the switching transistor *Q* is controlled by the switching frequency of the control circuit. *Q* alternates between on and off states during operation. To obtain a stable output voltage in a series regulator, the pass transistor, which is the control element of a series regulator, operates continuously. In a switching regulator, the switching transistor alternates between on and off states. Because this transistor always is saturated in the on state and is completely off at other times, the voltage loss associated with the switching transistor is very small compared to the voltage loss attributed to the pass

transistor of the series regulator. The output voltage can be stepped up to:

$$V_{out} = V_{in}\left(1 + \frac{T_{on}}{T_{off}}\right), \tag{1.13}$$

When *Q* is turned on at the beginning of the charge cycle, the voltage of $V_{in} - V_{sat}$ is developed across both ends of inductor *L*, as the inductor current increases linearly. At the end of the charge cycle, the current through the inductor is at its peak value. Peak current is expressed as

$$I_{peak} = \frac{V_{in} - V_s}{L} \bullet t_{on}\,, \tag{1.14}$$

At the end of the charge cycle, the switching transistor *Q* is turned off, and the regulator goes into discharge mode. The diode *D* acts as a flywheel diode and provides a current path from the inductor *L* to the output. The inductor current is reduced linearly as it is discharged. The ratio of the charge/discharge time is proportional to the input-to-output voltage difference divided by the input voltage.

$$\frac{t_{charge}}{t_{discharge}} = \frac{\Delta V}{V_{in}}, \tag{1.15}$$

Where ΔV is:

$$\Delta V = V_{out} - V_{in}\,, \tag{1.16}$$

As the voltage difference increases, the discharge time decreases and becomes smaller than the charge time.

$$t_{discharge} = \frac{I_{peak}}{V_{out} - V_{in}} \bullet L\,, \tag{1.17}$$

1.3 Comparison

For the majority of applications within portable devices where loads are operated from a battery source, the linear regulator offers a simple, small and cost-effective solution. While it is true that switching regulators are more efficient than linear regulators. Switching regulators produce electromagnetic interference (EMI) that can disrupt both analog and RF circuits. In contrast, the switching in linear regulators occurs in the bandgap reference and the level is in the microvolt, RMS range over a defined bandwidth, a level that is considerably lower than a switching regulator. This is a major design advantage in noise-sensitive applications. Additional advantages of fewer external components, simple design process, and lower cost make linear regulators a preferred solution for regulated power in many applications where the controlled voltage is lower than the source voltage. Linear regulators are best when is required low output noise, a fast response to input and output disturbance. At low levels of power, linear regulators are cheaper and occupy less chip area. While switching regulators garner a lot of attention because of their high efficiency, linear voltage regulators offer the optimum answer for powering circuitry in many of the portable device applications. Table 1.1 summarizes the significant points of comparison between linear and switching regulators.

Table 1.1 Comparison between linear and switching regulators

Regulator type	Linear	Switching
Function	Only steps down	Steps up, steps down or inverts
Efficiency	Low to medium	High
External Components	No	Yes
Ripple/noise	Low	Medium to high
Design Complexity	Low	Medium to high
Total cost	Low	Medium to high
Waste heat	High	Low
Size	Small to medium	Medium to high

2. POST REGULATION LDO

Post regulation LDO means that LDO is as a post regulator to reduce switching regulator output noise (Fig 2.1) [11]. The output of the switching voltage regulator may not be suitable for many noise sensitive applications because of its inherent switching noise. This is particularly true when the switching regulator is operating in PSM (pulse skip modulation) mode because the switching noise is in the audio range. The LDO regulator can greatly reduce

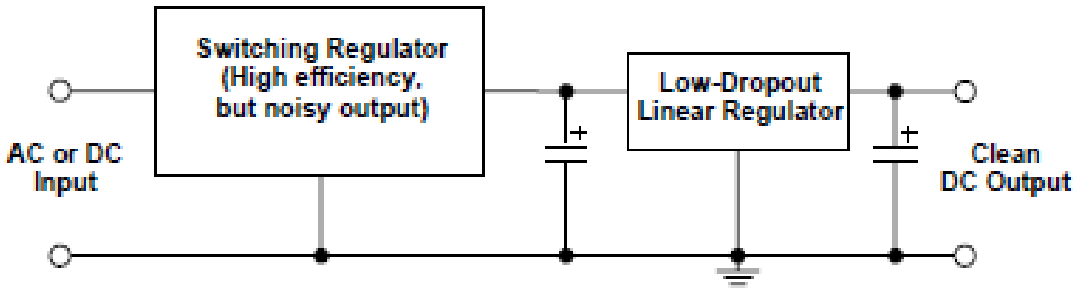

Fig. 2.1 Post regulation principle

the noise at the output of the switching regulator at high efficiency because of the load dropout voltage of the LDO regulator and the high PSRR (power supply rejection ratio) of the LDO regulator. Figure 2.2 show the noise reduction that is possible when the LDO is used as a post regulator.

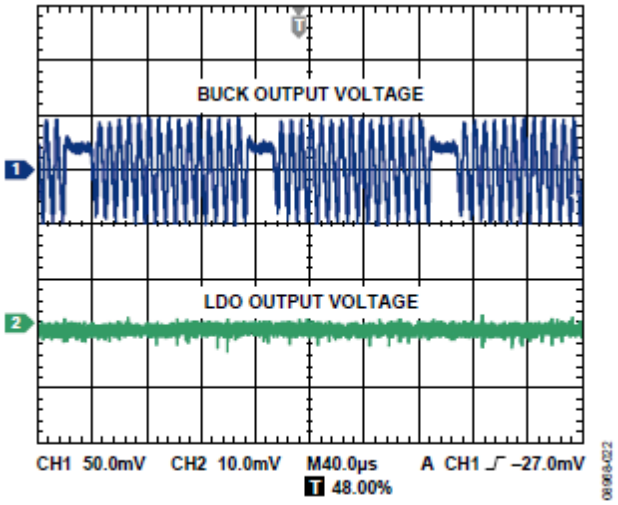

Fig. 2.2 LDO reduce buck regulator output noise

2.1 LDO basics

A LDO regulator is a DC linear voltage regulator which provides a well-specified and stable DC voltage whose input and output voltage difference V_{do} is low. The drop-out voltage is defined as the value of input/output differential voltage where the control loop stops regulating. The regulator circuit can be partitioned into four functional blocks: the reference, the pass element, the sampling resistors, and the error amplifier as shown in figure 2.3. Pass element is connected in series between input and output terminal of the regulator. The operation is based on feeding back an amplifier error signal to control the output current flow

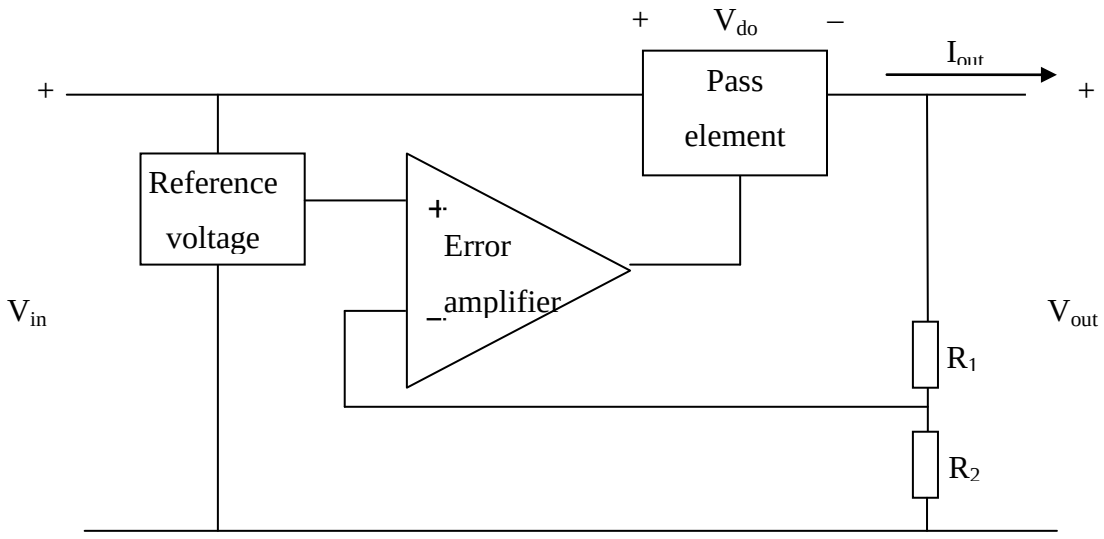

Fig. 2.3 Simple LDO block diagram

I_{out} of the pass element driving the load. Output voltage V_{out} is fixed with sampling resistors and reference voltage V_{ref}.

$$V_{out} = V_{ref}\left(\frac{R_1 + R_2}{R_2}\right), \tag{2.1}$$

2.2 Pass element

The pass element can be either an N-type (NMOS) or a P-type (PMOS) device. The MOSFET is a voltage driven device. In the linear region, the series pass element acts like a series resistor. In the saturation region, the device becomes a voltage-controlled current source. Voltage regulators usually operate in the saturation region because then is the channel resistance smallest and therefore power dissipation not wasted on transistor. N-type devices require a positive drive signal with respect to the output, while P-type devices are driven from a negative signal with respect to the input.

Figure 2.4 [8] shows how we define the voltages, currents, and terminal designations for a MOSFET. It is important to keep in mind that the MOSFET is a four-terminal device and that the source and drain of the MOSFET are interchangeable. Note that all voltages and currents are positive using the naming convention seen in the figure 2.5. For the PMOS device equations are same only must change order of suffix names. The devices are complementary.

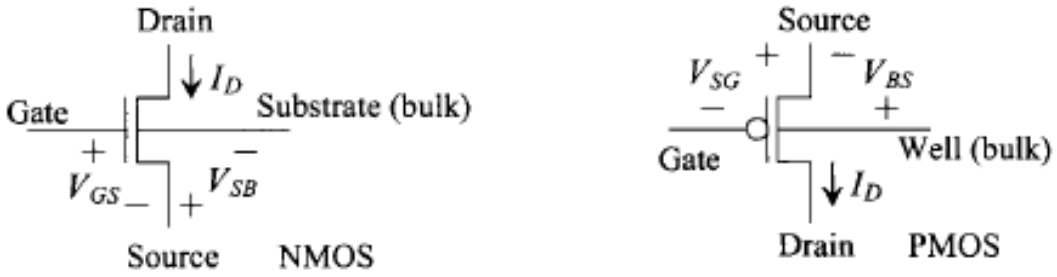

Fig. 2.4 MOSFET types

NMOS transistor majority carriers are electrons (greater mobility μ_n), p-substrate doped (positively doped) and PMOS transistor majority carriers are holes (less mobility μ_p), n-substrate (negatively doped).

Semiconductor/oxide surface is inverted when V_{GS} is greater than the threshold voltage V_{THN}. Under these conditions a channel of electrons is formed under the gate oxide (Fig 2.5) [8]. Below this channel, electrons fill the holes in the substrate giving rise to a depletion region (depleted of free carriers).

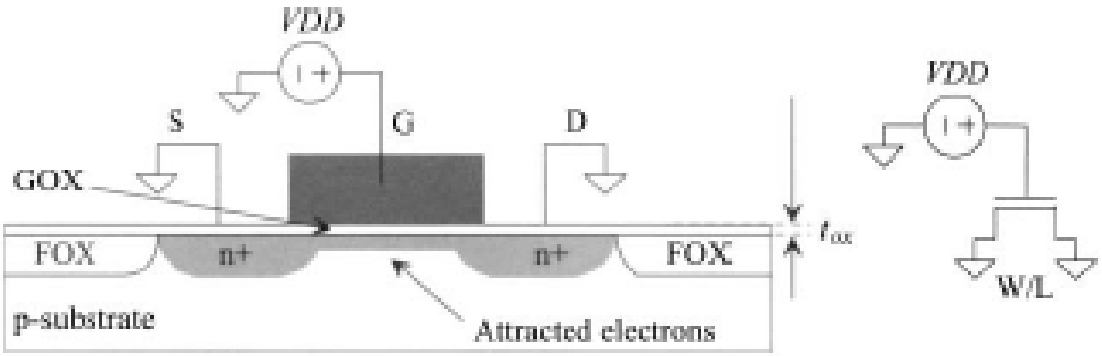

Fig. 2.5 NMOS device in strong inversion

If the source of the NMOS device is at a higher potential than the substrate, the potential difference is given by V_{SB}. This potential difference causes so called body effect. This effect raises transistor threshold voltage. The higher is source and bulk potential difference the more is needed gate voltage to form inversion layer under gate oxide.

MOSFET operates in saturation region when $V_{GS} \geq V_{THN}$ and $V_{DS} \geq V_{GS}$ - V_{THN}. When V_{DS} = V_{GS} - V_{THN}, the inversion charge under the gate at the drain-channel junction is zero. This drain-source voltage is called $V_{DS,sat}$ (= V_{GS} - V_{THN}), and indicates when the channel charge becomes pinched off at the drain-channel interface. Increases in V_{DS} beyond $V_{DS,sat}$ attract the fixed channel charge to the drain terminal depleting the charge in the channel directly adjacent to the drain. Further increases in V_{DS} cause only a little increase in the drain current. In other words the current saturates and thus almost stops increasing.

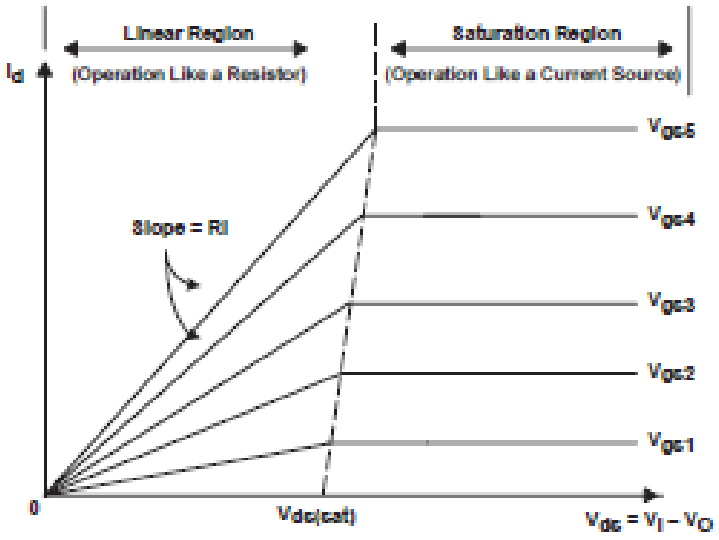

Fig. 2.6 Ideal characteristic of NMOS transistor

In figure 2.6 [8] is shown n-channel MOSFET characteristics in ideal case. When transistor is in cut-off region then it is in accumulation mode and zero current flows. In linear region there is weak inversion layer and drain current depends on V_{GS} and V_{DS}. In saturated region there is strong inversion layer and drain current independent of V_{DS}.

2.3 Error amplifier

For error amplifier we use the basic operational amplifier (op-amp) which is a fundamental building block in analog integrated circuit design. A block diagram of the two-stage op-amp is shown in figure 2.7.

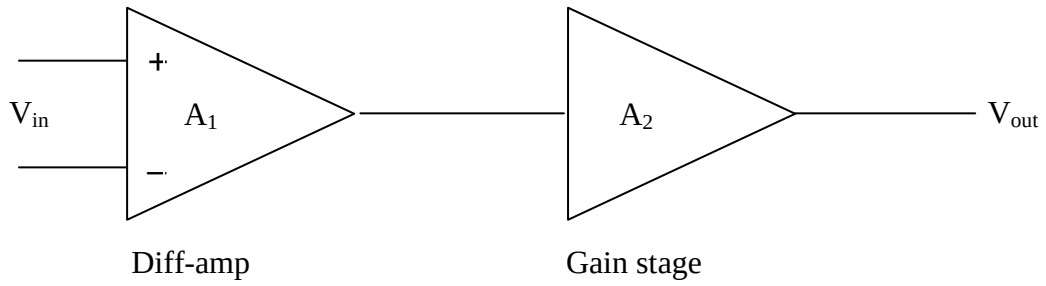

Fig. 2.7 Operational amplifier block diagram

The first stage of an op-amp is a differential amplifier. This is followed by another gain stage, such as a common source stage. If the op-amp is used to drive a resistive load or a large capacitive load (or a combination of both), the output buffer stage is used. Design of the op-amp consists of determining the specifications, selecting device sizes and biasing conditions, compensating the op-amp for stability, simulating and characterizing the op-amp A_{0L} (open-loop gain), CMR (common-mode range on the input), CMRR (common-mode rejection ratio), PSRR (power supply rejection ratio), output voltage range, current sourcing/sinking capability, and power dissipation. We are interested operational amplifier input pair influence to LDO so we use simple schematic for simulating. Operational parameter examining are not in scope of this work.

Figure 2.8 shows the basic two stage op-amp made using an NMOS diff-amp and a PMOS common-source amplifier (M6). NMOS input pair are made of transistors M1 and M2. M6 is biased to have the same current as M3 and M4. M5 and M7 are biased by V_{bias} from biasing circuit to sink certain amount of current.

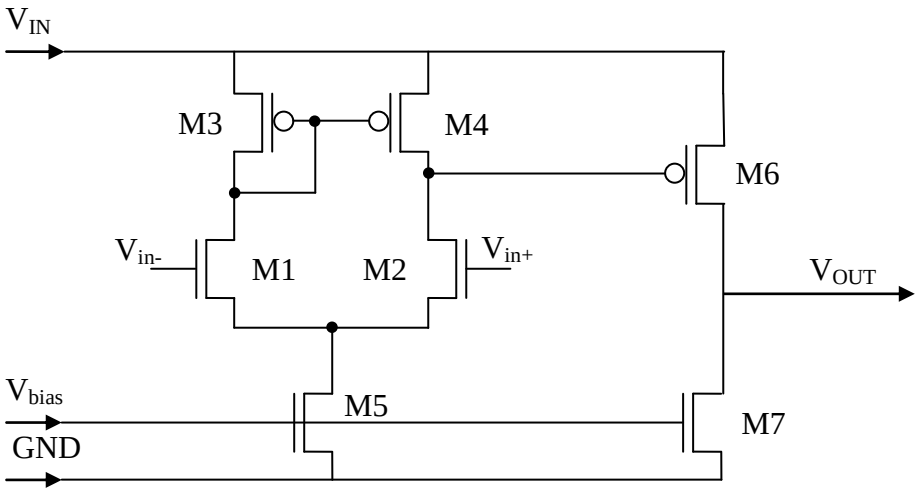

Fig 2.8 Simple operational amplifier schematic

3. LDO STRUCTURES

In next section is discussed different LDO structures which are in scope of this work. And then it is conclude and chosen best structure for simulation. For each case is used simplified circuit in figure 3.1 and 3.2 to describe working principle and voltage drops in schematic. Reference and feedback terminals are not connected to amplifier inputs because if we have NMOS pass element then we connect feedback to negative input and with PMOS to positive input of amplifier. Only variables are used, because there is no information of transistor voltage drops in this technology,

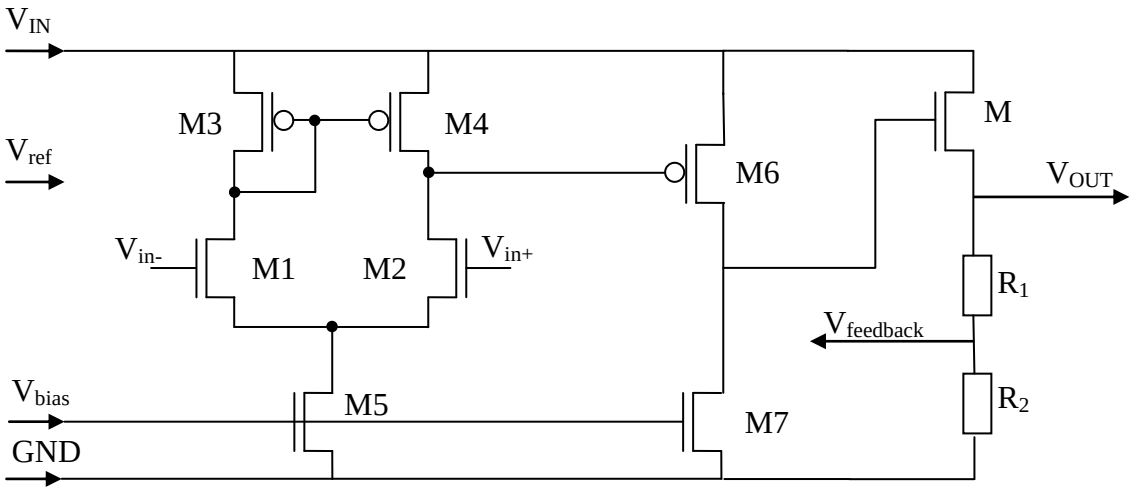

Fig. 3.1 LDO which amplifier have NOMS input pair

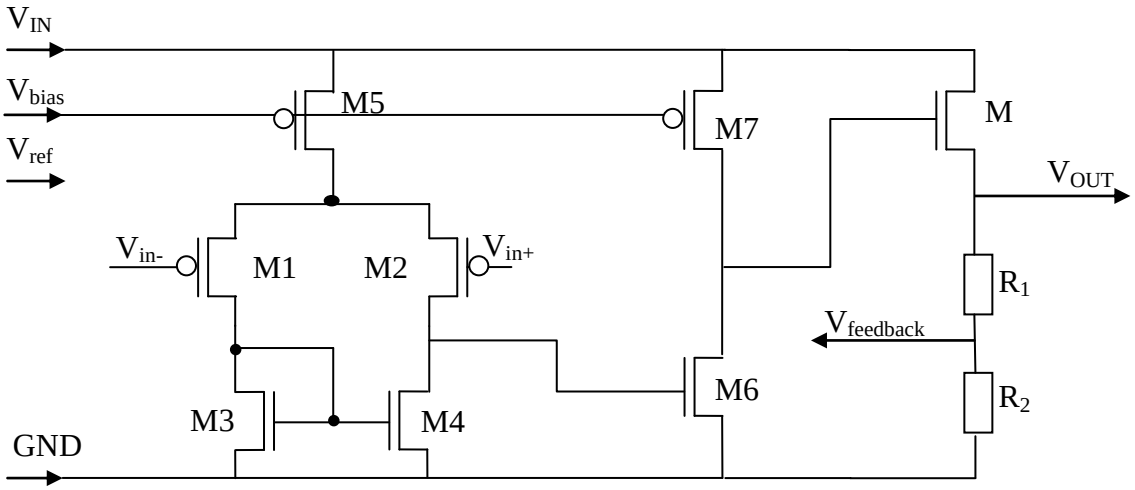

Fig. 3.2 LDO which amplifier have POMS input pair

3.1 OPAMP with NMOS input pair and NMOS pass element

This case simplified schematic is in figure 3.1. Pass element *M* needs voltage on drain to saturate $V_{DS,sat}$. Our source is at potential of V_{OUT}. On drain terminal should be at least:

$$V_D = V_{SD,sat} - V_{OUT} \, , \tag{3.1}$$

To hold pass element in saturation, amplifier must supply voltage to pass element gate terminal so much that V_{GS} is higher than threshold voltage. On gate terminal should be voltage:

$$V_G = V_{THN,be} + V_{OUT} \, , \tag{3.2}$$

$V_{THN,be}$ means that V_{THN} is higher than normally due to body effect because pass element V_{SB} is greater than zero.

From error amplifier circuit could see that supply voltage should overcome three transistor voltages to get all transistors operate in saturation region. These voltages are *M5´s* $V_{DS,sat}$, *M1´s* $V_{DS,sat}$ and *M3´s* V_{SG} voltage. Error amplifier needs supply voltage to operate in saturation region:

$$V_{IN,min} = 2 \bullet V_{DS,sat} + V_{SG} \, , \tag{3.3}$$

Amplifier inputs voltages must overcome input transistor threshold voltage and voltage $V_{DS,sat}$ what needs transistor *M5* to operate in saturation region. So reference voltage must be greater than:

$$V_{ref} > V_{THN,be} + V_{DS,sat} \, , \tag{3.4}$$

Amplifier maximum output voltage is:

$$V_{EAOUT,max} = V_{IN} - V_{SD,sat}\,, \tag{3.5}$$

In this case we can see that main problem with this circuit is that amplifier can supply to pass element gate almost all supply voltage but this is not enough to bring pass element in saturation region. This means that circuit dropout voltage is big because pass element work in sub threshold region. In this LDO structure case minimum V_{IN} formula is:

$$V_{IN,min} = V_{THN,be} + V_{OUT}\,, \tag{3.6}$$

And minimum output voltage is:

$$V_{OUT,min} = 0\,, \tag{3.7}$$

Dropout voltage is:

$$V_{DO} = V_{THN,be}\,, \tag{3.8}$$

3.2 OPAMP with NMOS input pair and PMOS pass element

This structure simplified schematic is in figure 3.1. Pass element *M* needs on source side that V_{SG} is higher voltage than threshold voltage because transistor gate need to overcome threshold voltage V_{THP}. PMOS device do not have body effect because source and bulk both are tied to V_{IN}. On pass element gate terminal should be on ground potential to achieve best performance. Amplifier minimum output voltage is 0 V. Error amplifier have same figures as previous case. In this LDO structure case minimum V_{IN} formula is:

$$V_{IN,min} = 2 \bullet V_{DS,sat} + V_{SG}\,, \tag{3.9}$$

Minimum output voltage formula is:

$$V_{OUT,min} = V_{IN,min} - V_{DS,sat}\,, \tag{3.10}$$

Dropout voltage is

$$V_{DO} = V_{DS,sat}\,, \tag{3.11}$$

3.3 OPAMP with PMOS input pair and NMOS pass element

This case simplified schematic is in figure 3.2. Pass element acts same way like in section 3.1. From this circuit could see that supply voltage should overcome three transistor voltages to get all transistors operate in saturation region. These voltages are *M5´s* $V_{SD,sat}$, *M1´s* $V_{SD,sat}$ and *M3´s* V_{GS} voltage. Minimum amplifier supply voltage is:

$$V_{IN,min} = 2 \bullet V_{SD,sat} + V_{GS}\,, \tag{3.12}$$

Amplifier inputs voltages must be as lower than two $V_{SD,sat}$ voltage. If input voltage is higher the source voltage needs to raise to stay in saturation. Amplifier maximum output voltage equals to input voltage. Here we can also see problem that amplifier still cannot supply to pass element gate enough voltage to overcome pass element threshold voltage. Circuit dropout voltage is big because pass element work in sub threshold region. In this LDO structure case minimum Vin formula is:

$$V_{IN,min} = V_{THN,be} + V_{OUT}\,, \tag{3.13}$$

And minimum output voltage is:

$$V_{OUT,min} = 0\,, \tag{3.14}$$

Dropout voltage is:

$$V_{DO} = V_{THN,be}\,, \tag{3.15}$$

3.4 OPAMP with PMOS input pair and PMOS pass element

Both blocks are discussed before sections 3.2 and 3.4. Only difference comes from amplifier where minimum output voltage is $V_{DS,sat}$. Therefore pass element needs part of $V_{DS,sat}$ voltage more at drain side than in section 3.2.

This case formulas are:

$$V_{IN,min} = 2 \bullet V_{DS,sat} + V_{SG}\,, \tag{3.16}$$

Minimum output voltage formula is:

$$V_{OUT,min} = V_{IN,min} - V_{DS,sat}\,, \tag{3.17}$$

Dropout voltage is

$$V_{DO} = V_{DS,sat}\,, \tag{3.18}$$

3.5 Conclusion

Different structures parameters are conclude in table 3.1 to compare them.

Table 3.1 Structures parameters comparison

Object / Parameter	N-type OPAMP	P-type OPAMP	NMOS transistor	PMOS transistor
V_{in_min}	$2 \bullet V_{DSsat} + V_{SGsat}$	$2 \bullet V_{SDsat} + V_{GSsat}$	$V_{DSsat} + V_{out}$	$V_{SDsat} + V_{out}$
V_{out_range}	$0....V_{in} - V_{SDsat}$	$V_{DSsat} ....V_{in}$	$0....V_{in} - V_{DSsat}$	$0....V_{in} - V_{SDsat}$
$V_{dropout}$	-	-	V_{DSsat}	V_{SDsat}
I_{out}	100 mA	100 mA	100 mA	100 mA
$V_{ref\_optimal}$	$>V_{THN} + V_{DSsat}$	$<V_{in} - V_{DSsat}$	$<V_{DSsat} + V_{out}$	$<V_{SDsat} + V_{out}$
Body effect	yes	yes	yes	no

Best structure is operational amplifier with NMOS input transistor pair and PMOS pass element. PMOS pass element gives lowest dropout in these structures. NMOS input transistors amplifier output voltage can go very low so the PMOS pass element threshold voltage can achieved faster with supply voltage raise. PMOS input transistors input voltage raises the amplifier minimum supply voltage. In addition amplifier with NMOS input pair reference voltage can be higher so there can use bandgap voltage reference which have good stability if temperature change.

NMOS pass device problem is error amplifier which cannot supply enough voltage. Problem can be fixed if take supply voltage for amplifier before first regulator DC-DC conversation. And further more it allows to go lower input and output voltages.

4. DESIGN AND SIMULATIONS

In this chapter is discussed and designed LDO parts and different simulations for LDO operational parameters.

4.1 Operational amplifier

Operational amplifier is design based on schematic what was proposed in section 2.3. The designed circuit in cadence is in figure 4.1. Transistor sizes are taken from earlier experience. Amplifier bias current is taken 1 μA. Transistor M8 current is mirrored to transistors M5 and M7. Transistor M5 width is twice time bigger than M8 because it sinks two branch current which is 2 μA. Input transistors M1 and M2 width are many time bigger than other transistors to minimize operational amplifier input offset voltage which is calculated by equation 4.1.

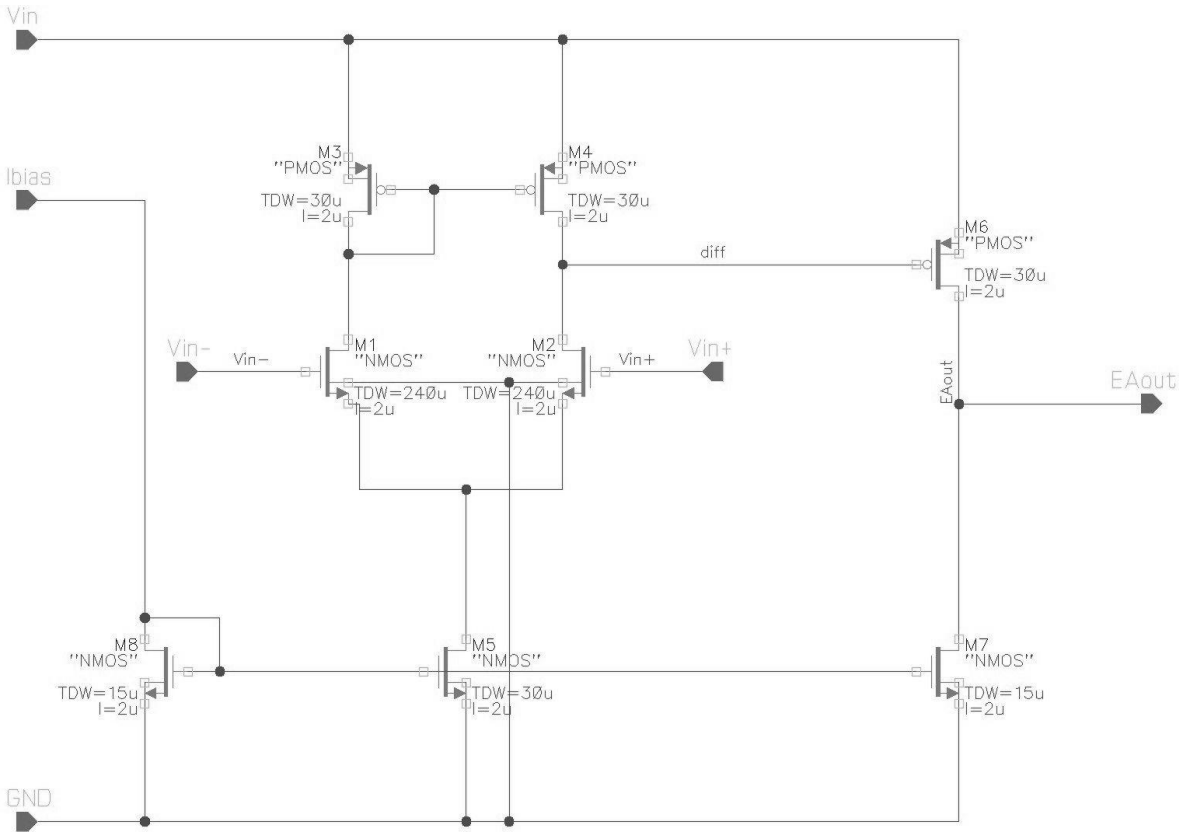

Fig 4.1 Operational amplifier with NMOS input pair design

$$V_{offset} = \frac{V_T}{\sqrt{W \cdot L}} = \frac{25{,}69}{\sqrt{240 \cdot 2}} = 1{,}172\ mV \tag{4.1}$$

$$V_T = \frac{k \cdot T}{q} = \frac{1{,}38 \cdot 10^{-23} \cdot 25}{1{,}6^{-19}} = 25{,}96\ mV \tag{4.2}$$

Simulation of sweeping operational amplifier supply voltage and reference voltage and same time observing M5 current is in figure 4.2. From there can find point where amplifier is started working correctly. This point is where M5 current line is crossing with 2 µA marker line. From figure can see that with reference voltage 825 mV, supply voltage should be at least 1,05 V. With higher reference voltage the amplifier supply voltage could be lower. Operational amplifier supply voltage can be one reason why we cannot go lower with input voltage. If this is the reason then solution is to use separate power supply or supply before post regulation, if it is suitable for operational amplifier. Because operational amplifier parameters are not in focus of this work, here is not simulated operational amplifier alone anymore.

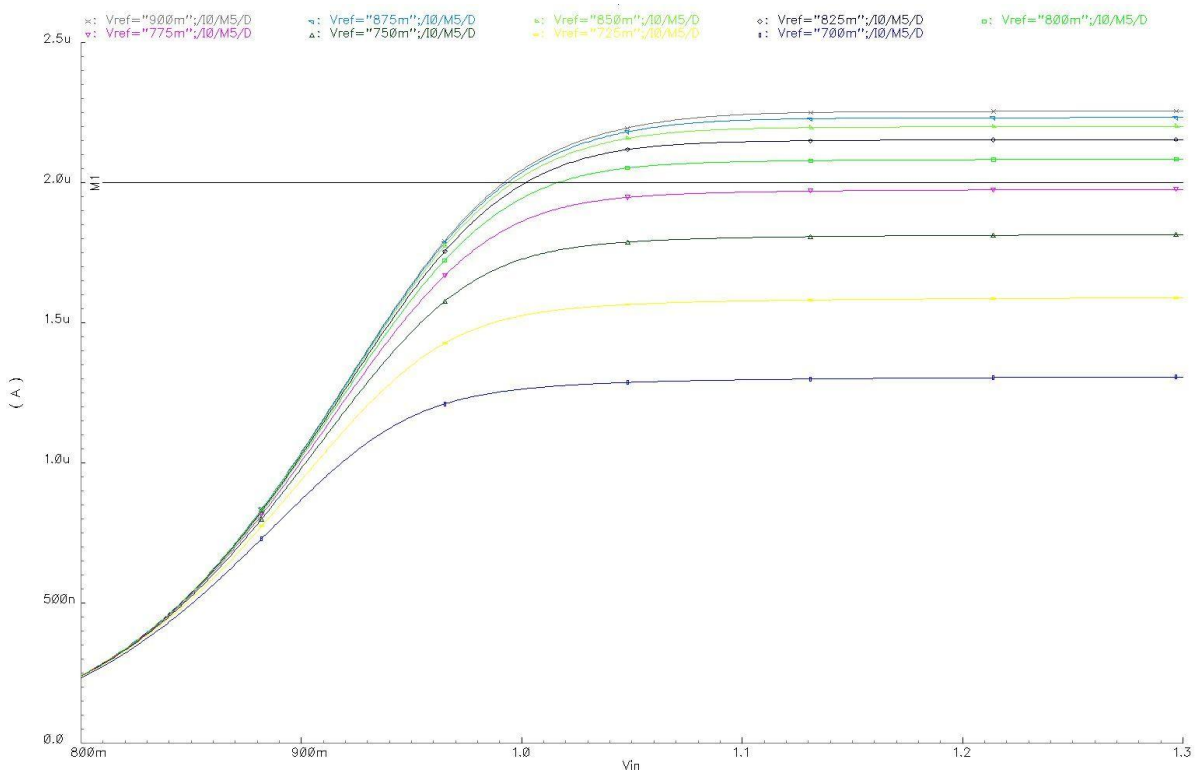

Fig. 4.2 Operational amplifier minimum supply voltage

4.2 LDO

LDO is designed accordingly to section 3 figure 3.1. In figure 4.3 is shown designed LDO circuit schematic. Here is used before designed operational amplifier cell.

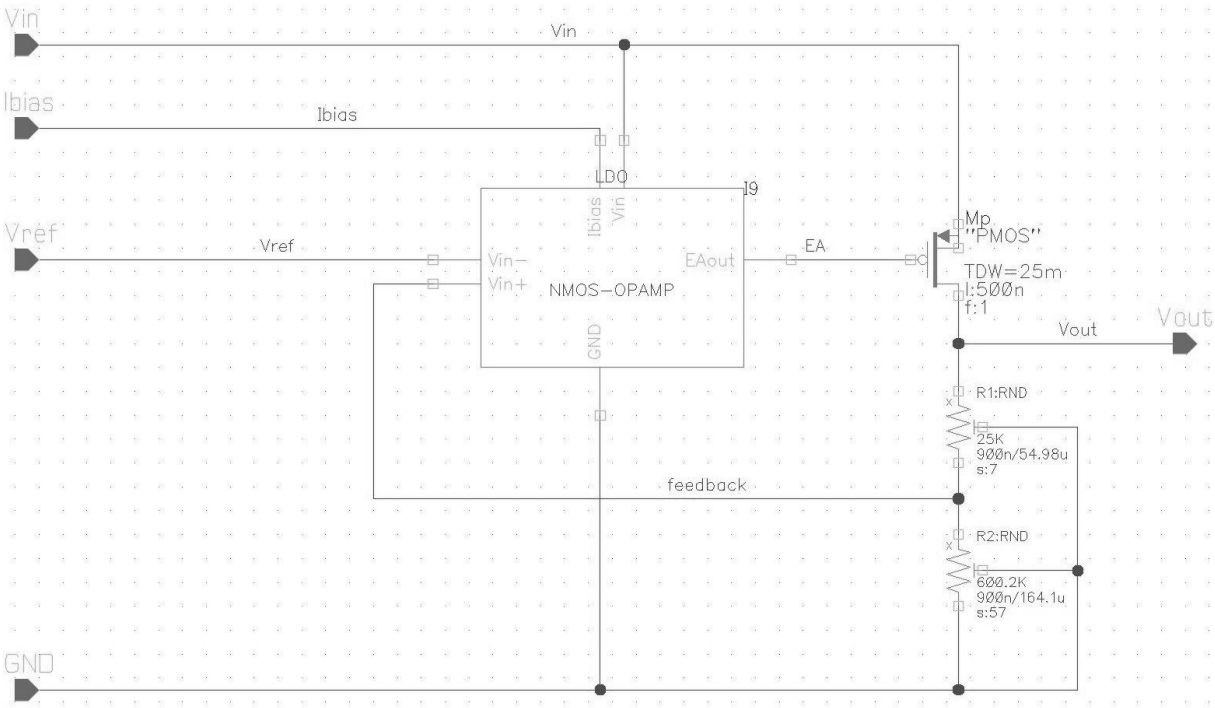

Fig. 4.3 LDO circuit design

To simulate this LDO is made another schematic in figure 4.4. There are added all power and bias supplies. Two transistors attached to LDO output forms current mirror which is used as load to LDO.

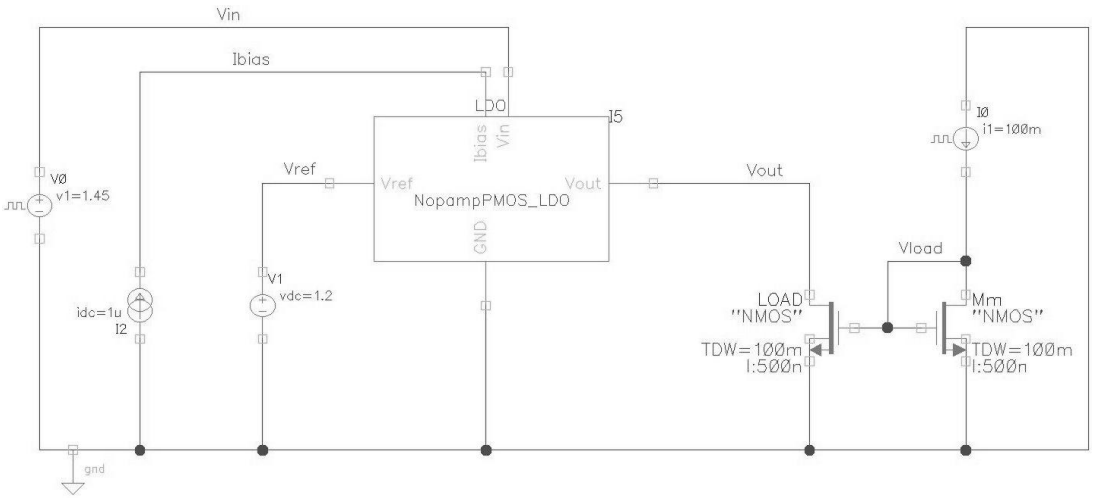

Fig. 4.4 Circuit design for simulating LDO

In first simulation I observe how pass element and operational amplifier affect output voltage when increasing input voltage from 0 to 5 V. This simulation is shown on figure 4.5. From figure can see that after about 1.1 V the transistor is slightly opening and dropout voltage is rapidly going to decrease. I did one simulation where operational amplifier has independent supply of 5 V and then the result was same like in figure 4.5. This means that here we see pass element characteristics and operational amplifier has no effect and can be powered by same input voltage.

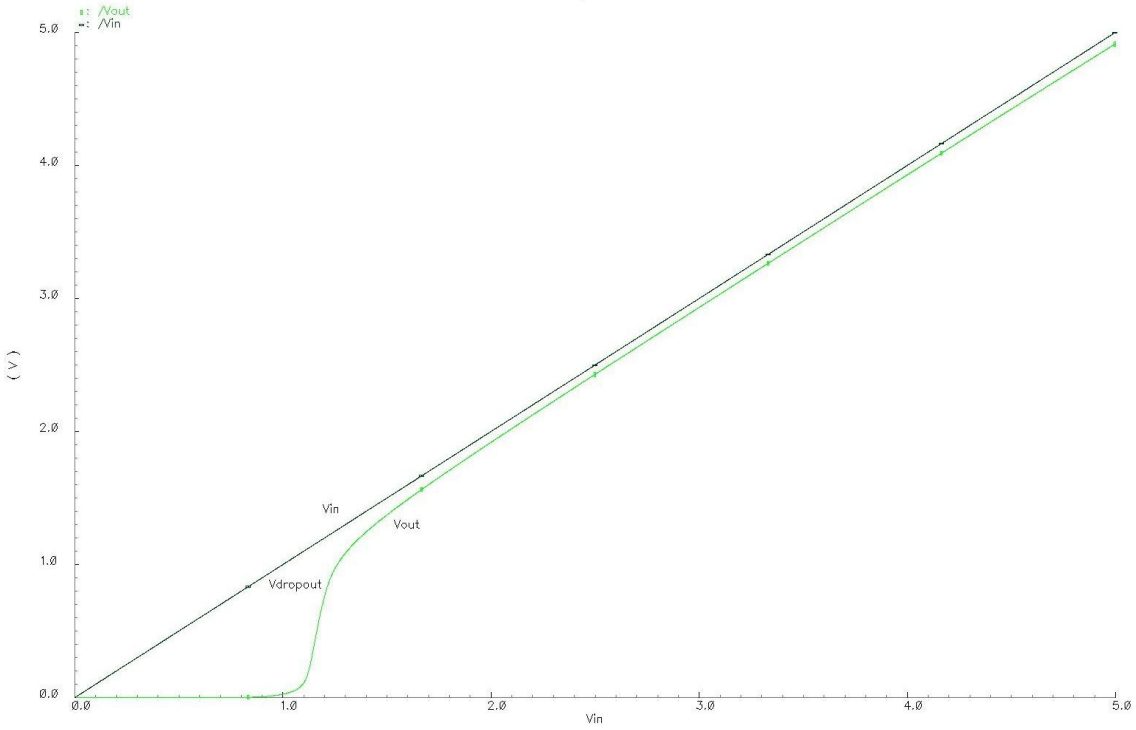

Fig 4.5 Pass element regulation

In next simulation I examine how pass element size affect dropout and minimum input voltage. Pass element size can be calculated with this formula:

$$I_D = \frac{KP_p}{2} \bullet \frac{W}{L} \bullet \left(V_{SD,sat}\right)^2 \tag{4.3}$$

Transistor can pass current with little dropout voltage when transistor length is minimum allowed size and width is chosen according to equation:

$$W = \frac{2 \bullet I_D \bullet L}{K \bullet P_p \bullet \left(V_{DS,sat}\right)^2} \tag{4.4}$$

Because there is no information about all technology parameters, I cannot calculate this but I can simulate schematic with sweeping pass element sizes and input voltage and observing dropout voltage. Simulations are done with maximum load (100 mA). This simulation results are shown in figure 4.6. Different curves is with different pass element size. This PMOS=”number” must be divide with 10 000 then can get PMOS transistor width size. Like PMOS=100 means that PMOS width is 10 mm and for all transistors the length is minimum allowed size 500 nm. Marker M1 shows 200 mV dropout line.

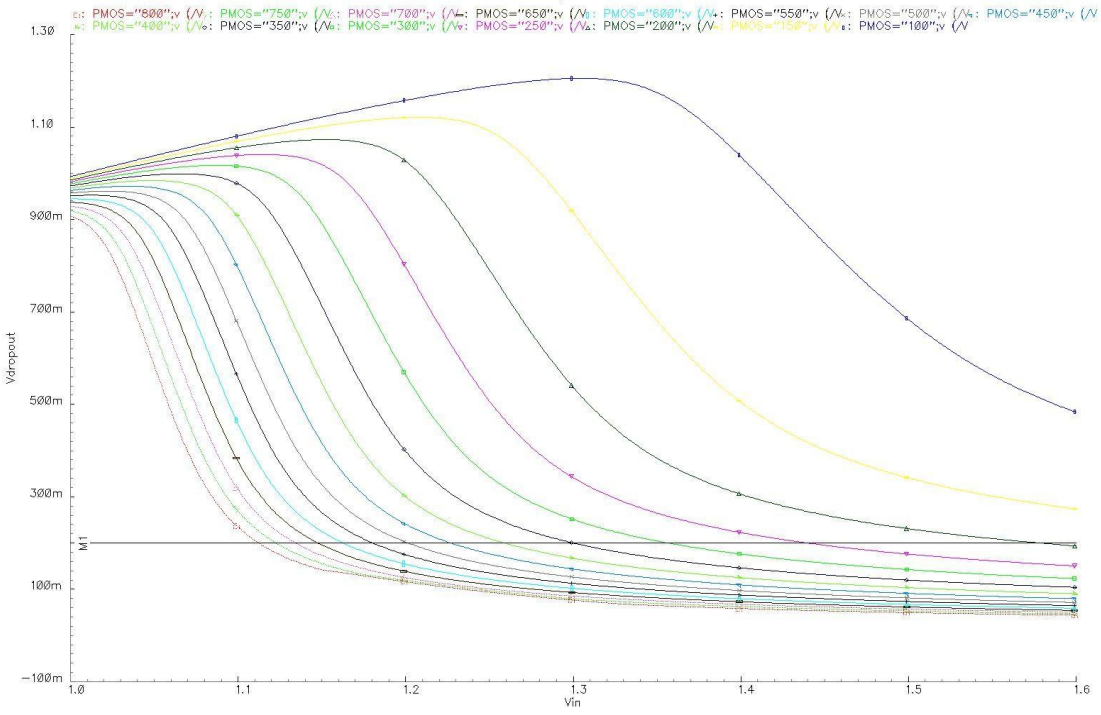

Fig. 4.6 Pass element sizes and input voltage sweep effect to dropout voltage

From figure can see that at the beginning the size effect is huge but at some point it do not affect dropout voltage and minimum input voltage so much but takes on silicon only more valuable space. So here is place where should decide how much valuable silicon area leave for pass element for getting acceptable dropout voltage and input voltage. I decided to take PMOS transistor width with 25 mm because I don't see point to waste more silicon area with so little drop in dropout voltage. So with my chosen size, minimum input voltage is 1.45 V and with dropout 200 mV the output voltage is 1.25 V.

For calculating divider circuit resistor sizes I choose for divider current to be about 2 μA. For operational amplifier reference voltage I take 1.2 V. From Ohm law can get divider estimated resistance:

$$R = \frac{U}{I} = \frac{1{,}25\ V}{2\ uA} = 625\ k\Omega \tag{4.5}$$

$$R = R_1 + R_2 \tag{4.6}$$

So divider resistors should be from equation 2.1 and 4.4:

$$R_2 = \frac{V_{ref} * (R_1 + R_2)}{V_{out}} = \frac{1{,}2\ V * (625\ k\Omega)}{1{,}25\ V} = 600\ k\Omega \tag{4.7}$$

$$R_1 = R - R_2 = 625\ k\Omega - 600\ k\Omega = 25\ k\Omega \tag{4.8}$$

In figure 4.7 is shown how LDO reacts when load current change from 0 to 100 mA. Here is only little voltage drop when load current change. Near the max load the voltage is

going to reduce faster because pass element reaches to maximum current with acceptable dropout voltage.

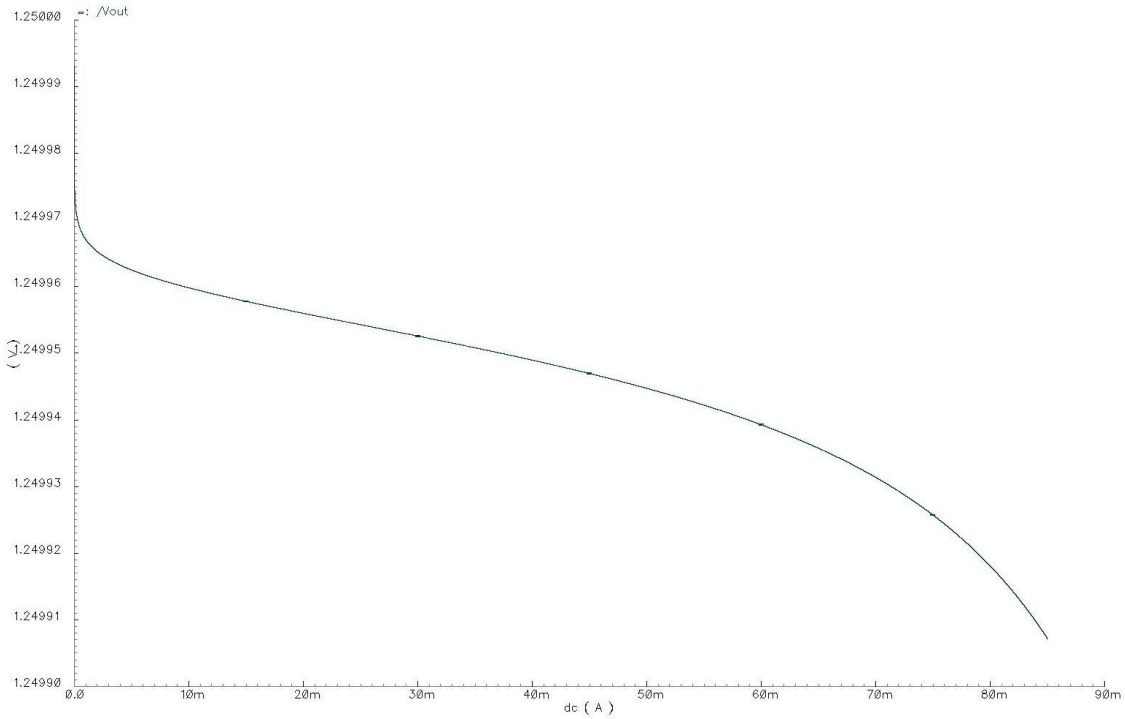

Fig 4.7 Load current change effect to output voltage

For AC sweep the schematic need to be modified. There need to be add inductor and capacitor to feedback circuit. Modified circuit is shown in figure 4.8.

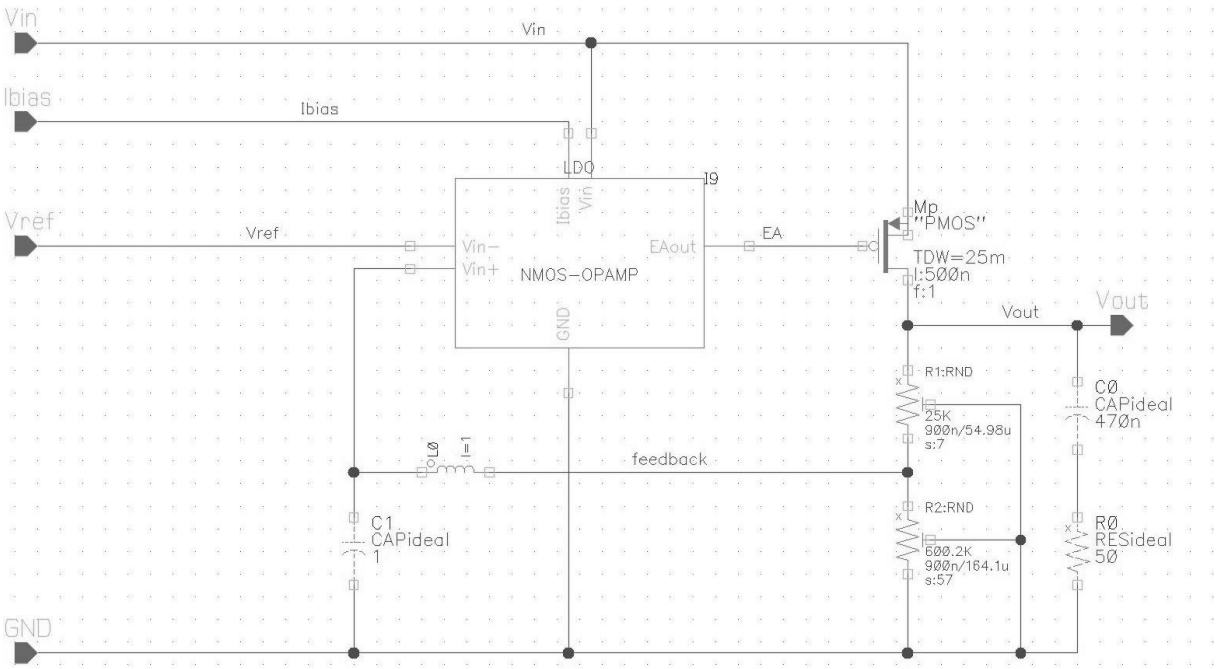

Fig 4.8 Modified schematic for AC sweep

AC sweep in figure 4.9 shows that circuit is not stable because phase is went over 180 degrees at the time gain is not yet zero. This can be avoided if put on output capacitor and resistor in series, this is called equivalent series resistance (ESR). With appropriate values they will stabilize LDO output. From simulations I found for these values which is for capacitor 470 nF and for resistor 50 Ω.

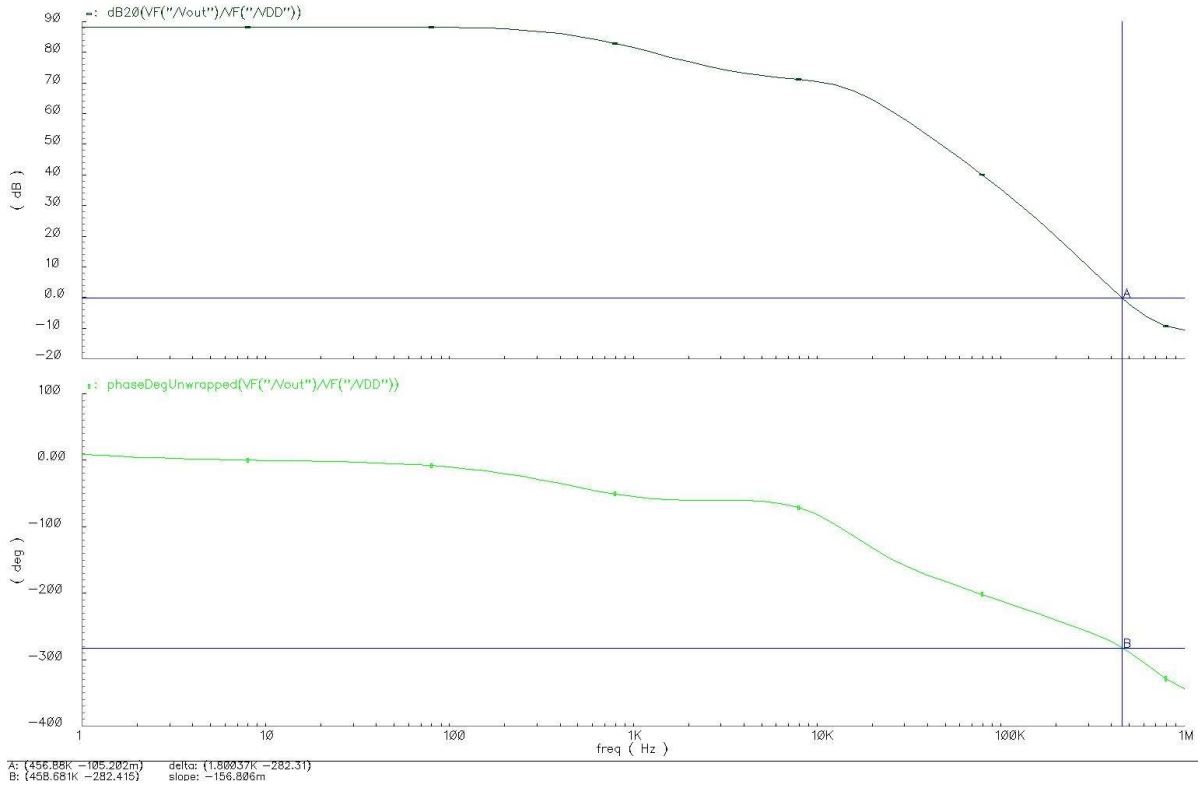

Fig 4.9 AC response without ESR compensation

Stabilized AC response is seen from figure 4.10. There can see that if gain is zero then phase is 116 degrees which guarantees stability. One problem is that now the ESR capacitor is so big that it waste lot of silicon space. So it is beneficial to use ESR as external component which attached later to circuit.

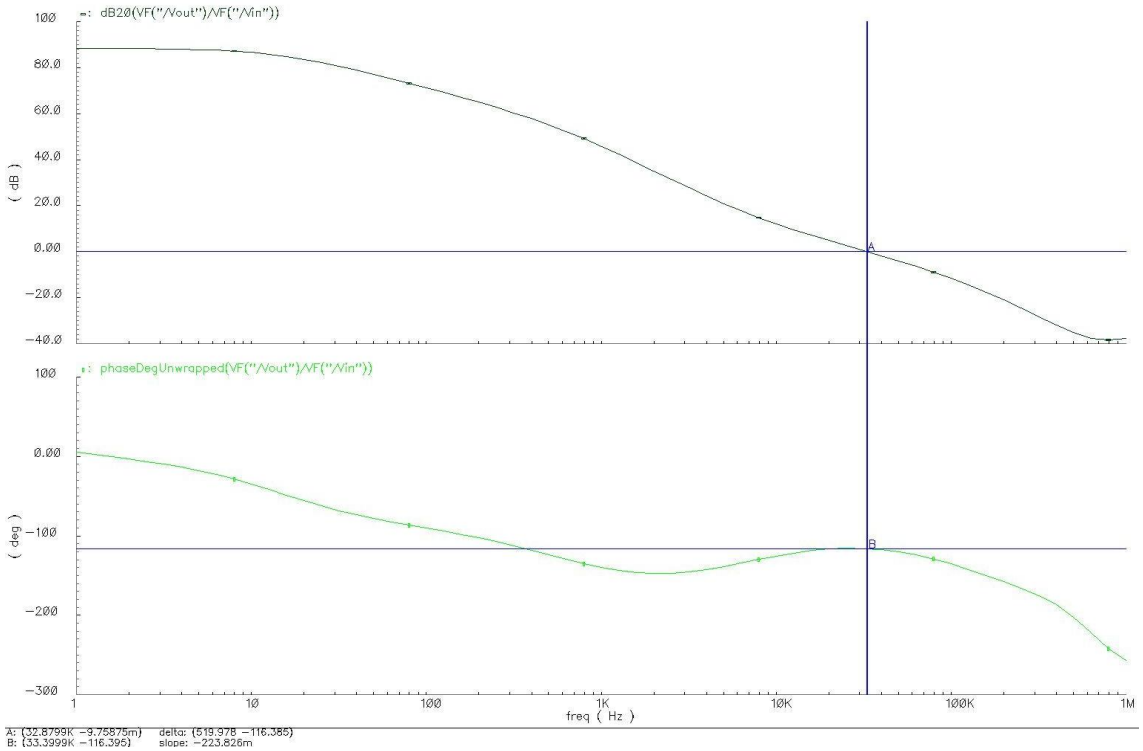

Fig 4.10 AC response with ESR compensation

Figure 4.11 shows how output reacts when output voltage raises from 0 to 1.45 V. There is clearly see that ESR stabilizes the output which wants do go to generate. Figure 4.11

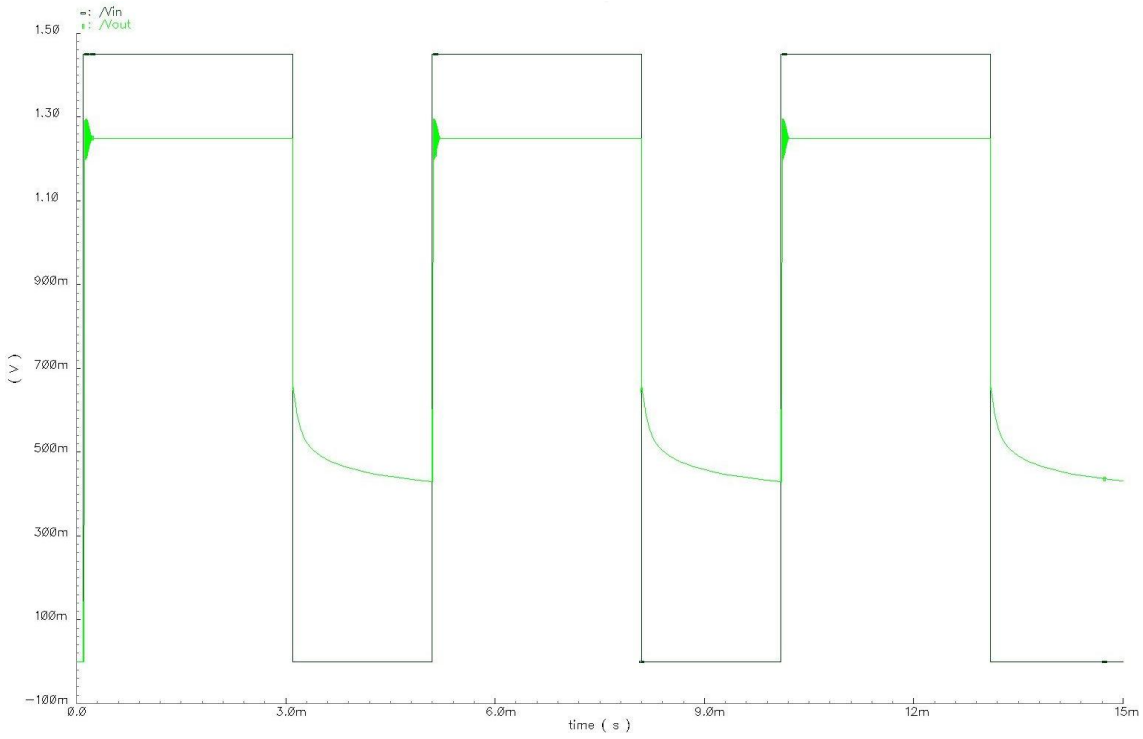

Fig 4.11 Transient response if input voltage appears with no load

is with no load and figure 4.12 is with maximum load. With maximum load the circuit do not want to go generate.

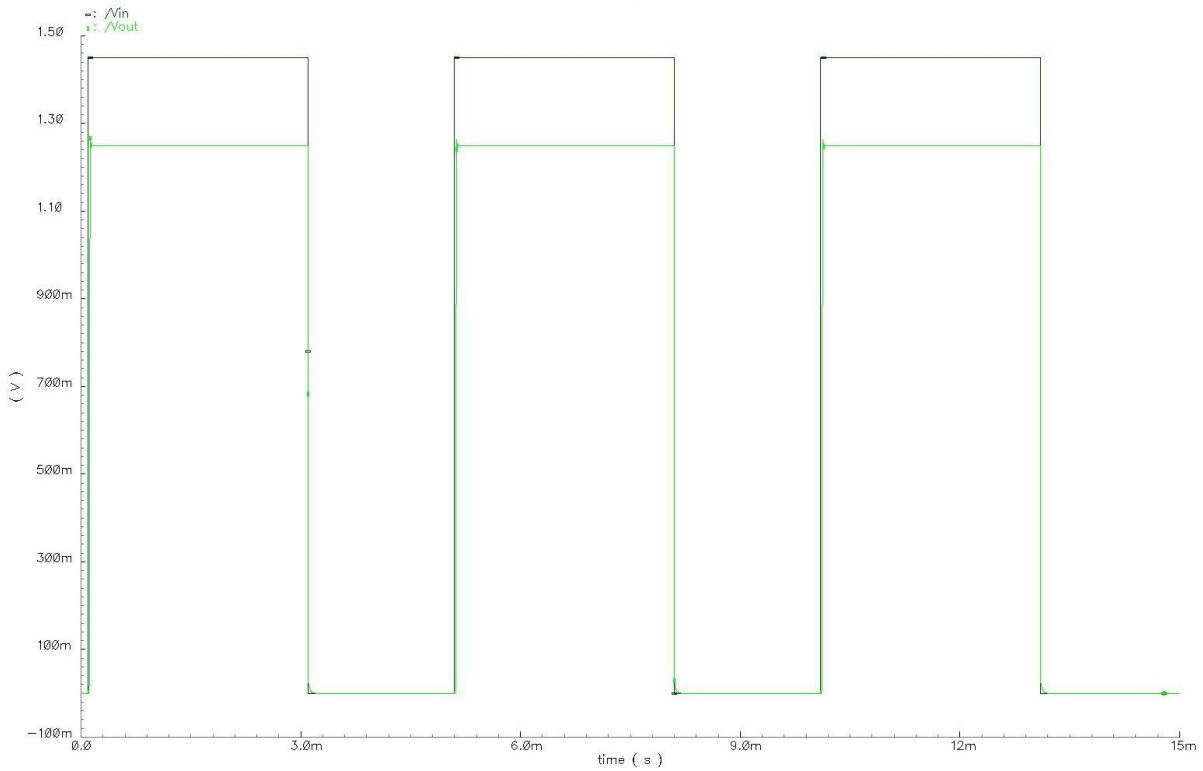

Fig 4.12 Transient response if input voltage appears with maximum load

Load regulation is a measure of the circuit ability to maintain the specified output voltage under varying load conditions. In figure 4.13 upper graph shows how output voltage reacts to change in output current(lower graph). Increasing open loop gain improves the load regulation. Load regulation is calculated by equation:

$$Load\ regulation = \frac{V_2 - V_1}{I_{L2} - I_{L1}} = \frac{19{,}3192\ uV}{100\ mA - 85\ mA} = 0{,}888\ mV/A \tag{4.9}$$

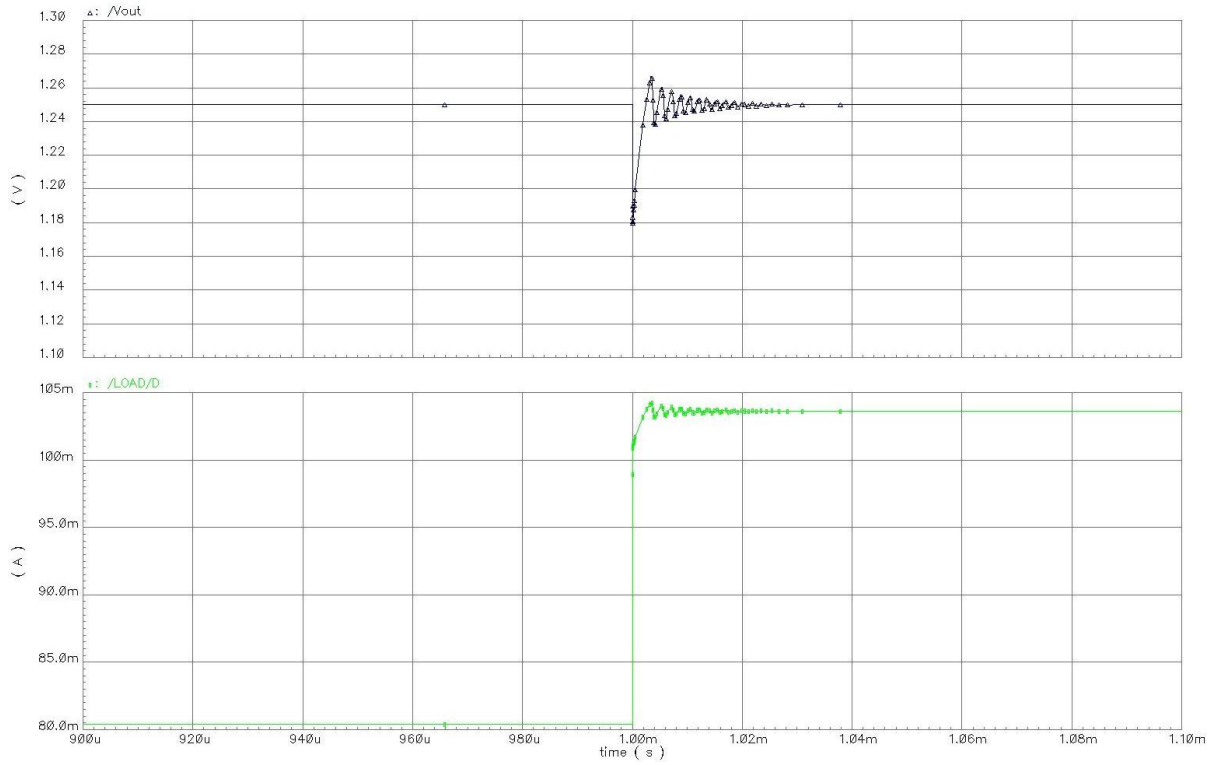

Fig 4.13 Load regulation when load change 20 mA

Line regulation is a measure of the circuit's ability to maintain the specified output voltage with varying input voltage. In figure 4.14 upper graph shows how input voltage change influence output voltage(lower graph). Line regulation is calculated by equation:

$$Line\ regulation = \frac{V_2 - V_1}{V_{L2} - V_{L1}} = \frac{71{,}1107\ uV}{1{,}55\ V\ - 1{,}45\ V} = 0{,}711\ mV/V \tag{4.10}$$

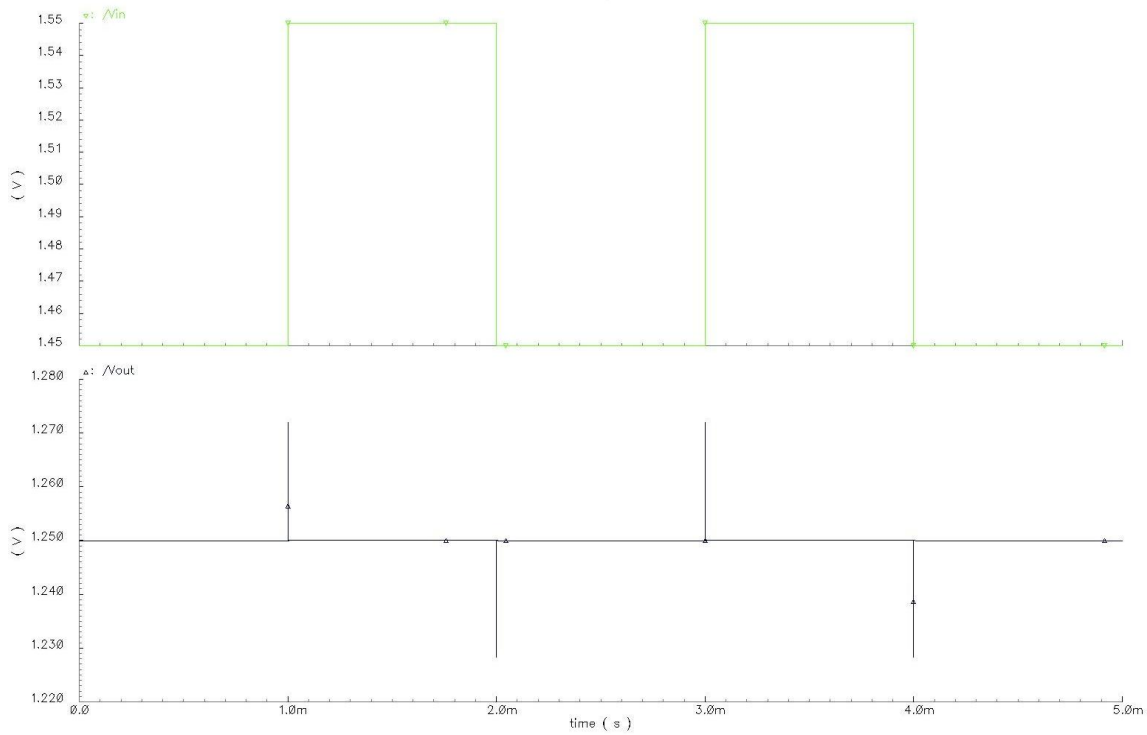

Fig 4.14 Line regulation when input voltage change 100 mV

Figure 4.15 shows how temperature affects LDO output voltage. Temperature change from -50° to 125° change output voltage 61 µV.

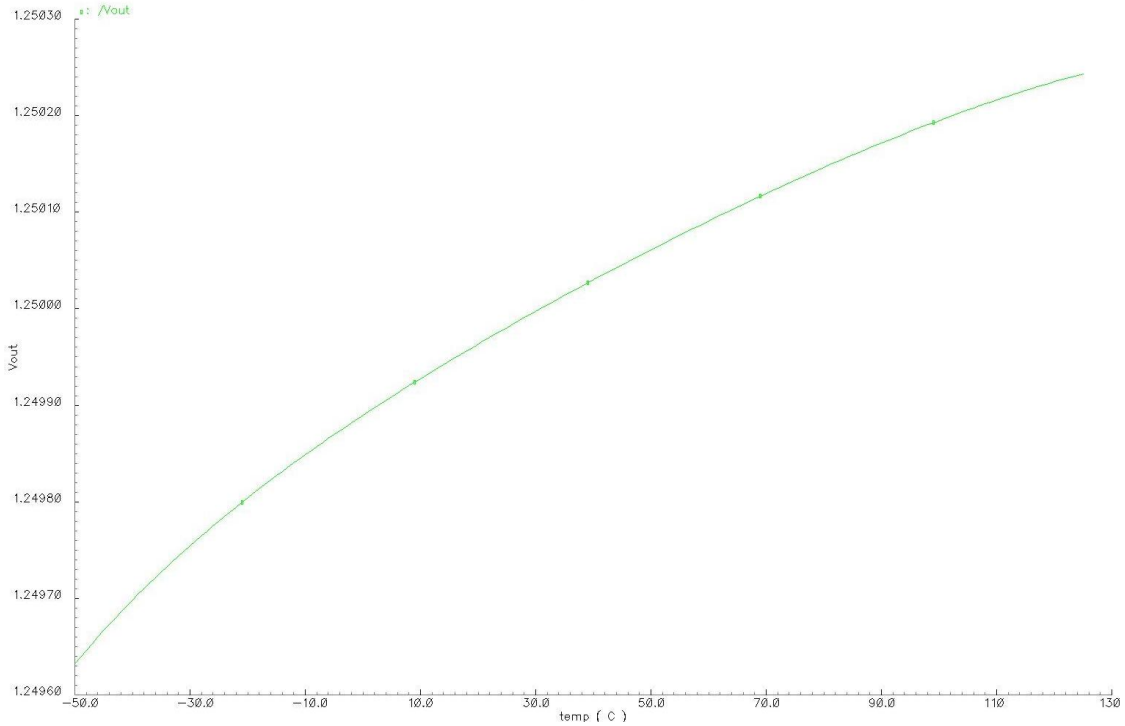

Fig 4.15 Temperature effect to output voltage

Table 4.1 LDO parameters

Parameter	**Conditions**	**Value**	**Units**
Input voltage		1.45	V
Output voltage	V_{IN} = 1.45 V	1.25	V
Dropout voltage	I_{load} = 100mA	200	mV
Quiescent current		6,31	μA
Load regulation		0,888	mV/A
Line regulation		0,711	mV/V

5. LAYOUT

In this section is explained how LDO layout was made. Firstly was designed output transistor because it takes most of silicon space. To save silicon area it is useful to design it as much possible to square shape. Output transistor is divided to 1250 pieces. After calculating various configurations it seemed that reasonable pattern should be 125 x 10 pieces which should be at the moment closest pattern to square. When the transistor pieces are moved to place it looks like area 1 in appendix B figure 1.

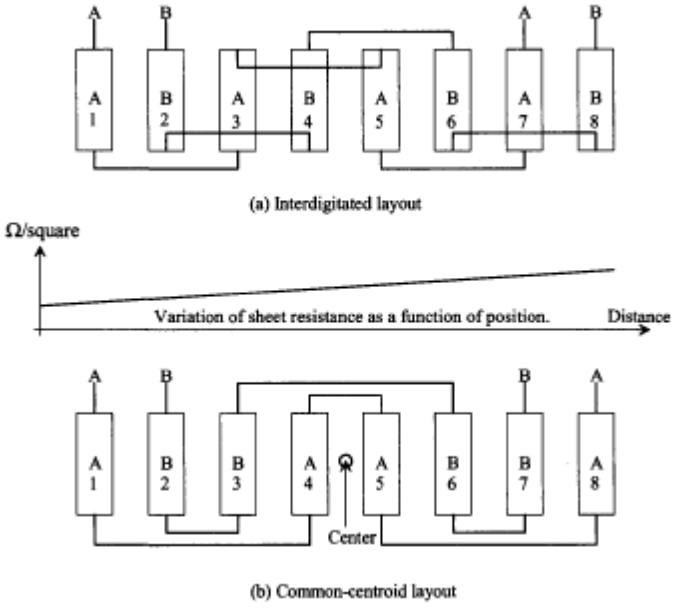

Fig. 5.1 Transistor matching methods

Next important thing is to match operational amplifier input transistors. Both transistors are divided to 12 pieces. They are matched with interdigitated method(Fig5.1[8]) in two rows. This matching helps to improve operational amplifier input offset because then input transistors have almost same conditions on silicon. The matched transistor are shown in figure 5.2.

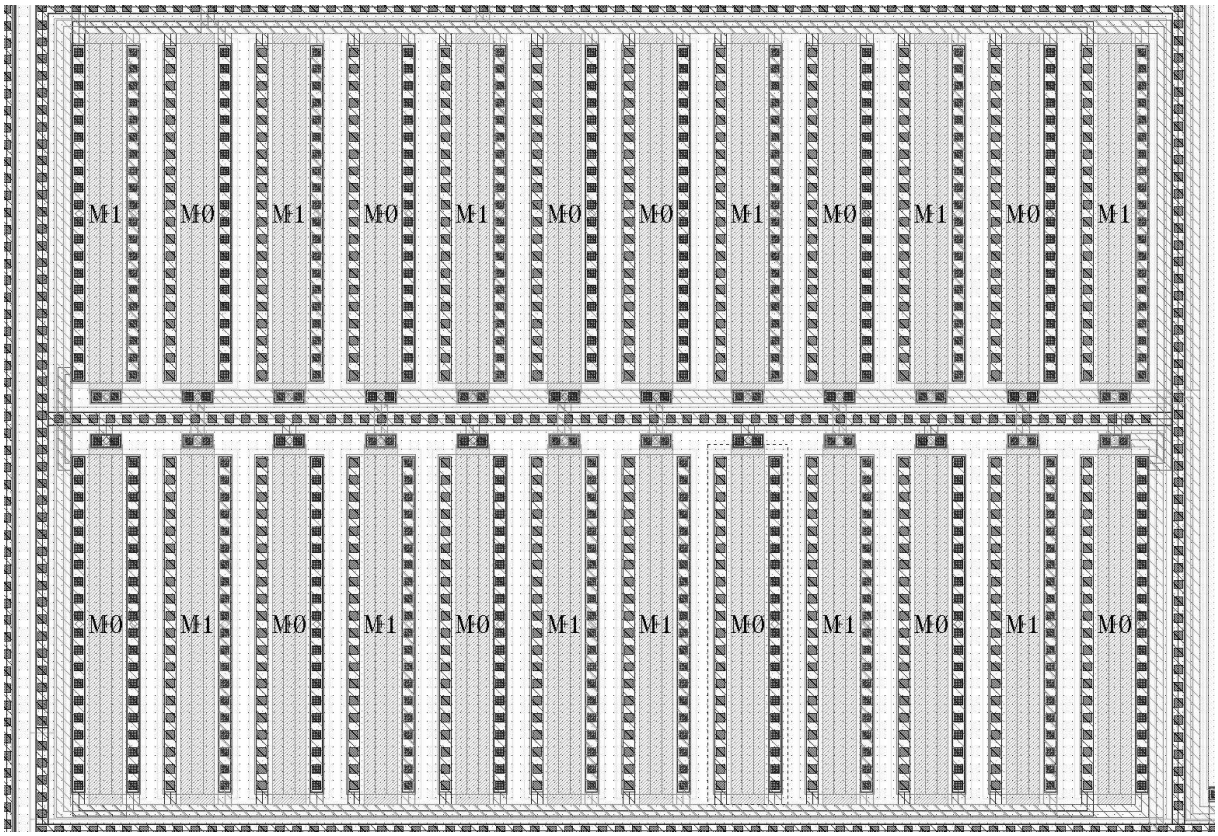

Fig 5.2 Matched differential input transistors

Bias current mirrors are matched together. Transistor M2 is divided to two pieces. One piece is first one and second one is last one. Transistor M3 and M4 is located between them(Fig 5.3). In this way the transistors sheet resistances are most equal and sizes are equal.

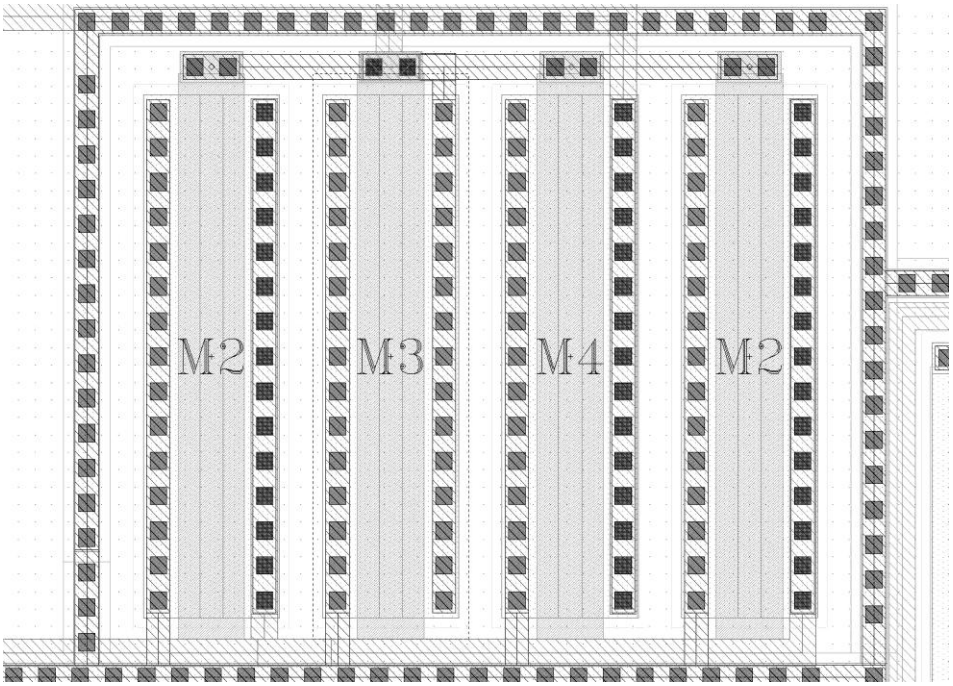

Fig 5.3 Matched OPAMP bias transistors

Transistors M5, M6 and M7 are matched with common-centriod method(Fig5.1[8]). Matching are shown on figure 5.4.

These three matched blocks are placed near to each other to have nearly same conditions on silicon. This helps to improve LDO output voltage stability because all transistors have nearly same conditions(temperature, sheet resistance, etc) on silicon.

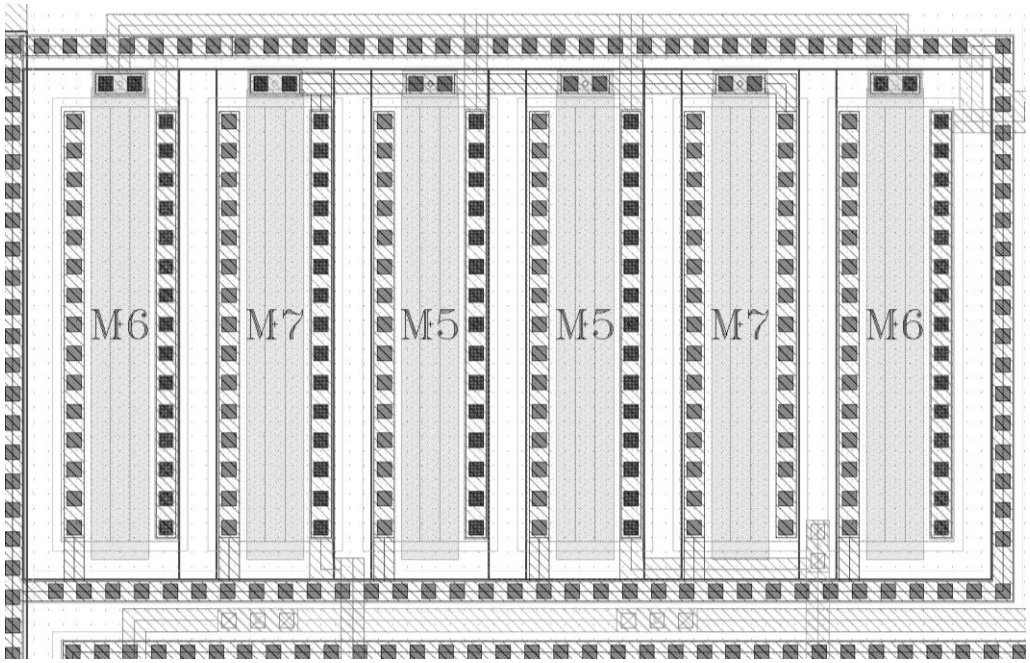

Fig 5.4 Matched OPAMP transistors

In appendix B figure 1 is designed LDO layout. The biggest rectangle(Area 1) is LDO output transistor. On top of output transistor is input voltage conductive path and bottom is output conductive path. On right side is attached operational amplifier matched transistors blocks. The biggest block is matched input transistors block(Area 3). On top left side of that is matched bias transistors block(Area 4) and on top right side is matched transistors M5, M6 and M7 block(Area 5). Area 2 and 6 are feedback divider resistors. From this figure can clearly see how much place takes only output transistor compared with operational amplifier transistors.

6. CONCLUSION

In this work first chapter gave short overview of DC voltage regulators main working principle. Linear and switching regulators main types and their advantages and disadvantages. Next chapter concentrated to post regulation LDO main blocks and working principle. Every LDO block was examined separately. LDO consist of four main block: error amplifier, pass element, feedback and reference voltage. Work main idea was examine LDO with different configurations and find best solution where is lowest input voltage and reasonable dropout voltage. Different configurations where made of OPAMP which had NMOS or PMOS input transistors and pass element was NMOS or PMOS transistor. After different configuration comparison appeared that best solution is OPAMP with NMOS input transistors and PMOS pass element.

Firstly was designed OPAMP circuit for LDO. This design did not concentrate to OPAMP parameters because this is not in focus of this work. For LDO circuit was added to OPAMP cell pass element and feedback resistors. To simulate LDO cell there was added voltage supplies, bias current and current mirror as load. Based on simulations was found pass element reasonable size and minimum input voltage. LDO was not stable so there was need for ESR. Simulating on output different C and R values were found best ESR values. Last chapter described how LDO layout was matched and designed.

Work target was find to minimum input voltage to LDO when dropout voltage is under 200 mV and maximum load current 100 mA was reached. Under these conditions in National's CMOS7-5V process technology this LDO minimum input voltage is 1,45 V and LDO output voltage is 1,25 V. This LDO chip needs ESR on output to be stable. Best ESR values are 50 Ω resistor and 470 nF capacitor.

It is possible to go lower with input voltage but this means that output transistor needs occupy more expensive chip area. For designed LDO there were found output transistor size were it was reasonable to give so much space to win in lowering input voltage. To lower input voltage same amount every time need always far more space than before. To go lower with input voltage then it is going gradually more expensive.

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APPENDIX A – LDO LAYOUT

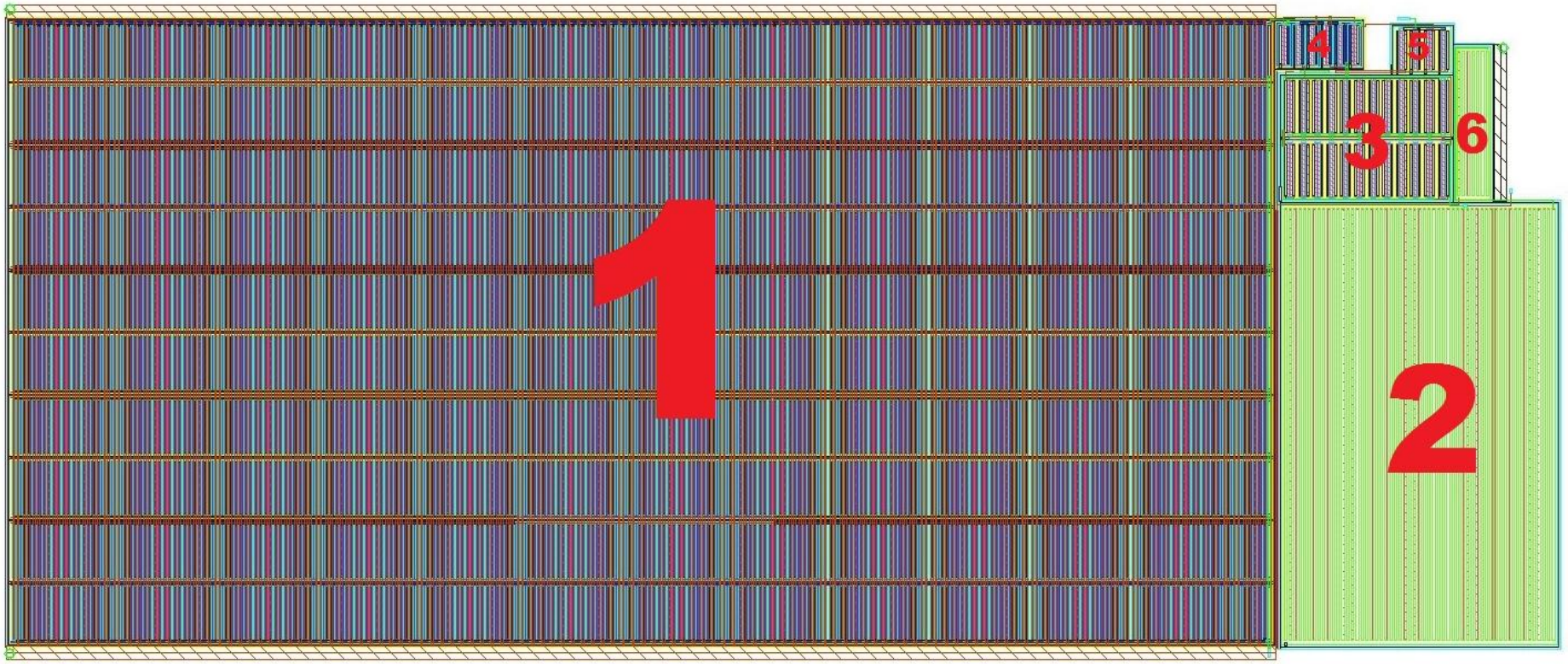

Fig. 1 LDO layout

1. Output transistor
2. Feedback resistor R2
3. Differential input transistors
4. OPAMP transistors M5, M6, M7
5. OPAMP bias transistors
6. Feedback resistor R1