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Transmitter Power Control in Wireless Communication Systems

MARKO KOORT

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Transmitter Power Control in Wireless Communication Systems

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Declaration: *Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for any degree or examination.*

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List of abbreviations

AC Alternating Current
ACI Adjacent Channel Interference
ACCH Associated Control CHannel
AGCH Access Grant CHannel
ARFCN Absolute Radio Frequency Channel Number
AGC Automatic Gain Control
ASIC Application Specific Integrated Circuit
AWG Arbitrary Waveform Generator
BeCMOS Bipolar-Enhanced CMOS IC technology
BiCMOS Bipolar-CMOS IC technology
BJT Bipolar Junction Transistor
BS Base Station
BSS Base Station System
CDMA Code Division Multiple Access
CCI CoChannel Interference
C/I Carrier to Interference ratio
CLPC Closed-Loop Power Control
CMOS Complementary Metal-Oxide-Semiconductor (IC technology)
CMR Common Mode Range
CMRR Common Mode Rejection Ratio
CS Cellular System
DC Direct Current
DCS Digital Communication System (wireless; operating at around 1.8 GHz)
DRX Discontinuous Receive (reception mode of MS)
DS/CDMA Direct-Sequence Code Division Multiple Access
DTX Discontinuous Transmit (transmission mode of MS)
DUT Device Under Test
ERP Effective Radiated Power
ESD ElectroStatic Discharge
ESR Effective Series Resistance
ETSI European Telecommunications Standards Institute
EWS Electrical Wafer Sort
FDMA Frequency Division Multiple Access
FET Field Effect Transistor
FH Frequency hopping
FL Forward Link
FSK Frequency Shift Keying
FT Final Test
GMSK Gaussian Minimum-Shift Keying
GSM Global System for Mobile Communications (originally: Grope Spéciale Mobile)
GTS Global system for mobile communications Technical Specification
IC Integrated Circuit
IF Intermediate Frequency
ISM Industry-Scientific-Medical (frequency band(s) allocated for these applications)
IEEE Institute of Electrical and Electronics Engineers
LDO Low Drop-Out linear voltage regulator
LNA Low-Noise Amplifier
LO Local Oscillator
MAS Micro Analog Systems OY
MIM Metal-Insulator-Metal (capacitor)
MPW Multi-Project Wafer
MS Mobile Station
OLPC Open-Loop Power Control
PAC Power Amplifier Controller
PC Power Control
PCB Printed Circuit Board
PCS Personal Communication System (wireless; operating at around 1.9 GHz)
PLL Phase-Locked Loop
ppm parts per million
PSK Phase Shift Keying
PSRR Power Supply Rejection Ratio
PTAT Proportional To Absolute Temperature
RF Radio Frequency
RMS Root of Mean Squares
Rx Receiver; Receive
RL Reverse Link
RMS Root Mean Square
SNR Signal-to-Noise Ratio
SIR Signal-to-Interference Ratio
SR Slew Rate
SS Spread-Spectrum
TCXO Thermally Compensated Crystal Oscillator
TDMA Time-Division Multiple Access
THD Total Harmonic Distortion
Tx Transmitter; Transmit
UMTS Universal Mobile Telephony System
VCO Voltage-Controlled Oscillator
VCTCXO Voltage-Controlled, Thermally Compensated Crystal Oscillator
VGA Variable-Gain Amplifier
WCDMA Wideband-CDMA (see also CDMA)
XO Crystal oscillator

I. Introduction

Since the advent of mobile telephony, the area has seen continuous accelerating growth, which has lead to ever-increasing number of mobile handsets. The versatility and flexibility of mobile communication has made a mobile telephone from a luxury of businessmen to a communication means for everybody in less than a decade.

Enormous R&D efforts are put to the development of mobile infrastructure; both hardware and software; the mobile station has grown from a mere wireless handset to a complicated handheld computer terminal. All the added functions and accessories will however need electrical power to operate. It is very important to ensure that an advance in mobile hardware or software development would not reduce the operating time of the handset.

This leads to a continuous need to reduce the power that is consumed by the circuits in the mobile handset. For that purpose, much work has been done in the area of digital circuit design, employing low-power design techniques, low-power modes and even low-power software design.

The power-hungriest part of any mobile handset is doubtlessly the radio transmitter. The radio power that is output by the transmitting antenna must be recognizable at the receiver, the base station, which could be several tens of kilometers away from the mobile terminal. On the other hand, in a city for example, the base station might be very close to the mobile terminal, with the distance between them changing, when the mobile is in a vehicle. These extremely varying radio propagation conditions will raise the need for some form of control, or ability to adjust the radio power that is transmitted.

Power control of the transmitted radio frequency signal is an important part of energy management infrastructure in the mobile communication environment. Both mobile station and base station must have some means for controlling or adjusting the power that is sent over the air interface. The GSM standard GSM 05.05 [8] and technical specification GSM 05.08 [7] define this rather complicated power control protocol, defining the necessary radio channel measurements and the algorithms that are employed in both mobile and base stations.

The first part of this Thesis, comprising of Sections II, III and IV, concentrates on radio power control hardware development in the mobile station side of the GSM wireless communication system. The development work bases on a need to integrate several discrete components on the PCB comprising the power control loop hardware to one integrated circuit. This will reduce the component count, required PCB area, power consumption and ultimately the price of a mobile handset.

The second part of the Thesis, consisting of Sections V and VI will handle other power consumption-related problem – namely, the high-precision reference clock signal generation in the mobile phone. The high-precision clock signal is of vital importance in all communication, lest the wireless one. Precise clock is required both for accurate timing between the mobile and base stations, the radio carrier signal generation, modulation, frequency hopping and baseband signal processing. Literally, there is no building block in the modern mobile phone that does not require high-precision reference clock.

Presently, the high-precision reference clock is generated using separate reference resonator, usually a quartz resonator. The thermal compensation and offset trimming circuitry for this quartz resonator and the oscillator core consumes presently rather large amount of power. There is however another clock signal needed in a mobile phone, which is required to run all the time – the real-time clock. It usually makes use of a lower-frequency quartz resonator that has different

temperature behavior than its higher-frequency counterpart and a price that is about one-tenth of that of the high-frequency quartz. Due to lower frequency, also the current consumption of such oscillator is considerably lower.

The aim of the second part of this work is to solve the problem of using the lower-frequency (real-time clock) quartz oscillator for replacing the reference oscillator. It is normally higher-priced, larger in size and more power-hungry than its low-frequency counterpart. This involves developing a new scheme for thermal compensation, the phase-locked loop for frequency up-conversion and verifying the design by computer simulation. Due to the space limitations, only the thermal compensation circuit design and verification is handled in this Thesis.

I.1. Description of the work and Thesis structure

In Section II, the practical implementation of a power control system will be presented along with the design of the integrated circuit implementing part of power control system. In this section, also the measurement results from laboratory are presented. Section II.2 describes the design of specialized operational amplifier to be employed in the power control chip and the results of its measurements. Section III deals with power measurement techniques, using novel techniques that had never been used before in the used technology. In addition, some aspects of the thermal compensation for the power detector circuitry are given in this section.

Section IV handles the practical design of a power detector. It is also aimed at the reduction of the discrete component count in the mobile phone.

All the sections laid out above include elements of system-level and circuit design, integrated circuit layout design and laboratory measurements. The design of power controller chip described in Section II has been carried through product pre-qualification phase of Micro Analog Systems OY and is ready for the commercial production. The integrated circuits that are designed as described in Sections III and IV are also fabricated and measured.

The subject of Section V is precision thermal compensation circuitry design for a crystal oscillator. This section addresses the same objectives as the previous, namely, reducing the component count in mobile phones and other wireless communication devices, such as tyre pressure monitors. Section VI verifies the thermal compensation system-level and circuit-level designs via statistical simulations.

At the end of the Thesis, the list of recommended literature references is given. This section is divided into two parts – the cited references used in writing the Thesis and recommended references for readers who are interested in the subject in depth.

I.2. Objectives and scientific novelty

For the power control part (Section II):

1) Reducing the discrete components count in the RF part of the GSM mobile phone by integrating these onto a silicon chip;
2) Reducing the cost and design time of the PCB of the mobile phone;
3) Reducing the current consumption of the mobile phone;
4) Designing and testing the PA Power Control chip and preparing it for the mass production.

For the RF power measurement part (Sections III and IV):

1) Seeking for integrated-circuit-compatible methods of reliably measuring the RF power without using external Schottky diodes;
2) Evaluating capability of the MAS9 IC technology from the point of view of RF power detection/rectification;

3) Preparing the RF power detector for integration with the designed PA power control chip.

For the crystal oscillator part (Sections V and VI):

1) Investigating the possibility to generate a high-precision reference clock using only a low-frequency (clock) quartz crystal and identify the system requirements;
2) Designing a thermal compensation circuit for the low-frequency XO;
3) Verifying the design using statistical simulations;
4) Integrating the system on silicon and measuring its performance.

I.3. Acknowledgements

This Thesis was mostly financed by Micro Analog Systems OY, Espoo, Finland. Author is most grateful to the company for providing resources to complete the Thesis. All the chips designed in the framework of this Thesis were fabricated in MAS OY, and their laboratory was used for making measurements.

Best thanks to my family for their support and understanding during the period of my PhD studies

Many thanks to patient colleagues from Micro Analog Systems OY and Analog Design Ltd. for their support and understanding.

II. Practical implementation of TX power control chip for GSM mobile phone

II.1. Specification

The power controller was initially specified as a schematic drawing. The schematic consisted of discrete components and the task was to design an IC that would reduce the total count of components on the PCB of the mobile phone. As an additional requirement, also a low drop-out (LDO) regulator was specified to be integrated. Several power-saving modes are specified. The chip to be designed needed to have three separate power-down control inputs that select among the operating modes of the IC. These modes and the states of the three inputs are listed in the Table 1 below.

Table 1. Power Control IC operating modes

VRCTRL – Voltage Regulator ConTRoL (shutdown of LDO); ENREF – ENable REFerences (regulator 'warm-up' mode); TXEN – Transmit ENable. All inputs are CMOS logic inputs. Postive logic is applied.			
VRCTRL	ENREF	TXEN	Result:
0	**0**	**0**	**Total power-down**
0	*****	**1**	**Only PAC works**
0	**1**	**0**	**'Warm-up' for references**
1	*****	**0**	**Only regulator works**
1	*****	**1**	**Everything works**

As both PACTL power control block and voltage regulator use the voltage and current references, these will be switched on as either VRCTRL or TXEN goes high, regardless of the state of ENREF. The mode where ENREF = 1 and PACTL = VRCTRL = 0 is used for preparation of fast start-up of the PA controller and the voltage regulator. The startup of the voltage and current reference generation blocks takes several tens of microseconds, which is too slow in some cases. The 'warm-up' mode ensures that the reference block outputs are correct and the startup of the regulator and power controller will occur at the required speed.

The RF power controller must be compatible with the GSM and DCS1800 standards and must assure enough precision to fulfil the requirements by GSM standards. The power levels for both bands (900 and 1800 MHz) are listed in GSM 05.05 [8] and are copied here for convenience:

Table 2. GSM900 radio output power levels

GSM 900			
Power control level	**Nominal Output power (dBm)**	**Tolerance (dB) for conditions**	
		normal	**extreme**
0-2	39	±2	±2.5
3	37	±3	±4
4	35	±3	±4
5	33	±3	±4
6	31	±3	±4
7	29	±3	±4
8	27	±3	±4
9	25	±3	±4
10	23	±3	±4
11	21	±3	±4
12	19	±3	±4
13	17	±3	±4

14	15	±3	±4
15	13	±3	±4
16	11	±5	±6
17	9	±5	±6
18	7	±5	±6
19-31	5	±5	±6

Table 3. DCS1800 radio output power levels

DCS 1 800			
Power control level	**Nominal Output power (dBm)**	**Tolerance (dB) for conditions**	
		normal	**extreme**
29	36	±2	±2.5
30	34	±3	±4
31	32	±3	±4
0	30	±3	±4
1	28	±3	±4
2	26	±3	±4
3	24	±3	±4
4	22	±3	±4
5	20	±3	±4
6	18	±3	±4
7	16	±3	±4
8	14	±3	±4
9	12	±4	±5
10	10	±4	±5
11	8	±4	±5
12	6	±4	±5
13	4	±4	±5
14	2	±5	±6
15-28	0	±5	±6

LDO regulator was specified to have 2.8 V, 50 mA. Thermal protection and short-circuit protection were also required.

The LDO output voltage along with the dropout voltage determines the lower limit of the supply voltage for the IC, in this case, 3 V. The maximum supply voltage is determined by the IC process and is 5.5 V.

II.1.1. Design flow

The design of GSM power controller was done by replacing and by need rescaling the individual discrete components of a given power controller schematic with one integrated component. As a next step, the exact behaviour of the system was investigated by simulations with Eldo. Also the power amplifier control characteristics were measured and modelled by macromodels that will be explained in details in the following subsection. Then the system model was assembled and simulated to verify its operation. Then, a prototype IC was designed and fabricated. After that, the IC operation was measured in the laboratory in many aspects, with results presented later in this Section.

II.1.2. Power amplifier model and PA control loop

This subsection derives and compares two methods of the GSM mobile station RF power amplifier (PA) control curve $P_{OUT}=f(V_{APC})$ approximation, which is needed for designing the PA control loop. Approximation functions are presented and comparison between simulation and measurement results of the designed PA control chip is made.

Two approximation methods of the power control curve of a GSM mobile phone radio power amplifier are discussed. First, the model of the PA control loop is briefly explained and the PA

control IC chip designed by the author is shortly described. Next, the measurement results of the controlling characteristic of a commercially available PA are presented and the system-level empirical approximation of the control curve is derived. Along with this, the physically meaningful model of the PA control curve is extracted. Then the simulation and measurement results of a PA control chip designed by the author are compared, for both approximation methods. Finally, a conclusion on modelling the PA control curve and the problems in the simulation is drawn.

II.1.2.1 System model of PA control loop

The objective of the power control is to compensate for the radio wave propagation artifacts such as fading, shadowing and also for the distance attenuation [8]. The power control helps reducing pollution of the environment with unneccessary radio power, increase the battery life in handheld phones and avoiding the jamming of the receivers of the other subscribers in the cell area and also the base station receiver [8], [153].

The power amplifier dissipates the most in the handheld phone and the power levels are quite high, reaching up to several watts. The supply current of a typical commercially available RF power amplifier goes up to 3.5 A, with the efficiency around 50% [165], [166], [167], [168], [171], [174], [175]. This results in excessive heating of the power amplifier. Heating in turn causes the change in the control characteristics of the PA. This change is very difficult to track with the digital circuitry, from which the power control command comes in form of a voltage level. In each case, maintaining the correct power level implies the presence of a feedback, either in form of measuring the temperature of the power transistor in the PA or measuring the output power [177], [178], [179]. In this work, the power measurement is used, since the temperature measurement is difficult to implement and inaccurate when the PA does not have the integrated temperature measurement capabilities. Output power measurement is also better in the sense of using PAs of different manufacturers– power measurement is independent of the arhitecture of the PA, while the temperature measurement might not be. The internal construction of PA is assumed to be unknown.

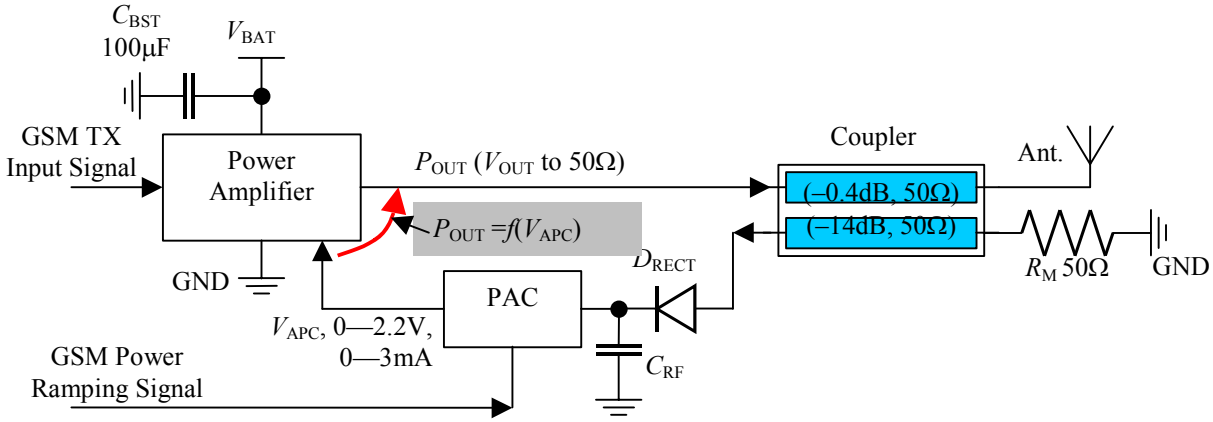


Figure 1. System-level model of PA control loop

The principle of controlling a RF PA is shown in Figure 1. The PA is fed directly from the battery of the handheld phone due to its large current consumption. The capacitor C_{BST} is a boost capacitor and provides the necessary peak current to the PA at the time of switching transients. The amplified GSM transmit signal P_{OUT} is fed to the directional coupler and through it to the antenna of the handheld phone. From the coupler, the 14 dB attenuated output power signal is retreived and fed to the peak detector consisting of D_{RECT} and C_{RF}. The resistor R_M at the decoupled output of the directional coupler is for matching purposes. The rectified signal, which essentially is the peak voltage of the measure of the output power fed to a 50-Ω load is

then inserted to a block marked 'PAC' (Power Amplifier Controller) on Figure 1. The PAC provides the PA with a power control signal necessary for maintaining the desired PA output power, independent of temperature and battery voltage. The output power level is provided from the digital part of the mobile phone in form of a voltage pulse, which has the length of the GSM transmit burst and duty cycle of 1:7. Normally, the length of the burst is 576 µs. The power level is controlled in 2 dB steps for output power levels from 5 dBm to 39 dBm ([8], Table 2 on page 12). The PA in use in this work is capable of providing output power of 34 dBm at nominal supply voltage of 3.5 V [165] – [175]. For further information on construction of PA control loops the interested readers are referred to [81], [182], [183] and [184].

The following discussion goes on approximation of the non-linear power control function of the PA, indicated as a function $P_{OUT}=f(V_{APC})$ in Figure 1.

II.1.2.2 PA control curve measurement and approximation

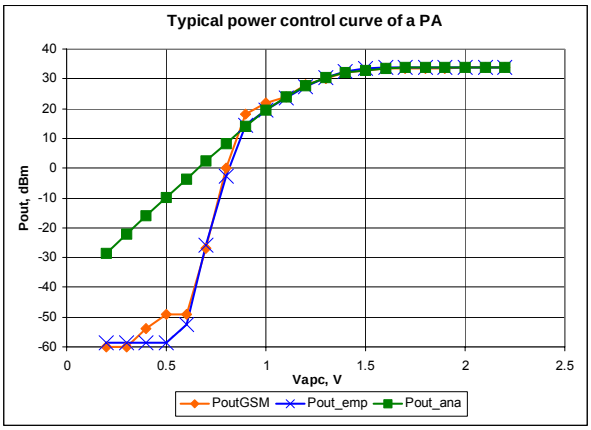


Figure 2. Measured and approximated power control curves

The PA control curve was measured point by point using a fixed-ouput-level RF generator and spectral analyzer. The curve was measured in continuous power mode, which at higher power levels resulted in substantial heating of the PA module. The voltage V_{APC} was changed and the PA output power in dBm was measured. In measurement setup, the PA was measured alone, without any feedback loops.

The measurement results are shown as a graph named PoutGSM in Figure 2.

II.1.2.3 Empirical model

As for the circuit-level simulations of the PAC, the approximation of the control curve PoutGSM from Figure 2 is necessary. First, it was decided to derive a simple mathematical approximation of the curve, following the knees of the curve.

The empirical model is a module of a function with one zero and two poles:

$$f(x) = L\sqrt{\frac{x^{80}+z_1^{80}}{\left(x^{60}+p_1^{60}\right)\left(x^{20}+p_2^{20}\right)}};\quad \begin{cases} z_1 = 0.58 \\ p_1 = 0.88 \\ p_2 = 1.4 \end{cases}, \tag{1}$$

In the model (1), the argument x takes real values of V_{APC}. Since the change of the power control function is quite rapid, the order of the function is high. The locations of the zero and the poles are found by visual inspection – when the two curves were 'close enough' to each other, the root locations of the complex function were frozen. The multiplier L is the value of the highest PA output power level, measured in mW. Here, L=34 dBm=2511 mW. However, for the sake of simplicity, the function does not employ any time delay or memory. It means, that the change in the argument is instantaneously propagated to the function. This is physically

justified, since the PA controller is much slower than the PA, and the effect of the lack of the delay modelling is evaluated in the simulation and measurement results comparison section. The graph of the empirical approximation function (1) is shown as curve named Pout_emp in Figure 2.

II.1.2.4 Alternative model of the PA control curve

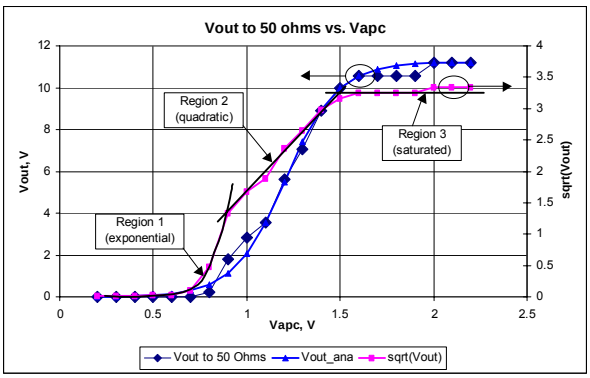


Figure 3. Regions of PA control curve

It can be noticed from Figure 3, that the power control curve of the power amplifier resembles in high degree to the transfer characterstic of a MOS transistor. It has three clearly distinguishable regions. These regions are best observed when the square root of the PA output voltage is plotted versus control voltage V_{APC}: trace sqrt(Vout) in Figure 3.

Note, that the output power is converted to output voltage to the 50 Ω load V_{OUT} and plotted on linear *y*-axis in Figure 3, as opposed to the curves in Figure 2, which are in the units of power (dBm) and thus the scale of the *y*-axis is logarithmic.

First, from $V_{APC} = 0$ V to 0.9 V, the curve resembles most to exponential function. From $V_{APC} = 0.9$ V to 1.5 V, the square root of the function is straight line, which implies the function to have quadratic behaviour. On V_{APC} values above 1.5 V, the curve saturates. These regions correspond to respectively subthreshold, linear and saturation region of a MOS transistor. The analytical function is as follows:

$$f(V_{APC}) = \frac{A}{2}(1+\tanh x) = A\frac{e^x}{e^x+1} = A\frac{1}{1+e^{-x}};$$
$$x = \frac{V_{APC}-V_{TH}}{V_T};\ \begin{cases} A = 11.22 \\ V_{TH} = 1.207 \\ V_T = 0.14 \end{cases}, \qquad (2)$$

The approximation function (2) has actually only one knee and is plotted as graph named Pout_ana on Figure 2. The second knee can be obtained by introducing other parameters to the argument function $x=g(V_{\mathrm{APC}})$ in some V_{APC} region, making thus the function x piecewise linear. The limited space does not allow for deeper discussion of this question.

In alternative control curve model (2), the parameter A represents some transconductance-related parameter of some internal transistor or group of transistors of the PA. V_{TH} can be interpreted as threshold voltage, and V_T as thermal voltage. In circuit-level simulations, the parameters were not changed, as the improvement of the approximation occurs only on low power levels, which are relatively unimportant in this work.

II.1.2.5 Comparison between simulation and measurement results

A 2-µm bipolar enhancement molybdenum-gate CMOS IC process was used for the realisation of the PA controller chip. This technology has very high-quality passive integrated

components – resistors and capacitors, all suitable for the integration so that there is no need for external discrete components.

The chip has in total 17 input-output pads and its size is 1980 µm × 1860 µm. The measurements were carried out with the whole PA control loop, as indicated in Figure 1.

The simulations were carried out with the circuit model of the PAC and the two derived control characteristic models derived above. The PA control curve models were realised in form of voltage controlled current sources with transconductance functions as in expressions (1) and (2).

There were some difficulties in performing the simulations. First, most noticeably, the carrier frequency is 900 MHz (used in all simulations), resulting in very large number of data points even when the simulation time was short. Due to that, the simulations took quite a long time to perform (several hours) and consumed large amounts of computer memory.

For the sake of simplicity, the ramping voltage step of 0.5 V was used for both simulations and measurements. The supply voltage of 3.5 V was used. The rising and falling edges were captured with a digital oscilloscope and the signals were enveloped during 100 pulses of power ramping voltage to get the picture of the RF signal packet growing and diminishing. The signals from the oscilloscope were plotted on the same graphs as the simulation results. The simulation and measurement results for the rising edges of the V_{RAMP}, V_{APC} and V_{OUT} are plotted in Figure 4, and the falling edges of the respective signals are shown in Figure 5.

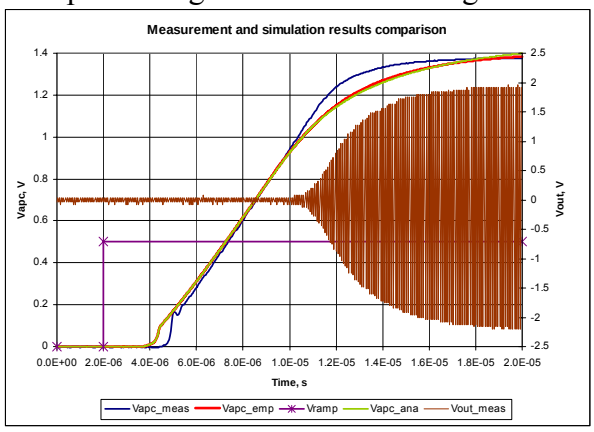


Figure 4. Comparison between simulation and measurement results: rising edge

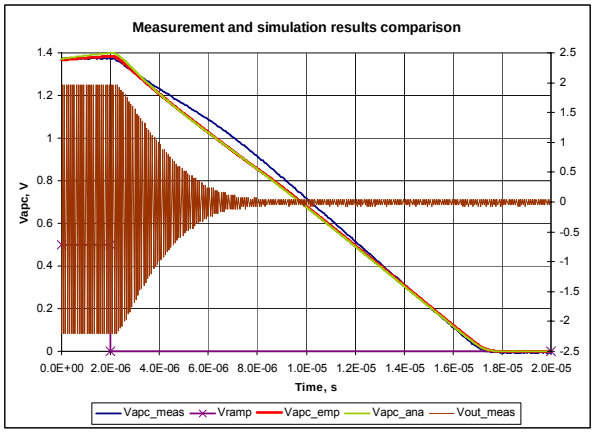


Figure 5. Comparison of simulation and measurement results: falling edge

Both approximations work well as PA control function models, as can be seen from Figure 4 and Figure 5. The difference of the controlling voltages were taken between the simulation results for both rising and falling edges of power ramping signal. The differences are shown in Figure 6, with curve Vdiff_rise showing the difference in rising edge and Vdiff_fall for the

falling edge. It can be observed that the difference of V_{APC} caused by using two distinct approximations is everywhere below ±20 mV. The difference is less than 1.5% of the V_{APC} swing.

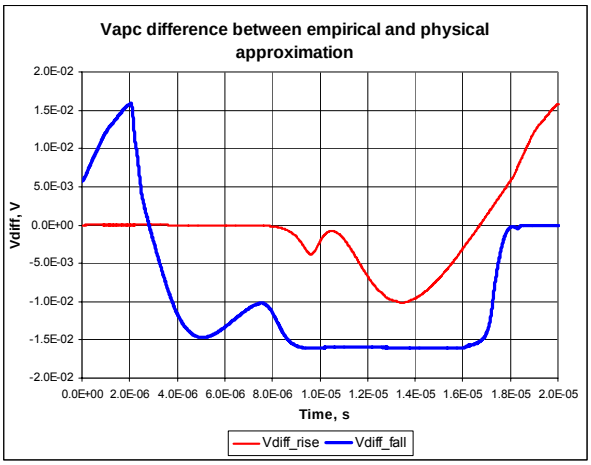


Figure 6. Difference between the two approximations

II.1.2.6 Results of modelling PA control curve and the control loop

Two approximations of the PA control curve were derived and verified with PA control loop circuit-level simulations and measurements. The measurements were carried out with the developed PAC chip and with commercial PA, directional coupler and RF rectifier. The comparison of circuit-level simulations with the measurement results showed good agreement. The differences in the simulation and measurement could be caused by a number of reasons – first, the PA control model was based only on one set of the measurements. Also, due to technical reasons, the wires to the rectifier diodes in the measurement setup were quite long (approximately 8 cm) and thus might have been contributed to the parasitic inductance in the circuit. The slight differences between simulation and measurement results could be also justified as the presence of phase shift in real PA power controlling function, which was not modeled.

The final conclusion is: both PA control curve approximation methods are reasonable and present no numerical difficulties for the circuit simulator. Sometimes it is not feasible to search for a physically meaningful model of an object, it is enough to have a set of measurement results on the object. In this particular case, the dynamic properties of the control function were not included into the model, but this was justified by the fact that the PA is much faster than the rest of the control loop. Its contribution to overall dynamics of the control loop is thus negligible.

II.2. Operational amplifier design

In MAS9142A power controller, a high-performance operational amplifier (OA) is needed. It must fulfil all the specifications of its discrete counterpart on the original schematic. In this Section, the OA design for the power amplifier controller will be briefly presented. The schematic design methods and schematic topologies will not be detailed.

The design bases on the previous experience and literature, see e. g., [195], [196], [207], [196], [197], [198], [199], [205], [206], [209], [210], [211].

II.2.1. Specification

Low noise, heavy load, rail-to-rail output operational amplifier with power-down feature was designed. The technology is 2.0 μm linewidth molybdenum-gate MAS9T twin-well BeCMOS process with 10 kΩ thin-film resistors, high-density metal-insulator-metal type (MIM) capacitors

and bipolar transistors. The OA has been processed on the MAS2602 MPW run. Maximum drive capability is C_L=200 pF, I_{load}=±5 mA. Required bias current for the operational amplifier is –5 µA. Bias block has to be of PTAT type.

Input common mode ranges from VSS to VDD–0.8 V. Nominal common-mode voltage is designed close to 0 V. All characteristics in the following specification (Table 4) are at room temperature and with 10 kΩ || 10 pF load, if not said otherwise.

Table 4. Specifications of the OA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{DD}		2.8	3.6	6.0	V
Bias current	I_{BIAS}			–5		µA
Supply current	I_{DD}	V_{DD}=3.6 V, V_{CM}=1.8 V	2.4	2.6	2.9	mA
		V_{DD}=3.6 V, V_{CM}=0.01 V	0.74	1.1	1.30	mA
		V_{DD}=3.6 V, V_{CM}=2.8 V	0.83	0.86	1.30	mA
Power Dissipation	P_d	V_{DD}=3.6 V, V_{CM}=0…2.8 V	2.7	4.0	10.4	mW
Current consumption in Power Down Mode	$I_{DD, PD}$	V_{DD}=3.6 V, T=+27 °C		2.0 *1		nA
Power Dissipation in Power Down Mode	$P_{d, PD}$	V_{DD}=3.6 V, T=+27 °C		7.2 *1		nW
Offset Voltage (systematic)	$V_{OS, S}$	V_{DD}=4.5 V, T=+27 °C		0.8 *1		mV
Offset Voltage	V_{OS}	V_{DD}=3.6 V, V_{CM}=1.8 V	-4.9	-0.28	10.3	mV
		V_{DD}=3.6 V, V_{CM}=0.01 V	-4.8	-0.29	9.5	
		V_{DD}=3.6 V, V_{CM}=2.8 V	-63	-33	63	
DC Open Loop Gain	$A_{V, OL}$	V_{DD}=3.6 V, V_{CM}=1.8 V	90	93	97	dB
		V_{CM}=1.8 V no load	90	93	97	
		V_{CM}=0.01 V no load	92	93	95	
		V_{CM}=2.8 V, no load	84	92	118	
Min Input CM Voltage	$V_{CM–}$			0.0		V
Max Input CM Voltage	V_{CM+}			V_{DD}– 0.8		V
Vout min	$V_{M–}$		0	0.05	0.3	V
Vout max	V_{M+}		V_{DD}– 0.09			V
CMRR	CMRR	f=0, V_{CM}=1.8 V	66	76	128	dB
		f=10 kHz *2 V_{CM}=1.8 V	66	72	76	
		f=100 kHz *2 V_{CM}=1.8 V	37	46	56	
PSRR VDD	PSRR+	f=0, V_{CM}=1.8 V	65	74	89	dB
		f=1 kHz *2 V_{CM}=1.8 V	66	72	81	
		f=10 kHz *2 V_{CM}=1.8 V	57	62	67	
		f=100 kHz *3 V_{CM}=1.8 V	24	26	28	
		f=1 MHz *3 V_{CM}=1.8 V	20	20	21	
Unity Gain Frequency	f_U	V_{CM}=1.8 V, no load		5.2		MHz
		V_{CM}=1.8 V, R_L to VSS		5.2		
		V_{CM}=1.8 V, R_L to VDD		5.2		
Gain Margin *1	G_m		5.5		10	dB
Phase Margin *1	φ_m		23		36	deg
Slew Rate , 0.3 – 2.8 V step	SR+	See note *4	0.3	3.2		V/µs
Fall time, 2.8 – 0.3 V step	t_{F-}		0.15	0.39	0.64	µs

Small signal overshoot , 1.25-1.85V step	OS			1.6		%
Small signal undershoot, 1.25-1.85V step	US			0.8		%
Total Harmonic Distortion (unity gain buffer)	THD	f=9 kHz, amplitude 0.5V, offset 1.8 V		–100		dB
Input referred noise voltage (integrated)	$V_{n,\,in}$	High frequency (above 100 kHz)		0.56		mV
		Low frequency (DC-100 kHz)		0.061		
		Low frequency, with mains filter		0.027		
Cell Width	Width	MAS9T, 2µm linewidth		770		µm
Cell Height	Height	MAS9T, 2µm linewidth		386.25		µm
Cell Area	Area	MAS9T, 2µm linewidth		0.297		mm^2

Notes in the table:
[*1] Simulated quantity (not measured); in simulations the load=700 Ω||150 pF
[*2] Input device: BK3105, output device BK3005
[*3] Input device: HP AWG, output device Tektronix TVS621
[*4] Slew rate measurement is not reliable, because due to the construction of the OA, the SR decreases rapidly near the VDD rail.

II.2.2. Design flow

The OAOMA11 operational amplifier is designed for the RF power amplifier control ICs like MAS9142A. There are special requirements for such operational amplifiers. Among others, the input common-mode range must include negative supply rail. The output of the operational amplifier must be rail-to-rail, in power down mode the output must be dragged to VSS, the input impedance must be high and the OA must be able to drive large resistive and capacitive loads. Due to the rather noisy working environment, the OA must have rather high PSRR values to ensure correct operation of the power control loop.

The input stage of the OA is realized as floating-PMOS source follower MIN1, MIN2. Then the bipolar differential input stage Q1, Q2 follows. This configuration shifts the input common-mode range down, to include the negative supply rail. The differential pair Q1, Q2 is loaded by the NMOS folded cascode stage MNFC1, MNFC2. Bipolar current mirror QFM1, QFM2 serves as active load for the folded cascode stage.

The output stage is class-AB and consists of transistors M1-M8. There are two translinear loops involved in the quiescent mode biasing of the output stage, namely M1-M3-M7-M5 and M2-M4-M8-M6. The complete OA schematic is shown in Figure 7. Figure 8 depicts the layout of the test chip which was designed for testing of the OAOMA11.

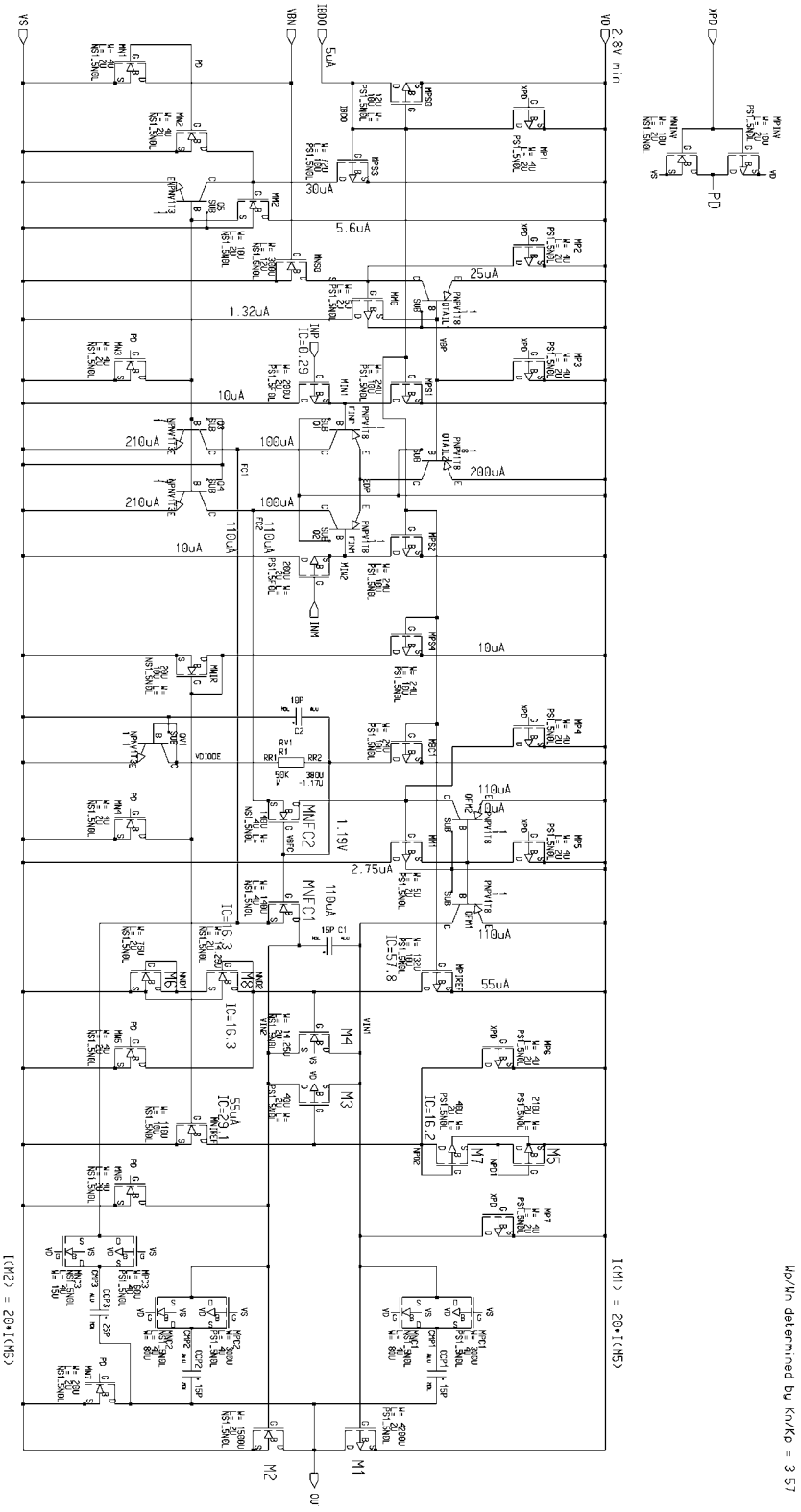


Figure 7. OAOMA11 schematic

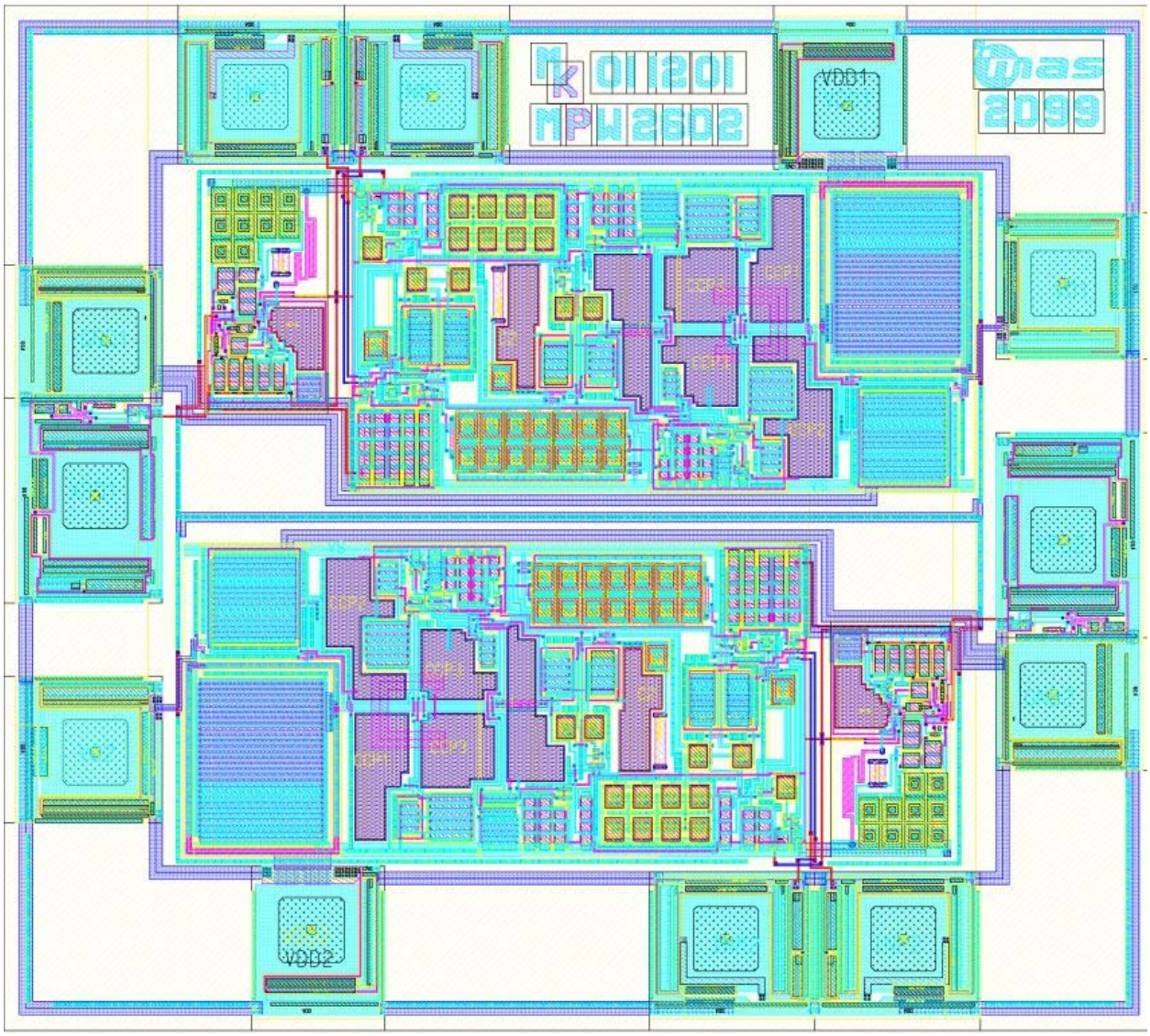


Figure 8. OAOMA11 testchip layout

II.3. Design-for-test

In this section, the needed laboratory and production tests for the power control IC, named MAS9142 are described.

Testing will be done with laboratory test system consisting of IntegraTEST VXIbus-based analog tester and IMS ATS 100 digital tester. Production tests will be done with a Credence STS 5000 production tester.

Laboratory tests will be done for components in SB-20 and TSSOP16 packages.

Temperature protection will be measured up to +180°C.

Temperature sensor shutdown-voltage will be characterized in SB-20 package measuring TEST-pin voltage as a function of temperature.

The toplevel schematics and the block schematics of MAS9142A are shown below.

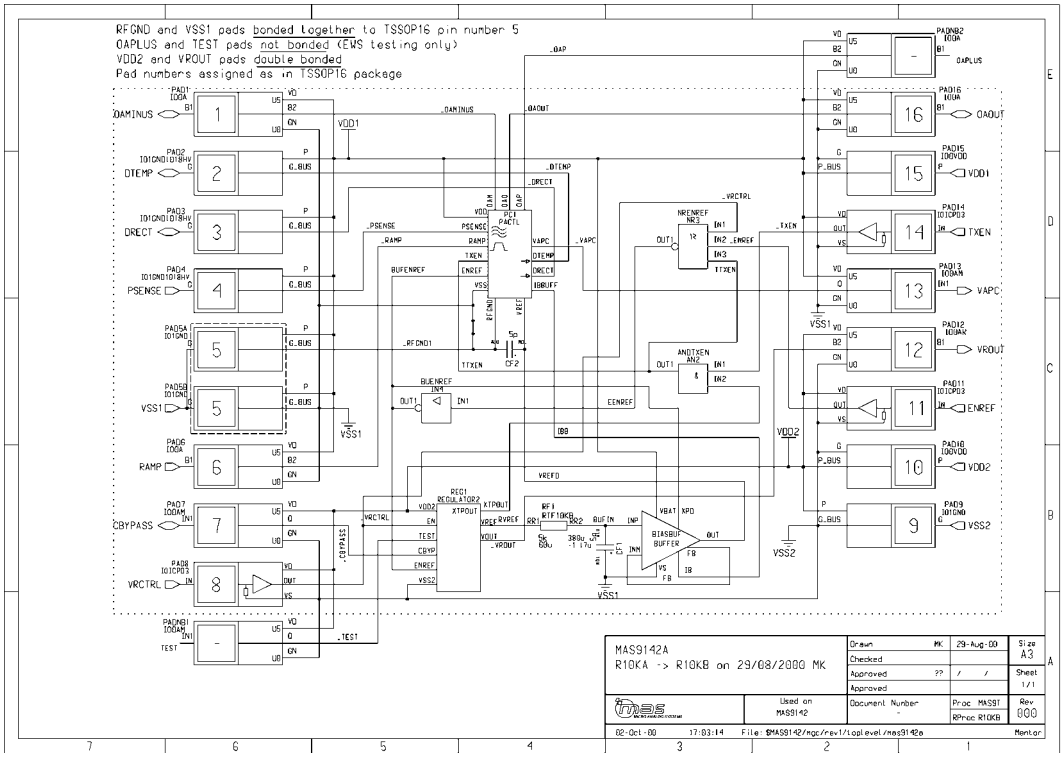


Figure 9. Toplevel schematic of MAS9142A describing pin connections of TSSOP-16 package

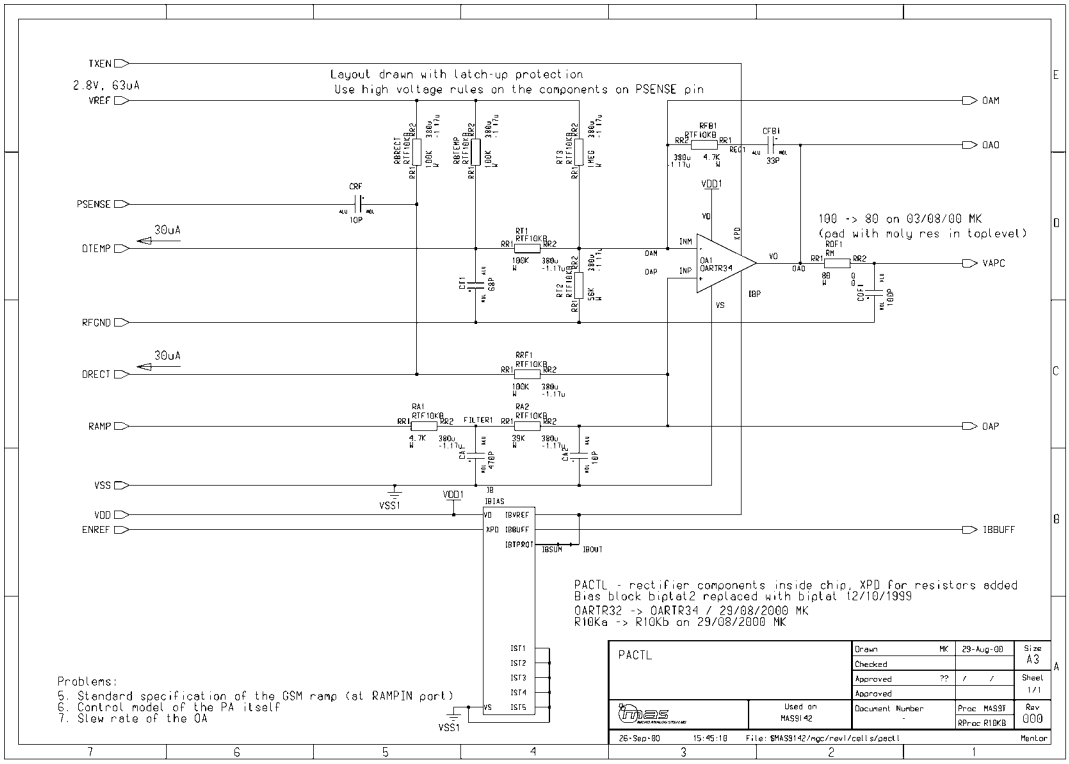


Figure 10. Schematic of PACTL block

The pads named TEST and OAPLUS are not bonded in the production version of the MAS9142A, but they can be used in EWS-testing and testing of engineering samples.

The schematic of Power Amplifier Control block (PACTL) is shown in Figure 10, the chip layout and bonding diagram are presented in Figure 11 and Figure 12, respectively. The voltage regulator (REGULATOR2) schematic is out of the scope of this Thesis and is not shown.

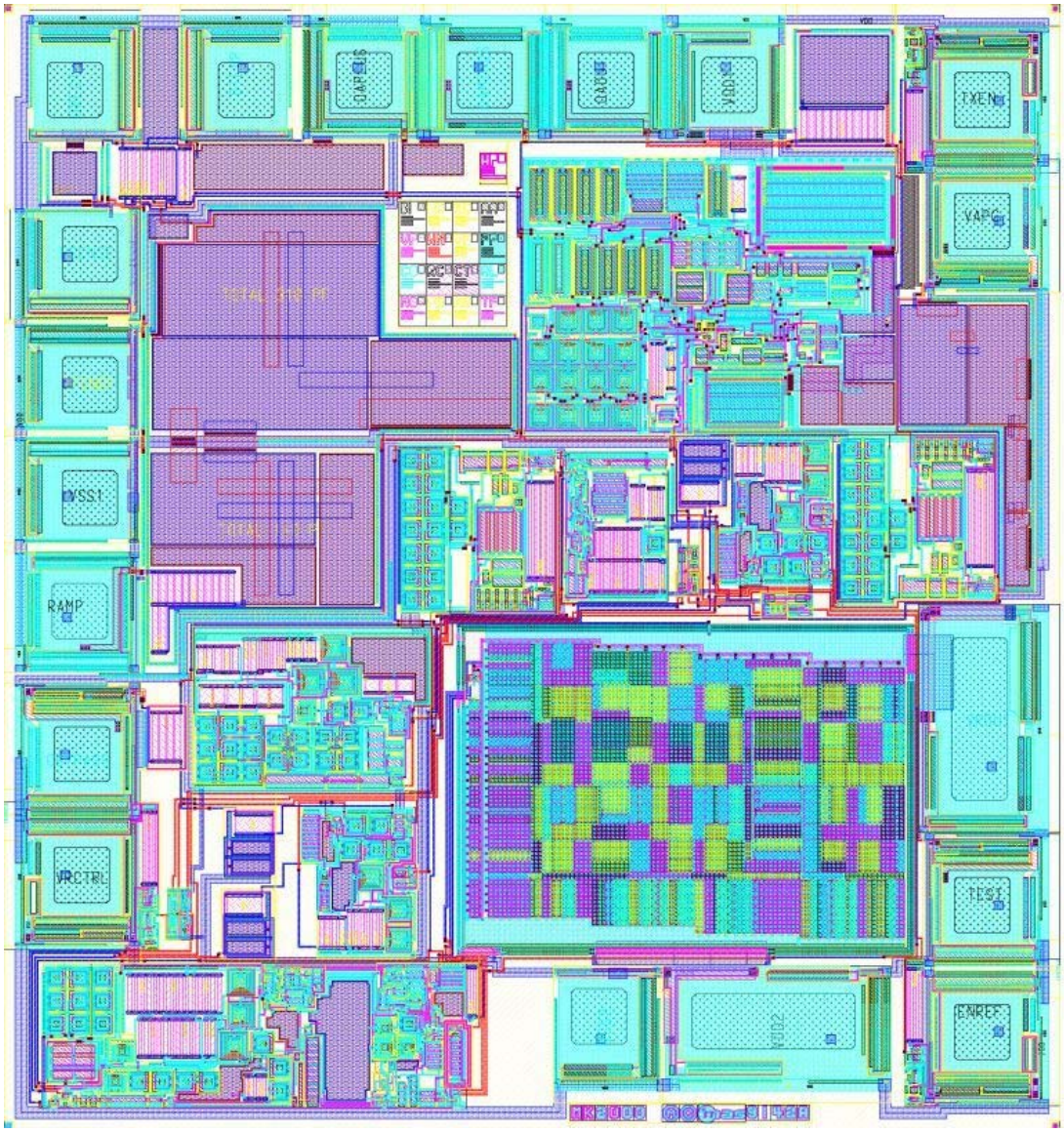


Figure 11. MAS9142A layout

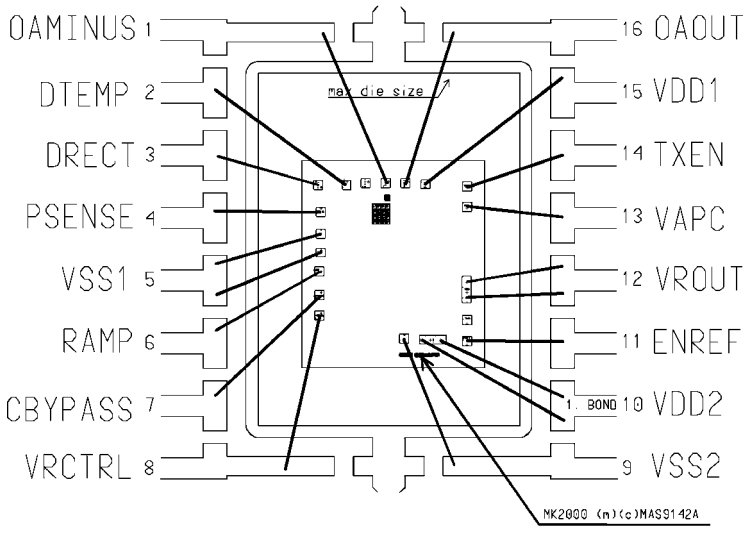


Figure 12. MAS9142A bonding diagram for TSSOP16 package

II.4. Measurement conditions and external components

II.4.1. External components for supply decoupling

Nominal supply voltage for MAS9142A is ***3.6 V***. Minimum is *3.0 V* and maximum is *6.0 V*.

The **VDD1** (pin 15 on TSSOP16) and **VDD2** (pin 10 on TSSOP16) **must be connected together on the *swap card*** (**not** on probe card, see Figure 13).

The **VSS1** (pin 5 on TSSOP16) and **VSS2** (pin 9 on TSSOP16) **must be connected together on the *swap card*** (**not** on probe card, Figure 13).

The decoupling capacitors must be placed as close to the chip as possible:

Connect 1 nF plastic-dielectric in parallel with 68 pF ceramic capacitor between **VSS1** (5) and **VDD1** (15).

Connect 10 nF plastic-dielectric capacitor between **VSS2** (9) and **VDD2** (10) as shown in Figure 13.

The common resistance for the two supply voltages must be as small as possible. It is also recommended to connect a 100 pF decoupling capacitor to the point where the power and ground lines converge on the swap card:

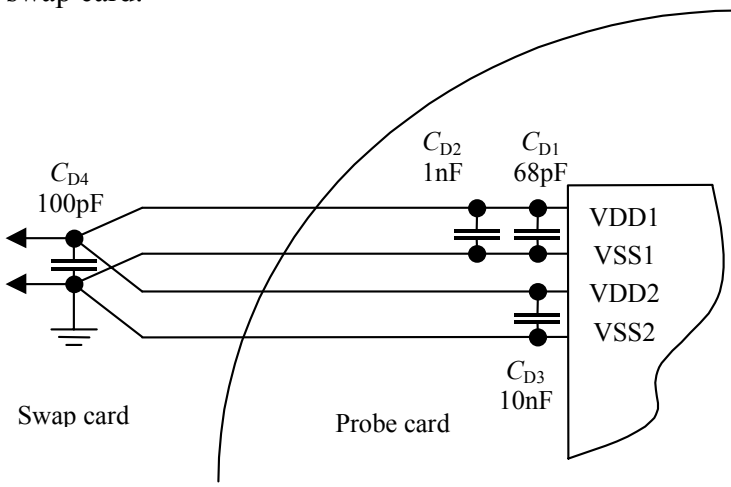


Figure 13. Supply connections and decoupling

The leads of the decoupling capacitors must be as short as possible to minimise the ESR and parasitic inductance.

II.4.2. Other external components

1. Bypass capacitor 100 nF between CBYPASS pin and VSS2 (as close to the chip as possible);
2. Regulator output capacitor 1 μF between VROUT and VSS2 (as close to the chip as possible);
3. Feedback resistor 100 kΩ between OAOUT and OAMINUS pins. This resistor must be programmably removable, i. e., it is necessary to connect it via relay.

II.5. Measurement specification of the PAC

II.5.1. Measurements of the LDO voltage regulator

The regulator is a common MAS voltage regulator with temperature protection and output current limitation. Thermal protection block is shared with the PACTL block. The nominal output voltage of the regulator is 2.8 V; nominal output current is 50 mA.

The testing of the regulator will not be detailed here.

II.5.2. DC measurements

II.5.2.1 Supply current measurements

Supply current consumption should be measured in the five operating modes defined in Table 1 on page 12. The values of the test limits will be specified in Table 5 below.

Table 5. Supply current of PAC in various operating modes.

VRCTRL	ENREF	TXEN	Result:	Current limits
0	**0**	**0**	**Total power-down**	**<5μA**
0	*****	**1**	**Only PAC works**	**0.5…1.3mA**
0	**1**	**0**	**'Warm-up' for references**	**0.12…0.24mA**
1	*****	**0**	**Only regulator works**	**0.22…0.36mA**
1	*****	**1**	**Everything works**	**0.6…1.4mA**

Input current of the digital input pads (TXEN, VRCTRL and ENREF) should be measured in all states. The current at low state should be close to zero and in high state, it could be calculated as $I_{LEAK,H}=V_{DD}/(900\ \text{k}\Omega \pm 30\%)$.

Bias current for the external Schottky diodes must be measured from the DRECT to VSS1 and from DTEMP to VSS1. The test limits are listed in Table 6:

Table 6. Bias currents for Schottky diodes.

Current from DRECT to VSS1	21…40μA
Current from DTEMP to VSS1	23…44μA

II.5.2.2 Voltage measurements

Reference voltage measurement:

1. All external components from DTEMP pin must be disconnected.
2. Put the chip into "reference warm-up" state by applying 0 V to VRCTRL and TXEN, and VDD to the ENREF pin.
3. Wait for 10 ms
4. Measure the voltage at the DTEMP pin respective VSS1 with a high-impedance voltmeter. The voltage must be 1.744 V±5%.
5. Measure voltage at the CBYPASS pin respective VSS2. The voltage must be 2.0 V±5%.

II.5.2.3 Resistance measurements

The power supplies must be connected to the chip to prevent the ESD protection diodes from opening during the measurements. The chip must be in total power-down mode (see Table 5 above).

The resistances that can be measured and their values are listed below. Note that the 30% tolerance must be allowed due to process variations.

1. **VAPC—OAOUT: 100 Ω±30% (tests: ROF1)**
2. **DTEMP—VSS1: 81.3 kΩ ±30% (tests: RBTEMP, RT1, RT2, RT3, buffer feedback resistors)**
3. **DTEMP—DRECT: 139.6 kΩ ±30%, DTEMP connected to VSS1 (tests: RBRECT plus all that are tested in previous test)**
4. OAMINUS—VSS1: 45.3 kΩ**±30%** (tests: RT2 plus all that are tested in test 2.)
5. OAPLUS—DRECT: 100 kΩ**±30%** (tests: RRF1)
6. OAPLUS—RAMP: 43.7 kΩ**±30%** (tests: RA1, RA2)
7. **DRECT—RAMP: 143.7 kΩ±30%, DRECT connected to VSS1 (tests: RA1, RA2, RRF1)**

The tests 1, 2, 3 and 7 are essential; others duplicate some tests on the resistors.

II.5.2.4 DC transfer function measurements

The following is valid provided there is a 100kΩ resistor connected between the OAOUT and OAMINUS pad. All voltages are measured respective to VSS1. The DC transfer characteristic of the PACTL block can then be expressed as

$$V_{APC} = 2.634V_{RAMP} + 1.151V_{DRECT} - 1.000V_{DTEMP} - 0.100V_{REF}, \quad (3)$$

where V_{REF} denotes on-chip reference voltage and is always equal to 2.8 V.

The following points of the transfer characteristic should be measured. In DC transfer function measurements, allow for a tolerance of ±25%.

Table 7. DC transfer characteristics

Force			Measure
DTEMP [V]	DRECT [V]	RAMP [V]	VAPC [V]
0.2	–1.5	1.0	0.428
		1.5	1.745
	–1.0	1.0	1.003
		1.5	2.320
	–0.5	0.5	0.262
		1.0	1.579
	0	0.5	0.837
		1.0	2.154

II.5.3. AC measurements

II.5.3.1 Frequency response measurements

Three frequency responses should be measured: RAMP→VAPC, DRECT→VAPC and DTEMP→VAPC.

The AC source for measurement from the RAMP input must have such DC offset that it would yield 1.8 V voltage at the VAPC pin of the chip and is calculated using formula (3). The DC offsets for DTEMP and DRECT sources are 0 V. For resistor error of 0%, the DC offset for the RAMP pin is 0.79 V, and for a full range of resistor tolerance, ±30%, the required offset voltage is 0.63…0.92 V. The on-chip absolute resistor tolerance can be calculated from all resistor measurements except the OAOUT-VAPC measurement, since between these pins, a molybdenum resistor is used instead of thin-film resistor.

All three frequency responses are low-pass by shape.

The points of interest of the frequency responses are indicated in the three tables below.

Table 8. Frequency response RAMP→VAPC

RAMP→VAPC		
Frequency	Gain	Gain in dB
1kHz	2.704	8.66
10kHz	2.704	8.66
79kHz	1.0	0.0

Table 9. Frequency response DRECT→VAPC

DRECT→VAPC NB! Apply appropriate DC voltage to RAMP pin! (see text)		
Frequency	Gain	Gain in dB
1kHz	1.18	1.30
10kHz	1.13	1.08
26kHz	1.0	0.0

Table 10. Frequency response DTEMP→VAPC

DTEMP→VAPC NB! Apply appropriate DC voltage to RAMP pin! (see text)		
Frequency	Gain	Gain in dB
1kHz	–1.0	0.0
10kHz	–0.975	–0.22
44kHz	$\|0.707\|e^{j136°}$	–3.0

The phase in Table 10 is indicated for reference only. Its measurement is not required.

The allowed tolerance for all of the AC measurements are ±2.0 dB.

II.6. Sophisticated measurements

The following measurements are too complicated to perform in production testing or exceed the capabilities of the production tester. Thus the tests described in this subsection are only performed in the laboratory.

II.6.1. Temperature measurements

Use the Thermonics 2500 Precision Temperature forcing system for application of the temperature to the DUT.

Make temperature measurements with 5 good samples in 5 temperature points: –40°C, 0°C, +27°C, +85°C and +125°C. Use reduced-length laboratory test program for the temperature measurements except for one sample, for which the full-length test program must be used. The shorter labtest program is used to reduce the temperature stress applied to other components on the laboratory PCB.

Measure the functionality of the thermal protection block by sweeping the temperature and measuring the regulator output voltage at the VROUT pin. The thermal protection is engaged when temperature rises over approximately +160°C and will turn the chip on again when the temperature has decreased to about +150°C.

The temperature dependences of the CBYPASS and VROUT voltages could also be measured.

II.6.2. RF crosstalk measurements

Measure the RF cross-talk with 1 good sample and in the following 5 frequency points: 100 MHz, 450 MHz, 900 MHz, 1.8 GHz, 2 GHz. Use bursted RF signal and constant input RF signal amplitude. Take into account that the real voltage on the DUT will be 4 times larger than indicated on the RF generator's display: 2 times for the unmatched transmission line effect and the other 2 times for the 100% amplitude modulation (0% to 200% in amplitude).

Measure the following cross-talk characteristics:

VDD→VROUT;

VDD→CBYPASS;

VDD→VAPC.

The cross-talk from PSENSE pin to VROUT pin must also be measured in the indicated frequency points with two amplitude values: “small” (100 mV) and “big” (2 V). The amplitude values are approximate.

The RF behaviour of the on-chip 10 pF RF decoupling capacitor C_{RF} must be measured. For that purpose, apply the RF signal to the PSENSE pin and measure the RF output level at the DRECT pin.

II.7. RF interference measurement

Laboratory measurement results of MAS9142A on RF-optimized PCB are reported here. The samples in production package (TSSOP16) were measured. The samples were encapsulated from prototype lot 29934.1. Two versions of RF-optimized PCB were made to test the functionality of the internal RF decoupling capacitor of MAS9142A, as specified in Section II.6.2 and to compare the results with the external capacitor.

Two versions of the laboratory measurement PCBs were made for the RF measurements. The only difference between the two schematics is the presence of the RF decoupling capacitor. This capacitor is present on the MAS9142_RF_PCB and missing in the MAS9142_RF_PCB_EXTRA. The two versions of the PCBs were made since the on-chip RF characterstics were not known. The measurement results of the two testboards were compared to evaluate if the on-chip capacitor could be used for RF decoupling in the mobile telephone.

The schematics of the measurement PCBs are shown in Figure 14 and Figure 15 below.

Note that the RF signal is given to different pins on the PCB’s. When the external capacitor is involved, the RF goes through that capacitor to the DRECT (3) pin of the MAS9142A. When the external RF capacitor is not employed, the RF is given to pin 4 (PSENSE) as can be seen from Figure 14. In this case, the internal RF decoupling capacitor is used.

The two buffers on the both PCBs are for the decoupling purposes and serve as decouplers for the excessive capacitive loading presented by the laboratory tester cables. The amplifier with the LM7131 operational amplifier is a feedback for the PA controller and forces the loop to be stable, as there is no on-chip DC feedback for the OA that is on the MAS9142A. It can also be viewed as the “PA model”.

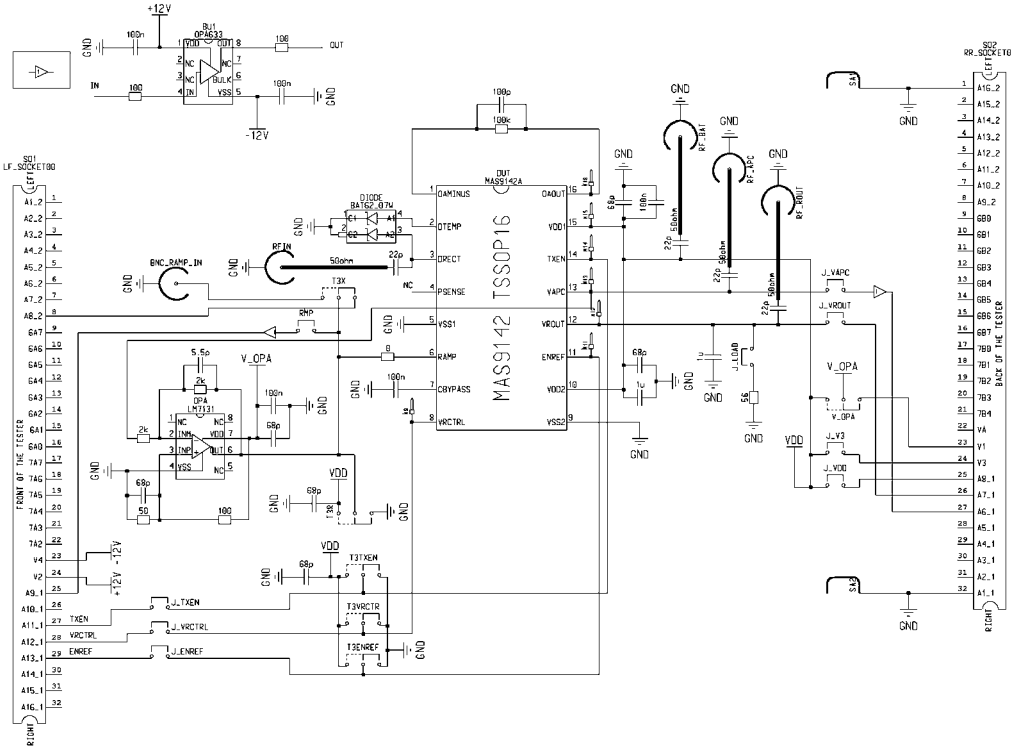


Figure 14. PCB with external RF capacitor

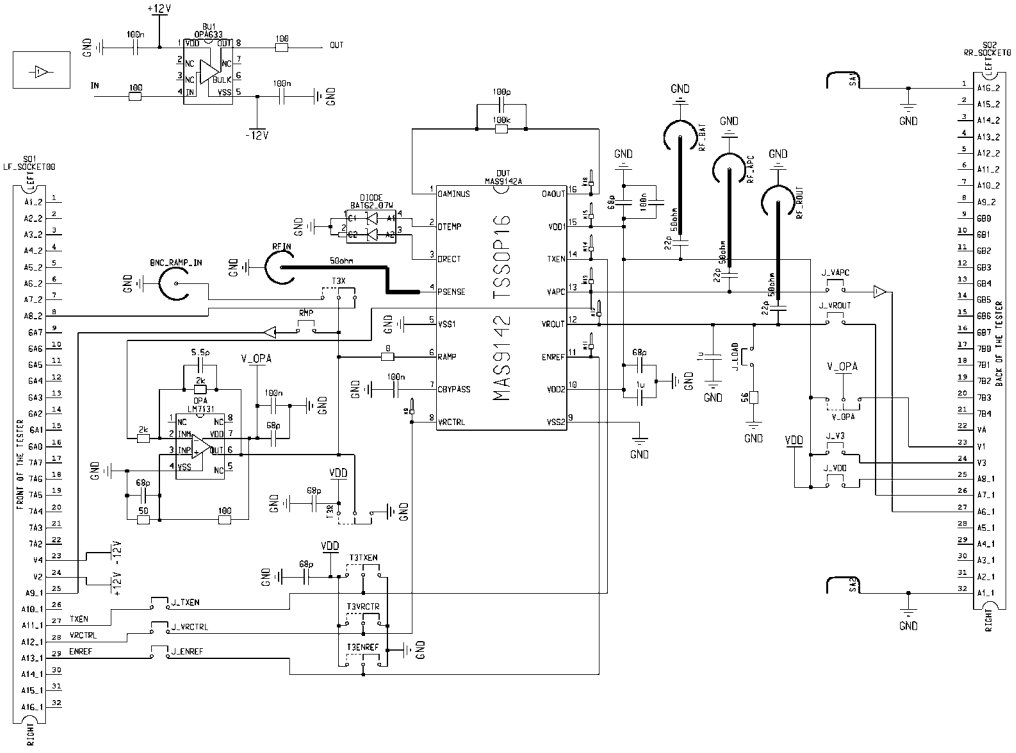


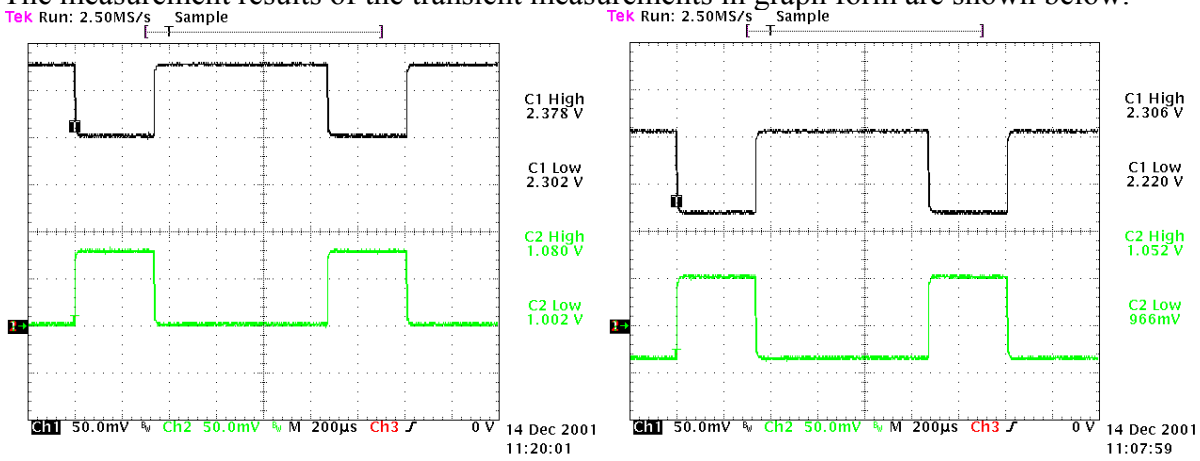
Figure 15. PCB without RF capacitor

MAS9142A RF measurements were done using IntegraTEST laboratory tester, a HP E2000S RF generator and TEK TDS744A four-channel oscilloscope. The temperature was forced using the Thermonics 2500 Precision Temperature Forcing System.

II.7.1. Measurement results

Two types of measurements were performed with the MAS9142 RF PCBs. These were the transient measurements (to evaluate the temporal waveforms at the output of the chip) and sweeping measurements, where RF signals with long duration were used to ensure the steady state of the device under test. Then the amplitude of the RF input signal was swept at 2 frequency points, 900 MHz and 1.8 GHz, from –30 to +10 dBm in 0.5 dB steps. Additionally, the frequency was swept from 100 to 2000 MHz in 10 MHz steps and the RF amplitude was held constant at +6 dBm.

The measurement results of the transient measurements in graph form are shown below.



(a) (b)

Figure 16. Oscilloscope pictures of waveforms on MAS9142: a) with MAS9142_RF_PCB and b) with MAS9142_RF_PCB_EXTRA.

RF frequency in the Figure 16 above is 500 MHz and oscilloscope channel 1 (upper curve on both screen prints) is VAPC signal (pin 13) and channel 2 (lower curve) is RAMP signal (pin 6). 500 MHz, 0 dBm (as read from generator display) pulsed input signal with 1.072 ms period and 336 us duty cycle was used for these measurements.

It can be seen from this figure, that the voltages on MAS9142_RF_PCB are offset by approximately 70 mV with respect to the corresponding voltages on the other PCB, the MAS9142_RF_PCB_EXTRA. This was found to be caused by the mismatching resistors on the PCB, which caused different quiescent DC levels on both versions of the board. It should be emphasized that this offset has nothing to do with the DUT itself, but is caused purely by the test equipment.

The RF frequency response of the MAS9142A was measured at frequencies of 100 MHz until 2 GHz with 100 MHz steps. The input RF level was 0 dBm (at generator display), and the pulsed RF was used as previously. The curves for the PCB and EXTRA are shown in Figure 17.

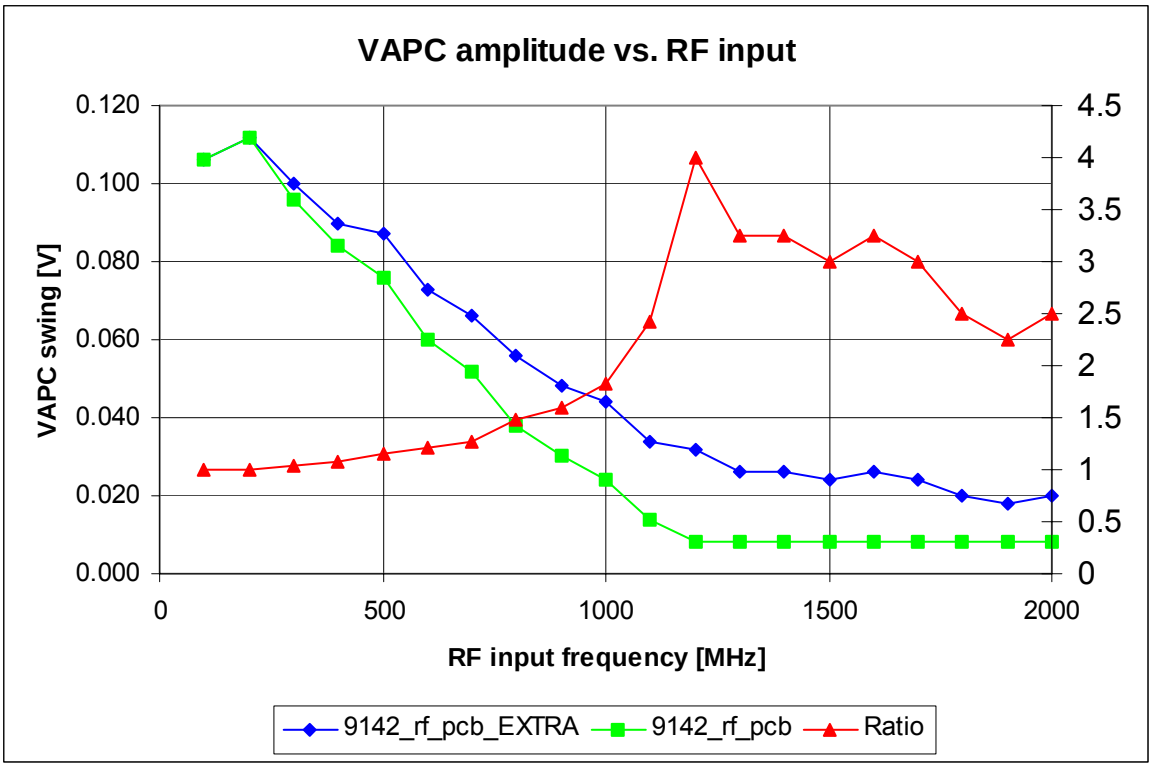


Figure 17. Frequency response of MAS9142A

The difference of the two PCBs is remarkable. The PCB which uses internal RF capacitor of MAS9142 seems to behave much better than the PCB with external capacitor.

The ratio of the two voltage swings is shown as a red line [the line with triangle markers].

In the next experiment, a linear ramp of RF signal with constant frequency was used as the input signal and the RAMP signal was measured as the output signal. The comparative graphs of one period of the RF ramp (averaged with 10 consecutive signal periods) at 450, 900, 1800 and 1900 MHz were measured. The results are shown in figures below.

In Figure 18, the RAMP signals (pin 6) for the frequencies of 450 and 900 MHz are shown. It can be seen from the curves that while at 450 MHz, the amplitude of the RAMP is almost equal for the two test boards, but substantial difference has been developed at already 900 MHz. Figure 19 shows that this is also valid for the frequencies of 1800 and 1900 MHz.

Finally, Figure 20 illustrates the ratios of the RAMP signals at different frequencies. The ratios are taken between the RAMP outputs of the MAS9142_RF_PCB and MAS9142_RF_PCB_EXTRA, the former divided by the latter. The great jitter at very low amplitude levels is caused by the measurement noise. The average ratios are collected into the following table.

Table 11. Average ratios of RAMP signals on different PCBs

At freq. [MHz]	Abs.	dB
450	0.9199	-0.725
900	0.6301	-4.011
1800	0.2583	-11.76
1900	0.3608	-8.85

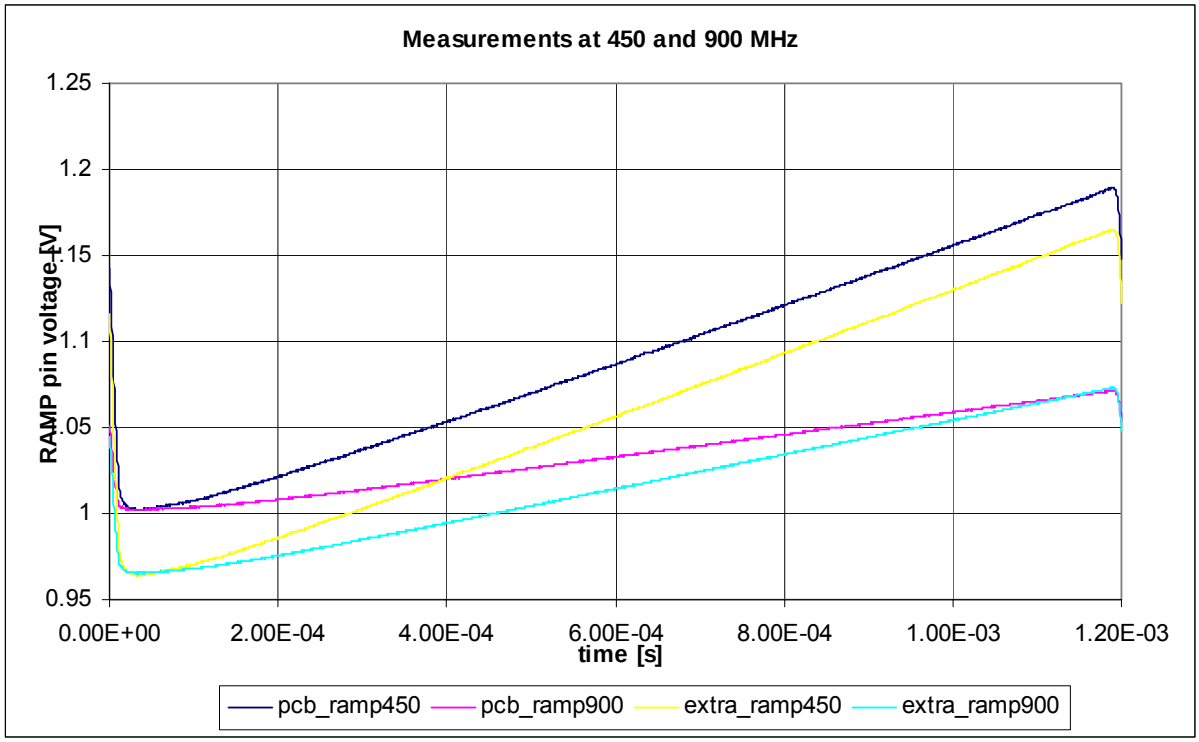


Figure 18. RAMP signals at 450 and 900 MHz

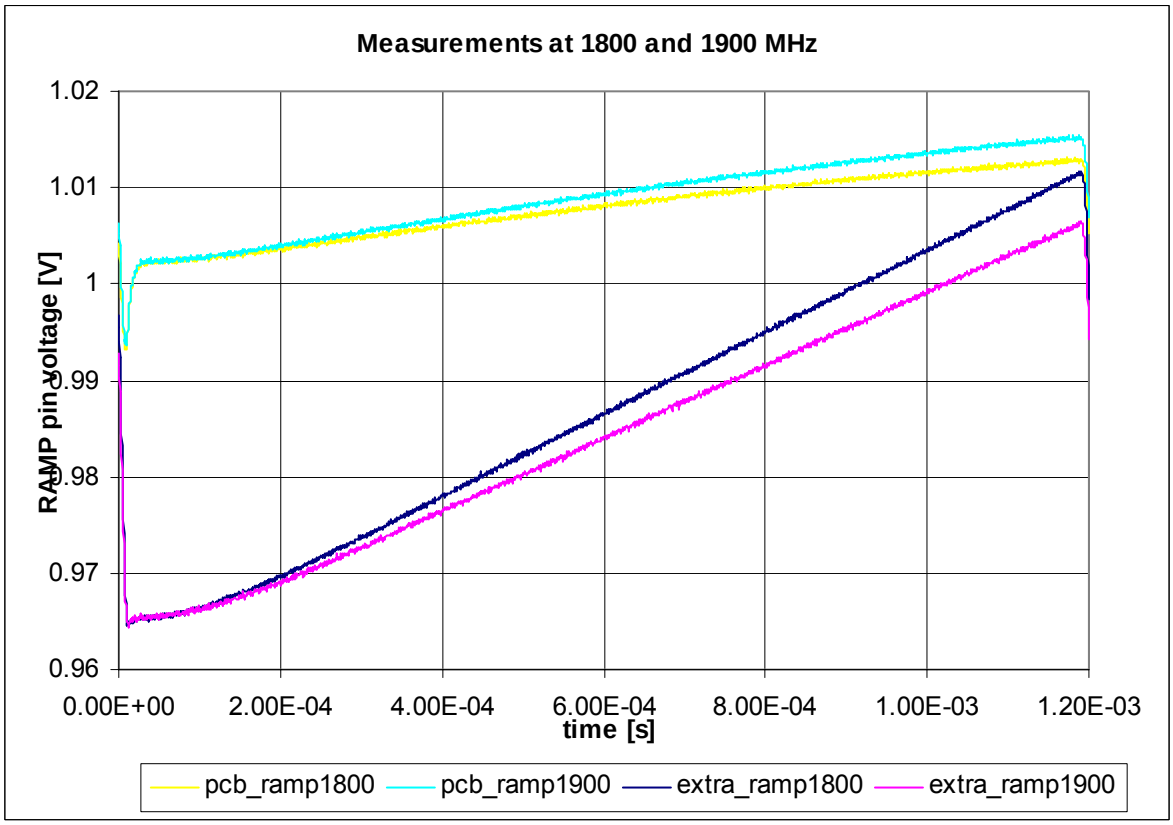


Figure 19. RAMP signals at 1800 and 1900 MHz

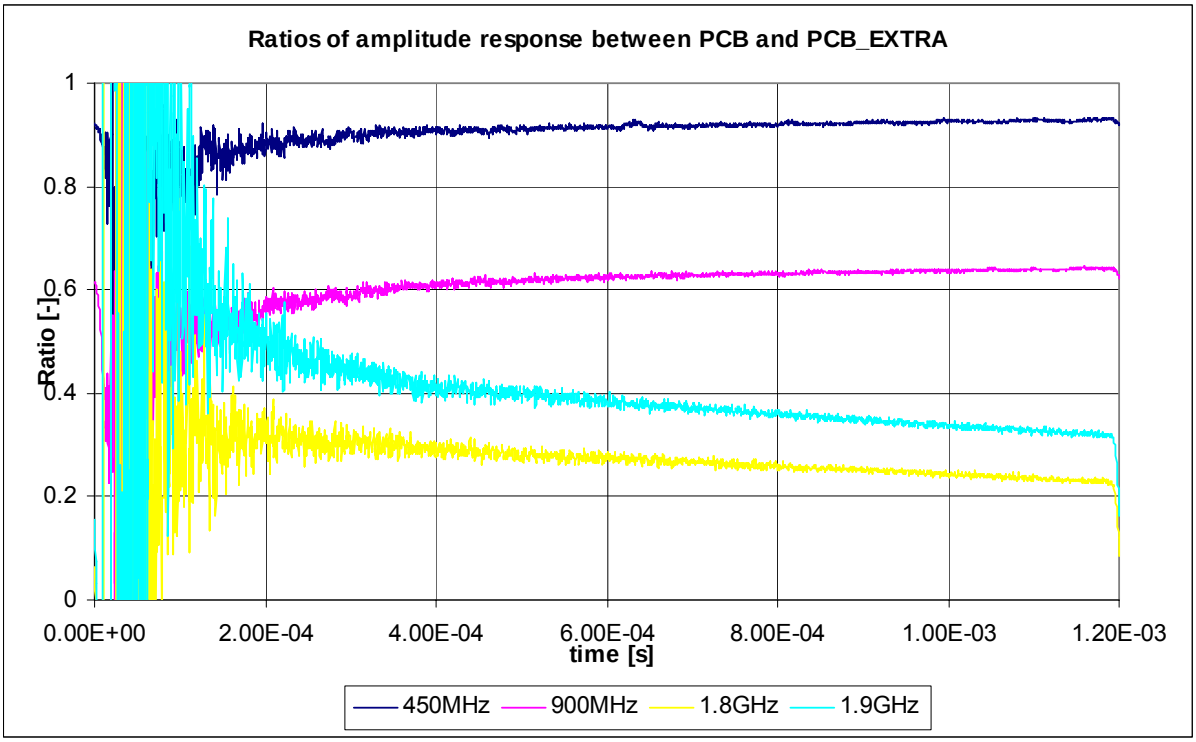


Figure 20. Amplitude ratios at different frequencies

The amplitude of RF signal was swept from –30 to +10 dBm, as read from the RF signal generator display. Two frequency points, 900 MHz and 1800 MHz were measured, and both 9142_RF_PCB and 9142_RF_PCB_EXTRA were measured in three temperature points, namely –40°C, +25°C and +85°C. Measurements at higher temperatures were not possible due to potential thermal damages to test equipment (RF cables).

The closed loop operation of both PCBs was used. The input was at the RF decoupling capacitor (9142_RF_PCB) and the PSENSE pin of MAS9142 (9142_RF_PCB_EXTRA). The output voltage was measured at the VAPC pin of MAS9142 on both PCBs.

The results of the amplitude sweep are shown in Figure 21 and Figure 22 below. It is interesting to note that the 9142_RF_PCB behaves very oddly at temperature –40°C and input frequency of 1800 MHz. (see Figure 22). This strange behaviour can be explained with the changes of other component values in temperature. This is particularly true for the off-chip decoupling capacitor, since the comparison with 9142_RF_PCB_EXTRA (with on-chip decoupling capacitor) there is no such observation.

To illustrate the differences of the two boards in more details, the normalized VAPC values are plotted in Figure 23 and Figure 24, in logarithmic scale. The normalization is done by subtacting the ‘zero input’ value of VAPC from the measured VAPC and taking the absolute value of the result to be able to use logarithmic scale.

In Figure 25, the ratios of the normalized VAPC values for the two boards are plotted, for both 900 and 1800 MHz and temperatures +25 and +85°C. It should be noted that while there is no big difference in the 900 MHz curves, the 1800 MHz curve shows quite large differences. This might be caused by inappropriate RF decoupling capacitor on the 9142_RF_PCB. The actual cause for this large difference is not known.

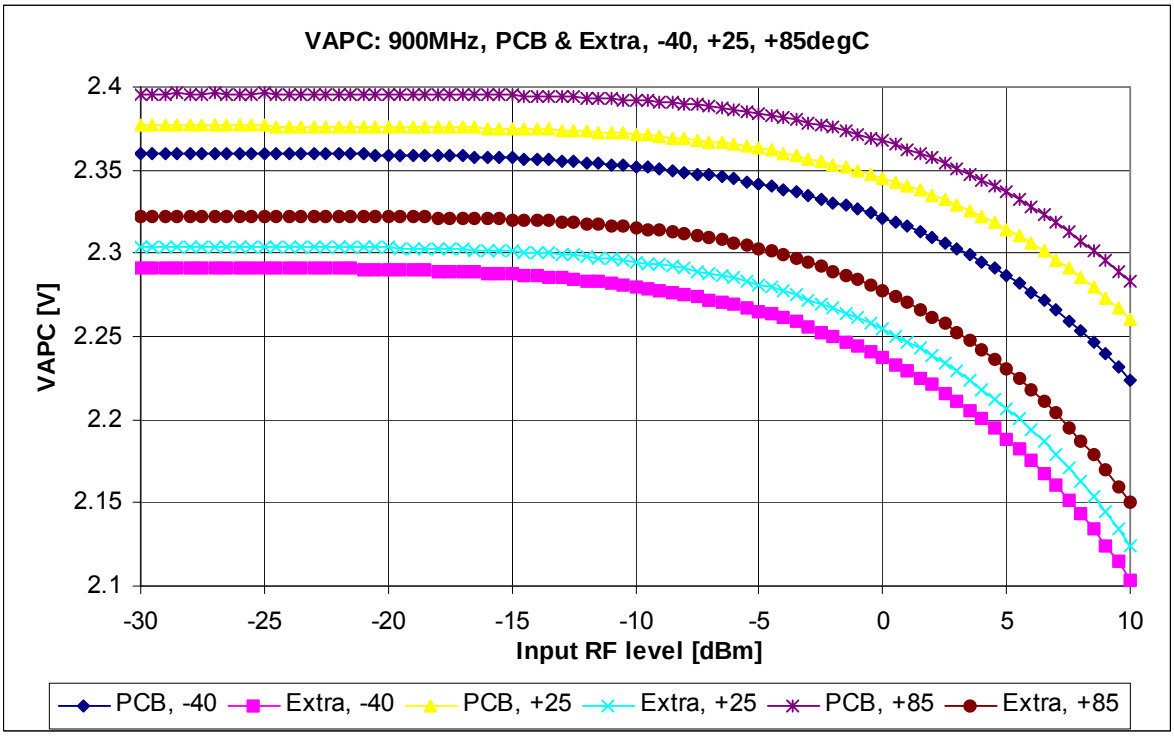


Figure 21. Amplitude sweep at 900MHz

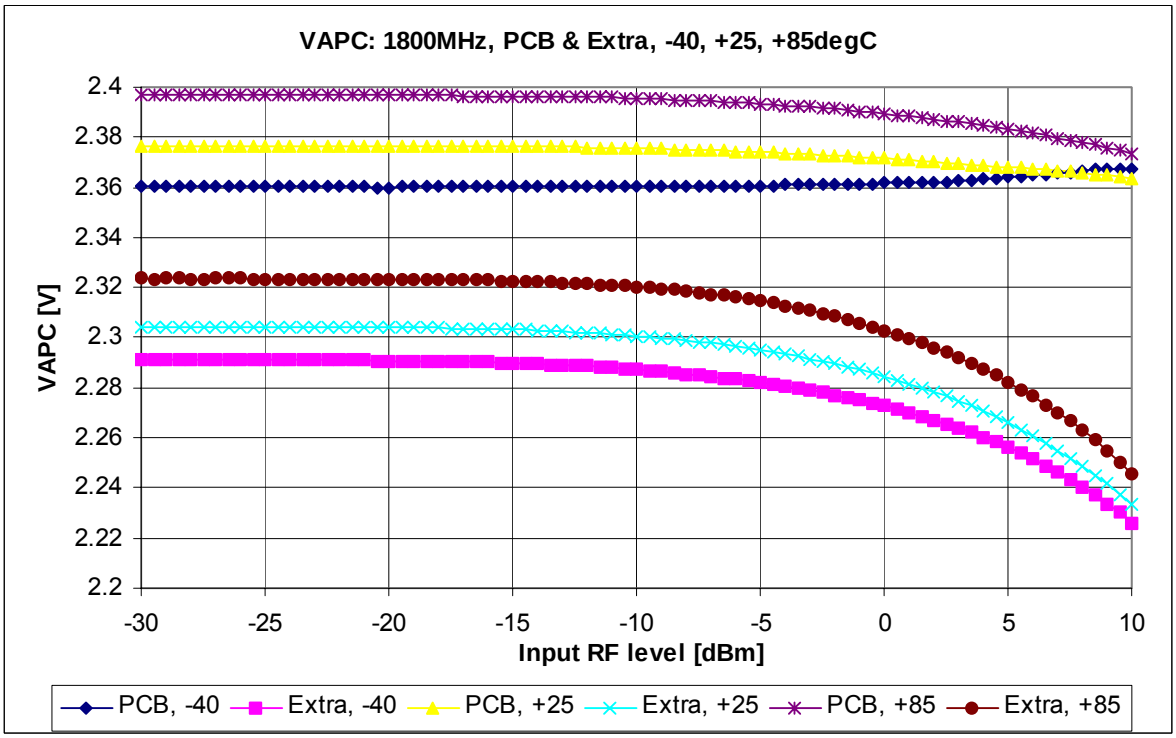


Figure 22. Amplitude sweep at 1800MHz

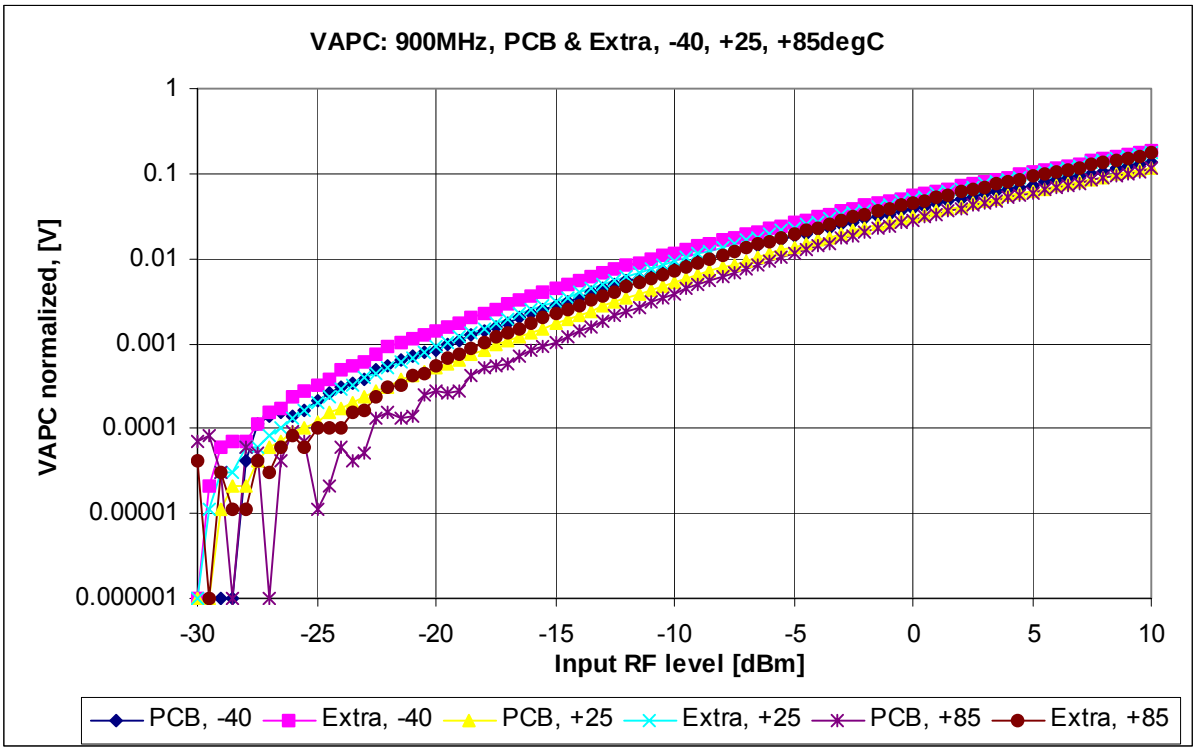


Figure 23. Amplitude sweep, 900MHz, normalized VAPC

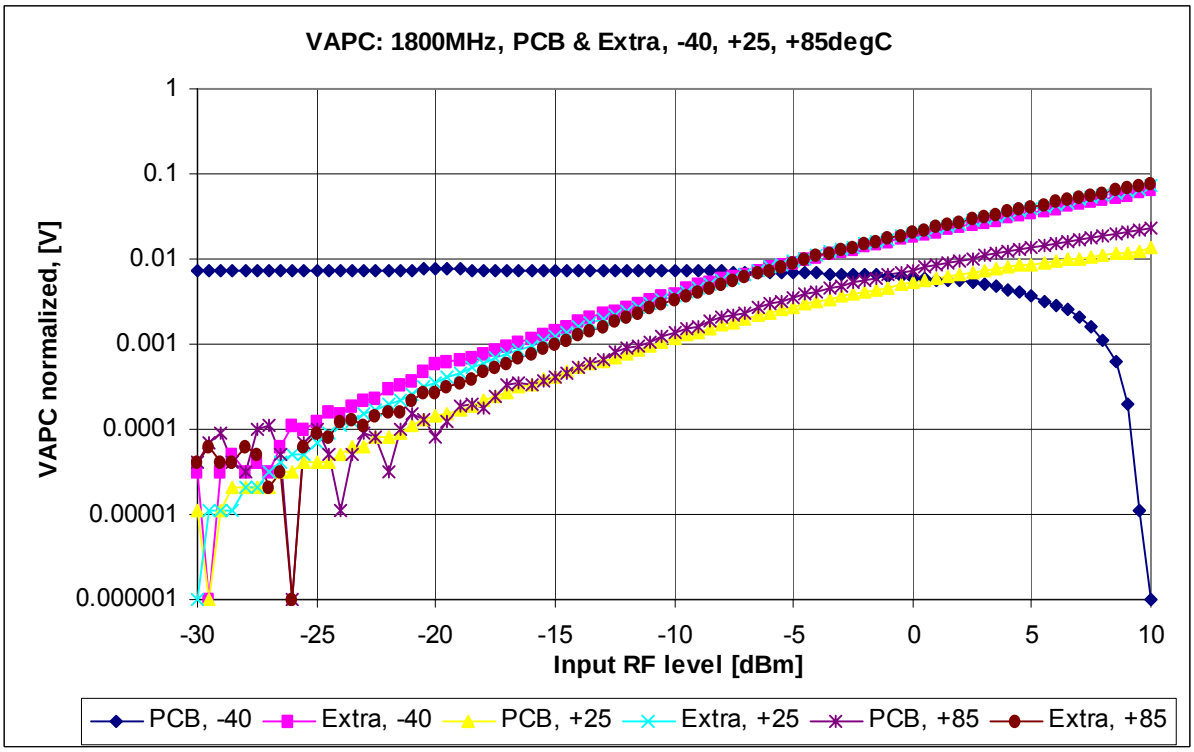


Figure 24. Amplitude sweep, 1800MHz, normalized VAPC

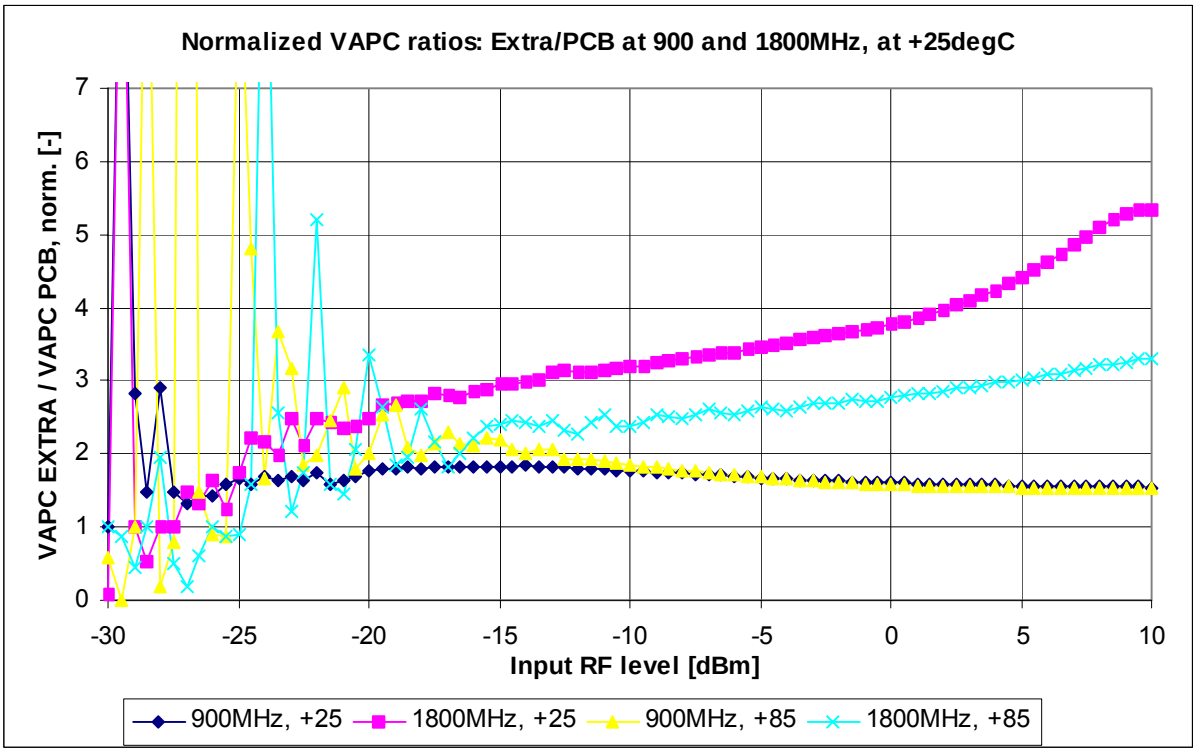


Figure 25. Ratios of normalized VAPC values

The frequency was swept from 100 to 2000 MHz, in 10 MHz steps. The RF input signal amplitude was +6 dBm. Also here, first the measurement results are shown in Figure 26. Then, the normalized VAPC values (normalized again with respect of the 'zero input' VAPC value and absolute value taken) are plotted in Figure 27, in logarithmic scale. It should be noted that at low temperatures and at frequencies above approximately 1.2 GHz, the 9142_RF_PCB almost does not work. It is also interesting to point out the sharp zeros in the curve, they are also seen in all other curves, but less sharply. Their presence in all measurements allows us to conclude that these zeros at frequencies of approximately 1370, 1420, 1650, 1850 and 1900 MHz are the properties of the measurement equipment, not the DUT.

Finally, the comparison is made of the frequency responses of the two measurement boards. It can be concluded by inspecting Figure 27, that at frequencies above 1.2 GHz, the off-chip RF decoupling capacitor of the 9142_RF_PCB has some parasitic resonances and thus the measurements above 1.2 GHz are not very reliable, especially at low temperatures (namely, –40°C).

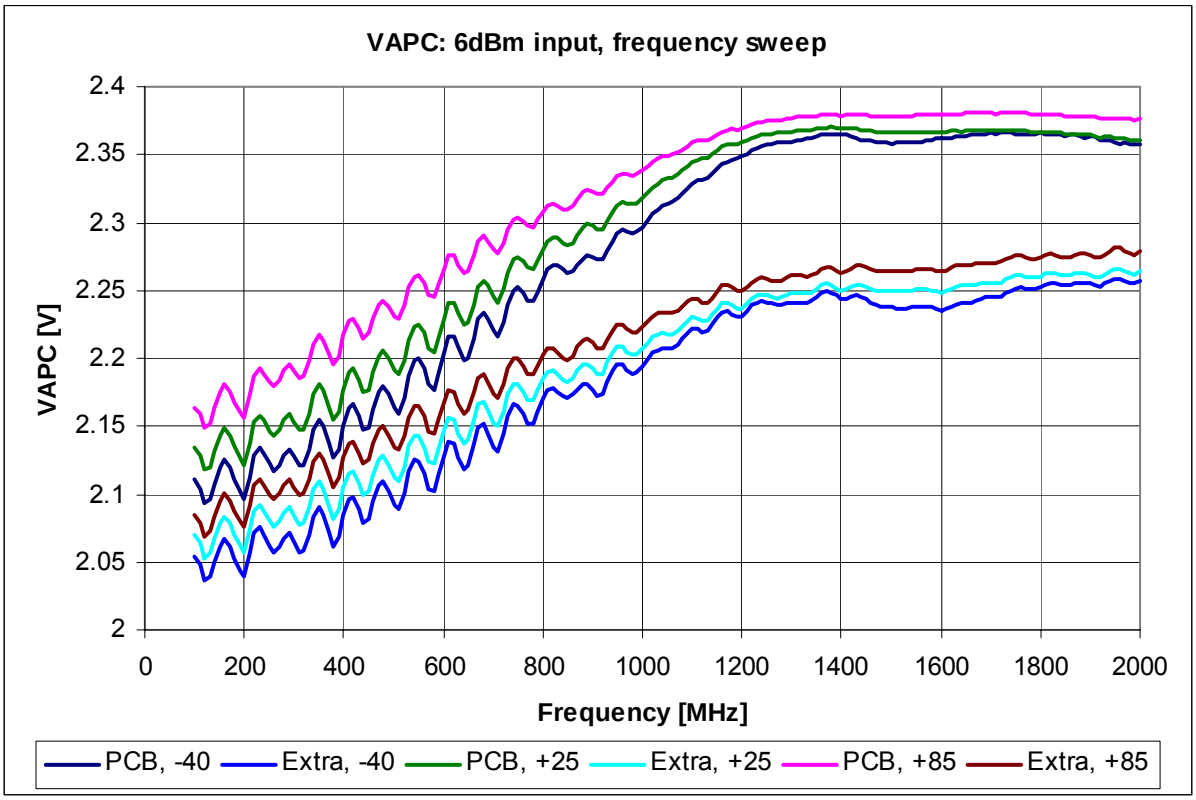


Figure 26. Frequency sweep results

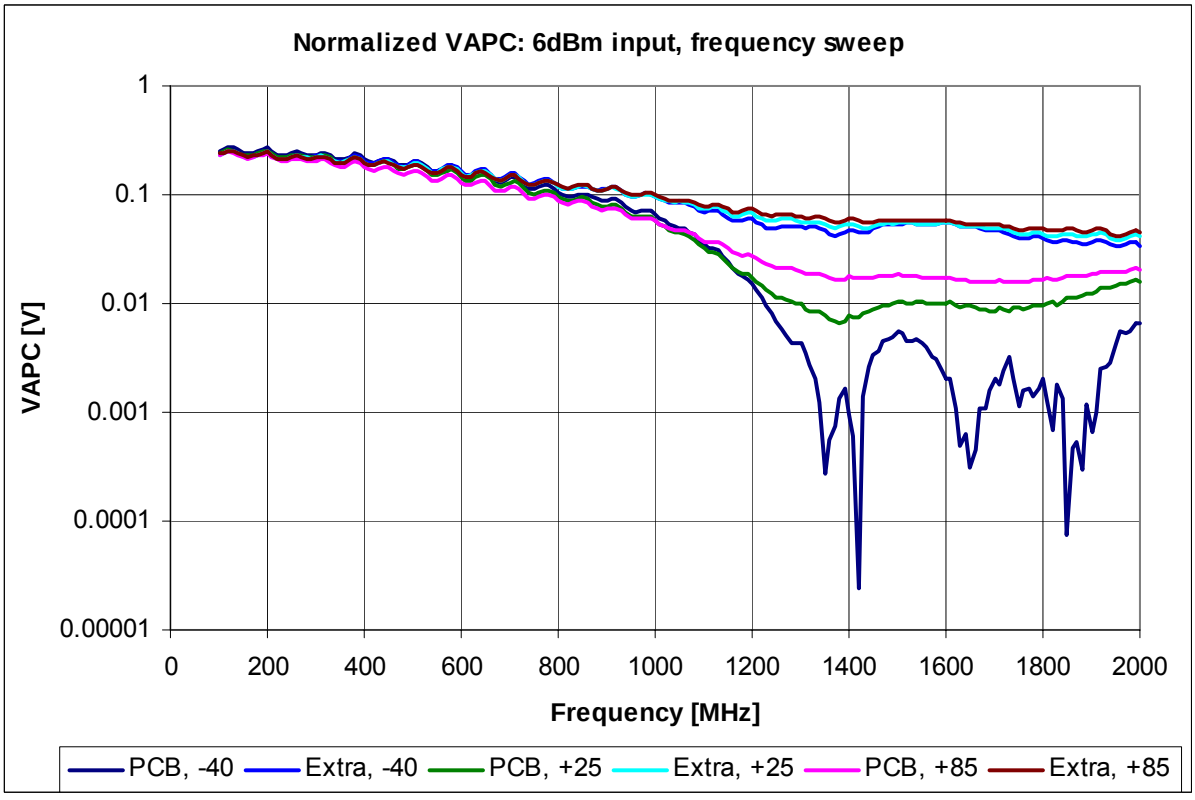


Figure 27. Normalized VAPC in frequency sweep

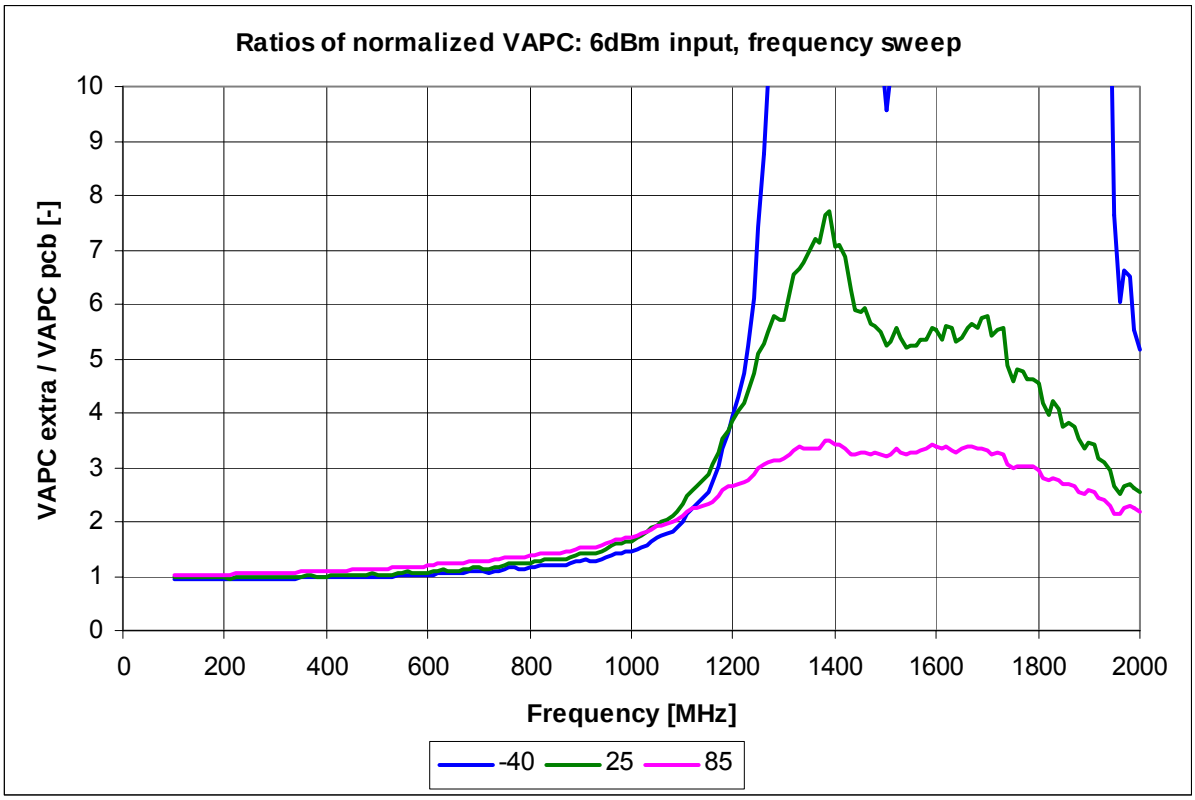


Figure 28. Normalized VAPC ratios at different temperatures

II.7.2. Conclusion

RF properties of MAS9142A chip were measured in the reported laboratory test.

The aim of the measurements was to evaluate the on-chip RF decoupling capacitor of the MAS9142. The RF response of the MAS9142 was measured both with on-chip and off-chip RF decoupling capacitors.

As seen from the measurements, the on-chip RF capacitor is usable and can produce better results than the used off-chip capacitor, especially at frequencies higher than 1.2 GHz. This is believed to be caused of the parasitic resonances of the discrete capacitor, which is used for RF signal decoupling at the DRECT input of the MAS9142A on 9142_RF_PCB.

The result of this measurement is that one could freely use the internal RF decoupling capacitor of MAS9142 in a cellular phone and get rid of one more external discrete component. For the reference, the discrete component count that is replaced by the MAS9142A in cellular phone, is 22, including the RF decoupling capacitor. The suitability for integration of the other 21 components (resistors, capacitors, operational amplifier and LDO voltage regulator) was known in beforehand and did not require extra studying.

III. RF power measurement techniques

In order to reduce the component count in mobile phone even further, one has to seek for possibilities to replace the separate Schottky diode pair used for power detection in the power control circuit under investigation, see Figure 14 and Figure 15 on page 30. The idea that has been investigated relies on the fact that there are bipolar transistors available in the used IC technology (both PNP and NPN transistors). At least equally important is the fact that in rectification mode, the transistor will not act as amplifier – this would lead to novel application of a BJT in above-f_T frequency range.

A new research project, MAS2099 was started. At first, the alternative schematic solutions for the RF rectifiers were chosen and the RECTIF1 IC chip was designed. On chip RECTIF1, there are six different schematics of rectifiers. Each rectifier consists of two diodes: one for rectifying and the other for temperature compensation. The details of the schematics and the layout are presented below.

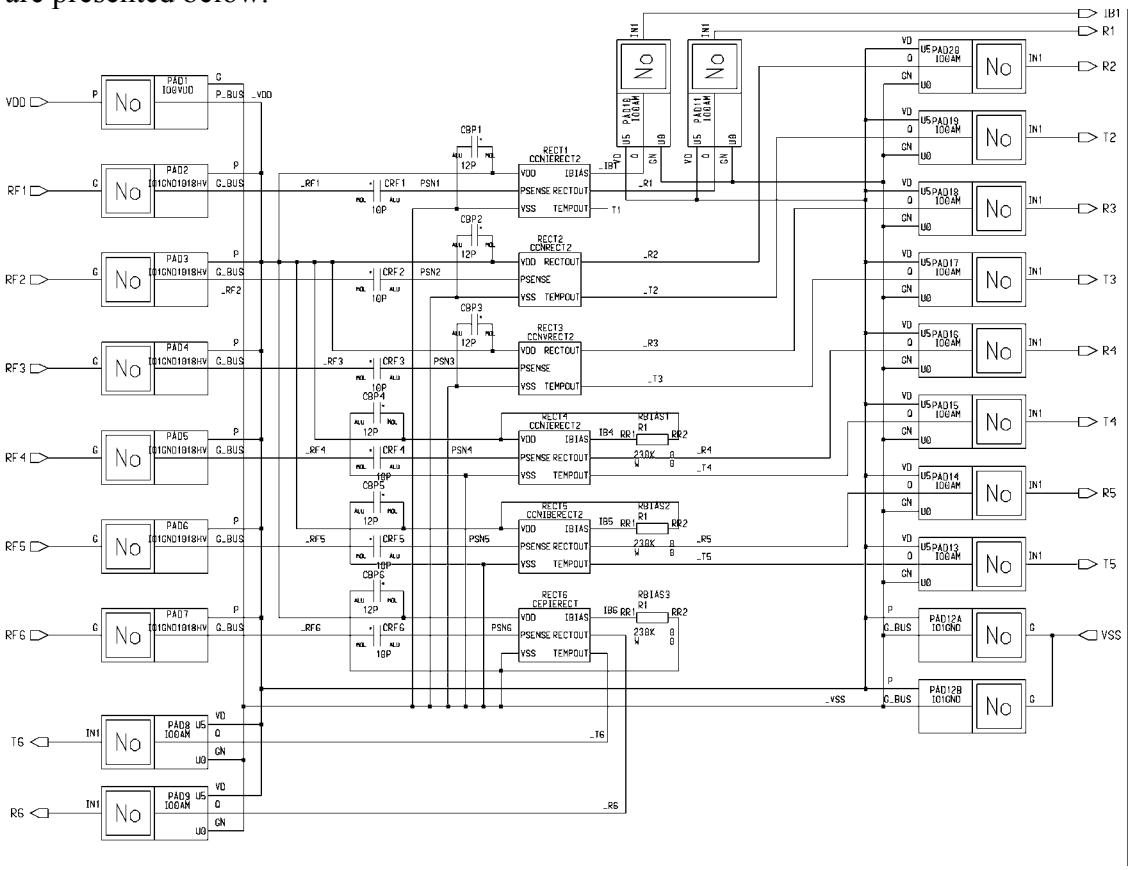


Figure 29. Top schematic of RECTIF1 MPW structure

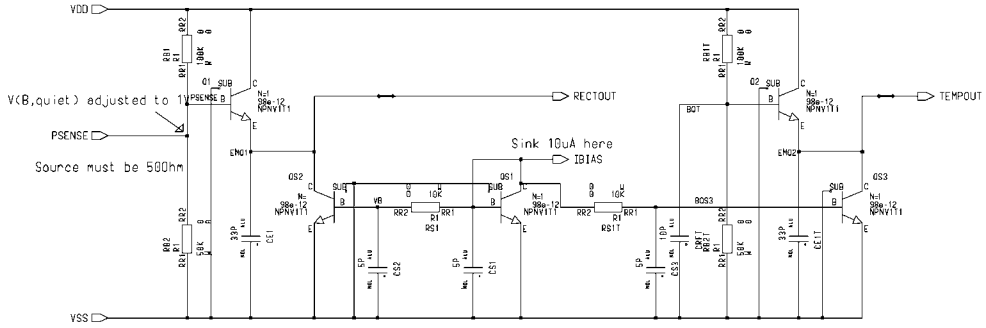


Figure 30. Schematic of R1 and R4 rectifier structures (they are identical)

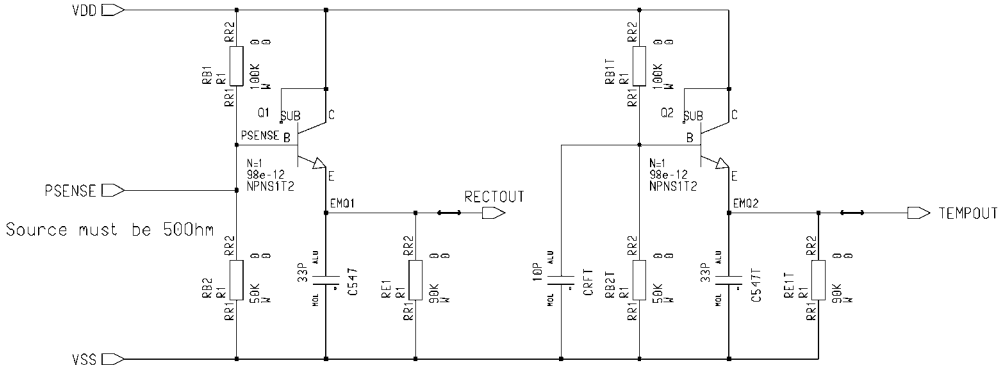


Figure 31. Schematic of R2 rectifier structure

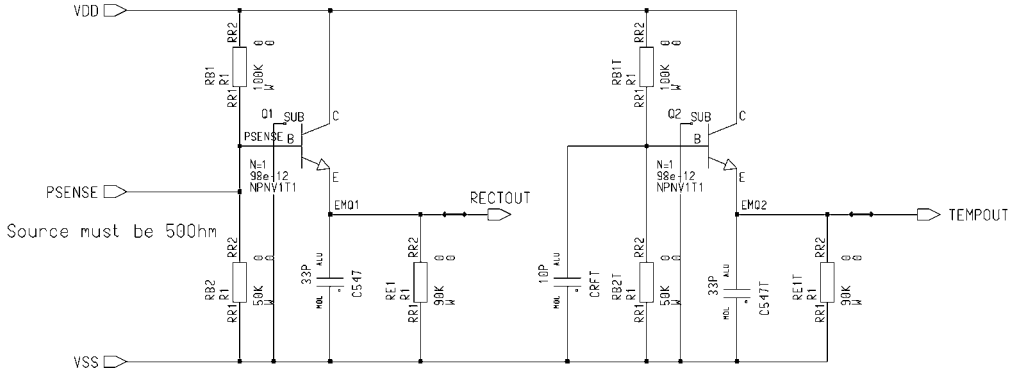


Figure 32. Schematic of R3 rectifier structure

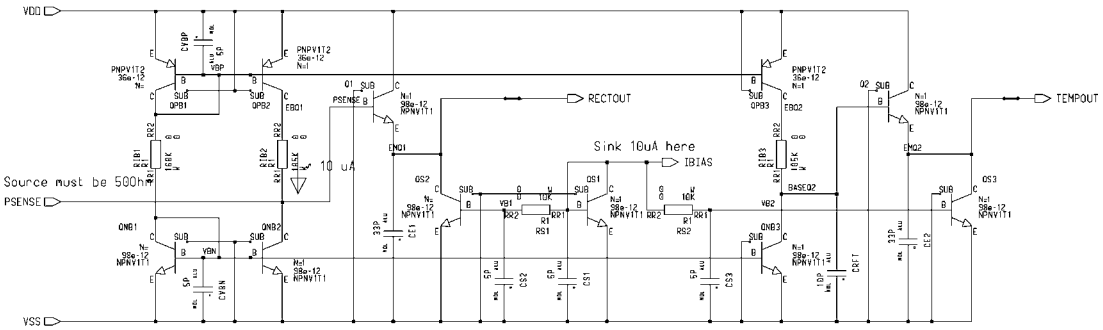


Figure 33. Schematic of R5 rectifier structure

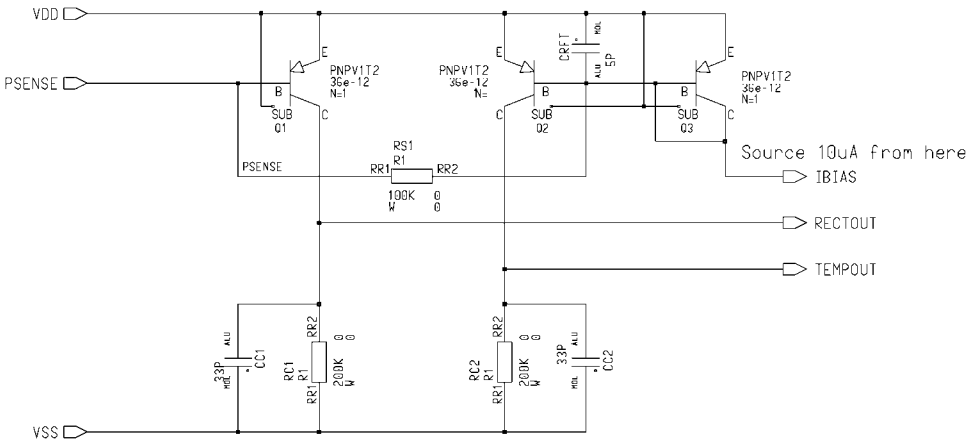


Figure 34. Schematic of R6 rectifier structure

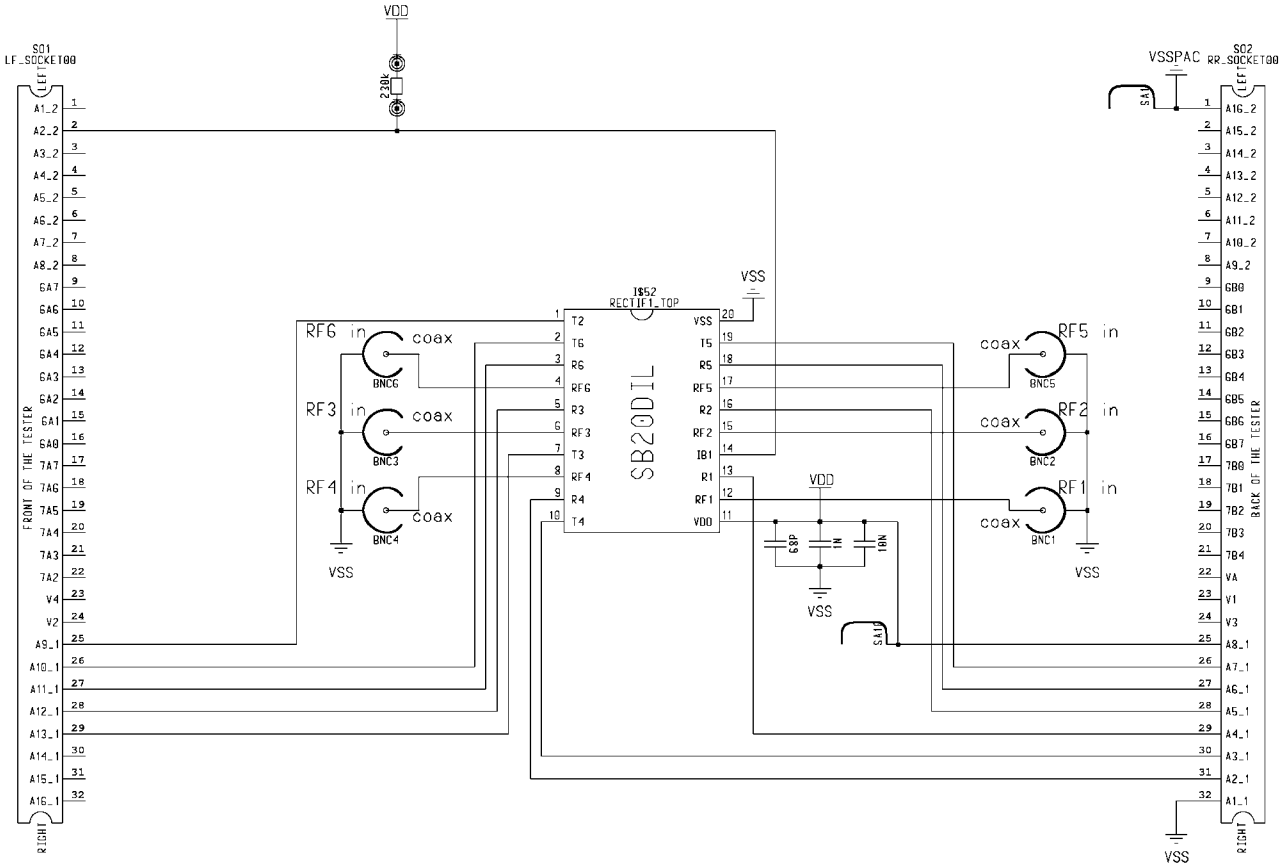


Figure 35. Schematic of laboratory PCB

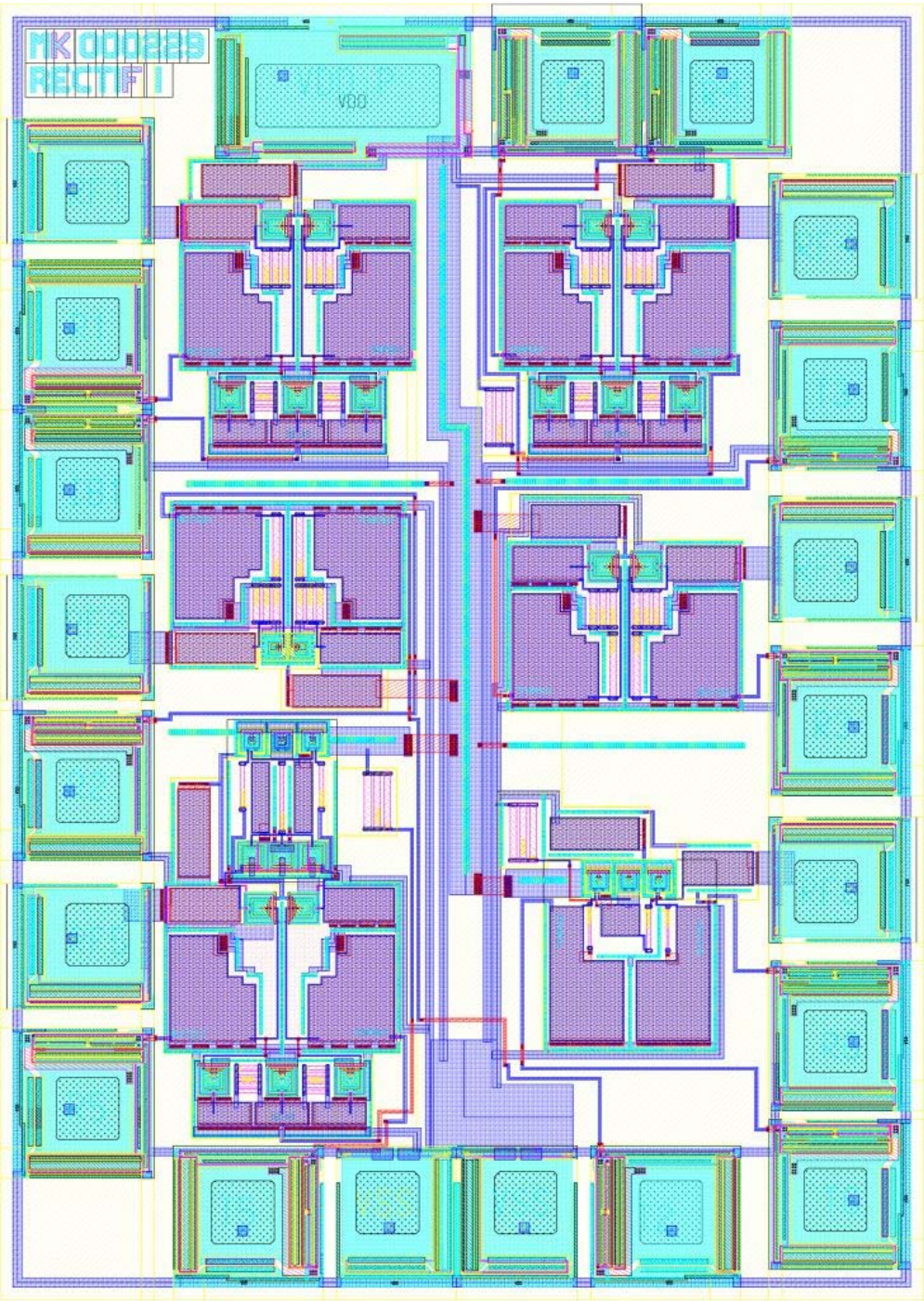


Figure 36. RECTIF1 chip layout

III.1. Statistical measurements of amplitude characteristics

III.1.1. General

The measurements were carried out using common SB20DIL test board. Due to that, the RF signals with frequencies above 500 MHz reached the DUT substantially attenuated. There have also been other reflection and transmission-line effects that affected the measurements.

The MAS9T technology used for fabrication of the RECTIF1 MPW structure has no RF active devices. The bipolar rectification transistors were forced to work as voltage followers

with large degeneration capacitors, which cause the DC bias to change while operating at high frequencies. That was the basic idea of rectification – the restoration of DC component of the input signal, that is proportional to the signal amplitude.

Due to mismatch at the RF generator → DUT input interface and the 100% AM-pulsed output, the signal parameters indicated at the display of the RF generator (RMS value) and the DUT end of the signal cable (peak value) were different. The relationship between the generator output and the DUT input voltages is as follows:

Table 12. Voltage levels at DUT

2	times due to mismatch (1Mohm -- 50ohm)
2	times due to 100% AM
1.414214	times due to RMS to amplitude conversion (sine signal
5.656854	times is amplitude bigger on chip

In the presentation of the measurement results, the REAL PEAK values at the DUT input are indicated as the input signal and the REAL PEAK values are also used in all figures throughout this section. The relationships between the generator and real peak values are shown in Table 13.

Table 13. Input levels of the rectifiers

generator mV RMS	Real mV ampl	generator dBm	Real dBm
1	5.657	-47	**-34.9**
2	11.31	-41	**-28.9**
3	16.97	-37.4	**-25.4**
5	28.28	-33	**-21**
7	39.6	-30.1	**-18**
10	56.57	-27	**-14.9**
15	84.85	-23.5	**-11.4**
20	113.1	-21	**-8.93**
30	169.7	-17.4	**-5.41**
40	226.3	-14.9	**-2.91**
50	282.8	-13	**-0.97**
60	339.4	-11.4	**0.61**
70	396	-10.1	**1.95**
80	452.5	-8.93	**3.11**
90	509.1	-7.9	**4.14**
100	565.7	-6.99	**5.05**
120	678.8	-5.41	**6.64**
150	848.5	-3.47	**8.57**
200	1131	-0.97	**11.1**
250	1414	0.97	**13**
300	1697	2.55	**14.6**
350	1980	3.89	**15.9**
400	2263	5.05	**17.1**
450	**2546**	6.07	**18.1**
500	2828	6.99	**19**
600	3394	8.57	**20.6**
700	3960	9.91	**22**

All measurements were carried out at room temperature and the supply voltage was 3.0 V. Amplitude responses of all nine chips were measured at four frequencies: 100 MHz, 450 MHz, 900 MHz and 1.8 GHz. Rectifier structures R1-R4 and R6 were measured on all chips, whereas

the R5 structure was measured on chip number 1 only. Thus, there is not statistics available for R5 rectifier structure. Please refer to Figure 29 – Figure 35 above for the chip schematics.

III.1.2. Statistical results

The statistical results of the measurements of rectifier structures R1-R4 are in the following table (Table 14). Error percentages are calculated as average ±1σ.

Table 14. RECTIF1 measurement results

gene mV RMS	Real mV ampl	gene dBm	Real dBm	R1			R2			R3			R4		
				100MHz											
				Avg	Stdev	Error%	Avg	Stdev	Error%	Avg	Stdev	Error%	Avg	Stdev	Error%
10	**56.57**	-26.99	-14.95	18.04	0.52	**2.88%**	17.73	0.141	**0.80%**	18.16	0.159	**0.88%**	18.73	0.346	**1.85%**
20	**113.14**	-20.97	-8.93	55.36	0.841	**1.52%**	54.18	0.484	**0.89%**	54.44	0.26	**0.48%**	57	0.424	**0.74%**
50	**282.84**	-13.01	-0.97	189	4.301	**2.28%**	181.6	1.59	**0.88%**	184.8	1.202	**0.65%**	191.3	2.236	**1.17%**
100	**565.69**	-6.99	5.05	426.9	6.936	**1.62%**	408.3	1.581	**0.39%**	413.9	3.951	**0.95%**	436.4	0.882	**0.20%**
200	**1131.37**	-0.97	11.07	908.2	14.51	**1.60%**	870.7	4.472	**0.51%**	874.4	5.981	**0.68%**	921.1	3.333	**0.36%**
300	**1697.06**	2.55	14.59	1396	26.51	**1.90%**	1329	13.64	**1.03%**	1379	15.37	**1.11%**	1424	11.02	**0.77%**
400	**2262.74**	5.05	17.09	1921	27.59	**1.44%**	1842	4.41	**0.24%**	1850	14.14	**0.76%**	1912	17.16	**0.90%**
500	**2828.43**	6.99	19.03	2394	31.27	**1.31%**	2317	10	**0.43%**	2321	7.817	**0.34%**	2386	16.67	**0.70%**
600	**3394.11**	8.57	20.61	2569	3.78	**0.15%**	2500	0	**0.00%**	2450	46.1	**1.88%**	2523	12.25	**0.49%**
				450MHz											
10	**56.57**	-26.99	-14.95	13.83	0.255	**1.84%**	13.49	0.162	**1.20%**	15.23	0.269	**1.77%**	13.4	0.424	**3.17%**
20	**113.14**	-20.97	-8.93	44.88	0.65	**1.45%**	43.16	0.536	**1.24%**	47.13	0.616	**1.31%**	42.73	1.068	**2.50%**
50	**282.84**	-13.01	-0.97	166.5	2.268	**1.36%**	153.6	1.236	**0.80%**	162.2	1.922	**1.18%**	152.7	2.318	**1.52%**
100	**565.69**	-6.99	5.05	393.4	6.781	**1.72%**	348.1	1.537	**0.44%**	369	4.301	**1.17%**	349.6	5.548	**1.59%**
200	**1131.37**	-0.97	11.07	841.3	3.536	**0.42%**	757.4	3.283	**0.43%**	787.8	8.743	**1.11%**	744.6	17.84	**2.40%**
300	**1697.06**	2.55	14.59	1254	5.175	**0.41%**	1149	23.15	**2.02%**	1222	6.667	**0.55%**	1145	20.27	**1.77%**
400	**2262.74**	5.05	17.09	1663	11.65	**0.70%**	1554	10.14	**0.65%**	1670	15.81	**0.95%**	1568	32.44	**2.07%**
500	**2828.43**	6.99	19.03	2133	20.53	**0.96%**	2019	22.61	**1.12%**	2119	54.19	**2.56%**	2022	45.22	**2.24%**
				900MHz											
10	**56.57**	-26.99	-14.95	5.025	0.175	**3.49%**	3.944	0.133	**3.38%**	4.3	0.235	**5.45%**	4.556	0.3	**6.60%**
20	**113.14**	-20.97	-8.93	18.29	0.679	**3.71%**	14.48	0.497	**3.43%**	15.42	0.719	**4.66%**	16.52	0.98	**5.93%**
50	**282.84**	-13.01	-0.97	78.95	2.211	**2.80%**	64.01	1.607	**2.51%**	66.11	2.207	**3.34%**	72.16	3.01	**4.17%**
100	**565.69**	-6.99	5.05	202.1	4.704	**2.33%**	161.1	3.887	**2.41%**	166.3	5.099	**3.07%**	181.9	6.274	**3.45%**
200	**1131.37**	-0.97	11.07	470.5	9.304	**1.98%**	365.3	9.014	**2.47%**	381.8	9.55	**2.50%**	418.7	13.34	**3.19%**
300	**1697.06**	2.55	14.59	753	15.53	**2.06%**	575.6	15.39	**2.67%**	593.9	15.45	**2.60%**	654.7	25.88	**3.95%**
400	**2262.74**	5.05	17.09	1033	21.21	**2.05%**	777.6	18.16	**2.34%**	819.1	24.96	**3.05%**	886	28.77	**3.25%**
500	**2828.43**	6.99	19.03	1290	25.63	**1.99%**	987.6	27.74	**2.81%**	1013	38.67	**3.82%**	1096	54.25	**4.95%**
600	**3394.11**	8.57	20.61	1530	17.1	**1.12%**	1196	33.35	**2.79%**				1208	128	**10.59%**
				1.8GHz											
10	**56.57**	-26.99	-14.95	0.414	0.038	**9.12%**	2	0.12	**5.98%**	1.711	0.127	**7.42%**	0.444	0.133	**30.00%**
20	**113.14**	-20.97	-8.93	1.943	0.113	**5.84%**	7.788	0.429	**5.51%**	6.533	0.469	**7.18%**	1.833	0.24	**13.08%**
50	**282.84**	-13.01	-0.97	11.77	0.692	**5.88%**	40.8	1.571	**3.85%**	34.57	1.877	**5.43%**	10.88	1.335	**12.27%**
100	**565.69**	-6.99	5.05	40.4	2.307	**5.71%**	112.9	3.523	**3.12%**	97.87	4.458	**4.55%**	37.54	4.027	**10.73%**
200	**1131.37**	-0.97	11.07	119.3	4.716	**3.95%**	270.6	8.518	**3.15%**	250.2	8.729	**3.49%**	110.1	9.253	**8.40%**
300	**1697.06**	2.55	14.59	208	7.483	**3.60%**	437.8	11.78	**2.69%**	413.1	11.14	**2.70%**	193.4	15.9	**8.22%**
400	**2262.74**	5.05	17.09	308.6	9.964	**3.23%**	614.8	20.48	**3.33%**	587.3	9.165	**1.56%**	282.9	22.25	**7.87%**
500	**2828.43**	6.99	19.03	428	12.6	**2.94%**	822	27.15	**3.30%**	783	15.48	**1.98%**	391.8	28.4	**7.25%**
600	**3394.11**	8.57	20.61	557.1	17.54	**3.15%**	1036	32.04	**3.09%**	956.9	17.18	**1.80%**	510.3	36.06	**7.07%**

All measured values in the above table are in mV DC.

The statistical results for rectifier structure R6 are shown in Table 15.

Table 15. Measurement results for rectifier R6

gene mV RMS	Real mV ampl	gene dBm	Real dBm	R6											
				100MHz			450MHz			900MHz			1.8GHz		
				Avg	Stdev	Error%	Avg	Stdev	Error%	Avg	Stdev	Error%	Avg	Stdev	Error%
0.5	**2.83**	-53.01	-40.97	2.511	0.105	**4.20%**	1.833	0.112	**6.10%**						
1	**5.66**	-46.99	-34.95	9.933	0.087	**0.87%**	6.967	0.071	**1.01%**	1.756	0.113	**6.44%**	0.767	0.206	**26.89%**
1.5	**8.49**	-43.47	-31.43	22.29	0.285	**1.28%**	16.11	0.145	**0.90%**	3.9	0.122	**3.14%**	1.967	0.087	**4.40%**
3	**16.97**	-37.45	-25.41	89.09	0.788	**0.88%**	64.67	0.707	**1.09%**	15.8	0.245	**1.55%**	7.444	0.181	**2.43%**
5	**28.28**	-33.01	-20.97	246.9	3.06	**1.24%**	180	2.062	**1.15%**	43.89	0.807	**1.84%**	21.82	0.514	**2.36%**
7	**39.60**	-30.09	-18.05	478.5	2.976	**0.62%**	347.5	2.777	**0.80%**	86	1.309	**1.52%**	42.38	1.408	**3.32%**
10	**56.57**	-26.99	-14.95	943.1	7.424	**0.79%**	688.2	4.177	**0.61%**	173.7	2.915	**1.68%**	86.56	2.603	**3.01%**
12	**67.88**	-25.41	-13.36	1036	48.08	**4.64%**	946	8.485	**0.90%**	251	1.414	**0.56%**	121.5	4.95	**4.07%**
15	**84.85**	-23.47	-11.43	1111	22.07	**1.99%**	1087	22.36	**2.06%**	384	7.794	**2.03%**	193.2	5.094	**2.64%**
20	**113.14**	-20.97	-8.93				1120	9.468	**0.85%**	638.7	49.55	**7.76%**	330.8	9.667	**2.92%**

All measured values in the above table are in mV DC.

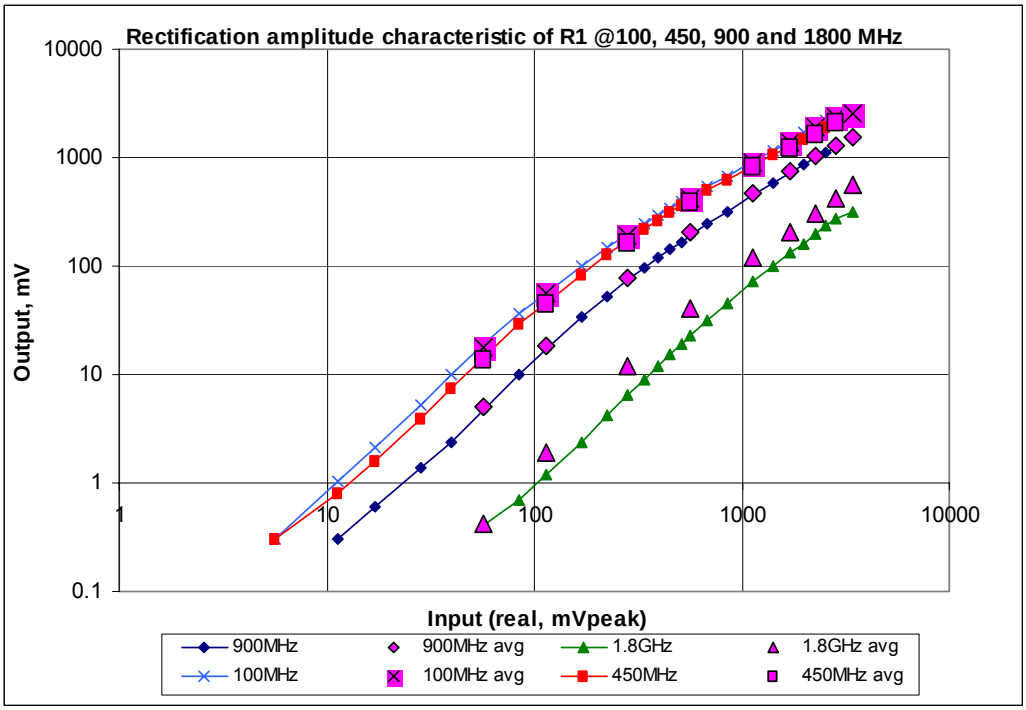


Figure 37. R1 amplitude characteristics

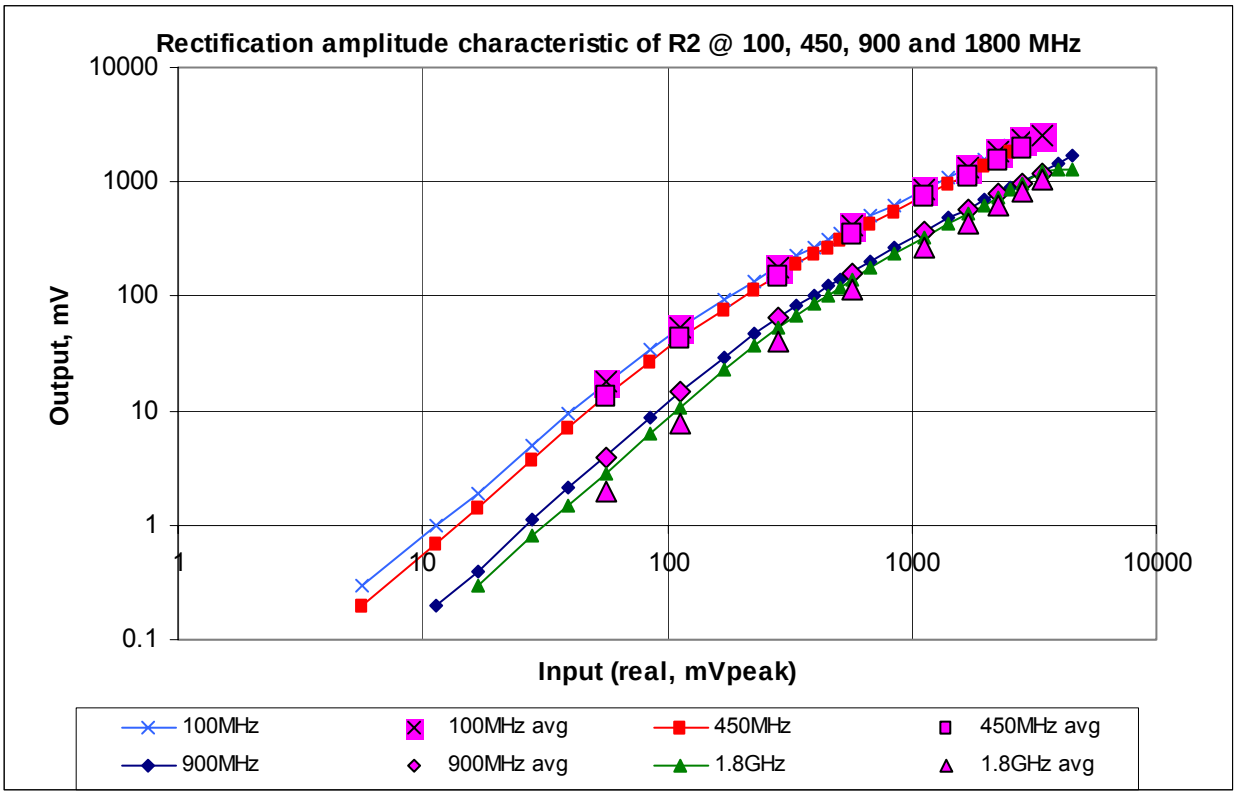


Figure 38. R2 amplitude characteristics

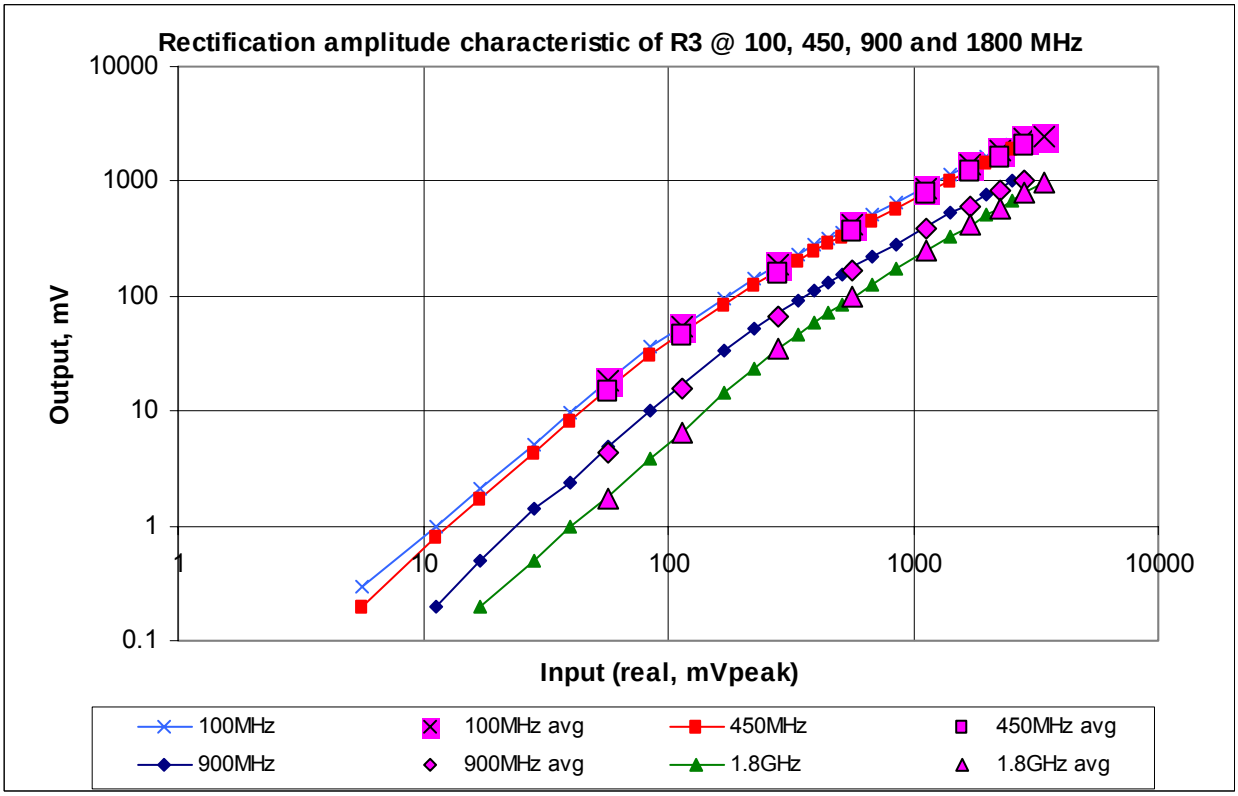


Figure 39. R3 amplitude characteristics

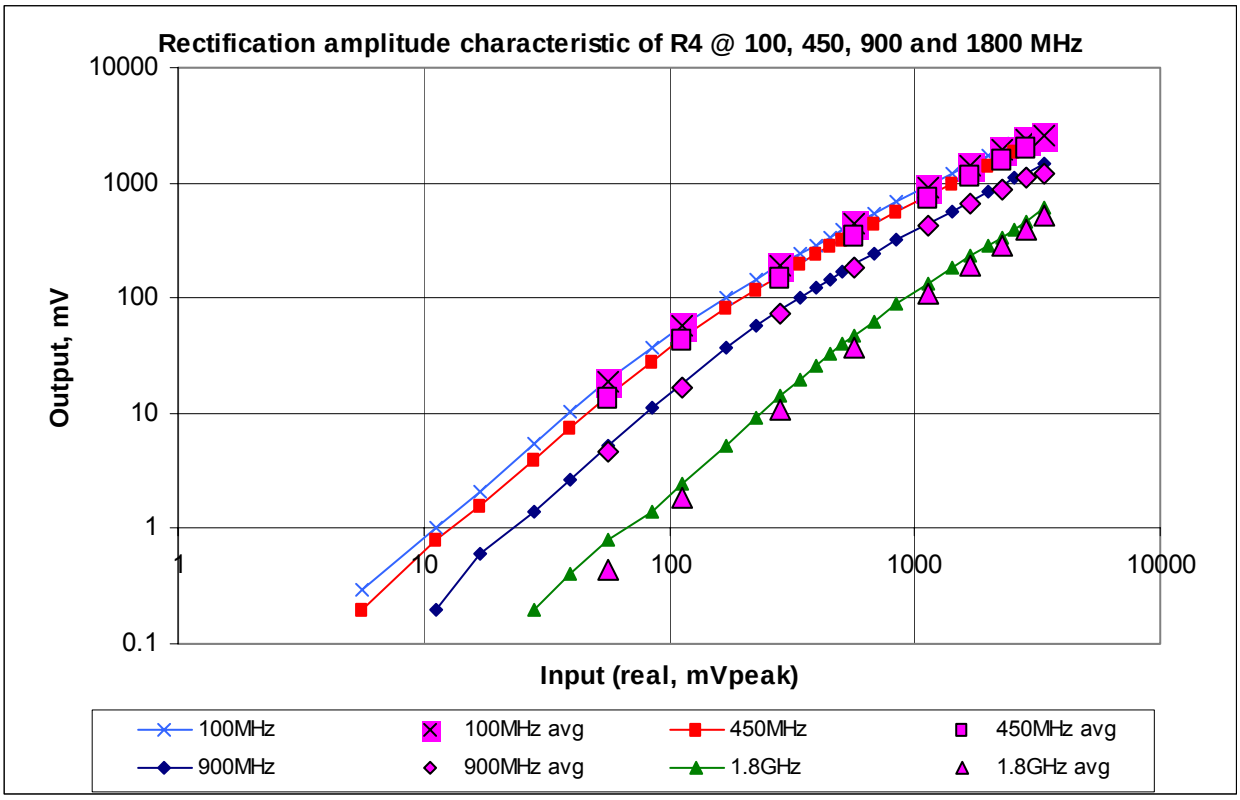


Figure 40. R4 amplitude characteristics

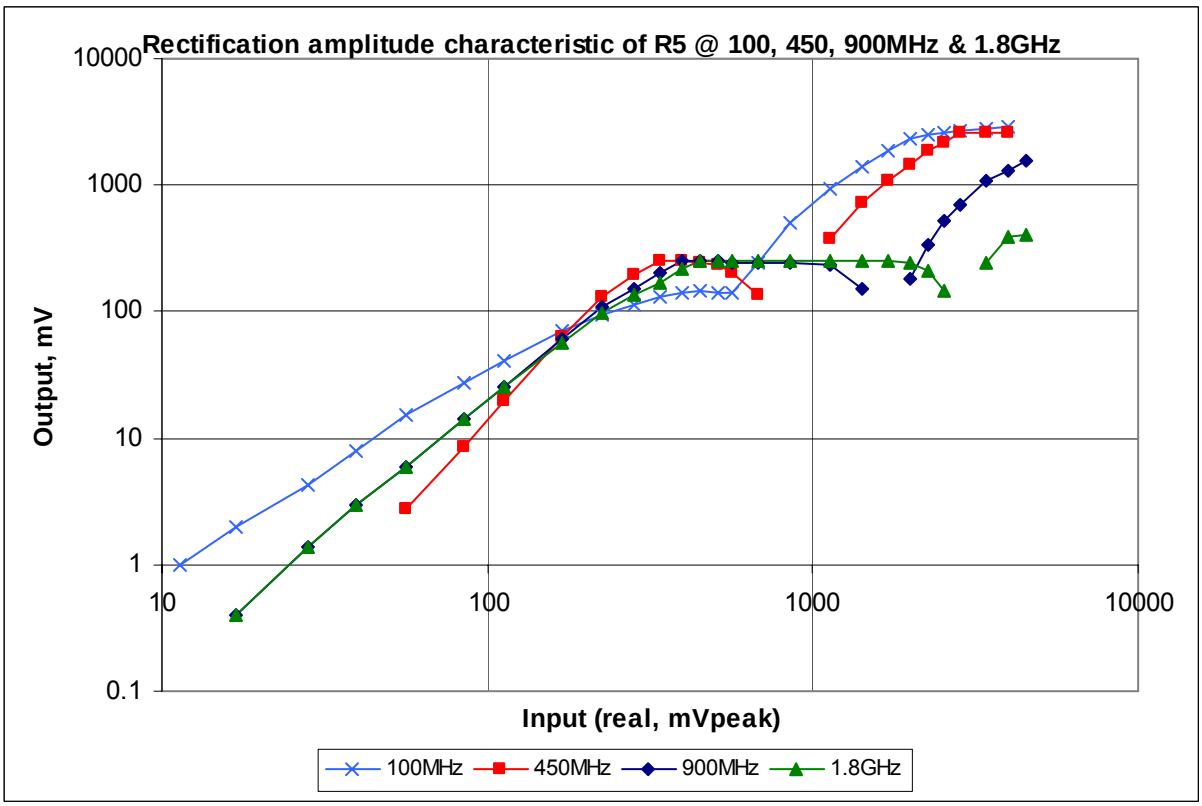


Figure 41. R5 amplitude characteristics

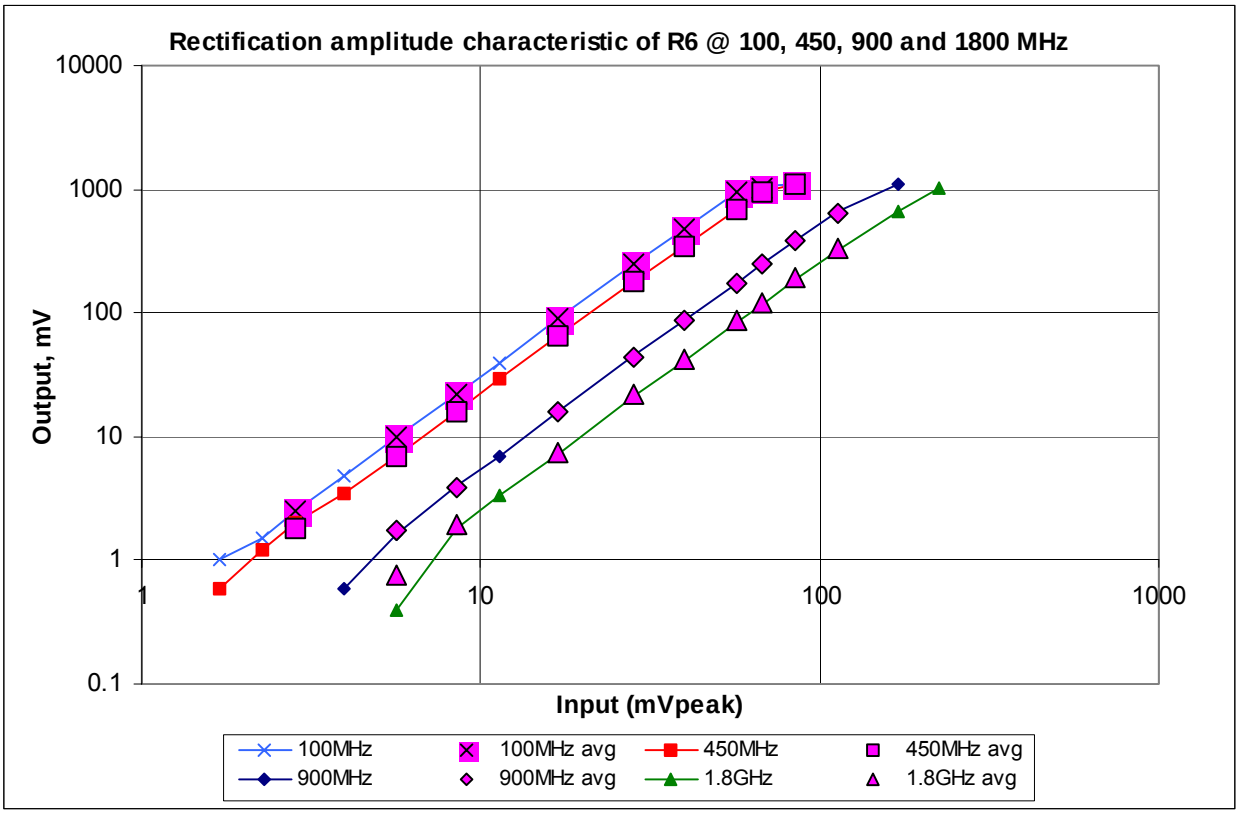


Figure 42. R6 amplitude characteristics

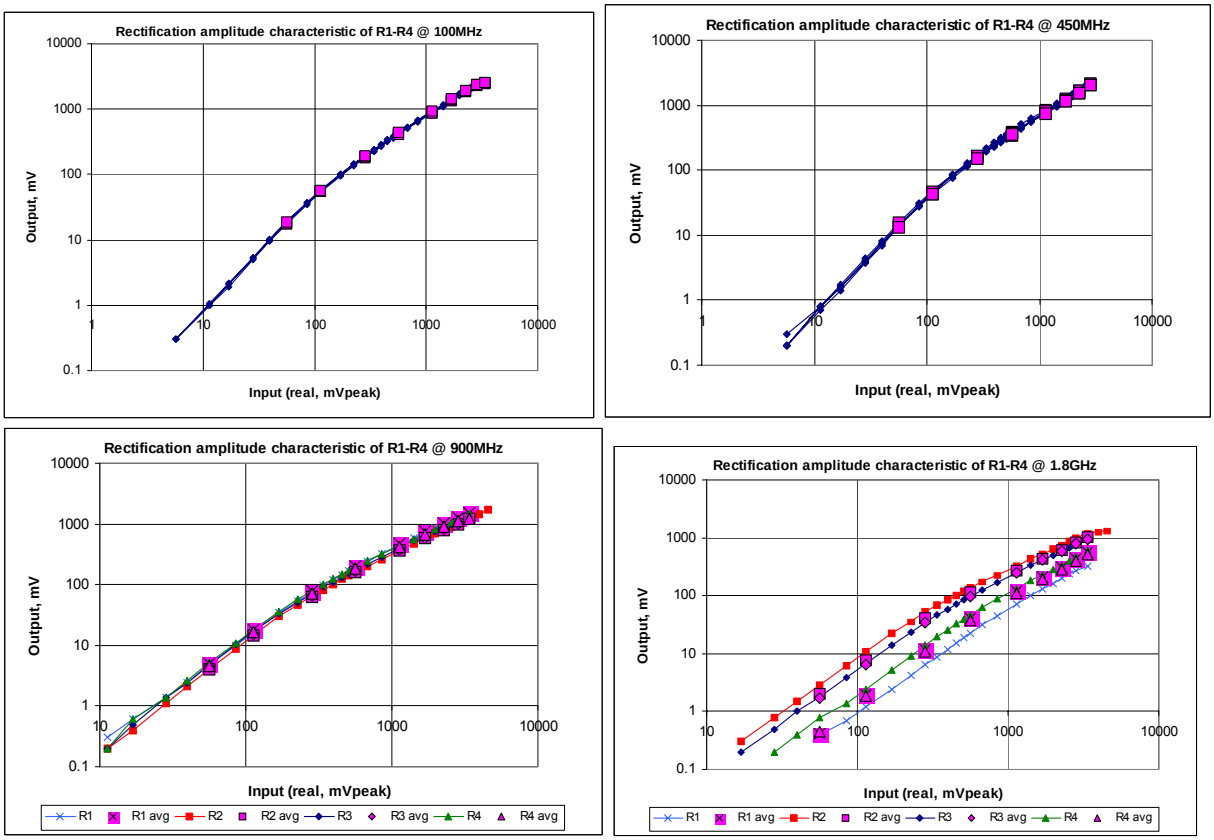


Figure 43. Comparison of rectifiers R1-R4

The attenuation from the generator to DUT with a high-resistance RF probe are also measured. The attenuation factors obtained for frequencies 900MHz and 1.8GHz are shown in Table 16:

Table 16. Attenuation of RF signal path

R2 analysis: correction of the RF attenuation			
Attenuation at 900MHz	**7.27**	dB	or **0.433** times
Attenuation at 1.8GHz	**13.52**	dB	or **0.211** times
Attenuation figures from separate measurement			

The corrected input signal values for the R2 measurement are presented in Table 17.

Table 17. Corrected input signal levels

gene mV RMS	Real mV ampl	gene dBm	Real dBm	R2					
				100 MHz	450 MHz	900MHz Input	900MHz Avg	1.8GHz Input	1.8GHz Avg
10	**56.57**	-26.99	-14.95	17.73	13.49	**24.495**	3.944	**11.93**	2
20	**113.14**	-20.97	-8.93	54.18	43.16	**48.99**	14.48	**23.86**	7.7875
50	**282.84**	-13.01	-0.97	181.6	153.6	**122.47**	64.01	**59.64**	40.8
100	**565.69**	-6.99	5.05	408.3	348.1	**244.95**	161.1	**119.3**	112.88
200	**1131.37**	-0.97	11.07	870.7	757.4	**489.9**	365.3	**238.6**	270.63
300	**1697.06**	2.55	14.59	1329	1149	**734.85**	575.6	**357.8**	437.75
400	**2262.74**	5.05	17.09	1842	1554	**979.79**	777.6	**477.1**	614.75
500	**2828.43**	6.99	19.03	2317	2019	**1224.7**	987.6	**596.4**	822
600	**3394.11**	8.57	20.61	2500		**1469.7**	1196	**715.7**	1036.3

All measured values in the above table are in mV DC.

The pictures of the corrected amplitude responses are shown below. It can be seen that the correction of input signal level brings the measurement results at 900 MHz to good agreement with the measurement results at lower frequencies. At 1.8 GHz, the attenuation 13.52 dB seems to be overestimated. The estimate of the real attenuation of the path to the DUT is 8.5 dB, see Figure 44

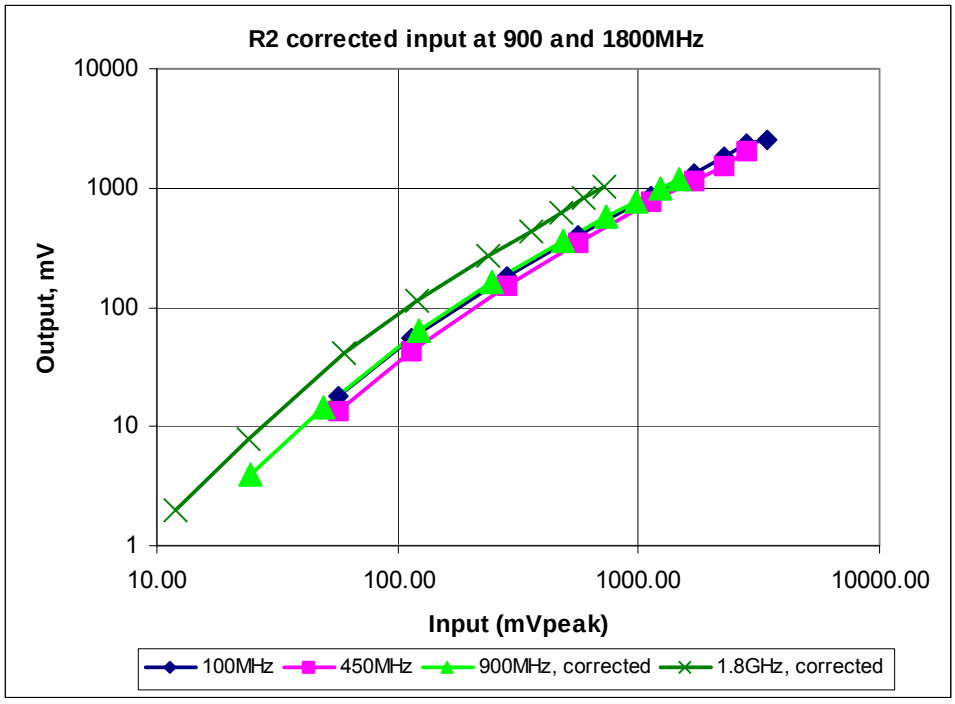


Figure 44. Corrected signal values in R2 rectifier

III.2. Results of RF detector design and measurement

1) The RF rectifiers MPW structure is able to peak detect a RF signal.
2) The RF input signal reaches the DUT on the laboratory PCB with considerable attenuation at input frequencies above 500 MHz.
3) Rectifier structures R1-R4 have similar behavior and their rectification properties are nearly equivalent. The input signal dynamic range is about 5—3500 mVpeak (attenuation on PCB not included). Above this range, the rectifier saturates.
4) Rectifier structure R5 is not working due to a biasing circuit mistake in the base biasing circuit (see Figure 33on page 41 for the schematic of R5).
5) Rectifier structure R6 has much narrower dynamic range than R1-R4. However, this structure is able to rectify small signals, dynamic range is about 2—200 mVpeak (attenuation on PCB not included).
6) R2 input was corrected with the RF attenuation factors at 900 MHz and 1.8 GHz according to Table 16 on page 50. The corrected output behaves well on 900 MHz. It seems that the 1.8 GHz signal attenuates around 5 dB less than reported in the table.
7) In Table 14 on page 45 and Table 15 on page 46, the error percentage is calculated as average±1σ. The error is in all cases in the range of 4% (except at low input levels and near saturation at high input levels), and is most evenly distributed for the rectifier structure R2.
8) **The 'best' rectifier structure on RECTIF1 chip is R2**. **Its use is recommended in the "next generation of PAC" design.**

IV. Practical power detector design

The background of this work is the need to improve the Power Amplifier Controller for cellular mobile handsets, MAS9142. In this work, the possibility of integration of the radio frequency power detector in MAS9T technology is investigated. MAS9T technology is a molybdenum-gate bipolar-enhanced 2 μm CMOS technology with vertical NPN and PNP transistors and a substrate NPN (collector tied to positive supply voltage). The transition frequency f_T of MAS9T bipolar transistors is in the range of a few hundreds of MHz, which is at the first glance considered not feasible for realising any circuitry for signal frequencies above approximately 100 MHz.

Fortunately, the f_T limitation has much smaller influence, when the transistor is used as a rectification diode. This is because the transistor is used not as an amplifier but as a diode and that the application of the RF signal causes the rectification diode to be closed most of the cycle. This causes the diode to have relatively high impedance at the RF, in order of 1-2 kΩ. The high frequencies involved cause the substantial influence of the parasitic elements on the circuit behaviour, but the high impedance level of the rectifier will somewhat decrease their impact.

First attempt to integrate the RF rectifier (alias power detector) was made in early 2000, on the MPW run MAS2580. Six circuit configurations were used, and two versions of the chip were fabricated and encapsulated in SB20DIL ceramic package. The chips were named RECTIF1 and RECTIF2 and the only difference of these was that RECTIF1 had on-chip DC decoupling capacitors and RECTIF2 had not. The RECTIF1 chip was thoroughly measured, and it was found working. The measurement and schematic details can be examined in Section III.

It was concluded that the MAS9T technology is capable of offering an RF rectification possibility. The results of RECTIF1 mpw chip are not directly applicable to MAS9142, due to the possible patent infringement (US patent no. 4,523,155 held by Motorola [252]). It concerns the thermal compensation scheme used – to bias two thermally coupled diodes at identical standby current and to apply the RF signal only to one of the diodes, taking the output as the difference of the voltage drops on the two diodes.

This was the main cause to further investigate the RF rectification. It was also decided to review the schematic topology for minimising the RF crosstalk to other parts of the IC by minimising the RF path length on the chip.

This section is divided into several parts. In the first part, the rectifier design start points are discussed, and the main design strategies. Also theory behind the rectification is shortly touched, as the parasitic elements possibly degrading the rectifier performance. Next part gives an overview of the alternative ideas of thermal compensation used in the rectifier design. Third part presents the designed rectifier schematics. In the fourth part, the analog processors performing thermal compensation are discussed. Fifth part gives a comparative analysis of the simulation and measurement results, and in the last part, conclusions are drawn.

IV.1. Design start points

It was learned from the early design of RF rectifier, RECTIF1&2 (see Section III on page 40) that the RF signal path should be as short as possible and the separate ground path for the RF signal should be provided. In the current design, it was decided to input the RF signal to the emitter terminal of the bipolar rectification transistor, since the emitter is the electrode of the smallest area. This would reduce the unwanted attenuation of RF input signal as well as reduce

cross-talk to other parts of the chip. It will also provide the AC input impedance sufficiently high to reduce the influence of parasitics.

As the input is at emitter, it leaves the choice of emitter itself or base as the output electrode. The connection of the collector is 'free' and the various methods of connecting the collector terminal yield many potential schematics of the RF rectifier, differing in the presence or absence or even the direction of the collector current. The possible choices of collector connection are e. g., to leave it open, to short it to base or to ground it. The base should be at AC ground in all cases. Special care should be taken in the large-signal working situation, where potentials of E and B electrodes vary largely and can cause various problems ranging from biasing uncertainty to latch-up.

Another important feature is the integration of the RF decoupling capacitor on the chip. This will economy one more RF capacitor for the phone manufacturer. It also will allow for larger input voltage ranges for the RF signal, since the internal circuitry is DC-decoupled and so the RF input signal can be ground-referenced (bipolar signal). We select 10 pF to be the value for DC blocking. Its impedance at 1 GHz is 15.9 Ω.

The expected accuracy of the RF detection can be directly related to the phase shift generated by the circuitry. This fact is intuitive, as in current design, the lumped-element approach is used. Fortunately, the physical dimensions of the circuit are small so that the field can be handled as quasi-stationary. For verification of this statement, let us make some calculations. The wavelength of 2 GHz in free space is $\lambda=3\cdot10^8$ m/s / $2\cdot10^9$ Hz=15 cm. The wavelength in silicon ($\varepsilon_{r\mathrm{Si}}=11.7$) and silicon dioxide ($\varepsilon_{r\mathrm{SiO2}}=3.9$) are respectively

$$\lambda_{\mathrm{Si}}=\frac{v_0}{f\sqrt{\varepsilon_{r\mathrm{Si}}}}=\frac{3\cdot10^8}{2\cdot10^9\cdot3.42}=4.39\,\mathrm{cm};\ \lambda_{\mathrm{SiO_2}}=\frac{v_0}{f\sqrt{\varepsilon_{r\mathrm{SiO_2}}}}=\frac{3\cdot10^8}{2\cdot10^9\cdot1.97}=7.61\,\mathrm{cm}, \qquad (4)$$

provided that $\mu_r\approx1$ in both materials. For example, for the ALDI chip size which is about 1.3 mm, the phase error for 2 GHz in silicon is 10.7°. It should be noted, that the RF path on the chip is considerably shorter. It is worth remembering, that 0.122 mm at 2 GHz is 1 ° of phase shift in silicon.

In order to get maximum swing of the rectifier output voltage, it is designed to go negative. At larger input RF signal amplitudes, the voltages go below the negative supply rail. This is more easily handled in MAS9T technology and also simplifies the design of the subsequent signal processing circuitry. This constraint was used for selecting the appropriate rectifier structures from the initial library of the rectifier schematics.

Provided that the output of the rectifier can go negative, it is desirable to have an opamp which could handle the common mode range near and below negative supply rail. The design of such opamp was started in Q2/2001, but was postponed due to low time resources. The course of the OA design is laid out in Section II.2. Instead, another OA named OARTR34 was used. This OA has rail-to-rail input stage. Since the output of the OA cannot go negative, it must be used in inverting configuration. A constant voltage is added to the rectifier output signal and thermal reference signal in order to achieve the thermal compensation and simultaneously handle the common-mode range problem.

The thermal compensation is done using a linear combination of the rectifier output signal and thermal signal. The implementation of thermal compensation varies with the rectifier structure and is discussed in details in the subsequent sections.

IV.1.1. Package, bonding and pad parasitics

Next, the parasitics of the bonding wire, package and pad should be evaluated. The information on the parasitic values of the TSSOP16 package are obtained from the manufacturer's specification. As in the manufacturer's data sheet the TSSOP16 package data is missing, the

values are interpolated as the mean of the worst-case values of TSSOP8 and TSSOP28 packages. The figures of the parasitics of the package leads are measured at 100 MHz. The average values for the parasitic elements are:

Table 18. Parasitics of TSSOP16 package

Quantity	Value
Inductance	1.785 nH
Capacitance	296 fF
Resistance	14.8 mΩ

The following equivalent schematic has been used for modelling the package leads:

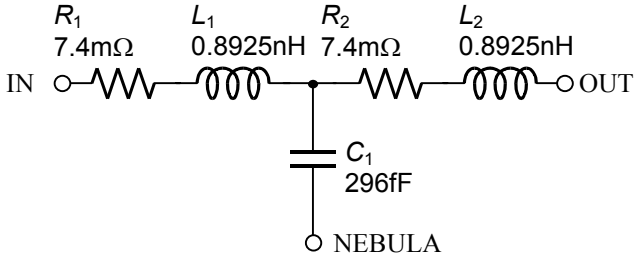


Figure 45. Model of TSSOP16 package lead

It can be seen that resistance and inductance had been splitted to two parts. The other end of the capacitor is 'nebulous', i. e., it is uncertain, against which node in the circuit the capacitance really is.

When the node NEBULA is grounded and transimpedance function calculated with both IN and OUT node loaded with 50 Ω resistors, somewhat astonishing fact comes out that the transimpedance starts increasing in frequency with 20 dB/dec slope at frequency so low as 7 MHz. The phase of the impedance at the frequencies of interest (at 900 MHz) is almost +90°.

The equivalent schematic model of the bonding wire is shown in Figure 46 below:

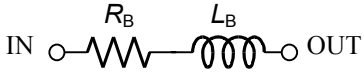


Figure 46. Bonding wire model

The bonding wires are gold wires with diameter d=25 μm and resistivity ρ=2.3·10^{-6} Ω·cm at room temperature (σ=4.35·10^{7} S/m). The skin-effect is not taken into account due to its relatively small influence. The skin-layer depth can be calculated from (5)

$$\Delta = \sqrt{\frac{2}{\omega\mu\sigma}} = \sqrt{\frac{1}{\pi f\mu\sigma}} \xrightarrow{f=1\text{GHz}} \sqrt{\frac{1}{3.14\cdot 10^{9}\cdot 4\cdot 3.14\cdot 10^{-7}\cdot 4.35\cdot 10^{7}}} = 2.41\mu\text{m} \qquad (5)$$

and it represents the depth into the conductor at which the electrical field strength has decreased e times. For reference, the permeability of gold is $\mu_r \approx 1$ and $\mu_0 = 4\pi\cdot 10^{-7}$ H/m. Now, assuming that all current flows no deeper than at the depth of 3Δ, we can calculate that the effective cross-section area of the bonding wire is decreased by 18% at 1 GHz. This increase can be neglected in our approximate model.

Using the resistivity and geometrical measures of the bonding wire, we calculate the resistance of 1 mm of the bonding wire to be 46.9 mΩ.

The calculation of self-inductance of the bonding wire is more complicated and is done using the following formula:

$$L = 2l\left[\ln\left(\frac{2l}{R}\right) - 1 + \frac{R}{l}\right] \text{ [nH]}, \tag{6}$$

where L is self-inductance in nH, R is self geometrical mean length in cm, in case of circle, R=0.7788r, r is radius of the wire in cm, and l is the length of the wire in cm. Putting the above geometrical figures into the formula above, we get the value of 0.865 nH for bonding wire with 1 mm length. Please note that since the self-inductance formula is a non-linear function of length, the simple nH/mm rule cannot be applied in general.

The bonding pad is considered to be modeled with sufficient accuracy as a capacitor against substrate (which is at supply potential in MAS9 technologies). The value of the capacitor was selected to be 1 pF. The parasitic diffusion resistor between the pad capacitor and supply voltage was chosen to be 100 Ω for single pad and 50 Ω for double pad. See Figure 47 below:

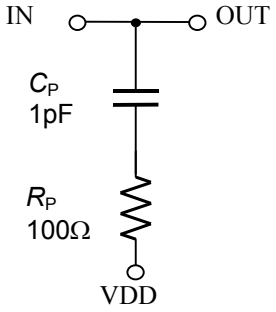


Figure 47. Pad model

IV.1.2. Rectifier formulas

In order to throw light on the somewhat strange shape of the rectification characteristic (V_{out} vs. $V_{in,\,ampl}$, see Figure 49 on page 56), a short referative theory excerpt is brought here. A simplified model for the RF detector is used as the start point and is shown in Figure 48.

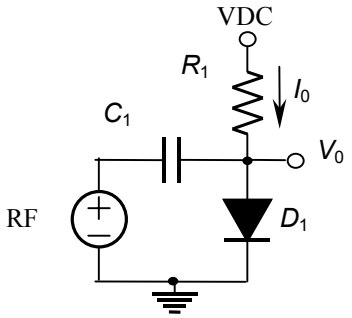


Figure 48. Rectifier model

Voltage drop over the diode is expressed as

$$V = V_0 + V_1 \sin \omega t\,. \tag{7}$$

Diode current is calculated with the classical formula

$$i_d = I_S\left(e^{\frac{V}{\varphi}} - 1\right) = I_S\left(e^{\frac{V_0}{\varphi}} e^{\frac{V_1 \cos \omega t}{\varphi}} - 1\right) = I_S\left(e^{\frac{V_0}{\varphi}} \mathrm{I}_0\left(\frac{V_1}{\varphi}\right) + 2\mathrm{I}_1\left(\frac{V_1}{\varphi}\right)\cos \omega t - 1\right). \tag{8}$$

Diode current expression includes the amplitudes of DC and 1st harmonic components. We are interested only in the DC part of the current, while the RF signal and higher harmonics are effectively filtered out. For the DC part of the current, we may write:

$$i_0 = I_S e^{\frac{V_0}{\varphi}} \mathrm{I}_0\left(\frac{V_1}{\varphi}\right) - I_S \tag{9}$$

The I_0 and I_1 functions are zero- and first-order modified Bessel functions.

Now expressing the V_0:

$$\ln i_0 = \ln I_S + \frac{V_0}{\varphi} + \ln \mathrm{I}_0\left(\frac{V_1}{\varphi}\right) \Rightarrow V_0 = \varphi\left[\ln \frac{i_0}{I_S} - \ln \mathrm{I}_0\left(\frac{V_1}{\varphi}\right)\right] \tag{10}$$

The quantity φ in the formulas is thermal potential, $\varphi=nkT/q$.

Now, consider the numerical example, where the $I_S=5\cdot10^{-17}$ A, n=1.5 and i_0=30 µA. The graph of the rectification curve is shown in Figure 49. Actually, the curve only represents the $\mathrm{I}_0(\cdot)$ part of the V_0 expression (10). It shows the nature of the behaviour, other members in this expression only perform linear scaling.

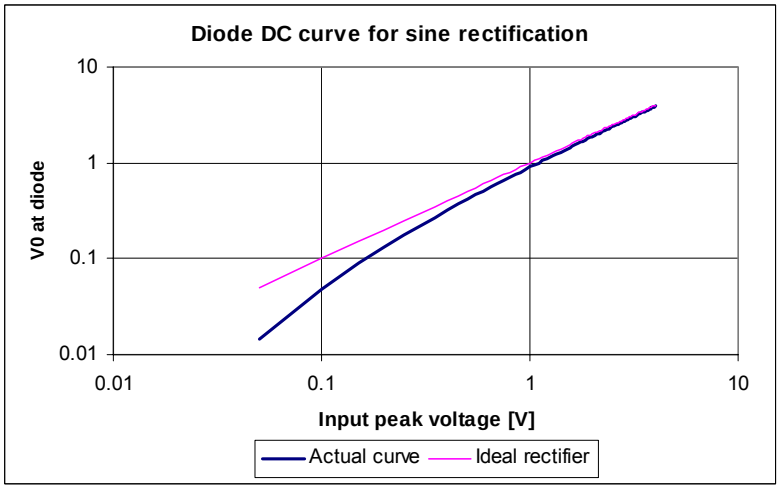


Figure 49. Normalized rectification curve

IV.2. Thermal compensation schemes

The rectification element, the diode, has very unpleasant thermal characteristic-the voltage drop over it decreases by about 2 mV for every Celsius' degree of temperature rise. Also the reverse saturation current, I_S, is strongly dependent on temperature and doubles for every 8-10 degrees of rise in temperature, the latter being the cause for the former.

The straightforward way of achieving the temperature compensation would be using two diodes instead of only one and using the differential signal developing between these identically biased and thermally coupled diodes. The signal to be rectified is indeed applied to only one of the diodes, while the other is decoupled of the signal as well as possible.

Due to the patent problem referred to in the Section IV on page 52, the thermal compensation described above cannot be used in the RF rectifier (and also in power amplifier controller) chip. It will be interesting to look at two alternative ways of thermal compensation, which do not violate the patent in question. The first method is using the molybdenum resistor as temperature sensing element. The other method, taking advantage of the natural 'two-diode' construction of a bipolar transistor is totally new and invented by the author of this text.

IV.2.1. Compensation with Molybdenum resistor

The molybdenum layer is gate material in MAS9T technology and has geometrical and electrical properties that are listed in Table 19.

Table 19. Molybdenum gate material properties

Property	Min	Typ	Max	Unit
Drawn width	2.0	-	-	µm
Sheet resistance		0.35		Ω/□
Temperature coefficient		2390		ppm/°C

The properties of the molybdenum resistor could be used for thermal compensation of the RF rectifier. As the temperature coefficient (tempco) of the diode is negative and that for the molybdenum resistor is positive, the thermally compensated output signal can be generated by adding the voltage drop on the diode and on the molybdenum resistor with proper weights. The weights of the sum depend on the chosen rectifying device and the resistance of the molybdenum resistor.

There are several limitations in using the molybdenum resistor for thermal compensation. First of all, due to its very small sheet resistance, the area of the resistor will be considerable, contributing to circuit parasitics and consuming chip area. Also the current through the resistor must be quite high, to generate voltage drop much larger than the worst-case offset voltage of the summing OA (in case of OARTR34, the maximum offset voltage is 2 mV).

In this design, the resistance for the molybdenum resistor was chosen 1 kΩ and the voltage drop 100 mV (both quantities at room temperature, 27°C). This will yield an voltage variation of roughly 43 mV for 180°C temperature change (83.9 mV for –40°C and 127 mV for +140°C). It requires the weighting coefficient approximately (180*2)/43 ≈ 8.4, provided that diode tempco is –2 mV/°C. The thermal signal generating circuit is in the Figure 50 below.

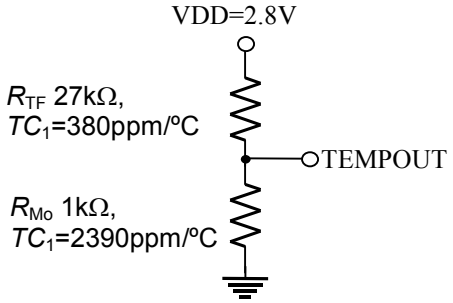


Figure 50. Temperature measurement with molybdenum resistor

The temperature dependence of other components (thin-film resistors, OA parameters) should not be forgotten and the weighting coefficients should be fine-tuned separately for each schematic containing thermal compensation with molybdenum resistor.

IV.2.2. Compensation with a BC-junction of a BJT

The idea of using the base-collector junction of an bipolar transistor is based on the idea that is available in every textbook containing the basics of bipolar transistors. Namely, the transistor could be represented as two diodes with a common anode (*npn*) or common cathode (*pnp*). From this point, it is easy to go forward. As we plan to use the base-emitter junction for RF rectification – recall that the RF signal is fed from emitter terminal – the BC junction is there unused and why not use it as a thermal compensation diode? The main advantage of this thermal compensation scheme is that the BC and BE diodes are strongly thermally coupled, and the two main disadvantages are that they are tightly electrically coupled too, and the thermal characteristics of the two junctions are not identical due to their differing areas and impurity concentrations. The principal schematic of this thermal signal generation method is in the Figure 51 below.

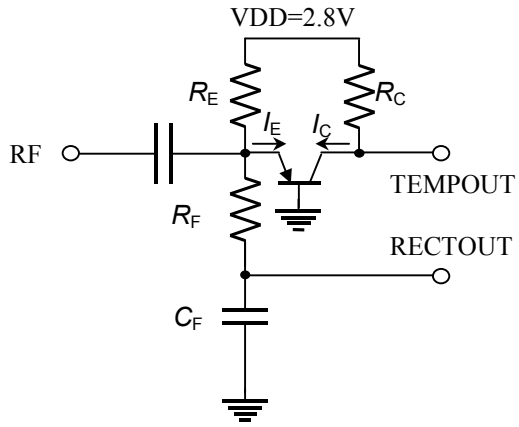


Figure 51. Thermal compensation with BC junction

Experimentation with the simulator show though, that the thermal compensation can be achieved in a manner similar to that of the thermal compensation involving molybdenum resistor, with the difference that the two signals should be subtracted in this case, since the tempco's of the both junctions of the bipolar transistor have the same sign.

In both thermal compensation schemes, the weighting coefficients should be found iteratively by finding the DC operating points versus temperature and re-calculating the weighting coefficient from the simulation results. Several iterations might be needed, and also the loading effects should be taken into account.

IV.3. Choosing rectifier structure

Initially, there were 8 possible rectifier structures developed. Among them those schematics were chosen which satisfy the following conditions:

1) Output signal is ground-referenced;
2) RF input signal can swing below negative supply voltage;
3) RF input signal is fed to the emitter of the rectifying transistor;
4) Output signal must go to negative direction when the RF input power increases.

Due to the RF input signal swing requirement, which allows the RF signal swing below negative supply rail, a special I/O pad is required. In the RECTIF1,2 and also in this ALDI1-3 project, a negative voltage pad from cell library was used. It has only one ESD protection diode against VDD. This same pad has been also used in MAS9142, where it has been proved to be suitable for this application.

With these goals in mind, the 8 rectifier structures were critically assessed and three of them were selected for further, detailed design. In following, all 8 initially designed structures are presented with their possible merits and drawbacks listed under the respective figure. The three selected rectifiers are then shown in a separate subsection with their final schematics.

The emitter current of all the rectifiers was chosen to be 30 μA.

IV.3.1. Initial rectifier schematics

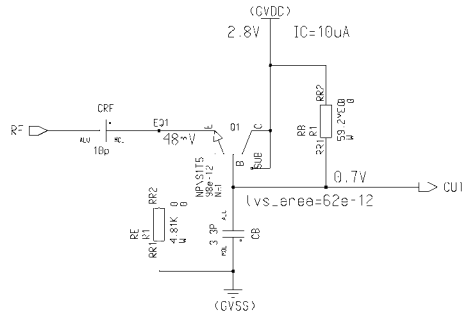


Figure 52. NPNS with grounded base

The main drawback of the circuit in Figure 52 is that it uses resistors of extremely large values, which causes large parasitics and layout area overhead. This schematic is discarded from further design.

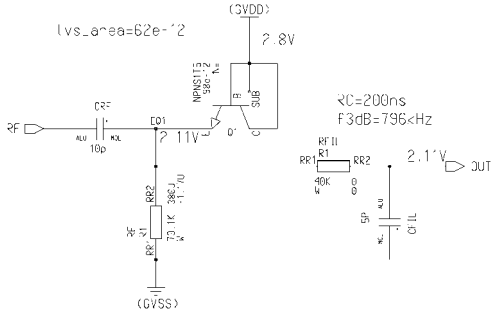


Figure 53. NPNS with base to VDD

This schematic (Figure 53) puts most of the RF current through VDD-line, and may cause substrate cross-talk problems, as the substrate is at VDD potential in MAS9 technologies. It is a feasible schematic in a sense that the input RF amplitude is not limited by the schematic itself, but only by the I/O pad. Since the output signal is referenced to VDD, this schematic is discarded.

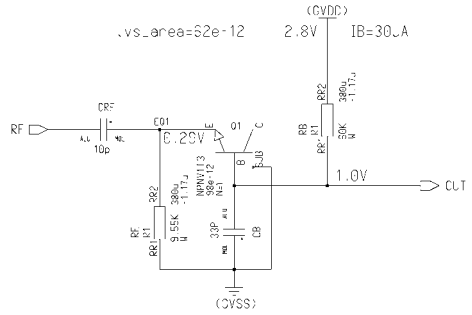


Figure 54. NPNV with grounded base and open collector

Figure 54: RF input amplitude is limited only by the I/O pad, output goes in negative direction with increasing input amplitude and the RF current uses ground as return path. This schematic is selected for further design and used in conjunction with molybdenum resistor thermal compensation.

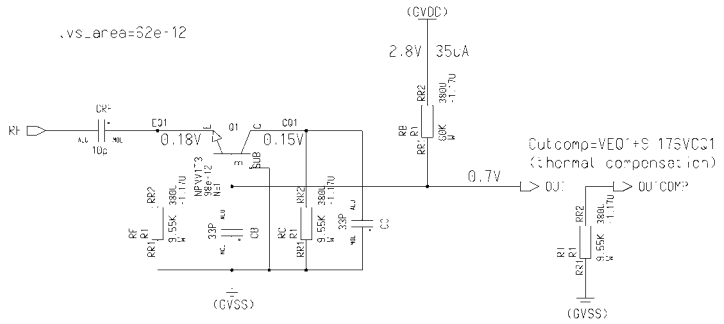


Figure 55. NPNV with grounded base and collector

This schematic (Figure 55) uses the BC diode for thermal compensation. While this is the merit, the major drawback of this circuit is that the input RF amplitude it can handle is limited to approximately VDD–1.3 V. This schematic is discarded.

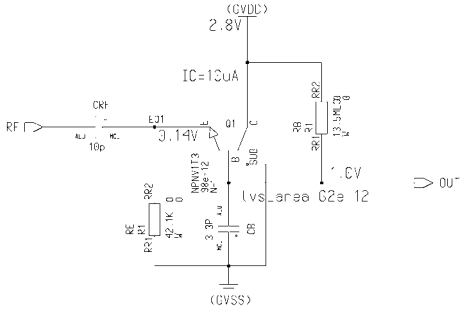


Figure 56. NPNV with grounded base and collector to VDD

Figure 56: This is the exact counterpart of schematic from Figure 52. The only difference is the type of the recifying device. Due to that, the schematic has all the drawbacks discussed earlier and will thus be discarded.

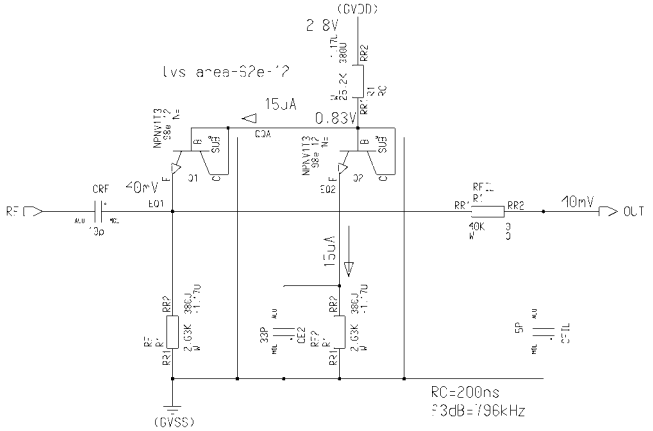


Figure 57. Two NPNV-s with split functions

The schematic in Figure 57 has two devices with separate functions: one for rectification and the other for thermal compensation. It has two major drawbacks, the first being that this kind of arrangement is patented by Motorola [252] and also that the RF current returns by both VDD and GND lines. This schematic is discarded.

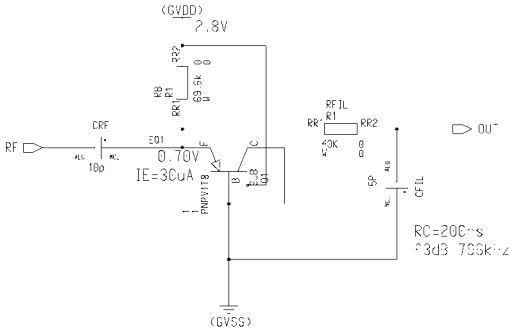


Figure 58. PNPV with grounded B and C

The PNPV arrangement (Figure 58) agrees well with the demands posed at the beginning of this section. The design of this schematic is continued.

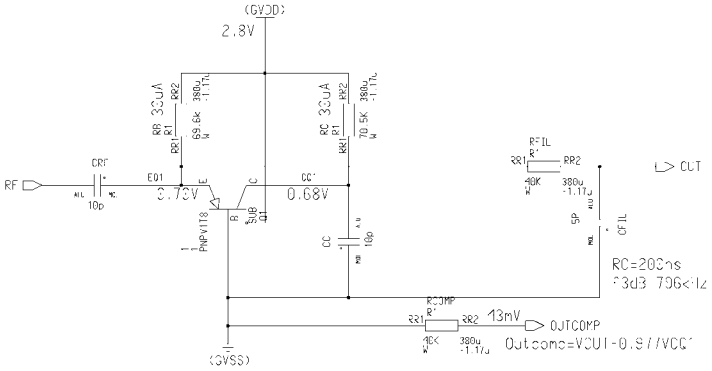


Figure 59. PNPV with grounded base and BC diode as thermal compensation

This is the most interesting schematic of those designed. It incorporates a PNPV transistor, the BE junction of which serves as rectification diode and the BC junction measures temperature (Figure 59). The design of this schematic is continued.

IV.3.2. Final rectifier schematics

From the initial 8 rectifier schematics, 3 rectifier structures were chosen. Two of them are using vertical PNP transistor as a rectifying element, one employs vertical NPN. The schematics are shown in Figure 54, Figure 58 and Figure 59, respectively. Two rectifiers are thermally compensated with the molybdenum resistor compensation scheme, one structure with PNP transistor is using the B-C junction of the rectifying transistor for that purpose.

Another important point is that rectifier and thermal compensation circuit must be designed to drive 80 kΩ load resistance. This is the input resistance of the adding circuitry employing the OARTR34 opamp and is selected as a compromise to keep the error due to input currents of the OA reasonably small. The selected rectifiers are shown in the following three figures.

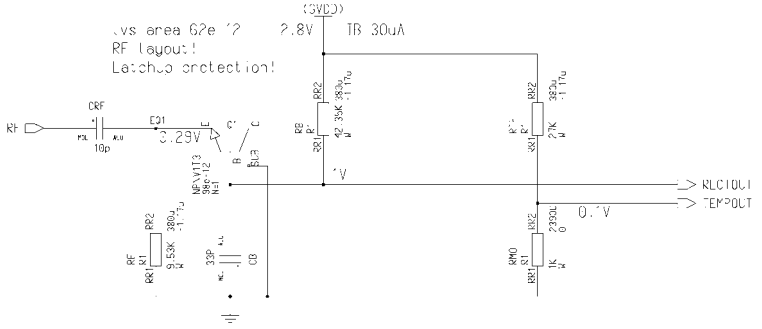


Figure 60. NPNV with grounded B and open C, Mo resistor compensation

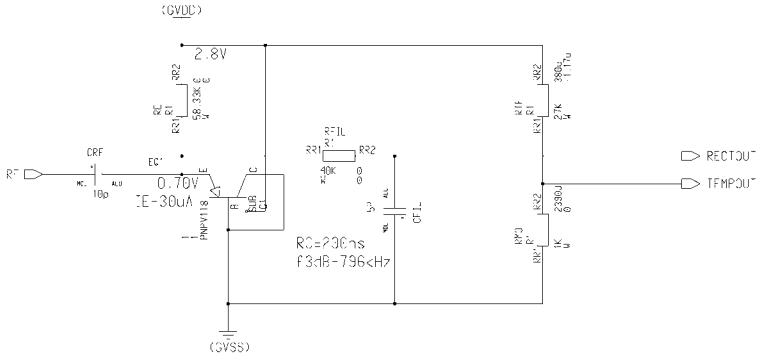


Figure 61. PNPV with grounded B and C, Mo resistor compensation

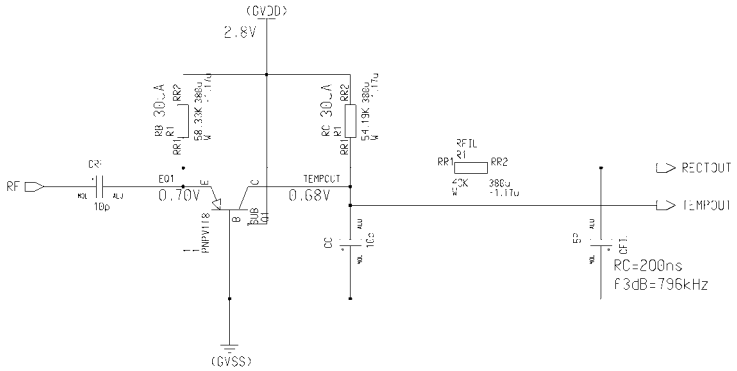


Figure 62. PNPV with grounded B and BC diode compensation

IV.4. Analog processors

Each of the three rectifiers has its own analog processor to perform the weighted sum operation on the rectifier output signal and the measured temperature signal to achieve thermal compensation. All rectifiers and analog processors need stabilised supply voltage 2.8V.

Due to the loading and also the thermal dependence of the biasing resistors, the weighting coefficients are different from those calculated in section IV.1.

The formulas of calculating the voltage transfer functions are shown in the respective figures (Figure 63, Figure 64 and Figure 65). With the processors with three inputs, it was not possible to satisfy simultaneously the transfer coefficient and input resistance requirement, so the input resistance of the TEMP input is 58 kΩ. This difference has been taken into account and the schematic of corresponding rectifier was adjusted accordingly.

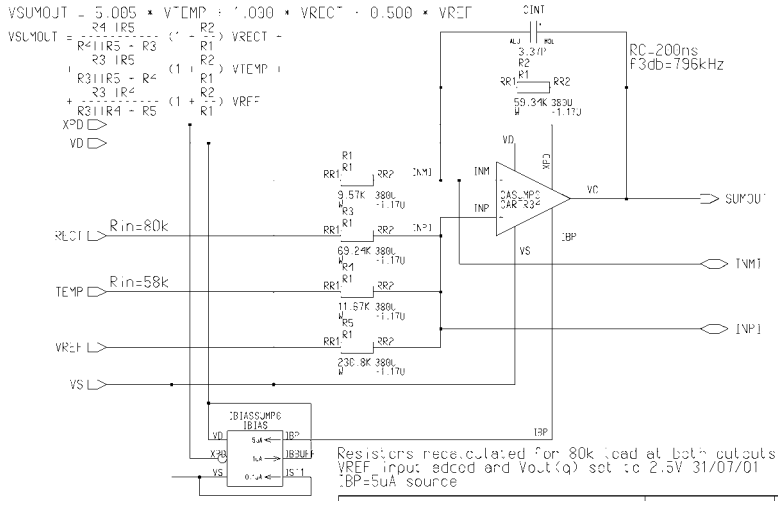


Figure 63. SUMN0: analog adder for use with NPNV rectifier

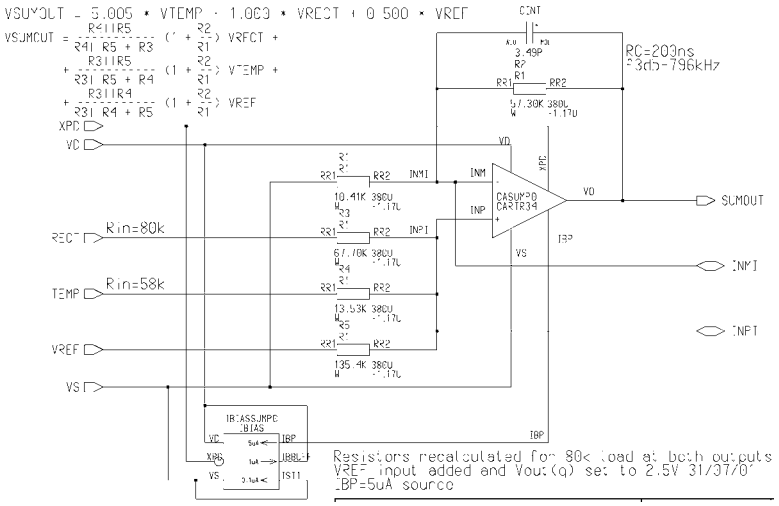


Figure 64. SUMP0: analog adder for use with PNPV rectifier+Mo R comp.

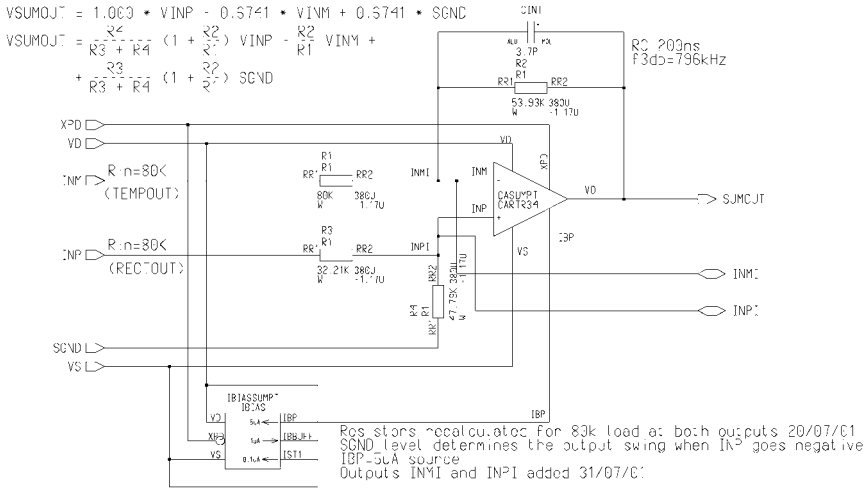


Figure 65. SUMPT: analog adder for use with PNPV rectifier with BC diode comp.

IV.5. Results of thermally compensated RF rectifier design

Three RF half-wave rectifier/power detector schematics were chosen to be put on silicon. Both PNP and NPN transistors are used, and both molybdenum resistor and BC-junction thermal

compensation schemes are applied. MAS9T technology was used with R10Kb resistor process, standard bipolar transistors and capacitors.

The simulation results will be verified with measurements, which are reported in the subsequent section.

The following Table 20 indicates, which structures are on which of the three ALDI chips:

Table 20. Contents of ALDI1-3 chips

Chip name	Identification resistor value (pins 11 & 12)	Rectifier name	Thermal compen-sation method	Analog processor name
ALDI1	10kΩ	rpvb0ct (Figure 62)	BC junction	sumpt (Figure 65)
ALDI2	40kΩ	rpvb0c0 (Figure 61)	Mo resistor	sump0 (Figure 64)
ALDI3	160kΩ	rnvb0c0 (Figure 60)	Mo resistor	sumn0 (Figure 63)

Identification resistor is provided as a measure of precaution in the case when the structures should mix with each other during encapsulation. As an example, the layout of ALDI2 chip is shown in Figure 66.

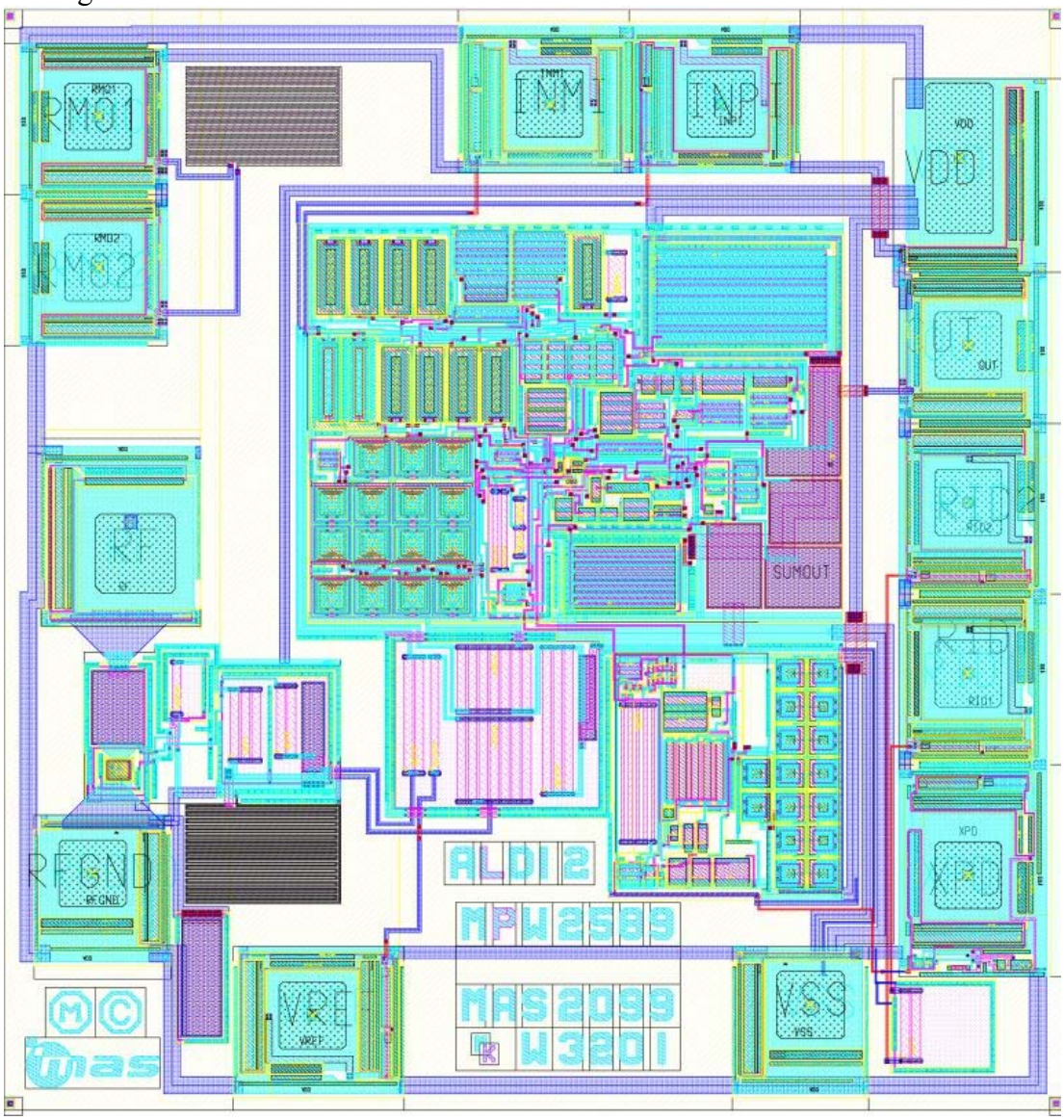


Figure 66. ALDI2 layout

IV.6. ALDI1-3 measurements

The measurements were carried out in 4th floor laboratory of MAS OY. The measurement equipment was the MAS testing system, a HP ESG2000 RF generator and Thermonics T2500 temperature forcing system. All the equipment was interconnected with the GP-IB instrumentation bus. The ALDI1-3 chips were encapsulated in TSSOP16 packages and soldered to the 9142_RF_PCB_EXTRA printed circuit boards. A modified MAS9142 test program was used to set the DC voltages to the DUT. The frequency and amplitude of the input signal were swept and the measurement results were read with a dedicated program (or virtual instrument, as it is called in LabVIEW environment).

The measurements were carried out in two-day period: 04-05/01/2002. Following quantities were measured for each of the ALDI1-3 chips (Table 21):

Table 21. ALDI1-3 measurement specification

Date	Nr	What was measured	Start	Stop	Step	Unit	Temperature
04/01/02	1	Frequency sweep: RF level is +6 dBm	100	2000	5	MHz	Room
	2	Amplitude sweep: frequency is 900 MHz	–30	10	0.5	dBm	Room
05/01/02	3	Frequency sweep: RF level is +6 dBm	100	2000	5	MHz	+125 °C
	4		100	2000	5	MHz	+85 °C
	5		100	2000	5	MHz	+25 °C
	6		100	2000	5	MHz	0 °C
	7		100	2000	5	MHz	–40 °C
	8	Amplitude sweep: frequency is 900 MHz	–30	10	0.5	dBm	+125 °C
	9		–30	10	0.5	dBm	+85 °C
	10		–30	10	0.5	dBm	+25 °C
	11		–30	10	0.5	dBm	0 °C
	12		–30	10	0.5	dBm	–40 °C
	13	Temperature sweep: 900 MHz, +6 dBm	–40	+100	10	°C	-
	14	Surface plot: freq and ampl. sweep	–22	11	1	dBm	Room
			100	2000	25	MHz	

In table Table 21 above, ‘room temperature’ means that no temperature control is applied.

In the following, the graphs of the measurement results are presented.

IV.6.1. Rectification characteristics

In this subsection, the 3-D surface plots of the amplitude and frequency responses for all three chips, ALDI1-3 are shown. A normalized version of each characteristic is presented. The normalization is done with respect to zero input signal and the results are plotted in logarithmic scale. In all three rectifiers, the output voltage has a value near the positive supply rail without the input signal and the output will go to negative direction when the input signal is applied.

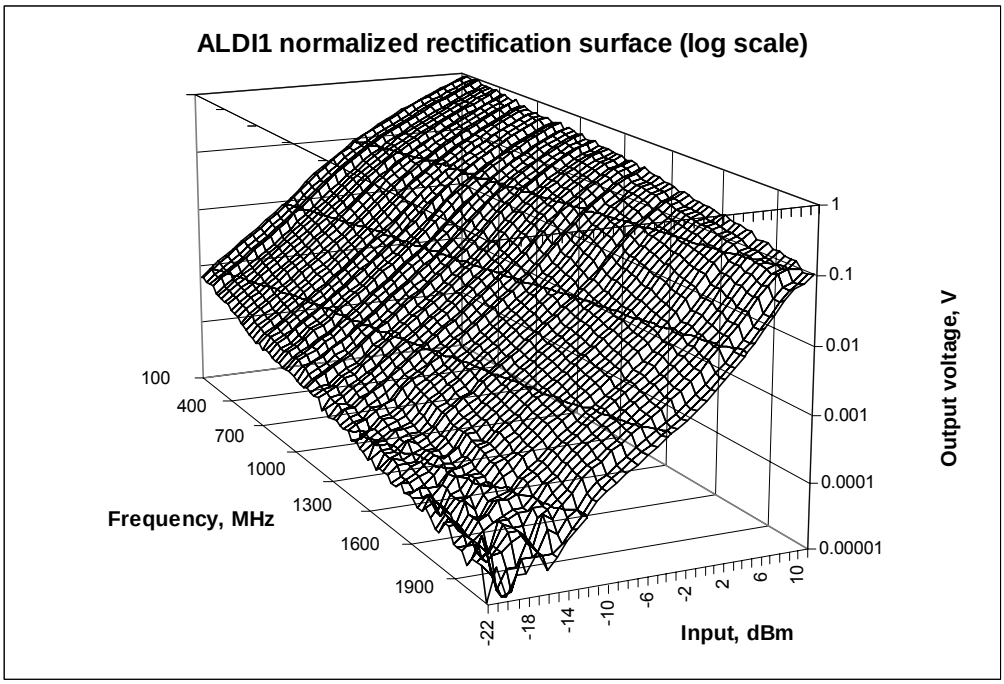


Figure 67. ALDI1 normalized frequency/amplitude response (log scale)

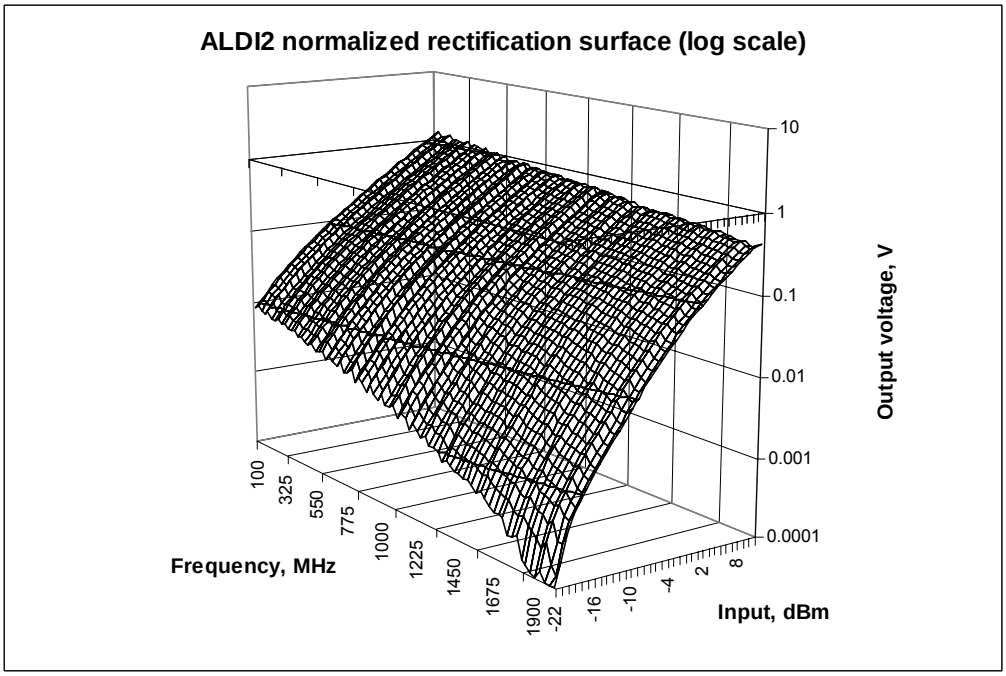


Figure 68. ALDI2 normalized frequency/amplitude response (log scale)

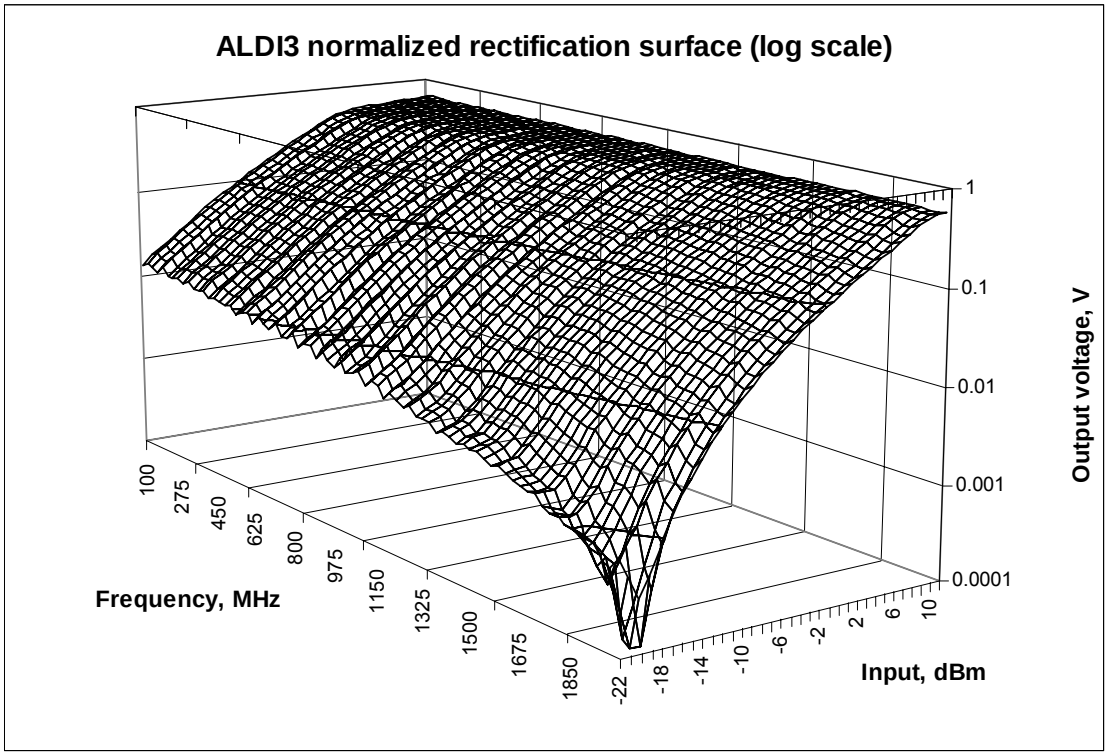


Figure 69. ALDI3 normalized frequency/amplitude response (log scale)

IV.6.2. Frequency responses

The frequency responses shown in this section are measured at +6 dBm input level (as read from the generator display) and at five temperatures: –40, 0, +25, +85 and +125°C. The frequencies were from 100 to 2000 MHz, with 5 MHz step.

At the end of this section, the summary graph will be presented, where the frequency responses of all ALDI1-3 are plotted in the same plot.

Several interesting points can be made based on these frequency response graphs. At the first glance, it is quite clear that the thermal compensation is not working for ALDI3. The same way, the best compensated is ALDI2, with a slightly smaller tolerance range than ALDI1.

In Figure 70, the differences between the measurement results in (almost) identical conditions, but in two different days are shown. The slight difference between the measurements was that on 04/01/2002, there was no temperature forcing used, and measurements were performed at room temperature. On 05/01/2002, on the contrary, the temperature was forced to be +25°C. This might introduce some slight temperature error, as it can also be seen from the graph.

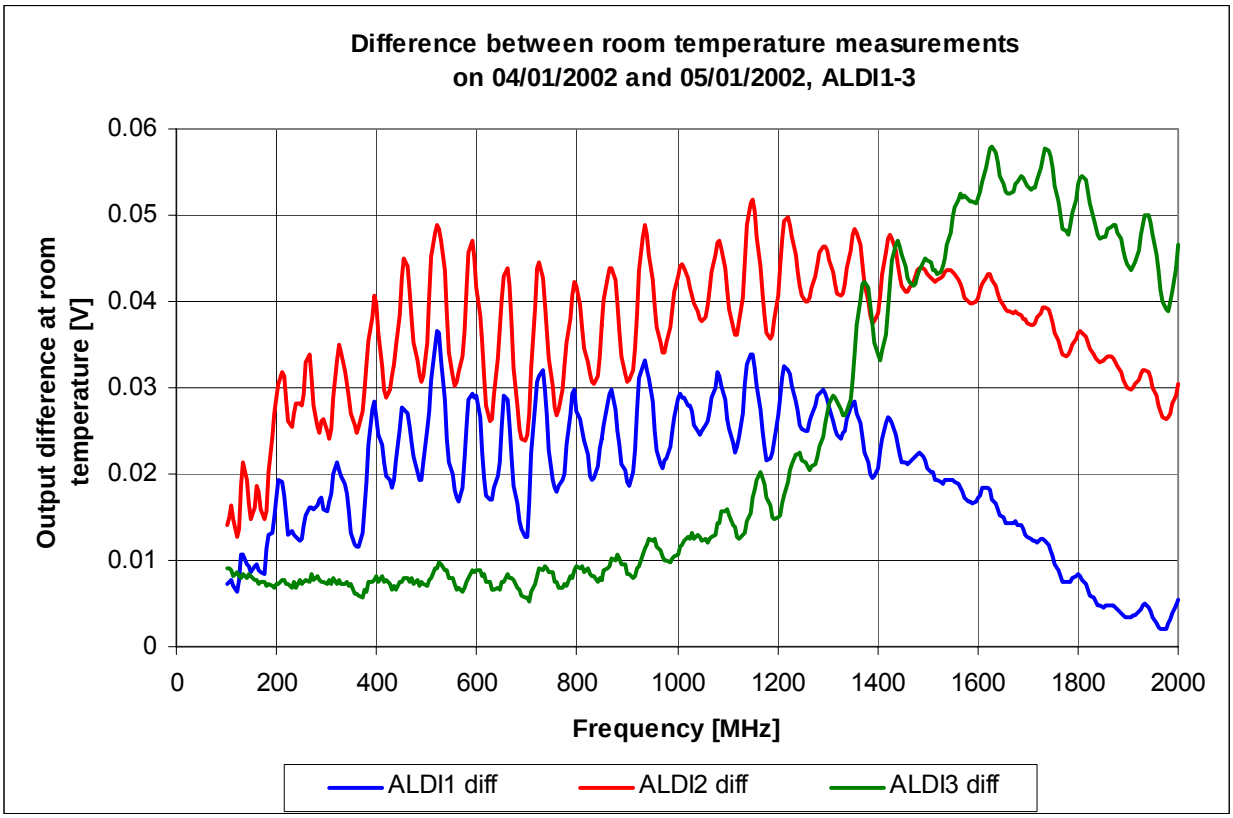


Figure 70. Differences in measurement results on two subsequent days

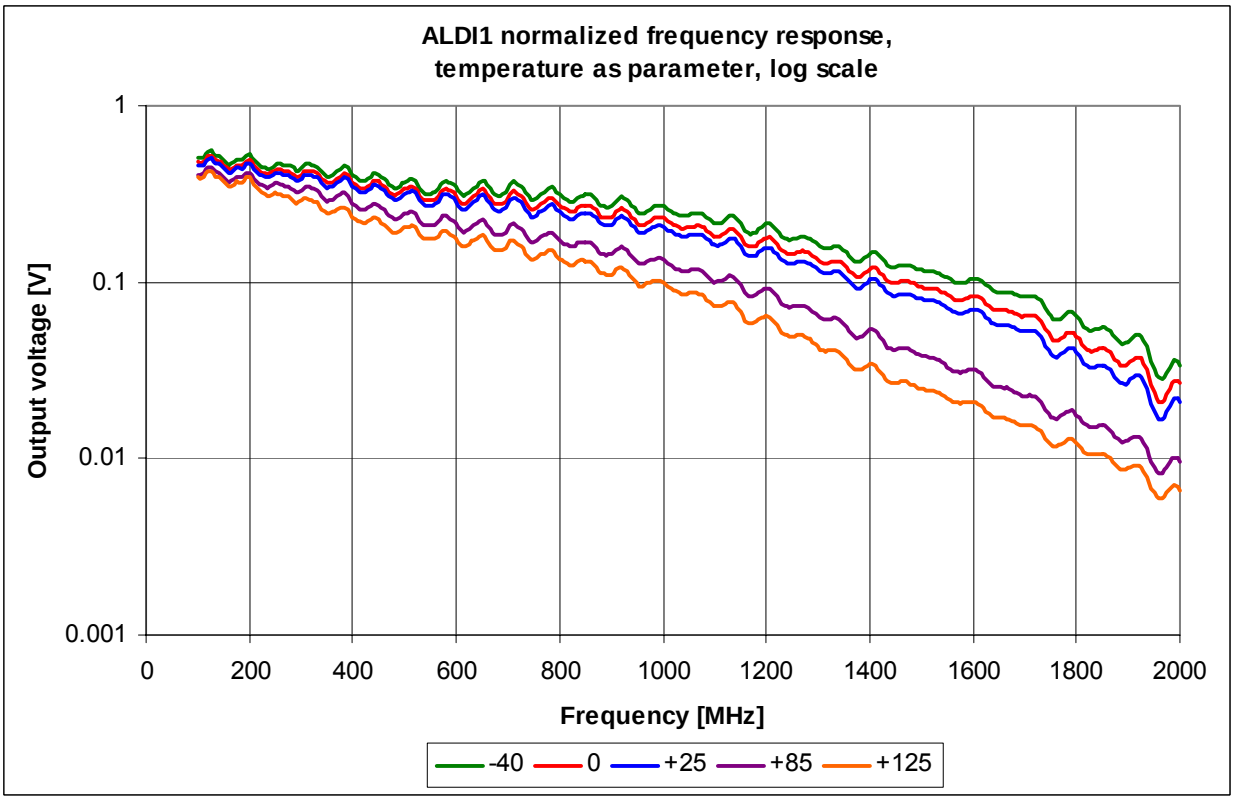


Figure 71. ALDI1 normalized frequency response at five temperature points (log scale)

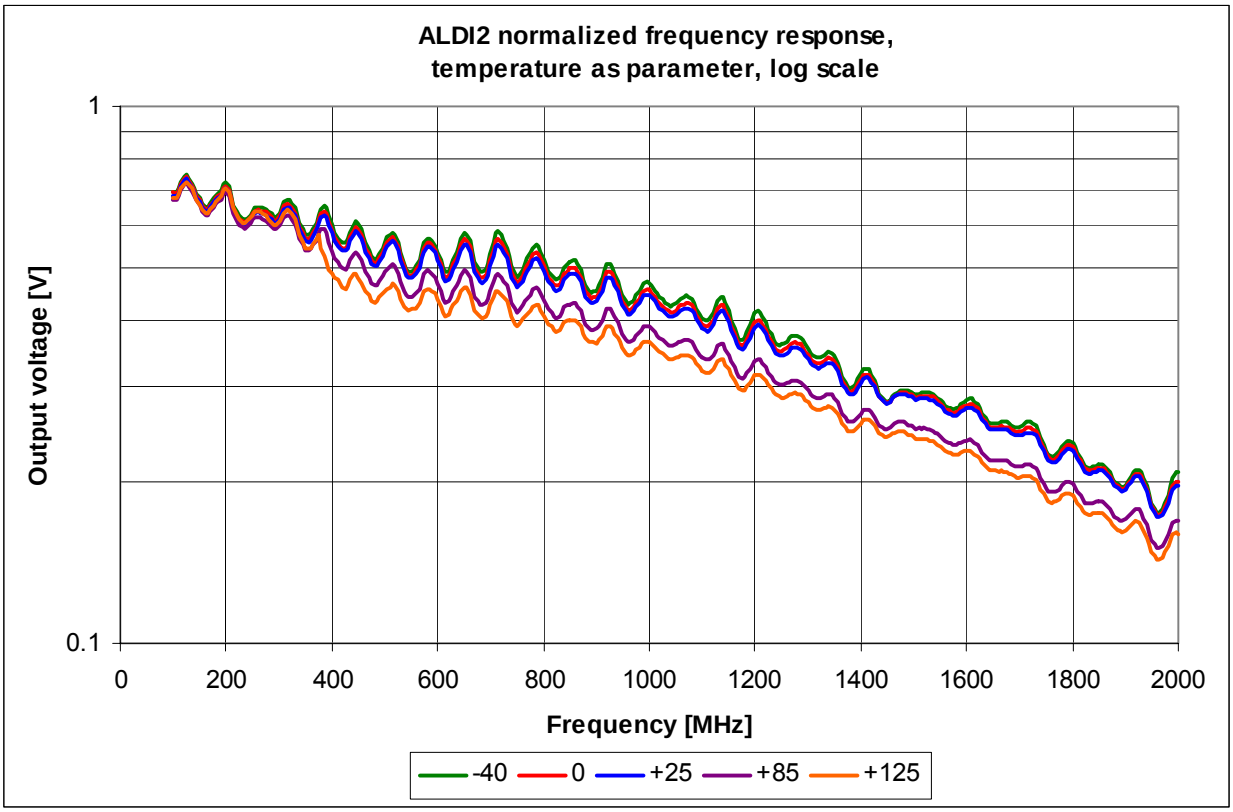


Figure 72. ALDI2 normalized frequency response at five temperature points (log scale)

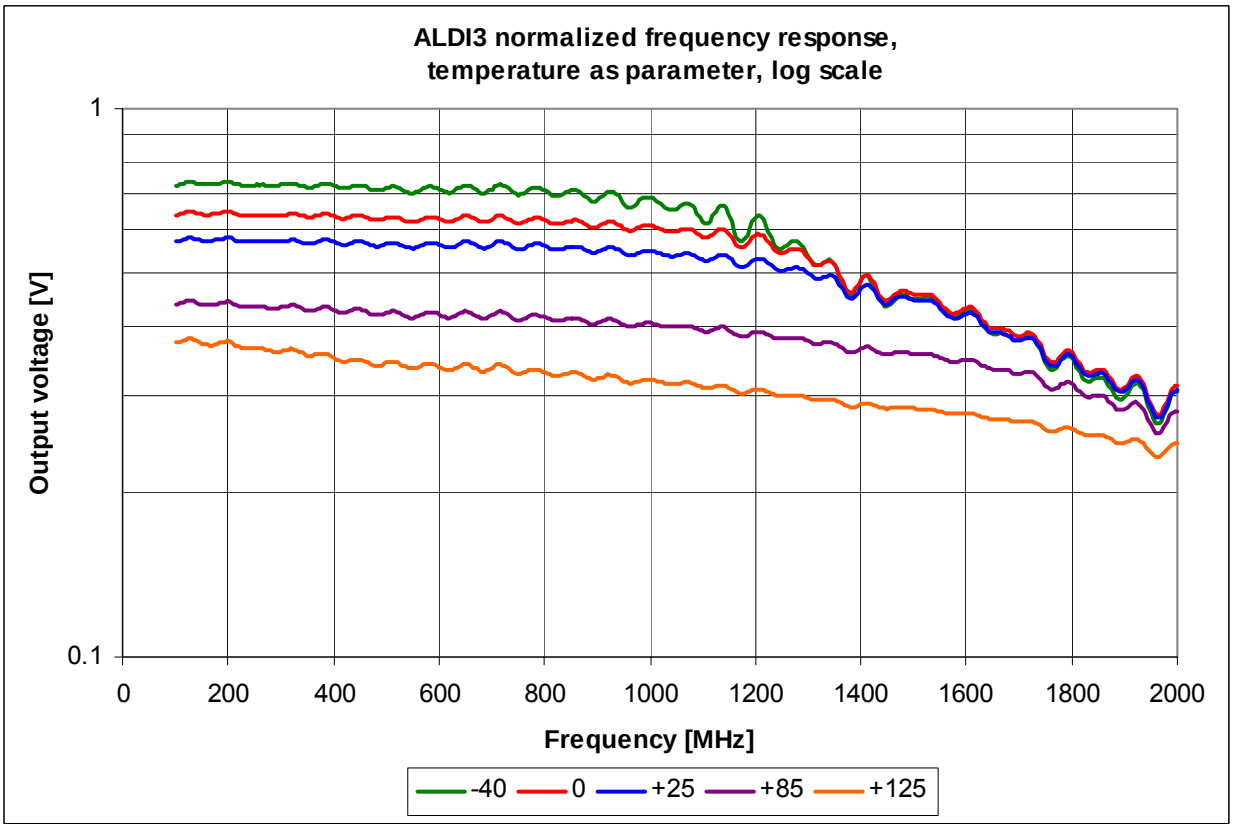


Figure 73. ALDI3 normalized frequency response at five temperature points (log scale)

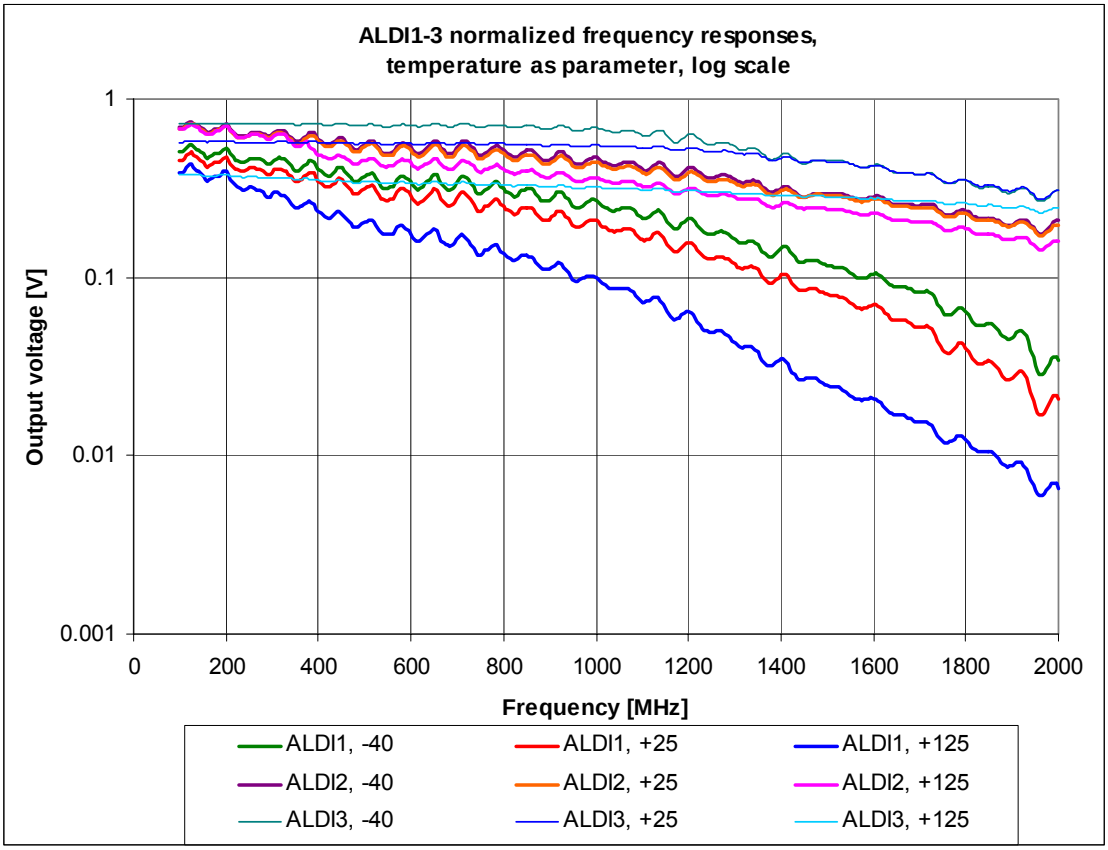


Figure 74. Comparison of ALDI1-3 normalized frequency responses at three temperature points (log scale)

IV.6.3. Amplitude responses

The amplitude responses were measured at 900 MHz frequency, at the temperatures –40, 0, +25, +85 and +125°C. The measurements were made at amplitudes from –30 dBm to +10 dBm. The amplitude step used was 0.5 dBm.

At first, the DC thermal compensation can be estimated. As there is no detectable output signal with the –30 dBm input, it was assumed to be 'zero-input' and the output DC level was then plotted against the temperature. These three graphs are shown below along with the mean values of the output and its standard deviation. It is quite interesting to note, that the best thermal compensation is by the ALDI1, where the DC no-signal output almost does not depend on the temperature. It should be noted though, that the measurements were performed at constant supply voltage, which did not depend on the temperature either. The second best DC compensated is ALDI2, where the standard deviation of the output is about an order of magnitude bigger than in ALDI1. The worst in this sense is ALDI3, with very large variance in the DC level.

It is also interesting to note that there is a qualitative difference in the shape of the amplitude responses. Notably different is ALDI1, with the most similarity to the simulation results. The ALDI2 and ALDI3 responses are rather similar to each other. Finally, again the measurement results and the normalized results are shown in the graphs.

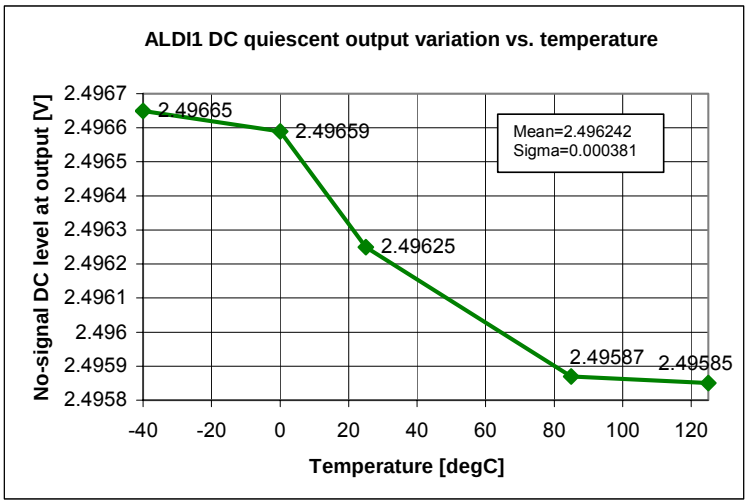


Figure 75. DC thermal compensation of ALDI1

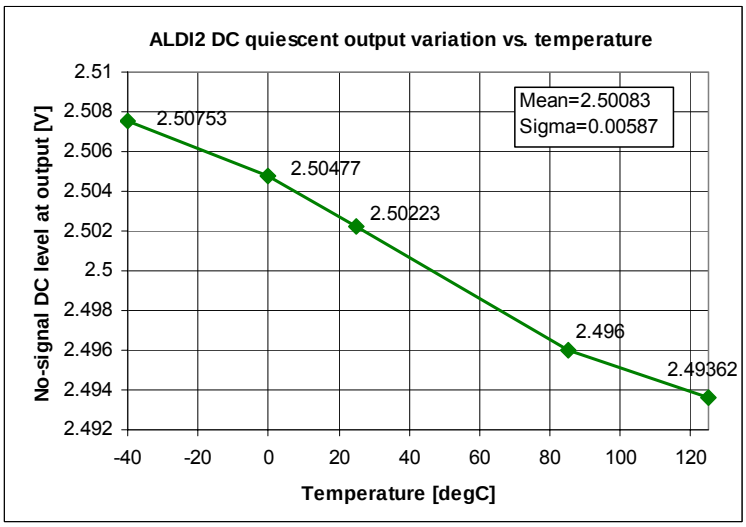


Figure 76. DC thermal compensation of ALDI2

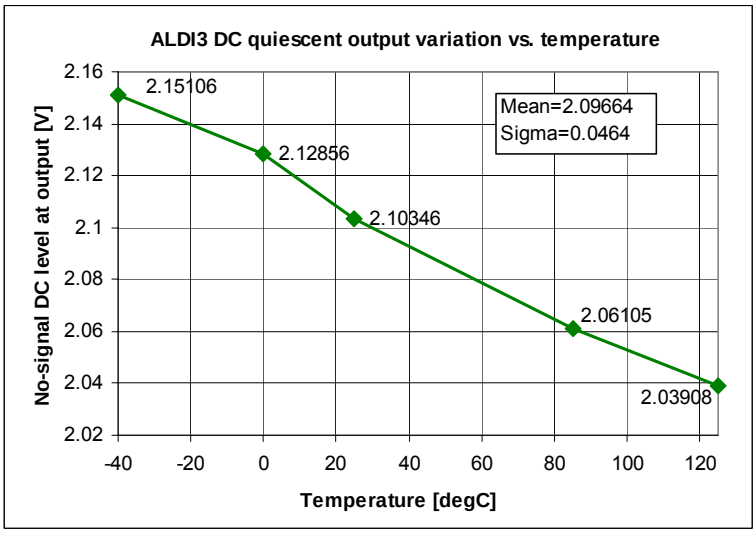


Figure 77. DC thermal compensation of ALDI3

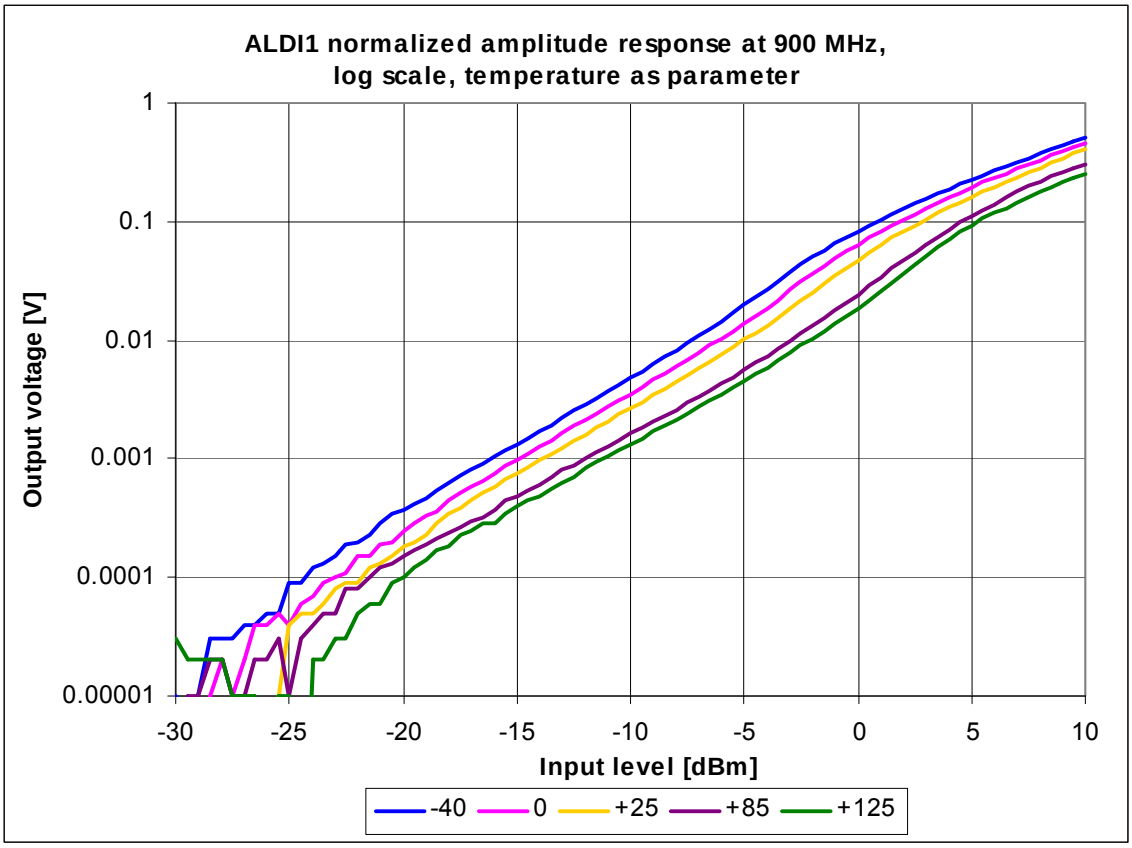


Figure 78. ALDI1 normalized amplitude response at five temperature points (log scale)

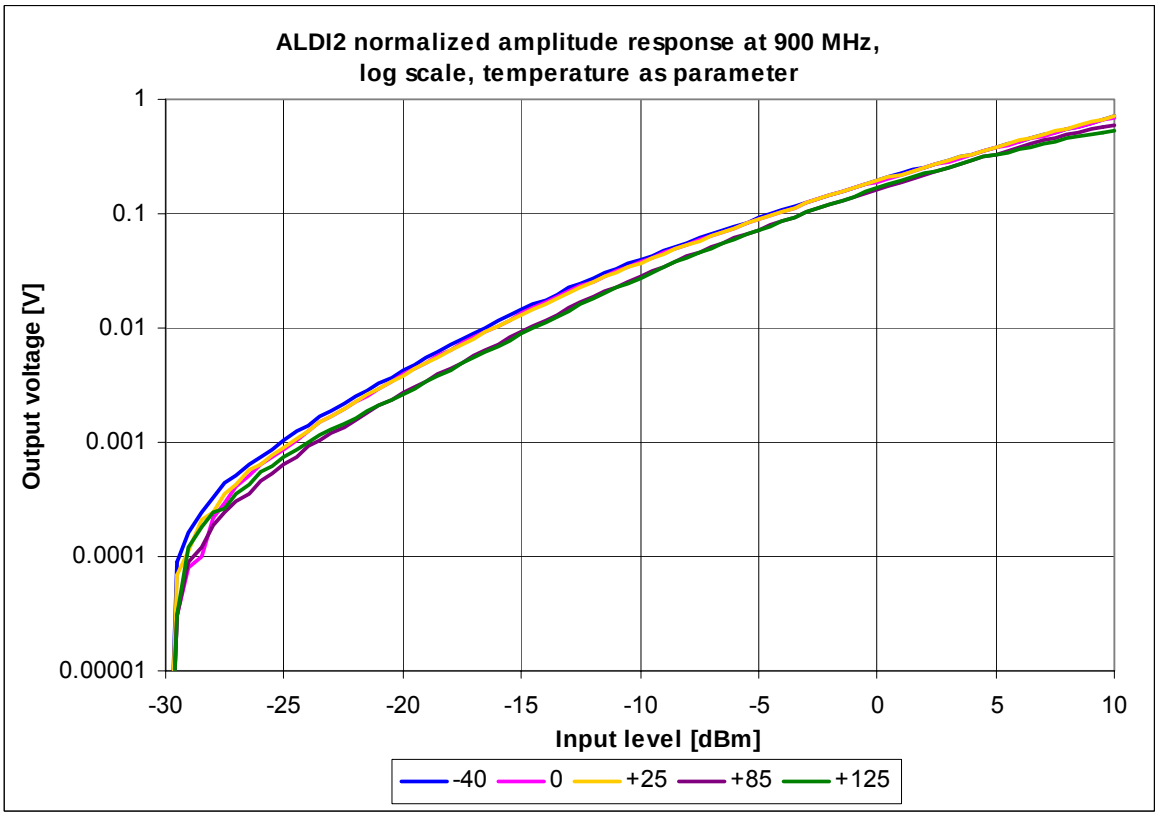


Figure 79. ALDI2 normalized amplitude response at five temperature points (log scale)

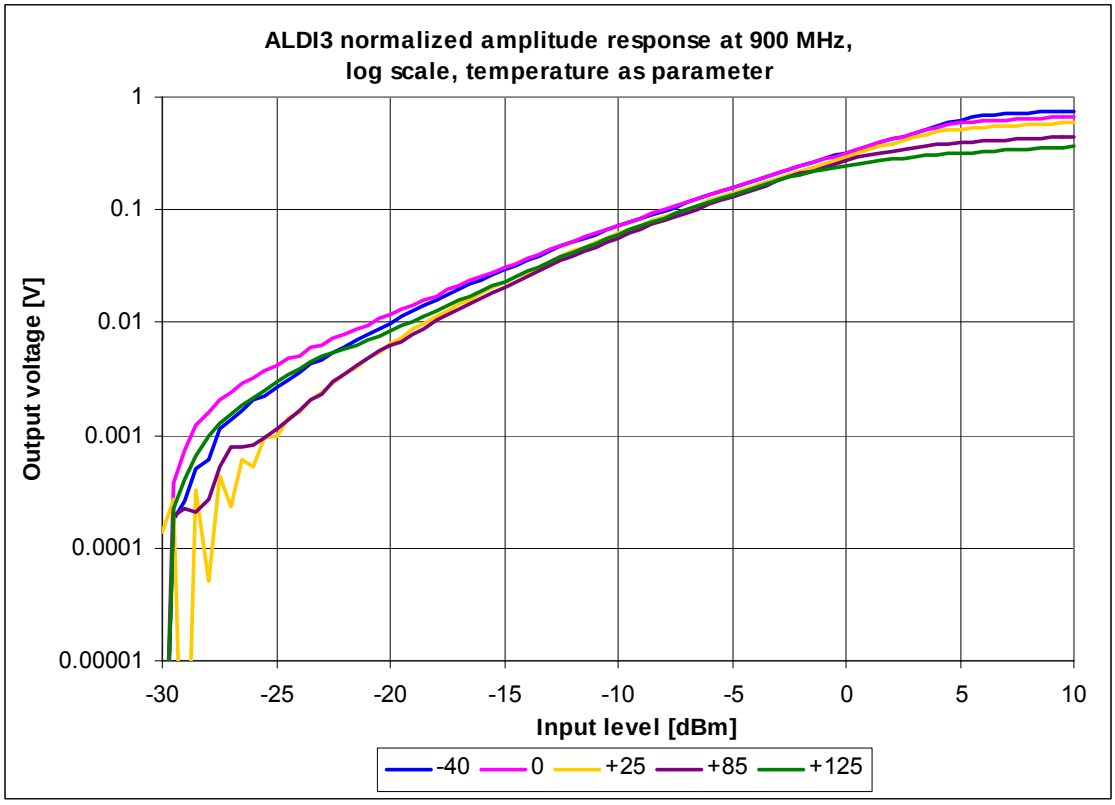


Figure 80. ALDI3 normalized amplitude response at five temperature points (log scale)

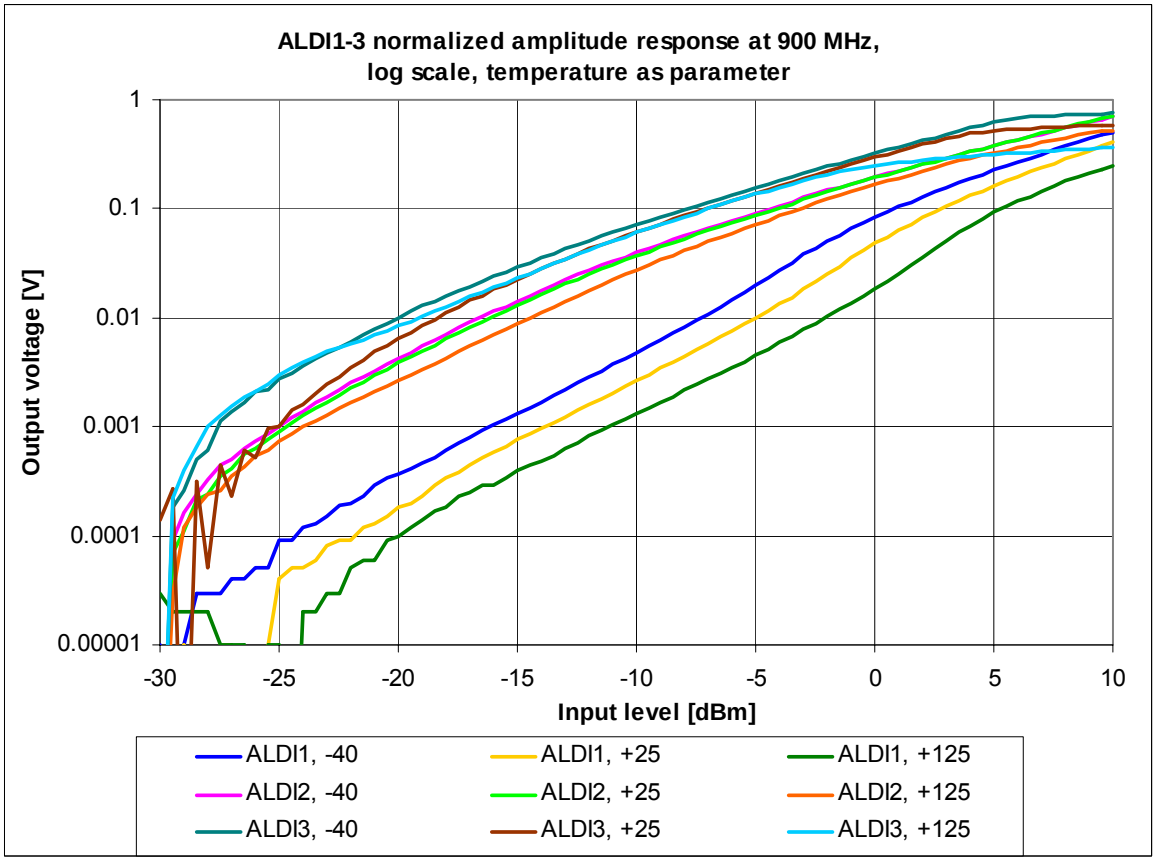


Figure 81. ALDI1-3 normalized amplitude responses at three temperature points (log scale)

IV.6.4. Temperature responses

This is the third kind of sweep which was performed during the measurements. Now the frequency is fixed at 900 MHz, also the amplitude is fixed, at +6 dBm. Then the temperature is swept from –40 to +100°C in 10°C steps.

From this sweep it is clear that the best rectifier from the point of view of thermal compensation is ALDI2, where the variance of the output level is the least.

As for the previous sweeps, here also two kinds of figures are presented; first, the measurement results and then the normalized version of these. The results of all ALDI chips are shown on the same graphs. This helps to compare the results more easily.

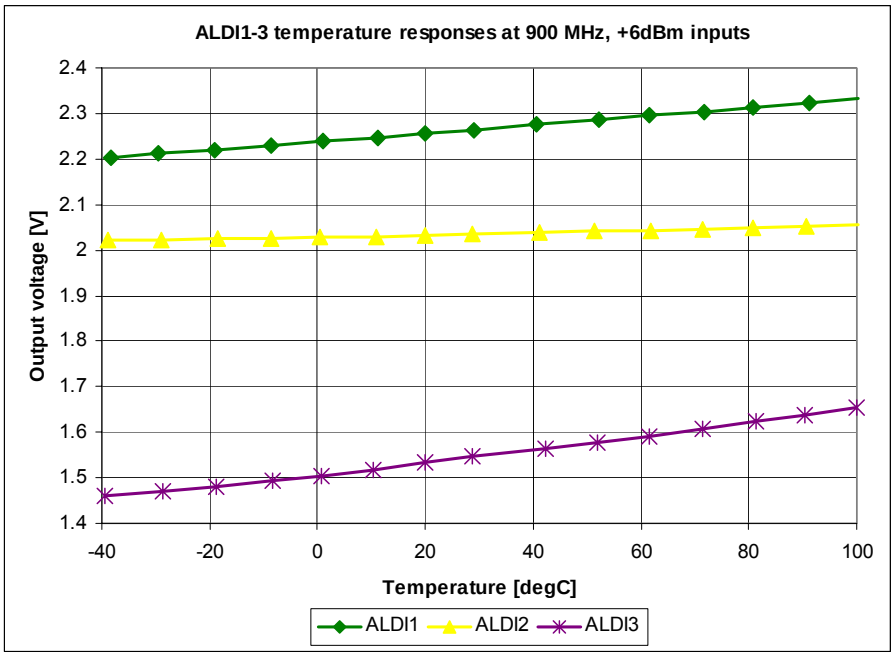


Figure 82. ALDI1-3 temperature responses

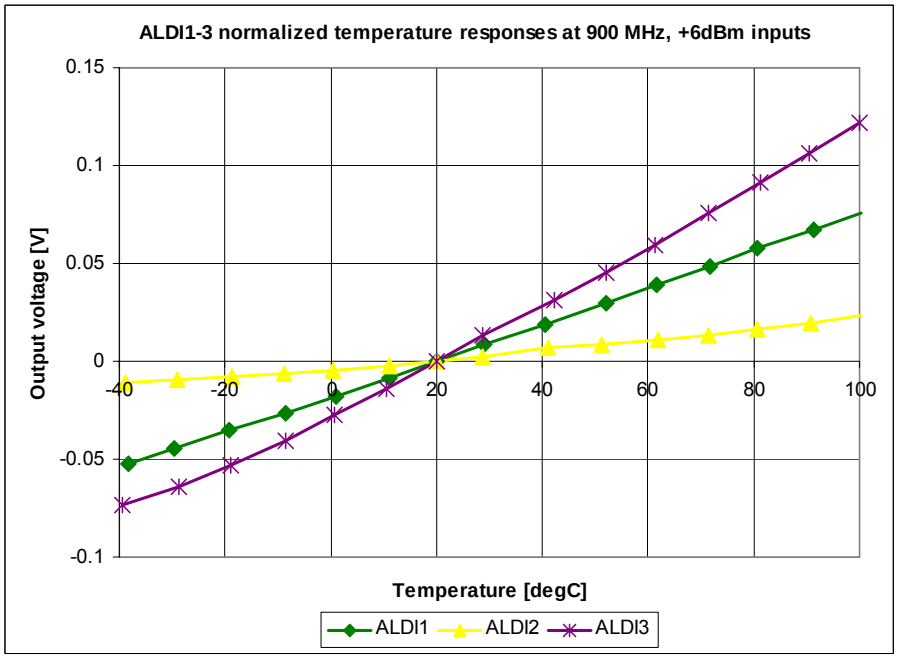


Figure 83. ALDI1-3 normalized temperature responses

IV.7. Conclusion of measurement results

Short conclusion: ALDI2 is the best rectifier for use in the power amplifier controlling chip.

Notes. Care must be taken in interpreting the measurement results shown here. There is notable package and PCB influence in the results, appearing as the ripple in the frequency response graphs (see Figure 71 through Figure 74). Yet the ripple is expected because the input impedance of the rectifier is not matched to the generator's output impedance, in this case, 50 Ω. This mismatch makes the rectification with MAS9 bipolar transistors possible in the first place.

An important notice can be made though. As the ALDI2 is the best rectifier, both in the point of view of the thermal compensation and flatness of the frequency response, the most suitable topology to be used for the rectification is that using the PNPV with grounded base and collector terminals, as shown in Figure 61. The most appropriate thermal compensation scheme here is the molybdenum resistor compensation, shown in the same figure. The analog processor, which combines the rectified and thermal signal is shown in Figure 64.

The DC thermal compensation is the best for the ALDI1 chip, as correctly predicted by the simulations. The compensation gets worse when the RF signal is applied. This BC-diode compensation will eventually become less attractive than the Mo-resistor compensation used in ALDI2 (and ALDI3), but it might find applications in another fields. Although the supply voltage of the ALDI1-3 was stabilized during the measurements, the ALDI1 output voltage without RF input signal only changed by about 800 μV, with standard deviation of 380 μV (see Figure 75).

V. Precision crystal oscillator thermal compensation design

This part of the Thesis concentrates on other method of reducing power consumption in mobile phone. As said before, the high-precision reference oscillator has rather high power consumption and requires comparatively expensive frequency reference, which is normally a crystal resonator. The idea here is to make use of the other crystal resonator which is also present in all modern mobile phones, namely, the real-time clock. Frequencies of these two crystals differ largely – usually, the reference oscillator uses AT-cut quartz resonator with 13.000 MHz oscillation frequency, while the real-time clock incorporates tuning-fork type low-frequency resonator of 32.768 kHz.

The idea to be verified in this and the next sections is to thermally compensate the lower-frequency oscillator so that its output could be used as the reference signal. The frequency upconversion will be done with a conventional phase-locked loop (PLL) arrangement. However, the PLL design will be out of scope of this Thesis.

The schematic under investigation is called DualOscillator and is shown in Figure 84.

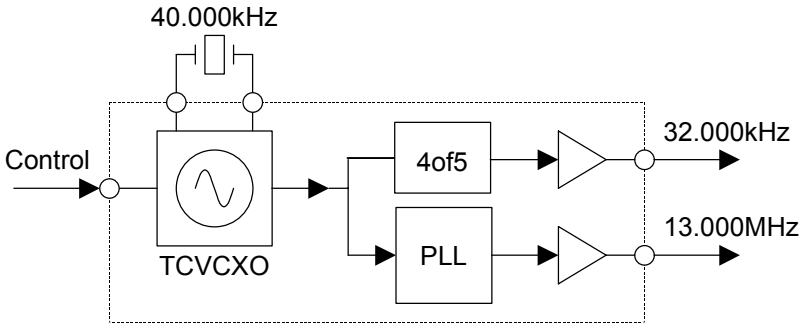


Figure 84. The idea of DualOscillator is to replace two oscillators (32 kHz and 13 MHz) with one TCVCXO and PLL

The block named '4of5' in Figure 84 is a pulse skipper. It skips every fifth pulse in the 40 kHz signal so that the average frequency at its output will be 32 kHz. The TCVCXO (thermally compensated, voltage controlled crystal oscillator) has the internal system-level construction as shown in Figure 85.

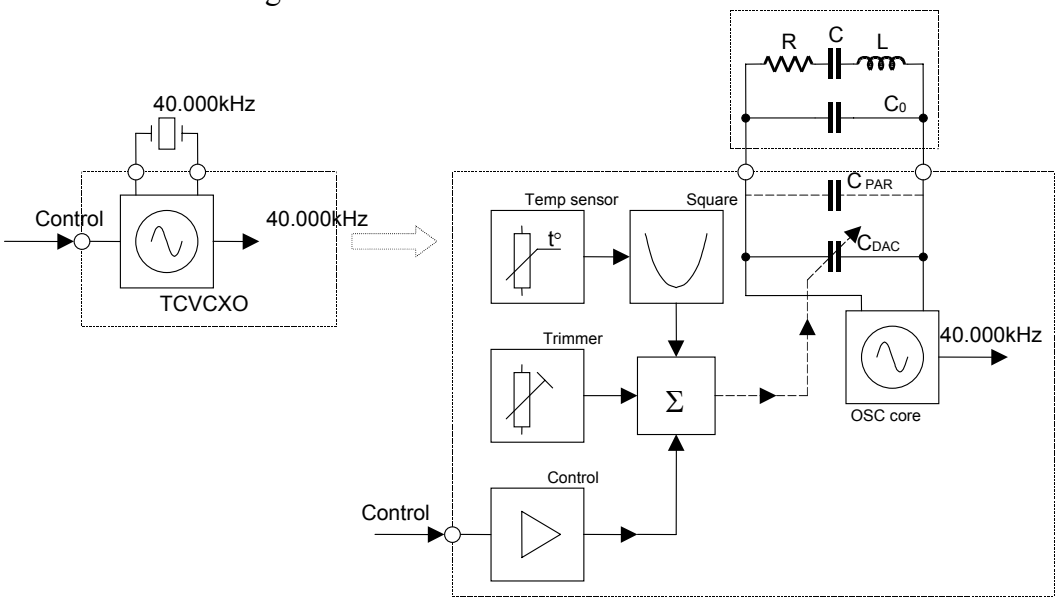


Figure 85. TCVCXO: Model for thermal frequency control

The block diagram of the PLL is shown in Figure 86. This will explain the choice of the 40 kHz quartz resonator: to have the integer-N PLL, the PLL reference and output frequencies must have integer relationship.

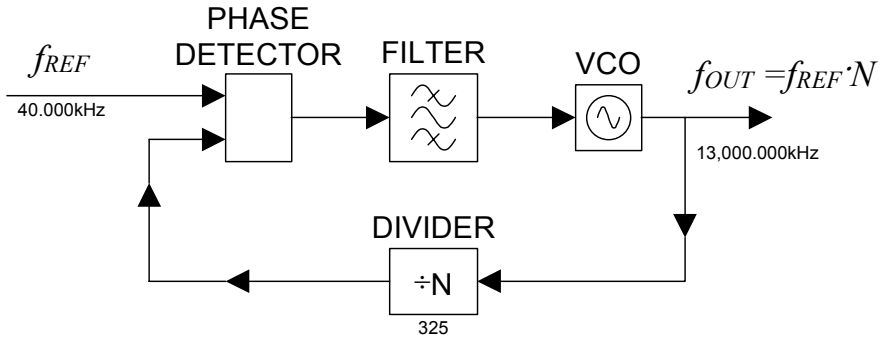


Figure 86. Block diagram of the PLL

It is important to have the integer N in the PLL. The use of rational-M/N PLL is not feasible, since it involves also division by M for the PLL reference signal. As the frequency of this signal is already low, dividing it down will yield enormous problems in VCO design, as its free-running specifications for phase noise and stability must be very tight. In addition, the filter design will be more complicated, since the elements of the filter will have larger values due to the lower frequency.

The non-integer PLL has also been studied. The use of 'uneven' pulse train as the feedback signal to the phase detector will have devastating consequences on the PLL output phase noise. This is caused by the fact that the switching edge from the divider arrives at the phase detector at a time that is not a full multiple of the periods of the reference frequency. This again will be reflected by the system so that the VCO will be overdriven to either direction – to compensate for its lead or lag. The average frequency will be correct, but instantaneous frequency will not and phase noise will be enormous.

The following discussion skips the problems of PLL design details and concentrates on the design of thermal compensation for the crystal oscillator core. The design of oscillator core itself is out of scope and will not be handled here.

V.1. Thermal compensator design flow

The goal of this section is to find the temperature-dependent load capacitance for a crystal oscillator (XO) so that the resulting frequency thermal behavior of the thermally compensated XO (TCXO) would be maximally flat.

The following summarizes the calculations of required load capacitance temperature dependence and varactor control voltage dependence of a crystal oscillator, when the temperature dependence of the resonator is known. In this schematic, the temperature sensor is a diode with constant current bias and the variable capacitor is varactor.

MicroCrystal's CC1V03 40 kHz tuning-fork crystal resonator was used in this design:

Table 22. Crystal parameters

C_s	2.2196 fF	f_0	39995.9688 Hz
R	34.27 kΩ	C_0/C_s	901.063
L	7134 H	Q	52314
C_0	2 pF	T_{inf} (inflection temp.)	25 °C
ω_0	251302.084 rad/s	k (parabolic freq. coef.)	$4.0 \cdot 10^{-8}$ 1/K^2

V.2. Capacitance calculations – one varactor case

V.2.1. Input data

Crystal nominal parameters from Table 22 are used in the following calculations. The schematic of the XO is shown in Figure 87. Crystal has quadratic frequency-temperature characteristic.

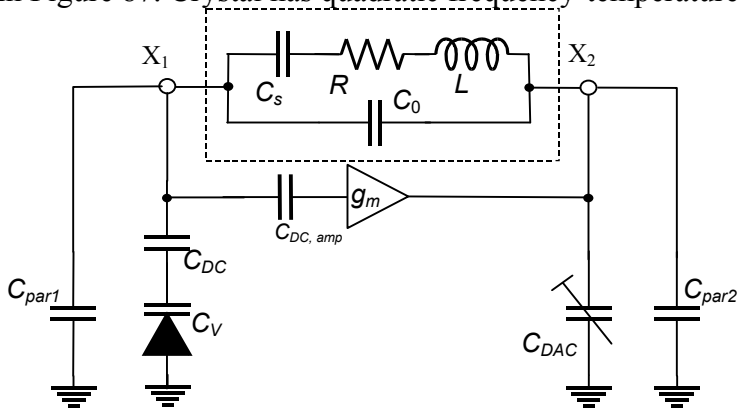


Figure 87. Principal XO schematic

Table 23. Circuit parameters

f_{exp}	40000.000 Hz	C_{DAC}	40 pF
$C_{LOAD,\ nom.}$	9 pF	C_{DC}	50 pF
C_{par1}	3 pF	f/f_0	1.00010079
C_{par2}	3 pF	$(f/f_0)^2-1$	0.00020159

V.2.2. Step 1 – required load capacitance vs. temperature

Determine the required load capacitance range. In this step, the load capacitance includes the following capacitances: C_{DAC}, C_V, C_{DC}, C_{par1}, C_{par2} to combine as follows (see Figure 87):

$$C_{LOAD} = \frac{1}{\dfrac{1}{\dfrac{C_{DC}C_V}{C_{DC}+C_V}+C_{par1}}+\dfrac{1}{C_{DAC}+C_{par2}}}. \tag{11}$$

The oscillation frequency can be expressed in form

$$f_{\exp} = \frac{1}{2\pi\sqrt{LC_{ekv}}}\left(1-kT^2\right);\ C_{ekv} = \frac{C_s\left(C_0+C_{LOAD}\right)}{C_s+C_0+C_{LOAD}}. \tag{12}$$

Here, T is the deviation from inflection temperature, $T = T_{actual} - T_{INF}$. f_{exp} is expected oscillation frequency, C_{ekv} – equivalent load capacitance, combined of C_0 in parallel with C_{LOAD} in series connection with motional capacitance C_s.

Assume f_{exp} to be constant in temperature and from (12) find C_{ekv}:

$$C_{ekv} = \frac{\left(1-kT^2\right)^2}{\omega_{\exp}^2 L} = \frac{1-2kT^2+k^2T^4}{\omega_{\exp}^2 L} = \frac{C_s\left(C_0+C_{LOAD}\right)}{C_s+C_0+C_{LOAD}}. \tag{13}$$

Dividing (13) by C_s and solving for C_{LOAD} yields

$$C_{LOAD} = C_s \cdot \frac{1-2kT^2+k^2T^4}{\left(\dfrac{\omega_{\exp}}{\omega_0}\right)^2-1+2kT^2-k^2T^4} - C_0. \tag{14}$$

Formulas (11)–(14) have been entered to an Excel table and the following resulting C_{LOAD} versus T_{actual} dependence has been obtained:

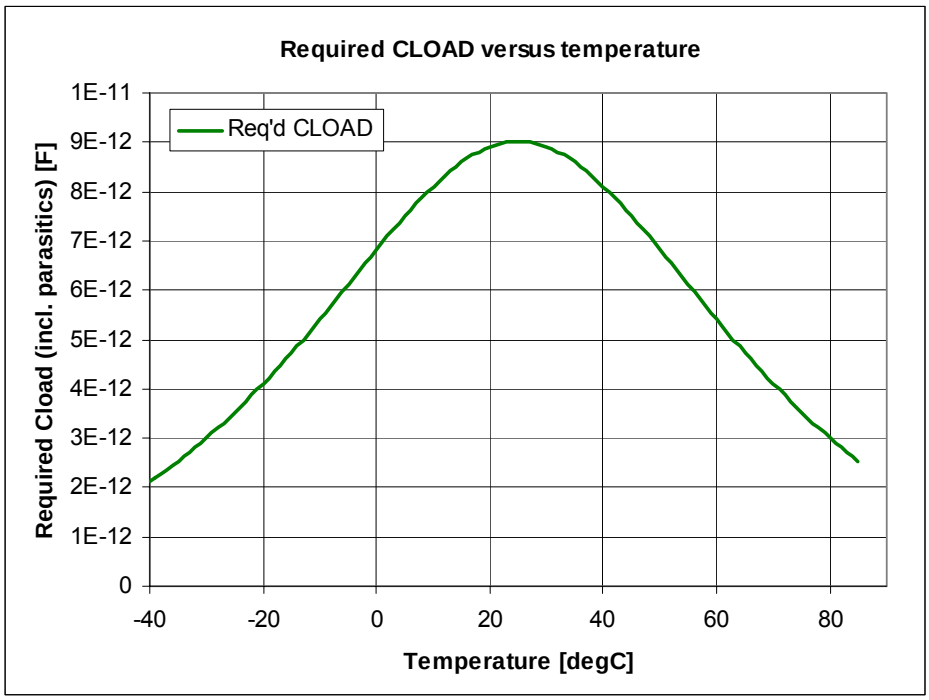


Figure 88. Load capacitance versus temperature

V.2.3. Step 2 – Required varactor capacitance vs. temperature

Basing on (14) and (11), find the required varactor capacitance C_V temperature dependence. Insert the expression for C_{LOAD} (14) to (11) to get

$$C_{LOAD} = C_s \cdot f\left(T^2\right) - C_0 = \frac{1}{\dfrac{1}{\dfrac{C_{DC}C_V}{C_{DC}+C_V} + C_{par1}} + \dfrac{1}{C_{DAC}+C_{par2}}}. \tag{15}$$

From (15), let us find expression for C_V, assuming all other capacitances to be constant. This will yield the required varactor capacitance range. Omitting the algebra and defining the following coefficients,

$$\begin{cases} K_2 = \dfrac{1}{C_{DAC}+C_{par2}}; \quad K_3 = C_{DC}+C_{par1}; & K_4 = C_{DC}C_{par1}; \\ K_5 = 1 + K_2K_3; & K_6 = C_{DC} + K_2K_4. \end{cases} \tag{16}$$

we will obtain

$$C_V = \frac{K_6C_{LOAD} - K_4}{K_3 - K_5C_{LOAD}}. \tag{17}$$

Expression (17) was again evaluated in an Excel table. The result is illustrated in Figure 89.

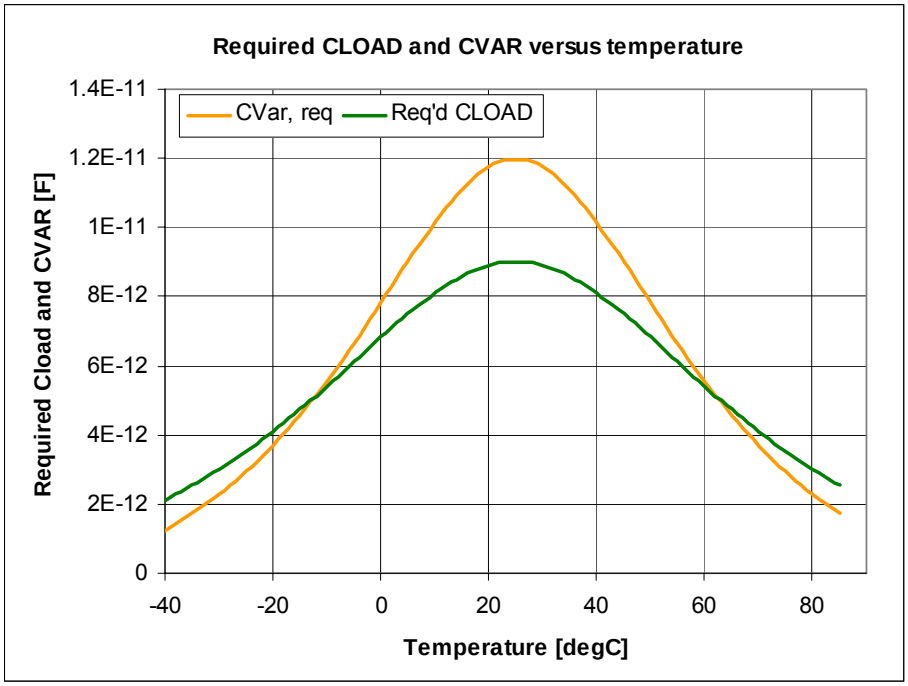


Figure 89. Required varactor capacitance

It should be noted that the parasitic capacitance C_{par1} has much more influence on required varactor capacitance than C_{par2}. This can be explained by the fact that C_{par2} is in parallel with large capacitor C_{DAC}, while C_{par1} is in parallel with practically only varactor capacitance.

V.2.4. Step 3 – Required varactor control voltage vs. temperature

The varactor model is based on the $C(V)$ curve measurement data of a real varactor (Figure 90). For modeling details please refer to SPICE diode capacitance equations (18, 19). The following diode model parameters were extracted from curve fitting (for room temperature only):

CJO=29pF, MJ=0.999, VJ=0.41

It should be noted that there are problems with simulating the diode capacitance, when the parameter MJ is greater than 0.9. The simulator in use adjusts (erroneously) the MJ parameter value to 0.9, thus invalidating the model. It is not known if the same happens with all circuit simulators.

The following formulas for diode level 1 depletion capacitance model are extracted from SPICE manual:

$$C_{dep} = C_{dep,a} + C_{dep,p};$$
$$C_{dep,a} = C_{JO}\left(1 - \frac{v_d}{V_J}\right)^{-MJ}; \qquad (18)$$
$$C_{dep,p} = C_{JSW}\left(1 - \frac{v_d}{V_J}\right)^{-MJSW}.$$

v_d is the diode voltage (negative for reverse bias), C_{JO} is zero-bias junction depletion capacitance, C_{JSW} is zero-bias junction sidewall capacitance. MJ and $MJSW$ are correcponding capacitance exponents. Please note that equations (18) are valid only for reverse-biased diode; up to v_d=0.5V_J. The resulting varactor capacitance curves are shown in Figure 90, curve named Ctot, mod.

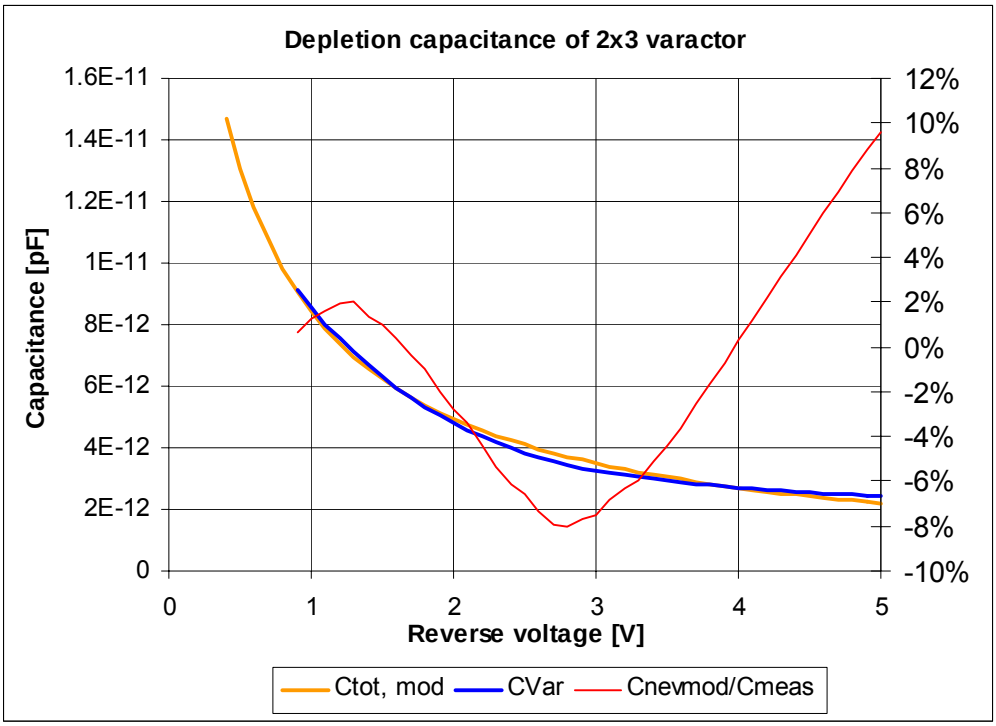


Figure 90. Varactor capacitance model

The varactor temperature (parameter is reverse voltage) and reverse voltage (parameter is temperature) plots are shown in Figure 91 and Figure 93, respectively. It should be noted that with this set of model parameters, the temperature dependence of varactor capacitance are quite noticeable. This can be intuitively understood, since the hyperabrupt doping profile (which ensures M_J=1) and small V_J (ensures more rapid change of capacitance with reverse voltage) both contribute to the temperature sensitivity of the capacitance.

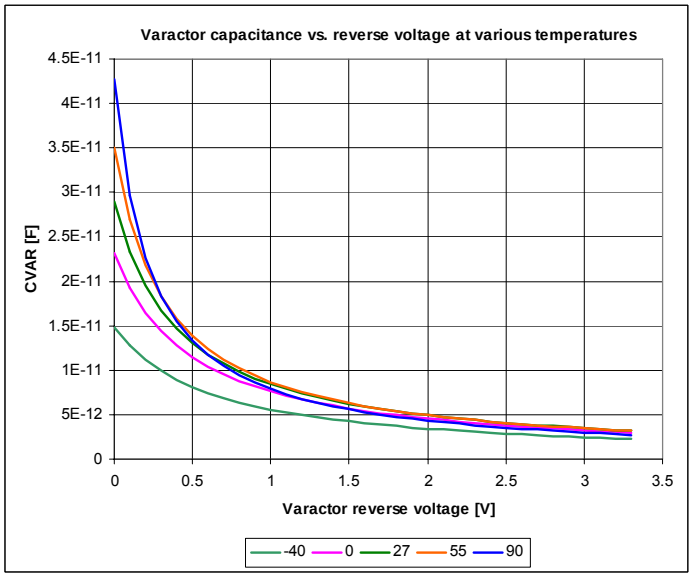


Figure 91. *C*(*V*) curves at various temperatures

The temperature dependence of the junction diode is modeled in SPICE with temperature dependence of parameters V_J, C_{JO} and C_{JSW} with the following formulas:

$$
\begin{aligned}
V_J(T) &= V_J\frac{T}{T_{nom}} - V_t(T)\left(\frac{E_g(T_{nom})}{V_t(T_{nom})} - \frac{E_g(T)}{V_t(T)} + 3\ln\frac{T}{T_{nom}}\right);\\
E_g(T) &= 1.16 - 7.02\cdot 10^{-4}\cdot\frac{T^2}{T+1108};\ V_t(T) = \frac{kT}{q};\\
C_{JO}(T) &= C_{JO}\left\{1 + M_J\left[1 + 4\cdot 10^{-4}\cdot(T - T_{nom})\right] - \frac{V_J(T)}{V_J}\right\};\\
C_{JSW}(T) &= C_{JSW}\left\{1 + M_{JSW}\left[1 + 4\cdot 10^{-4}\cdot(T - T_{nom})\right] - \frac{V_J(T)}{V_J}\right\}.
\end{aligned}
\tag{19}
$$

The temperature dependencies described in (19) are shown in Figure 92.

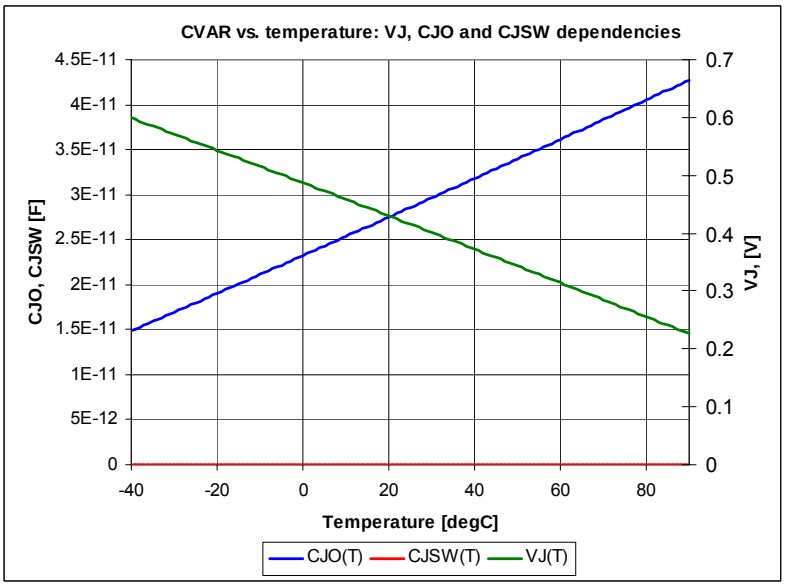


Figure 92. Temperature dependencies of VJ, CJO and CJSW

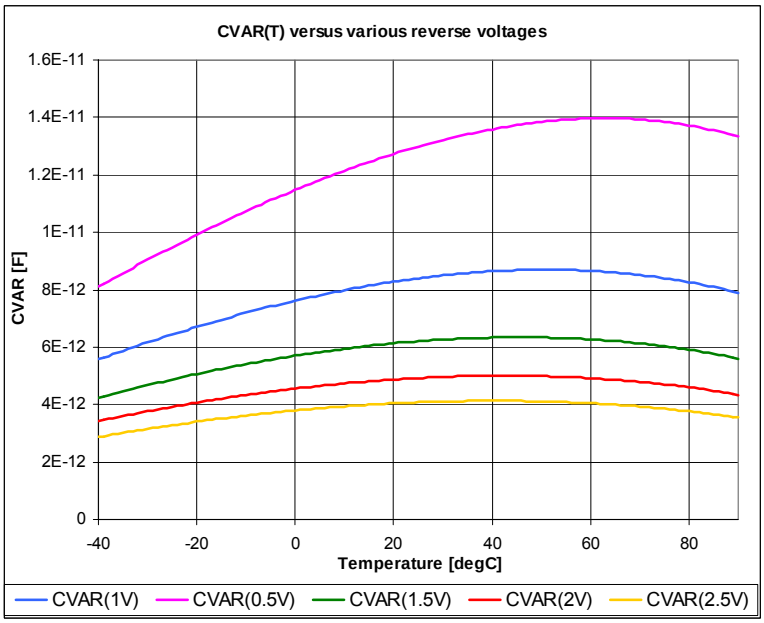


Figure 93. C(T) curves at various reverse bias voltages

Next, from the varactor $C(V, T)$ curve model (SPICE model is used), find the required control voltage temperature dependence. Let us assume first no temperature dependence of varactor capacitance. We can also drop the varactor sidewall capacitance at the moment. Then combination of (17) and (18) yields

$$C_V = \frac{K_6 C_{LOAD} - K_4}{K_3 - K_5 C_{LOAD}} = C_{JO}\left(1 - \frac{v_d}{V_J}\right)^{-MJ} \xrightarrow{MJ=1} \frac{V_J C_{JO}}{V_J - v_d}. \quad (20)$$

From (20), we can solve for $-v_d$, as the reverse voltage is used:

$$-v_d = v_{req} = V_J\left[\frac{C_{JO}(K_3 - K_5 C_{LOAD})}{K_6 C_{LOAD} - K_4} - 1\right]. \quad (21)$$

It is now time to insert voltage dependencies of V_J and C_{JO}, which, as can be seen from Figure 92, have approximately linear thermal dependencies:

$$v_{req}(T) = V_J(1+\alpha T)\left[\frac{C_{JO}(1+\beta T)(K_3 - K_5 C_{LOAD})}{K_6 C_{LOAD} - K_4} - 1\right], \quad (22)$$

where α and β are calculated coefficients and T is again T_{abs}–T_{NOM}:

$\alpha = -0.0056979$ 1/K	$\beta = -0.00609184$ 1/K

The required control voltages of the varactor from (21) and (22) are plotted in Figure 94.

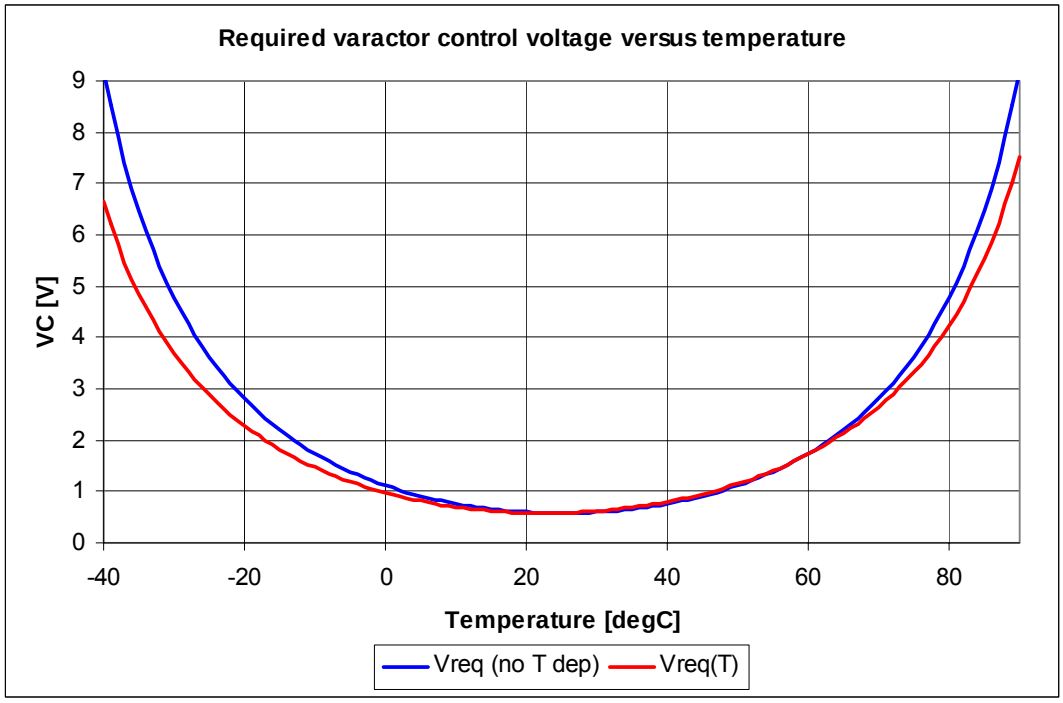


Figure 94.

The varactor parameters must be adjusted so that thermal compensation is achieved within control voltage range of 0.5—2 V. From Figure 94 it can be seen that with the assumed capacitance values the thermal compensation is achieved from –15 °C to +65 °C. Remember that the tolerance analysis must also be done and the varactor parameters are hand-fitted to one set of measurement data. However, it is quite sure that the thermal dependence of the varactor capacitance is important and will make the required control voltage non-symmetric with respect to inflection temperature.

V.2.5. Step 4 – approximate the *V*(*T*) curve

Find the power series (polynomial) coefficients of the required varactor control voltage, as shown with red line in Figure 94. For that purpose, an Excel trendline feature was used. The required coefficients were the 4th, 2nd, 1st order and a constant. See Figure 95.

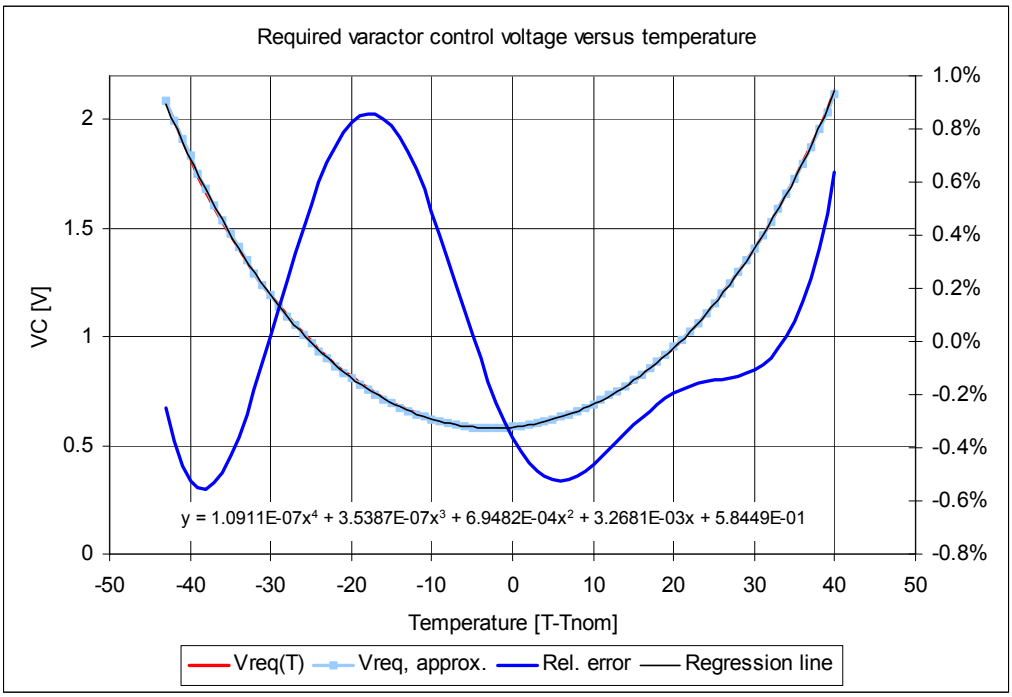


Figure 95.

The 3rd order coefficient was dropped and the linear coefficient was modified to compensate for that. The coefficients to use are as in the following formula:

$$v_{req} = 1.0911 \cdot 10^{-7} \cdot T^4 + 6.9450 \cdot 10^{-4} \cdot T^2 + 3.6100 \cdot 10^{-3} \cdot T + 0.58449, \qquad (23)$$

where T is the deviation from inflection temperature, as usual. The reason for leaving out the third-order term of (23) is to have somewhat simpler schematic of the IC realization.

The approach used above is not the most suitable, since it needs the trendline insertion by another program (Excel), which uses algorithms and approaches that might not yield the desired result in some cases. For that purpose, the approximation step was later programmed as a least-squares fit with appropriate model and updated automatically in response to any change in input data.

V.3. Capacitance calculations – dual-varactor case

This section summarizes the calculations of required load capacitance temperature dependence and **dual-varactor** control voltage dependence of a crystal oscillator, when the temperature dependence of the resonator is known. It bases on the previous section and adds more tunability since the tuning range of one varactor is less than resultant tuning range of the two-varactor circuit.

V.3.1. Input data

Crystal nominal parameters are used in the following calculations. The schematic of the XO is shown in Figure 96. Crystal has again quadratic frequency-temperature characteristic. The crystal parameters are summarized in Table 22 on page 77, the circuit parameter in Table 24.

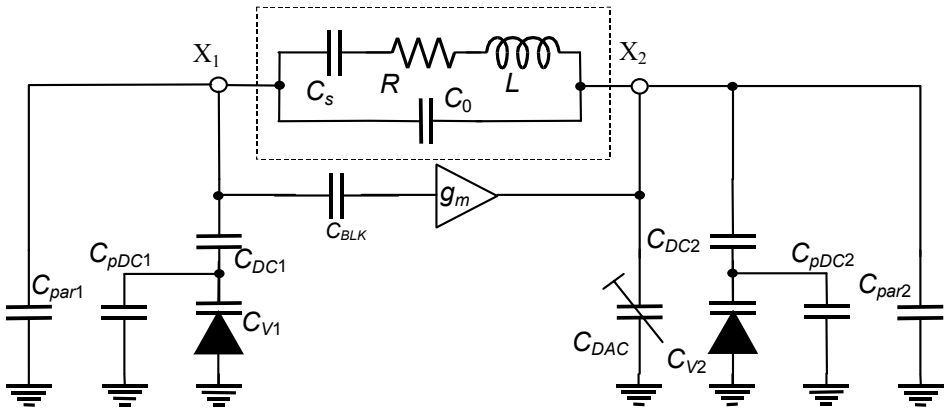


Figure 96. Principal dual-varactor XO schematic

Table 24. Circuit parameters for dual-varactor case

f_{exp}	40000.000 Hz	C_{DC1}	40 pF	C_{DAC}	0…20 pF in 64 steps
$C_{LOAD,\ nom.}$	9 pF	C_{DC2}	40 pF	C_{V1}	2x3 unit cells
C_{par1}	1.5 pF	C_{pDC1}	0.40pF	C_{V2}	2x3 unit cells
C_{par2}	3 pF	C_{pDC2}	0.40pF	f_{exp}/f_0	1.00010079

V.3.2. Step 1 – required load capacitance

Determine the required load capacitance range. In this step, the load capacitance includes the following capacitances: C_{V1}, C_{DC1}, C_{par1}, C_{pDC1}; C_{DAC}, C_{V2}, C_{DC2}, C_{par2}, C_{pDC2} to combine as follows (see Figure 96):

$$C_{LOAD} = \frac{1}{\dfrac{1}{\dfrac{C_{DC1}\left(C_{V1}+C_{pDC1}\right)}{C_{DC1}+C_{pDC1}+C_{V1}}+C_{par1}} + \dfrac{1}{\dfrac{C_{DC2}\left(C_{V2}+C_{pDC2}\right)}{C_{DC2}+C_{pDC2}+C_{V2}}+C_{DAC}+C_{par2}}}. \qquad (24)$$

The oscillation frequency can be expressed in form

$$f_{\exp} = \frac{1}{2\pi\sqrt{LC_{ekv}}}\left(1-kT^2\right);\ C_{ekv} = \frac{C_s\left(C_0+C_{LOAD}\right)}{C_s+C_0+C_{LOAD}}. \qquad (25)$$

Here, T is the deviation from inflection temperature, $T = T_{actual} - T_{INF}$. f_{exp} is expected oscillation frequency, C_{ekv} – equivalent load capacitance, combined of C_0 in parallel with C_{LOAD} and all this in series connection with motional capacitance C_s.

Assume f_{exp} to be constant in temperature and from (25) find C_{ekv}:

$$C_{ekv} = \frac{\left(1-kT^2\right)^2}{\omega_{\exp}^2 L} = \frac{1-2kT^2+k^2T^4}{\omega_{\exp}^2 L} = \frac{C_s\left(C_0+C_{LOAD}\right)}{C_s+C_0+C_{LOAD}}. \qquad (26)$$

Dividing (26) by C_s and solving for C_{LOAD} yields

$$C_{LOAD} = C_s \cdot \frac{1-2kT^2+k^2T^4}{\left(\dfrac{\omega_{\exp}}{\omega_0}\right)^2 - 1 + 2kT^2 - k^2T^4} - C_0. \qquad (27)$$

The formulas (24)–(27) have been entered into an Excel table and the following resulting C_{LOAD} versus T_{actual} dependence has been obtained:

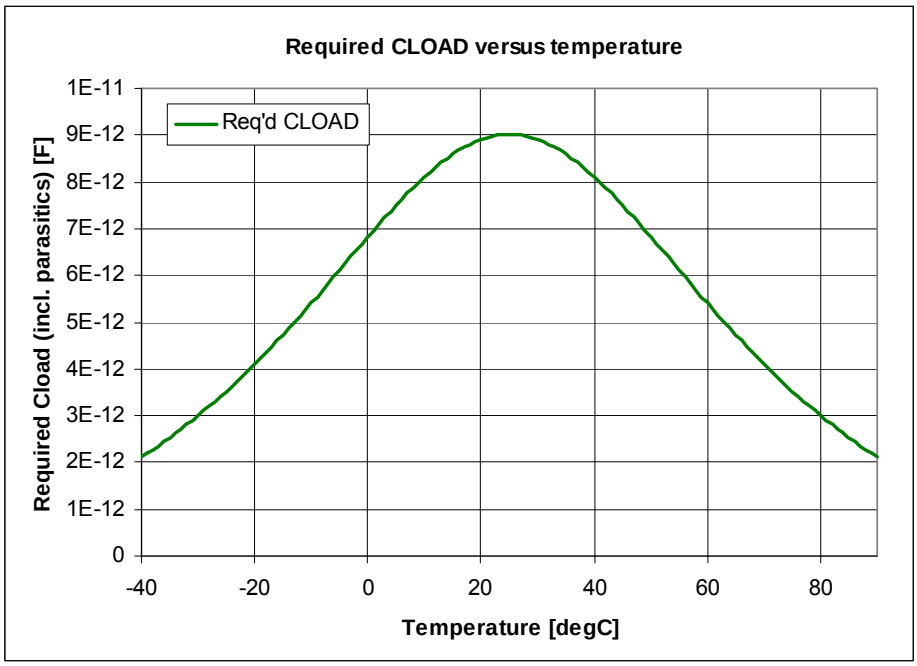


Figure 97. Load capacitance versus temperature

V.3.3. Step 2 – varactor control voltage

Basing on (27) and (24), find the required varactor capacitance C_V temperature dependence. Insert the expression for C_{LOAD} (27) to (24) to get

$$C_{LOAD} = C_s \cdot f\left(T^2\right) - C_0 = \frac{1}{\frac{1}{\frac{C_{DC1}\left(C_{V1}+C_{pDC1}\right)}{C_{DC1}+C_{pDC1}+C_{V1}}+C_{par1}} + \frac{1}{\frac{C_{DC2}\left(C_{V2}+C_{pDC2}\right)}{C_{DC2}+C_{pDC2}+C_{V2}}+C_{DAC}+C_{par2}}} \quad (28)$$

From (28), we must find expressions for C_{V1} and C_{V2} assuming all other capacitances to be constant. The problem at this point is: How to divide the required variable capacitance between the two varactors? How to distribute other (constant) capacitors between the X1 and X2 nodes? First answer to this question that will occur is to use equal varactors and to use as small capacitors as possible for X1 node and connect the rest of capacitances to X2 node. The X1 node is much more sensitive to parasitic capacitances, so this capacitance dividing scheme will minimize the parasitics connected to X1 node.

It can be seen from expression (28) that the solution for both C_{V1} and C_{V2} will be equivalent, since the expression is symmetrical for both varactors. It is also known that the capacitors C_{DC1} and C_{DC2} (see Figure 96) will have parasitics C_{pDC1} and C_{pDC2}, respectively, related to their capacitance values as a certain percentage (ie., 4% of the capacitance value for regular metal-insulator-metal capacitors and 1% for capacitors with isolated bulk. This fraction of the parasitic capacitance to total capacitance will be referred to as quantity a.

Now, with the following quantities defined:

$$\begin{cases} v_1 = a + \frac{C_{V1}}{C_{DC1}}; & C_{X1} = C_{par1}; \\ v_2 = a + \frac{C_{V2}}{C_{DC2}}; & C_{X2} = C_{DAC} + C_{par2} \end{cases}, \quad (29)$$

we can rewrite expression (28) as follows:

$$C_{LOAD} = \frac{1}{\frac{1}{\frac{v_1}{1+v_1}C_{DC1} + C_{X1}} + \frac{1}{\frac{v_2}{1+v_2}C_{DC2} + C_{X2}}}. \quad (30)$$

Equation (30) is symmetrical with respect to both variables v_1 and v_2, yielding similar solutions for both of these variables.

Now it must be decided how to distribute the required crystal load capacitance between the varactor capacitances C_{V1} and C_{V2} and their decoupling capacitors C_{DC1} and C_{DC2}. There is at least two degrees of freedom in choosing these four values, but only one equation relating these [equation (28)]. For simplicity of calculations, we choose so that $C_{DC1} = C_{DC2} = C_{DC}$ and $C_{V1} = C_{V2} = C_V$, making also $v_1 = v_2 = v$, as can be seen from (29). Next, let us define

$$x = \frac{v}{1+v} C_{DC}. \quad (31)$$

Solving (30) for x yields two solutions:

$$x^2 + (C_{X1} + C_{X1} - 2C_{LOAD})x + [C_{X1}C_{X2} - C_{LOAD}(C_{X1} + C_{X2})] = 0;$$
$$x_{1,2} = -\frac{C_{X1} + C_{X1} - 2C_{LOAD}}{2} \pm \sqrt{\frac{(C_{X1} + C_{X1} - 2C_{LOAD})^2}{4} - [C_{X1}C_{X2} - C_{LOAD}(C_{X1} + C_{X2})]}. \quad (32)$$

x has dimension of capacitance. It can be easily seen that the only correct and physical solution is that with the '+' sign. Recalling from (29) and (31), we can now calculate C_V:

$$C_V = C_{DC}\left(\frac{x}{C_{DC} - x} - a\right). \quad (33)$$

Expressions (32) and (33) were again evaluated in Excel table which is mentioned earlier. The result is illustrated in Figure 98.

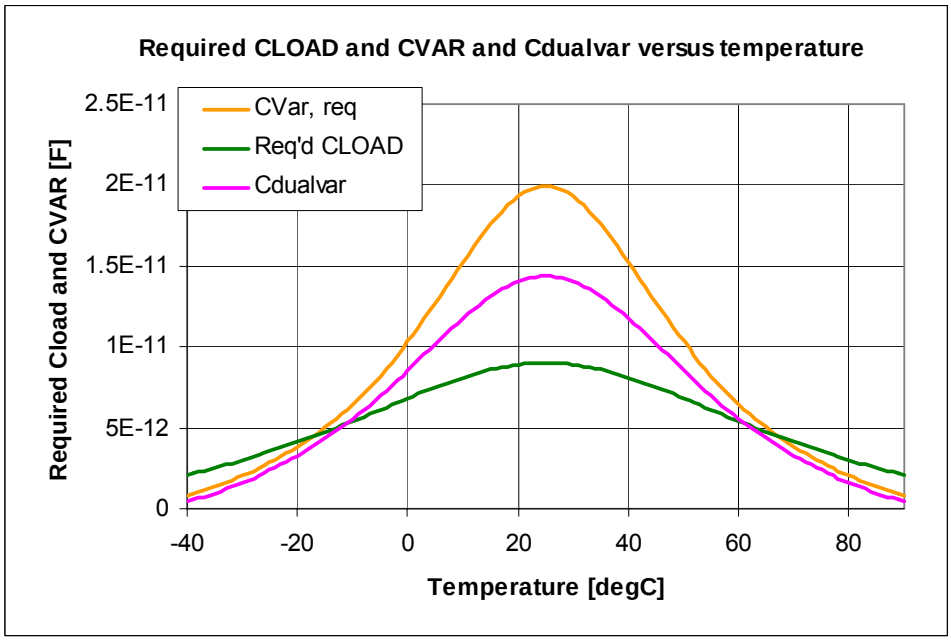


Figure 98. Required varactor capacitance: comparison between single- and dual-varactor solutions.

As expected, the required maximum varactor capacitance has increased, because the two varactors are effectively in series connection. Also the decoupling capacitors C_{DC1} and C_{DC2} have been changed from 75 pF to 40 pF, both for area and parasitics considerations.

It should be noted that the parasitic C_{par1} has much more influence on required varactor capacitance than C_{par2}. This can be explained by the fact that C_{par2} is in parallel with large capacitor C_{DAC}, while C_{par1} is in parallel with practically only varactor capacitance.

For evaluating the performance merits of dual-varactor solution over the single-varactor solution, the following two graphs are plotted. First, the range of required varactor capacitance is plotted on Figure 99, and from this figure it could be decided that dual-varactor yields wider range of thermal compensation, since the curve is flatter on mid-temperature range.

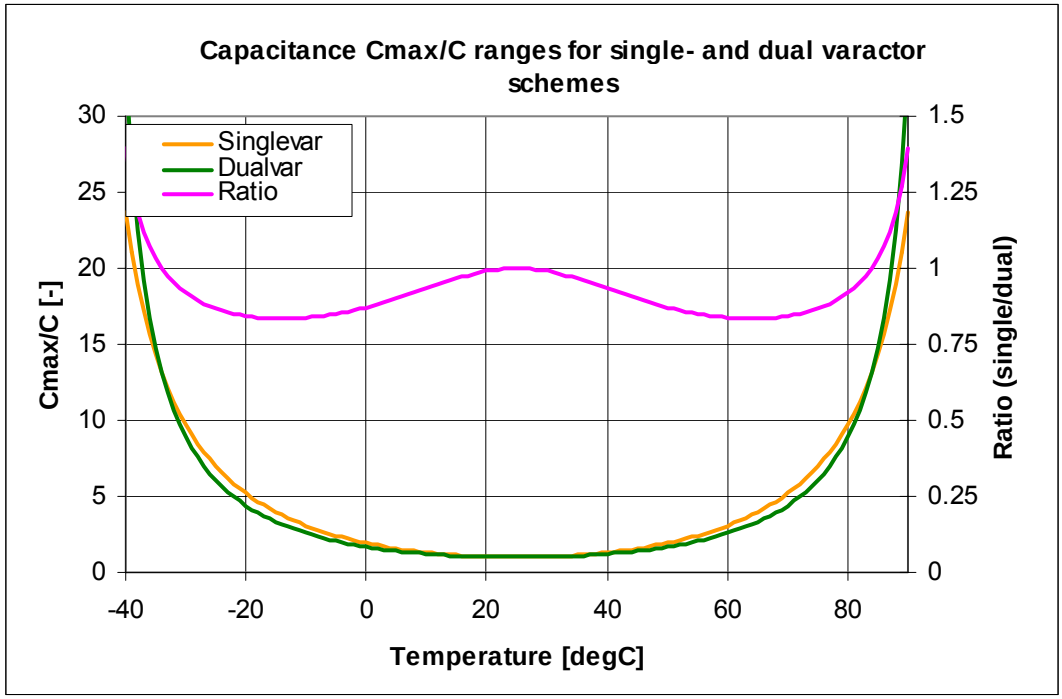


Figure 99. Comparison of single- and dual-varactor thermal compensation scheme: range of required capacitance change

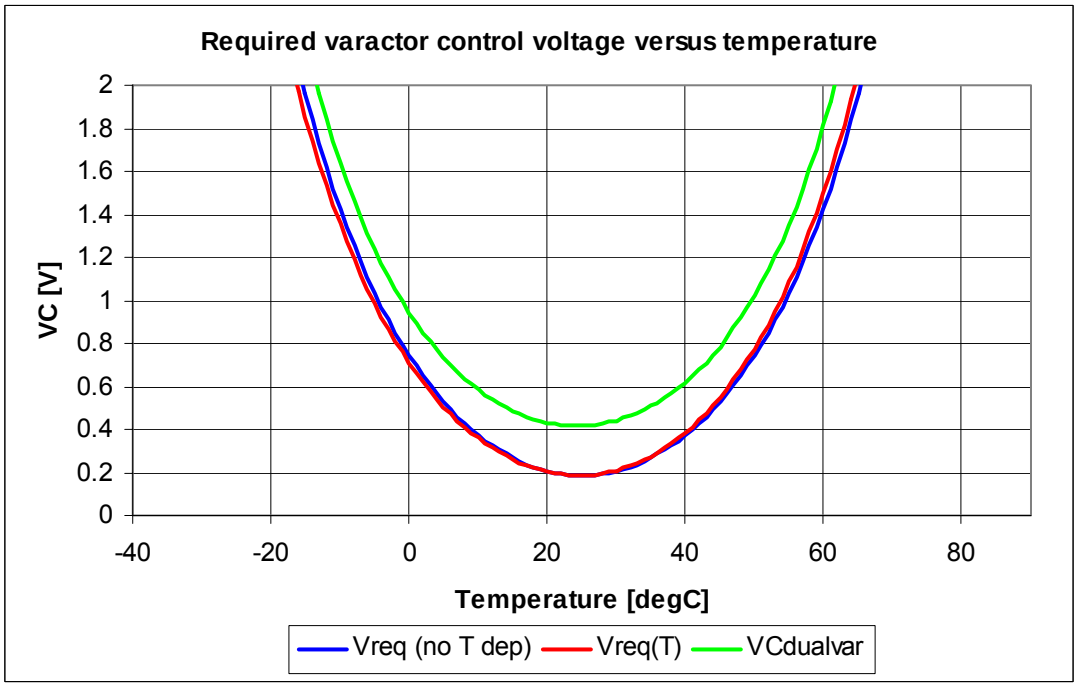


Figure 100. Required control voltage for the single- and dual-varactor schemes

A look at Figure 100 indicates, that the benefit of the dual-varactor scheme for the wider thermal compensation range is consumed by the higher control voltage requirement, as the control voltage cannot exceed 2 V due to the fact that the minimum operating voltage for the schematic is specified to be 2.4 V and the circuitry that generates the varactor control voltage will have at least one V_{DS} voltage drop less available maximum voltage (linear regulator output).

As a conclusion at this point, it will not be feasible to use the dual-varactor thermal compensation scheme for the DualOscillator crystal oscillator thermal compensation in the SPECIAL CASE where the varactors and their decoupling capacitor values are equal. The further work on the thermal compensation will be done to find out, whether there are other sets of values and sizes for the varactors and their decoupling capacitors, which yield wider range of thermal compensation and simultaneously address the maximum varactor control voltage limit problem in the system.

Another approach is to use different control voltages for the two varactors. This possibility remains yet to be explored.

The layout of the DualOscillator integrated circuit that was designed using the approach described in this Section is shown in Figure 101.

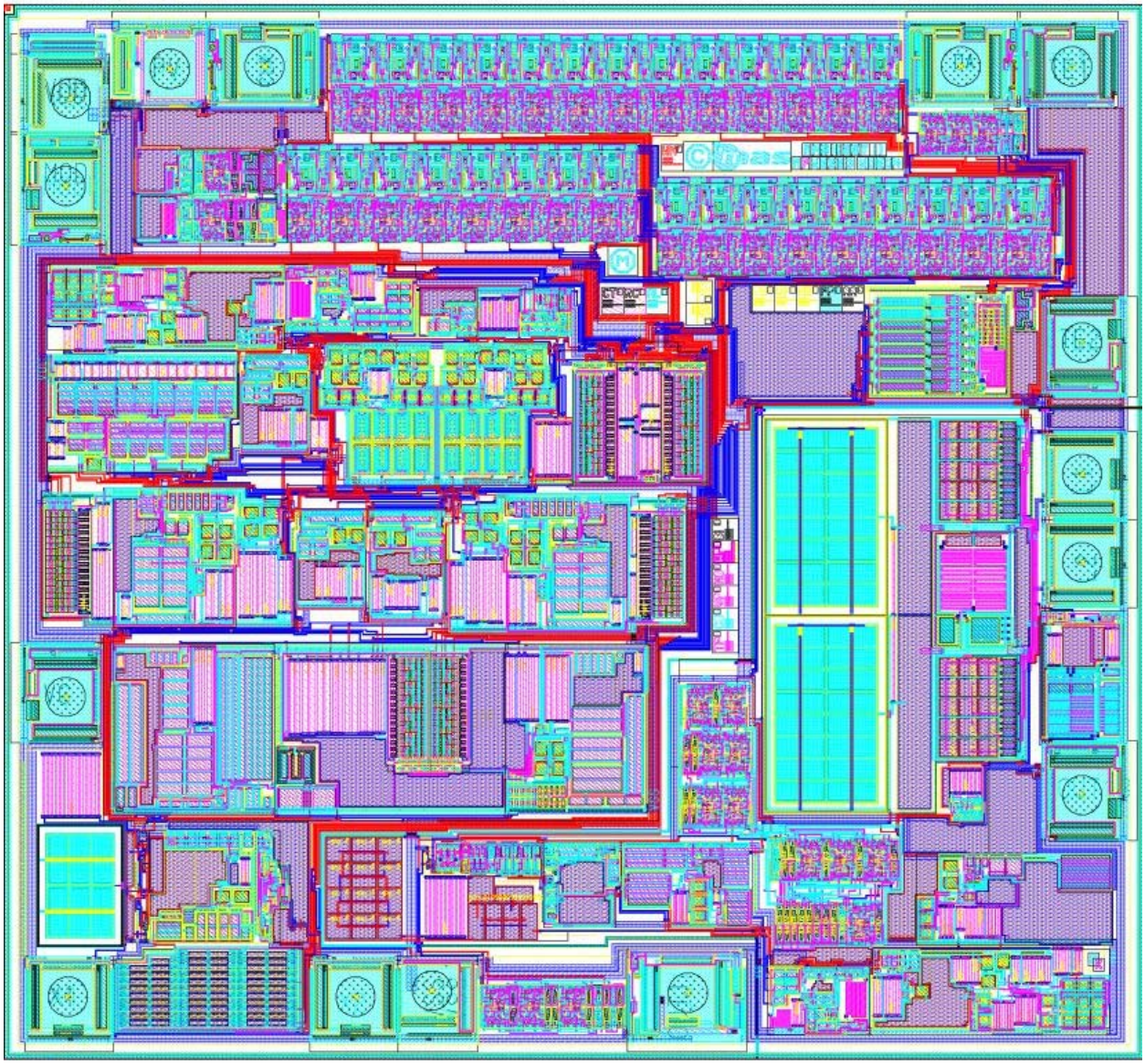


Figure 101. DualOscillator layout

VI. Statistical analysis of the TCXO

Since the system of thermal compensation of the crystal oscillator does not use feedback from the resonator and thus is unable to take into account the possible variance in both resonator and schematic elements, a trimming must be available to correct for these variances. Detailed statistical analysis is needed for evaluating the trimming range, precision and also the trimming algorithm evaluation. Due to the trimming requirement, the system must be composed and trimmed sample-by-sample; thus the algorithm must be fast and simple.

The purposes of this Section are:

1. To check the operation of DualOscillator TCXO within allowed tolerances of the system components;
2. To find out the "worst case" combinations of tolerances of the system parameters and suggest the respective steps to be taken to change the system;
3. To suggest/design the most suitable trimming algorithm for the TCXO;
4. To verify the correctness of the system-level design of DualOscillator TCXO.

Originally, it was intended to use MathCad 11 for the realization of the simulation system. The lack of suitable file I/O and iteration tools in MathCad 11 caused me to choose the C language (particularly, gcc for PC) instead.

VI.1. System specification

The system to be simulated, either with fixed parameters or statistically, consists of the following parts:

1. Crystal resonator;
2. Crystal oscillator core;
3. Varactor diode;
4. Frequency adjustment element for coarse tuning (C_{DAC});
5. Thermal compensation block (incorporating temperature sensor).

The listed components are interconnected in a manner, described in Figure 102 below.

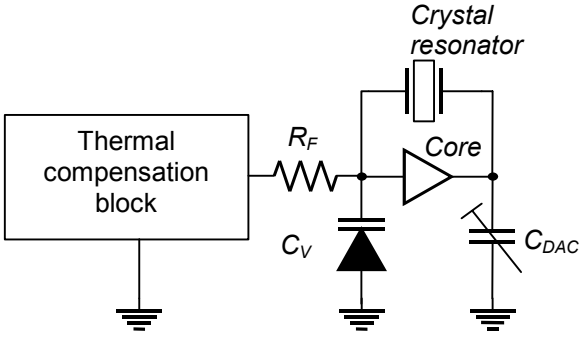


Figure 102. System operation diagram

The system from Figure 102 operates as follows. First, the IC containing the oscillator, varactor diode, capacitor DAC and thermal compensation block is assigned a certain crystal resonator. Due to the variance in the parameters of the IC and the crystal as well as the thermal dependence of the oscillations, the oscillation frequency will not fulfill the specification (see

e. g., Figure 107 on page 103) for all temperatures and IC-crystal pairs. For squeezing the operating frequency within the bounds of the specification, a special block – the thermal compensation block – is designed. This block has also its tolerances. For overcoming the problem of the tolerances of all components in the system plus temperature variations, several fine-tuning places are available in the thermal compensation block.

Thermal compensation in this system makes use of the fact that the temperature-frequency dependence of the crystal resonator is quite well defined and has only small tolerances. We assume that when we know the temperature of the resonator (actually, the IC temperature is measured), then we can tell what equivalent (or load) capacitance has to be connected in parallel with the crystal resonator to obtain the correct oscillation frequency. The questions of finding the compensation formulas and designing the compensation block are described in previous section.

VI.2. Simulation specification

The simulations of the system described in Figure 102 will be carried out using the macromodels of the components. These macromodels must relate to the real circuit topology of the IC circuit and must allow for trimming and variations of the component values just like the real IC component values change from chip to chip, wafer to wafer and lot to lot.

There will be 3 simulation modes:

1. Single simulation with user-defined input parameters for the circuit;
2. Statistical simulations, where the parameters are varied according to predefined parameter/component tolerances with known distributions. In this case, the number of simulations and the trimming parameters are given by the user and the component value sets are evaluated using the pseudo-random number generator of a computer;
3. Trimming algorithm simulations, where a predefined (single or generated statistical set of) parameters are assigned to the system and a trimming algorithm is applied to the trimming parameters in order to compensate for the current situation.

The thin-film resistors and MIM capacitors which are fabricated in the IC and also the bipolar transistors have all predefined statistical models. The temperature dependence of the resistors, capacitors and transistors' β are described with appropriate temperature coefficients. The statistical models are described in the following table (Table 25):

Table 25. Statistical parameters of circuit elements

Component	Param.	TC1	Distribution	Lot	Dev
Resistor	R	380µ	Normal for lot and dev	±20 %	±0.5 %
Capacitor	C	0	Normal for lot and dev	±10 %	±1 %
BJT	β	7.5m	Lognormal for lot, uniform for dev	±25 %	±5 %

The tolerances in Table 25 represent the ±3σ values. TC1 represents linear term of temperature dependency, Lot tolerance represents the absolute variance of the parameter in question and Dev is the relative variance between the parameters of the elements that are on the same integrated circuit.

The simulation will yield an output file, which contains the following information:

1. The input data (schematic parameter values, deviations from the nominal values, trimming register values;
2. The $f(T)$ curve points for the current input data set. The nominal temperature range is –40…+90°C with 1°C step (frequency deviation in ppm);
3. The $-R(T)$ curve points for the current input data set (XO core negative resistance);
4. The $V_{VAR}(T)$ curve points for the current input data set (varactor control voltage);
5. Post-processing information for each input/output set of parameters, including:

5.1. Pass/Fail flag (fulfils spec or not);
5.2. Temperature range(s) where the spec is violated;
5.3. Min/Max frequency and their occurrence temperature(s);
5.4. Negative resistance characteristics, compared to the crystal loss resistance; min/max values and the range(s) where the oscillations cannot start (ie., $|-R| < R_m$)

6. Simulation collection analysis results: average $f(T)$ curve for all runs, envelope curves (higher and lower), percentage of pass/fail runs (only when statistical simulation is run)

The information must be entered to the output file in text format so it can be directly imported to Excel for more post-processing.

VI.3. Detailed specifications for system components

The system consists of 5 main blocks as shown in Figure 102. All of those blocks have to be behaviorally modelled. All models have the following options in common:

1. The model internal parameters are given as global variables, used by the model functions;
2. The input parameters for the model (or arguments to the function) are only the temperature and the applicable trimming register bits;
3. The model functions are considered to be deterministic, ie. the formulas remain the same during all statistical simulations. The model parameters are varied by the calling functions;
4. The output of a function describing a block is a single number.

VI.3.1. Specification of crystal resonator

Inputs:

Temperature [°C]

Parameters:

Table 26. Crystal resonator simulation parameters

Symbol	Nom. value	Tolerance	Stat?	Meaning
f_{osc}	40000 Hz	±30 ppm	Yes	f_{osc} when loaded with C_{LOAD} at T_0
C_s	2.2196 fF	?	No	Motional capacitance
L	(calculated)	?	No	Motional inductance
C_{LOAD}	9 pF	-	No	Load capacitance
C_0	2 pF	±0.5 pF	Yes	Case (parasitic) capacitance
R	60 kΩ	±30 kΩ	Yes	Motional resistance
T_0	25 °C	±5 °C	Yes	Turnover temperature (or inflection temp.)
k	0.035 ppm/°C^2	±0.008 ppm/°C^2	Yes	Parabolic temperature coefficient

Output:

Actual oscillation frequency [Hz]

The model calculations are carried out using the following crystal electrical equivalent model (Figure 103).

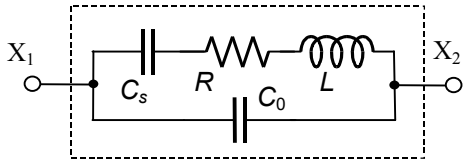


Figure 103. Equivalent circuit of the crystal resonator

First, the motional inductance L is calculated from C_s, C_0, C_{LOAD} and f_{osc}. Then, the L, C_s, C_0, C_{bond}, C_{par1}, C_{par2}, C_{BLK}, C_{amp}, V_{VAR}, C_{DAC} and T values are used for calculating the actual oscillation frequency. The values which are not in function parameters are stored in the global variables and accessed directly by the function. The schematic of the capacitor block is shown in Figure 104.

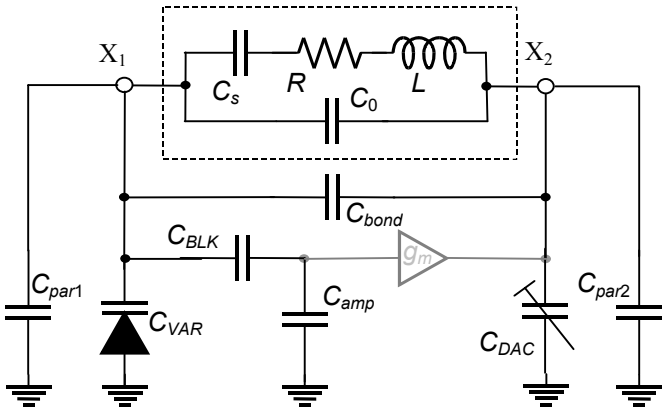


Figure 104. Capacitor block for calculating the actual oscillation frequency

VI.3.2. Specification of oscillator core

Inputs:

Temperature [°C], actual oscillation frequency [Hz]

Parameters:

Table 27. Oscillator core simulation parameters

Symbol	Nom. value	Tolerance	Stat?	Meaning
g_{mstart}	3.57 µS	±30 %	Yes	Initial transconductance of the core
C_{VAR}	from varactor function	-	No	Varactor capacitance as calculated from varactor control voltage and temperature by the varactor model
R_F	2.2 MΩ	±20 % lot, 0.5 % dev	Yes	Coupling resistor for applying varactor voltage
C_{par1}	1.5 pF	±10 %	Yes	Parasitic capacitance at node X1 (Figure 103)
C_{par2}	2 pF	±10 %	Yes	Parasitic capacitance atnode X2 (Figure 103)
C_{DAC}	from CDAC function	-	No	Capacitor DAC capacitance, calculated from the CDAC model
C_0	2 pF	±0.5 pF	Yes	Crystal case (parasitic) capacitance
C_{bond}	0.3 pF	±20 %	Yes	Parasitic capacitance due to bonding or otherwise connecting the crystal to the IC
C_{BLK}	25 pF	±10 % lot, 1 % dev	Yes	DC blocking capacitor at core input
g_{BIAS}	0.02 µS	±30 %	Yes	Core biasing resistor
C_{amp}	1.3 pF	±20 %	Yes	Core input capacitance

Output:

Negative resistance [Ω] at the oscillation frequency

The model calculations are carried out using the model in Figure 105.

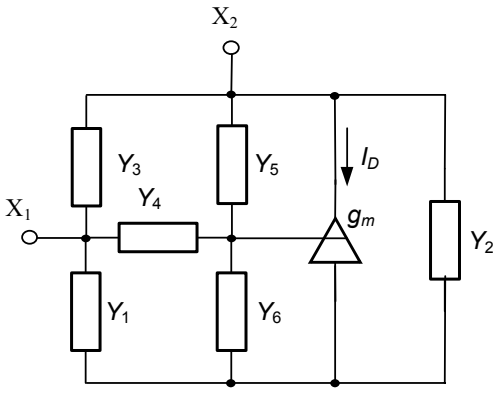


Figure 105. Oscillator core model

The listed parameters are related to the admittances in Figure 105 with the following formulas:

$$Y_1 = sC_{VAR} + \frac{1}{R_F} + sC_{par1}; \quad Y_2 = s\left(C_{DAC} + C_{par2}\right); \quad Y_3 = s\left(C_0 + C_{bond}\right);$$
$$Y_4 = sC_{BLK}; \quad Y_5 = g_{BIAS}; \quad Y_6 = sC_{amp}. \tag{34}$$

VI.3.3. Specification of varactor diode

Inputs:

Varactor control voltage V_{VAR} [V], temperature [°C]

Parameters:

Table 28. Varactor diode simulation parameters

Symbol	Nom. value	Tolerance	Stat?	Meaning
C_{JO}	23.2 pF	±10 %	Yes	Zero-bias junction capacitance
V_J	1.0 V	?	No	Junction potential (empirical!)
M_J	1.433	±5 %	Yes	Junction grading coefficient (empirical!)
β	0.00119 1/°K	±10 %	Yes	Varactor temperature coefficient
T_{VARREF}	25 °C	-	No	Varactor reference temperature

Output:

Varactor capacitance C_{VAR} [F]

For the varactor capacitance calculations, SPICE level 1 diode junction depletion capacitance model is used (refer to equations (18) in Section V.2.4 on page 80)

VI.3.4. Specification of capacitor DAC (CDAC)

Inputs:

Code at the CDAC[5:0] bus (0…63)

Parameters:

Table 29. CDAC simulation parameters

Symbol	Nom. value	Tolerance	Stat?	Meaning
C_{step}	665 fF	±10 % lot, 1 % dev	Yes	CDAC step capacitance

Output:

CDAC capacitance C_{DAC} [F]

Model returns simply product of CDAC code and step capacitance.

VI.3.5. Specification of Thermal Compensation Block

Table 30. Thermal compensation block inputs

Symbol	Nom. value	Range	Meaning
Temperature	25 °C	–40…+90 °C	Circuit temperature
TINF[5:0]	32	0…63	Reference temperature adjustment register
LIN[3:0]	8	0…15	Linear tern adjustment register
SQ[3:0]	8	0…15	Second-order term adjustment register
S4[3:0]	8	0…15	Fourth-order term adjustment register

Table 31. Thermal compensation block simulation parameters

Symbol	Nom. value	Tolerance	Stat?	Meaning
General for whole TEMP_COMP block				
V_{DD}	2.8 V	2.4…5.0 V	No	Supply voltage (for output limiting)
I_0	1.0 µA	±20 % lot, ±2% dev	Yes	Bias current for translinear squarer core
I_{EE}	6.0 µA			Bias current for V-I converter

V_{REF}	1.257 V	±50 mV	Yes	Bandgap reference voltage
Parameters for VMIN_GEN				
R_{1vmin}	150 kΩ	±20 % lot, 0.5 % dev	Yes	Voltage divider resistors
R_{2vmin}	65 kΩ			
Parameters for VT_GEN (temperature sensor)				
T_{0VT}	25 °C	-	No	Nominal temperature
V_{TNOM}	0.6654 V	±10 mV	Yes	Diode voltage at nominal temperature
α	–1.95 mV/°C	-	No	Diode voltage thermal coefficient
Parameters for VT0_GEN				
R_{10}	100 kΩ	±20 % lot, 0.5 % dev	Yes	Resistors for V_{T0} voltage divider and trimming potentiometer (TINF)
R_{20}	101 kΩ			
R_{30}	12 kΩ			
R_{LSB1}	12 kΩ			
R_{LSB2}	350 kΩ			
R_{end0}	2.4 kΩ			
R_{step0}	6.98 kΩ			
Parameters for DIVIDER				
R_{2div}	260 kΩ	±20 % lot, 0.5 % dev	Yes	Voltage divider resistors
R_{3div}	38 kΩ			
Parameters for IU_CONV2				
β_{iu2}	150	±25 % lot, 5 % dev	Yes	β of the bipolar transistors
R_{Eiu2}	240 kΩ	±20 % lot, 0.5 % dev	Yes	Resistors for voltage divider and trimming potentiometer (SQ)
R_{7iu2}	50 kΩ			
R_{8iu2}	260 kΩ			
R_{endiu2}	1.2 kΩ			
$R_{stepiu2}$	3.49 kΩ			
R_{9iu2}	50 kΩ			
Parameters for IU_CONV4				
β_{iu4}	150	±25 % lot, 5 % dev	Yes	Beta of the bipolar transistors
R_{Eiu4}	240 kΩ	±20 % lot, 0.5 % dev	Yes	Resistors for voltage divider and trimming potentiometer (S4)
R_{7iu4}	50 kΩ			
R_{8iu4}	260 kΩ			
R_{endiu4}	1.2 kΩ			
$R_{stepiu4}$	3.49 kΩ			
Parameters for TRANSLIN_SQ				
(none)				
Parameters for V_I_CONV				
β_{ui}	150	±25 % lot, 5 % dev	Yes	Beta of the bipolar transistors
R_{VI}	17.5 kΩ	±20 % lot, 0.5 % dev	Yes	Resistor for voltage-to-current conversion
Parameters for SUM_AMP				
R_{VTC}	105 kΩ	±20 % lot, 0.5 % dev	Yes	Weighing resistors for V_T and V_{T0}
R_{VT0C}	105 kΩ			
R_{ends}	4 kΩ			Linear member weighing potentiometer resistors
R_{steps}	11.63 kΩ			
R_{VSQ}	135 kΩ			Weighing resistor for V_{SQ}
R_{V4P}	140 kΩ			Weighing resistor for V_{4P}
R_{VMIN}	$R_{VSQ} \parallel R_{V4P}$			Weighing resistor for V_{MIN}
R_{3A}	200 kΩ			Resistors in sum_amp
R_{4A}	200 kΩ			
R_{1S}	100 kΩ			Resistors in V_C adder
R_{2S}	200 kΩ			
R_{3S}	100 kΩ			
R_{4S}	180 kΩ			

Output:

Varactor control voltage V_{VAR} [V] at given temperature

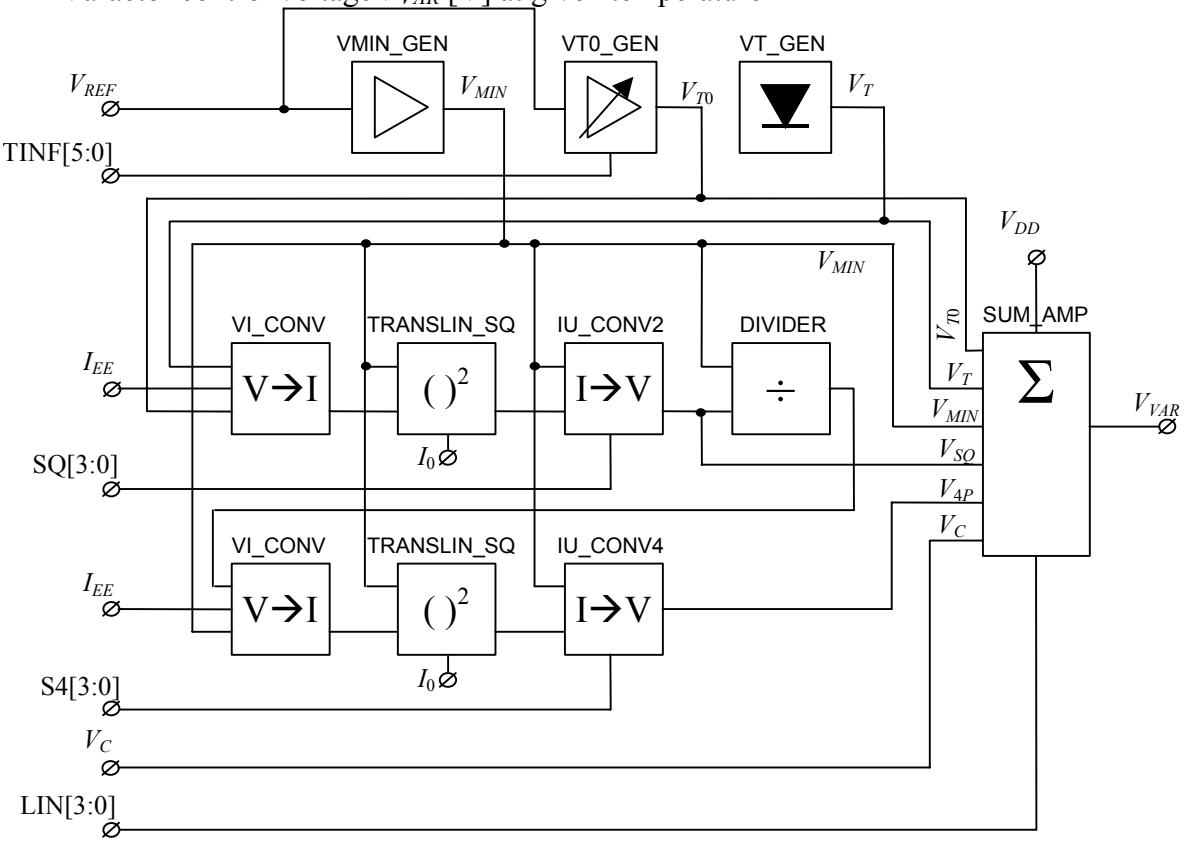


Figure 106. TEMP_COMP block diagram

The thermal compensation block (see Figure 106) implements a 4th order polynomial approximation function to ensure the correct varactor control voltage. which in turn makes the correct load capacitance for the crystal resonator.

$$V_{VAR} = B_0 + B_1(T - T_0) + B_2(T - T_0)^2 + B_3(T - T_0)^4 \qquad (35)$$

There are 4 trimming points for the polynomial: TINF[5:0], LIN[3:0], SQ[3:0] and S4[3:0], influencing the polynomial coefficients B_i (i>0) and T_0 in (35) in the following quantities:

Table 32. Influence of trimmers

Trimming register	is influencing	by	step size
TINF[5:0]	T_0	–2.7…2.4 %	0.08 %
LIN[3:0]	B_1	–43…38 %	5.06 %
SQ[3:0]	B_2	–32…28 %	3.75 %
S4[3:0]	B_3	–30…26 %	3.63 %

Coefficient B_0 in (35) is determined by V_{MIN}.

The model will be designed so that when the voltage at some point of the TEMP_COMP exceeds a predefined value (V_{DD} – 0.2 V), the result of a formula will be clipped to that value. This simulates the real op-amp saturation behavior.

VI.3.6. Specification of the simulation controller

All simulation is controlled by the Simulation Control Block. This block is not shown in Figure 102, since its task is only to control the simulations, allocate memory and other, program flow

related actions. This block organizes calling order of the other system blocks and also controls the parameter variations (during statistical simulations). This block also controls the output of the simulations.

Table 33. Simulation controller inputs

Item	Default	Range	Comment
Simulation Mode	1 – single	1, 2 or 3	Simulation mode (1-single, 2-statistical, 3-trimming simulation)
Number of iterations	-	≥1	Number of iterations in simulation modes 2 (statistical) and 3 (trimming simulation).
StatPart	1 – crystal stat. model	1, 2 or 3	Defines which part of the system will be modeled statistically: 1–crystal only, 2–IC only, 3–both crystal and IC.
Matrix handle	(allocated)	-	Pointer to Matrix, where the simulation parameters and results are saved. Has to be previously allocated alsewhere. Will be used for the simulation result data.

Parameters:

(none)

Output:

Modified parameter vector used in the simulations

First, the polynomial coefficients of the approximating polynomial (35) are calculated (for nominal circuit data); these coefficients are used as a reference in calculating further deviations from the nominal as well as the range of the trimming of the polynomial coefficients.

There are 3 simulation modes: single, statistical and trimming simulations. The descriptions of each simulation mode follow.

VI.3.6.1 Single simulation

In this mode, the simulator will take a vector of all system parameters and calculate the $f(T)$, $-R(T)$ and $V_{VAR}(T)$ function values for the parameter set. As the parameter set will also include the trimming register values, this mode is suitable for estimating whether the compensation has been achieved and how good this compensation is. The parameter values used in the simulations will be exactly the same as given in the input file, no modifications made.

VI.3.6.2 Statistical simulation

This mode is designed for estimating what happens when the system parameters will be varying from sample to sample, lot to lot. All parameters used in the calculations will be varied statistically before calculations, excluding trimming register values. The number of statistical simulation cycles and the system blocks for which the statistical model will be used will be required. Basically, the crystal only, the IC only or both the crystal and the IC will be the options for the statistical simulation.

VI.3.6.3 Trimming simulation

For this simulation mode, first a set of statistical model parameters will be generated. Next, this set will be used in thermal compensation trimming algorithm simulations, for obtaining the best agreement with the predefinied specification. Also in this mode, the crystal, the IC or both will have the statistical model, and the trimming simulation can be repeated multiple number of times, as requested by the user. The output will be the set of parameters plus the found trimming register values along with the resulting $f(T)$ curve points and pass/fail flag. Also information about the specification fulfilment or violation(s) will be produced.

VI.3.7. Specification of the Post-Processor

Table 34. Post-processor inputs

Item	Default	Range	Comment
Specification	-	-	Pointer to the array with specifications (from caller; const.)
String Buffer	(allocated)	-	String for writing output data.
Number of iterations	-	≥1	Number of iterations in simulation modes 2 (statistical) and 3 (trimming simulation).
Data type	SINGLE	SINGLE, COLLECTION	Single run or collection of runs is analysed.
Matrix handle	(allocated)	-	Pointer to Matrix, where the simulation results are saved. Has to be previously allocated alsewhere.

Parameters:

(none)

Output:

Output string is stored in the StringBuffer provided by the caller function and will contain the information about specification fulfilment/violation(s) with additional comments.

VI.3.8. Specification of the Random Number Generator

Table 35. Random number generator inputs

Item	Default	Range	Comment
STAT_MODE	NO_STAT	NO_STAT, STAT	Statistical mode on/off switch
par_avg	0	-	Average value of a parameter
par_tol	1	-	(one-sided) tolerance of a parameter (+3σ)
DISTRIB	NORMAL	UNIFORM, NORMAL, LOGNORM	Type of statistical distribution of the current parameter

Parameters:

(none)

Output:

Statistically varied parameter

Description. The pseudorandom number generator will first be seeded (once per simulation session) with a number, combined from the current computer system date and time. After the seeding, the following calls to the random number generator will give different series of pseudorandom numbers as the seeds differ from session to session.

The pseudorandom number generator of a computer system usually generates random numbers with uniform distribution between 0 and 1. The normalized normal distribution (with average value 0 and standard deviation 1) will be generated by adding up 12 consecutive uniformly distributed random numbers and subtracting 6 from the resulting number. It is known that the normalized uniform distribution (from 0 to 1) will have the standard deviation of 1/12. The lognormal distribution is generated by adding up 12 uniformly distributed random numbers, subtracting 6, exactly as for normal distribution, then rising the basis $\sqrt[6]{2} \approx 1.12246$ to the exponent of the random number with normal distribution. The result will lie in the range from 0.5 to 2. In lognormal case, the minimum specification limit will correspond to 0.5, mean value will be equivalent to 1 and maximum limit will be defined to be equal to 1.5 times the one-sided tolerance.

In these system parameters, which have the lot and dev distributions, first, the lot average tolerance will be randomly generated. Next, each element will be generated the dev tolerance, using the previously found lot average as the mean value and the dev as standard deviation.

VI.3.9. Specification of the main program

Table 36. Main program input files and modes

Item	Default	Range	Comment
Specification File	./spec.txt	-	File with rows of temp/freq. deviation values in format, deviations given in ppm: <lower-temp> <tab> <lower-spec> <tab> <upper-temp><tab><upper-spec>\n
Parameter File	./params.txt	-	Nominal parameter file (one parameter per row in the sequence defined in the program, see code)
Output File	stdout	-	File to write the output data to. If opening fails, or not specified, stdout will be used.
Simulation mode	1	1, 2 or 3	See previous sections

Table 37. Arguments of main program

Symbol	Meaning
-h	Print help page to stdout
-s	Next argument is specification file name – if not found, try to open default file in the current directory, if fails, use internal specification
-i	Next argument is parameter file name – if not found, try to open default file in the current directory (params.txt), if fails, use internal parameters
-o	Next argument is output file name – if creation fails, use stdout
-m	Next argument is simulation mode number 1, 2 or 3
-d	Switch to debug mode

Output:

Named output file; if `-o` argument is given, then the file name given with this argument; else stdout. If "`-`" is specified with `-o`, or the output file creation fails, then the output will be printed to stdout.

Operation. The random number generator will be seeded with a value of 'seconds since epoch' (returned by function `gettimeofday()`), executed as a first sentence. This date and time will also be written to output file along with the random number seed and number of statistical iterations , when appropriate.

Next, the main program checks for command-line arguments. If any syntax errors are found, the program exits with value 1. If `-i` argument is omitted, the default parameter file name is assumed. If this file does not exist in the current directory, then the internal parameter values will be used. If `-o` argument is omitted, or the output file creation fails, stdout will be used. Argument `-m` defines the simulation mode – 1, 2 or 3. If the `-m` is omitted, the simulation mode 1 is used. `-s` defines the specification file; if omitted, the default spec file will be used. If the default file does not exist in the current directory, then internal specification values will be used. `-h` outputs the online help on standard output and `-d` enters debug mode, where values of internal variables and information about function calls is printed on standard output.

When simulation mode is >1, the user will be asked for the number of statistical analysis runs.

Simulation organization phase follows. First the appropriate size Matrix is allocated to fit the input and output data. plus the memory for the Actual Parameter Vector. Also a buffer for the post-processor string is allocated.

If simulation mode is 1, the data from the input file (parameters) will be copied to Actual Parameter Vector and the Number of Iterations is set to 1.

Next, the iteration counter is set to zero.

If Simulation Mode is 2 or 3, an Actual Parameter Vector is created using a Random Number Generator and the input parameter vector. Then the Simulation Controller is called with Actual Parameter Vector, simulation mode and the Matrix handle.

If Simulation Mode is 3 (trimming simulation), the Trimming Algorithm will be called specified number of times entered earlier by user.

Now the Post-Processor is called. The Actual Parameter Vector, the appropriate data from the Matrix and and the string produced by the Post-Processor will be written to output file.

Iteration Counter is incremented and compared to the Number of Iterations. Next iteration is started, when necessary.

Finally, if the simulation mode is 2 or 3, the collection analysis is done for the Matrix using the Post-Processor. The output data is also appended to the output file.

Upon closing the output file, the new date and time are written to the output file.

VI.3.10. Specifications of data structures

Parameter structure is an data structure combining the input and some calculated parameters of the system, as described in Table 26, Table 27, Table 28, Table 29, Table 30 and Table 31. There will be one ParaVec structure allocated for each statistical/trimming simulation run

Matrix is an (`3 × 131 × (Number of Iterations+3)`) array of double numbers.

Temperature is an range variable from –40 to 90 with steps of 1 (131 values in total).

`StringBuf` is a buffer of `char[1000]` for post-processor comment string.

VI.3.11. File structure

Table 38. Files, definitions and functions in TCXO simulation program

File name	Contents

`globals.h`	Global variables, system header file inclusions, function prototypes:
	`double Xtal (double Temp);`
	`double Core (double Temp, double factual);`
	`double Varactor (double Vvar, double Temp);`
	`double Cdac (double Temp, int CDAC);`
	`double Temp_Comp (double Temp, int TINF, int LIN, int SQ, int S4, double VC);`
	`struct ParaVec Simu_Controller (int SimMode, int N, int StatPart, double **Matrix);`
	`double RandNumGen (int stat_mode, double par_avg, double par_tol, int distrib);`
	`double RTFtemp (const double Temp, const double Rvalue);`
	`double CMIMtemp (const double Temp, const double Cvalue);`
	`double Betatemp (const double Temp, const double Bvalue);`

`paravec.h`	ParaVec structure definition; function prototypes
	`void ParaVecSave (struct ParaVec *SafePlace);`
	`void ParaVecRestore (struct ParaVec *SafePlace);`
	`void ParaVecCopy (struct ParaVec *Dest, struct ParaVec *Src);`
	`void ParaVecStatistics (struct ParaVec *Current, int StatPart);`
	`void ParaVecFileInput (FILE *ptr_params_file, struct ParaVec *p);`

`spec.h`	spec structure definition with default value assignment; function prototypes which use the spec structure:
	`void Post_Processor (struct spec *Spec, char **buffer, int N, int DataType, double **Matrix);`
	`void PrintSpecValues (FILE *outfile, struct spec* S, int rows) {};`

`main.c`	Main function, outputting functions
	`void PrintOutParams (FILE *outfile, const struct ParaVec *p) {};`
	`void PrintOutResults (FILE *p, int N, int DataType, char **buf, double **Matrix) {};`
	`int main (int argc, char *argv[]) {};`

`tempcomp.c`	TEMP_COMP block model functions
	`double VMIN_GEN (double Temp) {};`
	`double VT_GEN (double Temp) {};`
	`double VT0_GEN (double Temp, int TINF) {};`

	double DIVIDER (double Temp, double Vin, double Vref) {}; struct Iout TRANSLIN_SQ (double isig) {}; double V_I_CONV (double Temp, double Vin, double Vin0) {}; double IU_CONV2 (double Temp, int SQ, struct Iout Iin, double V0) {}; double IU_CONV4 (double Temp, int S4, struct Iout Iin, double V0) {}; double SUM_AMP (double Temp, int LIN, double Vmin, double Vt, double Vt0, double Vsq, double V4p, double VC) {}; double Temp_Comp (double Temp, int TINF, int LIN, int SQ, int S4, double VC) {};
core.c	Crystal oscillator core model function + complex number functions + temperature dependence functions struct complex cdbl (const double Re, const double Im) {}; struct complex cadd (const struct complex A, const struct complex B) {}; struct complex cmult (const struct complex A, const struct complex B) {}; struct complex cdiv (const struct complex A, const struct complex B) {}; double RTFtemp (const double Temp, const double Rvalue) {}; double CMIMtemp (const double Temp, const double Cvalue) {}; double Betatemp (const double Temp, const double Bvalue) {}; double Core (const double Temp, const double factual) {};
varactor.c	Varactor model function double Varactor (double Vvar, double Temp) {};
cdac.c	CDAC model function double Cdac (double Temp, int CDAC) {};
crystal.c	Quartz crystal model function double Xtal (double Temp) {};
random.c	Random Number Generator functions double drand48() {}; double RandNumGen (int stat_mode, double par_avg, double par_tol, int distrib) {};
control.c	Simulation controller functions void ParaVecFileInput (FILE *pfile, struct ParaVec *p) {}; void ParaVecSave (struct ParaVec *SafePlace) {}; void ParaVecRestore (struct ParaVec *SafePlace) {}; void ParaVecCopy (struct ParaVec *Dest, struct ParaVec *Src) {}; void ParaVecStatistics (struct ParaVec *Current, int StatPart) {}; struct ParaVec Simu_Controller (int SimMode, int N, int StatPart, double **Matrix) {};
algorm.c	Trimming algorithm functions void PrintOut3x3 (double A[3][3]) {}; void mmult3x3 (double A[3][3], double B[3][3], double result[3][3]) {}; double det (double A[3][3]) {}; void minv3x3 (double A[3][3], double result[3][3]) {}; struct ParaVec Trim_Algorithm (int k, int Stat_Part, double **Matrix) {};
postproc.c	Post-processor functions void CheckForSpec (struct spec *Spec, char *buf, int m, double **Matrix) {}; void Post_Processor (struct spec *Spec, char *buffer[], int N, int DataType, double **Matrix) {};

VI.4. System simulation report

In this section, the goals stated in Section VI on page 90 are addressed.

VI.4.1. Operation check of DualOscillator TCXO with allowed tolerances of the system components

The allowed tolerances for the system parameters along with the distribution functions are given in Sections VI.2 and VI.3. The check was made in Simulation Mode 3 (trimming mode), where a large number of TCXO's with statistically dispersed parameters were generated and subsequently a trimming algorithm was simulated to evaluate its ability and the trimmability of the individual TCXO's.

Three variations of the simulation were done (see Section VI.3.6 on page 96):

1) only crystal has statistical model (TCXO has nominal model);
2) only TCXO has statistical model (the crystal has nominal model);
3) both TCXO and the crystal have the statistical models.

In each of the three cases above, a simulation of 10'000 (TCXO+crystal) systems were done.

VI.4.2. The "worst case" combinations of tolerances of the system parameters

The worst case in the DualOscillator TCXO operation was identified, when the loss resistance of the crystal in the macromodel was larger than +20% of the nominal and the g_{mstart} of the XO core was more than 10% smaller than the nominal value. This combination of parameters yielded quite a large number of oscillators, that would not start at all. There were no other parameters that influenced the operation so heavily.

The remedy for this problem would be increasing the g_{mstart} parameter from its initial value, 3.57 µS (about 45% of 10'000 oscillators were not starting at some temperature when both TCXO and the crystal had statistical models) to about 9 µS, which resulted in 3 non-starting oscillators out of 10'000 in the same simulation conditions. This phenomenon was confirmed in DualOscillatorT2, where some of the oscillators had startup problems in different temperatures.

In the next version, DualOscillatorT4, the XO core was redesigned to have larger g_{mstart} than the T2 version. Also the adaptive bias generator was left out and replaced with a bipolar PTAT bias current generator, which has the advantage of yielding nearly constant g_{mstart} in whole temperature range, when MOS transistors in subthreshold are used.

VI.4.3. The most suitable trimming algorithm for the TCXO

In the present trimming simulations, the following trimming algorithm was used.

1. Measure f1, f2 and f3 at T1, T2, T3 of TCXO, while holding VCOUT = const;
2. Using the T1, T2, T3, and f1, f2 and f3 calculate Tinf using least squares 2-nd order curve fit;
3. At T=Tinf adjust TINF(5:0) so that VT0=V(TE1);
4. At T=Tinf adjust CDAC(5:0) and VC so that:
   - f=40.000 kHz;
   - VCOUT is about 0.58 V;
5. At T=Tinf+20 adjust SQ(3:0) so that f=40.000 kHz;
6. At T=Tinf–20 adjust LIN(3:0) so that f=40.000 kHz;
7. Repeat 5. and 6. until frequency error from 40.000 kHz becomes <2 ppm;
8. At T=Tinf+35 adjust S4(3:0) so that f=40.000 kHz
9. At T=Tinf–35 adjust LIN(3:0) so that f=40.000 kHz
10. Repeat 8. and 9. until frequency error from 40.000 kHz becomes <2.5 ppm
11. Repeat 5. … 9. until frequency error will be <2 ppm at T=Tinf±20 and be <2.5 ppm at T=Tinf±40;
12. Adjust CDAC so that frequency error becomes minimal at T=Tinf.

As the trimming results obtained with this algorithm were not satisfactory in all aspects, a development of an alternative trimming algorithm was started.

A result of trimming simulation is shown in Figure 107.

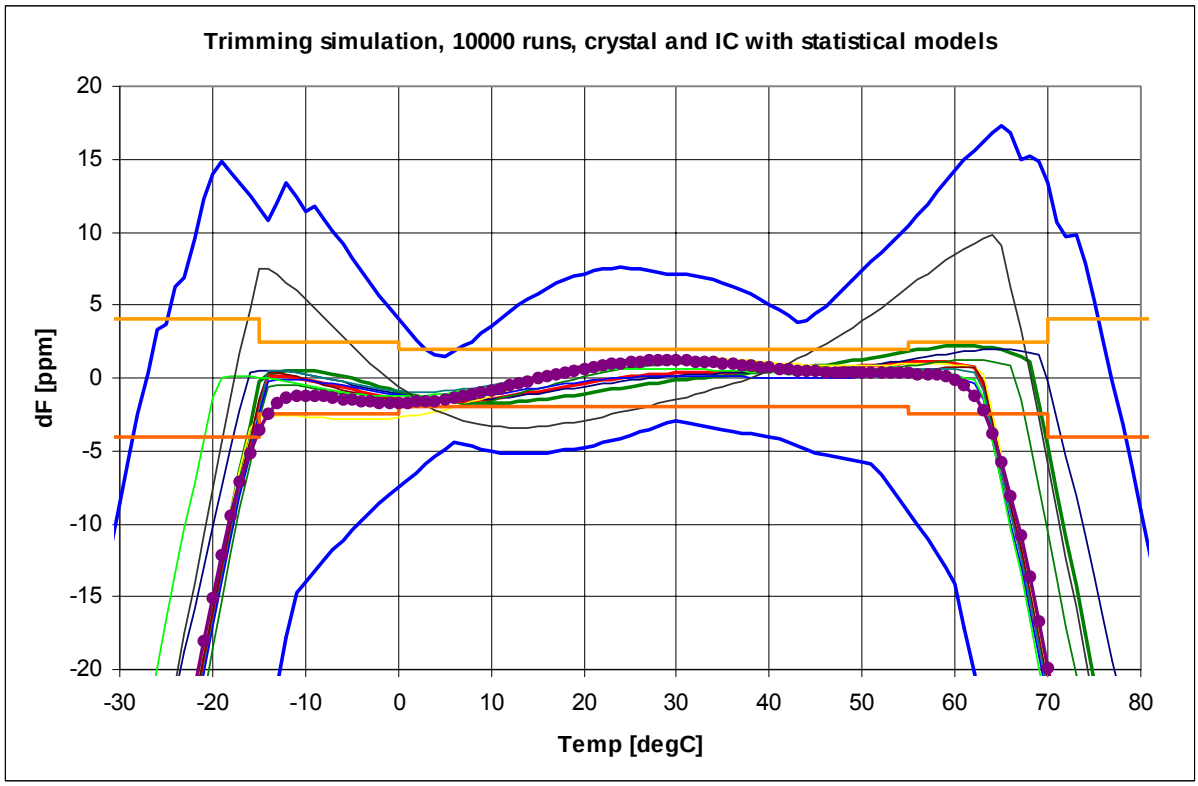


Figure 107. Trimming simulation results (min/max: blue lines, average: magenta line with markers, specification lines: orange, others are some curves of the 10'000 simulations)

VI.4.4. The correctness of the system-level design of DualOscillator TCXO

The correctness of the system-level design was evaluated using the previously obtained simulation results (three sets of 10'000 simulations). The contents of trimming registers TINF, CDAC, S4, SQ and LIN and also the control voltage VC were extracted from the simulation results and the histograms of the resulting trimming register values were created. The histograms are shown in the figures below.

Comments about the histograms: As it can be seen, the crystal tolerances have much larger influence on system performance than the IC process variations. It is also interesting to note that negative VC control voltage is required in both cases, when crystal tolerances are involved. This is clearly non-practical situation and might be a weak point in the trimming algorithm or an logical error in the simulation program. This issue will be addressed later. It should also be noted that the LIN code in all three cases is at its minimum code in most of the cases and SQ, on the contrary, is at mostly at the maximum code. S4 is more moderately distributed and has peaking at both minimum and maximum codes. This might indicate the need for wider tuning range for the corresponding polynomial coefficients.

VI.4.4.1 Histograms for the case when crystal has statistical model and TCXO has nominal model

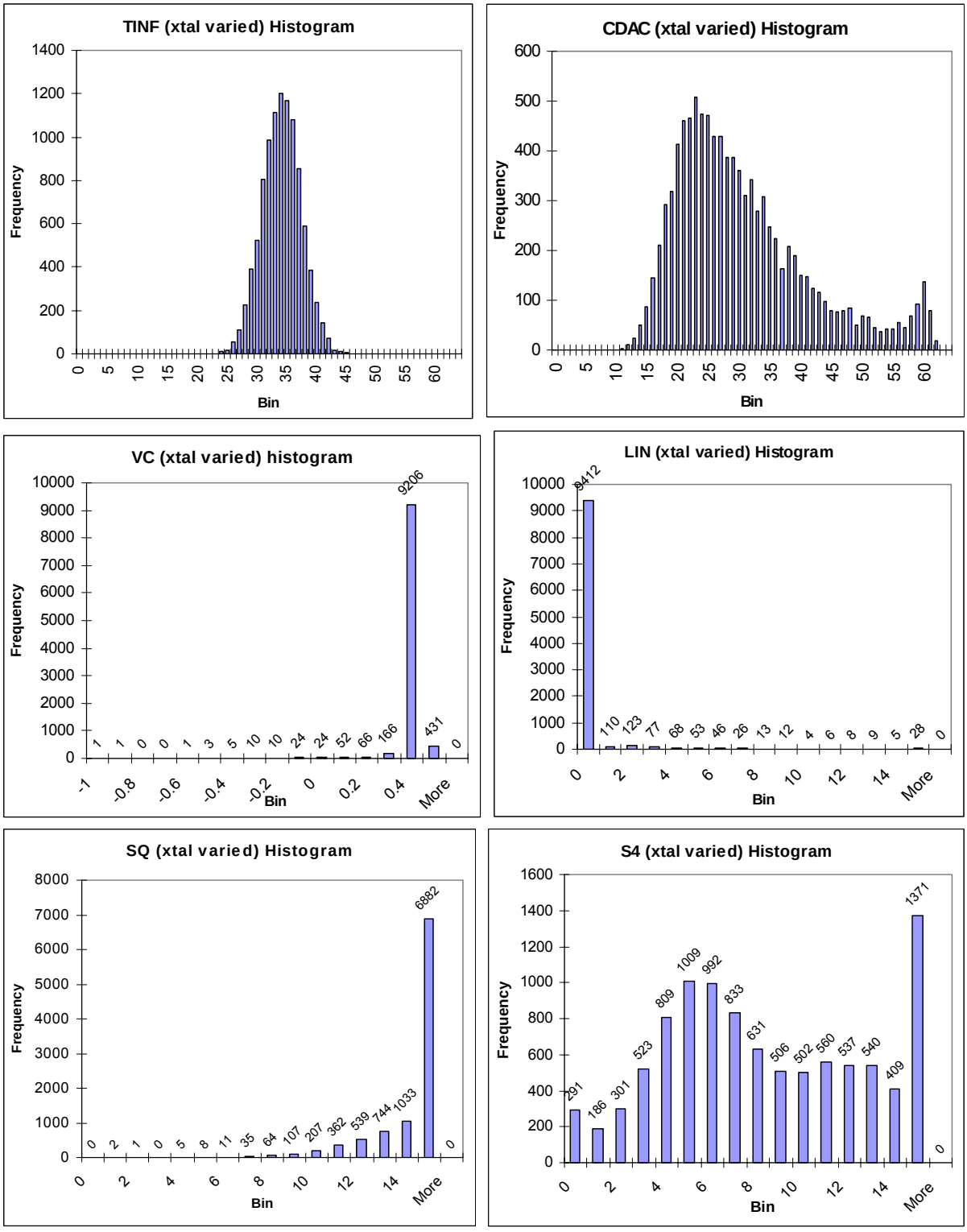


Figure 108. Histograms of trimming values, when crystal parameters vary statistically (IC is nominal)

VI.4.4.2 Histograms for the case when crystal has nominal model and TCXO has statistical model

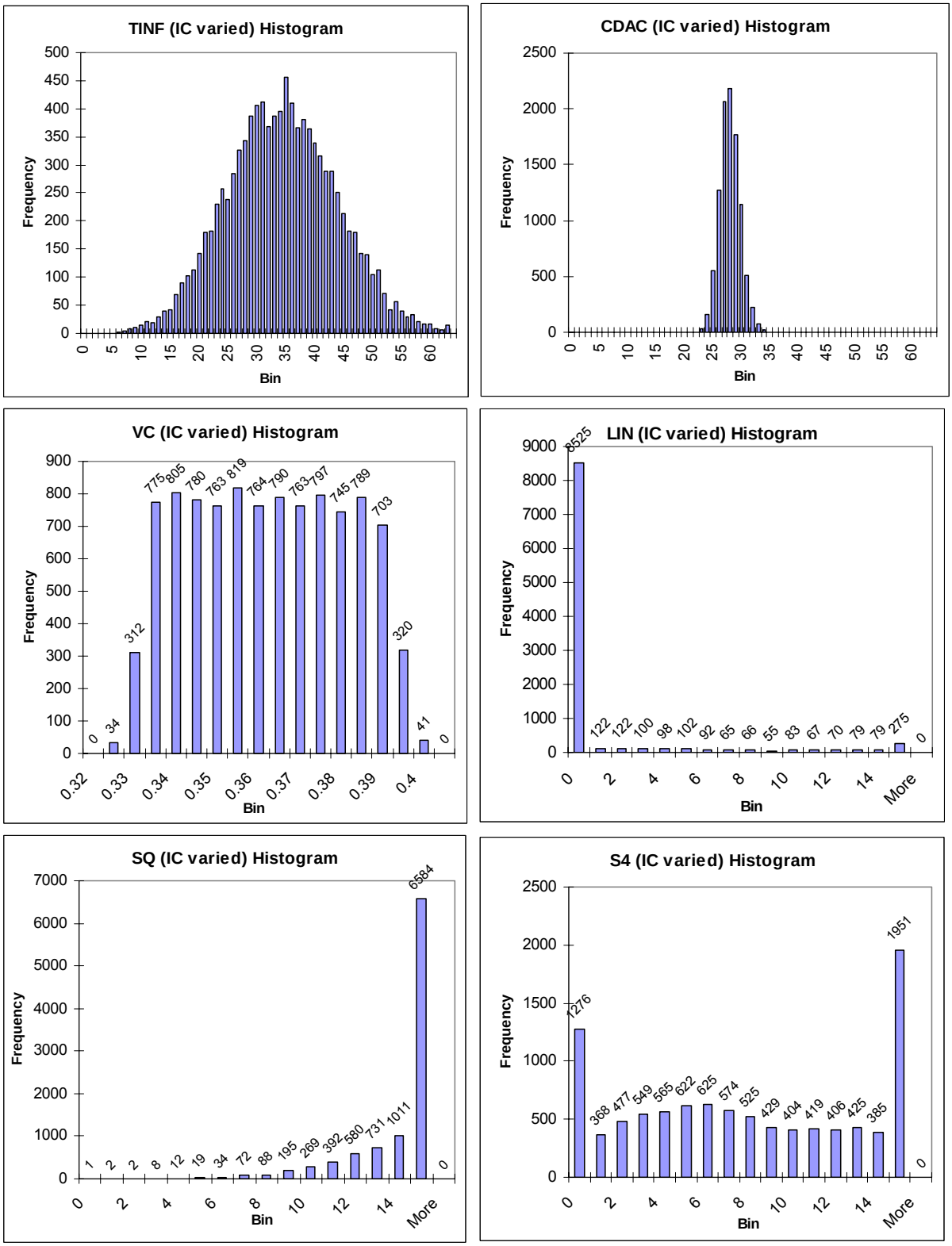


Figure 109. Histograms of trimming values, when IC parameters vary statistically (crystal is nominal)

VI.4.4.3 Histograms for the case when both crystal and TCXO have statistical models

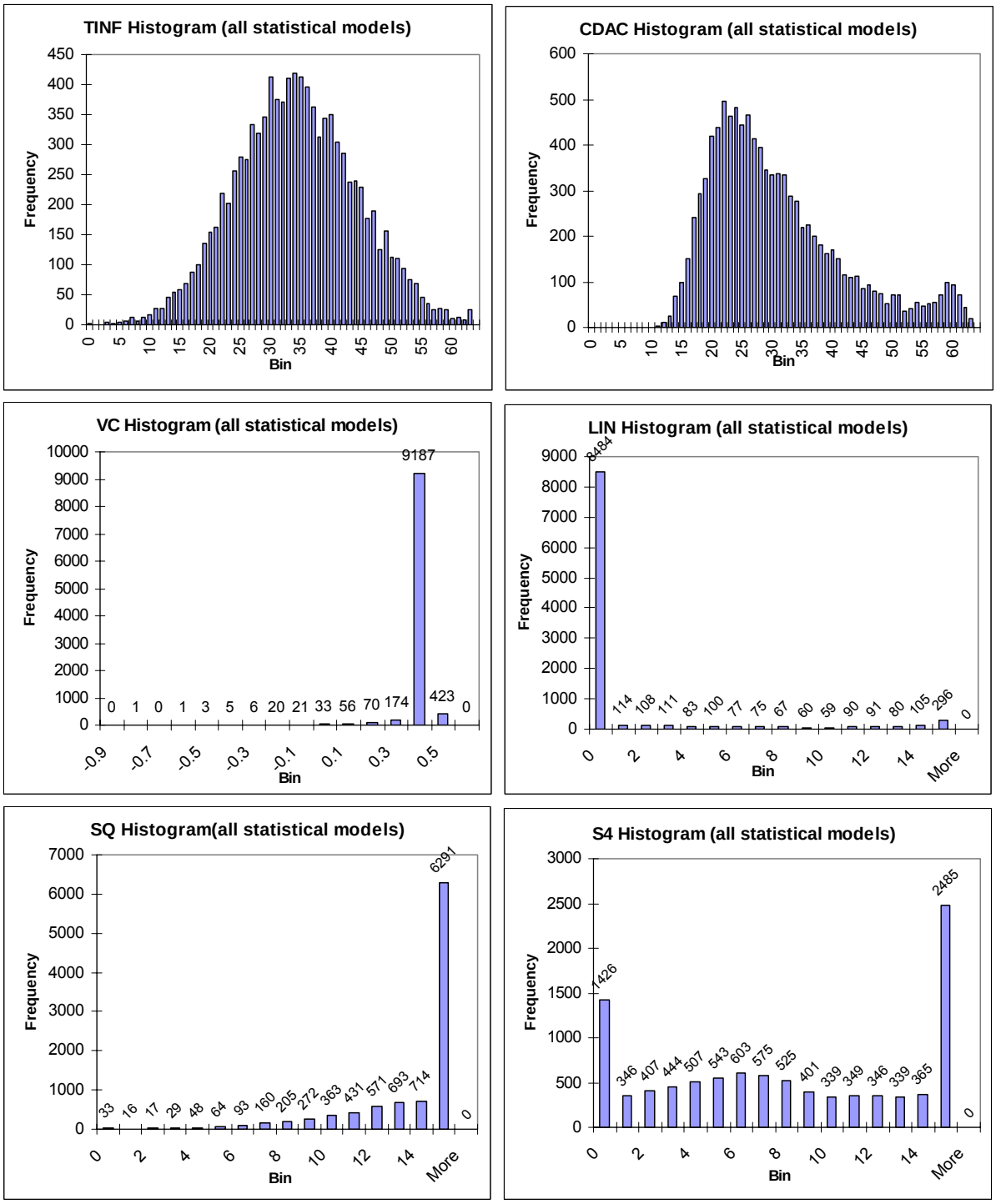


Figure 110. Histograms of trimming values, when both crystal and IC parameters vary statistically

VI.5. Conclusion

The system-level program implementing a macromodel for the DualOscillator TCXO and the 40 kHz tuning-fork crystal macromodel based on Micro Crystal CC1V03 quartz resonator was written and used for evaluating the circuit performance. It was discovered, that the g_{mstart} parameter (the transconductance of the oscillator core transistor) in the oscillator core should be increased from 3.57 μS to about 9 μS because of the startup problems, which were discovered during system-level simulations. This modification has been made in the DualOscillatorT4, which has been put to MPW2621 (week 47/2003).

As it can be seen from the histograms in the subsections VI.4.4.1, VI.4.4.2 and VI.4.4.3, the crystal tolerances have much larger influence on system performance than the IC process variations. It is also interesting to note that negative VC control voltage is required in the two cases, when crystal tolerances are involved. This is clearly non-practical situation and might be a weak point in the trimming algorithm or a logical error in the simulation program. This issue will be addressed elsewhere.

It should also be noted that the LIN code in all three cases is at its minimum code in most of the cases and SQ, on the contrary, is mostly at the maximum code. S4 is more moderately distributed and has peaking at both minimum and maximum codes. This might indicate the need for wider tuning range for the corresponding polynomial coefficients.

The alternative trimming algorithm will be designed in the future. The polynomial coefficient tuning range problem will also be investigated.

In conclusion, a project-specific system-level simulation tool was built and successfully used in DualOscillator design.

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Elulookirjeldus

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HARIDUSTEE	• TTÜ doktorand alates septembrist 1999, kavandatud lõpetamine 2005. aasta suvel; • Tehnikateaduste magistri kraad Tallinna Tehnikaülikoolist 1996–1999, arvuti- ja süsteemitehnika teaduskonnast; • Inseneridiplom Tallinna Tehnikaülikooli automaatikateaduskonnast elektrotehnika ja telekommunikatsiooni erialalt 1991–1996 (5-aastase õppekava alusel); • Fr. R. Kreutzwaldi nim. Võru 1. Keskkool 1988–1991, matemaatika ja füüsikakallakuga klass; • Võru 3. 8-klassiline kool 1980-1988; • Muude õpingute kõrvalt: Võru Lastemuusikakool, akordioni eriala 1985–1990.
ERIALANE SPETSIALISEERUMINE ÕPINGUD VÄLISMAAL	***Alates 1999:*** IC disaini projektijuht Analoogdisaini AS-is; läbi viinud mitmeid integraalskeemide disaini- ning uurimisprojekte, sh. kaasalöömine europrojektis MiMOSA: http://www.mimosa-fp6.com. ***1. juuli 1996 kuni praeguse ajani:*** Mitmesugused mikroelektroonika- (komponentide modelleerimine CAD-tarkvaras) ja skeemitehnika (vooluallikad, operatsioonvõimendid) alased kursused (Micro Analog Systems OY, Mentor Graphics Finland); ***10.–19. juuni 1996:*** Kursus "Low-power, high-frequency integrated circuits course" Helsingi Tehnikaülikoolis ***Novembrist 1995 kuni aprillini 1996***: Diplomitöö tegemine Rootsi Kuningliku Tehnikaülikooli (KTH) elektroonikasüsteemide disainilaboris (ESDlab). Töö teema oli üldistatud immitantsikonverterite (GIC) realiseerimine Ericsson AB EPIC3B 0.6-µm BiCMOS integraalskeemitehnoloogias. Testskeem valmis 1998. aasta kevadeks. ***Juuni-august 1995***: Õpingud ja töö TIMA mikroelektroonikalabori juures Prantsusmaal, Grenoble'i Rahvuslikus Polütehnilises Instituudis (INPG). Töö

	teema oli mikrotermopaaride geomeetriliste ja muude parameetrite optimiseerimine (näit. tundlikkus ja ajakonstant). Muuhulgas õppisin tundma integraalskeemide tehnoloogiaid, ning eriti põhjalikult CMOS-protsessi.
PUBLIKATSIOONID	1. M. Koort, V. Kukk, "Interactive Circuit Synthesiser", Proc. of Baltic Electronics Conference, Tallinn, Estonia, Oct. 7—11, 1996, pp. 245—248. 2. M. Koort, V. Kukk, "Interactive Synthesiser Development", Proc. of First Electronic Circuits and Systems Conference, Bratislava, Slovakia, Sept. 4—5, 1997, pp. 67—70. 3. P. Ööpik, M. Koort, R. Kipper, V. Kukk, "High-Q Bandpass Filters Based on Immittance Converters", Proc. of ECCTD'97, Budapest, Hungary, August 30—Sept. 3, 1997, pp. 599—604. 4. P. Ööpik, M. Koort, R. Kipper, V. Kukk, "High-Q Active Bandpass Filters", Proc. of First Electronic Circuits and Systems Conference, Bratislava, Slovakia, Sept. 4—5, 1997, pp. 133—136. 5. H. Tenhunen, M. Koort, V. Kukk, "Implementation of Impedance Converters in BiCMOS-Technology", Proc. of Baltic Electronics Conference, Tallinn, Estonia, Oct. 7—11, 1996, pp. 405—408. 6. M. Koort, V. Kukk, "Principles of Interactive Analog Circuit Synthesis", in Proc. of Second Electronic Circuits and Systems Conference, Bratislava, Slovakia, Sept. 1999., pp. 67—71. 7. M. Koort. Võimsuse juhtimine GSM-mobiiltelefonis. Elektroonika 2000, VII rahvusvahelise telekommunikatsioonipäeva konverentsi ettekannete materjalid. TTÜ ja Eesti Elektroonikaühing, Tln. 2000, lk. 57—67. 8. M. Koort, "RF Power Amplifier Control Curve Approximation", in Proc. of Baltic Electronics Conference BEC2000, Tallinn, Oct. 8—11, 2000, Tallinn, Estonia, pp. 71—74. 9. M. Koort, E. Kängsep, V. Kukk, "Design of RF Power Detector", in Proc. of European Conference on Circuit Theory and Design ECCTD'03, Sep. 1—4, 2003, Krakow, Poland, pp. II-273—II-276 10. M. Koort, E. Kängsep, V. Kukk, "An RF Power Detector", in Proc. of 4th Electronic Circuits and Systems Conference ECS'03, Sep. 11—12, 2003, Bratislava, Slovakia, pp. 175—178.
TÖÖ	***Juuli 1996–praeguseni: AS Analoogdisain***: Integraalskeemide (IC) disainer. IC disainiprojektide juhtimine, arvutidisain (CAD), süsteemitaseme disain, elektriskeemide koostamine ja simuleerimine, laotuse (layout) joonistamine, integraalskeemide testimine, programmeerimine, arvutivõrgu haldamine, uute IC disainerite väljaõpetamine.
	Alates septembrist 2000 TTÜ siduteooria ja -disaini õppetooli teadur osalise tööajaga (valitud 5 aastaks). Kandideerin samale akadeemilisele positsioonile ka järnevaks valimisperioodiks (sept. 2005 – sept. 2010) ***September 1993 – juuni 1996*** ***Tallinna Tehnikaülikooli Sidu- ja Süsteemiteooria Õppetool***: Insener (osalise tööajaga). Aktiiv- ja passiivfiltrite projekteerimine ja arvutamine ning komponentide väärtuste optimiseerimine; programmeerimine, arvutidisain, skeemide simuleerimine, interaktiivne süntees.
VÕÕRKEELTE OSKUS JA HOBID	***Keeled***: emakeel – eesti keel, inglise keel – väga hea, vene keel, soome keel – hea, rootsi keel – rahuldav, saksa keel, prantsuse keel – elementaarteadmised. ***Hobid:*** Elektroonika, arvutid, programmeerimine, jahindus, fotograafia, keeled, kirjanduse lugemine originaalkeeles.
TEGUTSEMINE ELUKUTSELIITUDES	Institute of Electrical and Electronics Engineers (IEEE): Üliõpilasliige (Student Member) 1996; Täisliige (Member) alates 1997–

Curriculum Vitae

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EDUCATION	• PhD student in TUT since Sept. 1998, planned graduation time: summer 2005; • M. Sc. E. E. scientific degree from TUT (1996—1999), dept. of Computer Science and Automation; • Engineer's Diploma from department of Automation in TUT on Electrical Engineering and Telecommunications 1991–1996 (5-year curriculum); • Fr. R. Kreutzwald's Võru 1st Secondary School 1988–1991, math and physics-biased class; • 3rd Elementary School in Võru 1980-1988; • Besides other studies: Võru Children's Music School, accordion 1985–1990.
PROFESSIONAL SPECIALIZATION STUDIES ABROAD	***Since 1999:*** IC design project manager in Analoogdisaini AS; carried out several projects in the field of research and design of integral circuits. Participation in European Project MiMOSA: http://www.mimosa-fp6.com. ***July 1st 1996 up to now:*** Various courses on microeletronics design (modelling of circuit elements in CAD software, current source and operational amplifier design) by Micro Analog Systems OY, Mentor Graphics Finland; ***June 10th–19th 1996:*** Low-power, high-frequency integrated circuits course in Helsinki UT ***November 1995 until April 1996***: Writing Diploma Thesis by Electronics System Design lab (ESDlab) in Royal University of Technology in Stockholm, Sweden (KTH). The topic of research was integrated realization of generalized-immittance converters (GIC) in Ericsson's EPIC3B 0.6-µm BiCMOS IC process. The chips were fabricated by spring 1998 ***June-August 1995***: Studies and research by TIMA microelectronics lab in Grenoble, France. The research subject was optimization of micromachined

	thermopiles with respect to performance parameters like sensitivity and time constant. Among other, I learned IC technology basics with special focus on CMOS fabrication process.
PUBLICATIONS	1. M. Koort, V. Kukk, "Interactive Circuit Synthesiser", Proc. of Baltic Electronics Conference, Tallinn, Estonia, Oct. 7—11, 1996, pp. 245—248. 2. M. Koort, V. Kukk, "Interactive Synthesiser Development", Proc. of First Electronic Circuits and Systems Conference, Bratislava, Slovakia, Sept. 4—5, 1997, pp. 67—70. 3. P. Ööpik, M. Koort, R. Kipper, V. Kukk, "High-Q Bandpass Filters Based on Immittance Converters", Proc. of ECCTD'97, Budapest, Hungary, August 30—Sept. 3, 1997, pp. 599—604. 4. P. Ööpik, M. Koort, R. Kipper, V. Kukk, "High-Q Active Bandpass Filters", Proc. of First Electronic Circuits and Systems Conference, Bratislava, Slovakia, Sept. 4—5, 1997, pp. 133—136. 5. H. Tenhunen, M. Koort, V. Kukk, "Implementation of Impedance Converters in BiCMOS-Technology", Proc. of Baltic Electronics Conference, Tallinn, Estonia, Oct. 7—11, 1996, pp. 405—408. 6. M. Koort, V. Kukk, "Principles of Interactive Analog Circuit Synthesis", in Proc. of Second Electronic Circuits and Systems Conference, Bratislava, Slovakia, Sept. 1999., pp. 67—71. 7. M. Koort. Võimsuse juhtimine GSM-mobiiltelefonis. Elektroonika 2000, VII rahvusvahelise telekommunikatsioonipäeva konverentsi ettekannete materjalid. TTÜ ja Eesti Elektroonikaühing, Tln. 2000, lk. 57—67. 8. M. Koort, "RF Power Amplifier Control Curve Approximation", in Proc. of Baltic Electronics Conference BEC2000, Tallinn, Oct. 8—11, 2000, Tallinn, Estonia, pp. 71—74. 9. M. Koort, E. Kängsep, V. Kukk, "Design of RF Power Detector", in Proc. of European Conference on Circuit Theory and Design ECCTD'03, Sep. 1—4, 2003, Krakow, Poland, pp. II-273—II-276 10. M. Koort, E. Kängsep, V. Kukk, "An RF Power Detector", in Proc. of 4th Electronic Circuits and Systems Conference ECS'03, Sep. 11—12, 2003, Bratislava, Slovakia, pp. 175—178.
PROFESSIONAL CAREER	***July 1996 until nowadays: AS Analoogdisain***: Integral circuit (IC) designer. Leading IC design projects, CAD, system-level design, composing and simulation of electrical schematics, drawing IC layout, testing of IC's, programming, computer network administration, and training of new IC designers.
	Since September 2000 part-time research scientist in chair of circuit theory and design in TUT (for 5-year election period). I also apply for the same academic position for the next election period (Sept. 2005 – Sept. 2010) ***September 1993 – June 1996*** ***Chair of Circuits and Systems Theory in TUT***: Part-time engineer. Design of active and passive electronic filters, optimization of filter component values, programming, CAD, simulation, interactive circuit synthesis.
LANGUAGES AND HOBBIES	***Languages***: Estonian – Mother's tongue, English – very good (spoken and written), Russian, Finnish – good, Swedish – satisfactory, German, French – elementary knowledge ***Hobbies:*** Electronics, computers, programming, hunting, photography, languages, reading literature in original languages.
ACTIVITY IN PROFESSIONAL SOCIETIES	Institute of Electrical and Electronics Engineers (IEEE): Student Member 1996; Member since 1997–

Publications

1. M. Koort, V. Kukk, “Interactive Circuit Synthesiser”, Proc. of Baltic Electronics Conference, Tallinn, Estonia, Oct. 7—11, 1996, pp. 245—248.
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10. M. Koort, E. Kängsep, V. Kukk, “An RF Power Detector”, in Proc. of 4th Electronic Circuits and Systems Conference ECS’03, Sep. 11—12, 2003, Bratislava, Slovakia, pp. 175—178.