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High-κ Metal Oxide Thin Film by Chemical Spray Pyrolysis: From Optimization of Material Properties to Application in Thin Film Transistor

ABAYOMI TITILOPE OLUWABI

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TALLINN UNIVERSITY OF TECHNOLOGY
School of Engineering
Department of Materials and Environmental Technology
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Supervisor: Ilona Oja Acik, Dr.
Department of Materials and Environmental Technology
Tallinn University of Technology, Tallinn, Estonia

Co-supervisor: Malle Krunks, Prof.
Department of Materials and Environmental Technology
Tallinn University of Technology, Tallinn, Estonia

Arvo Mere, Dr.
Department of Materials and Environmental Technology
Tallinn University of Technology, Tallinn, Estonia

Opponents: Thomas Dittrich, PD Dipl. Phys. Dr. Habil.
Institute of Silicon Photovoltaics
Helmholtz Zentrum Berlin, Germany

Kaupo Kukli, Dr.
Research Professor in Materials Science
Institute of Physics
University of Tartu, Estonia

Defence of the thesis: 19/08/2020, at 13:00pm, lecture hall U06A-229.

Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for doctoral or equivalent academic degree.

Abayomi Titilope Oluwabi

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Metallioksiidi õhukesed kiled keemilise pihustuspürolüüsi meetodil: materjali omaduste optimeerimine ja rakendamine õhukesekilelistes transistorides

ABAYOMI TITILOPE OLUWABI

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Contents

List of Publications

The list of author's publications, on the basis of which the thesis has been prepared:

I **A. T. Oluwabi**, A. O. Juma, I. Oja Acik, A. Mere, and M. Krunks. Effect of Zr doping on the structural and electrical properties of spray deposited TiO_2 thin films. Proceedings of the Estonian Academy of science, 2018, 67, 2, 147–157.

II **A. T. Oluwabi**, I. Oja Acik, A. Katerski, A. Mere, and M. Krunks. Structural and electrical characterisation of high-κ ZrO_2 thin films deposited by chemical spray pyrolysis method. Thin Solid Films, 2018, 662, 129–136.

III **A. T. Oluwabi**, A. Katerski, E. Carlos, R. Branquinho, A. Mere, M. Krunks, E. Fortunato, L. Pereira, and I. Oja Acik. Application of ultrasonic spray zirconium oxide dielectric in zinc tin oxide-based thin film transistor. J. Mater. Chem. C, 2020, 8, 3730–3739.

IV **A. T. Oluwabi**, D. Gaspar, A. Katerski, A. Mere, M. Krunks, L. Pereira, and I. Oja Acik. Influence of post-UV/ozone treatment of ultrasonic-sprayed zirconium oxide dielectric films for low-temperature oxide thin film transistor. Materials, 2020, 13, 6, 1–14.

Author's Contribution to the Publications

Contribution to the papers in this thesis are:

I Deposition of Zr doped TiO_2 thin film by spray pyrolysis, characterization of the film, analysis of results, and major role in writing.

II Deposition of ZrO_x thin film by spray pyrolysis, characterization of the thin film, analysis of results, and major role in writing.

III Deposition of ZrO_x thin film by spray; deposition of the ZTO layer by spin coating, characterization of the layers, fabrication device, characterization of TFTs, analysis of results, and major role in writing.

IV Deposition of ZrO_x thin film by spray, UV-Ozone surface treatment, thin film characterizations, fabrication of TFT, analysis of the device, and major role in writing.

Introduction

Transistors are key component in modern electronic devices, and they are often used to amplify or switch electronic signals [1]. The first transistor was developed in 1957, ever since then, it has undergone a progressive development from the traditional silicon-based transistor to the metal oxide semiconductor field effect transistor (MOSFET) or the thin film transistors (TFTs) [2, 3].

The application of TFT in transparent electronic display was first envisaged in a science fiction novel titled, "The shape of Things to come" by Herbert George Wells in 1930s [4]. Now, the discovery of metal oxide semiconductor or conductor materials that can be made transparent have made the idea about transparent electronic displays truly conceivable [3]. As a matter of fact, the concept of transparent electronic display has been industrialised and the first commercial product (such as liquid crystal displays) have been produced massively since 2011 by Samsung [5, 6].

The fundamental research on TFTs have been driven towards addressing development of a stable, reliable, light weight, and cost-effective transistor [7, 8]. However, based on the prediction of the International Technology Roadmap (ITR) [9], the scaling down of a TFT device is gradually approaching the atomic scale, and further size reduction would no longer be possible due the possibility of reviving the problem of leakage current through the dielectric layer [9]. This problem was solved by Intel technology when they replaced conventional SiO_2 dielectric with HfO_2 dielectric in their 45 nm technology in 2007 [6, 10]. The success achieved by Intel was because HfO_2 has high permittivity (high-κ) value, which will help to achieve same capacitance needed to reduce the leakage current [11].

The recent integration of high-κ dielectric material in flexible electronic has led to a paradigm shift in the transparent oxide electronic market where the next generation of electronic display is expected to be employed in disruptive applications like wearable sensors, electronic skin, and internet of things (IoT) [12]. Flexible TFTs based on high-κ dielectric are considered a superior option when compared to the conventional rigid Si technologies, as they offer a unique advantage of lightweight and low processing temperature [13]. However, this brings a new challenge in TFT fabrication as the current methods of production require an expensive vacuum-based technology, which is not simple to maintain and not easy to scale for mass production. To achieve a cost effective transparent and flexible TFTs, solution processing method which is perhaps an easy and cheaper method needs to be adopted [14, 15]; however, this method still requires high processing temperature to decompose the organic residue originating from the precursor. Thus, a facile post-deposition treatment like ultraviolet-Ozone (UVO) treatment would be needed to help facilitate low temperature processing.

Although, solution processed method like chemical spray pyrolysis (CSP) has the potential to reduce the fabrication cost and can be easily scaled for mass-production; but, its adoption in electronic fabrication industry would take a long time because the conventional methods have been optimized to outperform the emerging rival like CSP. In this respect, this thesis will demonstrate the application of CSP as a viable fabrication method, capable of fabricating metal oxide TFT with excellent performance that can be compared to the conventional vacuum based methods.

Organization of thesis:

This research work is aimed at strategizing the development of high-κ metal oxide thin film as the gate dielectric layer in low-cost solution processed TFT, but the primary

optimization and integration of high-κ metal oxide thin film in transistor is of major concern. The use of CSP method, which utilizes an ultrasonic atomizer offers the possibility to fabricate low-cost dielectric films with high scalability for industrial production. Therefore, this work will extend the potential application of CSP to flexible electronic applications.

Based on the literature survey, there are few numbers of publications on the fabrication of metal oxide TFTs by CSP method in the past ten years, and little is known about the deposition and integration of high-κ metal oxides like titanium dioxide (TiO_2) or zirconium oxide (ZrO_x) as the gate dielectric layer in TFT by CSP method. In fact, the fabrication of TFTs by CSP at low processing temperature has not been reported.

In order to achieve the target aim, some specific issues were addressed in this work, and they serve as objectives of the study: Firstly, to demonstrate the influence of doping on the properties of TiO_2 thin films. Secondly, to develop and optimize the deposition of zirconium oxide (ZrO_x) thin film by CSP. Thirdly, to lower the processing temperature of CSP deposited ZrO_x through UVO post-deposition treatment. Finally, to integrate the optimized ZrO_x gate dielectric in fully solution processed TFTs. In all experiments, the morphological, structural, optical, and electrical properties of the deposited thin films either Zr-doped TiO_2 or ZrO_x thin film was investigated. For the TFT fabrication, only the ZrO_x thin film whose derived properties gave the most comprehensible electrical and physical requirement was incorporated in TFT. The experiment that led to the development of the ZrO_x dielectric material was carried out at the Laboratory of Thin Film Chemical Technologies in the Department of Material and Environmental Technology, TalTech, Estonia. The fabrication and characterization of fully solution metal oxide TFT as well as the optimization of the metal oxide channel layer was done at i3N/CENIMAT, FCT-NOVA, and CEMOP/UNINOVA, Portugal.

The findings presented in this thesis is based on four published articles and sub-divided into three sections by chapters. The first chapter is the literature overview where the basic operational principles and different architectures in TFT are reviewed. Also, the important TFT parameters, the knowledge gap, and the basic aim and objective of this research work is succinctly highlighted. In the second chapter, the experimental methods and processes are described. The characterization techniques and methods are explained with details. The results and discussions of the research work is divided into four different sections, in the third chapter. Each section focuses on each published paper starting from the development of dielectric layer to the incorporation of the optimized layer as the gate dielectric layer in TFT.

This work is directly related to the ongoing research project in the Laboratory of Thin film Chemical Technologies, which is focus on the development of high-κ metal oxide thin film by wet-chemical process for electronic application. This study was financially supported by the Estonian Ministry of Education and Research project IUT194, Estonian research council grant PRG627, TTÜ based financing project B24, and the European Union through the European Regional Development Fund project TK141 “Advanced materials and high-technology devices for energy recuperation systems”. The Archimedes foundation financed the research mobility through the “DoRa Plus Action 1”, and ASTRA “TTÜ Institutional Development Program for 2016 – 2022” Graduate School of Functional Materials and Technologies (2014-2020.4.01.16-0032).

Abbreviations, Terms and Symbols

a-Si:H	Hydrogenated amorphous Silicon
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
CMOS	Complementary Metal Oxide Semiconductor
CSP	Chemical Spray Pyrolysis
C-V	Capacitance Voltage
C-F	Capacitance Frequency
DUV	Deep Ultraviolet radiation
IGZO	Indium gallium zinc oxide
IoT	Internet of Things
ITO	Indium tin oxide
I-V	Current voltage measurement
SEM	Scanning electron microscope
T_{anh}	Annealing temperature
TTIP	Titanium isopropoxide
TFT	Thin Film Transistor
TCO	Transparent Conductive Oxide
L/W	Aspect ratio (length to width) of the channel layer
LED	Light Emitting Diode
LCD	Liquid Crystal Display
MIS	Metal Insulator Semiconductor
MO	Metal oxide
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
OLED	Organic Light Emitting Diode
Poly-Si TFT	Polycrystalline silicon thin film transistor
R2R	Roll-to-Roll
RMS	Root mean square
SC	Spin coating
S/D	Source-drain electrode
SP	Spray pyrolysis
SS	Subthreshold slope
Sqrt-I_{DS}	Square root of the trans-conductance
USP	Ultrasonic spray pyrolysis
UV	Ultraviolet light
UVO	Ultraviolet-Ozone
V_S	Voltage at source terminal
V_D	Voltage at drain terminal
V_G	Voltage at gate terminal
XRD	X-ray diffraction
XPS	X-ray photoelectron spectroscopy
$Zr(acac)_4$	Zirconium acetylacetonate
ZTO	Zinc tin oxide

C_i	Area capacitance
eV	Electron volt
κ	Permittivity

μ	Mobility
μ_{fe}	Field effect mobility
μ_{sat}	Saturation mobility
I_{on}/I_{off}	On-to-off state current ratio
L	Channel length
W	Channel width
ΔG	Change in Gibbs free energy

1 Literature overview

The early years of research on transistor started from the Bells laboratory by Lilienfeld and Heil in 1940s [16 – 19]. Although, it took over ten years for the first thin film transistor (TFT) to be made by the vacuum based technology. At that time, TFT device was made of gold electrodes, a polycrystalline cadmium sulfide (CdS) n-type channel, and a silicon monoxide (SiO) dielectric [3, 16]. Now, TFT has undergone a lot of developments such as size reduction, flexibility, cost, resolution, and speed.

There are authors [3, 20] that have succinctly explained in detail about the physics and architecture involved in TFTs. Herein, the thesis literature survey shall focus on the fundamentals of TFTs: their architecture, operations, and brief historical trends. Relevance is drawn toward the emerging oxide TFTs, gate dielectric layer, processing methods, and post deposition treatment.

1.1 TFT structures, working principle, and parameters

1.1.1 Structure and working principle

Structure

TFTs are three terminal field-effect devices, which consist of the electrodes (gate, source and drain), dielectric layer, and the channel layer. The dielectric layer insulates the channel from the gate electrode [3]. TFTs can be fabricated in different architectures, which are top-gate (coplanar or staggered) configuration shown in Fig. 1.1 (a, b); and bottom-gate (coplanar or staggered) configuration also shown Fig. 1.1 (c, d).

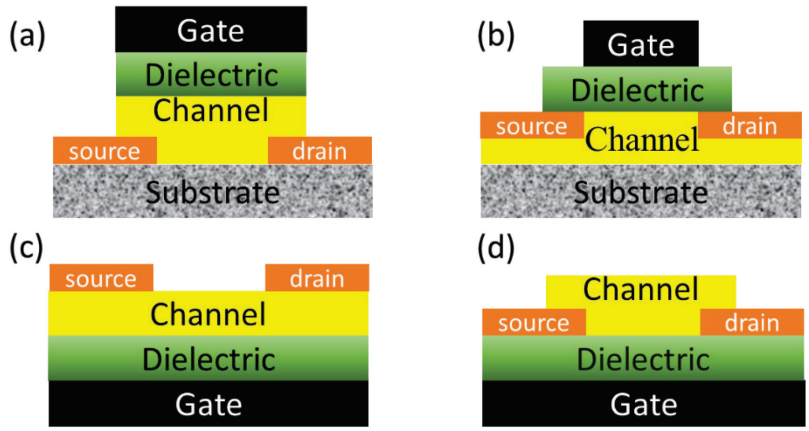

Figure 1.1. Different fabrication structures of thin-film transistor: (a) top-gate staggered TFT; (b) top-gate coplanar TFT; (c) bottom-gate, staggered TFT; and (d) bottom-gate coplanar TFT.

The advantages or disadvantages of these architectures are strongly dependent on the properties of the materials used during the fabrication process [16]. As an example, the top-gate staggered structure (Fig. 1.1 (a)) is mostly used in the fabrication process of Hydrogenated- amorphous silicon thin film transistors (a-Si:H TFTs) because the a-Si:H layer is protected by the metal gate electrode from light interference, and it is easy to fabricate. For a polycrystalline Silicon TFT (poly-Si TFT), the top-gate coplanar structure (Fig. 1.1 (b)) is mostly preferred because it favors a flat channel layer TFTs. Secondly, high

temperature is required to crystallize the poly-Si layer, which can affect other layers of the device [21]. The bottom-gate structures (either staggered or coplanar, Fig. 1.1 (c, d) is mostly used for oxide based TFTs especially the solution processed methods, but with this structure the surface of the channel layer is exposed making it susceptible to environmental influence; nevertheless, it can be solved by passivating the device [22].

Working principle

The working principle of TFT relies on the accumulation of carriers at the interface between two vertically aligned channel and dielectric layers, and the carriers that flows within the channel layer is modulated by the application of electric field at the interface [3]. For effective modulation of the source to drain carriers a dielectric layer with high capacitance must be employed [23]. Since electric field effect are generated in a typical TFT device, they are often confused with metal oxide semiconductor field effect transistor (MOSFET) [16]. The differences between TFT and MOSFET are: First, the channel layer in TFTs is a thin film deposited either by vacuum or solution method, while MOSFETs are fabricated on a single crystalline Si-wafers. Second is the migration of carriers, which in TFTs is by accumulation of electron, while in MOSFET it is by inversion [24]. This is the reason why n-type MOSFET have a p-type silicon substrate and an n-type TFTs has an n-type semiconductor [3, 16, 23 – 24].

Figure 1.2 shows the schematic representation of n-type TFT in saturation regime operating in enhancement mode (electron transporting). By grounding the source and drain (V_S, $V_D = 0$), and applying a positive voltage to the gate V_G, higher than the threshold voltage V_{TH}, we make an accumulation of charge carriers at the channel/dielectric interface whose density diminishes exponentially with its distance from the interface [25 – 27]. For every slight increase in the value of V_D there will be charge infusion at the source electrode, which creates current flow I_D, within the channel to the drain. Under these conditions the device obeys the ohm's law as an ordinary resistive component [27]. When the strength of the V_D is comparable to the induce V_G, the dielectric field strength of the dielectric layer is still enough to maintain charge accumulation [25]. As V_D increases, so I_D will keep on expanding linearly until it reaches the 'pinch off point', where the current flowing in the device is saturated. This statement about what happens between the S/D electrodes can be express as: $V_x = V_G - V_{TH}$ [25]

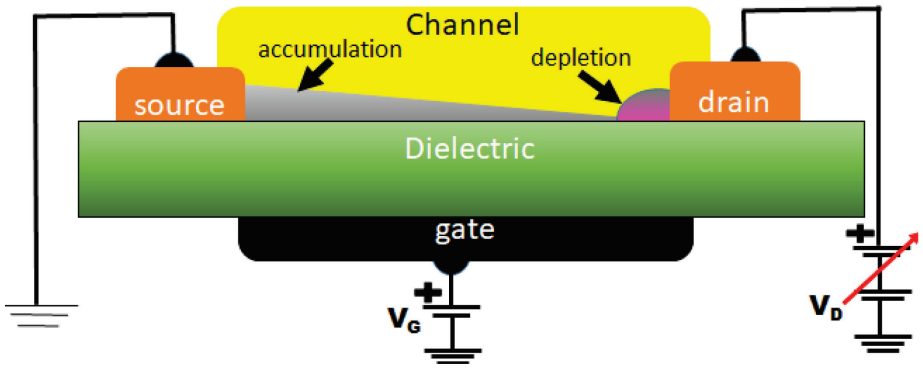

Figure 1.2. Illustration of n-channel thin film transistor showing graphical representation of both the depletion and accumulation regions. Assuming the device is at saturation where $V_D > V_G - V_{TH}$ [25].

1.1.2 Important device parameters

TFT device parameters can be characterized at two main conditions: (1) the transfer shown in Fig. 1.3 (a), and (2) the output shown in Fig. 1.3 (b). Based on these conditions certain parameters are extracted from the device under test [3, 28, 29]. Fig. 1.3 (a) depicts the behavior of the device as a function of gate voltage (V_{GS}) bias at constant drain voltage. It is important that for all measurement taken in this regime the voltage at the source electrode must be zero. Fig. 1.3 (b) shows a linear plot of the drain current (I_{DS}) as a function of the drain voltage (V_{SD}) at different V_G sweeps. In addition, the pinch off region is also graphically identified on Fig. 1.3 (b), which is a point where the TFT is completely independent of V_{SD}, at this point the drain is depleted of charge carriers due to the insufficient electric field strength of the dielectric layer [25].

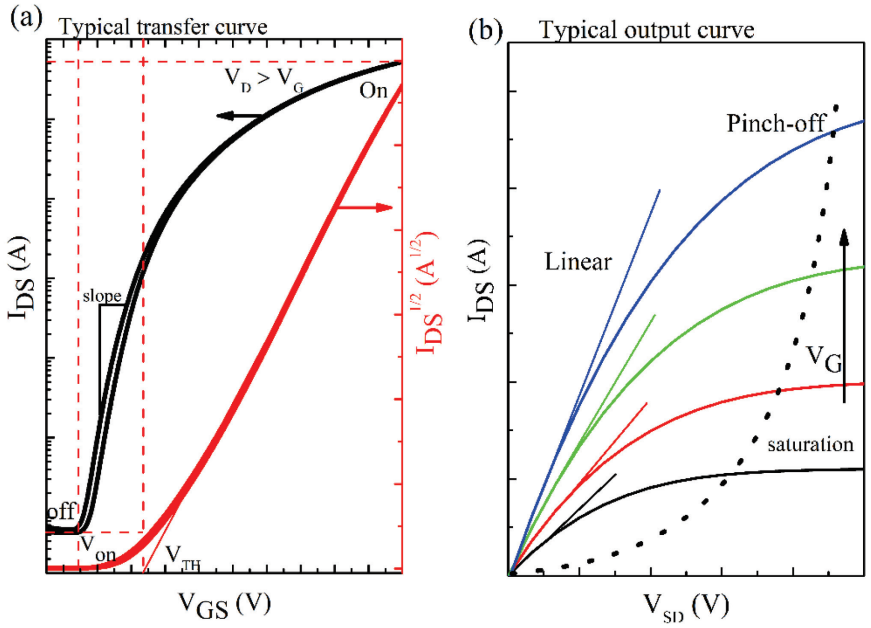

Figure 1.3. (a) Transfer curve showing the drain current as a function of gate bias. (b) Output curve showing the linear and saturation regimes [25].

Magnitude of the on-off current ratio (I_{on}/I_{off}): It can be determined by calculating the ratio between the maximum and the minimum current flow within the drain-source terminal of the device [25]. The higher the value of on/off ratio, the lower the amount of leakage current, that is, low power is dissipated during the off-state measurement of the device [16]. On/off ratio, above 10^6 are required for effective switching.

Mobility (μ): This parameter quantifies the amount of charge carriers available to migrate across the active site of the transistor. It gives information about the efficiency of the device in terms of mobility of electron or hole within the device. This parameter is often affected by a lot of other factors like device structure, nature or type of scattering mechanism within the material. Generally, the mobility can be extracted depending on the value of the drain terminal voltage [24].

- Linear mobility (μ_{lin}): V_{SD} is lower than V_{GS}

$$I_{DS} = \frac{W}{L}\mu_{lin}C_i\left[(V_{GS} - V_{TH})V_{SD} - \frac{V^2{}_{SD}}{2}\right]$$

Where W and L are the width and length of the channel respectively, C_i is the capacitance per unit length of the dielectric layer, μ_{lin} is the linear mobility of charge carrier (electron or hole), and V_{TH} threshold voltage [25].

- Saturation mobility (μ_{sat}): V_{SD} is greater than V_{GS} [16]

$$I_{DS} = \frac{W}{2L}\mu_{sat}C_i(V_{GS} - V_{TH})^2$$

Threshold Voltage (V_{TH}): This parameter gives information about the minimum gate voltage at which significant current starts to flow from the source to the drain terminals within the active layer or accumulation layer. We can also get information about the electronic trap site at the channel/dielectric interface. Since TFT operates as a result of gate voltage bias, V_{TH} give a physical understanding on how depleted or invasive the semiconductor layer and the electronic mode at which the TFT is capable of working [6].

Subthreshold slope (SS): This value can be obtained from the maximum slope of the TFT transfer curve. It practically represents how the value of current flowing through the source-drain terminals can increase in one decade under a relatively increased gate voltage (V_{GS}) bias. This value should be reasonably small as it reflects the consumption power of the device [24].

$$SS = \left(\frac{dlog(I_{DS})}{dV_{GS}}\right)^{-1}$$

In this part, the structure, theory, and the extraction of data from a TFT device under test has been reviewed. However, the optimal performance and efficiency depends on the properties of the channel and dielectric materials; hence it is important to review the material development of TFTs.

1.2 Brief review on TFT development and application

1.2.1 General TFT materials

The development of transistor started at Bell's Laboratory in 1940s, but it was at the Radio Corporation of America's (RCA) laboratories that the first TFT was developed in 1962 [16], and by 1970s it became a component in consumer electronics [3]. Different classes of materials such as silicon, metal oxides, organic, and graphene can be employed in TFT as depicted in Fig 1.4. The hydrogenated amorphous silicon (a-Si:H) was first introduced as suitable material in liquid crystal displays (LCDs) in 1979 [30]. In 1982, a-Si material was later introduced in TFT by Cannon as a dot matrix display [31] and became prevalent for many years serving as a major material in TFT fabrication until the metal oxide revolutionized the industry.

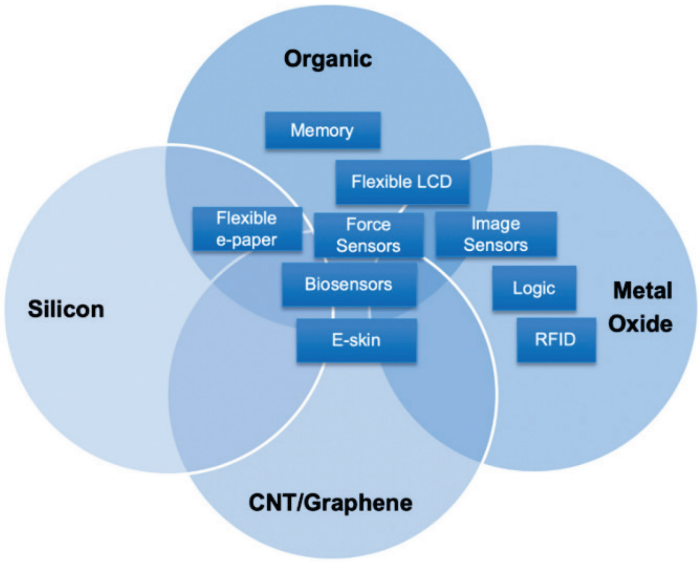

Figure 1.4. Venn diagram illustrating the relationship between the different classes of TFT materials and their possible applications in the industry [32]. The chart is based on the reports on flexible TFT technology that was compiled by a TFT consulting firm based in the UK.

TFTs can be used in a range of applications in as much as there is a class of material that can be employed [16]. For example, organic and silicon materials are mostly used in flexible electronics, while the metal oxide have revolutionized the display and logic applications [24]. Carbon-based materials like cellulose, graphene is recently employed in flexible or stretchable microelectronic, biochemical sensing, and e-skin [15, 16].

As at 2018, the global market forecast for transparent electronics have grown to nearly $7.1 billion [14, 33]. Analysis from the forecast indicated that electronic market would grow at a compound annual rate of 21.73% and 121.3% for lightweight and stretchable devices respectively in the future [14]. Now, in order to meet the future demands in electronic, researchers in this field are working on development of suitable TFT material that will address issues like size reduction, scalability, flexibility, and fabrication cost [15]. Among the classes of materials presented in Fig 1.4, the metal oxide (MO) has the highest interest because they have a degree of stability due to the ionic bonding between metal and oxygen atoms [25], MOs have good electrical properties due to the spatial distribution of metal in their s orbital state, which makes it possible to form the high conduction band serving as an electronic pathway for mobile charge carriers [14, 34].

1.2.2 Metal oxide based TFTs

Metal oxide (MO) based TFTs are transistors whose channel and dielectric layers are based on metal oxide materials. The advantages of this material are that, they have high mobility of charge carriers, optically transparent, and they can be amorphous or crystalline [35]. The atoms of crystalline MO are chemically bonded with strongly bonded together with low concentration of defects in the lattice [36]. Atoms of crystalline MO are delocalized, which means that there is freedom for electron and hole transportation [35, 37, 38].

The first MO TFT was made with SnO_2 and In_2O_3 channel layer in 1964 [39, 40], but due to poor performance compared to a-Si TFTs the research was stopped. In 2003, it later took off when Masuda et al. [38], Hoffman et al. [35], Carcia et al. [41] reported ZnO TFT with mobility (μ) > 1 $cm^2V^{-1}s^{-1}$. Nomura et al. [37] reported on quaternary transparent semiconductor oxide (TSOs) like indium gallium zinc oxide (IGZO), developed by epitaxial growth on SiO_2 dielectric layer; which later became an active electronic component in LCD displays in 2012 [24]. Most of the reports on MO TFTs demonstrated that high post-deposited treatment above 500 ^oC is needed to improve the microstructure and charge mobility properties MO thin films [41]. However, it was the work of Hosono et al. [42] on a-IGZO based TFTs by laser deposition and the work of Fortunato et al. [43] on ZnO based TFT by RF magnetron sputtering that demonstrated the possibility of fabricating MO-TFT at room temperature.

In the past decade, MO TFTs have established its usefulness as the active matrix in liquid crystal displays or LED displays because of high mobility (μ > 10 $cm^2V^{-1}s^{-1}$). However, the a-IGZO MO material has been mostly preferred over the ZnO as a suitable channel material [44]. The a-IGZO material is uniform, stable, and has a low charge carrier density. Thus, ensures the fabrication of TFT with low off-state current ~10^{-13}A [45]. The method of fabrication at that time was vacuum based methods and they were well established because of the reliability and good TFT device performance [46]. However, the method of fabrication was expensive and difficult to maintain due to complex vacuum system [3].

The solution processed methods started in 2001 when solution processed ZnO was introduced as the channel layer in TFTs [47]. It was considered as an alternative to the vacuum based method; nevertheless, this method has faced numerous challenges such as low film quality, low brightness due to low mobility, non-uniformity, high processing temperature, and instability [36]. Most of the research on MO TFTs by solution methods have focused on the development of the channel materials, such as zinc oxide (ZnO), indium zinc oxide (IZO), indium gallium zinc oxide (IGZO), zinc tin oxide (ZTO), In_2O_3, indium tin oxide (ITO), and SnO_2. Furthermore, amorphous and crystalline structures have been reported for the channel layer of most MO TFTs, and they have both exhibited n-type characteristics. High electron mobility of about 90 $cm^2V^{-1}s^{-1}$ has been reported for solution processed MO TFTs [15]. The interest in fully amorphous oxide TFTs stems up from the fact that amorphous metal oxide film is smooth with low density of state, which means they are less defective [38, 41], and smooth surface is needed to improve interface quality of the device to yield good electrical performance [46]. Thus, the application of amorphous MO TFT has been prevalent in display technology as the active matrix layer [48]. For instance, top electronic companies like Sharp, LG, and Samsung who are known to produce smart phones, laptops, flexible TVs among others have easily adopted the MO-TFTs in their technology. Furthermore, MO-TFTs can be employed in other innovative applications like flexible biological sensors [49], X-ray detector [50, 51], and neuromorphic computing.

Based on the review, research on MO TFTs have focused on the channel layer, while the development dielectric layer which plays an important role in TFT lags; hence the need to start developing MO materials for dielectric layer in TFT. Amorphous MO materials control the interest in oxide TFTs [37] and revolutionized the electronic display market. It would be an excellent approach to consider the application of MO-TFTs in light sensors, biosensor, integrated circuits, e-skin, and radio frequency applications like rectifiers or energy harvesters.

1.3 Dielectric layer of thin film transistor

The dielectric layer insulates the channel layer from the gate electrode. The development of the dielectric materials is lagging as opposed to the channel materials [25, 46]. However, several reviews on dielectric materials have focused on a class of material with high permittivity (high-κ) because they possess high gate capacitance needed to reduce leakage current caused by quantum tunneling effect [15, 52]. High-κ dielectrics can be of different materials like polymer, electrolyte, organic, inorganic, and hybrid [52]. This review will be focused on inorganic metal oxide high-κ dielectrics. This group of elements is empirically the best choice of dielectric for future electronic, but the selection process is not simple, and many aspects must be taken into consideration [6].

1.3.1 Criterial for choosing metal oxide dielectric

In TFT, it is important that the surface of dielectric layer is smooth in order to improve the quality of the interface between layers; hence amorphous structure is mostly required. The electric field strength of the layer must be large (>4 MV cm^{-1}), the leakage current density must be low (<1 nA/cm^2 at 1 MV cm^{-1}), relative high-κ value greater than 7, and the interface defect density with the semiconductor layer must be low [29]. The reasons for these are briefly explained below:

1. High permittivity (κ): This is an important factor to consider before selecting potential dielectric material for TFT. Its value is mainly influenced by the dipole moment of the material, which in the case of most inorganic high-κ metal oxide is facilitated by their d-state electrons [6]. High κ value is advised, but too large κ is also unrequired, because this could lead to polarization of electric field between the drain electrode and the dielectric layer; thus, lowering the barrier between source to channel, and it can also affect the threshold voltage (V_{TH}) of the device [53, 54].
2. Bandgap (E_g): The bandgap is the width between the valence band and the conduction band of a material. Its value varies in different materials due to difference in structure and electronic transition within the materials [52]. In high-κ MO E_g is controlled by the electronegativity of metal ions, and their small band offset is caused by the d-state electrons, and the high coordination of ionic bond [55]. However, there is a trade-off between E_g and κ, because the E_g of most inorganic high-κ dielectric is inversely proportional permittivity (κ) as depicted in Fig. 1.5. This has imposed a major difficulty in choosing suitable dielectric material, because there are several of such possibilities e.g. ZrO_2, Al_2O_3, CaO, MgO, TiO_2 etc. that can be considered as high-κ dielectric materials, but not all are suitable. Therefore, it is required that in selecting a suitable gate dielectric material, the κ-value should be in the range 20 – 30, and the E_g should be greater than 5 eV [56].

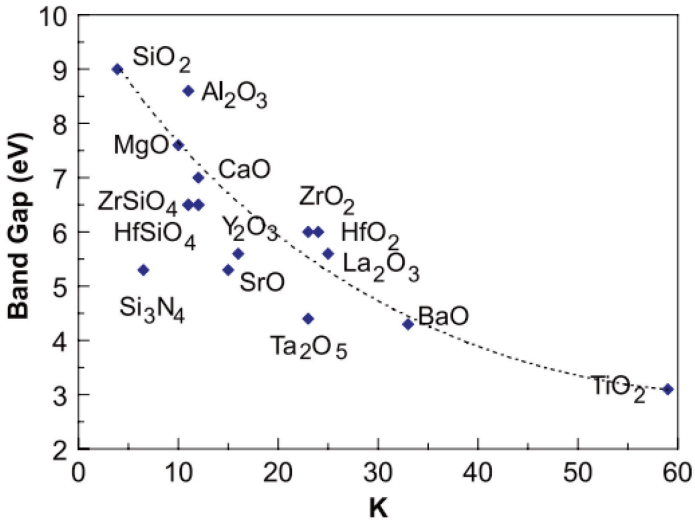

Figure 1.5. Bandgap versus permittivity *of most inorganic dielectric materials [56].*

3. Moisture adsorption: MO dielectric materials faces a crucial and inescapable problem of exposure to moisture and air. Therefore, resistance to moisture retention is an imperative issue for selection of high-κ dielectrics. The absorption speed is firmly related to the adjustment in Gibbs free energy, ΔG, during the reaction [56]. Large ΔG implies increased system energy, which tends to suppress moisture absorption [57], because high moisture absorbing material will degrade the electrical properties and resisted the practical applications of the selected gate dielectric layer of TFT [58].
4. Surface morphology and surface defects: In order to select a suitable dielectric layer, the surface morphology or surface defect must be considered, because it affects the quality of the interface, since charge transport occurs at close region to the interface [59]. Surface defects can dissipate and trap the charge carrier, resulting to the degradation or instability of the TFT device [60]. For a given high-κ MO dielectric, surface morphology and defect states are firmly related to the fabrication process and post-treatment conditions. Many of the MO materials on the Periodic table are very reactive with water, but the transition MOs are presumably stable, especially the Zr and Hf [6].

1.3.2 Processing methods for metal oxide dielectric

The processing of MO dielectric can broadly be grouped into the vacuum based methods and solution processed methods [61]. The former, also known as physical method includes several techniques such as sputtering, and pulsed laser deposition (PLD) [52]. Sputtering, for example, is suitable for the deposition of thin film with low contamination at low processing temperature. In addition, atomic layer deposition (ALD) is another class of vacuum deposition, which is often regarded as a solution-in-vacuum method. It is possible to deposit MO thin films with less pinholes at processing temperature ~ 300 ^{o}C [62]. In 2002, Kukli et al. reported the deposition of HfO_2 thin film grown by ALD [63]. The HfO_2 film deposited at 570 ^{o}C was 54 nm thick and exhibited a dielectric field strength of 2.0 MV/cm and effective permittivity (κ_{eff}) in the range 12 – 15. However, the cost of maintenance has been a major drawback for the scalability of ALD method [61, 64, 65].

On the other hand, solution processed methods offer a huge decrease in the maintenance and production cost, and they can easily be scaled for mass-production [6, 24]. In TFTs, solution processed methods are the only approach that can potentially address simple fabrication technique and high device performance [25], for this reason this review will be focusing solution processed methods.

The unique advantage of solution processed methods over vacuum-based method is the cost effectiveness [6], and the possibility to produce uniform film with excellent composition at high throughput [36]. There are several solution processed methods by which dielectric thin films can be deposited, for example, spin coating, dip coating, spray pyrolysis, bar coating, drop casting, and inkjet printing methods, all of which have their advantages and disadvantages [6]. These methods have been employed in depositing several high-κ MOs like TiO_2, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, and Y_2O_3 at least for the past ten years. Some of the properties of the common high-κ MOs dielectric films deposited by different processing methods are summarized in Table 1.1.

Table 1.1 Summary of deposition methods and dielectric properties of common high-κ metal oxides. Thickness (d), Area capacitance (C_i), Permittivity (κ)

Materials	Methods	T_{dep} (^oC)	d (nm)	C_i (nF/cm^2)	κ	Year	Reference
Al_2O_3	Spin coating	350	115	75	9.7	2013	[66]
	ALD	33	33	201	7.5	2004	[67]
	Spray pyrolysis	350	85	70	7.1	2016	[68]
	Bar coating	380	16	380	7.9	2015	[69]
	Sputtering	25	150	52	8.8	2014	[70]
	PLD	200	100	60	6.8	2014	[71]
ZrO_2	Spin coating	350	154	-	-	2011	[72]
	ALD	325	88	226	22.5	2001	[73]
	Spray pyrolysis	350	25	370	14.3	2016	[69]
	Inkjet	500	60	325	22	2015	[74]
	Sputtering	600	50	530	30	2008	[75]
TiO_2	Spin coating	250	23	560	27	2015	[76]
HfO_2	ALD	570	54	0.5	14.9	2002	[63]
	Spin coating	500	5.7	2953	19	2005	[77]
	Spray pyrolysis	450	104	151	18.8	2015	[78]
	Bar coating	380	16	409	11	2015	[69]

The state-of-art of solution processed high-κ dielectrics in TFTs show that it is possible to achieve a low leakage current, high permittivity, low operation voltage, high dielectric breakdown voltage, improved interface, and low defect density [25, 46, 79]. Many

developments such as novel precursor engineering have been employed in order to lower the processing temperature of solution processed dielectric material [80]. Shan et al. [81] use water induce precursor to reduce the volatility of complex organic ligand during the fabrication of ScO_x gate dielectric. Also, doping with metal cation or anion, and mixing of two or more high-κ oxides with each other in order to enhance the interface quality of TFT have been investigated [82]. Peng et al., have attempted scandium doping of ZrO_x gate dielectric [83], Yang et al. have demonstrated the zirconium doping of AlO_x gate dielectric to improve the electrical performance of a flexible TFT [82], and Fortunato et al., have investigated the use of multilayer dielectric layers to boost the electrical performance of solution processed TFT [84]. Among the several high-κ oxides, ZrO_2, Al_2O_3, and HfO_2 are gaining more preference because of higher band offset (above 2 eV) [46], lower trap density, and chemical stability [85].

Although, TiO_2 dielectric thin film may not attract a lot of interest for most n-type TFTs, but it can be targeted for hybrid dielectric or p-type TFTs [86]. TiO_2 dielectrics have a large value of κ (κ = 60), which means that phonon-limited carrier mobility will be lower when TiO_2 is employed as the gate dielectric layer.

1.3.3 Titanium oxide dielectric by solution processed methods

Titanium oxides (TiO_2) are attractive high-κ dielectric with unique optical and electronic properties [87]. Its high-κ value (~ 60) make it a target material for the dielectric layer in TFT. They exist in three different polymorphs like anatase [88], rutile [89], and brookite. They have been processed by solution methods like dip coating [90], spin coating [21] and spray pyrolysis [86]. Despite its attractiveness, the use of TiO_2 as potential gate dielectric in MO TFTs remains surprisingly unprogressive [91]. This is because the bandgap (3.0–3.4 eV) of TiO_2 is close to the conduction band of most n-type semiconductor material (e.g. ZnO, 3.2 eV) that are frequently used as the channel layer in TFTs, and in practice could cause an injection of electrons through the dielectric layer to the channel layer [16]. Anthopoulos et al have employed TiO_2 as the gate dielectric layer in TFT by spray pyrolysis [86]. TiO_2 thin film deposited by spin coating method have been reported in [21] and [90] as the gate dielectric layer of a p-type channel TFT.

Several efforts have been adopted to enhance the properties of TiO_2 and doping with either anionic or cationic impurities is one of them [92, 93]. Doping affect the band structure introducing an energy state within the band, which then alters the electronic and structural properties of the film [92, 94]. Chang and Doong [95], have reported a series of Zr doped TiO_2 experiments by sol-gel process. Studies have also shown that doping will improve amorphous phase formation [92], which is a required parameter for the dielectric layer of TFTs. According to literature survey, lots of work have been reported on Zr-doping of TiO_2 by sol-gel spin coating [95], but spray pyrolysis method has not been employed for Zr doping of TiO_2. The state-of-art of the application of Zr doped TiO_2 as the gate dielectric layer in TFT has shown that this material has not been used before.

1.3.4 Zirconium oxide dielectric by solution processed methods

ZrO_x thin films are optically transparent with wide bandgap energy (ca 5.8 eV). Its high permittivity value (ca 25) makes it a suitable candidate for gate dielectric layer of TFTs [96, 97, 82]. There are three different polymorphs of ZrO_x with each exhibiting different properties. These polymorphs are tetragonal (t), monoclinic (m), and cubic (c) [98, 99]. Vanderbelt et al., reported the average permittivity value for the three ZrO_x polymorphs, which are 47, 37, and 17 for tetragonal, cubic, and monoclinic ZrO_x, respectively. These

values were calculated using computational techniques [100]. The tetragonal or cubic phases of ZrO_x has been reported to exhibit high permittivity [62], but amorphous structure of ZrO_x is better for TFT because the films have smoother surface [82, 101, 102].

ZrO_x thin films have been processed by different solution methods like spin coating [103], spray pyrolysis [25], inkjet printing [82] among others. Shan et al. have reported on the performance of In_2O_3 TFTs based on ZrO_x gate dielectric layer deposited by spin coating, the device exhibited saturation mobility (μ_{sat}) of 3.08 $cm^2\ V^{-1}\ s^{-1}$ and the magnitude of the on-off state current ratio was 10^8 [103]. Peng et al., have investigated on the potential application ZrO_x gate dielectric layer in TFT by inkjet printing method [104]. Lee et al. reported on solution processed ZrO_x gate dielectric layer in ZTO based TFT on glass substrate after annealing at 500 ^oC. The device operated a low voltage (> 5V) with low hysteresis [105].

Based on the review, gate dielectric must exhibit a wide bandgap to insulate the channel layer from the gate electrode. The polarization in the dielectric material must not be too high as this affects the charge mobility in the channel [24]. It is very important to understand the synergy between the application of the device and the processing conditions of the material before selection any gate dielectric material [46]. TiO_2 and ZrO_x dielectric was also reviewed because they fit to the scope of this thesis, and they can be easily processed by spray pyrolysis for wide area deposition; although, post-deposition treatment is required to enhance the film quality.

1.4 Processing of metal oxide thin film transistor by solution methods

The processing of MO TFTs by solution processed techniques and the different post deposition treatments employed will be reviewed in the following subsection.

1.4.1 Solution processed methods employed in thin film transistor

Typical solution deposition method involves a chemical conversion of precursor through hydrolysis and decomposition reactions [25, 106]. There are several of these methods, but just a few of them are briefly discussed below:

1. Spin coating: This method is often used to deposit dielectrics or channel films on a substrate. The advantage of this method is that it is cost-effective and very easy to operate [107]. Spin coating method has great reproducibility, and simple integration with conventional micro-fabrication systems [6]. It can be used for nanoparticle-based processing, sol–gel route, and organic-inorganic-type routes, permitting fast deposition of oxide films [59]. This method wastes a lot of precursor solution (about 95%) during the deposition, and the thin film suffers poor uniformity when deposited on large substrate. Thus, this method is limited to small area fabrication. Hwang et al. have also demonstrated the role of precursor salt on deposited a-IGZO thin film by spin coating [108]. Talapin and his team [6, 80, 109] deposited high-κ ZrO_2 dielectrics, with CdSe n-channel (NC) transistors exhibiting an extreme mobility record of μ_{fe} = 450 $cm^2\ V^{-1}\ s^{-1}$.
2. Spray pyrolysis: Spray pyrolysis is a cheap and simple deposition method, suitable for large area deposition [110]. The film is grown by spraying an aerosol precursor solution with the aid of a carrier gas onto preheated substrate, where the constituents experience a chemical reaction [111]. The unique advantage of this method over other methods is the degree of freedom for mixing precursor solution, suitable for doping, no wasting of material, and it is not selective to substrate type [112, 113]. Anthopoulos et al., have previously reported a series

of work on the application spray pyrolysis MO-TFT fabrication [25, 91, 113]. They reported on outstanding performance for Li:ZnO based TFT with high I_{on}/I_{off} ~10^6, and high ionic mobility μ_{fe} = 85 $cm^2 V^{-1} s^{-1}$ [78, 114] by spray using ZrO_x gate dielectric. Based on the limited number report from the review, the full potential of this deposition method in TFT fabrication has not been reached yet.

3. Inkjet printing: This is a unique and emergent noncontact solution deposition method [6]. Mechanism of ink ejection from the nozzle can either be thermally or piezo-electrically induced, and this influences the morphology of the deposited film. Similarly, there other important parameters like nozzle type, temperature, viscosity, and wettability of target substrate, which influences the quality of the film produced [46, 115]. This method does not require additional lithography, it requires small amount of ink, and it can be suitable for narrow area deposition. This method is limited by the choice of ink, viscosity, and it tends to suffer the problem of agglomeration of film [46]. Subramanian et al., have previously reported on the deposition of Sb doped SnO_2 electrode, SnO_2 semiconductors, and ZrO_2 dielectric [116]. Jang et al. [117] have printed ZrO_2 (d ≈ 40 μm) dielectric thin film with low leakage current ~10^{-5} A cm^{-2} at 1 MV cm^{-1}, and an electric field strength surpassing 4.0 MV cm^{-1}. They reported a fully inkjet-printed MO TFT fabricated on glass substrate with high mobility μ_{fe} = 11 $cm^2 V^{-1} s^{-1}$, high I_{on}/I_{off} = 10^6, and operates at low voltage (<5.0 V).

The reviewed deposition methods have been employed in MO TFTs, but the potential of spray pyrolysis has not been fully acclaimed. Currently, this method still requires high processing temperature and more work is needed to reduce the process temperature in order to target the application of this method in flexible TFTs.

1.4.2 Post-deposition treatments employed in thin film transistor

Thin films made by solution methods often require post-deposition treatments. There are several of these treatments, but the common post-deposition treatments employed in solution processed MO TFT is summarized this section (Fig. 1.6) and briefly explained.

1. Conventional treatments*:* Conventional treatments are vacuum annealing, thermal annealing, microwave annealing and vapor annealing. They are used to improve the quality of thin films after deposition [6]. Some of these methods require a great deal of energy; hence, they can be ineffective. They also require high temperature that can lead to increased thermal budget. Zhu et al. reported on spin coated ZrO_x gate dielectric, which was tested in an InO_x based-TFTs [118, 119]. The device was thermally treated at temperature range of 250 – 300 °C, and the obtained mobility (μ_{fe}) from the device changes from 1.8 $cm^2 V^{-1} s^{-1}$ to 10.78 $cm^2 V^{-1} s^{-1}$ with increase in the thermal treatment. Also, Peng and co-worker fabricated a fully ink-jet printed InGaO-based TFTs using ZrO_x dielectric layer, a high mobility of 10.8 $cm^2 V^{-1} s^{-1}$ was achieved after hard baking the film at 350 ^oC [83].
2. Plasma treatment: The process involves the generation of a reactive oxygen species called plasma, which oxidizes the surface of the deposited thin film. This method is suitable for the removal of organic impurities from the film surface. Meena et al. investigated and build a low temperature O_2 plasma-assisted method for fabricating solution-based HfO_2 dielectric layer on adaptable polyimide (PI) substrates [120]. Prior to plasma treatment, the HfO_2 film has a leakage current ~10^{-5} A/cm^2 and dielectric breakdown voltage lower than 1 MV/cm. After the treatment process, the leakage current was reduced by 3

order of magnitude and the breakdown voltage was doubled [6]. This method can be employed for the treatment ZrO_x or AlO_x thin films [121].

3. Ultraviolet assisted treatment: This is a photo-activation process that involves the use of light energy to lower the annealing temperature of most solution processed films [46]. Two types of UV light sources have been considered: high pressure mercury light (1 kW, prevailing wavelength = 365nm) [122, 123]; and low-pressure mercury Hg light, with two deep UV (DUV) emission peaks at 253.7 (90%) and 184.9 nm (10%) have been reported. Park et al. was the first to test an ultrathin (d = 6.3 nm) ZrO_x thin film produced from an acetylacetonate precursor by spin coating at almost room temperature after treating the film under a high-pressure UV irradiation [124, 125]. During the UV treatment, organic residues emanating from the precursor salt on the surface of the gel films were oxidized leaving behind the Zr and O atoms on the film's surface [126].

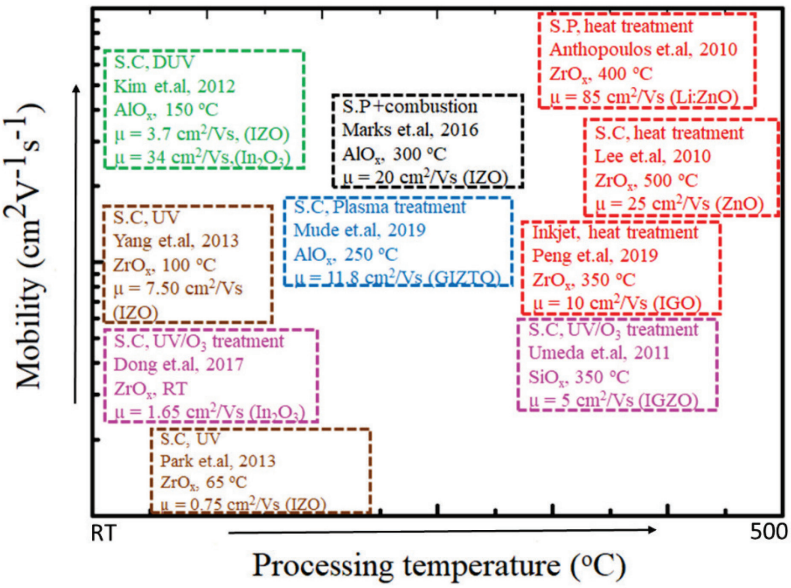

Figure 1.6. Recent published results for MO TFTs fabricated by some of the common solution processed methods. The report is based on the processing temperature, and the different post-deposition treatments that have been employed for solution processed methods. The mobility of the fabricated TFT devices are reported in the chart, and the channel materials are presented in parenthesis. Data were compiled from ref. [7, 38, 46, 68, 83, 121, 124, 127].

Based on the review, Fig. 1.6 summarizes the recent results on the post-deposition treatments of metal oxide TFTs by solution methods. It can be deduced that conventional thermal treatment yielded a high device performance with mobility above 80 cm^2/Vs at high processing temperature. Although, this may not be suitable option when considering its application in flexible electronics. However, for the UV treatments like DUV, laser, Ozone treatment, it is possible to produce quality device at low processing temperature below 200 °C. So far, the UV treatment method has not been applied for TFTs fabricated by spray pyrolysis.

1.4.3 TFTs based on ZrO_x gate dielectric fabricated by solution processed methods

ZrO_x gate dielectrics have been employed in TFT fabricated by solution processed methods. According to the ten years survey (presented in Fig. 1.7), it shows that ZrO_x thin films fabricated by spin coating have mainly been tested in TFT. Although there are some reports on dip coating, spray pyrolysis and Ink jet printing methods, but these methods are yet to gain popularity in TFT fabrication.

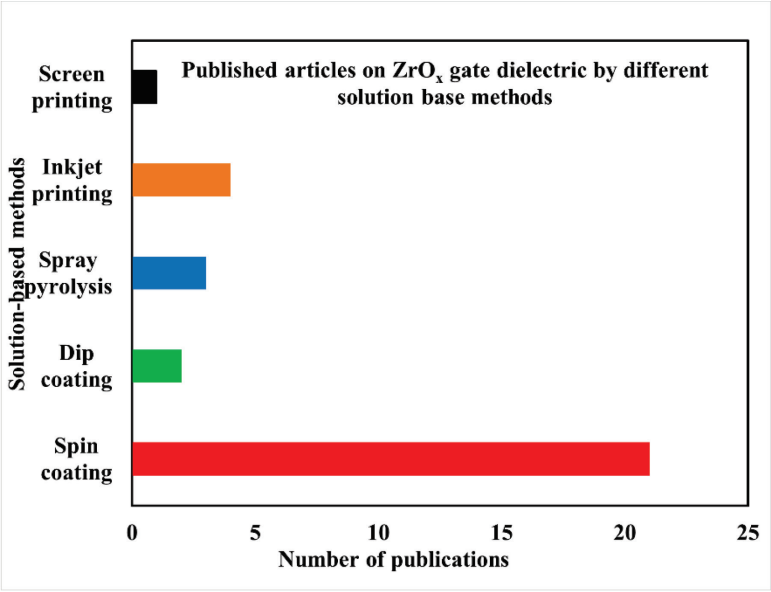

Figure 1.7. Number of published papers on MO-TFTs based on ZrO_x gate dielectric by different solution processed methods in the past ten years. (Data were acquired according to ISI web of knowledge).

Table 1 (presented in appendix 2) offers an overview of the most common results on solution processed MO TFTs with ZrO_x dielectric layer. In the case of spin coating, both amorphous and crystalline ZrO_x dielectric have been tested in TFTs [25, 128, 129], and post-deposition thermal treatment (usually between 300 to 500 ^oC) was used to tune properties of the film. The amorphous ZrO_x thin film has been reported to give better performance than the crystalline ZrO_x deposited by spin coating [118]. This is because the surface of amorphous thin film is smooth and improves the quality of the interface between layers [118, 130]. Furthermore, most of the reports on MO TFTs based on ZrO_x gate dielectric by spin coating methods have been fabricated on Si-substrates [118], and a fully amorphous oxide TFTs have only been fabricated with TFTs based on NiO_x, and In_2O_3 based channel layers [72, 118]. In the work of Zhu et al., the high capacitance of the ZrO_x gate dielectric was claimed to have enhanced the carrier mobility by reducing the activation energy of carrier during transition [118].

Reports on ZrO_x gate dielectric by inkjet printing, have mostly been fabricated on glass substrates because ZrO_x grows uniformly on them; however, there is a possibility of pinhole formation or poor substrate coverage when they are fabricated on flexible substrates [131]. The processing temperature was about 350 ^oC, because annealing process is still required to dry and decompose precursor inks [83]. Li et al. reported that it was difficult to deposit amorphous MO TFT with top-gate configuration because the

gate dielectric was susceptible to acidic environment [83]. Based on Zeumault's report, there is an inherent difficulty in fabricating ZrO_x gate dielectric by inkjet printing method [106].

In the case of spray pyrolysis, the potential feasibility of ZrO_x gate dielectric was demonstrated in ZnO based TFTs [7], and crystalline ZrO_x dielectric films have mostly been reported [118, 132]. The reports showed that ZrO_x dielectric TFTs can be fabricated on Silicon [133] or glass [91] substrates. The crystalline ZrO_x gate dielectric has been reported to demonstrate high mobility above 80 $cm^2V^{-1}s^{-1}$ [7]. In the work of Adamopoulos [7] Li metallic dopant was used to improve the stability of the ZnO channel layer, and the carrier mobility was enhanced due to increased crystallite size of the Li-ZnO channel. Also, the processing temperature reported was about 400 ^oC with layer thickness of 100 nm, except for one study that reported on spray combustion synthesis (SCS) of ZrO_x gate dielectric at 300 ^oC [52, 68]. Owing to the work of Adamopoulos [7] and Wang's [68] significant thickness above 100 nm is needed for spray deposited gate dielectric layer in order to completely insulate the channel layer from the gate electrode. Though Wang was able to reduce the thickness (ca 25 nm) of the ZrO_x gate dielectric by introducing facile aqueous synthesis route, but the process temperature was still ~300 ^oC and the corresponding carrier mobility was ~5 $cm^2V^{-1}s^{-1}$.

However, based on the review, solution processed TFTs based on ZrO_x dielectric has not been produced at low temperature by spray pyrolysis. The crystalline ZrO_x gate dielectric layer has mostly been reported for sprayed MO TFT; although the crystalline structure is undesired because the presence of grain boundary within the film could act as leakage site for electric current. Therefore, future research should focus on the deposition of amorphous ZrO_x dielectric film at the low temperature.

1.5 Summary of literature review and aim of the study

Based to the literature survey, different classes of materials have been used in the fabrication of TFTs. But the metal oxide (MO) materials have attracted the most research interest, thanks to the development of single or multicomponent channel materials. However, the gate dielectric layer needs more improvement in order to reduce the problem associated with scaling down of TFT devices.

In light of this, high-κ MO dielectrics have attracted a lot of research interest, although selecting a suitable high-κ MO is very challenging since the E_g and κ of MOs are inversely proportional. Several studies have shown that the properties MO TFT can be improved by doping two or more high-κ MOs, or by employing a multi-layer gate dielectric. Some studies have considered amorphous MOs suitable in improving the performance of TFTs. Some studies have shown that amorphous HfO_2 dielectric film developed by ALD with ~54 nm thickness exhibited a high dielectric field strength, but the cost of this technology is not suitable for industrial scalability. Other high-κ MOs like, Al_2O_3, and ZrO_2 are still a good option to be exploited, and they can easily be processed by cost-effective solution processed methods.

Moreover, several solution processed methods have been studied for the fabrication of high-κ MO gate dielectric in TFT, but the potential of spray pyrolysis such as wide area uniformity, high degree of freedom, scalability, and cost-effectiveness has not been fully acclaimed in TFT fabrication. Although this method is limited to high processing temperature, but more improvements can be done on this area in future research. Conventional thermal annealing has vastly been used to improve the properties of sprayed high-κ MOs gate dielectrics, yet the processing temperature is still high (above

350 ^{o}C) to be considered in flexible electronic fabrication. Studies have shown that post-deposition treatments like UV-Ozone (UVO) treatments can help to reduce the thermal budget of solution processed high-κ MOs, and this has been reported for solution processed methods like spin coating, and Inkjet print. However, this concept of UVO treatment has not been reported for sprayed high-κ MO gate dielectric.

The few studies on spray fabricated TFTs based ZrO_x gate dielectric have focused mainly on the growth mechanism such as the influence on high processing temperature (~300 ^{o}C), and the substrate system (glass or silicon) on which the layers were fabricated. However, there exist a knowledge gap on the fabrication of TFTs by spray pyrolysis at low processing temperature. Not until now, amorphous ZrO_x thin film processed at 200 ^{o}C by spray pyrolysis has also not been incorporation in TFT. Novelty of this work is the introduction of UVO post-deposition treatment, allowing the possibility to lower the processing temperature of ZrO_x gate dielectric films down to 200 ^{o}C. This has not been achieved before and will extend the application of spray to a low-cost flexible electronic application.

Based on the literature overview, this thesis seeks to employ chemical spray pyrolysis method in the development of amorphous metal oxide thin film at low processing temperature; which will be suitable for the gate dielectric layer of low-power flexible TFT devices. This will expand the application of spray pyrolysis to large area electronic fabrication. Therefore, the following objectives are specified:

1. To develop Zr-doped TiO_2 (Zr-TiO_2) thin film and to investigate the influence of varying Zr dopant impurity in the precursor solution on the morphology, microstructure, and electrical properties of the deposited Zr-TiO_2 thin film by chemical spray pyrolysis.
2. To develop and optimize the deposition of amorphous zirconium oxide thin film by chemical spray pyrolysis and to systematically study the effect post-deposition thermal and UV-Ozone treatments on the structure, surface, and the electrical properties of the film.
3. To fabricate a fully amorphous metal oxide TFT based on zirconium oxide gate dielectric layer using a completely solution processed methods.
4. To evaluate the performance of a low temperature processed ZrO_x gate dielectric in TFT.

2 Experimental method

In this section, the experimental procedure undertaken during this work is presented, nevertheless a detailed report about the step by step process of the spray pyrolysis deposition, thin film characterization, metal insulator semiconductor (MIS) capacitor, and TFT device fabrication has been reported in the publications listed in Appendix 1 as [paper **I, II, III, IV**]. This work is based on deposition of gate dielectric thin film and the fabrication of TFT by spray pyrolysis. However, characterization techniques (such as morphology, optical spectroscopy, structural analysis, and chemical composition) and device fabrication technique like electrode/contact deposition are essentially needed.

2.1 Deposition of metal oxide thin film by chemical spray pyrolysis

The numerous benefits of spray over other solution processed deposition techniques have the previously discussed in section 1.4.1 especially the fact that doping can easily be done through this method. Here in this thesis, the deposition of Zr-doped TiO_2 (Zr-TiO_2) and ZrO_x thin film will be briefly described.

2.1.1 Zirconium doped titanium dioxide thin film deposition

The zirconium doped titanium dioxide (Zr-TiO_2) precursor solution was synthesized using titanium (IV) isopropoxide (TTIP) and zirconium acetylacetonate reagents (98% MERCK and 98% ALDRICH, respectively) without prior purification because all reagents are analytical graded. The detailed description about the preparation of both TiO_2 and Zr-TiO_2 precursor solutions have been published in paper [**I**]. The substrates (c-Si and quartz) were placed in a tin bath kept at 450 ^oC and the precursor was sprayed at 2.5 ml/min of spraying rate, while the carrier gas flow rate was at 8l/min. The nozzle-substrate distance was maintained at 27 cm and the precursor solution was sprayed for five cycles each consisting of 60 s of spraying plus 60 s of pause. All the samples were prepared under similar condition and the post-deposition thermal treatment (500 – 1000 ^oC) was carried out in air for one hour. For proper identification, the samples under test was labelled 'undoped TiO_2' and '*x*-Zr–TiO_2' for the undoped and doped TiO_2 thin films, respectively, where *x* corresponds to the concentration (0 – 40 mol %) of Zr in the sprayed solution.

2.1.2 Zirconium oxide thin film deposition

An analytical graded zirconium acetylcatonate ($Zr(acac)_4$) reagent (98%, ALDRICH) was used in the preparation of ZrO_x precursor solution. The reagent was used without prior purification. After the preparation of precursor solution, the ZrO_x thin film was deposited using an ultrasonic spray pyrolysis set-up (schematic shown in Fig. 2.1) onto a heated quartz and c-Si substrates at different temperatures (T_{dep} = 200, 300, 400, 500 ^oC). The details about the deposition of ZrO_x thin film has been extensively described in [Article **II, III, and IV**], but the technological scheme in respect to deposition temperature (T_{dep}), concentration (c), and spray rate is summarized in Table 2.1 below.

Table 2.1. Technological parameters for the deposition of ZrO_x thin film

Sample	T_{dep}, ^oC	precursor	Spray Volume	c, mol/l	Deposition time (min)
ZrO_x	200	$Zr(acac)_4$	25	0.25, 0.05	21
ZrO_x	300	$Zr(acac)_4$	25	0.25, 0.05	21
ZrO_x	400	$Zr(acac)_4$	25	0.25, 0.05	21
ZrO_x	500	$Zr(acac)_4$	25	0.25, 0.05	21

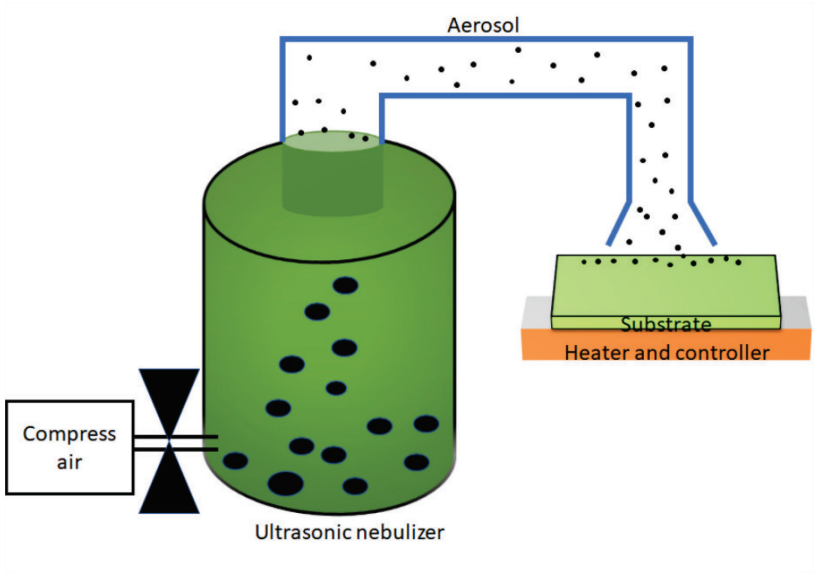

Figure 2.1. A typical image of ultrasonic spray pyrolysis set-up (home-made).

2.2 Metal oxide thin film post-deposition treatment

As discussed in the literature review, the possibility of depositing quality metal oxide thin film by solution process at low temperature is very challenging. This problem also persists in the spray pyrolysis method. Thus, explains why films are mostly deposited above 400 ^{o}C. Here we will describe two post-deposition treatments we employed in this research work.

2.2.1 Thermal post-deposition treatment

This process usually involves heating metal oxide thin film at a suitable temperature above the decomposition or deposition temperature to alter the physical or chemical properties of the film. It can be done at different atmospheres, but in this thesis MO films were treated in a furnace (Nabertherm L5/11/06D) at a temperature range from 500 to 800 ^{o}C in steps of 100 for 60 minutes.

2.2.2 UV-Ozone post-deposition treatment

This is a photo chemical process used to clean or modify the surface of metal oxide thin film, through the production of reactive oxygen radical. The mechanism of this treatment method has been succinctly described in paper **IV** and in section 1.4.2. Immediately after the deposition process, samples were transfer into Petri-dish to avoid environmental contamination. The UV system (NOVASCAN PSD-series, from Novascan Tech Inc., Boone, NC, USA) has a mercury vapor lamp, whose main irradiation peaks are generated at 184.9 nm and 253.7 nm as its light source.

2.3 Characterization of metal oxide thin film

The Zr-TiO_2 and ZrO_x thin films were characterized by various analytical methods available at Tallinn University of Technology (TalTech), while the fabricated TFT devices were characterized by the semiconductor analyzer available at the Centre for Material Research (CENIMAT) Lisbon Portugal. An explicit description of each analytical techniques can be found at the experimental section of the publish papers [**I – IV**], but their summary is presented in Table 2.2 below.

Table 2.2. Analytical techniques used for the characterization of the deposited Zr-TiO_2 and ZrO_x dielectric thin films and the fabricated MO TFTs.

Properties	Characterization methods	Apparatus	Ref.
Surface morphology; film thickness	SEM	Zeiss EVO-MA15, Zeiss HR FESEM Ultra 55	[**I, II, IV**]
Elemental composition	EDX	Zeiss EVO-MA15, Zeiss HR FESEM Ultra 55	[**I, II**]
Surface roughness	AFM	NT-MDT Solver 47 Pro	[**II, III, IV**]
Phase composition; crystallite orientation; crystallite size	XRD	Rigaku Ultima IV	[**I, II, III**]
Phase composition	Raman	Horiba's LabRam HR800	[**I, II**]
Optical transmittance, Reflectance, bandgap,	UV-VIS spectroscopy	Jasco V-670	[**I, II and IV**]
Wettability	H_2O Contact angle measurement	DSA 25 (KRUSS Instrument)	[**III**]
Chemical composition	XPS	Kratos Analytical Axis Ultra DLD	[**III**]
I-V, Nyquist, Capacitance, Dielectric constant	Impedance spectroscopy	Autolab Spec.	[**I, II, III, IV**]
TFT parameters	Output, and transfer	semiconductor parameter analyzer (Agilent 4155C)	[**III, IV**]

2.4 Device fabrication

2.4.1 Metal-insulator semiconductor device

To access the electrical properties of the as-deposited thin films, MIS capacitor was produced on Si-substrate. The dielectric thin film under study was deposited on p-type Si substrate (Siegert wafer) with resistivity between 3 – 10 ohm.cm, followed by thermal evaporation of contact electrode using a Quorum K975X vacuum evaporator on top of the thin film surface (either Zr-TiO_2 or ZrO_x). To quantify the working area of the electrode, a shadow mask with area of 1.7 mm^2 was employed for patterning.

2.4.2 Thin film transistor device

Fully solution processed TFT was fabricated with a bottom-gate architecture (see Fig. 1.1 c, in section 1.1). According to the image shown in Fig. 2.2, the fabrication is a three step processes: (1) the gate dielectric layer was deposited by spray onto a clean p-type Si wafer, (2) the channel layer was later deposited onto the surface of the dielectric layer, (3) the source and drain aluminum electrode was deposited onto the surface of the channel via a shadow mask. To improve the interface between the deposited layer the device was soft baked at 120 °C. The details about deposition of each layers and device characterization has been explained in publication [**III, IV**].

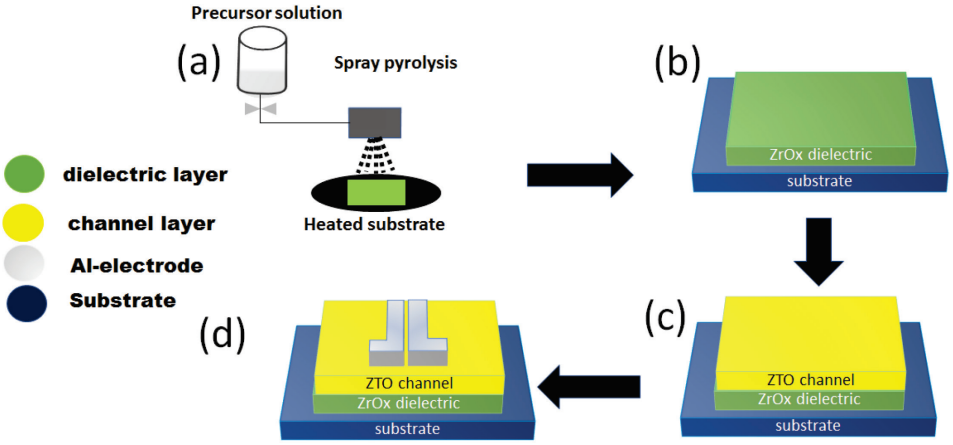

Figure 2.2 Schematic showing the whole fabrication stages from bottom up: (a) spraying of ZrO_x precursor solution, (b) deposited of ZrO_x dielectric layer onto Si-substrate, (c) spin coating ZTO channel layer onto ZrO_x/Si, and (d) aluminium S/D electrodes. The ratio between channel width (W) and channel length (L) is W/L = 14.

3 Results and discussions

This section encompasses the results and the discussions of the various investigations on the deposition and characterizations of two different high-κ metals oxides (Zr-TiO_2 and ZrO_x) by chemical spray pyrolysis (CSP). These results have been published in papers **[I**, **II**, **III** and **IV]**.

3.1 Development of Zr-doped TiO_2 thin film by chemical spray pyrolysis

In this study, Zr-doped TiO_2 (Zr-TiO_2) thin film was developed using CSP method, this is unique in this thesis as the deposition of Zr-TiO_2 by CSP is reported for the first time in this thesis. The changes in the Zr-TiO_2 thin film properties was investigated by varying the Zr/Ti stoichiometric mole ratio in the precursor solution. The films were deposited at 450 ^oC on quartz and n-Si substrate, other details about the experimental methods have been succinctly explained in paper [**I]** in appendix 1.

3.1.1 Influence of Zr dopant impurity on the structural properties of TiO_2 thin film

The changes in the phase composition of TiO_2 thin film as a function of Zr dopant impurity in the solution was investigated in order to screen the amount of Zr dopant that will be suitable for the deposition of quality amorphous Zr-TiO_2 thin films. Phase composition was obtained by XRD for both the undoped TiO_2 and Zr-TiO_2 films and their diffraction pattern is presented in Fig 3.1.

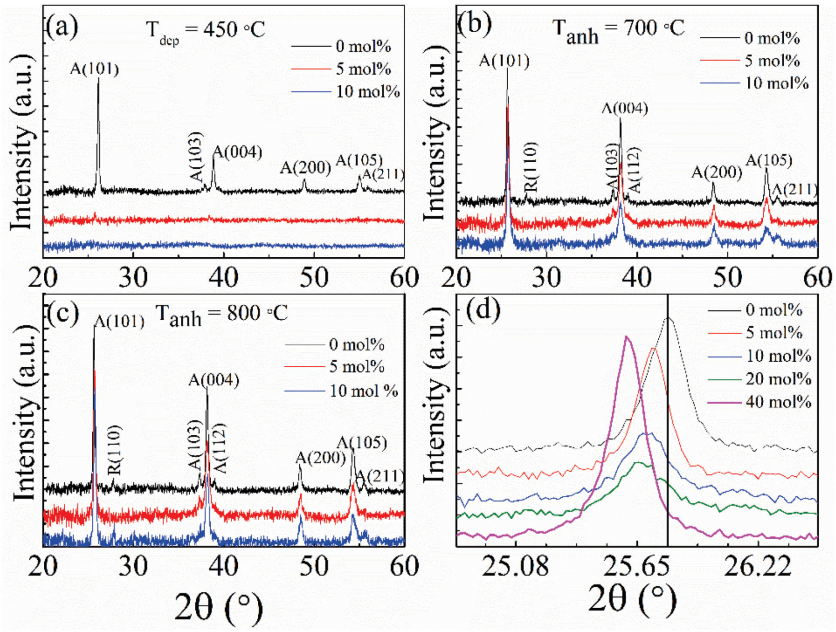

Figure 3.1. Measured XRD patterns for undoped and Zr-doped TiO_2 thin films with varied Zr amount in sprayed solution: (a) as-deposited films at 450 °C, (b) annealed films at 700 °C, and (c) annealed films at 800 °C. The shift in the anatase (101) main diffraction peak position as a function of the Zr/Ti mole ratio in the spray solution is presented in (d) after annealing at 500 °C. (All the films were deposited on a quartz substrate.)

As seen in Fig. 3.1 (a), the XRD pattern of the as-deposited undoped TiO_2 thin film exhibits a sharp crystalline peak, which belongs to the anatase (101) phase of TiO_2 (PDF powder diffraction-01-075-1573). On the contrary, the XRD pattern of the as-deposited 5-Zr–TiO_2 thin film shows a weak peak at 2θ = 25.40°, while the (10, 40)-Zr–TiO_2 thin films have no peak. This indicated that the (10, 40)-Zr–TiO_2 thin films are amorphous because the increase in the amount of Zr in the TiO_2 matrix causes an inhibitory effect in the crystallization of TiO_2 thin film. However, after annealing at 500 °C, the XRD pattern of (5, 40)-Zr–TiO_2 thin films show the diffraction peaks of TiO_2 anatase phase, which was sustained in the film even after annealing at 700 °C (Fig. 3.2 b). The delay in the formation of anatase phase in the (5, 40)-Zr–TiO_2 films was obviously due to the incorporation of Zr into the TiO_2 matrix. A mixture of both rutile (at 2θ = 27.43°) and anatase (at 2θ = 25.40°) phases appear in the undoped TiO_2 film (PDF powder diffraction-01-0714808) after 800 °C (Fig. 3.2 c), while the anatase phase remained in the Zr-doped TiO_2 films.

Figure 3.2 (d) demonstrates the enlargement of the anatase (101) diffraction peak at 2θ = 25.40° for both the undoped and the Zr-doped TiO_2 thin films annealed at 500 °C. It can be clearly seen that the position of the anatase (101) diffraction peak shifted to lower angle (2θ) of diffraction from 25.79° to 25.60° by increasing Zr amount in the precursor solution from 0 to 40 mol %. Considering the fact that the ionic radius of Zr^{4+} (0.072 nm) is larger than that of Ti^{4+} (0.061 nm), it is expected that this would cause an increase in the unit cell parameters, and result to a decrease in 2θ angle, following the explanation of the Bragg's law [134]. This observation confirms that Zr^{4+} was incorporated into the lattice of TiO_2; and thus, doping the Ti^{4+} in the film matrix substitutionally. It is worth mentioning that the Raman studies for all the films were also carried out and their results concur with the XRD results (presented in Fig. 4 in paper [**I**]).

According to the XRD studies, it can be inferred Zr doping promotes amorphization by delaying crystallization of TiO_2 thin film, and about 10 mol % of Zr is enough to completely dope TiO_2 film.

3.1.2 Influence of Zr dopant impurity on the optical properties of TiO_2 thin film

The optical properties of the deposited TiO_2 thin film was acquired in the visible region by measuring the total transmittance which is presented in Fig. 3.2. All the as-deposited films are optically active with optical transparency above 50% in the spectral region from 400 to 800 nm. The transparency of the film increases as the amount of Zr in the precursor solution was increased, while interference pattern on the spectra reduces with increase in the concentration of Zr in the solution. The optical absorption edge of the film exhibited a left shift with increase in the concentration of Zr in the precursor solution. The optical direct bandgap energy of the deposited films was calculated by applying the expression (3.1) on a Tauc plot [135, 136].

$$\alpha h\nu = A\,(h\nu - E_g)^n \qquad (3.1)$$

The description of each component of the equation and how the interference on the total transmittance spectra was eliminated is explained in Appendix 1, paper [**I**]. The extracted optical bandgaps are plot in Fig 6b in paper [**I**], where it was observed that the optical bandgap for the as-deposited undoped TiO_2 film and 40-Zr-TiO_2 film amounted to 3.12 and 3.45 eV, respectively. The increase in the optical bandgap with Zr doping could be the effect of Zr incorporation in the TiO_2 film matrix. Gao et al. [134] reported that electronic band changes in TiO_2 can only occur when large amount Zr is incorporated into the bulk of the TiO_2 thin film matrix, which depends on the solubility limit of Zr^{4+} in the precursor solution.

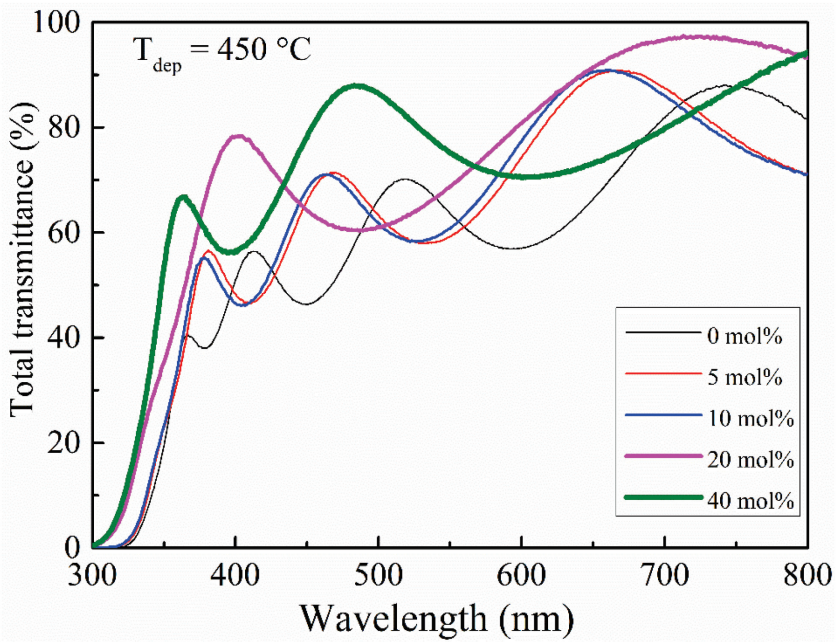

Figure 3.2. Total transmittance spectra of the as-deposited TiO_2 films at different amount Zr in the spray solution. (Films were deposited on a quartz substrate at 450 °C)

Based on the optical studies, the optical bandgap increases due to the incorporation of Zr into the TiO_2 lattice. This effect causes an upward shift in the conduction band of the Zr-TiO_2 film; thus, leading to an increase in the optical band gap from 3.12 eV (in undoped TiO_2) to 3.45 eV (in 40-Zr-TiO_2).

3.1.3 Influence of Zr dopant impurity on the electrical properties of TiO_2 thin film

The electrical properties for both the undoped and doped Zr-TiO_2 thin film was accessed by fabricating a simple MIS capacitor, and the dielectric response was acquired through impedance spectroscopy, the details have been described in paper [**I**].

The forward bias leakage current density in the fabricated Si/Zr–TiO_2/Au MIS structure for both undoped TiO_2 and (20, 40)-Zr–TiO_2 films is presented in Fig. 3.3. It was observed that the leakage current density at 1 V amounted to 1.7×10^{-3} A/cm^2, and 4.5×10^{-5} A/cm^2 in the undoped TiO_2, and 40-Zr-TiO_2 thin films, respectively. The reduction in the leakage current was by two orders of magnitude, which was as a result of the Zr-doped film losing its conductivity at the forward bias regime. However, as reported in paper [I], there was no significant changes the reverse saturation current I_o density for both the undoped TiO_2, and (20-40)-Zr–TiO_2 films, but the value of Schottky barrier ($\emptyset_B$) (presented in paper [I]) increases slightly from 0.536 eV in the undoped TiO_2 film to 0.571 eV in the Zr-doped TiO_2 films. According to the literature, the Schottky barrier heights between 0.4 and 1.0 eV have been reported for similar structures of TiO_2 thin film deposited by other fabrication methods such as dip-coating, spray pyrolysis, sputtering, and plasma enhanced physical vapor deposition. The dielectric relaxation response for the Zr-doped TiO_2 films (present in Fig. 8, paper [**I**]) shows that the oxide–electrode interface dipole influences the dielectric properties of the fabricated Si/Zr–TiO_2/Au MIS structure [137].

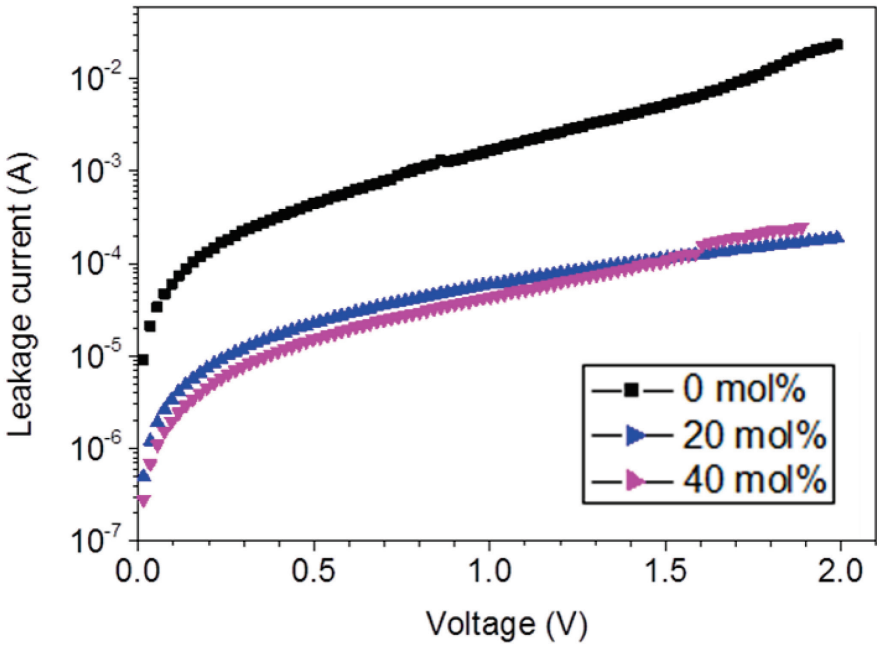

Figure 3.3. The current – voltage characteristics of Si/x-Zr-TiO_2/Au MIS device with Zr-TiO_2 films. Where x is 20, 30 mol % concentration of Zr in the precursor solution.

Based on this section, amorphous Zr-TiO_2 films can be deposited by spray at 450 °C, and the incorporation of Zr in TiO_2 film matrix was established to have caused delay in the crystallization of TiO_2 in the film matrix. This was supported by a slight increase in the optical bandgap in the Zr-TiO_2 film, and reduction in the leakage current by 2 order of magnitude from 1.7×10^{-3} to 4.5×10^{-5} A/cm^2 by increasing the concentration Zr in the precursor solution from 0 to 40 mol %. However, due to narrow bandgap, the deposited Zr-TiO_2 film was not tested in TFT.

3.2 Development of ZrO_x thin film by chemical spray pyrolysis

In this study, we aimed to develop and optimize the process of depositing high-κ ZrO_x thin film that will be suitable for the gate dielectric layer in TFT by CSP method. The effect of deposition temperature (T_{dep} =200, 300, 400, 500 °C) and post-deposition thermal treatment (T_{anh}=500, 800 °C) was studied on the optical, microstructural and electrical properties of the film. The films were deposited on p-Si and quartz substrate. The details of the experiments and the obtained results have been published in paper [**II, III**], appendix 1.

3.2.1 Morphology of sprayed ZrO_x thin film

To develop a high-performance gate dielectric, the film morphology plays a crucial role, therefore it is important to investigate the changes ZrO_x film morphology as a function of deposition temperature. Results of the AFM and SEM analysis are presented in Fig. 3.4.

The surface morphology of the ZrO_x thin films deposited at different temperatures was obtained via atomic force microscope (AFM, Fig. 3.4 a, and c) and SEM analysis (Fig. 3.4 b and d). The films surface roughness was estimated from the AFM height profile

and scanned through an area of 1 µm × 1 µm. The ZrO_x films deposited at 200 °C (Fig. 3.4 a) demonstrated a higher surface roughness with a root mean square (RMS) roughness value of 0.33 nm compared with that deposited at 400 °C with an RMS value of 0.29 nm. The decrease in the film surface roughness at higher temperature could be due to film densification, which was aided by the decomposition of volatile organic precursor during the spray pyrolysis process. In addition, as depicted by the SEM images (Fig. 3.4 b and d), the ZrO_x dielectric thin films were uniform, compact, and very smooth. The ZrO_x thin film was thermally stable as there was no pronounce changes in the film's morphology at high deposition temperature. As reported in paper [II] that even after post-deposition thermal treatment, the ZrO_x film's smoothness and compactness was retained and there were no visible cracks on the surface of the film (see Fig. 1(c) and (d), paper [**II**]). Examining the changes in film's thickness for the ZrO_x samples deposited 300 and 500 °C after annealing at 800 °C, there was a reduction in thickness (65 to 51 nm, and 165 to 75 nm, respectively), which could be attributed to densification of film at high annealing temperature.

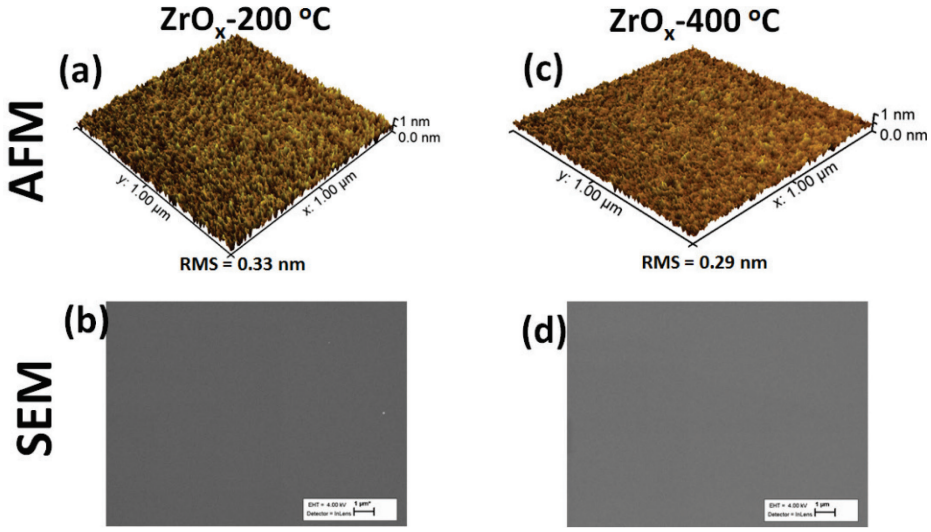

Figure 3.4. Surface morphology of sprayed ZrO_x thin films. AFM deflection images of the as-deposited ZrO_x thin film at both (a) 200 °C, and (c) 400 °C; and their corresponding SEM images at (b) 200 °C and (d) 400 °C. The film was deposited on p-type-Si-substrate.

Based on the SEM and AFM analysis, uniform ZrO_x film was deposited by spray with no cracks and low surface roughness; which is a required property for a gate dielectric film.

3.2.2 Structural properties of sprayed ZrO_x thin film

The ZrO_x thin film microstructural analysis was obtained from the XRD and Raman analysis. The XRD pattern shown in Fig. 3.5 (a-d) indicated that the ZrO_x thin film deposited at 200, 300, and 400 °C are amorphous, while the film deposited at 500 °C is poorly crystalline exhibiting two broad diffraction peaks centred at $2\theta = 30.57^o$ and $2\theta = 35.42^o$. Due to the broadness of the peak centred at $2\theta = 30.57^o$ it was difficult to assign the particular ZrO_x phase the peak belongs to as both the tetragonal and cubic phases of ZrO_x are position within the broad peak. After post-deposited thermal

treatment at 800 °C, the peak became narrow and intense, and an additional peak centred at 2θ = 31.48° appeared, which belongs to the m-ZrO_x phase (PDF powder diffraction- 01-080-0966). The monoclinic ZrO_x phase formed at 800 °C could be the effect of crystallization of the ZrO_x thin film at high annealing temperature. Similar observations have been reported for ZrO_x thin films deposited by other solution processed method like spin coating [100, 138].

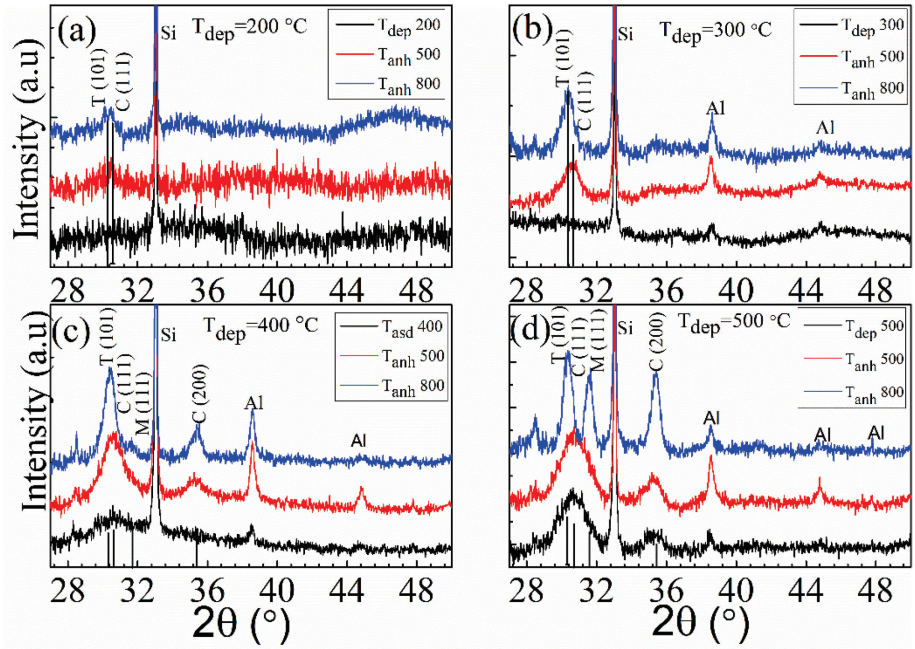

Figure 3.5. X-ray diffractograms of ZrO_x thin films as-deposited (T_{asd}) at (a) 200 °C, (b) 300 °C, (c) 400 °C, and (d) 500 °C; with varied thermal annealing (T_{anh}) at 500 and 800 °C. "T", "C", and "M" denote tetragonal, cubic, and monoclinic phases of ZrO_2 respectively.

The results of the Raman analysis [presented in paper **II** as Fig. 5] for the ZrO_x thin films deposited at 500 °C demonstrated three identifiable peaks: First at ~139 cm^{-1}, which belongs to t-ZrO_2 B_{1g} vibration mode, while the other two peaks located at ~304 cm^{-1} and ~438 cm^{-1} are not related with the deposited thin film rather they are Raman signals from the silicon substrate [139 – 141]. However, after post-deposition thermal treatment at 800 °C, a mixture of both tetragonal and monoclinic phases of ZrO_x was formed, which is in good support with the XRD result.

According to the structural studies, amorphous ZrO_x thin film can be deposited below 500 °C by spray pyrolysis. However, after annealing at 800 °C the ZrO_x film became polycrystalline with a mixture of ZrO_x phases formed.

3.2.3 Electrical properties of sprayed ZrO_x thin film

The electrical properties of the spray deposited amorphous ZrO_x thin films (200, 400 °C) was accessed by fabricating MIS-capacitor with a structure of Al/ZrO_x/n-Si. All the device was characterized at room temperature in dark box.

The leakage current density in the forward and reverse regime for the MIS-capacitor produced from ZrO_x thin films at 200, and 400 °C is presented in Fig. 3.6. From the plot, the leakage behavior of the ZrO_x thin films was estimated from in the reverse bias regime

at 1 V. It was observed that the ZrO_x deposited at 400 °C has a lower leakage current of 3.56×10^{-6} A/cm^2 that is lower than the one measured for the 200 °C deposited dielectric film (4.26×10^{-4} A/cm^2). This result demonstrated a reduced leakage current density by 3 order of magnitude with increase in deposition temperature. This can be attributed to the decomposition of volatile organic compounds in the film at higher temperature, resulting in the improvement of the density of the dielectric films [142, 143].

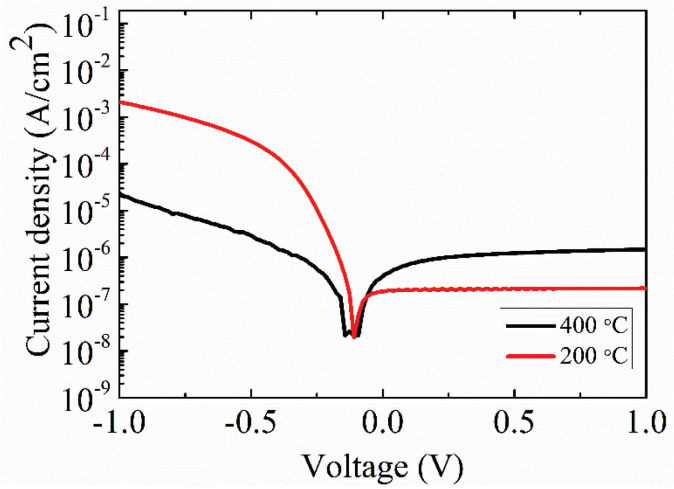

Figure 3.6. Current–voltage characteristics of Al/p-type Si/ZrO_x/Al MIS capacitors with the ZrO_x films obtained at various deposition temperatures.

According to the capacitance dispersion curve, presented in [Fig.5a, paper **III**] it was found that area capacitance at 100 kHz for the ZrO_x dielectric film deposited 200 °C and 400 °C is 0.37, 0.67 µF/cm^2, corresponding to a permittivity of 8.4 and 22.7, respectively. The observed increase in the permittivity value of the 400 °C deposited film can be due to the densification of the film at a higher temperature. An important point is that the observed increase in the dispersion curve for ZrO_x deposited at 200 °C as the frequency decreases may be an indication that there is another dielectric relaxation mechanism at lower frequencies related with mobile ionic species as a result of the incomplete decomposition of the ZrO_x precursors at a low temperature [paper **III**].

The capacitance–voltage (C-V) curves presented in (Fig 5c, paper [**III**]) for both the 200 °C and 400 °C deposited amorphous ZrO_x thin films. The voltage bias was carried in the forward and reverse sweep at 100 kHz, to ascertain the stability of the MIS capacitor. When the ZrO_x film was deposited at 400 °C, there was a saturation of the capacitance in the accumulation regime, which did not occur for that at 200 °C due to the leakage current (as confirmed in Fig. 3.6). Moreover, and contrary to that for the film deposited at 200 °C, there are no bumps when reaching accumulation, indicating a reduction in the density of electron trap sites at the interface between ZrO_x–silicon. Depending on the type of shift in the C–V curve, an understanding about the charge trapping/de-trapping within the oxide band structure can be obtained [144]. In this case, the device produced at 200 °C showed that a more negative bias was needed to complete accumulation due to electron trapping, corroborating the C–F results.

Based on this section, the electrical properties of the deposited amorphous ZrO_x thin film varies with deposition temperature. This work has demonstrated that 400 °C is a

suitable condition to deposit a uniform and amorphous ZrO_x thin film by CSP to achieve high electrical performance and low leakage. However, this processing condition is too high to be considered for flexible electronic.

3.3 UV-Ozone post-deposition treatment for lowering the process temperature of sprayed ZrO_x thin film

This section was aimed to lower the processing temperature of amorphous ZrO_x thin film by employing the UV-Ozone (UVO) post-deposition treatment. This concept is novel to this thesis work as it has not been applied for spray ZrO_x thin film before. Though, UVO irradiation can be applied in different fields, and it has been reported that ozone can be produced mainly at two different wavelengths: (1) at $\lambda < 243$, and (2) at $240 < \lambda < 320$ nm [127, 145]. The reaction mechanism about the generation of ozone from an atmospheric air is given as follows [**IV**]:

$$O_2\ (air) + (\lambda < 243\ nm\ \longrightarrow 2O^{\cdot}\ (free\ radicals)$$
$$O\ + O_2\ \longrightarrow O_3\ (Ozone)$$
$$O_3\ + (240\ nm < \lambda\ < 320\ nm\ \longrightarrow O_2 + O^{\cdot}$$
$$O\ + O_3\ \longrightarrow 2O_2$$

The ZrO_x film was deposited at 200 °C, and other details regarding the experiment and the obtained results have been published in paper [**IV**], appendix 1.

3.3.1 Influence of UV-Ozone post-deposition treatment on surface properties of ZrO_x thin film

The changes in the surface chemistry of the ZrO_x thin film at different UVO exposure time was monitored by performing the XPS and AFM analysis. The XPS analysis based on the deconvolution of O1s core spectra (presented in Fig. 3.7) was used to quantify the changes in chemical composition on the surface of the films at different UVO exposure time.

Figure 3.7a shows the XPS spectrum of the O 1s core level for the untreated ZrO_x thin film. The spectrum was fitted into four different peaks components centred at different binding energy (BE) 530.1, 531.3, 532.0, and 533.4 eV, which correspond to the metal oxygen (Me-O) bond, surface defects (V_o), metal-hydroxide (Me–OH) bond, and the adsorbed oxygen (O_{ads}) bond, respectively [146, 147]. Similarly, the XPS spectrum for the O 1s core level of the 60 min UVO treated ZrO_x thin film is presented in Fig. 3.7b and was fitted into different peaks components centred at 530.1, 531.3, 531.8 and 533.2 eV. The peak component located at 533.2 eV is assigned to adsorbed oxygen from moisture on the surface of the ZrO_x film [146, 148, 149]. The ratio between each of all the components peaks (MeO, Vo, −OH, H_2O_{ads}) was quantified by calculating the integrated areas of the O1s spectrum using Scofield´s cross-sections, and the obtained values are summarized in Table 3.1 for all the ZrO_x thin films treated at different UVO time (0, 30, 60, 120 min). The [Me-OH]/[Me-O] component ratios increases from 0.94 to 1.22 by increasing the UVO treatment time from 0 min to 120 min, while the [Vo]/[Me-O] ratio decreases from 0.65 to 0.38 by increasing the UVO treatment time from 0 min to 120 min. The reduction in the [Vo]/[Me-O] with UVO treatment indicated that the UVO makes the surface of the deposited ZrO_x film less defective. Similar behavior has been reported in [147, 150, 151] on metal oxide thin films deposited by other solution processed methods.

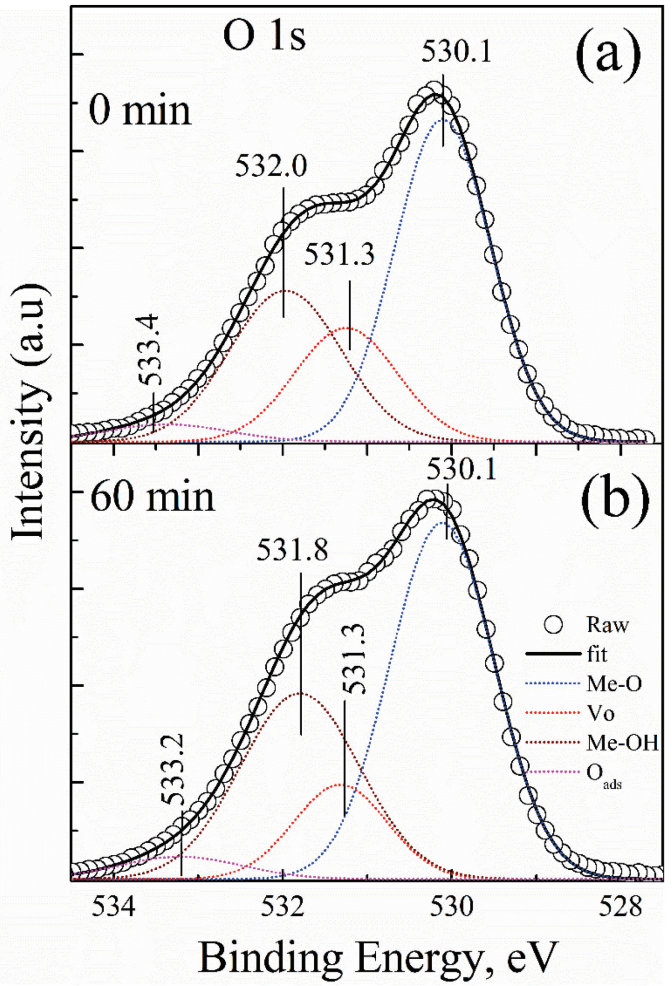

Figure 3.7. XPS spectra of O1s core level for (a) 0 minute, (b) 60 minutes of UVO treated ZrO_x thin film.

Table 3.1 Binding energy of O 1s peak components and their corresponding ratios at 0, 30, 60, and 120 minutes of UV-Ozone treatment

UV-Ozone treatment time (min)	Binding Energy (eV)				Component ratios	
	Me-O	Vo	Me-OH	OH_{ads}	[Vo]/[Me-O]	[Me-OH]/[Me-O]
0	530.1	531.3	532.0	533.4	0.65	0.94
30	530.1	531.3	532.0	533.3	0.59	1.04
60	530.1	531.3	531.8	533.2	0.41	1.10
120	530.1	531.4	532.8	533.2	0.38	1.22

According to the AFM results presented in paper **[IV]** as Fig.1, the surface of the ZrO_x films were uniform and of plain morphology. The RMS roughness value amounted to 0.63 nm, 0.51 nm, 0.32 nm, and 0.28 nm for ZrO_x films treated at 0, 30, 60, and 120 min, respectively. This indicated that the surface of the film is smooth, which can be attributed

to the removal of the organic residues by the oxygen radicals generated during the UVO treatment process [146].

Based on this study, the oxygen radical produced during UVO treatment eliminates the organic residues on the ZrO_x thin film surface, thereby effecting a change in the chemical properties of the ZrO_x film. Thus, the effect of UVO treatment is evidently seen by the reduction in the donor defects (Vo) and surface roughness of the ZrO_x film.

3.3.2 Influence of UV-Ozone post-deposition treatment on electrical properties of ZrO_x thin film

The electric properties of the ZrO_x thin film was accessed by producing a MIS-capacitor with structure Al/ZrO_x/p-Si after UVO treatment from 0 to 120 min.

Fig. 3.8(a) shows the leakage current density obtained from the accumulation regime in the MIS structure at 1 V, which is the same regime the TFT operates. It was observed that by increasing the UVO treatment time from 0 to 120 min the leakage current density was reduced by 3 order of magnitude. The ZrO_x thin film that was treated for 120 min exhibited the lowest leakage current of 1.0×10^{-8} A/cm^2 at 1 V with a breakdown voltage of 5 V, corresponding to a breakdown field of 2.5 MV/cm, which is above the minimal value considered as reasonable for a gate dielectric (1 MV/cm).

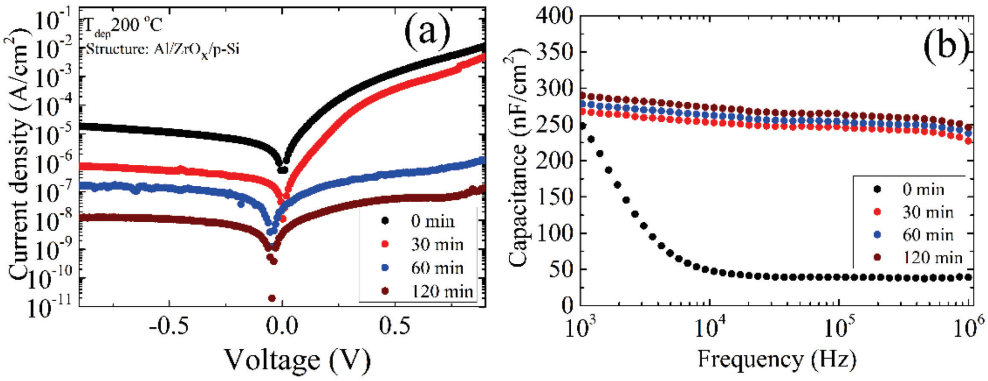

Figure 3.8. Electrical characterization of the metal insulator semiconductor (MIS) device made from ZrO_x thin film: (a) current–voltage curve under positive and negative biases; and (b) capacitance–frequency dispersion curve in the range between 1 kHz and 1 MHz at different UV–Ozone treatment times.

Figure 3.8(b) shows the capacitance dispersion curve for the ZrO_x thin film measured at different UVO treatment times. The untreated (0 min) ZrO_x thin film demonstrated a high capacitance at the low frequency region, which indicates the contribution of ionic polarization [152]. On the other hand, the capacitance of the UVO-treated ZrO_x thin films are stable in the high-frequency region. The area capacitance amounted to 268, 272, and 290 nF/cm^2 for the films treated at 30, 60, and 120 minutes, respectively.

The electrical result corroborates the XPS and AFM results discussed above. The UVO treatment ensures the effective removal of organic residues that can limit the formation more Zr-O bond network on the surface of the film. These residues could serve as trap site at the electrode interface and can cause poor electrical performance of the film, as seen in the untreated ZrO_x film exhibiting lower leakage current.

Based on this section, the UVO treatment is a good approach to fabricate device quality films at low processing temperature, most especially by solution processed method like CSP. The preliminary results show that the contributions of ionic polarization the interface of the fabricated MIS device was eliminated by UVO treatment.

3.4 Application of sprayed ZrO_x dielectric thin film in TFT

Herein, the application of sprayed ZrO_x gate dielectric in TFT was demonstrated in paper **[III]** and [**IV**], the fabricated devices was processed at 400 and 200 ^oC respectively. The TFT tested in paper [**III**] was fully solution processed and ZTO MO was employed as the channel layer. The details about the deposition of both the channel and dielectric layer was published in paper **III**, presented in appendix 1. On the other hand, we also incorporated the ZrO_x gate dielectric processed at low temperature (200 ^oC) into a sputtered IGZO channel TFT after UVO treatment, the result of this study has been published in paper [**IV**]. It is important to note that the thickness of the ZrO_x layer deposited at this stage of the experiment was about 20 to 30 nm and the deposited ZrO_x thin film was amorphous.

3.4.1 Electrical properties of fully solution processed ZTO-TFTs based on ZrO_x gate dielectric

In this study, a combination of CSP and spin coating was adopted in the fabrication of ZrO_x gate dielectrics and ZTO semiconductor, respectively, onto a rigid substrate and the obtained result from the solution processed TFTs made with similar ZTO channel layer was compared to the conventional SiO_2 dielectric. An all-amorphous oxide TFT with low operational voltage fabricated by CSP is reported in thesis for the first time.

Sprayed ZrO_x thin film was incorporated into ZTO based TFT as the dielectric layer in a bottom-gate architecture. We characterize the electrical performance of the device in the output and transfer regime (as shown in Fig. 3.9) in continuous mode with both back and forth sweeps. Since the device was measured in a quasi-static regime, it is important to note that the capacitance ($C = 1.0\ \mu F/cm^2$) of ZrO_x dielectric was calculated at 50 Hz to reduce the inaccuracy when extracting the mobility and sub-threshold slope (SS).

It can be seen from the output characterization curve presented in Fig. 3.9a that the device shows an excellent performance with clear distinction between the linear and saturation regimes, and no current crowding was observed. Fig. 3.9b shows the typical transfer characteristics of the ZTO/ZrO_x-TFT device, and the off-state (I_{off}) current increased with a decrease in the gate voltage. This observation is typical of most high-κ metal oxide derivatives, which has been reported to be caused by their relative narrow bandgap [153, 154].

We compared the performance of the ZTO/ZrO_x TFT with the ZTO/SiO_2 TFTs (details about the ZTO/SiO_2 TFTs was explained in paper **III, Fig. 7**) and it was observed that ZTO/ZrO_x TFTs demonstrated excellent performance with a significant reduction in its operation voltage window (between -1 V and 3 V), high saturation mobility of 4.6 $cm^2\ V^{-1}\ s^{-1}$, I_{on}/I_{off} ratio of 10^6, small SS value of 250 mV per decade, and a turn-on voltage of -0.9 V. The improvement in the transistor parameters is mainly due to the higher permittivity of the ZrO_x dielectric when compared with that of the SiO_2 dielectric. The ZrO_x-based TFT dissipated a much lower power (0.3 mW) than TFT based on the SiO_2 dielectric (30 mW).

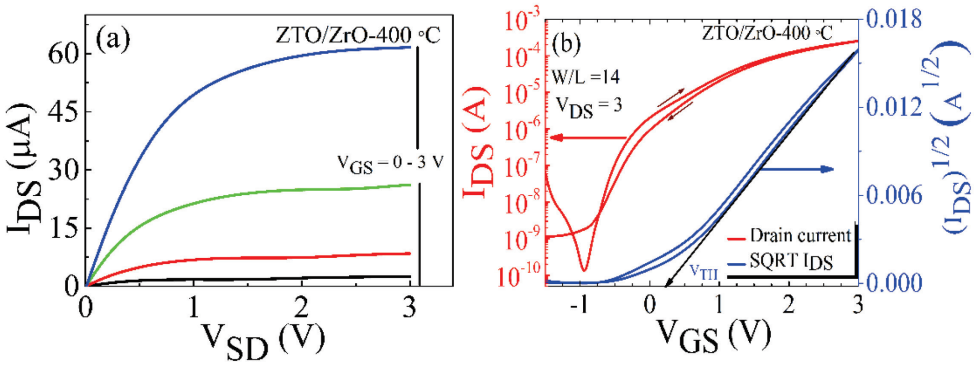

Figure 3.9. Measured (a) Output, and (b) transfer characteristics and the square-root of the trans-conductance of fully solution processed MO-TFT based on ZrO_x gate dielectric. The drain-source voltage (V_{DS}) was set at 3 V, and the channel aspect ratio (W/L) is 14.

The device operates in a depletion mode exhibiting a negative V_{TH} value with the clockwise hysteresis, which was estimated to be -0.1 V. This means that electron trapping occurred during forward sweeping and during the reverse gate voltage sweeping, these states remain filled until the trapped electrons were thermally de-trapped [142, 155]. The improved performance in the ZTO/ZrO_x-TFTs as opposed to the ZTO/SiO_2-TFTs could have originated from the thin and amorphous structure of the ZrO_x gate dielectric, providing a smooth interface between the ZrO_x dielectric and ZTO semiconductor layer.

Based on the obtained result, this thesis work have demonstrated that the use of a very simple technique, such as both CSP and spin coating for the sequential deposition of amorphous ZrO_x gate dielectrics layer and amorphous ZTO channel layer represents a significant step towards the development of low-cost, large-area oxide TFTs.

3.4.2 Electrical properties of IGZO-TFTs based on low temperature processed ZrO_x gate dielectric

In paper [**IV**], the integration of low temperature processed ZrO_x thin film in TFT after UVO treatment was investigated. As described in the experimental part of paper [**IV**], the UVO exposure time was varied, the maximum intensity of the UV-lamp is ~160 nm [reference therein: [144]]. The electrical performance of the fabricated TFT is shown in Fig. 3.10, and the extracted electrical parameters is presented in Table 3.2.

All the fabricated TFTs were working and show a clear gate dependence corresponding to n-type channel conductivity. The transfer characteristics measured in forward and backward sweeps for the TFT device produced from both the untreated and the UVO treated ZrO_x gate dielectric are shown in Fig 3.10 (a) and (b), respectively. The TFT device with the untreated ZrO_x gate dielectric demonstrated a poor performance with a negative V_{on} of about -2 V. However, the TFT device fabricated with UVO treated ZrO_x gate dielectric layer shows better electrical performance compared to the TFT device with untreated ZrO_x gate dielectric. The turn-on voltage (V_{on}) changes from – 0.3 V to 0.02 V when the UVO treatment time was increased from 30 to 120 min. This indicated that the surface potential of the ZrO_x gate dielectric films was changing with increase in the UVO treatment time; thus, affecting the electrical behavior of the device. In paper [IV], it was reported that the Schottky barrier at the ZrO/electrode interface changes with UVO treatment time.

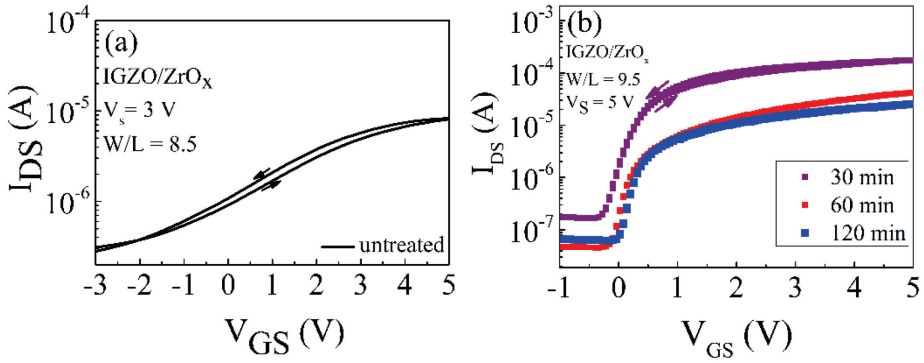

Figure 3.10. (a) Transfer characteristics of the TFT fabricated with untreated ZrO_x gate dielectric layer, and (b) the transfer characteristics of the TFT fabricated with treated ZrO_x gate dielectric at different UV–Ozone exposure times. Deposition temperature T_{dep} = 200 °C for the ZrO_x layer. The source voltage (V_S) was set at 5 V, and the channel aspect ratio (W/L) is 9.5.

The TFT parameters such as saturation mobility (μ_{sat}), on-off current ratio (I_{on}/I_{off}), threshold voltage (V_{TH}) and sub-threshold slope (SS) was extracted from the equation described in section 1.1.1 above and summarized in Table 3.2. The μ_{sat} amounted to 2.9 $cm^2 V^{-1}s^{-1}$, 7.0 $cm^2 V^{-1}s^{-1}$, and 8.4 $cm^2 V^{-1}s^{-1}$ for the TFT device made with UVO treated ZrO_x gate dielectric at 30, 60, and 120 min, respectively. While the I_{on}/I_{off} for the TFT device fabricated with UVO treated ZrO_x gate dielectric at 120 min was low, about 10^4. According to the reports by Dong et al. [127] on InO_x/ZrO_x TFTs fabricated by spin coating, improvement in the device performance was attributed high capacitance of the ZrO_x gate dielectric. Carlos et al. [144] show the use of powerful UV lamp to improve the gate leakage current of the IGZO/AlO_x TFT devices fabricated by spin coating.

Table 3.2. Summary of the extracted TFT parameters for an average of ten IGZO/ZrO_x devices at different UV-Ozone treatment time.

UV-Ozone treatment time (min)	V_{on} (V)	I_{on}/I_{off}	V_{th} (V)	SS ($V.dec^{-1}$)	μ_{sat}. ($cm^2 V^{-1} s^{-1}$)	I_{GS} at V_{GS} = 5 V (A)
0	- 2.0±1.0	~ 4.0×10^1	-	-	~ 0.02	~ 3.4×10^{-2}
30	-0.3±0.02	~ 1.0×10^3	-0.12±0.02	0.27±0.02	2.9±0.5	~ 7.4×10^{-5}
60	-0.12±0.1	~ 0.4×10^4	0.02±0.01	0.22±0.01	7.0±0.01	~ 2.3×10^{-5}
120	0.02±0.01	~ 1.0×10^4	0.01±0.005	0.21±0.01	8.4±0.01	~ 3.8×10^{-7}

To summarize this section on the integration of low temperature processed ZrO_x thin film as the gate dielectric layer in sputtered IGZO-TFTs. The fabricated TFT with treated ZrO_x thin film demonstrated better performance than the device produced with the untreated ZrO_x thin film. The improved performance can be attributed to the UVO post-deposition treatment of the CSP deposited ZrO_x thin film.

Conclusions

This thesis presents the strategies to develop amorphous MO thin films, which will be suitable for the gate dielectric layer of TFT by chemical spray pyrolysis (CSP). Two main novelties were achieved: (1) Zirconium doping was employed for the first time in this thesis to improve the properties of TiO_2 thin films deposited by CSP. (2) The concept of UV-Ozone (UVO) post-deposition treatment allows the possibility to lower the processing temperature of ZrO_x gate dielectric films down to 200 °C, thus extending the potential of CSP method to flexible or wearable electronic application. The main highlights from this work is summarised below:

1. A uniform and homogeneous Zr-TiO_2 film was deposited by spray. The XRD data reveals that as-deposited Zr-doped TiO_2 (Zr-TiO_2) thin films were amorphous and became crystalline with anatase crystal structure after thermal post-deposition treatment at 500 °C. A mixture of anatase and rutile phases were observed for the 10-Zr-TiO_2 thin film after thermal treatment at 800 °C. The optical bandgap of the as-deposited film was increased from 3.14 eV (undoped TiO_2) to 3.52 eV (40-Zr-TiO_2), the leakage current density in the as-deposited TiO_2 (1.7×10^{-3} A/cm^2) was reduced by two orders of magnitude in the as-deposited 40-Zr-TiO_2 thin film (4.5×10^{-5} A/cm^2).
2. Zirconium oxide thin film deposition was systemically optimized by CSP method at different deposition temperatures. As a result, from the SEM and AFM analysis, the as-deposited ZrO_x films demonstrated a uniform and smooth morphology, the RMS roughness value obtained from AFM was in the range 0.29 – 0.33 nm. The films were highly transparent above 80% in the visible region. The optical bandgap was increased from 5.21 eV to 5.68 eV with deposition temperature increasing from 200 °C to 500 °C. The films deposited below 500 °C were amorphous, while the films deposited at 500 °C were poorly crystalline. The leakage current density decreases by 2 order of magnitude from 4.3×10^{-4} A/cm^2 (200 °C deposited films) to 3.6×10^{-6} A/cm^2 (400 °C deposited films). The capacitance increases from 0.4 µF/cm^2 (in 200 °C deposited films) to 0.8 µF/cm^2 (400 °C deposited films).
3. Amorphous ZrO_x thin film was produced at 200 °C and the UVO post-deposition treatment was employed to improve the film quality. The XPS results confirm that UVO treatment effectively eliminates organic residue from the surface of ZrO_x thin film, which is evidently seen by a reduction in the ratio between the donor and metal-bonded oxygen components ([Vo]/[Me-O]) from 0.65 is in the untreated ZrO_x thin film to 0.38 in the UVO treated ZrO_x films. The UVO treated ZrO_x thin film attained desirable dielectric properties, such as a low leakage current density of 10^{-8} A/cm^2, a capacitance of 290 nF/cm^2 and relative permittivity of 6.6 (both at 1 kHz), which is acceptable for a gate dielectric.
4. A fully solution processed amorphous oxide TFT was fabricated by exploring both CSP and spin coating methods to deposit the dielectric (ZrO_x) and the channel (ZTO) layers respectively. Both layers were amorphous and processed at 400 °C and 350 °C, respectively. The fabricated ZTO/ZrO_x-TFTs exhibited high electrical performance with the magnitude of I_{on}/I_{off} current ratio of ~10^6, a low operation voltage of 3 V, high saturation mobility of 4.6 cm^{2}V^{-1}s^{-1}, a low threshold voltage of 0.03 V, a small sub-threshold swing of 0.25 V.dec^{-1}. Thus, confirming the applicability of CSP in low-cost, wide-area electronic fabrication.

5. As a proof of concept, amorphous ZrO_x thin film deposited at 200 ^oC was integrated as the gate dielectric layer in IGZO-TFT. The IGZO channel layer was sputtered and processed at 150 ^oC. The fabricated IGZO/ZrO_x-TFT with the untreated ZrO_x films demonstrated a poor electrical performance, while the IGZO/ZrO_x-TFT with UVO treated ZrO_x gate dielectric displayed a low I_{on}/I_{off} current ratio of ~10^3, $V_{on} > 0$, saturation mobility of 8.4 $cm^2V^{-1}s^{-1}$, threshold voltage of 0.01 V, and sub-threshold swing of 0.21 $V.dec^{-1}$. Thus, extending the potential application of CSP to flexible electronic fabrication.

This thesis introduces spray pyrolysis method as a viable method for the deposition of quality high-κ metal oxide thin films, which can work as the gate dielectric layer in TFT. In this thesis, the unique properties of spray such as wide area uniformity and cost-effectiveness was leverage upon to improve the mass-production of future electronic devices.

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Abstract

High-κ metal oxide thin film by chemical spray pyrolysis: From optimization of material properties to application in thin film transistor

In today's electronic market, the demand for durable, flexible, and reliable electronic products have increased; hence electronic gadgets are becoming smaller in size, and they perform better than they have been in the past. The invention of transistor as an electronic component has been the major driving force for this rapid improvement. However, the current methods for fabricating thin film transistors (TFT) involves the stepwise deposition, patterning, and etching of either the channel or dielectric layer materials of TFT. This involves complex vacuuming or lithographic process, which add to the fabrication cost of TFT devices. For this reason, there has been a growing interest in the development of solution processed methods as an alternative TFT fabrication method. The unique advantage of solution processed method is the low processing cost, simplicity, and improved scalability. Despite the importance of solution processed methods, the unique potential of chemical spray pyrolysis (CSP) method has not been fully maximized in TFT fabrication. Although, due to densification or stability issues, this method is limited to high processing temperature, which inhibit its application in flexible electronics. Thus, to extend the application of spray pyrolysis in flexible electronic fabrication, it is important to focus on the reduction in the processing temperature of this method below 400 ^{o}C.

In light of fabricating metal oxide (MO) TFTs by CSP, many of the studies have focused on developing the channel layer of TFT, while the dielectric layer is neglected. Some studies on the dielectric layer have focused mainly on the effect of the growth mechanism such as high processing temperature (~300 ^{o}C), and the substrate system (glass or silicon) on the properties of fabricated dielectric layer. However, there exist a knowledge gap on the fabrication of MO-TFTs by CSP at low processing temperature.

Therefore, this thesis is aimed at strategizing the development of amorphous MO gate dielectric for TFT at low temperature, which will be suitable for low power consumption, and flexible electronic application by employing CSP method. The scope of this work is based on process optimization, thin film characterization and device fabrication.

The results presented in this thesis is based on four published papers: (1) the development of zirconium doped TiO_2 (Zr-TiO_2) thin film by CSP was discussed, (2) the development of ZrO_x thin film by CSP, (3) ultraviolet-ozone (UVO) post-deposition treatment of CSP deposited ZrO_x was discussed in order to lower the processing temperature of CSP deposited ZrO_x films, (4) application of ZrO_x thin film as the gate dielectric layer of TFT.

Zirconium doping was employed as a strategy to improve the properties of CSP deposited TiO_2 thin films and its influence on the morphological, optical, structural, and electrical properties of CSP deposited TiO_2 film was investigated. The surface morphology of the as-deposited Zr-TiO_2 films were uniform and smooth. The structural studies obtained from both X-ray diffraction (XRD) and Raman spectroscopy revealed that the Zr-dopant promotes amorphization in the film by inhibiting the TiO_2 growth rate. The as-deposited Zr-TiO_2 thin film was transparent with higher bandgap (3.52 eV, 40 mol% Zr-TiO_2) than the as-deposited undoped TiO_2 (3.14 eV). As a result of doping, the leakage current density was reduced from 1.7×10^{-3} A/cm^2 (in undoped TiO_2 film) to

4.5×10^{-5} A/cm^2 (in 40 mol % Zr-TiO_2 film). However, due to small bandgap value, the deposited Zr-TiO_2 film cannot be tested as gate dielectric layer in TFT. Thus, it is crucial to optimise and develop dielectric material with wider bandgap such as ZrO_x.

The influence of growth temperature on the structural and electrical properties of ZrO_x thin film was studied in order to establish the conditions to deposit a uniform and amorphous ZrO_x with high electrical performance. The SEM and XRD analysis revealed that a smooth and amorphous ZrO_x film can only be obtained at a deposition temperature below 500 °C. As the ZrO_x film deposition temperature was increased from 200 °C to 400 °C, the capacitance increased from 0.4 to 0.8 μF/cm^2, the relative permittivity increased from 8.5 to 22.7, and the leakage current density decreased from 4.3×10^{-4} A/cm^2 to 3.6×10^{-6} A/cm^2.

In addition, the processing temperature of sprayed ZrO_x thin film was lowered down to 200 °C by introducing ultraviolet-ozone (UVO) post-deposition treatment. The changes in the surface chemistry of the deposited ZrO_x thin film at different UVO exposure time was investigated by performing the X-ray photoelectron spectroscopy (XPS) and AFM analysis. By increasing the UVO treatment time from 0 to 120 min, the ZrO_x dielectric film demonstrated a slight increase in the [Me-OH]/[Me-O] component ratios from 0.94 to 1.22, and a decrease in the [Vo]/[Me-O] ratio from 0.65 to 0.38. The electrical properties, which was obtained through a DC and AC voltage revealed that the leakage current in the film was reduced by 3 order of magnitude from 2.0×10^{-5} A/cm^2 (untreated sample) to 1.0×10^{-8} A/cm^2 (120 min treated sample), and the area capacitance increases from 50 nF/cm^2 to 280 nF/cm^2 as the UVO treatment time increases from 0 to 120 minutes.

Furthermore, fully solution processed TFT was fabricated by employing the optimised CSP deposited amorphous ZrO_x thin film (at 400 °C) as the gate dielectric layer, and an amorphous zinc tin oxide deposited by spin coating (ZTO, at 350 °C) as the channel layer. The device demonstrated an excellent electrical performance with low hysteresis (−0.18 V), high I_{on}/I_{off} current ratio of 10^6 orders of magnitude, saturation mobility of 4.6 cm^{2}V^{-1}s^{-1}, subthreshold slope (SS) of 0.25 V dec^{-1}, and operating at a low voltage window of 3 V. However, as a proof of concept, the low temperature (200 °C) processed ZrO_x thin film was integrated in TFT without and after UVO treatment, and sputtered IGZO was employed as the channel layer. The TFT device with the untreated ZrO_x gate dielectric performs poorly, while the TFT device with the UVO treated ZrO_x gate dielectric exhibited better performance with saturation mobility ~ 8.4 cm^{2}V^{-1}s^{-1}, low I_{on}/I_{off} current ratio ~10^3, and operates at a low voltage window of 5 V.

In conclusion, the strategy to improve the properties of CSP deposited TiO_2 film by doping, and the possibility to fabricate MO-TFT by CSP method at 200 °C is first reported in this thesis. The presented results are of practical importance in the development of solution process metal oxide TFTs for low-cost and wide area fabrication. The simplicity and wide area uniformity of CSP is been exploited in this work. And concept of UVO post-deposition treatment adopted in this work will extends the potential of CSP to flexible electronic applications.

Lühikokkuvõte

Metallioksiidi õhukesed kiled keemilise pihustuspürolüüsi meetodil: materjali omaduste optimeerimine ja rakendamine õhukesekilelistes transistorides

Tänapäeva elektroonikaturul kasvab nõudlus vastupidava, painduva ja töökindla elektroonika järele – elektroonikaseadiste mõõdud kahanevad, kuid jõudlus kasvab varasemaga võrreldes. Transistori kui elektroonikakomponendi leiutamine on olnud elektroonilise aparatuuri kiire arengu peamiseks liikumapanevaks jõuks. Praegu rakendatakse õhukesekileliste transistoride (TFT) valmistamisel järjestiksadestamise skeemi ja keerulisi vaakum- või litograafiaprotsesse soovitud konfiguratsiooni saavutamiseks, mis teeb TFT-de valmistamise kulukas.

TFT-de valmistamine keemiliste vedeliksadestusmeetoditega on alternatiiv senistele tavapärastele valmistamismeetoditele. Keemiliste vedeliksadestusmeetodite peamisteks eelisteks on kulutõhusus, lihtsus ja valmistatava kihi ühtlus, mis loob eelduse nende meetodite kasutamiseks tööstuses. Hoolimata keemiliste vedeliksadestusmeetodite eelistest, ei ole keemilise pihustuspürolüüsi (CSP) meetodi ainulaadset potentsiaali TFT-de tootmises veel täielikult rakendatud. CSP meetodi rakendamist painduvate elektroonikaseadiste valmistamiseks on siiani piiranud suhteliselt kõrged sadestamis- ja/või järeltöötluse temperatuurid ja sellega kaasuvad tihenemis- ja püsivusprobleemid. CSP rakendamiseks painduvate elektroonikaseadiste tootmises on esmatähtis langetada valmistamisprotsessi temperatuur alla 400 °C.

Kirjanduses toodud uuringute järgi on CSP meetodil metalloksiidi (MO) TFT-de valmistamisel keskendutud TFT kanalikihi väljaarendamisele, ent dielektrilise kihi väljatöötamine on jäetud suurema tähelepanuta. Senistes dielektrilise kihi arendamise uuringutes on keskendutud peamiselt kile kasvumehhanismi, sadestus- ja järeltöötluse temperatuuri ja alusmaterjalide (klaas, räni) mõju uurimisele valmistatud kilede omadustele. Senini puudub teadmine, kas CSP meetodit on võimalik rakendada MO-TFT-de valmistamiseks madalatel temperatuuridel.

Käesoleva doktoritöö eesmärk on välja töötada strateegia amorfse metalloksiidi dielektriku kihi sadestamiseks keemilise pihustuspürolüüsi meetodil TFT jaoks, mis sobiks rakendamiseks energiatõhusas ja painduvas elektroonikaseadises. Doktoritöö keskendub metallioksiidide valmistamise protsessi optimeerimisele, materjalide omaduste uurimisele ja antud materjalidest TFT -de koostamise e ja karakteriseerimisele.

Doktoritöö põhineb neljal avaldatud teadusartiklil: (1) Zr-legeeritud TiO_2 (Zr-TiO_2) õhukese kile tehnoloogia väljatöötamine CSP meetodil, (2) ZrO_x õhukese kile väljaarendamine CSP meetodil, (3) CSP meetodil sadestatud ZrO_x kilede järeltöötluse tehnoloogia väljatöötamine ultraviolettkiirguse ja osooni (UVO) koosmõju all eesmärgiga alandada ZrO_x kilede sadestuse- ja järeltöötluse temperatuuri (4), CSP meetodil valmistatud ZrO_x õhukese kile rakendamine TFTs dielektriku kihina.

Uuriti Zr-ga legeerimise mõju TiO_2 kilede morfoloogilistele, optilistele, struktuursetele ja elektrilistele omadustele eesmärgiga parendada CSP sadestatud kilede omadusi. Leiti, et Zr-ga legeerimine pärsib kristallilise TiO_2 moodustumist, suurendab kilede keelutsooni väärtust 3,14 eV kuni 3,52 eV-ni (40 mol% Zr) ja vähendab lekkevoolu $1{,}7 \times 10^{-3}$ A (TiO_2) kuni $4{,}5 \times 10^{-5}$ A (40 mol% Zr-TiO_2). Paraku ei ole Zr-legeeritud TiO_2 kile keelutsooni väärtus piisav, et seda oleks otstarbekas kasutada TFT-s dielektrikuna. Seega on üliolulineb

välja arendada ja optimeerida laiema keelutsooniga dielektrilise materjali nagu ZrO_x kilede valmistamise tehnoloogia.

ZrO_x õhukese dielektrilise kile tehnoloogia väljatöötamiseks uuriti kasvutemperatuuri mõju CSP meetodil sadestatud kile struktuursetele ja elektrilistele omadustele. SEM ja XRD analüüsist selgus, et sile amorfne ZrO_x kile tekib kui sadestustemperatuurid on alla 500°C. Kilede kasvatamise temperatuuri tõstmine 200°C kuni 400°C suurendab nii kile mahtuvust (0,4 μ F cm^{-2} vs 0,8 μ F cm^{-2}) kui suhtelist dielektrilist läbitavust (8,5 vs 22,7). ZrO_x kile valmistamise temperatuuri saab alandada kuni 200°C-ni kui rakendada sadestamisjärgselt UVO töötlust. ZrO_x kile pinna keemilise koostise ja kareduse muutusi sõltuvalt UVO töötluse ajast uuriti röntgenfotoelektron-spektroskoopia (XPS) ja AFM meetoditel. XPS tulemuste analüüsist selgus, et UVO töötluse aja suurenemisega kuni 120 minutini vähenes hapniku vakantside osakaal ([Vo]/[Me-O]) 0,65-lt 0,38-ni. Mahtuvustakistuse mõõtmistest ilmnes, et 120 minutit UVO töötlust vähendab kile lekkevoolu tihedust 3 suurusjärku ($1,0 \times 10^{-8}$ A/cm^{-2} vs $2,0 \times 10^{-5}$ A cm^{-2}) ning mahtuvustihedus suurenes enam kui viis korda (280 nF cm^{-2} vs 50 nF cm^{-2}).

Täielikult vedeliksadestuse meetoditel põhinev TFT valmistati kasutades optimeeritud CSP tehnoloogiat amorfse ZrOx dielektrilise kihi valmistamiseks 400˚C juures ja pindvurritamise tehnoloogiat amorfse tsinktinaoksiidi (ZTO) kanalikihi jaoks. TFT elektrilised näitajad on: vähene hüsterees (−0,18 V), $I_{sees}/I_{väljas}$ =1x10^6, küllastunud laengukandjate liikuvus 4,6 cm^2 $V^{-1}s^{-1}$, lävieelne kalle (SS) 0,25 V dec^{-1}, ja madal 3 V-ne tööpinge. Madalal temperatuuril (200°C) sadestatud ZrO_x õhuke kile integreeriti TFT-sse töötlemata kujul ja UVO töödelduna. Kanalikihina kasutati katoodsadestuse meetodil valmistatud InGaZnO (IGZO) kilet. Töötlemata ZrO_x-dielektrikuga TFT oli kasina töövõimega, samas kui UVO töödeldud ZrO_x dielektriku kihiga TFT elektrilised näitajad on: tühine hüsterees, $I_{sees}/I_{väljas}$ =1x10^3, küllastusliikuvus 8 cm^2 $V^{-1}s^{-1}$, ja madal 5 V-ne tööpinge.

Kokkuvõtteks, doktoritöös töötati välja strateegia CSP-TiO_2 dielektriliste omaduste parendamiseks kasutades selleks tsirkooniumiga legeerimist. Selles töös näidati esmakordselt, et CSP meetodit on võimalik kasutada dielektrilise kihi sadestamiseks nii madalal temperatuuril nagu 200 °C kui sadestusjärgselt rakendada UVO järeltöötlust. Pihustussadestatud MO kihid näitavad omadusi, mis võimaldab neid kasutada TFT-des. Saadud tulemused on andnud olulise panuse vedeliksadestuse meetoditel valmistatud TFT-de väljatöötamise strateegiasse ja loonud aluse TFT-de kuluefektiivseks tootmiseks. Käesolevas väitekirjas rakendatakse CSP lihtsust ja võimet tagada sadestatud pinna ühtlus suurel pindalal. Selle töös arendatud ja rakendatud UVO järeltöötlus võimaldab CSP meetodit integreerida painduvate elektroonikaseadiste tootmisse.

Appendix 1

Publication I

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MATERIALS SCIENCE

Effect of Zr doping on the structural and electrical properties of spray deposited TiO_2 thin films

Abayomi T. Oluwabi[a*], Albert O. Juma[b], Ilona Oja Acik[a], Arvo Mere[a], and Malle Krunks[a]

[a] Laboratory of Thin Film Chemical Technologies, Department of Materials Science, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia
[b] Department of Physics and Astronomy, Botswana International University of Science and Technology, Private bag 16, Palapye, Botswana

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Abstract. Doping is an effective material re-engineering technique, which provides a possibility of improving properties of materials for different applications. Herein, a Zr-doped TiO_2 thin film was deposited applying the chemical spray pyrolysis method and the influence of varying zirconium dopant concentrations on the properties of the film was studied. Morphological studies showed that the Zr–TiO_2 films were homogeneous with smaller grain sizes compared to the undoped TiO_2 films. As-deposited Zr–TiO_2 films were amorphous while the undoped TiO_2 films were crystalline with anatase structure as revealed by both X-ray diffraction and Raman spectroscopy studies. The optical band gap of the Zr–TiO_2 film was higher (3.44 eV) than that of the undoped TiO_2 films (3.13 eV) showing a strong dependence on the phase composition. As revealed by energy dispersive spectroscopy analysis, the Zr/Ti ratio in the film increased from 0.014 to 0.13 as the doping concentration in the spray solution was increased from 5 to 40 mol%. The current–voltage (I–V) characteristic revealed a reduction of the leakage current in the Zr-doped TiO_2 film (6.06×10^{-5} A) compared to the undoped TiO_2 films (1.69×10^{-3} A) at 1 forward bias voltage. The dielectric relaxation response at the oxide–electrode interface dipole was strongly influenced by the Zr doping concentration in the film.

Key words: chemical spray pyrolysis, doping, thin films, dielectric relaxation, Zr–TiO_2.

1. INTRODUCTION

Recently, silicon-based materials have been in limited use because of the growing interest in cost-effective and low-temperature processing materials that could for example replace the SiO_2 gate dielectric layer of most conventional thin film transistor (TFT) devices [1]. However, solution-processed metal oxide materials such as titanium oxide (TiO_2), zirconium oxide (ZrO_2), hafnium oxide (HfO_2), aluminium oxide (Al_2O_3), tantalum oxide (Ta_2O_5), and their mixtures are tenable alternatives due to their demonstrated uniformity over a large area and a suitable dielectric constant [1,2].

Titanium oxide and its polymorphs have attractive and promising unique properties ranging from optical to electronic properties, hence it has gained its use in a wide range of applications, especially in TFTs [3–7]. Many routes have been adopted to enhance its properties, but the doping of TiO_2 with different metallic or non-metallic elements has displayed its effectiveness [8,9] owing to the fact that doping affects the phase transition temperature [10] and it can be easily harnessed by controlling the composition of mixed oxides [8].

* Corresponding author, abayomioluwabi@gmail.com

The Zr doping in TiO_2 is chosen because Zr and Ti are isovalent, which supports adequate incorporation of Zr into the TiO_2 lattice thereby increasing its bond length to form a solid solution of $Ti_{x-1}Zr_xO_2$ and stabilizing the anatase phase by delaying crystallite growth [8,11]. In the microstructure of the film formed from the mixture of TiO_2 and ZrO_2, whose band gap (5.8 eV) and ionic radius (0.084 nm) are higher than those of TiO_2 (band gap 3.0–3.4 eV and ionic radius 0.061 nm), plays an important role [1,8]. Owing to these remarkable properties, different research groups have reported Zr-doped TiO_2 thin films, nanorods, and microspheres for different applications [12,13]. Lukáč et al. [14] reported the effect of the annealing temperature on the photo-catalytic performance of Zr-doped TiO_2 films. Wang's research group [15] investigated the behaviour of Zr^{4+} dopant ion in Zr-doped TiO_2 nanoparticles.

Several methods such as chemical vapour deposition, the sol–gel method, reactive sputtering, and ultrasonic spray pyrolysis have been used to deposit Zr-doped TiO_2 films ([11] and references therein). Among these methods, chemical spray pyrolysis (CSP) is an attractive technique for the preparation of thin films because it is simple to operate and use, film thickness and deposition parameters are easy to control, it can be operated at moderate temperatures, it does not require vacuum, and it is not selective in the choice of substrate [11]. This technique offers an opportunity to deposit uniform and compact films for a wide area of device applications, while the film properties strongly depend on the precursor reagent and on the deposition conditions [16]. Castañeda et al. [17] reported deposition of TiO_2 thin films by spray pyrolysis in the substrate temperature range of 300–500 °C. Okuya et al. [18] also reported the influence of additives in the precursor solution on the mechanism of the crystallization of TiO_2. The properties of TiO_2 films prepared by the spray pyrolysis method are also reported in [6]. To the best of our knowledge, the properties of Zr-doped TiO_2 thin films deposited by CSP have not been completely studied.

In our study, Zr-doped TiO_2 thin films were deposited using CSP by varying the Zr/Ti mole ratio in the solution. The structural, morphological, optical, and electrical properties of the deposited films were investigated for their application as the dielectric layer in a TFT.

2. EXPERIMENTAL

The Zr-doped TiO_2 films were deposited from analytical-grade titanium(IV) isopropoxide (TTIP) and zirconium acetylacetonate ($Zr(AcacH)_4$) reagents (from MERCK and ALDRICH, respectively) as the precursors. The synthesis of the TiO_2 precursor was performed as follows: TTIP (1.8 mL) was stabilized with acetylacetone (1.2 mL) in the ratio 1 : 2, which was maintained all through the experiment. To this solution, 13.5 mL of ethanol was added and the solution was stirred to ensure homogeneity. The prepared solution was sprayed onto preheated quartz and silicon substrates using a pneumatic spray set-up. The films deposited on the quartz substrate were used for structural studies, while the films deposited on the silicon substrate were used for electrical studies.

The Zr-doped TiO_2 solution was prepared by adding quantitative amounts of $Zr(AcacH)_4$ corresponding to Zr/Ti mole ratios of 5, 10, 20, and 40 mol% into an already stabilized TTIP and the above procedure was repeated. The substrates were placed on a tin bath (*T*sn) maintained at 450 °C and the precursors were sprayed at a rate of 2.5 mL/min with compressed air as the carrier gas. The flow rate of the carrier gas was 8 L/min with one spray cycle consisting of 60 s spraying plus 60 s pause. Ten spray cycles were made from each solution. The samples were then annealed in air for one hour at temperatures from 500 °C to 900 °C using a Nabertherm L5/11/06D furnace. The as-deposited and annealed films were labelled 'undoped TiO_2' and '*x*-Zr–TiO_2' for the undoped and doped samples, respectively, where *x* corresponds to the mol% concentration of Zr in the sprayed solution.

Optical measurements were performed by measuring total transmittance and total reflectance spectra using a Jasco-V670 spectrophotometer equipped with an integrating sphere in the wavelength range 300–800 nm. The X-ray diffraction (XRD) patterns were obtained using a Rigaku Ultima IV diffractometer, which has a silicon line detector and a Cu K_α radiation source operated at 40 kV and 40 mA. The surface morphology and elemental composition were studied using a ZEISS HR Ultra 55 scanning electron microscope (SEM) with a Bruker energy dispersive spectroscopy (EDS) system ESPRIT 1.8. The acceleration voltage for SEM measurements was 4.0 kV and for EDS, 7.0 kV. Raman spectra were acquired using a micro-Raman spectrometer HORIBA Jobin Yvon Model HR800 with 532 nm laser excitation line, which delivers 5 mW of power at 10 μm laser spot size during measurements. Raman peak analysis was based on Lorenzian fitting. To access the electrical properties of the as-deposited films, we produced a metal-oxide semiconductor (MOS) device by growing gold contact using a Quorum K975X vacuum evaporator on top of the TiO_2 film surface with a contact area of 1.7 mm^2, giving a Si/TiO_2[Zr]/Au structure. The c-Si wafer was contacted through a eutectic indium alloy to ensure ohmic conductivity. The current–voltage and impedance data were obtained using AUTOLAB PGSTAT30/2 and analysed using frequency–response analysis software. A schematic presentation of the investigated MOS structure is given in Fig. 1.

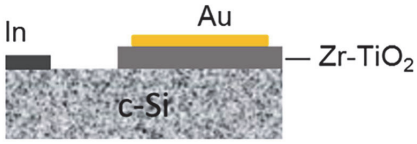

Fig. 1. Metal oxide semiconductor device for measuring electrical properties of x-Zr–TiO_2 thin films ($0 \leq x \leq 40$ mol%).

3. RESULTS AND DISCUSSIONS

3.1. Surface morphology and composition

The SEM images were used to study the influence of varying Zr concentrations in the precursor solution on the morphology of the TiO_2 films. Figure 2 presents the SEM images of the as-deposited (Tsn = 450 °C) samples and those annealed at 600 and 800 °C. The as-deposited undoped TiO_2 and (5, 20)-Zr–TiO_2 films were uniform and compact. Grains started to increase in the film after annealing at 600 °C (Fig. 2 B, E, H). After annealing at 800 °C the surface of the undoped-TiO_2 film consisted of smaller and larger grains of up to about 250 nm in size (Fig. 2C); however, the surface of the 20-Zr–TiO_2 film (Fig. 2I) consisted of grains with a size of up to about 50 nm.

The thicknesses of films are shown in the insets of Fig. 2. The results obtained revealed that the undoped TiO_2 film was thicker than both 5-Zr–TiO_2 and 20-Zr–TiO_2 films (330 nm, 310 nm, and 250 nm, respectively), which means that the thickness of a film decreased with increasing the Zr concentration in the spray solution. This is a common behaviour of spray deposited doped films [19], which could be due to the fact that increasing the dopant concentration in the solution retards the growth of the film. The film thicknesses in both undoped TiO_2 (322 nm) and 5-Zr–TiO_2 (302 nm) films changed slightly after annealing at 800 °C, but changed significantly in the 20-Zr–TiO_2 film (167 nm). A similar result was reported for zirconium doping by atomic layer deposition [20].

The presence of Zr in the as-deposited Zr-doped TiO_2 film was confirmed by EDS analysis, which revealed an increase in the Zr/Ti atomic ratio in the film from 0 to 0.13 as the mole ratio in the precursor solution was increased from 0 to 40 mol%. The evaluation of Zr content in the film revealed that more than 10% of the Zr content in the precursor solution adequately doped into the film, which indicates that Zr was actually present in the deposited film. This is similar to what was observed for Zr-doped ZnO films deposited by the spray method in [19].

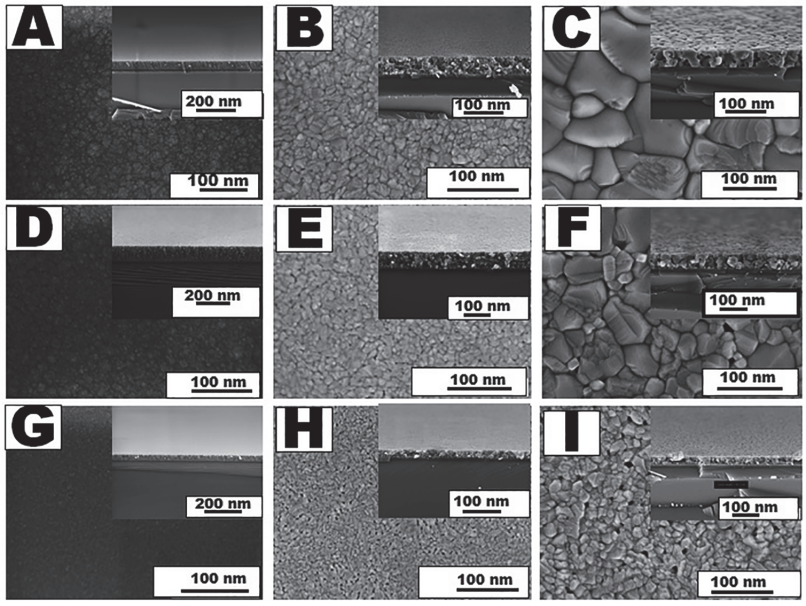

Fig. 2. SEM images of undoped TiO_2 (A–C), 5-Zr–TiO_2 (D–F), 20-Zr–TiO_2 (G–I) thin films; as-deposited (A, D, G) and after annealing at 600 °C (B, E, H) and 800 °C (C, F, I). The inset contains their corresponding SEM cross-sectional images. (Films were deposited on a Si substrate.)

3.2. Structural and phase characterization

3.2.1. XRD study

The obtained XRD patterns of undoped TiO_2 and Zr-doped TiO_2 films are shown in Fig. 3. For the as-deposited samples (Fig. 3a), the undoped TiO_2 film shows a sharp peak and the 5-Zr–TiO_2 film, a weak peak at $2\theta = 25.40°$ belonging to the anatase (101) phase (PDF powder diffraction-01-075-1573). The (10, 40)-Zr–TiO_2 films were amorphous, which indicates an amorphization effect of incorporating Zr into the TiO_2 lattice structure. Gao et al. also reported that Zr doping delays the transition of the amorphous to the anatase phase of TiO_2 deposited by the sol–gel method [21].

The (5, 40)-Zr–TiO_2 films showed amorphous to anatase phase transition after annealing at 500 °C, which was sustained up to 700 °C. After annealing at 700 °C and 800 °C (Fig. 3b and c), the undoped TiO_2 film showed a mixture of both rutile and anatase phases with the anatase (101) peak at $2\theta = 25.40°$ and the rutile (110) main peak at $2\theta = 27.43°$ (PDF01-0714808) while the doped films remained anatase. However, anatase and rutile mixed phases appeared in the 10-Zr–TiO_2 film after annealing at 800 °C, which is an indication of the stabilization of the anatase phase thereby delaying the formation of the rutile phase. A similar result on the formation of anatase and rutile mixed phases was also reported by research groups of Schiller et al. and Wang et al. on sol–gel deposited Zr-doped TiO_2 powders and films, respectively [8,15].

Figure 3d reveals the shift in the position of the anatase (101) main peak as a function of the Zr concentration in the solution after annealing at 500 °C. The position of the (101) diffraction peak shifted to lower values of the diffraction angle 2θ (from 25.79° to 25.60°) in the diffraction pattern with the increasing Zr amount in the film, which confirms the incorporation of Zr^{4+} in the TiO_2 lattice structure. The presence of Zr^{4+}, which

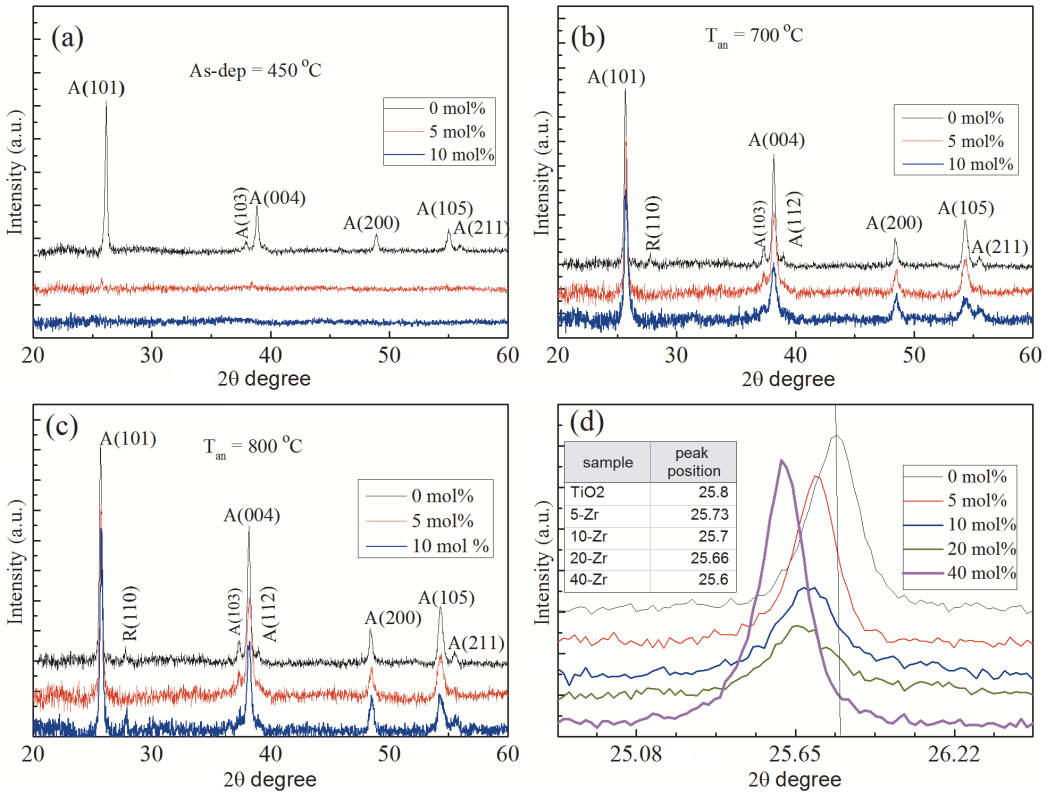

Fig. 3. XRD patterns of undoped and *x*-Zr–TiO_2 films where $x = 0$, 5, 10 mol%: (a) as-deposited at 450 °C, (b) after annealing at 700 °C, and (c) 800 °C. The shift in the anatase (101) main diffraction peak position (P.P) as a function of the Zr/Ti mole ratio in the spray solution is presented in (d) after annealing at 500 °C. (Films were deposited on a quartz substrate.)

has a larger ionic radius of 0.072 nm compared to Ti^{4+} (0.061 nm) in the TiO_2 matrix, causes an increase in the unit cell parameters, which brings about a shift in the peak position to a lower 2θ angle as explained by Bragg's law [21].

The mean crystallite size of the undoped TiO_2 and Zr-doped TiO_2 films annealed at different temperatures was calculated by applying the Scherrer formula on the (101) anatase peak; the values obtained are presented in Table 1. The Zr-doped TiO_2 films have smaller mean crystallite sizes than the undoped TiO_2 films, which decrease with an increase in the Zr concentration in the film. At temperatures above 700 °C, the Zr-doped samples displayed distinctively smaller crystallite sizes than the undoped TiO_2 sample, which is an indication of increased amorphization due to Zr doping. This phenomenon is explained by the increase in the number of nucleation sites that inhibit the growth of larger crystallites with doping [8,22,23].

Table 1. Mean crystallite size of undoped TiO_2, 5-Zr–TiO_2, and 20-Zr–TiO_2 films calculated by applying Scherrer's formula on the anatase (101) peak at different temperatures of annealing

Annealing T (°C)	Mean crystallite size, nm		
	TiO_2	5-Zr–TiO_2	20-Zr–TiO_2
500	40	50	30
600	30	30	20
700	35	30	25
800	40	35	30
1000	50	45	40

3.2.2. Raman study

The Raman spectra for the undoped and Zr-doped TiO_2 films are shown in Fig. 4. The as-deposited TiO_2 spectrum reveals a Raman band at 141 cm^{-1} belonging to the TiO_2

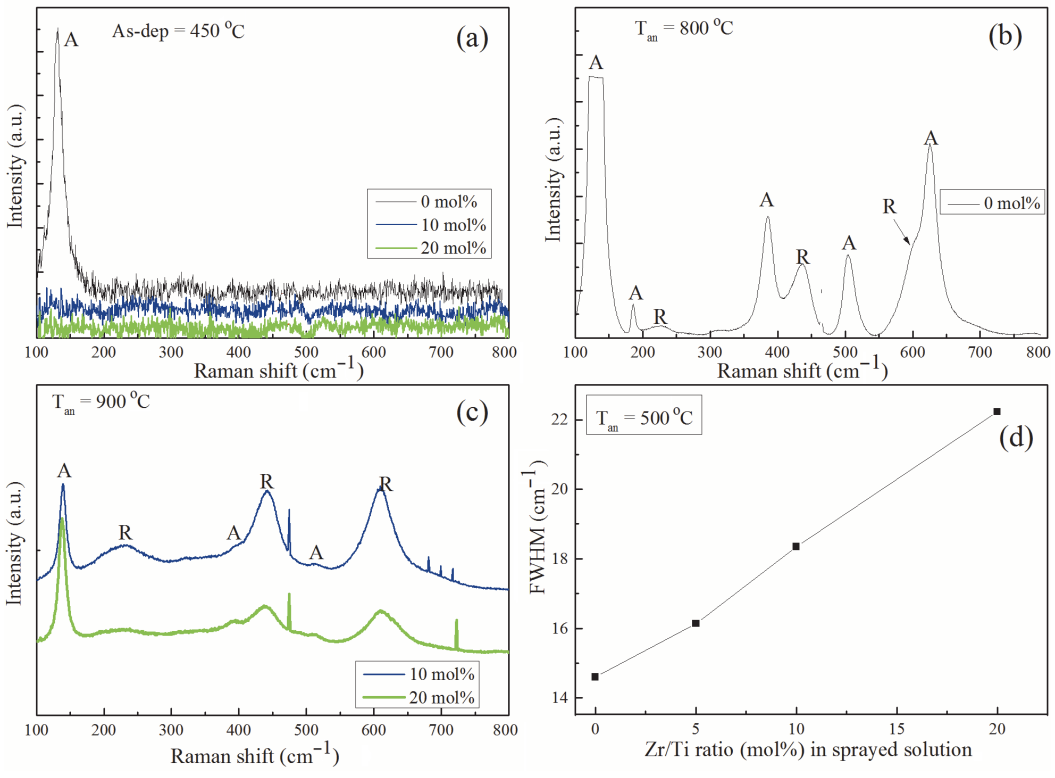

Fig. 4. Raman spectra of the as-deposited undoped and (10, 20)-Zr–TiO_2 films grown at 450 °C (a), undoped TiO_2 film after annealing at 800 °C (b), and (10, 20)-Zr–TiO_2 films after annealing at 900 °C (c). The FWHM as a function of Zr/Ti mol ratio in the spray solution after annealing at 500 °C is presented in (d). (Films were deposited on a quartz substrate.)

anatase phase while the doped films are amorphous, concurring with the XRD data (Fig. 4a). After annealing at 800 °C the undoped TiO_2 films revealed Raman peaks at 141, 191, 398, 513, and 639 cm^{-1} (Fig. 4b), which are characteristic of the crystalline TiO_2 anatase phase [24]. The peaks at 141, 191, and 639 cm^{-1} correspond to E_g vibration modes, while the 398 and 513 cm^{-1} peaks correspond to B_{1g} and $A_{1g} + B_{1g}$ modes of the anatase phase, respectively [25]. In addition to those, the undoped TiO_2 film Raman spectrum shows additional peaks at 232 and 499 cm^{-1}, which belong to the TiO_2 rutile phase after 800 °C (Fig. 4b).

The observed intensity of the Raman peaks decreased upon the introduction of Zr (figure not shown). This indicates an increase in lattice imperfections due to the incorporation of Zr [26]. The undoped TiO_2 film shows additional peaks at 232 and 449 cm^{-1}, which belong to the TiO_2 rutile phase after annealing at 800 °C (Fig. 4b). Also after annealing at 900 °C, the 10-Zr–TiO_2 and 20-Zr–TiO_2 films show mixed anatase and rutile phases (Fig. 4c). The full width half maximum (FWHM) values as a function of doping concentration presented in Fig. 4d are those of the anatase main peak positioned at 141 cm^{-1} after the films were annealed at 500 °C. The FWHM increases from 14.5 cm^{-1} to 22.23 cm^{-1} with the concentration of Zr^{4+} dopant, indicating a reduction in the size of the crystallite.

Table 2 summarizes the XRD and Raman results of Zr-doped TiO_2 thin films at different annealing temperatures for different Zr doping concentrations present in the precursor solution. As-deposited x-Zr–TiO_2 films, where values of x are in the range $5 \le x \le 40$ mol%, are mainly amorphous with no trace of other crystalline phases detected in the samples. This is an indication that Zr inhibits the crystallization of TiO_2 films and that Zr is distributed into the TiO_2 matrix as a dilute solid solution [21]. The higher the doping concentration, the more phase transition temperature is shifted to higher temperatures. The 40-Zr–TiO_2 films show that the anatase phase is stable even after annealing at 900 °C, indicating high phase stability.

3.3. Optical properties

Figure 5 shows the total transmittance spectra for the as-deposited TiO_2 thin film at different Zr-doping concentrations in the wavelength range between 300 and 800 nm. All the thin films show interference patterns with optical transparency above 60% in the visible region (from 400 to 800 nm). The interference patterns are a result of multiple reflections at the air–film and film–substrate interfaces due to the difference in the refractive index between the air, the TiO_2 film, and the substrate. This confirms that the films were transparent in the visible region, homogeneous, and uniformly coated on the substrates [27,28] as seen in the SEM images (Fig. 2). The interference occurs when the film surface is reflective with less scattering or absorption in the bulk. If the film surface is rough, the incident light will be scattered in all directions without reflection [28]. The total transmittance increases as the concentration of Zr in the solution is increased. A blue shift in the absorption edge of the transmittance spectra of the Zr-doped TiO_2 films compared with the TiO_2 spectrum

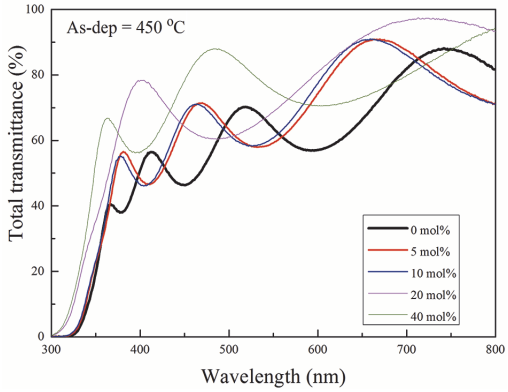

Fig. 5. Total transmittance spectra of the as-deposited TiO_2 films with different Zr-doping concentrations. (Films were deposited on a quartz substrate.)

Table 2. Phase composition of Zr-doped TiO_2 thin films at different annealing temperatures T_{an}. The phases are shaded in the cells: A – anatase, R – rutile, amorf – amorphous

[Zr], mol% in spray solution	As-deposited		T_{an} = 500 °C		T_{an} = 600 °C		T_{an} = 700 °C		T_{an} = 800 °C		T_{an} = 900 °C		T_{an} = 1000 °C	
	Raman	XRD	Raman	XRD	Raman	XRD	Raman	XRD	Raman	XRD	Raman	XRD	Raman	XRD
0	A	A	A	A	A	A	A	A+R	A+R	A+R	A+R	A+R	–	A+R
10	Amorf	Amorf	A	A	A	A	A	A	A	A+R	A+R	A+R	–	A+R
20	Amorf	Amorf	A	A	A	A	A	A	A	A	A+R	A+R	–	A+R
40	Amorf	Amorf	A	A	A	A	A	A	A	A	A	A	–	A+R

denotes an increase in the optical band gap with an increasing Zr concentration caused by a change of the lattice constant.

The optical direct band gap energy of the deposited films was calculated by applying expression (1) on a Tauc plot [29] after taking into consideration the reflectivity, absorption coefficient, and film thickness as these strongly affect the transparency of the film.

$$(ahv) = A(hv - E_g)^n. \quad (1)$$

Here α is the optical absorption coefficient, hv is the photon energy, A is a constant called critical absorption, the value of n varies depending on whether the band transition is direct or indirect, and E_g is the optical band gap. The values of E_g for undoped and Zr-doped TiO_2 films were obtained by plotting $(ahv)^{1/n}$ against the photon energy (hv) when the value of $n = 0.5$ for direct transition. The linear part of the curve was then extrapolated to the hv axis as shown in Fig. 6a for (0-10)-Zr–TiO_2 films [30,31]. The band gap energy of the 10-Zr–TiO_2 thin film (3.2 eV) was higher than that of the undoped TiO_2 film (3.14 eV). The value of E_g increased slightly (from 3.23 eV to 3.38 eV) with annealing temperature rising up to 600–700 °C and later decreased (to 3.05 eV) as the rutile phase started to form in the 10-Zr–TiO_2 thin film (Fig. 6b).

Theoretical calculations of the electronic properties of Zr-doped TiO_2 films show no change in the band gap [32,33] while experiments have given mixed results depending on the method of the preparation and the nature of doping. An increase in the band gap was reported for nanocrystalline samples, which was attributed to the quantum confinement effect because of the small particle sizes [34]. The increase in the band gap and decreased crystallite sizes with Zr-doping were reported for sol–gel deposited samples [17,28]. The slight change in the band gap values observed in this work can therefore be due to structural changes caused by Zr-doping and annealing [14].

3.4. Electrical studies

3.4.1. Current–voltage characteristics

The leakage current in the forward bias regime is illustrated in Fig. 7 for the as-deposited undoped TiO_2 and (20, 40)-Zr–TiO_2 films. The leakage current at 1 V amounted to 1.7×10^{-3} A, 6.1×10^{-5} A, and 4.5×10^{-5} A for undoped-TiO_2, 20-Zr–TiO_2, and 40-Zr–TiO_2, respectively. The Zr dopant helped to reduce the leakage current by two orders of magnitude. Considering the fact that the leakage current is exponentially dependent on the thickness of the insulating layer, we normalized the thickness value in both undoped TiO_2 and Zr-doped TiO_2 layers to 200 nm in our calculations. This helped us to prove that the tendency we show in Fig. 7 was due to the dopant effect. For TiO_2 deposited by the CSP technique, leakage currents of similar magnitudes were reported in the literature [35]. The zero-bias barrier heights of the undoped and Zr-doped TiO_2 samples were determined from the vertical intercept of the ln(I)–V plots (plot not shown) and calculated using the following expression [36]:

$$\emptyset_B = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_0}\right), \quad (2)$$

where A is the effective area of the diode, A^* is the effective Richardson constant equal to 1200 A cm^{-2} T^{-2}

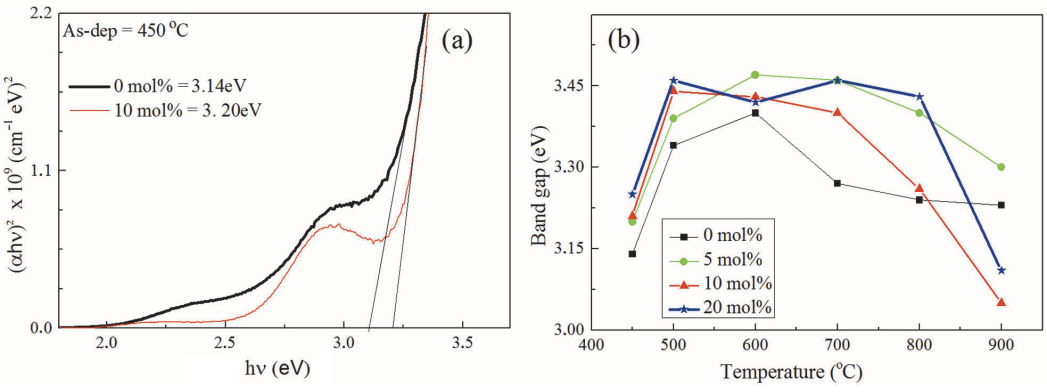

Fig. 6. (a) Determination of the optical band gap of as-deposited undoped and Zr-doped TiO_2 films and (b) the variation of the band gap of the undoped and Zr-doped TiO_2 films with the annealing temperature. (Films were deposited on a quartz substrate.)

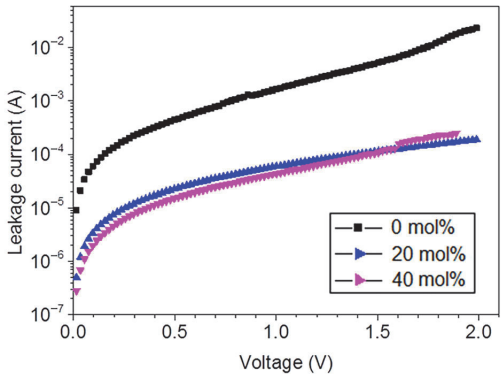

Fig. 7. Leakage current as a function of forward bias voltage for *x*-Zr–TiO_2 films where the concentration of Zr in the solution $x = 0$, 20, and 40 mol%. The metal oxide semiconductor structure is Si/TiO_2[Zr]/Au.

for TiO_2 [37], k is the Boltzmann constant, and $Ø_B$ is the Schottky barrier height.

The reverse saturation current I_0 amounted to 8.45×10^{-3} A/cm^{-2}, 3.84×10^{-3} A/cm^{-2}, and 2.53×10^{-3} A/cm^{-2} for the undoped TiO_2, 20-Zr–TiO_2, and 40-Zr–TiO_2, respectively. The values of $Ø_B$ obtained using Eq. (2) amounted to 0.536, 0.562, and 0.571 eV for the undoped TiO_2, 20-Zr–TiO_2, and 40-Zr–TiO_2, respectively. The decrease in the leakage current observed could be due to the possibility of the material losing its conductivity in the forward regime. These values compare well with those found in the literature for similar structures of TiO_2 deposited by other methods such as spray pyrolysis [35], magnetron sputtering [38], plasma enhanced physical vapour deposition [39], and dip coating [40], for which Schottky barrier heights between 0.4 and 1.0 eV were reported. It is evident that the electronic properties of TiO_2 thin films and their derivatives depend strongly on the deposition method and conditions.

3.4.2. Frequency response analysis

Figure 8a shows the Nyquist plot for the as-deposited undoped TiO_2 and Zr-doped TiO_2 thin films on Si substrates. The plots from the undoped TiO_2 and 20-Zr–TiO_2 with Zr/Ti = 20 mol% were multiplied by a factor of 50 for better presentation and comparison. The Nyquist plot for the undoped TiO_2 film shows more than one semicircle, implying that the sample could be modelled by more than one parallel resistor–capacitor (RC) circuit combination. For the (20, 40)-Zr–TiO_2 films, it appears that the semicircles enlarge and overlap to form a larger semicircle. The increase in the Z′ component is much greater than that in the Z″ component, indicating a strong increase in the parallel resistance compared to the change in the capacitance of the TiO_2 with doping.

In Fig. 8b a slight increase in the total impedance for the 20-Zr–TiO_2 sample and a strong increase in the 40-Zr–TiO_2 sample by almost two orders of magnitude can be observed. The undoped-TiO_2 sample shows two points of inflection (where the gradient changes) at frequencies of 4 kHz and 110 kHz, while the doped samples have inflection points at 42 kHz and 620 Hz for the 20-Zr–TiO_2 and 40-Zr–TiO_2 samples, respectively. The Bode phase plots show phase angles close to 90° in

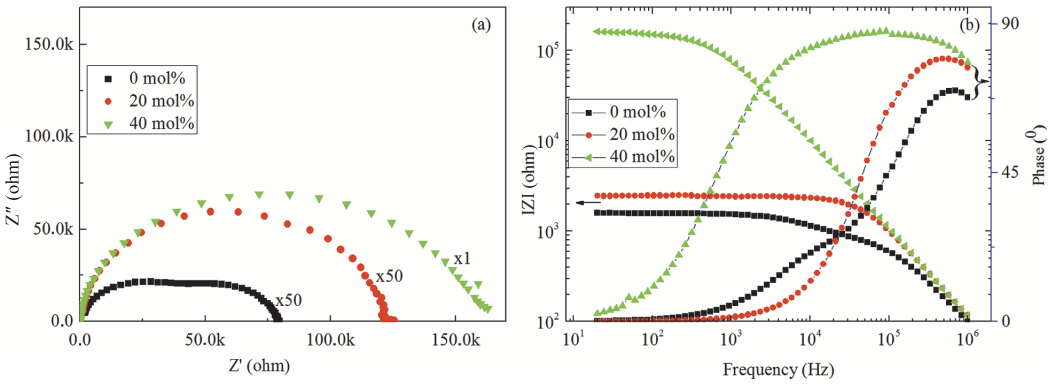

Fig. 8. Nyquist plot (a) and Bode plot (b) for the *x*-Zr–TiO_2 film where the concentrations of Zr in the solution $x = 0$, 20, and 40 mol%. The impedance plots for the TiO_2 and 20-Zr–TiO_2 samples were multiplied by a factor of 50 for the purpose of comparison. The metal oxide semiconductor structure is Si/TiO_2[Zr]/Au.

the high frequency region, exhibiting more capacitive behaviour, but in the low frequency region, the phase is close to zero. The undoped TiO_2 film shows two peaks in the mid- and high-frequency regions. However, the (20, 40)-Zr–TiO_2 films show one broad peak spanning the mid- and high-frequency regions, which broadens as the amount of Zr dopant in the film increases from 20 to 40 mol%.

By plotting Z' vs $\omega Z''$ as proposed by Abrantes et al. [41] and Walke et al. [42], the contributions from different relaxation frequencies that correspond to the circuit time constant can be resolved. The relaxation frequencies are determined from the slopes of the linear sections of the Z' vs $\omega Z''$ plots as demonstrated in Fig. 9. The undoped TiO_2 film shows three different slopes resulting in three relaxation frequencies of 72 kHz, 6 kHz, and 650 Hz. Based on this result, the undoped TiO_2 film can be accurately represented by an equivalent circuit composed of three parallel RC components. The 20-Zr–TiO_2 film shows only two slopes of relaxation frequencies 47 kHz and 30 kHz, which are quite close. The 40-Zr–TiO_2 film shows three slopes with relaxation frequencies 750 Hz, 540 Hz, and 186 Hz. It was observed that as the concentration of the dopant was increased, the relaxation frequency shifted to much lower frequencies. This implies that with higher Zr doping the dielectric response due to the oxide–electrode interface dipoles dominates the dielectric properties of the Si/Zr–TiO_2/Au structure [43]. Understanding the nature of such interfaces as a function of the dopant type and concentration is therefore crucial to the performance of any electronic devices.

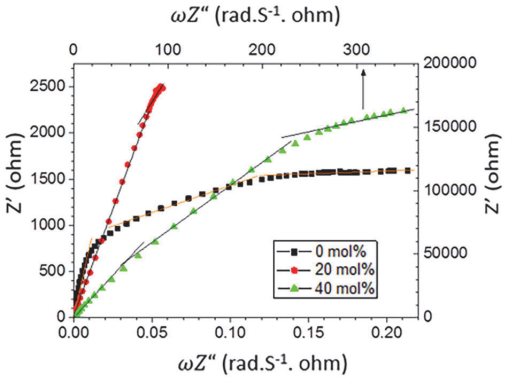

Fig. 9. Real part of the impedance vs imaginary part divided by the frequency for x-Zr–TiO_2 films where the concentrations of Zr in the solution x = 0, 20, and 40 mol%. The scale for the 40-Zr–TiO_2 film sample is top and right. The metal oxide semiconductor structure is Si/TiO_2[Zr]/Au.

4. CONCLUSIONS

The CSP method was successfully used to deposit a uniform and homogeneous Zr-doped TiO_2 film. The XRD data reveal that the as-deposited Zr-doped TiO_2 samples were amorphous, which became crystalline with anatase crystal structure after annealing at 500 °C. The average crystallite sizes were between 20 and 50 nm. A mixture of anatase and rutile phases was observed for the Zr-doped TiO_2 after annealing at 800 °C. Raman analysis, which complements the XRD results, showed that the FWHM value of the anatase main peak at 141 cm^{-1} increased with Zr/Ti mole ratio in the precursor solution, confirming the decrease in the crystallite sizes with enhanced Zr doping. The leakage current in the as-deposited TiO_2 was reduced by two orders of magnitude with Zr doping of TiO_2 and the dielectric relaxation response at the oxide–electrode interface shifted to lower frequencies, from 72 kHz to 750 Hz, as the Zr concentration in the sprayed solution was increased, thus influencing the dielectric properties of the Si/Zr–TiO_2/Au structure. The results indicated that Zr dopant influenced the properties of CSP deposited TiO_2 films, being compatibly useful as the gate dielectric layer in the transistor application of thin film.

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Zr-legeerimise mõju pihustuspürolüüsimeetodil sadestatud TiO_2 õhukeste kilede struktuursetele ja elektrilistele omadustele

Abayomi T. Oluwabi, Albert O. Juma, Ilona Oja Acik, Arvo Mere ja Malle Krunks

Antud uurimistöös sadestati zirkooniumiga legeeritud TiO_2 (Zr-TiO_2) kiled keemilisel pihustuspürolüüsimeetodil. Uurimistöö eesmärk oli uurida Zr kui legeeriva elemendi mõju pihustatud TiO_2 kilede morfoloogilistele, struktuurilistele, optilistele ja elektrilistele omadustele ning hinnata antud materjali võimekust töötada dielektrilise kihina õhukesekilelistes transistorides. Leiti, et pihustatud Zr-TiO_2 kiledel on väiksem tera suurus kui legeerimata TiO_2 kiledel. EDS-analüüs näitas, et Zr/Ti aatomsuhe kiledes suureneb 0,014 kuni 0,13, kui tõsta Zr kontsentratsiooni pihustuslahuses vahemikus 5–40 mol%. XRD- ja Ramani analüüs näitas, et äsja sadestatud TiO_2 kiled on kristallilised anataasi struktuuriga, kuid Zr-TiO_2 kiled on amorfsed. TiO_2 kilede kuumutamisel 700 °C ja Zr-TiO_2 kilede kuumutamisel 800 °C juures saadi kiled, mis koosnesid anataasi ning rutiili faaside segust. TiO_2 ja Zr-TiO_2 kiled näitasid optilist keelutsooni väärtust vastavalt 3,13 ning 3,44 eV. Äsja sadestatud 20-Zr-TiO_2 kiled näitavad rakendatud päripinge 1 V juures väiksemat lekkevoolu ($6{,}06 \times 10^{-5}$ A) kui TiO_2 kiled (1.69×10^{-3} A). Töö tulemusena leiti, et pihustuspürolüüsimeetodil sadestatud ja järelkuumutatud Zr-TiO_2 kiledel on perspektiivi, kasutamaks neid dielektrilise kihina õhukesekilelistes transistorides.

Publication II

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Structural and electrical characterisation of high-k ZrO_2 thin films deposited by chemical spray pyrolysis method

Abayomi T. Oluwabi*, Ilona Oja Acik*, Atanas Katerski, Arvo Mere, Malle Krunks

Laboratory of Thin Film Chemical Technologies, Department of Materials and Environmental Technology, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia

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ABSTRACT

As the applicability of high-k oxides in field-effect transistor became enormous, the physical and chemical understanding of their dielectric properties as well as preparation technique should be diligently studied. Herein, we have studied the deposition of zirconium oxide (ZrO_2) thin film by chemical spray pyrolysis and we have investigated the influences of deposition temperature (200, 300, 400, 500 °C) and annealing temperature (500, 800 °C) on the morphological, structural, optical, and electrical properties of the film. It was observed that the as-deposited ZrO_2 thin films at temperature below 500 °C were smooth, dense, and structurally amorphous – while the ZrO_2 thin film deposited at 500 °C are poorly crystalline. As confirmed by Raman and X-ray diffraction peak deconvolution, ZrO_2 tetragonal phase was predominant in the film upon annealing at 500 °C, and the monoclinic phase favoured after annealing at 800 °C. As-deposited ZrO_2 thin film are optically transparent (above 80% in the visible region) with a slight decrease in transmittance upon annealing at higher temperature. The optical band gap of ZrO_2 film was in the range 5.39–5.68 eV and the dielectric constant (k) in the range 4.3–13.0, depending on the deposition temperature.

1. Introduction

After the invention of the first microprocessor, the technological demand of transistor became enormous in integrated circuit, which led to its constant evolutionary improvement [1]. Now, the current interest in miniaturization in modern electronic devices has limit the silicon-based materials, because of increased gate leakage current due to quantum tunnelling effects [2], however, the use of structurally amorphous high-k materials offer the possibilities of controlling this problem owing to their wide band gap and high dielectric constant [3]. Moreover, amorphous high-k materials also help to improve the interface properties of thin film transistor (TFT) device compared to polycrystalline ones, because the former are smoother with no grain boundaries than the latter [1]. Nowadays the applicability and processability of various high-k materials (such as; Al_2O_3, Y_2O_3, Ta_2O_5, ZrO_2, HfO_2 etc.) have been studied by different researchers as the gate dielectric layer in TFT [3–6].

Among the plausible high-k materials, zirconium dioxide (ZrO_2) is a desirable gate insulator because it offers the possibility of ensuring an optimum band offset (above 2 eV) with the channel layer. Additionally, its optical property, high band gap energy, high refractive index, high thermal stability and high dielectric constant has all together contributed to its attractive study in different applications [4, 5, 7]. Generally, the properties of metal oxide material are structurally dependent and ZrO_2 is not an exception. Three different polymorphs of ZrO_2 exist; namely tetragonal (t), cubic (c), and monoclinic (m), with each having relatively different dielectric properties [8, 9]. For example, Vanderbelt et al., reported the average dielectric constant (k) for three ZrO_2 polymorphs (t-47, c-37, m-17) using computational techniques [10]. Kukli et al., have reported a mixture of t-ZrO_2 and c-ZrO_2 phases with a high dielectric constant (30) for ZrO_2 thin film deposited by atomic layer deposition (ALD) [11], and the performance of amorphous phase ZrO_2 thin film has been tested as a better and acceptable phase in TFT device operation [4, 12, 13].

In previous years, ZrO_2 thin films have been deposited by vacuum-based technology, which is a cost ineffective technique and not suitable for large area deposition. On the quest to overcoming this impediment, researchers have focus on the solution-processed techniques as an alternative deposition process, which includes chemical spray pyrolysis (CSP), spin-coating, dip coating, combustion synthesis [4, 6, 14, 15]. The operational simplicity, possibility of depositing uniform film over a large surface area, high degree of freedom in mixing precursor solution, and cost effectiveness distinguishes CSP technique among every other solution process methods. G.Adamopoulos et al., reported a low-

* Corresponding authors.
E-mail addresses: abayomioluwabi@gmail.com, Abayomi.Oluwabi@ttu.ee (A.T. Oluwabi), Ilona.Oja@ttu.ee (I.O. Acik).

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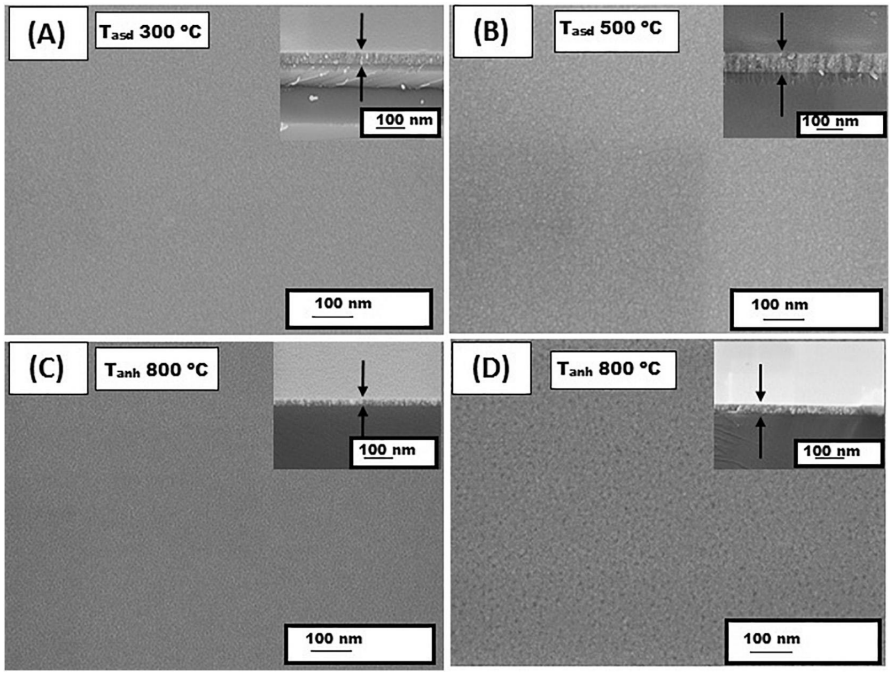

Fig. 1. SEM images of ZrO_2 thin film as-deposited at both (a) 300 °C, and (b) 500 °C from 0.025 M precursor solution; and their morphological changes after annealing at 800 °C in (c), and (d) for both deposition temperatures respectively. Corresponding cross-sectional images in the inset of (a), (b), (c) and (d).

voltage, high-electron mobility TFT based on ZrO_2 dielectric layer, which was fabricated by CSP [16], A. Ortiz et al., deposited cubic-phase ZrO_2 thin film layer by CSP [17], while A. Lintanf-salaun et al., have reported deposition of zirconia film by electro-spray deposition method [5].

Several Zr-precursor sources have been reported such as zirconium oxychloride, zirconium n-propoxide zirconium acetylacetonate etc., however, the zirconium acetylacetate demonstrated better advantage over others because no additional additive (or chelating agent) is needed to stabilize their sensitivity to hydrolysis or pyrolysis [15]. Despite the studies of ZrO_2 as the gate dielectric in TFT, comprehensive study on the effect of deposition temperature on structural and electrical properties of ZrO_2 thin film is still missing.

The aim of this work was to deposit high-k ZrO_2 thin film by CSP method – investigating the influences of deposition and annealing temperature on their structural and electrical properties as the gate dielectric layer in TFT application.

2. Experimental details

2.1. Precursor solution preparation

Zirconium (IV) acetyl acetonate [$Zr(C_5H_7O_2)_4$; Sigma-Aldrich, 98%] was dissolved in methanol (Me-OH, CH_3OH; Sigma-Aldrich, 99%) at room temperature to yield a solution with Zr^{4+} ion concentrations of 0.025 M and 0.05 M; on both cases, the solution was constantly stirred for at least 30 min to ensure complete dissolution of the solute in the solvent.

2.2. Thin film deposition and characterisation

Before the deposition, all substrates (n-type silicon wafer and quartz with 2 × 2 cm^2) were rinsed in an ultrasonic bath at 50 °C with acetone, ethanol, and distilled water for 15 min respectively; and later dried in air. Thin films were deposited by ultrasonic spray pyrolysis (USP) technique, which consist of a nebulizer operated at 1.5 MHz. The nebulized ZrO_2 precursor solution and its resulting aerosol was transported and directed onto a heated quartz and Si-wafer substrates with the aid of a compressed air as carrier gas (flow rate; 3 L/min) and director gas (flow rate; 1 L/min). In order to optimise and develop the deposition process, the deposition time (22 min), spray cycle (20 cycle) and carrier gas parameters were fixed, while the deposition temperature (T_{dep} = 200, 300, 400, 500 °C) and ZrO_2 precursor concentration were varied. The samples were annealed in air for one hour at temperatures (T_{anh}) of 500 °C and 800 °C using Nabertherm L5/11/06D furnace. The films deposited on c-Si substrate were used for electrical, morphological and structural characterisation, while the films on quartz substrate were used for optical studies.

Optical measurements were performed by measuring total transmittance and total reflectance using Jasco-V670 spectrophotometer equipped with an integrating sphere in the wavelength range 200–800 nm. X-ray diffraction (XRD) patterns were obtained using Rigaku Ultima IV diffractometer, which has a silicon stripe detector and a Cu K_α radiation source operated at 40 kV and 40 mA. Surface morphology and elemental composition were studied using ZEISS HR Ultra 55 scanning electron microscope (SEM) with Bruker EDS system ESPRIT 1.8. The acceleration voltage for SEM measurements was 4.0 kV and for EDS was 7.0 kV. Raman spectra were acquired using a micro-Raman spectrometer HORIBA Jobin Yvon Model HR800 with 532 nm laser excitation line, which delivers 5 mW of power at 10 μm laser spot size during measurement. To access the electrical properties of the as-deposited and annealed films, we fabricated a metal-oxide-semiconductor (MOS) device by depositing aluminium contact using Quorum K975X vacuum evaporator on top of ZrO_2 film surface with contact area of 1.7 mm^2, giving a $Si/ZrO_2/Al$ structure. The c-Si wafer was contacted through a carbon paste to ensure ohmic conductivity.

Impedance date were obtained using AUTOLAB PGSTAT30/2 and analysed using the frequency-response analysis software.

3. Results and discussions

3.1. Morphology

Fig. 1, shows the surface and cross-sectional images of 0.025 M ZrO_2 thin film deposited at 300 °C, 500 °C, and their corresponding film morphology after post-deposition annealing treatment at 800 °C. The as-deposited ZrO_2 thin film formed from both deposition temperatures [Fig. 1(a) and (b)] show a flat, uniform and homogenous surface, which implies that the surface of the deposited ZrO_2 film is very dense and smooth. The ZrO_2 film thicknesses obtained from the SEM cross-sectional images [inset of Fig. 1(a) and (b)] show that ZrO_2 films deposited at 300 °C has lower thickness (~65 nm) than ZrO_2 film deposited at 500 °C (~167 nm). However, it is imperative to point out that irrespective of the spray solution concentration and deposition temperature, the ZrO_2 film surface morphology do not change, as they were still very smooth and compacted. The smooth and compact morphology of the film was retained with the absent of cracks or porosity even after post deposition annealing treatment was done, as depicted in Fig. 1(c) and (d). However, the ZrO_2 film thicknesses was reduced to ~51 nm, and ~75 nm for films deposited at 300 °C, and 500 °C in respective order, this could be attributed to densification of film after annealing at 800 °C. To support the surface morphology obtained by SEM analysis, Atomic force microscopy (AFM) analysis was performed (images not shown) only on the ZrO_2 film deposited at 500 °C, we found out that the uniformity obtained by AFM conforms with that of SEM, and the calculated room mean square roughness amounted to ~0.45 nm.

Fig. 2 shows the variation in ZrO_2 thin film thickness as a function of deposition temperature for films deposited from 0.025 M and 0.05 M spray solutions. The film thickness value was obtained from the SEM's cross section taken at three different points on the ZrO_2 film, and the average of the thickness gotten from these points was calculated with their error margins. The ZrO_2 thin film deposited from 0.025 M spray solution has a reduced film thickness (26–167 nm) than in the film deposited from 0.05 M spray solution (132–271 nm), but in both cases, thickness was increasing with deposition temperature. The increase in the observed film thickness with deposition temperature could be related with the zirconium acatylacetate [$Zr(acac)_4$] precursor source being a volatile precursor. Just as it has been reported in the literature by several authors that decomposition mass loss of $Zr(acac)_4$ is temperature dependent [18]. This means that more evaporation of volatile precursor source occurred during low temperature (200 °C) deposition, which led to higher loss of precursor solution, and thinner film was formed. However, as deposition temperature was increased, technically, evaporation of volatile precursor solution was reduced, which resulted in lower loss in precursor solution, and thicker films were formed. The technological consideration of this was to ensure optimisation, which was what we did in order to reduce the ZrO_2 film thickness, as well as showing that it is possible to deposit a thin layer by spray technology by reducing concentration of spray solution to 0.025 M and depositing at temperature from 200 to 500 °C in steps of 100.

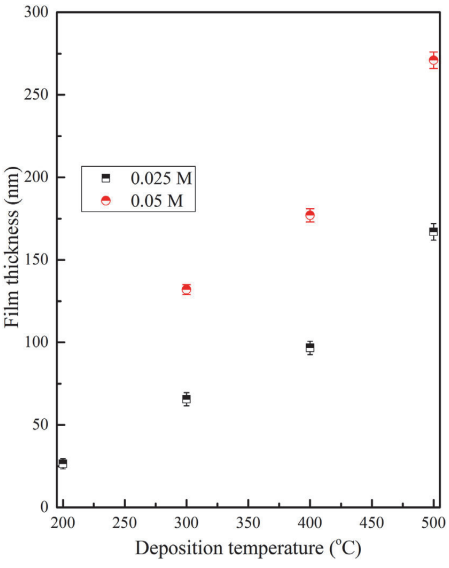

Fig. 2. ZrO_2 thin film thickness as a function of deposition temperature. The thickness value was obtained from SEM's cross-section of the ZrO_2 films deposited with [Zr] = 0.025 M and 0.05 M in the spray solution.

Table 1
O/Zr atomic ratio in the ZrO_2 thin film deposited from a solution with [Zr] = 0.025 M at different deposition temperature (300–500 °C).

O/Zr ratio in the film at different deposition temperature			
Concentration [M]	300 °C	400 °C	500 °C
0.025	4.5	4.0	1.3

According to the EDS results presented in Table 1, the O/Zr ratio is greater than 2 in the ZrO_2 films deposited at low temperature (below 500 °C), while the films deposited at 500 °C exhibited O/Zr ratio lesser than 2. The result explains that the films formed at low temperature are not stoichiometric, while the 500 °C deposited films were nearly stoichiometric. One possible explanation for such behaviour could be due to an incomplete chemical reaction needed for the oxidation of zirconium in the film at low deposition temperature. Similar result has been reported by Ortiz et al. for spray deposited ZrO_2 film [17].

3.2. Structural properties

XRD patterns of the 0.025 M ZrO_2 thin films annealed at different temperatures in air for different deposition temperatures (200, 300, 400, and 500 °C) were shown in Fig. 3. Fig. 3(a), shows the XRD pattern of ZrO_2 thin film as-deposited at 200 °C and annealed in air for 1 h at 500 and 800 °C. According to the result, the film deposited at 200 °C are amorphous, however, after annealing at 800 °C a weak peak centred at $2\theta = 30.35^o$ appeared. Fig. 3(b, c), shows the XRD pattern of ZrO_2 thin film deposited at 300 and 400 °C respectively. The ZrO_2 thin films deposited at both temperatures are also amorphous, but after annealing at 500 °C a broad peak appeared, centred at approximately $2\theta = 30.57^o$ in both films. Furthermore, an additional peak located at $2\theta = 35.42^o$appeared in the ZrO_2 thin film, which was deposited at 400 °C. Owing to the broad nature of the peak centred at "$2\theta = 30.57^o$", differentiating between the t-ZrO_2 and c-ZrO_2 phases by XRD becomes very difficult as they were both positioned at different points within the broad peak. This was confirmed from the ZrO_2 powder X-ray diffraction files (PDF 01-088-1007 and 01-077-3168) and their positions were also marked on the plots. The reason for such an overlap could be due to an internal stress within the film. As the annealing temperature was increased up to 800 °C, the peak centred at $2\theta = 30.57^o$becomes a bit narrow and intense, with the appearance of an extra shouldered peak located at $2\theta = 31.48^o$, which belongs to the m-ZrO_2 phase (PDF 01-080-0966) in the 400 °C deposited film.

Fig. 3(d) shows the XRD pattern of the ZrO_2 thin film deposited at 500 °C. As opposed to the as-deposited ZrO_2 films at lower temperatures, the film shows a broad diffraction peak at $2\theta = 30.57^o$ and another peak at $2\theta = 35.42^o$. The peak remains broad and intense after

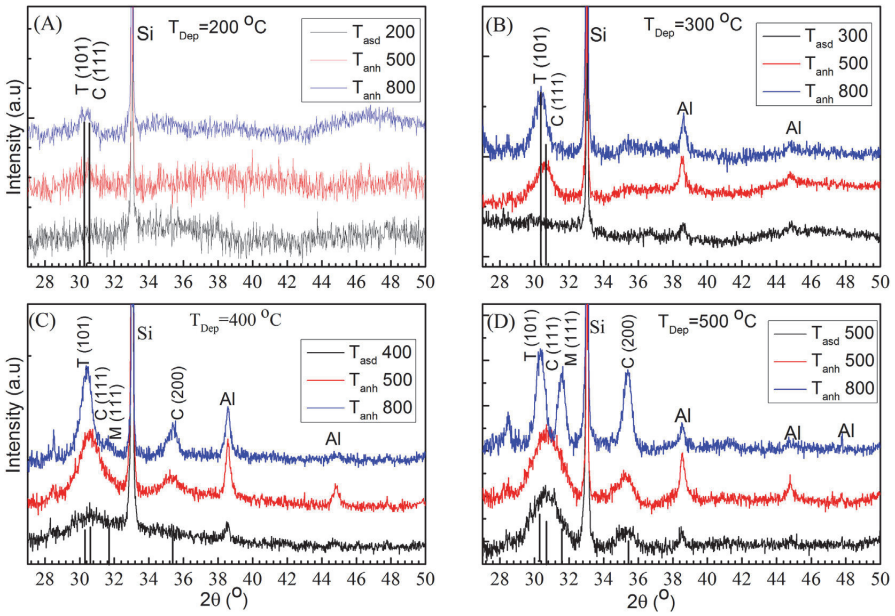

Fig. 3. X-ray diffractograms of ZrO_2 thin films as-deposited ($T_{asd.}$) from 0.025 M precursor solution at (a) 200 °C (b) 300 °C, (c) 400 °C, and (d) 500 °C; and the effect upon annealing (T_{anh}) at both 500 °C and 800 °C, where "T", "C", and "M" denote tetragonal, cubic, and monoclinic phases of ZrO_2 respectively.

annealing in air at 500 °C. However, after annealing at 800 °C the additional peak located at $2\theta = 31.48^o$ which also belongs to the m-ZrO_2 phase (PDF 01-080-0966), became very visible and intense. The formation of the monoclinic phase after annealing at 800 °C could be due to the crystallisation in the ZrO_2 dielectric film because of high processing temperature. However, it is known that the m-ZrO_2 phase is thermodynamically stable at temperature below 1200 °C, similar phase transition has been reported in [10, 11] for ZrO_2 film deposited by spin coating and ALD. The reason for the amorphous nature of the ZrO_2 thin films deposited at low temperature (200, 300, 400 °C) could be related to the fact that the impinging ZrO_2 precursor solution lacks enough surface mobility to produce crystal growth [17]. Similar behaviour of such overlapping between the t-ZrO_2 and c-ZrO_2 has been reported [19].

In order to separate the contributions from the two over lapping t-ZrO_2 and c-ZrO_2 peaks in the broad peak located at $2\theta = 30.35^o$, deconvolution of the diffraction peaks located in the range $29.2^o \leq 2\theta^o \geq 32.0^o$ was carried out after annealing at 800 °C for the ZrO_2 thin films deposited at 200, 300, 400, and 500 °C as depicted in Fig. 4(a, b, c, d). The XRD peak centred at $2\theta = 30.35^o$ was fitted by a Lorenzian distribution into two different fractions centred at "$2\theta = 30.27^o$" and "$2\theta = 30.55^o$" respectively. It is known from the powder diffraction peaks that the peak at $2\theta = 30.27^o$ corresponds to the t-ZrO_2 phase and the peak at "$2\theta = 30.55^o$" correspond to c-ZrO_2 (PDF 01-088-1007, PDF 01-077-3168, and PDF 01-080-0966). It can be clearly seen that the intensity of the c-ZrO_2 fraction decline as the deposition temperature was increased, while the peak intensity of the t-ZrO_2 fraction increases as the deposition temperature of ZrO_2 thin film was increased to 500 °C, indicating that t-ZrO_2 phase was a major fraction in the broad peak. According to Fig. 4 (c) and (d) the m-ZrO_2 phase centred at "$2\theta = 31.48^o$" appeared slightly in the film deposited at 400 °C, which later became clearly visible in the 500 °C deposited film. Some groups have explained such structural transformation to be a

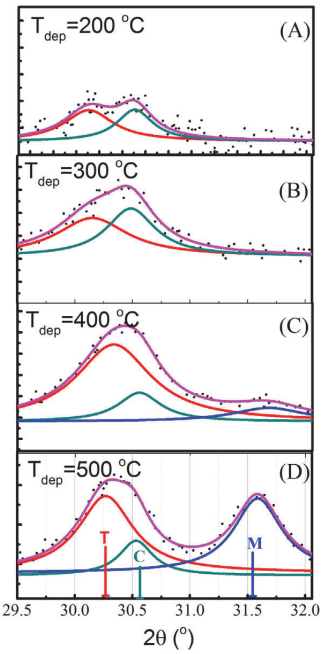

Fig. 4. Deconvolution of XRD peaks at range $29.2^o \leq 2\theta^o \geq 32.0^o$ after annealing (T_{anh}) at 800 °C for ZrO_2 thin films deposited (T_{asd}) at (a) 200 °C, (b) 300 °C, (c) 400 °C, and (d) 500 °C. Note: "T", "C" and "M" denote characteristic peaks from tetragonal, cubic, and monoclinic phases, respectively.

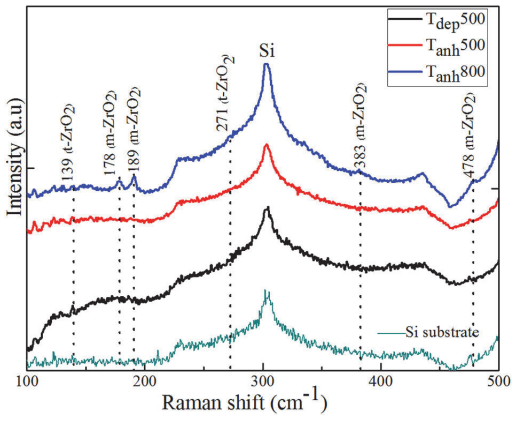

Fig. 5. Raman spectra of ZrO_2 thin film as-deposited (T_{asd}) from 0.025 M precursor solution at 500 °C and annealed (T_{anh}) at 500 °C, and 800 °C. Si denotes the Raman signal from Si substrates.

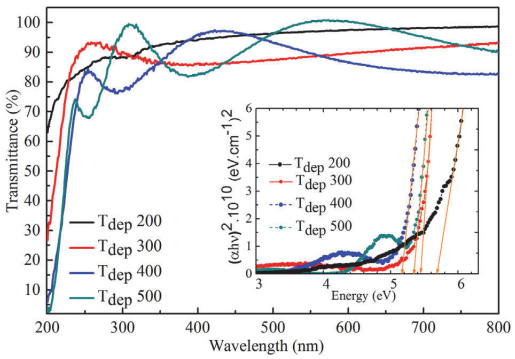

Fig. 6. Optical transmittance spectra of ZrO_2 thin film deposited from 0.025 M precursor solution at various temperatures. The insect shows their corresponding bandgap determination on a Tauc plot.

Table 2
Summary of the changes in the bandgap of ZrO_2 thin films deposited (T_{asd}) from 200 to 500 °C, and after annealing at T_{anh} = 500, 800 °C.

Band gap value (eV) of ZrO_2 (0.025 M films)			
T_{asd} (°C)	As-deposited	T_{anh}-500	T_{anh}-800
200	5.68	5.39	5.25
300	5.43	5.48	5.58
400	5.21	5.58	5.60
500	5.39	5.25	5.14

result of sonication process – thus stabilizing the cubic phase at room temperature [17, 20]. We are considering the dominant phase to be the t-ZrO_2 phase rather than the c-ZrO_2 phase, because amorphous and doped ZrO_2 films synthesized by other solution-based or sol−gel processes have been reported to crystallize into mostly t-ZrO_2 ([21]: references therein,) [22].

Raman spectroscopy – a more precise analytical technique for detecting structural changes was used to study the corresponding structural changes in ZrO_2 thin film upon annealing, the result obtain for the 500 °C deposited film is shown in Fig. 5. The Raman spectrum of the as-deposited ZrO_2 films depict three identifiable peaks, one at ~139 cm^{-1} which belongs to t-ZrO_2 B_{1g} vibration mode, while the other two peaks at ~304 cm^{-1} and ~438 cm^{-1} are from the silicon substrate [19, 21, 23]. The absence of no other peaks corresponding to other ZrO_2 phases shows that the as-deposited films were predominantly tetragonal. As the annealing temperature increases to 500 °C, t-ZrO_2 was sustained in the film, with additional two weak peaks at ~178 cm^{-1} and ~189 cm^{-1} belonging to m- ZrO_2 A_g + B_g and A_g vibration modes respectively [24, 25]. Further annealing at 800 °C, the m-ZrO_2 fractions became visible, while the t-ZrO_2 was sustained in film. The Raman study identified the t-ZrO_2 phase formed in the ZrO_2 films deposited at 500 °C, which later transformed to tetragonal-monoclinic mixed phases upon annealing at higher temperature. The result also corroborate the XRD peak deconvolution result, which demonstrated that t-ZrO_2 phase was the major fraction.

3.3. Optical properties

The optical transmittance spectra of the 0.025 M ZrO_2 thin film deposited at 200, 300, 400, and 500 °C on quartz substrate is shown in Fig. 6. All deposited ZrO_2 thin films demonstrated a high optical transparency, with an average transmittance above 80% in the visible range (400–700 nm), which indicates their applicability in transparent electronics. The absence of interference fringes on the spectra of the films deposited at both 200, and 300 °C show that they are thin and there are no multiple reflections at the air/film and film/substrate interfaces, thereby making it possible for maximum amount of the travelled beam of light to be transmitted through the films [13]. However, as the deposition temperature was increased to 400 °C and later to 500 °C, interference fringes appeared. The obtained increase in the number of interference fringes with deposition temperature suggested an increase in the film thickness, which support the SEM cross-sectional results. Upon annealing at 800 °C (plot not shown), transmittance decreases slightly in all deposited ZrO_2 thin films and the interference fringes remain. The decrease in transmittance can be attributed to the elimination of interstitial oxygen at higher annealing temperatures; however, different groups have reported similar observation on low-temperature solution processed ZrO_2 films [26–29]. The corresponding optical direct bandgap energy of all deposited ZrO_2 thin film was calculated after taken into consideration the reflectivity, absorption coefficient, and film thickness, as these strongly affect the transparency of the film. The interference peaks was eliminated by relating transmittance (T) to absorption coefficient (α) in Eq. (1)

$$T \cong (1 - R)^{-\alpha d} \tag{1}$$

where R is the reflectance and d is the thickness of the ZrO_2 dielectric layer by applying expression (2) on a Tauc plot [30].

$$(\alpha h\nu) = A(h\nu - E_g)^n \tag{2}$$

where $h\nu$ is the photon energy, A is a constant called critical absorption, $n = 0.5$ for direct transition and E_g is the optical band gap. The values of E_g for as-deposited and annealed ZrO_2 films were obtained by plotting $(\alpha h\nu)^2$ against the photon energy ($h\nu$) and extrapolating the linear part of the curve to the energy axis as shown in the inset of Fig. 6. The band gap values of all the as-deposited ZrO_2 film at 200, 300, 400, and 500 °C are 5.68, 5.43, 5.21, and 5.39 eV respectively. The decrease in the energy bandgap is strongly dependent on the structural changes in the ZrO_2 film from amorphous to crystalline phase. However, the summary of the bang gap changes in the 200, 300, 400, and 500 °C deposited ZrO_2 thin films with annealing temperature are presented in Table 2. The band gap energy changes differently in the films just as annealing temperature was increased from 500 to 800 °C, and it could be due to the structurally disordered nature of amorphous materials [28, 29]. Furthermore, just as we have already shown by XRD that a mixture of t-ZrO_2, and m-ZrO_2 with a fraction of c-ZrO_2 phases was formed in the film, and the EDS result showing a nonstoichiometric ZrO_2 films could also be a reason for this behaviour.

In addition to the bandgap results, structural changes in the film has

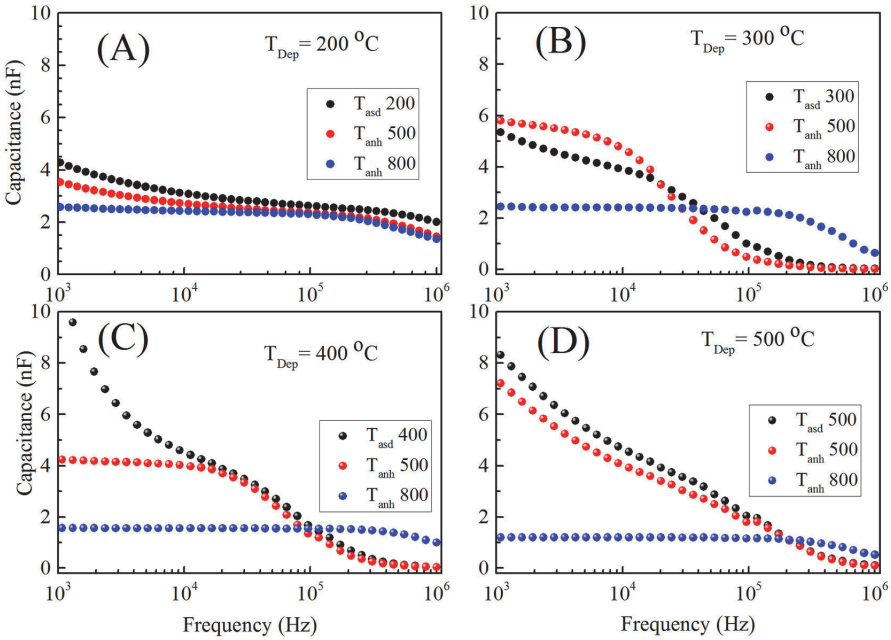

Fig. 7. Capacitance – frequency curves of ZrO_2 thin films as-deposited (T_{asd}) from 0.025 M precursor solution at (a) 200 °C (b) 300 °C, (c) 400 °C, and (d) 500 °C; and the effect upon annealing (T_{anh}) at both 500, and 800 °C.

been the reason mostly stated in the literature for experimentally studied ZrO_2 thin films, because different polymorphs of ZrO_2 have different bandgap values. The E_g value of 5.78 eV (for t-ZrO_2), 5.83 eV (for m-ZrO_2) and 6.10 eV (for c-ZrO_2) have been reported for the bulk form of ZrO_2 [10, 31] and Gao et al. [29] have reported an E_g value of 5.65 eV for ZrO_2 film formed by liquid phase deposition method. While the E_g values we obtained in our study are comparable with most of the reported ones by wet-chemical process [28, 29, 31], and even much higher than reported ones for ZrO_2 thin film prepared by sputtering (4.52–4.67 eV) [32]. Secondly, the general high band gap obtained from our result is a good indication that the spray deposited ZrO_2 film could effectively prevent the conduction of carriers between the semiconductor layer and dielectric layer. It is also worth pointing out that film thickness generally affect the properties of sprayed films [33, 34], however, in this study the effect of film thickness is not obvious in the optical properties of our films. As we experience no significant changes in the transmittance (above 80%) and band gap values (5.56–5.66 eV) of the as-deposited ZrO_2 film (from 0.05 M precursor solution), compared to as-deposited ZrO_2 films (from 0.025 M precursor solution), which are relatively thinner than the former at different deposition temperatures (300, 400, and 500 °C).

3.4. Electrical properties

To characterise the electrical properties of the deposited ZrO_2 thin films, films deposited with a molar solution of 0.025 M were considered, because they were comparably thinner, and they were employed in capacitor with a structure of Al/ZrO_2/n-Si. From the Nyquist plot (not shown), we obtained the resistive property of the film by determining the impedance parallel resistance (Rp) after fitting the plot in the frequency range 100 Hz – 1 MHz with an equivalent circuit consisting of a constant phase element. The Rp of the as-deposited ZrO_2 thin films at 200, 300, 400, and 500 °C were 6.0×10^5, 1.6×10^6, 1.1×10^6, and 8.0×10^5 Ω respectively, which shows that the values of Rp varies differently in the films. This gives an indication that the grain boundary or ionic transportation path in the deposited ZrO_2 capacitors are different at different deposition temperature, and it could be intimately linked with the structural changes within the ZrO_2 film, thus influencing electronic behaviour. A similar behaviour has been reported on ZrO_2 powdered film calcinated at different temperatures [35].

The dispersion curve of the capacitance value for both the as-deposited and annealed ZrO_2 films, which was calculated from the imaginary impedance in the range 1 kHz and 1 MHz are shown in Fig. 8 for all the deposited ZrO_2 thin films. As shown in Fig. 7a, b, c and d, for 200, 300, 400, and 500 °C deposited ZrO_2 film respectively. It was found that irrespective of the deposition temperature, the changes in capacitance value is strongly dependent on frequency in all as-deposited films. After annealing at 500 °C both 300, and 400 °C deposited films shows lesser dependence on frequency, with capacitance value still stable until approximately 10 kHz before decreasing. However, the 200 °C deposited film shows a less dependence on frequency, while the 500 °C film was still strongly dependent on frequency. After 800 °C, capacitance value became strongly independent of frequency irrespective of the ZrO_2 deposition temperature. The observed stability at higher annealing temperature could be due to high densification of film leading elimination of interface capacitance. It is important to point out that the capacitance value did not increase with annealing treatment, however, the increase shown by the 300 °C deposited ZrO_2 film after annealing at 500 °C in Fig. 7b, could be due to interface capacitance. The decreased capacitance at higher temperature could be attributed to the formation of a low permittivity at the film-electrode interface inform of a passive layer, which is capable of causing high concentration of defects, thereby serving as trap-centre for mobile charge carriers [36].

According to equation $C = \varepsilon_0 kA/d$: where, 'C' is capacitance, ε_o is the permittivity of free space, 'k' is the dielectric constant, 'A' is the contact area, 'd' is the ZrO_2 film thickness, the dielectric constant of all the deposited ZrO_2 films were calculated. Fig. 8 shows the dependence of dielectric constant on frequency for all deposited ZrO_2 films after annealing at 800 °C. We found out that irrespective of deposition

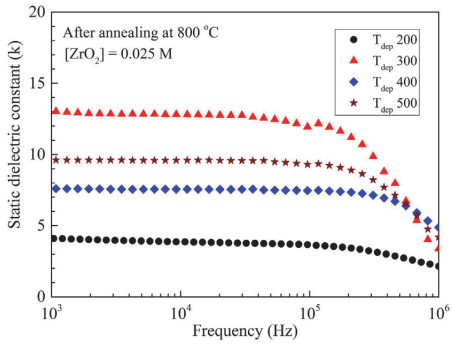

Fig. 8. Frequency dependence of the dielectric constant of various ZrO_2 thin films deposited (T_{asd}) at 200, 300, 400, and 500 °C after annealing (T_{anh}) at 800 °C.

Table 3
Summary of electrical characterisation result of the ZrO_2 capacitors at different deposition temperature after annealing at 800 °C.

Electrical characteristics of ZrO_2 capacitor after annealing at 800 °C				
Deposition temperature °C	Thickness (nm)	Resistance (Ω)	Resistivity (Ω.cm)	Dielectric constant (1 kHz)
200	24	7.6×10^8	5.5×10^{11}	4.3
300	51	1.2×10^7	4.1×10^9	13.0
400	73	1.6×10^8	3.7×10^{10}	7.8
500	120	8.0×10^6	1.1×10^9	9.8

temperature, dielectric constant was strongly independent of frequency. However, its value was also increasing with deposition temperature, which is as a result of structural changes in the film from amorphous to a mixture of monoclinic-tetragonal ZrO_2 phases. ZrO_2 film deposited at 300 °C exhibited the maximum dielectric constant value (13.0) after annealing at 800 °C, same film also exhibited a larger fraction c-ZrO_2 phase, which happens to be a metastable phase with high dielectric constant. Similar changes in electronic behaviour due to structural phase transformation have been reported in the literature by Soliz et al. [35], and Kukli et al. on ZrO_2 film grown by chemical vapour deposition [11].

The summary of the electrical properties of the various ZrO_2 capacitors at different deposition temperature are presented in Table 3. Based on this result, all the deposited ZrO_2 thin films exhibited a stable but different dielectric properties depending on deposition temperature and structural changes in the films, the obtained results are comparable to that of the polycrystalline ZrO_2 films grown from $ZrCl_4$ by ALD, where the dielectric constant did not exceed 20 [11]. Thereby explaining the fact that spray deposited ZrO_2 films can effectively serve as the dielectric layer of thin film transistor, capable of working for low frequency applications.

4. Conclusion

In summary, CSP was successfully adopted for the deposition of a smooth and homogenous zirconium oxide thin film at different deposition temperatures. As a result, the as-deposited ZrO_2 films displayed a high optical transparency above 80% and high optical band gap between 5.21 and 5.68 eV, as well as an amorphous structure at different deposition temperatures (200–500 °C). The phase transformation of ZrO_2 film was predominantly amorphous to tetragonal after annealing at 500 °C with the mixture of both tetragonal and monoclinic phases formed after annealing at 800 °C. Annealing temperature was effective in stabilizing the electrical performance, thus yielding ZrO_2 thin films, which was highly resistive with dielectric constant in the range 4.3–13.0, depending on the deposition temperature (200–500 °C). Based on high optical band gap, high resistive property, and dielectric constant obtained from this study, CSP deposited ZrO_2 thin film may find practical application as the gate dielectric layer in thin film transistor applications.

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Publication III

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Application of ultrasonic sprayed zirconium oxide dielectric in zinc tin oxide-based thin film transistor†

Abayomi T. Oluwabi, *[a] Atanas Katerski, [a] Emanuel Carlos, [b] Rita Branquinho, [b] Arvo Mere, [a] Malle Krunks, [a] Elvira Fortunato, [b] Luis Pereira [b] and Ilona Oja Acik *[a]

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Solution processing of metal oxides has been the focal point of interest for many researchers mainly because of the cost effectiveness and improved properties of metal oxides. However, achieving uniform and high-quality film deposition has been a recurring challenge using various wet-chemical techniques. Herein, we report a fully solution-based fabrication process exploiting both the ultrasonic spray pyrolysis (USP) and spin coating techniques owing to their simplicity, high degree of freedom for mixing metal oxide precursor salt, and larger area deposition. An amorphous zirconium oxide (ZrO_x) dielectric and zinc tin oxide (ZTO) semiconductor were deposited, respectively. The dielectric characteristics of the ZrO_x thin films were accessed by fabricating MIS-devices for the samples deposited at 200 °C and 400 °C, which exhibited a capacitance of 0.35 and 0.67 μF cm^{-2} at 100 kHz and relative permittivity of 8.5 and 22.7, respectively. The ZrO_x thin film was then integrated as the gate dielectric layer in ZTO solution-processed thin film transistors, exhibiting a high electrical performance with low hysteresis (−0.18 V), high on/off current ratio of 10^6 orders of magnitude, saturation mobility of 4.6 cm^2 V s^{-1}, subthreshold slope of 0.25 V dec^{-1}, and operating at a low voltage window of 3 V. Based on these results, the as-fabricated ZTO/ZrO_x TFT opens the potential application of solution-processed transistors for low-cost electronic devices.

1. Introduction

Metal oxide materials are an excellent class of materials with enormous electronic functionalities depending on their area of usefulness, either as an insulator or a semiconductor. Recently metal oxide thin films have attracted significant interest for future electronic applications especially in thin film transistors (TFTs) due to their large-area uniformity, high mobility, good optical transparency in the visible light region, thermal stability, and excellent environmental impact, and they can be produced at low cost.[1–5] However, most of these metal oxide transistors are incorporated into traditional silicon dioxide (SiO_2) dielectrics and they are operated at a high voltage window above 30 V, which hinder their use in low-voltage, smart and portable applications. Since the induced electric field directly corresponds to charge accumulation, replacing the SiO_2 gate dielectric layer of TFTs with a high permittivity (high-κ) material would help accomplish low operation voltage. Furthermore, the scaling-down of electronic devices (below 100 nm) has also called for the need to replace the SiO_2 gate dielectric layer because of the problem of leakage current caused by the quantum tunnelling effect.[2,6] Also, at a lower thickness (10–100 nm), a high-κ gate dielectric can achieve high capacitance, allowing enough charge injection into the active layer of the transistor.[2,7] Several inorganic high-κ oxides such as titanium dioxide (TiO_2), zirconium dioxide (ZrO_2),[8,9] yttrium oxide (Y_2O_3), tantalum oxide (Ta_2O_5),[10,11] hafnium oxide (HfO_2)[12,13] and aluminium oxide (Al_2O_3)[14] have been investigated as attractive candidates to replace the SiO_2 gate dielectric in TFTs. Barquinha *et al.*[11] studied the behaviour and stability of transparent TFTs produced at low temperature using a multicomponent amorphous dielectric material. Their findings revealed that the Ta_2O_5 dielectric can help to improve the device performance based on the fact that this material has the tendency to increase amorphization when mixed with other dielectric materials with lower permittivity.

[a] Laboratory of Thin Film Chemical Technologies, Department of Materials and Environmental Technology, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia. E-mail: abayomioluwabi@gmail.com, ilona.oja@ttu.ee
[b] CENIMAT/i3N Nova School of Science Technilogy (FCT-NOVA), Universidade NOVA de Lisboa and CEMOP/Uninova, Campus de Caparica, 2829-516 Caparica, Portugal

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Among the inorganic high-κ dielectrics, zirconium oxide (ZrO_x) is a desirable gate insulator because bulk ZrO_2 has a high permittivity value ($\sim$25), low leakage current, good thermal stability, adequate band alignment and forms good adhesion with Si-substrates.[3,15] Most importantly, the wide bandgap (5.0–7.8 eV) of ZrO_x is beneficial to suppress charge penetration from the gate electrode and to reduce the generation of charge as a result of the thermal/photoexcitation process.[8] In the past, good quality ZrO_x thin films have been deposited using different methods, for example, atomic layer deposition, sputtering, chemical vapour deposition, and e-beam evaporation,[16] but these methods are very expensive and the growth rate of the thin film is time consuming due to the high vacuum. As opposed to the vacuum-based methods, solution-based method such as spin coating, dip coating, inkjet printing, and spray pyrolysis (SP) offer additional advantages including cost effectiveness, simplicity, high degree of freedom, and larger area of deposition.[5,9,11–19]

Interestingly, among the many wet-chemical methods, ultrasonic spray pyrolysis (USP) is an excellent thin film deposition technique, offering an easy deposition process that gives room for free mixing of precursor solutions at the molecular level before deposition. The cost-effectiveness and non-selective tendency to any substrate of USP distinguish it among several other solution processes. It can easily be scaled up for industrial or commercial fabrication processes and still maintain good film uniformity over a wide area.[18,20] Ortiz *et al.*[21] fabricated a cubic phase of ZrO_x thin film by SP, and Oluwabi *et al.*[17,20] reported the deposition of a ZrO_x thin film by USP. Wang *et al.*[22] reported that a ZrO_x dielectric deposited by SP has a low leakage current (1.2×10^{-7} A cm^{-2}) and a high dielectric breakdown of 9.5 MV cm^{-1} at a substrate temperature below 350 °C.

Moreover, to achieve reliable TFTs, the optimum band offset between the conduction band of the dielectric in an n-type transistor device must be above 1 eV with respect to that of the channel layer in order to reduce the leakage caused by the Schottky effect,[2,23] and ZrO_x can help prevent such effect. Owing to its physical and chemical properties, ZrO_x has been employed in various TFTs, such as MoS, organic, graphene and oxide TFTs.[24–26] As part of the TFT, the channel layer is significant especially in transparent amorphous semiconductors, as suggested by Honoso *et al.*[27] Although solution-processed metal oxide semiconductors, namely, indium zinc oxide (IZO) and indium gallium zinc oxide (IGZO), have been reported as attractive choices of the channel layer, indium-free semiconductors such as zinc tin oxide (ZTO), among others have also attracted significant attention due to the scarcity of naturally available indium resources,[27,29] enabling competitive device performance in comparison with their indium-based counterparts.[28,30] The ZTO semiconductor has good applicability in TFT, but typically requires a high deposition temperature (above 350 °C), and the mechanism of its synthesis has not been fully comprehended. Salgueiro *et al.*[31] reported the role organic solvents in the performance of solution-processed zinc tin oxide (ZTO)-based TFTs. Table 1 presents the reported solution-processed ZrO_x dielectric TFTs. Adamopoulos *et al.*[32] reported a fully solution-processed TFT by SP with a ZrO_x gate dielectric operating at a low voltage with high mobility. Similarly, Xinge *et al.*[22] fabricated a fully solution-processed TFT by spray combustion synthesis (SCS) to achieve a device with high carrier mobility and good reliability. Also, several solution-processed ZrO_x dielectric TFTs have been reported *via* spin coating.[3,25,26,33]

In this work, we demonstrate a combination of ultrasonic spray pyrolysis (USP) and spin coating in the fabrication of high-quality ZrO_x gate dielectrics and ZTO semiconductor, respectively, onto a rigid substrate. To the best of our knowledge, this is the first report of an all-amorphous oxide TFT with low operational voltage. Furthermore, the introduction of USP into our device fabrication process allowed the fabrication of the TFT over a larger area, it improved the properties of the gate dielectric layer and eliminated the problem of pinholes, which have the tendency to jeopardise the final performance of the TFT device. In our previous publication, ZrO_x thin films were tested only as a capacitor, but herein, we further tested a ZrO_x thin film with a thickness of $\sim$30 nm as both a capacitor and gate dielectric in TFTs, which is considerably lower than the thickness of ZrO_x in our previous report.[17,18,20]

2. Experimental details

2.1 Precursor solution preparation

The ZrO_x precursor solution was prepared by dissolving zirconium(IV) acetyl acetonate ($Zr(C_5H_7O_2)_4$; Sigma-Aldrich, 98%) in methanol (Me–OH, CH_3OH; Sigma-Aldrich, 99%) at room

Table 1 Reports on the various solution-processed ZrO_x gate dielectrics at different temperatures in the range of 250 °C $\leq T \leq$ 500 °C tested in TFT devices

Gate dielectric layer				Channel layer				Transistor parameters			
Method	Material	T (°C)	Structure	Method	Material	T (°C)	Structure	Mobility (cm^2 V^{-1} S^{-1})	V_{on} (V)	SS (V dec^{-1})	Ref.
Spin coating	ZrO_x	400	Crystalline	Spin coating	InO_x	300	Crystalline	4.42	0.31	0.07	3
Spin coating	ZrO_x	300	Amorphous	Spin coating	NiO_x	250	Amorphous	4.8	−1.6	0.35	8
Spin coating	ZrO_x	250	Amorphous	Spin coating	InO_x	250	Amorphous	10.0	0	0.1	8
Spin coating	ZrO_x	500	Crystalline	Spin coating	ZTO	500	Crystalline	2.50	1	0.23	34
Spin coating	ZrO_x	350	Amorphous	Spin coating	IZO	250	Amorphous	0.16	0	1.49	26
Spin coating	ZrO_x	400	Crystalline	Spin coating	SnO_x	350	Crystalline	2.50	−0.5	0.30	33
SCS	ZrO_x	350	Amorphous	SCS	IGZO	350	Amorphous	28.5	0.3	—	22
Spray pyrolysis	ZrO_x	400	Crystalline	Spray pyrolysis	ZnO	400	Crystalline	32.0	−1	—	32
Spray pyrolysis	ZrO_x	400	Amorphous	Spin coating	ZTO	350	Amorphous	4.60	−0.9	0.25	Present study

temperature to yield a solution with a Zr^{4+} ion concentration of 0.025 M, and the solution was constantly stirred for at least 30 min to ensure complete dissolution of the solute in the solvent. The solution was completely transparent and remained transparent even after aging.

The zinc oxide precursor solution was prepared by dissolving zinc nitrate salt (zinc nitrate hexahydrate; Sigma-Aldrich, 98%) in 2-methoxyl ethanol (ME) (Roth, 98%). The tin oxide precursor was prepared from a tin chloride source (tin(II) chloride; Sigma-Aldrich, 98%) dissolved in ME solvent. Both the zinc and tin oxides solutions were prepared at a metal ion concentration of 0.1 M and stirred for about 12 h. The ZTO precursor was made by mixing the corresponding zinc and tin oxide precursor solutions in the ratio of 2 : 1. The resulting solution was then stirred for 1 h to ensure homogeneity and finally filtered through a hydrophilic filter with a 0.20 μm pore size before use.

The ZTO precursor solution was characterized by thermogravimetry and differential scanning calorimetry (TG-DSC) analysis of the 0.1 M solution of the ZTO precursor to account for methoxy propanol solvent evaporation events. TG-DSC analyses were performed under an air atmosphere up to 550 °C with a 10 °C min^{-1} heating rate in an aluminium crucible using a simultaneous thermal analyser (TG-DSC – STA 449 F3 Jupiter, Netzsch).

2.2 Thin film deposition and characterisation

Prior to the film deposition, all substrates (p-type silicon wafer and quartz with 2 × 2 cm^2) were rinsed in an ultrasonic bath at 60 °C in acetone, isopropanol, and distilled water for 15 min respectively, and were later dried in air. ZrO_x dielectric films were deposited *via* the ultrasonic spray pyrolysis (USP) technique as shown in Fig. 1a, and the deposition parameters have been reported in.[17] For the purpose of this study, the films were deposited at both 200 °C and 400 °C without further annealing.

The film structure was assessed by glancing angle X-ray diffraction (GAXRD) performed on an X'Pert PRO PANalytical powder diffractometer using Cu Kα line radiation (λ = 1.540598 Å) with the angle of incidence of the X-ray beam fixed at 0.9°. The thickness of ZTO and ZrO_x was obtained by spectroscopic ellipsometry measurement in the energy range of 1.5–6.0 eV with an incident angle of 70° using a Jobin Yvon Uvisel system. Total transmittance spectra were obtained using a Jasco-V670 spectrophotometer equipped with an integrating sphere in the wavelength range of 200–800 nm, which was later used to calculate the optical bandgap of the ZrO_x dielectric at different deposition temperatures. Surface morphology was studied using a ZEISS HR Ultra 55 scanning electron microscope (SEM). The acceleration voltage for SEM measurements was 4.0 kV. Attenuated total reflectance (ATR) Fourier transform infrared spectroscopic characterization of the thin films deposited on silicon substrates was performed in the range of 4500–560 cm^{-1}.

2.3 Fabrication of ZrO_x MIS devices

The dielectric characteristics of ZrO_x were accessed through metal–insulator–semiconductor (MIS) capacitors by depositing the ZrO_x thin film onto p-type silicon substrates (1–3 Ω cm), as described above. Al gate electrodes (80 nm thick) with an area of 8.0 × 10^{-3} cm^2 were deposited by thermal evaporation *via* a shadow mask, and a similar thickness of Al film was also deposited on the back of the silicon wafer to improve the ohmic conductivity. Electrical characterization was performed by measuring both the current–voltage (*I*–*V*) and capacitance–voltage (*C*–*V*) characteristics of the devices using a semiconductor device analyser (Keysight 1500A) connected to a Casecade M150 microprobe station inside a dark box at room temperature with humidity between 30% and 40%. The capacitance–frequency (*C*–*F*) curve was obtained from the impedance data measured in the range of 10 Hz to 1 MHz using an AUTOLAB PGSTAT30/2.

2.4 Fabrication of ZrO_x TFT devices

TFTs were produced in a staggered bottom-gate, top-contact architecture by depositing the ZrO_x thin films onto p-type silicon substrates, as described above and shown in Fig. 1a and b. The ZTO active layer was later deposited by spin coating (using a Laurell Technologies instrument). Four layers of 0.1 M

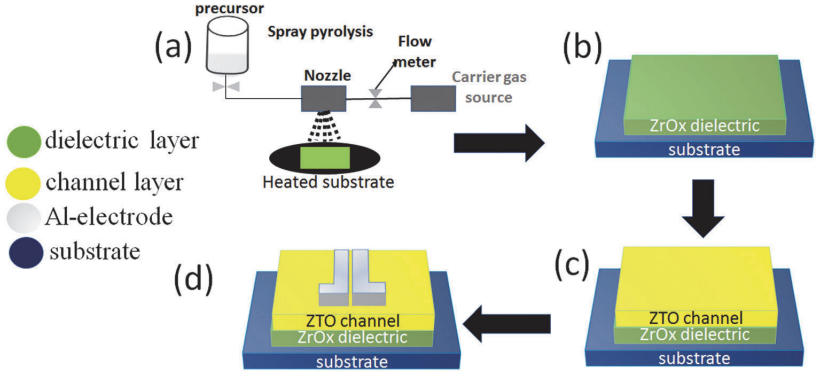

Fig. 1 Fabrication stages of ZrO_x gate dielectric TFT devices with ZTO semiconductor layer: (a) spraying of ZrO_x precursor solution, (b) deposition of ZrO_x dielectric onto Si-substrate, (c) spin coating ZTO semiconductor onto ZrO_x/Si, and (d) aluminium electrode deposition, yielding a TFT device with the channel width (*W*) of 1400 μm and length of 100 μm (*W*/*L* = 14).

ZTO precursor solution was spun for 35 s at 2000 rpm onto the ZrO_x thin films and annealed at 150 °C, 250 °C, and 350 °C for 30 min (Fig. 1c). Finally, the source and drain aluminum electrodes (100 nm thick) were deposited by thermal evaporation *via* a shadow mask onto the annealed films (Fig. 1d). The output and the transfer characteristics of the devices were obtained in continuous mode with both back and forth sweeps recorded in ambient conditions inside a Faraday cage (in dark conditions) using a semiconductor parameter analyzer (Agilent 4155C).

The saturation mobility (μ_{sat}) was determined from the following equation:[14]

$$I_d = \left(\frac{C_{ZrO} B \mu_{sat}}{2L}\right)(V_G - V_T)^2 \quad (1)$$

where C_{ZrO} is the gate dielectric capacitance per unit area, B and L are the channel width and length, respectively, V_G is the gate voltage, and V_T is the threshold voltage, which was determined in the saturation regime by fitting of the curve of $I_d^{1/2}$ *versus* V_G and extrapolating the linear part to V_G axis.

3. Results and discussion

3.1 ZrO_x dielectric thin film characterisation

The surface morphology of the ZrO_x dielectric films deposited at different temperatures was observed *via* atomic force microscope (AFM, Fig. 2a and c) and SEM analysis (Fig. 2b and d). The films surface roughness was estimated from the AFM height profile and scanned through an area of 1 μm × 1 μm. The ZrO_x films deposited at 200 °C (Fig. 2a) demonstrated a higher surface roughness with a root mean square (RMS) roughness value of 0.33 nm compared with that deposited at 400 °C with an RMS value of 0.29 nm. The decrease in the film surface roughness at higher temperature could be due to film densification, which was aided by the decomposition of volatile organic precursor during the spray pyrolysis process. According to the TG/DTG/DTA results of Oja *et al.*[35,36] for spray-deposited TiO_2 dielectrics, the complete decomposition of volatile organic complexes occurs above 400 °C. In addition, the deposited ZrO_x films were structurally amorphous

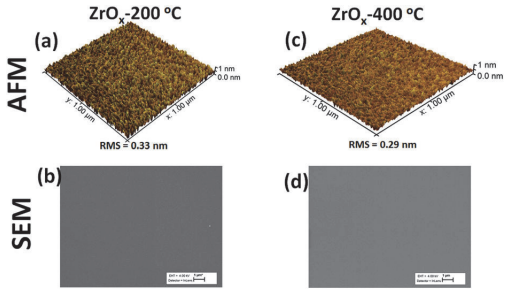

Fig. 2 Surface morphology of the solution-processed ZrO_x dielectric films. AFM deflection images of the as-deposited ZrO_x dielectric at both (a) 200 °C, and (c) 400 °C; and their corresponding SEM images at (b) 200 °C and (d) 400 °C on an Si-substrate.

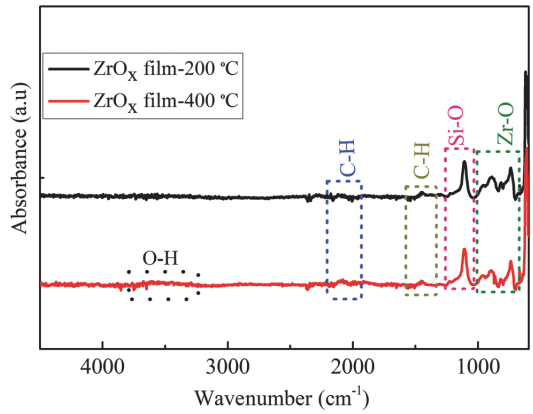

Fig. 3 FTIR ATR absorbance spectra of ZrO_x dielectric films deposited at 200 °C and 400 °C.

(see Fig. S1 in the ESI†) as confirmed by X-ray diffraction. Furthermore, as depicted by the SEM images (Fig. 2b and d), the ZrO_x dielectric films were uniform, compact, and very smooth.

The FT-IR spectra of the deposited ZrO_x dielectric thin films deposited at 200 °C and 400 °C on Si-substrates is shown in Fig. 3. All the films show a sharp infrared absorbance peak at 1120 cm^{-1}, which can be ascribed to the optical stretching of the Si–O bond from the Si-substrate. The asymmetric CH_3 deformation vibration centred at 1430 cm^{-1} was observed and a slightly broad peak at 3545 cm^{-1} associated with the bending and stretching vibrational bond of the native O–H group from the adsorbed water molecules on the surface of the ZrO_x dielectric was also observed.[13]

Furthermore, a weak absorbance peak centred at 2110 cm^{-1} corresponding to the C–H bond stretching was observed for both films, which can be ascribed to the organic residues from the ZrO_x precursor reagent; thereby suggesting the presence of organic residue in the ZrO_x dielectric film network even after annealing at 400 °C. Both the ZrO_x dielectric films deposited at 200 °C and 400 °C exhibited infrared absorption peaks centred at 880, 750, and 945 cm^{-1}, which are related to the metal oxygen bond (Zr–O) stretching.[13,31]

The optical transmittance of the as-deposited ZrO_x dielectric film at 200 °C and 400 °C is shown in Fig. 4a. The absence of interference fringes on the transmittance spectra indicates that the films are very thin, which was later confirmed by spectroscopic ellipsometry (~20 nm and ~30 nm thick for the 200 °C and 400 °C deposited films, respectively). It was observed that both deposited ZrO_x dielectric films demonstrated a high optical transparency in the visible region (350–700 nm) with a percentage transmittance of above 80%.

In addition, the transmittance decreased with an increase in the deposition temperature, which can be attributed to the changes in the film microstructure, although it was impossible to be detected by XRD since the films are amorphous according to the XRD result (ESI† S1, XRD). Another reason may be because of the removal of oxygen vacancies in the film when they were

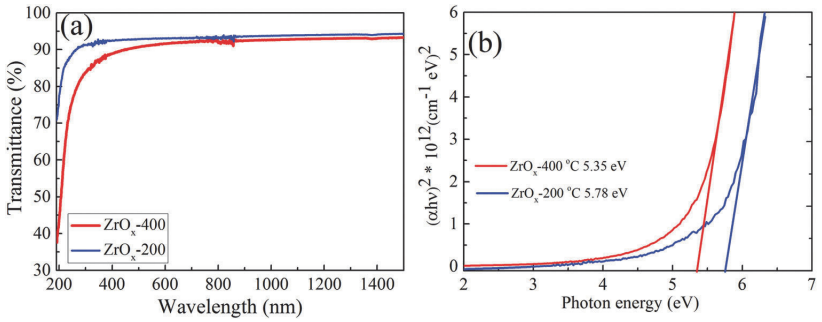

Fig. 4 (a) Total transmittance spectra of the ZrO_x dielectric film deposited at 200 °C and 400 °C and (b) corresponding bandgap extrapolation in the Tauc plots.

grown at 400 °C. A similar tendency was reported in our previous publication.[8,17] The optical bandgap (E_g) was estimated by fitting the transmittance spectra to the standard Tauc plot,[37] which was determined to be 5.78 and 5.35 eV for the ZrO_x films deposited at 200 °C and 400 °C, respectively (Fig. 4b). The reduction in the E_g value with the deposition temperature can be attributed to many reasons, including microstructural changes within the film, the presence of localised defects within the ZrO_x band structure thereby causing a reduction in the E_g value, and the disordered nature of the amorphous materials.[3,8,17] Nevertheless, the E_g values being generally high above 5 eV is a good indication that the spray-deposited ZrO_x dielectric film would provide enough barrier needed to prevent carrier conduction between the active layer and the gate dielectric layer of TFT.

3.2. ZrO_x MIS characterisation

To demonstrate the insulating property of the sprayed ZrO_x dielectric thin film, an MIS-capacitor with the Al/p-Si/ZrO_x/Al structure was fabricated. The capacitance–frequency (C–F) dispersion curves in Fig. 5a show that the area capacitance at 100 kHz for the ZrO_x dielectric film deposited 200 °C and 400 °C is 0.37, 0.67 μF cm^{-2}, corresponding to a permittivity of 8.4

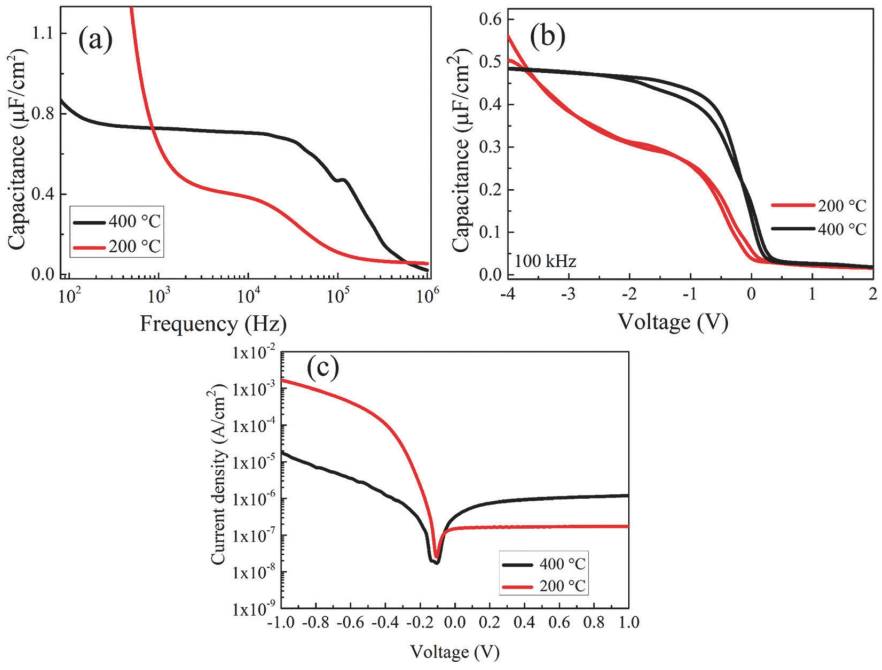

Fig. 5 (a) Capacitance–frequency curve, (b) capacitance–voltage, and (c) current–voltage characteristics of Al/p-type Si/ZrO_x/Al MIS capacitors with the ZrO_x films obtained at various deposition temperatures.

and 22.7, respectively. The observed increase in the permittivity value of the 400 °C deposited film can be due to the densification of the film at a higher temperature. An important point is that the observed increase in the dispersion curve for ZrO_x deposited at 200 °C as the frequency decreases may be an indication that there is another dielectric relaxation mechanism at lower frequencies related with mobile ionic species as a result of the incomplete decomposition of the ZrO_x precursors at a low temperature.

Fig. 5b shows the capacitance–voltage curves for both the 200 °C and 400 °C deposited ZrO_x dielectric films. The voltage bias was carried in the forward and reverse sweep at 100 kHz, to ascertain the stability of the MIS capacitor. When the ZrO_x film was deposited at 400 °C, there was a saturation of the capacitance in the accumulation regime, which did not occur for that at 200 °C due to the leakage current (as confirmed in Fig. 5c). Moreover, and contrary to that for the film deposited at 200 °C, there are no bumps when reaching accumulation, indicating a reduction in the density of electron trap sites at the interface between ZrO_x–silicon. Depending on the type of shift in the *C–V* curve, an understanding about the charge trapping/de-trapping within the oxide band structure can be obtianed.[14] In our case, the device produced at 200 °C showed that a more negative bias was needed to complete accumulation due to electron trapping, corroborating the *C–F* results.

Fig. 5c shows the plot of the current density against voltage for the 200 °C, and 400 °C deposited ZrO_x dielectrics. From the plot, the leakage behaviour of the ZrO_x gate dielectric films was estimated from in the reverse bias regime at 1 V. It was observed that the ZrO_x deposited at 400 °C has a lower leakage current of 3.56×10^{-6} A cm^{-2} that is lower than the one measured for the 200 °C deposited dielectric film (4.26×10^{-4} A cm^{-2}). The observed decrease in the leakage current is 2 orders of magnitude and can be attributed to the decomposition of volatile organic compounds in the film at higher temperature, resulting in the improvement of the density of the dielectric films.[8,17]

3.3 ZTO semiconductor thin film formation and characterisation

The semiconductor, ZTO, film was formed *via* a simple sol–gel synthesis approach, and the ZTO precursor is a mixture of both Zn-nitrate and Sn-chloride salts and dispersed in ME at a mole ratio of 2 : 1 at room temperature. The thermal gravimetry and differential calorimetry analyses for both the Zn–nitrate and the Sn–chloride precursor solution were studied and are presented in Fig. S2(a) and (b), ESI,† respectively. The degradation of the Zn–nitrate precursor is very fast with almost 80% degradation below 200 °C, while the degradation of the Sn-precursor is fairly slow requiring a minimum temperature of 400 °C to complete the decomposition process. On the other hand, the gravimetric and differential scanning calorimetry analyses for the ZTO precursor solution is presented in Fig. S3(a and b), respectively, and the total residual mass loss for the decomposition process from 20–550 °C is 70.28%. Thus, to obtain the desired ZTO thin film phase, the reaction is expected to occur at a much higher temperature (preferably, above 400 °C).

The FTIR spectrum of the ZTO precursor solution made from the ME solution is presented in [S5] and the FTIR spectra of the ZTO semiconductor thin films produced from this solution at various annealing temperatures are presented in Fig. 6a. All the ZTO semiconductor films show a sharp infrared absorbance peak at 1120 cm^{-1}, which can be related to the optical stretching of the Si–O bond from the Si-substrate, and they equally exhibited infrared absorption peaks centred at 880, 750, and 945 cm^{-1}, corresponding to the metal oxide bond (Zn–O and Sn–O) stretching.[13,31] This result indicates that the ZTO films were composed of some metal oxygen bonds and organic residues. The microstructures of the ZTO thin films at various annealing temperatures were measured using XRD, and the results are shown in Fig. 6b. The absence of obvious peaks in the X-ray diffraction patterns demonstrate the amorphous nature of the ZTO thin films.

3.4 Electrical properties of solution-processed TFTs based on SiO_2 gate dielectric

Based on the above discussion on the properties of the ZrO_x thin film, it can be inferred that the films deposited at a higher temperature displayed better dielectric characteristics. Nevertheless, to juxtapose this behaviour in TFTs, we first investigated the feasibility of a solution-processed ZTO active layer in a bottom gate and top source/drain contact architecture.

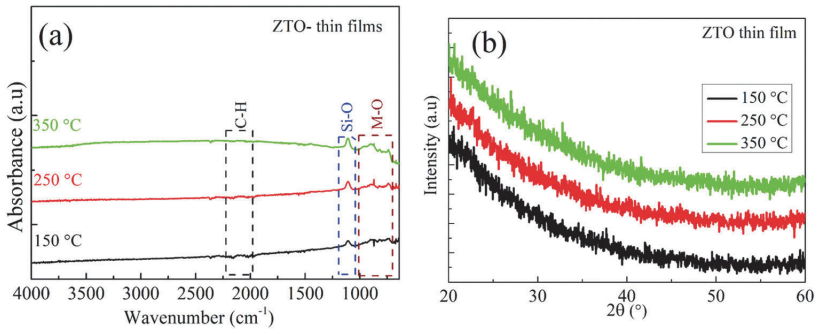

Fig. 6 (a) FTIR spectra of the ZTO semiconductor thin films annealed at various temperatures. (b) XRD patterns of the ZTO semiconductor thin films annealed at various temperatures.

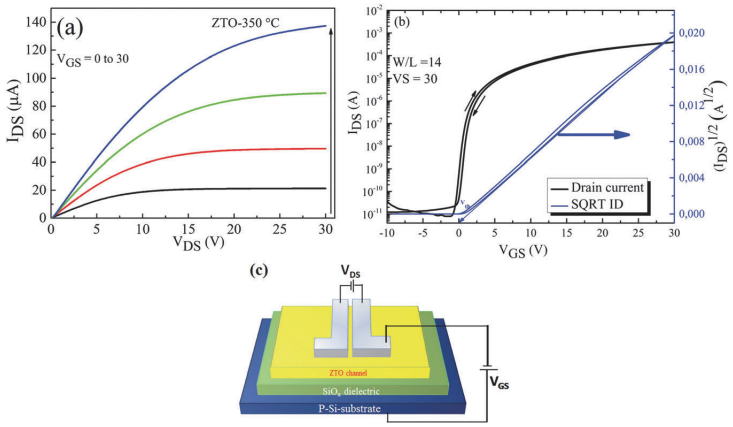

Fig. 7 TFT characteristics of the ZTO-350/SiO_2 device. (a) Output, and (b) transfer performance; while a schematic representation of the device structure is shown in (c).

The conventional SiO_2/Si-substrate was used as the gate electrode and gate dielectric because of its reliability and low defect density. Fig. 7 shows the output and the transfer characteristics of the solution-processed ZTO-TFT and scheme of the TFT architecture. The output curve of the ZTO-TFT after annealing at 350 °C shows that the device has a clear distinction between the linear and the saturation regimes (Fig. 7a). The absence of overcrowding data points at the low drain voltage region demonstrates the excellent ohmic contact between the Al electrode and the ZTO channel layer. The TFT trans-conduction characteristics are depicted in Fig. 7b, which showed very little hysteresis during the sweep of the gate voltage in both the forward and reverse directions. The result of the saturation mobility was extracted by fitting the transconductance curve to eqn (1), and the statistical summary of both the TFT and MIS devices is presented in Table S1 (ESI†). The calculated saturation mobility (μ_{sat}) is ~0.5 cm^2 V^{-1} s^{-1}, the threshold voltage (V_{th}) is 1.3 V, the on–off current ratio (I_{on}/I_{off}) is up to 10^8, the sub-threshold swing (S.S.) is 760 mV per decade, the hysteresis is −0.4 V, and the on-voltage (V_{on}) is −0.5 V. The extracted device parameters are also summarised in Table 2. The SS value was used to estimate the density of the interface state (D_{it}) of 1.1 × 10^{12} cm^2 for the ZTO-TFT device using eqn (2):

$$D_{it} = \left[\frac{SS\log(e)}{kT/q} - 1\right]\frac{C_i}{q} \quad (2)$$

where k, T, and q are Boltzmann's constant, absolute temperature, and electronic charge, respectively. However, the Dit value is significantly lower as opposed to what has been reported for ZTO-TFTs fabricated using other techniques.[38] It can also the attributed to the ZTO thin film deposition technique yielding good quality film (Fig. S4 in the ESI†) at a high annealing temperature, which aided the good adhesion between the ZTO/SiO_2 interface.[39]

On the contrary, the behaviour of ZTO-TFT produced after annealing at 250 °C (see Fig. S6 in the ESI†) is of poor quality and the device exhibited a huge hysteresis voltage and high V_{th} of about 8 V, meaning that more power will be required to turn-on the device. This can be due to the low quality of the channel layer at a lower temperature because the ZTO semiconductor layer at 250 °C has more organic residue compared to that at 350 °C. This assumption is consistent with the observation from the TG analysis of the Zn(II) precursor compared with the Sn(II) precursor (see Fig. S1a and b in the ESI†). According to the study by Sanctis *et al.*,[28] the degree of oxidation of the ZTO semiconducting layer plays a crucial role in the performance of ZTO-based TFTs because of the of oxygen defects arising from the highly defective SnO_2 within the ZTO semiconductor layer.

3.5 Electrical properties of solution-processed TFT based on ZrO_x gate dielectric

The electrical performance of the TFTs presented in the previous section proved that solution-processed ZTO can be adopted as the active layer in TFTs. Here, we demonstrate the applicability of the ZrO_x dielectric as a likely replacement for the SiO_2 dielectric layer in improving the performance of ZTO-based TFTs. To avoid the problem of charge trapping at the interface between the dielectric and channel layers, only the ZrO_x thin film processed at 400 °C was tested, and to reduce the inaccuracy when

Table 2 Summary of the TFT parameters for both the ZTO/SiO_2 and ZTO/ZrO_x devices

Device	V_{on} (V)	I_{on}/I_{off}	Sat. mob. (cm^2 V^{-1} s^{-1})	V_{Th} (V)	SS (V dec^{-1})	Hysteresis (V)	D_{it} (cm^{-2})
ZTO-250/SiO_x	7.80 ± 0.2	~10^4	—	~8.45	—	1.71 ± 0.5	—
ZTO-350/SiO_x	−0.30 ± 0.5	~10^8	0.47 ± 0.01	1.32 ± 0.08	0.76 ± 0.01	−0.37 ± 0.08	1.1 × 10^{12}
ZTO-350/ZrO_x-400	−0.94 ± 0.04	~10^6	4.61 ± 0.06	0.03 ± 0.02	0.25 ± 0.01	−0.18 ± 0.06	5.7 × 10^{12}

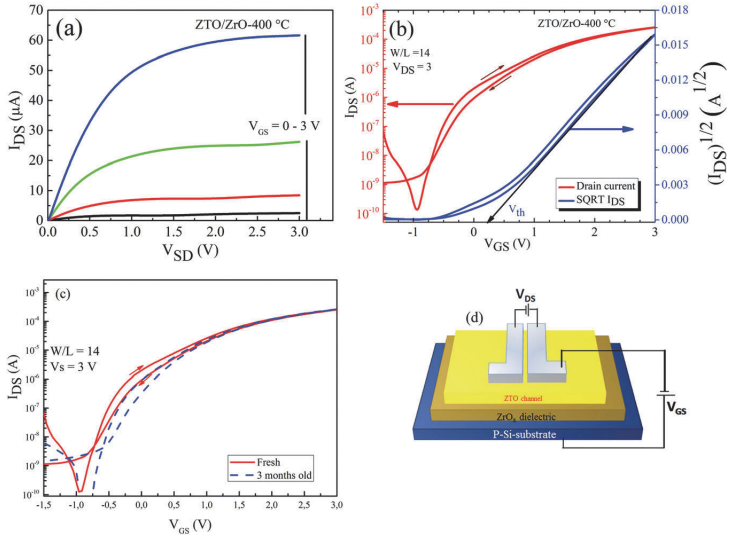

Fig. 8 TFT characteristics of ZTO-350/ZrO_x-400 devices. (a) Output, and (b) transfer performance; while (c) transfer characteristic of both the freshly made device and the performance after 3 months shelf-life, and the schematic representation of the device structure is shown in (d).

calculating the mobility and SS since the devices are characterised in a quasi-static regime, the capacitance (C = 1.0 μF cm^{-2}) of ZrO_x was calculated at 50 Hz. The typical transfer and output characteristics of the as-fabricated TFTs and the corresponding device schematic are shown Fig. 8a–d. It can be seen in Fig. 8a that again, the device exhibited a clear distinction between the linear and saturation regimes and no current crowding was observed. Fig. 8b shows the typical transfer characteristics of the ZrO_x-TFT device, and it can be seen that the off-state (I_{off}) current increased with a decrease in the gate voltage. This observation is typical of most high-κ metal oxide derivatives, which has been reported to be caused by their relative narrow bandgap.[10,11] Contrary to the ZTO/SiO_2 TFTs, the ZTO/ZrO_x TFT demonstrated a significant reduction in its operation voltage window (between −1 V and 3 V), higher saturation mobility of 4.6 cm^2 V^{-1} s^{-1}, I_{on}/I_{off} ratio of 10^6, small SS value of 250 mV per decade, and a turn-on voltage of −0.9 V. The improvement in the transistor parameters is mainly due to the higher permittivity of the ZrO_x thin film compared with that of the SiO_2 dielectric. The ZrO_x-based TFT dissipated a much lower power (0.3 mW) than TFT based on the SiO_2 dielectric (30 mW).[8]

In our case, the clockwise hysteresis was estimated to be −0.1 V, which means that electron trapping occurred during forward sweeping. During the reverse gate voltage sweeping, these states remain filled until the trapped electrons were thermally de-trapped.[3] Moreover, D_{it} is very important for device stability and charge carrier mobility, which was estimated to be 5.7 × 10^{12} cm^{-2} for the ZTO/ZrO_x TFT. These results show that we obtained a good interface between the ZrO_x gate dielectric and the ZTO channel layer. Also, despite being larger than that using SiO_2 as the dielectric, the D_{it} value is comparable to the reported values for solution-processed ZrO_x TFTs (1 × 10^{12} cm^{-2}),[8,38] and much lower than that for sputtered TFT devices.[40] The improved performance is believed to have originated from the thin and amorphous structure of the ZrO_x gate dielectric, providing a smooth interface between the ZrO_x dielectric and ZTO semiconductor layer.

The aging stability of the fabricated ZTO/ZrO_x TFT device was accessed by re-measuring its performance after 3 months of storage without encapsulation or any specific storage conditions (Fig. 8c). The device showed excellent stability with time and no significant changes in its electrical performance was observed, indicating it demonstrates an effective performance towards cost-effective and low operation voltage solution-based oxide electronics. This may be as a result of the slow sensitivity of the active ZTO layer to native contaminants such as dust and moisture, which have a tendency of increasing the surface energy of semiconductor materials. Moreover, the degradation of the active layer of metal oxide-based TFTs is mostly due their sensitivity to surface adsorbates such as H_2O molecules and humidity, which act as trap sites for mobile carriers, and therefore cause depletion of the active layer material.[41] Another reason for the shelf-life stability of the device can be due to the *in situ* deposition of the ZTO layer at high temperature, which led to the formation of a ZTO film with less defects, surface adsorbed species, and organic contaminants. Riedl *et al.*[41] demonstrated that *in situ* annealing can also be used to improve the stress stability of ALD-processed ZTO-based TFTs.

4. Conclusions

In summary, we successfully reported the solution processing of ZrO_x thin films *via* a low-cost ultrasonic spray pyrolysis method

and explored their applicability as a gate dielectric layer in TFTs. The fabricated ZrO_x films were uniform, smooth, amorphous, and optically transparent with an E_g value of 5.35 eV. The ZrO_x film exhibited a relative permittivity value of 22.7 (50 Hz) and leakage current of 3.56×10^{-6} A cm^{-2} at a bias of 1 V. The optimized ZTO/SiO_2 TFTs annealed at 350 °C exhibited excellent electrical performances, including a saturation mobility of 0.5 cm^2 V^{-1} s^{-1}, a high I_{on}/I_{off} value of 10^8, a threshold voltage of 1.32 V, and a small sub-threshold swing value of 0.76 V dec^{-1}. The SiO_2 gate dielectric was replaced by the sprayed-deposited ZrO_x dielectric to achieve a cost-effective and fully solution-processed device. The ZTO/ZrO_x TFTs exhibited a low operation voltage of 3 V with optimized performances, including a high saturation mobility of 4.6 cm^2 V^{-1} s^{-1}, a low threshold voltage of 0.03 V, appreciable I_{on}/I_{off} current ratio of 10^6, and a small sub-threshold swing of 0.25 V dec^{-1}. These results demonstrate that the use of a very simple technique, such as both ultrasonic spray pyrolysis and spin coating for the sequential deposition of high-κ gate dielectrics and metal oxide semiconductors represents a significant step towards the development of low-cost, large-area oxide TFTs.

Conflicts of interest

There are no conflicts to declare.

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Publication IV

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Influence of Post-UV/Ozone Treatment of Ultrasonic-Sprayed Zirconium Oxide Dielectric Films for a Low-Temperature Oxide Thin Film Transistor

Abayomi Titilope Oluwabi [1,*], Diana Gaspar [2], Atanas Katerski [1], Arvo Mere [1], Malle Krunks [1], Luis Pereira [2] and Ilona Oja Acik [1,*]

[1] Laboratory of Thin Film Chemical Technologies, Department of Materials and Environmental Technology, Tallinn University of Technology, Ehitajate tee 5, 19086 Tallinn, Estonia; atanas.katerski@ttu.ee (A.K.); arvo.mere@ttu.ee (A.M.); malle.krunks@ttu.ee (M.K.)

[2] i3N/CENIMAT, Department of Materials Science School of Science and Technology, FCT-NOVA, Universidade NOVA de Lisboa and CEMOP/UNINOVA, Campus de Caparica, 2829-516 Caparica, Portugal; dfpgaspar@gmail.com (D.G.); imnp@fct.uni.pt (L.P.)

* Correspondence: abayomi.oluwabi@ttu.ee (A.T.O.); Ilona.Oja@ttu.ee (I.O.A.); Tel.: +372-5671-0366 (A.T.O.); +372-620-3369 (I.O.A.)

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Abstract: Solution-processed metal oxides require a great deal of thermal budget in order to achieve the desired film properties. Here, we show that the deposition temperature of sprayed zirconium oxide (ZrO_x) thin film can be lowered by exposing the film surface to an ultraviolet (UV) ozone treatment at room temperature. Atomic force microscopy reveals a smooth and uniform film with the root mean square roughness reduced from ~ 0.63 nm (UVO-O) to ~ 0.28 nm (UVO-120) in the UV–ozone treated ZrO_x films. X-ray photoelectron spectroscopy analysis indicates the formation of a Zr–O network on the surface film, and oxygen vacancy is reduced in the ZrO_x lattice by increasing the UV–ozone treatment time. The leakage current density in Al/ZrOx/p-Si structure was reduced by three orders of magnitude by increasing the UV-ozone exposure time, while the capacitance was in the range 290–266 nF/cm^2, corresponding to a relative permittivity (k) in the range 5.8–6.6 at 1 kHz. An indium gallium zinc oxide (IGZO)-based thin film transistor, employing a UV-treated ZrO_x gate dielectric deposited at 200 °C, exhibits negligible hysteresis, an I_{on}/I_{off} ratio of 10^4, a saturation mobility of 8.4 cm^2 V^{-1}S^{-1}, a subthreshold slope of 0.21 V.dec^{-1}, and a V_{on} of 0.02 V. These results demonstrate the potentiality of low-temperature sprayed amorphous ZrO_x to be applied as a dielectric in flexible and low-power-consumption oxide electronics.

Keywords: spray pyrolysis; low-temperature; zirconium oxide; Indium-Gallium-Zinc-Oxide; UV-ozone; high-κ dielectrics; thin film transistor

1. Introduction

Zirconium oxide (ZrO_x) has gained a large amount of attention in different applications such as thin film transistors (TFT) [1,2], sensors [3,4], display technology [1], and memory technology [5,6] due to its unique thermal stability, optical, and electronic properties. Additionally, in TFT applications, ZrO_x has been employed as a plausible replacement for the silicon oxide dielectric layer, owing to its high permittivity (κ) (~25), and wide bandgap (5.1–7.8 eV) [7–9]. However, the production of ZrO_x dielectrics by a wet chemical process is still slow because of high processing temperature (above 400 °C), arising from the need to decompose the organic moiety from the film's matrix, which in turn increases the thermal budget [10,11].

Different authors have reported on the solution-processing technologies that can be used to produce ZrO_x dielectric films and the need for post deposition heat treatment in order to achieve a good-quality film that will yield promising electrical performance in TFTs [12–15]. For instance, according to Park et al., a ZrO_x dielectric was synthesized by adding hydrogen peroxide, and the fabricated dielectric film was tested as a TFT, which demonstrated a low leakage current with high breakdown strength (3.4 MV/cm) after film treatment at 350 °C [12]. Lee et al. [13] fabricated a solution-processed ZrO_x TFT on a glass substrate; however, the desired carrier mobility (~25 cm^2/Vs) was achieved at a high annealing temperature of 500 °C. Ha and co-workers [14] employed solution-processed ZrO_x as a gate dielectric layer of Zinc Tin Oxide (ZTO)-TFTs, which demonstrated a low operating voltage (<5 V) and high channel carrier concentration, but the optimized annealing temperature of the ZrO_x dielectric film was as high as 500 °C. Oja et.al [16], Juma et al. [17], and Oluwabi et al. [18,19] have deposited metal oxide films by spray pyrolysis; in light of their results, the desired morphology and electrical properties were attained after annealing at temperatures above 700 °C. Also, Morvillo et.al [20] reported that annealing does not only influence the performance of metal oxide films but also influences electronic changes in their underlying substrate (e.g. ITO), which eventually makes the optimization process very challenging.

In recent years, different approaches have been reported regarding material selection and curing conditions that can reduce the processing temperature (<250 °C) of solution-processed metal oxide films [21–24]. These approaches can be grouped into two groups: (1) chemical methods that deal with the chemistry of the precursor solution to facilitate a low external temperature [25]—for instance, in combustion synthesis [10,26,27]—and (2) annealing methods that use alternative energy sources or mediated annealing conditions to reduce the processing temperature of metal oxide thin films [25]—examples of this approach are vapour, photo, and vacuum annealing [28].

Among the annealing methods, photo-assisted annealing such as UV, laser, and pulsed light are potential alternatives to traditional high-thermal annealing because an adequate amount of light energy can directly illuminate the surface of the film. Kim et al. proposed an effective way to fabricate solution-processed metal oxide films using deep ultraviolet (DUV) irradiation at 150 °C [29]. Although the approach was highly efficient, the damage caused by such UV equipment may render it unattractive for production. Therefore, it is of great significance to develop a simple route to fabricate high-quality dielectrics at low temperature, as it would be suitable as a gate-dielectric layer in TFT application.

Here, we present a systematic study of the effect of the UV–ozone (UVO) treatment of s solution-processed ZrO_x dielectric by the ultrasonic spray pyrolysis (USP) method; the influence of UVO treatment was investigated with respect to the film's morphology and electrical properties, while the optimized ZrO_x thin film was tested in indium gallium zinc oxide (IGZO)-based TFT devices. It is essential to point out that UVO treatment is newly introduced for sprayed ZrO_x dielectric films and will be informative for future studies, opening the possibility of depositing ZrO_x thin films onto flexible substrates for electronic applications. The deposition temperature reported in this study differs from a related work on the characterization of ZrO_x deposited by the wet chemical method [24,30]. Most literature usually adopts thermal annealing plus UV treatment, whereas in this present work, the photochemical post-deposition treatment was done at room temperature.

Mechanism of UV-Ozone Irradiation

UVO irradiation has been widely studied owing to its broad applicability in different fields, and two regions of wavelengths have been significantly reported in the production of ozone. First, light at $\lambda < 243$ nm splits the atmospheric oxygen molecules, and secondly light at $240 < \lambda < 320$ nm decomposes ozone molecules to oxygen free radicals (O), which effectively performs the oxidative treatment of the ZrO_x films. The chemical reactions involved when the atmospheric air is used for ozone production are [24,31] as follows:

$$O_2 \text{ (air)} + (\lambda < 243 \text{ nm}) \rightarrow 2O \text{ (free radicals)}$$

$$O + O_2 \rightarrow O_3 \text{ (Ozone)}$$

$$O_3 + (240 \text{ nm} < \lambda < 320 \text{ nm}) \rightarrow O_2 + O$$

$$O + O_3 \rightarrow 2O_2$$

2. Materials and Methods

ZrO_x thin films of about 20 nm thickness were deposited (T_{dep}) at 200 °C by the ultrasonic spray pyrolysis (USP) technique, which uses a nebulizer operated at 1.5 MHz. The nebulized precursor solution consisted of zirconium acetylacetate ($Zr(acac)_4$) and methanol. The resulting aerosol was transported onto a heated p–Si-wafer with the aid of air as the carrier gas (flow rate; 3 L/min). After the deposition process, the UVO cleaning process was carried out using a commercially available UVO system (NOVASCAN PSD-series, from Novascan Tech Inc., Boone, NC, USA) with UV-light (184.9 nm and 253.7 nm) generated by a mercury vapor lamp. The UVO exposure time was varied at 30, 60, and 120 min, respectively. The corresponding sample data in figure are labelled as UVO-0, UVO-30, UVO-60, UVO-120 for 0, 30, 60, and 120 min of exposure time, respectively.

The surface morphology of the ZrOx dielectric film was determined by the atomic force microscopy (AFM, from NT-MDT, S & L, Ireland) technique in a non-contact mode. All the scans were taken in air using the instrument NT-MDT solver 47 pro with a resolution in the range of 3 nm, and the investigated area was 2 μm × 2 μm per scan. A silicon cantilever was employed as a probe for the AFM image acquisition and connected to a resonator. AFM measurements were carried out on both the untreated and UV–ozone (UVO)-treated ZrOx thin films to investigate the surface morphology and root mean square (RMS) roughness. The RMS roughness was estimated using the Gwyddion software (Version 2.54, GNU, General public license). The wettability of the ZrO_x dielectric films was studied using a DSA 25-KRÜSS instrument (from Krüss GmbH, Hamburg, Germany). The contact angle (CA) of water on the film surface was measured at room temperature using the sessile drop fitting method. X-ray photoelectron spectroscopy (XPS) measurements were performed on a Kratos Axis Ultra DLD (delay line detector) spectrometer (from Kratos Analytical Ltd., Manchester, England) in conjunction with a 165 mm hemispherical electron energy analyzer. Analyses were carried out with a monochromatic Al Kα X-ray source (1486.6 eV) operating at 150 W. The XPS spectra were recorded using an aperture slot of 300 μm × 700 μm and a base pressure of 2×10^{-9} Torr. The spectrometer was configured to operate with a 20 eV pass energy and a 90° take-off angle from the surface. The spectra were calibrated using a C 1s core level peak centered at a binding energy of 285.0 eV.

Al contact was made using Quorum K975X vacuum evaporator (from Quorum Tech. Ltd., East-sussex, England) on top of the ZrO_x film surface with a contact area of 1.7 mm^2, giving an $Al/ZrO_x/p–Si$ structure. The crystalline p–Si wafer was contacted through an indium metal electrode. The I–V curves were measured by applying a DC bias voltage from −1 to 1 V, while impedance measurements were taken by applying an AC signal of amplitude 20 mV in the frequency range of 100 Hz–1 MHz using AUTOLAB PGSTAT30/2.

The TFTs were produced in a staggered bottom-gate, top-contact structure by depositing AlO_x thin films onto p-type silicon substrates (1−10 Ωcm). The IGZO semiconductor film was sputtered onto the ZrO_x thin films via a shadow mask from a commercial 2:1:1 IGZO ceramic target (from LTS Chemical Inc., Orangeburg, NY, USA) by radiofrequency magnetron sputtering without intentional substrate heating in an AJA 1300-F system. The sputtering atmosphere included an Ar/O_2 flow ratio of 14:2, a 0.3 Pa deposition pressure, a power density of 4.9 W cm^2, and a deposition time of 13 min 30 s to obtain a 30 nm thickness [32].

Finally, source and drain aluminium electrodes (80 nm thick) were deposited by thermal evaporation through a shadow mask onto films, and the ratio between the channel length and width was 10. Thereafter, the IGZO TFTs with the ZrO_x gate dielectric produced by spray were annealed at 150 °C temperature for 1 h in air. The output and the transfer characteristics of the devices

were obtained in both forward and backward sweeps recorded in ambient conditions inside a Faraday cage using a semiconductor parameter analyser (Agilent 4155C, from Santa Clara, CA, USA).

3. Results and Discussion

3.1. Surface Morphology and Wettability of the ZrOx Gate Dielectric Film

Figure 1 depicts the 3D AFM images (2 μm × 2 μm) for the ZrOx dielectric films at different UV-ozone exposure times (0–120 min), labelled as UVO-0, UVO-30, UVO-60, and UVO-120, respectively. Irrespective of the UVO treatment time, the ZrOx thin films demonstrated a plane surface morphology. The RMS roughnesses of the ZrO_x thin film at different UVO exposure times of 0, 30, 60, and 120 min were evaluated to be 0.63 nm, 0.51 nm, 0.32 nm, and 0.28 nm, respectively, indicating that the ZrOx thin films are smooth and that increasing the UVO exposure time reduces the surface roughness of the films. This reduction relative to UVO treatment is due to the removal of organic residue by the oxygen radicals produced during the UVO process, leaving the surface of the film very smooth with a low RMS roughness [11]. A smooth surface is a convenient requirement for the dielectric layer in TFTs because the surface roughness of a dielectric layer strongly influences the quality of the interface with the channel layer, which in turn plays a significant role in the operation of the TFT device [10].

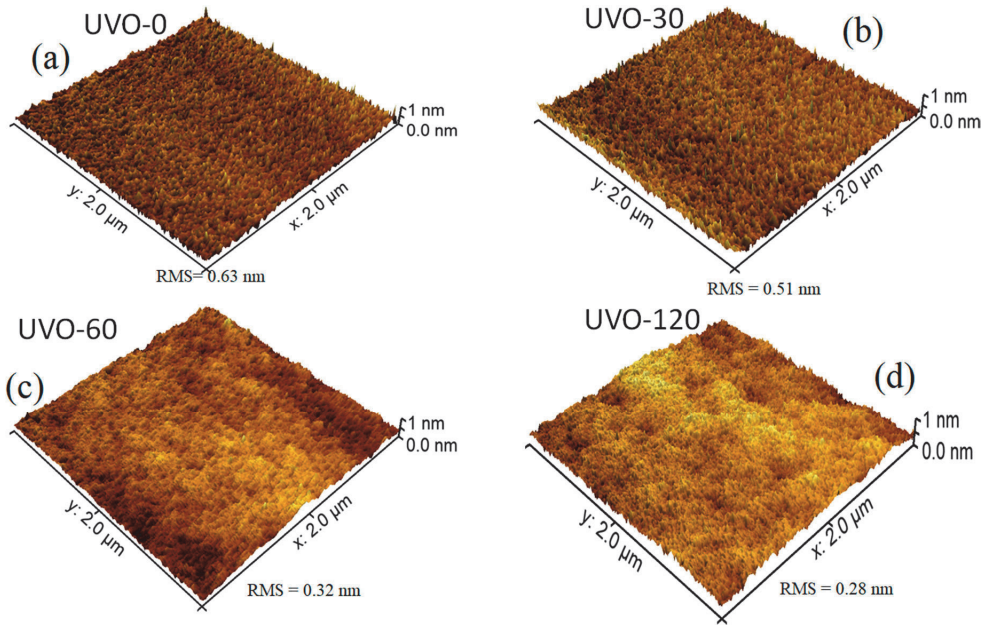

Figure 1. Atomic force microscopy (AFM) morphologies of (**a**) UV–ozone (UVO)-0 (untreated), (**b**) UVO-30, (**c**) UVO-60, and (**d**) UVO-120 treated ZrO_x dielectric thin films.

The wettability of the ZrO_x dielectric surface was studied by measuring the water contact angle (CA), although the XRD pattern of the films indicated an amorphous structure (figure not shown). Figure 2 shows the droplet pictures alongside the mean CA values of water on both UVO-0 and UVO-120 treated ZrO_x films. It also shows the changes in CA values with aging. In the observed results, the UVO-120-treated ZrO_x dielectric is super-hydrophilic with a CA of 7°, while the UVO-0 film is hydrophilic with a CA of 48°.The intermediate treatment time (30 and 60 min) shows a CA value of 40°, which was 17° for UVO-30 and UVO-60, respectively. It is undoubtedly true that the UVO irradiation induces the presence of more OH-groups on the surface of the ZrO_x film due to the simultaneous conversion between the Zr–O–Zr and Zr–OH groups, thereby increasing the hydrophilicity of the

ZrO_x film. A similar observation that supports this hypothesis was reported for ZrO_x thin films grown by dip-coating [33]; however, for ZrO_x dielectric films deposited by both sputtering [34] and electrochemical methods [35], a hydrophobic property was indicated. Gromyko et al. have also reported a difference in CA values for ZnO rods grown by both spray pyrolysis and electrodeposition methods [36].

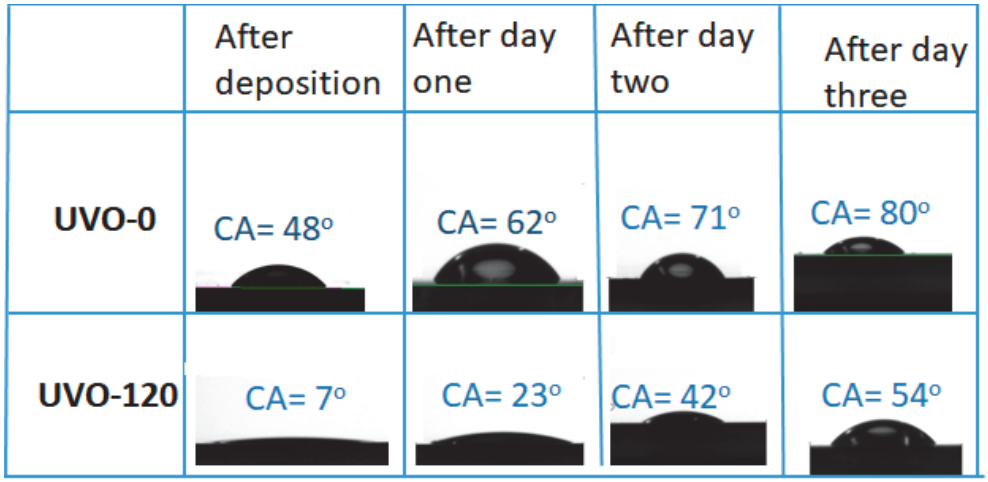

Figure 2. Images of the water contact angle (CA) measurements for both treated (UVO-120) and untreated (UVO-O) ZrO_x thin film and their corresponding contact angles after aging for three days.

Furthermore, after both samples were kept in a Petri-dish and allowed to age for three days, it was observed that the CA increased slightly in both UVO-120 and UVO-0 ZrO_x dielectric films. This indicates that the surface properties of the ZrO_x dielectric thin film can change owing to surface contamination from native carbon-containing species and that ZrO_x test samples should be kept in special conditions. This is because, during the treatment process, the oxygen radicals are produced to remove the organic residues present on the film's surface, leaving the ZrO_x very active, and since test samples were not kept in any special conditions, this makes them vulnerable to native or environmental contaminants.

3.2. XPS Characterization of ZrOx Gate Dielectric Film

To study the surface composition of the deposited ZrOx thin films, XPS measurement was carried out. Figure 3 shows the survey XPS spectra for both the UVO (30–120)-treated and untreated ZrO_x dielectric films. The spectra showed zirconium features at Zr 3s (432.4 eV), Zr 3d (182.0, 184.4 eV), Zr 3p (346, 322 eV), and Zr 4p (30.8 eV) [37,38]. The C 1s peak of adventitious carbon is present at 284.6 eV for all films including the UVO-treated samples. Auger peaks for O (KLL) are also detected at the high-binding-energy region. The peak intensity of Zr 3d increases slightly with increasing UVO exposure time. In addition, the intensity of the O 1s peak was increased. Here, our discussion will be based on the O 1s and Zr 3d core levels, making a correlation between the UVO-0 and UVO-60 samples.

Figure 4 shows the XPS spectra of the O 1s core level for two different UV-ozone treatment conditions. All the XPS spectra are asymmetric, and they were deconvoluted using Lorentzian–Gaussian (function pseudo-Voigt) distribution. Figure 4a displays the measured intensity of the O 1s core level of the UVO-0 sample; the peaks observed were fitted in four different components and centred at the binding energy (BE) values of 530.1, 531.3, 532.0, and 533.4 eV. The peak centred at 530.1 eV can be attributed to the BE of a well-bonded oxygen to zirconium (Me–O) in the ZrOx dielectric film lattice, while the peaks cantered at 531.3 imply the presence of an associated oxygen atom in the form of surface defects or vacancies in the film lattice (Vo). In addition, the peaks centred at 532.0 eV and 533.4 eV can

be attributed to the oxygen in hydroxide-form (Me–OH) as a result of the high electronegativity of hydrogen atoms and the adsorbed oxygen (O_{ads}), respectively [11,39]. Similarly, Figure 4b displays the measured intensity of the O 1s core level after a 60 minute UV-ozone treatment (UVO-60). The peaks on the XPS spectra are all located at BE and centred at BE values of 530.1, 531.3, 531.8, and 533.2 eV. The relatively weak peak component located at 533.2 eV is either due to oxygen connected with carbon or due to adsorbed oxygen in the form of moisture on the surface of the film [11,40,41]. This is certainly not connected to our samples, but to the environment (note that the films well sprayed directly on the Si-substrate were kept in a plastic box).

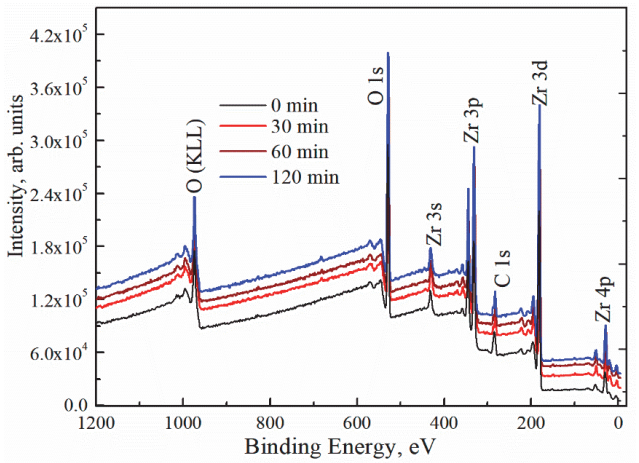

Figure 3. X-ray photoelectron spectroscopy (XPS) survey spectra of ZrOx thin films at different UV–ozone treatment times.

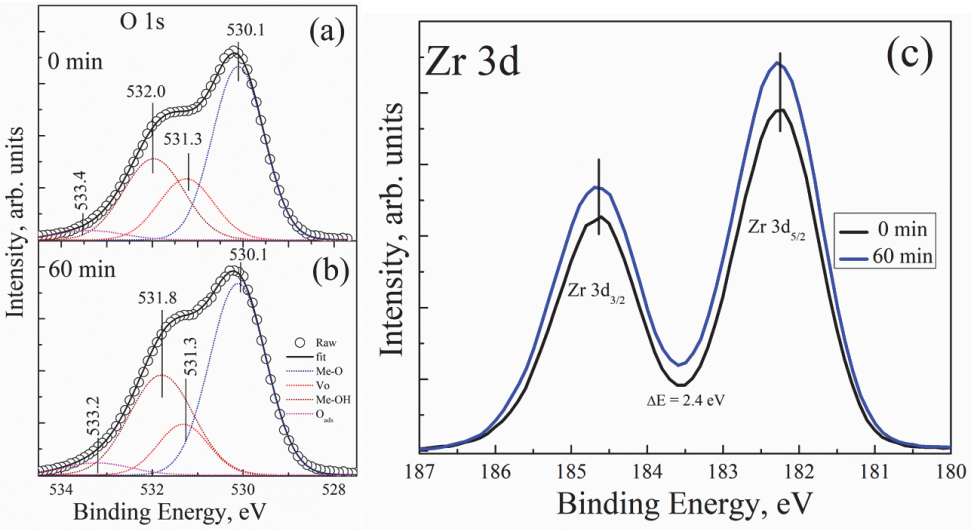

Figure 4. XPS spectra of the O 1s core level for (**a**) 0 minute and (**b**) 60 minutes of UVO treatment of the ZrOx dielectric film; the corresponding XPS spectra for the Zr 3d core level for the ZrO_x dielectric film is presented in (**c**).

To resolve peak quantification properly, the peak ratios of all the components (MeO, Vo, –OH, H_2O_{ads}) found in the O 1s core level spectrum of UVO-0, UVO-30, UVO-60, and UVO-120 ZrO_x

dielectric films were calculated from integrated areas of the O 1s spectrum using Scofield's cross-sections, and their corresponding values are summarized in Table 1. We observe that, by increasing the UVO treatment time from 0 min to 120 min, the ZrO_x dielectric film demonstrated a slight increase in the [Me–OH]/[Me-O] component ratios, and a decrease in the [Vo]/[Me–O] ratio. It is confirmed that the UV–ozone treatment helps to eliminate the organic residues from the surface of the film, which makes our observation very reasonable, and a similar observation has been reported for solution-processed metal oxide films in [36,39,42]. The increase in the Me–OH component is an indication that the XPS study corresponds to the wettability study, suggesting that a high amount of –OH group at the film surface aided hydrophilicity in the UV-ozone treated ZrO_x films.

Table 1. Binding energy of O 1s components and their corresponding ratios for UVO-0, UVO-30, UVO-60 and UVO-120 ZrO_x dielectric films.

Treatment Conditions	Binding Energy (eV)				Component Ratios	
	Me-O	Vo	Me-OH	OH_{ads}	[Vo]/[Me-O]	[Me-OH]/[Me-O]
UVO-0	530.1	531.3	532.0	533.4	0.65	0.94
UVO-30	530.1	531.3	532.0	533.3	0.59	1.04
UVO-60	530.1	531.3	531.8	533.2	0.41	1.10
UVO-120	530.1	531.4	532.8	533.2	0.38	1.22

Figure 4c shows the corresponding XPS spectra of the Zr 3d core level for both UVO-0 and UVO-60 ZrO_x thin films. All the films showed the typical Zr 3d spectra with spin-orbit doublets ($d_{5/2}$ = 182.3 eV, and $d_{3/2}$ = 184.7 eV) separated by ~2.4 eV, which suggests the formation of ZrO_x thin films [17,43]. A similar BE has been reported for Zr 3d in our previous study on Zr-doped TiO_2 films by spray pyrolysis [17].

According to the material characterisation section, an oxygen radical is generated by the UVO treatment to remove organic impurities, thereby effecting a change in the chemical properties of the ZrO_x film's surface. This effect is evidently seen by the reduction in the donor defects (Vo) as well as an increase in the hydroxide group (Me-OH), actively changing the wettability and surface roughness of the ZrO_x dielectric film. The UVO treatment serves as a good insight to reduce the thermal budget of solution-processing techniques—especially spray pyrolysis. Furthermore, the amorphous structure of the ZrO_x dielectric film is essential to enhance the interface quality between different layers and to improve the electronic performance of the fabricated TFT device.

3.3. Electrical Characterization of ZrOx Capacitor

The electrical properties of the amorphous ZrO_x dielectric film was assessed by fabricating a metal insulator semiconductor (MIS) capacitor with the structure Al/ZrO_2/p-Si. Figure 5a shows the plot of leakage current density–voltage (J-V) for ZrO_x dielectric films at different UVO treatment times. An asymmetric behavior can be seen due to the difference in the Schottky barrier height at the electrode interface. However, the leakage current density was calculated in the reverse bias regime, and it was found that the leakage current density in the UVO-0 ZrO_x dielectric film is ~ 2.0×10^{-5} A/cm^2 at 1 V. A similar behavior has been reported for a ZrO_x dielectric deposited by atomic layer deposition (ALD) [44]. In contrast to the untreated sample, the UVO-treated samples demonstrated a remarkable reduction in leakage current density. Thus, by increasing the UVO treatment time to 30 min, the leakage current density was ~ 8.0×10^{-7} A/cm^2, and a further increase in exposure time to 2 h yielded a leakage current density of ~ 1.0×10^{-8} A/cm^2 at 1 V. It was reported that UV irradiation ($\lambda > 185$ nm) can produce hydroxyl radical ($OH^{\cdot}$) at a high quantum yield, which however aids the condensation reaction process of sol-gel metal oxide precursor films [25]. Therefore, it can be inferred that the reduction in the leakage current could be due to densification in the ZrO_x thin film, which occurred as a result of the longer UVO exposure time, increases the formation of metal–oxygen lattices and lowers the amount of oxygen defects on the surface of the ZrO_x thin film. A detailed explanation is given in the XPS study in

Section 3.2. The zero-bias barrier heights of both the untreated and UVO-treated ZrOx dielectric were calculated by fitting the right part of Figure 6 into the following expression [42]:

$$\varnothing_B = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_0}\right) \quad (1)$$

where A is the effective area of the capacitor; A^* is the effective Richardson constant, which is equal to 36 $Acm^{-2}T^{-2}$ for ZrO_2, assuming an electron effective mass 0.3 m_o for ZrO_x; m_o is the free electron mass [30,44]; k is the Boltzmann constant; and $\varnothing_B$ is the Schottky barrier height.

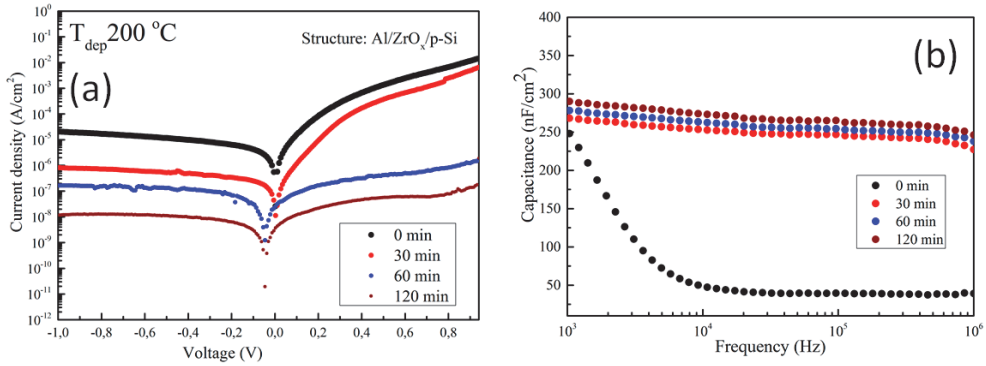

Figure 5. Electrical characterization of the metal insulator semiconductor (MIS) device made from ZrO_x dielectric: (**a**) current–voltage curve under positive and negative biases; and (**b**) capacitance–frequency dispersion curve in the range between 1 kHz and 1 MHz at different UV–ozone treatment times. The device has an Al/ZrOx/p–Si structure.

The values of $\varnothing_B$ extracted from Equation (1) amounted to 0.76, 0.84, 1.04, and 1.09 eV for UVO-0, UVO-30, UVO-60, UVO-120 samples, respectively. The increase in $\varnothing_B$ could be due to surface changes at the ZrO_x/electrode interface, which is caused by a change in surface energy due to UVO oxidative treatment. These values compared well with a similar report on a uniform and amorphous-ZrO_x dielectric film deposited on the native tungsten oxide surface by ALD [44,45]. The observed changes in the barrier height showed that the energy barrier at the electrode/dielectric interfaces is influenced by chemical changes at the surface of dielectric apart from the effect of the image charge build-up at the electrode. To fully understand the changes in the observed barrier height, the effect of charge traps in the dielectric located at the electrode interface of the capacitor constituent layers must be considered [46]. The obtained result is a good indicator of the potential applicability of UVO treatment in reducing the process temperature of solution-processed dielectric films by changes in the surface chemistry of the ZrOx dielectric layer.

To account for the dielectric properties of the deposited ZrO_x films, the capacitance–frequency (C–F) relation was measured at 0 V biased voltage. Figure 5b shows the C–F dispersion curve of ZrO_x capacitors measured at different UVO treatment times. The untreated ZrO_x dielectric demonstrated a high capacitance at the low frequency region, which suggests the contribution of ionic polarization [10]. On other hand, the UVO-treated samples exhibited a slight increase in capacitance (268, 272, and 290 nF/cm^2 for UVO-30, UVO-60, and UVO-120 samples, respectively), which was stable in the high-frequency region. The result obtained from the UVO-treated samples revealed that, by increasing the UVO exposure time, the contributions from the interface or native oxide capacitance can be eliminated. This result concurs with the AFM and XPS results on the condensation and defect reduction from the surface of the UVO treated ZrO_x dielectric films.

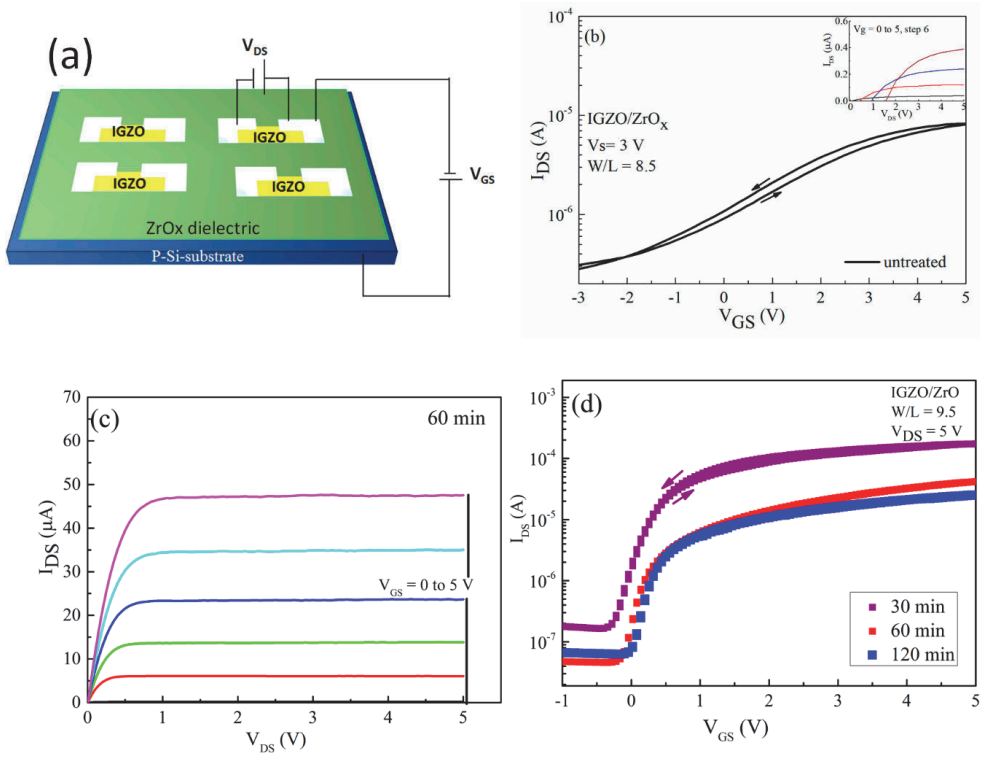

Figure 6. Thin film transistor (TFT) characteristics of indium gallium zinc oxide (IGZO)/ZrOx devices. (**a**) Schematic representation of device structure, (**b**) transfer and output (inset) characteristics of the devices with an untreated ZrOx gate dielectric, (**c**) output characteristic of a TFT-device with a treated ZrOx gate dielectric for 60 min, and (**d**) the transfer performance of the TFT devices with a treated ZrOx gate dielectric at different UV–ozone exposure times.

According to the equation $C = \varepsilon_0 \kappa A/d$, where C is capacitance, ε_0 is the permittivity of free space, κ is the relative permittivity, A is the contact area, and d is the ZrO_x film thickness (~ 20 nm), the relative permittivity (κ) of all the deposited ZrO_x films was calculated. As with the capacitance, the value of κ increases slightly from 5.8 to 6.6 with an increase in the UVO exposure time. It can be inferred from our previous study on ZrO_x dielectric films by spray pyrolysis that thermal annealing (~800 °C) was needed to obtain a κ value of 4.8 [19]. However, in this study, with UVO treatment, a κ value of 6.6 is obtained, thus indicating the advantage of UVO treatment in improving the properties of high-κ oxide dielectric films.

Generally, we observed that the value of κ is smaller compared to the most anticipated theoretical κ value for ZrO_x. This could be due to the influence of interfacial barriers in the film's microstructure during deposition. Also, the sprayed deposited ZrO_x films are amorphous and inevitably contain pores because of the low deposition temperature. Nevertheless, this does not limit the performance of our film, as a similar value has been reported for a ZrO_x dielectric deposited by spin-coating in [2,11].

3.4. TFT Characterization of the Fabricated IGZO-Based Device

In order to ascertain the applicability of the deposited sprayed ZrO_x film in TFT, we fabricated a TFT with a bottom-gate–top-contact configuration, and the alignment between the channel and dielectric layer was patterned and staggered to reduce the probability of the source/drain infringing on the channel. Both the architecture and electrical performance of the TFT devices are shown in Figure 6,

with the extracted electrical parameters presented in Table 2. All transistors which were fabricated are working and show a clear gate dependence corresponding to the n-type channel. The transfer characteristics of the IGZO based devices, which were measured in forward and backward sweeps for both the untreated and the UVO-treated ZrO_x gate dielectric, are shown in Figure 6b,d respectively. The device with the untreated gate dielectric showed a poor performance with a negative V_{on} of about −2 V, which means that the device was working in a depletion mode, and the ratio between the on current and off current (I_{on}/I_{off}) was very low at about 40 the leakage current (I_{GS}) flowing through the gate was about 3.4×10^{-2} A. However, the device with a UVO-treated ZrO_x gate as its dielectric layer showed better electrical performance with negligible hysteresis, which later improved by increasing the UVO exposure time. The V_{on} changed from −0.3 V to 0.02 V when the UVO treatment time was increased from 30 to 120 min, respectively, indicating that the device changes its mode of operation from the depletion mode to enhancement mode. The positive shift in the device V_{on} could stem from the influence of the UV treatment influencing the surface potential of the ZrO_x dielectric. As the UV–ozone exposure time increases, a new chemical state is induced on the surface of the ZrO_x dielectric which is capable of effecting high electron trapping at the interface, particularly when a gate bias is applied to the device. Therefore, in order to compensate the charge, more mobile hole charges are induced, which explains the positively shifted threshold voltage of the TFT [47].

Table 2. Summary of the extracted TFT parameters for an average of ten IGZO/ZrOx devices at different UV–ozone treatment times.

Treatment Conditions	V_{on} (V)	I_{on}/I_{off}	V_{th} (V)	S ($V.dec^{-1}$)	μ_{sat}, $cm^2\ V^{-1}S^{-1}$	I_{GS} at V_{GS} = 5 V (A)
As-dep	−2.0 ± 1.0	~40	–	–	~0.02	$\sim 3.4 \times 10^{-2}$
30 min	−0.3 ± 0.02	$\sim 1.0 \times 10^{3}$	−0.12 ± 0.02	0.27 ± 0.02	2.9 ± 0.5	$\sim 7.4 \times 10^{-5}$
60 min	−0.12 ± 0.1	$\sim 0.4 \times 10^{4}$	0.02 ± 0.01	0.22 ± 0.01	7.0 ± 0.01	$\sim 2.3 \times 10^{-5}$
120 min	0.02 ± 0.01	$\sim 1.0 \times 10^{4}$	0.01 ± 0.005	0.21 ± 0.01	8.4 ± 0.01	$\sim 3.8 \times 10^{-7}$

This result concurs with the wettability measurement as well as the Schottky barrier determination, demonstrating an increase in the energy barrier height caused by changes in the surface potential of the ZrO_x dielectric layer during the UV-ozone treatment. Furthermore, the magnitudes of the on–off current ratio, $I_{on}/I_{off,}$ are 1×10^3, 0.4×10^4, and 1×10^4 when the UVO treatment time increases from 30, 60 to 120 min, respectively. The Figure 6c shows the typical output characteristic curve for the 60 min UVO-treated ZrO_x gate dielectric TFT. It can be seen that the UVO-treated TFTs exhibit typical n-type channel conduction behavior with a clear pinch-off voltage and current saturation.

The fabricated TFT parameters, such as saturation mobility (μ_{sat}), threshold voltage and sub-threshold slope, were extracted from the following equation [45] and are summarized in Table 2.

$$I_d = \left(\frac{C_{ZrO} B \mu_{sat}}{2L}\right)(V_G - V_T)^2 \quad (2)$$

where C_{ZrO} is the gate dielectric capacitance per unit area, B and L are the channel width and length, V_G is the gate voltage, and V_T is the threshold voltage, which was determined in the saturation regim by the fitting of the curve of $I_d^{\frac{1}{2}}$ versus V_G and extrapolating the linear part to the V_G axis. As expected, the devices with a UVO-treated ZrOx dielectric layer have better mobility, which increases from 2.9 to 8.4 $cm^2\ V^{-1}S^{-1}$ with increasing treatment time (from 30 to 120 min).

The observed changes in mobility may be due to an increase in the capacitance of the ZrO_x gate dielectric layer when exposed to UVO treatment. According to Dong et al. [24] in their recent publication, there is the possibility of using UVO treatment to improve the device performance of InO/ZrO_x TFTs. Also, Carlos et al. [46] demonstrated the possibility of reducing the gate leakage current of $IGZO/AlO_x$ TFT devices by using a very powerful UV lamp. The device demonstrated a positive

shift in its threshold voltage (Vth) from −0.12 to 0.01 V, and a slight decrease in the sub-threshold slope (S) with increasing UVO treatment. The positive V_{th} indicated that the device can completely be switched off and can be turned on by a voltage as minimal as 0.01 V. In addition, the small S value extracted from the TFTs may be attributed to the large area capacitance at the ZrO_x gate dielectric layer and smoother surface due to the UVO cleaning of the layer, thereby improving the interface quality between IGZO and ZrO_x [11,39].

4. Conclusions

In summary, we have demonstrated the possibility of lowering the processing temperature of ultrasonically sprayed amorphous ZrO_x thin films by introducing UV–ozone post deposition treatment. It was confirmed by XPS and wettability measurement that by increasing the UVO exposure time, the surface of the sprayed ZrO_x films became less defective and hydrophilic, with a contact angle of 7°, indicating the removal of organic impurities associated with the precursor reagents from the surface of the film. The AFM result showed that the deposited ZrO_x film was smooth, and the surface roughness was reduced from 0.63 nm (UVO-0 film) to 0.28 nm (UVO-120 film). Finally, to demonstrate the electrical performance of the film, a MOS-capacitor was fabricated, and we observed a reduction in the leakage current density by three orders of magnitude by increasing the UV–ozone treatment time. The UVO treated ZrO_x capacitor attained desirable dielectric properties, such as a low leakage current density of 10^{-8} A/cm^2, a capacitance of 290 nF/cm^2 and relative permittivity of 6.6 (both at 1 kHz).

As a proof of concept, both untreated and UV–ozone post deposition-treated ZrO_x thin film were used as the gate dielectric in TFT. The fabricated TFT with the treated ZrOx films demonstrated an improved performance compared to a device produced with the untreated ZrOx dielectric thin film. The former operates in an enhancement mode (Von > 0), with low power consumption and a high saturation mobility of 8 cm^2 V^{-1}s^{-1}. UV-ozone treatment is the key to developing a metal oxide film at low temperature by wet chemical techniques. This concept thus opens the potential application of ultrasonic spray technology in flexible electronics.

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Appendix 2

Table 1.1: Reports on solution processed oxide thin film transistors (TFTs) based on ZrO_x gate oxide layer deposited at different temperature range $250\ ℃ \leq t \leq 500\ ℃$ by different methods. (T = process temperature, SCS = Spray combustion synthesis)

Gate dielectric layer				Channel layer				Transistor parameters			Reference
Method	Material	T °C	Structure	Method	Material	T (°C)	Structure	Mobility ($cm^2V^{-1}S^{-1}$)	V_{on} (V)	SS ($Vdec^{-1}$)	
Spin coating	ZrO_x	400	crystalline	Spin coating	InO_x	300	crystalline	4.42	0.31	0.07	[130]
Spin coating	ZrO_x	300	amophous	Spin coating	NiO_x	250	amorphous	4.8	-1.6	0.35	[118]
Spin coating	ZrO_x	250	amophous	Spin coating	InO_x	250	amorphous	10.0	0	0.1	[118]
Spin coating	ZrO_x	500	crystalline	Spin coating	ZTO	500	crystalline	2.50	1	0.23	[105]
Spin coating	ZrO_x	350	amophous	Spin coating	IZO	250	amorphous	0.16	0	1.49	[36], [72]
Spin coating	ZrO_x	400	crystalline	Spin coating	SnO_x	350	crystalline	2.50	-0.5	0.30	[116]
Spin coating	ZrO_x	300	amorphous	Spin coating	IZO	250	-	0.91	-0.5	0.12	[132]
Spin coating	ZrO_x	300	-	Spin coating	InO_x	200	-	0.44	1	-	[74]
Spray pyrolysis	ZrO_x	400	crystalline	Spray pyrolysis	Li:ZnO	400	crystalline	85	0.2	-	[91] [7]
Spray pyrolysis	ZrO_x	400	crystalline	Spray pyrolysis	ZnO	400	crystalline	32.0	-1	-	[91] [7]
Spray pyrolysis	ZrO_x	300	amorphous	Spray pyrolysis	IZO	275	-	6.2	-0.2	-	[133]
SCS	ZrO_x	350	-	SCS	IGZO	350	-	5.3	-0.6	-	[133]
SCS	ZrO_x	350	amophous	SCS	IGZO	350	amorphous	28.5	0.3	-	[52] [68]
Ink Jet	ZrO_x	350	amorphous	Ink Jet	IGO	350	amorphous	10.8	-0.6	0.12	[83]
Ink Jet	ZrOx	300	amorphous	Ink Jet	ZTO	300	-	0.04	4	-	[106]
Sol-gel	ZrO_x	100	-	Sol-gel	ZnO	100	-	0.48	0.24	0.48	[156]

Curriculum vitae

Personal data

Name:	Oluwabi Abayomi Titilope
Date of birth:	07.10.1990
Place of birth:	Abeokuta, Nigeria
Citizenship:	Nigerian
ORCID:	0000-0001-9377-8791

Contact data

E-mail:	abayomioluwabi@gmail.com

Education

2016–2020	Tallinn University of Technology, Chemical and Materials Technology, Doctoral study (PhD)
2014–2016	Tallinn University of Technology, Materials and Sustainable Energetics, MSc. (Cum laude)
2008–2012	Federal University of Agriculture, Abeokuta. Chemistry, BSc. (Second class upper).
2000–2006	Rose-born International Secondary School.

Language competence

English	Fluent
Yoruba	Fluent
German	Beginner
French	Basic

Training Courses, Conferences, and visit to international laboratories

2017–2020	Graduate school "Functional materials and technologies FMTDK", Tallinn University of Technology, Estonia.
Sept. 2018–May 2019	Smart electronic fabrication by solution based methods. Centre for material research (CENIMAT), New University of Lisbon Portugal.
July–Aug. 2018	Circular Economy of Material: Summer School in Lappeenranta Finland. (Business Pitch)
Feb. –May 2018	Tallinn Business Incubator, Estonia.

International conferences attended

1–5.09.2019	European congress and exhibition on advance materials and processes (EuroMat), Stockholm, Sweden (Oral presentation)
20–22.06.2018	International conference on microelectronic devices and technologies (micDat), Barcelona, Spain (Oral presentation)
20–22.09.2017	Baltic polymer symposium, Tallinn, Estonia (Oral presentation)
26–27.05.2016	13th International conference of young scientists on energy issues (CYSENI), Kaunas, Lithuania. (Oral presentation)

Defended dissertations

2016 Master's Degree: Zirconium doped titanium dioxide thin films by chemical spray pyrolysis, Supervisors: Ilona Oja Acik, Albert Juma.

2012 Bachelor's Degree: Inhibitory effect of Sodium dodecylsulphate in the corrosion of copper metals, Supervisors: M. Nkiko, and Bamgbose.

Recognitions (Awards)

2015 Student union award given to the most active student with best academic record.

Research projects involved

1.01.2020−31.12.2024 PRG627 Antimony chalcogenide thin films for next-generation semi-transparent solar cells applicable in electricity producing windows.

1.01.2016–1-03.2013 TK141 Centre of Excellent: "Advanced materials and high technology devices for sustainable energetics, sensorics, and nanoelectronics".

1.01.2014–31-12.2019 IUT19-4 "Thin films and nanomaterials by wet chemical methods for next generation photovoltaics".

1.01.2013−31.12.2015 B24 "Metal oxide thin films by wet chemical methods for electronic devices".

Supervised dissertations

Khalil Omotosho, Master's Degree, 2019, (sup) **Abayomi Titilope Oluwabi**; Ilona Oja Açik, Spray deposited aluminum oxide thin films for electronic applications, Tallinn University of Technology School of Engineering, Department of Materials and Environmental Technology. (Student now PhD student in Texas University, USA).

List of publications

1. **Oluwabi, A. T**.; Gaspar, T.; Katerski, A.; Mere, A.; Krunks, M.; Pereira, L.; Oja Acik, I. (2020). Influence of post-uv/ozone treatment of ultrasonic sprayed zirconium oxide dielectric films for low temperature oxide thin film transistor. Materials.10.3390/ma13010006.
2. **Oluwabi, A. T**.; Katerski, A.; Carlos, E.; Branquinho, R.; Mere, A.; Krunks, M.; Fortunato, E.; Pereira, L.; Oja Acik, I. (2020). Application of ultrasonic sprayed zirconium oxide dielectric in zinc tin oxide-based thin film transistor. Journal of Materials Chemistry C.10.1039/C9TC05127A.
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6. **Oluwabi, A. T**; Oja Acik, I.; Krunks, M.; Mikli, V.; Juma, A. (2016). Characterisation of zirconium doped titanium dioxide thin films deposited by chemical spray pyrolysis. In: Proceedings 13th International Conference of Young Scientists on Energy Issues, May 26-27, 2016, Kaunas, Lithuania (VII-210−VII-218). Kaunas, Lithuania: Lithuanian Energy Institute.

Elulookirjeldus

Isikuandmed

Nimi:	Oluwabi Abayomi Titilope
Sünniaeg:	07.10.1990
Sünnikoht:	Nigeeria
Kodakondsus:	Nigeeria
ORCID:	0000-0001-9377-8791

Kontaktandmed

E-post:	abayomioluwabi@gmail.com

Hariduskäik

2016–2020	Tallinna Tehnikaülikool – PhD, keemia-ja materjalitehnoloogia
2014–2016	Tallinna Tehnikaülikool – MSc, Materjalid ja protsessid jätkusuutlikus energeetikas (Cum laude)
2008–2012	Federal University of Agriculture, Akeokuta – BSc, keemia
2000–2006	Roseborn International Secondary School (Keskharidus)

Keelteoskus

Inglise keel	Kõrgtase
Joruba keel	Kõrgtase
Saksa keel	Algtase
Prantsuse keel	Algtase

Täiendkursused, töö välisboris, Konverentsiettekanded

2017–2020	Funktsionaalsete materjalide ja tehnoloogiate doktorikool, Tallinna Tehnikaülikool, Eesti
Sept. 2018–Mai 2019	Centre for material research (CENIMAT), New University of Lisbon, Portugal
Juuli–August 2018	Circular Economy of Material: Suvekool Lappeenranta, Soome
Veebr. –Mai 2018	Tehnopol Startup Inkubaator Tallinna, Eesti

Osalemine teaduskonverentsidel

1–5.09.2019	European congress and exhibition on advance materials and processes (EuroMat), Stockholm, Rootsi (Suuline ettekanne)
20–22.06.2018	International conference on microelectronic devices and technologies (micDat), Barcelona, Hispaania (Suuline ettekanne)
20–22.09.2017	Baltic polymer symposium, Tallinn, Eesti (Suuline ettekanne)
26–27.05.2016	13th International conference of young scientists on energy issues (CYSENI), Kaunas, Leedu. (Suuline ettekanne)

Teaduskraadid

2016, magistrikraad, Zr-legeeritud titaandioksiidi õhukesed kiled pihustuspürolüüsi meetodil, Tallinna Tehnikaülikool, juhendajad: Ilona Oja Acik, Albert Juma.

2012, bakalaureuse kraad: Inhibitory effect of Sodium dodecylsulphate in the corrosion of copper metals, Federal University of Agriculture Abeokuta, juhendajad: M. Nkiko, and Bamgbose.

Tunnustused

2015 Tallinna Tehnikaülikool: TalTech üliõpilasesinduse auhind.

Teadusprojektid

1.01.2020−31.12.2024 PRG627 "Antimon-kalkogeniid õhukesed kiled järgmise põlvkonna pool-läbipaistvatele päikeseelementidele kasutamiseks elektrit tootvates akendes".

1.01.2016–1-03.2013 TK141 "Tippkeskused: Uudsed materjalid ja kõrgtehnoloogilised seadmed energia salvestamise ja muundamise süsteemidele".

1.01.2014–31-12.2019 IUT19-4 "Õhukesed kiled ja nanomaterjalid keemilistel vedeliksadestusmeetoditel uue põlvkonna fotovoltseadistele".

1.01.2013−31.12.2015 B24 "Keemilistel meetoditel kasvatatud metalli oksiidide õhukesed kiled elektroonikaseadistele ".

Juhendatud väitekirjad

Khalil Omotosho, Magistrikraad, 2019, (juhendajad) **Abayomi Titilope Oluwabi**; Ilona Oja Açik, Pihustuspürolüüsi meetodil sadestatud alumiiniumoksiidi õhukesed kiled elektroonikaseadistele, Tallinna Tehnikaülikool, Inseneriteaduskond, Materjali- ja keskkonnatehnoloogia instituut.

Publikatsioonid

1. **Oluwabi, A. T**.; Gaspar, T.; Katerski, A.; Mere, A.; Krunks, M.; Pereira, L.; Oja Acik, I. (2020). Influence of post-uv/ozone treatment of ultrasonic sprayed zirconium oxide dielectric films for low temperature oxide thin film transistor. Materials.10.3390/ma13010006.
2. **Oluwabi, A. T**.; Katerski, A.; Carlos, E.; Branquinho, R.; Mere, A.; Krunks, M.; Fortunato, E.; Pereira, L.; Oja Acik, I. (2020). Application of ultrasonic sprayed zirconium oxide dielectric in zinc tin oxide-based thin film transistor. Journal of Materials Chemistry C.10.1039/C9TC05127A.
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