TALLINN UNIVERSITY OF TECHNOLOGY
School of Information Technologies

Erkan Köprübasi 184576IVEM

SIC MERGED PIN SCHOTTKY DIODE DESIGN WITH TCAD AND REVERSE RECOVERY OPTIMIZATION

Master's thesis

Supervisor: Prof. Ants Koel
Co-supervisor: Hasan Mehadi Ziko

Tallinn 2022

TALLINNA TEHNIKAÜLIKOOL
Infotehnoloogia teaduskond

Erkan Köprübasi 184576IVEM

SIC ÜHILDATUD PIN SCHOTTKY DIOODI DISAIN KASUTADES TCAD-I JA VASTUTAKISTUSE TAASTUMISE OPTIMEERIMINE

Magistritöö

Juhendaja: Prof. Ants Koel
Kaasjuhendaja: Hasan Mehadi Ziko

Tallinn 2022

Author’s declaration of originality

I hereby certify that I am the sole author of this thesis. All the used materials, references to the literature and the work of others have been referred to. This thesis has not been presented for examination anywhere else.

Author: Erkan Köprübasi

09.05.2022

Abstract

It is well known that electronic component design and optimization play very important role on electronic device applications. Everyday components are being developed thanks to fast development on new technologies. In this master thesis work, SiC Merged PiN Schottky Diode design is carried out from fabrication process in terms of semiconductor process, device simulation and electrical behaviour. Design and electrical behaviour analysis are done with Silvaco TCAD tool. Electrical static and transient characteristic of SiC MPSD is executed. Studies and simulation results showed that reverse recovery response can be improved with changing the properties of physical parameters. Reducing metal contact, increasing area of N- doped Epitaxial Layer and adding P+ doped Controlled Injection of Backside Holes (CIBH) into the epitaxial layer results an improvement on reverse recovery response. Meaning that improvement on switching speed of the SiC MPS Diode while going from OFF to ON state.

This thesis is written in English and is 36 pages long, including 5 chapters, 19 figures and 5 tables.

Annotatsioon

SiC ühildatud PIN Schottky dioodi disain kasutades TCAD-i ja vastutakistuse taastumise optimeerimine

Elektroonikakomponentide projekteerimine ja optimeerimine mängivad elektroonikaseadmete edasirakendustes väga olulist rolli. Igapäevaseid komponente arendatakse edasi tänu uute tehnoloogiate kiirele arengule. Käesolevas magistritöös on SiC integreeritud PiN+Schottky (MPSD) dioodi projekteerimine läbi viidud tootmisprotsessist pooljuhtprotsessi, teostatud analüüs elektriliste karakteristikute osas, kasutades seadise simulatsiooni. Disain ja elektriliste karakteristikute analüüs on tehtud Silvaco TCAD simulatsioonipaketiga. Simulatsioonide tulemusel on saadud SiC MPSD elektriline staatiline ja dünaamiline siirdekarakteristik. Uuringud ja simulatsioonitulemused näitasid, et vastupidist taastumisreaktsiooni saab parandada tehnoloogiliste parameetrite omaduste muutmisega. Metallikontakti vähendamine, N-leegitud epitaksiaalse kihi pindala suurendamine ja epitaksiaalkihti P+ legeeritud alasse aukude kontrollitud injektsiooni (Controlled Injection of Backside Holes, CIBH) lisamine epitaksiaalsesse kihti parandavad taastumisreaktsiooni vastupingele. See resulteerub SiC MPS-dioodi lülituskiiruse paranemises.

Lõputöö on kirjutatud inglise keeles ning sisaldab teksti 36 leheküljel, 5 peatükki, 19 joonist, 5 tabelit.

List of abbreviations and terms

SiC	Silicon Carbide
PiN	Positive Intrinsic Negative
TCAD	Technology Computer Aided Design
MPSD	Merged PiN Schottky Diode
RF	Radio Frequency
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
JFET	Junction Field Effect Transistor
MESFET	Metal Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
GaN	Gallium Nitride
I-V	Current – Voltage
V	Voltage
VWF	Virtual Wafer Fab
2D	2 dimension

Table of contents

1 Introduction 11
2 SILICON CARBIDE MATERIAL 12
2.1 Crystal Structure 13
2.2 Electrical Properties 15
2.3 Physical Properties 15
2.4 Effects on Diode Characteristic 16
2.5 Applications 16
3 POWER DIODES 17
3.1 Schottky Barrier Diode 17
3.1.1 Static Characteristic 19
3.1.2 Transient Characteristic 20
3.1.3 Key Parameters 20
3.2 Merged PiN Schottky Diodes 22
3.2.1 Static Characteristic 23
3.2.2 Transient Characteristic 24
3.3 Comparison of Schottky Barrier and MPS/JBS Diodes 24
3.4 Application 25
4 DIODE MODELLING AND SIMULATION 26
4.1 Introduction 26
4.2 Familiarization with SILVACO TCAD 26
4.3 Challenges of Using TCAD 28
4.4 Diode Modelling 28
4.4.1 Base Diode Model 29
4.4.2 Proposed Diode Model 30
4.5 Diode Simulation 38
4.5.1 Introduction 38
4.5.2 Simulation Results 39
4.5.3 Forward I-V Curve Simulation Results 40
4.5.4 Reverse Recovery Simulation Results 42

5 Summary 51
5.1 Future Work 52
References 53
Appendix 1 – Non-exclusive licence for reproduction and publication of a graduation thesis 56
Appendix 2 – Silvaco Input Deck Source Code of Proposed Diode Design and Electrical Characteristic Analysis 57

List of figures

Figure 1. Atomic Structure of Polytypes [7]. 13
Figure 2. SBD Physical Structure of forward bias (a) and reverse bias (b) [18]. 18
Figure 3. I-V Characteristic of SBD vs. PN [13]..... 19
Figure 4. ON-state JBS diode, lines show current flow (a) OFF-state JBS diode, dotted line shows the edge of depletion region (b) [16]. 23
Figure 5. Workflow of Silvaco Deck Build..... 27
Figure 6. Base SiCMPSD Physical Model [24]. 29
Figure 7. Structure Output File of Base Diode Design 30
Figure 8. 2.5D Structure Output File of Base Diode Design. 30
Figure 9 Proposed SiCMPSD Physical Model 31
Figure 10. Structure Output File of Proposed Diode Design 32
Figure 11. 2.5D Structure output file of Proposed Diode Design 32
Figure 12. A Mesh Example [30] 34
Figure 13. Proposed Mesh Design. 35
Figure 14. Degradation Example with Excessive Reduction 35
Figure 15. Reverse Recovery of Diode [28]. 39
Figure 16 Forward Bias I-V Curve of Base Diode 40
Figure 17. Forward Bias I-V Curve of Proposed Diode 40
Figure 18 Forward I-V Curve Comparison of Base and Proposed Diode 41
Figure 19. Reverse Recovery of Base SiC MPSD 45
Figure 20. Base Diode Model vs. Bigger Epitaxial Layer Base Diode Model 46
Figure 21. Base Diode Model vs CIBH Region Added Base Model Diode 47
Figure 22. Base Diode Model vs. Three Different Metal Contact Dimensions 48
Figure 23. Reverse Recovery of Proposed SiC MPSD 49
Figure 24 Comparison Between Base and Proposed Diode Models of Reverse Recovery Response 50

List of tables

Table 1 Comparison Electrical Properties [8], [9], [10]. 15
Table 2. Comparison Physical Properties [11]. 16
Table 3. Comparison of SBD vs. MPSD/JBSD. 24
Table 4. Physical Distances of Regions..... 29
Table 5. Physical Distances of Proposed Diode Model..... 31
Table 6 Physical Dimensions Comparison..... 32
Table 7 Dimension Comparison of Epitaxial Layer..... 46
Table 8 Metal Contact Dimensions 48

1 Introduction

Silicon Carbide technology brings many advantages on power electronics area. Nowadays SiC usage on the power electronic applications are getting more common. For power diodes, SiC material is very good choice as well. SiC power diodes are superior on their equivalent devices in various ways. SiC power diodes have high efficiency on high voltage applications. SiC Merged PiN Schottky Diodes are specifically investigated in this Master thesis work. Thanks to its physical structure, SiC MPS diodes has low forward voltage and extremely high switching speed. However the main drawback is high leakage current.

TCAD tools are very important in terms of processing and manufacturing semiconductors, electronic components and devices. With the help of TCAD tools, electronic components can be investigated from many perspectives such as physical/electrical properties, design process and electrical behaviours.

In this Master thesis work SiC MPS diode is studied in terms of theoretical information of SiC material, diode characteristics and practical work of SiC MPS diode modelling, simulation and reverse recovery response optimization. Diode modelling covers, semiconductor processing parts such as defining impurities(dopings), dopant types, minority/majority carriers, conductors, junctions etc. Simulation shows the physical output of the device design and electrical behaviour of the device.

The purpose of the present Master thesis work is, modelling and designing a SiC MPS diode with using TCAD tool and making an optimization on reverse recovery response of the diode in order to achieve high switching speed.

2 SILICON CARBIDE MATERIAL

SILICON has long been the dominant semiconductor of choice for high power and temperature related electronic devices. However, recently, wide bandgap semiconductors, particularly Silicon Carbide (SiC) has attracted much attention because it offers tremendous benefits over other semiconductor materials in a large number of industrial and military applications.[1] The physical and electronic properties of SiC make it the foremost semiconductor material for short wavelength optoelectronic, high temperature, radiation resistant, and high-power/high-frequency electronic devices. [2]

Silicon carbide, exceedingly hard, synthetically produced crystalline compound of silicon and carbon. Its chemical formula is SiC. Since the late 19th century silicon carbide has been an important material for sandpapers, grinding wheels, and cutting tools. More recently, it has found application in refractory linings and heating elements for industrial furnaces, in wear-resistant parts for pumps and rocket engines, and in semiconducting substrates for light-emitting diodes. [3]

Silicon Carbide is the only chemical compound of carbon and silicon. It was originally produced by a high temperature electro-chemical reaction of sand and carbon. Silicon carbide is an excellent abrasive and has been produced and made into grinding wheels and other abrasive products for over one hundred years. Today the material has been developed into a high quality technical grade ceramic with very good mechanical properties. It is used in abrasives, refractories, ceramics, and numerous high-performance applications. The material can also be made an electrical conductor and has applications in resistance heating, flame igniters and electronic components. Structural and wear applications are constantly developing. [4]

Key Silicon Carbide properties;

- Low density
- High strength
- Low thermal expansion
- High thermal conductivity
- High hardness
- High elastic modulus
- Excellent thermal shoch resistance
- Superior chemical inertness

2.1 Crystal Structure

SiC occurs many types of polytypes which is also called as crystal structures. Although SiC is consist of 50% Carbon and 50% Silicon, SiC has more than 200 polytypes. Most common polytypes are 3C-SiC, 4H-SiC and 6H-SiC. The biatom layers are being stacked with sequence of the SiC structure so that polytypes are characterized. [5] [6]

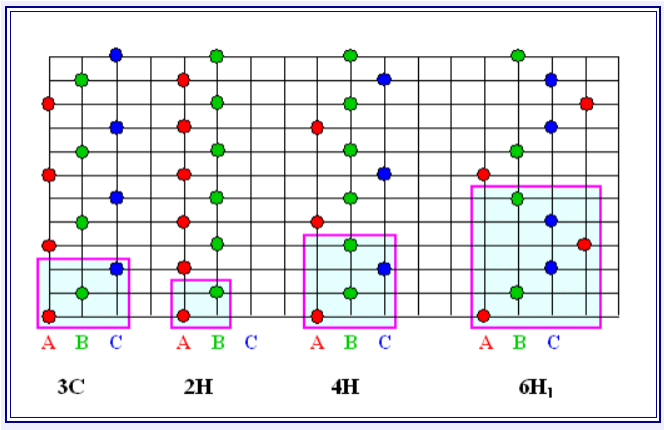

Figure 1. Atomic Structure of Polytypes [7].

3C : Cubic crystal lattice structure form of SiC polytype. Stacking sequence is ABC. Number of hexogonal bonds is 0. Number of cubic bonds is 1.

2H : Hexogonal symmetry structure form of SiC polytype. Stacking sequence is AB. Number of hexogonal bonds is 1. Number of cubic bonds is 0.

4H : Hexogonal and cubic symmetry structure form of SiC polytype. 4H includes of equal number of hexogonal and cubic bonds in its structure. Stacking sequence is ABCB. Number of hexogonal bonds is 1. Number of cubic bonds is 1.

6H : Proportionaly hexogonal and cubic symmetry structure of SiC polytype. 6H consists of one-third hexogonal bonds two-thirds cubic bonds. Stacking sequence is ABCACB. Number of hexogonal bonds is 1. Number of cubic bonds is 2.

2.2 Electrical Properties

Each polytypes has its own unique electrical properties. Considering this properties which type of polytype would be inuse is determined. Most commonly used polytypes and silicon are compared in terms of electrical properties in Table 1.

Table 1 Comparison Electrical Properties [8], [9], [10].

Properties / Material	**Si**	**4H-SiC**	**6H-SiC**	**3C-SiC**
Bandgap Energy [eV]	1.12	3.26	3.03	2.4
Relative dielectric constant (∈r)	11.9	9.7	9.66	9.72
Thermal Conductivity [W/cmK]	1.31	4.9	4.9	3.2
Breakdown Field [MV/cm]	0.3	3.0	3.2	1.5
Electron Mobility [cm2/Vs]	1430	900	60	800
Hole Mobility [cm2/Vs]	480	115	90	40
Saturated Electron Velocity [10^7 cm/s]	1	2	2	2.5
Intrinsic Carrier Concentration [cm^-3]	9.65x10^9	5x10^-9	1.6x10^-6	1.5x10^-1

Silicon Carbide politypes have advantages on three key properties above. These are Bandgap Energy, Thermal Conductivity and Breakdown field. Breakdown field is ca. 10 times in favor of Silicon Carbide protypes. Thermal conductivity and bandgap energy of SiC politypes are 3 times more than silicon.

Electron mobility is one of the Silicon has advantage however it is one of the main reason that 4H-SiC is being chosen instead of 6H-SiC prototype.

All the properties above are temperature dependant. 300K degree is taken into account in order to make the comparison.

2.3 Physical Properties

In Table 2, most commonly used polytypes and silicon are compared in terms of physical properties.

Table 2. Comparison Physical Properties [11].

Properties / Material	Si	4H-SiC	6H-SiC	3C-SiC
Lattice α [Å]	5.43	3.08	3.08	4.36
Lattice c [Å]	n.a.	15.12	10.05	n.a.
Bond Lenght [Å]	2.35	1.89	1.89	1.89
TEC [10^-6/K]	2.6	-	4.5	3.0
Density [gm/cm^3]	2.3	3.2	3.2	3.2
Thermal Condition [W/cmK]	1.5	5	5	5
Melting Point [°C]	1420	2830	2830	2830
Mosh Hardness		9	9	9

2.4 Effects on Diode Characteristic

There are several advantages of how SiC material effects on diode characteristics. These are low voltage drop, high switching speed and low noise. Thanks to SiC material, SiC based diodes have higher breakdown voltage and greater current carrying capacity.

2.5 Applications

SiC devices are used in many areas. The most beneficial advantages that SiC-based electronics offer are in the areas of high-temperature device operation, high-power device operation, high-frequency device operation, and optoelectronic device operation. Device types include rectifiers, power switches, RF and microwave power devices (PiN and Schottky barrier diodes, MOSFETs, JFETs and MESFETs) [12].

- Wind turbine
- Railway
- Inverter for Industry
- Power conditioner
- Power modules in 5G base stations.

3 POWER DIODES

Power devices are generally either simple two-terminal devices like power diodes, or more complex three-terminal devices like MOSFET or IGBT. The power diodes can be divided into three main classes: (I) Schottky diodes, (II) PiN diodes and (III) merged structure diodes like Junction-Barrier Schottky (JBS) / Merged PiN Schottky diodes. The highly valued characteristics of (I) Schottky diodes is extremely high switching speed but the drawbacks being at the same time relatively high leakage current, can not hold higher voltage without breakdown. The good characteristics of PiN diodes (II) is the low leaking current, but unfortunately the drawback being low switching speed. Merged PiN Schottky diodes merge also the good sides of the (I) and (II) type diodes showing at the same time low impact from the drawbacks of the (I) or (II) typed diodes mentioned before.

3.1 Schottky Barrier Diode

One of the primarily useful power diode in power applications is Power Schottky Barrier Diode. Thanks to its physical structure, power SBDs has extremely low forward voltage(Vf) and extremely high switching speed. However there is a large reverse loss because of the high reverse current. The reverse current may be change depending on the physical material of the SBD.

Today, Schottky barrier diodes (SBDs) play a very important role in the contemporary electronic circuits, e.g. SMPS. They belong to the class of unipolar devices having very short recovery time, which follows from the lack of minority carriers in the diode epitaxial layer. The fundamental advantage of SBDs, in comparison to pin diodes, is their very high switching speed, whereas the most important drawback is a low value of the blocking (breakdown) voltage of silicon SBDs. The improvement of properties of the considered power devices is possible by using wide bandgap materials such as silicon carbide (SiC), gallium nitride (GaN) or diamond (C), in SBDs fabrication process. [15]

Schottky barrier diodes, have high switching speed but also they have high reverse current. Schottky Barrier Diodes have low voltage drop therefore they are useful for energy efficiency applications. Rectifiers in switched-mode power supplies is an example of usage area of Schottky Barrier Diodes. [17]

There are three main features of the SBDs. These are;

- Low Forward Voltage(Vf); Low forward voltage is a great advantage for heat loss and energy efficiency related problems.
- High Speed; High switching speed is huge advantage. It is because of metal barrier and including no holes.
- Large Reverse Current(Ir); Large reverse current is the main drawback of the SBDs. However this can be compansated with using special variants of SBDs for example using different types of metals and semiconductor completes.

Schottky Barrier Diode is different from classical PN junction diode. Instead of holes, SBD has got metal structure. One side is semiconductor, other side is metal. This type of metal-semiconductor junction is called as a Schottky Junction.

Forward and Reverse biased physical structure can be seen in below figure.

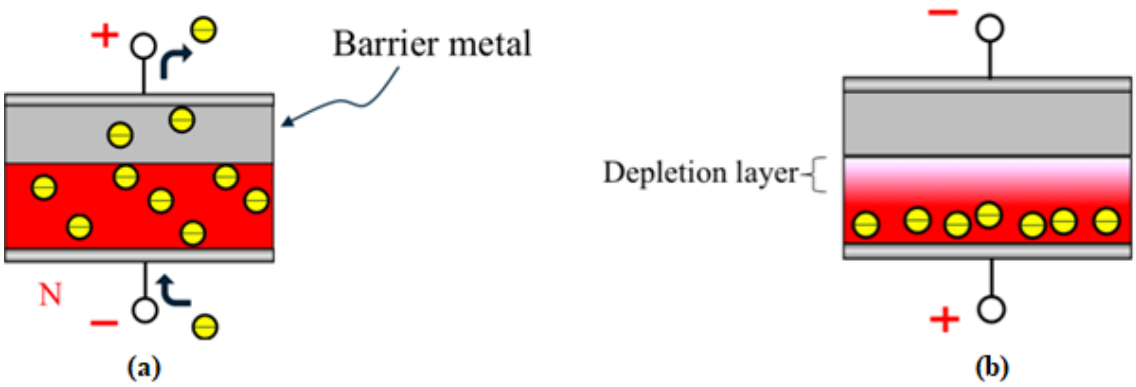

Figure 2. SBD Physical Structure of forward bias (a) and reverse bias (b) [18].

3.1.1 Static Characteristic

Static characteristic of schottky diode is also refer as the current-voltage(I-V) characteristic. Schottky diode has voltage drop because of the metal-semiconductor junction. This voltage drop is usually between 0.2-0.8V. When forward voltage applies, the voltage level which is on the diode, reduces and electron flow as well as current flow begins. Schottky diode is majority carrier diode so just electrons flow into metal from semiconductor. When reverse voltage applies thanks to majority carriers due to lacking of holes, the electron flow stops nearly immediately(at picosecond levels). Junction equation explains the relationship between Current and Voltage on the barrier diode.

The I-V characteristic is being represented as in the figure below. It looks like conventional P-N junction diode characteristic whereas barrier diode has much lower ON voltage. When forward voltage reaches ON level, current rises exponentially. On reverse characteristic, current is stable at the leakage current level. When it reaches breakdown voltage, current jumps immediately. The I-V characteristic can be seen in the figure below. It also includes the comparison between conventional P-N junction diode.

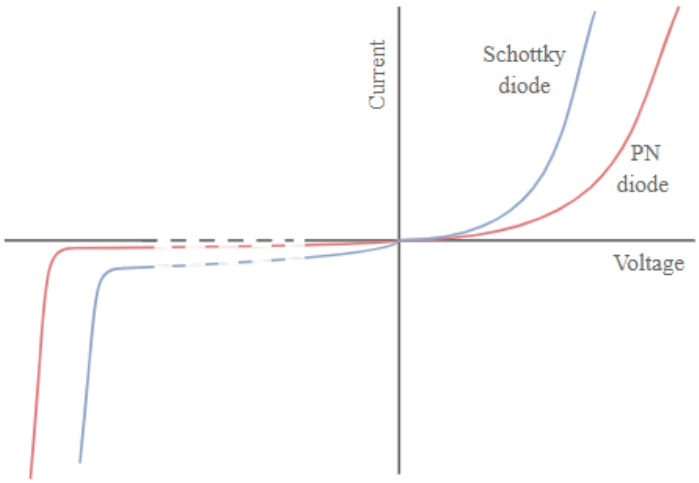

Figure 3. I-V Characteristic of SBD vs. PN [13]

The junction equation which gives the expression of current flows through the diode;

$$I = I_{SAT}(e^{\frac{q(V-IR_S)}{\eta KT}} - 1) \quad (1)$$

where k = Boltzmann's constant, $1.38044\,x\,10^{-23}\,J/K$; q = electronic charge, $1.60206\,x\,10^{-19}$; T = Temperature, K; R_S = series resistance, Ω; I_{SAT}= saturation current, A; η = ideality factor (typically 1.0) and

$$I_{SAT} = AA ** e^{(\frac{q\phi_B}{kT})} \quad (2)$$

where A = area, cm^2 A^{**} = Modified Richardson constant, $(A/K)^2/cm^2$; k = Boltzmann's Constant; T = absolute temperature, K; ϕ_B= barrier height, V. [20]

The use of a guard ring in the fabrication of the diode has an effect on its performance in both forward and reverse directions. Both forward and reverse characteristics show a better level of performance. However the main advantage of incorporating a guard ring into the structure is to improve the reverse breakdown characteristic. There is around a 4:1 difference in breakdown voltage between the two - the guard ring providing a distinct improvement in reverse breakdown. Some small signal diodes without a guard ring may have a reverse breakdown of only 5 to 10 V [21].

3.1.2 Transient Characteristic

Resulting of being majority carrier devices, Schottky diodes have high switching speed. Whereas fluctuations might have been happening on the voltage and current outputs because of the parasitic effect of capacitance and inductance.

3.1.3 Key Parameters

There are number of key parameters of Schottky Diodes in order to taken into account before using them. These parameters define the characteristics of the diodes. These parameters effect on how diodes react in the circuits and how they response at certain current or voltage levels.

The Schottky diode is a majority carrier device. This gives it tremendous advantages in terms of speed because it does not rely on holes or electrons recombining when they enter the opposite type of region as in the case of a conventional diode. By making the devices small the normal RC type time constants can be reduced, making these diodes an order of magnitude faster than the conventional P-N diodes. This factor is the prime reason why they are so popular in radio frequency applications. [21]

Forward Voltage Drop= It is also called by turn-on voltage. As it can be seen at the figure 19, diode needs a certain voltage in order to start a current flow through it. Which is also same as the voltage drop between metal and semiconductor. This voltage level is usually around 0.2V for schottky barrier diode.

Reverse Breakdown Voltage= As in the I-V characteristic of SBDs, they do not have high breakdown voltage. If this breakdown voltage exceeded, diode breaks down and starts conducting in the reverse direction is called Reverse Breakdown Voltage.

Reverse Recovery Time= Reverse recovery time is the time being passed while diode conducts from ON state(forward conduct) to OFF state(reverse conduct). Reverse recovery time is the most important difference between PN junction diodes and Schottky -barrier diodes. In a typical PN-junction diode reverse recovery time can vary from several microseconds to 100 nanoseconds. Schottky diodes recovery time is at picosecond levels, because Schottky diode doesn't have a depletion region at the junction.

- Qrr (Reverse Recovery charge)= There is a charge that stored on the diode while being ON state and behaves just like capacitor. While switching from ON to OFF state, Qrr is needed to be removed. The time being passed while Qrr is removed is majorly effects the reverse recovery time. That is why it can be said that; Reverse Recovery time is mostly determined by the barrier capacitance.

- During discharge, diode conducts and this causes a switching loss.

Reverse Leakage Current= Current flows through diode while it is OFF state. Schottky diode has higher leakage current compared to the PN junction diodes. Leakage current rises significantly while temperature being risen.

Series Resistance= The series resistance of a Schottky diode is the sum of the resistance due to the epi layer and the resistance due to the substrate. The resistance of the epi is given by the following equation:

$$R_{epi} = \frac{L}{q\mu_N N_D A} \quad (1)$$

where L = thickness of epi in cm μN = mobility of electrons for n-type Si (for p-type silicon the mobility of holes would be used) N_D = doping density of the epi layer in

$atoms/cm^3$ A = area of Schottky contact in cm^2. The resistance of the substrate is given by the following equation:

$$R_{sub} = 2 * \rho_S * (A/\pi)^{1/2} \quad (2)$$

Where ρ_S = substrate resistivity in Ω-cm. [21]

Capacitance= The capacitance parameter is one of great importance for small signal RF applications. Typical values of a few picofarads are normal. The Schottky diode can be imagined as a parallel-plate capacitor. The capacitance of this region is determined by the physical dimensions of the junction as well as the doping profile of the semiconductor layer. The thickness of the depletion layer can be affected by the magnitude of an externally-applied voltage: a forward bias will reduce the thickness of the depletion layer, effectively moving the plates of the capacitor closer together; and, a reverse bias voltage increases the thickness of the depletion layer, effectively spreading the parallel plates farther apart. The relationship between reverse bias voltage and diode capacitance is;

$$C_j(V_R) = \frac{C_j(0)}{(1-\frac{V_R}{V_I}-\frac{kT}{q})^{\frac{1}{2}}} \quad (3)$$

where $C_j(V_R) =$ junction capacitance at reverse bias voltage V_R ; V_R = reverse bias voltage from external voltage source; $C_j(0)$ = junction capacitance with $V_R = 0\ V$; V_I = internal contact potential = ϕ_B-0.15 for n-type silicon k = Boltzmann's constant; T = absolute temperature; q = charge of an electron.[21]

Schottky Barrier Diode behaves like a capacitor. During ON state there is a charge is stored which is determined by the Qrr parameter. SBD bahaves like a capacitor and during switching, it helps to be faster than the PN junction diodes.

3.2 Merged PiN Schottky Diodes

Merged PiN Schottky diodes behave like two different diodes. During ON state, it behaves like Schottky diode, during OFF state, it behaves like PiN diode.

In the Figure 4, it can be seen that, SiC MPS diode operating forward bias on the left and operating reverse bias on the right. SiC MPS diode includes both Schottky-metal contact

and hole injection areas. In most cases, below 3 Volt, conduction is just at schottky areas and that is why during this condition diode behaves as Junction Barrier Schottky Diode.

There are a few important features that defines the behaviour of On and Off state voltage drop characteristics.

- Resistance of Heavily P+ doped area
- Dimensions of metal contact
- Dimensions of drift region

During reverse bias situations, due to the heavily p+ doped drift region, the leakage current rises from the metal contacts.

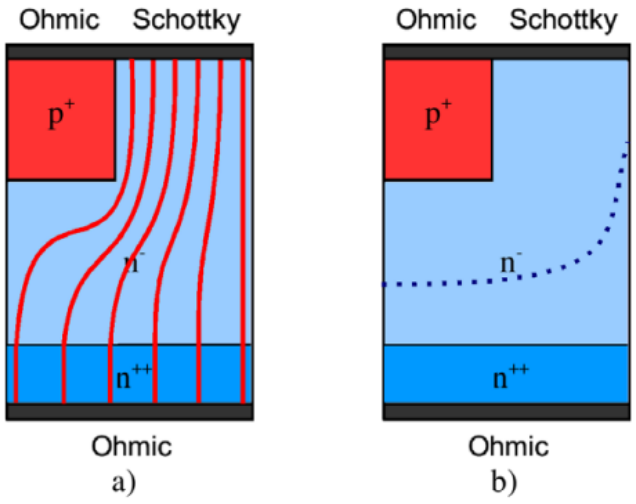

Figure 4. ON-state JBS diode, lines show current flow (a) OFF-state JBS diode, dotted line shows the edge of depletion region (b) [16].

3.2.1 Static Characteristic

Under forward bias condition there are two operation modes JBS and MPS. These modes are determined by the forward bias voltage level;

- **JBS Mode=** If bias voltage is below a level, only Schottky region conducts. At this moment, the diode works like Schottky diode. This type of situation is called JBS mode.

- **MPS Mode=** When bias increases from JBS mode, minority carriers causes a conduction in the drift layer. This situation is called as MPS mode.

Under reverse bias condition Diode behaves like PN junction diode. That is why the leakage current is lower than the SBD diode.

3.2.2 Transient Characteristic

Unlike PiN diodes, SiC MPS diodes do not need to discharge the carriers during reverse bias. This feature brings superiority in terms of switching speed. At the high forward voltage level, the switching might be slower than low forward voltage levels because diode uses same minority carrier charge.

3.3 Comparison of Schottky Barrier and MPS/JBS Diodes

In the Table 3, physical fundamentals and diode parameters of Schottky Barrier Diode and Merged PiN Schottky/Junction Barrier Schottky Diode are compared.

Table 3. Comparison of SBD vs. MPSD/JBSD.

Schottky Barrier Diode(SBD)	MPSD/JBSD
Physical Fundamentals	
There is only N semiconductor	There are N and P semiconductor
It has, N- drif region and N+ substrate	It has, P+ in the N- dift region and N+ substrate
It is minority carrier diode	It is both minority and majority carrier diode
It has metal part	It has metal part
There is metal-semiconductor junction	There is metal-semiconductor junction
There is only Schottky contact	There is both Schottky and Ohmic contact
Behaves Schottky-like ON and OFF state	Behaves Schottky-like ON state, PiN-like OFF state
Diode Parameters	
Leakeage Current is high	Leakage current is low
Reverse Recovery is faster	Reverse Recovery is slower
Reverse Breakdown voltage is lower	Reverse Breakdown voltage is higher
Low Forward voltage drop	Low Forward voltage drop
High blocking voltage	High blocking voltage

3.4 Application

Every design engineer has to select the right Schottky diode according to the need of his application. For rectification designs, a high voltage, low/medium current, and low frequency rated diodes will be required. For switching designs, the frequency rating of the diode should be high.

4 DIODE MODELLING AND SIMULATION

4.1 Introduction

In this section, Silicon Carbide Merged PiN Schottky Diode model design and transient characteristic optimization is taken place. Diode model design is made with fabrication design, process simulation and device simulation. Results of design and transient characteristic are presented by the results visualization tool.

Simulation and diode modelling play key role in terms of semiconductor process and device production. Accurate simulation results of complete design gives a vital input for final product. For simulation and diode modelling in this study Silvaco TCAD tool is being used. There are number of TCAD(Technology Computer Aided Design) simulation, modelling and analog circuit tools are avaible for use. Advantage of Silvaco TCAD is that, it brings whole life cycle process of devices in one platform. From semiconductor fabrication and physical fundamentals to electrical behaviours and data visualisation problems can be solved in this tool.

4.2 Familiarization with SILVACO TCAD

Silvaco's TCAD modelling services provides a solution for users who have unique semiconductor device modelling requirements but do not have the time or resources to operate TCAD software in-house. Using TCAD modelling service provides access to Silvaco's expertise in semiconductor physics and TCAD software operation to provide a complete, fast, and accurate solution. [23]

Typical applications[23];

- Physical etch and deposition process simulation
- Calibration of doping profiles and MOS/Bipolar transistors
- Modelled effects include self-heating and thermal gradients for power device
- Single Event Effect, Total dose simulation
- Stress simulation

Silvaco TCAD includes a couple of TCAD Interface tools. These tools are interactive deck development and run time environment. “Deck Build“ is single simulation runtime environment. “Virtual Wafer Fab(VWF)“ is multi-run desing of experiment environment.

Silvaco Deck Build suggests 3 main modules in terms of concluding the workflow. These are Process Simulation, Device Simulation and Result Visualization.

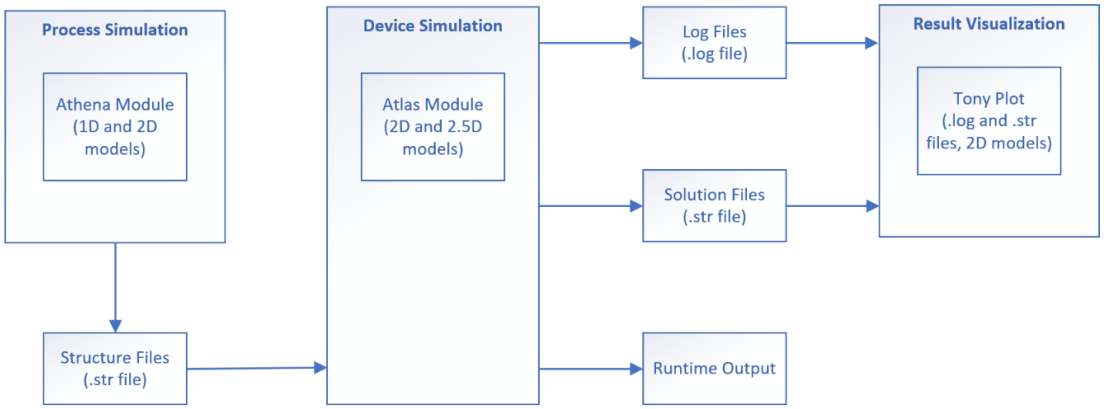

Figure 5. Workflow of Silvaco Deck Build

Process Simulation; This module simulates the semiconductor fabrication process. Material type, geometry, area definition, physical constant values and doping profiles are defined with process simulation. The module of process simulation is called as “Athena“. It generates “structure file(.str)“ as a output of Athena module in order to be used as a input of Device Simulation module.

Device Simulation; This module simulates the behaviour of device. Circuit and measurement description is being made according the structure file of process simulation. Submodel selection is done in this module. For example; the user can apply device voltage and module gives solutions which are electrical curves. The module of device simulation is called as “Atlas“. Atlas has capability of semiconductor fabrication process as well. The outputs of Atlas are log files(.log), solution files(.str) and runtime output.

Result Visualization; Log files and solution files generated by device solution can be investigated by user. The module named “Tony Plot“ opens the log files and structure files in order to visualize the information.

Structure Files(.str); Structure file describes how the micro structure of the device looks like.

Log Files(.log); It can be Electrical curves, I-V curves, photo response, output beam, etc.

Solution Files(.str); It can be electrical field distrubution.

Runtime output; Mostly used for diagnose the code being put in the device simulation.

4.3 Challenges of Using TCAD

There are number of challenges of using TCAD programs alongside many advantageous;

- Good understanding of the physics involved in the device technology. Numerous of questions should be answered before using the program. For instance; how the carriers flow in the device? What is the majority/minority carrier? What is the recombination rate? What is the lifetime, scattering. etc.
- Knowing the materials and process as detailed as possible. For example; If a doped wafer will being used, dopant, doping concentration and orientation of the wafer must be known.
- Being aware of the learning curve.
- Understanding the trade-offs between accuracy and simulation time. Spending time of the simulation can be too long.

4.4 Diode Modelling

In this thesis work, one Silicon Carbide Merged PiN Schottky Diode model design is proposed, based on a the model is defined in the paper[24]. In the below sections, physical parameters are extracted and model definition is being made. The aim of the proposed model is to achieve higher switching frequency at the reverse recovery situation. Parameters which are inputs of the device simulation are listed. These parameters define the structure files, log files and solution files.

4.4.1 Base Diode Model

In the Figure 6, physical model of the base "4H-SiC Merged PiN Schottky Diode" is presented. Proposed mode is prepared based on this model and at the further sections the output files/graphs shall be presented.

Device simulation tool of Silvaco is used to simulate the design. The two p-type injections used in 4H-SiC MPS diodes and the formed structures are as follows: high concentration doping (P+) forms the P+iN region in the active region and P+ transition region, and low concentration doping (P−) forms the P− transition region and three rings. It should be noted that the contact type of each region in the baseline structure is different, and the p-type region is ohmic contact, while the n-type region is Schottky contact. [24] Doping concentration of n-SiC Epitaxial Layer is $8e15cm^{-3}$. n-SiC Substrate layer doping concentration is $1e19cm^{-3}$.

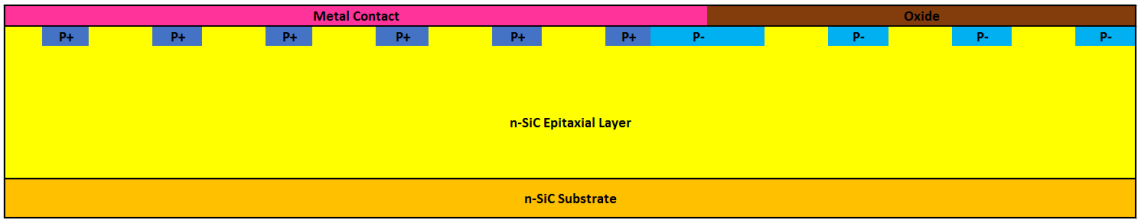

Figure 6. Base SiCMPSD Physical Model [24].

Physical distances of the each areas are given in the Table 4;

Table 4. Physical Distances of Regions

Region	**Distance**
Metal Contact	W: 42.5 um
Oxide	W: 77.5 um
P+ Regions	W: 1.5 um, 2 um, 3 um D: 1.5 um
P- Regions (Guard Rings)	W: 34 um, 10 um D: 1 um
n-SiC Epitaxial Layer	W: 120 um, D: 9 um
n-SiC Substrate	W: 120 um, D: 1 um

Design structure is developed with device simulation tool. Structure file output is generated by Silvaco Atlas module. Unit of X and Y axis are micron meter(um). In the structure file the doping concentrations of each region is also shown.

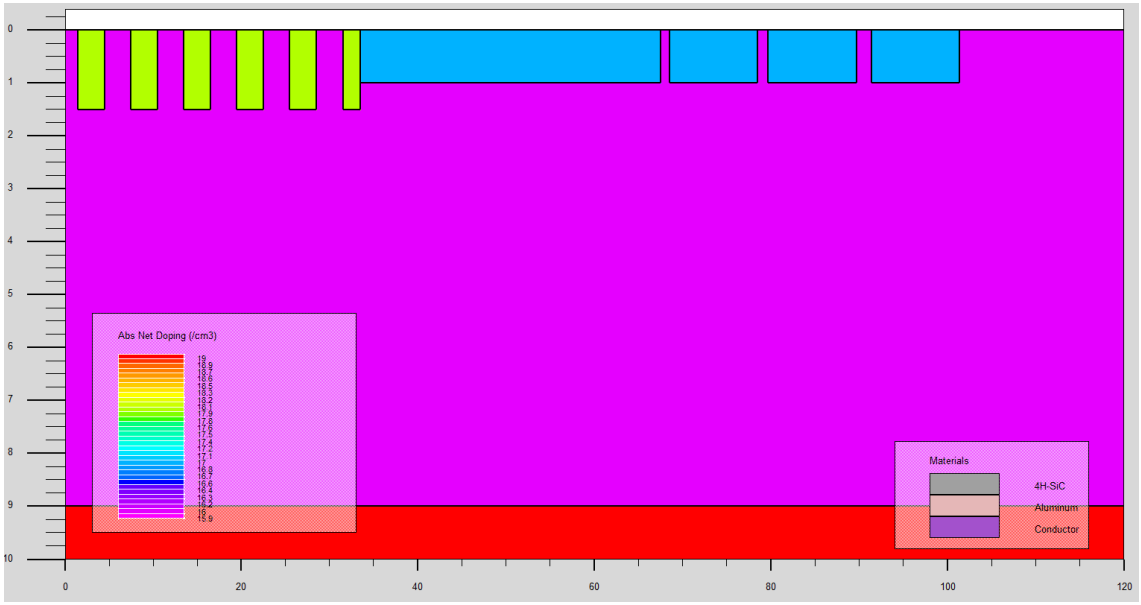

Figure 7. Structure Output File of Base Diode Design

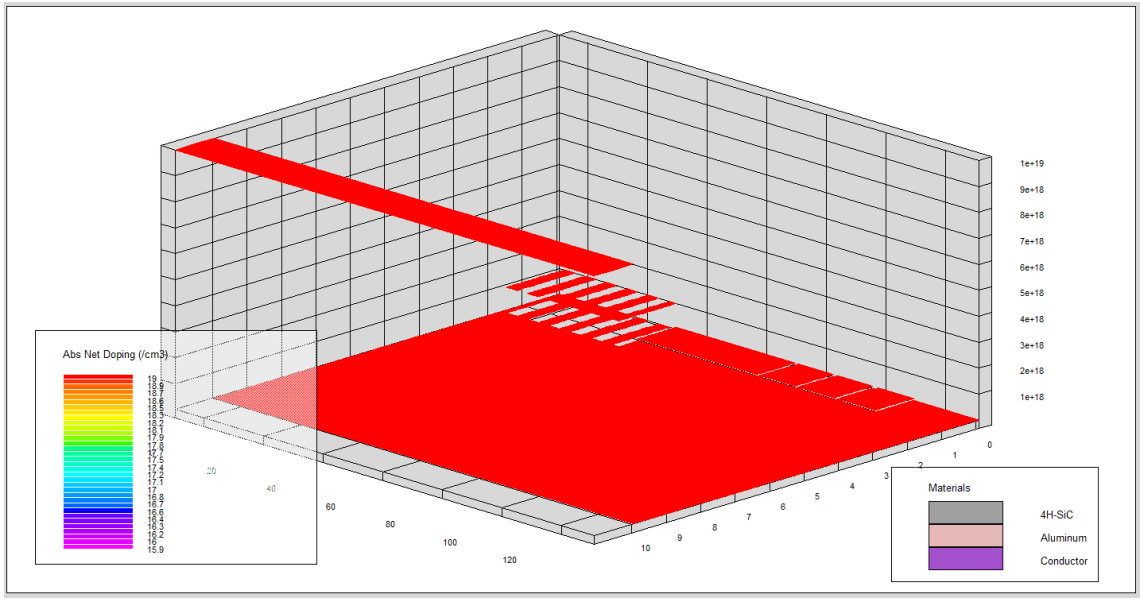

Figure 8. 2.5D Structure Output File of Base Diode Design.

4.4.2 Proposed Diode Model

In order to achive high reverse recovery response meaning that high switching frequency, a new design of a 4H-SiC Merged PiN Schottky Diode is proposed. This design is inspired by the base diode model which is presented at the section 4.4.1.

In the proposed diode model, two pieces P+ doped islands are added in the epitaxial layer of base diode model. Doping concentration of islands is $1e17cm^{-3}$. This islands are

called as “Controlled Injection of Backside Holes(CIBH)“. CIBHs are added in order to achive high dynamic ruggedness and low reverse recovery time.[25] Doping concentration of n-SiC Epitaxial Layer is $8e15cm^{-3}$. n-SiC Substrate layer doping concentration is $1e19cm^{-3}$

In the proposed model, structure of metal contact width is reduced from 42.5 micron meter to 12.5 micron meter and epitaxial layer depth is increased from 9 micron meter to 20 micron meter.

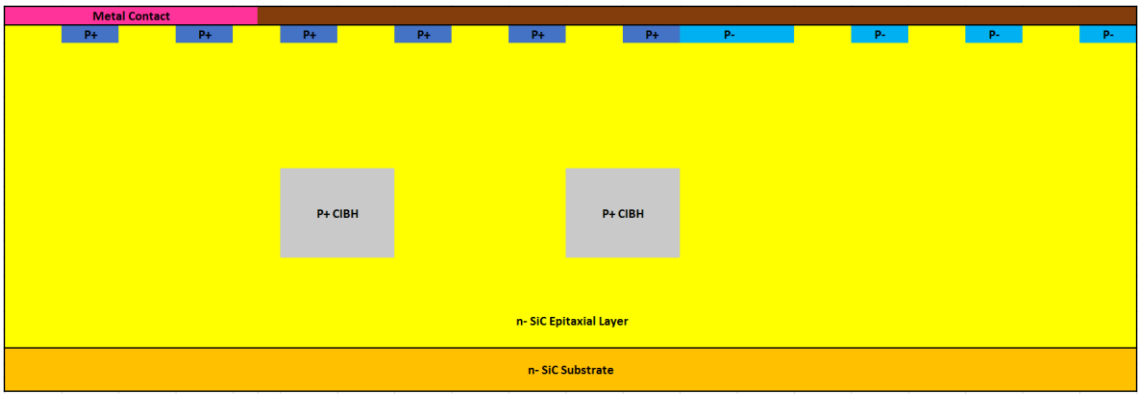

Figure 9 Proposed SiCMPSD Physical Model

Physical distances of the each areas are given in the Table 5;

Table 5. Physical Distances of Proposed Diode Model

Region	**Distance**
Metal Contact	W: 12.5 um
Oxide	W: 77.5 um
P+ Regions	W: 1.5 um, 2 um, 3 um D: 1.5 um
P- Regions (Guard Rings)	W: 34 um, 10 um, D: 1 um
P+ Regions (CIBH)	W: 10 um, D:2 um
n-SiC Epitaxial Layer	W: 120 um, D: 20 um
n-SiC Substrate	W: 120 um, D: 1 um

Silvaco structure file output with doping information is shown in the Figure 10 and Figure 11. Unit of X and Y axis are micron meter(um).

The comparison of physical dimensions between base model and proposed model can be seen in the Table 6.

Table 6 Physical Dimensions Comparison

Region	Base Model Dimensions	Proposed Model Dimensions
Metal Contact	W: 42.5 um	W: 12.5 um
Oxide	W: 77.5 um	W: 77.5 um
P+ Regions	W: 1.5 um, 2 um, 3 um D: 1.5 um	W: 1.5 um, 2 um, 3 um D: 1.5 um
P- Regions (Guard Rings)	W: 34 um, 10 um D: 1 um	W: 34 um, 10 um, D: 1 um
P+ Regions (CIBH)	N/A	W: 10 um, D:2 um
n-SiC Epitaxial Layer	W: 120 um, D: 9 um	W: 120 um, D: 20 um
n-SiC Substrate	W: 120 um, D: 1 um	W: 120 um, D: 1 um

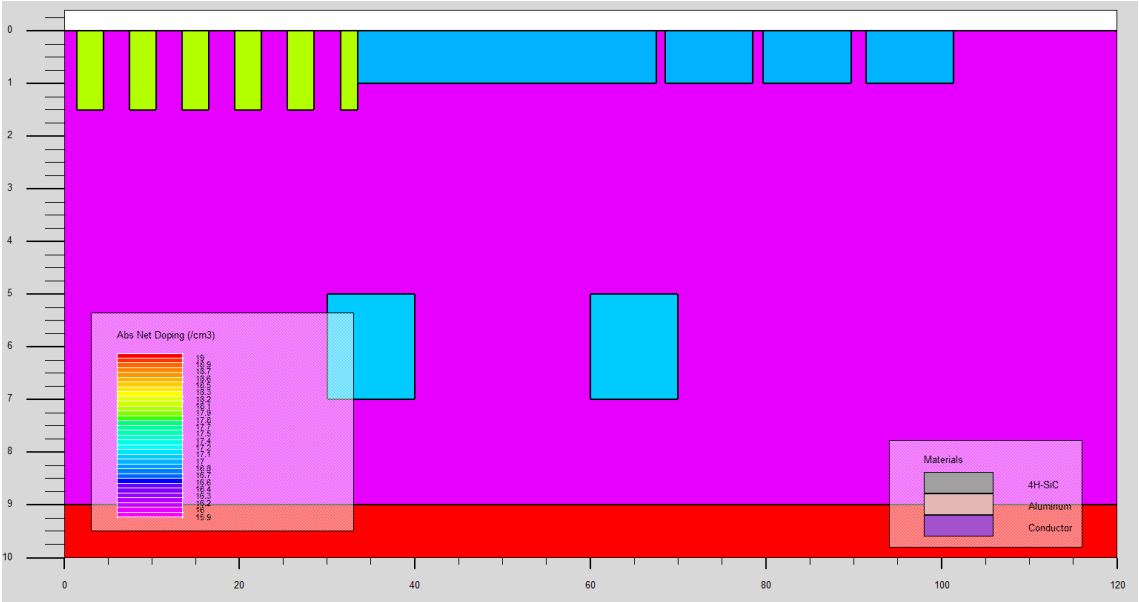

Figure 10. Structure Output File of Proposed Diode Design

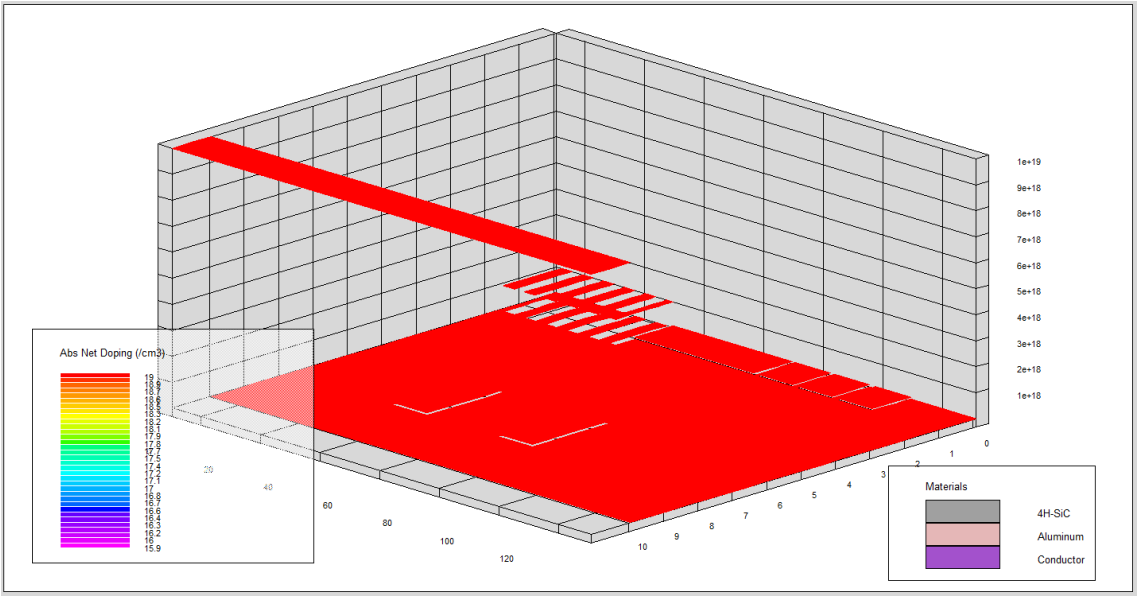

Figure 11. 2.5D Structure output file of Proposed Diode Design

Proposed SiC Merged PiN Schottky Diode design is made with Silvaco TCAD tool, Atlas device simulation tool.

Input deck of Atlas input file needs to be created with correct order of group statements.

Steps of the command groups can be listed as below;

1) Structure Specification Group consist of Mesh, Region, Electrode and Doping statements.

2) Material Models Specification Group consist of Material, Models, Contact and Interface statements.

3) Numerical Method Selection Group consist of Method statement.

4) Solution Specification Group consist of Log, Solve, Load and Save statements.

5) Result Analysis Group consist of Extract and Tonyplot statements.

Steps of the command groups, statements, physical parameters and Atlas tool software is explained followingly;

- **Mesh Definition;**

In order to define a structure of a device, firstly mesh shall be defined. Mesh represents the grid covers of the physical simulation domain. Mesh consists of lines in different axis and spacings between them. This lines can be divided into regions. Each region can be allocated with different materials and with their features. For example, for SiC diode, SiC material can be defined in desired areas of layers and doping levels can be arranged accordingly.

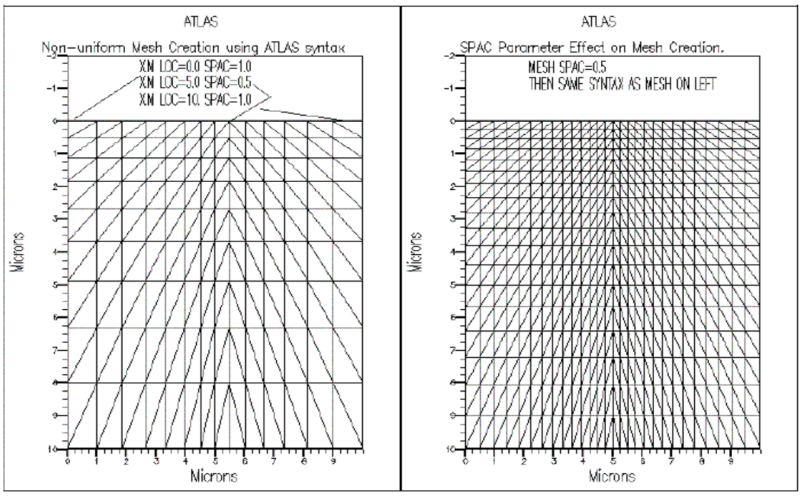

Figure 12. A Mesh Example [30]

In the proposed design mesh is defined by the Atlas module input deck. Input deck syntax as follow;

```
X.MESH LOCATION=<VALUE> SPACING=<VALUE>

Y.MESH LOCATION=<VALUE> SPACING=<VALUE>
```

In the proposed diode model, Atlas input deck is defined as;

```
#Mesh Define

x.m         l=0.0     spac=0.1
x.m         l=120.0   spac=0.1

y.m         l=0.0     spac=0.1
y.m         l=1.5     spac=0.5

y.m         l=9.      spac=0.5
y.m         l=10.     spac=0.5
```

With the #Mesh Define code group, in X axis, between 0 and 120 micron meter, each spacing of each mesh location is 0.1 micron meter.In Y axis between 0 and 1.5 micron meter, each mesh location is 0.1 micron meter. In Y axis between 1.5 and 10 micron meter, each mesh location is 0.5 micron meter.

Spacing values in the input deck is the most suitable one that have been found. Figure 13 represents the proposed design with mesh grids;

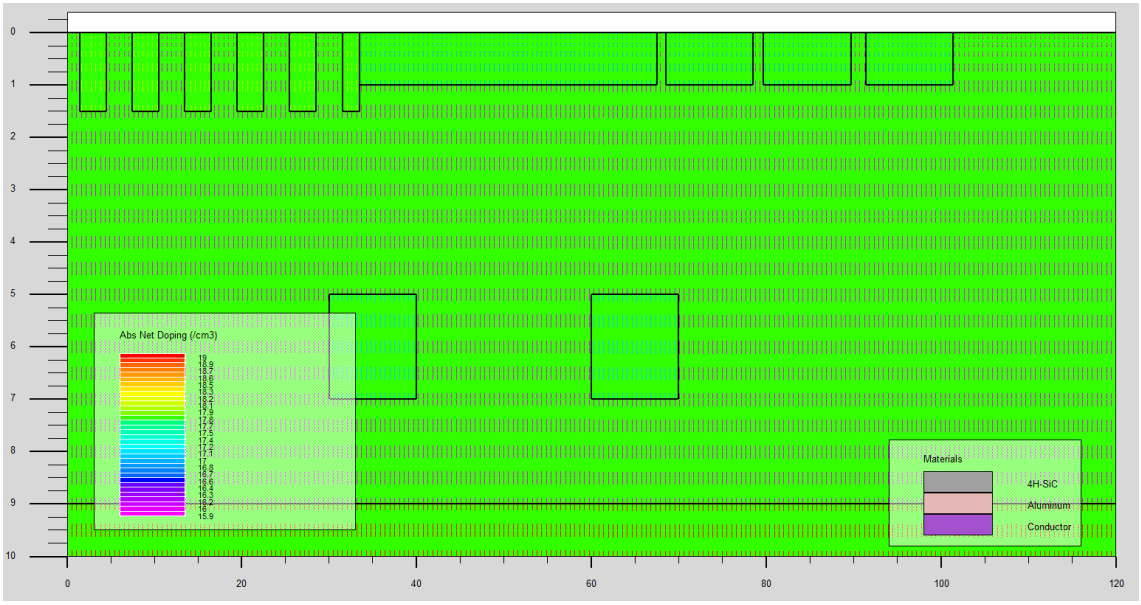

Figure 13. Proposed Mesh Design.

The run output of the proposed mesh design has got 28824 total grid points, 55200 total triangles, 0% obtuse triangles. Type of mesh is non-cylindrical.

Different spacing values are being tried out to achieve the most convenient outcome. Reducing the spacing value results lower grid points however after one point some degradation starts at the edges of each region.

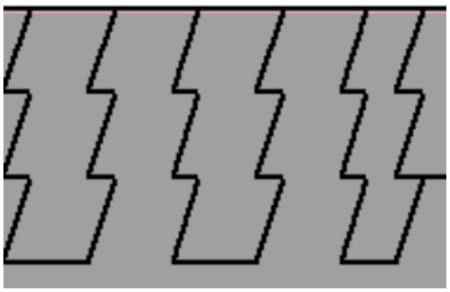

Figure 14. Degradation Example with Excessive Reduction

- **Region Definition**

Every region with specific material and doping concentration is specified by region definition. Atlas code syntax example of region definition;

```
REGION   number=<integer> <material_type> <position parameters>
```

Example region definition piece of code of Proposed model input deck;

SiC Epitaxial Layer Region;

```
Region num=1 material=4H-SiC x.min=0. X.max=120. Y.min=0. Y.max=20.0
```

SiC Substrate Layer Region;

```
Region num=2 material=4H-SiC x.min=0. X.max=120. Y.min=20.0 y.max=21.
```

For complete source code includes all regions, can be seen in the appendixe 1.

- **Electrode Definition**

Anode and Cathode electrodes are defined by electrode definition. In the proposed diode design, Anode width reduced from 42.5 micron meter to 12.5 micron meter. Anode is proposed as Aluminum. Cathode is lying on the bottom edge of the diode. Atlas code syntax example of electrode definition;

```
ELECTRODE NAME=<electrode name> <position_parameters>
```

Proposed diode model code of the electrode definition as follows;

```
electrode name=anode material=Aluminum x.min=0. X.max=12.5
electrode name=cathode bottom
```

- **Doping Definition**

Doping concentration of n-SiC Epitaxial Layer is $8e15cm^{-3}$. n-SiC Substrate layer doping concentration is $1e19cm^{-3}$ and Controlled Injection of Backside Holes(CIBH) islands is $1e17cm^{-3}$.

Atlas code syntax example of doping definition;

```
DOPING <distribution_type> <dopant_type> <position_parameters>
```

Proposed diode model example piece of code of doping definition as follows;

SiC Epitaxial Layer Region;

```
doping     region=1  uniform conc=8.0e15   n.type
```

SiC Substrate Layer Region;

```
doping     region=2  uniform conc=1.0e19   n.type
```

For complete source code includes all regions, can be seen in the appendixe 1.

- **Model Definition**

Physical models are specified using the MODELS statements. Parameters for these models appear on many statements including: MODELS, IMPACT, MOBILITY, and MATERIAL. The physical models can be grouped into five classes: mobility, recombination, carrier statistics, impact ionization, and tunneling. [26, p 74]

All models with the exception of impact ionization are specified on the MODELS statement. Impact ionization is specified on the IMPACT statement. For example, the statement:

```
MODELS CONMOB FLDMOB SRH FERMIDIRAC
```

specifies that the standard concentration dependent mobility, parallel field mobility, Shockley-Read Hall recombination with fixed carrier lifetimes, Fermi Dirac statistics and Selberherr impact ionization models should be used. [26, p 74]

Proposed diode model code of the model definition as follows;

```
models conmob fldmob consrh auger bgn

material taun0=5e-6 taup0=2e-6
```

4.5 Diode Simulation

In this section, transient analysis of Base and Proposed SiC Merged PiN Schottky Diodes are investigated. Reverse recovery response and switching characteristic results are compared.

4.5.1 Introduction

Reverse recovery time of diode is time taken when diode switch from forward bias(ON state) to reverse bias(OFF state). Idealy during diode should conduct from ON state to OFF state immediately but practically, there is a reverse current overshoot occur as a result. This period of time for Schottky diodes normally in nano seconds level.

Large amount of current flows on the diode in the reverse direction (Irr in Figure 15) during the reverse recovery time. Although the magnitute of current gets reduce in fairly small amount of time and gets saturated at the reverse saturation current level when the time-line reaches the reverse recovery time (trr) of the diode. Visually reverse recovery time can be described that between beginning of the reverse current thorugh peak time of the current untill 25% of Irr is the reverse recovery time. Negative peak time is called as time peak(tp) while decaying time is called as time decay(td). Mathematically reverse recovery time (trr) is the sum of tp and td.

Transient characteristic gives the information of the diode;

- Time duration between On and OFF state of the diode
- Showing the current/voltage magnitude differentiation of the switching period
- Transient behavior switching losses.

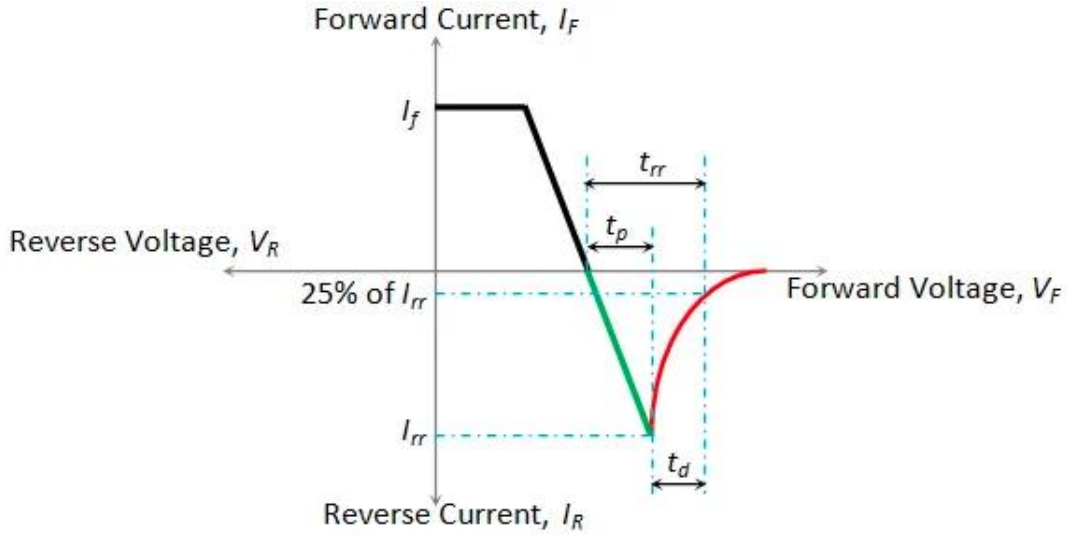

Figure 15. Reverse Recovery of Diode [28].

4.5.2 Simulation Results

As a simulation tool Tonyplot module of Silvaco TCAD is used. Tonyplot takes the log files and solution files as a input and gives the tonyplot 2D models as a result visualization output.

In the solution file, mixed mode simulation is used. The limitations of compact models can be overcome by using physically-based device simulation to predict the behaviour of some of the devices contained in a circuit. The rest of the circuit is modelled using conventional circuit simulation techniques. This approach is referred to as mixed-mode simulation, since some circuit elements are described by compact models, and some by physically-based numerical models. [26, p 729]

4.5.3 Forward I-V Curve Simulation Results

I-V curve of the forward bias simulation is executed on the base diode. Forward bias characteristic behaviour can be seen in the Figure 16.

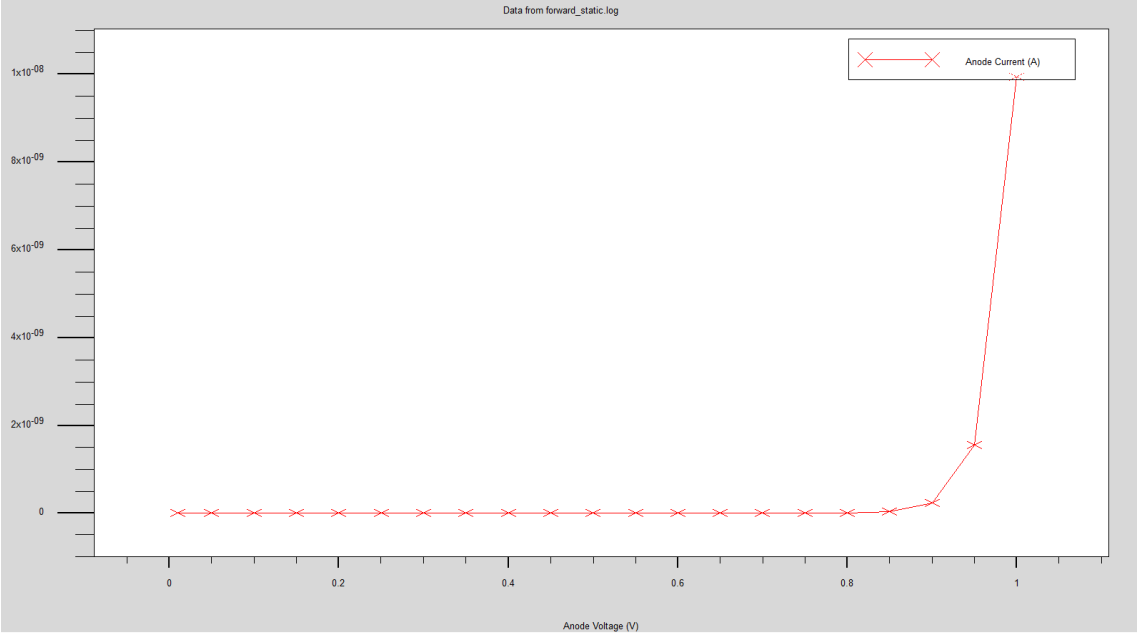

Figure 16 Forward Bias I-V Curve of Base Diode

I-V curve of the forward bias simulation is executed on the proposed diode. Forward bias characteristic behaviour can be seen in the Figure 17.

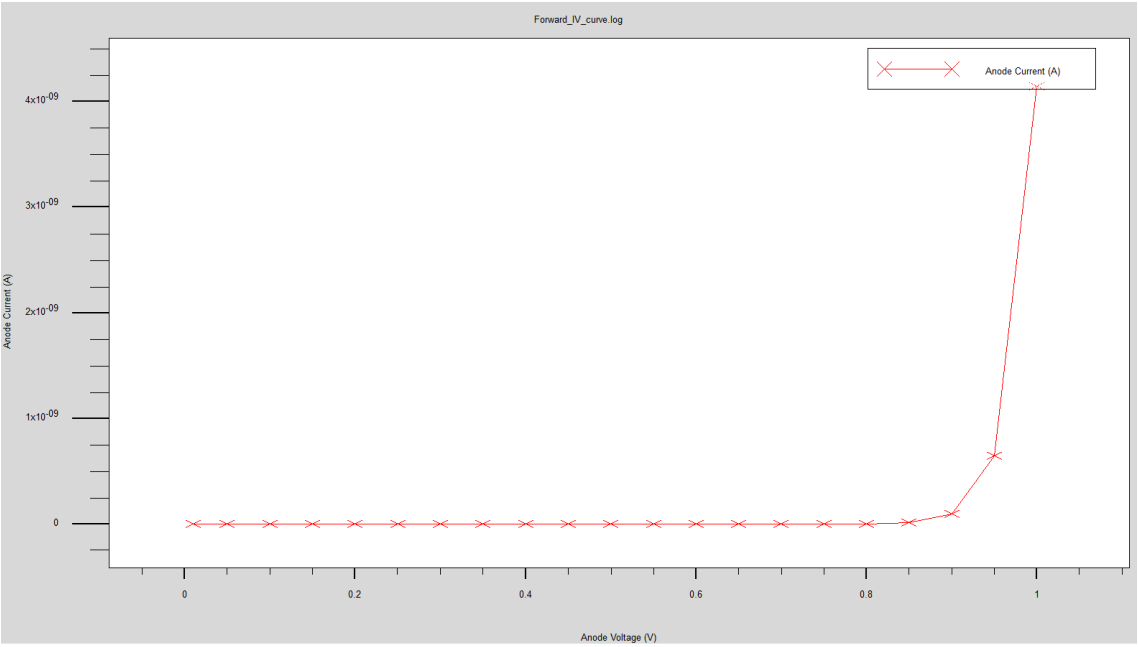

Figure 17. Forward Bias I-V Curve of Proposed Diode

In the Figure 18, comparison graph of forward I-V characteristics are given. Comparison made between proposed and base diodes. Curves are displayed as overlay mode of tonyplot. Green curve represents proposed diode model of forward bias I-V curve and red curve represents base diode model of forward bias I-V curve.

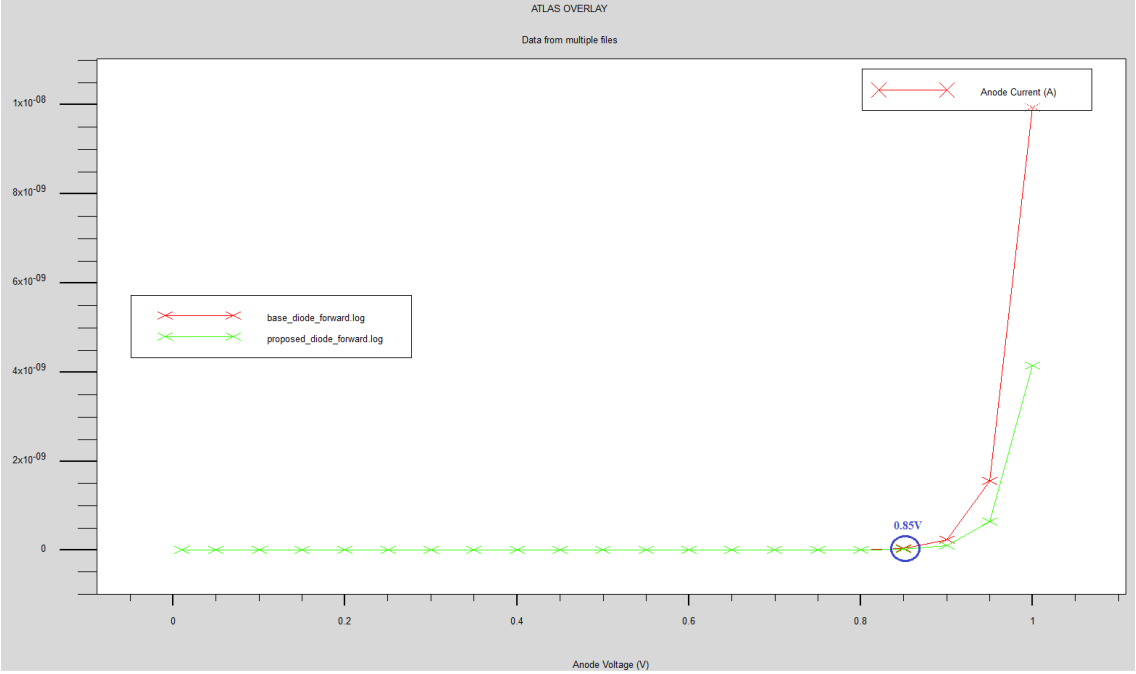

Figure 18 Forward I-V Curve Comparison of Base and Proposed Diode

As expected, after a specific forward voltage level, diode turns into ON mode. This voltage level is called as forward voltage (V_F) or threshold voltage (V_{th}) . Forward voltage of the both proposed and base diode is 0.85 Volt as it is in the Figure 18.

Forward bias I-V characteristic of base and proposed diode observed very much similar and forward voltage level where the diode behaviours ON state is 0.85V which is same both in proposed and base diode. After ON state, voltage level of proposed diode is slightly higher(0.01 levels). The reason behind that might be is metal contacts are smaller in the proposed diode. This might be effect of the Schottky like behaviour during ON state and forward voltage drop is smaller on Schottky diodes than PiN diodes.

Adding CIBH region seems like no major effect on forward behaviour of the diode. The reason behind that might be, total area of the epitaxial layer is relatively too high than CIBH region. Total area of epitaxial layer is 2400 um^2 and total area of CIBH regions are 40 um^2 . So that the epitaxial layer is 60 times larger than the CIBH region.

4.5.4 Reverse Recovery Simulation Results

A mixmode command set is used in the solution file as input of the simulation. There are predefined command sets for reverse recovery analysis. This command sets are used in the solution file. Below the explanation of this command sets and effects on the simulation is explained.

Command set in the solution file; [26, p 741]

```
1. go atlas
2. .BEGIN
3. V1 1 0 1000.
4. R1 1 2 1m
5. L1 2 3 2nH
6. R2 4 0 1MG EXP 1MG 1E-3 0. 20NS 10 200
7. IL 0 4 300
8. ADIODE 3=cathode 4=anode WIDTH=5.E7 INFILE=pd.str
9. .NUMERIC LTE=0.3 TOLTR=1.E-5 VCHANGE=10.
10..OPTIONS PRINT RELPOT WRITE=10
11.$
12..LOAD INFILE=pdsave
13..LOG OUTFILE=pd
14..SAVE MASTER=pd
15.$
16..TRAN 0.1NS 2US
17.$
18..END
19.$
20.MODELS DEVICE=ADIODE REG=1 CONMOB FLDMOB CONSRH AUGER
BGN
21.MATERIAL DEVICE=ADIODE REG=1 TAUN0=5E-6 TAUP=2E-6
22.IMPACT DEVICE=ADIODE REG=1 SELB
23.$
24.METHOD CLIM.DD=1.E8 DVMAX=1.E6
25.$
26.go atlas
27.tonyplot pd_tr.log
```

Explanation; [26, p 741]

Line 1: All Atlas input files should begin with GO atlas

Line 2: The .BEGIN and .END statements indicate the beginning and end of the circuit simulation syntax. These commands are similar to those used in SPICE.

Lines 3-7: Circuit components, topology, and analysis are defined within. Generally, the circuit component definition consists of three parts: the type of component, the lead or terminal mode assignments, and the component value or model name. For example, if the first component definition in this simulation is a DC voltage source, then V1 defines the component as voltage source number one, 1 and 0 are the two circuit modes for this component, and 1000 indicates that the voltage source value is 1000 volts. The remaining circuit components are resistors (R1, R2) inductor (L1) and independent current source (IL). The reverse recovery of the diode is simulated by dropping the value of output resistor R2 over a small increment of time. The R2 statement contains additional syntax to perform this task. Here, the resistor is treated as a source whose resistance decreases exponentially from 1 mOhm to 1 mOhm over the specified time step. This action essentially shorts out the parallel current source IL, which is also connected to the base of the diode.

Line 8: The ADIODE statement specifies a device to be analyzed by Atlas. The A part of the ADIODE command specifies that this is a device statement. The DIODE portion simply defines the device name. The option INFILE= indicates which device structure file is to be used.

Lines 9-10: These set numerical options for the circuit simulation. WRITE=10 specifies that every tenth timestep will be saved into the solution file specified on the .SAVE statement.

Line 12: Specifies a file generated by a previous MixedMode simulation to be used as an initial guess to the voltage.

Line 13-14: Specifies the output log and solution filenames. These names are root names and extensions will be added automatically by the program.

Line 16: Indicates the type of analysis required. In this case, it is a transient simulation lasting 2 microseconds with an initial timestep of 0.1 nanoseconds.

Line 18: Indicates the end of the circuit description. All following statements will be related to the Atlas device.

Lines 20-22: To completely specify the simulation, the physical models used by Atlas must be identified. Note that DEVICE=ADIODE must be specified for each line. The MODELS statement is used to turn on the appropriate transport models. This set includes:

- conmob: the concentration dependent mobility mode,
- fldmob: the lateral electric field-dependent mobility model,
- consrh: Shockley-Read-Hall recombination using concentration dependent lifetimes,
- auger: recombination accounting for high level injection effects,
- bgn: band gap narrowing.

The MATERIAL statement is used to override default material parameters. In this case, the carrier recombination fixed lifetimes are set. Finally, the Selberherr impact ionization model is enabled using the IMPACT statement with the SELB option.

Line 24: The METHOD statement specifies numerical options for the device simulation. The METHOD statement must come after all other device simulation statements.

Line 26: The command GO Atlas or a QUIT statement is needed to initiate simulation. Since a plot of the final log file is desired, the GO ATLAS option is used to restart Atlas after the end of the MixedMode simulation.

Line 27: The TonyPlot command is used to plot the resulting log file.

Command set in the solution file and structure file constitute the complete input deck. With the output of input deck transient analysis, switching speed and reverse recovery response of the base and proposed design of Silicon Carbide Merged PiN Schottky Diode are investigated and compared.

In the following headlines, reverse recovery responses are presented for each parameter changings separately. Comparison graphs are given following the relevant parameter changing. Finally Base and Proposed diode reverse recovery responses are compared.

Transient Response of Base SiC Merged PiN Schottky Diode Model;

In the Figure 19 reverse recovery characteristic of base model is given.

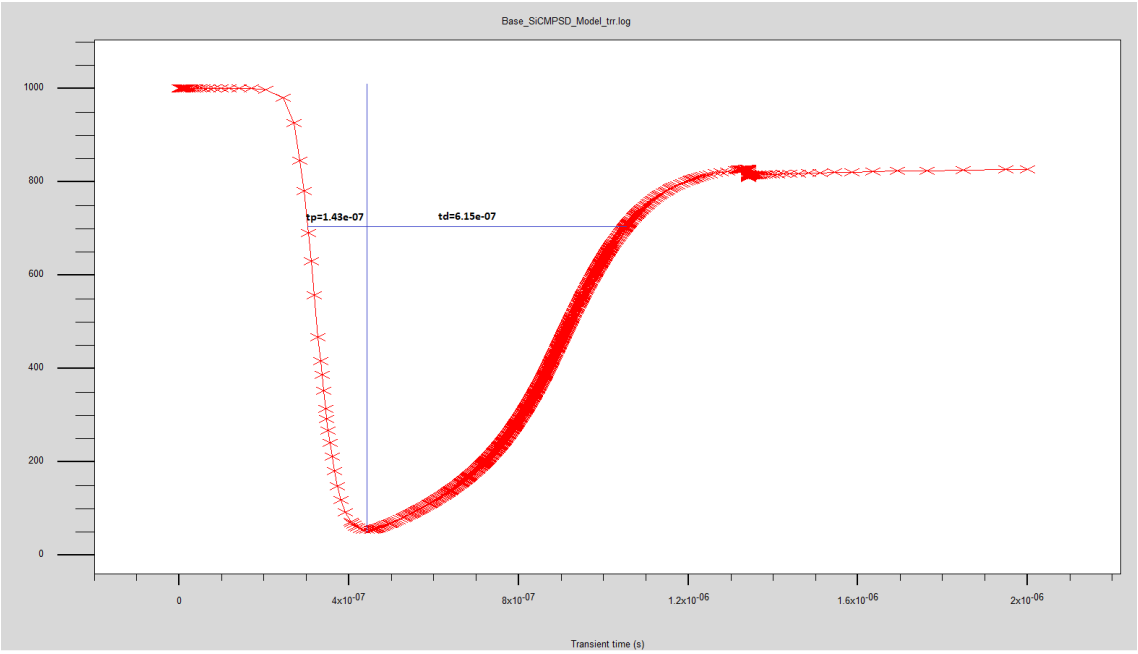

Figure 19. Reverse Recovery of Base SiC MPSD

Peak time(tp) of base diode reverse recovery response is 1.43e-07 seconds. Decaying time(td) of base diode reverse recovery response is 6.15e-07 seconds. Total time of reverse recovery response of base diode is 7.68e-07 seconds equals to 768 nano seconds.

Tp= 1.46e-07 sec.

Td= 6.15e-07 sec.

Trr= Tp + Td = 1.46e-07 + 6.15e-07

Trr= 7.68e-07 seconds = 768 nano seconds

Epitaxial Layer Changing Effect on Reverse Recovery Response

In the Figure 20, epitaxial layer dimension changing effect is investigated. Comparison made between base diode model and bigger epitaxial layer version of the base model diode. Epitaxial layer depth is increased from 9 micrometer to 20 micrometer.

Table 7 Dimension Comparison of Epitaxial Layer

Parameter	Base Diode Model	Proposed Diode Model
n-SiC Epitaxial Layer	W: 120 um, D: 9 um	W: 120 um, D: 20 um

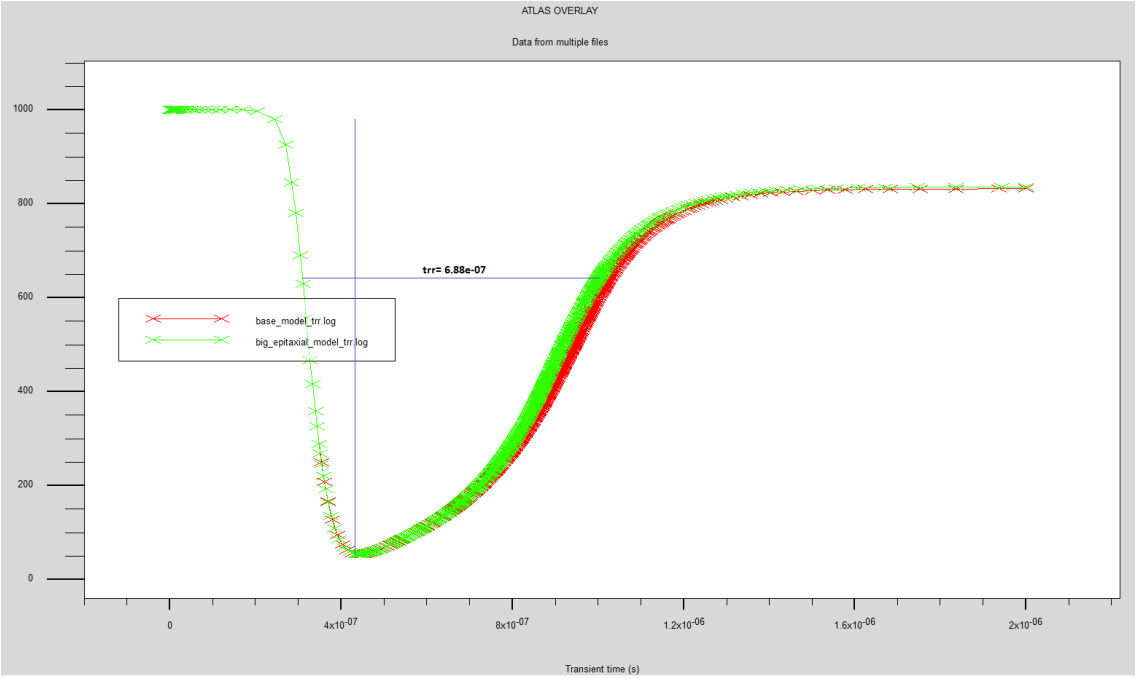

Figure 20. Base Diode Model vs. Bigger Epitaxial Layer Base Diode Model

In the Figure 20, red curve is base diode model and green curve is proposed(bigger epitaxial layer version of base model) diode model of reverse recovery characteristic. Proposed model behaviour has 80 nano seconds faster recovery time than base model.

Base model Trr= 7.68e-07 seconds = 768 nano seconds

Proposed model Trr= 6.88e-07 seconds = 688 nano seconds

CIBH Region Addition Effect on Reverse Recovery Response

In the Figure 21 CIBH region addition is investigated. Comparison made between base diode model and base model diode with embedded CIBH regions.

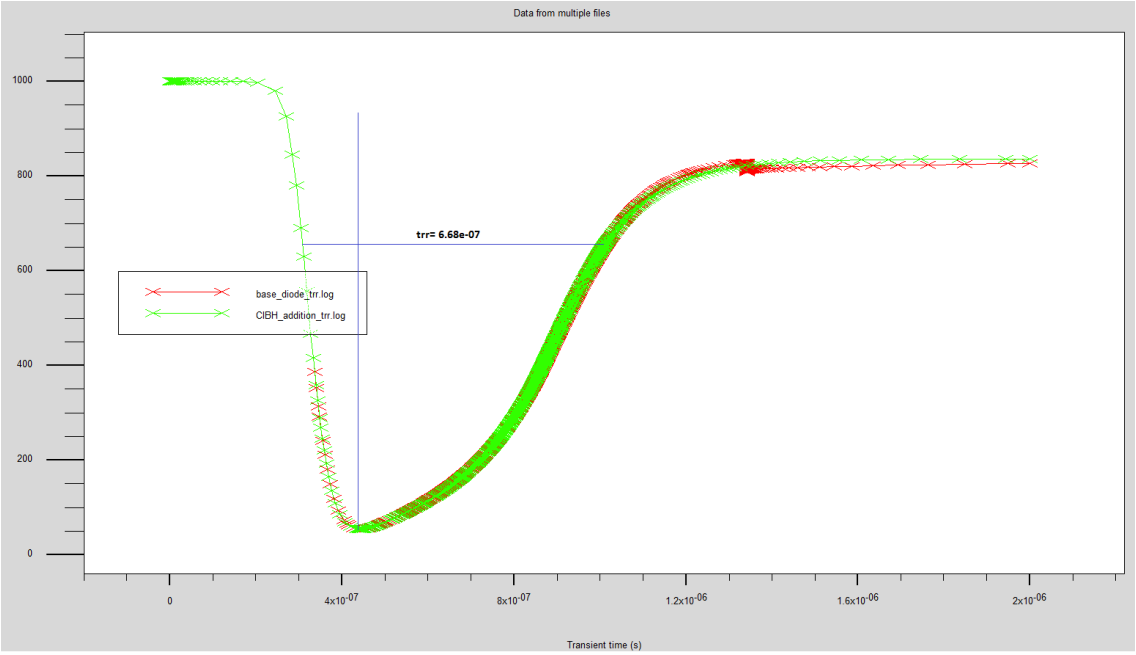

Figure 21. Base Diode Model vs CIBH Region Added Base Model Diode

In the Figure 21, red curve is base diode model and green curve is proposed(bigger epitaxial layer version of base model) diode model of reverse recovery characteristic. Proposed model behaviour has 100 nano seconds faster recovery time than base model.

Base model Trr= 7.68e-07 seconds = 768 nano seconds

Proposed model Trr= 6.68e-07 seconds = 668 nano seconds

Metal Contact Dimension Effect on Reverse Recovery Response

In the Figure 22 metal contact dimension changing effect is investigated. Comparison made between base diode model and 3 different metal contact dimension of the base model diode. Metal contact dimensions and reverse recovery times (trr) are given in the Table 8.

Table 8 Metal Contact Dimensions

Diode Model	Metal Contact Width	Curve Colour	Trr
First Try	3 um	Red	1.21e-07 ns
Second Try	12.5 um	Green	3.18e-07 ns
Third Try (Base Model)	42.5 um	Dark blue	6.54e-07 ns
Fourth Try	72 um	Light blue	6.78e-07 ns

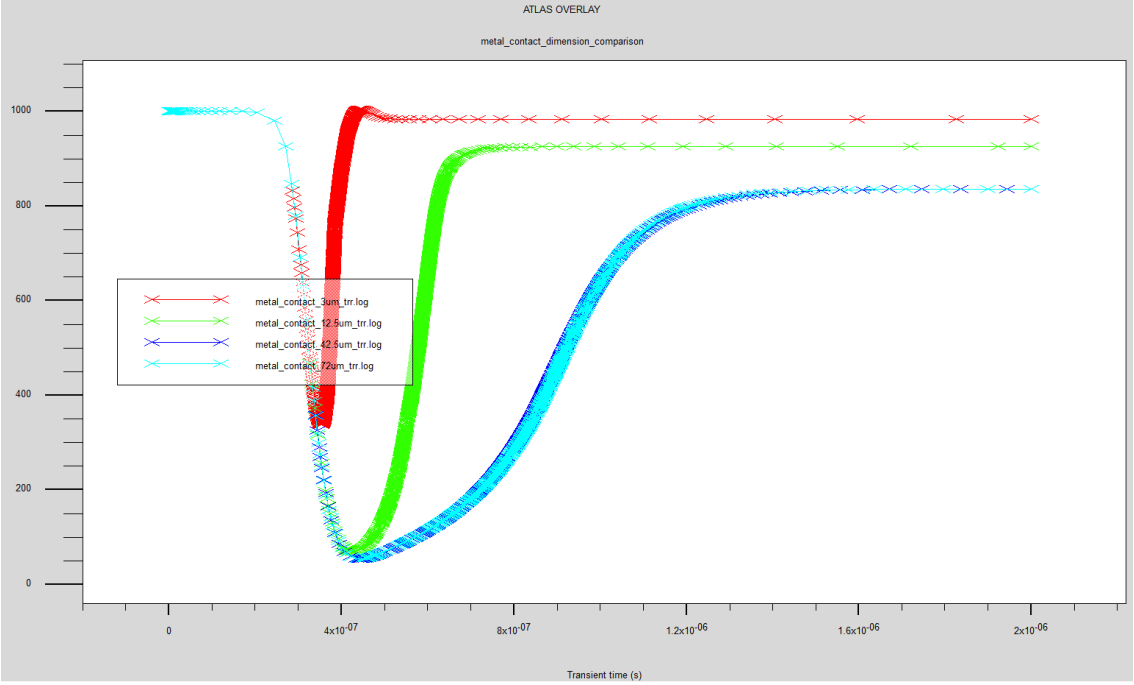

Figure 22. Base Diode Model vs. Three Different Metal Contact Dimensions

According to results in Table 8, first try with 3 micro meter metal contact has fastest reverse recovery. However, metal contact is too small to touch the desired P+ areas on the top of the diode. As it is shown in the Figure 6. Base SiCMPSD Physical Model [24]., each P+ areas are 3 micro meter and there is 1.5 micro meter hole before the forst P+ area. So 3 micro meter of metal contact is not long enough.

After first try, second try has the best reverse recovery time. It has long enough metal contact width and it touches at least 2 whole P+ areas on the top of the diode.

Third try is the base diode itself. Fourth try has worse reverse recovery time than the base diode. According to results, second try which has 12.5 micro meter metal contact has chosen as a proposed diode metal contact width dimension.

Transient Response of Proposed SiC Merged PiN Schottky Diode;

Proposed diode has 3 main different than the base diode. These differences are given in the section 4.4.2. Differences are; bigger epitaxial layer, 2 pieces CIBH region addition and smaller metal contact. Proposed diode consists of all these 3 main differences. In Figure 23 reverse recovery characteristic of proposed diode is investigated.

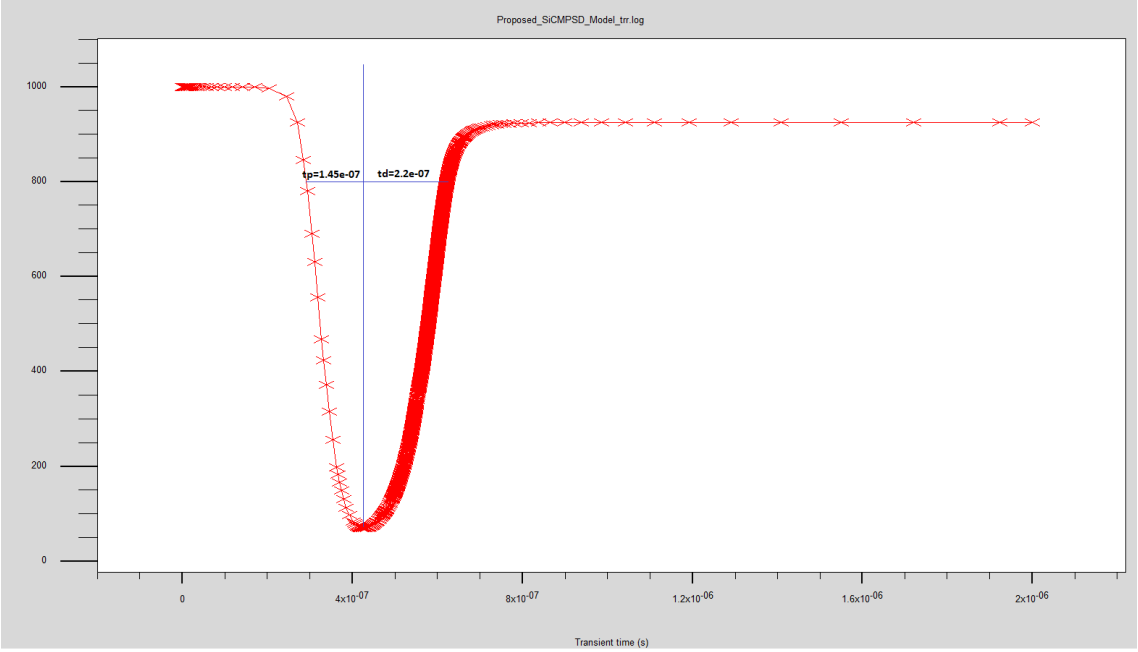

Figure 23. Reverse Recovery of Proposed SiC MPSD

Peak time(tp) of base diode reverse recovery response is 1.43e-07 seconds. Decaying time(td) of base diode reverse recovery response is 6.15e-07 seconds. Total time of reverse recovery response of base diode is 3.65e-07 seconds equals to 365 nano seconds.

Tp= 1.45e-07 sec.

Td= 2.2e-07 sec.

Trr= Tp + Td = 1.45e-07 + 2.2e-07

Trr= 3.65e-07 seconds= 365 nano seconds.

Transient Response Comparison between Base and Proposed SiC Merged PiN Schottky Diode;

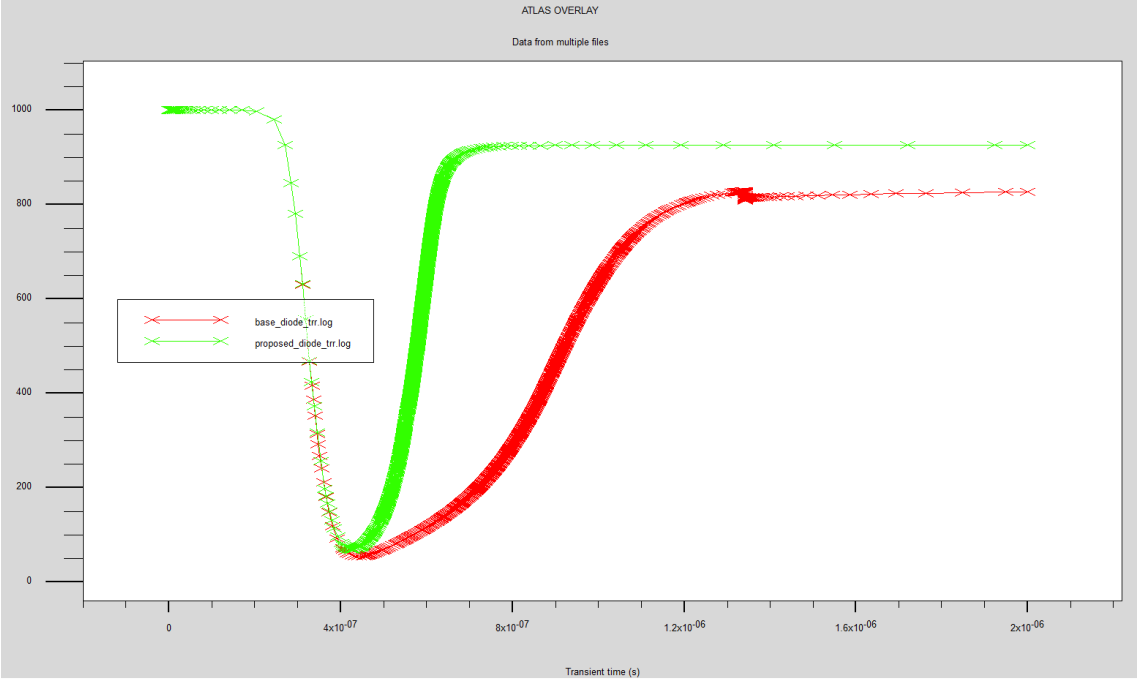

Figure 24 Comparison Between Base and Proposed Diode Models of Reverse Recovery Response

In the Figure 24. comparison of reverse recovery curves can be seen. Green curve represents reverse recovery behaviour of proposed diode model and red curve represents reverse recovery behaviour of base diode model. Atlas overlay feature is used for showing the different curves in one graph.

With the proposed diode model, reverse recovery time reduced from 768 nano seconds to 365 nano seconds. Reverse recovery time of base diode reduced by 52.47% of its initial reverse recovery time. As result with the proposed diode model, there is 52.47% improvement is achieved on the reverse recovery time.

5 Summary

This thesis work represents, SiC-MPSD proposed model design with Silvaco TCAD tool and simulation of design in terms of static/transient characteristic. Process and device simulation is executed with the Silvaco Atlas tool. Output files(Log files, structure files and solution files) are executed in order to verify and interpret the design. According to output files of Atlas tool, reverse recovery of diode design is studied in order to make optimization process to improve reverse recovery process of proposed diode design. Proposed design is inspired by the base design which is already defined as a SiC MPSD and details are explained in the section 4.4.1. Some physical properties of base diode are tuned which are reducing metal contact, increasing area of N- doped Epitaxial Layer and adding P+ doped Controlled Injection of Backside Holes (CIBH) into the epitaxial layer results improvement on reverse recovery response. Metal contact reduced from 42.5 micrometer to 12.5 micrometer. Depth of the epitaxial layer is increased from 9 micrometer to 20 micrometer. New 2 pieces p+ islands are added as CIBH regions. Dimensions of the CIBH regions are; width is 10 micrometer and depth is 2 micrometer. According to results the major effect on reverse recovery time is metal contact dimension among metal contact, CIBH region addition and enlarging epitaxial layer. Results showed that with the proposed design 52.47% improvement is achieved on the reverse recovery time compared to base diode.

5.1 Future Work

As a future work, reverse I-V characteristic of the SiC MPS diode can be investigated. An impact ionization model can be added in order to get the avalanche behaviour of the carriers.

During off state, SiC MPS diode behaves more like a PiN diode rather than a Schottky diode. This feature brings advantage to MPSD compare to normal Schottky diodes. Improving the PiN like features more, can be the initial ideas about the optimization of reverse I-V characteristic and breakdown voltage.

References

[1] A. R. Powell and L. B. Rowland, "SiC Materials Progress, Status, and Potential Roadblocks," Proc.IEEE, vol. 90, no. 6, pp. 942-955, 2002.

[2] P. G. Neudeck, R. S. Okojie, and L. Y. Chen, "High-Temperature Electronics-A Role for Wide Bandgap Semiconductors?," Proc.IEEE, vol. 90, no. 6, pp. 1065-1076, 2002.

[3] https://www.britannica.com/science/silicon-carbide

[4] http://accuratus.com/silicar.html

[5] G. R. Fisher and P. Barnes, "Toward a Unified View of Polytypism in Silicon Carbide," Phil. Mag., vol. 61, no. 2, pp. 217-236, 1990.

[6] [3] F. Bechstedt, P. Käckell, A. Zywietz, K. Karch, B. Adolph, K. Tenelsen, and J. Furthmüller, "Polytypism and Properties of Silicon Carbide," Phys. stat. sol. (b), vol. 202, no. 1, pp. 35-62, 1997.

[7] https://www.tf.uni-kiel.de/matwis/amat/semi_en/kap_a/backbone/ra_1_1.html

[8] G. L. Harris, Properties of SiC. EMIS Datareviews Series, no. 13, INSPEC, IEE, UK, 1995.

[9] G. Pensl, H. Morkoc, B. Monemar, and E. Janzen, "Silicon Carbide, III-Nitrides, and Related Materials," Materials Science Forum, vol. 264-268, pp. 3-89, 1998.

[10] S. M. Sze, Semiconductor Devices: Physics and Technology. John Wiley $ \&$ Sons, Inc., 2nd ed., 2002.

[11] C. M. Zetterling, Process Technology for Silicon Carbide Devices. EMIS processing series, no. 2, INSPEC, IEE, UK, 2002.

[12] A. Elasser and T. P. Chow, "Silcon Carbide Benefits and Advantages for Power Electronics Circuits and Systems," Proc.IEEE, vol. 90, no. 6, pp. 969-986, 2002.

[13] Nanying Yang, “Characterization and Modeling of Silicon and Silicon Carbide Power Devices,” pdf, Ph.D. Thesis , November 2010.

[14] B. J. Baliga, Power Semiconductor Devices, PWS Publishing Company, 1995.

[15] Zarębski and J. Dąbrowski, “SPICE modelling of power Schottky diodes,” International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, vol. 21, no. 6, pp. 551–561, Nov. 2008.

[16] A. Hefner, D. Berning, J. S. Lai, C. Liu and R. Singh, "Silicon carbide merged PiN Schottky diode switching characteristics and evaluation for power supply applications," Conference Record of the 2000 IEEE Industry Applications Conference (Cat. No.00CH37129), Rome, Italy, 2000, pp. 2948-2954 vol.5.

[17] https://www.futureelectronics.com/c/semiconductors/discretes--diodes--schottky-diodes/products

[18] https://www.shindengen.com/products/semi/column/basic/diodes/sbd.html

[19] Robert F. Pierret, Semiconductor Device Fundamentals, ADDISON-WESLEY Publishing Co. 1996

[20] FEATURE ARTICLE, Schottky Diodes by Rick Cory, Skyworks Solutions, Inc. FEBRUARY, 2009

[21] Oleksandr Veher, Natalja Sleptsuk, Jana Toompuu, “ The Dependence Of Reverse Recovery Time On Barrier Capacitance And Series-On Resistance In Sic Schottky Diodes“ pp. 16 Master Thesis 2017

[22] Tsunenobu Kimoto, James A. Cooper, “Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications“, Book,pp. 296, Nov 2014

[23] https://silvaco.com/services/tcad-services/

[24] A. Wang et al., "Analysis of Transient Surge Current Mechanism in SiC MPS Diode With the Transition Region," in IEEE Transactions on Electron Devices, vol. 68, no. 12, pp. 6330-6337, Dec. 2021, doi: 10.1109/TED.2021.3122403.

[25] H. Ma and Y. Wang, "Si MPS with CIBH Structure for Fast Recovery Applications," 2021 International Conference on IC Design and Technology (ICICDT), 2021, pp. 1-4, doi: 10.1109/ICICDT51558.2021.9626467.

[26] Silvaco Atlas User's Manual Device Simulation Software. August 26, 2016 edition.

[27] SILVACO International, 4701 Patrick Henry Drive, Building 1, Santa Clara, CA 95054, "ATLAS User's Manual," vol. 1, 2000.

[28] https://www.electrical4u.com/reverse-recovery-time-of-diode/

[29] https://circuitdigest.com/tutorial/schottky-diode-characteristics-parameters-and-applications

[30] Kim, Jaehong. (2022). Wide-Band and Scalable Equivalent Circuit Model for Multiple Quantum Well Laser Diodes.

Appendix 1 – Non-exclusive licence for reproduction and publication of a graduation thesis[1]

I Erkan Köprübasi

1. Grant Tallinn University of Technology free licence (non-exclusive licence) for my thesis "SIC MERGED PIN SCHOTTKY DIODE DESIGN WITH TCAD AND REVERSE RECOVERY OPTIMIZATION", supervised by Ants Koel
   1.1. to be reproduced for the purposes of preservation and electronic publication of the graduation thesis, incl. to be entered in the digital collection of the library of Tallinn University of Technology until expiry of the term of copyright;
   1.2. to be published via the web of Tallinn University of Technology, incl. to be entered in the digital collection of the library of Tallinn University of Technology until expiry of the term of copyright.
2. I am aware that the author also retains the rights specified in clause 1 of the non-exclusive licence.
3. I confirm that granting the non-exclusive licence does not infringe other persons' intellectual property rights, the rights arising from the Personal Data Protection Act or rights arising from other legislation.

09.05.2022

1 The non-exclusive licence is not valid during the validity of access restriction indicated in the student's application for restriction on access to the graduation thesis that has been signed by the school's dean, except in case of the university's right to reproduce the thesis for preservation purposes only. If a graduation thesis is based on the joint creative activity of two or more persons and the co-author(s) has/have not granted, by the set deadline, the student defending his/her graduation thesis consent to reproduce and publish the graduation thesis in compliance with clauses 1.1 and 1.2 of the non-exclusive licence, the non-exclusive license shall not be valid for the period.

Appendix 2 – Silvaco Input Deck Source Code of Proposed Diode Design and Electrical Characteristic Analysis

```
go atlas

#Mesh Define

mesh        rect    smooth=1 diag.flip

x.m         l=0.0    spac=0.1

x.m         l=120.0    spac=0.1

y.m         l=0.0     spac=0.1

y.m         l=1.5     spac=0.5

y.m         l=9.      spac=0.5

y.m         l=10.     spac=0.5

# Region Define

region        num=1     material=4H-SiC  x.min=0.  x.max=120.
y.min=0.    y.max=20.0

region        num=2     material=4H-SiC  x.min=0.  x.max=120.
y.min=20.0  y.max=21.

region        num=3     material=4H-SiC  x.min=1.5  x.max=4.5
y.min=0.    y.max=1.5

region       num=4    material=4H-SiC  x.min=7.5   x.max=10.5
y.min=0.    y.max=1.5
```

```
region       num=5    material=4H-SiC x.min=13.5 x.max=16.5
y.min=0.    y.max=1.5

region       num=6    material=4H-SiC x.min=19.5 x.max=22.5
y.min=0.    y.max=1.5

region       num=7    material=4H-SiC x.min=25.5 x.max=28.5
y.min=0.    y.max=1.5

region       num=8    material=4H-SiC x.min=31.5 x.max=33.5
y.min=0.    y.max=1.5

region       num=9    material=4H-SiC x.min=33.5 x.max=67.5
y.min=0.    y.max=1.

region      num=10    material=4H-SiC x.min=68.5 x.max=78.5
y.min=0.    y.max=1.

region      num=11    material=4H-SiC x.min=79.7 x.max=89.7
y.min=0.    y.max=1.

region     num=12   material=4H-SiC x.min=91.4 x.max=101.4
y.min=0.    y.max=1.

region    num=13   material=4H-SiC x.min=30 x.max=40 y.min=5
y.max=7

region    num=14   material=4H-SiC x.min=60 x.max=70 y.min=5
y.max=7

# Electrode Define

electrode name=anode material=Aluminum x.min=0. x.max=12.5

electrode name=cathode bottom

#Doping Define

doping     region=1  uniform conc=8.0e15 n.type
```

```
doping     region=2  uniform conc=1.0e19 n.type

doping     region=3  uniform conc=1.0e18 p.type

doping     region=4  uniform conc=1.0e18 p.type

doping     region=5  uniform conc=1.0e18 p.type

doping     region=6  uniform conc=1.0e18 p.type

doping     region=7  uniform conc=1.0e18 p.type

doping     region=8  uniform conc=1.0e18 p.type

doping     region=9  uniform conc=8.0e16 p.type

doping     region=10  uniform conc=8.0e16 p.type

doping     region=11  uniform conc=8.0e16 p.type

doping     region=12  uniform conc=8.0e16 p.type

doping     region=13  uniform conc=1.0e17 p.type

doping     region=14  uniform conc=1.0e17 p.type

# Model Define

models conmob fldmob consrh auger bgn

material taun0=5e-6 taup0=2e-6

# Contact Define

contact name=anode workfunc=4.7

contact name=anode RESISTANCE=1.0

# Methode Define

method newton trap

solve init
```

```
save outfile= SiCMPSD_struc.str

tonyplot SiCMPSD_struc.str

quit

# Forward I-V curve

log outfile=forward_static.log

solve vanode=0.01

solve vanode=0.05 vstep=0.05 vfinal=1 name=anode

tonyplot forward_static.log

go atlas

.begin

# Steady-state simulation of circuit with power diode

v1 1 0 1000.

r1 1 2 1m

l1 2 3 3nH

adiode 3=cathode 4=anode width=5.e7 infile=SiCMPSD_struc.str

r2 4 0 1mg

i1 0 4 300.

.nodeset v(1)=1000. v(2)=1000. v(3)=1000. v(4)=1000.5

.numeric vchange=0.1

.save outfile=trr_save

.options m2ln print

.end
```

```
models device=adiode reg=1 conmob fldmob consrh auger bgn
material device=adiode reg=1 taun0=5e-6 taup0=2e-6
impact device=adiode reg=1 selb
go atlas
.begin
# Reverse recovery of power diode
v1 1 0 1000.
r1 1 2 1m
l1 2 3 3nH
adiode 3=cathode 4=anode width=5.e7 infile=SiCMPSD_struc.str
r2 4 0 1mg EXP 1mg 1e-3 0. 20ns 10 200
i1 0 4 300
.numeric lte=0.3 toltr=1.e-5 vchange=10.
.options print relpot write=10
.log outfile=trr
.load infile=trr_save
.save master=trr
.tran 0.1ns 2us
.end
models device=adiode reg=1 conmob fldmob consrh auger bgn
material device=adiode reg=1 taun0=5e-6 taup0=2e-6
impact device=adiode reg=1 selb
```

```
go atlas

tonyplot trr_tr.log

quit
```