THESIS ON INFORMATICS AND SYSTEM ENGINEERING C82

FPGA-based Embedded Virtual Instrumentation

IGOR ALEKSEJEV

TUT
PRESS

TALLINN UNIVERSITY OF TECHNOLOGY
Faculty of Information Technology
Department of Computer Engineering

Dissertation was accepted for the defence of the degree of Doctor of Philosophy in Computer and System Engineering on January 23, 2013.

Supervisors: Dr. Artur Jutman,
Dr. Sergei Devadze
Department of Computer Engineering, TUT

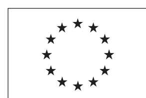
Opponents: Prof. José Manuel Martins Ferreira
University of Porto, Portugal

Dr. Heinz-Dietrich Wuttke
Ilmenau University of Technology, Germany

Defence of the thesis: February 25, 2013

Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for any academic degree.

/Igor Aleksejev/


European Union
European Social Fund

Investing in your future

Copyright: Igor Aleksejev, 2013
ISSN 1406-4731
ISBN 978-9949-23-432-5 (publication)
ISBN 978-9949-23-433-2 (PDF)

INFORMAATIKA JA SÜSTEEMITEHNIKA C82

FPGA-sisesed virtuaalsed test- ja mõõtevahendid

IGOR ALEKSEJEV

TTÜ
KIRJASTUS

Abstract

In the middle of the 20th century, with the growth of electronic systems, a traditional test and measurement instrumentation started to rapidly evolve. Stand-alone oscilloscopes, signal generators, logic analyzers and multimeters are widely known traditional instruments that are used for test purposes. Later, when computers became economically affordable, engineers started to exploit computer software capabilities for controlling instruments, collecting and analyzing data. The concept of using computer software for implementing the core functionality of the instrument is known as virtual instrumentation.

During the last decade, systems under test (SUTs) undergo significant changes. As transistors become smaller, integrated circuits may now accommodate more functionality inside one chip. What was a big system ten years ago, nowadays can easily be fitted into the one system-on-a-chip device. Contemporary printed circuit board assemblies (PCBAs) are so densely populated that there is practically no free space for test points. A vast part of interconnections is placed in internal PCB layers, thus cannot be accessed from the surface anymore. These changes shifted the instrumentation to an embedded on-chip or on-board domain. Embedded instrumentation can also be divided into traditional and virtual subclasses. In both cases instruments are incorporated to the SUT itself and have an access to devices or signals under test from the inside.

In this thesis, we concentrate on the analysis of embedded virtual instrumentation (EVI) approach. We see a great potential of EVI for testing emerging integration technologies, like 3D stacked chip or 3D stacked systems in package. In this work we focus on the implementation of embedded virtual instruments for the sake of improving test speed and test quality of printed circuit board assemblies. As a platform for instruments we utilize nowadays widely used FPGA devices.

The virtual instruments that we propose in this thesis are pre-compiled ready-to-use test instruments capable to overcome limitations of many technologies. These instruments are designed in a special way that allows on-the-fly

adaptation of the instrument to test the particular product. The main advantage of the presented EVI approach is that the compiled instrument (compiled FPGA IP core) can be immediately used for every SUT and does not need to be recompiled for a new product or after a product change.

During this work a complete EVI framework that combines both instruments and corresponding supervisory software was developed. This research was industry-driven from the beginning and was successfully integrated afterwards into commercial test system. The obtained real life experimental results and conducted industrial evaluation proved the efficiency of proposed instruments over state-of-the-art test technologies. The developed instruments are applicable in test cases where the conventional techniques do not work or are very time-consuming.

Kokkuvõte

20. sajandi keskel toimus traditsiooniliste test- ja mõõtevahendite (instrumentide) kiire areng. Eraldiseisvad ostsilloskoobid, signaaligeneraatorid, loogikaanalüsaatorid ning multimeetrid on laialt tuntud traditsioonilised instrumendid, mida kasutatakse süsteemide testimiseks. Hiljem, kui arvutid muutusid odavamaks, hakkasid insenerid kasutama tarkvaralisi vahendeid instrumentide juhtimiseks, andmete kogumiseks ning töötlemiseks. Arvuti-tarkvara kasutamist instrumendi põhifunktsionaalsuse teostamiseks nimetatakse virtuaalvahendite metoodikaks.

Selle aastakümne jooksul on testitavad süsteemid täielikult muutunud. Kuna transistori suurus on vähenenud, võimaldavad digitaalskeemid mahutada rohkem funktsionaalsust ühele kiibile. Süsteem, mis oli suur kümme aastat tagasi, võib täna olla vabalt paigaldatud ühele kiibisüsteemile. Tänapäevased trükkplaadid on nii tihedalt asustatud, et nendel praktiliselt ei ole vaba kohta testpunktide lisamiseks. Suur osa ühendustest on paigutatud sisekihtidesse, mistõttu pinnalt nendele juurdepääsu enam ei ole. Need muudatused on viinud instrumendid kiibi või plaadi sisse. Sardinstrumendid võib jagada ka traditsioonilisteks ja virtuaalseteks. Mõlemal juhul on instrumendid ehitatud süsteemi sisse ning tagavad sisemise juurdepääsu skeemidele ning signaalidele.

Antud väitekirjas keskendume sardvirtuaalvahendite (SVV) metoodika analüüsile. Näeme SVV suurt potentsiaali tekkivate integratsioonitehnoloogiate testimiseks, näiteks 3D kiibi testimiseks. Käesolevas väitekirjas aga keskendume sardvirtuaalinstrumentide rakendamisele, mis on suunatud trükkplaatide testimise kiiruse ning kvaliteedi tõstmisele. Instrumendi platvormina on kasutusele võetud tänapäeval laialt levinud FPGA programmeeritavad skeemid.

Meie poolt pakutud sardvirtuaalinstrumendid on eelnevalt kompileeritud valmis instrumendid, mis võimaldavad ületada mitmeid tehnoloogilisi piiran-guid. Need instrumendid on disainitud viisil, mis võimaldab instrumendi kohandamist konkreetse toote testimisele, kui instrument on juba ehitatud süsteemi sisse. Arendatud SVV instrumentide peamine eelis on see, et eelkompileeritud instrument sobib iga süsteemi testimiseks (seda ei ole vaja

uuesti kompileerida teise süsteemi testimiseks, ka juhul, kui süsteemis toimuvad muutused).

Käesoleva töö käigus töötati välja täielik SVV raamistik, mis ühendab nii FPGA instrumente kui ka vastava juhtiva tarkvara moodulit. Antud teadustöö oli algusest peale suunatud tööstusele ning sai pärast arendamist ka edukalt integreeritud tööstuslikku testsüsteemi. Katsetulemused ning saadud tööstuslik hinnang tõestasid pakutud instrumentide efektiivsust, võrreldes teiste nüüdisaegsete testimistehnoloogiatega. Arendatud instrumente on võimalik kasutada sellistes olukordades, kus traditsioonilised tehnoloogiad ei toimi või nende kasutamine on väga aeganõudev.

Acknowledgements

I would like to thank everyone who has helped me during my PhD studies and writing of the thesis.

First and foremost, I would like to express my deep gratitude to my supervisors Dr. Artur Jutman and Dr. Sergei Devadze for giving me an interesting topic of research and being always ready to help during my study. It was a real delight and fun to work with you, share ideas and discuss all tricky problems.

Furthermore, I would like to thank all my colleagues from Department of Computer Engineering. The working atmosphere in our institute is so cosy and pleasant that doing a research here was an easy and ordinary task.

I am thankful to my friends and colleagues from IT-231 Anton Tsertov, Anton Tsepurov, Sergei Kostin, Konstantin Shibin and Sergei Odintsov. I have learned a lot from our everyday discussions about everything in the world.

The work on this thesis was supported by many organizations which I would like to acknowledge: Tallinn University of Technology, Testonica Lab, Estonian Information Technology Foundation (EITSA), EUROSTARS FP7 project COMBOARD, National Graduate School in Information and Communication Technologies (IKTDK) and ELIKO Development Centre.

Finally, I would like to warmly thank my family for their infinite support and willingness to help. Special thanks to my wife, Viktoria, for her love and patience.

Igor Aleksejev

Tallinn, January 2013

List of Publications

Board-level test issues

Aleksejev, I; Jutman, A.; Devadze, S.; Odintsov S.; Wenzel, T., "FPGA-Based Synthetic Instrumentation for Board Test", *43th IEEE International Test Conference (ITC'12),* Austin, USA, 2012.

Jutman, A.; Devadze, S.; Aleksejev, I; Wenzel, T., "Embedded synthetic instruments for Board-Level testing", *17th IEEE European Test Symposium (ETS'12),* Annecy, France, 2012.

Devadze, S.; Jutman, A.; Aleksejev, I.; Ubar, R., "Fast Extended Test Access via JTAG and FPGAs", *40th International Test Conference (ITC'09)*, Austin, USA, 2009.

Devadze, S.; Jutman, A.; Aleksejev, I.; Ubar, R., "Turning JTAG inside out for fast extended test access", *10th IEEE Latin American Test Workshop (LATW'09)*, Buzios, Brazil, 2009.

LFSR reseeding based optimization methods

Jutman, A.; Aleksejev, I.; Raik, J., "Design and Test Technology for Dependable Systems-on-Chip", chapter "Sequential Test Set Compaction in LFSR Reseeding", pp. 476 – 493, Hershey - New York: Information Science Reference IGI Global, 2011

Aleksejev, I.; Jutman, A.; Raik, J.; Ubar, R., "Application of Sequential Test Set Compaction to LFSR Reseeding", *26th Norchip Conference*, Tallinn, Estonia, 2008, pp. 291 - 294.

Jutman, A.; Aleksejev, I.; Raik, J.; Ubar, R., "Reseeding Using Compaction of Pre-Generated LFSR Sub-Sequences", *15th IEEE International Conference on Electronics, Circuits and Systems (ICECS'08)*, St. Juliens, Malta, 2008, pp. 1290 - 1295.

Raik, J.; Ubar, R.; Jutman, A.; Aleksejev, I., “A Scalable Static Test Set Compaction Method for Sequential Circuits”, *9th IEEE Latin American Test Workshop (LATW’08)*, Puebla, Mexico, 2008, pp. 87 – 91.

Ubar R., Jervan G., Kruus H., Orasson E., Aleksejev I., "Optimization of the Store-and-Generate Based Built-In Self-Test", *10th Biennial Baltic Electronics Conference (BEC’06)*, Laulasmaa, Estonia, 2006, pp.199 - 202.

Laboratory environment for education and research of design and test

Ubar, R.; Jutman, A.; Raik, J.; Devadze, S.; Aleksejev, I.; Chepurov, A.; Chertov, A.; Kostin, S.; Orasson, E.; Wuttke, H.-D., “E-Learning Environment for WEB-Based Study of Testing”, 8*th European Workshop on Microelectronics Education* (*EWME’10*), Darmstadt, Germany, 2010, pp. 47 – 52

Jutman, A.; Tsertov, A.; Tsepurov, A.; Aleksejev, I.; Ubar, R.; Wuttke, H.-D., “Teaching Digital Test with BIST Analyzer”, *19th EAEEIE Annual Conference*, Tallinn, Estonia, 2008, pp. 123 - 128

Jutman, A.; Tsertov, A.; Tsepurov, A.; Aleksejev, I.; Ubar, R.; Wuttke, H-D., “BIST Analyzer: a Training Platform for SoC Testing“, *37th Annual Frontiers in Education Conference (FIE’07)*, Milwaukee, USA, 2007, pp. 1534 – 1539