THESIS ON POWER ENGINEERING,
ELECTRICAL ENGINEERING, MINING ENGINEERING D53

Research of Switching Properties and Performance Improvement Methods of High-Voltage IGBT based DC/DC Convertes

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for any academic degree.

Andrei Blinov............................

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ENERGEETIKA. ELEKTROTEHNIKA. MÄENDUS D53

Kõrgepingelistel IGBT transistoridel põhinevate alalispingemuundurite lülitusomaduste ja jõudluse suurendamise meetodite uurimine

ANDREI BLINOV

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Abbreviations

2L	two-level
3L-NPC	three-level neutral point clamped
AC	alternating current
ACS	active-clamp snubber
AFBR	active full-bridge rectifier
BJT	bipolar junction transistor
CDR	current doubler rectifier
CTE	coefficient of thermal expansion
CS	carrier storage
DBC	direct bonded copper
DC	direct current
EMI	electromagnetic interference
ETO	emitter turn-off thyristor
FBSOA	forward-bias safe operation area
FWD	freewheeling diode
GTO	gate turn-off thyristor
HB	half-bridge
HV	high-voltage
HS	hybrid switch
IGBT	insulated gate bipolar transistor
IGCT	integrated gate-commutated thyristor
JFET	junction gate field-effect transistor
MOSFET	metal–oxide–semiconductor field-effect transistor
NPT	non punch through
PT	punch through
PWM	pulse-width modulation
RB	reverse-blocking
RBSOA	reverse-bias safe operation area
RC-IGBT	reverse-conducting insulated gate bipolar transistor
RMS	root mean square
SCSOA	short-circuit safe operation area
SOA	safe operating area
SPT	soft punch through
TIM	thermal interface material
PCM	phase change material
VSC	voltage-source converter
VSI	voltage-source inverter
ZVS	zero voltage switching
ZCS	zero current switching

Symbols

A_{on}, B_{on}	turn-on loss coefficients
A_{off}, B_{off}	turn-off loss coefficients
A_m	area of the thermal interface material layer
C_E	summarised output capacitance of IGBT
C_f	output filter capacitance
C_r, C_p	resonant capacitances
C_T, C_B	output capacitance of IGBT
$C_{Tr\text{-}p}$	equivalent capacitance
C_s	snubber capacitance
$C_{s(RC)}$	capacitance of the *RC* snubber
D	switch duty cycle
D_{max}	maximum switch duty cycle
D_{min}	minimum switch duty cycle
D_{nom}	nominal switch duty cycle
D_{rect}	duty cycle of the rectifier switches
D_s	freewheeling state duty cycle
E_{cond}	conduction energy losses
E_{off}	turn-off energy losses
E_{on}	turn-on energy losses
E_{osc}	energy of oscillations
E_{rec}	reverse-recovery energy
E_{rec}^{DS}	reverse-recovery energy specified in the datasheet
E_{sw}	switching energy losses
E_{tot}	total energy losses
f_{osc}	oscillation frequency
f_{out}	output frequency
f_{sw}	switching frequency
$f_{sw(max)}$	maximum switching frequency
$I_{F(peak)}$	maximum forward current
i_F	instantaneous forward current
I_C	collector current
I_C^{rms}	RMS collector current
$I_{C(max)}$	maximum collector current
$I_{F(avg)}$	average forward current
I_{HS}	hybrid switch current
$I_{L_{f(min)}}$	minimum filter inductor current
$I_{L_{f(max)}}$	maximum filter inductor current
i_{osc}	instantaneous oscillating current
I_{osc}	peak value of the oscillating current
I_{out}	average output current

I_{rec}	peak reverse-recovery current
I_{SA}	IGCT current
I_{SB}	IGBT current
$i(t)$	instantaneous current
k_{on}^{rec}	scale factor for the turn-on losses
k_{rec}	scale factor for the reverse-recovery energy
$k_{R_{G-on}}$	turn-on resistor scale factor
$k_{R_{G-off}}$	turn-off resistor scale factor
k_L	relative filter inductor current ripple
$k_{(sat)}$	scale factor of the on-state voltage
k_{th}	thermal conductivity of the TIM
k_U	relative output voltage ripple
$k_{(U_{CE-on})}$	scale factor for the actual turn-on commutation voltage
$k_{(U_{CE-off})}$	scale factor for the actual turn-off commutation voltage
L_E	equivalent inductance
L_f	output filter inductance
L_r, L_p	resonant inductance
N_p	number of trurns of the transformer primary
N_s	number of trurns of the transformer secondary
P_{out}	output power
P_{cond}	conduction power losses
P_{off}	turn-off power losses
P_{on}	turn-on power losses
$P_{s(RC)}$	power dissipation of the *RC* snubber
P_{tot}	total power losses
Q	oscillatory circuit quality factor
Q_{rec}^{DS}	reverse-recovery charge specified in the datasheet
R_E	equivalent resistance
R_{G-on}	turn-on gate resistance
R_{G-off}	turn-off gate resistance
R_{G-on}^{US}	user-specific turn-on gate resistance
R_{G-on}^{DS}	datasheet turn-on gate resistance
R_{G-off}^{US}	user-specific turn-off gate resistance
R_{G-off}^{DS}	datasheet turn-off gate resistance
R_E	equivalent active resistance
R_{HF}	equivalent high-frequency resistance
R_L	equivalent load resistance
$R_{s(RC)}$	resistance of the *RC* snubber
r_T	slope resistance

R_{thcs}	thermal resistance case-to-heatsink
R_{thsa}	thermal resistance heatsink-to-ambient
t_a	active state time
T_{amb}	ambient temperature
t_d	dead time
$t_{d(off)}$	turn-off delay time
t_f	collector current fall time
T_j	junction temperature
$T_{j(max)}$	maximum junction temperature
t_{off}	off-state time
t_{on}	on-state time
t_{rec}	reverse-recovery time
T_{sw}	duration of the switching period
t_{tr} t_{tr1} t_{tr2} t_{tr3}	energy transfer period
u_{osc}	instantaneous oscillating voltage
U_{out}	output voltage
U_{CE-on}^{US}	user-specific collector-emitter voltage prior to turn-on
U_{CE}^{DS}	datasheet collector-emitter voltage prior to switching transient
$U_{CE(sat)}$	collector-emitter saturation voltage
$U_{F(max)}$	maximum forward voltage
U_{GE}	gate-emitter voltage
U_{in}	input voltage
$U_{in(max)}$	maximum input voltage
$U_{in(min)}$	minimum input voltage
$U_{in(nom)}$	nominal input voltage
$U_{out(max)}$	maximum output voltage
$U_{out(min)}$	minimum output voltage
U_{Prms}	transformer primary RMS voltage
U_{rec}^{DS}	reverse-recovery voltage specified in the datasheet
U_{rect}	output voltage of the active rectifier
U_{Tr-s}	amplitude voltage across transformer secondary
$u(t)$	instantaneous voltage
U_T	on-state voltage drop of the IGCT
U_{T0}	threshold voltage
Z_{Tr-p}	magnitude of the circuit impedance
δ	attenuation coefficient
γ_{min}	snubber capacitor recharge time
ω_0	undamped resonance frequency
ΔI_{ripple}	peak-to peak inductor current ripple
ΔU_{ripple}	peak-to-peak output voltage ripple

1 INTRODUCTION

1.1 Definition of power electronic converters

Today, it is crucial to increase the energy efficiency because of higher awareness of excessive carbon dioxide emissions, safety of energy and possible increase in energy prices. It is expected that the trend toward more efficient and advanced systems that transform electrical energy, i.e. convert electrical energy from one form to another, will continue and accelerate in the future. Power electronics is concerned with processing of electrical power by electronic devices with a switching converter as a major element [1]. As an engineering branch, power electronics appeared about 50 years ago, with the introduction of the thyristor (previously called silicon-controlled rectifier). The basic idea of all switching power converters is to divide the input flow of energy into small packets, process these packets and deliver the energy in another, modified flow to the output [2]. Generally, the converter features a power input (source), control input ports and a power output port (load). In a DC/DC converter, the DC input voltage is converted to DC output voltage having a larger or smaller magnitude, possibly with galvanic isolation of the input and output sides. In an AC/DC converter, an AC input voltage is rectified, producing a DC output voltage. The DC output voltage as well as AC input current may have adjustable value. The DC/AC conversion involves transforming (inverting) a DC input voltage into an AC output voltage and AC/AC conversion involves converting an AC input voltage to an AC output voltage. In both cases the AC output voltage could have an adjustable magnitude and/or frequency (Figure 1.1) [1].

In the majority of applications the DC or AC output voltage should be regulated, despite variations in the input voltage and load current. In some systems the converter should manage reversible energy flows depending on the operating conditions as well. In this case the real-time regulation is desired. To achieve this regulation a controller block typically featuring linear integrated circuits and digital signal processors together with additional sensing loops is used as an integral part of the power converter (Figure 1.2).

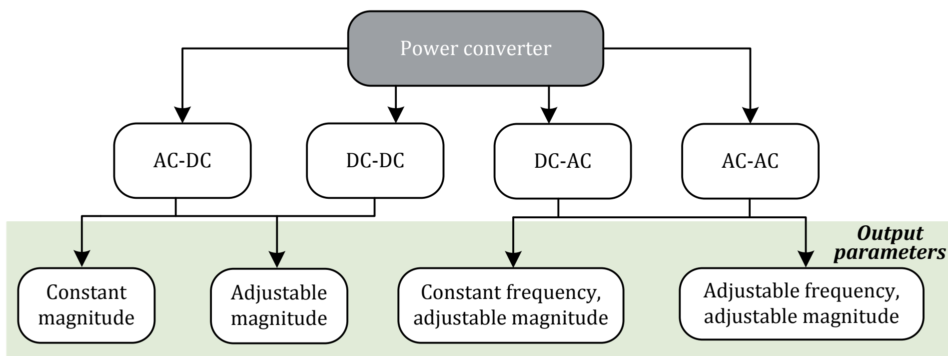


Figure 1.1 Classification of power converters

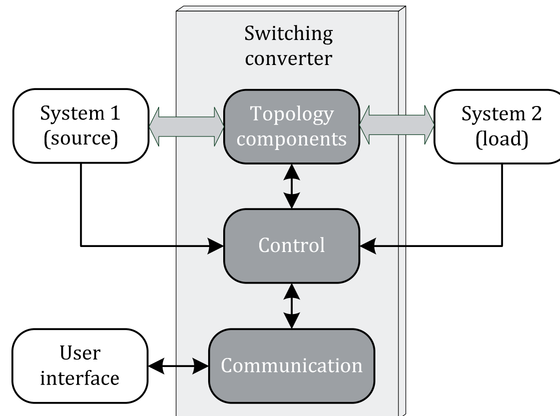


Figure 1.2 The power converter system

The improved power capabilities, simplification of control and reduced costs of state-of-the-art power semiconductors compared to those two decades ago have made power electronic converters feasible and advantageous in a considerably wider field of applications and inspired development of new converter topologies [3]. General application fields of power electronic converters are:

- residential (refrigerators, air conditioning, cooking, lighting, personal computers, chargers, etc.),
- commercial (elevators, uninterruptible power supplies, office equipment, lighting systems, etc.),
- telecommunications (battery chargers, power supplies)
- transportation (traction control and battery chargers for electric vehicles, trolleybusses, subways, locomotives, etc.),
- industrial (pumps, compressors, fans, blowers, robotics, induction heating, etc.)
- utility systems (high-voltage DC transmission, renewable and alternative energy sources, energy storage systems, etc.),
- aerospace (satellite and aircraft power systems) and marine applications.

As described in application notes and standards (for instance, IEEE 519-1992 and IEC 61000-3-6), the energy flow at the input and at the output of the switching converter should be continuous and substantially free from harmonics and electromagnetic interferences (EMI). Filter components are necessary in this case, although in some applications these components can be part of the source or the load. According to the basic circuit theory and component design, higher operating frequencies will result in smaller passive topology components and filter elements. Therefore, all converter designs aim for increased operating frequencies to minimise the total price of the converter [4][5]. However, higher switching frequencies lead to the reduction of the converter efficiency. This is undesired not only because of the increase in energy consumption, but especially for thermal issues and the associated cost of cooling. The part of the

power processed by a converter is converted into heat which must be removed. In the case of a high-power converter this leads to large and expensive cooling systems and/or increases of the operating temperature of the electronic components, affecting the reliability [6][7][8]. Besides high efficiency, the other typical desired parameters of a power converter are: high reliability, high power density, low maintenance or service requirements, and low price. To achieve these goals a proper choice of electronic components is essential. The available circuit elements fall broadly into the following classes:

- resistive elements,
- capacitive elements,
- magnetic devices (inductors, transformers),
- semiconductor elements,
- control units (analogue and digital electronics, signal processors, and sensors).

In switching converters, capacitive and magnetic devices are very important elements, since ideally they do not consume power. On the contrary, resistive elements should be avoided whenever possible [1]. In a semiconductor device, a small portion of transferred power is converted into heat. Hence, generally in any power converter the number of semiconductor elements should be optimised to avoid excessive losses, simplify control and improve reliability.

Owing to rapid development of high-voltage switched-mode semiconductors, such as insulated gate bipolar transistors (IGBTs), characteristics of most of the presently used converters could be substantially improved due to the reduced number of series and/or parallel connected switches, simplification of the topology, lower power dissipation, and easier control.

1.2 Need for HV IGBT based converters

The topologies used for high-power conversion applications are mainly determined by the available voltage ratings of the power semiconductor devices. The IGBTs today are widely represented for blocking voltages ranging between 0.6 kV and 6.5 kV, making them suitable for a large range of power electronic systems.

Most AC-to-AC conversion systems (excluding matrix converters and cycloconverters) include a series connection of a rectifier and an inverter. To temporarily store the energy between the conversion stages, most converters generally feature at least one DC-link. Depending on the type of the DC-link, the converters can be divided into current source and voltage source converters (VSCs). Current source converters have an inductor to store the energy magnetically and operate with constant current in the DC-link, while the VSC uses a capacitor to keep the constant voltage at the DC-link. Current source converters require semiconductors with reverse blocking (RB) capability (symmetrical voltage blocking devices). Although such semiconductors are available, the RB is often realised by a series connection of a controlled switch

Table 1.1 Typical line voltages and preferred semiconductor voltage ratings

Nominal line voltage		Preferred semiconductor blocking voltage rating (kV)
AC (kV_{RMS})	DC (kV_{DC})	
0.4	0.6	1.2
0.69	0.75	1.7
	1.3	2.5
	1.5	3.3
1.7		4.5
2.3	3.0	6.5

and a diode. The VSCs require reverse conducting (asymmetrical) semiconductors to provide a freewheeling path during transients. This is generally realised by the integration of a freewheeling diode (FWD) connected in parallel to the controlled asymmetrical device.

In real applications due to the lower losses in the DC-link capacitor than in the DC-link inductor, the power density of a VSC can be substantially higher than in a current source converter, especially at light loads due to lower current in the DC-link [9]. Furthermore, due to the inductive behaviour of most loads and sources, the VSC may not require application of additional impedances or filters, while capacitors are generally required at the output terminals of a current source converter. According to these considerations, the growing importance of voltage source converters in comparison to current source converters becomes obvious. The semiconductor device manufacturers have responded to this growing market, introducing optimised and efficient asymmetrical semiconductors. These devices often have two-level (2L) phase legs integrated into single housing (also referred to as “power electronic building blocks”), allowing more compact, cheap and reliable converters [2].

High-power converters have been traditionally designed with thyristor based devices, such as a gate-turn-off thyristor (GTO), an emitter-turn-off thyristor (ETO), an integrated-gate-commutated thyristor (IGCT), etc [10]. The thyristor based devices are generally slow in the switching speed and have a lack of *di/dt* (and sometimes *du/dt*) handling capability. A snubber inductor is required to limit the turn-on speed and energy stored in it has to be dissipated by resistors. The thyristor devices also lack the feature of fast de-saturation protection during fault condition [11]. On the other hand, IGBTs offer such advantages as snubberless operation, simpler voltage control, faster switching speed, a wide safe operation area (SOA), and short-circuit current limitation [12]. Thus, the high-voltage (HV) IGBT has been considered as the substitute to the thyristor based devices for high-power applications. Depending on line voltage, different voltage class IGBTs should be implemented (Table 1.1)

1.3 Thesis motivation

High-voltage semiconductors allow implementation of well-known and simple topologies with a small number of components in applications where multilevel converters or converters with a number of semiconductors connected

in series were previously required. Focus of the present PhD research is on VSCs with HV IGBTs (3.3…6.5 kV), which are designed to be implemented in traction and industrial applications. Despite providing many advantages, the major drawback of HV IGBT based converters is limited (typically up to few kHz) switching frequency. Relatively low operating frequencies require implementation of bulky and costly magnetic and capacitive components. The switching frequency is generally limited not by minimum IGBT on-state or off-state time requirements, but due to thermal management issues. Traditional simple and robust hard-switched topologies require modifications in order to reduce losses in semiconductor elements and increase the switching frequency.

Generally, to reduce the switching losses in a semiconductor device, additional elements are necessary, which leads to an increased number of topology components. As the number of components is increasing, the system becomes more complex. As a result, the robustness together with reliability are estimated to decrease accordingly. Another challenge related to systems with HV semiconductors is high price of the HV side components. Therefore, investigation of different possibilities to reduce semiconductor losses, which require only minor modifications to the HV side of the power converter, are of major importance.

This thesis is a part of the research project dealing with the elaboration of new methods and solutions for the mass production of power electronic converters based on the new generation of HV IGBT modules. The project was launched in 2006 by Tallinn University of Technology, Department of Electrical Drives and Power Electronics, in cooperation with Estonian company Estel Electro Ltd. The research activities were also supported by targeted financing research project SF0140016s11, two grants G7425 and G8020 and in 2008 the project received financial support from Tallinn University of Technology (BF110).

The main importance of this research lies in the development of new state-of-the-art converter topologies and control methods that will help to improve the energy efficiency of such demanding applications as transportation (e.g. rolling stock) or energy sectors. With the recent growing demand to improve the efficiency and flexibility of the interface converters, the results of this PhD research may become especially topical, since they could lead to lower unit cost of power converters and to lower energy consumption. This project matches the main priorities set by Estonian Energy Technology Programme for 2007-2013, which are to develop new energy efficient technologies and support objectives, measures and activities of the Development Plan of the Electricity Sector. The results obtained during the PhD research can be implemented in different applications and support Estonian industrial companies to increase their competitiveness and export potential.

1.4 Main hypotheses and objectives

The main goal of the PhD research is to develop and experimentally validate new methods, topologies, control algorithms, and design guidelines, which will substantially contribute to the further improvement of the HV IGBT based DC/DC converters and will help to extend their application possibilities.

The main hypotheses of the PhD research:

1) Due to the specific features of the physical design of HV IGBT based converters, the influence of parasitic processes has more impact on the performance than in the case of IGBT-based converters used in lower voltage applications. By help of detailed mathematical and simulation models as well as by minor modifications in the HV side, the efficiency and power density of HV IGBT based converters could be substantially increased.

2) By combining positive properties of different commercially available HV semiconductor switches, more energy-efficient solutions could be obtained.

The main objectives of the PhD research:

- to analyse and classify the current state-of-the-art technologies and development trends of HV IGBTs,
- to define implementation challenges of HV IGBTs in two-level hard-switched DC/DC converters,
- to propose and validate improvement methods of HV IGBT based two-level hard-switched DC/DC converters,
- to define directions for future research and development.

In order to achieve the above presented objectives and to verify the hypotheses set forth here comprehensive research and development tasks should be solved. The research methods applied are based on the mathematical analysis, computer simulations and prototyping. To estimate performance, power losses and operating frequency of proposed solutions are compared. Computer simulations are generally performed in PSIM9, MATHCAD14, PSpice9.2 and MATLAB/Simulink simulation packages.

1.5 Results and dissemination

This section presents the most important findings obtained in the current PhD research. These results comprise both the scientific and practical novelties.

Scientific novelties:

- systematisation and analysis of the current state-of-the-art technologies and development trends of high-voltage IGBTs,
- analysis of thermal limitations and switching frequency limits of HV IGBT modules operating under hard switching conditions,

- synthesis of an improved mathematical method of semiconductor power loss estimation based on IGBT datasheet characteristics,
- comparative analysis of different performance improvement methods of two-level hard-switched half-bridge DC/DC converters in HV applications,
- synthesis of a new method of loss reduction in HV semiconductors by combining the advantages of commercially available HV IGBTs and IGCTs.

Practical novelties:

- detailed mathematical models of switching transients of HV IGBTs in galvanically isolated DC/DC converters,
- new method of power loss reduction in high-voltage IGBT based half-bridge DC/DC converters by means of a phase shifted active rectifier,
- power density improvement method of two-level hard-switched DC/DC converters by the implementation of the 3L-NPC based on HV IGBTs with lower blocking voltage,
- design guidelines for switching frequency selection and associated cooling system dimensioning.

Practical results are oriented to the Estonian and international industrial companies. For example, Estel Elektro AS (Estonia) is highly interested in the production of innovative energy efficient DC/DC converters for rolling stock and aircraft applications. By the introduction of new flexible DC/DC converter solutions proposed in the PhD research, the production list, competitiveness and export turnover of the Estonian company Estel Elektro could definitely be improved. Most of these results could be implemented not only in state-of-the-art HV traction converters, but also in other power electronic applications, e.g. in industrial, renewable energy or aerospace systems. During the PhD research a couple of prototypes were built to verify the theoretical estimations.

Dissemination of results and publications

The results obtained during the PhD research were reported at 15 international conferences and workshops and published in 10 papers. Seven of them have appeared in international peer-reviewed journals and three are available through IEEExplore database. The most important papers directly connected to the topic of the dissertation are listed in the Appendix. In addition, one patent application "Energy-efficient high-voltage hybrid switch" (P201100020) was submitted to Estonian patent office in 2011. Presented novelties, e.g. efficiency of optimisation methods and control algorithms, may substantially contribute to faster advancement of modern energy efficient power electronics and reliable and sustainable power engineering as well as be used in the study process in Tallinn University of Technology.

Additionally, in terms of international collaboration, the PhD research helps to promote international cooperation between Tallinn University of Technology

and other European universities and institutions. This would help to popularise Estonian science (and science of power electronics, in particular) and to strengthen the positions of Estonian scientific and industrial communities worldwide. In compliance with its objectives and activities, the project will support the Estonian Research and Development and Innovation Strategy 2007-2013 “Knowledge-based Estonia”.

2 STATE-OF-THE-ART AND TECHNOLOGY TRENDS OF HV IGBT MODULES

2.1 Current state-of-the-art

To ensure reliable operation, the semiconductors should fulfil the following requirements: high junction temperature limit, large safe operating area, high surge current capability, and sufficient thermal cycling capability. During the design process of power semiconductors there is a trade-off between conducting characteristics (the on-state resistance and/or the forward voltage drop) and the switching characteristics. Advances in the device technology are estimated in terms of ameliorations in this trade-off relationship [13].

The IGBT was invented in 1980s as a minority-carrier device with high input impedance and large bipolar current-carrying capability [2][14]. At first approximation it can be considered as a p-n-p bipolar junction transistor (BJT) and an n-channel metal-oxide-semiconductor field-effect transistor (MOSFET) in a Darlington configuration, the two devices sharing two of the four semiconductor regions and the base current of BJT is controlled by a MOSFET (Figure 2.1a). The IGBT combines all the advantages of the BJT and MOSFET and has three terminals called Collector (C), Gate (G) and Emitter (E). As can be seen from the structures of these transistors (Figure 2.2), the only difference with MOSFET lies in the additional p-region at the collector side of the IGBT. As a result, a carrier overflow is created by holes, which are injected into the highly resistive n^- drift region. Obtained increase in the conductivity allows reductions in the on-state voltage drop of the IGBT. Compared to the pure resistive on-state behaviour of the MOSFET, the IGBT has an additional threshold voltage due to the collector p-n^- junction layer, but the on-state voltage of higher voltage IGBTs (above 0.6 kV) is generally lower than that of MOSFETs because of the injection of minority carriers in the highly resistive n^- region. Furthermore, IGBTs may be designed for significantly higher currents and voltages for similar chip areas [15].

Based on the structure shown in Figure 2.2b, a more precise equivalent circuit model of an IGBT can be drawn, as shown in Figure 2.1b. It contains MOSFET, JFET, NPN and PNP transistors. The collector of the PNP is

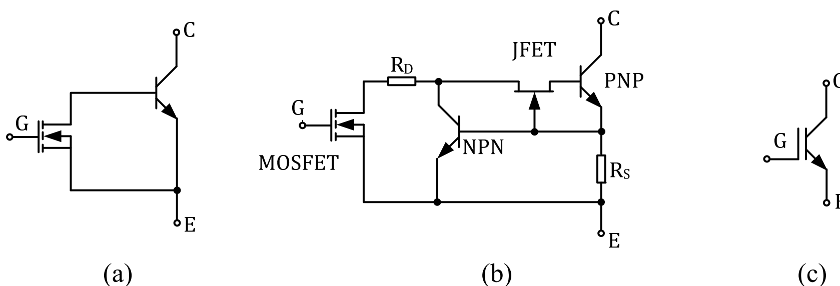


Figure 2.1 Simplified equivalent circuit (a), detailed equivalent circuit (b) and symbol (c) of IGBT

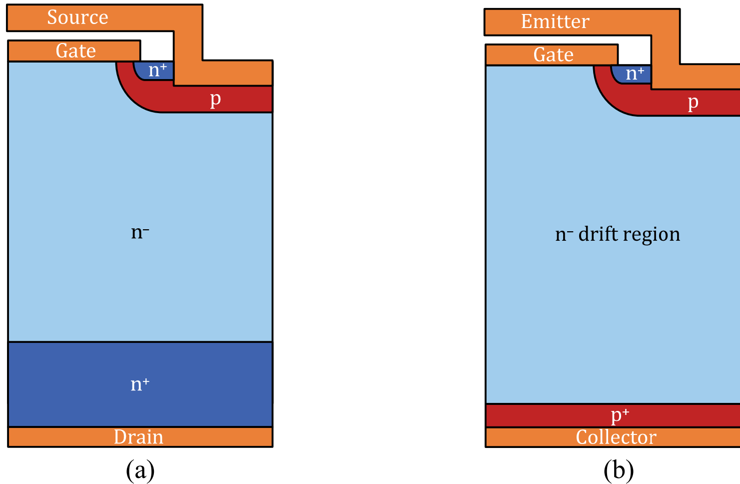


Figure 2.2 Generalised MOSFET (a) and IGBT (b) structures

connected to the base of the NPN and the collector of the NPN is connected to the base of the PNP through the JFET. The NPN and PNP transistors represent the parasitic thyristor structure. The resistor R_D represents the drift region resistance and the resistor R_B represents the base-emitter shorting of the NPN transistor, to prevent the latch-up of the parasitic thyristor. Otherwise that will lead to the IGBT breakdown. The JFET represents the contraction of current between two neighbouring IGBT cells. It supports most of the voltage, therefore the low-voltage MOSFET with low on-state resistance can be applied [14]. A circuit symbol for the IGBT is shown in Figure 2.1c.

The added p-n$^-$ junction of the IGBT is not normally designed to block significant voltage. Therefore, the IGBTs typically have negligible reverse voltage blocking capability [1]. The desired reverse characteristics are generally realised by connection of an integrated diode in series (for current-source converters) or in anti-parallel (for voltage-source converters) to the IGBT.

In contrast to the MOSFET, the IGBT has a tail current during turn-off. PNP collector current continues to flow due to the remaining charge carriers that have to be recombined in the n$^-$ region after the collector-emitter voltage has increased [16]. This effect increases the turn-off transient time and the losses in the device. In comparison to the MOSFET, the turn-on time of the IGBT is increased as well, mainly due to limited reverse-recovery characteristics of integrated higher-voltage FWDs.

IGBT gate drive requirements are imported from the MOSFET and are much less demanding than those of the GTO: the gate appears to its driver as a capacitor, which is charged to approximately +15 V to turn-on the transistor and discharged to turn it off. Another feature inherited from the MOSFET is an ability of the gate voltage to control the device current. This could be utilised in some situations, for example, for running a number of devices in series. Limiting of *du/dt* and *di/dt* can be achieved (if required) by the gate drive.

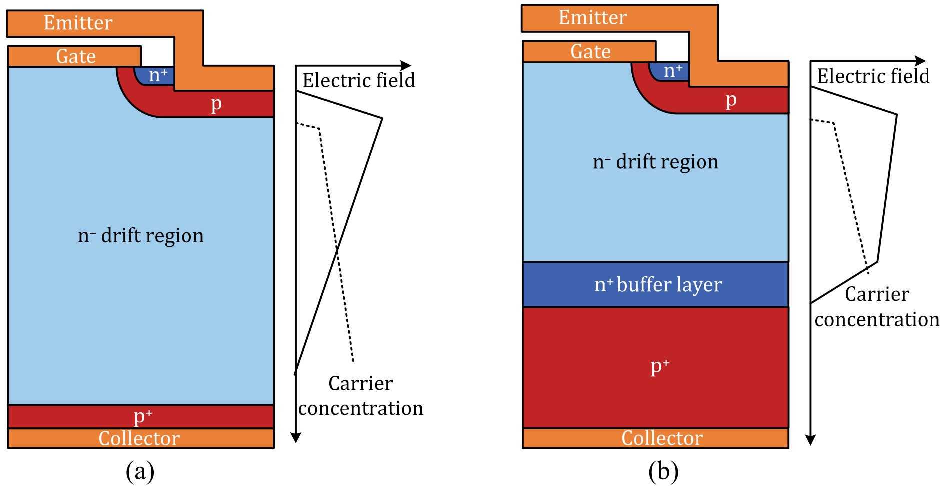


Figure 2.3 Generalised NPT (a) and PT (b) IGBT structures (cross-section of one cell)

Hence, the external snubbers are unnecessary, improving reliability and reducing both physical size and cost of a system. The switching delay for the IGBT is much shorter than for the GTO, with a switching transient generally taking a few hundred nanoseconds to complete, in comparison to around 10 ms in the case of the GTO. This allows using higher switching frequencies, even with the possibility of moving this frequency out of the audible range. Improved short circuit behaviour is another added feature: the IGBT limits its own current to around ten times the normal operating current and can turn off safely from such a condition, assuming that this condition is sufficiently quickly detected (5…10 µs) [17].

High power IGBT switches are made from a number of smaller chips (typically rated at 75 to 100 A) operating in parallel. The structural design of the IGBT (as well as the power MOSFET) consists of a silicon-micro-cellular structure of about $100{\cdot}10^3$ basic cells per cm^2 (HV-IGBTs) distributed over a chip surface that can vary between 0.3 and 1.5 cm^2 [18]. Since the current density is limited, the current capability can be increased by integration of several dies in an isolated module. Parallel connection of chips is performed by ultrasonic soldering of aluminium wire bonds to the chip's metallisation. Dies are soldered on a direct bonded copper (DBC) substrate consisting of a ceramic layer (AL_2O_3 or AIN) and two copper layers which are soldered on a copper or AlSiC baseplate (for better thermal cycling capability). Additionally, the IGBT modules generally include freewheeling diode chips and other elements, providing additional integrated functions, such as temperature sensing, gate driving, protection, etc [15].

Traditionally, two different IGBT structures exist: the PT-structure (punch through) and the NPT-structure (non-punch-through). The physical constructions for both NPT and PT technologies are presented in Figure 2.3a and 2.3b, respectively.

NPT transistors have triangular electric field in the blocking state. The drift region is poorly doped and rather thick in order to sustain an electric field during off-state, meaning that the drift region has a rather high internal resistance. The thickness is therefore the main contributor of the collector-emitter saturation voltage $U_{CE(sat)}$, which directly relates to conduction losses. The NPT IGBTs feature small part parameter variation, positive temperature coefficient, low-amplitude temperature-independent tail current and good short-circuit capability.

On the contrary, the PT design has a much thinner n^{-} region, designed so that the electric field extends right through it ("punches through") when blocking high voltages. An additional highly-doped thin n^{+} layer on the collector side prevents the electric field from reaching the collector p^{+}-doping, leading to a trapezoidal shape of this field. The thinner n^{-} base results in a much lower $U_{CE(sat)}$ and, therefore, decreased conduction losses. Unfortunately, the other characteristics of the PT IGBTs are less desirable: negative temperature coefficient and higher tail current, strongly increasing with temperature [17][19].

Parallel connection

The increased power demand of modern converters for industrial applications results in higher currents and voltages. Currents up to tens of kA and voltages up to tens of kV, exceeding the ratings of currently available IGBTs are required [20]. These ratings can be achieved by implementing cascaded connection of converters, multilevel converters or by series/parallel connection of semiconductor switches. Series and/or parallel connection of semiconductors in individual cascaded or in multilevel converters is possible as well. Devices are paralleled to increase current capability or connected in series to increase voltage ratings [21].

By paralleling power IGBT modules, the integrated freewheeling diodes are also paralleled. Maximum utilisation of the switch generated by parallel connection will only be achieved in the case of ideal current sharing of the single modules during the conduction and switching periods. The current sharing is achieved either by matching electrical and thermal characteristics of an appropriate device or by using external forced sharing techniques.

Initially, the major current share of paralleled modules is conducted by the IGBT with the lower $U_{CE(sat)}$, which will therefore have higher forward and switching losses. As a result, the junction temperature will increase rapidly. If the temperature coefficient of the IGBT is positive ($U_{CE(sat)}$ rises together with the temperature), the current will be transferred to the transistor that carried the smaller current share. Finally, the current will evenly distribute (in ideal case) over the paralleled transistors. Therefore, power semiconductors with a positive temperature coefficient are preferable for parallel connections. Since it is positive for most HV IGBTs over almost the whole rated current range, the paralleling of the modules is simplified.

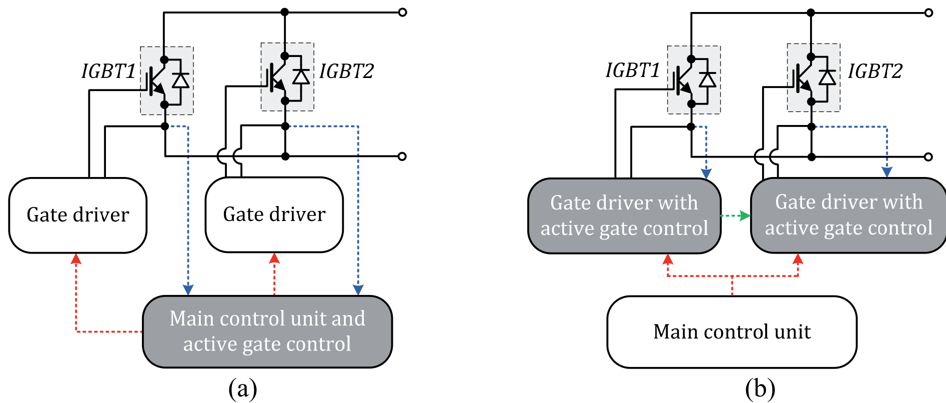


Figure 2.4 Paralleled IGBTs driven by centralised gate control unit (a) and individual gate control units containing decentralised active gate control (b)

In real systems several factors may cause dynamic and static unbalance of currents of the parallel connected IGBT modules leading to necessity of deration of the IGBT modules, which results in an increased number of devices being required. The possible reasons of unbalances could be in the asymmetrical connection of the switches to the busbar and heatsink, parameter variations of the semiconductors, as well as deviations in the transfer characteristics, threshold voltages and switching delay times. Additional circuit components, such as series resistors or inductances in the current paths, could improve current sharing [22]. These methods, however, result in additional losses and reduced switching speed. Alternatively, the currents can also be balanced by controlling the switching and on-state behaviour with the gate drivers. A common gate driver for all parallel connected IGBT modules can be used for reduced costs. Balancing cores, common mode chokes, or individual gate resistors must be used in this case in order to reduce the influence of the different emitter voltages caused by the inductive coupling. An individual gate driver can be used for each IGBT module to avoid these effects. In this case the differences in the gate driver's supply voltages and in the gate resistors have to be minimised.

The active gate control method can compensate the delays in gate timings as well as tolerances in component parameters. Usually a centralised active gate control is applied (Figure 2.4). Current of the each IGBT is measured by a central unit to detect the rising and falling edges. According to the measured delay times between the different IGBT modules, the centralised control unit adjusts the turn-on and turn-off instants independently for each gate driver to ensure simultaneous switching and a dynamically-balanced current sharing, which generally leads to a statically-balanced current sharing for IGBTs with positive temperature coefficient as well. Usually the centralised gate control circuit is designed for a certain system configuration with a given number of IGBT modules connected in parallel, which complicates modifications.

An alternative modular concept of a decentralised active gate control consisting of independent and equal gate drives for current balancing of parallel connected IGBT modules is presented in [20]. In this case there are no restrictions on the number of IGBT modules connected in parallel. Each gate drive measures and controls the current of its IGBT module individually. In consequence, the control for the current balancing is distributed to all gate control units and no centralised control circuit is required. On the other hand, communication between the gate control units is required.

Series connection

As mentioned previously, HV switches can be realised by connecting lower voltage devices in series. For HV applications, two-level topologies with series connected devices are attractive due to lower cost and lower complexity in circuit design and control compared to multilevel topologies [21]. As estimated in [23], the switch consisting of six series-connected 1.2 kV IGBTs to form an equivalent 6.5 kV switch could operate with 2.4 times increased switching frequency, while having the same power dissipation as a single 6.5 kV transistor. However, equal static and dynamic voltage sharing across series connected devices should be ensured. Uneven voltage may lead to exceeding of the individual device voltage and causing its failure. The failed device can result in a breakdown of the entire string of series connected devices.

The main factors causing voltage unbalance are device parameter variations and gate drive delays. Static voltage balancing can be achieved relatively easily by the connection of high resistance resistors in parallel with each IGBT. Dynamic voltage sharing is more difficult to achieve. The methods for dynamic voltage balancing can be divided into two groups: one concentrates on the power side (passive snubbers, voltage clamping circuits) and the other one on the gate control techniques [23].

The use of a passive snubber is the most popular technique in series operation of power devices. The resistors in parallel with series devices are used for static sharing and resistor-capacitor (RC) or resistor-capacitor-diode (RCD) circuit is used in parallel for dynamic sharing (Figure 2.5a). The use of passive snubbers is a very robust method, however, optimum values of snubber components have to be selected for the balance between the switching losses of the devices and snubber losses to ensure minimum total losses. These methods also involve power scheme complication, resulting in increased weight, volume and price. The active clamping circuits are typically used as backup or protection methods since they generally cause additional switching losses in the devices. The active gate control techniques ensure better voltage balancing and do not increase switching losses and transient times significantly. On the other hand, these circuits are complex, could be less reliable and require components with high operation speed and sensitivity. Moreover, in some cases (unequal recovery of the freewheeling diodes, IGBT tail current period) the active gate

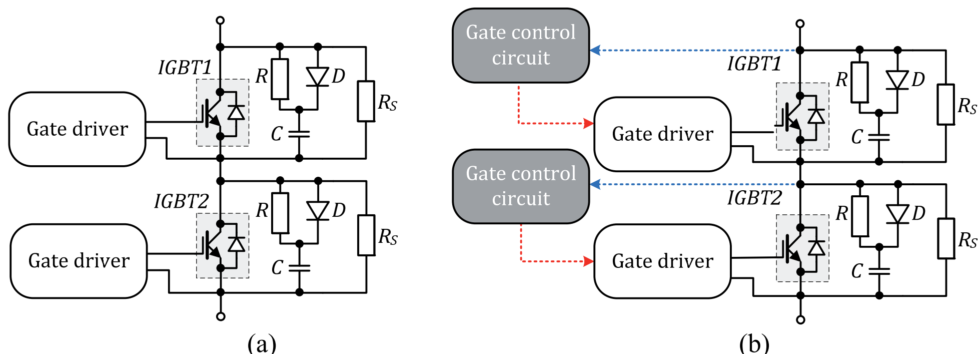


Figure 2.5 RCD snubber network (a) and hybrid voltage balancing method (b)

control methods are unable to ensure proper voltage balancing [24][25]. In this case a hybrid voltage balancing method is an attractive solution (Figure 2.5b). This technique is based on both an active gate control circuit and a small passive snubber, as proposed in [26]. The gate control circuit compares the measured collector-emitter voltage of the IGBT with a reference voltage. The reference is generally defined around 60-70% of the rated voltage of the IGBTs to keep a margin for voltage overshoots. If the sensed voltage is greater than the reference one, the IGBT is supplied with additional charge by driving a small MOSFET. Hence, the gate control circuit will intervene only when the device's voltage is higher than the reference value, therefore the power losses in the gate control circuit are minimised. The snubber in the hybrid circuit minimises the power losses and helps to reduce the voltage overshoot.

HV IGBT

Generally, the HV IGBTs have the same advantages that have supported a wide use of lower voltage IGBTs in modern applications. The gate drive requirements are approximately similar and only require greater isolation of the control system and power supplies. The HV IGBT has a robust switching SOA, allowing snubberless switching [27].

Like lower voltage devices, the HV IGBT module typically includes a FWD to provide a path for the energy flow in reverse direction during the operation. These diodes are generally integrated in the IGBT housing for increased performance and simplified converter design. The typical module package has an IGBT to diode area ratio of around 2:1 [12]. In HV IGBTs fast-recovery power pin-diodes are used. The middle region of these diodes has a much lower doping concentration than the outer p^+- and n^+-layers. The on-state resistance is greatly reduced by high-level injection in the base region, which is known as conductivity modulation. Hence, pin-diodes can be used up to very high blocking voltages. Diodes with blocking voltages of 1.2 kV and above are fabricated by diffusion, where the p^+-layer and the n^+-layer are created by diffusion on a low-doped wafer. Depending on the width of the n^--layer, the diodes could have triangular (NPT- type, Figure 2.6a) or trapezoidal (PT-type,

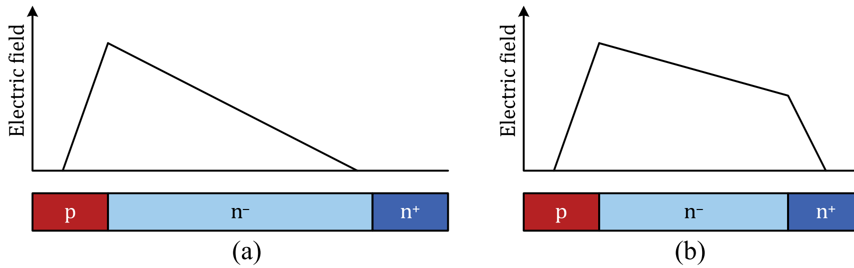


Figure 2.6 Generalised diode structures and electric field distribution: NPT diode (a) and FS diode (b)

Figure 2.6b) shape. The diodes used in power IGBTs are usually produced by using radiation-induced recombination centres (CAL-diodes). In this case the diodes have positive temperature coefficient when conducting the rated current. These diodes should also have "soft" reverse-recovery characteristic (transition period from the conducting to the blocking state) in order not to cause rapid changes in voltage due to high *di/dt* [27].

The first IGBTs for blocking voltages of 1.7 kV and higher were NPT devices [29]. For HV devices this concept leads to a thick device structure and in the case of 6.5 kV modules it may lead to unacceptable forward voltage drop as well as to the switching losses [30]. To overcome this situation the field stop (FS)-concept has been introduced combining PT and NPT features. Using the manufacturing process of the NPT devices, the FS-, as the PT-IGBT, has an additional n^+-buffer layer. This layer, in contrast to the PT-device, is rather lightly doped, just enough to stop the electrical field under blocking voltage conditions. As a result, the thickness of the n^--layer could be reduced significantly in comparison to the NPT-devices, decreasing the conduction losses. The switching characteristics of FS-devices during turn-off depend on

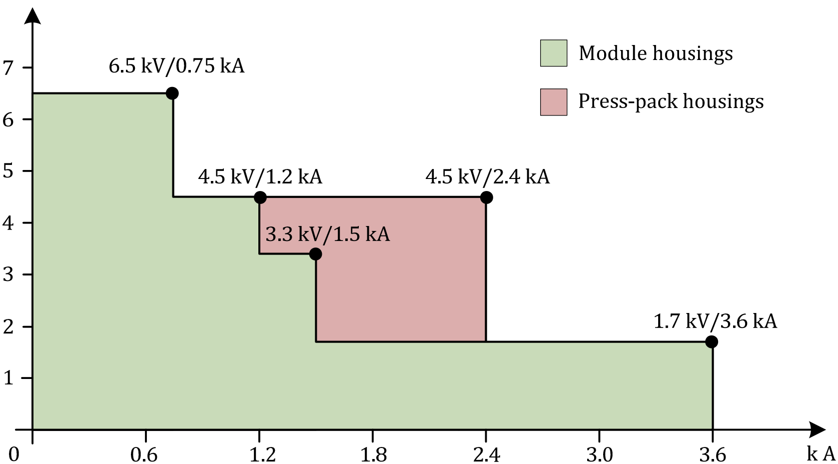


Figure 2.7 Maximum voltage and current ratings of currently commercially available IGBTs

the blocking voltage. At low blocking voltages, the electrical field does not reach the buffer layer, leading to long and low amplitude tail current. At blocking voltages above a certain value, the electrical field reaches the buffer layer leading to a trapezoidal shape of the field. As a result, the IGBT turns-off with a short tail current. A positive temperature coefficient of $U_{CE(sat)}$ has been achieved since the FS technology does not require any additional lifetime reducing processes. However, as in PT-devices, the tail current increases with a higher junction temperature [31][32]. The maximum ratings of presently commercially available IGBTs are presented in Figure 2.7.

Recent improvements in HV IGBT technology

The revealed drawback of the FS-concept was a snappy behaviour when operating in a circuit with high stray inductance. During turn-off at a certain voltage, when the depletion layer is reaching the FS-layer, the collector-emitter voltage increases rapidly, leading to large overvoltages and parasitic oscillations caused by the circuit's parasitic inductance and output capacitance of FS-IGBT [33].

In the last several years, a tendency towards new PT type vertical structures, namely "Soft Punch Through" IGBT (SPT) (Figure 2.8a), "Carrier Storage" (CS) (Figure 2.8b) and "Trench-Field Stop" (Figure 2.8c), has emerged. Further improvements are achieved by an optimisation of the charge carrier concentration in the conducting state. PT-, NPT- and FS-IGBTs have higher carrier concentration on the back side than on the top side. The lower carrier concentration near the emitter increases the $U_{CE(sat)}$, while the high concentration at the collector increases the stored charge and thereby the switching losses. The introduced technologies have increased charge carrier concentration at the top of the device, improving the balance between on-state losses and stored charge. The turn-off behaviour of these IGBTs is similar to that of FS-devices without carrier enhancement technologies [34]. These improvements of IGBT structures allow higher output current per module, enabling a reduction of converter size, weight and cost [29]. Due to diversity of application requirements, some manufacturers produce different versions of HV IGBTs: "soft" – with low conduction losses for low frequency operation and "fast" – with low switching losses for high frequency operation. These modules also feature PT-type freewheeling diodes for lower condition losses. These diodes have an optimised crystalline wafer structure and a deep collector-side n^+ layer concentration profile. Additionally, to provide fast reverse-recovery capability (high *di/dt*) the cathode is designed with a structure that suppresses the concentration of current at the border of the active area [35].

However, substantial work needs to be done to produce diodes with a voltage range of 3 kV and above with satisfactory reverse-recovery behaviour. The applications they operate combine very high switching power and switching transients, which are much faster than those using thyristors and GTOs, with a large parasitic inductance in the circuit. For these applications the

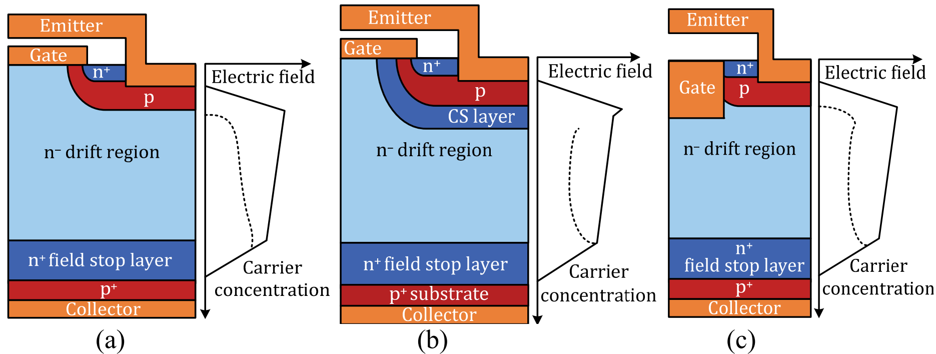


Figure 2.8 Generalised structures of 3.3 kV IGBT technologies: FS- or SPT- IGBT (a), CS-FS-IGBT (b) and Trench-FS-IGBT (c) [29]

optimised diodes are necessary in order to avoid voltage spikes and parasitic oscillations [2]. Additionally, in high-power IGBT modules the diode became a limiting factor in terms of maximum current capability (in both inverter and rectifier mode operation) as well as in terms of its surge current capability. These limitations are a result of the limited diode chip area available in a given package footprint design [12].

2.2 Technology trends

IGBTs with reverse conducting or reverse blocking capability

As mentioned previously, the restricted area available for a freewheeling diode in a power module brings several limitations, such as power density and surge current capability. The simple solution of increasing the diode area is restricted by the package standard footprint design. Therefore, the development effort must aim for improved diode characteristics to match at least the performance of the present state-of-the-art IGBTs. The possible solution to these limitations is an integration of the IGBT and the diode in a single chip forming a reverse-conducting RC-IGBT. The reverse-conducting property of the IGBT could be achieved by forming the n^+-region in a part of the collector p^+-area. Unfortunately, the realisation of such a concept has always been limited by the design and process issues resulting in a number of IGBT vs. diode performance drawbacks. For instance, the moulded diode with a highly doped p-emitter has a very high plasma distribution at the anode side and low at the cathode side, which leads to a high reverse recovery peak and snappy reverse-recovery behaviour.

An improved concept introduced for 3.3 kV IGBT features additional n^--layer surrounding p-well area (Figure 2.9a) [36]. Additionally, low-doped n^- areas together with highly-doped p^+-regions are applied in order to further optimise the reverse-recovery behaviour and IGBT characteristics. As a result, the RC-IGBT exhibits low losses in both rectifier and inverter modes of operation, while also maintaining high levels of SOA performance. In addition,

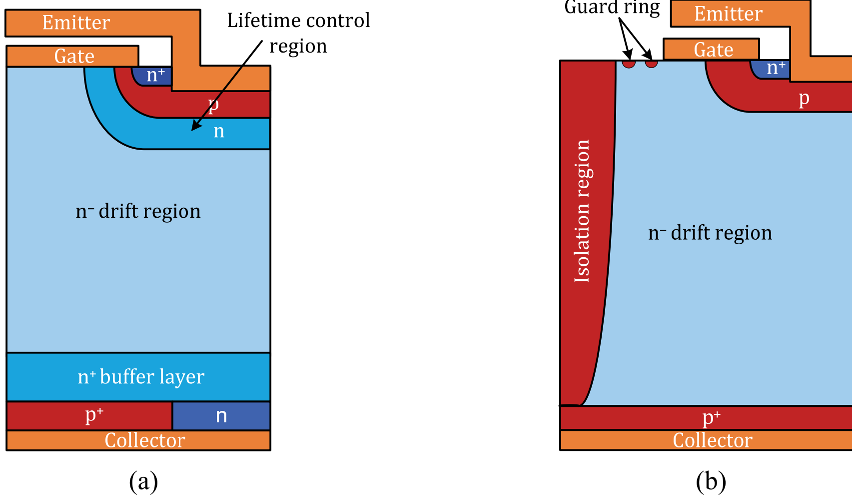


Figure 2.9 RC-IGBT structure with optimised built-in diode (a) and RB-IGBT structure (b)

a number of device performance advantages, such as reliable short-circuit behaviour and better diode mode surge current capability are obtained. The effective IGBT area is increased by 50% and the effective diode area by 200%. Therefore, potentially 50% higher current capability for IGBT modules with the same area is provided. Unfortunately, only a part of it may be used in a real system because of the thermal resistance limitations of the housing [12]. Nevertheless, this technology offers a feasible path for the next generation of power modules with increased power density and good performance.

In some applications of power electronics, such as the matrix converter, current-source converter or AC voltage control systems, a symmetrical voltage blocking device is required. This means that the device should block both forward and reverse voltage during its off-state. The basic IGBT structure is capable of taking an electric field at the bottom-side pn^{-}-junction as well as at the top-side $n^{-}p$-junction, similarly to the reverse-blocking thyristor structure. Unfortunately, the bottom-side pn^{-}-junction does not have defined junction termination, since modern semiconductor fabrication technology is optimised to create microstructures only on one side of a wafer. A possible solution is to lead the back-side pn-junction to the front side of the wafer to create a heavily p^{+}-doped collector wall surrounding the IGBT chip active area (Figure 2.9b) [37]. This collector isolation allows the IGBT to block reverse voltage and maintain stable leakage current characteristics. The NPT IGBT structure is mandatory in this case, hence the RB-IGBT does not have as low $U_{CE(sat)}$ as modern IGBTs with a buffer layer, but the on-state voltage drop will surely be lower than that of a series connected IGBT and diode [2][38]. However, there are still many shortcomings and trade-offs in the design, for example, between reverse-recovery characteristics and $U_{CE(sat)}$.

Semiconductors based on wide band-gap materials

The state-of-the-art HV semiconductor structures are close to the theoretical limits of the silicon (Si) material properties and further optimisations will bring only small steps in performance improvements [39]. This technological barrier has led to consistent research on the development of alternative semiconductor materials. These materials with band-gap energies larger than in Si bring potential advantages, such as higher achievable junction temperatures, thinner drift regions, coefficient of thermal expansion (CTE) better suited to the ceramics used today in packaging technology, etc [40]. The most notable alternative materials are: GaAs, GaN, 4H-SiC, 6H-SiC and diamond. Among all of them, the 4H-SiC polytype material and device fabrication technology is the most developed presently thanks to innovations in bulk and epitaxial growth technologies [41]. Therefore, in the near future, developments in the power devices will be focused on further improvements in this direction.

Commercially available 0.6 kV, 1.2 kV and 1.7 kV 4H-SiC Schottky barrier diodes (SBD) have already made significant changes in the market of lower voltage power converter systems [42]. Active switching devices, such as MOSFETs, BJTs and JFETs, are presently offered in the voltage range up to 1.2 kV [43]. 4H-SiC offers 10 times higher breakdown electrical field compared to silicon, which enabled fabricating samples of MOSFET transistors and junction barrier controlled Schottky (JBS) freewheeling diodes having blocking voltages of up to 10 kV and currents of up to 120 A [42]. The most remarkable recently reported high-voltage SiC semiconductor voltage ratings are presented in Figure 2.10 [43] - [48].

However, there are still a number of technological barriers in the development of HV semiconductors based on wide band-gap materials. The unit cost is still too high to achieve a breakthrough on the commercial market and the long-term reliability, especially at high temperatures, is still under investigation [41]. In addition, a number of the performance advantages offered

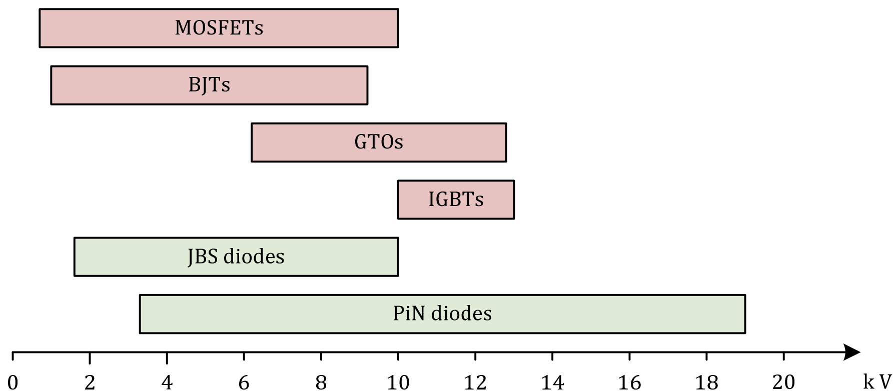


Figure 2.10 Recently reported HV SiC semiconductor voltage ratings

by HV SiC semiconductors, like faster switching or higher blocking voltages, cannot be fully applied presently because of drawbacks in peripheral components. Even state-of-the-art Si HV IGBTs are often slowed down to reduce high *di/dt* values causing transient overvoltages due to relatively high stray inductances in many present applications. Another challenge lies in the packaging technology, where problems with silicone gel stability and partial discharge in ceramics must be solved to utilise all benefits on SiC [49].

As stated above, the major limitation of the state-of-the-art HV IGBTs today is unsatisfactory reverse-recovery behaviour of HV Si FWDs. Therefore, the main focus presently will be on the improvement of the performance of HV IGBTs by using SiC FWDs [49].

2.3 Limitations and failure mechanisms

The reliability of individual power electronic devices and components determines the reliability of the final power electronic system. The system should perform according to the requirements for a defined period under specific conditions [50]. Typical requested lifetime of power electronics products is from 10 years and up to 30 years [6][51]. The requirements to reliability are continuously growing due to several factors, such as constantly increasing power density of the semiconductor housings, which leads to increased temperatures and temperature gradients or appearance of new fields of applications with more severe ambient conditions, like hybrid automotive traction systems. The temperature gradients lead to degradation of materials and interconnections, reducing the lifetime. Among failures due to temperature changes the device could fail due to short-term exceeding its maximum

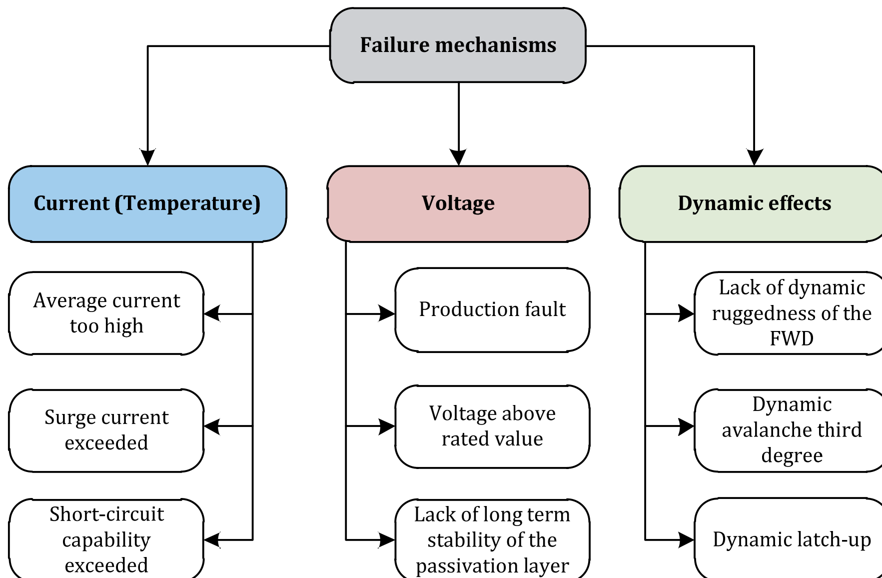


Figure 2.11 Classification of main failure mechanisms in IGBT modules

allowable ratings. The typical failure mechanisms of IGBT modules are given in Figure 2.11 [2]. The present chapter will briefly describe some of the IGBT limitations and their peculiarities.

Safe operation area

Despite having many advantages, the IGBT inherits some drawbacks from both technologies it combines, such as its sensitivity to electrostatic charges (MOSFET) and the tail current at turn-off (BJT) [15]. The other disadvantages include higher conduction losses than in the thyristor-type devices (GTOs, IGCTs), leading to reduced efficiency of the whole system and increasing cooling requirements. Among any other characteristics, the failure-free operation is of major significance. It is particularly important that the maximum allowable ratings − safe operation area (SOA) for forward-bias (FBSOA), reverse-bias (RBSOA), or short-circuit (SCSOA) are wide enough for a given application. This characteristic is usually presented as a dependency between maximum allowable U_{CE} and I_C. Additionally, separate SOA curves may be plotted for different switching times. The SOA characteristic combines the various device limitations, such as maximum current, voltage, power and temperature, in one curve, allowing the design process to be simplified.

Previous experience and publications have reported that the SOA performance of voltage semiconductors rated above 2 kV degrades significantly in comparison to the low and medium voltage class devices. The reason of this downtrend lies in increased stress of operating conditions and physical restrictions in HV structures. Furthermore, the trade-off between the optimisation of the overall losses and the SOA requirements applied further limitations in the design of HV semiconductors [52]. Performance of power semiconductor devices is evaluated in terms of trade-off relationship, which

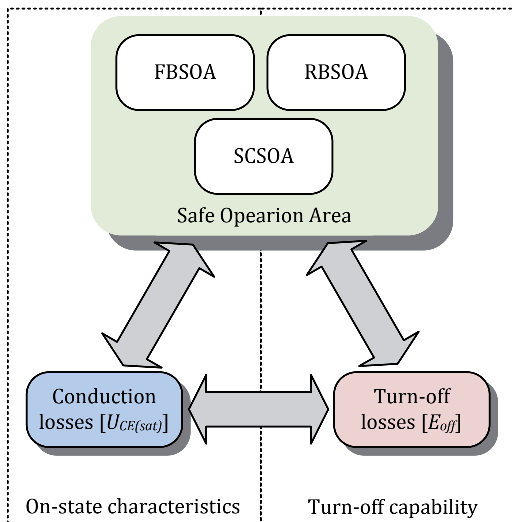


Figure 2.12 IGBT design trade-offs

includes three different safe operation areas, on-state characteristics and turn-off capability (Figure 2.12) [13][53].

The SOA of the freewheeling diode is defined by the maximum instantaneous power dissipation. This limitation determines the maximum current and voltage gradient of the IGBT during switching transients. According to these requirements, a minimum gate resistor is selected [31]. The FBSOA of the IGBT is usually square for short pulse durations. However, since the IGBT is thermally limited, the FBSOA decreases for longer switching periods, as shown in Figure 2.13a.

The RBSOA progressively decreasing as the rate of change of reapplied U_{CE} is increased (Figure 2.13b), due to increased possibility of IGBT latch-up that leads to loss of controllability of the device and its destruction [3].

While for low-voltage IGBTs the short-circuit failure is typically limited due to thermal issues and ageing, this is not the case for HV IGBTs. Thanks to the larger thickness of the device and smaller current density, the temperature increase is typically lower than expected [54]. The ratio between the short-circuit current and the rated current values lies between three (3.3 kV IGBT) and five (6.5 kV IGBT) [32]. The destructive short-circuit tests usually occur before the device has reached its steady short circuit current level, indicating that the failure mechanism is not due to the overtemperature of the device. Furthermore, it was found that minimum ruggedness is about 1 kV for a 3.3 kV rated IGBT, between 1.2 kV and 1.8 kV for a 4.5 kV rated IGBT and around 2 kV for the 6.5 kV IGBT [54]. This failure mode is induced by creating high local current densities due to the imbalance of the electron and hole densities on the surface of the chip. One of the solutions is to increase current density of holes by increasing the collector-emitter efficiency (ratio of minority carrier current in the base region to the total current). Additionally, this eliminates the overshoots in the collector current [55].

The introduction of new IGBT design technologies allows major progress in the SOA limits to be achieved. State-of-the-art devices are able to withstand the high, previously unachievable phase of dynamic avalanche, resulting in a remarkable increase of ruggedness that leads to the ideal square SOA [12].

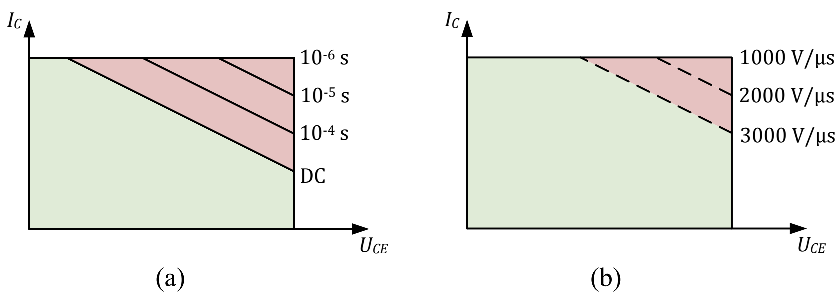


Figure 2.13 Typical safe operating areas of an IGBT: forward-bias (a) and reverse-bias (b)

Switching frequency

The IGBTs are limited not only in terms of highest voltage and current ratings but also in maximum switching frequency. There are several reasons for this limitation. First of all, the switching frequency is limited due to the maximum power dissipation the cooling system could handle. Higher frequencies require more powerful heatsinks to dissipate the heat generated. At some point further increase in the switching frequency becomes infeasible due to size, weight volume and cost of the cooling system required. Secondly, power electronic converters have so-called "critical frequency value". Below this frequency the switching losses are comparable to the other converter losses, and therefore the converter efficiency is not a strong function of the switching frequency. Above the critical frequency, the switching losses start to dominate the total loss and the converter efficiency decreases rapidly with increased frequency (Figure 2.14). At some point, the efficiency of the converter drops below a certain desired value. Hence, the switching losses limit the maximum switching frequency of real converters [1]. Lastly, the transistors have minimum on-state and off-state time requirements. These requirements may depend on a transistor and its driver (turn-on and turn-off delay times, the reverse recovery times of the FWDs, the driver output power or dead times necessary for measuring, protection and monitoring) as well as on actual circuits they operate in. For instance, the HV switches may have limited on-state and off-state periods due to minimum recharge time requirements of external networks (snubbers).

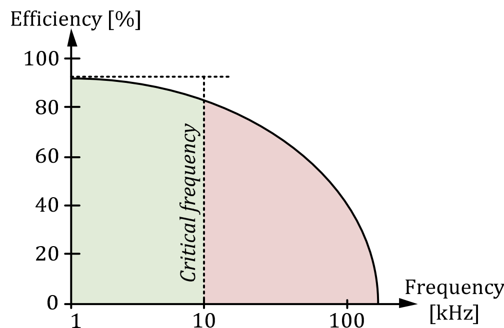


Figure 2.14 Converter efficiency vs. switching frequency using arbitrary values

Packaging and thermal cycling

The housing type of a semiconductor is based on its power range. The most widely used housing type for HV IGBTs is the module-type package. It is characterised by the insulation of electrical components from the heatsink and the integration of additional functions (freewheeling diode, phase-leg, chopper, etc.). On the other hand, single-side cooling limits the maximum power dissipation and internal wire bond interconnections inside the module are

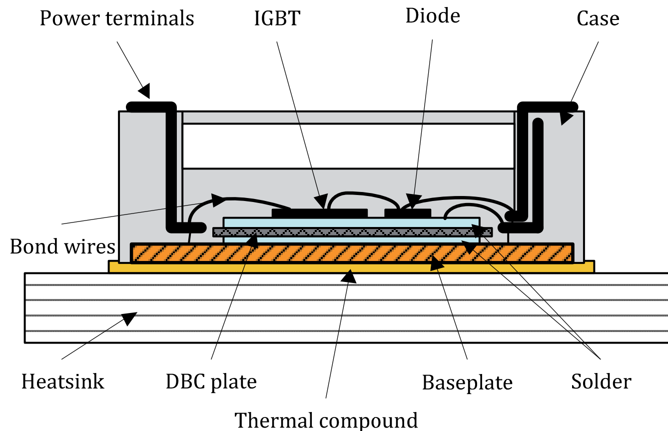


Figure 2.15 Cross-section of a typical power module

a reliability constrictive feature. Another problem that comes from the module-type package is that in some failure modes the power semiconductor is failing as an open circuit, instead of the usual short-circuit failure experienced by GTOs and thyristors. This requires careful design, particularly in current-source applications. The adaptation of the IGBTs to press-pack type housings used for thyristors offers a solution to these problems [17]. In contrast to power modules, a press-pack package could be cooled from two sides, allowing for higher current-rated semiconductors. However, the packages are not dielectrically insulated from the cooling system and are typically used as an element of the electrical circuit. Moreover, complex construction of a press-pack IGBT leads to a considerably increased demand on allowable part tolerances in comparison with a semiconductor module.

In the majority of modern power electronic applications the module-type packages are preferred solutions. Thanks to isolated construction it is easier to integrate multiple electrical chips operating in parallel. Cross-section of a typical power module consisting of different material layers soldered together is shown in Figure 2.15.

As mentioned earlier, in addition to failures due to overload conditions (exceeding of SOA limits) and overheating, the modules could fail due to the thermo-mechanical stress induced by changes in temperature. Since testing the reliability under real application conditions would take as long as the expected lifetime of the power module, the manufacturers have developed a range of accelerated test procedures to estimate expected functionality over the total lifetime in real applications [56]:

- High temperature reverse bias test – verifies the long-term stability of the chip leakage currents. The test is typically performed for 1000h at maximum allowed operation temperature. Devices are stressed with voltages of 80-100% of the nominal blocking voltage.

- High temperature gate stress test – ensures that gate oxide layer is free of defects and clean during the assembly process of a module. The test is performed for 1000h to check blocking capability of gate oxide at maximum allowed gate voltage and operation temperature.
- Temperature humidity bias test – focuses on the impact of humidity on the long-term performance of a power component. The test is performed for 1000h at 85°C and 85% relative humidity. It should verify that high humidity does not lead to corrosion on the chip surfaces.
- High temperature and low temperature storage tests – verifies the integrity of the module components, which must maintain their characteristics in the complete specified storage temperature range. The test should verify that no damage occurs to materials as well as connections due to different CTE.
- Temperature cycling and temperature shock test simulates ambient temperature swings during the field lifetime. This is done to determine the number of cycles when the device fails due to the initiation of cracks, quality of the bond wires and growing delamination in materials.
- In the power cycling test the power chips are actively heated by the losses generated in the power devices themselves to determine the number of cycles when the device fails due to bond wire lift-off or solder degradation.

To determine the lifetime for standard power modules, a research project named LESIT was started in the early 1990s. Modules from different suppliers have been tested with different temperature swings and maximum temperatures. The goal was to create different models of lifetime prediction in accordance with the obtained results. However, since the power module technology is continuously developing, the prediction may not be valid. For instance, the experiments with newer IGBTs show an increase of the number of cycles to failure by a factor of 3 to 5 [2].

The bond wire contact detachment from the IGBT chip is reported to be one of the main reasons of IGBT failure during power cycling. Higher power cycling capability can be achieved by a substitution of the chip solder with a silver sinter technology and by coating with a polyamide cover layer [2].

The next mechanism observed during large temperature swing power cycling is the reconstruction of the chip metallisation. This effect reduces the density of the contact layer and therefore increases its specific resistivity. Change of resistivity impacts the current distribution in the device, which will reduce the lifetime under high stress conditions, such as repetitive short cycles [57].

The degradation of the solder interface is another major mechanism that leads to module failure. The formation of fractures in the solder interface leads to an increase in thermal resistance. This, in turn, increases temperature and power losses (in devices with positive temperature coefficient), resulting in accelerated solder degradation.

Cosmic ray failures

With the introduction of high-voltage semiconductors at the beginning of the 1990s, spontaneous failures were observed unrelated to ageing of the devices or any other failure mechanisms. The failures occurred during the blocking state and their rate increased dramatically past a certain voltage within the nominal operational range. Neutrons with high energy levels generated by cosmic radiation were found to be the reason of this destructive mechanism. In high-power devices a neutron interaction with the semiconductor material produces one or more charged particles, which are accelerated by the high electric field and create secondary charged particles, causing a particle avalanche which allows the device to draw large currents and be destroyed [58]. The failure rate is a strong function of the applied voltage and lowers with increased temperature. Most of the semiconductor devices were redesigned for acceptably low cosmic ray induced failure rates by lowering the maximum internal electric field by hardening of emitters and careful design of edge termination structures [59][60]. To achieve a neglectable failure rate of 100 FIT (1FIT= 1 failure in 10^9 h), specified in requirements, safety margins for typical DC voltages are installed which are higher than necessary for the required blocking capability. These dimensioning rules for cosmic ray stability contradict with other characteristics of a power semiconductor device: conduction and switching losses for IGBTs and soft-recovery behaviour requirements for diodes. A trade-off between different requirements must be made [61].

2.4 Generalisations

The application field of the power electronic converters is constantly increasing thanks to improved power capabilities, simplification of control and reduced costs of power semiconductors. Continuous improvements of the HV IGBTs and cooling system technology have considerably increased the power density of state-of-the-art IGBT chips. A copper baseplate generally used for low-voltage modules has been replaced by that of AlSiC in HV IGBTs, because its CTE is closer to that of the AlN substrate. As a result, both power cycle and temperature cycle lifetimes are several times higher than in the case of a copper baseplate [35]. The physics of silicon semiconductor devices allows maximum junction temperatures up to 200°C. This limit is still not achieved due to limitations is the packaging technology. However, new techniques for joining parts as well as soldering technologies allow increasing the maximum junction temperature of state-of-the-art HV modules to 150°C from the typical 125°C. Extending the maximum operation temperature leads to a significant increase of current carrying capability and dissipateable power [59].

Further improvements in power cycling capability can be achieved by adapting diffusion sinter technology. This interconnection technology has superior properties over traditional solder interfaces: higher thermal and electrical conductivity, lower parameter manufacturing distribution. The power

cycling tests reposted an extreme increase in reliability – by more than a factor of 20 compared to results estimated with LESIT data. [62][63]. Aluminium wire bonds with silver foil contacts can be improved by the silver diffusion sinter technology. As a result, thermal and electrical conductivity as well as CTE become more favourable, improving the power cycling capability [64].

State-of-the-art HV IGBTs feature an ultimate square SOA and a neglectable cosmic ray failure rate. The technology of these devices is close to the so-called "Silicon Design Limits" and future improvements will provide only small steps in further optimisation. A major progress is estimated with the HV semiconductors based on wide band-gap materials. However, presently only experimental samples of these devices are being produced. The quality, power handling and manufacturing cost leave much to be desired.

3 IMPLEMENTATION CHALLENGES OF HV IGBTs IN TWO-LEVEL HARD-SWITCHED DC/DC CONVERTERS

Recent advancements in power semiconductor technology, such as the introduction of IGBT modules with blocking voltages up to 6.5 kV, have made it possible to construct simple two-level inverters for high-voltage converter systems, without using series connection of semiconductor switches or converter stages. New high-voltage semiconductor switches and topologies could be used in a wide variety of applications, like transmission line converters, volt-ampere reactive compensators, rolling stock traction, marine and auxiliary power supply converters. The rolling stock is one of the most demanding applications of power electronics with its very high safety and reliability requirements.

As a case study for this PhD research, the two-level galvanically isolated half-bridge DC/DC converter developed for 3.0 kV DC-fed rolling stock was selected. The converter is aimed for interfacing the HV contact line with low voltage secondary systems, which provide a wide range of output voltages for different on-board systems of rolling stock, like ventilation, lighting, communication and batteries. The converter consists of primary and secondary parts, galvanically isolated by the high frequency transformer. The primary part is a square-wave two-level half-bridge PWM inverter with two input capacitors.

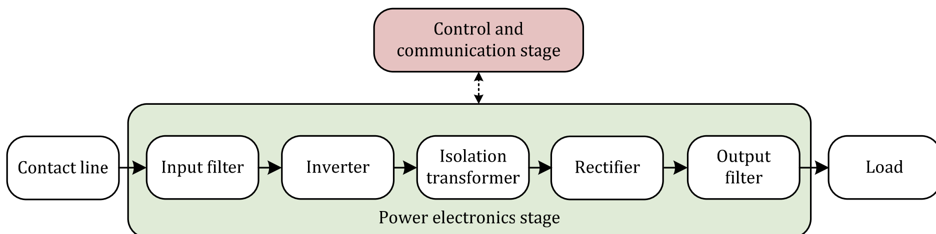


Figure 3.1 Block diagram of the developed converter

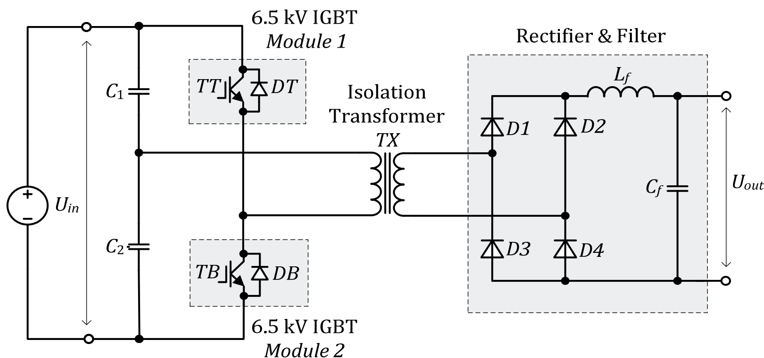


Figure 3.2 Simplified schematic of the developed two-level converter

Table 3.1 Desired parameters of the converter

Parameter	Symbol	Value
Maximum input voltage, kV	$U_{in(max)}$	4.0
Minimum input voltage, kV	$U_{in(min)}$	2.2
Nominal input voltage, kV	$U_{in(nom)}$	3.0
Maximum switch duty cycle	D_{max}	0.4
Minimum switch duty cycle	D_{min}	0.22
Nominal switch duty cycle	D_{nom}	0.30
Output power, kW	P_{out}	50
Nominal output voltage, V	U_{out}	350
Switching frequency, Hz	f_{sw}	1000

Table 3.2 Main components of the two-level converter prototype

Component	Symbol	Type	Value
Input capacitors	C_1, C_2	Polymer film capacitor	3×100 µF
Inverter switches	*Module 1,2*	FZ200R65KF1	600 A/6.5 kV
Transformer	*TX*	High frequency toroidal transformer with soft nanocrystalline core material GM14DC	44/18
Rectifier diodes	*D1-D4*	Dual FRED modules IXYS DSEI2x101-12A (2 diodes in parallel)	2x100 A / 1.2 kV
Filter inductor	L_f	Laminated steel core inductor	5 mH
Filter capacitor	C_f	Electrolytic capacitor	735 µF

The secondary part consists of a full-bridge diode rectifier and an LC filter (Figure 3.1).

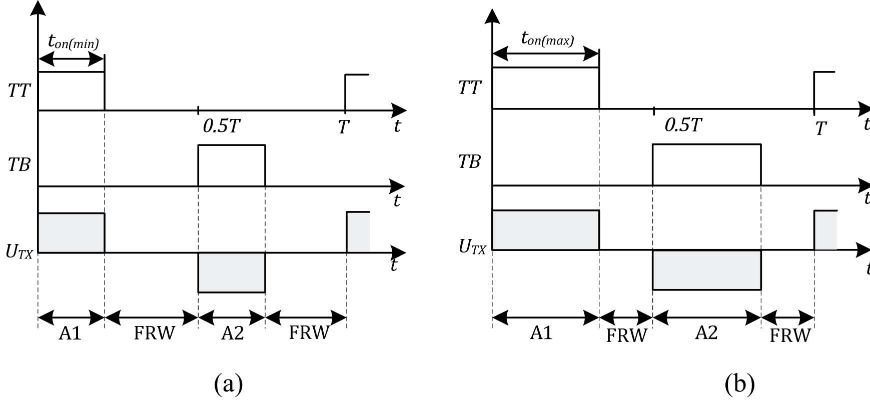
The simplified schematic of the converter is shown in Figure 3.2 and the main parameters are listed in Table 3.1. The components used in the converter prototype are listed in Table 3.2.

3.1 Influence of parasitic transient processes

The two-level half-bridge inverter has two main operating states: active states (A1, A2) and a freewheeling state (FRW). During active states, the two transistors *TT* (top switch) and *TB* (bottom switch) are switched alternately, providing positive and negative square-wave impulses with the amplitude of $U_{in}/2$ on the isolation transformer *TX* primary winding (Table 3.3). Since even a short-time simultaneous opening of the two transistors will result in short-circuit, the maximum on-state time t_{on} of the transistor control pulse should not exceed 80% of the half period (Figure 3.3) [67]. Another part of the switching period is a freewheeling state when both transistors are off. During this state the transformer voltage is zero.

Table 3.3 Switching states of a two-level inverter

Switching state	Transistor state		Output Voltage
	TT	*TB*	
A1	ON	OFF	- $U_{in}/2$
FRW	OFF	OFF	0
A2	OFF	ON	+ $U_{in}/2$



(a) (b)

Figure 3.3 Operation principle of a two-level half-bridge DC/DC converter: maximal input voltage (a) and minimal input voltage (b)

In a real inverter, every element has stray inductance, resistance and capacitance. These parasitic components have an influence on the performance and if not considered, could lead to dangerous overvoltages, electromagnetic interference (EMI) problems and damage of the inverter. In the studied case the switching process is mostly influenced by the stray inductance of the isolation transformer and parasitic inductance of the wiring as well as the junction capacitances of HV IGBT modules. The IGBT turn-on energy loss decreases while the turn-off energy loss increases together with the circuit inductance. During turn-on, the inductance takes over part of the blocking voltage due to the current slope, so the remaining blocking voltage across the IGBT during the turn-on decreases. Thus, the turn-on energy decreases as well. Turn-off energy, on the other hand, increases because of the increase in the current fall time due to increased inductance [68].

In high frequency inverters, overvoltages caused by the energy stored in the circuit parasitic inductance could cause a high voltage spike on the switching semiconductor device. Increased gate resistance slows the IGBT switching process, limiting overvoltages, on the other hand, increasing switching losses. However, this process does not occur in the investigated inverter, since the freewheeling diode starts to conduct before a noticeable overvoltage spike occurs. On the other hand, the stored energy causes voltage across the transistor to increase up to U_{in} during turn-off; this process is then followed by voltage and current oscillations typical for hard-switched half-bridge (HB) topologies. As a result, the energy stored in parasitic circuit elements is dissipated during every half-period.

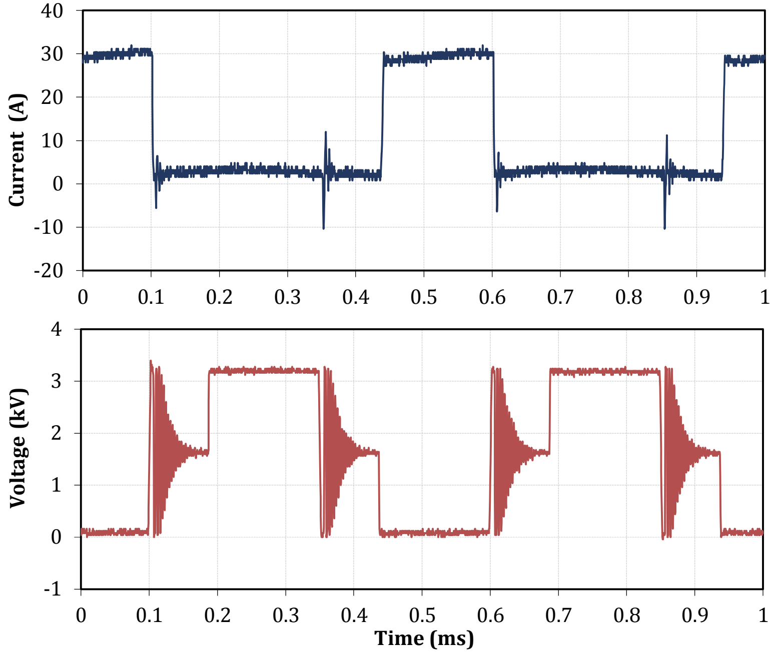


Figure 3.4 Experimental current and voltage of the IGBT Module 1 (U_{in}=3.2 kV; f_{sw}=2 kHz, D=0.32, 30 kW load)

As shown in Figure 3.4, the switching process is far from ideal, especially during turn-off. Although the frequency of these oscillations is not high (around 330 kHz) to generate radiated EMI, it can cause some problems with conducted EMI in the contact line. The analysis of the switching processes was presented in [PAPER-I] and the most important aspects are pointed out in the following sections.

Mathematical analysis of switching transients

Based on the parameters that are most influential to the active and freewheeling states, simplified equivalent circuits for the considered half-bridge converter were elaborated (Figure 3.5).

The value of the equivalent load resistance (neglecting losses) can be obtained from [69]:

$$R_L = \frac{U^2{}_{Prms}}{P_{out}}, \tag{3.1.1}$$

where U_{Prms} is the transformer primary RMS voltage. The transformer primary RMS voltage is proportional to the converter input voltage:

$$U_{Prms} = \frac{U_{in}}{2} \cdot \sqrt{2 \cdot D}\,. \tag{3.1.2}$$

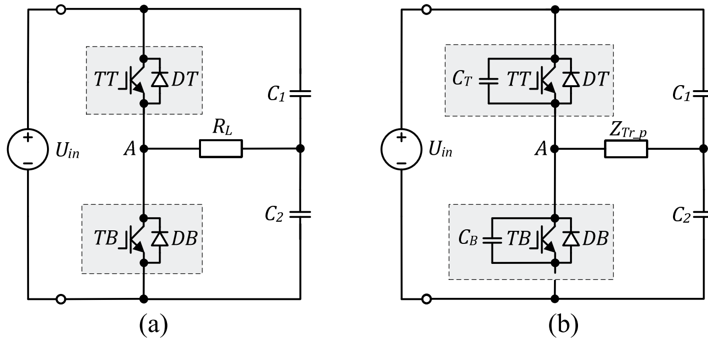


Figure 3.5 Simplified equivalent circuit of the half-bridge converter according to the active state (a) and according to the FRW state (b)

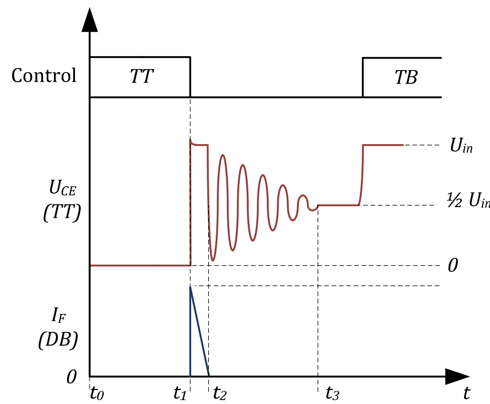


Figure 3.6 Generalised inverter switching waveforms

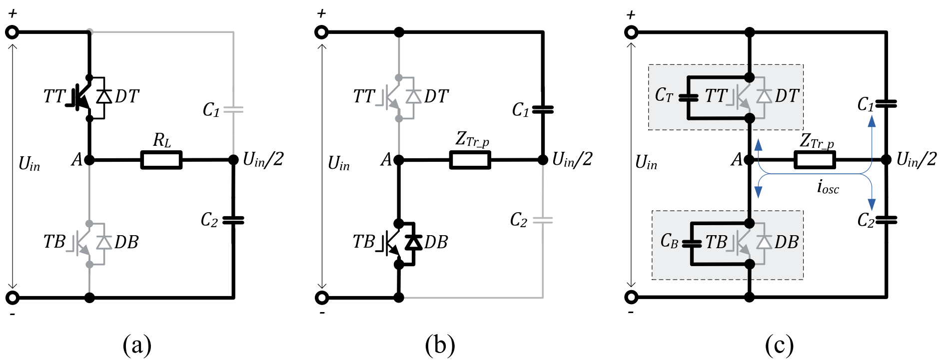


Figure 3.7 Equivalent circuits and current flow paths according to intervals t_0-t_1 (a), t_1-t_2 (b) and t_2-t_3 (c)

The magnitude of the circuit impedance is

$$Z_{Tr-p} = \sqrt{R_E{}^2 + \left[2 \cdot \pi \cdot f_{osc} \cdot L_E - \frac{1}{2 \cdot \pi \cdot f_{osc} \cdot C_{Tr-p}}\right]^2}, \qquad (3.1.3)$$

where f_{osc} is the frequency of parasitic oscillations, L_E and R_E in this section are mainly represented by inductance and active resistance of inverter busbar, wiring and transformer primary winding, respectively. Parasitic capacitive component $C_{Tr\text{-}p}$ is generally represented by effective distributed capacitances of the primary winding.

During the active state the current I_C flows through the top or bottom transistor, input capacitors C_1 and C_2 and the primary and secondary windings of the isolation transformer. The generalised turn-off process of the *Module 1* is shown in Figure 3.6 [70]. The following events can be distinguished:

t_0-t_1 – Transistor *TT* is conducting, the current flows through R_L (Figure 3.7a),

t_1 – A negative gate control voltage is applied to the *TT* transistor, closing it and starting the freewheeling state. Transistor internal capacitances begin to discharge and the collector-emitter voltage $U_{CE(t)}$ of the IGBT begins to rise. As the current I_C through the transistor decreases, the energy stored in the stray inductance of the power circuit develops a negative voltage potential at point *A*.

t_1-t_2 – After the voltage potential at point *A* becomes lower than the ground potential of U_{in}, the current i_F begins to flow through the freewheeling diode *DB* (Figure 3.7b). The maximal current $I_{F(peak)}$ through the diode at the instant of turn-off is equal to the *TT* collector current $I_{C(max)}$ before turn-off. The current then decays exponentially when $i_F(t) \geq 0$ according to

$$I_C = I_{F(peak)} = \frac{P_{out}}{U_{in} \cdot D} = \frac{U_{in}}{2 \cdot R_L}, \tag{3.1.4}$$

$$i_F(t) = \left(I_{F(peak)} + \frac{U_{in}}{2 \cdot R_E} \right) \cdot e^{\frac{-R_E \cdot t}{L_E}} - \frac{U_{in}}{2 \cdot R_E}. \tag{3.1.5}$$

The current follows this equation until it equals zero. The current then remains at zero until the next diode conduction. The duration of decaying *DB* current is described by the following equation:

$$t_2 - t_1 = \frac{L_E}{R_E} \left[\ln\left(I_F + \frac{U_{in}}{2 \cdot R_E} \right) - \ln\left(\frac{U_{in}}{2 \cdot R_E} \right) \right]. \tag{3.1.6}$$

t_2-t_3 – After depletion of the energy stored in stray inductance, the current through *DB* stops. The output capacitances of IGBT modules C_T and C_B together with the stray inductance L_E and equivalent impedance of circuit $Z_{Tr\text{-}p}$ form an oscillating RLC circuit (Figure 3.7c). Voltage and current in this RLC circuit oscillates until being damped by active resistance and the voltage potential of point *A* becomes equal to U_{in} /2.

Determination of the parasitic elements causing oscillations requires a simulation model to be elaborated. The oscillation frequency of the damped circuit f_{osc} is

$$f_{osc} = \frac{1}{T_{osc}} = \frac{\omega}{2 \cdot \pi} = \frac{\sqrt{{\omega_0}^2 - \delta^2}}{2 \cdot \pi}, \quad (3.1.7)$$

where undamped resonance frequency $\omega_0 = 1/\sqrt{L_E \cdot C_E}$, attenuation $\delta = R_{HF}/(2 \cdot L_E)$, R_{HF} is the equivalent high-frequency resistance and C_E is generally represented by the sum of equal paralleled IGBT parasitic capacitances C_T and C_B

According to the measurements, the oscillation frequency is 330 kHz. Oscillation is described by the oscillatory circuit quality factor Q as follows:

$$Q = \frac{2 \cdot \pi \cdot f_{osc} \cdot E_s}{P_{osc}} = \frac{1}{R_{HF}} \cdot \sqrt{\frac{L_E}{C_E}} = \frac{\pi}{\ln(U_n / U_{(n+1)})}, \quad (3.1.8)$$

where, U_n and U_{n+1} are amplitude values of voltage oscillations separated by the time interval of T_{osc}. The equivalent stray inductance L_E can be obtained by

$$L_E = \frac{R_{HF}}{2 \cdot \ln(U_n / U_{n+1})) \cdot f_{osc}}. \quad (3.1.9)$$

Equivalent module capacitances can be obtained from the oscillation frequency equation

$$C_T = C_B = \frac{1}{2} \cdot \left(\frac{1}{L_E \cdot (\omega^2 + \delta^2)} \right). \quad (3.1.10)$$

The voltage oscillations across transistor after *DB* current decay follow the equation [71]:

$$u_{osc} = \frac{U_{in} \cdot \omega_0}{2 \cdot \omega} \cdot \cos\left(\omega \cdot t - \arctan \frac{\delta}{\omega} \right) \cdot e^{-\delta \cdot t}, \quad (3.1.11)$$

and oscillating current is

$$i_{osc} = \frac{U_{in}}{2 \cdot \omega \cdot L_E} \cdot \sin \omega \cdot t \cdot e^{-\delta \cdot t}. \quad (3.1.12)$$

Simulation models and results

According to a generalised equivalent circuit, the simulation model is created using PSIM software. The simulation model elaborated includes the values presented in Table 3.4. Obtained simulation results shown in Figure 3.8a were compared with the laboratory measurements of the inverter prototype (Figure 3.4). Since the simulation is based on an idealised IGBT model, the freewheeling diode reverse-recovery influence on the operation was not considered. To overcome this inaccuracy, a more precise model was created using PSpice software (Figure 3.8b). The obtained simulation results were

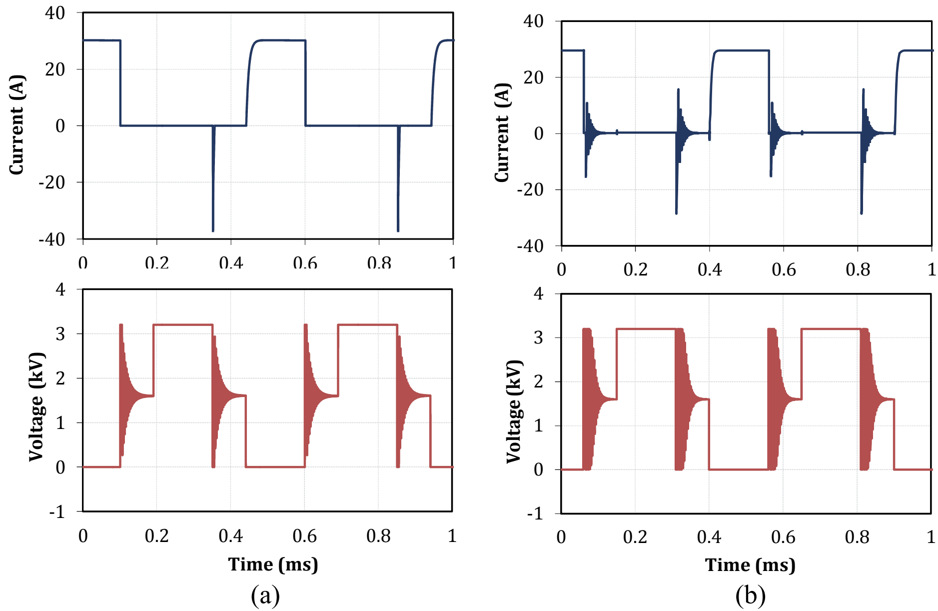


Figure 3.8 IGBT Module 1 voltage and current simulated in PSIM (a) and PSpice (b) (U_{in}=3.2 kV; f_{sw}=2 kHz, D=0.32; 30 kW load)

Table 3.4 Simulation parameters

Parameter	Symbol	Value
Input voltage, kV	U_{in}	2.2…4.0
Inverter input capacitances, μF	C_1, C_2	300
IGBT parasitic capacitances, nF	C_T, C_B	1.4
Equivalent stray inductance, μH	L_E	186
Equivalent impedance at 310 kHz, Ω	$Z_{Tr\text{-}p}$	81.8
Switch duty cycle	D	0.22…0.4

found to be in better compliance with the experimental values, as shown in Figure 3.9. The presence of the oscillations showed no significant impact on the performance in the simulations as well as during the laboratory tests. The oscillating current remained relatively low; hence, the energy of the oscillations is relatively low as well. The frequency of oscillations was found independent of the input voltage or the switching frequency of transistors and remained at approximately 330 kHz. The amplitude value of oscillations is proportional to the input voltage. The value of the diode current depends on the converter output power, i.e. the more energy is stored in the parasitic inductance, the more current is required to deplete it. On the contrary, under light load operation, the duration of diode current is decreased.

The simulation model showed similar results compared to the values obtained during the laboratory test of the converter prototype. Although not entirely precise, the simulation model gives an adequate estimation of the processes that occurred during the laboratory tests.

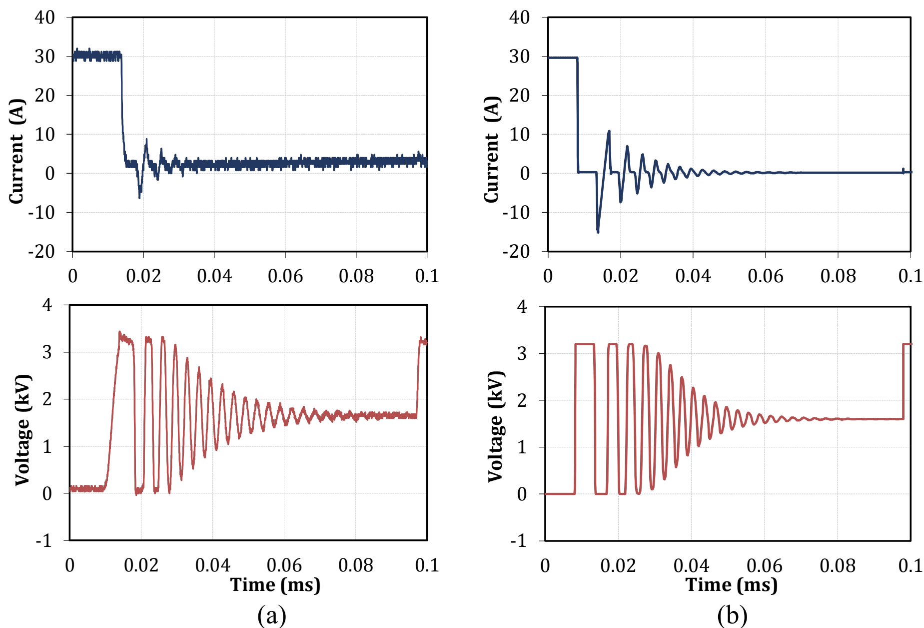


Figure 3.9 Turn-off process of the TT IGBT: experimental (a) and simulated in PSpice (b) (U_{in}=3.2 kV; f_{sw}=2 kHz, D=0.32; 30 kW load)

3.2 Power loss distribution and thermal management issues

The accurate estimation of power losses is an important step in thermal management system design [72]. A number of calculation methods have been proposed. One of the approaches is based on the switching functions or coefficients obtained through measurements to guide the simulation during switching transients [73][74]. However, this method requires a number of parameters to be extracted from the test waveforms. Another approach is based on the use of simple functions derived for losses based on typical switching waveforms [75][76]. This method was extended in [77] by providing a set of equations for switching losses based on the predicted current and voltage waveforms of the device. In this method the predicted waveforms conform to the physics of the switching process and take into account the dependency of the switching losses on various factors, such as the switching voltage, switching current, stray inductance, and the reverse recovery process of the freewheeling diode [77]. Another advantage is that it requires a smaller number of parameters from the test waveforms. If a power electronic system prototype is unavailable, the losses can be estimated by the help of the datasheet parameters of the devices using linear interpolation of characteristic curves [78][79].

This approach is generally limited in accuracy, however, it could be considered as a first approximation. Improved calculation methods using manufacturers' datasheet parameters of semiconductors for inverters with the

square-wave output were presented in [PAPER-II]. The most important aspects are pointed out in the following sections.

Energy loss definitions

The power loss of each switching operation for the given current and voltage waveforms of the IGBT is divided into three sections, as illustrated in Figure 3.10 [80]. The leakage loss is only a small part of the total loss so that

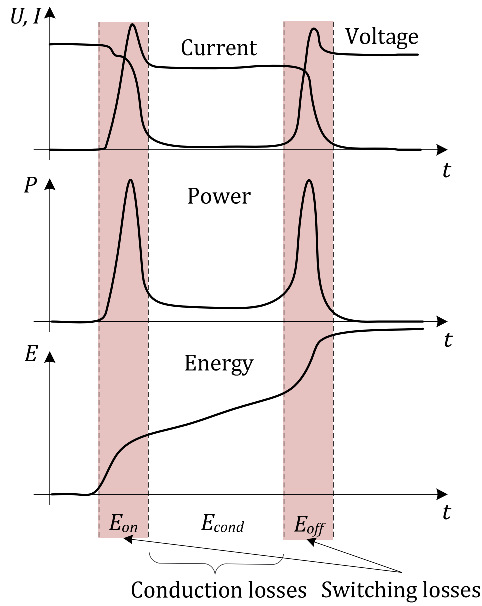


Figure 3.10 Three sections of losses

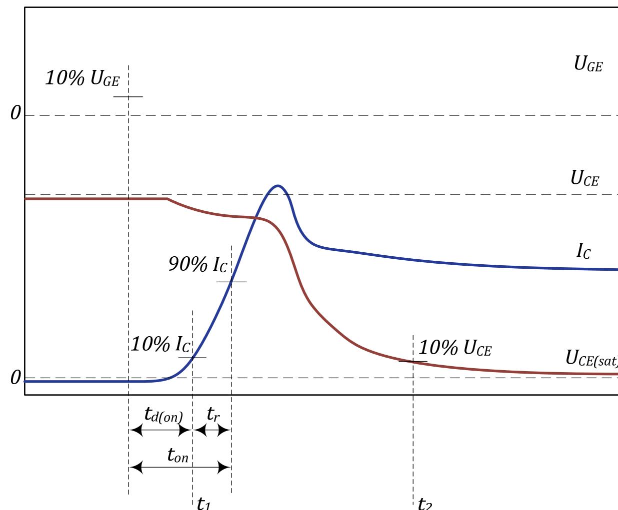


Figure 3.11 IGBT switching times and energy definitions during turn-on

neglecting it, the error is usually insignificant. Therefore, the total energy losses during each operating cycle of the IGBT are the sum of the turn-on and turn-off loss, saturated conduction loss as well as the reverse-recovery loss of the FWD [77]:

$$E_{tot} = \int i(t) \cdot u(t) \cdot dt \,, \tag{3.2.1}$$

where *i(t)* and *u(t)* are transistor instantaneous current and voltage, respectively.

The datasheets of IGBTs contain typical information about switching transients, on-state behaviour and energy losses during a single operation pulse. These characteristics refer to a specific test circuit which simulates a clamped inductive load operating with a specific diode [75].

For high-voltage IGBT modules, the turn-on energy loss E_{on} is generally defined as the integral of the product of the collector current and the collector-emitter voltage over the interval from when the collector current rises above

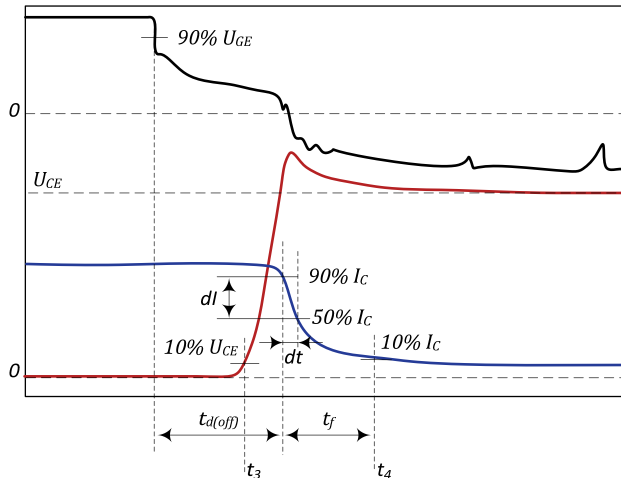


Figure 3.12 IGBT switching times and energy definitions during turn-off

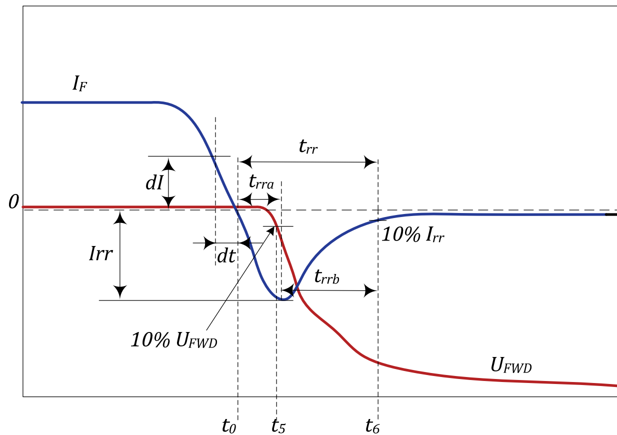


Figure 3.13 Diode switching times and energy definitions during reverse-recovery

10% of the test current to when the voltage falls below 10% of the test voltage (Figure 3.11). The turn-off energy loss E_{off} is the integral of the product of the collector current and the collector-emitter voltage over the interval starting from when the collector-emitter voltage rises above 10% of the test voltage to when the collector current reaches 10% of the test current (Figure 3.12). The diode reverse-recovery energy E_{rec} is the integral of the product of the diode current and voltage over the interval starting from when the voltage across the diode rises above 10% of the test voltage to when the diode reverse current drops to 10% of its peak value (Figure 3.13).

Power loss calculation using datasheet parameters

The on-state voltage drop of the NPT-IGBT device generally increases with a higher collector current and the junction temperature. Moreover, it could vary from one device to another. The datasheets typically indicate the typical and the maximum values. The maximum values generally refer to the worst case device that the manufacturers consider as qualitative. For example, the 200A 6.5 kV IGBT $U_{CE(sat)}$ varies from 5.3 V (typical) to 5.9 V (maximal) for the 200 A collector current at the junction temperature of 125°C. Generally, use of typical values at the maximum junction temperature could be considered reasonably accurate. The conduction losses are estimated by

$$P_{cond} = \frac{1}{T_{sw}} \cdot \int_{0}^{t_{on}} i_C \cdot u_{CE(sat)}\left(i_C, T_j, k_{(sat)}\right), \qquad (3.2.2)$$

where T_{sw} is the switching period, t_{on} is the on-state time, T_j is the switch junction temperature, i_C and $u_{CE(sat)}$ are instantaneous collector current and collector-emitter voltage, respectively, $k_{(sat)}$ is the scale factor based on the properties of the device considered.

The switching energy loss of a device is variable due to the device's current, voltage, gate resistance and junction temperature. Generally, the latter dependency is not indicated in the datasheets, while the energy loss versus current and gate resistance are indicated at the maximum junction temperature. Since the losses increase with increased temperature, it is assumed in the following that the junction temperature will be 125°C as a worst case [78]. In general, the turn-on and turn-off energies are obtained by

$$E_{on} = \int_{t_1}^{t_2} i_C \cdot u_{CE} \cdot dt \,, \qquad (3.2.3)$$

$$E_{off} = \int_{t_3}^{t_4} i_C \cdot u_{CE} \cdot dt \,. \qquad (3.2.4)$$

To achieve fast analytical calculations, the on-state voltage drop can be characterised by a dynamical resistance r_T and a constant voltage drop U_{T0}. The voltage drop across the IGBT with rms collector current is then determined by

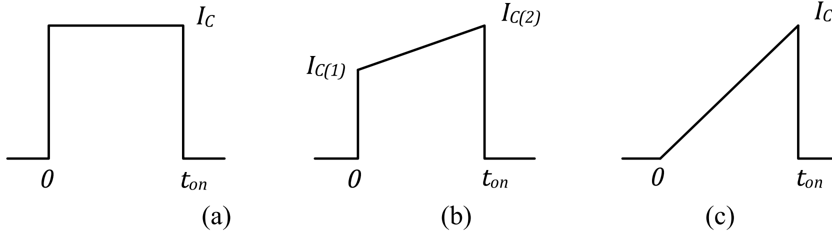


Figure 3.14 Typical current waveforms of IGBTs operating in switching converters

$$U_{CE(sat)} \approx U_{T0} + r_T \cdot I_C^{rms}, \tag{3.2.5}$$

where U_{T0} is the device's threshold voltage, r_T is the device's slope resistance and I_C^{rms} is the transistor RMS collector current.

The on-state energy dissipation for typical IGBT current waveforms (Figure 3.14) could be obtained by simple equations:

a) For the waveform shown in Figure 3.14a

$$i_C(t) = I_C. \tag{3.2.6}$$

Conduction energy losses for the given pulse length

$$E_{cond} = \left(U_{T0} \cdot I_C + r_T \cdot I_C^2\right) \cdot t_{on}. \tag{3.2.7}$$

b) For the waveform shown in Figure 3.14b

$$i_C(t) = I_{C(1)} + \left(I_{C(2)} - I_{C(1)}\right) \cdot \frac{t}{t_{on}}. \tag{3.2.8}$$

Conduction energy losses for the given pulse length

$$E_{cond} = \begin{bmatrix} U_{T0} \cdot \dfrac{I_{C(1)} + I_{C(2)}}{2} + \\ + \dfrac{1}{3} \cdot r_T \cdot \left(I_{C(1)}^2 + I_{C(1)} \cdot I_{C(2)} + I_{C(2)}^2\right) \end{bmatrix} \cdot t_{on}. \tag{3.2.9}$$

c) For the waveform shown in Figure 3.14c

$$i_C(t) = I_C \cdot \frac{t}{t_{on}}. \tag{3.2.10}$$

Conduction energy losses for the given pulse length

$$E_{cond} = \frac{1}{6} \cdot I_C \cdot t_{on} \cdot \left(3 \cdot U_{T0} + 2 \cdot I_C \cdot r_T\right). \tag{3.2.11}$$

The conduction power losses can then be calculated by

$$P_{cond} = f_{sw} \cdot E_{cond}. \tag{3.2.12}$$

The conduction losses of the diodes are calculated in a similar way by using the appropriate dynamical resistance and a constant voltage drop of the investigated diode.

No simple expression can be found for the voltage and current during a switching transient. The datasheet parameters concerning the switching losses can be used in this case. To simplify the analysis for different current levels, the datasheet energy loss curves could be replaced by their linear interpolations using simple equations:

$$E_{on} = A_{on} \cdot I_C + B_{on}, \qquad (3.2.13)$$

$$A_{on} = \frac{\Delta E_{on}}{\Delta I_C} = \frac{E_{on(2)} - E_{on(1)}}{I_{C(2)} - I_{C(1)}}, \qquad (3.2.14)$$

$$B_{on} = E_{on(2)} - A_{on} \cdot I_{C(2)}, \qquad (3.2.15)$$

where $I_{C(1)}$, $I_{C(2)}$ are currents and $E_{on(1)}$, $E_{on(2)}$ the corresponding energy loss values taken from the datasheet graphs. The turn-off coefficients A_{off} and B_{off} are calculated in the similar way.

Since the actual operation parameters of semiconductors are in most cases different from the reference circuit, datasheet values should be scaled accordingly. If the gate resistor of a user's gate drive does not have the same value as the gate resistor in the test circuit specified in the datasheet, some corrections may be necessary. This can be done with the help of the datasheet using graphs $E_{on}=f(R_G)$ and $E_{off}=f(R_G)$. The scale factor is obtained by the relation between the switching losses with the used-specific gate resistance R_{G-on}^{US} and the one specified in the datasheet R_{G-on}^{DS} [73]:

$$k_{(R_{G-on})} = \frac{E_{on}\left(R_{G-on}^{US}\right)}{E_{on}\left(R_{G-on}^{DS}\right)}. \qquad (3.2.16)$$

The turn-off resistor scale factor $k_{(R_{G-off})}$ is calculated in the similar way.

Generally, the switching losses scale almost linearly with U_{CE}, hence the following approximation of the scale factor for the actual commutation voltage could be considered reasonably accurate:

$$k_{(U_{CE-on})} = \frac{U_{CE-on}^{US}}{U_{CE}^{DS}}, \qquad (3.2.17)$$

where U_{CE-on}^{US} is DC voltage across the IGBT during the off-state before the beginning of the turn-on transition, U_{CE}^{DS} is the collector-emitter voltage specified in the datasheet graphs $E_{on}=f(I_C)$, $E_{off}=f(I_C)$. The scale factor for the actual commutation voltage $k_{(U_{CE-off})}$ during the turn-off is obtained in the similar way.

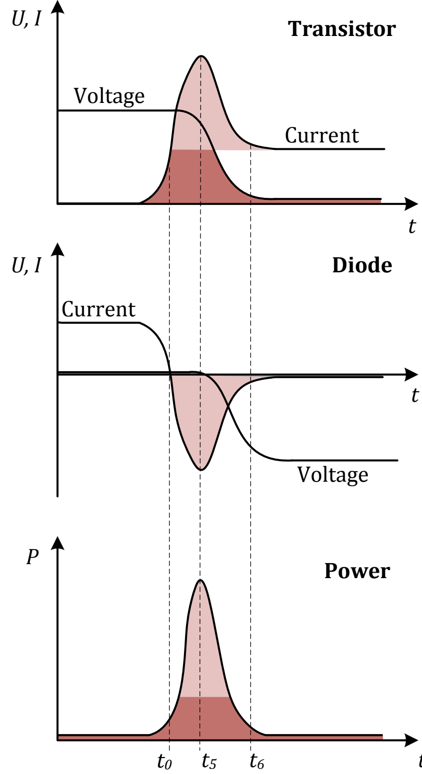


Figure 3.15 Typical IGBT module voltage, current and power turn-on waveforms

The turn-on energy losses indicated in the datasheet of the IGBT typically include the losses caused by the reverse-recovery current of turning-off the freewheeling diode (Figure 3.15). No simple expression can be given for these additional losses, since they depend on a number of factors, such as turn-on *di/dt*, circuit inductance and diode characteristics. The following equation [81] assumes that the voltage across the diode stays close to zero during the interval t_0-t_5, rising to the supply voltage during t_5-t_6, as shown in Figure 3.13:

$$\begin{aligned} E_{on} &= U_{CE-on}^{US} \cdot I_C \cdot \left[\left(1 + \frac{1}{2} \cdot \frac{I_{rec}}{I_C} \right) \cdot t_{0-5} + \frac{1}{4} \cdot \frac{I_{rec}}{I_C} \cdot t_{5-6} \right] = \\ &= U_{CE-on}^{US} \cdot \left(I_C \cdot t_{0-5} + Q_{t_{0-5}} + \frac{1}{2} \cdot Q_{t_{5-6}} \right), \end{aligned} \tag{3.2.18}$$

where I_{rec} is the peak reverse-recovery current.

However, according to the experimental waveforms (Figure 3.4) in the considered two-level half-bridge DC/DC converter, the reverse-recovery process of the freewheeling diodes is typically finished during the freewheeling state. The IGBT turns on without the effect of the reverse recovery current of a commutating diode, adding to the IGBT turn-on loss (Figure 3.4) that results in

lower losses. Therefore, additional scale factor k_{on}^{rec} should be applied to the turn-on loss equations. This scale factor depends on the properties of the freewheeling diode and operation temperature. For typical IGBT modules it is generally in the range of 0.5…0.7.

The switching energy losses for typical current waveforms (Fig. 5) can be approximated by the following expressions.

a) For the waveform shown in Figure 3.14a

$$E_{on} = \left(A_{on} \cdot I_C + B_{on}\right) \cdot k_{R_{G-on}} \cdot k_{U_{CE-on}} \cdot k_{on}^{rec}, \tag{3.2.19}$$

$$E_{off} = \left(A_{off} \cdot I_C + B_{off}\right) \cdot k_{R_{G-off}} \cdot k_{U_{CE-off}}. \tag{3.2.20}$$

b) For the waveform shown in Figure 3.14b

$$E_{on} = \left(A_{on} \cdot I_{C(1)} + B_{on}\right) \cdot k_{R_{G-on}} \cdot k_{U_{CE-on}} \cdot k_{on}^{rec}, \tag{3.2.21}$$

$$E_{off} = \left(A_{off} \cdot I_{C(2)} + B_{off}\right) \cdot k_{R_{G-off}} \cdot k_{U_{CE-off}}. \tag{3.2.22}$$

c) For the waveform shown in Figure 3.14c

$$E_{on} = 0, \tag{3.2.23}$$

$$E_{off} = \left(A_{off} \cdot I_C + B_{off}\right) \cdot k_{R_{G-off}} \cdot k_{U_{CE-off}}. \tag{3.2.24}$$

The data available to calculate the reverse recovery losses of the diode differs from one manufacturer to another. Furthermore, these losses depend on the current slope during the transition which in standard voltage source inverters (VSIs) is basically determined by the inductance of the circuit, IGBT *di/dt* during turn-on and operation temperature [80]. If the reverse-recovery energy in the datasheet is provided only for one operating point, then the scale factor k_{rec} can be calculated according to [68]:

$$k_{rec} = \frac{E_{rec}^{DS}}{Q_{rec}^{DS} \cdot U_{CE}^{DS}}, \tag{3.2.25}$$

where E_{rec}^{DS}, Q_{rec}^{DS} and U_{CE}^{DS} are reverse-recovery energy, reverse-recovery charge and voltage specified in the datasheet, correspondingly.

The reverse-recovery energy can now be approximated as

$$E_{rec} = k_{rec} \cdot Q_{rec}^{US} \cdot U_{CE}^{US} = k_{rec} \cdot \frac{I_{rec} \cdot t_{rec}}{2} \cdot U_{CE}^{US}. \tag{3.2.26}$$

The drawback of the above presented equations is generally related to the limited accuracy of the linearly interpolated characteristics of $U_{CE}=f(I_C)$, $E_{on}=f(I_C)$ and $E_{off}=f(I_C)$. A better result, especially at lower currents, can be achieved by approximating these curves with the following function:

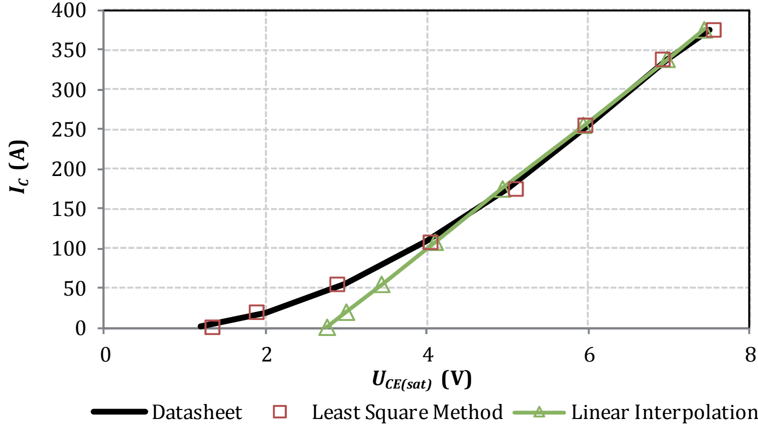


Figure 3.16 Comparison of the collector-emitter saturation voltage with the collector current using different interpolation methods

$$f(x) = A \cdot x^3 + B \cdot x^2 + C \cdot x + F. \tag{3.2.27}$$

The coefficients A, B, C and F of the proposed function can be estimated from the datasheet curves using the least square fitting method. The comparison of results obtained with different interpolation methods is shown in Figure 3.16.

The conduction losses can then be expressed as

$$P_{cond} = \frac{1}{T_{sw}} \cdot \int_{0}^{t_{on}} i_C(t) \cdot u_{CE(sat)}(i_C(t)) \cdot dt \,, \tag{3.2.28}$$

where $i(t)$ could be expressed according to Equations 3.2.6, 3.2.8 or 3.2.10.

Analytical loss estimation method of a two-level half-bridge inverter

The proposed approximation of the transistor switching process is shown in Figure 3.17. The turn-on energy is calculated by integrating the multiplied turn-on voltage and the current ramp. As the current changes slower than the voltage at the turn-on, the power loss equation is divided into two parts. In the first part both the voltage and current are changing, in the second part only the current changes. This energy is multiplied by the switching frequency f_{sw}. The result of this equation is the IGBT turn-on power loss

$$P_{on} = f_{sw} \cdot \left[\int_{t_{on1}}^{t_{on2}} u_{CE(on)}(t) \cdot i_{C(on)}(t) dt + \int_{t_{on2}}^{t_{on3}} u_{CE(sat)}(i_C) \cdot i_{C(on)}(t) dt \right], \tag{3.2.29}$$

where t_{on1} to t_{on3} is the total IGBT turn-on time; t_{on1} to t_{on2} is the IGBT collector-emitter voltage fall time from operation to saturation level, and t_{on1} to t_{on3} is the IGBT collector current rise time. $u_{CE(on)}(t)$ is the IGBT collector-emitter voltage at turn-on and $i_{C(on)}(t)$ is the collector current function during the turn-on of the

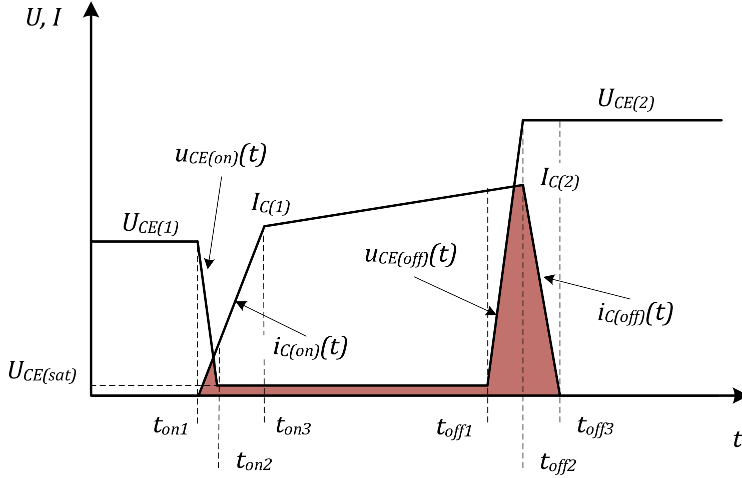


Figure 3.17 Generalised IGBT waveforms in the two-level half-bridge voltage-source inverter

IGBT. To simplify the calculations, voltage and current waveforms can be replaced by the linear functions:

$$u_{CE(on)}(t) = U_{CE(1)} - \frac{(t - t_{on1}) \cdot \left(U_{CE(1)} - U_{CE(sat)}\right)}{t_{on2} - t_{on1}}, \tag{3.2.30}$$

$$i_{C(on)}(t) = \frac{(t - t_{on1}) \cdot I_{C(1)}}{t_{on3} - t_{on1}}. \tag{3.2.31}$$

Transistor turn-off losses could be calculated assuming that the current through the IGBT stays close to $I_{C(2)}$ during the interval t_{off1}-t_{off2} and the voltage across the IGBT is close to $U_{CE(2)}$ during the interval t_{off2}-t_{off3}. The turn-off energy loss can then be approximated by

$$P_{off} = f_{sw} \cdot \frac{U_{CE(2)} \cdot I_{C(2)} \cdot (t_{off3} - t_{off1})}{2}. \tag{3.2.32}$$

The energy stored in the circuit lost during the oscillations after the IGBT turn-off is

$$E_{osc} = \frac{1}{2} \cdot L_E \cdot I_{osc}^2, \tag{3.2.33}$$

where, I_{osc} is the peak value of the oscillating current.

Estimation of power losses in the experimental converter

Using the analytical approach (Equations 3.2.25-3.2.33) and the experimental waveforms of the converter prototype, the losses for one switching period are estimated (Table 3.5). In the investigated modes of operation the conduction losses of the freewheeling diodes are negligible and not included in the analysis.

Table 3.5 Results of the analytical loss calculation (U_{in}=3.2 kV, P_{out}=30 kW)

Energy losses	Symbol	Value (mJ)	
		Analytical	Datasheet
Turn-on	E_{on}	5	77
Turn-off	E_{off}	254	177
Reverse-recovery	E_{rec}	17	43
Conduction	E_{cond}	10	
Oscillation	E_{osc}	9	
Total	E_{tot}	295	316

3.3 Switching frequency and power density limits

Semiconductor losses are a central evaluation criterion due to the direct correlation with virtually all other electrical parameters of the converter. The losses of high-voltage IGBTs are one of the limiting factors during power converter design with such devices. It finally leads to more powerful and complicated cooling systems to be implemented to ensure the proper junction temperature of semiconductors or limiting of the f_{sw}. Both of these measures result in a negative impact on power density. From the designer's point of view any improvements in the switching frequency lead to the minimisation of passive components, like filter capacitors and inductors as well as isolation transformers. The most critical passive components in the developed two-level half-bridge converter are the input capacitors (C_1 and C_2) and the isolation transformer *TX*.

Evaluation of the passive components

The input capacitors have to withstand high voltage and current ripple. In the current design they occupy around 25% of the total converter volume, which can change proportionally to the switching frequency. The minimum capacitance required for the input capacitors C_1 and C_2 for different voltage

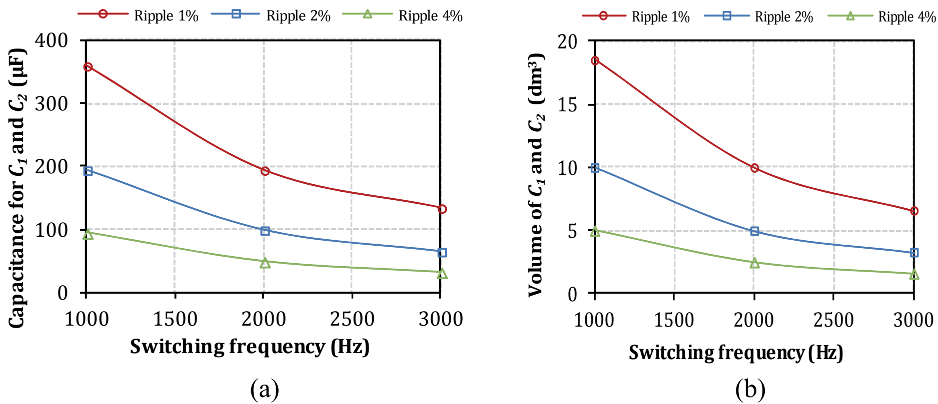


Figure 3.18 Capacitance requirements (a) and capacitor volumes (b) vs. operating frequency for different voltage ripple factors (high-voltage capacitor with organic film dielectric ELCOD K-75-80-4kV-100µF)

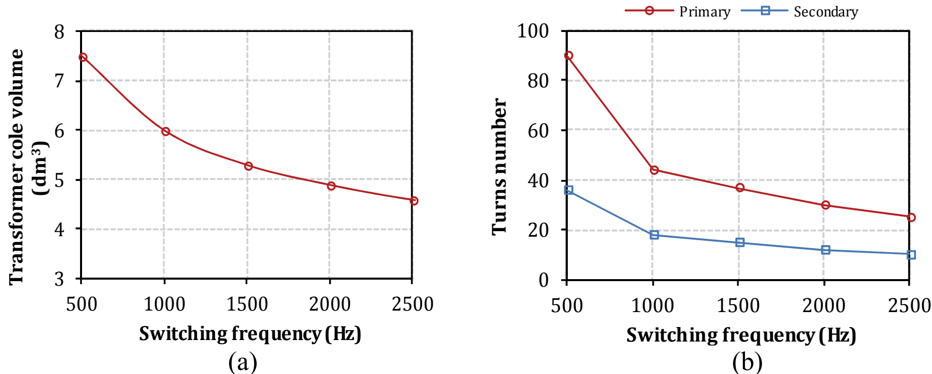


Figure 3.19 Minimum required core volume (a) and turns number (b) vs. operating frequency for the 50 kVA isolation transformer with the GM14DC toroidal magnetic core

ripple factors is shown in Figure 3.18a [82]. With the increased switching frequency, the required capacitance value is decreasing exponentially. For example, by increasing the operation frequency from 1 kHz to 2 kHz, the size and volume of input capacitors could be reduced by approximately 50% (Figure 3.18b). Similar power density improvements could be achieved for the output filter components as well [83]. High-frequency isolation transformer *TX* is another bulky component in converters with such power range. The transformer core volume should be selected to meet the power requirements and temperature rise for the selected operating frequency. For instance, by doubling the switching frequency (from 1 kHz to 2 kHz), the magnetic core volume could be effectively reduced by 18% (Figure 3.19a). At the same time, the number of turns in the primary winding is reduced by 14 and by 6 in the secondary (Figure 3.19b). This gives an additional benefit in terms of smaller power dissipation of the isolation transformer [84].

Evaluation of switching performance of different 6.5 kV IGBTs

Despite allowing simpler topologies with a smaller number of elements to be implemented, the 6.5 kV modules generally have inferior performance characteristics than lower voltage class transistors. This results in higher power losses, leading to increased requirements to passive components and the thermal management system of the converter. Thus, it is essential to compare available 6.5 kV IGBT modules in terms of switching performance and overall feasibility to investigate different possible relations of converter parameters. This section is based on the principle of the analysis discussed in [PAPER-III] .

In terms of total power losses, the most demanding operating point of the developed converter is at maximum input voltage $U_{in(max)}$=4 kV at minimum duty cycle D_{min}=0.22 [66]. The following analysis will focus on the estimation of switching frequency limits of different 6.5 kV IGBT modules, operating at this operating point. The maximum module power dissipation was calculated assuming that modules are operating in a two-level half-bridge inverter, sharing

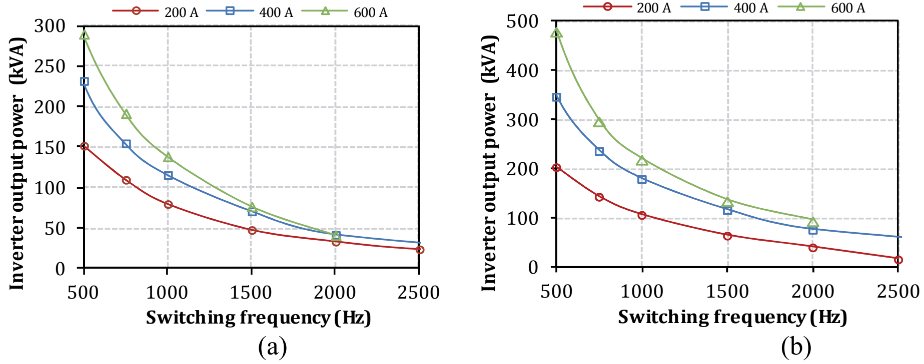


Figure 3.20 Side-by-side comparison of switching frequency limits of different investigated Infineon 6.5 kV IGBT modules (T_j=125°C, T_{amb}=60°C) for air cooling (a) and liquid cooling (b)

Table 3.6 Conditions for the performance estimation

Parameter	Symbol	Value
Maximum junction temperature, °C	T_j	125
Ambient temperature, °C	T_{amb}	60
Thermal resistance heatsink-to-ambient (forced air cooling), °C/W	R_{thsa}	0.013
Thermal resistance heatsink-to-ambient (liquid cooling), °C/W		0.005
Input voltage, kV	$U_{in(max)}$	4.0
Duty cycle	D_{min}	0.22

Table 3.7 Typical values of different investigated IGBTs (T_j=125 °C)

IGBT type	Conditions	E_{on} (J)	E_{off} (J)	E_{rec} (J)	$U_{CE(sat)}$ (V)	IGBT power loss limit (W)	
						Forced air cooling	Liquid cooling
FZ200R65KF1	I_C=200 A	1.90	1.20	0.55	5.3	870	1100
FZ400R65KF1	I_C=400 A	4.00	2.30	1.05	5.3	1275	1850
FZ600R65KF1	I_C=600 A	5.90	3.50	1.60	5.3	1510	2410
FZ600R65KE3	I_C=600 A	5.20	3.40	2.40	3.7	1545	2470

a common heatsink with the conditions listed in Table 3.6. To provide a better comparability, the datasheet values of high-voltage IGBTs from one vendor (Infineon) are compared. Since the developed converter is based on the first generation NPT IGBTs (FZ200R65KF1), the devices from the same product line were taken for the comparison (KF1-series). Further, the characteristics of the first generation modules will be compared to those of the third generation (KE3-series) using the example of the 600 A devices. The analysed IGBTs are listed in Table 3.7.

In practice, the switching frequency limit $f_{sw(max)}$ of the IGBT is mostly determined by the thermal management system of the IGBT module.

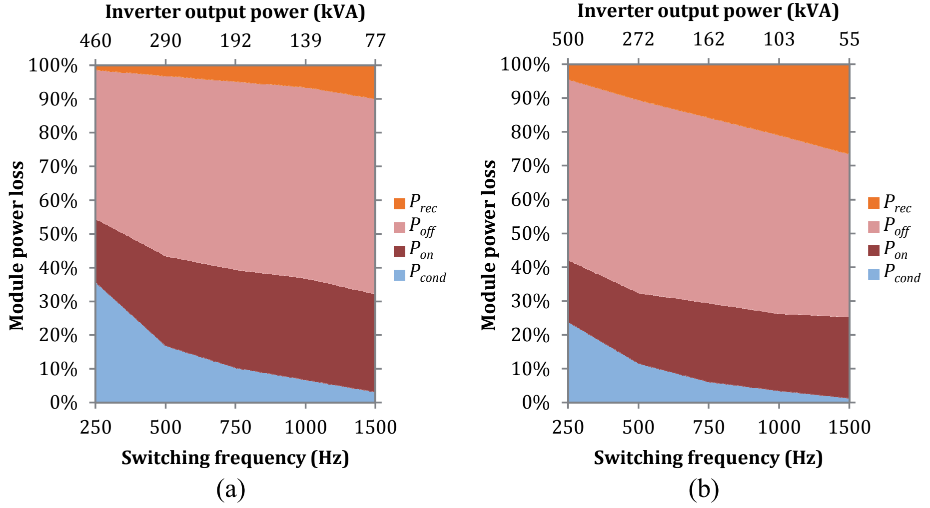


Figure 3.21 Breakdown of maximum power losses vs. frequency in Infineon 600 A 6.5 kV IGBT modules (T_j=125°C, T_{amb}=60°C): KF1-series (a) and KE3-series (b)

The thermal limit to frequency is derived by [85]

$$f_{sw(max)} = \frac{P_{tot} - P_{cond}}{E_{on} + E_{off}}, \tag{3.3.1}$$

Further analysis will estimate practical switching frequency limits, which can be achieved by each KF1-series IGBTs in the hard switching mode with the conditions listed in Table 3.6 and 3.7. The approximate values are calculated using datasheet values of devices and one-dimensional thermal models. The influence of parasitic circuit inductance on the distribution between the turn-on and the turn-off loss is not considered. Comparison of the switching frequency limits presented in Figure 3.20 shows that with forced air cooling a noticeable output power increase using higher current rated devices could be achieved at frequencies below 2 kHz. The performance estimation for higher frequencies is complicated due to insufficient datasheet information provided for operation with currents much lower than nominal. The implementation of liquid cooling allows increasing the maximum output power by at least 30%.

The comparison of power losses of the first generation modules with those of the third generation shown in Figure 3.21 reveals that the third generation modules show superior switching performance only at frequencies below 0.5 kHz. This is the result of the design trade-offs that led to much higher SOA (for both IGBTs and diodes) and increased overall robustness.

3.4 Generalisations

High stray inductance of the isolation transformer results in higher losses as well as voltage and current oscillations after turn-off. Although the frequency of those oscillations is not high to generate radiated EMI, it can cause some

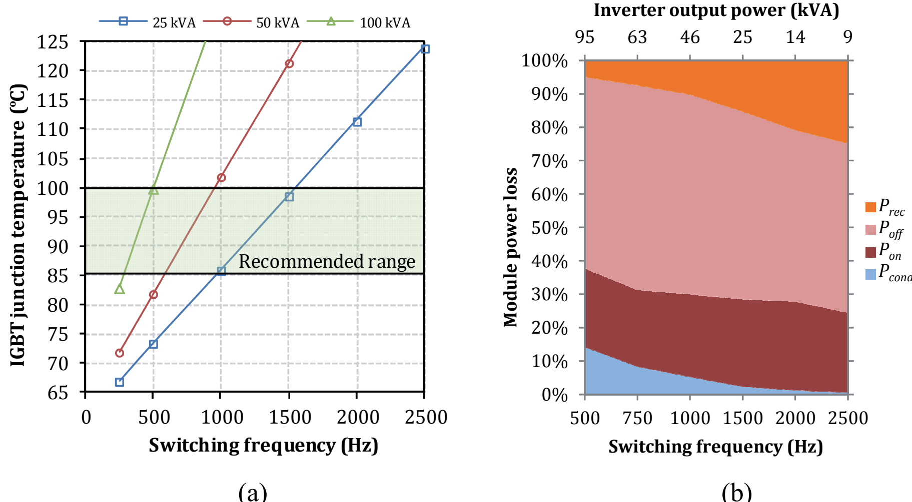


Figure 3.22 Junction temperatures vs. switching frequency at different output power levels (a) and breakdown of power losses (b) of 200 A module, operating with maximum recommended junction temperature of 100 ℃

problems with conducted EMI in the contact line. Due to the required high isolation voltage of the isolation transformer, the high stray inductance is hard to avoid, moreover, the capacitance of HV IGBT modules cannot be avoided. In the case of the considered high-voltage inverter, these parasitic effects are not dangerous to HV IGBT modules, neither are they dangerous to other circuit elements since they do not create noticeable overvoltages.

Using the proposed analytical loss estimation method it is possible to estimate the contribution of the turn-on or the turn-off losses in the total switching losses, which could be beneficial in estimating the feasibility of implementation of different loss reduction methods in semiconductors. The following peculiarities of power loss estimation in two-level half-bridge DC/DC converters could be allocated:

- The IGBT turns on without the effect of the reverse recovery circuit of a commutating diode adding to the IGBT turn-on loss, resulting in lower losses.
- The voltage prior to the turn-on of the IGBT is equal to $U_{in}/2$, assuming that the oscillation process is finished during the freewheeling state.
- The IGBT turn-on energy loss decreases while the turn-off energy loss increases with the stray inductance. Both effects almost compensate each other.
- Power loss estimation with the least square interpolated datasheet curves could offer a more accurate result, especially at lower currents.

Good design practice with considerations of reliability and the worst-case maximum junction temperature is to limit the steady state junction temperature to 70%-80% of the maximum allowable or less [86]. Lower operation temperatures increase long-term reliability of semiconductors. Considering the

maximum junction temperature of 125ºC, the maximum recommended operation junction temperature ranges between 85 and 100ºC (Figure 3.22a). It should be noticed that the values presented are calculated without taking into account the influence of the junction temperature on semiconductor losses. By selecting the operating junction temperature of 100ºC, the maximum allowable 200 A module power loss is reduced by 40%, which leads to a corresponding decrease in the achievable output power of the inverter. On the example of 200 A module it can be seen that at 1 kHz switching frequency the achievable inverter output power is reduced from 75 kVA (Figure 3.20a) to 46 kVA (Figure 3.22b), assuming that all the remaining conditions are the same.

The achievable switching frequency is in direct correlation with the maximum allowable module power dissipation. Higher current rated devices with higher baseplate area have superior heat transfer characteristics and allow higher frequencies of operation. An additional/alternative way to achieve higher switching frequencies is to implement a liquid cooling system. For the modules used in the developed converter prototype, the maximum recommended switching frequency is approximately 1 kHz assuming the worst case operating conditions: maximum input voltage, maximum output power and highest ambient temperature. The volumes of input capacitors and transformer core can decrease proportionally to the switching frequency. Additional modifications to the topology are necessary to reduce losses in semiconductor elements and improve the switching frequency.

4 METHODS FOR IMPROVEMENT OF HV IGBT BASED TWO-LEVEL HARD-SWITCHED DC/DC CONVERTERS

Main problems of the topology described in the previous chapter are high power losses in semiconductors due to hard switching and consequently, limited switching frequency because of thermal issues. This imposes increased requirements on passive components of the converter and its cooling system, leading to increased price and reduced power density. The oscillations after transistor turn-off related to the common disadvantage of hard-switched half-bridge topologies can cause some problems with conducted EMI in the contact line. Several ways exist of how to improve the switching process of semiconductor switches in the HB inverters, including application of dissipative snubbers or using resonant, asymmetrical and auxiliary switch topologies [87]. However, due to wide variations of input voltage and output power in some applications (e.g. rolling stock), not all solutions are feasible since they could limit the main features of the HV IGBT-based converter. For example, the asymmetric control method is sometimes used as one of the ways to utilise the leakage inductance. The duty cycles of the switches are not equal in this case and due to the very short freewheeling state (both main switches are turned off), the zero voltage switching (ZVS) of both of the switches can be achieved. However, an asymmetric half-bridge converter has the asymmetric stress distribution in the components and a DC bias in the transformer. Therefore, it is generally not suitable for applications with a wide input voltage range. Moreover, the input-output relationship of the asymmetric-controlled half-bridge converter is nonlinear, resulting in a lower duty cycle at high input voltages compared to the symmetric-controlled half-bridge converter, which results in degrading the converter performance [88].

The main focus in this chapter is on the study and comparison of different methods for improvement of the HV IGBT-based two-level hard-switched DC/DC converters in order to suppress the oscillations and improve the switching performance of the IGBT modules without increasing its complexity or reducing reliability and efficiency significantly.

4.1 Passive snubbers and active auxiliary circuits

Passive snubbers

The snubber circuit is an additional part to the basic converter, which is used to reduce the stresses on electrical components. Usually, in a power semiconductor device, snubbers may be used singly or in combination depending on the requirements. The complexity and the cost added to the converter circuit by the presence of the snubber must balance against the benefits of limiting the stresses on critical circuit components [3] [PAPER-IV]. There are three broad classes of passive snubber circuits:

- unpolarised *RC* snubbers,
- polarised *RC* snubbers,
- polarised *LR* snubbers.

Unlike thyristor based converters, the HV IGBT based two-level hard-switched DC/DC converter does not require any additional *di/dt* control. Therefore, there is no actual need for limiting *di/dt* with *LR* snubbers. On the other hand, after turn-off the parasitic oscillations could be damped using *RC* snubbers (Figure 4.1a). These passive snubbers are typically placed across semiconductor devices and dissipate the energy stored in the circuit during the active state. The lowest value of peak voltage is proportional to the size of C_s. A larger C_s should be used if a lower peak voltage is required. This means that the power dissipation increases as the peak voltage is reduced [89].

The polarised *RC* snubbers, also referred to as *RCD* snubbers (Figure 4.1b), are applicable to either rate of rise control or clamping. At turn-off, the snubber will carry most of the switch current and transfer power dissipation into the

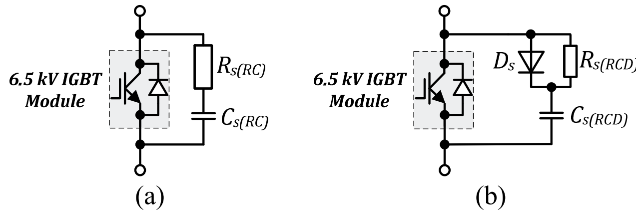


Figure 4.1 RC (a) and RCD (b) snubbers connected across the IGBT module

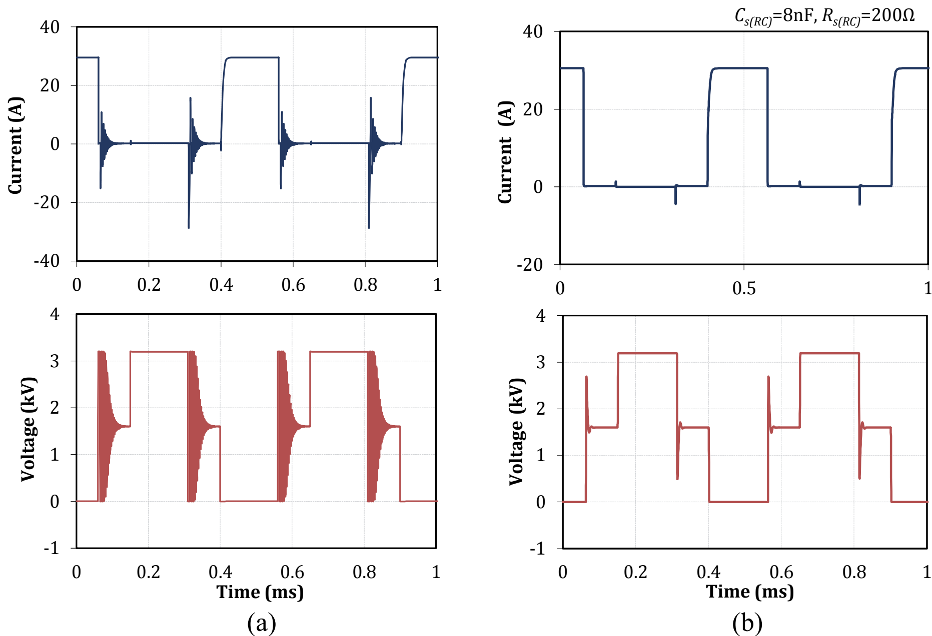


Figure 4.2 TT IGBT Module voltage and current simulated in PSpice without a snubber (a) and with an RC snubber (b) (U_{in}=3.2 kV; f_{sw}=2 kHz, D=0.32; 30 kW load)

snubber, increasing the reliability of the switch. The main disadvantage of the *RCD* snubber is in the following: since there is a diode in parallel to the resistor the effective value of $R_{s(RCD)}$ during the charging of $C_{s(RCD)}$ is close to zero, the voltage across the switch for a given $C_{s(RCD)}$ will be higher than the corresponding value using an *RC* snubber. Moreover, during the switch turn-on a capacitive discharge current occurs, increasing turn-on losses. Therefore when using an *RCD* snubber in the half-bridge inverters, the turn-on snubber should be included as well [3].

The *RC* snubber capacitance can be estimated by

$$C_{s(RC)} = L_E \cdot \left(\frac{I_{rec}}{U_{in}} \right)^2 . \tag{4.1.1}$$

The snubber resistance is then approximated by

$$R_{s(RC)} = \frac{U_{in}}{I_{rec}}. \tag{4.1.2}$$

Finally, the power dissipation in the snubber resistor in the case of the HB (two voltage transitions per cycle) converter is estimated by [90]

$$P_{s(RC)} = C_{s(RC)} \cdot U_{in}{}^2 \cdot f_{sw} . \tag{4.1.3}$$

With a smaller snubber capacitor, the freewheeling diodes of the main switches conduct to partly recycle the energy while part of the energy is dissipated in the snubber resistor. For a larger snubber capacitor, the energy in the leakage inductance may be fully dissipated in the snubber without recycling through freewheeling diodes. The simulated waveforms of the converter operating with unpolarised *RC* snubbers are shown in Figure 4.2.

Since the transformer leakage energy is being dissipated in the passive snubber circuits, the overall efficiency of the converter may be reduced. Alternative methods to eliminate the oscillations and utilise the leakage inductance in order to improve the efficiency should be evaluated.

Active clamping

An active clamping method proposed in [91] uses an auxiliary circuit where the leakage energy is circulating during the freewheeling state. Prior to the main switch turn-on, the auxiliary circuit energy is released. The freewheeling diodes of the main switches conduct, creating the ZVS condition. However, there are several drawbacks. Firstly, the leakage inductance should be large enough for the freewheeling current to maintain, especially at low duty cycles. Secondly, there is high conduction loss in the auxiliary switches. To overcome disadvantages of the active-clamp snubber (ACS) a modified method is introduced in [88] (Figure 4.3). Instead of circulating, the transformer leakage energy is transferred to the auxiliary capacitor, which also blocks the DC component, avoiding saturation of the transformer. Since the energy transfer

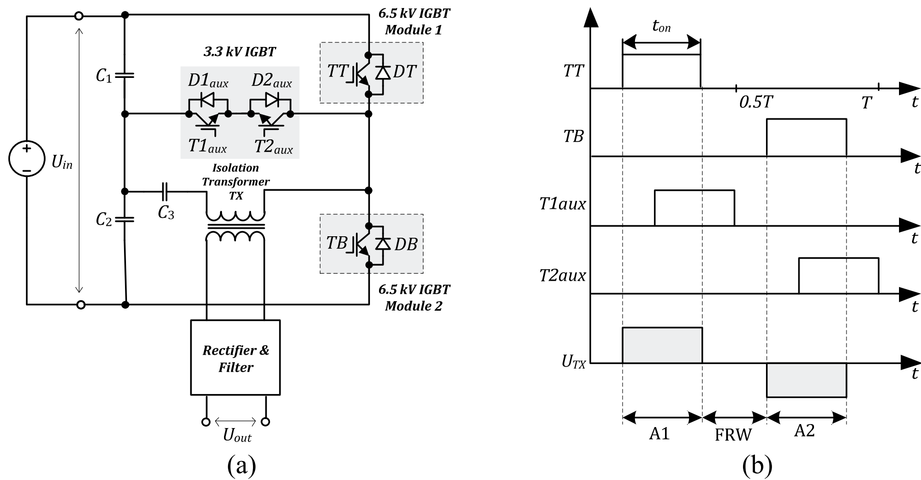


Figure 4.3 Half-bridge DC/DC converter with active-clamp snubber circuit and auxiliary capacitor (a) and its generalised operation principle (b)

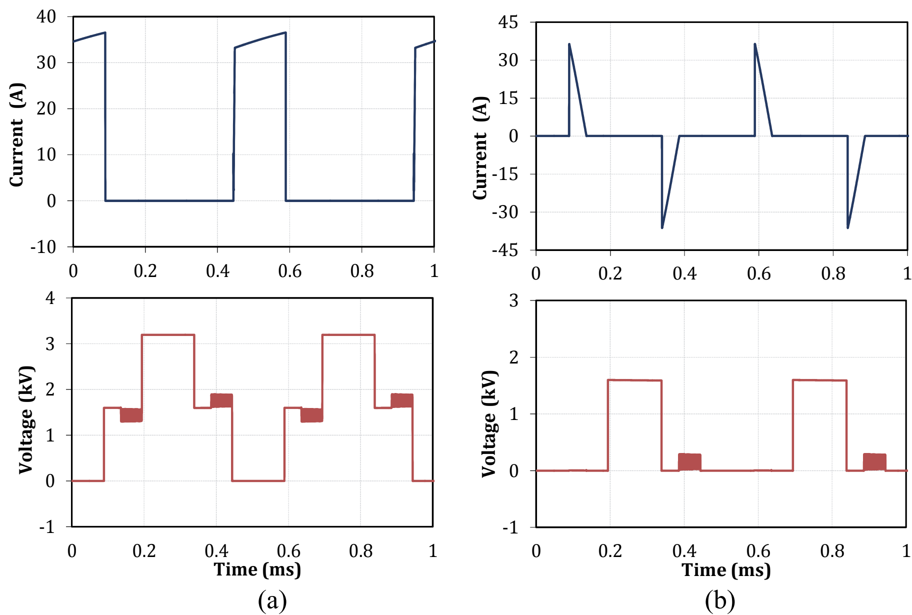


Figure 4.4 Simulated collector-emitter voltage and collector current waveforms of the TT IGBT Module (a); $T1_{aux}$ and $D1_{aux}$ (b) (U_{in}=3.2 kV; f_{sw}=2 kHz, 30 kW load)

accounts for a small part of the switching period, the conduction energy loss of the auxiliary switches is minimised. The primary switches are still hard switched; however, the voltage stress is reduced to $U_{in}/2$ during the turn-off transient, leading to reduced losses. The freewheeling diodes of the main switches never conduct and the auxiliary switches $T1_{aux}$ and $T2_{aux}$ turn on with ZVS and turn off with ZCS (zero current switching). The energy transfer period to the capacitor is estimated by [88]

$$t_{tr} = \frac{2 \cdot C_3 \cdot L_E}{t_{on}}. \tag{4.1.4}$$

The simulation waveforms are presented in Figure 4.4. Minor oscillations caused by the voltage across C_3 could be observed, however, since this voltage is much smaller than U_{in} , the ringing is almost negligible.

The ACS topology described requires two additional switches with half of the voltage rating and two additional PWM channels in comparison to the reference HB topology. In the case of the studied topology, two additional 3.3 kV switches and an associated control system are required, affecting the converter price.

4.2 Multilevel topologies

As an alternative to two-level topologies based on semiconductors with high voltage blocking capability, multilevel topologies with lower voltage devices having increased switching performance could be implemented. Lately, the three-level neutral-point-clamped (3L-NPC) topology became popular in high-voltage, medium- and high-power applications. In terms of achievable voltage blocking capability the 3L-NPC topology with 3.3 kV IGBT modules could replace previously investigated solution based on 6.5 kV semiconductors. The current chapter will investigate the feasibility of application of multilevel converters on the example of the 3L-NPC topology.

The three-level phase leg in the NPC topology consists of four IGBTs with their associated FWDs, arranged in series, and two additional diodes – *Dcl1* and *Dcl2* – connecting intermediate nodes to the neutral point of the DC-link. All power semiconductors used have the same blocking voltage. The inverter schematic shown in Figure 4.5 is based on two dual 200 A 3.3 kV Infineon

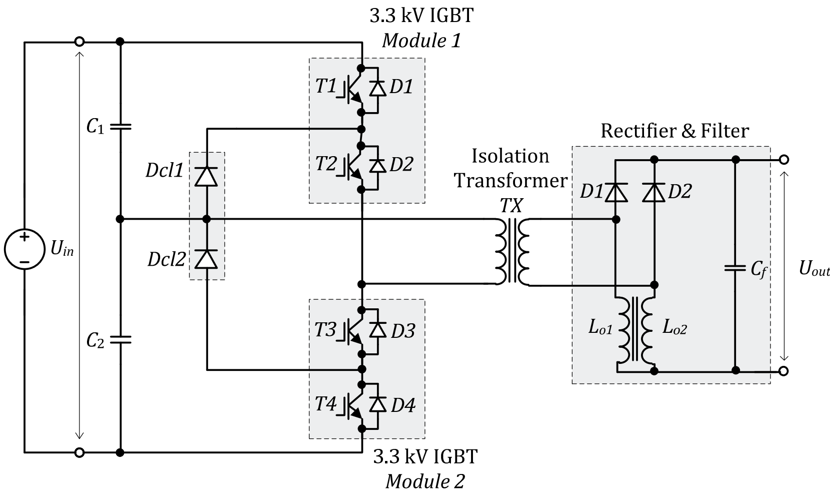


Figure 4.5 Simplified schematic of the developed 3L-NPC converter

4.1 Components of the 3L-NPC converter prototype

Component	Symbol	Type	Value
Input capacitors	C_1, C_2	ELCOD K-75-80g-4000	100 µF
Inverter switches	*Module 1, Module 2*	FF200R33KF2C	200 A/3.3 kV
Transformer	*TX*	High frequency toroidal transformer with soft nanocrystalline core material GM14DC	30/24
Clamping diodes	*Dcl1, Dcl2*	Dual FRED modules IXYS DH2x61-18A (2 diodes in series)	2x60 A / 1.8 kV
Rectifier diodes	*D1, D2*	Dual FRED modules IXYS DSEI2x101-12A (2 diodes in parallel)	2x100 A / 1.2 kV
Output inductor	L_{o1}, L_{o1}	Laminated steel core inductor	2.5 mH
Filter capacitor	C_f	Electrolytic capacitor	180 µF

IGBT modules. Since these dual modules are available in packages with the standard 73×140 mm baseplate areas, the required installation area requirements remain similar to the two-level topology based on two 6.5 kV IGBTs. The current doubler rectifier (CDR) reduces the power losses in rectifier diodes and allows reducing the volume of CDR inductor cores by 50 % [92]. The components used in the converter prototype are listed in Table 4.1

Control algorithm

Three-level DC/DC inverters enable an alternative PWM strategy to be implemented, allowing the inner switches *T2* and *T3* to operate under ZVS conditions without addition of any additional hardware components. There are three main commutation states: positive (Pos) zero (O) and negative (Neg) and the output voltage can take three different levels ($+U_{in}/2$; 0; $-U_{in}/2$) and the voltage stress of each switching device is limited to $U_{in}/2$.

Ideally, the four switching devices are turned in pairs. *T1* and *T4* are main switching devices and *T2* and *T3* are the auxiliary switching devices to clamp the output voltage to the neutral point potential, together with *Dcl1* and *Dcl2*. When the top two switches *T1* and *T2* are on, the output voltage is $+U_{in}/2$ and when the bottom two switches *T3* and *T4* are on, the output voltage is $-U_{in}/2$. If both outer switches *T1*, *T4* are off, the output voltage is zero (Table 4.2).

Two additional channels can be derived by inverting the main PWM channels. Thus, the microcontroller only generates two 180º phase shifted PWM signals (PWM1 and PWM4). PWM2 is derived by inverting PWM4 and similarly PWM3 is derived by inverting PWM1. Each PWM signal controls an individual switch, as shown in Figure 4.6. Since the IGBTs have a certain turn-on and turn-off delay time, a situation can occur where three devices *T1*, *T2*, *T3* or *T2*, *T3*, *T4* are simultaneously conducting. Having three devices conducting at the same time would result in the short circuit of the corresponding input

Table 4.2 Switching states of a 3L-NPC inverter

Switching state	**Switching conditions**				**Output voltage**
	T1	***T2***	***T3***	***T4***	
Pos	ON	ON	OFF	OFF	$+U_{in}/2$
O	OFF	ON	OFF	OFF	0
	OFF	ON	ON	OFF	
	OFF	OFF	ON	OFF	
Neg	OFF	OFF	ON	ON	$-U_{in}/2$

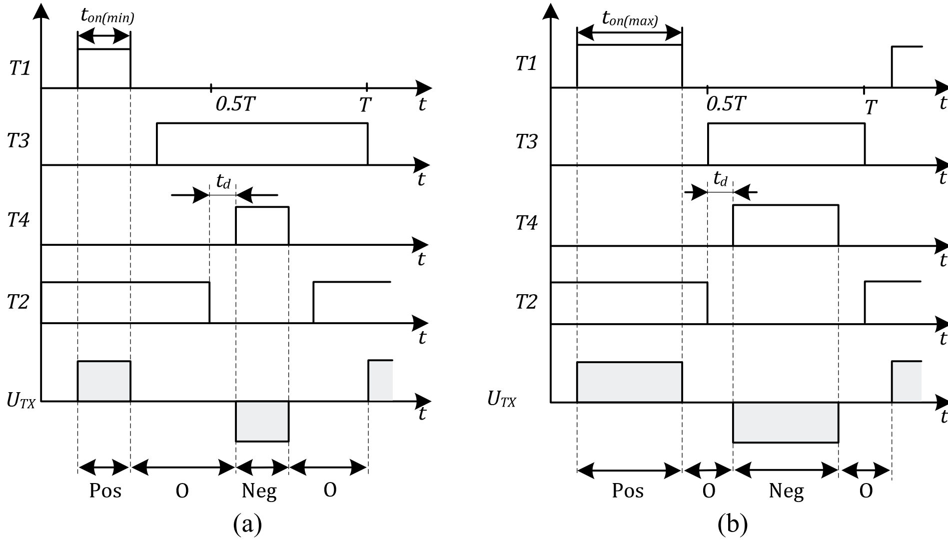


Figure 4.6 Operation principle of a 3L-NPC half-bridge DC/DC converter at maximal (a) and minimal (b) input voltages

capacitor C_1 or C_2 and the IGBTs would be destroyed. In order to prevent short circuit it is necessary to add a dead time t_d between the original and the inverted PWM signal. The minimal dead time requirement is determined by the turn-off and turn-on delay times of the corresponding transistors and the control signal propagation delay from the control system to the power transistor.

Analysis of switching transients

During the laboratory tests the inverter prototype was operating with the minimum input voltage. Dead time existence together with capacitance and inductance in the circuit complicate commutation processes in the topology. Once again, based on the parameters, most influential to different switching states, the corresponding simplified equivalent circuits of the converter were elaborated. Experimental waveforms of three-level VSI operating with ZVS of the inner switches are presented (Figure 4.7). In accordance with time intervals shown in Figure 4.7, the transient processes during a half period could be described as follows [65]:

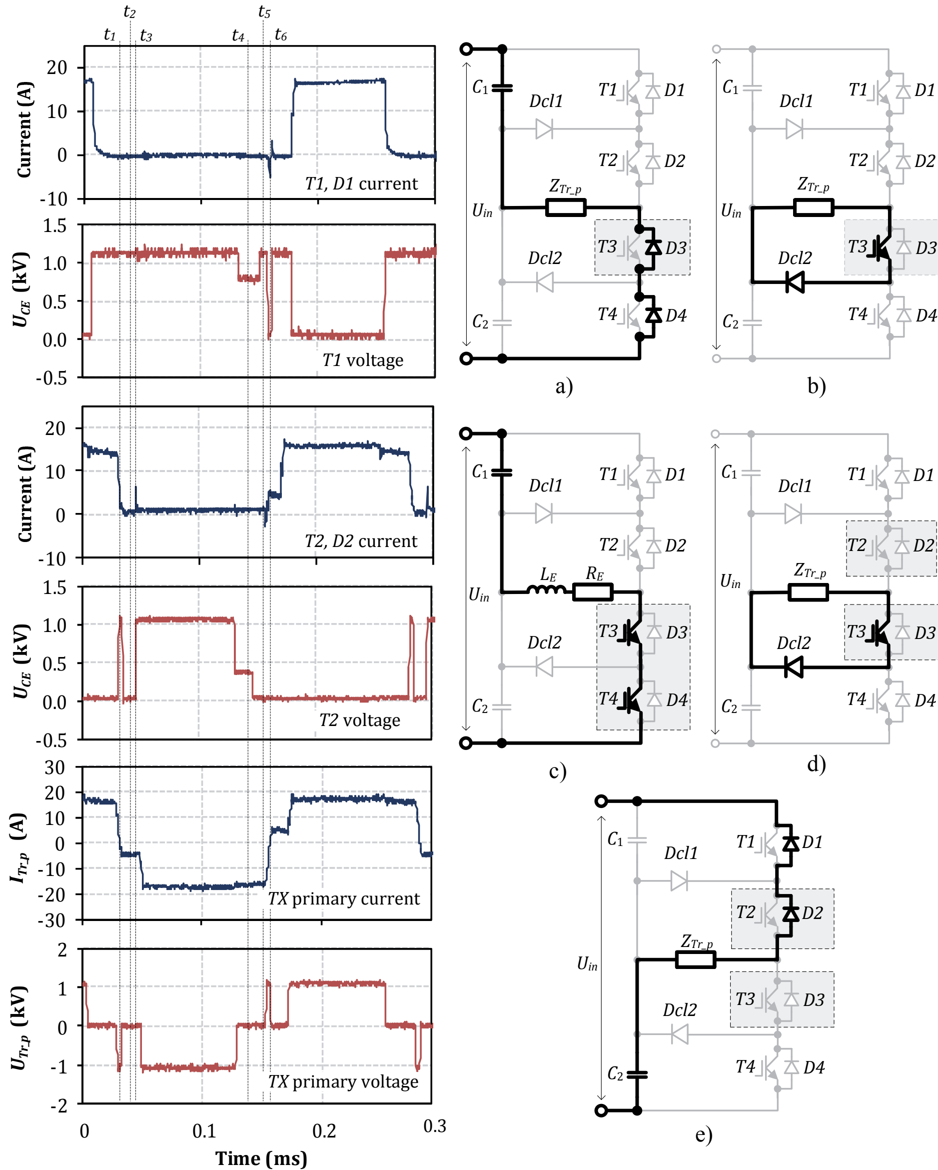


Figure 4.7 Experimental waveforms and analysis of switching states of a 3L-NPC inverter (U_{in}=2.2 kV, D=0.4, P_{out}=15 kW, f_{sw}=4 kHz, t_d=20 μs)

t_1 – The inner transistor *T2* is turned off. The stray inductance draws the current through freewheeling diodes *D3* and *D4* (Figure 4.7a). Maximal voltage is applied across transistors *T1* and *T2*. A voltage peak occurs on the transistor *T2*. The pulse width of the peak depends on the stray inductance value. Voltage across T4 drops to zero and a negative voltage impulse occurs on the transformer primary.

t_2 – After the energy stored in the load inductance has been utilised, the current stored in parasitic circuit elements starts to flow through *Dcl2*, *T3* and the load until the end of the dead time. The voltage across *T1* and *T4* is maximal; the voltage across *T2* and *T3* and the load is close to zero (Figure 4.7b).

t_3 – The outer transistor *T4* is turned on. Both bottom side transistors are conducting. Current spike caused by recharging of output capacitance of *T2* appears across *Dcl1* and *T2*. Maximal voltage is applied across top side transistors and negative voltage is applied to the load (Figure 4.7c).

t_4 – The outer transistor *T4* is turned off. The stray inductance draws the current through clamping diode *Dcl2* and *T3* (Figure 4.7d). Instead of maximal voltage now only half of the value is applied on the top side transistors. The load voltage drops to zero and the current decreases, being damped by circuit active resistance.

t_5 – After the dead time *T2* is turned on and the voltage drops to zero. The voltage across *T1* increases to maximal.

t_6 – The inner transistor *T3* is turned off. The stray inductance draws the current through freewheeling diodes *D1* and *D2* (Figure 4.7e). Maximal voltage is applied across transistors *T3* and *T4*. A voltage peak occurs on the transistor *T3*, the voltage across *T1* drops to zero and a positive voltage impulse occurs on the transformer primary.

Analysis of power losses

The power losses of the 3L-NPC inverter are estimated at the most demanding operating point: input voltage $U_{in(max)}$=4 kV and duty cycle D_{min}=0.22 [66]. The following analysis will focus on the definition of switching frequency limits of 3.3 kV IGBT modules, operating at this operating point. The

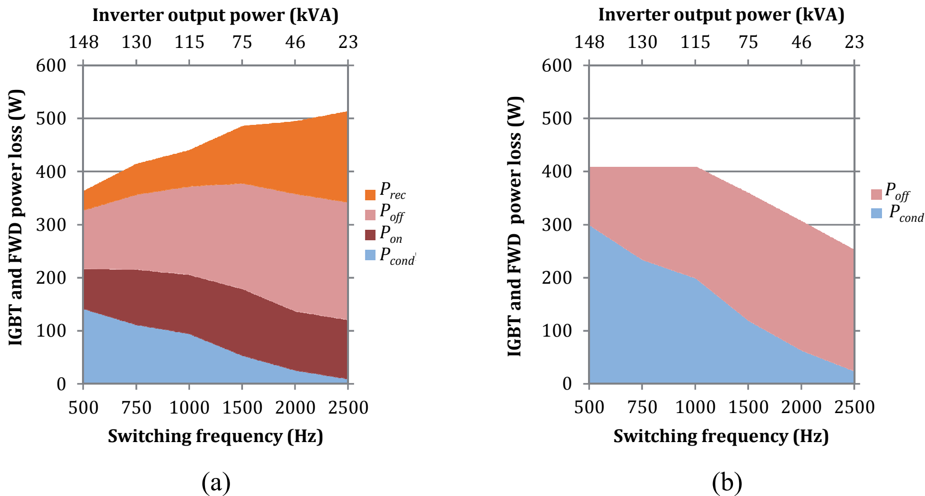


Figure 4.8 Breakdown of maximum power losses vs. frequency in Infineon 200 A 3.3 kV IGBT modules (T_j=125°C, T_{amb}=60°C): outer switches (a) and inner switches (b)

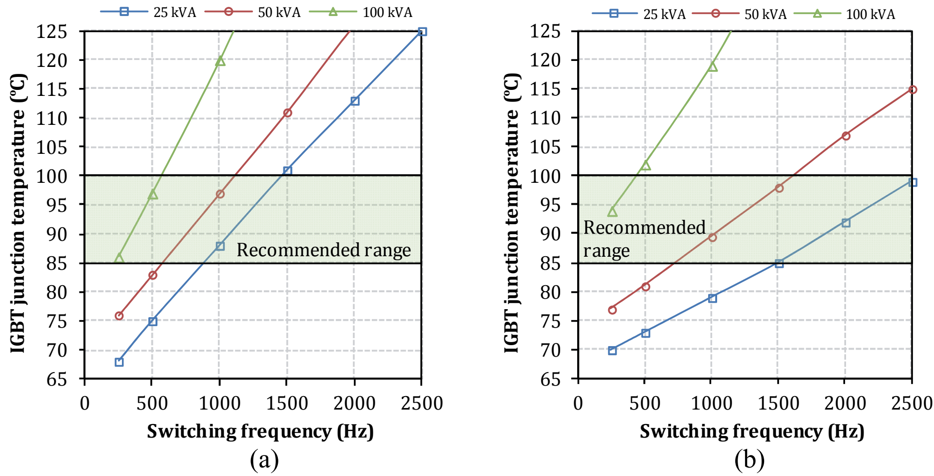


Figure 4.9 Junction temperature vs. switching frequency at different output power levels: outer switches (a) and inner switches (b) of Infineon 200 A 3.3 kV IGBT modules

maximum module power dissipation was calculated assuming that two dual FF200R33KF2C modules are operating in the 3L-NPC converter, sharing a common heatsink with the same conditions as for a two-level inverter (Table 3.6).

As it could be observed from Figure 4.8, the inner and outer switches have unequal loss distribution. Inner switches have the losses concentrated only in the IGBT chips, while the losses of outer switches occur both in IGBT and freewheeling diode chips, allowing for higher total power dissipation due to better temperature spreading. The inverter performance is limited by switching losses in outer switches at higher switching frequencies (>1 kHz). On the contrary, at lower frequencies the performance is limited by conduction losses in inner switches. If the losses of both switches are nearly equal (at 1…1.5 kHz), the 3L-NPC inverter with 3.3 kV IGBTs could provide up to 50% increase in the switching frequency, while having similar power dissipation as the two-level inverter with 6.5 kV IGBTs.

In the comparison of the performance at the maximum recommended junction temperature in Figure 4.9, it is shown that at 100 kVA output, the switching frequency is limited to 400 Hz by losses in inner IGBTs. At 50 kVA, the achievable switching frequency is approximately 25% higher than that of the two-level inverter with 6.5 kV IGBTs and its further increase is limited by losses of outer transistors. It should be noticed that the values presented are calculated without taking into account the influence of the junction temperature on semiconductor losses. Unequal loss distribution within an IGBT module could increase the thermal stress on its internal elements due to differences in CTE. In order to balance power losses within a dual IGBT module, one module could be used for the *T1* and *T4* transistors, while the other for *T2* and *T3*. The control system should be changed accordingly. A better balancing of power losses has also been obtained by using 3L-ANPS and 3L-SNPC topologies [93].

On the contrary, such solutions require an increased number of IGBT modules, have a more complex control system and consequently would be more expensive.

Another challenge of the 3L-NPC topology, despite allowing use of lower voltage devices, is insufficient blocking and insulation voltage of such devices. The requirements for rolling stock power electronics are defined in the international standard IEC 1287. Following the IEC 1287, each Infineon module has to sustain the rms. value insulation test voltage (50…60 Hz) of [94]:

$$U_{isol} = 2 \cdot U_{CE} / \sqrt{2} + 1000. \quad (4.2.1)$$

Thus, the insulation test voltage of the modules with 3.3 kV blocking voltage is 6.0 kV (RMS), 1 min. A single IGBT must have voltage blocking capability two times the nominal catenary voltage level, hence in the case of using 3.3 kV class IGBTs in rolling stock inverters, an additional protection system is required to fulfil the standard requirements. Generally, additional insulation could be delivered by additional electrical resistive coating of module baseplate. Such additional layer of insulation could lead to increased thermal resistance between IGBT and heatsink, decreasing thermal performance of the whole system. Such drawback could be overcome by the implementation of KU-KC 15 insulation material produced by Kunze Folien (150 µm thick polymid with breakdown voltage of 12.5 kV AC and thermal resistance of 0.36 K/W) [95]. The driver circuits for IGBTs (based on dual 2SD315AI-33 driver cores) should be provided with additional protection as well.

Recently, some manufacturers, such as ABB [96], Infineon [97] and Mitsubishi [98], have responded to this issue by introducing 3.3 kV devices in 10.2 kV isolated packages. Implementation of these devices will eliminate abovementioned problems and allow easier assembling of three-level converters.

The implementation of the 3L-NPC topology with 3.3 kV IGBTs provides a noticeable increase in the achievable power density. Moreover, the total price of the converter could by reduced dramatically (up to 50%) due to the price difference between 6.5 and 3.3 kV IGBT modules and associated control circuits [92].

4.3 Resonant converters

Resonant converters could also be considered to optimise the hard-switched DC/DC converters in order to suppress the oscillations and improve the switching performance of the HV IGBT modules. The high input voltage of the resonant converter could be achieved by multilevel topologies [99] or converters with series-parallel connection [100]. This, however, requires increased number of components including controlled switches. Due to the increased complexity the reliability is expected to be decreasing. Investigations of 6.5 kV IGBTs operating in resonant topologies report significant increases in efficiency [101][102], however, the transistors were operating in both the ZVS

and the quasi-ZCS mode. This mode of operation is hard to achieve with wide input voltage and load variations. The following investigation focuses on the HB resonant converters based on two 6.5 kV IGBT modules that require minimum modifications to the hard-switched topology [103].

Resonant converter types

Resonant converters are an attractive alternative to traditional hard-switched converters because of reduced switching losses and the EMI due to the sinusoidal behaviour of the resonant circuit. Such converters (Figure 4.10) could operate at high frequencies to reduce the size of their reactive components. These converters generally feature the second or the third order resonant tank circuit, i.e. the storage tank consists of two or three energy storage elements [104]. Resonant tanks can be divided into three groups: series (Figure 4.10a), parallel (Figure 4.10b), and series-parallel. In turn, converters with series-parallel resonant tanks could be classified as LCC, and LLC (Figure 4.10c and Figure 4.10d, respectively). In resonant converters regulation of output parameters is performed by varying the IGBT switching frequency around the resonance frequency of the converter [87].

A major advantage of a series-resonant converter is that the current in the power devices decreases with a decrease in the load, leading to higher efficiency. However, there are difficulties in regulating the output voltage at light load operation [105]. Since the studied converter must operate with wide load variations, this topology is not considered suitable. In contrast to the series-resonant converter, the parallel-resonant converter can regulate the output voltage at no load by running at a frequency above resonance. On the other hand, such converters have higher device current that is relatively independent of the load. This leads to high conduction losses in semiconductor and reactive components, decreasing the efficiency, especially at light loads.

LLC Resonant Converter

LLC resonant converters introduce several advantages over other resonant converters. These converters require a relatively narrow variation of switching frequency to control the output voltage; can operate with a wide load range and ZVS could be achieved over the entire operating range. Moreover, the transformer leakage and magnetizing inductances can be utilised as the resonant elements of the power stage and, thus, they reduce the overall part count. In addition, the series resonant capacitor also provides DC blocking, favourable for an isolation transformer in the half-bridge configuration.

The LLC converter has two resonant frequencies: L_r and C_r determine the higher resonant frequency, while lower resonant frequency is determined by C_r and the series inductance of L_p and L_r. The characteristics of the converter depend on the L_r/L_p inductor ratio. As L_r is reduced, the lower frequency needed at low voltage input decreases. In this case variations in the switching frequency within the operating range are increased, resulting in a complicated passive

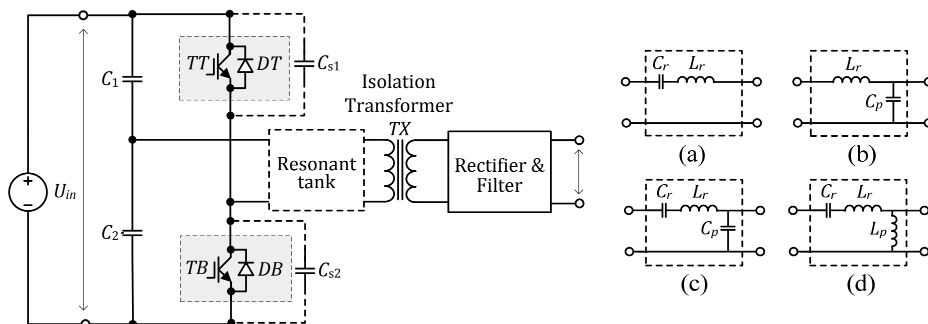


Figure 4.10 Generalised resonant HB converter topology and different resonant tanks

component design. On the other hand, larger L_r will raise the IGBT turn-off current, which increases switching losses. Since the load independent point (higher resonant frequency) is in the ZVS region, the converter could be designed to operate around this point [106]. High efficiency is achieved by the use of capacitive snubbers across the inverter transistors. The LLC converter does not require an LC output filter used in traditional hard-switching HB converters. Only the capacitor filter can be used, leading to a simpler secondary part.

LCC Resonant Converter

The series-parallel converter, also referred to as an LCC converter, aims at combining the advantages of the series and the parallel converters, at the same time reducing or eliminating their disadvantages. Similarly to the LLC, the LCC converter does not require an LC output filter used in a traditional hard-switching HB converter. The transformer leakage inductance can be utilised as the resonant element L_r.

The low resonant frequency is determined by a series resonant tank L_r and C_r while the high resonant frequency is determined by L_r and an equivalent capacitance of C_r and C_p in series. The behaviour is dependent on the C_r/C_p ratio. As C_p is reduced, the converter resembles a series converter and the upper frequency needed at light loads increases. On the other hand, with an increased C_p the converter resembles a parallel converter and the circulating current no longer decreases with the load [104].

Unlike in the case of the LLC converter, the load independent point (lower resonant frequency) is in the ZCS region, while in the ZVS region (the higher resonant frequency) the converter is more sensitive to changes in the load. Only the operation above the upper resonance will be considered in the following as it is more desirable from the practical point of view since the ZVS is provided for the IGBTs, allowing the use of capacitive snubbers to reduce turn-off losses.

Simulation Results

Design of resonant components is always a compromise between load power range, operating frequency, input voltage range, circulating energy in the resonant circuit, etc.

From the efficiency point of view, the LLC converter is best to be operated at the upper resonant frequency. In this case both the circulating energy in the resonant network and the switching losses are low. Since this operating point can only be achieved for one given U_{in} and load power, the LLC resonant converter is usually designed around an upper resonant frequency for a full load and maximum U_{in}. With an increase in the load or a decrease in the input voltage, the switching frequency is decreased to keep the output voltage regulated. The LCC converter is usually designed around an upper resonant frequency for a full load and minimum U_{in}.

The values of the resonant tank components of both converters are selected so that their switching frequency range is similar and relatively narrow (3…4 kHz) and the isolation transformer turns ratio is the same. The main parameters of the analysed converters are listed in Table 4.3. The input voltage

Table 4.3 Main parameters of the compared converters

Converter	f_{sw}, kHz	N_s/N_p	C_r (µF)	C_p (µF)	L_r (mH)	L_p (mH)	L_f (mH)	C_f (mF)
LLC	2.9…3.9	0.17	1.2	–	1.32	2.64	–	2.4
LCC	3.0…3.9	0.17	2.2	1.8	2.87	–	–	2.4

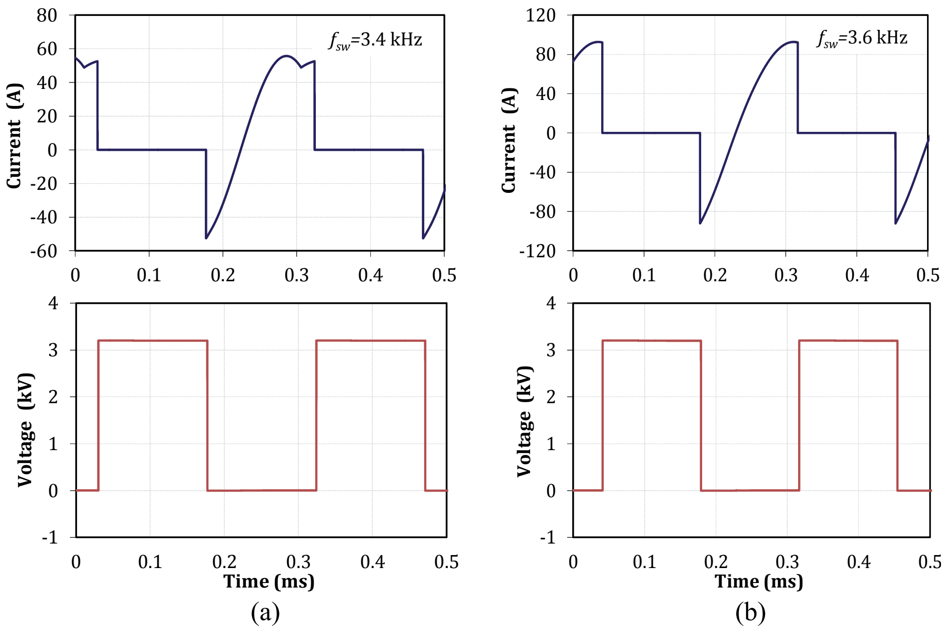


Figure 4.11 Simulated voltage and current waveforms of the TT IGBT module operating in LLC (a) and LCC (b) converters (U_{in}=3.2 kV; 30 kW load)

and load power range as well as the output voltage values are the same as for the hard-switched converter. Both converters are able to operate with ZVS within desired conditions. The simulated waveforms of LLC and LCC converters under nominal conditions are shown in Figure 4.11. According to simulations, the turn-off current of the IGBT as well as the peak current of the rectifier diodes is essentially higher in the LCC converter.

Despite operating with higher switching frequency than the hard-switched converter, the resonant LLC converter is able to provide essential reduction of inverter losses, since turn-off losses of the main switches can be reduced by the help of lossless capacitive snubbers. On the other hand, the LCC converter has higher power losses with a similar regulation frequency range and requires additional adjustments to C_r/C_p ratio in order to reduce switching losses. As a downside, this will result in a wider regulation frequency range, making passive component design more challenging [PAPER-IV].

4.4 Synchronous rectification

General information

The phase-shifted synchronous rectifier concept is a well-known method to reduce the ringing, increase the efficiency and achieve zero voltage switching (ZVS) of converter switches. The other advantages are the possibility of using non-dissipative capacitive snubbers in the inverter and constant frequency operation, allowing for simple control of the converter. Generally, these converters comprise a half- or a full-bridge inverter, a high-frequency transformer and a rectifier [107][108]. The rectifier part could be classified as: full-bridge, central-tapped and current-doubler [109]. The chapter will investigate the feasibility of the half-bridge topology with a full-bridge phase-shifted synchronous rectifier with reverse blocking switches (Figure 4.12), as it requires the least modifications to the reference topology [PAPER-V] .

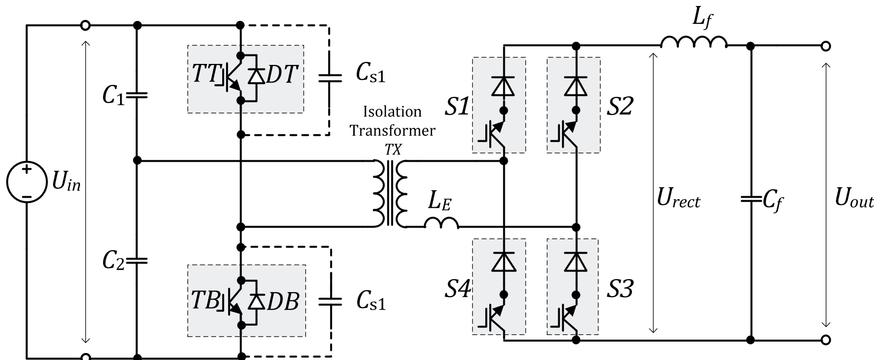


Figure 4.12 Investigated half-bridge converter topology with controlled RB switches at the secondary side

In converters with a synchronous rectifier the output voltage is generally controlled by the varying delay time between the turn-on of the switches in the rectifier and the turn-on of the IGBTs in the inverter. At the beginning of each half-period, the transformer current will have the same direction as in the previous one and will only change it when the other switch pair in the rectifier turns on. Therefore, at the beginning of each half-period, the current will flow through the freewheeling diode of the IGBT module to be turned on next, allowing the ZVS of both inverter transistors. This switching algorithm allows non-dissipative capacitive snubbers to be used in the inverter and the inductive ones in the rectifier [PAPER-IV]. The disadvantage of such a control algorithm is the presence of intervals of energy return from the load to the power supply (time intervals of the opposite sign of the current and voltage of the primary transformer winding during the delay time). If the energy return is not possible, there will be an increase of the input voltage of the inverter and a deviation of

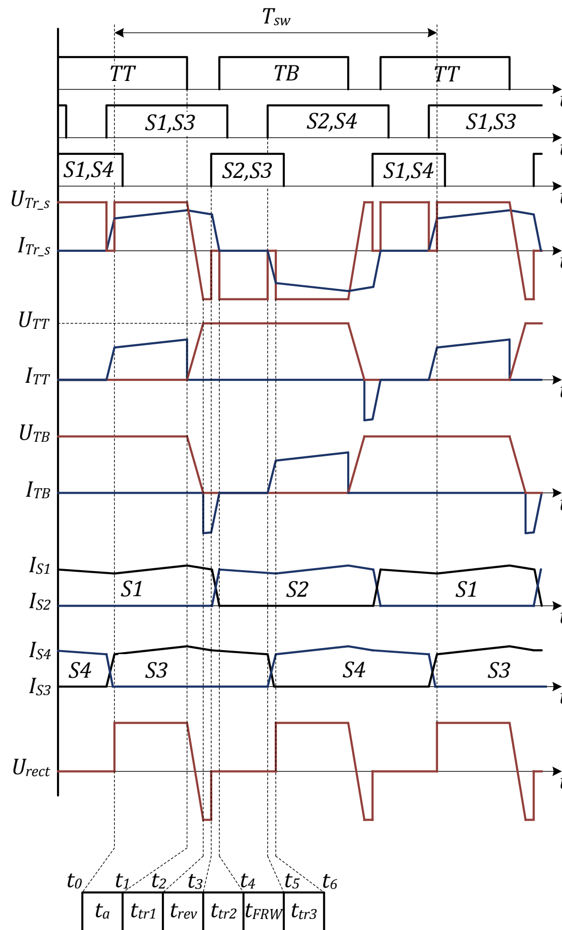


Figure 4.13 Generalised operation principle of a converter with a phase-shifted active full-bridge rectifier using the modified control algorithm

the midpoint potential of the capacitor input voltage divider. Moreover, energy circulation corresponds to the generation of the reactive power, resulting in the reduction of the converter power factor and the efficiency due to increased conduction losses. In the case of high input voltage (large periods of energy return), the effects of these drawbacks could be inacceptable. One of the ways to reduce such effects is to increase the capacitance value of the input voltage divider, however, that leads to an increase in the dimensions and cost of the converter.

Novel control method for a phase-shifted active full-bridge rectifier

To overcome the disadvantages of a conventional phase-shifted synchronous rectifier, the control algorithm of the rectifier switches could be modified, at the same time keeping the advantages of the reference phase-shifted control algorithm. A similar concept for the full-bridge converter was first introduced in [110]. The proposed algorithm provides phase-shifted control together with practically no return of energy into the power supply. This is achieved by introducing two additional switching states of the rectifier switches. The idea of such an algorithm is presented in Figure 4.13. The following events during the switching half-period could be distinguished:

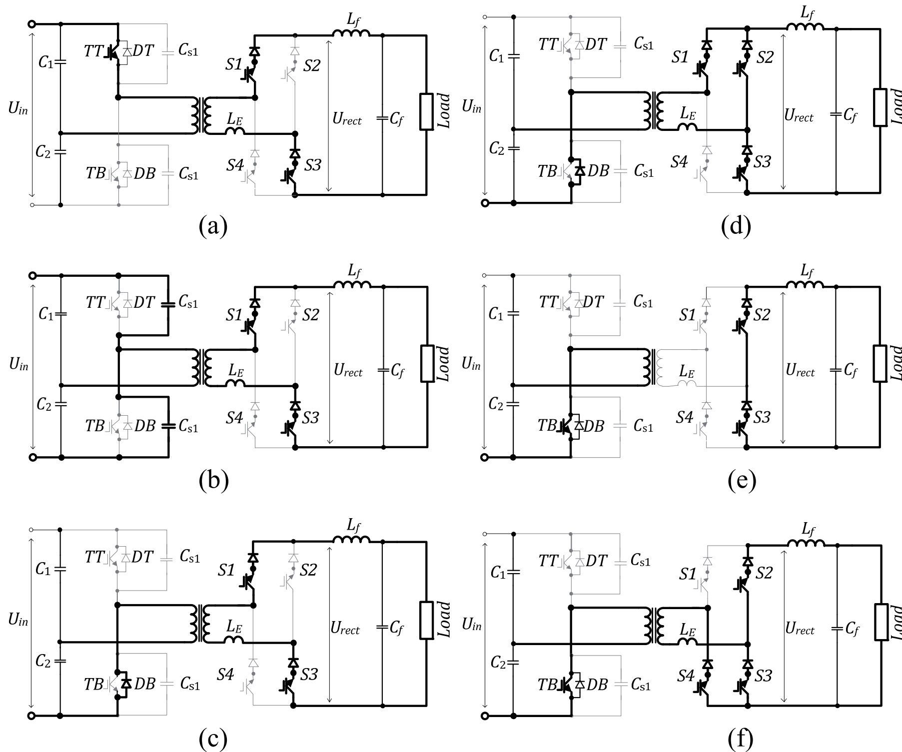


Figure 4.14 Operation modes of the converter with a modified phase-shifted active rectifier

t_0-t_1 – Transistor *TT* and switches *S1*, *S3* are conducting (Figure 4.14a). The voltage of the transformer primary winding is $+U_{in}/2$, and at the output, the voltage of the rectifier is $+U_{Tr\text{-}s}$. Switch S4 could be turned off with ZCS.

t_1-t_2 – Transistor *TT* is turned off. The transformer voltage and U_{rect} change their sign as the snubber capacitors are recharged (Figure 4.14b).

t_2-t_3 – The snubber capacitors are recharged and the transformer primary voltage reaches $-U_{in}/2$. The freewheeling diode *DB* opens, starting the energy return interval and the transistor *TB* could be opened with ZVS from now on. The output voltage of the rectifier is now $-U_{Tr\text{-}s}$ (Figure 4.14c). Until the moment t_3 the processes do not differ from the corresponding ones in the conventional phase-shifted synchronous rectifier.

t_3-t_4 – Switch *S2* is now opened (Figure 4.14d). The voltage across the transformer secondary drops to zero and the transformer current decreases gradually, as the load current transfers from *S1* to *S2* with *di/dt* limited by the circuit equivalent inductance.

t_4-t_5 – The energy return interval is over, the negative voltage $-U_{Tr\text{-}s}$ is applied to the transformer secondary and switch *S1* which can be turned off now with ZCS. Only small magnetising current is flowing through the transformer primary. The load current freewheels through *S3*, *S2*, L_f and the load (Figure 4.14e).

t_5-t_6 – Switch *S4* is opened (Figure 4.14f). The voltage across the transformer secondary drops to zero and the transformer and *TB* current increase gradually, as the load current transfers from *S3* to *S4* with *di/dt* limited by the circuit equivalent inductance.

The processes are then repeated with the difference that the transistors and the primary side diodes replace each other, so do switches *S1*, *S2* and *S3*, *S4*.

The control of the output voltage can be achieved by varying the current freewheeling duration t_s (time interval t_3-t_6). The energy return interval (time interval t_2-t_3) could be constant and should be kept as short as possible in order to maintain the high power factor and reduce conduction losses.

Design considerations

The current section will provide guidelines for the selection of the parameters for the experimental converter with the phase-shifted active full-bridge rectifier (AFBR). In order to simplify the calculations it is assumed that the opponents are lossless, the input capacitors and the transformer magnetising inductance are large enough and therefore the input voltage ripple and magnetising current are neglectable. For the introduced modified control algorithm, six PWM channels are used. The inverted control signals of *S1* and *S2* are shifted by the ratio D_y relative to the turn-off of inverter switches (Figure 4.15). The inverted control signals for *S3* and *S4* are shifted by the ratio D_s relative to *S1* and *S2*. Rectifier channels have a constant duty cycle and the

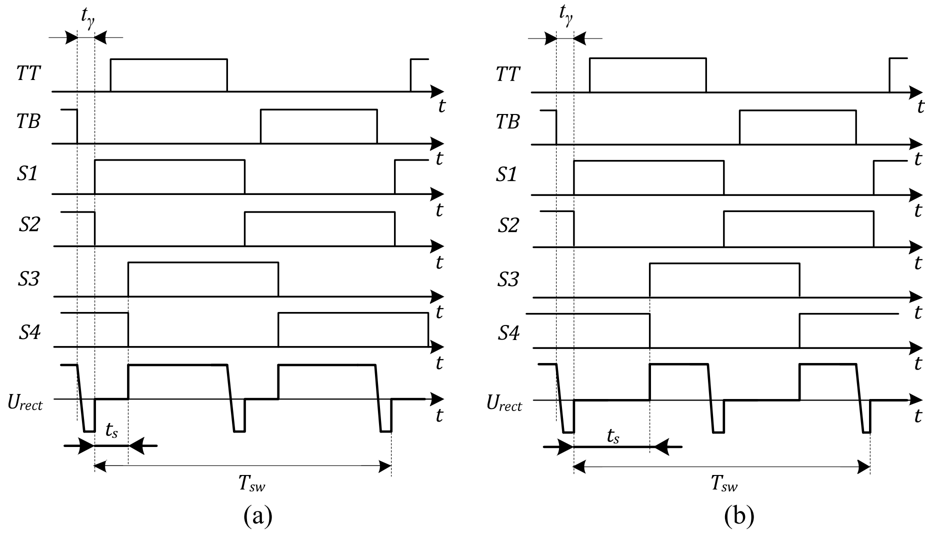


Figure 4.15 Proposed operation principle of the half-bridge converter with the phase-shifted active rectifier at maximal (a) and minimal (b) input voltages

output voltage is regulated by varying the ratio D_s. The values of D_γ and D_s are defined as follows:

$$D_\gamma = \frac{t_3 - t_1}{T}, \tag{4.4.1}$$

$$D_s = \frac{t_6 - t_3}{T} = \frac{t_s}{T}. \tag{4.4.2}$$

The active state duty cycle D_a of the converter can be calculated by

$$D_a = \frac{t_a}{T} = \frac{1 - 2 \cdot t_s - 2 \cdot t_{tr1} - 2 \cdot t_{rev}}{2 \cdot T_{sw}}. \tag{4.4.3}$$

The output voltage can be expressed by the following equation:

$$U_{out} = \frac{N_s}{N_p} \cdot \frac{U_{in} \cdot (t_a - t_{rev})}{T_{sw}}, \tag{4.4.4}$$

and the amplitude voltage across transformer secondary is

$$U_{Tr-s} = \frac{U_{out} \cdot T_{sw}}{2 \cdot (t_a - t_{rev})}. \tag{4.4.5}$$

The average and maximum collector currents of inverter transistors are calculated by

$$I_C = \frac{P_{out} \cdot T}{U_{in} \cdot (t_a - t_{rev})}, \tag{4.4.6}$$

$$I_{C(max)} = I_C + \frac{N_s}{N_p} \cdot \frac{\Delta I_{ripple}}{2}, \qquad (4.4.7)$$

where ΔI_{ripple} is the filter inductor L_f peak-to-peak current ripple.

The inverter switches require a certain dead time t_d to recharge snubber capacitors to maintain the ZVS condition, hence the following expression must be satisfied:

$$t_d \geq t_{tr1} = \frac{2 \cdot U_{in} \cdot C_s}{I_{C(max)}}. \qquad (4.4.8)$$

According to this equation, the most demanding point is at minimum load and maximum input voltage.

A certain time is required for the current of the rectifier switches to fall to zero during the natural commutation, therefore the rectifier switches should operate with a duty cycle higher than 0.5 to maintain the ZCS condition and exclude the situation when only one transistor in the rectifier is turned on. The additional time required can be equal for all the rectifier switches and is estimated from t_{tr2}:

$$D_{rect} \geq \frac{1}{2} + \frac{t_{tr2}}{T_{sw}} = \frac{1}{2} + L_E \cdot \frac{2 \cdot P_{out} \cdot (t_a - t_{rev})}{U_{out}^2 \cdot T_{sw}}, \qquad (4.4.9)$$

where L_E is the equivalent inductance, which in this section is mainly represented by the leakage inductance of the transformer secondary winding.

To estimate the parameters of the output filter inductor it is assumed that the current of the inductor is continuous:

$$L_f = \frac{\left(U_{Tr-s} - U_{out}\right) \cdot t_a}{\Delta I_{ripple}} = \frac{t_a \cdot U_{out}^2}{P_{out} \cdot k_L} \cdot \left[\frac{1}{2 \cdot f_{sw} \cdot (t_a - t_{rev})} - 1\right], \qquad (4.4.10)$$

where k_L is the relative current ripple of the output filter inductor:

$$k_L = \frac{\Delta I_{ripple} \cdot U_{out}}{P_{out}}. \qquad (4.4.11)$$

The capacitance of the output filter capacitor can be approximated as:

$$C_f = \frac{\Delta I_{ripple} \cdot t_a}{\Delta U_{ripple}} = \frac{t_a \cdot k_L \cdot P_{out}}{k_U \cdot U_{out}^2}, \qquad (4.4.12)$$

where ΔU_{out} is the peak-to-peak output voltage ripple and k_U is the relative voltage ripple.

$$k_U = \frac{\Delta U_{out}}{U_{out}}, \qquad (4.4.13)$$

The proposed control concept was simulated using PSIM software. As shown in Figure 4.16, the simulation results were in full accordance with the estimated waveforms.

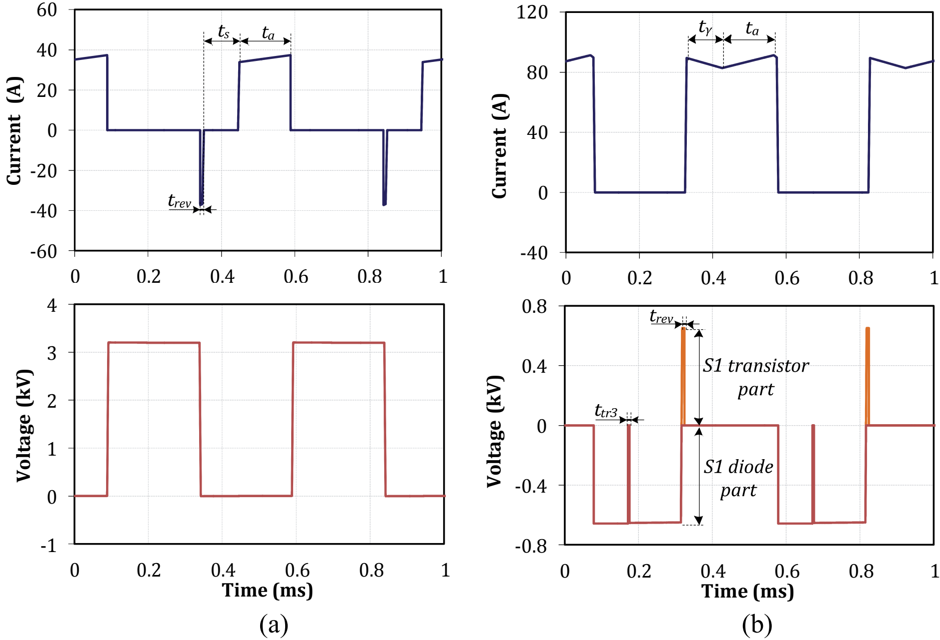


Figure 4.16 Simulated voltage and current waveforms of the TT IGBT module (a); S1 (b) (U_{in}=3.2 kV; f_{sw}=2 kHz, 30 kW load)

Experimental verification

To validate the proposed novel control algorithm for an AFBR, a small-scale prototype with the output power of 1 kW was assembled. Six independent PWM channels were used. Two channels with small dead time were used to drive IGBTs in the inverter and four channels were used to control the rectifier.

As mentioned, rectifier switches should have reverse blocking capability. In the prototype MOSFETs with series connected diodes were used. These switches could be replaced by reverse-blocking IGBTs or fast thyristors for reduced power dissipation during the on-state. The main parameters and components are presented in Table 4.4.

Table 4.4 Main parameters and components of the experimental prototype

Parameter	Symbol	Value / Type
Input voltage, V	U_{in}	300…500
Output voltage, V	U_{out}	40
Switching frequency, kHz	f_{sw}	10
Transformer turns ratio	N_s/N_p	0.28
Output filter capacitance, uF	C_f	220
Output filter inductance, mH	L_f	1.5
Inverter switch	*TT, TB*	BSM75GB120DLC
Rectifier switch	*S1-S4*	IXFX 48N60P
Rectifier diode		ON MBR40250
Output power, W	P_{out}	1000

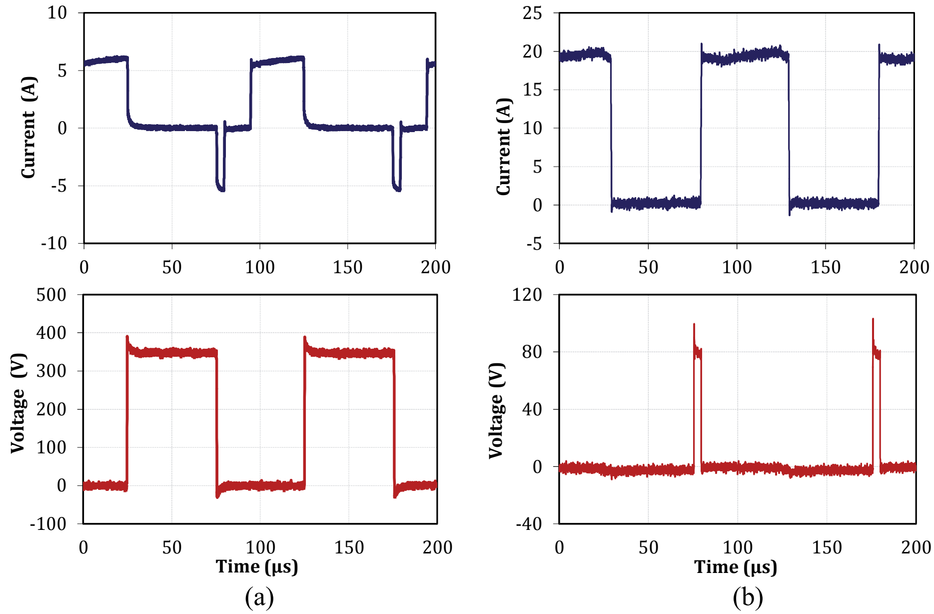


Figure 4.17 Experimental voltage and current waveforms of the TT IGBT module (a); S1 transistor (b) (U_{in}=350 V; f_{sw}=10 kHz, 800 W load)

During the first tests the converter was operating without snubbers and only junction capacitances of the IGBT modules were responsible for reduction in turn-off losses. As shown, the experimental waveforms presented in Figure 4.17 completely correspond to the estimated waveforms. Since the application of capacitive snubbers allows turn-off losses of the inverter IGBTs to be further reduced, the operation of the experimental prototype was tested with different snubber capacitors. The power losses without a snubber could be estimated using Equation 3.2.34. The required capacitance value could be roughly estimated by [111]:

$$C_s \approx \frac{I_C \cdot t_f}{4 \cdot U_{in}}, \tag{4.4.14}$$

where t_f is the interval starting from when collector current falls from 90% to 10% of the turned-off current (Figure 3.12).

The IGBT turn-off losses with a snubber capacitor assuming linear current and voltage slopes can be calculated by

$$E_{off} = \frac{U_{in} \cdot I_C^2 \cdot t_f^2}{24}. \tag{4.4.15}$$

The experimental waveforms are shown in Figure 4.18. As it could be observed, with the application of a snubber, the dU_{CE}/dt is reduced to 500 A/μs with a 10 nF snubber capacitor and to 330 A/μs with a 22 nF snubber capacitor

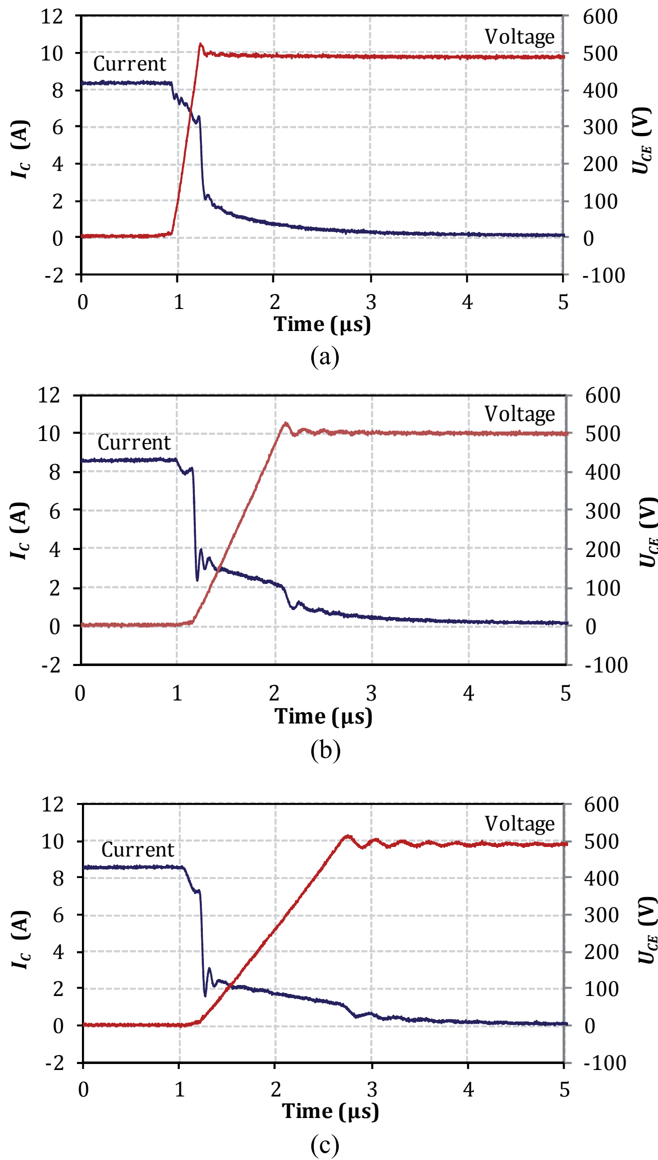


Figure 4.18 Experimental turn-off waveforms of the TT IGBT module: no snubber (a), 10nF snubber (b) and 22nF snubber (c) (U_{in}=500 V; f_{sw}=10 kHz, 1000 W load)

from 2000 A/µs in the case of turn-off without snubber. By the use of a snubber the duration of the tail current remained approximately the same, but its amplitude increased, since the voltage applied to drive out the remained charge carriers from the drift region was lowered. The turn-off loss reduction with a snubber connected is substantially lower than that estimated from the theoretical equations due to the tail current increase with a lower dU_{CE}/dt. Nevertheless, even with a 10 nF snubber, the total turn-off losses were significantly reduced

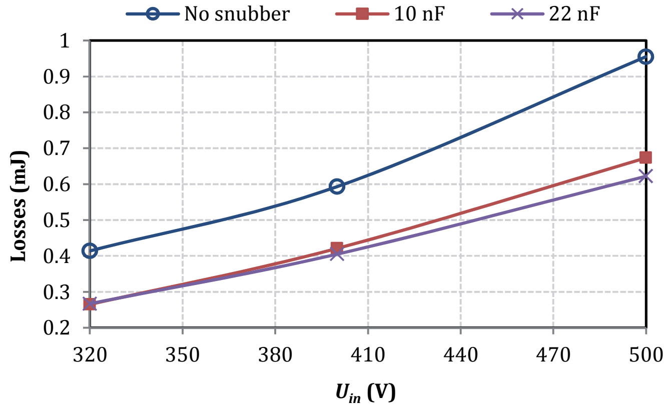


Figure 4.19 Turn-off energy losses of the TT IGBT module with different snubber capacitors

(by 30-35%) in comparison to turn-off without a snubber and roughly by 50% from the losses expected during hard-switched turn-off (Figure 4.19). However, in terms of energy losses the effect of using a larger snubber capacitor becomes less obvious, especially at lower voltages.

The reduction in the IGBT turn-off power loss by help of capacitive snubbers has been reported to be dependent on the IGBT technology and the junction temperature. Typically, it is lower than expected from theoretical estimations due to increased current tail duration and should be experimentally estimated for every particular application to obtain a precise result. A 50% reduction of turn-off losses of soft-switched 6.5 kV FS- and SPT-IGBTs is reported in [122]. Similar results were obtained with a range of IGBTs with different blocking voltages [111][123][124][126]. Hence, the approximate average reduction of 50% is considered reasonable.

4.5 Parallel connection of a HV IGBT and an IGCT

Overview

As mentioned previously, during the design process the power semiconductor devices could be optimised either to have superior switching performance or on-state characteristics. Presently most manufacturers offer several versions of devices optimised for different applications. For high current applications with low switching frequency the devices with low conduction loss are the most feasible option. In fact, in the following generation of IGBTs, the balance between switching losses and conduction losses will increasingly move towards lower on-state voltage drop (conduction losses) [102]. On the contrary, fast switching converters require devices optimised for lower switching losses. The appearance of IGCTs and HV IGBTs on the market has encouraged the development of high power hard switching converters for industrial and traction applications. HV IGBTs (>3.3 kV) typically have higher conduction losses than

the IGCTs generally used in higher-power applications. These devices feature better thermal handling capability thanks to the press-pack housing type where double-side cooling is possible. Unfortunately, due to the structure of the thyristor, the *di/dt* cannot be controlled during the turn-on of the IGCT; therefore a small clamp circuit is required to limit the *di/dt* of the freewheeling diodes during turn-off, in order to keep it within the SOA.

Different approaches have been introduced to achieve improved performance of semiconductor switches. The goal was to combine the controllable and fast switching characteristics of IGBTs with the superior on-state characteristics of thyristors. A wide range of devices, like MCT (MOS-Controlled Thyristor), DG-EST (Dual-Gate Emitter Switched Thyristor), IEGT (Injection Enhanced Gate Transistor), etc. have been introduced. These are generally hybrid devices, combining different semiconductor structures. Very few of the proposed devices have been introduced into mass production mainly due to current sharing problems, small SOA complex driving requirements or difficult and expensive manufacturing technology [112].

Alternatively, improved characteristics could be obtained by a parallel connection of commercially available semiconductors with different design optimisations [PAPER-VI], for example, 4.5 kV IGCT 5SHY35L4512 (ABB), optimised for low frequency operation with low on-state losses, and IGBT T0900EA45A (Westcode) with relatively low turn-off losses. Since both IGBT and IGCT type semiconductors are available in press-pack type housings, an easy connection of these devices in series by special cooling systems is possible. The rated permanent DC voltage for both semiconductor devices is 2.8 kV. Using two- or three-level topologies, if necessary, this is sufficient to cope with the requirements of many traction and industrial applications with voltage ratings of 2.0-5.6 kV without the need of series connection of several semiconductors.

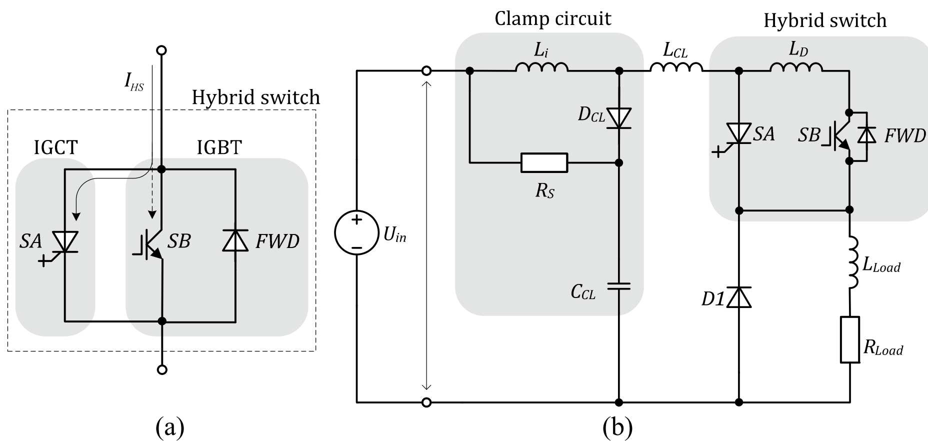


Figure 4.20 Proposed hybrid switch configuration (a) and operation circuit (b)

The idea is based on the integration of positive properties of gate-commutated thyristors in terms of low turn-on and on-state power losses as well as high surge current capability and IGBTs with their relatively low losses during turn-off. This may allow creating high-voltage and high-current energy-efficient switches with increased switching frequency, which could be advantageous in high-power (>500 KVA) industrial, marine and railway traction systems, such as (flexible alternating current transmission systems) FACTS and high power variable frequency AC drives.

Operation principle

As presented in Figure 4.20a, the proposed hybrid switch (HS) consists of a parallel connected asymmetrical press-pack IGCT and a press-pack IGBT with a FWD. In the following analysis, the HS is assumed to be operated in VSI circuits including a clamp circuit. The clamp circuit typically used in IGCT applications limits the surge reverse-recovery current of the turning-off freewheeling diodes and generally consists of a *di/dt* limiting inductor L_i, a clamp capacitor C_{CL}, a clamping diode D_{CL} and a resistor R_S (Figure 4.20b). In the case of a failure, the clamp inductance limits the short circuit current as well. The inductances L_{CL} and L_D represent the stray inductance of the clamp and the stray inductance between the IGCT and IGBT housings, respectively. The generalised operation principle is shown in Figure 4.21 and the following time intervals during the operation period can be distinguished:

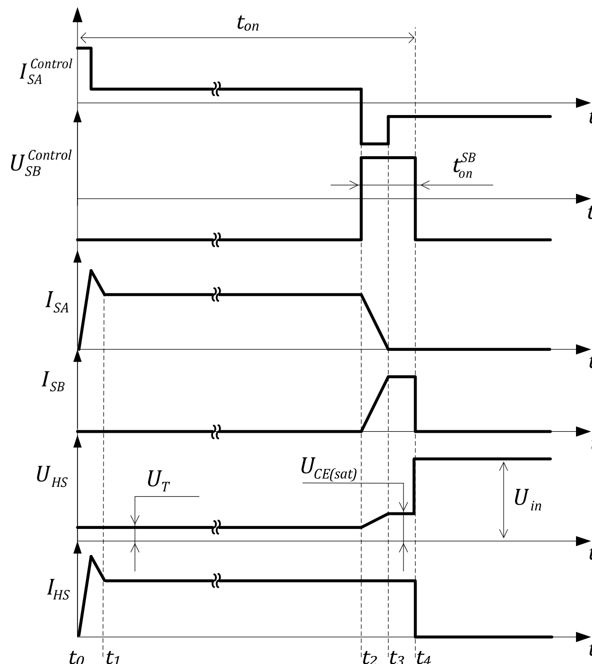


Figure 4.21 Generalised operation principle and switching waveforms of the proposed HS

t_0 – the beginning of each switching period of PWM. The thyristor *SA* is turned on by the control signal, applying full load current. During this time the transistor is turned off.

t_0-t_1 – freewheeling diode reverse-recovery process, duration and behaviour are dependent on the diode type and *di/dt*.

t_1-t_2 – thyristor is conducting with low losses. The on-state voltage is determined by the voltage drop across the thyristor U_T.

t_2 – the turn-off control impulse is applied to the thyristor and simultaneously the turn-on impulse is applied to the transistor *SB*.

t_2-t_3 – as the turn-on behaviour of the IGBT is faster than the turn-off transient of the IGCT, the thyristor turn-off process occurs when the transistor is already in the on-state. The load current is distributed between both semiconductors.

t_3 – the *SA* returns to the blocking state, the full load current is applied to the transistor *SB*. Hence, the turn-off transient of the thyristor occurs when the voltage is limited to the voltage drop $U_{CE(sat)}$ across the conducting transistor *SB*. Moreover, during the current transfer to the transistor, the voltage across its terminals is limited to the voltage drop across the *SA* during the on-state. The required duration of the transistor on-state should not be shorter than the turn-off transient of the thyristor.

t_4 – the turn-off of the HS occurs by applying negative gate voltage to the transistor after the thyristor returns to the blocking state. The turn off transient of the HV IGBTs is generally 2…7 μs. After the transistor is switched off, the voltage across HS and all its components become equal to the supply voltage.

In real conditions the minimal and maximal duty cycle of the HS could be limited by a number of factors, such as IGCT gate driver limitations or behaviour of the clamp circuit and a turn-off snubber (if used). The minimal off-state time should be maintained to stay within SOA of the circuit's components. The minimal on-state time of the HS is generally not limited since during an operation with duty cycles near zero, only the transistor of the HS could be used.

Switching behaviour and analysis of losses

To simulate the HS operation, the switching behaviour was modelled in PSpice software using idealised switch models. The equivalent diode model was used in the topology and the values of the clamp circuit were determined according to [113]. The simulations confirm the estimated behaviour of the proposed switch configuration. At turn-on the HS operates like an IGCT with the *di/dt* clamp. The on-state voltage is equal to the voltage drop across the thyristor during the on-state. At turn-off the transistor is turned on for a short period. During this hold-off period the turning-off thyristor current is transferred to the transistor, which is closed right after the thyristor current, becomes close to zero (Figure 4.22).

After the turn-on of the IGBT, the current distribution between the conducting IGBT and IGCT is mainly influenced by different characteristics of the semiconductors, temperature differences and asymmetrically distributed stray inductances in the circuit [114][115]. Assuming both semiconductors in the conducting state, the current sharing inside the HS, neglecting cell resistances and inductances, can be calculated by

$$k_I = \frac{I_{SA}}{I_{SB}} = \frac{U_{CE(sat)}(I_{HS})}{U_T(I_{HS})}. \quad (4.5.1)$$

Using Equation (4.4.1) the IGBT and IGCT currents could be obtained by

$$I_{SB} = I_{HS} \cdot \frac{1}{1+k_I}, \quad (4.5.2)$$

$$I_{SA} = I_{HS} \cdot \frac{k_I}{1+k_I}. \quad (4.5.3)$$

The turn-off losses of the IGCT may not be completely removed due to several factors. Firstly, for a large area device, such as the IGCT, a significant output capacitance must be charged in order to establish the depletion region to support voltage. Another factor is the free carriers which had not recombined, being swept from the junction. According to previous investigations, the IGCT switching losses at zero current switching can be reduced by about 35% at small hold-off times (5 μs) to about 95% at large hold-off times (30 μs) [116].

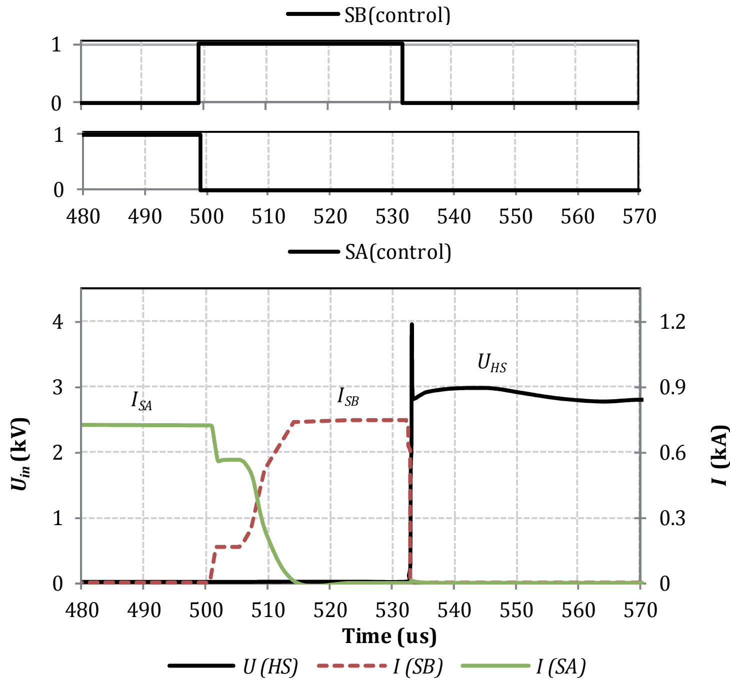


Figure 4.22 Simulated turn-off behaviour of HS at I_{HS}=750 A, U_{in}=2.8 kV

The task to be solved next is to estimate the power losses and performance of the proposed switch configuration with transistor- and thyristor-only counterparts at similar operation parameters. In the comparison, a variable switched current of 350 A < I_{HS} < 900 A and U_{in}=2.8 kV is assumed. The total losses are calculated as the sum of conduction, turn-on and turn-off losses at the maximum junction temperature (125°C), using the datasheet values of the devices. Three commercially available 4.5 kV class devices are compared: asymmetric IGCT-5SHY35L4512 (optimised for low on-state losses), RC-IGCT-5SHX26L4510 and IGBT-T0900EA45A (optimised for medium switching frequency). The losses in *di/dt* limiting turn-on snubbers are not considered in this section.

According to simulations, the considered asymmetric IGCT is showing better dynamics for currents above 650 A, whereas the IGBT is performing better at lower currents (Figure 4.23). The proposed switch configuration is estimated to provide 2.3…2.8 times increased switching frequency in comparison to a single hard switched IGBT or an asymmetric IGCT with *di/dt* clamp circuit exhibiting the same power dissipation of 3 kW. Assuming the same switching frequency in the range of 250…1050 Hz and switch current of 750 A, the IGBT performs better than the asymmetric IGCT at frequencies above 450 Hz, whereas the HS provides substantial (1.9…2 times) decrease in power losses in comparison to single semiconductors (Figure 4.24). In all simulations the reverse-conducting IGCT had 25-30% lower power losses than the IGBT. This difference is mainly due to the fact that the thyrisor is assumed to be operating with *di/dt* limiting turn-on snubber. If the snubber is used with both the IGBT and asymmetric IGCT devices, the turn-on losses would be similar. On the other hand, the turn-off losses of the IGBT may increase slightly [117].

In the simulations of losses, the minimum IGBT switching losses with a very small gate resistances of $R_{G\text{-}on}$=4 Ω and $R_{G\text{-}off}$=2.5 Ω are assumed. In real

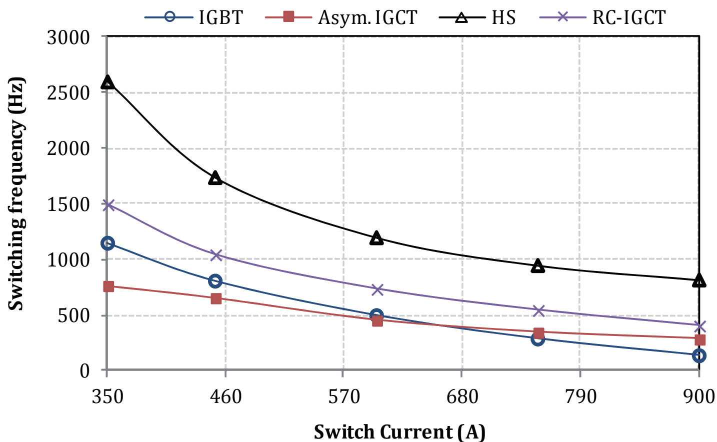


Figure 4.23 Maximum switching frequency vs. current for different semiconductor configurations corresponding to 3 kW total power dissipation at U_{in}=2.8 kV, D=0.5

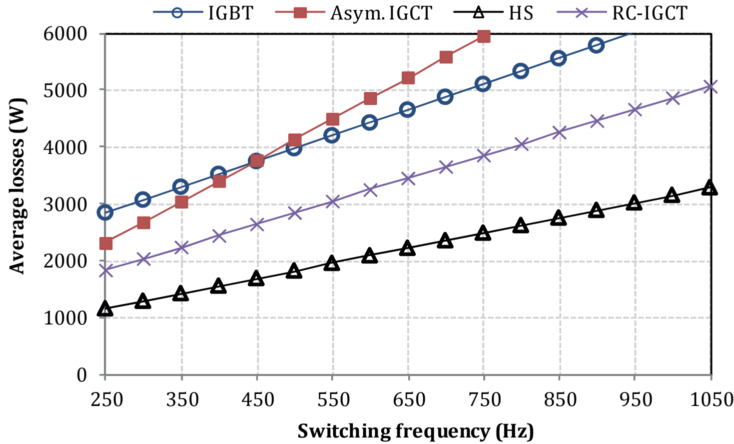


Figure 4.24 Switch power dissipation vs. switching frequency for different semiconductor configurations at I_{HS}=750 A, U_{in}=2.8 kV, D=0.5

industrial converters the IGBT gate units are adjusted to generate the desired *di/dt* and *du/dt* to avoid large voltage and current spikes during transients. However, the use of the gate resistor to control the *di/dt* results in substantially higher switching losses in IGBT [118].

Implementation of hybrid switches in the 3L-NPC inverter

One of the applications, where the proposed approach may provide substantial benefits is the 3L-NPC inverter. The inverter to be analysed in this section is operating with a sinusoidal PWM strategy and has three different commutation states: P, O and N (Table 4.2). The output voltage can take three different levels ($+U_{in}/2$; 0; $-U_{in}/2$) and the voltage stress of each switching device is limited to $U_{in}/2$. The main operation parameters are presented in Table 4.5. More detailed analysis of the topology and its control strategy is presented in [119].

During operation of the three-level inverter, the switching frequency of the inner switches *S2* and *S3* is equal to the output frequency f_{out}, hence the switching losses of these switches are minor. IGCTs optimised for low on-state losses are an attractive option for these switches. On the contrary, the outer switches *S1* and *S4* operate at high frequency and switching losses represent a significant part of the total power dissipation, limiting the frequency of operation. Due to significantly lower losses during turn-off, the implementation of HS as outer switches could provide a significant increase in the overall inverter performance. The analysed inverter topology is presented in Figure 4.25. As shown, in contrast to the classical 3L-NPC topology with reverse-conducting IGCTs, the proposed optimised inverter features two additional IGBTs in parallel to outer switches. The goal is not only to achieve better power loss distribution, but in addition, to reduce the overall losses in the semiconductors.

The power losses in the classical 3L-NPC topology with reverse-conducting IGCTs-5SHX26L4510 are compared to those in the optimised inverter featuring ABB IGCTs-5SHY35L4512 and Westcode IGBTs-T0900EA45A (see Figure 4.26 and 4.27). It could be observed that power losses in the optimised inverter are more evenly distributed across semiconductor components. Similar properties are observed in three-level active NPC topologies [119][121], but in addition, the optimised inverter features 27% lower total power losses. The losses in the most stressed device are reduced by a factor of 2.25. If the topology is working in the rectifier mode with a low modulation index, then it is

Table 4.5 Main operation parameters of the 3L-NPC inverter

Parameter	Value
Supply voltage of the inverter, U_{in}	5.6 kV DC
Rated power	1 MVA
Switching frequency, f_{sw}	750 Hz
Output frequency, f_{out}	50 Hz
Maximum junction temperature of semiconductors, $T_{j(max)}$	125°C

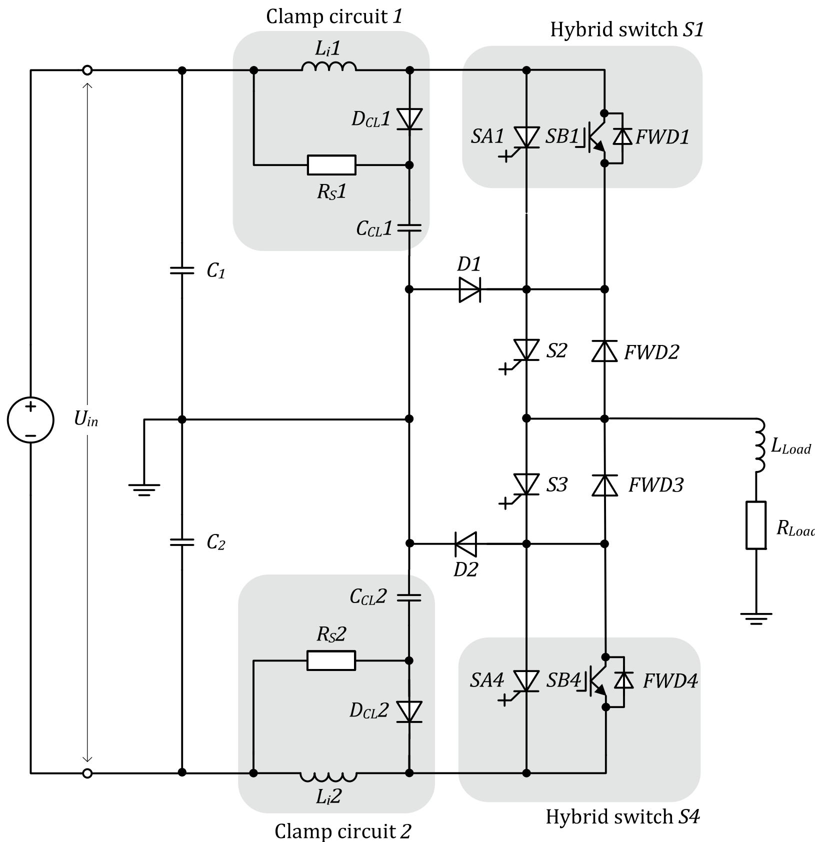
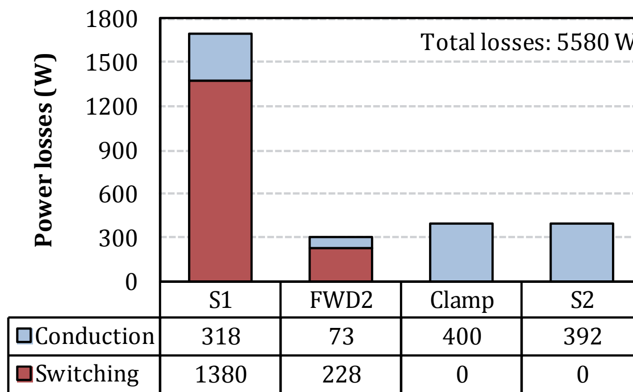


Figure 4.25 Analysed 3L-NPC inverter topology

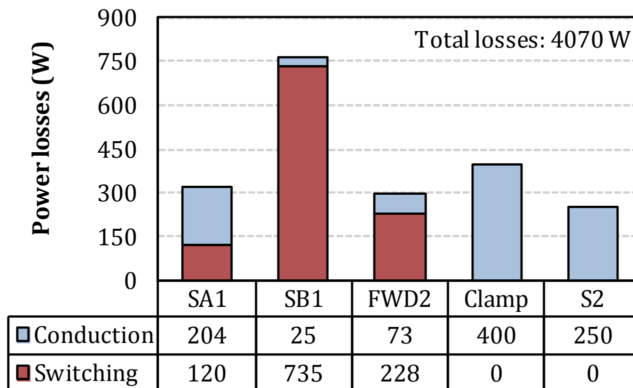
feasible to use hybrid switches as inner switches. This allows higher efficiency and/or increasing switching frequency to be achieved at the cost of increased complexity and semiconductor price.

The control strategy shown in Figure 4.21 could be further extended to take into account total losses in the individual device and apply the control strategy in order to balance the power losses and junction temperature. For example, to reduce losses in *SB1*, some of the turn-off operations can be performed by switch *SA1*. Further improvement in the characteristics could be achieved by using modified IGBT modules with shifted balance to lower switching losses. As shown in [102] by additional irradiation of the standard HV IGBT, the turn-off energy losses could be reduced by roughly 50 %, accepting double on-state losses.



	S1	FWD2	Clamp	S2
Conduction	318	73	400	392
Switching	1380	228	0	0

Figure 4.26 Loss distribution in the 3L-NPC inverter featuring ABB IGCTs-5SHX26L4510 (PF=0.9, M=0.95)



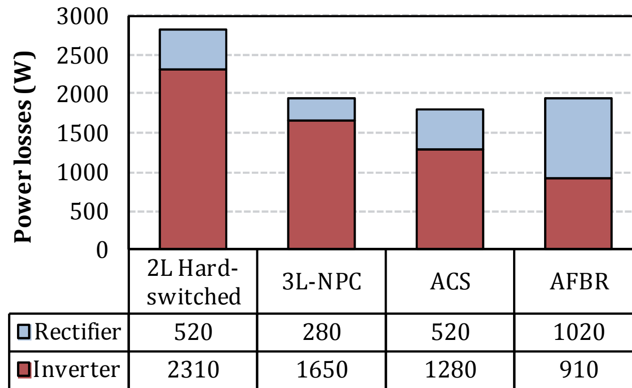
	SA1	SB1	FWD2	Clamp	S2
Conduction	204	25	73	400	250
Switching	120	735	228	0	0

Figure 4.27 Loss distribution in the 3L-NPC inverter featuring ABB IGCTs-5SHY35L4512 and Westcode IGBT-T0900EA45A (PF=0.9, M=0.95)

4.6 Generalisations

The focus of the present chapter was on the investigation and verification of different performance improvement methods of the 6.5 kV IGBT based two-level hard-switched DC/DC converter. During the research, a couple of prototypes were built to verify the theoretical assumptions.

The estimated semiconductor power losses of different investigated converter topologies at f_{sw}=2 kHz and at f_{sw}=1...4 kHz are presented in Figure 4.28 and Figure 4.29, respectively. As it could be observed, the converter with a phase shifted active rectifier outperforms both the 3L-NPC and the two-



	2L Hard-switched	3L-NPC	ACS	AFBR
Rectifier	520	280	520	1020
Inverter	2310	1650	1280	910

Figure 4.28 Semiconductor power loss distribution of different investigated converters (f_{sw}=2 kHz, U_{in}=4kV, 50 kW load)

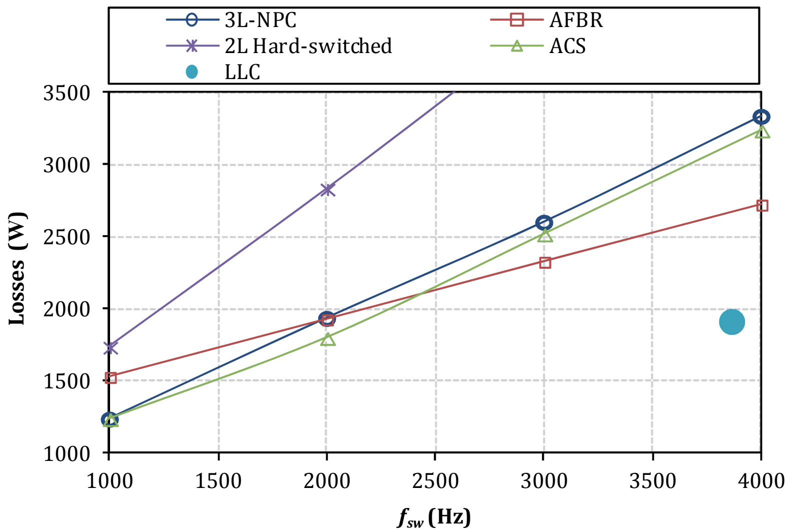


Figure 4.29 Semiconductor power losses vs. switching frequency of different investigated converters (U_{in}=4 kV, 50 kW load)

Table 4.6 Maximum switching frequency of different investigated converters assuming T_{amb}=60ºC and forced air cooling with R_{thsa}=0.013 K/W

Topology	Maximum frequency at 125ºC (kHz)
2L Hard-switched	1.6
3L-NPC	2
ACS	2.5
AFBR	4
LLC	3...4

level active clamped converters at frequencies above 2.5 Hz. The LLC resonant converter could provide even lower losses in semiconductors, however, in real systems the total power losses could be distinctly higher than the values presented due to the additional power dissipation of passive components. It should be mentioned that the maximum achievable switching frequency is different for the converters investigated due to power losses in the HV IGBTs. The values are presented in Table 5.2, assuming forced air cooling and other conditions listed in Table 3.6. The power loss estimations of the LLC converter and the converter with a phase-shifted active full-bridge rectifier consider a 50% IGBT loss reduction during turn-off with the snubber capacitors.

According to performed investigations, the following generalisations are made:

- implementation of passive *RC* snubber is the simplest and effective way of damping the parasitic oscillations. On the other hand, since the transformer leakage energy is dissipated in the resistors, the overall efficiency of the converter is not increased.
- The investigated ACS topology uses auxiliary switches during the freewheeling state to transfer the transformer leakage energy to the auxiliary capacitor, which is utilised during the next active state. The FWDs of the main switches never conduct and their voltage during turn-off is reduced to $U_{in}/2$, therefore the turn-off losses are reduced by approximately 50%. This allows the topology to operate at switching frequencies up to 2.5 kHz. The topology, however, requires one auxiliary HV capacitor and, more importantly, two additional switches having half of the blocking voltage of the main switches as well as associated control and protection systems. Increased HV component count and complexity will have a negative impact on the price of the converter.
- The implementation of the 3L-NPC converter allows implementing lower voltage rated and significantly cheaper 3.3 kV IGBTs. The modified control algorithm provides the ZVS of inner switches over the whole range of operation conditions. Despite providing an increase in achievable maximum switching frequency, the topology suffers from uneven power loss distribution in the main switches. The most stressed device limits the maximum frequency of operation. At maximum output power the achievable recommended switching frequency is approximately 25%

higher than that of the two-level inverter with 6.5 kV IGBTs and its further increase is limited by the losses of outer transistors.

- Implementation of resonant converters instead of the hard switching half-bridge topologies seems to be an attractive way to improve the efficiency of the power converter. Both LLC and LCC converters can deliver low noise and ZVS of the inverter switches over the whole range of operation conditions. Despite providing advantages in terms of switching performance, the additional complexity of the resonant topologies, more complicated control and protection as well as possible reduction in robustness reliability may not overcome the advantages they bring.
- The introduced modified control algorithm for the converter with an AFBR allows the ZVS of the inverter switches and the ZCS of the rectifier switches over the whole range of operation conditions. At the same time the parasitic oscillations after the turn-off of the inverter's IGBTs are completely avoided. The leakage inductance of the transformer acts as the turn-on snubber for rectifier transistors and turn-off losses of the inverter transistors could be reduced using lossless capacitive snubbers. Unlike the resonant converter, the proposed solution has only minor modifications on the HV side, it does not require any additional bulky passive components or frequency-control algorithm, it features reduced energy circulation during the operation and provides the highest power loss reduction in the inverter. The operation of the converter was verified with the experimental prototype and the test results were in full accordance with the expected waveforms. Since presently the current capability of commercially available 1.2 kV RB-IGBTs is not high enough to make their implementation feasible in the given application, a worst-case scenario of a series connected IGBT and a diode is considered in power loss estimations. Fast thyristors or RB-IGBTs could provide around 50% reduced power dissipation in the rectifier. The required adjustments to the low-voltage side are estimated to have significantly lower impact on the final price than both resonant and auxiliary switch converters as well as provide higher benefits in terms of maximum switching frequency (up to 4 kHz) than the 3L-NPC converter.
- Using commercially available 4.5 kV IGBTs and IGCTs in press-pack housings it is possible to create energy efficient switches with decreased power losses. Despite having decreased maximum current capabilities in comparison with parallel connected identical transistors or thyristors and a higher price than single semiconductor switches, the proposed switch configuration could be beneficial in applications where higher switching frequencies are required or decreased cooling system requirements are essential.

5 FUTURE RESEARCH AND DEVELOPMENT: Alternative Methods for Power Density Improvement of High-Power DC/DC Converters

5.1 High-performance cooling for power electronic converters

The maximum junction temperature $T_{j(max)}$ of power semiconductors (generally 125…175°C for IGBT modules) is provided by the manufacturer and has to be followed at any time of operation. The heat potential due to energy losses has to be dissipated by a cooling system, which may also be a constructional element (case, chassis etc.) [77]. A more detailed overview is presented in [125], while the most important aspects are presented in the following sections.

There are many ways to remove heat from a device, however, nearly all of them are based on the same common principle: to move heat away from the device to the ambient medium (in most cases air) by convection, conduction and radiation.

With the drastically increased power dissipation of HV IGBTs only high-performance cooling systems should be used in order to improve converter dimensions. The ability to dissipate heat greatly influences the overall converter design and to achieve a cost-optimised solution, all the electrical and thermal components should be considered carefully. Figure 5.1 demonstrates the heat transfer coefficient attainable with different cooling techniques [127].

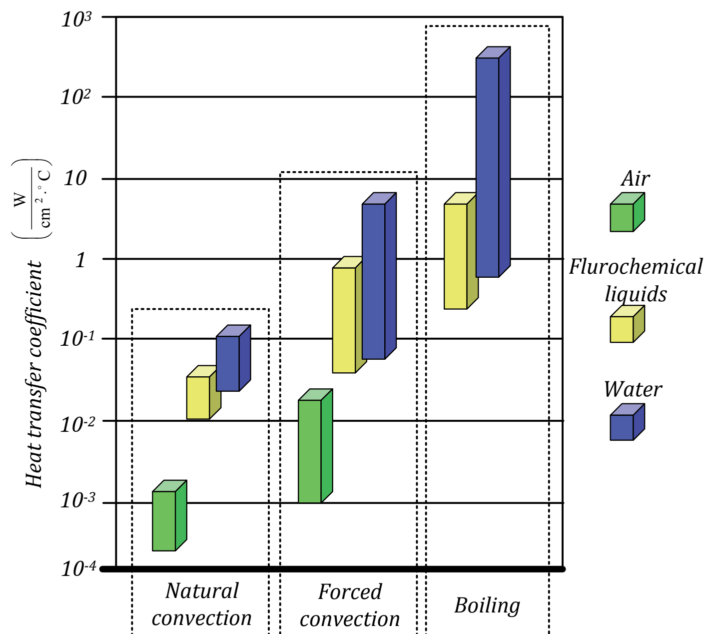


Figure 5.1 Heat transfer coefficient attainable with different coolants and cooling methods

Estimation of parameters

Since losses in semiconductors generally increase with temperature, it is recommended to keep it as low as possible in order to improve the efficiency of the power electronic system. Conduction losses for an actual operating temperature could be estimated by using on-state voltage U_{T0} and slope resistance r_T characteristics at 25°C [68]:

$$P_{cond}(T°\mathrm{C}) = \left(\frac{f_V - 1}{100°\mathrm{C}} \cdot T°\mathrm{C} + \frac{5 - f_V}{4}\right) \cdot U_{T0}^{25°\mathrm{C}} + \left(\frac{f_R - 1}{100°\mathrm{C}} \cdot T°\mathrm{C} + \frac{5 - f_R}{4}\right) \cdot r_T^{25°\mathrm{C}}, \quad (5.1.1)$$

where f_V is a factor for the temperature dependency of U_{T0}, and f_R expresses the temperature dependency of on-resistance r_T. The factors f_V and f_R depend on the device technology and blocking voltage (IGBT ≈ 0.76…1.56; FWD ≈ 1…1.73).

Analogous to conduction losses, both IGBT and diode switching energies are assumed to depend linearly on the temperature according to

$$P_{sw}(T°\mathrm{C}) = \left(\frac{f_T - 1}{100°\mathrm{C}} \cdot T°\mathrm{C} + \frac{5 - f_T}{4}\right) \cdot \frac{1}{f_T} \cdot E_{sw}^{125°\mathrm{C}}, \quad (5.1.2)$$

where $E_{sw}^{125°\mathrm{C}}$ is the energy loss at 125°C; f_T is the temperature coefficient (IGBT ≈ 1.32…1.6; FWD ≈ 2.28).

The first approximation of the average junction temperature is obtained using the one-dimensional equivalent circuit and datasheet values of the device. However, if the semiconductor is operating with low duty cycle, at low frequency pulsed loads, the transient thermal impedance characteristics are used instead. The Foster network is the most popular model of a device's transient thermal impedance [80]:

$$Z_{thjc}(t) = \sum_{i=1}^{n} R_{thi}\left(1 - \exp^{\frac{-t}{\tau_i}}\right), \quad (5.1.3)$$

where R_{thi} is the thermal resistance of the i-th RC-pair,τ_i is the time constant of the i-th RC pair: $\tau_i = R_i \cdot C_i$ and n is the number of the thermal time constants. These coefficients are often listed in the datasheet of the device.

In the majority of cases, the focus of interest with respect to a periodic sequence of power pulses is the stationary temperature swing in the stationary condition. It can be derived from the general equation of the Foster network in an analytical expression [2]:

$$\Delta T_{stat}^{max} = P_{pulse} \cdot \sum_{i=1}^{n} R_{thi} \frac{1 - \exp\left(-\frac{t_{on}}{\tau_i}\right)}{1 - \exp\left(-\frac{t_{on} + t_{off}}{\tau_i}\right)}, \quad (5.1.4)$$

where P_{pulse} is the single pulse power dissipation, t_{on} and t_{off} are switch on-state and off-state times, respectively.

For pulse width low values, the T_j is lower since the thermal capacity of the die, solder and package sets different time constants on the rate at which T_j rises. Therefore, the thermal impedance is smaller at short pulse durations, explaining why the SOA is wider for short pulse widths.

The disadvantage of such an analytical approach is that it is based on the one-dimensional thermal model. Hence, it is impossible to estimate the influence of heat sources on each other neither is it possible to estimate the impact of non-uniform temperature distribution along the heatsink. The three-dimensional models created in computational fluid dynamics software could provide more precise results. In order to validate the precision of the model it is always recommended to compare simulation results with measurements or with the other models.

Current state-of-the-art and trends

A comparison of the thermal resistance layers in the IGBT module reveals that a copper baseplate is the greatest contributor (around 50%) to the overall thermal resistance from chip to case [2]. The recently introduced Semikron SKiiP module structure is without the baseplate. These modules are designed to be used typically with liquid cooling systems. A special mechanical pressure system is used to attach the DBC plate to the heatsink with no need of soldering.

Thermal Interface Materials (TIMs) are widely used to provide a path with low thermal resistance between the heat generating devices and the heatsink. The case to heatsink thermal resistance R_{thcs} value depends on the semiconductor installation conditions. If not installed properly, an excessive thermal resistance or an early failure can occur. The R_{thcs} value depends on the thermal resistance value of the thermal interface material between the module and the heatsink. Thermal interface materials come in a wide variety of product types: thermal compounds (greases), thermal pads (films) or phase change materials (PCMs) and could be either electrically conducting or insulating. The thermal resistance of the TIM could be estimated by

$$R_{thcs} = \frac{L}{A_m \cdot k_{th}} + R_{ct} + R_{ts}\,, \tag{5.1.5}$$

where k_{th} is the thermal conductivity of the thermal interface material, L is the thickness of TIM, A_m is the area of TIM's layer, R_{ct} and R_{ts} are contact resistances of the TIM at the boundary with the two surfaces.

In addition to traditional TIMs, alternatives, such as thermally conductive adhesives, polymer solder hybrids, and metal composites are increasing in use. Typical properties of different TIM solutions are presented in Figure 5.2. However, TIMs are still a bottleneck in many traditional thermal management systems, since thermally induced stresses that arise from differences in the coefficient of the thermal expansion of the various materials used can result in thermal grease pump-out or dry-out [128], causing a significant deterioration of thermal performance of the TIM. This barrier can be eliminated by embedding

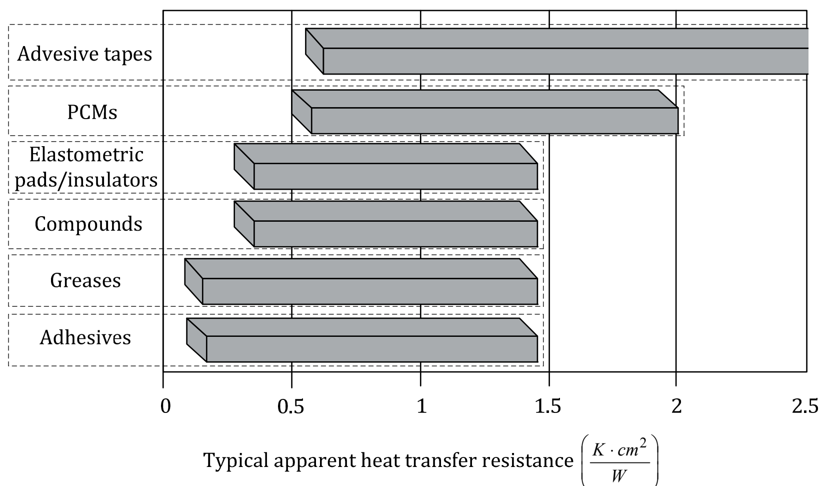


Figure 5.2 Comparison of typical characteristics of different TIMs

the baseplate of the module with the cold plate with either macro- or microchannel structure. In this case coolant flow is in the direct contact with the baseplate. Investigations [129] show that this approach has the capability of reducing the thermal resistance between the semiconductor chip junction and the ambient by about 60%. However, it requires modification of the IGBT package. Therefore, such techniques are more expensive than standard module assembly configurations.

If a series connection of semiconductors is necessary, the most suitable way is to stack the devices on top of each other, as it is well known from press-pack thyristors and diodes. This type of housing offers several advantages compared to modules, like a higher thermal and power cycling capability, easier series connection and explosion-free failure mode. In addition to thyristors, IGBTs in press-pack housings are commercially available as well. These modules have essentially increased current capabilities (Table 5.1) and are designed to replace GTO thyristors in pulse power industrial and transportation applications.

The most widespread technology involving liquid to vapour phase change is heat pipe assisted cooling systems. The heat pipe is a passive system that combines the advantages of both phase change and thermal conductivity to achieve greatly increased heat transfer properties (5-200 kW/m·K) in comparison to solid metals (0.25-1.5 kW/m·K). Since heat pipes can serve only as heat conductors, they are integrated into other heatsink technologies to further increase their thermal efficiency. The modern heat pipe assisted forced

Table 5.1 Nominal current capability of IGBTs in different housings

Collector-emitter voltage	Module (ABB)	Press-pack (Westcode)
1.7 kV	2.4 kA	2.5 kA (in development)
2.5 kV	1.2 kA	2.25 kA
4.5 V	1.2 kA	2.4 kA

air cooling solutions designed by Thermacore™ dissipating 6 kW of heat while maintaining more uniform temperature distribution along the mounting plate, occupying 27% less volume and consuming less air flow volume than traditional extruded heatsinks [130]. Another alternative for improving heatsink performance is to use flat heat pipes or heat chambers applied on the basis of the heatsink to provide more uniform temperature distribution along the surface.

Further improvements in the performance can be achieved by active two-phase cooling loops involving boiling. The evaporative coolant takes away heat losses by the use of latent heat when a liquid turns to vapour. Cooling can be direct (immersion, using dielectric fluids) or indirect (water containing liquids could be used) and can involve pool boiling, flow boiling, and jet impingement boiling. These cooling solutions offer impressive results [133]; however, such systems experience a significant effect of module load cycles, ambient conditions and component orientation on the performance. Aside from heat pipe-based cooling systems, two-phase cooling is not typically used for cooling power electronics at present.

Generalisations

An optimum power electronic system design requires many factors, such as size, noise, complexity, robustness, cost, and maintenance requirements, to be evaluated. Intelligent power management is required to achieve the desired result. As a result of increased heat dissipation from electronic devices, alternative methods of cooling, such as liquid cooling, are becoming more attractive. Considering the wide range of available cooling solutions, the following conclusions can be made [125]:

- forced air cooling is generally the best option for <1 MW converters;
- the performance of the natural or forced air systems could be improved by achieving more uniform temperature distribution by the help of integrating heat pipes or heat chambers while maintaining the positive properties of such systems;
- for higher power applications, liquid cooling systems offer a wide range of new possibilities and could considerably improve the performance of the semiconductors;
- despite showing better results, two-phase methods can have unpredictable performance depending on ambient conditions, are costly and harder to implement and control;
- single-phase methods are simpler, more reliable and predictable. From single-phase systems, tube or fin designs are cost-effective, while jet impingement and microchannel show better performance;
- future directions are increased application of liquid cooling systems as well as their further integration with semiconductor devices.

5.2 GaAs and SiC semiconductors

Comparison of performance of different diodes

As it was stated earlier, there is a growing trend towards semiconductors based on alternative or wide band gap materials, since the present semiconductor structures are close to the so-called "Silicon Design Limits". Five power diodes are tested to compare the performance of different semiconductors: two GaAs diodes DULM1506A and DUT1506; two fast recovery Si diodes - 30EPH06 and DHG20I600HA; and the SiC Schottky diode C3D20060D. The diodes are mounted on natural air-cooled heatsink and the diode test circuit used is based on the voltage fed quasi-Z-source inverter (qZSI) topology [132]. The main parameters of the tested diodes are presented in Table 5.2.

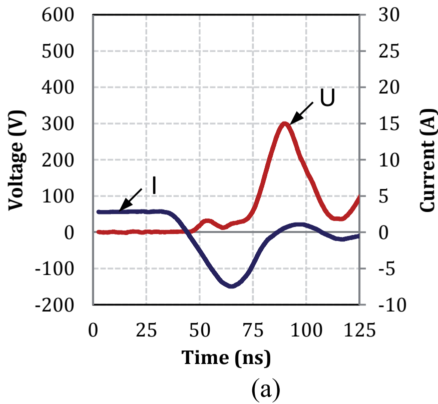
During the operation, the reverse recovery current of the switching-off diode appears across MOSFET during its turn-on transient, increasing its losses. The number of tests made with DULM1506A diode was limited, since the current of this diode falls sharply at the end of the reverse recovery period (low snappiness factor). This enables stray circuit inductance to develop dangerous overvoltages across the device during turn-off. Comparing the performance of both GaAs diodes under similar conditions, it is seen that the voltage peak across soft-recovery DUT1506 diode is around 50% lower than in the case of DULM1506A, as shown in Figure 5.3.

According to the performed tests it was observed that the GaAs DUT1506 diode behaves similarly to hyperfast Si diodes during the turn-off. The maximum reverse current of the SiC diode was 2…3 times lower than that of other diodes tested. This drastic reduction is due to the SiC diode only having to dissipate a small reverse recovery charge, which happens while the diode voltage is low. This charge in the SiC is extremely low and is the result of junction capacitance, not the stored charge [133].

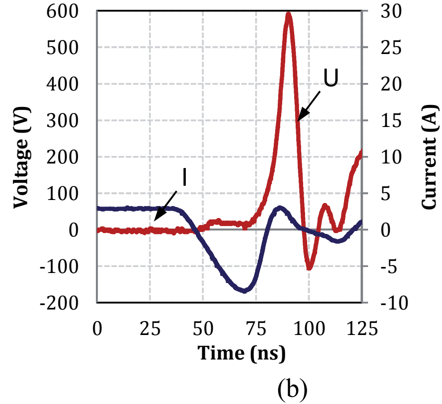
As a result of the comparison, the current waveforms of diodes operating with a range of duty cycles were plotted on graphs shown in Figure 5.4. The reverse-recovery time increases with the increase in *D* for Si diodes, whereas for GaAs diodes, this time is generally independent of the *D* and remains at 43 ns.

Table 5.2 General parameters of the tested diodes at junction temperature of 175ºC.

Diode	Blocking voltage, V	$U_{F(MAX)}$, V	$I_{F(AVG)}$, A	t_{rec}, ns
C3D20060D	600	2.4	20	0
30EPH06		1.75	30	28
DHG 20 I 600 HA		2.2	20	40
DULM1506A		1.5	15	30
DUT1506		2.2	15	65

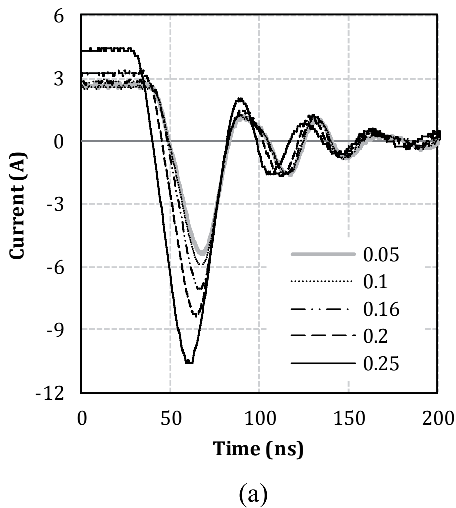


(a)

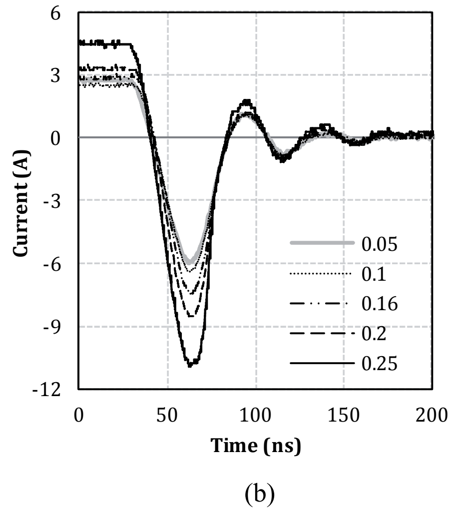


(b)

Figure 5.3 Turn-off waveforms of GaAs diodes (D=0.16 and f_{sw}=60kHz): DUT1506 (a) and DULM1506A (b)



(a)



(b)

Figure 5.4 Reverse recovery current at different MOSFET duty cycles (f_{sw}=60 kHz): Si diode 30EPH06 (a) and GaAs diode DUT1506 (b)

Generalisations

Experimental results show that at low temperatures of operation, GaAs diodes seem to be a viable alternative to hyperfast Si ones. With the increase in T_j the implementation of GaAs diodes is estimated to be more beneficial in terms of reverse-recovery characteristics.

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List of authors' publications directly connected to the topic of dissertation (copies shown in Appendix)

[PAPER-I] **Blinov, A.**; Jalakas, T.; Vinnikov, D.; Janson, K.; "Switch-Off Behaviour of 6.5 kV IGBT Modules in Two-Level Voltage Source Inverter", Scientific Journal of Riga Techical University: Power and Electrical Engineering, pp. 121-126, 2010.

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[PAPER-III] **Blinov, A.**; Jalakas, T.; Vinnikov, D.; Laugis, J.; "Analysis of Switching Properties of Different High Voltage IGBTs Operating Under Hard-Switching Conditions", in Proceedings of the IEEE 12th Biennial Baltic Electronics Conference, pp. 323-326 October 4-6, 2010.

[PAPER-IV] **Blinov, A.**; Vinnikov, D.; Ivakhno, V.; "Study of performance improvement methods for 6.5 kV IGBT based two-level half-bridge converters", Технічна електродинаміка, pp. 56-62, 2011.

[PAPER-V] **Blinov, A.**; Ivakhno, V.; Zamaruev, V.; Vinnikov, D.; Husev, O. "A Novel High-Voltage Half-Bridge Converter with Phase-Shifted Active Rectifier", IEEE International Conference on Industrial technology, ICIT'2012, pp. 967-970, 19-21 March 2012.

[PAPER-VI] **Blinov, A.**; Vinnikov, D.; Ivakhno, V. (2011). "Energy-Efficient High-Voltage Switch Based on Parallel Connection of IGBT and IGCT", 7th IEEE Conference-Workshop Compatibility and Power Electronics, CPE'11, pp. 360-364, 2011.

Abstract

Research of Switching Properties and Performance Improvement Methods of High-Voltage IGBT based DC/DC Converters

High reliability, reduced price and improved power capabilities of modern power semiconductors compared to those two decades ago have made power electronic converters feasible in a wide range of areas, such as residential, telecommunication, traction, industrial, aerospace applications.

The topologies used in high-power conversion applications are mainly determined by the available ratings of the power semiconductor devices. With the emergence of modern high-voltage semiconductors, like insulated gate bipolar transistors, simple and robust topologies with a low number of semiconductor switches, became an attractive alternative to the complex systems implemented previously. Still, much is left to be desired in the characteristics of these semiconductor devices. One of the major challenges is related to rather high power losses, since relatively high price of high-voltage components enforces higher frequencies of operation to be used for smaller passive topology components. Associated efficiency, thermal management and power density limitations impose many difficult, multidisciplinary tasks and a compromise has to be found in order to obtain an optimal design. Therefore, investigation of the methods that allow losses in semiconductor elements to be reduced is of major importance.

This PhD research presents an overview of the state-of-the-art high-voltage IGBT technology. Further, switching transients and power losses are analysed in order to estimate maximum operating frequency of high-voltage semiconductors operating in a converter case study. According to the performed analysis, different methods for improvements in the performance of the converter are proposed and evaluated. One of the proposed solutions is a converter controlled by an active rectifier with a novel control algorithm. It allows an operation frequency increase up to a factor of 2.5 in comparison to a reference converter, resulting in associated reduction of passive topology components. The analysis, methods and results obtained during the PhD research are applicable not only to the case study converter, but could be beneficial in other power electronic applications as well.

Kokkvõtte

Kõrgepingelistel IGBT transistoridel põhinevate alalispingemuundurite lülitusomaduste ja jõudluse suurendamise meetodite uurimine

Tänapäevaste pooljuhtseadeldiste kõrge kasutegur, madal hind ja parendatud väljundvõimsus on muutnud jõuelektroonilised muundurid majanduslikult tasuvaks sellisel laial kasutusalal nagu koduseadmed, telekommunikatsioon, transport, tööstus, lennundus jne. Suure võimsusega muundurseadmetes kasutatavad skeemilahendused on enamikul juhtudel määratud jõupooljuhtlülitite näitajatega. Moodsate kõrgepingeliste jõupooljuhtlülitite nagu isoleeritud paisuga bipolaarsete transistoride kasutuselevõtuga muutusid lihtsad ja robustsed, väheste lülitatavate elementidega skeemilahendused atraktiivseks alternatiiviks seni kasutatavatele keerulistele skeemitopoloogiatele. Kirjeldatavate uute jõupooljuhtlülitite juures on veel palju uurida. Üks nende põhiprobleemidest on seotud suure kaovõimsusega suure lülitussageduse korral. Suur lülitussagedus on vajalik skeemides kasutatavate passiivelementide mõõtmete vähendamiseks. Kaovõimsuse hajutamine, jahutusprobleemid ja võimsustiheduse tõstmine on keerulised multidistsiplinaarsed probleemid, mis eeldavad mitmete kompromisside tegemist saavutamaks optimaalset lahendust. Seega on väga oluline uurida võimalusi kadude vähendamiseks jõupooljuhtseadeldistes.

Antud doktoritöö annab ülevaate kaasaegsest kõrgepingeliste isoleeritud paisuga bipolaarsete transistoride tehnoloogiast. Töös on uuritud ka antud pooljuhtlülitite lülitusprotsesse ning lülitussageduste piirväärtusi prototüüpmuunduri näitel. Analüüsi tulemuste põhjal on välja pakutud mitmeid erinevaid jõudluse suurendamise võimalusi. Üheks pakutud rakenduseks on uudse juhtalgoritmiga aktiivalaldi, mis võimaldab tõsta lülitussagedust kuni 2,5 korda võrreldes seniste tehniliste lahendustega. Kõrgem lülitussagedus võimaldab omakorda tunduvalt vähendada kõigi seadmes kasutatavate passiivkomponentide mõõtmeid. Doktoritöös väljatoodud analüüsimeetodid ja katseliselt saadud tulemused on kasutatavad mitte ainult töös kirjeldatud seadmega, vaid on rakendatavad ka paljude teiste jõuelektroonikaseadmete väljatöötamisel.

Elulookirjeldus

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    - Lep11101 "Raudteeveeremi abitoitemuunduri EL-21 tootearendus"
    - AR10126 "Energiasüsteemi talitluse optimeerimine muutuv-koormuste tasakaalustamiseks"
    - BF137 "Intelligentse transformaatori kontseptsiooni väljatöötamine ning eksperimentaalne uuring laboratoorse katseseadme abil"

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01.01.2011 - 30.06.2011	Tallinn University of Technology, Department of electrical drives and power electronics	Researcher
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   - ETF7425 “Research of Dynamic Performance of High-Voltage IGBTs”
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   Andrei Blinov, Master's Degree, 2008, (sup) Dmitri Vinnikov, Cooling Methods For High-Voltage IGBTs, Tallinn University of Technology , Faculty of Power Engineering, Department of Electrical Drives and Power Electronics, Chair of Electrical Drivers and Electrical Supply.

9. Main areas of scientific work / Current research topics
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   - Energetic Research(Cooling methods of high-voltage IGBTs)

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    - SF0140016s11 “New Converter Topologies and Control Methods for Electronic Power Distribution Networks”
    - Lep11101 “Product development of rolling stock auxiliary power converter EL-21”
    - AR10126 “Optimization of the functioning of the Energy System to balance changeable loads”
    - BF137 “Development and Experimental validation of conceptual solution of the Intelligent Transformer”

Appendix

[PAPER-I] **Blinov, A.**; Jalakas, T.; Vinnikov, D.; Janson, K.; "Switch-Off Behaviour of 6.5 kV IGBT Modules in Two-Level Voltage Source Inverter", Scientific Journal of Riga Techical University: Power and Electrical Engineering, pp. 121-126, 2010.

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Switch-Off Behaviour of 6.5 kV IGBT Modules in Two-Level Voltage Source Inverter

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***Abstract* – This paper presents an analysis of the switch-off process of 6.5 kV/200 A IGBT modules in a two-level half-bridge voltage source inverter. During experiments, it was stated that real switching process is far from ideal switch-off since parasitic inductance and capacitance in the circuit cause voltage spikes and high frequency oscillations during transition processes. Operation states of the inverter are described and analyzed. Experimental and simulation results are compared, the main transients are analyzed and mathematically expressed and possible problems and solutions are discussed.**

***Keywords* – Pulse width modulated power converters, insulated gate bipolar transistor, freewheeling state, oscillations**

I. Introduction

Recent advancements in power electronic technologies have made further optimization possibilities in high-voltage high-power converters available. The introduction of 6.5 kV IGBTs has enabled simple and reliable two-level half-bridge voltage-source inverter (VSI) topologies to be implemented for the rolling stock auxiliary power units. Investigations have shown that an experimental converter based on very simple half-bridge topology with two Infineon 200 A/6.5 kV IGBTs (FZ200R65KF1) is capable of providing required performance within the whole range of rolling stock supply voltage of 2.2…4.0 kV and a wide power range – 10…70 kW [1]. Such inverters (Fig. 1, Table I) are very simple in control and protection, have reduced component count and provide good reliability. Converters with described topology and switching elements are perfectly suitable for use in isolated DC/DC rolling stock converters as front-end converters of auxiliary power supplies.

Main problems of this topology are high power losses in semiconductors due to hard switching and consequently, limited switching frequency because of thermal issues. This imposes increased requirements on passive components of the converter. These downsides are related to the common peculiarity of half-bridge topologies – voltage spikes after transistor turn-off (Fig. 2). The voltage spikes are followed by oscillations, obviously caused by presence parasitic capacitive and inductive circuit elements. This paper describes the reasons of these processes in high voltage (≥2 kV) high power (≥20 kW) half-bridge inverters with modified sine wave output operation as well as their effect on the overall performance of the converter.

II. Operation of the Two-Level Half-Bridge Inverter

Two equal capacitors C_1 and C_2 are connected in series across the DC input voltage source, providing a constant potential of the one-half U_{IN} at their junction. Two-level half-bridge inverter has two operating states: active states (*A1, A2*) and a freewheeling state (*FRW*). During active states, the two transistors *TT* (top switch) and *TB* (bottom switch) are switched alternately, providing positive and negative square-wave impulses with the amplitude of $U_{IN}/2$ on the isolation transformer *TX* primary winding (Table II). Even a short-time simultaneous opening of the two transistors will result in

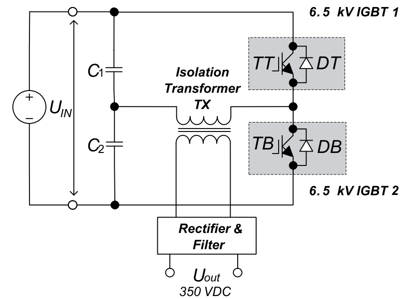

Fig. 1 Two-level half-bridge 6.5 kV IGBT based converter

TABLE I
MAIN PARAMETERS OF THE HALF-BRIDGE CONVERTER

Parameter	Symbol	Value
Maximum input voltage, V	$U_{IN\,(max)}$	4000
Minimum input voltage, V	$U_{IN\,(min)}$	2200
Nominal input voltage, V	$U_{IN\,(nom)}$	3000
Output power, W	P_{out}	50000
Nominal output voltage, V	U_{out}	350
Switching frequency, Hz	f_{SW}	1000

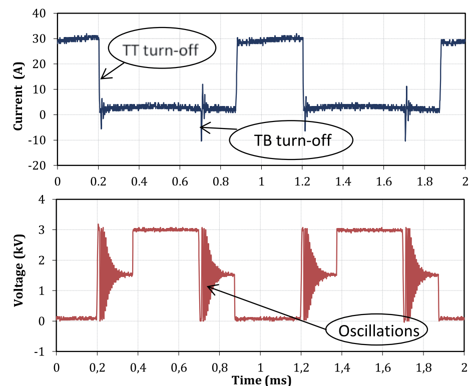

Fig. 2. *TT* IGBT collector-emitter current (top) and voltage (bottom) waveforms during the test of the prototype (U_{IN}=3000 V; f_{SW}=1 kHz, D=0.32, 46 % load)

TABLE II

SWITCHING STATES OF A TWO-LEVEL INVERTER

Inverter state	Transistor state		Output Voltage
	TT	*TB*	
A1	ON	OFF	$- U_{IN}/2$
FRW	OFF	OFF	0
A2	OFF	ON	$+ U_{IN}/2$

TABLE III

PARASITIC AND LOW-SIGNAL CAPACITANCES OF THE IGBT

Capacitances	Designation
C_{GE}	Gate-emitter capacitance
C_{CE}	Collector-emitter capacitance
C_{GC}	Gate-collector capacitance (Miller capacitance)
$C_{IES} = C_{GE} + C_{GC}$	Input capacitance
$C_{RES} = C_{GC}$	Reverse transfer capacitance
$C_{OES} = C_{GC} + C_{CE}$	Output capacitance

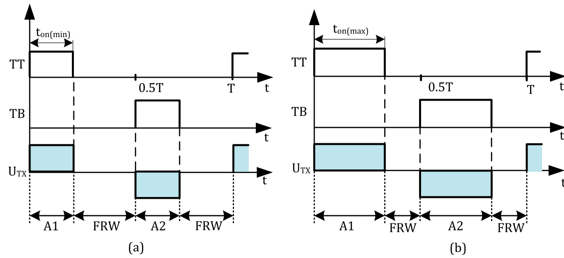

Fig. 3. Switching waveform of a two-level half-bridge DC/DC converter: maximal input voltage (a) and minimal input voltage (b)

short-circuit, therefore the maximum on-state time t_{on} of the transistor control pulse should not exceed 80% of the half period (Fig. 3). This implements a freewheeling state when both transistors are off. During this state, the output voltage is zero [2].

III GENERALIZED EQUIVALENT CIRCUITS OF A TWO-LEVEL HALF-BRIDGE CONVERTER

In a real inverter, every detail has stray inductance, resistance and capacitance. These parasitic components have an influence on the performance and if not considered, could lead to dangerous overvoltages, EMI problems and damage of the inverter. Switch-off process is most influenced by the stray inductance of the isolation transformer and parasitic inductance of the wiring as well as the junction capacitances of HV IGBT modules.

A. Structure of the IGBT module

The switching behaviour (turn-on and turn-off) of an IGBT module is generally determined by its structural, internal capacitances (charges) and the internal and outer (gate drive) resistances (Fig. 4, Table III).

The gate resistor R_G is limiting the magnitude of the gate current I_G, which dictates what the time is needed to charge/discharge IGBT input capacitance C_{IES} during turn-on and turn-off. Generally, a turn-off resistor must have a higher value than a turn-on one.

TABLE IV

DATASHEET VALUES OF INFINEON FZ200R65KF1 MODULES

Parameter	Symbol	Value
DC collector current, A	I_C	200
Collector-emitter blocking voltage, V	I_{CES}	6500
Maximum junction temperature, ºC	Tj_{max}	125
Input capacitance, nF	C_{IES}	28
Turn-on delay time, µs	$t_{d(on)}$	0.75
Rise time, µs	t_r	0.40
Turn-off delay time, µs	$t_{d(off)}$	6
Turn-off fall time, µs	t_f	0.5
Diode peak reverse-recovery current, A	I_{rm}	270
Typical turn-on gate resistance, Ω	$R_{G,on}$	13
Typical turn-off gate resistance, Ω	$R_{G,off}$	75

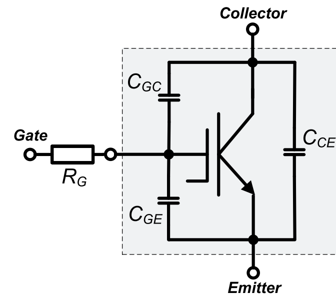

Fig. 4. Equivalent intrinsic capacitances of the IGBT

In high frequency inverters, overvoltage caused by the energy stored in the stray inductance of a transformer could cause a high voltage spike on the IGBT. However, this process does not occur in the investigated inverter since the nominal switching frequency f_{SW} is only 1 kHz and freewheeling diode starts to conduct before noticeable overvoltage spike occurs. It is evident that the increased gate resistance slows the IGBT switching process, limiting overvoltage, on the other hand, increasing switching losses. Reference values of Infineon FZ200R65KF1 modules are presented in Table IV [3][4]. IGBT parasitic capacitance values are dependent on the transistor module type and not presented in the datasheet of FZ200R65KF1, complicating further calculations.

B. Equivalent parameters of the converter

Based on the parameters, most influential to the active and freewheeling states, the simplified equivalent circuits for the considered half-bridge converter were elaborated.

The value of the equivalent load resistance can be obtained from [5]:

$$R_L = \frac{U^2_{Prms}}{P_{Tr}}, \quad (1)$$

where U_{Prms} is the transformer primary rms voltage and P_{Tr} is the power of the isolation transformer (neglecting losses).

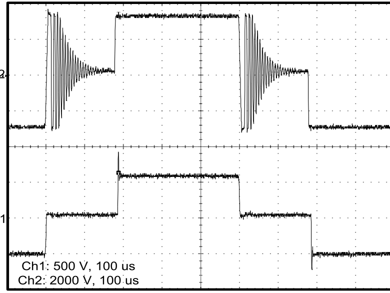

Fig. 5. Isolation transformer primary (top) and secondary voltage (bottom) waveforms during the test of the prototype (U_{IN}=3000 V; f_{SW}=1 kHz, D=0.32, 46 % load)

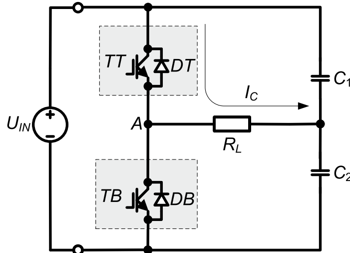

Fig. 6. Active state of the *TT* transistor in the two-level half-bridge converter

The transformer primary rms voltage is proportional to the converter input voltage:

$$U_{Prms} = \frac{U_{IN}}{2} \cdot \sqrt{2 \cdot D}\ , \qquad (2)$$

As Fig. 5 reveals, the parasitic oscillations occur only on transformer primary winding, hence only primary winding parameters are considered. Freewheeling state model includes a third-order oscillatory circuit. The total parasitic inductance of the equivalent circuit is described by:

$$L_E = \sum_{i=1}^{n} L_i\ , \qquad (3)$$

where $L_1 ... L_n$ is the inductance of the inverter circuit elements including bus, wiring and contact parasitic inductance, as well as the equivalent stray inductance of the transformer primary. The magnitude of the circuit impedance is:

$$Z_{Tr_p} = \sqrt{R_E^{\,2} + \left(2 \cdot \pi \cdot f_{osc} \cdot L_E - 1/(2 \cdot \pi \cdot f_{osc} \cdot C_{Tr_p})\right)^2} \qquad (4)$$

where f_{osc} is the frequency of parasitic oscillations, R_E is the equivalent active resistance of inverter busbar, wiring and transformer primary winding. Parasitic capacitive component $C_{Tr\text{-}p}$ is generally represented by effective distributed capacitances of the primary winding.

IV Analysis of Freewheeling State of the Two-Level Half-Bridge Converter

Two-level half-bridge inverters have two basic operating states: active state and freewheeling state. During the active

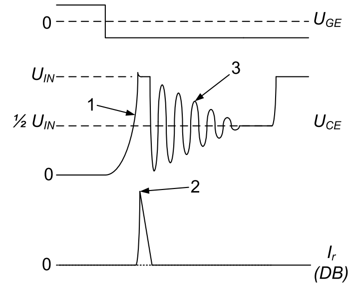

Fig. 7. Generalized representation of the turn-off process of *TT* IGBT. U_{GE} is the gate-emitter voltage of transistor (control signal), U_{CE} is the collector-emitter voltage, I_r is the current impulse through *DB*, events 1-3 are marked

state either *TT* or *TB* is turned on. During the active state the current I_C flows through the top or bottom transistor, input capacitors C_1 and C_2 and the primary and secondary windings of the isolation transformer. The active state of the *TT* transistor is presented in Fig. 6. The freewheeling state takes place when both switches are off.

At the end of the active state, a negative gate control voltage is applied to the *TT* transistor, closing it and starting the freewheeling state (Fig. 7) [6]. The following events can be distinguished:

1. Transistor internal capacitances begin to discharge and the collector-emitter voltage $U_{CE}(t)$ of the IGBT begins to rise. As the current I_C through the transistor decreases, the energy stored in the stray inductance of the power circuit develops a negative voltage potential at point A calculated by:

$$U_{Stray} = L_E \cdot \frac{dI_C}{dt}\ , \qquad (5)$$

where L_E is the stray inductance of the power circuit, dI_C/dt is the rate-of-fall of the transformer primary current, Fig. 8(1). This voltage potential is added to the collector-emitter voltage after transistor turn-off:

$$U_{CEpeak} = U_{IN} + U_{Stray}\,. \qquad (6)$$

2. After the voltage potential at point A becomes lower than the ground potential of U_{IN}, the current I_r begins to flow through the freewheeling diode *DB* (Fig. 8). The maximal reverse current $I_{r(peak)}$ through the diode at the instant of turn-off is equal to the *TT* collector current $I_{C(max)}$ before turn-off. The current then decays exponentially when $I_r(t) \geq 0$ according to [7]:

$$I_{C(max)} = I_{r(peak)} = \frac{P_{Tr}}{U_{IN} \cdot D} = \frac{U_{IN}}{2 \cdot R_L} \qquad (7)$$

$$I_r(t) = I_{r(peak)} \cdot e^{\frac{-R_E \cdot t}{L_E}} - \frac{U_{IN}}{2 \cdot R_E} \cdot \left(1 - e^{\frac{-R_E \cdot t}{L_E}}\right) = \left(I_{r(peak)} + \frac{U_{IN}}{2 \cdot R_E}\right) \cdot e^{\frac{-R_E \cdot t}{L_E}} - \frac{U_{IN}}{2 \cdot R_E}. \quad (8)$$

The current follows this equation until it equals zero.

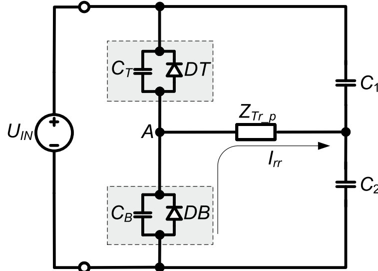

Fig. 8. Reverse current of the *DB* diode after *TT* transistor switch-off

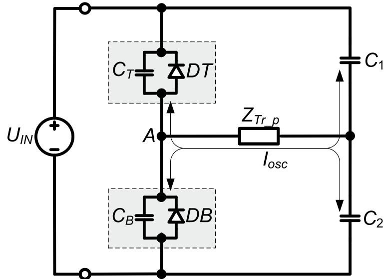

Fig. 9. RLC circuit causing the oscillations after IGBT switch-off

The current then remains at zero until the next diode conduction. The duration t_{Ir} of decaying reverse current is described by equation:

$$t_{I_r} = \frac{L_E}{R_E}\left[\ln\left(I_{r(peak)} + \frac{U_{IN}}{2 \cdot R_E}\right) - \ln\left(\frac{U_{IN}}{2 \cdot R_E}\right)\right]. \quad (9)$$

3. After depletion of the energy stored in stray inductance, the reverse current through *DB* stops. The output capacitances of IGBT modules C_T and C_B together with the stray inductance L_E and equivalent impedance of circuit Z_{Tr-p} form an oscillating RLC circuit (Fig. 9). C_B and C_T begin to charge and discharge. Voltage and current in this RLC circuit oscillates until being damped by R_E and the voltage potential of point A becomes equal to $1/2\ U_{IN}$.

V Elaboration of the simulation model

Determination of the parasitic elements causing oscillations requires a simulation model to be elaborated. The oscillation frequency of the damped circuit f_{osc} is [8]

$$f_{osc} = \frac{1}{T_{osc}} = \frac{\omega}{2 \cdot \pi} = \frac{\sqrt{{\omega_0}^2 - \delta^2}}{2 \cdot \pi}, \quad (10)$$

where undamped resonance frequency $\omega_0 = 1/\sqrt{L_E \cdot C_E}$, attenuation $\delta = R_{HF}/(2 \cdot L_E)$, R_{HF} is equivalent high-frequency resistance and C_E is generally represented by the sum of equal paralleled IGBT parasitic capacitances C_T and C_B.

TABLE V
Values of simulation parameters

Parameter	Symbol	Value
Input voltage, V	U_{IN}	2200…4000
Inverter input capacitances, μF	C_1, C_2	300
IGBT parasitic capacitances, pF	C_T, C_B	450
Equivalent impedance at 310 kHz, Ω	Z_{Tr_p}	81.8
Switch duty cycle	D	0.22…0.4
Switching frequency, kHz	f_{SW}	1…2

According to the measurements, the oscillation frequency is 310 kHz (Fig.7). Oscillation is described by the oscillatory circuit quality factor Q:

$$Q = \frac{2 \cdot \pi \cdot f_{osc} \cdot E_s}{P_{osc}} = \frac{1}{R_{HF}} \cdot \sqrt{\frac{L_E}{C_E}} = \frac{\pi}{\ln(U_n / U_{(n+1)})}, \quad (11)$$

where U_n and U_{n+1} are amplitude values of voltage oscillations separated by the time interval of T_{osc}. The equivalent stray inductance L_E can be obtained by

$$L_E = \frac{R_{HF}}{2 \cdot \ln(U_n / U_{n+1)}) \cdot f_{osc}}. \quad (12)$$

Equivalent module capacitances can be obtained from the oscillation frequency equation

$$C_T = C_B = \frac{1}{2} \cdot \left(\frac{1}{L_E \cdot (\omega^2 + \delta^2)}\right). \quad (13)$$

The voltage oscillations across transistor after reverse current impulse follow the equation [9]:

$$U_{osc} = \frac{U_{IN} \cdot \omega_0}{2 \cdot \omega} \cdot \cos\left(\omega \cdot t - \arctan\frac{\delta}{\omega}\right) \cdot e^{-\delta \cdot t}. \quad (14)$$

and oscillating current is described by:

$$I_{osc} = \frac{U_{IN}}{2 \cdot \omega \cdot L_E} \cdot \sin \omega \cdot t \cdot e^{-\delta \cdot t}. \quad (15)$$

VI Simulation results

According to the generalized equivalent circuit, a simulation model is created using PSIM software. The simulation model elaborated has the same configuration as the

test prototype in Fig. 1 and includes the values presented in Table V.

Obtained simulation results were compared with laboratory measurements of the converter prototype (Fig. 11). Further, inverter performance was simulated under different operation conditions (Figs. 11-12). The presence of the oscillations showed no significant impact on the performance in the simulations as well as during the laboratory tests. The current amplitude during oscillations remained relatively low; hence, the energy of the oscillations is relatively low as well.

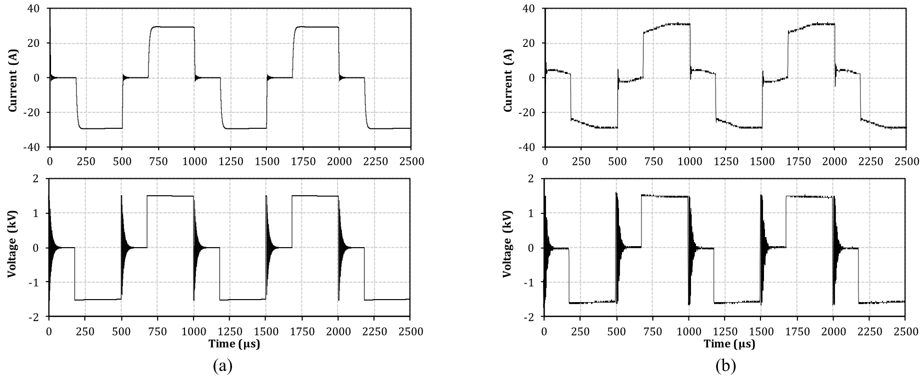

Fig. 10. Simulated (a) and experimental (b) transformer primary current (top) and voltage (bottom) (U_{in}=3000V; f= 1 kHz; D=0.32; R_L=48.4 Ohm)

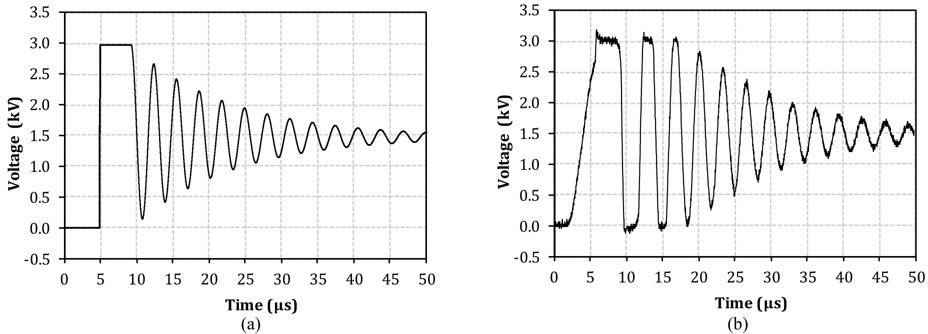

Fig.11. Simulated (a) and experimental (b) *TT* IGBT collector-emitter voltage (U_{IN}=3000 V; f_{SW}=1 kHz, D=0.32; R_E=48.4 Ohm)

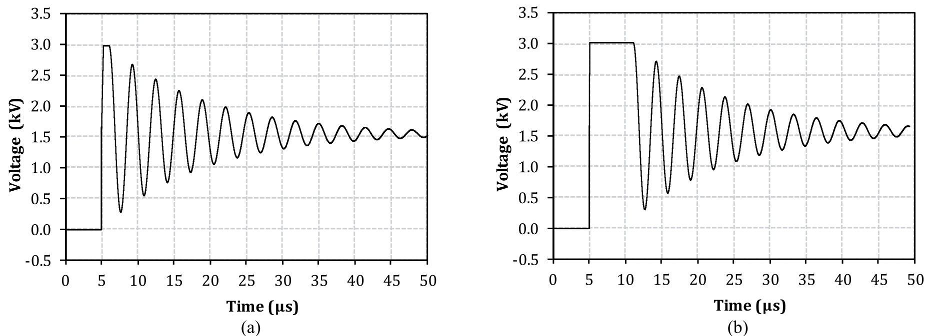

Fig.12. Simulated *TT* IGBT collector-emitter voltage: U_{in}=3000V; f= 1 kHz; D=0.32; R_L=288 Ohm(10% load) (a); R_L=28.8 Ohm (100% load) (b)

VII. Conclusions

During the laboratory test of the prototype, as well as in the computer simulations, the frequency of oscillations was found independent of the input voltage or the switching frequency of transistors and remained at approximately 310 kHz. The amplitude value of oscillations is proportional to the input voltage. The value of the reverse current impulse depends on the converter output power, i.e. the more energy is stored in the parasitic inductance, the more reverse current is required to deplete it. On the contrary, under light load operation, the duration of reverse impulse is decreased. The simplified simulation model showed similar results compared to the values obtained during the laboratory test of the converter prototype. Although not entirely precise, the simulation model gives an adequate estimation of the processes that occurred during the laboratory tests.

High stray inductance of the isolation transformer results in higher losses as well as voltage and current oscillations after switch-off. Although the frequency of those oscillations is not high enough to generate strong radiated EMI, it can cause some problems with conducted EMI in the contact line. Due to the required high isolation voltage of the isolation transformer, the high stray inductance is hard to avoid, moreover the capacitance of HV IGBT modules cannot be avoided. In the case of the considered high-voltage inverter, these parasitic effects are not dangerous to HV IGBT modules, neither are they dangerous to other circuit elements since they do not create noticeable overvoltage. On the other hand, the losses are increased, thus the nominal switching frequency is limited at 1 kHz. Generally, the ways to reduce the impact of parasitic effects are dissipative snubber circuits and low inductivity busbar system. Due to high-voltage supply, implementation of snubber circuits is complicated and is unlikely to significantly improve the performance of the converter.

ACKNOWLEDGEMENT

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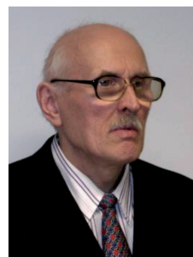

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Loss Calculation Methods of Half-Bridge Square-Wave Inverters

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Introduction

The insulated gate bipolar transistors (IGBTs) are widely used in many modern fields of power electronics that are related to power conversion, transmission and distribution. Today IGBTs with blocking voltages up to 6.5 kV are commercially available, allowing simple and robust two-level topologies to be used in applications with nominal DC voltages up to 3.6 kV without the need of series connection of several IGBTs. The other advantages of IGBTs are easy driving and snubberless operation. On the other hand, the high-voltage IGBTs have limited current capability and high power losses, resulting in limited switching performance due to thermal issues. Therefore, thermal management became one of the most important aspects in the development of high-voltage IGBT converters. The accurate estimation of power losses is an important step in thermal management system design [1–3]. A number of calculation methods have been proposed. One of the approaches is based on the switching functions or coefficients obtained through measurements to guide the simulation during switching transients [4, 5]. However, this method requires a number of parameters to be extracted from the test waveforms. Another approach is based on the use of simple functions derived for losses based on typical switching waveforms [6, 7]. This method was extended in [1, 8] by deriving a set of formulae for switching losses based on the predicted current and voltage waveforms of the device. In this method the predicted waveforms conform to the physics of the switching process and take into account the dependency of the switching losses on various factors such as the switching voltage, switching current, stray inductance and the reverse recovery process of the freewheeling diode [8]. Another advantage is that it requires a smaller number of parameters from the test waveforms.

If a power electronic system prototype is unavailable, the losses can be estimated by the help of the datasheet parameters of the devices using linear interpolation of characteristic curves [9, 10]. This approach is generally limited in accuracy, however could be considered as a first approximation.

This paper will focus on the improvement of the calculation methods using manufacturers' datasheet parameters of semiconductors for inverters with the square-wave output [11]. The second part presents an analytical method of estimating losses, including the losses caused by parasitic components of the circuit.

Definitions

The power loss of each switching operation for the given current and voltage waveforms of the IGBT is divided into three sections as illustrated in Fig. 1 [12]. The leakage loss is only a small part of the total loss so that neglecting it the error is usually insignificant. Therefore, the total energy losses during each operating cycle of the IGBT are the sum of the turn-on and turn-off loss, saturated conduction loss as well as the reverse-recovery loss of the integrated freewheeling diode (FWD) [8]

$$E_{tot} = \int I(t) \cdot U(t) \cdot dt \,, \quad (1)$$

where *I(t)* and *U(t)* are transistor current and voltage, respectively.

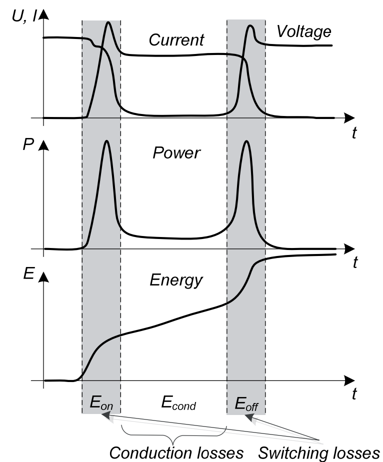

Fig. 1. Three sections of losses

Table 1. Characteristic values of 200 A 6500 V IGBT (FZ200R65KF2)

Parameter	Symbol	Value
Collector-emitter voltage	U_{CES}	6500 V
DC collector current	$I_{C(nom)}$	200 A
Collector-emitter saturation voltage	$U_{CE(sat)}$	5.3 V
Turn-on delay time	$t_{d(on)}$	0.72µs
Rise time	t_r	0.40 µs
Turn-off delay time	$t_{d(off)}$	6.00 µs
Fall time	t_f	0.50 µs
Critical rate of rise of current	dI_r/dt_{cr}	1000 A/µs
Turn-off delay time	$t_{d(off)}$	11 µs
Turn-on energy loss per pulse	E_{on}	1900 mJ
Turn-off energy loss per pulse	E_{off}	1200 mJ
Diode's repetitive peak current	I_{FRM}	400 A
Diode's forward voltage	U_F	3.90 V
Diode's peak reverse-recovery current	I_{RM}	330 A
Reverse-recovery energy	E_{rec}	550 mJ

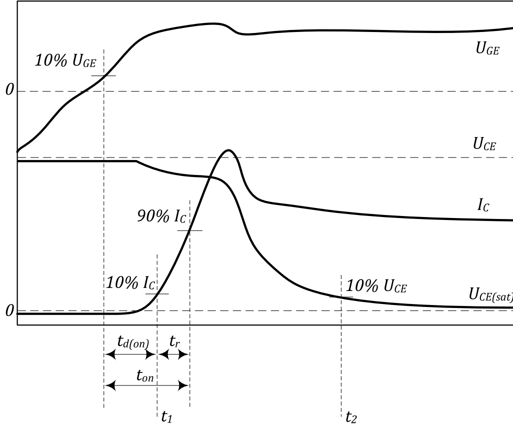

Fig. 2. IGBT switching times and energy defenitions during turn-on

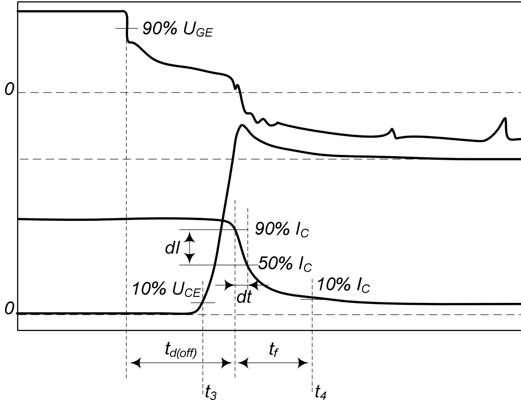

Fig. 3. IGBT switching times and energy defenitions during turn-off

The datasheets of IGBTs contain typical information about switching transients, on-state behaviour and energy losses during a single operation pulse. These characteristics refer to a specific test circuit which simulates a clamped inductive load operating with a specific diode [6]. Typical datasheet values of Infineon 200 A 6.5 kV IGBT module are presented in Table 1.

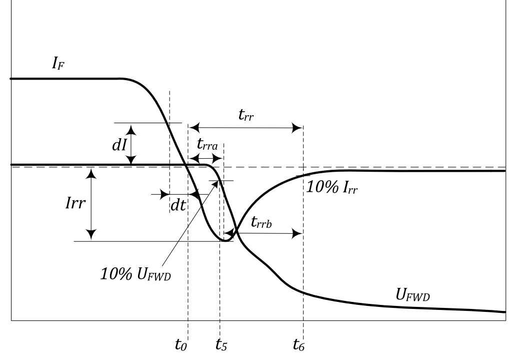

Fig. 4. FWD switching times and energy definitions during reverse-recovery

For high-voltage IGBT modules, the turn-on energy loss E_{on} is generally defined as the integral of the product of the collector current and the collector-emitter voltage over the interval from when the collector current rises above 10% of the test current to when the voltage falls below 10% of the test voltage (Fig. 2). The turn-off energy loss E_{off} is the integral of the product of the collector current and the collector-emitter voltage over the interval starting from when the collector-emitter voltage rises above 10% of the test voltage to when the collector current reaches 10% of the test current (Fig. 3). The diode reverse-recovery energy E_{rec} is the integral of the product of the diode current and voltage over the interval starting from when the voltage across the diode rises above 10% of the test voltage to when the diode reverse current drops to 10% of its peak value (Fig. 4).

Loss calculation method using datasheet parameters

General equations. The on-state voltage drop of the non-punch-through (NPT) IGBT device generally increases with a higher collector current and the junction temperature. Moreover, it could vary from one device to another. The datasheets typically indicate the typical and the maximum values. The maximum values generally refer to the worst case device that the manufacturers consider as qualitative. For example, the 200A 6.5 kV IGBT collector-emitter saturation voltage varies from 5.3 V (typical) to 5.9 V (maximal) for the 200 A collector current at the junction temperature of 125°C. Generally, use of typical values at the maximum junction temperature could be considered reasonably accurate. The conduction losses are estimated by

$$P_{cond} = \frac{1}{T_{sw}} \cdot \int_{0}^{t_{on}} I \cdot U_{CE(sat)}\left(I, T_j, k_{(sat)}\right), \qquad (2)$$

where T_{sw} is the switching period, t_{on} is the on-state time, I is the IGBT current, T_j is the switch junction temperature, $k_{(sat)}$ is the scale factor based on the properties of the device considered.

The switching energy loss of a device is variable due to the device's current, voltage, gate resistance and junction temperature.

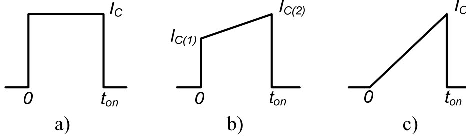

Fig. 5. Typical transistor current waveforms operating in inverters with the square-wave voltage output

Generally, the latter dependency is not indicated in the datasheets, while the energy loss versus current and gate resistance are indicated at the maximum junction temperature. Since the losses increase with increased temperature, it is assumed in the following that the junction temperature will be 125°C as a worst case [9]. In general, the turn-on and turn-off energies are obtained by:

$$E_{on} = \int_{t_1}^{t_2} I \cdot U_{CE} \cdot dt \,, \quad (3)$$

$$E_{off} = \int_{t_3}^{t_4} I \cdot U_{CE} \cdot dt \,. \quad (4)$$

Calculation equations, linear approximation. To achieve fast analytical calculations, the on-state voltage drop can be characterized by a dynamical resistance r_T and a constant voltage drop U_{T0}. The voltage drop across the IGBT with rms collector current is then determined by

$$U_T = U_{T0} + r_T \cdot I_C^{rms} \,, \quad (5)$$

where U_{T0} is the device's threshold voltage, r_T is the device's slope resistance and I_C^{rms} is the transistor RMS collector current.

For inverters with the square-wave output voltage the on-state energy dissipation for typical output current waveforms (Fig. 5) could be obtained by simple equations.

Case A.

$$I(t) = I_C \,. \quad (6)$$

Conduction energy losses for the given pulse length

$$E_{cond} = \left(U_{T0} \cdot I_C + r_T \cdot I_C^2\right) \cdot t_{on} \,. \quad (7)$$

Case B.

$$I(t) = I_{C(1)} + \left(I_{C(2)} - I_{C(1)}\right) \cdot \frac{t}{t_{on}} \,. \quad (8)$$

Conduction energy losses for the given pulse length

$$E_{cond} = \left[\begin{array}{l} U_{T0} \cdot \dfrac{I_{C(1)} + I_{C(2)}}{2} + \\ + \dfrac{1}{3} \cdot r_T \cdot \left(I_{C(1)}^2 + I_{C(1)} \cdot I_{C(2)} + I_{C(2)}^2\right) \end{array} \right] \cdot t_{on} \,. \quad (9)$$

Case C.

$$I(t) = I_C \cdot \frac{t}{t_{on}} \,. \quad (10)$$

Conduction energy losses for the given pulse length

$$E_{cond} = \frac{1}{6} \cdot I_C \cdot t_{on} \cdot \left(3 \cdot U_{T0} + 2 \cdot I_C \cdot r_T\right). \quad (11)$$

The conduction power losses can then be calculated by

$$P_{cond} = f_{sw} \cdot E_{cond} \,. \quad (12)$$

No simple expression can be found for the voltage and current during a switching transient. The datasheet parameters concerning the switching losses can be used in this case. To simplify the analysis for different current levels, the datasheet energy loss curves could be replaced by their linear interpolations using simple equations:

$$E_{on} = A_{on} \cdot I_C + B_{on} \,, \quad (13)$$

$$A_{on} = \frac{\Delta E_{on}}{\Delta I_C} = \frac{E_{on(2)} - E_{on(1)}}{I_{C(2)} - I_{C(1)}} \,, \quad (14)$$

$$B_{on} = E_{on(2)} - A_{on} \cdot I_{C(2)} \,, \quad (15)$$

where $I_{C(1)}$, $I_{C(2)}$ are currents and $E_{on(1)}$, $E_{on(2)}$ corresponding energy loss values taken from the datasheet graphs. The turn-off coefficients A_{off} and B_{off} are calculated in the similar way.

Since the actual operation parameters of semiconductors are in most cases different from the reference circuit, datasheet values should be scaled accordingly. If the gate resistor of a user's gate drive does not have the same value as the gate resistor in the test circuit specified in the datasheet some corrections may be necessary. This can be done with the help of the datasheet using graphs $E_{on}=f(R_G)$ and $E_{off}=f(R_G)$. The scale factor is obtained by the relation between the switching losses with the used-specific gate resistance R_{G-on}^{US} and the one specified in the datasheet R_{G-on}^{DS} [4]

$$k_{(R_{G-on})} = \frac{E_{on}\left(R_{G-on}^{US}\right)}{E_{on}\left(R_{G-on}^{DS}\right)} \,. \quad (16)$$

The turn-off resistor scale factor $k_{(R_{G-off})}$ is calculated in the similar way.

Generally, the switching losses scale almost linearly with U_{CE}, hence the following approximation of the scale factor for the actual commutation voltage could be considered reasonably accurate

$$k_{(U_{CE-on})} = \frac{U_{CE-on}^{US}}{U_{CE}^{DS}} \,, \quad (17)$$

where U_{CE-on}^{US} is DC voltage across the IGBT during the off-state before the beginning of the turn-on transition, U_{CE}^{DS} is the collector-emitter voltage cpecified in the datasheet graphs $E_{on}=f(I_C)$, $E_{off}=f(I_C)$. The scale factor for the actual commutation voltage $k_{(U_{CE-off})}$ during the turn-off is obtained in the similar way

$$k_{(U_{CE-off})} = \frac{U_{CE-off}^{US}}{U_{CE}^{DS}}, \quad (18)$$

where U_{CE-off}^{US} is DC voltage at IGBT after the end of the turn-off transition.

The switching energy losses for typical current waveforms (Fig. 5) can be approximated by the following expressions.

Case A.

$$E_{on} = \left(A_{on} \cdot I_C + B_{on}\right) \cdot k_{R_{G-on}} \cdot k_{U_{CE-on}}, \quad (19)$$

$$E_{off} = \left(A_{off} \cdot I_C + B_{off}\right) \cdot k_{R_{G-off}} \cdot k_{U_{CE-off}}. \quad (20)$$

Case B.

$$E_{on} = \left(A_{on} \cdot I_{C(1)} + B_{on}\right) \cdot k_{R_{G-on}} \cdot k_{U_{CE-on}}, \quad (21)$$

$$E_{off} = \left(A_{off} \cdot I_{C(2)} + B_{off}\right) \cdot k_{R_{G-off}} \cdot k_{U_{CE-off}}. \quad (22)$$

Case C.

$$E_{on} = 0, \quad (23)$$

$$E_{off} = \left(A_{off} \cdot I_C + B_{off}\right) \cdot k_{R_{G-off}} \cdot k_{U_{CE-off}}. \quad (24)$$

Diode reverse-recovery losses. The data available to calculate the diodes' reverse recovery losses differs from one manufacturer to another. Furthermore, these losses depend on the current slope during the transition which in standard VSIs is basically determined by the inductance of the circuit, IGBT *dI/dt* during turn-on and operation temperature [12]. If the reverse-recovery energy in the datasheet is provided only for one operating point, then the scale factor k_{rr} can be calculated according to [13]

$$k_{rr} = \frac{E_{rr}^{DS}}{Q_{rr}^{DS} \cdot U_{CE}^{DS}}, \quad (25)$$

where E_{rr}^{DS}, Q_{rr}^{DS} and U_{CE}^{DS} are revese-recovery energy, reverse-recovery charge and voltage specified in the datasheet, correspondingly.

The reverse-recovery energy can now be approximated as

$$E_{rr} = k_{rr} \cdot Q_{rr}^{US} \cdot U_{CE}^{US} = k_{rr} \cdot \frac{I_{rr} \cdot t_{rr}}{2} \cdot U_{CE}^{US}. \quad (26)$$

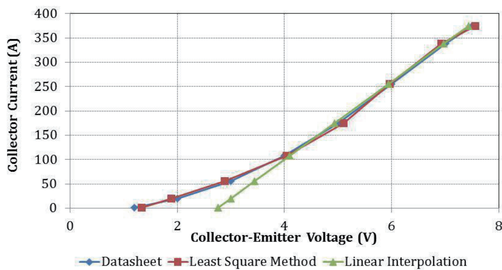

Fig. 6. Collector-emitter saturation voltage comparison with collector current using different interpolation methods

Calculation equations, least square approximation. The drawback of the above presented equations is generally related to the limited accuracy of the linearly interpolated characteristics of $U_{CE}=f(I_C)$, $E_{on}=f(I_C)$ and $E_{off}=f(I_C)$. A better result, especially at lower currents, can be achieved by approximating these curves with the following function

$$f(x) = A \cdot x^3 + B \cdot x^2 + C \cdot x + F. \quad (27)$$

The coefficients A, B, C and F of the proposed function can be estimated from the datasheet curves using the least square method with the help of software, such as SOLVER in EXCEL. The comparison of results obtained with different interpolation methods is shown in Fig. 6.

The conduction losses can then be expressed as

$$P_{cond} = \frac{1}{T_{sw}} \cdot \int_0^{t_{on}} I(t) \cdot U_{CE(sat)}\left(I(t)\right) \cdot dt, \quad (28)$$

where *I(t)* could be expressed according to Eqs. 6, 8 and 10.

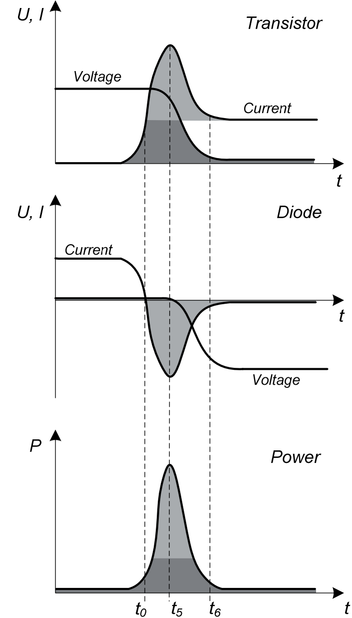

Fig. 7. Typical transistor voltage,current and power waveforms during turn-on

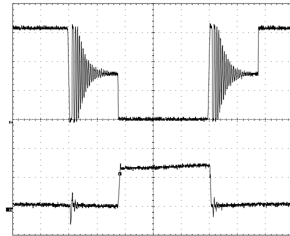

Fig. 8. Experimental waveforms of IGBT collector voltage (top) and current (bottom) during the tests of the inverter prototype (D=0.32), 20 A/div, 50 us/div

Analytical loss estimation method of two-level VSI

The turn-on energy losses indicated in the datasheet of the IGBT typically include the losses caused by the reverse-recovery current of turning-off freewheeling diode (Fig. 7).

No simple expression can be provided for these additional losses, as they depend on a number of factors: turn-on *di/dt*, citruit inductance and diode characteristics. The following equation assumes that the voltage across the diode stays close to zero volts during the interval t_0-t_5, rising to the supply voltage during t_5-t_6 (Fig. 4)

$$E_{on} = U_{CE-on}^{US} \cdot I_C \cdot \left[\left(1+\frac{1}{2}\cdot\frac{I_{rr}}{I_C}\right)\cdot t_{0-5} + \frac{1}{4}\cdot\frac{I_{rr}}{I_C}\cdot t_{5-6}\right] = U_{CE-on}^{US} \cdot \left(I_C \cdot t_{0-5} + Q_{t_{0-5}} + \frac{1}{2}\cdot Q_{t_{5-6}}\right), \quad (29)$$

where I_{rr} is the peak reverse-recovery current.

However, in the square-wave two-level half-bridge converters, the reverse-recovery process of freewheeling diodes is finished during the freewheeling state. Hence, there is no additional current during the turn-on of the IGBT, resulting in lower losses. Due to the leakage induction of the isolation transformer and the parasitic capacitances of HV-IGBT modules there are oscillations after the IGBT turn-off (Fig. 8). The energy stored in the circuit is lost during this process, moreover the IGBT modules seem to sustain additional reverse-recovery losses. This process was studied in [11] and the energy lost during the oscillation period is

$$E_{osc} = \frac{1}{2}\cdot L_E \cdot I_{osc}^2, \quad (30)$$

where L_E is the total parasitic inductance of the circuit, I_{osc} is the peak value of the oscillating current.

The proposed improved approximation of the transistor switching process is shown in Fig. 9. The turn-on energy is calculated by integrating multiplied turn-on voltage and current ramp. As the current changes slower than the voltage at the turn-on, the power loss equation is divided into two parts. In the first part both the voltage and current are changing, in the second part only the current changes. This energy is multiplied by the switching frequency f_{sw}. The result of this equation is the IGBT turn-on power loss

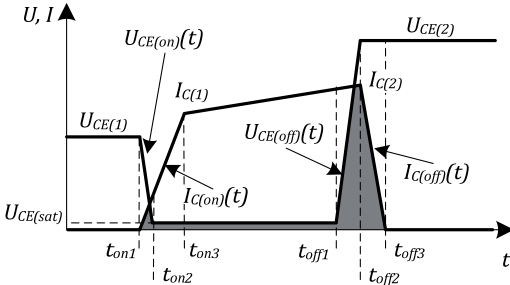

Fig. 9. Generalised IGBT waveforms in the two-level half-bridge voltage-source inverter

$$P_{on} = f_{sw} \cdot \left[\int_{t_{on1}}^{t_{on2}} U_{CE(on)}(t)\cdot I_{C(on)}(t)dt + \int_{t_{on2}}^{t_{on3}} U_{CE(sat)}(I_C)\cdot I_{C(on)}(t)dt\right], \quad (31)$$

where t_{on1} to t_{on3} is the total IGBT turn-on time; t_{on1} to t_{on2} is the IGBT collector-emitter voltage fall time from operation to saturation level, and t_{on1} to t_{on3} is the IGBT collector current rise time. $U_{CE(on)}(t)$ is the IGBT collector-emitter voltage at turn-on and $I_{C(on)}(t)$ is the collector current function during the turn-on of the IGBT. To simplify the calculations, voltage and current waveforms can be replaced by the linear functions:

$$U_{CE(on)}(t) = U_{CE(1)} - \frac{(t-t_{on1})\cdot\left(U_{CE(1)} - U_{CE(sat)}\right)}{t_{on2}-t_{on1}}, \quad (32)$$

$$I_{C(on)}(t) = \frac{(t-t_{on1})\cdot I_{C(1)}}{t_{on3}-t_{on1}}. \quad (33)$$

Transistor turn-off losses could be calculated assuming the current through the IGBT stays close to $I_{C(2)}$ during the interval t_{off1}-t_{off2} and the voltage across the IGBT is close to $U_{CE(2)}$ during the interval t_{off2}-t_{off3}. The turn-off energy loss can then be approximated by

$$P_{off} = f_{sw} \cdot \frac{U_{CE(2)}\cdot I_{C(2)}\cdot(t_{off3}-t_{off1})}{2}. \quad (34)$$

Table 2. Results of the analytical loss calculation

E_{on} (mJ)	E_{off} (mJ)	E_{rr} (mJ)	E_{cond} (mJ)	E_{osc} (mJ)	E_{total} (mJ)
5.2	254.3	16.6	10.1	9.3	295.5

Using the analytical approach (Eqs. 25-34) and the measured waveforms of the converter prototype the switching losses of the IGBT module are estimated (Table 2). Using the proposed analytical loss estimation method it is possible to estimate the contribution of the turn-on or turn-off losses in the total switching losses, which could be beneficial in estimating the feasibility of implementation of different loss reduction methods in semiconductors, such as passive or active snubbers. As known, the IGBT turn-on energy loss decreases while turn-off energy loss increases with the stray inductance. Both effects almost compensate each other [13]. In the studied converter due to the high stray inductance of the isolation transformer this effect is clearly observed.

Conclusions

As a result of increased heat dissipation from electronic devices, thermal management appears to be one of the most important issues of power converter design. The estimation of power dissipation of semiconductor devices is essential to determine operation parameters and cooling system requirements of a power converter. This paper presented an overview of different methods for loss calculation in inverters with the square-wave output, using IGBT module parameters extracted from the manufacturer's datasheets and test waveforms. A better method of approximating datasheet curves for fast analysis

at different current levels is proposed. Further, an improved analytical loss calculation method using test results of the half-bridge converter prototype is introduced.

Acknowledgements

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A. Blinov, D. Vinnikov, T. Jalakas. Loss Calculation Methods of Half-Bridge Square-Wave Inverters // Electronics and Electrical Engineering. – Kaunas: Technologija, 2011. – No. 7(113). – P. 9–14.

This paper presents methods of loss calculation of IGBT modules, operating in two-level half-bridge inverters with square-wave output. The equations for calculating IGBT module losses for typical collector current waveforms using linearly interpolated datasheet curves are presented. Since this method is generally limited in accuracy, a better approximation of datasheet curves is introduced. In the second part the switching waveforms of experimental two-level half-bridge inverter based on two 6.5 kV Infineon IGBT modules are analysed. Ill. 9, bibl. 13, tabl. 2 (in English; abstracts in English and Lithuanian).

A. Blinov, D. Vinnikov, T. Jalakas. Nuostolių įvertinimo metodų taikymas kvadratinės bangos keitikliuose // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2011. – Nr. 7(113). – P. 9–14.

Analizuojami IGBT tranzistorių, naudojamų dviejų lygių keitikliuose, nuostolių įvertinimo metodai. Pateiktos formulės IGBT tranzistoriaus nuostoliams apskaičiuoti. Pateiktos tiesiškai interpoliuotos kolektoriaus srovės kreivės. Pristatytas naujas aproksimacijos, kuria siekiama padidinti ribotą analizuojamojo metodo tikslumą, pavyzdys. Atliktas eksperimentas naudojant du 6,5 kV IGBT tranzistorius „Infineon“. Il. 9, bibl. 13, lent. 2 (anglų kalba; santraukos anglų ir lietuvių k.).

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2010 12th Biennial Baltic Electronics Conference (BEC2010)
Tallinn, Estonia, October 4-6, 2010

Analysis of Switching Properties of Different High Voltage IGBTs Operating Under Hard-Switching Conditions

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ABSTRACT: This paper studies the switching properties of different IGBTs with blocking voltage of 6.5 kV operating under hard-switching conditions. The reference topology used in analysis is a half-bridge inverter with power rating of 300 kVA. Since the development of high-voltage IGBT based converters is often a tradeoff between compactness, complexity, efficiency and cost the different state of the art 6.5 kV IGBTs with collector currents of 200 A, 400 A, 600 A and 750 A were compared under the desired operation conditions. The most technically and economical feasible solution is proposed. Some generalizations and practical considerations are provided.

1 Introduction

Modern high-voltage power electronic applications relate to several fields, such as electrical drives in industry and traction as well as equipment for power generation, transmission and distribution. Along with the development of 6.5 kV IGBT modules, complex applications managed by GTOs can be simplified by the implementation of 6.5 kV modules [1]. These modules are mainly designed for the two-level traction inverters with catenary voltage of 3.6 kV DC. A single IGBT has the voltage blocking capability two times the nominal catenary voltage level, which copes with the requirements for the rolling stock power electronics [2]. Today's state-of-the-art 6.5 kV IGBT modules are available in three basic configurations: with 200 A, 400 A and 600 A collector current capabilities and recently introduced 750 A modules.

Competitiveness requires reduced converter volume and cost as well as high reliability. Those requirements force the use of high switching frequencies in order to reduce passive component sizes. Thus, it is required to compare available module configurations in terms of switching performance and overall feasibility to achieve the best possible relation of desired parameters. Focus here is on a feasibility study of different 6.5 kV switch configuration solutions for the 300 kVA half-bridge inverter supplied from 3.6 kV DC line.

2 Definition of evaluation criteria

In the half-bridge voltage source inverter topology [3] two equal capacitors are connected in series across the DC input voltage source, providing a constant potential of one-half U_{IN} at their junction. A two-level half-bridge inverter has two main operating states: active and freewheeling states. During the active state two switches connected in series across the DC input voltage source (top and bottom switches) are turned on and off alternately, providing positive and negative square-wave impulses with the amplitude of $U_{IN}/2$ on the load. Table I shows the basic data of the reference half-bridge and conditions for the comparison.

TABLE I
BASIC DATA OF THE REFERENCE INVERTER

Parameter	Value
Supply voltage of the inverter, U_{IN}	3.6 kV DC
Inverter switch duty ratio, D	0.4
Rated power of the inverter, P_{out}	300 kVA
Maximum junction temperature of semiconductors, $T_{j,max}$	125 ^{0}C

The required rms collector current of switching transistors in the evaluated topology will be:

$$I_{Crms} = \frac{P_{out}}{U_{IN}} \cdot \frac{1}{\sqrt{D}} = 131.8\,(\text{A}). \quad (1)$$

In terms of this current value and in order to achieve increased switching frequency f_{sw} different HV switch configurations could be considered, for example, single 400 A 6.5 kV IGBT modules. The alternative solutions are: parallel connection of two 200 A 6.5 kV IGBTs (rms collector current per switch in this case is 65.9 A) or overmatching the requirements by the implementation of 600A or 750 A 6.5 kV modules.

3 Comparative evaluation of different high-voltage IGBTs

Semiconductor losses are a central evaluation criterion for a topology due to the direct correlation with virtually all other electrical parameters of the converter. The losses of high-voltage IGBTs are one of the limiting factors during power converter design with such devices. It finally leads to more powerful and complicated heatsinks to be implemented for ensuring the proper junction temperature of semiconductors or limiting of the f_{sw}. Both of these measures result in a negative impact on space-weight parameters, which are essential during the design of modern power electronic converters [3]. To provide a

better comparability, the datasheet values of high-voltage IGBTs from one vendor (Infineon) are compared. The analysis below is based on the IGBTs listed in Table II.

As shown in Table III, the dynamics of the 750 A 6.5 kV IGBT are slower in terms of the turn-on delay time ($t_{d,on}$) and the turn-off delay time ($t_{d,off}$) than that of the 200 A, 400 A and 600 A counterparts.

TABLE II
TYPICAL VALUES OF DIFFERENT INVESTIGATED IGBTS

IGBT type	Conditions	E_{on}, mJ	E_{off}, mJ	E_{rec}, mJ	U_{CEsat}, V
FZ200R65KF2	I_C=200 A, T_j=125 ^{0}C	1900	1200	550	5.3
FZ400R65KF2	I_C=400 A, T_j=125 ^{0}C	4000	2300	1050	5.3
FZ600R65KF2	I_C=600 A, T_j=125 ^{0}C	5900	3500	1600	5.3
FZ750R65KE3	I_C=750 A, T_j=125 ^{0}C	6500	4200	3000	3.7

TABLE III
SWITCHING DYNAMICS OF DIFFERENT INVESTIGATED IGBTS

IGBT type	Conditions	$t_{d\,on}$, µs	t_r, µs	$t_{d\,off}$, µs	t_f, µs
FZ200R65KF2	I_C=200 A, T_j=125 ^{0}C	0.72	0.4	6.0	0.5
FZ400R65KF2	I_C=400 A, T_j=125 ^{0}C	0.72	0.4	6.0	0.5
FZ600R65KF2	I_C=600 A, T_j=125 ^{0}C	0.72	0.4	6.0	0.5
FZ750R65KE3	I_C=750 A, T_j=125 ^{0}C	0.80	0.4	7.6	0.5

4 Derivation of upper switching frequency

Increased switching frequency is a desired parameter from the designer's point of view, since any improvements in f_{sw} lead to the minimization of passive components, like filter capacitors and inductors as well as isolation transformers. The most critical passive components in the given application are the half-bridge capacitors.

In practice, the switching frequency limit $f_{sw,max}$ of the IGBT is mostly determined by the thermal management system of the IGBT module. The thermal limit to frequency was derived by [4]:

$$f_{\text{sw,max}} = \frac{P_{tot} - P_{cond}}{E_{on} + E_{off}}, \quad (2)$$

where P_{tot} is the inverter total power loss, P_{cond} is the conduction power loss, E_{on} and E_{off} are the switching loss energies.

The practical switching frequency limits, which can be achieved by each IGBT in the hard switching mode and in the discussed operation conditions (see Table I), are shown in Fig. 1. The analysis is based on Iposim simulations (ambient temperature is 50 ºC, thermal resistance of the liquid cooling system is 0.005 K/W).

Comparison of the switching frequency limits shows that the dynamics of the 750 A IGBT is slower than that of the 600 A module for rms currents below 135 A. This factor in addition to its higher price makes 750A 6.5 kV modules unpractical for the considered inverter. On the other hand, in comparison with the 400 A module, both parallel connection for two 200 A IGBTs and application of 600 A IGBT theoretically allow the increased $f_{sw,max}$ to be used (by 15.4 and 34.6%, respectively).

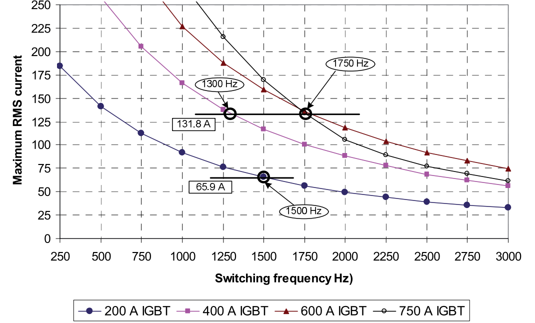


Fig. 1. Side-by-side comparison of switching frequency limits of different investigated Infineon 6.5 kV IGBTs (T_J=125 ºC)

5 Analysis of switch losses

Power losses are mainly the function of switching frequency, operating current and voltage, and the junction temperature. Increased f_{sw} allows the requirements of inverter's passive components to be decreased, but on the other hand, it leads to higher losses in semiconductor modules.

In order to simplify the analysis and receive a first approximation of dissipated power, the total power losses can be divided into conduction and switching losses. The losses during the off state of the transistor are negligible and will be not discussed. The half-bridge topology is symmetrical. As a result, it is enough to analyze only the losses in one switch.

$$P_{tot} = P_{cond} + P_{sw}. \quad (3)$$

Conduction losses occur between the end of the turn-on transition and the beginning of the turn-off transition. In order to calculate the power losses the dependence of both the gate-emitter voltage and the collector current has to be taken into account. This information can be found in the datasheet. In the case of the square-wave current waveform the conduction energy loss for a given pulse length is [5]:

$$E_{cond} = I_{Cmax} \cdot U_{CE}(I_C) \cdot t_{on}. \quad (4)$$

Conduction power losses for a periodical signal with the given duty cycle:

$$P_{cond} = I_{Cmax} \cdot U_{CE}(I_C) \cdot D. \quad (5)$$

The switching losses in the IGBT during one period of a periodical signal include the turn-on and turn-off losses:

$$P_{sw} = \lfloor E_{on}(I_C) + E_{off}(I_C) + E_{rr}(I_F) \rfloor \cdot f_{sw}. \quad (6)$$

where I_F is the forward diode current and E_{rr} is the freewheeling diode reverse recovery energy.

It should be pointed out that if the gate resistor of a users' gate drive does not have the same value as the gate resistor in the test circuit specified in the datasheet, some corrections may be necessary. This can be done with the help of the datasheet. The example of losses breakdown of the 400 A 6.5 kV module is shown in Fig. 2.

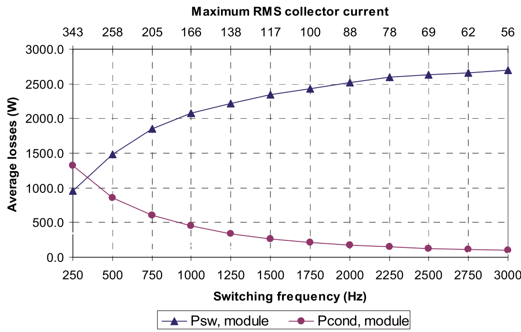


Fig. 2. Breakdown of 400 A 6.5 kV module static and dynamic losses vs. rms collector current and switching frequency at maximum performance (T_J=125 ºC)

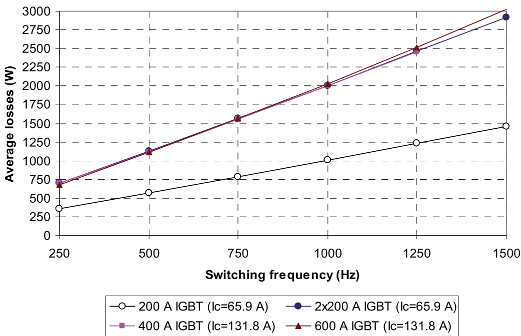


Fig. 3. Switch power dissipation as a function of switching frequency for different 6.5 kV Infineon IGBTs.

Fig. 3 reveals that at lower switching frequencies the total average losses are similar for all switch solutions. Thus, in terms of f_{sw} parity, neither the parallel connection of 200 A IGBTs to combine the switch, nor the implementation of 600 A IGBT provides a serious advantage over the 400 A IGBT in terms of power losses. Despite similar total power losses of all switch configurations, the 200 A IGBT with its smaller per-switch dissipation provides an effect of "distributed power losses". By the incorporating of distributed heatsinks (for each transistor separately) it could contribute to improved inverter reliability. The price for the distributed liquid-cooled heatsinks could be also reduced, because in the case of 200 A modules, the total power loss is distributed between the two switches, thus requiring less powerful cold plates than 400 A and 600 A IGBTs with centralized heat sources.

6 Estimation of recommended parameters

An essential issue to be taken into account during the converter design with HV IGBTs are the thermal limitations. The maximum allowed junction temperature $T_{J,max}$ provided by the manufacturer is fixed and a suitable inverter operation frequency and cooling system should be selected in order to keep the junction temperature T_J below maximum. Exceeding $T_{J,max}$ may damage the IGBT. Good design practice with considerations of reliability and the worst-case maximum junction temperature is to limit the steady state junction temperature to 70%-80% of $T_{J,max}$ or less [6]. Lower operation temperatures increase long-term reliability of semiconductors. Considering the $T_{J,max}$ of 125ºC, the maximum recommended operation junction temperature ranges between 85 and 100ºC.

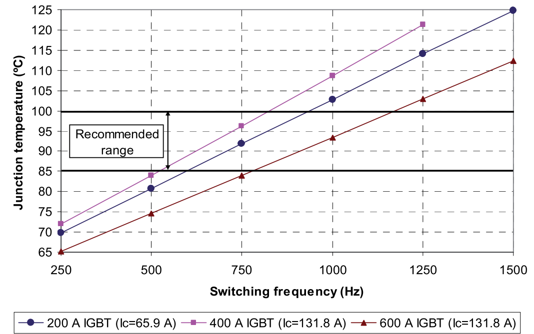
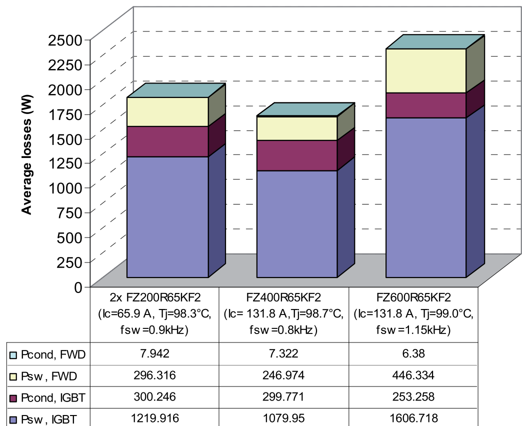


Fig. 4. Side-by-side comparison of junction temperature vs. switching frequency of different investigated 6.5 kV IGBTs.



	2x FZ200R65KF2 (Ic=65.9 A, Tj=98.3°C, fsw=0.9kHz)	FZ400R65KF2 (Ic= 131.8 A, Tj=98.7°C, fsw=0.8kHz)	FZ600R65KF2 (Ic=131.8 A, Tj=99.0°C, fsw=1.15kHz)
Pcond, FWD	7.942	7.322	6.38
Psw, FWD	296.316	246.974	446.334
Pcond, IGBT	300.246	299.771	253.258
Psw, IGBT	1219.916	1079.95	1606.718

Fig. 5. Breakdown of switch losses for maximum recommended switching frequencies of different 6.5 kV IGBTs

As shown in Fig. 4, the maximum recommended operation frequency is up to 900 Hz for the 200 A IGBT, 800 Hz for the 400 A IGBT and 1150 Hz for the 600 A IGBT. Due to better thermal handling capability both the parallel connection of 200 A modules and overmatching the requirements with 600 A module could provide an increase in the recommended switching performance over the 400 A module (by 12.5 and 43.8%, respectively). On the other hand, the total switching losses are increased proportionally (Fig. 5). It is worth outlining that despite the total per switch loss level in all three cases seems too high (1.85...2.26 kW), they are lower than 1% of the total switched power (300 kW).

7 Study of overall feasibility

Technical feasibility is one of the basic designer challenges. Fig. 6 features installation surface area requirements for different high-voltage switch solutions. It is obvious that the implementation of a single 400 A 6.5 kV IGBT results in smaller baseplate area than the total baseplate areas of the two paralleled 200 A or single 600 A switches. Moreover, at their maximum performance, 200 A and 600 A switch solutions require more powerful heatsinks to extract extra losses. Thus, the use of single 400 A 6.5 kV modules instead of the alternative devices seems more attractive when the space constraints of IGBT installation are determinative.

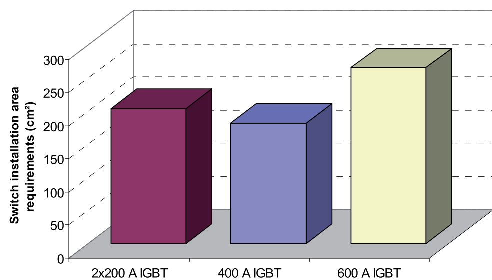


Fig. 6. Comparison of installation area requirements for different switch solutions.

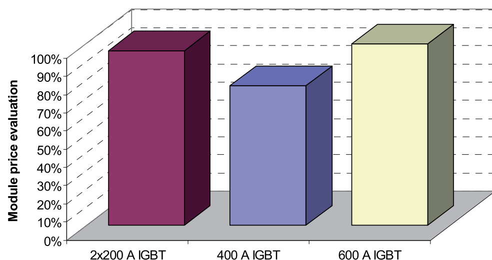


Fig. 7. Comparison of semiconductor prices

The price of the converter to be designed is one of the essential aspects from the designer's point of view. IGBT is one of the main components of such devices and their prices have a sufficient impact on the final price and, hence, on the overall competitiveness of the device produced (Fig. 7). It should be noted that this comparison considered only the semiconductor costs. This cost will be further increased by the price of the gate drivers and other associated components necessary for the operation of high-voltage IGBT modules, thus the requirement of more additional components for paralleled 200 A modules will further increase the cost of this solution.

Conclusions

Comparison of available 6.5 kV IGBT switch solutions for the 300 kVA half-bridge inverter has shown that both implementation of two paralleled 200 A modules or overmatching the requirements by implementation of 600 A module could provide an increase in switching frequency, while the implementation of the 750 A module is not feasible. According to previous investigations [3], the 12.5% increase in switching frequency in the case of paralleled 200 A modules and 43.8% increase in the case of the 600 A module could reduce the required capacitance and volume of the input capacitors by up to 13 and 31%, respectively. Hence, considering the need of more additional components, relatively small increase in performance and requirement of additional efforts to achieve desired current balancing between transistors, the implementation of paralleled 200 A modules seems unpractical. On the other hand, despite not providing advantages in switching losses, implementation of 600 A modules could offer more compact high power-density design, while application of 400 A modules provides a more cost-effective solution.

Acknowledgement

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[PAPER-IV] **Blinov, A.**; Vinnikov, D.; Ivakhno, V.; "Study of performance improvement methods for 6.5 kV IGBT based two-level half-bridge converters", Технічна електродинаміка, pp. 56-62, 2011.

STUDY OF PERFORMANCE IMPROVEMENT METHODS FOR 6.5 KV IGBT BASED TWO-LEVEL HALF-BRIDGE CONVERTERS

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Аннотация **– Использование 6.5 кВ IGBT транзисторов позволяет применять простые и надёжные полумостовые схемы для вспомогательных источников питания железнодорожного транспорта с напряжением контактной сети 3.0 кВ. Недостатком данных схем являются жёсткая коммутация ключей и паразитные колебания в инверторе, обусловленные индуктивностью рассеяния трансформатора и емкостями высоковольтных транзисторов. В данной статье приведён анализ различных способов улучшения характеристик прототипа высоковольтного полумостового преобразователя напряжения.**

Key words **– snubber, half-bridge, power dissipation.**

INTRODUCTION

Along with the development of 6.5 kV IGBT modules, complex applications managed by series connection of numerous lower voltage semiconductors could be simplified by replacing them with a single 6.5 kV module, which would enable simple and reliable two-level half-bridge (HB) voltage-source inverter (VSI) topologies to be implemented for the rolling stock auxiliary power units.

This research focuses on an experimental half-bridge converter based on two Infineon 200 A 6.5 kV IGBT modules (FZ200R65KF1) recently developed at Tallinn University of Technology. Investigations have shown that the experimental converter is capable of providing required performance within the whole range of rolling stock supply voltage of 2.2…4.0 kV and a wide power range – 10…50 kW [1]. The converter consists of primary and secondary parts galvanically isolated by the high frequency transformer. The primary part is a square-wave two-level half-bridge PWM inverter with two input capacitors. The secondary part consists of full bridge rectifier and *LC* filter. Such converter (Fig. 1, Table 1) is very simple

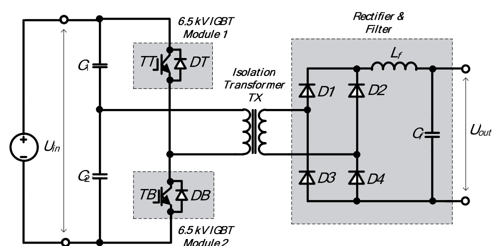


Fig. 1

Table 1

Parameter	Symbol	Value
Input voltage, kV	U_{in}	2.2…4.0
Output power, kW	P_{out}	10…50
Nominal output voltage, V	U_{out}	350
Switching frequency, Hz	f_{sw}	2000
Transformer turns ratio	N_s/N_p	18/44
Leakage inductance, μH	L_E	186.1

in control and protection, has reduced component count and provides good reliability.

Main problems of this topology are high power losses in semiconductors due to hard switching and consequently, limited switching frequency because of thermal issues. This imposes increased requirements on passive components of the converter.

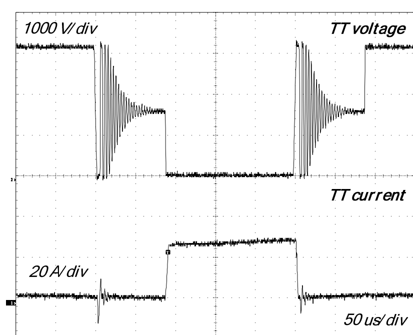


Fig. 2

These downsides are related to the common peculiarity of half-bridge topologies – oscillations after transistor turn-off caused by the presence of parasitic capacitive and inductive circuit elements. Although the frequency of these oscillations is not high enough (330 kHz, see Fig. 2) to generate strong radiated EMI, it can cause some problems with conducted EMI in the contact line. According to investigations, these parasitic effects are not dangerous to IGBT modules, neither are they dangerous to other circuit elements since freewheeling diodes conduct before noticeable overvoltage is created [2].

There are a number of ways of how to improve the switching process of semiconductor switches in the HB inverters ranging from simple passive *RC* and/or *RCD* snubbers to zero voltage/zero current switching topologies, which can be classified under three headings [3]:

- resonant converters,
- asymmetrical HB converters,
- auxiliary switch converters.

However, due to wide variations in the railway contact line voltage as well as a wide output power range not all solutions are feasible since they could limit the main features of the converter.

This paper focuses on further optimization of the experimental converter in order to suppress the oscillations and improve the switching performance of the IGBT modules without increasing its complexity or reducing reliability and efficiency significantly.

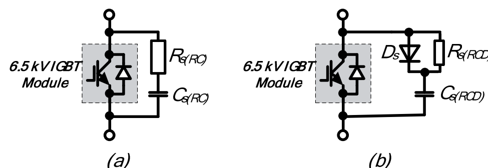


Fig. 3

DISSIPATIVE SNUBBERS

The snubber circuit is an additional part to the basic converter, which is added to reduce the stresses on an electrical component. Usually, in a power semiconductor device, snubbers may be used singly or in combination depending on the requirements. The additional complexity and the cost added to the converter circuit by the presence of the snubber must balance against the benefits of limiting the stresses on critical circuit components [4]. There are three broad classes of passive snubber circuits:

- unpolarised *RC* snubbers,
- polarised *RC* snubbers,
- polarised *LR* snubbers.

The measured IGBT waveforms of the experimental square-wave two-level half-bridge inverter are shown in Fig. 2. In the considered inverter, the reverse recovery process of freewheeling diodes is finished during the freewheeling state. Hence, there is no additional current during the turn-on of the IGBT, resulting in lower losses at turn-on. Therefore there is no actual need for limiting *dI/dt* with *LR* snubbers. On the other hand, after turn-off the parasitic oscillations could be damped using *RC* snubbers (Fig. 3a). These passive snubbers are generally placed across semiconductor devices and dissipate the energy stored in the circuit during the active state. An important point is that the lowest value of peak voltage attainable is determined by the size of C_s. If a lower peak voltage is required, then a larger C_s must be used. This means that the power dissipation has to increase as the peak voltage is reduced [5].

The polarised *RC* snubbers, also referred as *RCD* snubbers (Fig. 3b) are applicable to either rate of rise control or clamping. At turn-off, the snubber will carry most of the

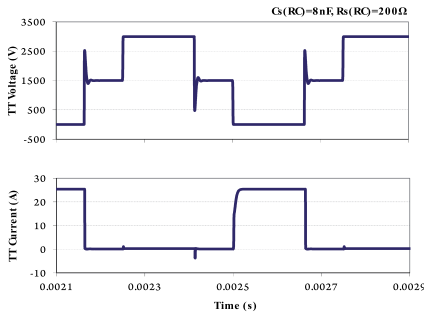


Fig. 4

switch current and transfer power dissipation into the snubber, increasing the reliability of the switch The main disadvantage of the *RCD* snubber is due to the diode across the resistor the effective value of $R_{s(RCD)}$ during the charging of $C_{s(RCD)}$ is close to zero, hence the voltage across the switch for a given $C_{s(RCD)}$ will be higher than the corresponding value using an *RC* snubber. Moreover, during the switch turn-on a capacitive discharge current occurs, increasing turn-on losses. Therefore when using an *RCD* snubber in the half bridge inverters, the turn-on snubber should be included as well [4].

The *RC* snubber capacitance can be estimated by:

$$C_{s(RC)} = L_E \cdot \left(\frac{I_{rr}}{U_{in}}\right)^2, \quad (1)$$

where I_{rr} is the peak reverse recovery current, L_E is the stray inductance of the commutation loop and U_{in} is the DC supply voltage. The snubber resistance is then approximated by:

$$R_{s(RC)} = \frac{U_{in}}{I_{rr}}. \quad (2)$$

Finally, the power dissipation in the snubber resistor in the case of the HB (two voltage transitions per cycle) converter is estimated by [6]

$$P_{s(RC)} = C_{s(RC)} \cdot U_{in}^{\ 2} \cdot f_{sw}, \quad (3)$$

where f_{sw} is the switching frequency.

The simulated waveforms of the converter operating with unpolarised *RC* snubbers are shown in Fig. 4.

With a smaller snubber capacitor, the freewheeling diodes of the main switches

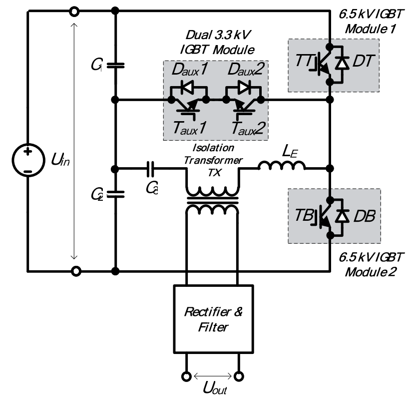


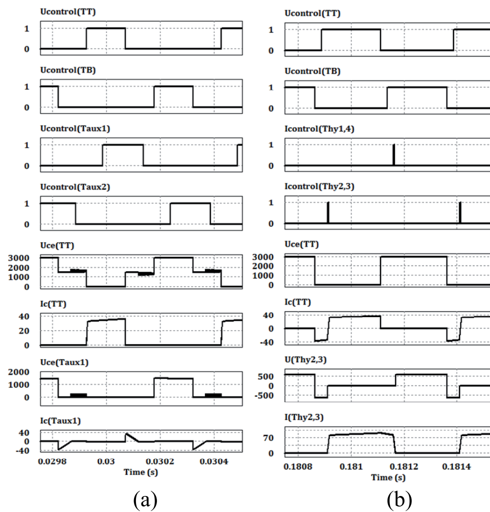
Fig. 5

conduct to partly recycle the energy while part of the energy is dissipated in the snubber resistor. For a larger snubber capacitor, the energy in the leakage inductance may be fully dissipated in the snubber without recycling through freewheeling diodes.

ACTIVE SNUBBERS

Since the transformer leakage energy is being dissipated in the passive snubber circuits, the overall efficiency of the converter is reduced. In order to utilise the leakage inductance and eliminate the oscillations an asymmetric control method could be implemented. The duty cycles of the switches are not equal in this case and due to the very short freewheeling state (both main switches are turned off) the zero voltage switching (ZVS) of both of the switches can be achieved. However, an asymmetric half-bridge converter has the asymmetric stress distribution in the components and a DC bias in the transformer. Therefore, it is generally not suitable for applications with a wide input-voltage range. Moreover, the input-output relationship of the asymmetric-controlled half-bridge converter is nonlinear, resulting in a lower duty cycle at high U_{in} compared to the symmetric-controlled half-bridge converter, which results in degrading the converter performance at high U_{in} [7].

An active clamping method proposed in [8] uses an auxiliary circuit where the leakage energy is circulating during the freewheeling state. Prior to the main switch turn - on, the auxiliary circuit energy is



(a) (b)

Fig. 6

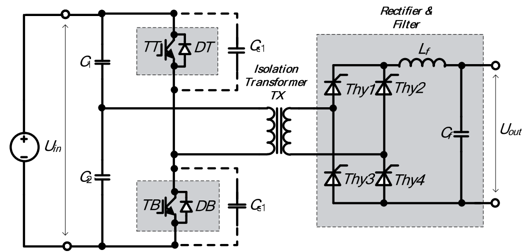


Fig. 7

released. The freewheeling diodes of the main switches conduct, creating the ZVS condition. However, there are several drawbacks. Firstly, the leakage inductance should be large enough for the freewheeling current to maintain, especially at low duty cycles. Secondly, there is high conduction loss in auxiliary switches.

To overcome disadvantages of the active-clamp snubber, a modified method is introduced in [7] (Fig. 5). Instead of circulating, the transformer leakage energy is transferred to the auxiliary capacitor, which also blocks the DC component avoiding saturation of the transformer. Since the energy transfer accounts for a small part of the switching period, the conduction energy loss of the auxiliary switches is minimised. The primary switches are still hard switched, however the voltage stress is reduced to $½U_{in}$ during turn-off transient, leading to reduced losses. The freewheeling diodes of the main switches never conduct and the auxiliary switches $T_{aux}1$ and $T_{aux}2$ turn on with ZVS and turn off with ZCS (zero current switching). The energy transfer period to the capacitor is estimated by

$$t_{tr} = \frac{2 \cdot C_S \cdot L_E}{t_{on}}, \quad (4)$$

where t_{on} is the on-state time of the switches.

The switching diagram and the simulation waveforms are presented in Fig 6(a). It could be observed that the voltage across C_3 causes minor oscillations across the transformer primary, however since this voltage is much smaller than U_{in} the ringing is almost negligible.

The topology decstibed requires two additional switches with half of the voltage rating and two additional PWM channels in comparison to the basic HB topology. In the case of the studied topology, two additional 3.3 kV switches are required, affecting the converter price.

CONVERTER WITH DISTRIBUTED COMMUTATION

In the discussed topologies the secondary part of the converter consists of a full bridge diode rectifier and an *LC* filter. Hence, the forced commutation processes occur only in the converter primary. However, by replacing the rectifier diodes with thyristors (Fig. 7) or transistors with series diodes (for example reverse blocking IGBTs), the active state of the converter could be controlled by the rectifier [9]. The inverter switches operate with consant duty cycle of 0.45 to avoid short-circuit and the output voltage is controlled by the varying delay time between the turn-on of the thyristors in the rectifier and the turn-on of the IGBTs in the inverter. Hence, at the begining of each half period the current will have the same sign as in the previous one and will only change its sign when the other thyristor pair turns-on. Therefore at the beginning of each half period the current will flow through the freewheeling diode of the transistor to be turned on next, achieving the ZVS of both

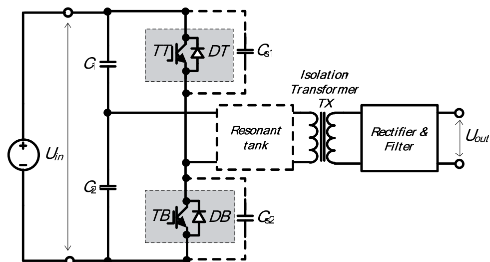


Fig. 8

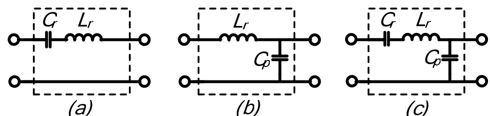


Fig. 9

main switches. The switching diagram and the simulation waveforms are presented in Fig 6(b).

The leakage inductance of the transformer secondary replaces the thyristor turn-on snubber and capacitive snubbers across the IGBTs in the inverter could reduce the losses during the turn-off. Therefore the switching losses of the inverter are dramatically decreased. On the other hand, the conduction losses are increased because more current is circulating in the inverter and the transformer due to the high duty cycle of the primary switches.

RESONANT CONVERTERS

Resonant converters are an attractive alternative to traditional PWM topologies because of reduced switching losses and the EMI due to the sinusoidal behaviour of the resonant circuit. Such converters (Fig. 8) could operate at high frequencies to reduce the size of their reactive components. These converters generally feature the second or the third order resonant tank circuit, i.e. the storage tank consists of two or three energy storage elements [10].

Resonant converters can be divided into three groups as series (Fig. 9a), parallel (Fig. 9b) and series-parallel (Fig. 9c) converters. Power control is achieved by varying the switching frequency around the resonance frequency [3].

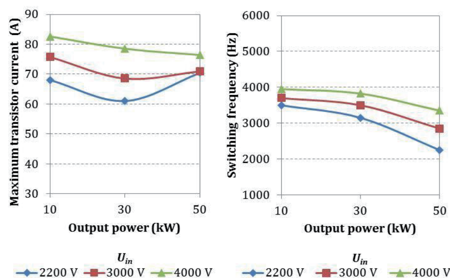


Fig. 10

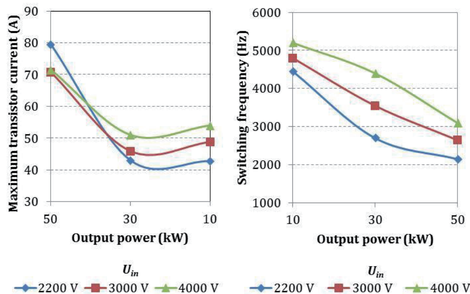


Fig. 11

Table 2

Parameter	Symbol	Value
Resonant inductance, mH	L_r	2.87
Resonant capacitance 1, μF	C_r	2.2
Resonant capacitance 2, μF	C_p	1.1(2.2)
Output power, kW	P_{out}	10…50
Series resonant frequency, Hz	f_{sw}	2000
Transformer turns ratio	N_s/N_p	18/44

The major advantage of a series-resonant converter is that the current in the power devices decreases with a decrease in the load, leading to higher efficiency. However, there are difficulties in regulating the output voltage at light load operation [11, 12]. Since the studied converter must operate with wide load variations, this topology is not considered suitable.

In contrast to the series-resonant converter, the parallel converter can regulate the output voltage at no load by running at a frequency above resonance. On the other hand, such converters have higher device current that is relatively independent of the load. This leads to high conduction losses in semiconductors and reactive components,

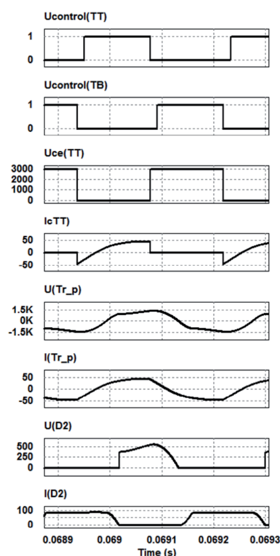


Fig. 12

decreasing the efficiency, especially at light loads.

The series-parallel converter, also referred as *LCC* converter, aims at combining the advantages of the series and the parallel converters whilst reducing or eliminating their disadvantages. The behaviour is dependent of the C_r/C_p ratio. As C_p gets smaller, the converter resembles a series converter and the upper frequency needed at light loads increases. On the other hand, with increased C_p the converter resembles a parallel converter and the circulating current no longer decreases with the load [10]. The following analysis will study two cases: $C_r=C_p$ and $C_r=2 \cdot C_p$. Table 2 presents the resonant circuit parameters calculated using the approximations proposed in [13]. Only the operation above resonance will be considered in the following as it is more desirable from the practical point of view since the ZVS is provided for the IGBTs, allowing use of capacitive snubbers to avoid turn-off losses.

As shown in Fig. 10, with $C_r=C_p$, the operation frequency range is relatively narrow (2.25…3.95 kHz), however the maximum switch current is almost independent of the load, hence the converter behaves as parallel-resonant. On the contrary,

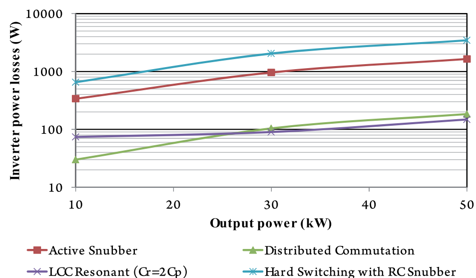


Fig. 13

with $C_r=2 \cdot C_p$ (Fig. 11), the operation frequency range gets wider (2.15…5.2 kHz), but the maximum switch current reduction at light loads is clearly observed. For this reason, it is considered as a compromise design. The switching waveforms are shown on Fig. 12 (f_{sw}=3.55 kHz, P_{out}=30 kW).

LOSS COMPARISON

The power loss of the studied solutions is estimated and presented on Fig. 13. It should be mentioned that only the semiconductor and snubber losses in the inverter part are included. As shown the active snubber solution could provide up to 50% decrease in the inverter losses in comparison to the inverter with dissipative snubber. The *LCC* resonant converter and converter with distributed commutation are able to provide even more essential reduction of inverter losses. In these topologies using the capacitive snubbers the switching losses of the main IGBT switches could be eliminated completely.

CONCLUSIONS

According to the analysis, the dissipative *RC* snubber is the most effective and the cheapest solution to damp the parasitic ringing. Among other solutions, the converter with distributed commutation could provide a very effective way to completely avoid the oscillations as well as provide sufficient increase in the operating frequency with a relatively low increase in the overall complexity of the system. The main disadvantages, such as low power factor at some operating points are planned to be discussed in the future papers. The implementation of a lossless active snubber

and a series-parallel resonant converter will affect the overall cost of the system more noticeably, therefore these solutions are not considered as feasible as the former ones.

ACKNOWLEDGEMENT

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[PAPER-V] **Blinov, A.**; Ivakhno, V.; Zamaruev, V.; Vinnikov, D.; Husev, O. "A Novel High-Voltage Half-Bridge Converter with Phase-Shifted Active Rectifier", IEEE International Conference on Industrial technology, ICIT'2012, pp. 967-970, 19-21 March 2012.

A Novel High-Voltage Half-Bridge Converter with Phase-Shifted Active Rectifier

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***Abstract*- The half-bridge converter with phase-shifted active rectifier allows us to avoid drawbacks of the traditional hard-switched half-bridge converter with a diode rectifier, such as high semiconductor losses and parasitic oscillations in the inverter. This paper introduces a novel improved control algorithm for a full-bridge phase-shifted active rectifier, allowing reduction of the energy circulation during its operation. The advantages of the algorithm are verified with a small-scale converter prototype. The experimental results were found in full accordance with expected waveforms.**

I. INTRODUCTION

Simple conventional converters based on a half-bridge voltage-source inverter with fully controlled switches and non-controlled diode rectifier can be used in high-voltage applications such as railroad traction with contact grid voltage of 2.2–4.0 kV and output power of 10…50 kW that implement high-voltage IGBT modules [1]. The advantages of the converter are a small number of power components, galvanic isolation of primary and secondary sides and simplicity of the control algorithm.

Since the transistors in this conventional topology are hard-switched, in the case of high-voltage IGBTs the switching losses could be rather high. That leads to a necessity to reduce the switching frequency down to 1-2 kHz due to thermal issues. With such relatively low conversion frequency the passive components have significant dimensions and price. Moreover, after transistor turn-off the undesired parasitic oscillations occur, caused by the presence of parasitic capacitive and inductive circuit elements, mainly the IGBT module capacitance and the transformer leakage inductance. These drawbacks highlight the need to investigate how to improve the performance of such topology, preferably without significant increase in its complexity or reduction of reliability.

Previously made investigations [2] revealed that among a wide range of available options (dissipative snubbers, active clamping, resonant topologies etc.) the topology with a phase-shifted active rectifier is one of the most promising candidates.

This paper focuses on the analysis of this topology and its further optimization by introducing an improved control algorithm, which improves the power factor of the converter. The implementation of the algorithm is described and tested on a small-scale experimental prototype.

II. PHASE-SHIFTED SYNCHRONOUS RECTIFIER

The phase-shifted synchronous rectifier concept is a well-known method to reduce the ringing, increase the efficiency and achieve ZVS (zero voltage switching) of converter switches. The other advantages are relatively small circulating energy and constant frequency operation, allowing for simple control of the converter. Generally, these converters comprise a half- or a full-bridge inverter, a high-frequency transformer and a rectifier [3-4]. The rectifier part could be classified as [5]:

- Full-bridge
- Central-tapped
- Current-doubler

The paper will investigate the feasibility of the half-bridge topology with a full-bridge phase-shifted synchronous rectifier with reverse blocking switches (Fig. 1), as it requires the least modifications to the reference topology.

In this topology the inverter switches operate with a constant duty cycle of 0.45 to avoid short-circuit and the output voltage is controlled by the varying delay time between the turn-on of the switches in the rectifier and the turn-on of the IGBTs in the inverter. At the beginning of each half-period, the transformer current will have the same direction as in the previous one and will only change it when the other switch pair in the rectifier turns on. Therefore, at the beginning of each half-period the current will flow through the freewheeling diode of the IGBT module to be turned on next, allowing the ZVS of both inverter transistors. The switching diagram is presented in Fig. 5. This switching algorithm allows using non-dissipative capacitive snubbers in the inverter and the inductive ones in the rectifier. Their role is performed by the transformer leakage inductance [2].

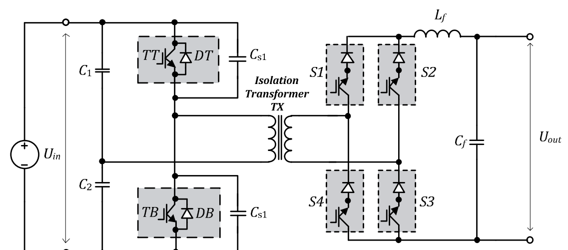


Fig. 1. Investigated half-bridge converter circuit with controlled switches at the secondary side.

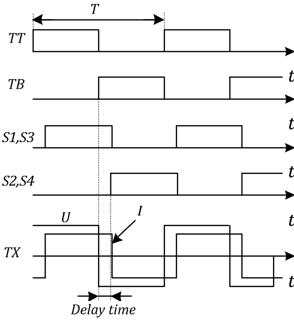


Fig. 2. Switching states of a conventional converter with a phase-shifted active full-bridge rectifier.

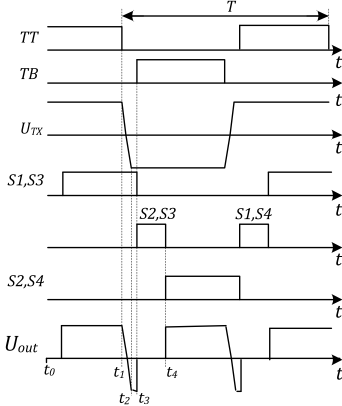
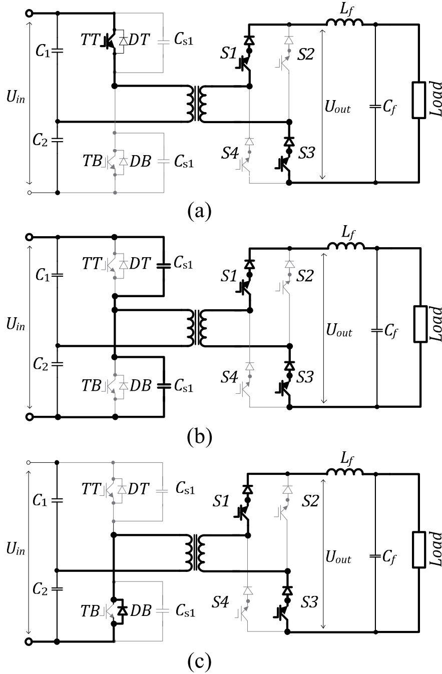


Fig. 3. Modified switching states of a converter with a phase-shifted active full-bridge rectifier.



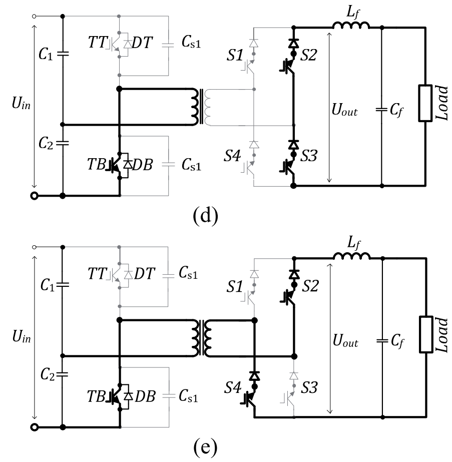


Fig. 4. Operation modes of the converter with a modified phase-shifted active full-bridge rectifier.

According to Fig. 2, the disadvantage of the converter control algorithm is the presence of intervals of energy return from the load to the power supply (time intervals of the opposite sign of the current and voltage of the primary transformer winding during the delay time). If the energy return is not possible there will be an increase of the input voltage of the inverter and a deviation of the midpoint potential of the capacitor input voltage divider. Such effects can be reduced by increasing the capacitance of the input voltage divider. On the other hand, that leads to an increase in the dimensions and cost of the converter. Moreover, energy circulation corresponds to the generation of the reactive power, resulting in the reduction of the converter power factor and the efficiency due to increased conduction losses. In the case of high input voltage (large periods of energy return), the effects of these drawbacks could be unacceptable.

III. NOVEL CONTROL METHOD OF A PHASE-SHIFTED ACTIVE RECTIFIER

To overcome the disadvantages of a conventional phase-shifted active rectifier, the control algorithm of the rectifier switches could be modified, at the same time keeping the advantages of the reference phase-shifted control algorithm. A similar concept for the full-bridge converter was firstly introduced in [6]. The proposed algorithm provides phase-shifted control together with practically no return of energy into the power supply. This is achieved by introducing two additional switching states of the rectifier switches. The idea of such an algorithm is presented in Fig. 3. The following events during the switching half-period could be distinguished:

t_0-t_1 – transistor TT and switches S1, S3 are conducting (Fig. 4a). The voltage of the transformer primary winding is $+U_{in}/2$, and at the output, the voltage of the rectifier is $+U_{out}$.

t_1-t_2 – transistor TT is turned off. The transformer voltage and U_{out} change their sign as the snubber capacitors are recharged (Fig. 4b).

t_2-t_3 – the snubber capacitors are recharged and the transformer primary voltage reaches $-U_{in}/2$. The freewheeling diode DB opens, starting the energy return interval. The output voltage of the rectifier is now $-U_{out}$ (Fig. 4c). Until the moment t_3 the processes do not differ from the corresponding ones in the conventional phase-shifted synchronous rectifier.

t_3-t_4 – switch S1 is now closed and S2 is opened (Fig. 4d). The load current freewheels through S3, S2, L_f and the load. The energy return interval is over, the negative voltage ($-U_{out}$) is applied to switch S1 and is turned off with ZCS. The IGBT TB could be opened with ZVS during this period.

t_4 – switch S4 is opened (Fig. 4e) and its di/dt is limited by the transformer leakage inductance. Transistor TB and switches S2, S4 are conducting. The voltage of the transformer primary winding is $+U_{in}/2$, and at the output voltage of the rectifier is $+U_{out}$. The processes are then repeated with the difference that the transistor and the primary side diodes replace each other, so do switches S1, S2 and S3, S4.

The control of the output voltage is achieved by varying current freewheeling duration (time interval t_3-t_4). The energy return interval (time interval t_2-t_3) required to recharge snubber capacitors could be constant and should be kept as short as possible in order to maintain high power factor and reduce conduction losses.

The proposed control concept was simulated using PSIM software. The simulation parameters are selected to data presented in Table I. As shown in Fig. 5, the simulation results were in full accordance with estimated waveforms.

IV. Experimental Verification of the Phase-Shifted Active Rectifier

In order to implement the introduced modified control algorithm (Fig. 3) for the experimental half-bridge converter with the phase-shifted active rectifier, six independent PWM channels were used. Two channels with small dead time were used to drive IGBTs in the inverter (Fig. 5). Four channels were used to control the rectifier. The inverted control signals of S1 and S2 are shifted by the ratio γ relatively to turn-off of inverter switches (Fig. 6). The inverted control signals for S3 and S4 are shifted by the ratio D_s relatively to S1 and S2. All channels have a constant duty cycle: the inverter switches operate with D_i=0.45, while the rectifier switches operate with D_r=0.51 to avoid the situation when only one transistor in the rectifier is turned on. The output voltage is regulated by varying the ratio D_s. The values of γ and D_s are obtained as follows:

$$\gamma = \frac{t_3 - t_2}{T}. \tag{1}$$

$$D_s = \frac{t_4 - t_3}{T}. \tag{2}$$

The output voltage can be expressed by the following equation:

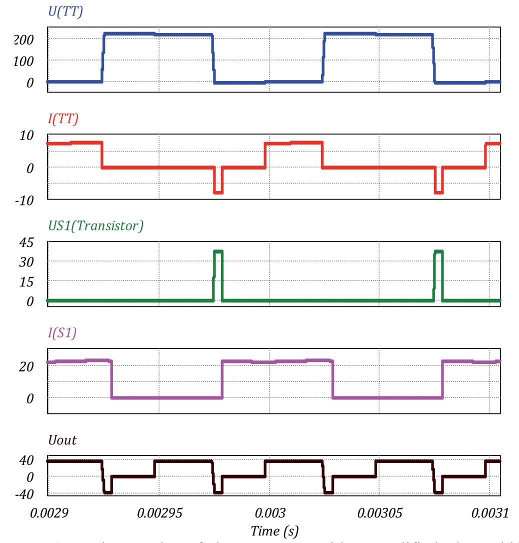


Fig. 5. Operation modes of the converter with a modified phase-shifted active full-bridge rectifier.

TABLE I
PARAMETERS AND COMPONENTS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Symbol	Value / Type
Input voltage, V	U_{in}	200…400
Load voltage, V	U_{load}	20
Switching frequency, kHz	f_{sw}	10
Transformer turns ratio	n	0.28
Inverter switch	TT, TB	IRGPS60B120KD
Rectifier switch	S1-S4	IXFX 48N60P
Rectifier diode		ON MBR40250
Output power, W	P_{out}	1000

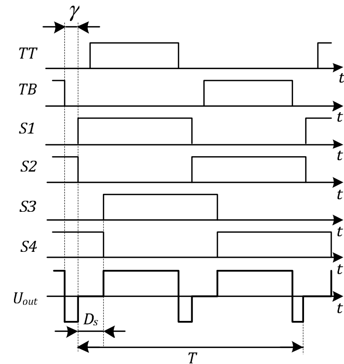


Fig. 6. Practical implementation of the modified switching diagram of a converter with a controlled rectifier.

$$U_{out} = n \cdot U_{in} \cdot (1 - 4 \cdot \gamma - 2 \cdot D_s), \tag{3}$$

where n is the transformer turns ratio.

To validate the proposed novel control algorithm for a half-bridge converter with a phase-shifted active rectifier, a small-scale prototype with the rated power of 1 kW was constructed (Fig. 9). The main parameters are presented in Table I.

During the first tests the converter was operating without snubbers and the measured waveforms are presented in Figs. 7-8. The duration of γ is relatively high only for visual purposes. As shown, the test results completely correspond to estimated waveforms.

As mentioned, rectifier switches should have reverse blocking capability. In the prototype MOSFETs with series connected diodes were used. In the real system these switches could be replaced by reverse-blocking IGBTs or fast thyristors (the switches turn-off with ZCS) for reduced power dissipation during the on-state.

The application of capacitive snubbers allows turn-off losses of the inverter IGBTs to be reduced. Since this loss reduction has been reported to be lower than expected due to increased tail current duration, it should be experimentally estimated for every particular application [7-9].

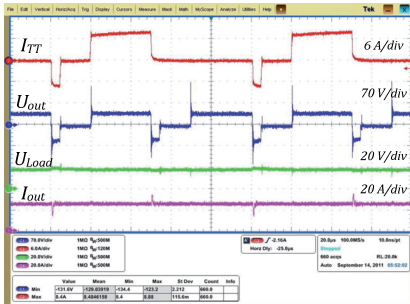


Fig. 7. IGBT current, output voltage, load voltage and current of the experimental converter prototype.

Fig. 8. IGBT voltage and current (top), S1 MOSFET voltage and current (bottom) of the experimental converter prototype.

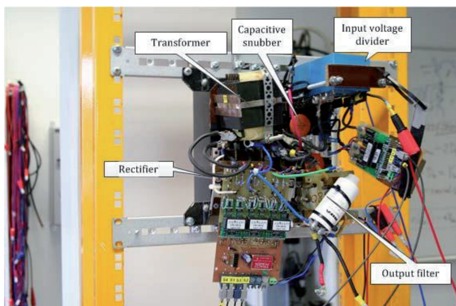


Fig. 9. Photo of the experimental converter.

V. Conclusions

The introduced modified control algorithm for the half-bridge converter with an active rectifier allows the ZVS of the inverter switches and the ZCS of the rectifier switches. At the same time the parasitic oscillations after the turn-off of the inverter IGBTs are completely avoided. The leakage inductance of the transformer acts as the turn-on snubber for rectifier transistors and turn-off losses of the inverter transistors could be reduced using capacitive snubbers. Unlike resonant converter solution, the proposed system requires only minor modifications to the basic circuit, does not need any additional bulky passive components or a complex frequency-control algorithm and allows reduction in the energy circulation during the operation.

The operation of the converter was verified with the experimental prototype and the test results were in full accordance with expected waveforms.

Focus in the further research will be on the possibilities of conduction loss reduction in the rectifier and estimation of the overall converter efficiency.

Acknowledgement

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Energy-Efficient High-Voltage Switch Based on Parallel Connection of IGBT and IGCT

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Abstract- **This paper presents an analysis of a hybrid high-voltage switch based on the parallel connection of IGBT and IGCT. The proposed configuration allows combining the advantages of both semiconductors, resulting in substantially reduced power losses. Such energy efficient switches could be used in high-power systems where decreased cooling system requirements are a major concern. The operation principle of the switch is described and simulated and power dissipation is estimated at different operation conditions.**

I. INTRODUCTION

High power densities together with a high functionality are the key aspects of modern power electronics. Further requirements are decreased volume and weight of the power systems as well as low cost. In order to fulfil these demands high switching frequencies of the semiconductors are necessary. Insulated gate bipolar transistors (IGBTs) are the major representatives in present day's medium- and high voltage electronics. In terms of blocking voltages (up to 6.5 kV) these devices have reached a level which can satisfy the majority of needs. The major advantages of IGBTs are easy driving and snubberless operation [1]. On the other hand, the switching behaviour of low voltage class IGBTs (<1 kV) is generally slower in comparison to MOSFETs, and high voltage class IGBTs (>3.3 kV) generally have higher conduction losses than GTO and IGCTs. In order to improve the performance of IGBTs, different approaches and methods were introduced and developed. For instance, at lower voltages, increased performance was achieved by a parallel IGBT-MOSFET-combination as shown in [2]. The hybrid integration of a unipolar and a bipolar power semiconductor in parallel allowed combining of their advantages whilst avoiding their disadvantages [3]. However, these positive results were observed only for certain applications and operation parameters.

Similarly, for high power applications the performance of high-power switches could be increased by a parallel connection of IGBT and IGCT switches [4-6]. This paper will focus on 4.5 kV class switches, since both IGBT and IGCT type semiconductors in press-pack type housings are commercially available, allowing easy connection of these devices in series by special cooling systems. The rated permanent DC voltage for both semiconductor devices is generally 2.8 kV. Using two- or three-level topologies, if necessary, this is sufficient to cope with the requirements of many traction and industrial applications with voltage ratings of 2.0-5.6 kV without the need of series connection of several semiconductors. Comparing parameters of two 4.5 kV class press-pack semiconductors: T0900EA45A-Westcode (Table 1 [7]) and 5SHY35L4512-ABB (Table 2 [8]), it could be observed that the on-state voltage U_T of IGCT is lower than the corresponding parameter $U_{CE(sat)}$ of IGBT. The turn-on behaviour is similar for both devices, while turn-off behaviour of IGCT is distinctly slower, which results in greatly increased losses during turn-off (Fig. 1).

The idea is based on the integration of positive properties of gate-commutated thyristors in terms of low turn-on and on-state power losses as well as high surge current capability and IGBTs with their relatively low losses during turn-off. This may allow creating high-voltage and high-current energy-efficient switches with increased switching frequency, which could be advantageous in high-power (>500 KVA) industrial and railway traction systems.

TABLE I
CHARACTERISTIC VALUES OF 900 A 4500 V IGBT (T0900EA45A)

Parameter	Symbol	Value
Collector-emitter voltage	U_{CE}	4500 V
Permanent DC voltage	U_{DC}	2800 V
Collector-emitter saturation voltage (I_C=900 A)	$U_{CE(sat)}$	4.7 V
Turn-on delay time	$t_{d(on)}$	1.6 µs
Rise time	t_r	2.3 µs
Critical rate of rise of diode current	dI_t/dt_{cr}	2000 A/µs
Turn-off delay time	$t_{d(off)}$	1.2 µs
Fall time	t_f	1.2 µs
Turn-off energy (I_C=900 A)	E_{off}	2.6 J

TABLE II
CHARACTERISTIC VALUES OF 4000 A 4500 V IGCT (5SHY35L4512)

Parameter	Symbol	Value
Peak off-state voltage	U_{DRM}	4500 V
Permanent DC voltage	U_{DC}	2800 V
On-state voltage (I_T=900 A)	U_T	1.15 V
Turn-on delay time	$t_{d(on)}$	3.5µs
Rise time	t_r	1 µs
Critical rate of rise of current	dI_t/dt_{cr}	1000 A/µs
Turn-off delay time	$t_{d(off)}$	11 µs
Turn-off energy (I_T=900 A)	E_{off}	6-8 J

II. OPERATION PRINCIPLE

The structure of the proposed hybrid switch (HS) configuration is presented in Fig. 2. The HS consists of a parallel connected asymmetrical press-pack IGCT and press-pack IGBT with an integrated freewheeling diode (FWD).

In the following analysis the HS is assumed to be operated in voltage - source inverter (VSI) circuits. The test circuit shown in Fig. 3 represents the main events that could occur in

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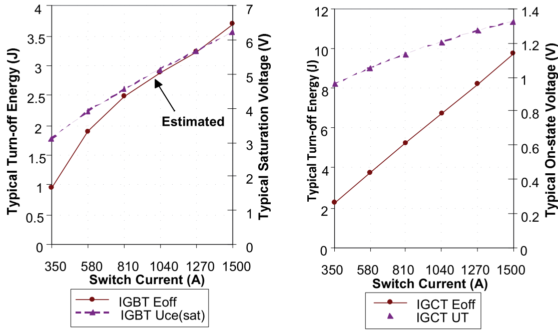

Fig. 1. Side-by side comparison ofT0900EA45A IGBT and 5SHY35L4512 IGCT on-state voltages and turn-off energies vs. current

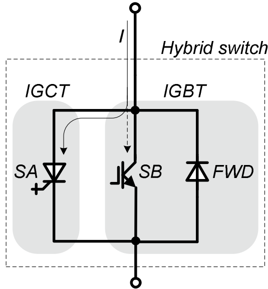

Fig. 2. Proposed hybrid switch configuration

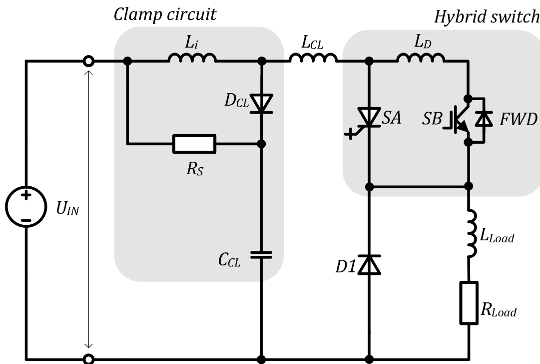

Fig. 3. Configuration of the commutation circuit

VSI topologies and includes the clamp circuit, hybrid switch, D1 (representing FWD of the opposite HS) and inductive load. The inductances L_{CL} and L_D represent the stray inductance of the clamp and the stray inductance between the IGCT and IGBT housings, respectively. The values of these inductances should be minimized in order to meet the specified SOA of the devices. The clamp circuit typically used in IGCT applications limits the surge reverse-recovery current of the turning-off freewheeling diodes and generally consists of a *dI/dt* limiting inductor L_i, a clamp capacitor C_{CL}, a clamping diode D_{CL} and a resistor R_S. In the case of a failure, the clamp inductance limits the short circuit current as well.

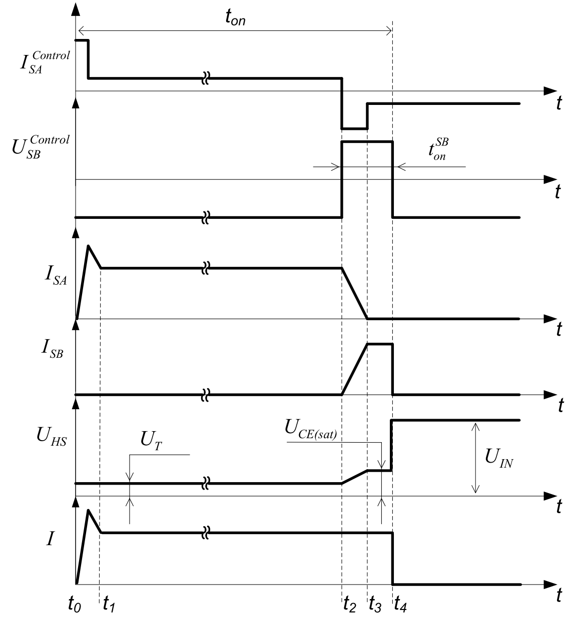

Fig. 4. Generalised operation principle and switching waveforms of the proposed HS

The generalised HS operation principle is shown in Fig. 4 and the following time intervals during the operation period can be distinguished:

t_0 – the beginning of each switching period of PWM. The thyristor SA of the HS is turned on by the control signal, applying full load current. During this time the transistor of the HS is turned off.

t_0-t_1 – freewheeling diode reverse-recovery process, duration and behaviour are dependent on the diode type and *dI/dt*.

t_1-t_2 – thyristor is conducting with low losses. The voltage across the HS determined by the voltage drop across the thyristor U_T.

t_2 – the turn-off control impulse is applied to the thyristor and simultaneously the turn-on impulse is applied to the transistor SB of the HS.

t_2-t_3 – as the turn-on behaviour of the IGBT is faster than the turn-off transient of the IGCT, the thyristor turn-off process occurs when the transistor is already in the on-state. The load current is distributed between both semiconductors.

t_3 – the SA returns to the blocking state, the full load current is applied to the transistor SB. Hence, the turn-off transient of the thyristor occurs when the voltage is limited to the voltage drop $U_{CE(sat)}$ across the conducting transistor SB of the HS. Moreover, during the current transfer to the transistor the voltage across its terminals is limited to the voltage drop across the SA during the on-state. The required duration of the

transistor on-state should not be shorter than the turn-off transient of the thyristor.

t_4 – the turn-off of the HS occurs by applying negative gate voltage to the transistor after the thyristor returns to the blocking state. The turn off transient of the HV IGBTs is generally 2…7 µs. After the transistor is switched off, the voltage across HS and all its components become equal to the supply voltage.

III. Simulation Model

A. Simulation circuit

To simulate the HS operation the commutation circuit shown in Fig. 3 was modelled in PSpice software using idealised switch models. The same diode model was used in the topology for simplicity and the following simulation parameters were assumed: the input voltage is 2800 V, the maximum load current is 750. The values of the circuit's passive components are determined according to [9].

B. Control algorithm

Active states are generated using two-phase shifted triangle waveform generators operating with constant frequency and duty cycle and two comparators. Additional logic elements ensure that the SB is turned on right at the instant the turn-off of SA occurs (Fig. 5).

In real conditions the minimal and maximal duty cycle of the HS could be limited by a number of factors, such as IGCT gate driver limitations or behaviour of the clamp circuit and a turn-off snubber (if used). The minimal off-state time $t_{off(min)}$ should be maintained to stay within the safe operating area (SOA) of the circuit's components. The minimal on-state time $t_{on(min)}$ of the HS is generally not limited since during an operation with duty cycles near zero, only the transistor of the HS could be used. The example of SOA control flowchart is shown in Fig. 6.

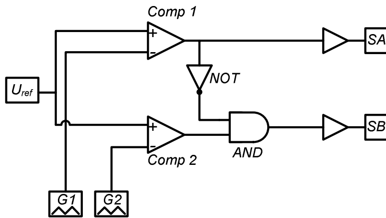

Fig. 5. Control algorithm of the HS

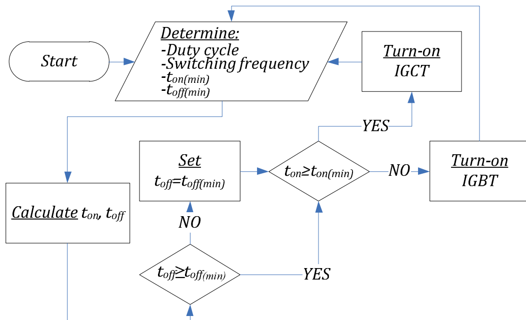

Fig. 6. Generalised SOA control flowchart of HS

The simulations confirm the estimated behaviour of the proposed switch configuration. At turn-on the HS operates like an IGCT with the *dI/dt* clamp (Fig. 7). The on-state voltage of the HS is equal to the voltage drop across the thyristor during its conducting period (Fig. 8). During turn-off of the HS the transistor is turned on for a short period; the turning-off thyristor current is then transferred to the transistor, which is closed right after the thyristor current becomes zero. The turn-off dynamics of the HS are greatly increased, while the excellent on-state characteristics of IGCT remain (Fig. 9) and all the elements are operated within the SOA.

IV. Generalised Loss Evaluation

The power loss estimation is one of the key points, crucial for the circuit mechanical structure and the cooling system design. The aim is to compare the power losses and performance of the proposed switch configuration with transistor- and thyristor-only counterparts at similar operation parameters. In the comparison, a variable switched current of 350A < I < 900A and U_{DC}=2800 V is assumed. The total losses P_{tot} are calculated as the sum of conduction, turn-on and turn-off losses at maximum junction temperature (125°C) using the datasheet values of the devices.

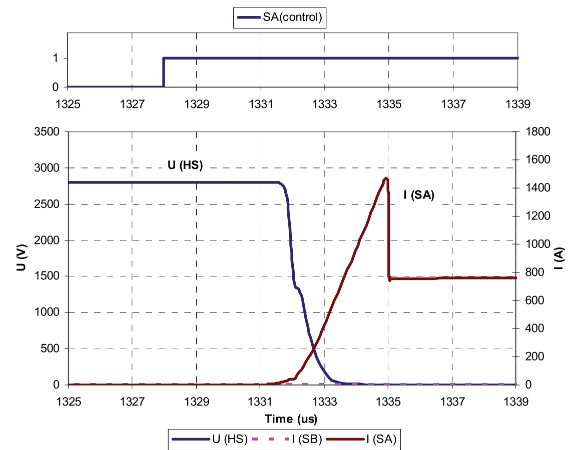

Fig. 7. Simulated turn-on behaviour of HS at I=750 A, U_{DC}=2800 V

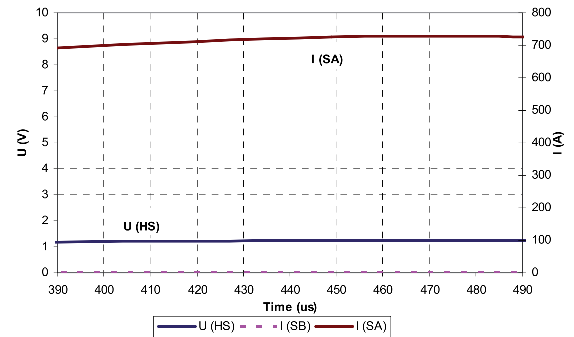

Fig. 8. Simulated conduction behaviour of HS at I=750 A, U_{DC}=2800 V

In the simulations of losses, the minimum IGBT switching losses with a very small gate resistances of R_{Gon}=4 Ω and R_{Goff}=2.5 Ω are assumed. In real industrial converters the IGBT gate units are adjusted to generate the desired *dI/dt* and *dU/dt* to avoid large voltage and current spikes during transients. However, the use of the gate resistor to control the *dI/dt* results in substantially higher switching losses in IGBT [10]. If a *dI/dt* limiting turn-on snubber is used with both IGBT and IGCT devices, the turn-on losses would be similar [11]. On the other hand, the turn-off losses of the device may increase slightly [12].

The turn-off losses of the IGCT were excluded in the simulations; however, according to the test results presented in the previous papers [13], the turn-off losses may not be completely removed due to several factors. Firstly, for a large area device, such as the IGCT, a significant output capacitance must be charged in order to establish the depletion region to support voltage. Another factor is the free carriers which had not recombined being swept from the junction. Nevertheless, an 89% reduction in turn-off losses was reported in [14]. In real conditions, the power losses of industrial applications could be distinctly higher than the simulated values.

After the turn-on of the IGBT, the current distribution between conducting IGBT and IGCT is mainly influenced by different characteristics of the semiconductors, temperature differences and asymmetrically distributed stray inductances in the circuit [15][16] Assuming both semiconductors in conducting state, the current sharing inside the HS neglecting cell resistances and inductances can be calculated by

$$k_I = \frac{I_{SA}}{I_{SB}} = \frac{U_{CE(sat)}(I)}{U_T(I)} \qquad (1)$$

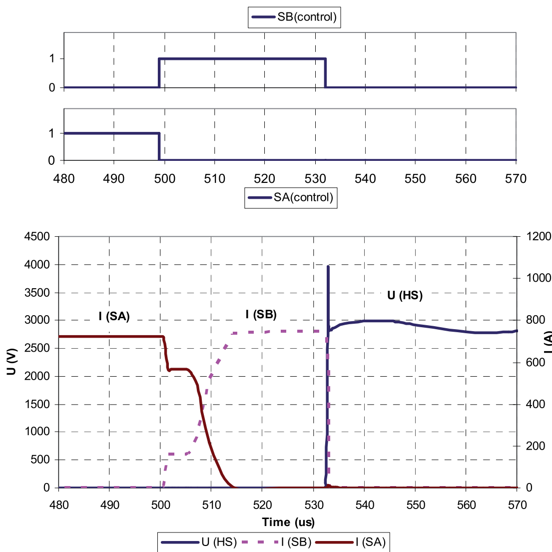

Fig. 9. Simulated turn-off behaviour of HS at I=750 A, U_{DC}=2800 V

Using Eq. (1) the IGBT and IGCT currents could be obtained by

$$I_{SB} = I \cdot \frac{1}{1+k_I} \qquad (2)$$

$$I_{SA} = I \cdot \frac{k_I}{1+k_I} \qquad (3)$$

According to simulations, the considered IGCT is showing better dynamics for currents above 650 A, whereas the IGBT is performing better at lower currents (Fig. 10). The proposed switch configuration is estimated to provide 2.3…2.8 times increased switching frequency in comparison to single hard switched IGBT or IGCT with *dI/dt* clamp circuit exhibiting the same power dissipation of 3 kW. Assuming the same switching frequency in the range of 250…1050 Hz and switch current of 750 A the IGBT performs better than IGCT at frequencies above 450 Hz, whereas the HS provides substantial (1.9…2 times) decrease in power losses in comparison to single semiconductors (Fig. 11). Fig. 12 shows average losses of all considered switch solutions operating in the studied circuit with the wide range of duty cycles. The IGBT performs better than IGCT up to D=0.85. Again, the HS shows substantially (1.8…2.2 times) reduced power dissipation in comparison to single semiconductors.

Unlike in the case of the typical parallel connection of identical semiconductors, in the proposed HS both switches are conducting full input current during the operation, thus the current rating of both semiconductors must be sufficient. On the other hand, the overall power dissipation is decreased in comparison with single switches allowing one to increase the switching frequency or reduce cooling system requirements. Moreover, if one of the semiconductors fails, the other one can still continue to operate independently unless sufficient cooling is applied.

The economical feasibility of the HS implementation greatly depends on the application and its operation conditions. The comparison of semiconductor prices of discussed switch configurations is shown in Fig. 13. It should be mentioned, that semiconductor price is only a part of the overall power electronic system. The prices of the passive components greatly vary for different applications and are not considered in this paper.

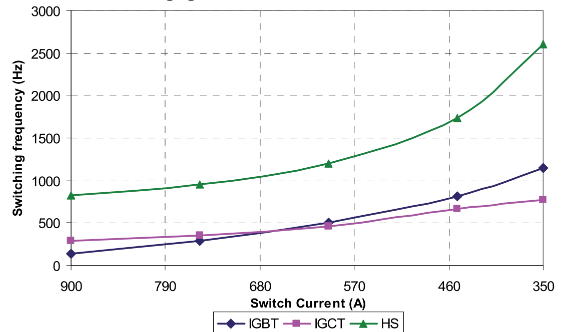

Fig. 10. Switch switching frequency vs. current for different semiconductor configurations corresponding to 3 kW total power dissipation at U_{DC}=2800 V, D=0.5

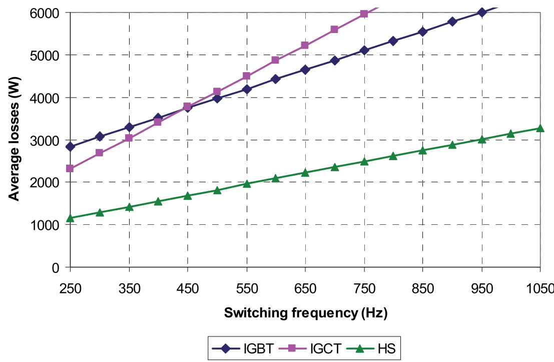

Fig. 11. Switch power dissipation vs. switching frequency for different semiconductor configurations at I=750 A, U_{DC}=2800 V, D=0.5

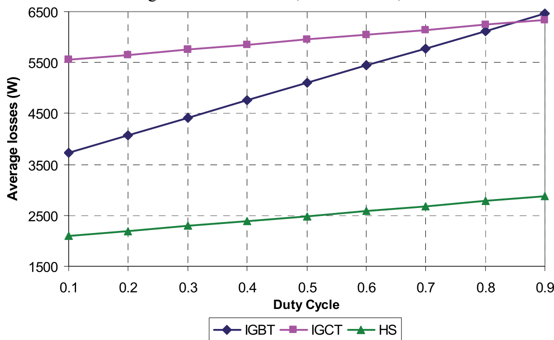

Fig. 12. Switch power dissipation vs. duty cycle for different semiconductor configurations at I=750 A, U_{DC}=2800 V, f_{sw}=750 Hz

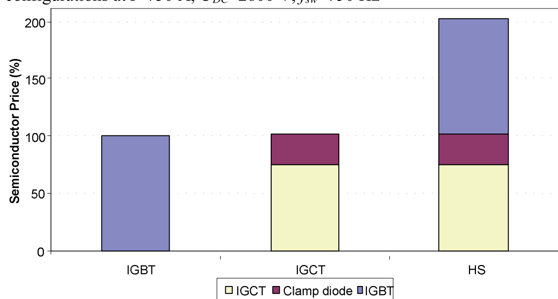

Fig. 13. Comparison of semiconductor prices of studied switch configurations

V. Conclusion

Using commercially available 4.5 kV class IGBTs and IGCTs in press-pack housings it is possible to create energy efficient switches with essentially decreased power losses. Despite having decreased maximum current capabilities in comparison with parallel connected identical transistors or thyristors and a higher price than single semiconductor switches, the proposed switch configuration could be beneficial in rolling stock converters or other applications where higher switching frequencies are required or decreased cooling system requirements are essential.

The future research will include construction of the hybrid switch prototype, improvement of the simulation model according to test results as well as investigation of the benefits it could provide in modern converter topologies.

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