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DOCTORAL THESIS

Design and Control of Bidirectional Step-Up/Down Partial Power Converters for DC Microgrid Applications

Naser Hassanpour

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Declaration:
Hereby, I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology, has not been submitted for doctoral or equivalent academic degree.

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signature

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Alalisvoolu mikrovõrkudele osavõimsuse töötlusega kahesuunalise tõste-langetusmuunduri projekteerimine ja juhtimine

NASER HASSANPOUR

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Contents

List of Publications

The list of author's publications, on the basis of which the thesis has been prepared:

I Hassanpour, N., Blinov, A., Chub, A., Vinnikov, D., & Abdel-Rahim, O. (2021, November). A series partial power converter based on dual active bridge converter for residential battery energy storage system. In 2021 IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON) (pp. 1–6). IEEE, doi: 10.1109/RTUCON53541.2021.9711725.

II Hassanpour, N., Chub, A., Blinov, A., & Vinnikov, D. (2022, June). Comparison of full power and partial power buck-boost dc-dc converters for residential battery energy storage applications. In 2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG) (pp. 1–6). IEEE, doi: 10.1109/CPE-POWERENG54966.2022.9880862.

III Hassanpour, N., Chub, A., Blinov, A., & Vinnikov, D. (2023). Soft-switching bidirectional step-up/down partial power converter with reduced components stress. *IEEE Transactions on Power Electronics*, 38(11), 14166–14177, doi: 10.1109/TPEL.2023.3289061.

IV Chub, A., Hassanpour, N., Yadav, N., Jalakas, T., Blinov, A., & Vinnikov, D. (2024). Analysis of design requirements and optimization possibilities of partial power converter for photovoltaic string applications in DC microgrids. *IEEE Access*, *12*, 14605–14619, doi: 10.1109/ACCESS.2024.3354375.

V Yadav, N., Chub, A., Hassanpour, N., Blinov, A., & Vinnikov, D. (2025). Protection and Control Implementation for Bidirectional Step-Up/Down Partial Power Converter for Droop-Controlled DC Microgrids. *IEEE Transactions on Industry Applications*, doi: 10.1109/TIA.2025.3561767

VI Hassanpour, N., Chub, A., Yadav, N., Blinov, A., & Vinnikov, D. (2024). High-Efficiency Partial Power Converter for Integration of Second-Life Battery Energy Storage Systems in DC Microgrids. *IEEE Open Journal of the Industrial Electronics Society*, pp. 847–860, 2024, doi: 10.1109/OJIES.2024.3389466.

Author's Contribution to the Publications

Contribution to the papers in this thesis are:

I Naser Hassanpour, as the main author of this conference paper, carried out analytical calculations and simulations. He also wrote and submitted the paper to the RTUCON 2021 conference at Riga Technical University. Naser Hassanpour presented the paper physically at the RTUCON 2021 conference in Riga, Latvia.

II Naser Hassanpour, as the main author of the paper, created a methodology to compare the partial power converter and full power converter. He also simulated both converters and wrote the paper's draft version. Naser Hassanpour prepared the final version of the paper, submitted it, and presented it online at the CPEPOWERENG 2022 conference in Birmingham, United Kingdom.

III Naser Hassanpour, as the main author of this journal paper, carried out analytical calculations and simulations, designed and assembled a prototype, and performed experimental verification of the theoretical analysis results and converter performance. He also created the structure of the paper in collaboration with his supervisors, wrote the draft version, and revised it to prepare the final version. Naser Hassanpour also prepared the response letters and revised the paper during peer review.

IV Naser Hassanpour, as the second author, proposed the topology morphing techniques for the converter and was responsible for testing the converter with different modulations and conditions. He also collected all the required experimental data to prepare the plots and waveforms. He also took part in the peer-review process of the paper.

V Naser Hassanpour, as the third author of this journal paper, examined the converter model against different fault conditions and developed the appropriate protection methodology to safeguard the converter in each scenario. He also conducted PSIM simulations to confirm the effectiveness of these methods. He also cooperated with his colleague, Neelesh Yadav, to carry out experimental tests to verify the functionality of the protection strategies.

VI Naser Hassanpour, as the main author, developed a guideline for designing a PPC for a second-life battery energy storage system. He developed a firmware for the converter based on droop control and a state machine to control the converter, combining different modulation strategies to ensure the smooth operation of the converter in different conditions. He prepared the structure and wrote the paper. He also designed the final prototype of the PPC to test it in real-world conditions and collect the data for the paper. Naser Hassanpour submitted the final version of the paper to the Open Journal of Industrial Electronics Society and then prepared all the response letters and revisions in the peer-review process.

Abbreviations

AC	Alternative Current
BBFPC	Buck-Boost Full Power Converter
BESS	Battery Energy Storage System
BDSUD	Bidirectional Step-Up/Down
BMS	Battery Management System
CSF	Component Stress Factor
CLF	Component Load Factor
CCSF	Capacitor Component Stress Factor
CSFB	Current Source Full Bridge
CS	Current Source
CCM	Continuous Conduction Mode
DAB	Dual Active Bridge
DPSM	Dual Phase Shift Modulation
DC	Direct Current
EV	Electric Vehicle
ESR	Equivalent Series Resistance
EMI	Electromagnetic Interference
FPC	Full Power Converter
FB	Full Bridge
FBK	Flyback
HV	High Voltage
IPOS	Input Parallel Output Series
ISOP	Input Series Output Parallel
IC	Integrated Circuit
LV	Low Voltage
LPF	Low Pass Filter
MCB	Mechanical Circuit Breaker
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOV	Metal Oxide Varistor
OC	Open Circuit
PSFB	Phase Shift Full Bridge
PPC	Partial Power Converter
PV	Photovoltaic
PSM	Phase Shift Modulation
PWM	Pulse Width Modulation
PCB	Printed Circuit Board
RCD	Resistor Capacitor Diode
RMS	Root Mean Square
SCSF	Switch Component Stress Factor
SMC	Secondary Modulated Converter

SPSM	Single Phase Shift Modulation
SoC	State of Charge
SC	Short Circuit
SSCB	Solid State Circuit Breaker
SiC	Silicon Carbide
SoH	State of Health
TPSM	Triple Phase Shift Modulation
TVS	Transient Voltage Suppressor
TMC	Topology Morphing Control
VS	Voltage Source
V2G	Vehicle to Grid
V2H	Vehicle to Home
WCSF	Winding Component Stress Factor
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching

Symbols

φ_{boost}	Phase shift in the boost mode (rad)
φ_{buck}	Phase shift in the buck mode (rad)
C_{oss}	Output capacitance of the switch
D_{rev}	Duty cycle of the reverse power flow period
D_s	Duty cycle of the shoot-through state
D_{lv}	LV port switches duty cycle
D_{hv}	HV port switches duty cycle
D_a	Duty cycle of the active power transfer period
f_r	Resonance frequency
f_{sw}	Switching frequency
G_{boost}	Voltage gain of the DC-DC stage in the boost mode
G_{buck}	Voltage gain of the DC-DC stage in the buck mode
K_{pr}	Coefficient of partiality
I_{in}	Input current
I_O	Output current
I_C	DC-DC stage output/input current
L_{eq}	Leakage Inductance of the transformer
$L_{eq,m}$	Leakage Inductance of the main transformer
$L_{eq,sn}$	Leakage Inductance of the snubber transformer
n	Turns ratio of the transformer
n_m	Turns ratio of the main transformer
n_{sn}	Turns ratio of the snubber transformer
Q_{rr}	Reverse recovery charge of the transistor's body diode
$R_{ds\text{-}on}$	On resistance of the switch
t_{red}	Redistribution time interval
t_{res}	Resonance time interval
V_{BR}	Breakdown voltage
V_{in}	Input voltage
V_O	Output voltage
V_b	Batter voltage
V_{dc}	DC microgrid voltage
V_C	Series capacitor voltage

1 Introduction

1.1 Background

The growing concern over climate change has highlighted the significant role that buildings play in global carbon dioxide (CO_2) emissions, accounting for approximately 40% of total emissions worldwide. In response to this environmental challenge, the European Union (EU) has enacted legislation that mandates the transition toward zero-emission buildings (ZEBs) [1]. Achieving this transformation requires a shift to more sustainable energy systems, with the integration of renewable energy sources, particularly Photovoltaic (PV) panels, being a key strategy for reducing emissions in buildings [2].

Microgrid technology, whether direct current (DC) or alternating current (AC), plays a key role in optimizing energy distribution and storage. A residential power system, as shown in Figure 1.1, utilizing a 350 V DC microgrid, provides a stable and efficient framework for energy distribution. DC microgrids enhance efficiency by up to 15% by eliminating AC–DC conversion losses [3], [4]. However, the intermittent nature of renewables necessitates the use of energy storage systems (ESS) to maintain grid stability. ESSs enhance energy management, with battery energy storage systems (BESS) proving economically viable in many locations, particularly in improving PV self-consumption [3]. Second-life battery storage solutions further optimize energy use and sustainability [5], [6].

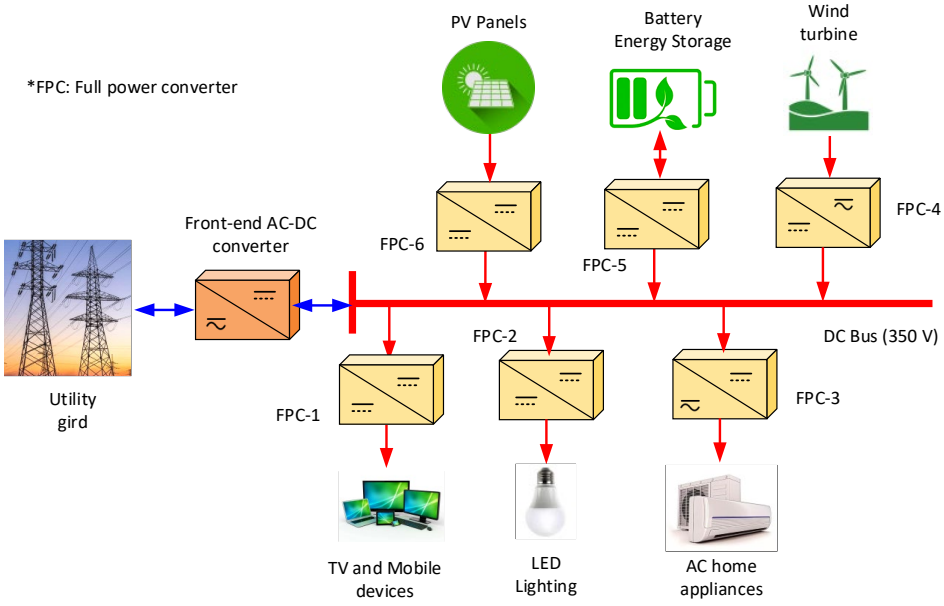

Figure 1.1. Generalized representation of 350 V DC microgrid-based residential power system.

In conventional systems, full power converters (FPC) are commonly employed to handle the power conversion between renewable energy sources and storage systems. However, full-power converters have certain drawbacks due to processing the entire power. These limitations reduce the overall efficiency of the system, highlighting the need for more advanced and efficient solutions. One promising concept that offers higher efficiency with high power density is Partial Power Processing (PPP). Initially

introduced in the spacecraft industry to reduce the size and weight of power converters, PPP has since evolved to significantly enhance the efficiency of renewable energy systems, including PV systems and energy storage [7]. The core principle of PPP is to process only a portion of the total power rather than the entire load, which reduces power losses and minimizes stress on system components. This is achieved in Partial Power Converters (PPCs), which can be rated only for a fraction of power and achieve unattainable efficiency levels for full-power converters.

1.2 Motivation of the Thesis

The rapid development of renewable energy systems, particularly solar photovoltaic (PV) technology and energy storage solutions such as batteries, has driven the need for efficient, reliable, and cost-effective power conversion systems. One of the key challenges in these systems is transferring power from sources such as PV panels or batteries to the load while maintaining energy efficiency and minimizing costs. Although widely used, traditional full-power converters often come with high component count, complexity, and costs, especially in low-power applications such as residential energy systems.

In contrast, PPC technology offers significant advantages over full-power converters, particularly in applications where the voltage difference between the source (e.g., a PV array or battery) and the load is relatively small. By processing only a portion of the total power, PPC systems offer a more efficient solution, reducing energy losses, component stress, and overall system costs. A visual representation of both systems is depicted in Figure 1.2, where P_p is the amount of processed power in a PPC, η_C is the DC-DC stage efficiency, and η_{sys} is the overall system efficiency. It can be seen from (1) that minimizing the processed power significantly increases the overall system efficiency, which is desirable for a PPC design.

The application of PPCs becomes especially beneficial in residential applications, where the power requirements are typically modest, and the cost-effective integration of renewable energy and storage systems is crucial. As microgrids become increasingly central to the future of energy management, PPCs have the potential to make energy systems more reliable, adaptable, and cost-effective for both residential and industrial applications. An illustration of a PPC-based DC microgrid is shown in Figure 1.3.

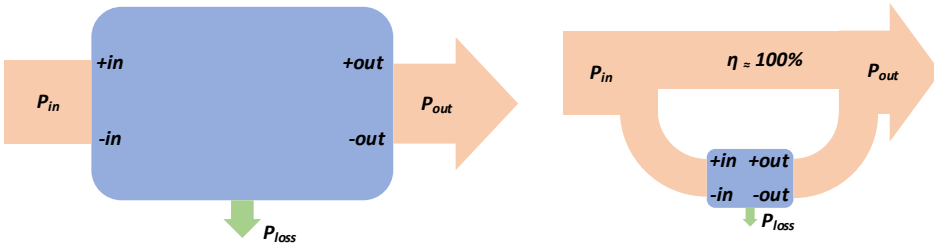

Figure 1.2. Representation of power flow paths (a) FPC (b) PPC.

$$FPC: \eta_{sys} = \eta_C = \frac{P_{out}}{P_{in}} \tag{1}$$

$$PPC: \eta_{sys} = 1 - \frac{P_P}{P_{out}}(1 - \eta_C) \tag{2}$$

This thesis examines the benefits and some potential use cases of PPCs in residential energy systems, with a focus on battery energy storage systems. By investigating the practical implementation aspects, performance improvements, and economic benefits, this work aims to contribute to the development of more efficient and affordable solutions for integrating renewable energy sources in residential buildings. This thesis also examines the use of PPCs to optimize the integration of second-life electric vehicle (EV) batteries, specifically lithium-iron-phosphate (LFP) batteries, into residential energy systems. As the availability of used EV battery cells increases, repurposing these batteries offers a sustainable and cost-effective solution for residential energy storage. By incorporating these second-life batteries into a DC microgrid, residential systems can benefit from affordable, reliable storage that would provide improved energy management, maximizing the self-consumption of renewable energy and reducing reliance on the utility grid.

This thesis also investigates efficient DC-DC energy conversion, focusing on step-up/down PPC. The most scalable versions of these converters employ galvanically isolated DC-DC topologies. Nevertheless, some of these topologies encounter difficulties like poor current controllability at zero voltage and excessive stress on components. The thesis proposes protection for partial-voltage-rated semiconductors, soft start, and multimode control as potential solutions to these issues. The efficacy of these methods is supported by experimental findings, which demonstrate that partial power converters can be effectively utilized in real-world applications.

This research was carried out in alignment with one of the focus areas of the Power Electronics Group at Tallinn University of Technology. The objective is to explore power conditioners and design an efficient power electronics interface to integrate second-life EV batteries or PV modules into a DC microgrid, addressing issues related to power conversion and overall system efficiency. This research received direct support from the target financing research PRG1086, funded by the Estonian research council, and TK230U2, funded by the Ministry of Education and Research.This research was supported by the Estonian Research Council grant PRG1086 and by the Estonian Centre of Excellence in Energy Efficiency, ENER (grant TK230) funded by the Estonian Ministry of Education and Research.

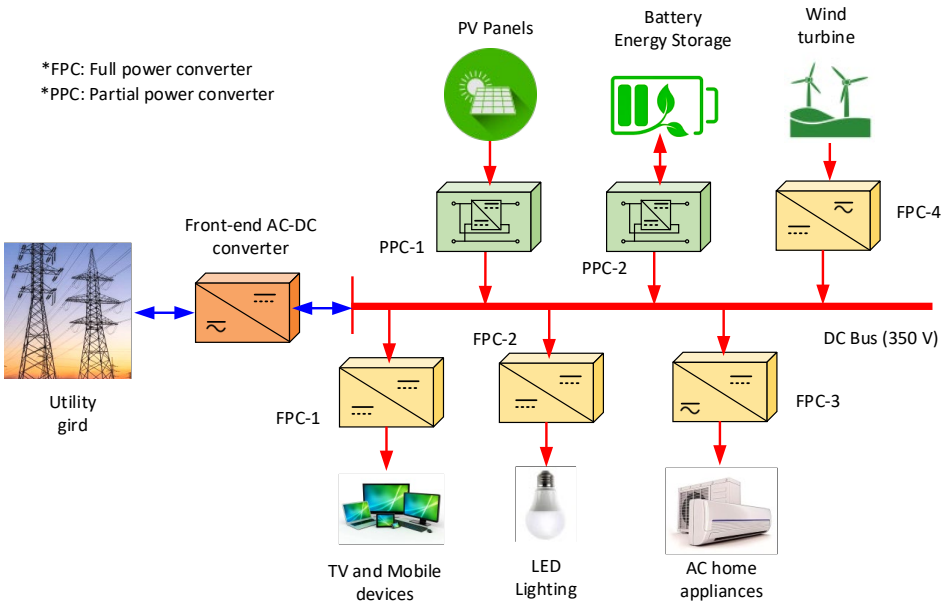

Figure 1.3. Generalized representation of 350 V DC microgrid based residential power system incorporating partial power converters.

1.3 Aim, Hypotheses, and Research Tasks

The aim of this PhD project is to develop a step-up/down power converter (PPC), taking advantage of its superior characteristics compared to step-up or step-down PPCs. The ultimate goal of the work is to experimentally validate the applicability of the developed converter as an interface between a second-life battery energy storage system and a residential DC microgrid. To achieve this, the existing literature must be reviewed, and the gap between the practical and non-practical solutions must be recognized. The developed PPC must encompass all the enhancements that hinder the adoption of the converter in a real-world DC microgrid application. Besides an efficiency target, the converter's dynamic behavior and issues arising from faulty conditions or critical operation points need to be addressed. Eventually, a TRL4 PPC was implemented, which is currently undergoing daily tests in the Residential DC Innovation Hub of the Tallinn University of Technology.

Hypotheses:

1. Application of current source topologies in step-up/down PPCs could avoid high cumulative component stress factor caused by wide DC gain operation range of DC-DC stage.
2. In addition to protection capabilities, the integration of the solid-state circuit breaker could enable features like soft start and improved current controllability in step-up/down PPCs.
3. Regulation capabilities and efficiency of step-up/down PPCs could be improved by implementing topology morphing control without hardware modifications.
4. Circulating power/energy could be harnessed for controlling the series port current near and at zero partiality.

Research Tasks:

1. To review the literature in the field of PPC technology and assess their application possibilities.
2. To identify the key performance indicators (KPI) of the PPC converters and analyze different solutions based on these indicators using simulation models.
3. To analyze the bidirectional step-up/down PPC concept based on the current source DC-DC converter and compare it with existing solutions regarding KPIs.
4. To develop a proof-of-concept prototype of bidirectional step-up/down PPC based on the current source full bridge DC-DC converter and assess its limitations.
5. To develop protection strategies for short circuit and open circuit faults and a soft start strategy utilizing solid-state circuit breaker, existing converter components, and available control and modulation methodologies.
6. To develop a control algorithm based on phase shift modulation and enhance it using various methods like topology morphing control to ensure smooth operation of the converter within the entire operation range.
7. To assess, implement, and validate a method of reducing voltage stress on semiconductor devices.
8. To implement a droop control method that utilizes bidirectional step-up/down PPC in all four quadrants, allowing it to act as an interface between battery energy storage and DC microgrid.
9. To develop guidelines for the practical design of bidirectional step-up/down PPCs interfacing battery energy storage to droop-controlled DC microgrid.
10. To develop the final experimental prototype considering all the enhancement techniques and verify its application in the residential DC microgrid.

1.4 Research Methods

The research presented in this work employs mathematical analysis, PSIM simulation, and experimental methods to investigate various types of series-connected partial power converters. It examines the voltage and current stresses on components and assesses the control effectiveness of various converter designs under identical conditions. Theoretical models are developed using volt-second and amp-second balances to establish voltage gain and current stress. The expressions (1) and (2) state the volt-second and current-second balance, respectively. An illustration of the volt-second balance and the current-second balance is given in Figures 1(a) and 1(b), respectively.

$$\left\langle v_{L(t)} \right\rangle = \frac{1}{T_{SW}} \cdot \left(\int_0^{T_{SW}} v_L(t).dt \right) = 0 , \tag{1}$$

$$\left\langle i_{C(t)} \right\rangle = \frac{1}{T_{SW}} \cdot \left(\int_0^{T_{SW}} i_C(t).dt \right) = 0 , \tag{2}$$

where $\langle v_{L(t)} \rangle$ and $\langle i_{C(t)} \rangle$ are average inductor voltage and capacitor current, correspondingly. Instantaneous values are represented by v_L and i_C. The switching period is designated by T_{sw}.

Stress factors could be used to compare stresses on the components, along with other metrics like non-active power defined in IEEE 1459-2010 standard.

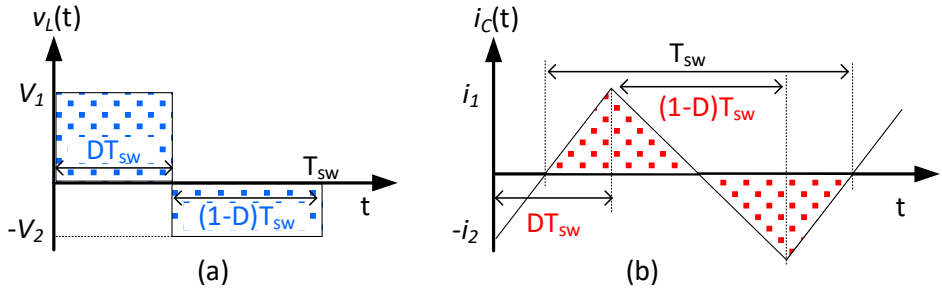

Figure 1.3. Steady-state converter analysis methods: (a) volt-second balance in an inductor and (b) current-second balance in a capacitor.

Methods for increasing efficiency and reducing power loss are also examined. The theoretical models are validated, and the behavior of the converters under various conditions is investigated using PSIM simulation. Tests are conducted in the Power Electronics Research Laboratory at TalTech, utilizing prototype converters with varying loads and voltage levels. During the test process, devices such as an oscilloscope, voltage and current probes, a thermal camera, programmable DC power supplies, and a precision power analyzer were used to carry out various tests and collect the required data. Second-life battery stacks are also assessed to determine their compatibility with partial power converters, and their data is entered into the programmable DC power supply to emulate their behavior. The experiments confirm that the converters operate effectively under droop control, transitioning seamlessly between voltage step-up and step-down modes, reaching an efficiency of 99.45%.

Furthermore, tests are conducted in real-world conditions at the TalTech Residential DC Innovation Hub, which exhibits variations in microgrid voltage and solar irradiance, to ensure reliability. Various testing scenarios are developed, and the experimental data is thoroughly analyzed. The results demonstrate that partial power converters offer significant efficiency, compactness, and cost-effectiveness advantages, positioning them as a viable solution for industrial applications.

1.5 Contributions and Disseminations

The outcomes of this research have been disseminated through multiple journal papers and presentations at various IEEE conferences and doctoral schools. The author's research contributions include ten papers published in IEEE peer-reviewed journals, one book chapter, and eleven presentations at IEEE-indexed international conferences. The PhD dissertation is based on six main publications, including four journal papers and two conference presentations at IEEE conferences.

Scientific novelties:

- Demonstration of poor voltage and current regulation performance of step-up/down PPCs based on voltage-source DC-DC topologies near zero partiality.
- Derivation of topology and analytical model of novel step-up/down PPC based on DC-DC stage with a four-quadrant current source LV port and reduced stress of the components.

- Development of hybrid modulation and topology morphing control (TMC) techniques for step-up/down PPCs, which enable PPC operation near zero partiality by regulating the amount of circulating energy.
- Method for implementing soft start and short circuit and open circuit protection in step-up/down PPCs based on current source DC-DC topologies.

Practical Novelties:

- Design guidelines for step-up/down PPCs interfacing battery energy storage into DC microgrid.
- Implementation approach for a closed-loop control system that provides smooth transitions between converter operation modes in all four quadrants.
- Implementation approach minimizing voltage stress in low voltage series port of step-up/down PPC based on DC-DC stage with a four-quadrant current source LV port.
- Development and verification of droop-control implementation method for step-up/down PPC aimed at DC microgrid application.
- Development and demonstration of a fully operational prototype for battery energy storage with extremely high efficiency.

1.6 Experimental Setup and Instruments

The Power Electronics Laboratory at Tallinn University of Technology was utilized to construct the experimental setups and conduct various tests. The laboratory setup includes a mixed-signal oscilloscope (Tektronix MSO4034B) for capturing current and voltage waveforms, AC/DC current probe (Tektronix TCP0030A) for current measurement, differential voltage probes (Tektronix P5205A) for voltage measurement, precision power analyzer (Yokogawa WT1800E) for efficiency measurements, battery and DC microgrid emulators (iTECH IT6006C-800-25 and iTECH IT60012C-500-50), a microcontroller (STM32G474) board, and a thermal camera (Fluke Ti10).

1.7 Thesis Outline

The second chapter reviews the PPC technology and compares the three voltage conversion types. Moreover, it lists the requirements for the selection of an appropriate DC-DC topology according to the application and key performance indicators.

Chapter 3 introduces a novel step-up/down PPC based on DC-DC stage with a four-quadrant current source LV port and compares it with a dual active bridge (DAB)-based solution to confirm its superior characteristics.

Chapter 4 explains the possible enhancement techniques for the proposed PPC to overcome the practical issues arising from fault conditions, mode change, or critical operation points.

The guidelines for designing a PPC for interfacing a BESS into a droop-controlled residential DC microgrid are presented and verified in Chapter 5.

Chapter 6 provides a short overview of the possible future work needed in the topic of the thesis research work.

2 State of the Art PPC Configurations and Topologies

The main application of a PPC is to regulate the voltage difference between two ports, which can be defined as input/output or source/load. The examples of these voltage regulations will be discussed in the following sections. The main feature of PPCs is that they process a fraction of active power between two ports while the rest of the power is delivered without process through an ideally lossless path. There are various options for connecting a DC-DC converter with different structures to form a PPC. The type of DC-DC converter used inside the PPC system will be referred to as the "DC-DC stage topology," while the type of connection used to create the PPC system will be referred to as the "PPC configuration." The possible configurations are illustrated in Figure 2.1.

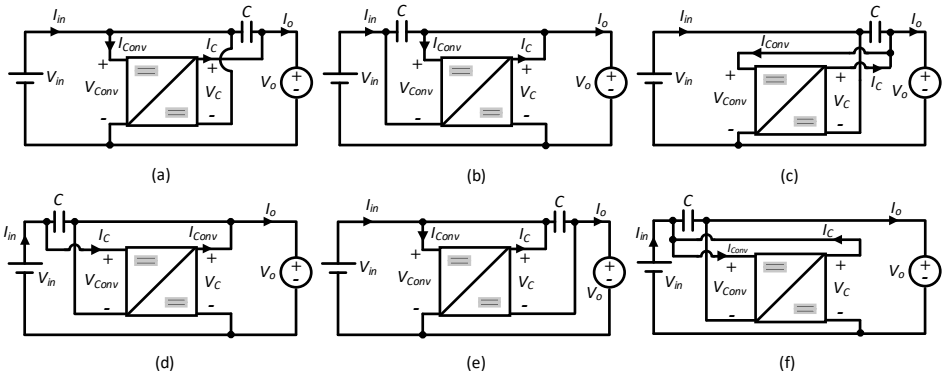

Figure 2.1. Possible PPC Configuration types utilizing isolated DC-DC topologies (a) IPOS, (b) ISOP-I, (c) ISOP-II, (d) ISOP, (e) IPOS-I, (f) IPOS-II.

In order to create a path for unprocessed power transfer between two ports, a series connection of these ports by a capacitor is needed. Depending on the position of this capacitor regarding the input or output of the DC-DC stage and the PPC, these configurations can be distinguished. The first one is the input parallel output series (IPOS), which is shown in Figure 2.1(a). The configurations in Figure 2.1(b) and (c) are input series output parallel (ISOP)-I and ISOP-II, respectively. Following the same naming pattern, the configurations in Figure 2.1 (d-f) are called ISOP, IPOS-I, and IPOS-II. It must be noted that the IPOS and ISOP are the most common PPC configurations utilized in the literature[7]-[9]. In most cases, the DC-DC stage must be an isolated converter to avoid a short circuit between both ports [7]. The requirements for the selection of the DC-DC topology will be discussed further in the following sections.

2.1 Definitions of PPC types (step-up, step-down, step-up/down) and application examples

The following equations can be derived by considering the most common configurations (IPOS and ISOP) and writing voltage/current equations for them.

$$\text{IPOS: } \begin{cases} V_O = V_{in} + V_C \\ I_{in} = I_O + I_{Conv} \end{cases} \quad (1)$$

$$\text{ISOP: } \begin{cases} V_{in} = V_O + V_C \\ I_O = I_{in} + I_{Conv} \end{cases} \quad (2)$$

where V_c is the output voltage of the DC-DC stage, V_{in} is the input port voltage, and V_{out} is the output port voltage. These equations mean that the voltage difference between input and output (Δv) is compensated by the output voltage of the DC-DC stage (V_c). In case of no voltage imbalance between two ports ($V_{in} = V_{out}$), the DC-DC stage ideally does not process any active power and remains idle [10]. Having a DC-DC topology with positive output and considering the IPOS configuration, the PPC system will be a step-up DC-DC converter. Negative V_c values will result in a step-down PPC. Finally, if the DC-DC stage is capable of changing its output voltage polarity in a series-connected port, the PPC will be a step-up/down DC-DC converter. Similar concepts are valid for the ISOP configuration, with the difference being that for the positive V_c values, the PPC will be a step-down converter.

The most critical parameter for any PPC is the proportion of power processed by the DC-DC stage relative to the total transferred active power, named in the literature as the coefficient of partiality (K_{pr}). Calculating this parameter for the series port shows that K_{pr} is determined by the ratio V_C/V_O. Consequently, the voltage difference between the ports, or the voltage regulation range of the PPC, defines the K_{pr} value and the PPC power rating [7], [8], and [10]. Hence, there is a strong dependency between the voltage regulation range and the converter power rating and size.

The design process for a PPC is highly application-oriented. As a first step, the voltage variation ranges of both the input source and output port must be defined. Historical data (2005–2014) from a PV module in São Martinho, Brazil, analyzing power level distribution relative to maximum power point voltage, indicates that 99.9% of the module's power is generated within approximately ±13.7% of the nominal voltage. Accordingly, by adopting a ±15% voltage variation range (relative Δv value of 30%), the design can effectively encompass the entire power generation range of the PV module [11], [12].

A series connection (98 cells) of Lithium-Ion batteries is considered for an EV battery pack with a voltage range of 2.8 V–4.2 V for each cell, resulting in a range of 274.4 V–411 V for the entire battery pack. In practice, the voltage range of the pack is limited by the battery management system (BMS). Therefore, a range of 330 V–390 V is considered for the system implemented in

[*13*]. For different battery technologies like Lithium Iron Phosphate (LiFePO4, LFP), Lithium Cobalt Oxide (LiCoO2, LCO), Lithium Manganese Oxide (LiMn2O4, LMO), and Lithium Nickel Manganese Cobalt Oxide (LiNiMnCoO2, NMC), this practical voltage range is a limited parameter that can be accurately selected as per application requirement [14].

The output side of a PPC is typically connected either to a DC microgrid, operating at 350 V (±30 V) for residential applications or 700 V for industrial applications, or to the DC link of an inverter. For inverters, the DC link voltage is typically 400 V for single-phase systems and > 650 V for three-phase systems. Since the voltage variation ranges for these applications are standardized, designers can accurately determine the total voltage regulation range for both ports, even under worst-case scenarios. Other output types must be analyzed based on the characteristics of the DC bus.

After determining the nominal voltage and the variation ranges for both the input and output ports, the next step is to select the appropriate voltage conversion type for the PPC, whether step-up, step-down, or step-up/down. In many applications, the nominal voltages and their variation ranges are dictated by the specific source, load, and

application requirements. This means that if any of the following conditions consistently apply to a particular application, the designer has to select the mentioned PPC type for each application

[*13*], [15]:

- **Step-up**: $V_{O,min} \geq V_{in,max}$
- **Step-down**: $V_{in,min} \geq V_{O,max}$
- **Step-up/down**: $V_{in,nominal} \approx V_{O,nominal}$

On the other hand, the flexibility of adjusting the nominal voltage at the input or output side, such as by varying the number of PV cells in a string or the number of series cells in a battery pack, enables the optimization of the converter characteristics and performance. By selecting the appropriate nominal voltage on each side, the designer can choose the best candidate among the three voltage conversion types to enhance the overall system efficiency and meet the specific application requirements. In such cases, the number of PV or battery cells can be chosen as per Table 2.1. For the battery and PV, each cell or module's min/max voltage must be put in Table 2.1 equations to obtain the desired number of cells or modules.

Table 2.1 Number of source cells for different PPC options [Paper I].

PPC type	Number of source cells
Step-up/down	$N_{Cells} \approx \frac{V_{O,nominal}}{V_{in,nominal}}$
Step-down	$N_{Cells} \geq \frac{V_{O,\max}}{V_{in,min}}$
Step-up	$N_{Cells} \leq \frac{V_{O,min}}{V_{in,max}}$

Considering a specific Δv for each type of source, the relationship between the minimum, maximum, and nominal voltages can be written as,

$$V_{in,max} = (V_{in,nominal} + \Delta v / 2) N_{Cells} \quad (3)$$

$$V_{in,min} = (V_{in,nominal} - \Delta v / 2) N_{Cells} \quad (4)$$

In a scenario where the output voltage remains constant, if the IPOS configuration is employed for the design procedure, there can be three options: step-up, step-down, and step-up/down PPCs. To minimize the active processed power for the step-up PPC, the maximum input can be selected as equal to the output voltage, so the active processed power by the DC-DC stage would be ideally zero at this point. This way, the worst-case operation point is the minimum input side voltage where the $K_{pr,max}$ will be $\Delta v/V_O$. On the other hand, with similar assumptions in mind, if the step-down solution is selected, the minimum input side voltage will be equal to the nominal output voltage, which ensures the processed active power will be again zero. In this case, the maximum processed power occurs at the highest input side voltage where $K_{pr,max}$ value, is $\Delta v/V_O$.

Finally, a DC-DC topology with a bipolar output voltage ($V_C \geq 0$ or $V_C \leq 0$) enables the step-up/down PPC implementation. In this condition, the nominal input voltage equals the output voltage and can vary below or above the output voltage. The advantage of

this scenario is that the voltage regulation range is divided into two parts above and below the nominal voltage ($\pm\Delta v/2$), resulting in the K_{prmax} value reaching $\Delta v/2V_O$ at the worst operation point.

2.2 Step-Up/Down PPCs and Their Requirements

It is evident that implementing a step-up/down PPC significantly decreases the power processed by the DC-DC stage compared to step-up or step-down PPCs. This reduction in the processed active power leads to a smaller converter size, increased power density, and enhanced overall system efficiency.

In [10], the difference between two PPCs based on full bridge (FB) and full bridge/push-pull (FB/PP) is analyzed. The latter one is capable of changing the voltage polarity at its output port. Hence, applying the same 30% voltage regulation range for both converters, the FB/PP-based PPC processed 112.5 W, whereas the FB PPC processed 225 W. This indicates that the DC-DC stage of FB/PP-based PPC handles half the active power compared to the FB PPC, enhancing the system efficiency (99.58% compared to 98.9%).

In [Paper I], a study evaluated the optimal PPC interfaces for connecting an NMC battery pack to a 350 V ±30 V residential DC microgrid. Using a nominal cell voltage of 3.6 V, the number of battery cells was determined according to Table 2.1. Two configurations were analyzed: the IPOS and the ISOP, both employing a current source full bridge (CSFB) based PPC. The findings in Figure 2.2 indicate that the K_{prmax} for step-up/down PPCs is 0.27 for the IPOS and 0.3 for the ISOP. In contrast, step-down and step-up PPCs exhibit significantly higher K_{prmax} values, as demonstrated in Figures 2.2(a) and 2.2(b), respectively.

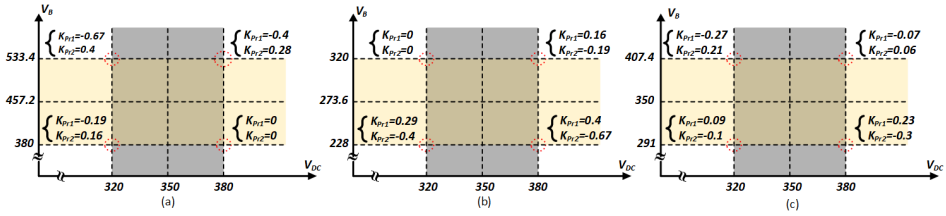

Figure 2.2. Coefficient of partiality considering battery voltage range and DC microgrid voltage range in IPOS (case 1) and ISOP (case 2) configuration for (a) step-down PPC (b) step-up PPC (c) step-up/down PPC [Paper I].

Although step-up/down PPCs offer a significant advantage in reducing processed active power, selecting an appropriate DC-DC stage topology requires careful consideration of several critical factors. Generally, the DC-DC stage can be a buck, a buck-boost, or a boost DC-DC converter. Implementing a step-up/down PPC using a boost converter makes no sense. When comparing buck and buck-boost topologies, the K_{pr} values for a PPC derived from the buck-boost topology can increase significantly, leading the DC-DC stage to handle substantial active power levels. Hence, the overall system efficiency will diminish, which is not desirable. Consequently, the only feasible candidates are buck topologies whose high voltage (HV) side can be connected to the parallel port and low voltage (LV) side to the series port of the implemented PPC.

In unidirectional applications like PV, fuel cells, LED drivers, and unidirectional power supplies, the DC-DC stage must be capable of changing voltage polarity at the LV port (V_C).

Therefore, to maintain a consistent power flow direction in the system, the current flow direction at the HV port will be reversed, leading to a change in the power flow direction within the DC-DC stage. Thus, regarding the V_C or I_{Conv}, the DC-DC stage topology is a two-quadrant converter. On the other hand, for bidirectional applications like BESS and EV chargers with vehicle-to-grid (V2G) or vehicle-to-home (V2H) features, both I_C and V_C have to be bidirectional and bipolar, respectively. Consequently, the DC-DC stage topology should be capable of operating as a four-quadrant converter to meet these criteria.

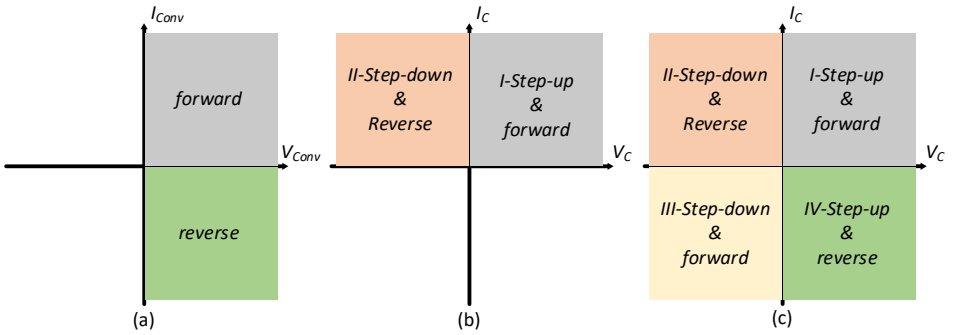

Figure 2.3. Operation quadrants of the DC-DC stage in step-up/down IPOS-based PPC for (a) HV side in both uni/bidirectional applications, (b) LV side in unidirectional cases, (c) LV side in bidirectional cases.

To fulfill these requirements, it's essential to use bipolar two-quadrant switches for unidirectional current flow and four-quadrant switches for bidirectional current flow in current source DC-DC stages or an unfolder circuit for voltage source structures. Additionally, the HV side should connect to the parallel port without inductive impedance, allowing the current flow direction to change instantly during transitions between step-up and step-down modes. Conversely, the LV side of the DC-DC stage requires inductive impedance to maintain consistent current flow direction while altering the voltage polarity (V_C). It's important to note that the current (I_C) cannot reverse direction instantaneously; it must first decrease to zero before inverting direction. Following these criteria, the modulation strategy should seamlessly change the converter modes from step-down to step-up, or vice versa, without hardware reconfiguration. On the HV side, frequently used structures like a full bridge, half-bridge voltage doubler, and push-pull can be implemented. On the other hand, the LV side can be formed by a full-wave center-tapped rectifier, current doubler, and the full bridge circuit accompanying the LC filter at the output. Other less common structures can also be utilized if they fulfill the requirements of the DC-DC topology discussed earlier.

Furthermore, the application of an isolation transformer or coupled inductor is essential to avoid short circuits between both ports. The design of the transformer is one of the crucial points of the PPC design procedure as it defines the voltage regulation range of the PPC and the amount of circulating non-active power within the converter components, which will be defined in later sections. It must be noted that the series connection of both ports eliminates the galvanic isolation between them. This point needs to be considered when the standards dictate the presence of isolation between ports.

To provide an overview of PPCs reported in the literature, Table 2.2 categorizes recent PPC designs based on configuration type and voltage conversion form. It can be seen that the predominant applications are in the domains of PV systems and BESS.

Table 2.2 PPC technology comparison among the published studies in recent years.

Ref	**PPC Config**	**Voltage Conversion type**	**DC-DC Stage Topology**	**Rated Power (*W*)**	**Application**	***K_{pr}***	***η_{max} (%)***	***Voltage level (Vin, Vo)***
[16]	IPOS	Step-Up	DAB	1000	PV-BESS	3.23-4.18	99.5	161.5, 200
[8]	IPOS	Step-Up	PSFB and Flyback	750	PV	0-0.43	99	154-220, 220
[15]	IPOS	Step-Up	PSFB	3200	EV Charger	0.2-0.33	98.4	300, 360-400
[17]	IPOS	Step-Up	DAB	3300	DC Microgrid	0.2-0.33	99	300, 360-400
[18]	IPOS	Step-Up	Flyback	48	LED Driver	0-0.56	98.73	N/A
[19]	IPOS	Step-Up	DAB	115	BESS	0.4-0.93	N/A	30, 51.7
[20]	IPOS	Step-Up	PSFB	1500	Wind Turbine	2.44-5.2	96.5	35-64, 220
[21]	ISOP	Step-Up	Flyback	44	PV	0.14-0.25	98	N/A
[22]	ISOP	Step-Up	FB	500	PV	0-0.09	99	190.4, 200
[23]	ISOP	Step-Up	Flyback	100	Power Supply	0-0.3	97	28-40, 40
[24]	IPOS	Step-Up	Flyback	100	PV	0-2	90	27.9-32.7, 32.7
[25]	ISOP	Step-Down	FB	1200	PV	0-0.37	99	230, 167
[26]	ISOP	Step-Down	LLC Resonant	100	DC-Bus Converter	2.57-4.26	96.74	36-72, 10-14
[27]	IPOS	Step-Down	FB	3500	BESS	0.04-0.3	98.2	50-58, 35-48
[*13*]	ISOP	Step-Down	PSFB	6500	EV Charger	0.133-0.289	99.11	450, 320-390
[10]	IPOS	Step-Up/Down	FB	750	PV	-0.13-0.18	99.58	187-253, 220
[28]	IPOS	Step-Up/Down	FB	10000	Fuel Cell	-0.21-0.35	N/A	N/A
[29]	IPOS	Step-Up/Down	FB	22000	BESS	-0.14-0.22	99	180-255, 220
[30]	IPOS	Step-Up/Down	FB	6480	BESS	-0.21-0.26	N/A	N/A
[31]	IPOS	Step-Up/Down	FB	330	PV	-0.17-0.32	N/A	25-40, 33
[32]	IPOS	Step-Up/Down	DAB + Unfolder	4500	DC Microgrid	-	N/A	350, 350

This prevalence is attributed to PPCs' advantages in these applications, particularly their ability to match the voltage regulation range with the variation range of battery energy storage and PV string voltages. Doing so minimizes the active power processed by the DC-DC stage, as the voltage variation range for battery cells (in their 20–80% of state of charge (SoC)) and PV modules at maximum power point is inherently limited.

An analysis of DC-DC stage topologies highlights that DAB, FB, Flyback, and Phase shifted full bridge (PSFB) topologies are the ones used in PPC systems the most widely. While relatively few step-up/down converters are discussed in the literature, the potential benefits of these designs, such as reducing active processed power and minimizing converter size, are not investigated thoroughly. Furthermore, practical considerations for PPC systems, including converter protection mechanisms, start-up procedures, and seamless transitions between step-up and step-down operating modes, are largely overlooked in the majority of studies.

To justify a PPC as a DC-DC converter operating with improved performance, it must be compared with the closest non-isolated FPC DC-DC converter regarding the factors that are elaborated on later in this chapter. In other words, establishing a series path between input and output does not guarantee the superior performance of a PPC compared to a non-isolated FPC. Moreover, the K_{pr} value is a critical performance metric for any PPC. However, additional requirements must also be met to justify a converter as a high-performance PPC. Many DC-DC topologies fail to meet these criteria, preventing them from being recognized as such.

2.3 Benchmarking Different PPCs and Against Full Power Converters (FPC)

In addition to the active processed power, which is directly controlled by the voltage regulation range between the input and the output side, other performance metrics must also be analyzed. This evaluation must be conducted among similar PPC solutions for the given application and with the closest non-isolated FPC alternative to reach the optimal candidate for a specific use case.

One of the key factors to consider is a parameter called non-active power, which represents the power oscillation within the passive components of the converter caused by the switching of the converter's active elements. Despite the volt-second balance in inductors and charge balance in capacitors being zero under steady-state conditions, these components temporarily absorb energy during one interval and return it to the converter during another. This behavior manifests as pulsatile power, resulting from a current ripple in the inductors and a voltage ripple across the capacitors. According to the IEEE 1459-2010 standard, this is termed non-active power (N), distinct from reactive power (Q) in AC systems.

$$\Delta E_C = \int_{t}^{t+DT_S} \left| v_C(t) i_C(t) dt \right| = \int_{t+DT_S}^{t+T_S} \left| v_C(t) i_C(t) dt \right| \tag{5}$$

$$\Delta E_L = \int_{t}^{t+DT_S} \left| v_L(t) i_L(t) dt \right| = \int_{t+DT_S}^{t+T_S} \left| v_L(t) i_L(t) dt \right| \tag{6}$$

Assessing the converter's performance in terms of non-active power is crucial due to its significant impact on converter losses and overall efficiency. A comparison between a 750 W FB-based step-up PPC and an FB-PP-based step-up/down PPC reveals that the

latter offers a 46.9% reduction in non-active power and a 23.4% decrease in volume. This disparity results in improved overall system efficiency and higher power density [10].

A similar evaluation was carried out for a 750 W non-isolated boost FPC, a flyback PPC, and a PSFB PPC, as reported in [8]. The flyback PPC exhibited nearly the same level of non-active power as the boost FPC. However, the PSFB PPC significantly reduced non-active power, by over 77%, even under the most critical operational conditions (maximum voltage regulation range). Additionally, the PSFB PPC maintained an almost flat efficiency curve despite incorporating a higher number of active components, yielding up to 99%, which is considerably higher than flyback PPC efficiency (95%–98.5%).

In [Paper II], a comparison between a PSFB-based PPC and a non-isolated buck-boost full power converter (BBFPC) illustrates that even with nearly identical inductor current ripple and capacitor voltage ripple (yielding equivalent non-active power, N), the BBFPC's inductor stores 48.02 mJ of energy compared to just 4.65 mJ for the PPC's inductor. This substantial difference results in a much larger inductor and capacitor size for the BBFPC (almost 10 times), as shown in Figure 2.3. Conversely, using components of similar size increases oscillatory power in the BBFPC, reducing its efficiency.

Another crucial factor when selecting the final topology for a DC-DC stage of a PPC or comparing a PPC with an FPC is the component stress factor (CSF). This parameter is derived from the component load factor (CLF) [27] and evaluates the stress experienced by the components in the converter, including capacitors, inductors, transformers (magnetic components), and switching devices, with a defined weight factor for each element. The CSF is calculated based on the maximum or average voltage values and the root mean square (RMS) current for these components. The overall stress factor is determined by summing the CSF values of all individual components [27].

An investigation is carried out in [27] to select the optimal structure for PPC among DAB and FB topologies. The results of the windings component stress factor (WCSF), capacitors component stress factor (CCSF), and switching devices component stress factor (SCSF) demonstrate that the stress values for FB are increasing almost linearly with increasing output power levels. On the other hand, the DAB topology has the worst performance in the light load operation range as the circulating current inside the transformer and the switching devices increase dramatically.

In [Paper II], a CSF analysis of the BBFPC and PSFB-based PPC was conducted to evaluate their total CSF for various power levels (1kW, 2kW, and 3kW). The current ripple of the inductors and the voltage ripple of the capacitors are kept at the same level to obtain a tangible result regarding the components' size and CSF. While both converters' capacitors and magnetic components exhibit relatively similar CSF values, these stresses are higher in the BBFPC's switching devices. Moreover, to reduce the current ripple in BBFPC and have a comparable non-active oscillating power, a bulky inductor is required. The total CSF for the BBFPC is also significantly higher, as depicted in Figure 2.4.

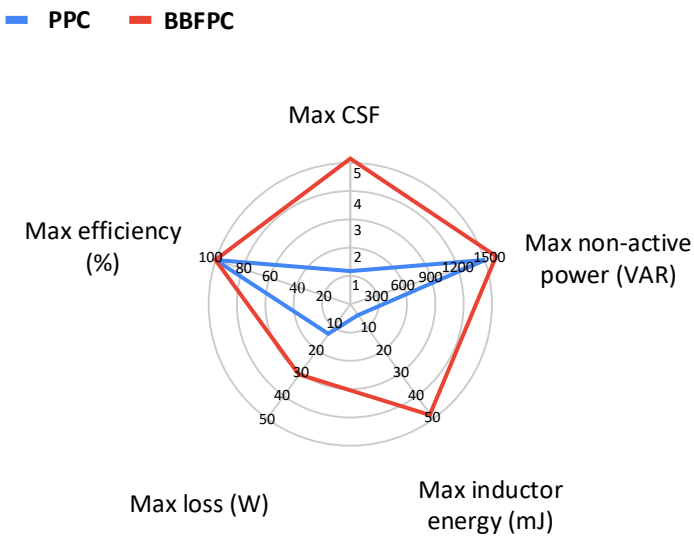

Figure 2.4. KPI comparison between BBFPC and CSFB-based PPC [Paper II].

2.4 Summary

In this chapter, the author has reviewed the PPC technology regarding the applicable configurations and the DC-DC stage topologies. The most common configurations are IPOS for step-up PPCs and ISOP for the step-down PPCs with the constant output voltage and positive DC-DC stage output voltage ($V_C \geq 0$). For the step-up/down PPC, the K_{pr} must be calculated for both IPOS and ISOP configurations to pick the optimal configuration for the active processed power level.

The three voltage conversion types (step-up, step-down, and step-up/down) of the PPCs are implemented in various applications like PV, BESS, EV chargers, DC microgrids, and others. However, the implementation of each type is limited in cases where a standard dictates the nominal voltage level and its variation range or the source/load type is somehow predefined, and thus, there is no freedom in terms of the PPC voltage conversion type.

Conversely, the flexibility of nominal voltage selection (either input or output ports or both) enables the designer to implement the optimal PPC among three voltage conversion types. Considering the same voltage regulation range for all types in a specific use case, it is demonstrated that the step-up/down PPC processes significantly lower active power, which is analytically proven in [Paper I]. Thus, the step-up/down solution is advantageous due to higher efficiency and power density. Despite this superiority, the implementation of step-up/down PPCs is less prevalent than the other two options, and there is a lack of investigations to elaborate further on the benefits of step-up/down PPCs.

Implementing step-up/down PPC requires careful consideration of various points when selecting the DC-DC stage topology. Based on the type of application (unidirectional or bidirectional), the two-quadrant (bipolar output voltage capability) or four-quadrant structure (bipolar voltage and bidirectional current) must be utilized at the LV side of the buck DC-DC converter. On the other hand, for the HV side, the structure needs to be

two-quadrant (bidirectional current). Moreover, the use of an inductive impedance at the LV side and zero inductive impedance at the HV side is essential. The last item is the connection of the isolation transformer between both ports to form an isolated DC-DC topology and avoid short circuits due to the series connection of PPC ports. The details for the design and selection of each item will be thoroughly explained in the following chapters.

A comparative evaluation must be conducted between PPC candidates and the closest non-isolated FPC to reach the optimal solution. Creating a series path between both ports of the PPC does not guarantee the efficient operation of the converter, and further key performance indicators need to be examined. The concepts of non-active power and CSF were defined, and some of the most important results in the literature are shown for different topologies. Moreover, the results in [Paper II] confirm the advantage of CSFB-based step-up/down PPC compared to BBFPC in terms of the total CSF and converter components' size when the non-active power amount is maintained equal. Therefore, the review and analysis in this chapter provide a comprehensive roadmap for the appropriate design procedure of an optimal step-up/down PPC, which will be detailed in the next chapters.

3 Novel Soft-Switching Current Source Bidirectional Step-Up/Down (BDSUD) PPC

The advantage of step-up/down PPC is elaborated in the previous chapter. The aim of this chapter is to present a step-up/down PPC for bidirectional applications. As discussed earlier, the requirements for the step-up/down bidirectional PPCs must be taken into account in the selection of the optimal DC-DC stage topology with the features explained earlier. The desired PPC needs to be able to control any voltage conversion type as well as the current direction. Hence, the more straightforward structures like PPCs based on flyback or two switch forward converter are incapable of fulfilling these criteria. The PPC based on DAB DC-DC topology with an unfolder circuit in its LV side is one of the few systems that can operate under the mentioned conditions. The DAB topology offers different advantages such as a simple control scheme, particularly with single phase shift modulation (SPSM), zero voltage switching (ZVS) operation, high efficiency, and high power density. However, the DAB structure inherently has some non-negligible drawbacks that limit its function in a practical PPC within the entire voltage regulation range and power level of the desired application. These issues include poor light load efficiency, excessive current stress around zero partiality where the voltages of both ports become close to each other ($V_{in} \approx V_O$), and limited soft-switching operation area. The current stress across the components stems from power circulation between the converter bridges, adversely affecting the converter performance, especially at higher frequency levels and low LV side voltage [33]. These limitations will be analyzed and quantified in detail in the following sections.

To overcome these concerns and propose an optimal PPC that can practically operate within the entire range of the desired application, an isolated current source full bridge (CSFB) advanced DC-DC topology is chosen to form the step-up/down bidirectional PPC system. The current source (CS) DC-DC converters offer some attractive features compared to the voltage source (VS) converters, particularly in applications, in which they are interfacing a very low voltage source with high voltage levels. The practical examples can be the connection of a BESS or fuel cell to a DC microgrid, when a CS DC-DC converter can manage a battery with deeply discharged cells or a fuel cell stack with a wide voltage range. Despite these benefits, the issue of handling and suppressing voltage spikes across the CS side switches of these converters is a challenging research topic in the literature. Generally, two methods are proposed to mitigate this obstacle, making them more reliable and efficient. The first one is the implementation of a capacitive snubber circuit as well as a passive/active switch to suppress the voltage overshoot caused by the leakage inductance and fulfill the soft witching condition for the CS side switches [35]. Although this strategy is straightforward and effective to some degree, it adds more active and passive components to the converter, leading to higher overall cost, complexity, and lower efficiency.

On the other hand, there are snubberless strategies where overshoot suppression is achieved without an auxiliary circuit. In these cases, the control scheme of the converter utilizes the converter parasitic inductor/capacitors and specific switching intervals within the operation period of the converter to guarantee the soft-switching condition as well as the voltage clamping [36]. Although the latter approach may require a more complicated control strategy, it is more favorable as there would be no additional components, increasing the converter's reliability, efficiency, and power density and decreasing the overall cost.

3.1 Proposed Topology Description

As described above, the chosen DC-DC topology is a CSFB-based structure with the desired characteristics required for the discussed applications. It is demonstrated in Figure 3.1 and thoroughly investigated in [Paper III]. The HV port is formed by a half-bridge voltage doubler (HB/VDR) structure, which is advantageous compared to the full bridge structure as it needs fewer active switching devices, and the voltage doubling feature decreases the turns ratio of the transformer by a factor of two, which is an additional merit of the HB/VDR. The LV side port comprises a matrix converter circuit that can alternate the voltage polarity and current direction simultaneously, as required by the operation point. The DC-DC topology is connected according to the IPOS configuration. Thus, the components in the parallel port are under-rated voltage and partial current stress. The limit of the partial current is determined by the values of K_{prmax}, which is calculated based on the maximum amount of active processed power. On the other hand, the series port elements will experience the rated current and partial voltage stress that ideally would be the maximum voltage difference between both ports. In practice, this voltage stress is higher as the current source structure tends to have voltage overshoot across the switches beyond the static blocking voltage of the devices. The clamping strategies will be discussed in detail in the next chapters.

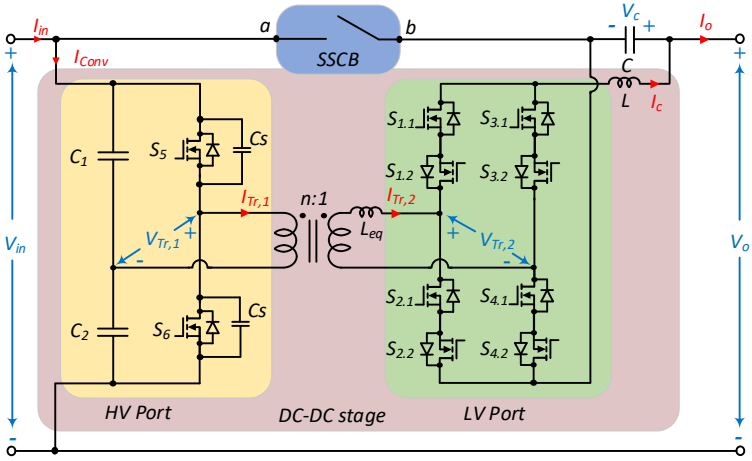

Figure 3.1. The structure of novel bidirectional step-up/down PPC [Paper III].

As the DC-DC stage transfers power in both directions between the HV and LV ports, it is considered as a buck converter concerning energy transfer from the HV to the LV port and as a boost converter in the opposite direction. The application of active switching devices is mandatory to ensure the bidirectional power flow within the DC-DC stage.

3.2 Operation Principle and Modulation Strategy

As discussed earlier, the desired modulation strategy in the CSFB DC-DC converter utilizes both the converter components and the control scheme to ensure voltage clamping of the converter for the current source (CS) side, which, in this case, is the LV port. This concept for the DC-DC stage of the proposed PPC is comprehensively elaborated in [34]. It utilizes the HV port switches to form an active rectifier, enabling current redistribution

for the CS side switches. This way, a secondary modulated converter (SMC) can be implemented. Phase shift modulation (PSM) and pulse width modulation (PWM) are the most common modulation strategies for CSFB converters. The PSM is advantageous due to its higher efficiency across the entire operation range of the converter; however, the use of reverse blocking switches in the LV port is obligatory. The PSM algorithm can be implemented for both buck and boost modes of the DC-DC stage. In both cases, the voltage gain between ports ($G_{buck} = V_C/V_{in}$ and $G_{boost} = V_{in}/V_C$) is controlled by a single phase shift (Ψ_{buck} and Ψ_{boost}) between the top and the bottom switches of the LV port, which simplifies the control strategy despite having different power flow modes. The transformer leakage inductance is inherently considered as a parameter that adversely impacts the converter performance. However, in the utilized CSFB, the energy stored in the leakage inductance facilitates the soft-switching condition at the HV port by transferring its energy to the snubber capacitors of the HV port switches and charging/discharging them. To successfully achieve this state, the energy stored in the leakage inductance must be greater than or equal to that stored in the snubber capacitors.

$$E_{L_{eq}} \geq E_{C_{eq}} \Rightarrow L_{eq} \cdot I_{Leq}^2 \geq C_S / 2 \cdot V_{in}^2 \quad (1)$$

In the conventional methods, soft-switching relies on the load current. Thus, in light load conditions where the I_{Leq} decreases, the converter loses the ZVS condition. To overcome this issue, a transformer with a higher magnetizing current level is typically implemented to increase the energy circulation within the DC-DC stage [37]. On the other hand, the solution proposed in [34] forms a resonant state between the snubber capacitors of the HV port and the leakage inductance of the transformer by short-circuiting the transformer LV side, which increases the resonant current amplitude beyond the load current level. Hence, the charge/discharge of the snubber capacitors can be accelerated without relying on the load current level. Besides minimizing energy circulation across the ports due to zero transformer voltage in this state, this method of soft-switching is load-independent, and the converter can achieve the ZVS condition across its entire power range by selecting appropriate parasitic element values and fine-tuning the time intervals.

Considering the polarity of the V_C and the direction of the I_C, four operation quadrants can be defined for the PPC based on the DC-DC stage operation modes, as showin in Figure 3.2. In the first quadrant (*Q-I*), the input voltage is lower than the output, and the power flow direction is from the input to the output side. Hence, the PPC is a step-up converter with $V_C > 0$. In this state, the DC-DC stage operates as a buck converter with positive output voltage and current. Thus, the power flow of the PPC and the DC-DC stage is in the same direction. Suppose the input voltage exceeds the output voltage ($V_C < 0$), maintaining the same IC direction. In that case, the converter operates in the second quadrant, where the power flow direction within the DC-DC stage is reversed. Therefore, the DC-DC stage starts operating as a boost converter with negative input voltage. The operating principles of the Q-III and Q-IV are analogous to those of the Q-I and Q-II, with the difference that the current direction and voltage polarity signs will be reversed. The modulation signals for both buck modes and boost modes are identical, with the difference that the top and bottom switch signals will be swapped when moving from *Q-I* to *Q-III* and from *Q-II* to *Q-IV* [Paper III].

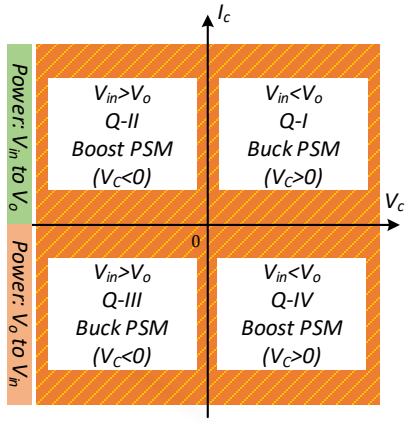

Figure 3.2. Operation quadrants and applied modulations for the BDSUD [Paper III].

The voltage gain of the CSFB in both buck and boost modes can be calculated as a function of the phase shifts (Ψ_{buck} and Ψ_{boost}) and the transformer turn ratio (n):

$$G_{buck} = \frac{V_C}{V_{in}} = \frac{\pi - (\varphi_{Buck} + \omega \cdot t_{red})}{2 \cdot \pi \cdot n} \tag{2}$$

$$G_{boost} = \frac{V_{in}}{V_C} = \frac{2\pi n}{1 - 2 f_{sw} \left(\frac{\varphi_{boost}}{\pi} + \frac{2 n L_{eq} (2 I_{C,max} - I_C)}{V_b} + t_{res} \right)} \tag{3}$$

In the boost mode, gain also depends on the load current and the converter parasitic elements. It is worth noting from (2) that the DC-DC stage gain in buck mode can be reduced to almost zero. This means that the converter can easily handle the zero series port voltage (when input and output voltages become equal) while operating in the buck mode of the DC-DC stage in Q-I and Q-III. On the other hand, observing (3), one can notice that the voltage gain of the DC-DC stage is limited in the boost mode, and it cannot convert very low voltage levels ($|V_C| < 10$ V) to the parallel port voltage, which in the case of a residential DC microgrid, can be 350 ±30 V.

The DC-DC stage in Q-I works as a buck converter, transferring power from the HV port to the LV port in the same direction as the power flow throughout the entire system. Figure 3.3(a) illustrates this operation. In this mode, switches $S_{1.2}$ and $S_{3.2}$ are activated, while $S_{2.1}$ and $S_{4.1}$ are either turned off or operate in synchronous rectification. A resonance period (t_{res} = t_1–t_2) that facilitates zero voltage switching (ZVS) for the HV port switches and permits current redistribution (t_{red} = t_2–t_3) for zero current switching (ZCS) in the top switches of the LV port is made possible by the switches $S_{1.1}$ and $S_{3.1}$ maintaining a fixed phase shift with respect to S_5 and S_6. Furthermore, Q-III mirrors the behavior of Q-I, provided the switching patterns for the top and bottom side switches in the LV port are appropriately swapped.

In Q-IV, the DC-DC stage operates as a boost converter, transferring power from the LV port to the HV port, aligning with the direction of the S-PPC power flow. This mode is depicted in Figure 3.3(b). In this setup, switches $S_{1.2}$ and $S_{3.2}$ are turned on, while $S_{2.2}$ and $S_{4.2}$ are either turned off or function in synchronous rectification mode. A fixed phase shift between the HV port switches and the top switches of the LV port enables the resonance period (t_{res} = t_4–t_5), which is essential for achieving zero voltage switching (ZVS)

of the HV port switches. Additionally, Q-II exhibits the same behavior as Q-IV, provided the switching patterns for the top and bottom side switches in the LV port are swapped to generate the negative voltage polarity.

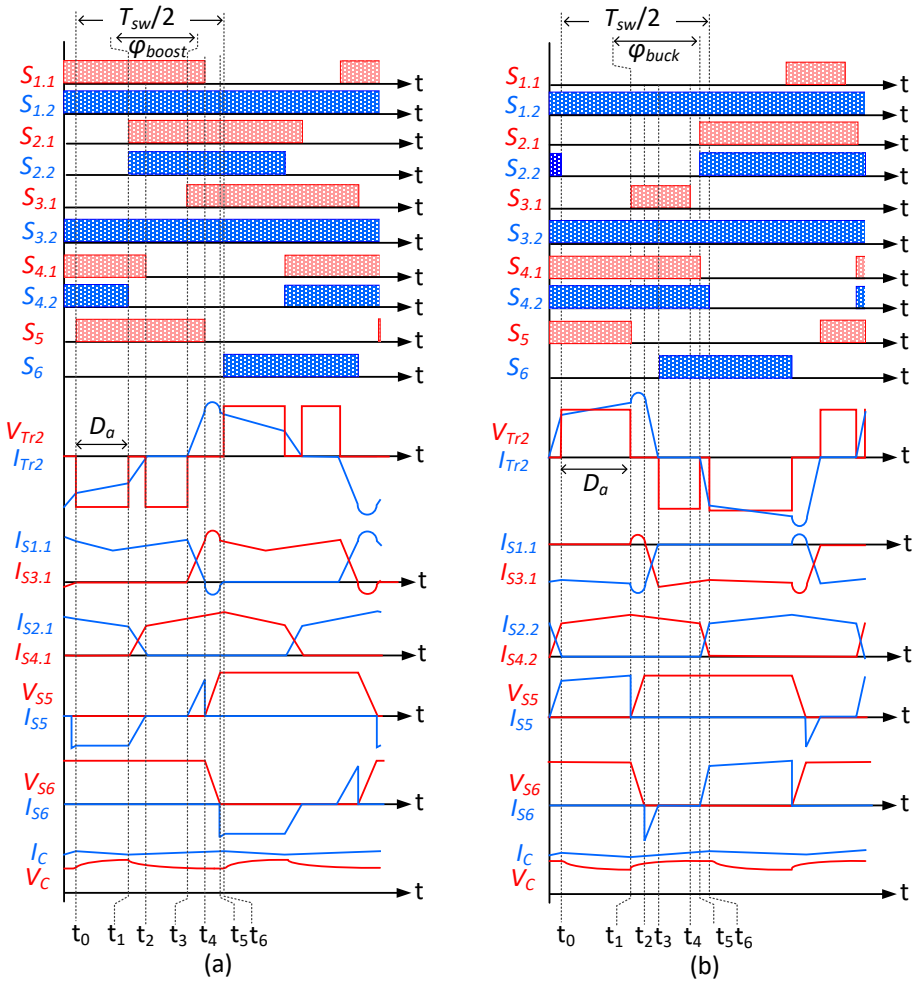

Figure 3.3. Phase shift modulation (PSM) modulations: (a) boost mode (power transfer from LV to HV port), (b) buck mode (power transfer from HV to LV port).

To overcome the limitations of the DC-DC in the boost mode, a third type of phase shift modulation is applied with the details discussed in [38] and [39] to extend the functionality of the converter in the critical operation zone near zero series capacitor voltage. The new modulation pushes the power from the HV port to the LV port (in the opposite direction of the boost mode active power flow) to charge the series port inductor and extend the boost factor of the converter. The proposed solution increases energy circulation within the DC-DC stage, which is undesirable. However, this energy circulation occurs within a very narrow voltage range compared to the entire voltage range of the converter. Therefore, the adverse impact of this energy circulation on the converter's weighted efficiency can be neglected. The advanced modulations used in this research are discussed in Chapter 4.

3.3 Comparison with Existing Solutions

The solution that most closely matches in terms of functional features (nominal voltages at both sides, power level, and four-quadrant operation) is the bidirectional step-up/down PPC described in [32], which serves as a power flow control converter (PFCC) in DC microgrids. This converter is formed by combining a DAB DC-DC converter with an unfolding circuit utilizing the IPOS configuration. The CSFB-based PPC can be examined against the DAB-based PPC in three key aspects: the component, the soft-switching operation range, and the component stress factor in each configuration. Regarding the number of devices, the CSFB design employs fewer active components on the HV port due to its HB/VDR-based architecture. With a voltage gain of 2, the voltage doubler structure reduces the required turns ratio of the isolation transformer, simplifying the transformer design and minimizing its parasitic parameters. A comparison table in [Paper III] highlights these factors, demonstrating the advantage of the CSFB-based converter over its DAB-based counterpart.

The soft-switching operation of the DC-DC stage plays a critical role in enhancing the converter's efficiency (η_C), thereby increasing the overall system efficiency (η_{sys}). For the DAB structure, the soft-switching operation is influenced by both the control strategy and the value of the transformer leakage inductance (L_{eq}). While SPSM modulation is the most straightforward control strategy for DAB converters, it is constrained by a limited ZVS range. To address this, more advanced techniques such as dual phase shift modulation (DPSM) and triple phase shift modulation (TPSM) have been proposed in the literature [40], [41], offering an extended soft-switching range and reducing power circulation between the primary and secondary bridges of the converter. However, none of these methods can ensure full ZVS on both the primary and secondary sides across the converter's entire power range. On the other hand, although increasing the leakage inductance extends the ZVS operation range, the maximum power transfer capacity of the converter can be decreased, limiting its applicability [42]. For the CSFB-based converter, the soft-switching region is guaranteed for the whole operation range by the appropriate selection of L_{eq}, C_S, and the resonance time interval between these two.

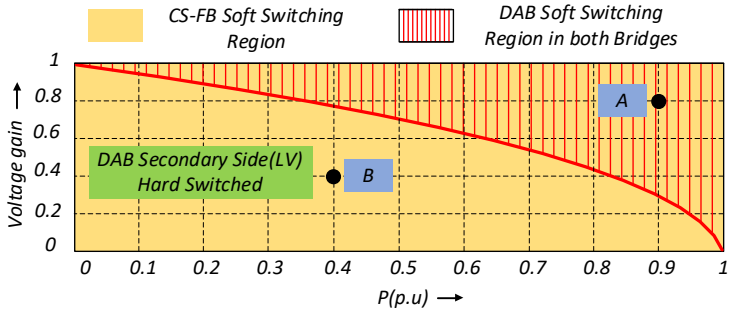

Figure 3.4. Soft-switching regions for DAB-based and CSFB-based PPCs [Paper III].

Finally, and most importantly, the CSF comparison for both converters is demonstrated in [Paper III]. The comparison evaluates the switching devices (SCSF), magnetic components, including inductors and transformers (WCSF), and capacitors (CCSF). For the CSFB-based PPC, the devices' stress calculation reveals an almost flat curve with a slight increase as the active power level, represented by the K_{pr} level, rises. In contrast,

the DAB structure has significantly higher stress levels, particularly at low K_{pr} values where the series port voltage approaches zero. This issue stems from excessive power circulation between the primary and secondary bridges of the DAB converter when $V_C \approx 0$. Consequently, to ensure reliable and smooth operation within the whole voltage range of the converter, implementing a bulky transformer and switches with extremely high current ratings is necessary. Such an overdesign approach adversely affects the converter power density and cost.

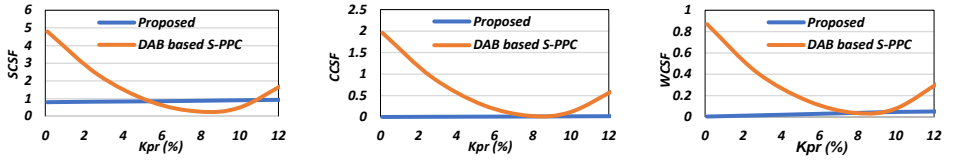

Figure 3.5. CSF values for the DAB-based and CSFB-based PPC regarding the K_{pr} levels (a) SCSF (b) CCSF (c) WCSF [Paper III].

3.4 Design Guidelines

The BDSUD's design guidelines must incorporate precise calculation, appropriate selection of the converter components, and optimization of control parameters. This ensures the converter's smooth and safe operation within its entire power and voltage regulation range. The BDSUD is designed to meet the application parameters, as illustrated in Table 3.1.

Table 3.1 System parameters for the designed PPC.

Parameter	Symbol	Value
Input voltage	V_{in}	350V
Output voltage	V_O	350V(±50V)
Rated Power	P_{rated}	3500W
DC-DC stage power	$P_{Conv\text{-}rated}$	600W

The DC-DC stage must be designed to regulate a voltage range of 100 V ($\Delta V_C = V_{Cmax} - V_{Cmin}$). However, since the input voltage equals the nominal output voltage, the regulation range can be symmetrically divided into two, with 50 V allocated for the step-up part and 50 V for the step-down part. As a result, the DC-DC stage must be capable of adjusting the series port voltage from –50V to 0V and from 0V to 50V. A safety margin is also considered to ensure stable system operation, typically around 10% of the maximum voltage regulation range (5 V). Hence, the amount of active processed power by the DC-DC stage can be calculated as a function of the voltage regulation range.

$$K_{Pr} = \frac{P_{Cout}}{P_{Out}} = \frac{V_C \cdot I_C}{V_O \cdot I_C} = 1 - \frac{V_{in}}{V_O} \tag{4}$$

When the input and output voltages are equal, the partiality coefficient becomes zero, and the DC-DC stage ideally does not process active power. However, in practice, a small but non-zero amount of power will still be consumed by the DC-DC stage due to inherent losses in the system. These losses stem from the equivalent series resistance (ESR) of passive components, conduction and switching loss of switching devices, transformer

core loss, and leakage current of protective components like metal oxide varistor (MOV) and transient voltage suppressor (TVS) diode, leading to a minimal but unavoidable power dissipation within the converter. Although the efficiency of the DC-DC stage drops significantly to very low numbers around this point, its impact on the overall system efficiency remains negligible as almost 100% of the system power is flowing through the series path between input and output. On the other hand, considering the maximum and minimum output voltage values, the maximum K_{pr} can be derived as 17%. Consequently, for a 3.5 kW system, the selection of a CSFB DC-DC topology with a rated power of around 600 W seems logical. This ensures the proper sizing of the DC-DC stage to handle the required amount of active power.

Another crucial step of the converter design procedure is the appropriate setting of modulation time intervals to achieve complete soft-switching within the entire power and voltage regulation range of the converter. The switches at the LV port will overlap to allow consistent inductor current flow without any interruption that may create voltage spikes. The overlap duration, which is required for the top LV port switches (S_1 and S_3) and bottom switches (S_2 and S_4), is determined based on the maximum converter current to ensure the ZCS for the LV port switches after current redistribution between them. It must be noted that the turn-off process of all switches at the LV port is designed to happen in full ZCS condition. In other words, after the current redistribution is completed for each switch pair (for example, $S_{2.2}$ and $S_{4.2}$), the gate signal turns off for the switch with zero current. On the other hand, the turn-on of all switches can be referred to as a soft turn-on assisted by the transformer's leakage inductance, as each switch is in series with the transformer's leakage inductance while turning on.

Another critical aspect of the converter design process is the accurate setting of modulation time intervals to ensure full soft-switching operation across the entire power and voltage regulation range. The LV port switches must have an overlap period to keep uninterrupted inductor current flow and prevent voltage spikes. The required overlap duration for the top LV port switches (S_1 and S_3) and the bottom switches (S_2 and S_4) is determined according to the maximum converter current ($I_{Cmax} = I_{Omax}$) to guarantee ZCS for the LV port switches after current redistribution between them.

It is essential to ensure that the turn-off process for all LV port switches occurs under full ZCS conditions. Specifically, after the current redistribution is completed for each switch pair (e.g., $S_{2.2}$ and $S_{4.2}$), the gate signal is turned off for the switch with zero current. On the other hand, the turn-on process for all switches of the LV port can be referred to as a soft turn-on condition, assisted by the transformer's leakage inductance, since each switch is in series with the leakage inductance during its turn-on transition. This means that upon applying the gate signal to any switch (S_1–S_4), the voltage across the switch starts to decrease and drops to zero. At the same time, the current gradually increases at a slope dictated by the transformer's leakage inductance. This controlled current rise reduces switching losses during the turn-on period but does not completely eliminate them. The duty cycle of the LV port switches can be written as

$$D_{lv} \geq 0.5 + \frac{2 \cdot n \cdot I_{C,max} \cdot L_{eq} \cdot f_{sw}}{V_{in}}, \tag{5}$$

which depends on the voltage across the leakage inductance during the current redistribution time ($V_{in}/2n$), the leakage inductance value of the transformer(L_{eq}), and the converter's switching frequency(f_{sw}).

On the other hand, the HV port switches (S_5 and S_6) require a dead time between their switching transitions, which is necessary for the VS structure. The duration of this dead time equals the constant phase shift between the HV port and LV port switches. Since ZVS occurs within this time interval, it has to be long enough to accommodate the current redistribution of the LV port switches and the resonance period between L_{eq} and C_{eq}. This guarantees the complete charging and discharging of the snubber capacitors and allows the body diode of S_5 or S_6 to turn on before applying the gate signal.

Unlike D_{lv}, the duty cycle of S_5 and S_6 must be determined based on their worst-case operating point, which is $I_C = 0$. This is because the converter current impacts the resonance period, which becomes longer at lower current levels and reaches its maximum duration when $I_C = 0$:

$$D_{hv} \leq 0.5 \cdot \left(1 - \frac{f_{sw}}{f_r}\right), \tag{6}$$

where the D_{hv} is the duty cycle of the HV port switches and the f_r is the resonance frequency between C_{eq} and L_{eq}.

The voltage regulation range of the PPC is defined by the capability of the DC-DC stage to control the series port voltage in either buck modes (Q-I and Q-III) or boost modes (Q-II and Q-IV). The key parameter that ensures the converter can achieve this regulation range is the transformer turns ratio (n), which determines the maximum voltage gain of the DC-DC stage in buck mode and the minimum voltage gain in boost mode. While calculating the transformer turns ratio, the converter's worst operation points must be considered. This means that the converter must create the maximum V_C plus the 10% safety margin to achieve stable operation within the entire operation range. It must be noted that a switching period of the converter includes inevitable duty cycle loss, which is the accumulation of the shoot-through state as well as the current redistribution time intervals, which happens every half cycle. Therefore, the active duty cycle, where the power transfer occurs from the HV to the LV port (in the buck modes) or in the opposite direction (in the boost modes), is less than one. Practically, considering the maximum duty cycle losses, the $D_{a,max}$ can be considered equal to 0.9 in the following equation:

$$n_{min} \geq \frac{V_{in,min}}{2 \cdot D_{a,max} \cdot V_{C,max}}. \tag{7}$$

3.5 Soft Start and Protection Issues

The significant advantage of PPC technology lies in limiting the active power processed by the converter to a fraction of the total active power of the system. This enables the use of low-voltage-rated devices at the series port (ideally around 20% of the nominal input or output voltages) and low-current-rated devices at the parallel port. However, this reduction in voltage and current is limited to the converter's steady-state operation. The voltage across the series port switches and the current through the parallel port switches can increase significantly during transient conditions. These abrupt variations can potentially damage the converter components, which are downsized and more vulnerable. The possible potential transient conditions that may arise during the converter operation are listed as follows:

I- ***Inrush current at the start-up time of the converter:*** Due to the voltage difference between the input and the output of the PPC, the series connection of these two sources with a capacitor in the connection path

can induce a high amplitude charge current because of high *dv/dt* on the series capacitor. Neglecting any preventive approach, the only limiting factor for this instantaneous surge current is the series resistance of the path, which includes the internal resistances of the sources and the ESR of the capacitor. Consequently, the current amplitude can exceed the rated current of the devices (which is considered 2–3 times higher than the nominal current of the converter), leading to converter damage.

II- ***Short Circuit (SC) at the Series or Parallel Port:*** In the event of an SC fault at either the input or output terminals, the series port of the PPC, which initially was operating under the voltage difference between the two sides($V_C = V_{in} - V_O$), will experience a considerably higher voltage level (equal to the input or output voltage itself). For DC-DC topologies employing a CS structure at the series port, the inductor current will swiftly rise within a microsecond timeframe. Conversely, the switching devices will be subjected to immediate and extreme voltage stress for topologies with a VS structure.

III- ***Open circuit (OC) fault or sudden disconnection at any side of the PPC:*** This fault is particularly critical for CS converters, as the sudden interruption of an inductive current can create substantial voltage spikes at the inductor terminals. If these spikes' amplitude exceeds the switching devices' breakdown voltage rating, they may be damaged. Additionally, if the converter current is interrupted while the modulation of the switches on the CS side continues, oscillations can occur between the series capacitor and inductor. As a result, a series RLC circuit is formed, oscillating from the initial inductor current value and damping ratio based on the ESR of the inductor and capacitor and on the resistance of the switches.

Assuming a positive or negative current (I_C), based on the converter's operation point, this phenomenon can alter the current flow direction within the LV port bridge. At the same time, the control scheme is designed to drive the switches based on either a positive or negative current direction, not both simultaneously. Consequently, the devices cannot accommodate these uncontrolled current swings, leading to an unintended interruption of the inductor current. This can lead to high-voltage spikes across the switches, ultimately causing their failure.

Upon reviewing the literature, it can be observed that only the benefits of PPCs are covered, and challenges arising from transient operating conditions are often overlooked. Table 3.2 collects examples of various PPC types, their power and voltage levels, and the switching devices utilized at the series and parallel ports. The data in the table highlight that, in the absence of protection measures, converters often employ devices with very high voltage and current ratings to guarantee the reliable operation of the PPC and safeguard the converter against different unwanted faulty or transient conditions. However, following this overdesign approach cancels one of the key advantages of the PPC concept – the downsizing of converter components compared to an FPC with equivalent input/output voltages and power levels. Therefore, the series connection of input-output using an isolated DC-DC converter is not enough to achieve a practical PPC, considering that it loses galvanic isolation despite using isolated topology.

The first and most crucial step in the protection strategy is the integration of a solid-state circuit breaker (SSCB) in the series path between the input and output.

Compared to mechanical circuit breakers (MCBs), SSCBs provide a significant advantage by responding to fault conditions in a microsecond timeframe, which is unattainable for MCBs. However, the primary drawback of using an SSCB is the introduction of static conduction losses caused by the on-resistance ($R_{ds\text{-}on}$) of the switches, which is inevitable. Therefore, selecting switches with the lowest possible on-resistance (considering the cost parameter) is essential to minimize power loss, increase the converter efficiency, and facilitate its thermal management. The structure of the implemented SSCB is elaborated in detail in [46], including two back-to-back MOSFETs, an RCD snubber circuit, and MOV to protect the switches from overvoltage conditions.

Table 3.2 PPC comparison regarding the switching devices [43].

Ref.	**PPC Config.**	**P (kW)**	**V_{in} (V)**	**V_O (V)**	**Series port devices**	**Parallel port devices**
[20] Full bridge with CS series port	IPOS	1.5	35-64	220	Cree C3D12065A (650 V)	Infineon IRF200P223 (200 V)
[44] Two-stage full bridge	IPOS and ISOP	7	450-700	600	SCT3030AR (650 V)	SCT3030AR (650 V)
[45] Full bridge	IPOS	24	180	408	C3M0015065 K (650 V)	C3M0015065K (650 V)
[*13*] Full bridge with CS port	ISOP	6.5	450	320-390	SEMIKRON SK25MH 120SCTp (1200 V)	STPSC20H065CW Y (650 V)
[10] Full bridge push-pull	IPOS	0.75	187-253	220	IPP220N25NF D (250 V)	IRFP360LC (400 V)
[29] Full bridge push-pull	IPOS	22	180-255	220	CM200DY-12NFigbt (600 V)	CM100DY-12NF (Mitsubishi) IGBT (1200 V)

The SSCB remains disconnected while initializing the PPC to prevent an inrush current during converter start-up. Depending on the values of V_{in} and V_O, the series capacitor must be precharged by the DC-DC stage to a positive or negative voltage by transferring energy from the parallel (HV) port to the series capacitor (LV port). This requires the DC-DC stage to be modulated using one of the buck modulation schemes (Q-I or Q-III) to establish either a positive V_C ($V_{in} < V_O$) or a negative V_C ($V_{in} > V_O$). Once the precharge process is finished, the SSCB can be connected safely, allowing the PPC to start its operation in the desired quadrant, considering both the polarity of V_C and the direction of I_{Cref}. This procedure avoids charing the series capacitor to eliminate the surge current.

3.6 Experimental verification

To validate the functionality of the designed PPC, a 3.5 kW prototype based on a 600 W CSFB topology was built. The experimental setup is depicted in Figure 3.6. Two iTECH IT6000C bidirectional DC power supplies were utilized for the input and output voltage source. Moreover, the Yokogawa WT1800 precision power analyzer was used to collect efficiency data at different operation points of the converter.

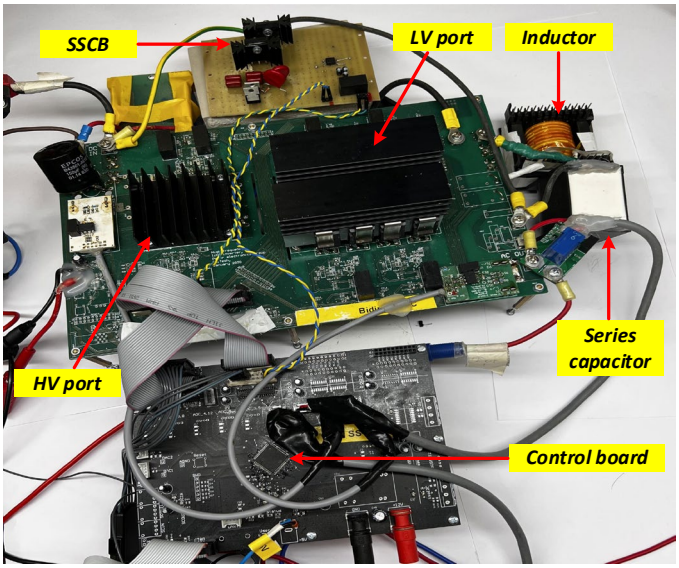

Figure 3.6. The assembled prototype of the proposed BDSUD [Paper III].

The switching waveforms are captured to confirm the soft-switching condition for the HV and LV port switches. Following this, the voltage-current waveforms of S_5, $S_{3.1}$, $S_{4.2}$, and the transformer LV side are recorded in the Q-I operation quadrant, where the buck PSM modulation is applied to the converter. It must be noted that the whole process is repeated for two distinct operation points represented by A and B in Figure 3.4. These points are selected to evaluate the converter performance in a power level close to the nominal power (0.9 p.u.) and in a light load condition (0.4 p.u.). The results for point A are illustrated in Figure 3.7. It can be seen from Figure 3.7(a) that the Switch S_5 turns on completely in ZVS condition after the resonance current, evident from the transformer current, discharges its snubber capacitor (C_{sn1}), and turns on its body diode. On the other hand, the turn-off process is a soft turn-off facilitated by the switch's snubber capacitor, constraining the dv/dt across the S_5.

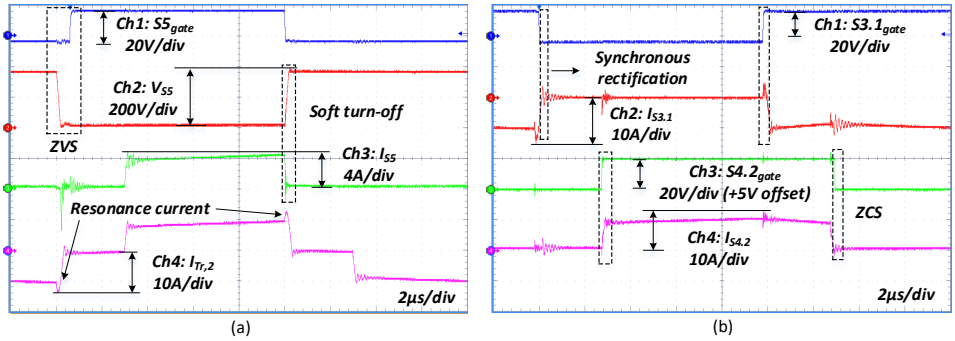

Figure 3.7. Experimental waveforms of the converter for (a) HV port switch (S_5) and transformer LV side (b) LV port switches [Paper III].

Considering the LV port switches, $S_{1.2}$ and $S_{3.2}$ are always turned on in Q-I. Moreover, the $S_{2.1}$ and $S_{4.1}$ work in synchronous rectification mode to eliminate body diode conduction loss. Therefore, due to the analogy of the behavior of both LV port legs, the waveforms of $S_{3.1}$ and $S_{4.2}$ are captured and exhibited in Figure 3.7(b). Regarding the $S_{3.1}$, its body diode naturally commutates and turns off during the synchronous rectification interval. The ZCS turn-off also occurs for $S_{4.2}$ after successful current redistribution between $S_{2.2}$ and $S_{4.2}$. Conversely, the turn-on process for both $S_{3.1}$ and $S_{4.2}$ is a soft turn-on with reduced *di/dt* assisted by the primary transformer leakage inductance.

Figure 3.8 shows the series capacitor voltage (V_C) and the output current to prove the soft start strategy's effectiveness. After the charging process initiation at t_1, the series capacitor voltage gradually increases to the voltage difference between the input and output. Once this criterion is met, permission is given to the SSCB to activate and allow the current flow from the input to output or vice versa. It is evident that the SSCB connects at t_3, and the output current rises from zero to the specified reference current (4A) without any current spike or inrush current. Additional dynamic test results are provided in [Paper III] to demonstrate the controller's capability to adjust the output current and maintain constant output current for variable output voltage levels.

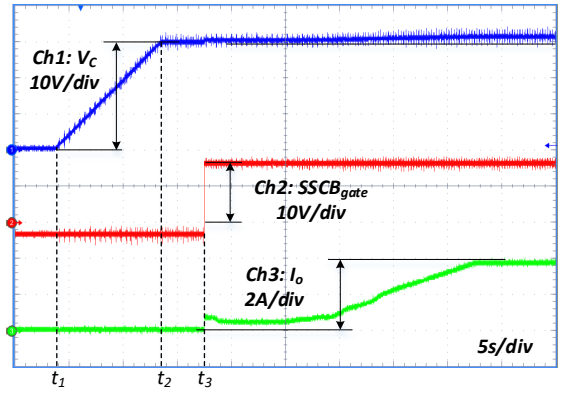

Figure 3.8. The soft start procedure for I_{dc_ref} = 4 A, V_{in} = 350 V, and V_O = 380 V [Paper III].

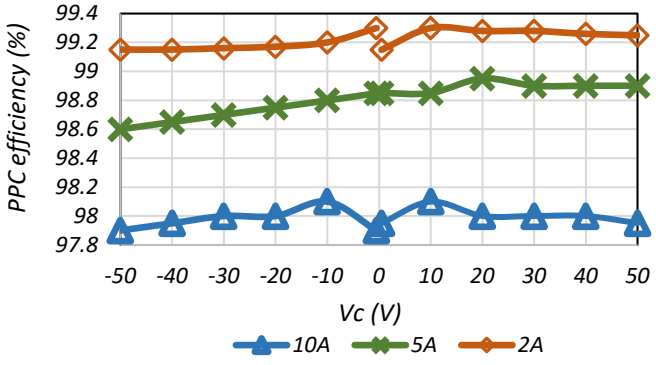

Figure 3.9. Efficiency curves of the proposed BDSUD for different current levels and voltage regulation range of 100 V [Paper III].

Eventually, the efficiency of the converter is measured for different current levels (2A, 5A, and 10A) with series capacitor voltage ranging from –50V to 50V. The results in Figure 3.9 reveal that the PPC can achieve a peak efficiency of 99.3%, dropping to the minimum efficiency of 97.8%. It must be stated that this initial prototype is implemented to prove the concepts claimed within this chapter. Therefore, hardware and control modifications can enhance its efficiency and power density.

3.7 Summary

In this chapter, the author proposed a BSUD based on a CSFB DC-DC topology and IPOS configuration. The DC-DC stage can change the voltage polarity and current direction at its LV port, enabling the implementation of a four-quadrant converter regarding voltage polarity and current direction. The power flow direction of the converter can be categorized as the system power flow (between input and output) and the DC-DC stage power flow (between DC-DC stage ports). They can be in the same or opposite direction according to the polarity of the LV (series) port voltage and its current direction. Therefore, the DC-DC stage performs a buck or boost converter dictated by the system operation point.

The converter's unique modulation strategy is based on PSM for both buck and boost modes of the DC-DC stage. It features full soft-switching operation within the entire power and voltage regulation range of the converter. The addition of the SSCB also enables the soft start feature for the converter, which is essential to prevent the start-up time inrush current.

A comparative study evaluates the characteristics of the CSFB-based PPC compared to its closest competitor, which is based on the DAB DC-DC converter. The results prove the superiority of the CSFB-based solution as it employs fewer hardware components, provides full soft-switching capability, and has lower CSF values due to negligible power circulation between the DC-DC stage ports.

Thorough design guidelines are provided to adjust the control variables optimally, overlap and dead time values, and the hardware components. When designing the hardware, the main transformer must be considered the most crucial component of the converter as it defines the voltage regulation range between the input and output.

The author has carried out different tests to verify the converter's operation according to the steps presented in this chapter. These tests encompass the switching behavior, dynamic behavior, and efficiency performance. All of the experimental results are in line with the claims provided within the chapter.

Nevertheless, this chapter demonstrates that VS topologies are not suitable for the given type of PPCs due to high circulating energy near zero partiality. Moreover, it proves that CS DC-DC stage topologies resolve this issue, even though still featuring limited voltage regulation capabilities in two operating quadrants. The obtained results confirm the first hypothesis. Moreover, the demonstration of a soft-start strategy employing SSCB proves the second hypothesis partially.

4 Performance Enhancement Techniques

To justify the proposed PPC as a practical non-isolated DC-DC converter across different operating modes, various critical operating points, potential issues arising from dynamic conditions or mode transitions, and possible fault scenarios must be considered. These challenges must be carefully addressed, and a possible solution for each issue must be provided.

4.1 Reverse Boosting and Flyback SMC Modulations alongside TMC

The advantage of the step-up/down PPC in decreasing the active processed power by the DC-DC stage compared to step-up and step-down converters is elaborated in the previous chapters. To successfully implement the step-up/down PPCs, the converter must operate smoothly around zero series port voltage and seamlessly transit between step-up and step-down modes dictated by voltage levels on both sides. The DC-DC stage must be able to control the nominal converter current while pushing the series port voltage to zero in the buck modes (Q-I and Q-III) and boost a very low voltage level to the parallel port voltage in the boost modes (Q-II and Q-IV). The four quadrant PPC proposed in [32] based on the DAB converter suffers from excessive power circulation when the series port voltage becomes almost zero. Therefore, the root mean square (RMS) value of the current flowing from the transformer and switches rises dramatically and impacts the functionality and reliability of the converter.

On the other hand, the BDSUD is inherently capable of decreasing the series port voltage to zero in buck mode while controlling the converter current from zero to the nominal level. The DC-DC stage in the buck mode is a voltage source converter with an inductive-capacitive filter at the output, and its voltage gain is controlled by the duration shoot-through state between the top and the bottom switches of the LV port (see Figure 4.1(a)). This phase shift can be changed from a minimum value, which depends on the redistribution and resonance time intervals, to its maximum value. Increasing the phase shift extends the shoot-through state period, leading to the active power transfer level drop. Consequently, at the maximum phase shift level, the voltage gain becomes zero, and ideally, the power transfer through the DC-DC stage stops.

In boost mode, the DC-DC stage functions as a current source converter with an HB/VDR rectifier at the output. The duration of the shoot-through state controls the voltage gain. During this time interval, active energy transfer from the LV port to the HV port is momentarily halted, allowing the inductor (L) to store energy and charge. However, unlike buck mode, the shoot-through control cannot accumulate enough energy in the inductor when the series port voltage V_C falls within a specific range ($-10V < V_C < 10V$). As a result, the DC-DC stage fails to boost these voltage levels to match the parallel port voltage, which is nominally 350 V, while maintaining the rated current flow.

Although reducing the converter current can slightly improve voltage gain and extend the operational range, as follows from (1), keeping the nominal current flow throughout the entire voltage regulation range is essential to ensure appropriate converter functionality. An alternative solution can be increasing the transformer turns ratio. However, it will decrease the BDSUD's voltage regulation range by constraining the maximum series port voltage (V_{Cmax}).

$$G_{boost} = \frac{2\pi n}{1 - 2f_{sw}\left(\frac{\varphi_{boost}}{\pi} + \frac{2nL_{eq}(2I_{C,max} - I_C)}{V_b} + t_{res}\right)} \quad (1)$$

To overcome this challenge and ensure stable converter operation within this critical voltage range, a new modulation strategy has been implemented and tested in [47]. This approach incorporates a specific time interval for reverse power flow from the HV port to the LV port in boost mode. This reverse power transfer allows the inductor to charge sufficiently, ensuring the minimum required energy storage to boost low voltage levels below 10 V while guaranteeing continuous conduction mode (CCM) operation.

As a result, both the shoot-through state duration and the reverse power flow interval are regulated to maintain precise voltage gain control within this zone (see Figure 4.1(b)). The voltage gain of the DC-DC stage can be written as

$$G_{boost} = \frac{2n}{1 - D_s - 2D_{rev}}, \quad (2)$$

in which the D_s is the duration of the shoot-through state, and the D_{rev} is the duration of the reverse power flow state. It is evident that the voltage gain is more sensitive to the D_{rev} value, and the control based on the D_{rev} provides a wider voltage regulation range. On the other hand, the converter's conduction loss increases in this state, resulting in an undesirable efficiency drop.

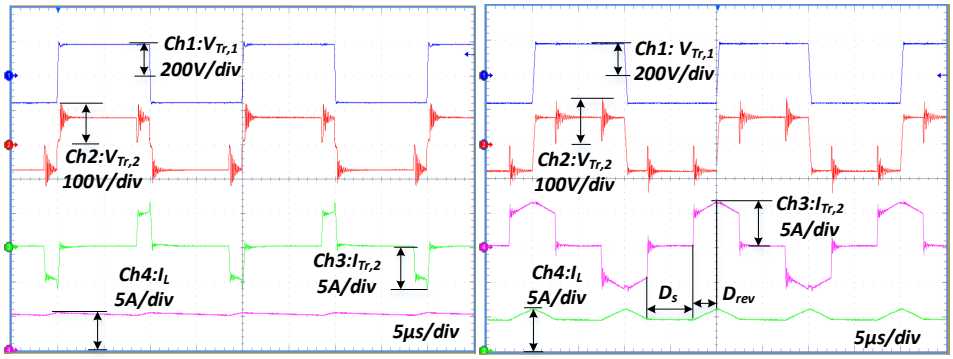

Figure 4.1. Current-voltage waveforms of the BDSUD while working with I_O = 5A in (a) buck mode of the DC-DC stage with V_{in} = 350 V and V_O = 350.5 V (Q-I) (b) boost mode of the DC-DC stage with V_{in} = 348 V and V_O = 350 V (Q-II) [47].

To further extend the boost factor of the DC-DC stage and guarantee stable operation across the entire voltage regulation range, an alternative strategy can be adopted by employing topology morphing control (TMC) combined with a new type of modulation technique known as flyback secondary modulated conversion (FBK-SMC).

The TMC technique is implemented through real-time reconfiguration of the converter structure using control signals. This dynamic adjustment enhances the converter's voltage gain or power handling capability without any need for hardware modifications. The control scheme reconfigures the LV port to operate as a current source flyback boost DC-DC converter in this approach. Positive V_C is achieved by permanently turning on one of the top switch pairs (S_1 or S_3) while turning off the other, with the remaining switches receiving modulation signals from the microcontroller.

This control method has been comprehensively analyzed in [48], and [49] for various reconfiguration types. In the BDSUD application, where an extended boost factor is necessary for the Q-II and Q-IV operation quadrants, the relevant reconfigurations are exhibited in Figure 4.2.

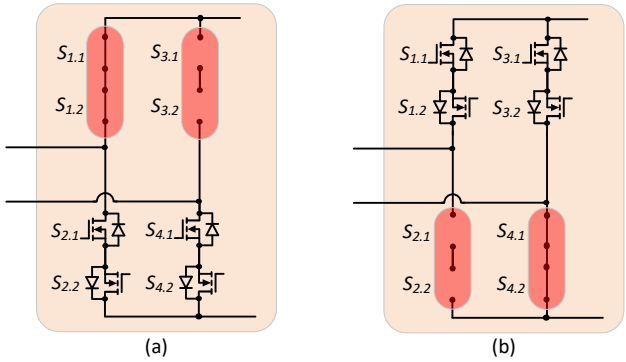

Figure 4.2. Proper reconfigurations to form the FBK-SMC DC-DC converter in (a) fourth quadrant (Q-IV) and (b) second quadrant (Q-II) [Paper IV].

The FBK-SMC modulation is illustrated in Figure 4.3. For Q-IV operation mode, which is illustrated in Figure 4.2(a), the modulation process unfolds across several distinct intervals. Initially, $S_{4.2}$ switches off, directing current to its body diode (BD), while S_2 activates under soft turn-on conditions aided by the transformer leakage inductance. The inductor (L) stores energy, and S_5 remains engaged to facilitate current transfer from S_4 to S_2. As the S_4 current drops to zero, the BD of $S_{4.2}$ commutates naturally, enabling L to continue energy storage while transformer magnetizing inductance absorbs energy from C_1 via S_5. To ensure proper switching transitions, $S_{4.1}$ turns off under ZCS, separating the LV and HV ports. The transformer output voltage reverses when S_5 turns off, assisted by the snubber capacitor C_s. The power is then delivered as transformer current flows through BD of S_6, transferring energy from magnetizing inductance to the output while maintaining soft-switching and reducing switching losses. The S_6 subsequently turns on under ZVS, allowing energy transfer to the HV terminal. As the cycle progresses, S_4 re-engages with a soft turn on, triggering reverse energy transfer from the HV to the LV port and storing it in the inductor. The energy accumulation in L influences the converter gain factor, with power transfer alternating between LV and HV transformer terminals to ensure efficient conversion.

The FBK-SMC modulation scheme employs only the reverse power flow control to adjust the voltage gain in the boost mode of the DC-DC stage. Hence, the voltage gain is modified to take the following form.

$$G_{boost} = \frac{4n}{1-4D_{rev}} \tag{3}$$

Comparing (2) and (3), one can observe that the voltage gain is increased by a factor of two, and it is two times more sensitive to the D_{rev} variations, which is the only control variable defining the voltage gain in this method. It must be noted that both reverse power flow modulation and FBK-SMC ensure the ZCS turn-off condition for the LV port switches and the ZVS turn-on condition for the HV port switches. The turn-off process of the HV port switches is a soft turn-off achieved by the snubber capacitors, which limits

the *dv/dt* across the switches. The LV switches all turn on in soft turn mode with reduced *di/dt* values, which is assisted by the transformer leakage inductance. Compared to the normal PSM modulation, the inductor accumulates energy during two separate time intervals by short-circuiting the LV port leg and the reverse power flow interval from the HV port. The impact of the D_{rev} state is dominant in the inductor charging process, as visible in Figure 4.4. Therefore, the current ripple in this operation mode is significantly higher, which leads to higher AC losses in the inductor *L* winding [Paper IV].

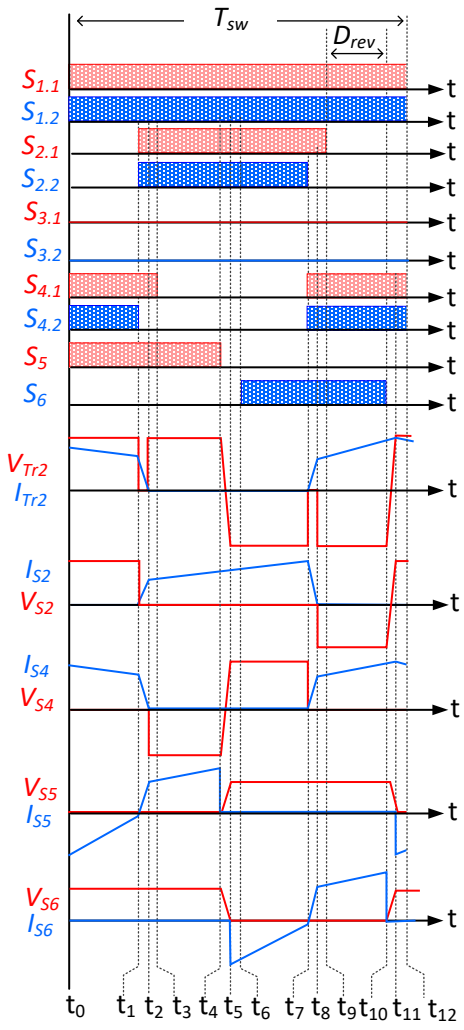

Figure 4.3. Flyback secondary modulated (FBK-SMC) modulation[Paper IV].

The major drawback of both approaches is the added conduction power losses caused by the power circulation in the converter components, particularly the isolation transformer. An extensive experimental analysis is carried out in [Paper IV] to investigate the impact of FBK-SMC alongside the LV port TMC on the overall converter performance in terms of the converter functionality and efficiency for different power levels for a predefined voltage regulation range($-60\ V < V_C < 60\ V$). The results indicate that the

FBK-SMC method leads to a maximum 1% efficiency drop in the worst-case scenario, which is an expected outcome. Although the PPC demonstrates poor efficiency performance when operating with FBK-SMC modulation, implementing this strategy is essential as it ensures smooth current controllability near zero partiality ($V_C \approx 0$).

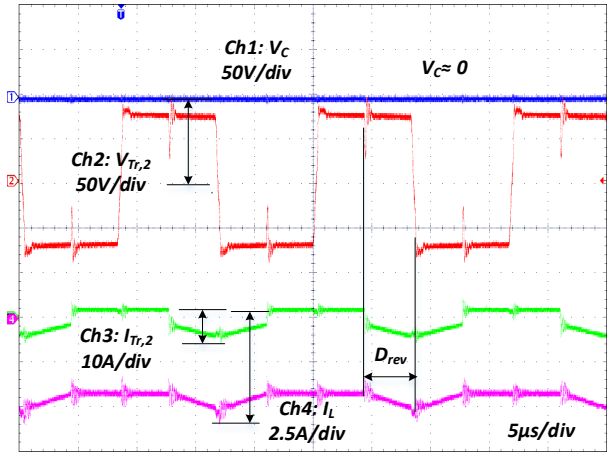

Figure 4.4. Current-voltage waveforms of the BDSUD with FBK-SMC modulation alongside the TMC while working with $I_O = 5$ A and $V_{in} = V_O = 350$ V in Q-IV.

It could be concluded that the application of FBK-SMC should be limited to a narrow voltage range ($-10V < V_C < 10V$), where boost PSM modulations in Q-II and Q-IV fail to regulate the converter current due to controller saturation. By adopting this approach, the overall effect of the efficiency drop within this voltage range on the weighted efficiency of the converter across the entire voltage regulation range ($-60V < V_C < 60V$) remains insignificant [Paper IV].

To investigate the impact of different TMC scenarios on the behaviour of the converter, the performance of the converter with a full bridge structure at the HV port was also assessed. It is also compared with the half bridge (voltage doubler) rectifier structure when the HV port is reconfigured from full bridge to half bridge. It must be noted that the DC-DC stage gain in the boost mode is reduced by a factor of two when working with a full bridge structure. In this condition, the transformer experiences double voltage stress, which increases the static loss of the converter due to higher transformer core loss. On the other hand, the RMS current of the transformer is reduced, which lowers the conduction loss in its windings. Moreover, the peak amplitude of the transformer current during the resonance period increases due to higher transformer voltage. These two factors adversely affect the converter efficiency, particularly in light load conditions, as reported in [Paper IV]. TMC at the HV port, i.e., reconfiguring into half bridge (voltage doubler) rectifier circuit, reduces the transformer static loss but elevates the conduction loss caused by higher RMS current. To better understand the performance of PPC with these two topology configurations, various tests were conducted with three different output currents (3 A, 7 A, and 10 A). From the analysis of the efficiency trends, it was found that the half bridge topology configuration always offers higher PPC efficiency, which is desirable. Regarding the operation near zero partiality, both structures have the same problem when the converter is operated with PSM without any TMC at the LV port

[Paper IV]. Therefore, it was concluded that the TMC at the LV port is the practical solution for the voltage/current regulation near zero partiality, while TMC in the HV port was found impractical. Therefore, in the proposed PPC, half bridge implementation of the HV port is preferable as it shows better efficiency performance.

4.2 Protection Against External Short Circuit and Open Circuit Faults

Considering the previous chapter's discussion of the necessity of a protection strategy to safeguard the converter against external short circuit and open circuit faults, the consequences of each fault must be analyzed, and the appropriate preventive approach must be applied. Short circuit faults (SC) and open circuit faults (OC) can happen at the input and output sides, as illustrated in Figure 4.5.

4.2.1 Short Circuit (SC) Fault Diagnosis and Management

Investigation of the short circuit faults on both sides reveals that the inductor current can rapidly increase to a value limited by the input/output voltage levels and ESR of the components. Since the ZCS condition is fulfilled for a certain maximum current at the series port of the converter, going beyond this maximum level (I_{Cmax}) will violate the ZCS limit. As a result, the predetermined redistribution time will not be enough to allow the LV port switch currents to reach the zero state before setting down the gate signal. Therefore, the switches will interrupt a significant inductive current, leading to a huge voltage spike across the devices. The consequence of such a scenario can be a failure of the converter, most likely due to the failure of the LV port MOSFETs. The simulation results in [Paper V] demonstrate that the peak voltage spike without any protection measure can reach up to 5 kV, considering a 0.5 Ω resistance in series with a 0.5 µH inductor as a short circuit impedance.

Besides facilitating a smooth start-up for the BDSUD, the incorporation of an SSCB is imperative as the core part of the protection routine. The BDSUD utilizes a current sensor at the series port to regulate the converter current required for each operation quadrant.

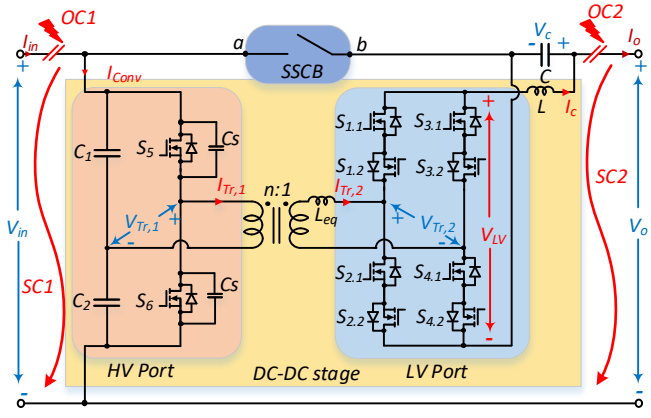

Figure 4.5. Possible short circuit and open circuit faults at the input and output side of the BDSUD [Paper V].

The selected current sensor can generate a very fast over-current detection (OCD) signal when the sensor current reaches the threshold level of (I_{th} = 0.82*25A = 20.5A) to trigger the protection routine using the microcontroller signals. After receiving the OCD signal, the microcontroller disconnects the SSCB after a certain delay time, which is the accumulation of the delays introduced by the current sensor, microcontroller, and switch drivers.

At the same time, the LV port switches need to be bypassed to create a freewheeling path for the fault current, allowing the inductor energy dissipation and fault current damping in an SSCB RCD circuit. The results in [Paper V] demonstrate that a successful fault clearance can be achieved following the procedure. The experimental result is illustrated in Figure 4.6 in the case of SC1 fault with V_{in} = 350 V, V_O = 320 V, and I_O = 5 A. The SSCB disconnection stops the increase in the inductor current, and the LV port bypass guarantees the voltage spike cancellation across the switches. This result confirms that this methodology effectively diagnoses and clears the SC fault and prevents any voltage spikes across the LV port switches whose voltage is represented by V_{LV}. Therefore, the safe operation of the converter can be ensured following SC fault at either side of the PPC.

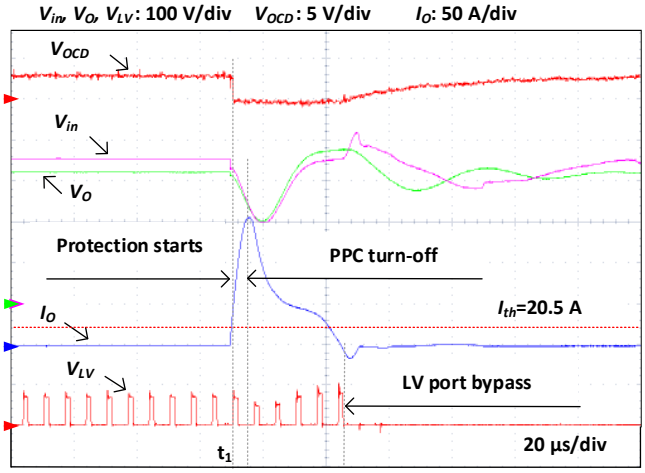

Figure 4.6. Short circuit protection for a fault occurring at the input side (SC1) [Paper V].

4.2.2 Open Circuit (OC) Fault Diagnosis and Management

The open circuit fault at either the input or output side of the PPC creates an RLC circuit at the LV port of the converter formed by the series capacitor, inductor, and the ESR of the components, as well as the on-resistance of switches. Following the fault event, an oscillation can initiate in this circuit with initial values of the inductor current and capacitor voltage, which can alternate the converter current with a frequency of $f = 1/2\pi\sqrt{LC}$. The current oscillation changes the inductor current from a positive value to a negative value or vice versa. Since the converter operates under certain modulation signals provided for each quadrant, the switches cannot properly switch currents of different polarities with ZCS, resulting in unwanted inductor current interruption. The consequence of such an event would be significant voltage spikes across the switches.

To diagnose the open circuit faults, the protection algorithm can utilize the actual current reading of the converter besides the reference current value and the control parameter variation. It must be noted that after the OC fault, the actual current measured by the current sensor will be zero. Still, the reference current maintains its original value, which is dictated by the operation point in each quadrant. Consequently, the value of the error signal, which is the input of the PI controller, will suddenly increase and saturate the controller. The fault identification signal signature could be the continuously high error of settling the inductor current.

Finally, the PWM switching must be stopped for the LV port switches, and a turn-on command must be sent to all of them to bypass the LV port for the oscillatory current damping. The time required for this command depends on the frequency of the oscillation, which is defined by the values of *L* and *C*. In the case of the BDSUD, this is more than several hundred microseconds (> 300 µsec). Therefore, the open circuit faults can be effectively cleared, ensuring the safe operation of the converter [Paper V]. The experimental result for the OC1 fault is provided in Figure 4.7, which are given for the same voltage levels as the SC1 fault and I_O = 2 A. It is observable that the LV port bypassing under the mentioned time (< 300µsec) removes the voltage spike across this port and secures the safe operation of the converter.

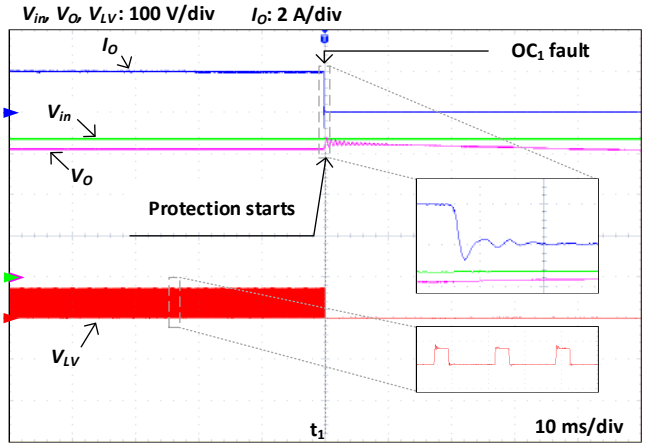

Figure 4.7. Open circuit protection for a fault occurring at the input side (OC1) [Paper V].

4.3 Use of LV Devices

Based on the discussions from the previous chapter about the voltage-current ratings of switching devices, it is evident that similar PPC solutions in existing literature utilize high-voltage devices to guarantee the reliable operation of the PPC throughout its entire operation range, taking into account possible unexpected dynamic behaviors and fault conditions. However, applying this overdesign approach to bidirectional step-up/down PPCs can adversely affect the system feasibility from different perspectives and lead to poor silicon utilization. Considering that the BDSUD and comparable converters employ a large number of active switching devices, several parameters must be considered to design the optimal converter and enhance its practical feasibility.

- ***Efficiency:*** Since the BDSUD's LV port operates in ZCS condition, conduction loss becomes predominant compared to the switching loss. Therefore, switches with low on-resistance are required to minimize the conduction loss, as the BDSUD utilizes 8 switches at the LV port, which is the high-current side of the converter.
- ***Cost:*** Low-cost devices are preferred to reduce the overall cost of the converter. However, high voltage (> 650 V breakdown voltage) silicon carbide (SiC) switches with very low resistance are considerably expensive (> 15 €), which negatively impacts the cost-effectiveness of the final system.
- ***Thermal management:*** Implementing switches with high conduction loss (high Rds-on > 20 mΩ) will necessitate bulky and expensive heat sinks to dissipate the power loss. Consequently, the power density of the PPC will reduce, which is undesirable.

Keeping in mind all the aforementioned factors, a low-voltage switch with low cost and low on-resistance is crucial to meet the system requirements. However, a very important challenge associated with current source converters must be addressed when reducing the breakdown voltage of the switches. Like all soft swithing current source converters, the LV port of the BDSUD experiences voltage overshoots across the switches due to resonant ringing between the transformer leakage inductance and the switch output capacitance (C_{oss}). Although SiC technology offers excellent dynamic and parasitic characteristics, such as lower C_{oss} compared to Si semiconductors, no SiC MOSFETs are available in the market with a breakdown voltage under 400 V. Therefore, identifying a switch with the lowest possible output capacitance remains a critical challenge in designing the BDSUD. Using GaN switches in these topologies is still challenging as these switches have no real repetitive avalanche rating.

Analyzing the resonance path and formulating the converter's behavior within this period disclose that the peak overshoot voltage can reach over twice the steady state blocking voltage of each switch ($V_{in}/2n$). This overshoot can be theoretically amplified to 2.5 times the steady-state blocking voltage when accounting for the body diode's reverse recovery charge (Q_{rr}) during synchronous rectification, which occurs through the body diodes of the switches at the LV port. Therefore, the reverse recovery charge of the switches' body diodes is another critical factor that must be considered carefully [50].

The converter's DC-DC stage is tested in open loop condition with Q-I modulation (buck PSM) to investigate the possible market options for LV port switches. Thus, three 120 V and three 150 V MOSFETs with the best possible C_{oss}-Q_{rr} combinations, as illustrated in Table 4.1, are selected and examined.

Table 4.1. Parameters of tested MOSFETs.

Part number	Breakdown voltage (V_{BR})	Rds-on (mΩ)	Coss (pF)	Qrr (nC)
GT100N12T		8-10	410	106
NTMFS008N12MC	120V	6.5-8	1150	165
TK32E12N1		11-13.8	330	160
BSC0403NS		9-11	520	50
IPI076N15N5	150V	5.9-7.6	900-120	96-192
NTP7D3N15MC		6.2-7.3	1250	720

It has been observed that the reverse recovery charge significantly affects the voltage overshoot, amplifying it up to levels higher than three times the steady-state voltage. The best result is obtained for the BSC0403NS from Infineon Technologies with an overshoot level of 2.65 times higher than the steady state voltage value, almost close to the theoretical value of 2.5 considering reverse recovery charge. However, the utilization of this switch remains impossible in the final PPC prototype since the voltage overshoot will definitely exceed the 150 V breakdown voltage of the switch regarding $V_{inmax} \approx 400$ V and $n \approx 2.2–2.4$ for the voltage regulation range of 50 V…60 V. Therefore, an effective strategy to limit the overshoot level below the breakdown voltage of the switch with a safety margin is essentially required. It has been shown in [50] that implementing an RC snubber across the LV side of the transformer or individual RC snubbers for each switch is practically ineffective since they dissipate a significant amount of energy, resulting in a noticeable reduction in the overshoot level, leading to a system efficiency drop.

Alternatively, a new solution called a regenerative snubber can be implemented. This solution includes an auxiliary transformer with a diode bridge to return the overshoot energy to the HV port voltage doubler capacitors during the overshoot time interval. The structure of the regenerative snubber circuit is illustrated in Figure 4.8.

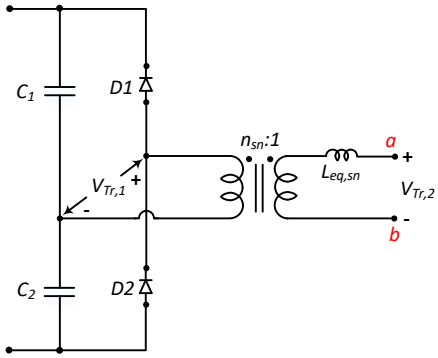

Figure 4.8. The structure of regenerative snubber for voltage overshoot suppression.

The C_1 and C_2 are the main capacitors for the voltage doubler circuit at the HV port. The turns ratio of the snubber transformer is less than the turn ratio of the main transformer. Therefore, in normal operating conditions, the diodes in this circuit remain reverse-biased. These diodes can be forward-biased whenever an overshoot happens and transfer energy to the HV port. Since this circuit is parallel to the main transformer, the ringing characteristic (frequency and time constant for damping) will change after connecting the diodes. While designing the snubber transformer, close attention must be paid to its turns ratio (n_{sn}), leakage inductance ($L_{eq,sn}$), and ac resistance. Selecting a turns ratio close to the main transformer's turns ratio will increase the RMS current in the snubber circuit and decrease the converter efficiency. In contrast, a very low turns ratio for the snubber transformer reduces the snubber effectiveness by preventing the forward bias of the diodes during the overshoot time. Generally, it is selected in a way that $n_{sn}/n_m = 0.85–0.95$. The snubber circuit's overall impedance ($R_{ac}+jX_{eq}$) must be lower than that of the main power circuit to allow the current flow and effectively suppress the overshoot. In practice, the leakage inductance of the snubber transformer must be a maximum of one-third of the main transformer leakage inductance, as recommended by [50]. To further reduce the voltage overshoot level, a passive RC snubber can be

implemented across the LV side of the main transformer and the snubber transformer between points a and b in Figure 4.8. Following this approach, the voltage overshoot can be suppressed from 2.65 times the steady-state voltage to 1.6 times, which enables us to utilize the chosen 150 V Si MOSFET.

4.4 Mode Change Strategy

The BDSUD operates under different modulations for all four quadrants. Considering the PSM modulations and FBK-SMC, a successful four-quadrant operation requires six different modulation schemes. To ensure the flawless function of the converter, it must seamlessly transit between different quadrants and modulations regarding the voltage levels at both sides and the output current level.

The seamless mode change ideally necessitates the simultaneous implementation of the correct modulation signals for all ten switches of the BDSUD when it enters from a certain mode to another one. Practically, such an ideal behavior does not occur, and the switches receive an arbitrary signal for 2–3 switching cycles due to how the microcontroller performs updates of the compare value registers. The unpredictable switching signals can be a source of various problems, including inductor current interruption and HV port capacitor short circuits. The experimental tests demonstrate that the latter case occurs, and the HV port capacitors become short-circuited by creating a very low resistance loop through the transformer and the LV port switches. Consequently, an inrush current flows from the HV port to the LV port and damages the LV port switches, as can be seen in Figure 4.9(a).

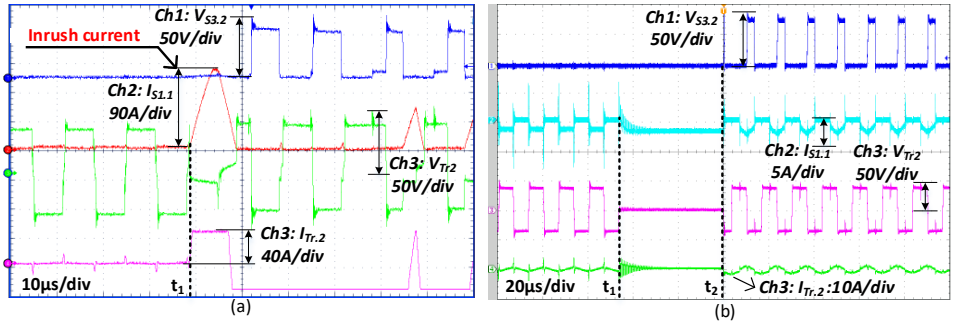

Figure 4.9. Experimental waveforms during mode change (a) without mode change strategy (b) with implemented mode change strategy.

The most applicable solution can be deactivating the PWM signals during the mode change and freely allowing the power flow between input and output. This can be achieved by turning off the HV port switches and turning on the LV port switches within the critical time interval, then delivering the modulation signals afterward. Such an approach can be implemented by combining a mode transition signal fed to a monostable multivibrator with “AND” and “OR” logic gates. This interval is illustrated in Figure 4.9(b) between t_1 and t_2. The length of the command signal can be adjusted using a variety of integrated circuits (IC) like monostable multivibrators [Paper V].

4.5 Summary

In this chapter, all possible improvements are discussed to enhance the performance of the proposed BDSUD, ensuring its practical viability for applications in energy storage, DC microgrids, and PV systems. As mentioned earlier, the PPCs in the literature mostly cover the converter's steady-state operation, focusing on major advantages like decreasing the active processed power. Considering the real application issues is essential to achieve the full benefits of PPCs.

To enable smooth operation near zero partiality in Q-II and Q-IV operation quadrants, where the PSM modulation struggles to control the converter below V_C = 10V, a new modulation strategy called FBK-SMC alongside TMC technique is applied. It can extend the boost factor of the DC-DC stage by adjusting the amount of reverse power flow from the HV port to the LV port.

Moreover, potential short circuit and open circuit fault scenarios at either the input or output side of the PPC are discussed to analyze the consequences of each fault. Then, the proper fault diagnosis and clearance methodology is developed for each of them. The SC faults need the SSCB and LV port bypass under a certain time to prevent voltage spikes across the LV port switches. Regarding the OC fault, bypassing the LV port is enough to allow the inductor energy dissipation by free oscillation within the LV port.

Finally, the constraints of utilizing low-voltage MOSFETs for the LV port are investigated. Although the problem of voltage spikes due to fault conditions is mitigated, switches can encounter avalanche conditions due to the voltage overshoots across the LV port switches. To address this issue, an auxiliary overshoot suppression circuit is implemented to reduce the peak overshoot level and enable the low-cost and low $R_{ds\text{-}on}$ 150 V Si switches to be used in the LV port. Therefore, the overall power loss of the converter can be considerably reduced, downsizing the heatsink size for its thermal management. As a result, the power density can be enhanced while decreasing the converter cost.

The findings of this chapter illustrate that the TMC technique effectively mitigates the regulation problem of the proposed PPC around and at zero partiality by software, reconfiguring the LV port and controlling the amount of circulating power from the HV port to the LV port. The results prove the third and fourth hypotheses. Furthermore, the developed protection methodology safeguards the converter against both SC and OC faults at either the input or output sides of the PPC. It confirms the remaining part of the second hypothesis regarding the protection features of the proposed converter.

5 Second Life Battery Energy Storage System Based On the Proposed PPC

The BESS can offer several benefits for residential applications of renewable energy systems as it can store energy during excessive energy generation times and deliver it to the consumer when there is a lack of energy production. One of the main obstacles to the widespread adoption of residential BESSs is the considerable capital cost of these systems, which currently varies between 250$ and 300$ per kWh. The second-life EV batteries with 70–80% residual capacity can reduce this capital cost by 15–25%, leading to their cost effectiveness and feasibility for residential applications.

Considering the battery cell technology, Lithium Iron Phosphate (LFP) is advantageous compared to its rivals since it provides a flat voltage curve even after degradation, less thermal runway risk, and a long lifetime, reaching up to 3000 charge-discharge cycles. The EV battery pack must be disassembled to examine the cell's state of health (SoH), internal impedance, residual capacity, and voltage profile. Then, they can be repacked and recertified for safety before being installed in a residential setting. Besides the battery performance, designing and implementing a high-efficiency DC-DC converter as an interface between the BESS and the residential DC microgrid (DCMG) is essential. As noted in earlier discussions of chapters two and three, the PPC technology demonstrates promising efficiency performance, particularly for the BESS and PV applications where the nominal battery stack or PV string voltage can be adjusted to be equal to the nominal DC bus voltage.

Previous chapters elaborated on the concept of step-up/down bidirectional PPC based on the CSFB DC-DC converter. Compared to similar structures in the literature, it offers unique features like full ZVS/ZCS operation and limited component stress within the entire power and voltage range. Moreover, the challenging issues arising from the dynamic behaviors, fault events, and critical operation points are addressed, and the applicable enhancement techniques are proposed. This chapter delves into a guideline for designing an application-oriented PPC from hardware and control points of view and verifying the final behavior of the converter when it manages the energy transfer between the BESS and a 350V residential DCMG. The details of the provided discussions in this chapter can be studied [Paper VI].

5.1 Design System and Converter Description

A detailed analysis using methods, like electrochemical impedance spectroscopy (EIS), is a prerequisite for second-life batteries to estimate their degradation level and residual capacity. For instance, the results of an LFP battery analysis subjected to 1000 charge-discharge cycles indicate that the residual capacity, the internal impedance, and the voltage profile will vary considering the C-rate [53]. The best consequences were observed for the 1C rate. In contrast, with higher C rates (2C and 5C), the residual capacity tends to decline more, raising doubts about the cost-effectiveness of implementing a second-life BESS-based on such batteries. Regarding the nominal voltage level of the DCMG, the Dutch national practical guideline NPR 9090 [54] is the only available standard for DC buildings, advocating 350 V (±30 V) for residential use. Since removing the AC/DC conversion stage allows many appliances to work at a 350 V DC level, the applicability of this voltage level for buildings is well justified. Therefore, the required number for a series connection of battery cells can be computed by taking into account the LFP nominal cell voltage (3.2V). The number of parallel connections depends

upon the needed energy storage capacity for each building and the amount of residual capacity of the batteries. With all of these points in mind, the 109s1p connection is selected as the final battery arrangement. It leads to the battery voltage range of 316 V–381 V for 10–90% of the battery SoC. Consequently, a step-up/down PPC can be designed according to the parameters depicted in Table 5.1.

Observing the numbers outlined in this table, the maximum voltage difference between the BESS and the DCMG becomes 60 V, which the converter must regulate. When choosing the converter components (particularly the main transformer turns ratio (n_m)) and adjusting the control variables, a safety margin of 10 V will be added. Therefore, the series port of the DC-DC stage must operate within a ±70 V bipolar voltage range, regulating the current injected into or absorbed from the DCMG to stabilize its voltage level within the specified boundaries.

Table 5.1. Parameters of the designed system [Paper VI].

Parameter	Symbol	Value
Battery voltage (10%-90% of SoC)	V_b	350V(±30V)
DC microgrid voltage	V_{dc}	350V(±30V)
Rated Power	P_{rated}	4kW
DC-DC stage power	$P_{Conv\text{-}rated}$	750W

Since the control objective is to regulate the DCMG current (I_{dc}), the series port of the PPC, which was initially the output side, is linked to the DCMG, while the parallel port is connected to the BESS (input side). Therefore, the positive I_{dc} values can be interpreted as energy transfer from the BESS to the DCMG, which will discharge the battery. The negative I_{dc}, on the other hand, will charge the battery. The K_{pr} calculation indicates that, given the voltage ranges on both the battery and DC bus sides, its maximum value reaches 0.19. Thus, for a PPC with a rated power of 4 kW, a DC-DC stage with a rated power of 750 W is sufficient to handle the required active power.

The final PPC designed in this chapter resembles the BDSUD proposed in the third chapter, with the hardware and software enhancements discussed in the fourth chapter. It means that the PPC is based on the same CSFB structure controlled by the PSM modulation strategy for both the buck and boost modes of the DC-DC stage by adjusting the phase shift between the top and bottom switches of the LV port (Ψ_{buck} and Ψ_{boost}). It also benefits from the soft start method enabled by the SSCB, which is needed to prevent start-up inrush current and ensure the safe operation of the converter. As discussed earlier, the applied buck PSM modulation strategies in Q-I and Q-III operation quadrants are capable of adjusting the maximum converter current (4000 W/320 V = 12.5 A), while pushing the series port voltage to zero when the battery and the DCMG voltages become equal. On the other hand, the boost PSM modulations in Q-II and Q-IV operation quadrants are incapable of stable converter control in the range of $|V_C| < 10$ V, where the series capacitor with virtually zero energy cannot accumulate enough energy in the inductor and boost a very low voltage to the battery voltage level at the parallel port. Consequently, implementing the FBK-SMC modulation scheme alongside the LV port TMC approach, which is verified in the fourth chapter, addresses this issue. It ensures the smooth functionality of the converter throughout the entire voltage regulation range($|V_C| < 60$V). Figure 5.1 represents this modulation strategy in relation to the series port voltage and current, whose average corresponds to the DCMG current ($I_C = I_{dc}$).

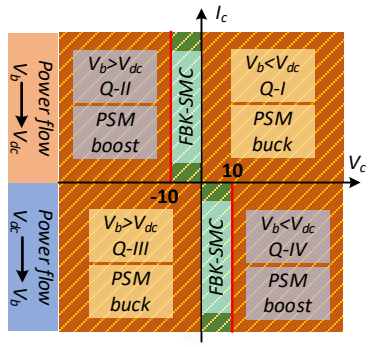

Figure 5.1. Operation quadrants and applied modulation schemes [Paper VI].

5.2 Control System Design for DC Microgrid and Converter

In every DCMG, the primary control objective is to regulate the DC bus voltage. Conventionally, the DCMG voltage value was defined as a nominal value with an allowable tolerance range. However, the NPR90 and Current OS [55] Regulations consider the nominal value as a label rather than a fixed set point. Instead, the voltage serves as an informative signal within upper and lower limits, allowing all DCMG elements (sources, loads, and storage devices) to interpret power availability or deficiency and react accordingly.

5.2.1 System Level Control

In this context, the BESS plays a vital role in stabilizing the DCMG voltage within the predefined band. It absorbs excess power generated by renewable energy resources (RERs) and discharges when consumption increases. Therefore, cooperating with an active front-end AC-DC converter (in grid-connected mode) will compensate for any imbalance between generation and consumption to ensure stable DCMG operation while preventing overvoltage conditions and critically low voltage emergencies. Consequently, the battery SoC must be monitored and carefully controlled within the range of (10–90%) to avoid any overvoltage or deep discharge, which can degrade the battery and shorten its lifetime.

The coordination of DCMG elements is achieved using either centralized or decentralized methods. The centralized approach relies on a core unit that collects data from and sends commands to the individual control units of each element. Effective communication links between these units are crucial and can be established through various protocols such as CAN bus, Ethernet, WiFi, or other communication protocols. However, this strategy has certain drawbacks, including susceptibility to cyberattacks and a lack of modularity in the overall control system, making scalability and adaptability more challenging.

Unlike the centralized method, the decentralized control strategy allows each control unit to independently measure data and make decisions regarding a predefined action profile for each unit. The most straightforward approach for decentralized control is droop control [56]. The droop curve describes how every element responds to variations in DCMG voltage. For the BESS, surplus power in the DCMG, indicated by voltage levels exceeding the nominal value, must be stored in the battery. Conversely, when a power deficit occurs, the BESS compensates by discharging power into the system. The droop

curve for the BESS can be represented as a linear equation with a specific dead band around the nominal voltage, avoiding unnecessary charge/discharge cycles within this region to enhance battery lifespan.

The droop curve in Figure 5.2 serves as the outer control loop for the PPC, dictating the required current to stabilize the DCMG voltage. The rate of current variation (also called the droop coefficient (R_{dr})) and the cut-off points (325 V, 345 V, 355 V, and 375 V) can be reconfigured based on the systems' requirements. Precise voltage sensing is essential, and proper filtering is necessary to have a disturbance-free reference current for the inner control loop of the converter.

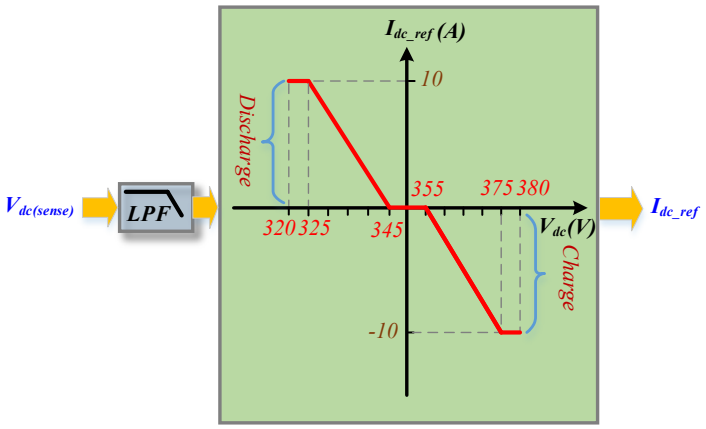

Figure 5.2. The droop curve for power management of BESS connected to DCMG [Paper VI].

In addition to utilizing a hardware low-pass filter (LPF) with a cut-off frequency of 1 kHz, other techniques, such as software-based averaging within the microcontroller, can help eliminate arbitrary voltage fluctuations caused by electromagnetic interference (EMI). Hence, minimizing EMI is critically important, especially in the design of analog circuits printed circuit board (PCB) layout, to guarantee noise-free input data for the correct decision-making process. Notably, the final prototype benefits from the CAN bus and ESP32 WiFi communication modules alongside the droop control to enhance the flexibility and functionality of the system. Therefore, features like real-time configuration of the parameters, system performance, condition monitoring, and data acquisition can be added to the system.

5.2.2 Closed-Loop Control Architecture for the PPC

The STM32G474 is the central digital control unit of the converter, possessing six dual-channel high-resolution timers (HRTIM). Therefore, it can effectively modulate up to 12 switches. Moreover, the SSCB switches are handled by general-purpose input-output (GPIO) pins. The microcontroller employs a 12-bit analog-to-digital (ADC) peripheral to convert the V_b, V_{dc}, V_C, and I_{dc} readings to digital values. Additionally, a software-based LPF with the same cut-off frequency as the hardware filter is implemented to suppress noise further and improve signal precision. The inner control structure is based on a state machine incorporating various functions for safety check, soft start, soft stop, series capacitor charging for positive and negative voltages, and six dedicated functions corresponding to the six possible modulations in all operation quadrants.

The capacitor precharge algorithm employs one of the buck PSM modulations in Q-I or Q-III to gradually charge the series capacitor by linearly incrementing the phase shift from the minimum value to the point where $V_C \approx V_b - V_{dc}$. Once this condition is met, the converter can leave the capacitor charge mode and enter one of the normal operation modes depending on the voltage levels and current direction defined by the droop curve, simultaneously activating the SSCB. The control strategy relies on a proportional-integral (PI) controller, which receives specific parameters (K_p and K_i) and limits for each quadrant and modulation scheme. The PI block output is the phase shift, which is directed to the microcontroller timers' compare value registers to generate PWM signals for each switch.

The battery charge/discharge process or DCMG voltage fluctuations necessitate the PPC to execute smooth mode transitions. To ensure seamless transitions and prevent any instability, failure, or power flow interruption, a feedforward block precomputes the initial phase shift for the subsequent mode according to the voltage gain equation for each mode, which is augmented by the PI controller output. This approach secures controller stability while minimizing the risk of unexpected dynamic oscillations, which could potentially damage the converter, especially under high current operating conditions. As previously noted, a mode transition signal is also generated to temporarily deactivate PWM signals for approximately three switching cycles, mitigating the inherent microcontroller-related issues.

5.3 Hardware Design

The components must be carefully designed to fulfill the criteria of the designed converter under the given voltage and power levels in Table 5.1. It involves the magnetic devices, including the main and snubber transformers and the series port inductor, the switching devices, the capacitors, and the SSCB elements.

Based on the discussions of Chapter 3, the isolation transformer is the main element of the converter since it creates galvanic isolation between the HV and the LV ports to prevent a short circuit by the series connection of both ports. Moreover, it defines the voltage regulation range between the DCMG and the BESS by determining the maximum voltage gain in the buck mode of the DC-DC stage and the minimum voltage gain in the boost mode of the DC-DC stage. Therefore, the calculation of the turns ratio must be performed in the worst operation point, which is the 320 V parallel port voltage and 70 V series port voltage in the buck mode of the DC-DC stage, indicating the maximum voltage gain of the buck mode ($G_{buck,max}$ = 70 V/320 V = 0.22). Following this approach, the stable converter operation can be guaranteed for higher voltage levels across the parallel port ($V_b > 320\ V$). Similar to the BDSUD in Chapter 3, the following equation can be utilized to obtain the exact turns ratio with the difference that $D_{a,max}$ is increased from 0.9 to 0.95 after the converter redesign and modifications.

$$n_{m,min} \geq \frac{V_{b,min}}{2 \cdot D_{a,max} \cdot V_{C,max}} \tag{1}$$

It leads to a turns ratio of 2.38 for given system parameters. Regarding the core selection, two parallel ferrite cores (material: Ferroxcube 3C95) with a maximum flux density of 100 mT are selected to avoid saturation, considering the maximum recommended flux density of 200 mT. Moreover, the converter's operation frequency is increased from 50 kHz for the BDSUD in chapter three to 75 kHz, downsizing the magnetic components by 50% for a similar system.

The leakage inductance of the main transformer is another crucial parameter that needs to be taken care of. The investigation of the impact of the leakage inductance value discloses that high leakage inductance increases the redistribution and resonance time intervals and leads to active power transfer duty cycle loss, which is undesirable. Moreover, a high leakage inductance level amplifies the voltage overshoot across the LV port switches. This is the consequence of resonance between the switches' output capacitance and the transformer leakage inductance.

After obtaining the turns ratio of the main transformer and its core selection, the snubber transformer design procedure must be initiated. As previously stated in Chapter Four, the snubber circuit efficacy depends on the ratio of n_{sn}/n_m, which must be in the range of 0.85–0.95. With this in mind, a snubber transformer with a turns ratio of 2.22 is built, resulting in the n_{sn}/n_m = 0.935. It can effectively suppress the voltage overshoot across the LV port switches based on the requirements of [*50*]. In terms of the leakage inductance of the snubber transformer, the minimum value that can be achieved in the selected low-profile core is 350 nH. Hence, the main transformer leakage inductance must be approximately three times higher than this number to allow the current to flow through the snubber transformer during the overshoot time interval. Concerning this requirement, the 1.2µH seems an appropriate value for the leakage inductance of the main transformer. Therefore, the transformer design procedure starts with selecting the main transformer turns ratio and core. Then, the snubber transformer turns ratio can be chosen. Finally, the minimum achievable value for the snubber transformer leakage inductance will determine the target leakage inductance for the main transformer. The entire design process must be executed simultaneously for both transformers to obtain optimal functionality.

The selection of the series port inductor (L) and the battery side voltage doubler capacitors ($C_1 = C_2$) must be in accordance with the allowable DCMG current ripple and the voltage ripple at the battery side. An off-the-shelf flat-wound wire inductor is chosen to downsize the converter volume and increase the power density. To address the issue of higher AC resistance of flat wound wires compared to litz wires, the inductor current ripple is reduced significantly by elevating the frequency level from 50 kHz to 75 kHz and increasing its value from 100 µH to 164 µH (Compared to [Paper III]), which is the series connection of two CPER3231-820MC inductors. Following this approach, the inductor current ripple can be pushed below 5% of the nominal DCMG current, making the inductor AC loss negligible.

Regarding the HV port capacitors, the allowable voltage ripple alongside the calculated ripple for the converter in [Paper VI] determines the minimum value of the capacitors. A parallel connection of an aluminum electrolytic capacitor and a film capacitor is implemented for both C_1 and C_2 to suppress high-frequency and low-frequency voltage ripples effectively.

The switching devices must be selected based on the voltage and current stress. For the HV port, the most critical factor is the voltage stress across the MOSFETs, defined by the maximum battery voltage of 380V. Therefore, a SiC MOSFET with 650V breakdown voltage can reliably operate at the HV port. On the other hand, the procedure for selecting the LV port switches is not as straightforward as the HV port switches since these switches' characteristics impact the converter performance from different points of view. Following the discussion of Chapter 4 for the use of low-voltage devices at the LV port, the implementation of a snubber circuit, including the regenerative snubber and an RC snubber reduces the voltage overshoot across the LV port switches from 2.65 times

the steady-state voltage to 1.6 times. Regarding the maximum battery voltage of 380 V and the main transformer turns ratio of 2.375, the steady-state voltage across switches becomes 380 V/2*2.375 = 80 V. Thus, the maximum overshoot level across switches reaches 128 V, enabling low-cost BSC0403NS Si MOSFETs from Infineon Technologies with a breakdown voltage of 150 V to be used.

Finally, the guidelines provided in [46] are followed to implement the SSCB components. To choose an appropriate MOSFET, current and voltage stresses in steady state and faulty conditions must be considered. It means that the SSCB switches must be capable of withstanding the pulse current flowing through switches during the SC fault, considering the fault clearance. Regarding the voltage stress, the maximum battery and DCMG voltages (380 V) define the steady-state voltage across the SSCB switches. The RCD snubber and the MOV suppress the dynamic voltage overshoots. Since the voltage and current levels of both [46] and the designed PPC closely match, the RCD snubber and the MOV type are taken from [46]. In addition to soft start and SC protection features, the SSCB enables the current controllability of the PPC near zero current. Below a certain current threshold ($|I_{dc}| < 1$ A), one of the SSCB switches turns off, allowing its body diode to conduct. This enhances the current controllability and stops the current oscillation near zero current region since the source with higher voltage tends to deliver power to the low voltage side irrespective of the droop control characteristics.

5.4 Experimental Study in DC Microgrid with Droop Control

The final experimental prototype is assembled according to the components and parameters outlined in [Paper VI], operating at a nominal power level of 4 kW. As exhibited in Figure 5.3(a), the prototype adopts a compact cubic structure, systematically separating the HV port, LV port, main and snubber transformers, SSCB and series port inductor/capacitor, and control circuit into five distinct boards interconnected via headers. This modular structure enhances the converter's serviceability, facilitating efficient maintenance and component replacement. Additionally, critical yet vulnerable devices, such as MOSFETs, gate drivers, and isolation buffers, are positioned on the outer layer of the boards, ensuring ease of access and streamlined repairs. Moreover, the surface-mounted heatsinks, directly soldered to the drain of MOSFETs, can effectively dissipate the thermal loss due to natural airflow around the outer surface of the converter.

Two iTECH6006C and 6012C power supplies are employed to emulate the behavior of DCMG and BESS, as shown in Figure 5.3(b). These power supplies can replicate any voltage function and emulate different battery stacks using iTECH BSS2000 Pro battery simulation software. Moreover, efficiency measurement and thermal analysis are carried out using the Yokogawa WT1800 precision power analyzer and Fluke Ti10 thermal imager, respectively.

A continuous test with 4 kW for more than one hour indicates that the maximum converter temperature can be observed at the LV port switches, reaching 71 ℃. This remains well below the maximum 125 ℃ allowable operation temperature for these devices. This result verifies the efficacy of thermal management design, which is crucial for the converter's reliable operation.

Multiple modulation compositions can be arranged based on the voltage levels on both sides and the criteria ($|V_C| < 10$ V) for entering into FBK-SMC modes in Q-II and Q-IV. The state machine automatically determines the optimal modulation strategy by real-time monitoring of the voltage conditions and DCMG current, ensuring the correct

modulation signals are being delivered to the switches. A hysteresis band of 1 V is introduced when entering and exiting a specific mode to avoid undesired bouncing between different modulations around the mode transition points. The switching characteristics of the final prototype are analogous to the BDSUD proposed in chapter three in terms of ZVS switching for the HV port switches and ZCS switching for the LV port switches. Compared to the previous version, the active power transfer duty cycle ($D_{a,max}$) is increased from 0.9 to 0.95, which is the consequence of modifications that decrease the component's ESR and limit the duration of current redistribution and resonance time intervals.

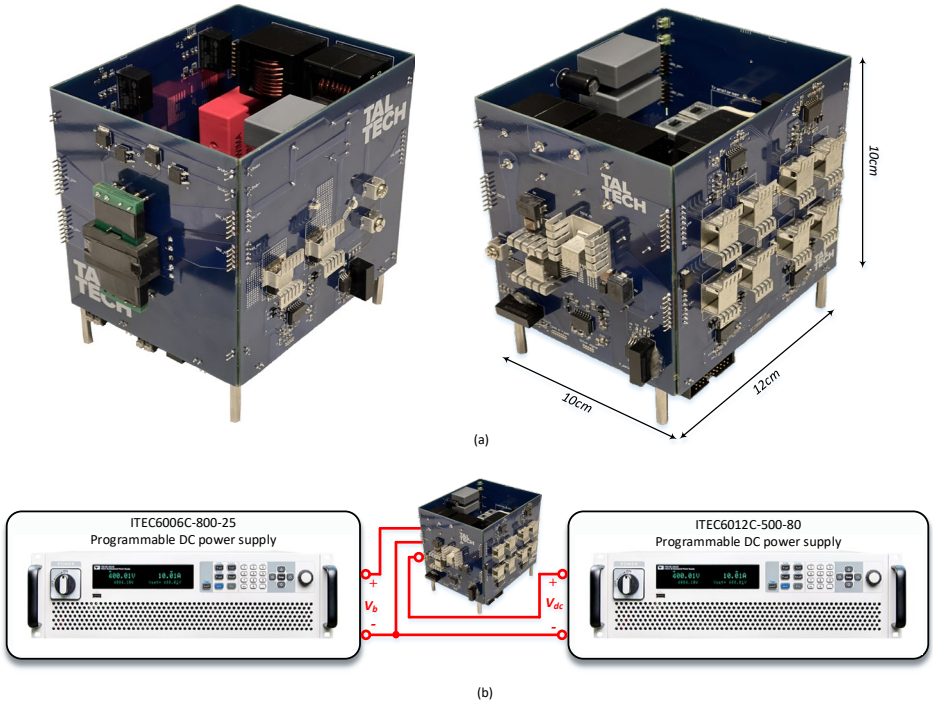

Figure 5.3. The PPC experimental prototype alongside the system connection diagram [Paper VI].

The converter underwent three distinct tests for battery voltage levels of 335 V, 350 V, and 365 V to confirm the droop control functionality in each scenario. As demonstrated in Figure 5.4(a) for the V_b = 335 V, the converter operation starts in Q-II with PSM boost modulation as ($V_{dc} < V_b$). With a gradual increase of the V_{dc} and reaching the threshold level of V_C = –10 V, the converter enters the FBK-SMC mode by software reconfiguration of the LV port and altering the modulation signals. At the instant when $V_b = V_{dc}$ = 335 V, the modulation scheme changes again, enabling the PSM buck in Q-I to obtain a step-up PPC, discharging the battery to the DCMG. While working in the 345 V < V_{dc} < 355 V range, all the PWM signals are deactivated, and only the SSCB remains active to maintain the series capacitor charge. Upon exceeding V_{dc} = 355 V, the PPC functions as a step-up converter in Q-IV, receiving boost PSM modulation. The state machine dynamically integrates four distinct modulation strategies to control the converter given this specific battery.

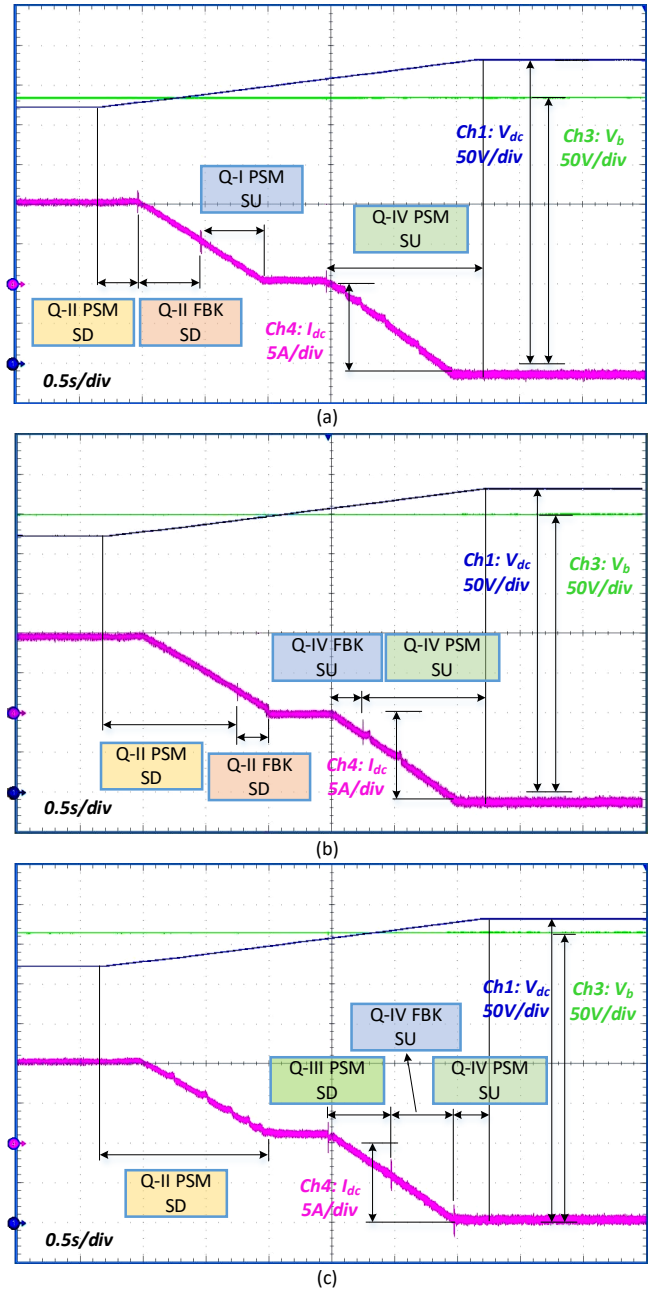

Figure 5.4. The droop control of DCMG current for three battery voltages (a) V_b = 335 V (b) V_b = 350 V (c) V_b=365 V [Paper VI].

The subsequent two case studies, corresponding to V_b = 350 V and V_b = 365 V in Figures 5.4(b) and (c), demonstrate the control strategy's capability in implementing the droop control using the PPC. The negligible current spikes at the mode change points prove that the designed feedforward approach can effectively calculate the required phase shift for the subsequent mode. Therefore, the PI controller must compensate for a minor residual error from the converter's non-idealities.

Efficiency measurements were also carried out for the PPC running under various power levels (1 kW, 2 kW, 3 kW, and 4 kW) with –60 V < V_C < 60 V, as well as for the droop control operation with three different battery voltage levels (320 V, 350 V, and 380 V). The outcomes indicate that the PPC achieves a peak efficiency level of 99.45% while maintaining a consistent efficiency above 99% across most tested points. These results are demonstrated in Figure 5.5.

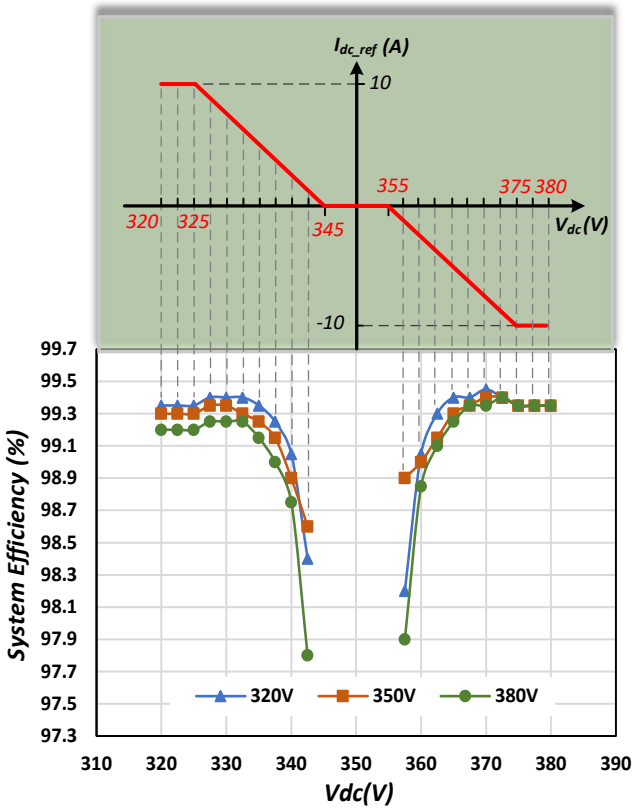

Figure 5.5. Efficiency curve for droop control operation under different battery voltages (V_b = 320V, V_b = 350V, and V_b = 380V) [Paper VI].

5.5 Summary

This chapter elaborates on thorough guidelines for designing an application-oriented step-up/down PPC based on the CSFB DC-DC converter for connecting second-life LiFePO4 BESS to a 350 V residential DCMG. The procedure starts with selecting the proper series and parallel number of battery cells to align with the nominal DCMG voltage and the building's required energy storage capacity.

In the next step, a 4 kW PPC design process can be initiated by optimally sizing the DC-DC stage based on the $K_{pr,max}$ level determined by the maximum voltage regulation range between the BESS and the DCMG. The derived power level, voltage regulation range, and voltage limits for the BESS and the DCMG will be utilized to configure the control variables of the converter and its hardware components.

Considering the converter control, there will be an outer control layer based on the linear droop control with a dead band of 10 V around the DCMG's nominal voltage.

It defines the reference current for the BESS regarding the voltage deviation from the nominal value. Subsequently, the I_{dc_ref}, battery, and DCMG voltage level will determine the appropriate operation quadrant. These data are received from sensors and filtered by the STM32G474 microcontroller. Afterward, the state machine specifies the correct converter state and utilizes the feed-forward + PI controller to regulate the DCMG current.

The converter's hardware is also designed to meet the system's voltage and power level criteria. The main and snubber transformers are the most crucial components of the converter, as their characteristics impact the converter's behavior from different points of view. Therefore, they must be designed and implemented simultaneously to reach both the optimal turns ratio and the leakage inductance levels. Moreover, the process of selecting the switching devices, the HV port capacitor, and the series port inductor are discussed.

Finally, the experimental results prove that the PPC can smoothly control the DCMG current for the different battery voltage levels (335 V, 350 V, and 365 V), incorporating various modulation schemes.

6 Future Work

The outcomes of this thesis establish a strong foundation for the design, control, and application of bidirectional step-up/down PPCs in DC microgrids. However, as the energy landscape continues to evolve with increasing emphasis on intelligent, sustainable, and interconnected systems, several promising research directions can be identified for future exploration.

Future research can focus on embedding the proposed PPC system into a smart grid or a building energy management system. By integrating communication interfaces and supporting IoT protocols (e.g., MQTT), PPCs can participate in demand-side management, real-time power balancing, and grid services such as frequency regulation and ancillary support. This necessitates the development of advanced energy management techniques and hardware, which should be capable of remote monitoring, two-way communication, and responding to dynamic grid or market feedback.

While this work has demonstrated the efficacy of modulation methods and topology morphing control (TMC), small- and large-signal analysis is still required to assess stability margings. Moreover, non-linear control principles could be applied to enhance the dynamic response of the developed converter. In addition, predictive diagnostics and fault classification algorithms can be developed using historical converter data to enable proactive maintenance and fault isolation.

The current work focuses on a two-port topology; however, future efforts could explore multi-port converter architectures capable of simultaneously managing multiple inputs and outputs (e.g., PV, BESS, EV charger, and DC loads). On the other hand, these topologies would require decoupled power flow control strategies. Furthermore, investigating modular converter implementation could improve system scalability, fault tolerance, and ease of deployment in diverse microgrid configurations.

The long-term operation of PPCs, especially in systems interfacing second-life battery energy storage, requires analysis of converter reliability and aging behavior. Future studies could focus on modeling electrothermal stress across power semiconductors and magnetics, thermal stresses verification, and accelerated life testing. These insights could enable predictive maintenance and improve the overall robustness of converter deployments in residential or industrial settings.

Finally, a comprehensive environmental and economic evaluation of PPC-based systems should be conducted. Life-cycle assessment methods can be applied to quantify the environmental impact associated with materials, manufacturing, operation, and end-of-life phases. Concurrently, techno-economic modeling can compare the cost-effectiveness of partial power conversion strategies against traditional full power converter systems, under various usage scenarios and deployment scales.

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Abstract

Design and Control of Bidirectional Step-Up/Down Partial Power Converters for DC Microgrid Applications

This PhD thesis is dedicated to the development of a high-efficiency step-up/down partial power converter for DC microgrid applications. The proposed type of converters can be utilized as an interface between battery energy storage or PV and a residential DC microgrid. It is proven that the proposed converter can provide higher efficiency than full power converters while featuring much lower stresses on switching and passive components.

The proposed converter possesses superior efficiency levels as well as a variety of features that are mostly overlooked in the literature on partial power converters, making it a suitable candidate for residential DC microgrid applications. Among these features, the most significant ones are the smooth combination of different modulations for seamless mode transitions, protection strategies for faulty and transient conditions, and the application of low-voltage compact switching devices for efficiency enhancement and simpler thermal management.

The current source full bridge DC-DC converter with four-quadrant switches is selected as the DC-DC stage considering its unique characteristics, like full soft-switching operation within the entire voltage and power regulation range of the converter and negligible power circulation between its ports. Afterward, the designed partial power converter is compared to a dual active bridge-based counterpart to prove its superior performance. It is demonstrated that the proposed solution demonstrates a much wider soft-switching range and lower stresses on components compared to the closest existing counterpart, particularly around zero partiality, suggesting it can be a potential replacement for the mature technology of full power converters.

A soft start procedure is implemented for the proposed converter to prevent the inrush current of the series capacitor during the converter startup by precharging the series port capacitor. A methodology is also developed to diagnose short circuit and open circuit faults based on the sensor signal and the converter voltage-current parameters and clear them with the help of the implemented SSCB and LV port switches.

A state machine is also designed to combine advanced modulation techniques for PPC in different operation quadrants and ensure smooth current regulation within quadrants and seamless transition between different quadrants. Such techniques were not demonstrated in the literature for step-up/down PPCs.

The final prototype of the proposed PPC was built with a power level of 4 kW and the processed power was limited to 18.75%. The droop control strategy was utilized to control the power flow between a battery energy storage and a 350 V residential DC microgrid. The proposed converter regulates DC microgrid current smoothly by combining six different modulations, proving its functionality as a practical high-efficiency (99–99.45%) converter for this application.

The scientific findings of this thesis contribute to the field of power electronics, particularly partial power processing electronic systems. The obtained results close the gap between the theoretical research and practical implementation of step-up/down partial power converters and provide solutions to enable the industrialization of this technology. Therefore, the outcomes of this thesis contribute to the widespread adoption of step-up/down PPCs in DC microgrid applications.

Lühikokkuvõte

Alalisvoolu mikrovõrkudele osavõimsuse töötlusega kahesuunalise tõste-langetusmuunduri projekteerimine ja juhtimine

See doktoritöö on pühendatud effektiivse osavõimsusega pinge tõste-langetusmuunduri (OVM) väljatöötamisele alalisvoolu mikrovõrgu rakendusteks. Väljapakutud muundureid saab kasutada liidesena akutoite või päikesepaneelide ja elamu alalispinge mikrovõrgu vahel. On tõestatud, et antud muundur on energiatõhusam kui täisvõimsusega töötavad muundurid, omades samal ajal palju väiksemat pinge- ja voolustressi lülitus- ja passiivkomponentidele.

Lisaks suurepärasele energiatõhususele pakub antud muundur ka omadusi, mis on enamasti jäänud tähelepanuta osavõimsusega muundureid käsitlevas kirjanduses kuid võiks hästi sobida just elamute alalispinge mikrovõrgu rakendustes. Nendest omadustest kõige tähelepanuväärsemad on modulatsioonimeetodite kombineerimine saavutamaks sujuvat töörežiimide muutust, kaitsealgoritmid vigade ja siirdeprotsesside jaoks, madalapingeliste kompaktlülitite rakendamine, mis tõstab kasutegurit ja lihtsustab termilist disaini.

Voolutoiteline täissild nelja kvadrandiliste lülititega valiti alalispinge astme teostuseks, arvestades tema erilisi tunnuseid nagu täis pehmelülitus üle terve töövahemiku ja minimaalne tsirkuleeriv energia tema erinevate portide vahel. Et tõestada pakutud lahenduse tõhusus, võrreldakse projekteeritud OVM-t alternatiivse kaksikaktiivsilla topoloogiaga. Võrdlus näitab, et välja pakutud muunduri topoloogia omab laiemat pehmelülitusvehmikku ja väiksemat voolu- ja pingestressi komponentidele, mistõttu on tegu potensiaalse alternatiiviga täisvõimsusega muunduritele.

Muunduri kontrollitud käivituse eest vastutab sujuvkäivitusalgoritm, mis laeb täis jadapordi kondensaatorid, et vältida suuri voolutõukeid sisselülitamisel. Samuti on välja töötatud metoodika lühise ja avatud ahela rikete diagnoosimiseks anduri signaali ja muunduri pinge-voolu parameetrite põhjal ning nende kõrvaldamiseks kaitselülitite ja madalpinge-pordi lülitite abil.

Samuti on loodud olekumasin, mis ühendab täiustatud modulatsioonitehnikaid OVM-te jaoks erinevates töökvadrantides ning tagab sujuva voolu reguleerimise ja sujuva ülemineku erinevate kvadrantide vahel. Selliseid tehnikaid OVM-te puhul ei ole varem demonstreeritud.

OVM lõplik prototüüp ehitati võimsusega 4 kW kus osavõimsuse piiriks seati 18.75%. Aku energiasalvesti ja 350 V elamu alalispinge mikrovõrgu vahelise võimsusvoo juhtimiseks kasutati pinge droop juhtimise strateegiat. Kavandatud muundur reguleerib alalispinge mikrovõrgu voolu sujuvalt, kombineerides kuut erinevat modulatsiooni meetodit. OVM tõestas oma funktsionaalsust ja suurt efektiivsust (99–99,45%) sellises rakenduses.

Selle väitekirja teaduslikud tulemused panustavad jõuelektroonika valdkonda, eriti osavõimsusega muunduritesse. Saadud tulemused sulgevad lünga OVM-te teooria ja praktilise rakendamise vahel ning pakuvad lahendusi selle tehnoloogia industrialiseerimiseks. Ühtlasi aitavad käesoleva doktoritöö tulemused kaasa OVM-te laialdaseks rakendamiseks alalispinge mikrovõrkudes.

Appendix

Publication I

Hassanpour, N., Blinov, A., Chub, A., Vinnikov, D., & Abdel-Rahim, O. (2021, November). A series partial power converter based on dual active bridge converter for residential battery energy storage system. In 2021 IEEE 62nd International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON) (pp. 1-6). IEEE, doi: 10.1109/RTUCON53541.2021.9711725.

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A Series Partial Power Converter Based on Dual Active Bridge Converter for Residential Battery Energy Storage System

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***Abstract*—Conventional Full Power DC-DC Converters (FPC) which process whole power between their input/output, are close to their limits in terms of efficiency and power density. One of the most promising solutions to overcome these limits is Partial Power Converters (PPCs). In this paper, a Series PPC (S-PPC), which connects a Residential Battery Energy Storage System (RBESS) to a DC-bus is introduced. In the proposed converter, in its critical point, just 27% of the overall power is processed. Application of a Dual Active Bridge (DAB) converter with bidirectional/bipolar Current Source (CS) port enables the buck-boost operation of the S-PPC in both charge and discharge operation mode. So, the processed power is further decreased. Simulations are done in PSIM to validate the mathematical analysis.**

Keywords— DC-DC converter; S-PPC; Pariality; Battery Energy Storage System(BESS), DAB converter with CS port

I. INTRODUCTION

Buildings, where nearly 40% of global energy is consumed, have great impact on the energy sector all over the world. They account for nearly 2790 Mtoe in 2010 and experts expect it to go over 4400 Mtoe by 2050[1]. It is followed by CO_2 emission increase, specifically in developing countries. These issues are the driving motivations for different countries and organizations to focus more on the building energy sector. The result is a variety of regulations for newly built buildings and modifications of old buildings. The European Commission has legislated strict rules for new buildings and in 2016 the commission established guidelines for the promotion of nearly zero-energy buildings (NZEBs)[2]. The concept of NZEB contains two major measures for every building: first, a building has to be at the highest energy performance. Second, the remaining low amount of energy must be produced from on-site renewable energy resources. Improvements in the field of modern power electronics have enabled the new buildings to be more efficient and capable of on-site energy production [3]. Power electronics enables the implementation of DC distribution grids in buildings. In comparison with the AC distribution grid, the DC one can simplify a wide variety of power conversion devices, such as power adapters in home appliances, AC/DC power supplies, LED drivers, and so on. Moreover, the modular connection of PV and battery energy storage systems is simplified in the DC distribution system [4]. It is shown that energy saving up to 15% can be achieved by DC distribution including on-site energy generation and energy storage systems. The cost-effectiveness of the system was also analyzed and it is proven that DC distribution system with storage and on-site generation is more cost-effective than an AC system[5]. There are several voltage ranges for DC microgrids from 12 to 800 V among which the 380-400V range is the most techno-economically feasible range in data centers and telecommunication systems [6].

The energy storage systems are the main contributors of NZEBs in terms of independency from grid due to fluctuating characteristics of renewable energy systems [5]. Parallel-series connection of battery cells can be connected to the DC microgrid. Usually, the ratio of power and capacity for the residential batteries is between 0.25-0.75W/(W.h). Within this range, the 0.25W/(W.h) is the most economically feasible point where major implementations are done [7]. The capital cost of energy storage systems is rather high and a detailed design and optimization must be considered in battery and interface converter design [8]. The price is typically in the range of 1-2 kEUR/KWh. The dominant voltage level of residential batteries is around 50V and they require a complex converter which, in most cases, utilizes high turn ratio transformers and increased number of energy conversion stages that lower the efficiency. The overall round/trip efficiency of 90% is a limit for such systems, while the application of high voltage batteries enables the use of non-isolated converters with higher efficiencies [9]. Results of a comparison between 220V and 380V DC residential microgrid with 220V AC reveals that the efficiency of the system is increased 4% and 10% respectively for 220V and 380V[10]. Therefore, there is strong motivation toward high voltage DC-DC converters for battery integration. There are two major groups of DC-DC converters: first, Full Power Converters (FPC) [11]–[13], which are typical systems that process whole power between the DC-bus and the battery. Second, Partial Power Converters (PPC), which have a higher share of power transferred directly to/from the DC-bus and the battery. The lower processed power means higher efficiencies and lower energy costs. A comparison between Dual Active Bridge (DAB) based FPC DC-DC and PPC DC-DC shows a 3% efficiency increase for a 3.3kW system with a nominal battery voltage of 380V. 70% of total power is transferred directly between battery/DC-bus. In addition to efficiency improvement, PPC can elevate the power density of the converter and the utilization of low power components. As a result, the overall cost of the converter can be further decreased[14]. PPCs can reach their best performance when the voltage difference between input and output terminals is low. This will be explained in detail in the following sections. Therefore, they are promising candidates for high voltage battery applications. Several PPCs are discussed in the literature and their application as battery or PV interface is analyzed. Based on the voltage range of the battery/PV three options can be discussed. Buck, Boost, and Buck-Boost PPC[15]. It is concluded that in the Buck-Boost PPC, processed power can be further decreased. The converter efficiency reaches 99.6% at the maximum point. The volume of the converter decreased by 23.4% for a 750W buck-boost converter in comparison with a boost converter[16]. Another 22kW buck-boost converter is implemented and the maximum efficiency of 99% is obtained[17].

In this paper a buck-boost S-PPC converter based on Dual Active Bridge Converter (DAB)with CS port and Phase Shift

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Modulation (PSM) is introduced to decrease the partiality of the converter. The DAB converter has bidirectional capability as well as capability of changing voltage polarity in CS side (low voltage port) without any change in the topology. Therefore, it is able to work in all voltage/current quadrants. Furthermore, it is shown that the DAB converter has soft switching characteristics in a wide regulation range which will further increase the efficiency of S-PPC, making it a strong candidate for PPC application.

II. Series Partial Power Converters

A. Configuration analysis

In this section the two widely researched S-PPC configuration for connection of a DC-DC switch mode converters with almost lossless direct path are discussed. The first one is Input Parallel Output Series (IPOS) which is shown in Fig. 1(a) where the battery voltage V_B is equal to DC-DC converter input voltage V_{Conv} .The output current of the DC-DC converter (I_C) is also equal to the DC-bus current(I_{DC}). The second configuration in Fig. 1(b) is Input Series Output Parallel (ISOP). In this configuration the input current of the DC-DC converter (I_C) is equal to the battery current (I_B) and the output voltage of DC-DC converter (V_{Conv}) is equal to the DC-bus voltage (V_{DC}). The power share between these two paths (direct and DC-DC converter) in both configurations just depends on the voltage gain of the S-PPC which is denoted as G in this paper [15]. In both configurations the P_P is processed power and P_U is unprocessed power.

Configuration I:

In this configuration (Fig. 1a) the following equations can be obtained.

$$V_{DC} = V_C + V_B \tag{1}$$

$$I_B = I_{DC} + I_{Conv} \tag{2}$$

It performs as step-up converter for $V_C > 0$ or as step-down converter for $V_C < 0$. Considering (1) and (2), the voltage gain of S-PPC can be calculated as:

$$G = \frac{V_{DC}}{V_B} = 1 + G_C , \tag{3}$$

where G_C is the DC-DC converter voltage gain.

Based on the sign of the output voltage of the DC-DC converter (V_C), the S-PPC can be buck or boost converter.

Configuration II:

For the second configuration (Fig. 1b) the equations can be calculated as follows:

$$V_B = V_C + V_{DC} \tag{4}$$

$$I_{DC} = I_B + I_{Conv} \tag{5}$$

According to (4) and (5) the voltage gain of S-PPC can be calculated as:

$$G = \frac{V_{DC}}{V_B} = \frac{1}{1 + G_C} \tag{6}$$

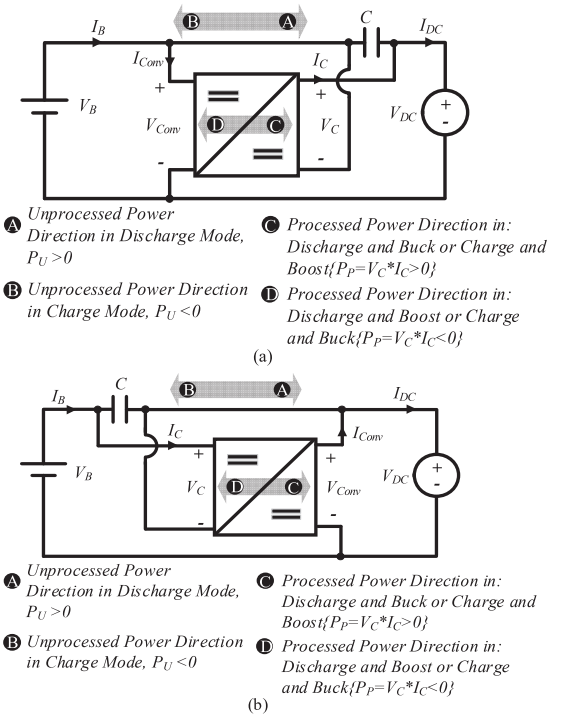

Fig. 1. S-PPC configurations (a) IPOS (b) ISOP.

Regarding (4) and (5), this configuration will be a step-up converter for $V_C < 0$ and step-down converter for $V_C > 0$.

For a DC-DC converter with Uni-Polar characteristic, one of the step-up or step-down modes can be implemented for each configuration. If the DC-DC converter can change its output voltage polarity, both modes can be reached at the same time. Therefore, with a Unipolar DC-DC converter only step-up or step-down mode can be achieved regardless of the configuration. On the other hand, a Bipolar DC-DC converter enables the step-up/down S-PPC operation.

B. Active power analysis

To analyze the performance of S-PPC converters a coefficient of partiality is defined to realize the amount of power processed by the DC-DC converter. It is defined as:

$$K_{Pr} = \frac{P_{in-Conv}}{P_{in}} \tag{6}$$

Here in this paper $P_{in} = P_B$. Efficiency of the S-PPC is

$$\eta_{sys} = \frac{P_{DC}}{P_B} = \frac{1 - P_{loss-Conv}}{\frac{P_{in-Conv}}{K_{Pr}}} \tag{7}$$

Where P_B is the battery power and P_{DC} is the power delivered to the DC-bus.

$$\eta_{Conv} = \frac{P_{loss-Conv}}{P_{in-Conv}} \tag{8}$$

Then,

$$\eta_{sys} = 1 - K_{Pr} * (1 - \eta_{Conv}) \quad (9)$$

From (9) it is clear that in a real condition, the overall efficiency of the S-PPC depends on both K_{Pr} and the DC-DC converter efficiency η_{Conv}.

For IPOS regarding (1) and (2) the K_{Pr} can be calculated as:

$$K_{Pr1} = \frac{P_{in-Conv}}{P_B} = \frac{I_B - I_{DC}}{I_B} = 1 - \frac{\eta_{sys}}{G} \quad (10)$$

Substituting (9) in (10) results in

$$K_{Pr1} = \frac{G-1}{G-1+\eta_{Conv}} \quad (11)$$

In order to compare different configurations, the DC-DC converter can be assumed ideal but for final design the (11) must be considered as real coefficient of partiality. By assuming lossless DC-DC converter the K_{Pr} is

$$K_{Pr1} = 1 - \frac{1}{G} \quad (12)$$

For ISOP configuration described by (4), (5), and (6) the following results can be derived

$$K_{Pr2} = \frac{P_C}{P_B} = \frac{V_B - V_{DC}}{V_B} = 1 - G \quad (13)$$

As it is illustrated in Fig. 2, the coefficient of partiality directly depends on the voltage gain of the converter. It means that moving from unity voltage gain to the boost operation or buck operation, the partiality will be increased. Negative partiality coefficient means reverse power flow inside DC-DC converter. In addition to partiality factor, another important factor for a S-PPC as battery interface is having bidirectional power flow characteristic. As it is illustrated in Fig. 1, the power flow is bidirectional for both configurations. It requires DC-DC converter to be bidirectional. For the Buck and Boost S-PPC, the sign of V_C does not change in whole operation range of the converter. As a result, the bidirectional DC-DC converter in both S-PPCs will operate in two quadrants. On the other hand, for the Buck-Boost S-PPC, the DC-DC converter will operate in four quadrants, as it changes both current direction and voltage polarity. It is shown in Fig. 3.

III. Case Study

For a DC-bus with nominal voltage of 350±30V, there can be three options to implement as interface between the battery and DC-bus. Firstly, the battery cell specifications must be chosen as a reference for further steps. In this case study, the CTS-S8688190, lithium-ion Nickel Manganese Cobalt (NMC) type is selected. In Table I, the battery cell specifications are listed. Regarding Buck/Boost, Buck, and boost converters along with the battery cell voltage range, the number of battery cells must be selected in a way that the following criteria will be fulfilled [16].

I. For Buck-Boost converter, the nominal battery voltage must be around nominal DC-bus voltage.

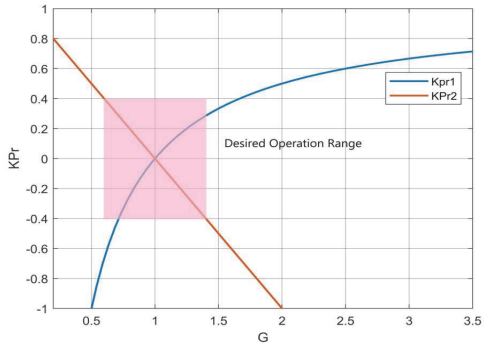

Fig. 2. Partiality coefficient for IPOS and ISOP configurations

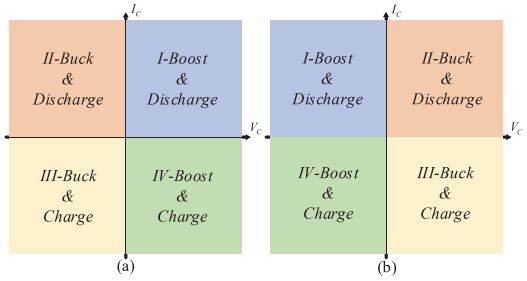

Fig. 3. DC-DC convertre operation quadrants regarding S-PPC operation mode (a) IPOS configuration (b) ISOP configuration

TABLE I. The Lithium-ion (NMC) battery cell specifications

Item	CTS-S8688190
Nominal capacity	15Ah
Nominal Voltage	3.6V
Operating Voltage Range (charging and discharging cutoff voltage)	(3 - 4.2) V
Charging Voltage	4.2V
Standard charging Method (maximum cell current)	0.5C

II. For Buck converter, minimum DC-bus voltage must be higher than maximum battery voltage.

III. For boost converter, maximum battery voltage must not exceed minimum DC-bus voltage.

Considering these requirements, the battery number for each option can be calculated as in Table II.

TABLE II. Battery cell numbers for each S-PPC type

S-PPC type	Number of battery cells
Buck-Boost	$N_{Batt} \approx \frac{V_{DC-nominal}}{V_{B-nominal}} = 97$
Buck	$N_{Batt} \geq \frac{V_{DC-\max}}{V_{B-min}} = 127$
Boost	$N_{Batt} \leq \frac{V_{DC-min}}{V_{B-max}} = 76$

In respect to the DC-bus voltage range and the battery specifications in Table I, the cell number equals 97, 127, and 76 respectively for Buck-Boost, Buck, and Boost operation modes. From (12) and (13) the maximum coefficient of partiality can be calculated for the three S-PPC type. In each S-PPC type there are four critical points regarding battery and DC-bus voltage ranges. As it can be seen from Fig. 4(b) for boost S-PPC, both IPOS and ISOP configuration reach to their maximum partiality coefficient in same point ($V_B = 228V$ and $V_{DC} = 380V$). This point is where the voltage difference between battery and DC-bus is at the maximum. Therefore, the S-PPC voltage gain will be maximum and according to Fig. 2, reaching to the maximum partiality in this point is logical. Moreover, for the buck converter, operation of which is shown in Fig. 4(c), same discussion is valid. The converter reaches the maximum partiality regardless of the configuration in a point where the voltage difference between battery and DC-bus is at maximum ($V_B = 533.4V$ and $V_{DC} = 320V$). On the other hand, utilizing buck-boost S-PPC and selecting nominal battery voltage equal to the nominal DC-bus voltage results in decreasing voltage difference between the battery side and the DC-bus side. This is the main reason for significant decrease in partiality when buck-boost converter is selected. It is depicted in Fig. 4(a). The maximum partialities are shown in Table III.

TABLE III. MAXIMUM PARTIALITY COEFFICIENT FOR DIFFERENT S-PPC TYPES AND CONFIGURATIONS

S-PPC type	Maximum K_{Pr}
Buck-Boost	$K_{Pr1max} = -0.27$ $K_{Pr2max} = 0.3$
Buck	$K_{Pr1max} = -0.67$ $K_{Pr2max} = 0.4$
Boost	$K_{Pr1max} = 0.4$ $K_{Pr1max} = -0.67$

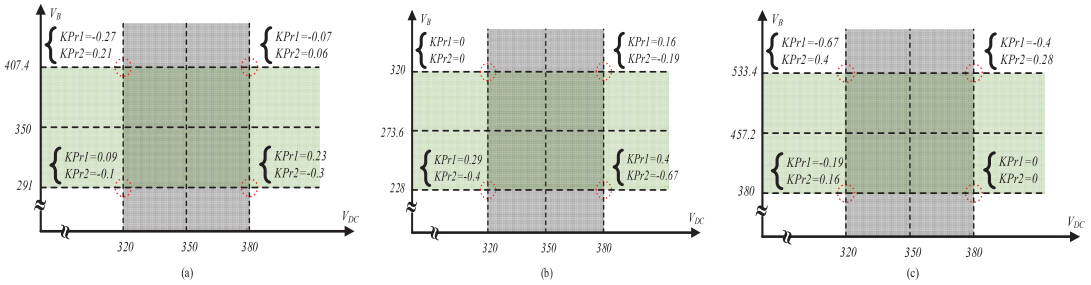

Fig. 4. Critical points based on Battery and DC-bus volatge variation for IPOS and ISOP configurations (a) Buck-Boost S-PPC (b) Boost S-PPC (C) Buck S-PPC

IV. PROPOSED S-PPC CONVERTER

The proposed topology is depicted in Fig. 5. It is based on IPOS configuration, which can be seen from the circuit connections. The topology consists of a bidirectional isolated Dual Active Bridge (DAB) converter with a CS port and with ZVS/ZCS feature in a wide regulation range. The modulation method for the converter is Phase Shift Modulation (PSM). Therefore, the phase shift and transformer turn ratio (n) are two variables that must be selected to reach the desired voltage gain and voltage regulation range. It also utilizes a specific phase shift method to decrease the energy circulation to further increase the efficiency[18], [19].In addition to bidirectional characteristic, the other important characteristic of this topology is the ability to work in both negative and positive voltage polarities at the CS side. Connection of CS port to DC-bus allows better control on the current of DC-bus. In the following all four quadrant operation modes of the converter are elaborated.

A. Quadrant I (Boost and Discharge mode)

In this operation mode the V_C and I_C are positive. Hence, the energy transfer within DAB converter is from Voltage Source (VS) side to CS side. According to operation principles of the DAB converter, the switching pattern must be buck operation of DAB converter for positive output voltage. It means that, $S_{1.2}$ and $S_{3.2}$ are always turned on in this mode. At the bottom side $S_{2.1}$ and $S_{4.1}$ are always turned off in this mode and their body diode acts as reverse blocking diode to prevent current flow in reverse direction. The $S_{1.1}$ and $S_{3.1}$ operate with constant phase and 180º shift relative to each other. The Bottom active switches ($S_{2.2}$ and $S_{4.2}$) have 180º shift relative to each other. At the same time, they are shifted a specific amount in regard to the top switches ($\varphi_{Control}$). S_5 and S_6 are in synchronous rectification mode with a specific constant phase shift relative to $S_{1.1}$ and $S_{3.1}$.

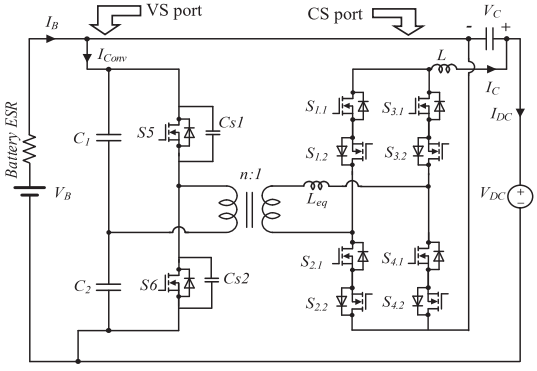

Fig. 5. Proposed S-PPC converter

B. Quadrant II (Buck and Discharge mode)

In this mode V_C is negative and I_C is positive. The energy flow direction within DAB converter is from CS (DC-bus) side to VS(Battery). According to [18], [19]for the mentioned power direction and negative voltage polarity, the boost operation mode of DAB converter is utilized and the switching signals are based on boost mode switching with negative CS side voltage. In this situation, $S_{2.1}$ and $S_{4.1}$ are always turned on and $S_{1.1}$ and $S_{3.1}$ are always turned off in this mode. $S_{2.2}$, $S_{4.2}$ and $S_{1.2}$, $S_{3.2}$ have 180º shift relative to each other. Additionally, $S_{1.2}$ and $S_{3.2}$ are shifted in regard to bottom switches ($\varphi_{Control}$). S_5 and S_6 are in synchronous rectification mode with a specific constant phase shift relative to $S_{2.2}$ and $S_{4.2}$.

For quadrant III the switching signals are according to Buck operation of DAB converter with negative CS side voltage. Furthermore, for the quadrant IV, the switching pattern is according to boost operation of DAB converter with positive CS side voltage.

In all four quadrants the control variable is the phase shift between top and bottom switch pairs in CS side ($\varphi_{Control}$). As it can be seen, for every mode some switches are on, some are off, and the remaining in operation. The control algorithm must recognize the operation quadrant and based on the order from the algorithm, the appropriate switching signals are imposed. The reference current and the battery voltage are to main factors which specify the quadrants.

V. Simulation Results

Simulation is done using PSIM software. The DC-bus voltage rises from 320V to 380V in 400ms. Two case studies are simulated. In the first one battery voltage is 320V and in the second one is 380V. So, the S-PPC is expected to work as boost converter is the first case study and as a buck converter in the second one. The reference current in Fig. 6. must be followed in both case studies. The simulation is done based on values and parameters in Table IV.

TABLE IV. Converter Parameters

Parameter name	value
V_B	320V, 380V
V_{DC}	320-380V
Battery ESR	300mΩ
L	200μH
C_1, C_2	47 μF
L_{eq}	10μH
C_{S1}, C_{S2}	10nF
Transformer turn ratio(n)	2.3
Output capacitor	200 μF
Switching frequency	50kHz

Simulation results are obtained to verify the capability of the S-PPC in following the reference current and to compare the partiality factor with the theory. In Fig. 7. The battery voltage is 320V. As it can be seen from Fig. 7(a) the S-PPC correctly injects the reference current to the DC-bus. The S-PPC works as boost converter in this mode and the maximum partiality coefficient must be driven in $V_{DC} = 380V$.

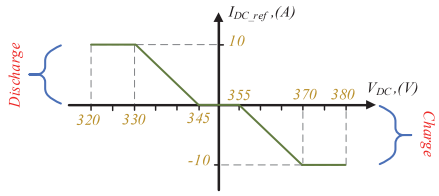

Fig. 6. Droop control of DC-bus cuurent based on DC-bus voltage

From the Fig. 7(b) the K_{Pr} is 15.5%. For the second case study the results are depicted in Fig. 8. The Fig. 8(a) demonstrates that the S-PPC follow the reference current. From the Fig. 8(b) the maximum K_{Pr} is 16.5% for $V_{DC} = 320V$. The results clearly confirm the mathematical calculations which are done in previous sections with a slight difference.

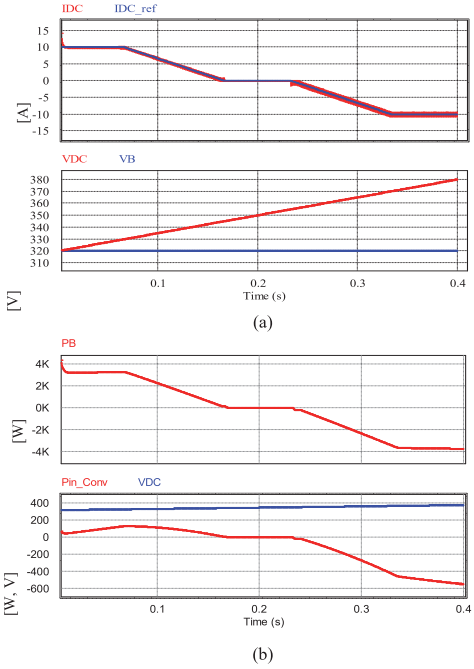

Fig. 7. Simulation results for $V_B = 320V$ (a)reference current (b) Total power and processed power

The simulation results are in accordance with the theoretical partiality for each case with a slight difference which stems from battery ESR and other non-ideal components loss. The partialities for idea converter and battery were 16% and 18.5% respectively for *VB=320V* and *VB=380V.*

VI. Conclusion

In this paper a series partial power converter based on IPOS configuration and DAB converter with CS port is introduced. The DAB converter can operate in all four quadrants regarding its voltage and current. This

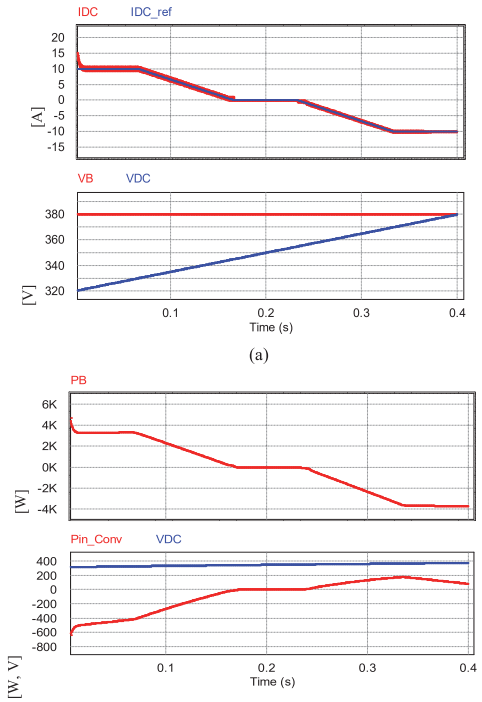

Fig. 8. Simulation results for $V_B = 380V$ (a) Reference current (b) Total power and processed power

characteristic enables the S-PPC to act as a buck-boost DC-DC converter. Hence, the battery nominal voltage can be chosen equal to the DC-bus nominal voltage. A case study for a battery with 97 cells is done for 320V and 380V. Simulation results confirms the correct reference current follow in the all four quadrants. The maximum partiality for two cases is 15.5% and 16.5% respectively.

VII. Acknowledgment

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Publication II

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Comparison of Full Power and Partial Power Buck-Boost DC-DC Converters for Residential Battery Energy Storage Applications

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***Abstract*— In this paper, a Series Partial Power dc-dc Converter (S-PPC) is compared with Buck-Boost Full Power dc-dc Converter (BBFPC) as an interface between Battery Energy Storage System (BESS) and dc microgrid. To achieve a fair and accurate result, several Key Performance Indicators (KPI) are considered. non-active power processing, Component Stress Factor (CSF), and efficiency of both converters are compared at three points of battery charging (3 kW, 2 kW, and 1 kW) and three points of battery discharging (3 kW, 2 kW, and 1 kW) application. Due to full power processing in BBFPC, higher non-active power processing, and CSF occurs in all operation points of the converters. Furthermore, the efficiency estimation results show that S-PPC has higher efficiency than BBFPC in all operation points, which was estimated using PSIM thermal module. Datasheet parameters of all the components are imported to the software library to simulate both converters. The simulation results confirm theoretical calculations and predictions.**

Keywords—dc-dc converters, Partial Power Converters, buck-boost full power converter, non-active power, component stress factor, efficiency, battery energy storage.

I. INTRODUCTION

Nowadays, renewable energy sources are penetrating a variety of applications. As one of the most important examples, the residential application of rooftop photovoltaic (PV) panels and small wind turbines can significantly reduce the CO_2 emission of buildings [1]. It is worth mentioning that the buildings are the source of more than 40% of overall CO_2 emissions in the world. The interconnection between renewable energy sources and loads in such applications can be implemented either by a conventional ac grid or dc microgrid. According to literature, it is proven that utilizing a dc microgrid can boost the overall system efficiency by up to 15%. This advantage stems from fewer energy conversion losses due to removing additional energy conversion stages (inverters/rectifiers), which is typically the last stage before the ac grid [2], [3]. The emergence of dc microgrids necessitates high-efficiency dc-dc converters to be implemented in different parts of the grid as an interface between dc microgrids and sources/loads. The conventional approach is to use full power dc-dc converters (FPCs). In these kinds of converters, all the active power between source/load or input/output is processed by the converter components.

On the other hand, the novel approach is partial power dc-dc converters that process only a small percentage of total power inside converter components. They can be divided into differential partial power processing dc-dc converters to regulate the current between two adjacent elements or between an element and the dc bus. The second type is the series partial power dc-dc converters (S-PPCs) that are used mainly for voltage regulation between two elements that can be source, load, dc-bus, or a battery energy storage system [4], [5].

In FPCs, all the converter components are under full load and experience full voltage or current stress. In the case of non-optimized design, the current stress can increase to huge amplitudes, which can damage or speed up their degradation process. Such a case is typical in switched-capacitor based dc-dc converters [6]–[9], as they experience extreme current stress. Furthermore, the high voltage stress of devices can trigger several unpleasant issues. Switched-inductor-based topologies suffer from this issue. Junction breakdown in switching devices and insulation degradation in transformers and inductors are some of the most typical problems of high voltage stress. To avoid any failure in FPCs and reliable operation of the converter over a certain time, the converter components mostly are overdesigned from the voltage and current rating point of view. The consequence is higher converter cost and larger devices that decrease the power density of the converter.

On the other side, the S-PPC concept decreases the processed power by either series or parallel connection in input or output power. Therefore, in the series port, the switching devices experience lower voltage stress. Moreover, in the parallel port due to decreased current processed by a converter, the switching components are under lower current stress than that in an FPC with the same power and voltage levels. As a result, S-PPCs employ devices with reduced current/voltage rating, which decreases the overall cost of the converter as well as increases the power density.

Most of the papers in the literature are just considering the active power processing as an identifier to compare various S-PPC topologies. Although it is the essential factor of an S-PPC and has the most impact on the efficiency of the whole converter, neglecting non-active power processing can decrease the validity and accuracy of any comparison. In the definition of partial power converters, it is strongly stated that to consider any converter as a partial power converter, it must decrease active power processing as well as non-active power processing [4], [5].

To quantify the differences between the FPCs and S-PPCs, there is a need to perform some numerical benchmarking. There are different key performance indicators (KPIs) to calculate for

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every converter to benchmark them in specific points regarding the same KPIs. The most important performance indicator is the converter efficiency at different power levels. In [10], the performance of three S-PPC converters is compared considering them as dc-dc interface converters for a two-stage PV system. It is concluded that the step-up S-PPC based on the full-bridge (FB) dc-dc converter reaches up to 98.5% efficiency which is higher than the step-down converter with 97.5% efficiency. Another comparison between FB-based S-PPC and FB-based FPC demonstrates an efficiency difference of 7% for the full-power operation (822W). In [11], three converters are compared for a 750W application. It is shown that the FB-based S-PPC reaches higher efficiency than both a conventional boost converter and a flyback-based S-PPC (about 1% and 4% respectively).

The second important KPI in non-active power processing. In [12]non-active power processing is formulated and experimentally verified for an FB-based S-PPC, conventional boost, and flyback-based S-PPC. The results reveal that the flyback-based S-PPC cannot be considered a real partial power converter as it processes the same amount of non-active power with a conventional boost. In most of the papers in the literature, this parameter is ignored. Hence the results are not completely clear for benchmarking [13].

The third KPI that must be calculated is the component stress factor (CSF) which is of significant importance to selecting appropriate devices for the converter. Exact calculations and experimental validations for CSF can enhance converter reliability and lifetime. In [14], [15], two well-known isolated dc-dc converters are compared from the CSF point of view. The Dual Active Bridge (DAB) converter and Isolated Full bridge Boost (IFBB) are analyzed considering stress on switching devices, capacitors, and windings. The obtained results confirm that IFBB achieves lower overall CSF and proves its suitability for partial power application. In [16], the FB-based S-PPC and FB-Push/Pull-based S-PPC are investigated. The output-side CSFs prove that the FB-Push/Pull-based S-PPC has lower CSF in all operation points due to step-up/down characteristics that lower the voltage regulation range, and consequently, the processed power.

In this paper, the S-PPC based on the current-source FB dc-dc converter (CSFB) [17] is compared with the conventional four-switch buck-boost full-power converter. Non-active power processing, CSF, and efficiency are considered KPIs to benchmark both converters. The organization of the paper is as follows. In the second section operation principles of both converters are elaborated. In section III, the non-active power concept, CSF, and efficiency estimations are provided and simulation results are brought out. Finally, the discussions and conclusions are presented in sections IV and V, respectively.

II. Operation Principle of Converters as a Battery Energy Storage Interface

A. CSFB based S-PPC

The proposed converter is illustrated in Fig. 1(a). It is connected according to the input parallel output series (IPOS) configuration. So, on the battery side, there will be a current division between the series path and dc-dc stage and most of the input current will flow through the series path. Consequently, the voltage source (VS) side switches are experiencing lower continuous and peak currents. At the dc microgrid side, the output of the dc-dc stage is connected in series with the battery and dc microgrid. So, the switches of this port are under lower average and peak voltages. This topology can work in all four quadrants considering I_c and V_c in Fig. 1(a). The detailed modulation scheme and control strategy is elaborated on in previous papers. To achieve the highest possible accuracy of results in the simulation of PSIM software, real parameters of all the converter components are imported to the PSIM thermal module to analyze the converter loss and stresses which are collected in Table I.

B. Buck-Boost Full Power Converter (BBFPC)

Four-switch BBFPC is a widely utilized converter in both PV and battery applications due to its simple structure and control system. Keeping positive voltage polarity in both input and output can change the current direction also. So, BBFPC can be easily implemented as an interface between battery energy storage and s dc microgrid. The conventional control approach is three-mode control for battery discharge and charge operation modes. They can be buck, boost, or buck-boost modes. The buck-boost control strategy is applied when input and output voltages are almost equal with slight variation. In other conditions, the converter will be acting as a conventional boost or buck converter.

The switching patterns of this converter are presented in Table II. In each operation mode, there are two PWM switches. The complementary PWM switch is equal to the diode in the conventional boost or buck converter, but to decrease the converter loss resulting from the forward voltage drop of the MOSFET body diode, the MOSFETs are turned on in these periods. Same as in the previous converter, all the components are selected based on case study power and voltage levels, and the component's data are imported to PSIM thermal module. Components values and types are shown in Table III.

III. Key Performance Indicators

A. Components Stress Factor (CFS)

Derivation of CSF is based on the component load factor [14]which is a numerical method considering the device voltage and current stresses. The results are normalized by dividing them by the nominal processed power to obtain a unitless value. A weight factor may also be defined for different components to consider their importance when comparing and selecting an ideal converter for a specific application. In this case study, these weight factors are equal to one for all the components. To simplify the calculations process, two assumptions must be adopted. Firstly, all the inductors are large enough to have an almost ripple-free current. Secondly, the converter loss is almost zero and efficiency can be 100%.

After these assumptions, the stress factor could be defined for every element of the converter: semiconductors – SCSF, capacitors – CCSF, and windings – WCSF (including inductors and transformers) are formulated separately and derived. For the switches, the maximum voltage of the switch and RMS current can determine the stress factor and the normalization gives the final dimensionless value. The same approach is valid for the

TABLE I. S-PPC COMPONENTS AND PARAMETERS.

$S_{1.1}$ ... $S_{4.2}$	Vishay Siliconix SiR610DP
S_5, S_6	Cree C3M0280090D
C_1, C_2	Film capacitor *60μF*, *ESR=32mΩ*
C_{out}	Electrolytic capacitor *330μF*, *ESR=200mΩ*
C_{s1}, C_{s2}	Ceramic capacitor *3nF*
L	KEMET HHBC24N-2R3A0104V *104μH, ESR=10.4mΩ*
L_{eq}	Transformer leakage inductance, *4μH*
ESR_{bat}, *dc grid resistance*	*300mΩ, 100mΩ*

TABLE II. SWITCHING PATTERNS OF BBFPC IN ALL FOUR QUADRANTS.

Mode		S1	S2	S3	S4
Discharge	Boost	ON	C-PWM[2]	OFF	M-PWM[1]
	Buck	M-PWM	ON	C-PWM	OFF
Charge	Boost	C-PWM	ON	M-PWM	OFF
	Buck	ON	M-PWM	OFF	C-PWM

1. Main PWM switch

2. Complementary PWM switch (function of the diode in conventional buck/boost converter)

TABLE III. BBFPC COMPONENTS AND PARAMETERS.

S_1 ... S_4	Cree C3M0120090D
C_b, C_{dc}	KEMET ALF70(1)621EL600 *620μF*, *ESR=204mΩ*
L1	Hammond Manufacturing-195C20 *1mH, ESR=13mΩ*
L2	LCPI CTX20-10-52-R 21.17 *μH, ESR=7mΩ*
Battery ESR and dc microgrid resistance	*300mΩ, 100mΩ*

winding stress factors with the difference that the maximum average voltage on winding must be taken into account. Finally, for capacitors, the maximum voltage across capacitors and their RMS current should be the parameters of the stress factor.

$$SCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{max}^2 \cdot I_{rms}^2}{P_{process}^2} \quad (1)$$

$$WCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{max\_average}^2 \cdot I_{rms}^2}{P_{process}^2} \quad (2)$$

$$CCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{V_{max}^2 \cdot I_{rms}^2}{P_{process}^2} \quad (3)$$

$$V_{max\_average} = \sum_i D_i \cdot |V_i| \quad (4)$$

In (1) to (4), $\sum_j W_j$ is the sum of weights of the same components and W_i is the weight factor of *i-th* component. The simulations are carried out at different points for battery voltage (V_B=*320V*, V_B=*380V*) and different dc microgrid side power (3 kW, 2 kW, and 1 kW), considering both charging and discharging of the battery. Positive power specifies the discharge operation mode and negative power determines the charge mode. This study considers the dc grid of 350 V, typical for residential applications.

The total CSF combining the stress factor of all the mentioned elements is illustrated in Fig. 2. The stress factors for windings and capacitors are higher for BBFPC but the values are extremely small compared to SCSF in both converters. The switch stress factor of BBFPC is considerably higher than that in the S-PPC. Consequently, as observed in Fig. 2, the total CSF of BBFPC is higher for both battery voltage levels and all power levels. Hence, it could be concluded that the considered step-up/down S-PPC can provide much lower stress on semiconductor components, i.e., much fewer damage accumulation during the converter operation. Hence, better reliability could be expected but requires more analysis.

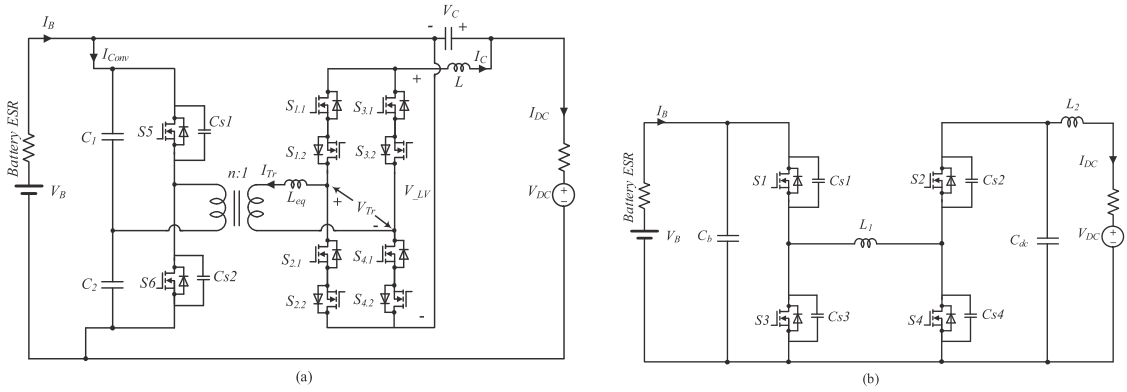
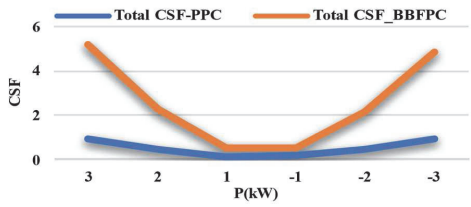
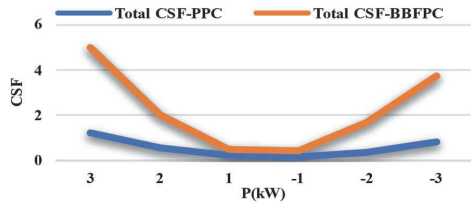


Fig. 1. Topology of CSFB S-PPC (a) and four-switch buck-boost converter (b)

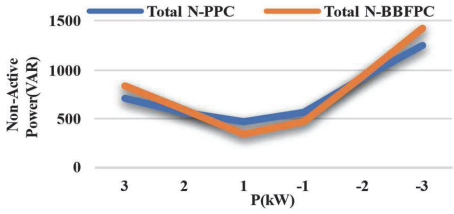


(a)

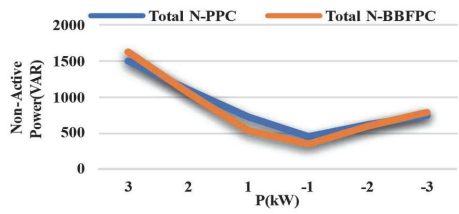


(b)

Fig. 2. Total CSF for (a) V_B = 320 V and (b) V_B = 380 V.



(a)



(b)

Fig. 3. Total non-active power for (a) V_B = 320 V and (b) V_B = 380 V.

B. Non-active power processing

In dc-dc converters, the voltage and current waveforms of all components include an average part plus an alternating periodic part that comes from switching devices in the converter. This alternating voltage and current are the sources of the power that oscillates in the components of the converter and is not delivered from source to load. The sources of this power are inductors and capacitors in the converter that absorb and release the energy in parts of switching periods. The IEEE 1459-2010 names this power as non-active power with the symbol of N to be different from reactive power in ac systems (Q). Similar to ac systems minimizing Q, decreasing non-active power is essential for reaching the least possible alternating power. It is of great importance due to the significant effect of the non-active power on converter power loss and, consequently, the efficiency.

In steady-state operation conditions of any converter, the charge balance in capacitors and volt-second balance in inductors are valid. It means that they do not consume any active power. If the total stored energy in a capacitor is E_{CT} and in an inductor is E_{LT}, the following equations can be written:

$$E_{CT} = \int_{t}^{t+T_S} v_C(t) i_C(t) dt = 0 \tag{5}$$

$$E_{LT} = \int_{t}^{t+T_S} v_L(t) i_L(t) dt = 0 \tag{6}$$

This means that the absorbed energy by these components in DT_S is equal to the released energy during $(1\text{-}D)T_S$, where T_S is the converter switching period and D is the duty cycle of the switches:

$$\Delta E_C = \int_{t}^{t+DT_S} \left| v_C(t) i_C(t) dt \right| = \int_{t+DT_S}^{t+T_S} \left| v_C(t) i_C(t) dt \right| \tag{7}$$

$$\Delta E_L = \int_{t}^{t+DT_S} \left| v_L(t) i_L(t) dt \right| = \int_{t+DT_S}^{t+T_S} \left| v_L(t) i_L(t) dt \right| \tag{8}$$

Considering (7) and (8), the non-active power in capacitors (N_C) and inductors (N_L) is calculated by the following equations.

$$N_C = \frac{2\Delta E_C}{T_S} \tag{9}$$

$$N_L = \frac{2\Delta E_L}{T_S} \tag{10}$$

The non-active power inside the converter can be derived by adding the non-active power of all capacitors and inductors:

$$N_{DC-DC} = \sum_{i=1}^{n} N_{L,i} + \sum_{j=1}^{m} N_{C,j} \,, \tag{11}$$

where n and m are the numbers of inductors and capacitors respectively. Finally, the non-active power of the input and output of the converter must be calculated and added to the internal non-active power to achieve the total value.

$$N_{in} = \sqrt{S_{in}^2 - P_{in}^2} \,, \; N_{out} = \sqrt{S_{out}^2 - P_{out}^2} \tag{12}$$

$$N_{tot} = N_{in} + N_{DC-DC} + N_{out} \quad (13)$$

In which S is defined by multiplying RMS voltage and RMS current in input and output. The non-active powers for the battery port, dc microgrid port, and inside both converters are obtained from PSIM simulations, and the total values are shown in Fig. 3. Based on the design requirement to equalize the current ripple in inductors and decrease the capacitors' voltage ripple, the final total non-active powers for both converters are close to each other at almost all points. If these assumptions are violated and the inductor and capacitor sizes are considered the same for the S-PPC and BBFPC, the BBFPC will experience considerably higher inductor current ripple and capacitor voltage ripple. The consequence of such an approach would be processing a significant amount of non-active power. The maximum energy that is stored in inductors equals 4.65 mJ and 48.02 mJ for S-PPC and BBFPC, respectively. A difference in the store energy by order of magnitude means a much different size of these inductors.

C. *Efficiency*

The S-PPC efficiency as discussed before in [2]depends on both the amount of processed power and the dc-dc topology efficiency which is used in S-PPC:

$$\eta_{sys} = 1 - K_{Pr} * (1 - \eta_{Conv}), \quad (14)$$

where the η_{sys} and η_{Conv} are the S-PPC and dc-dc stage efficiencies respectively, and K_{pr} is the partiality of the S-PPC converter. The dc-dc topology efficiency depends on various factors like soft-switching or hard switching, the amount of circulating non-active power inside it, and the ESR of components. It is worth mentioning that the CSFB converter utilized in the proposed S-PPC works fully in the soft-switching mode for a wide voltage and load variation range. Additionally, with the help of a modified phase shift modulation, the transformer current is pushed to zero during a controlled part of the shoot-through state to decrease the fluctuating power further and increase its efficiency. In experimental tests, the CSFB has reached 97.2% efficiency for the maximum power of 500 W.

On the other hand, BBFPC works completely in hard switching conditions and, due to bulkier components, the ESR of devices is higher in comparison with S-PPC, which increases the conduction losses. As mentioned before, the efficiency is estimated using PSIM thermal module for two battery voltage values: V_B = 320 V and V_B = 380 V. It can be seen from Fig. 4 that the S-PPC has higher efficiency in all operation points and the maximum difference is 0.7% for 3 kW (discharge) and V_B = 320 V.

IV. Discussion

To select the best candidate for the battery energy storage applications, all the mentioned KPIs must be calculated and considered. From the results of CSF, it is obvious that BBFPC devices (especially switches) are under much higher voltage and current stress. This is a noticeable drawback that can lead to faster component failures in the long-term usage of the converter. Moreover, the non-active power of both converters is almost close to each other. However, the problem of BBFPC is having approximately ten times higher energy stored in its inductor in comparison with S-PPC. It means that larger devices are needed which is a negative feature for a converter. Similarly, capacitors also store much less energy in the S-PPC.

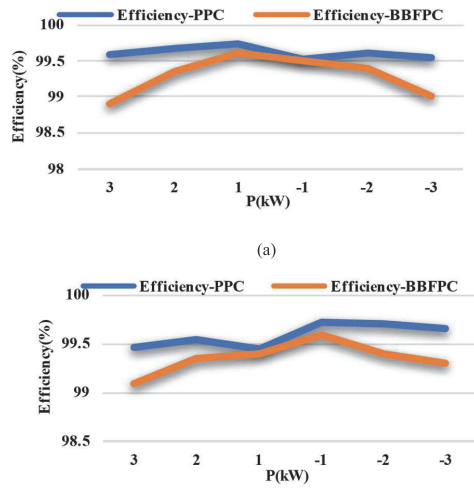


Fig. 4. The efficiency of both converters for (a) V_B=320V and (b) V_B=380V

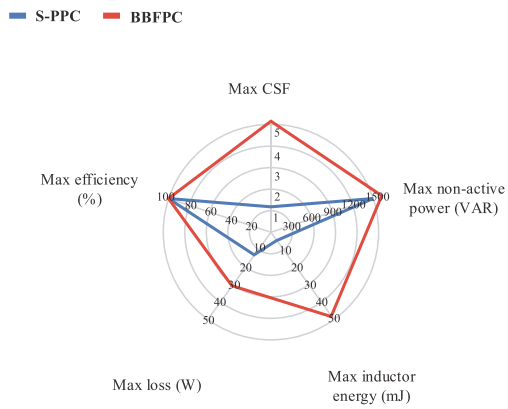


Fig. 5. Comparison of the maximum values of the key parameters in both converters

From the efficiency point of view, S-PPC gives higher efficiency in all power levels but the efficiency of BBFPC is also high and close to the S-PPC. These high efficiencies for the BBFPC are obtained by utilizing larger inductor and capacitors to decrease the voltage ripple on capacitors and current ripple on the inductor. Decreasing the size of these elements will result in

higher non-active power in BBFPC and lower efficiency. Fig. 5. Demonstrates maximum values for five parameters in both converters. It is visible that in terms of maximum CSF, maximum energy stored in the inductor, and maximum power loss the S-PPC is considerably advantageous.

V. Conclusions

In this paper, step-up/down S-PPC based on the current-source soft-switching dc-dc converter is compared with the conventional four-switch buck-boost dc-dc converter. Several KPIs are considered and the results for them are derived. A comparison of CSFs shows the superiority of the S-PPC which enables the implementation of low voltage/current rating devices. Experiencing lower stress also extends the lifetime of S-PPC in comparison with BBFPC, which could reduce the lifecycle cost of S-PPC. The non-active power is almost the same but the maximum energy stored in BBFPC inductor and capacitors results in its lower power density. Therefore, BBFPC can reach efficiencies almost as high as the S-PPC but it suffers from several drawbacks that are discussed in detail.

Acknowledgment

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Publication III

Hassanpour, N., Chub, A., Blinov, A., & Vinnikov, D. (2023). Soft-switching bidirectional step-up/down partial power converter with reduced components stress. IEEE Transactions on Power Electronics, 38(11), 14166-14177, doi: 10.1109/TPEL.2023.3289061.

Soft-Switching Bidirectional Step-Up/Down Partial Power Converter With Reduced Components Stress

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***Abstract*—This article introduces a step-up/down series partial power converter (S-PPC) based on isolated current-source dc–dc converter topology. The proposed S-PPC exploits the most important feature of the used current-source topology, such as the capability to operate with both voltage polarities in the series port to decrease its rated power. Other advantages include soft switching in the entire operating range and low current stress of semiconductor components even at very low series voltage. In addition, the proposed S-PPC provides protection and soft-start capabilities due to the integration of a solid-state circuit breaker. The article explains the operation principle of the proposed S-PPC and compares it to the closest known competing S-PPC based on the dual active bridge topology. An experimental prototype rated for 3.5 kW with maximum processed power of 600 W was built to confirm the converter operation principle and its features. Its experimental efficiency reaches 99.3%. The proposed S-PPC also shows a good regulation capability at challenging operating points, like nearly zero series voltage.**

***Index Terms*—Components stress factor, converter topology, dc–dc converter, partial power converter.**

I. Introduction

RECENT efforts of the power electronics community were targeting emerging applications associated with higher demand for direct current power distribution [1], [2], [3], [4], [5]. The current technology of full power converters is mature, and the performance of full power converters is limited by the technological barriers of semiconductor and magnetic components [6], [7]. To make a new step forward in the low-gain dc–dc converter, the partial power processing concept was adopted to limit the power processed by converter components and, consequently, reduce converter losses and volume. These converters are feasible and practical in applications where the input and output voltages are relatively close; the closer, the better the converter performance.

The partial power processing idea was conceptualized in the 1960s [8], but the new technology of series partial power converters (S-PPCs) saw its first application only thirty years later [9], [10]. These converters comprise a dc–dc conversion cell with one of its ports connected in series between the input and output ports of an S-PPC. Most of the literature on these converters was published in the last decade [11]. S-PPC dominates the literature among different partial power processing architectures [12]. Even though S-PPCs were used in different applications, relevant research favored their use in photovoltaic (PV) applications [13], [14]. However, S-PPCs that step-up PV string voltage to a dc link showed the best performance in photovoltaic applications [15].

Therefore, it is important to distinguish S-PPCs into three classes: step-up, -down, and -up/down [16]. The first two classes are straightforward and could be implemented with more advanced full-bridge topologies [15] as well as a simple flyback topology [17] that, however, has a limited scalability of power level. On the other side, step-up/down S-PPC converters require the series port to operate in two quadrants (positive and negative port voltage) with a unidirectional current. The two-switch forward converter is the simplest dc–dc converter topology used in such converters [18]. A step-up/down S-PPC is introduced in [19] based on a current source full-bridge converter with two-quadrant switches at the low-voltage port. The hard switch operation of the switches and voltage drop of the series switches are the main sources of the total converter loss, which cannot be neglected.

Moreover, the impact of leakage inductance on the voltage spikes is not investigated. The step-up/down S-PPC in [20] is also formed by two quadrant switch that suffers from hard switching problem and extremely high processed power in the low battery voltages that cancels the advantage of the PPC concept. Further development of this concept to bidirectional operation requires the utilization of more advanced dc–dc converter topologies capable of handling any combination of series port voltage polarities and current directions between S-PPC ports. The initial concept of bidirectional step-up/down S-PPC based on the four quadrant switches was presented in [21]. However, it did not discuss modulation strategy and operation principle in detail. It could be assumed that it was operating with hard switching, i.e., high switching losses.

Currently, there are a few examples of the voltage-source dual active bridge (DAB) converter used together with a voltage unfolder to achieve these properties [22]. However, their operation in critical points when S-PPC has to operate with low series voltage and full load current has not been demonstrated in

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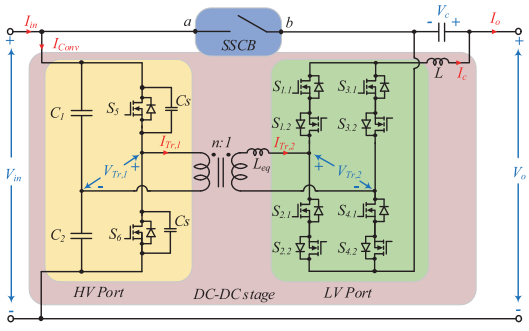

Fig. 1. Proposed bidirectional step-up/down (BDSUD) series partial power converter (S-PPC).

literature due to excessive current stress, which will be quantified in this article.

To overcome the limited voltage regulation and soft-switching properties of the existing solutions, this article proposes to use an advanced isolated current-source full-bridge dc–dc converter topology in the step-up/down S-PPCs. This topology shows superior voltage regulation capabilities and soft switching attainable in the entire converter operation range. The first version of this work was published in [23], where the main concept and some of the functions were demonstrated using simulations. This article presents the next step in developing the proposed S-PPC topology by implementing soft-start, demonstrating the feasibility of operation around zero partiality, developing design guidelines for wide-range soft-switching and confirming it, and comparing the given concept to the closest counterpart from the recent literature. Section II describes the operation principle of the proposed S-PPC and shows the limitations of its nearest competitor from [22]. Section III explains the design guidelines of the novel concept, which is followed by the experimental performance benchmarking, which is discussed in Section IV. Finally, Section V concludes this article.

II. Proposed S-PPC

This section proposes a novel bidirectional step-up/down (BDSUD) S-PPC based on an isolated current source full-bridge (CSFB) dc–dc converter. The configuration of the S-PPC is input-parallel-output-series (IPOS), which generally leads to less processed power regarding both step-up and step-down modes. In S-PPCs, a wide voltage regulation range capability is required at a low voltage (LV) port. The voltage across this port of the dc–dc stage ranges from zero (in the case of equal input/output voltage) to the maximum voltage regulation range for the desired application. Amongst various current source (CS) topologies, the current-source full-bridge features negligible energy circulation, which is highly favorable for both high/low voltage and power levels and improves the performance of the S-PPC. Fig. 1 introduces the proposed converter, including its main parts.

The first one is the high voltage (HV) port, which is connected in parallel to the input side. Thus, all elements in this port (C_1, C_2, S_5, S_6, and the snubber capacitors C_s) will be selected in accordance with the input voltage rating with the full voltage stress. Employing a half-bridge voltage doubler (HB/VDR) structure in the HV port is preferable due to less active components in comparison with a full-bridge structure [19]. In the S-PPC configuration, the parallel connected HV port features reduced current flow, which reduces the component current rating requirements.

A full-bridge matrix stage forms the LV port with an inductor at its output. The prominent feature of such a configuration is its capability to provide bipolar series voltage (Vc) as well as bidirectional current (Ic). This feature is eminent specifically in battery energy storage applications or dc microgrid power flow controllers, where bidirectional operation is required. The switching devices in this port experience rated current and partial voltage stresses.

A. Modulation Strategy and Operation Modes

Isolated current source converters typically include an auxiliary circuit like a snubber or clamp circuit to suppress the voltage spike across the semiconductors in the CS port generated by the leakage inductance of the transformer. Applying such strategies to eliminate voltage spikes will increase the converter hardware and control complexity as well as its cost. Instead, the clamping of voltage can be attained by an active rectifier at the voltage source (VS) port to redistribute the current in the CS port switches, effectively creating a secondary modulated converter (SMC).

Since the proposed S-PPC assumes energy exchange in both directions, the presence of active semiconductors in both ports is well justified. Both the phase shift modulation (PSM) and the symmetric pulsewidth modulation (PWM) can be implemented for regulation. The disadvantage of PWM-SMC is that it requires RC snubbers for the LV port switches to suppress the voltage spikes. Moreover, its voltage regulation range is limited. The PSM reduces energy circulation between two ports of the dc–dc stage but requires reverse blocking switches at the LV port [24]. The PSM is highly preferred to maintain high efficiency in all operating points, including zero-series port voltage. Again, the use of bidirectional switches is justified in the proposed S-PPC due to the bipolar voltage blocking capability requirement. Fig. 2 depicts the modulation and generalized current/voltage waveforms for the boost and buck modes of the CSFB converter utilized in the proposed S-PPC [24]. It must be stated that the terms buck/boost will be used for the dc–dc stage and the step-up/down for the whole S-PPC. The soft switching of this converter is guaranteed by introducing an additional short resonance period during the shoot-through state to ensure fast recharging of snubber capacitors C_S at the HV port and minimizing the energy circulating between the dc–dc cell ports. It occurs during the time interval (t_4-t_5) in the boost mode and (t_1-t_2) in the buck mode. Soft switching at the HV and LV ports is load-independent within the required operating range and does not need any further control, which will be investigated in detail in the following section.

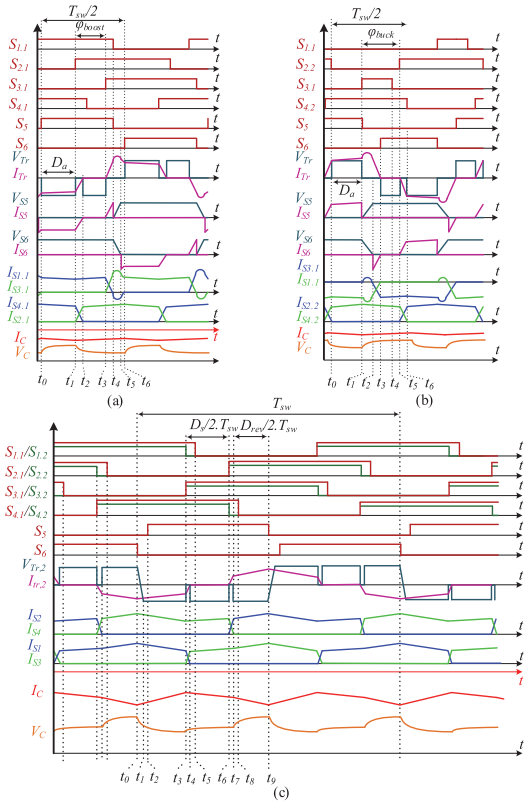

Fig. 2. Operation waveforms of the dc–dc stage in (a) boost mode (power transfer from LV to HV port) and (b) buck mode (power transfer from HV to LV port) (c) reverse power flow modulation.

The four-quadrant operation [see Fig. 3(c)] of the proposed S-PPC could be elaborated as follows.

Quadrant-I ($V_c > 0$ & $I_c > 0$): In this quadrant, the dc–dc stage operates as a buck converter, transferring power from the HV to the LV port, which is in the same direction as the power flow of the system. This mode is depicted in Fig. 3(a). The $S_{1.2}$ and $S_{3.2}$ are turned ON, and $S_{2.1}$ and $S_{4.1}$ are turned OFF or performing synchronous rectification. $S_{1.1}$ and $S_{3.1}$ work with a constant phase shift related to S_5 and S_6 to allow the resonance period for zero voltage switching (ZVS) of HV port switches and current redistribution for zero current switching (ZCS) of LV port top switches. The Quadrant-III ($V_c < 0$ and $I_c < 0$) is analogous to Quadrant-I if the switching patterns of the top and bottom side switches in the LV port are swapped accordingly.

Quadrant-IV ($V_c > 0$ & $I_c < 0$): In this quadrant, the dc–dc stage works as a boost converter, transferring power from its LV to the HV port in the same direction as the S-PPC power flow. It is demonstrated in Fig. 3(b). Both $S_{1.2}$ and $S_{3.2}$ are turned ON and $S_{2.2}$ and $S_{4.2}$ are turned OFF or performing synchronous rectification. A constant phase shift between the HV port switches and the top switches of the LV port allows the completion of the resonance period, which satisfies the ZVS switching of the HV port switches. Quadrant II ($V_c < 0$ & $I_c > 0$) is identical to Quadrant-IV if the switching patterns of the top and bottom side switches at the LV port are swapped to generate the negative voltage polarity. In all quadrants, the phase shift between the top and bottom switches of the LV port (φ_{buck} and φ_{boost}) regulates the LV port voltage and current (V_c and I_c).

During the buck mode of the dc–dc stage, the voltage gain is regulated by changing the shoot-through state duration between the top and bottom switches of the LV port. According to [24] the voltage gain can be determined by the following equation:

$$G_{\text{buck}} = \frac{\pi - \left(\varphi^{\text{buck}} + \omega \cdot t_{\text{red}}\right)}{2 \cdot \pi \cdot n} \tag{1}$$

in which G_{buck} is the voltage gain of the buck mode, φ^{buck} is the phase shift between the top and bottom switches of the LV port, $\omega = 2\pi f_{sw}$, t_{red} ($t_2 - t_3$) is the current redistribution time between LV port switches (for example, $S_{2.2}$ and $S_{4.2}$) that will be elaborated in the next sections, and n is the transformer turns ratio. Increasing the phase shift in a way that $\varphi^{\text{buck}} + \omega.t_{\text{red}} = \pi$ will minimize the active state duration and will push the V_c to zero. Therefore, the S-PPC operation near zero series capacitor voltage can be guaranteed.

On the other hand, the PSM modulation Fig. 2(a) is unable to control the boost operation of the dc–dc stage when $|V_c| \leq 10V$. To overcome this issue, a new modulation based on reverse power flow control is presented to smoothly control the S-PPC in the boost mode of the dc–dc stage near zero series capacitor voltage. The modulation strategy is depicted in Fig. 2(c). As can be seen, the reverse power transfer from the HV port to the LV port during the time interval of ($t_8 - t_9$) charges the LV port inductor and extends the boot factor of the dc–dc stage. The voltage gain in this mode can be written as

$$G_{\text{boost}} = \frac{2 \cdot n}{1 - D_s - 2 \cdot D_{rev}} \tag{2}$$

where D_s is the switching interval of the shoot-through state and D_{rev} corresponds to the duration of reverse power flow mode. It can be seen from (2) that the voltage gain is more sensitive to D_{rev} than D_s for this modulation strategy. A detailed explanation of modulation and operation modes can be found in [25] and [26]. In practice, both D_s and D_{rev} could be used to adjust the voltage in the series port near zero. The utilization of the reverse power flow mode is associated with higher conduction losses [25]. Therefore, it is used only in a narrow input voltage range near zero partiality (± 10 V in comparison to the full voltage regulation range of ± 50 V). Hence, the effect of reverse power flow on the weighted system efficiency is negligible.

B. Comparison of the BDSUD and DAB-Based S-PPC by the Number of Components

The closest alternative of the proposed converter in the class of BDSUD S-PPCs is the S-PPC based on DAB dc–dc converter and an unfolding circuit in the series port [22]. It is demonstrated in Fig. 4.

Table I compares these two approaches in terms of components count. As mentioned earlier, the number of switches

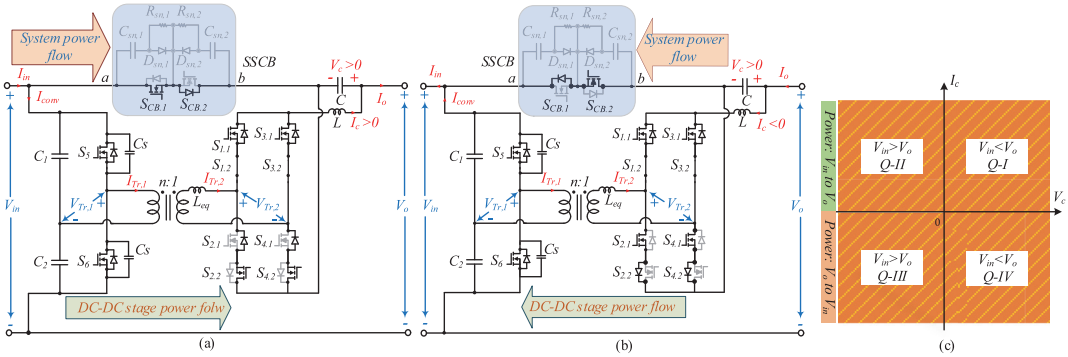

Fig. 3. Operation modes of the proposed S-PPC (a) step-up/forward current (Q-I) and (b) step-up/backward current (Q-IV) (c) operation quadrants.

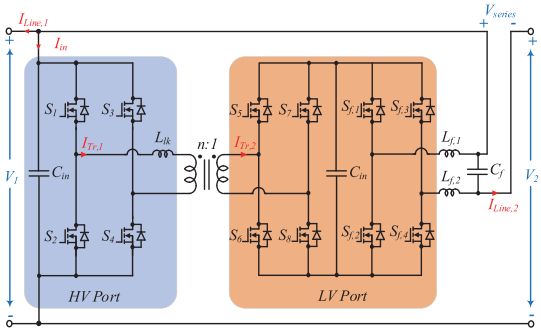

Fig. 4. DAB-based step-up/down bidirectional S-PPC proposed in [22].

TABLE I
COMPARISON OF THE PROPOSED AND DAB-BASED S-PPC FROM [22]

Component	Proposed BDSUD	DAB based S-PPC [22]
LV port switches	8	8
HV port switches	2	4
Inductors	1	2
Transformers	1	1
Transformer turns ratio	$n_{min} > \frac{V_{in,min}}{2D_{a,max}.V_{C,max}.}$	$n_{min} > \frac{V_{in,min}}{V_{C,max}.}$
Capacitors	5	3
Gate driver channels	10	12
Gate Power supplies	6	8
Current sensors	1	1
Voltage sensors	3	3

is lower in the proposed converter due to the application of a half-bridge circuit. Moreover, the transformer turns ratio is reduced at least by a factor of 2, considering the same voltage conversion ratio.

The transformer with lower turns ratio is preferable because of the design simplicity and easily achievable low leakage inductance, which is important for the CSFB converters.

Regarding the energy storage elements, the number of inductors in [22] is double that in the proposed BDSUD. On the other hand, the number of capacitors is higher in the proposed converter. However, two of them are small nF-scale ceramic snubber capacitors, much smaller than mF-scale capacitors used in the DAB-based S-PPC.

Another point to consider is that each of the bidirectional switches in the LV port is driven by a single auxiliary dc–dc power supply and one dual-channel gate driver. Accordingly, the driving circuitry is simpler and cheaper as competing solutions require more components. In contrast with [22], the dc-link capacitor at the LV port is eliminated, resulting in higher power density. An additional advantage of eliminating the dc-link capacitor is that in case of any short circuit fault in the LV port, having a dc-link capacitor will lead to a large inrush current through LV port devices, which might require extremely fast protection devices and strategies [27].

C. Soft-Switching Region of BDSUD and DAB-Based S-PPCs

As mentioned earlier, the proposed converter operates with soft switching within its defined voltage and power range. On the other hand, the DAB converter, which is widely exploited in the literature for step-up/down S-PPCs [22], [27] suffers from excessive power circulation between its high and low voltage ports. This limits the ZVS range of the converter, especially when the voltage across the LV port decreases to almost zero. To overcome this drawback, different modulation strategies could be used in the DAB-based S-PPCs.

The single PSM (SPSM) has the highest circulated power. Hence, dual-PSM (DPSM) could be used to reduce the power circulation and widen the ZVS range of the converter. Although DPSM reduces the high-power circulation in the converter power range compared to the SPSM, it cannot eliminate the power circulation, especially at small phase shifts where the converter works in light load conditions. The soft-switching range of the DAB converter is illustrated in Fig. 5. The voltage gain is normalized by the transformer voltage conversion ratio n for DAB and $2{\cdot}n$ for the isolated CSFB converter, considering the utilization of the half-bridge circuit in the HV port. The red line depicts the ZVS boundary of the DAB converter. Below the line, it loses the soft-switching operation in the LV port.

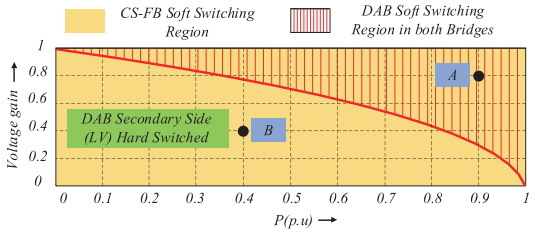

Fig. 5. Soft-switching range of the proposed BDSUD and the DAB-based S-PPC versus voltage gain and normalized output power.

The only parameter that affects this soft-switching border is the leakage inductance of the transformer. Increasing the leakage will widen the soft-switching region of the DAB-based S-PPC. However, the power transfer capacity between the two ports will be decreased by increasing the leakage inductance. A tradeoff between these two issues must be considered when designing an S-PPC based on the DAB converter. On the other hand, the BDSUD is based on a current-source converter. Its soft-switching region covers the whole operation range by considering duty cycle values for the HV and the LV port, the transformer leakage inductance, and the snubber capacitors in the HV port. The soft-switching design criteria will be discussed in Section III.

D. Component Stress Factor (CSF) Comparison

To compare the proposed S-PPC in terms of voltage and current stresses of components, the component stress factor (CSF) is calculated. It is based on the component load factor (CLF), which is a numerical method considering the root mean square (rms) current and the maximum voltage of the devices. The results are normalized to the nominal power of the converter to have a dimensionless parameter for better comparison. In order to simplify CSF calculations, two main assumptions are considered. All the converter elements are assumed to be lossless, and the inductor current is ripple free. For each type of converter element, CSF will be calculated independently. Therefore, there will be three categories of devices that have different CSF calculations. For the switching devices (active and passive), the semiconductor CSF (SCSF) is the maximum blocking voltage multiplied by the rms current of the device. The capacitor CSF (CCSF) is also derived by the multiplication of maximum voltage to the rms current. Regarding magnetic components of a converter, winding CSF (WCSF) is determined by the maximum average voltage across a component winding multiplied by its rms current. The mentioned parameters are estimated by the following equations:

$$\mathrm{SCSF}_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{\max}^2 \cdot I_{\mathrm{rms}}^2}{P_{\mathrm{rated}}^2} \tag{3}$$

$$\mathrm{CCSF}_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{\max}^2 \cdot I_{\mathrm{rms}}^2}{P_{\mathrm{rated}}^2} \tag{4}$$

$$\mathrm{WCSF}_i = \frac{\sum_j W_j}{W_j} \cdot \frac{V_{\max\_avg}^2 \cdot I_{\mathrm{rms}}^2}{P_{\mathrm{rated}}^2} \tag{5}$$

$$V_{\max\_avg} = \sum_i D_i \cdot |V_i| \tag{6}$$

where P_{rated} is the nominal power of the converter. The term $\sum_j W_j/W_j$ is the weight factor related to the resource distribution in the different components, which is assumed one for simpler calculation. The $V_{\max\_avg}$ is the maximum average voltage on the windings of magnetic devices. For both the proposed converter and the reference converter [22] the same input/output voltage and nominal power are defined to obtain a tangible comparison. The input voltage is 350 V, and the output voltage varies from 350.5 V, i.e., the relative amount of processed power regarding the total power (K_{pr}) of 0.1%, to 400 V ($K_{pr} = 12.5\%$). The nominal power is 3.5 kW, resulting from the nominal output voltage of 350 V and rated output current of 10 A. The impact of the solid-state circuit breaker (SSCB) on the CSF is neglected in both converters as it conducts 10 A dc with the same voltage drop across the SSCB. The results from (3) to (5) are portrayed in Fig. 6 in normalized units.

It can be observed that at the low voltage in the series port, the DAB-based S-PPC has considerably higher CSFs due to significant circulating power. To operate near zero voltage at the series port with single PSM, the DAB-based S-PPC needs to be overdesigned to withstand high current stress. At the higher voltage levels, the rms current of the transformer and the reactive power decreases, and the SCSF of DAB becomes lower than the proposed converter (at $K_{pr} = 5.4\% \ldots 10.7\%$). But this range is limited, and the SCSF increases at partiality coefficients above 12.5%. The CCSF and WCSF of the DAB-based S-PPC present similar behavior as the SCSF, but these parameters are always higher than the values of the CSFB.

On the other hand, the CSF values of the CSFB-based S-PPC are strongly correlated only with the amount of active power processed by the dc–dc cell. It can be seen from Fig. 6 that the CSF of all of the components is minimum at near zero partiality coefficient, and the CSFs increase slightly up to their maximum value at $K_{pr} = 12.5\%$. A similar comparison was also performed in [28] to investigate the feasibility of the DAB and CSFB converters configured as S-PPC. It also concludes that due to the high CSF values compared to the CSFB, the DAB topology does not always provide high performance in BDSUD S-PPCs.

E. SSCB Structure and Function

Considering the recent S-PPCs in the literature, in almost all of the studied converters, the start-up transients and the strategy for the precharging series capacitor are neglected [14]. One of the key roles of the SSCB is to help the converter to start safely and prevent any inrush current of the initially charged series capacitor. The structure of SSCB is demonstrated in Fig. 3, while its design constraints are elaborated in [29]. It includes two back-to-back connected MOSFETs and a snubber circuit to protect switches from overvoltage. In terms of voltage and current, the SSCB elements are selected for the full voltage and current of the S-PPC. In all four quadrant operation modes of the converter, the SSCB is initially turned off. After the converter starts up, the

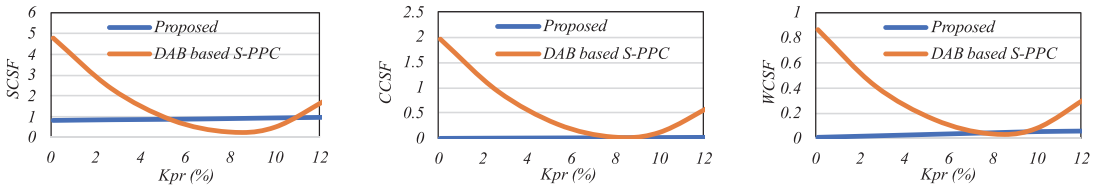

Fig. 6. CSF for both the proposed and DAB based [22] S-PPCs as a function of partiality coefficient (K_{pr}) (a) SCSF, (b) CCSF, (c) WCSF.

series capacitor is charged up to the voltage difference between the two dc sources (V_{in}-V_o). It must be noted that the charging operation is performed by one of the dc–dc stage buck operation modes according to the required voltage polarity of the series capacitor ($V_c > 0$ or $V_c < 0$). As soon as the capacitor voltage reaches the voltage difference ($V_c = V_{in} - V_o$), the SSCB turns ON and links the series path between input and output. By doing so, a high *dv/dt* is eliminated at the start-up, and the series capacitor charging will cause no inrush current. From this moment on, based on the sign of the reference current and the amplitude of the input/output voltage, one of the operation quadrants will be chosen, and the converter will start to work normally. Hence, the safe operation of the LV port could be ensured.

III. Design Guidelines

The most crucial factor in any S-PPC is the amount of active power processed by the dc–dc stage of the converter, which impacts the system efficiency. Hence, the first part of this section discusses the partiality of the proposed converter. It is followed by an analysis of how soft-switching requirements should be considered in the converter design. The guidelines for selecting passive and magnetic components are given in the last two sections.

A. Rated Power Selection

The amount of power processed by the S-PPCs is directly related to the voltage difference between both sides of the converter. In IPOS configuration, the voltage and current equations of the system can be written as follows:

$$V_o = V_{in} + V_c \tag{7}$$

$$I_{in} = I_o + I_{conv}. \tag{8}$$

It can be seen from Fig. 1 that $I_o = I_c$. The bipolar output voltage feature of the CSFB at its LV port allows us to quickly implement the step-up/down S-PPC based on (7). Therefore, the partiality coefficient, which is the ratio of processed power to the total power, can be defined as

$$K_{pr} = \frac{P_{Cout}}{P_{\text{out}}} = \frac{V_c \cdot I_c}{V_o \cdot I_c} = \frac{V_o - V_{in}}{V_o} = 1 - \frac{V_{in}}{V_o} \tag{9}$$

where K_{pr} is the S-PPC partiality coefficient. Considering constant input voltage (V_{in}) and variable output voltage (V_o), the variation of K_{pr} is illustrated in Fig. 7. Based on the application

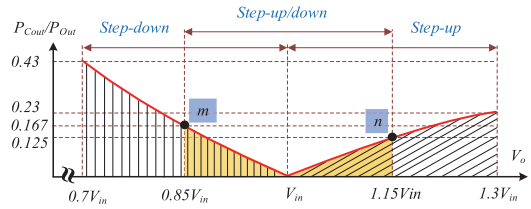

Fig. 7. Partiality of the S-PPC with constant V_{in} and variable V_o.

TABLE II
Case Study System Parameters

Parameter	Symbol	Value
Input voltage	V_{in}	350 V
Output voltage	V_o	350 V (± 50V)
Rated power	P_{reated}	3.5 kW
Dc-dc stage rated power	$P_{Conv\text{-}rated}$	600 W
Switching frequency	f_{SW}	50 kHz

requirements, both input and output voltages can change in a defined range. This voltage variation defines the voltage regulation range (ΔV_c).

The voltage regulation range is the only parameter that determines the amount of the processed power by the dc–dc stage and must be carefully chosen for every application. The advantage of the presented CSFB is that the ΔV_c can vary from a minimum negative voltage ($V_{c,\min}$) to zero and finally to the maximum positive voltage ($V_{c,\max}$). The limits are constrained by the transformer turn ratio (n) and the parallel port voltage.

The superiority of step-up/down S-PPCs over step-up or step-down SPPCs is distinctly evident in Fig. 7 regarding the maximum power processed by the dc–dc stage. These figures are drawn for the maximum 30 percent voltage regulation range for the input or output port ($\Delta V_c = V_{c,\max} - V_{c,\min}$). With a maximum ΔV_c of 50 V, the partiality is limited to 17%, based on the case study parameters in Table II. Points m and n in Fig. 7 depict the operating boundaries for the designed S-PPC. Considering η_c as the dc–dc stage efficiency, the system efficiency can also be calculated according to the following equation:

$$\eta_{sys} = 1 - K_{pr} \cdot (1 - \eta_c). \tag{10}$$

In this equation, η_{sys} stands for S-PPC efficiency. From (10), it can be perceived that the S-PPC efficiency is affiliated with both the partiality coefficient and the dc–dc stage efficiency. This is the phase in which improving the dc–dc stage efficiency could slightly improve the overall S-PPC efficiency. The partiality coefficient depends on the voltage regulation range, which is not entirely under control in every application.

For example, in PV systems defining the number of series connected PV modules determines the nominal output voltage of the PV string. The PV string output voltage, in most cases, varies within thirty percent variation from its nominal voltage [14]. On the other hand, in battery applications, the battery cell voltages at the state of charge (SoC) of 20% and 80% specify the voltage regulation range, which is typically wider than in PV systems [30]. The other parameter that is affected by the power electronics design is the dc–dc stage efficiency. Therefore, various sources of power loss ought to be carefully analyzed and designed to maximize the η_{sys}.

B. Soft-Switching Criteria

For the CSFB, the maximum output current at the LV port determines the soft-switching operation of LV port switches. The maximum output current is defined to fulfill the application of the S-PPC, which for instance, in battery energy storage applications, is the maximum permissible charge/discharge current. Considering $I_{c,\max} = I_{o,\max}$, the duty cycle (D_{lv}) of the LV port switches ($S_{1.1} \ldots S_{4.2}$) can be calculated as follows:

$$D_{lv} \geq 0.5 + \frac{2 \cdot n \cdot I_{c,\max} \cdot L_{eq} \cdot f_{sw}}{V_{in}}. \tag{11}$$

The duration of overlapping of the switches must be chosen to permit full ZCS for the switches to prevent any voltage spike across them caused by the current mismatch. It is understandable that above the maximum output current, the ZCS criterion of the converter will be violated. Therefore, in applications where the maximum output current is not a constant value, the adaptive regulation of the overlap time is recommended. With the parameters of the designed converter, $D_{lv} = 0.51$ is enough to ensure full soft-switching operation under the maximum output current of 10 A. The current redistribution time for LV port switches could be written as

$$t_{\text{red}} = \frac{2 \cdot n \cdot I_c \cdot L_{eq}}{V_{in}}. \tag{12}$$

From Fig. 2(a) and considering (12), the minimum phase shift in the boost mode must be high enough to allow for complete current redistribution between the switches

$$\varphi_{\min}^{\text{boost}} = \omega \cdot t_{\text{red}} \tag{13}$$

where $\omega = 2\pi f_{sw}$. The resonance time can be estimated by the following equation:

$$t_{res} = \frac{\frac{\pi}{2} - arctg\left(\frac{2 \cdot n \cdot I_c \cdot Z_r}{V_{in}}\right)}{\pi \cdot f_r}, \tag{14}$$

in which $Z_r = \sqrt{L_{eq}/C_{eq}}$, and $f_r = 1/\left(2 \cdot \pi \cdot \sqrt{L_{eq}/C_{eq}}\right)$ $C_{eq} = C_S \cdot n^2/2$. The longest resonance time occurs at no load conditions, which is the critical point for the selection of C_S. The unique feature of CSFB with asymmetric SMC modulation allows the C_{eq} to recharge by the resonant current (whose peak is equal to or higher than $I_{c,\max}$) regardless of the output current and operation point of the dc–dc stage. Consequently, the capacitor charge is load-independent and satisfies the complete soft switching in the operation range of the converter regardless of I_c value. As can be seen from Fig. 2(b), the resonance state during the buck mode of the dc–dc stage starts when one of the LV port switches turns ON and one of the HV port switches turns OFF. The duration of this time interval in the buck mode is load-independent and depends on only L_{eq} and C_s values. On the other hand, when the dc–dc stage operates in the boost mode, the resonance period starts right after finishing the current redistribution time (t_{red}). Consequently, the variation of the load current will change the t_{red} and resonance period start point as well as its duration. This dependency of resonance period in the boost mode appears as arctg term in (14).

There must also be a constant time interval between both port switches to allow for ZVS of the HV port switches. From Fig. 2, one can observe that this time interval is the accumulation of resonance time and current redistribution time in the buck mode. Hence, with the longest resonance time occurring in $I_c = 0$, the maximum duty cycle of HV port switches D_{hv} can be derived as

$$D_{hv} \leq 0.5\left(1 - \frac{f_{sw}}{f_r}\right). \tag{15}$$

Real prototype parameters require 2.8% dead time at the control of the HV port switches to allow resonance and current redistribution periods. Thus, $D_{hv} = 0.47$ is applied to the S_5 and S_6. The minimum phase shift in the buck mode is also the sum of both t_{red} and t_{res}

$$\varphi_{\min}^{\text{buck}} = \omega \cdot (t_{\text{red}} + t_{res}). \tag{16}$$

The minimum phase shift in buck mode is the basis for choosing the C_{eq} and L_{eq} due to more duty cycle loss in this mode. Fulfilling (11), (13), (15), and (16) guarantee the full soft switching of the CSFB within its operating range.

C. Design of Passive Components

The capacitors ($C_1 = C_2 = C_{\text{in}}$) and inductor ($L$) are selected regarding allowed voltage and current ripples at the HV and LV ports, respectively. The current ripple of the inductor can be determined as

$$\Delta i_L = \frac{V_c \cdot (1 - D_a)}{4 \cdot L \cdot f_{sw}} \tag{17}$$

where the D_a is the active power transfer duration, which is shown in Fig. 2 for both the buck and boost operation of the dc–dc stage.

Regarding the HV port capacitors, the voltage ripple across them can be estimated by

$$\Delta V_{\text{HV}} = \frac{P \cdot (1 - D_a)}{2 \cdot C_{in} \cdot V_{in} \cdot f_{sw}} \tag{18}$$

where the ΔV_{HV} is the voltage ripple across the HV port of the converter.

D. Transformer Design

The isolation transformer is undoubtedly one of the most critical components of the dc–dc stage in every S-PPC, as it denotes the voltage regulation range between input and output. In the selected CSFB dc–dc converter, a careful design of the transformer is one of the crucial design steps. Minimizing the leakage inductance reduces the resonance time (t_{res}) and the duty cycle loss, leading to reduced component stresses. In addition, the power circulation during the resonance period within LV port switches can be minimized. It is of significant importance due to the flow of high current through four series switches in every resonance period that could add to the conduction loss. The lowest HV port voltage specifies the minimum dedicated turns ratio, so

$$n_{\min} \geq \frac{V_{in,\min}}{2 \cdot D_{a,\max} \cdot V_{c,\max}} \tag{19}$$

$$V_{c,\max} = V_{in,\min} - V_{o,\max}. \tag{20}$$

In (19), the maximum absolute value is to be calculated since (20) would yield a negative value. The $D_{a,\,\max}$ is limited by the t_{res}, $t_{\mathrm{red},}$ and the voltage drop in components of the converter. It is different for the buck and boost operation modes, but the worst case, the boost mode, must be considered as the design basis. In the final design $D_{a,\,\max} = 0.9$ is considered to include all the mentioned duty cycle losses. The maximum flux density for the square-wave transformer is the result of the expression as follows:

$$B_{\max} = \frac{V_{in,\max}}{4 \cdot n_1 \cdot f_{sw} \cdot A_e} \tag{21}$$

where n_1 is the number of HV side turns and A_e is the effective cross section of the transformer core. Due to the application of a half-bridge circuit at the HV port, the transformer turns ratio is half for the same voltage values compared to the full-bride structure. From the transformer point of view, the result is a smaller and cheaper transformer with low leakage inductance.

IV. Experimental Results and Discussion

To confirm the theoretical analysis and prove the mentioned claims, a prototype with a rated power of 3.5 kW is assembled (see Fig. 8). Two iTECH IT6000C bidirectional dc power supplies are connected to the S-PPC ports. They can apply a defined function of voltage/current to both ports. The control system is based on an STM32G474 Cortex M4 microcontroller. The whole system is connected to the Yokogawa WT1800 high-performance power analyzer was used to measure the efficiency of the converter. Table III lists the real parameter values and component types in the tested converter.

To verify the soft-switching operation, two points are selected in Fig. 5. Point (A) represents 0.9 p.u. of output power and 0.8 normalized voltage gain. As can be seen from Fig. 9, the HV port switches turn ON in ZVS condition, which is clear in Fig. 9(a). In the turn-OFF process [see Fig. 9(b)], the switching loss is reduced by limiting *dv/dt* using snubber capacitors.

Moreover, Fig. 9(c) depicts the switching waveforms of the LV port switches in which $S_{3.1}$ turns OFF by natural commutation

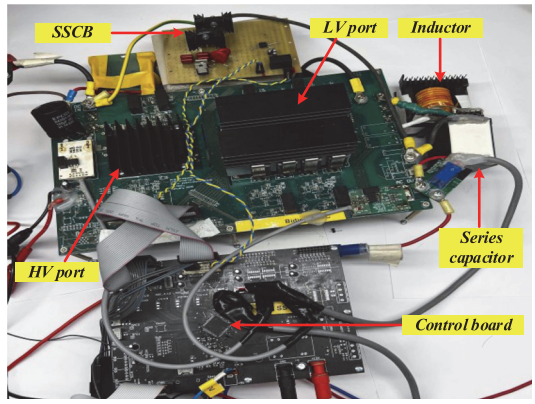

Fig. 8. Proposed BDSUD experimental prototype.

TABLE III
Components and Parameters of the Experimental Prototype

Component/Parameter	Symbol	Value/Type
LV port switches	$S_{1.1}$-$S_{4.2}$	C3M0120090D
HV port switches	S_5, S_6	C3M0120090J
LV port inductor	L	100μH
Inductor core	-	ETD54/28/19/3C97
Transformer leakage inductance	L_{eq}	850nH
Transformer turns ratio	n	2.3:1
Transformer core	-	ETD54/28/19/3C97
HV port capacitors	C_1=C_2	60μF
Series capacitor	C	100μF
HV port snubber capacitors	C_s	1.1nF
Isolated gate drivers	-	UCC21520-Q1

of the body diode during the synchronous rectification period. The $S_{4.2}$ also turns OFF totally in ZCS condition. The current redistribution between LV port switches happens successfully during their turn-ON/OFF period. The same measurements in point (B) from Fig. 5 are given in Fig. 10 to prove the soft-switching operation at low power and low series port voltages.

The turn-ON process of switches $S_{3.1}$ and $S_{4.2}$ are shown in Fig. 11. To clearly distinguish each figure, the turn-ON points in Figs. 9(c) and 10(c) are marked with the numbers from 1 to 4 depicting the turn-ON of $S_{3.1}$ and $S_{4.2}$ in high and low powers respectively. During the turn-ON time of the LV port switches, both for top and bottom switches, they become in series with the leakage inductance of the transformer. Due to this reason, the *di/dt* is limited by the leakage inductance. The current of the switch $S_{3.1}$ starts from zero and enters resonance mode. During this time interval, the peak resonance current is limited to less than 2 A, which is evident from Fig. 11(a) and (c). The current rise during the turn-ON process is even lower than this number (around 1A). The current of the switch $S_{4.2}$ starts to increase from zero to the maximum value because of the current redistribution from the switch $S_{2.2}$. As can be seen from Fig. 11(b) and (d), the current slope is low, and the peak current during the turn-ON process reaches 1 A. Therefore, the turn-ON condition of the LV side switches is a

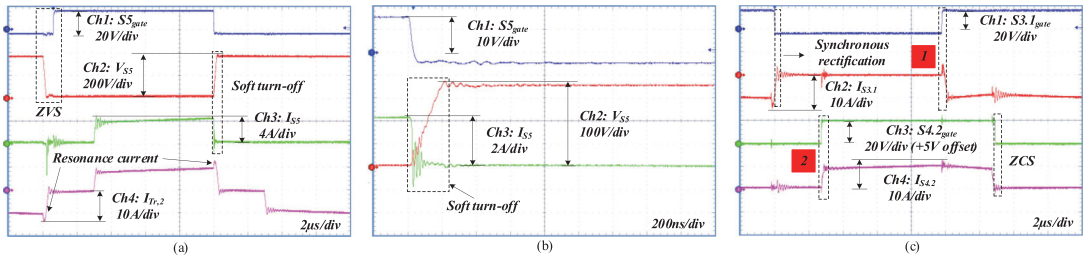

Fig. 9. Experimental waveforms at point (A) of Fig. 5(P(p.u.) $= 0.9 = 3150$ W and $G = 0.8$). (a) Current and voltages of the switch S_5 and transformer current. (b) Soft turn-OFF of the switch S_5. (c) ZCS of the LV port switches.

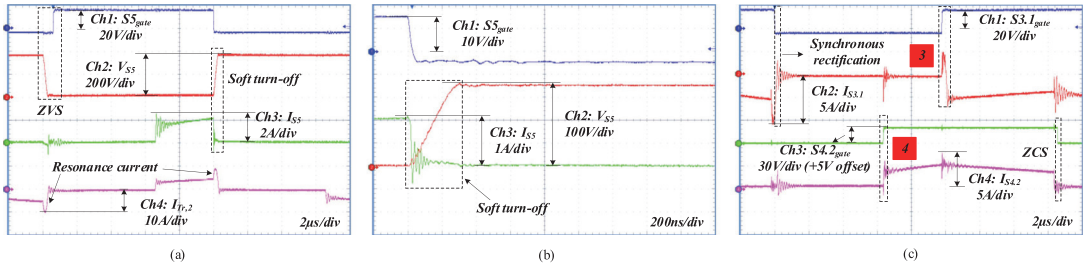

Fig. 10. Experimental waveforms at point (B) of Fig. 5 (P(p.u.) $= 0.4 = 1400$ W and $G = 0.4$). (a) Current and voltages of the switch S_5 and transformer current. (b) Soft turn-OFF of the switch S_5. (c) ZCS of the LV port switches.

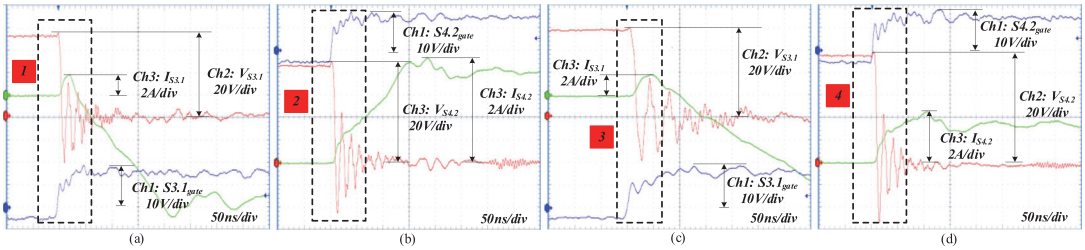

Fig. 11. Soft turn-ON of LV side switches. (a) $S_{3.1}$ turn-ON [point 1 in Fig. 9(c)]. (b) $S_{4.2}$ turn-ON [point 2 in Fig. 9(c). (c) $S_{3.1}$ turn-ON (point 3 in Fig. 10(c)), (d) $S_{4.2}$ turn-ON [point 4 in Fig. 10(c)].

soft turn-ON that is fulfilled by the leakage inductance of the transformer.

Fig. 12(a) demonstrates the soft start when the series capacitor starts to charge (t_1) and reaches the voltage difference between the input and the output (t_2). Afterward, the SSCB connects (t_3) to create a series path for unprocessed power transfer. It is visible that there is no inrush current after the SSCB connection, and the controller can smoothly increase the output current from almost zero to 4 A. In Fig. 12(b), the current reference ramp is applied as reference output current to the controller to observe the capability of the S-PPC to follow the ramp current. The result shows that the PI regulator successfully follows the reference current without any perturbation. It is worth noting that the series capacitor voltage increases slightly by the current ramp due to the parasitic resistances of the component. In Fig. 12(c), the output voltage ramps up from 360 V to 390 V, and the PI controller regulates the output current at the constant reference current of 10 A.

The S-PPC functionality near zero voltage of the series capacitor is also examined to confirm the claims of the previous sections. The result in Fig. 13 verifies the capability of the proposed BDSUD S-PPC to operate at this critical point. Fig. 13(a) illustrates the converter operation in the Q-I where the dc–dc stage works as a buck converter. The modulation strategy here is the PSM implemented throughout the entire voltage regulation range. It can be seen from Fig. 13(a) that the S-PPC can deliver 5 A current without any power circulation between the HV and LV ports. These results prove that S-PPC can regulate the energy transfer to the LV port down to zero.

The results for Q-IV near zero operation are shown in Fig. 13(b). Both D_{rev} and D_s are regulated in a way that D_s is regarded as a constant value ($D_s = 0.25$) and varies to regulate

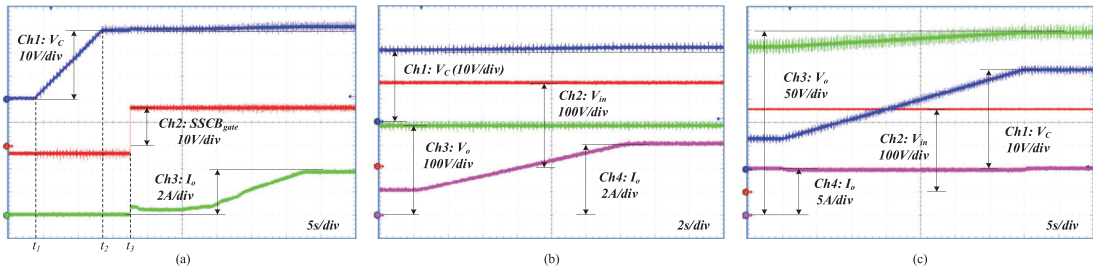

Fig. 12. Dynamic operation of the proposed converter. (a) Soft start procedure to $I_{o\_ref} = 4$ A. (b) S-PPC response to a ramp reference current ($I_{o\_ref} = 2$–6 A). (c) S-PPC response to a voltage ramp at the output port ($V_o = 360$–390 V).

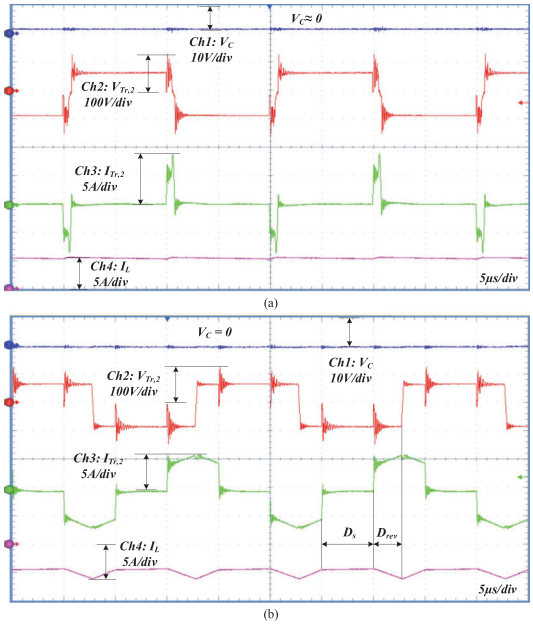

Fig. 13. Operation near the zero voltage of the series capacitor (a) PSM in Q-I with $V_{in} = 350$ V, $V_o = 350$ V (b) Reverse power flow control modulation in Q-IV with $V_{in} = 350$ V, $V_o = 350$ V.

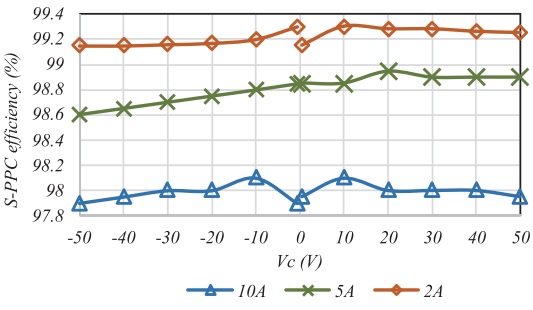

Fig. 14. Efficiency of the proposed S-PPC versus V_c for different currents.

the current at the output port. Both of them are designated in Fig. 13(b). Using the reverse power flow mode of duration D_{rev} provides an opportunity to control the LV side inductor current when the input voltage is too low for its regulation using D_s. During D_{rev}, the energy from the HV port charges the LV port inductor, which can be seen from this figure. When compared to the DAB structure in [22], almost zero energy circulation in Q-I operation mode [see Fig. 13(a)] and controllable limited energy circulation in Q-IV operation mode [see Fig. 13(b)] confirm much better controllability of the BDSUD. As expected, the proposed concept provides low total CSF, over the DAB-based S-PPC. It must be noted that the functionality of DAB-based step-up/down S-PPCs is not investigated in detail in the literature.

Finally, the efficiency measurement is done throughout the different V_C voltages for three current levels (2 A, 5 A, and 10 A in Fig. 14). The peak efficiency of 99.3% is achieved at the output current of 2 A and $V_C = 10$ V, which agrees with (8), as discussed in Section III.

It is worth noting that the given prototype was designed to prove the proposed concept and does not contain any costly components, like transistors with very low R_{DSon}. It was built for robust operation while testing soft-start and soft-switching functionality, resulting in relatively high conduction losses, leaving room for improvement. However, the proposed prototype can still achieve efficiency values of over 99%. Based on the experimental results, the proposed concept could be compared to the other S-PPCs in Table IV. It is worth noting that the comparison demonstrates strong dependence between the range of partiality K_{pr} and maximum efficiency. The wider the range, the lower peak efficiency could be due to design tradeoffs. Also, the efficiency of the reference S-PPC was not provided in [21] to compare with the proposed concept.

Although the closest topology to the BDUSD is the one presented in [22], a comparison table including some of the other similar S-PPCs is demonstrated in Table IV. None of these topologies provide full-range soft switching, and only [22] works with ZVS conditions at high load levels, as discussed in previous sections. The components count is generally higher in bidirectional step-up/down SPPCs than in unidirectional analogs. The same could be concluded about the step-up and step-down S-PPCs, which results in higher maximum power processed by the components. Additional switches are employed

TABLE IV
COMPARISON OF THE PROPOSED S-PPC TO THE EXISTING SOLUTIONS

Ref.	Configuration	Voltage conversion mode	No. of components (S+D+C+M) *	V_{in}	V_o	$K_{pr,max}$	Nominal power (W)	Efficiency range	Soft switching	Soft start
[14]	IPOS	Step-up/down	6+2+2+2	187-253	220	15	750	98.6-99.6	no	no
[16]	IPOS	Step-up	4+2+1+2	154-220	220	30	750	99	no	no
[18]	IPOS	Step-up/down	4+4+2+2	187-253	220	15	950	98.7-99.48	no	no
[19]	-	Step-up/down	8+4+2+2	400	347-435	8	7300	98.5-99.6	no	no
[21]	IPOS	Step-up/down	12+0+3+3	350	300-400	7	1500	-	partial	no
[27]	-	Step-up	8+0+2+2	2-23	50-58	22	3456	80-98.2	no	no
This work	IPOS	Step-up/down	12+0+5+2	300-400	350	17	3500	97.9-99.3	yes	yes

* S – switches, D – diodes, C – capacitors, M – magnetic components.

to form four-quadrant switches or unfolding circuits to enable bipolar operation of the dc–dc stage in the LV port. The presence of diodes in [14], [16], [18], and [19] creates additional conduction loss due to the forward voltage drop of the diodes.

Regarding soft start and near-zero-voltage operation of the series LV port, the existing literature does not demonstrate how the asserted current controllability and high efficiency have been achieved other than by short-circuiting the LV port switches. As the smooth operation of S-PPC at this critical point is important, the methodology to operate at this point must be demonstrated. In [19], the mode change from step-down to step-up is depicted, but the transformer current/voltage becomes zero during this mode change. Apparently, the dc–dc stage stops delivering power in this interval, but the control strategy is not provided. Being based on a current-source dc–dc topology, the converter from [19] is a unidirectional alternative to the proposed converter. It is worth mentioning that the proposed converter provides good current control capabilities by utilizing nearly 90% of the ± 0.5 phase-shift duty cycle theoretical range, while the converter in [19] employs shoot-through duty cycle control, which has little dependence on the power level. As a result, the converter from [19] performs current control at the constant dc voltage gain in a very narrow duty cycle range, raising concerns about its robustness in battery energy storage applications.

V. CONCLUSION

The S-PPC concept can be considered a highly promising solution for various dc–dc applications. However, its practical feasibility is highly influenced by the voltage regulation range requirement and corresponding partiality coefficient. To deal with the application requirements, the S-PPCs based on basic topologies often have to be designed for relatively large power levels, reducing their practical feasibility due to cost and complexity reasons. The proposed BDSUD solution addresses this issue thanks to its step-up/down capability, effectively reducing the partiality coefficient twofold. Moreover, the solution allows bidirectional power flow, making it suitable for various storage and dc microgrid applications. The operation was verified with an experimental prototype with dc–dc stage power of 600 W and total power of 3.5 kW in start-up, steady-state and transient operation modes. When compared to the other known BDSUD S-PPC based on DAB, the proposed solution based on CSFB topology features the following advantages.

1) Thanks to the HB/VDR structure, the turns ratio of the transformer is reduced by at least a factor of 2, simplifying its design.
2) Having the same number of semiconductor devices, the number of gate driver channels and isolated gate supplies is reduced by 2.
3) The topology can be designed for full-range soft switching with simple single phase shift control.
4) The regulation close to zero series port voltage can be provided without excessive energy circulation.
5) The overall component stress factor is lower for most of the operating points

At the same time, the design and operation of the converter are highly influenced by the leakage inductance of the transformer, which has to be always minimized at the design stage. The parasitic oscillations at the LV stage appear regardless of the modulation strategy, resulting in higher voltage stress and requiring approximately 50% higher voltage rating of the devices than that in the DAB counterpart. Nevertheless, the cumulative advantages of the proposed BDSUD make it among the most versatile and promising S-PPC concepts for practical applications.

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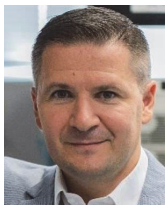

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Publication IV

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APPLIED RESEARCH

Analysis of Design Requirements and Optimization Possibilities of Partial Power Converter for Photovoltaic String Applications in DC Microgrids

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ABSTRACT The paper analyzes the application flexibility of partial power converters for interfacing photovoltaic strings in dc microgrids. Step-up/down partial power converters were considered for providing the lowest active power processing. This study considers three Si-based photovoltaic modules commonly used in residential applications: 54-, 60-, and 66-cell. Different configurations of photovoltaic strings are analyzed to find at what voltages most energy is generated in hot and cold climates. Combining these results with the operating voltage range of a droop-controlled dc microgrid yields design requirements for the partial power interface converters. The proposed design limits the maximum power the converter processes to optimize its components. Next, the application of the topology morphing control is studied regarding the performance enhancement of partial power converters. Experimental results verify good converter performance and feasibility of efficiency improvement with the topology morphing control.

INDEX TERMS DC-DC converters, dc microgrids, partial power conversion, photovoltaic energy.

I. INTRODUCTION

Power electronic converters are the backbone of future energy use, considering the increasing electrification of technical processes [1], [2], [3]. The deployment of renewable energy sources keeps growing year-to-year, pushing the power electronics industry to produce converters with better performance and lower cost [4], [5]. Despite its intermittent nature, photovoltaic (PV) energy is considered the most promising solution for a sustainable future [6]. The cumulative PV generation capacity has recently reached 1 TW [7]. All these developments pushed the technology of power converters for large-scale PV installations to a good level of maturity [8], [9].

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At the same time, PV technologies enable nearly zero-energy buildings by replacing electricity demand with on-site energy generation [10], [11]. PV string inverters are also widely available and highly efficient [12]. The next step in the efficiency enhancement of residential and small commercial buildings is the adoption of dc microgrids [13], [14], [15]. However, dc-dc power electronics converters for these applications are based on the conventional full power processing approach, which is mature and limited by the barriers of the existing technologies of semiconductor and passive components [16].

Partial power processing is a novel concept for dc-dc energy conversion, as shown in Fig. 1. It allows for processing only a fraction of the total power, reducing the power losses to much below those of conventional full-power converters [17]. Partial power converters (PPCs) are typically implemented

using an isolated dc-dc cell that is connected in parallel to one of the ports (V_{DC} in Fig. 1) and in series between the ports on the other side (V_C in Fig. 1) [16]. The dc-dc cell regulates the voltage difference between two ports, i.e., the voltage of the series-connected side (V_C in Fig. 1). As a result, the parallel high-voltage (HV) port is rated for full voltage but partial current. Also, the series low-voltage (LV) port operates at full current and partial voltage. The power processed by the dc-dc cell depends on the voltage range in the series port [17]. Hence, PPCs are a niche technology that works best when this voltage range can be narrowed down [18]. It has been demonstrated for PV applications, electric vehicle charging, power flow control in dc microgrids, wind turbines, fuel cells, and other applications [17].

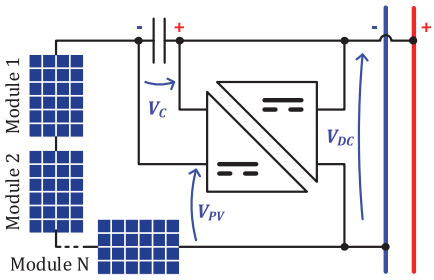

FIGURE 1. The concept of partial power interface converter for integration of PV strings in dc microgrids.

The advantages of PPC technology have attracted the interest of researchers, especially in PV applications [19], [20]. Numerous PPC topologies are proposed for PV string applications [17]. However, only a few show a peak efficiency of at least 99% [16]. Typically, a PPC comprises a voltage-fed dc-dc cell connected in parallel input series output (PISO) configuration and performs either voltage step-up or step-down between two ports [16]. Series input parallel output (SIPO) configurations were also demonstrated recently. It could be concluded from the recent literature that SIPO configuration must be implemented with a current-fed dc-dc to provide a peak efficiency of over 99% [21], [22].

It was shown that the performance of a PPC interfacing a PV string could be improved by limiting the relative amount of power processed by the dc-dc cell, i.e., limiting its partiality coefficient K_{pr} [18]. The concept of step-up/down PPC capable of reversing polarity in the series port voltage (V_C) was introduced to reduce the fraction of the processed power [23], [24]. The step-up/down PPCs can operate with up to two times lower active power than the step-up and -down PPCs in the same applications. Hence, more research is required to establish the most suitable application scenarios and demonstrate performance enhancement techniques.

Prior studies have not targeted PPC applications for interfacing PV strings in droop-controlled dc microgrids, which creates a knowledge gap in this field. In these applications, the voltage of both PV and dc microgrid ports feature some operating range, extending the voltage range in the series port of PPC. For example, the study [23] considered possible variations of the maximum power point (MPP) voltage for hot environmental conditions in Brazil. In contrast, this work considers how MPP voltage varies in hot and cold environmental conditions to show a realistic estimate of possible operating voltage on the PV side, which was not analyzed before. Moreover, it considers three typical residential Si-based PV module types and their different number in a PV string. In addition, the droop control voltage range on the dc microgrid side is included in the analysis. As a result, this study synthesizes practical PPC design requirements for PV string applications in residential dc microgrids, closing the existing knowledge gap in this field. Since voltage variations at both PV string and dc microgrid ports are considered, such an interface step-up/down PPC should operate in a relatively wide dc gain range, which would deteriorate its peak efficiency [18]. Hence, this study also analyzes the feasibility of efficiency improvement by applying topology morphing control (TMC) techniques [25].

Residential droop-controlled dc microgrids with a nominal voltage of 350 V and droop control range of ±30 V are being standardized in the EU [26]. This study analyzes step-up/down PPC technology to provide optimized solutions for integrating PV strings in 350 V residential droop-controlled dc microgrids. This paper builds upon the results published in [27]. The contributions of this paper are as follows:

- Modeling of dependence between energy production and operating voltage for three typical residential PV modules for two climates to define the applicability of step-up/down PPCs for residential PV string.
- Analysis of PPC application requirements and feasibility of PPC-based residential PV string implementations with restricted voltage regulation range, considering the droop control voltage range of residential dc microgrids.
- Demonstration of TMC for efficiency improvement of step-up/down PPCs and experimental performance evaluation of two feasible TMC implementations.

Hence, the paper provides a comprehensive analysis of realistic PPC operating conditions and draws design requirements in Section II. Also, it studies the feasibility of improving PPC efficiency by applying the TMC modulations proposed in Section III. Experimental results in Section IV yield a discussion about the validity of the taken assumptions. The conclusions are drawn in Section V.

II. ANALYSIS OF DESIGN REQUIREMENTS

This section considers three typical PV modules of monocrystalline Si marketed for residential users. Their types and parameters are listed in Table 1. These modules differ in the equivalent number of PV cells, which could also be composed of half-cut cells to reduce in-module conduction losses. As these PV modules have virtually the same surface area, the difference in the number of equivalent cells originates from the use of different standardized sizes of PV cells available on

TABLE 1. Datasheet parameters of residential PV modules.

Parameter	PV modules		
	Qcell Q.PEAK DUO BLK M-G11 [28]	Trina Solar TSM-DE06X.05(II) [29]	Canadian Solar HiKuBlack CS3L-370MS [30]
No. of cells (half cells)	54	66 (132)	60 (120)
Nameplate power, W	400	380	370
$V_{MPP(STC)}$, V	31.2	37.8	34.1
$I_{MPP(STC)}$, A	12.8	10.1	10.9
$V_{OC(STC)}$, V	37.2	45.5	40.8
$I_{SC(STC)}$, A	13.4	10.5	11.5
$V_{MPP(NOCT)}$, V	29.7	35.6	31.9
$I_{MPP(NOCT)}$, A	10.1	8.1	8.7
$V_{OC(NOCT)}$, V	35.1	42.8	38.5
$I_{SC(NOCT)}$, A	10.8	8.5	9.3
NOCT, °C	42±3	43±2	42±3
β, %/K	-0.27	-0.25	-0.25
γ, %/K	-0.34	-0.34	-0.34

the market [16]. Hence, nearly the same power is achieved at different MPP voltages. This phenomenon allows for making PV strings of different power levels, i.e., suitable for various roof areas, within a limited MPP voltage range.

To identify practical MPP voltage range, modeling of annual energy yield was performed using mission profiles of the solar irradiance and ambient temperature recorded in Arizona, USA, and Aalborg, Denmark. The methodology [31] based on approximating the MPP voltage and current using the Lambert W_0 function was used. This methodology assumes that the PV modules are installed at the optimal angle corresponding to the location latitude to estimate the maximum available PV energy. The modeling is based on fitting some parameters using a specialized add-on of the PSIM software and datasheet parameters for the standard test conditions (STC) and nominal operating cell temperature (NOCT), such as the short-circuit current (I_{SC}), open-circuit voltage (V_{OC}), MPP voltage (V_{MPP}), MPP current (I_{MPP}), V_{OC} temperature coefficient (β), and MPP power temperature coefficient (γ). All other assumptions and modeling constants/coefficients are assumed to be the same as in [31]. The modeling assumes a PV string always operates in the MPP. Twenty eight yearly simulations were performed.

The modeling results are given in Fig. 2, where the height of each bar corresponds to the annual energy generated within a given voltage band. PV strings operate at higher MPP voltages but produce less PV energy in cold climates than in hot ones. Performing analysis for both climate types allows for demonstrating real variability of the MPP tracking range required for each PV string configuration. It was identified that the PV voltage range between 250 V and 450 V can accommodate fourteen possible PV string configurations using the selected three PV module types:

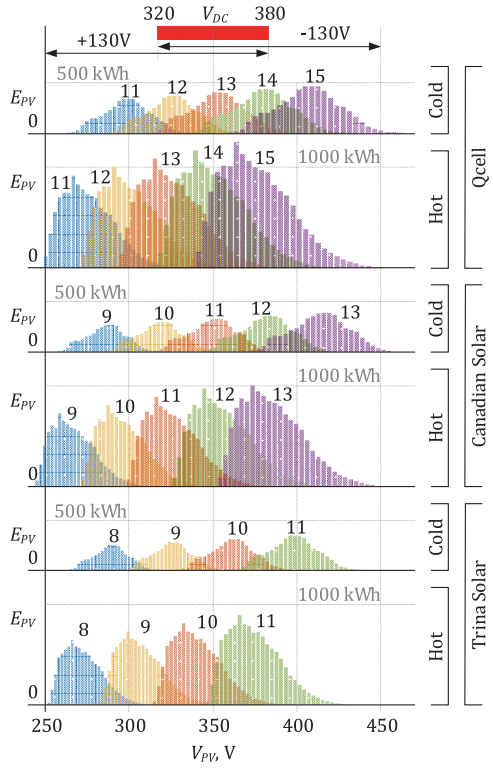

FIGURE 2. Probability of annual PV energy production versus PV string voltage for different PV strings in hot and cold climates for three PV module types.

1) 54-cell PV module: PV strings of 11 to 15 modules are feasible with power ratings between 4.4 kW and 6 kW for the roof installation area between 21 m^2 and 29 m^2.
2) 60-cell PV module: PV strings of 9 to 13 modules are feasible with power ratings between 3.3 kW and 4.8 kW for the roof installation area between 17 m^2 and 24 m^2.
3) 66-cell PV module: PV strings of 8 to 11 modules are feasible with power ratings between 3 kW and 4.2 kW for the roof installation area between 15 m^2 and 21 m^2.

These results prove that PPC technology could be a practical solution for residential PV string applications in dc microgrids. Fig. 2 also depicts the droop-control voltage range of residential dc microgrids between 320 V and 380 V. As a result, an interface step-up/down PPC must be designed for the operating voltage range of the series port voltage V_C of ±130 V. The selected PV string MPP tracking voltage range of 250 V to 450 V limits the PPC power rating at 1.65 kW to cover the selected PV strings with rated power between 3 kW and 6 kW. This variety of power levels and, consequently, the roof surface areas, provide sufficient versatility to suit most small residential installations. Moreover, the PV modules are built in different sizes, simplifying the PV string design for any roof geometry.

The obtained series voltage regulation range of ±130 V should be satisfied even at the lowest dc microgrid voltage of 320 V. This could be converted into the maximum ratio between the dc-dc converter power, i.e., the power processed by PPC, of roughly 40%. However, this metric is misleading as the rated power of dc-dc converter, i.e., the partiality, remains the same for both the maximum and minimum dc microgrid voltages of 320 V and 380 V, respectively. In these points, the dc-dc converter processes up to 1.65 kW, considering the MPP current of the PV modules is below 13 A. Moreover, connecting the parallel port of the PPC to the dc microgrid causes lower worst-case current stress in its semiconductor devices as the dc microgrid voltage range is considerably narrower than the PV string voltage range.

It is worth mentioning that modern TMC techniques employ the capability of some dc-dc converters to reconfigure their topology. Typically dc gain is changed in integer steps to optimize converter operation in a wide input voltage range. The next section presents the case-study PPC topology and demonstrates possible TMC implementation that will be evaluated experimentally.

III. TOPOLOGY AND CONTROL OF THE CASE-STUDY PPC

The topology of the case-study step-up/down PPC shown in Fig. 3 was first presented in [27] and analyzed in [32]. It was synthesized from the current-fed dc-dc converter topology described in [33] and [34]. This section presents three possible modulation techniques that could be used for the TMC implementation. Also, it includes a solid-state circuit breaker (SSCB) for protection and soft-start functionality, which results in extra conduction losses during PPC operation.

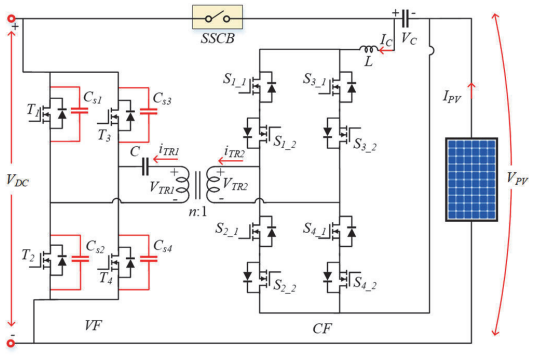

FIGURE 3. Topology and connection configuration of the case-study PPC.

The case-study PPC comprises a dual active bridge dc-dc converter with current-fed (CF) and voltage-fed (VF) sides. The converter operation is described for the CF to VF side power flow. In the power stage, the PV and dc bus voltage ranges are considered equal to 250-450 V and 320-380 V, respectively. The VF consists of a full bridge with a capacitor connected in series with the primary side of the transformer. This capacitor enables reconfiguring the full-bridge VF side into the corresponding half-bridge cell. The CF comprises a full-bridge matrix inverter and a series-connected inductor. Four-quadrant switches enable soft-switching of all semiconductors and simple changing of voltage V_C polarity by flipping gating signals in the CF bridge [33], [34].

A. BASELINE MODULATION

The dc-dc converter operation with the baseline modulation [34] is shown in Fig. 4 (a). The baseline modulation (where I_C is negative and CF side voltage is positive) is shown in Fig. 4 (b) and explained as follows. Using this modulation, the switches S_{1_1}, S_{3_1} and S_{2_1}, S_{4_1} operate in PWM mode with a 180° phase shift. Here, the switches S_{2_1}, S_{4_1} are shifted regarding S_{1_1}, S_{3_1}. The phase shift angle $\phi_{control}$ is the main control variable defining the dc-dc converter gain. Interval t_0- t_1 represents the active state of the converter when the power is transferred from CF to VF side.

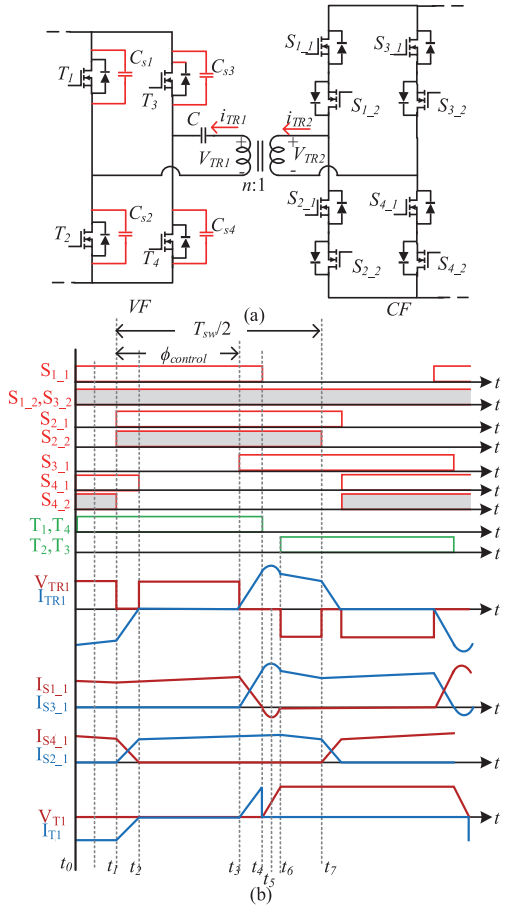

FIGURE 4. Operation of the dc-dc cell with the baseline modulation (a) and the corresponding idealized voltage and current waveforms (b).

During it, the switches T_1 and T_4 are turned on while T_2 and T_3 are turned off. During the interval t_2- t_3, the switches S_{1_1},

S_{1_2}, S_{2_1}, and S_{2_2} conduct to energize the inductor. Turning off of S_{4_1} with ZCS is achieved. In t_4-t_5, the converter current rises with the same slope and exceeds the inductor current.

The current direction reverses in switches S_{1_1} and S_{1_2}, enabling the turning off of switch S_{1_1} with zero-current switching (ZCS). The converter also benefits from ZVS on the VF side. From t_6, the converter enters the next active state and a similar process can be repeated. Soft-switching could be achieved in the same manner for negative CF voltage. It would require the switches S_{2_1}, S_{4_1} to be turned on, while the switches S_{1_2}, S_{3_2} function similarly to a synchronous rectifier. Switches S_{2_2}, S_{4_2} operate with a fixed phase shift with respect to VF side switches and perform the ZVS and ZCS for VF and CF side semiconductors, correspondingly. Equation (1) represents the voltage equation for a PPC, where V_{PV}, V_{DC}, and V_C define the PV voltage, dc microgrid voltage, and the series voltage to the PCC, respectively. A generalized PPC voltage gain (G_{PPC}) can be carried out as (2), where the phase shift angle $\varphi_{control}$ defines the dc gain [33], [34].

$$V_{PV} = V_{DC} + V_C \tag{1}$$

$$G_{PPC} = \frac{V_{DC}}{V_{PV}} = \frac{1}{1 + G_{dc-dc}} \tag{2}$$

Here, the partiality ratio K can be written as (3).

$$K = 1 - \frac{1}{G_{PPC}} \tag{3}$$

The simplified equation for voltage gain of the dc-dc converter G_{dc-dc} can be expressed as (4). The detailed equation of the dc-dc gain is given by (5), where t_{res} represents the resonance period t_4- t_6, and f_{SW} is the switching frequency [33].

$$G_{dc-dc} = \frac{V_C}{V_{DC}} \tag{4}$$

$$G_{dc-dc} = \frac{\pi n}{1 - \frac{\varphi_{control}}{\pi} - 2f_{sw}\left(\frac{2nL(2I_{c(max)} - I_c)}{V_{DC}} + t_{res}\right)}, \tag{5}$$

where $I_{C(max)}$ is the maximum input current of the dc-dc cell defined at the design stage, and I_C is the average input current of the dc-dc cell. This makes the dc gain weakly dependent on the operating power.

B. MODULATION WITH VF-SIDE TMC (TMC-VF)

In the TMC-VF modulation, a small modification is made in the baseline modulation explained earlier. Fig. 5 (a) shows the dc-dc stage operation with the TMC-VF modulation detailed in Fig. 5 (b). The VF side switch T_3 is turned off, and T_4 is turned continuously. At the same time, the switches T_1 and T_2 operate in PWM mode. The CF-side switches are modulated with a duty cycle of slightly over 0.5 to ensure their ZCS and perform synchronous rectification (bottom switches). The time intervals in the switching sequence are essentially the same as in the baseline modulation.

The TMC-VF modulation effectively doubles the normalized dc voltage gain of the dc-dc converter from equation (5),

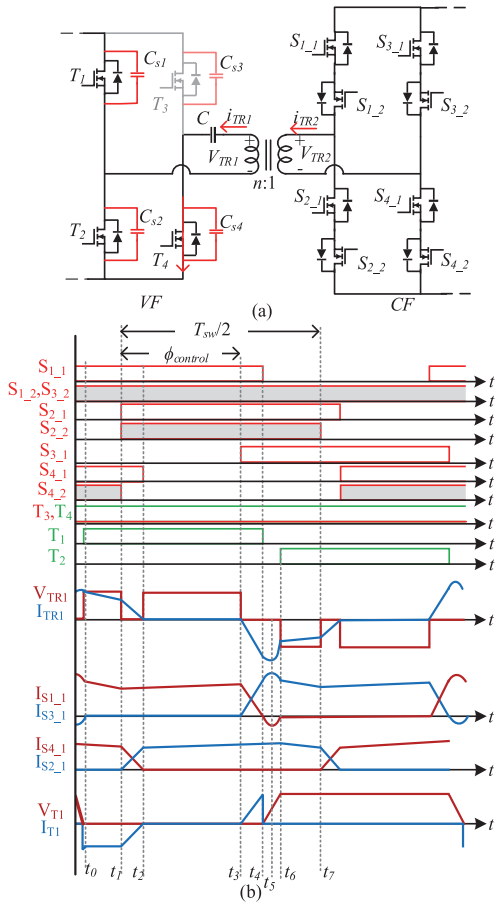

FIGURE 5. Operation of the dc-dc cell with the TMC-VF modulation (a) and the corresponding idealized voltage and current waveforms (b).

which can be written as (6).

$$G_{dc-dc} = \frac{2\pi n}{1 - \frac{\varphi_{control}}{\pi} - 2f_{sw}\left(\frac{2nL(2I_{c(max)} - I_c)}{V_{DC}} + t_{res}\right)} \tag{6}$$

C. MODULATION WITH CF-SIDE TMC (TMC-CF)

The equivalent circuit corresponding to the TMC-CF modulation is illustrated in Fig. 6 (a). The bottom switches of the CF side S_{2_1}, S_{2_2}, and S_{4_1}, S_{4_2} are modulated complementary with a duty cycle of slightly over 0.5. The VF-side switches $T_1 \ldots T_4$ are modulated in diagonals complementary with a duty cycle of slightly below 0.5.

The TMC-CF modulation is shown in Fig. 6 (b) for one switching period. During t_0- t_1, the switch S_{2_1} turns on with ZCS with the help of the leakage inductor. The interval t_2- t_3 allows the switch S_{4_1} to turn off with ZCS. In the interval t_3- t_4, the VF-switches T_1, T_4 start to turn off with ZVS assisted by the snubber capacitors C_{s1} and C_{s4}, respectively. At the same time, the snubber capacitors C_{s2} and C_{s4}

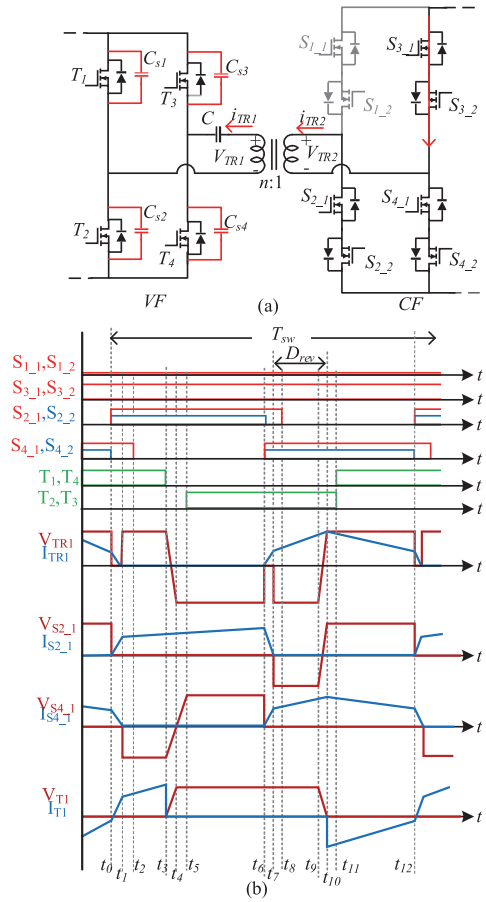

FIGURE 6. Operation of the dc-dc cell with the TMC-CF modulation (a) and the corresponding idealized voltage and current waveforms (b).

discharge to zero. The energy is delivered to the VF side during the time interval t_5-t_6 after the switches T_2 and T_3 are turned on with ZVS. Next, in the interval t_6- t_7, the CF-side switches S_{4_1} and S_{4_2} turn on with ZCS. The interval t_7- t_8 is equivalent to t_1- t_2, and it begins the reverse energy transfer direction. Interval t_8- t_9 allows S_{4_1} to turn off with ZCS. In the following intervals, i.e., t_9- t_{10} and t_{10}- t_{11}, the energy transfers from CF to VF via the transformer with the help of body diodes of T_2 and T_3, similar to the classical forward dc-dc converter. In the last interval t_{11}- t_{12}, switches T_2 and T_3 are turned on with ZVS. Therefore, the relative duration of the reverse energy transfer period (D_{rev}) is the control variable defining the dc-dc converter gain, as given in (7) from [35].

$$G_{dc-dc} = \frac{V_C}{V_{DC}} = \frac{2n}{1-4D_{rev}} \tag{7}$$

This modulation TMC technique was first proposed in [35]. This modulation differs from the previous two, featuring minimized energy circulation between the VF and CF sides. The TMC-CF modulation harnesses high circulating energy for charging the inductor L. As a result, the current stress factors of components would increase, but it would provide good controllability at very low voltage V_C values. Unlike the other two modulations, the TMC-CF has two voltage-boosting mechanisms: short-circuiting the inductor L and circulating the energy, where the second one is dominant.

D. SUMMARY OF THE TMC MODULATIONS

Equations (5) – (8) show that the TMC-VF and -CF modulations provide doubled dc-dc converter gain compared to the baseline modulation. These modulations could be used in the V_C range of ±60 V in the given applications.

The TMC-VF modulation reduces transformer core losses due to the twice-reduced swing of the voltage v_{TR1}, i.e., its flux density is twice lower. On the other hand, the transistors T_1 and T_2 should operate with doubled current stress. Hence, efficiency improvement is expected to be more prominent at higher dc microgrid voltages, closer to 380 V. The TMC-CF cannot reduce core losses but features fewer CF-side devices conducting current even with higher current stress.

Based on their characteristics, it could be predicted that the TMC-VF should provide higher efficiency than the TMC-CF. The following section provides experimental evaluation and benchmarking of these modulations. It is worth emphasizing that all three modulations feature soft-switching of the semiconductor devices, but the TMC-CF modulation uses circulating energy, causing higher current stress on the components.

IV. EXPERIMENTAL VERIFICATION

This section provides an extensive experimental study detailing the performance of all modulations and corresponding control variables using an experimental prototype described in the first subsection. Moreover, a discussion on performance enhancement of the case study step-up/down PPC is provided with quantification of efficiency differences.

A. PROTOTYPE DESCRIPTION

An experimental prototype (Fig. 7) was constructed. The isolation transformer was designed with a turns ratio of 2.1, according to (8). This value leaves a sufficient margin for the overlap of CF-side gating signals needed for soft-switching.

$$n \leq \frac{min\,(V_{DC})}{max\,(V_C)} = \frac{320}{130} \approx 2.46 \tag{8}$$

The transformer was designed using two parallel EE42/21/20 cores of N87 material. The windings utilize 10 turns of 2000 × 0.04 mm Litz wire and 21 turns of 1200 × 0.04 mm Litz wire, which results in the maximum flux density of 100 mT. This design achieves leakage and magnetizing inductance values reflected to the CF-side winding of 0.6 μH and 800 μH, respectively. The input inductor L is built using a gapped ETD54/28/19 core of 3C97 material. The dc blocking capacitor in the winding *TR1* and the capacitor in the CF port are both equal to 60 μF.

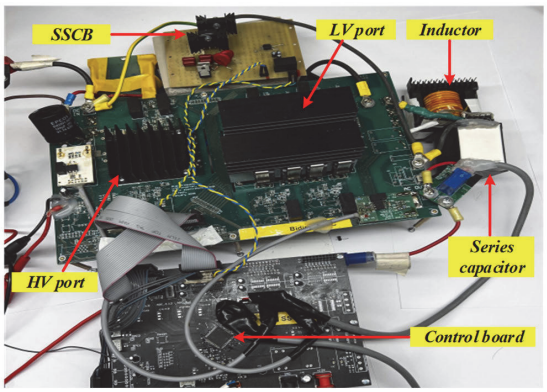

FIGURE 7. Photo of the experimental prototype.

TABLE 2. Components and parameters of the experimental prototype.

Component/Parameter	Symbol	Value/Type
LV port switches	$S_{1.1}$-$S_{4.2}$	C3M0120090D
HV port switches	T_1-T_4	C3M0120090J
Isolated gate drivers	-	UCC21520-Q1
LV port inductor	L	100µH
Inductor core	-	ETD54/28/19/3C97
Transformer leakage inductance	L_{eq}	850nH
Transformer turns ratio	n	2.3:1
Transformer core	-	ETD54/28/19/3C97
HV port capacitors	C_1=C_2	60µF (Foil)
Series capacitor	C	100µF (Foil)
HV port snubber capacitors	C_s	1.1nF (Ceramic)

To ensure robust operation during testing, 120 mΩ/900 V SiC MOSFETs were used on the VF and CF side. Despite the relatively high $R_{DS,on}$ the prototype is still viable as the converter exhibits predominantly conduction losses. Their reduction will be more prominent with this design, allowing efficiency measurement with higher accuracy. The SSCB utilizes 30 mΩ Si switches, which put the associated conduction losses below 7 W during tests. The control system is based on STM32G474 microcontrollers comprising a multichannel high-resolution PWM timer (HRTIM). The main components and parameters of the prototype are listed in Table 2.

The efficiency was measured at PV currents of 3 A, 7 A, and 10 A using a Yokogawa W1800E power analyzer with basic power accuracy of 0.05%. A bidirectional power supply from iTECH IT6000C series was used to emulate a stiff dc microgrid, while a PV string emulator Chroma 62150H-1000S was utilized as the input power source. Voltage waveforms were measured using a differential voltage probe with 100 MHz bandwidth, and the current waveforms were measured using an isolated AC/DC current probe with 120 MHz bandwidth. The probes were used with a 4-channel oscilloscope with 350 MHz bandwidth/channel.

B. PERFORMANCE EVALUATION OF THE PPC WITH BASELINE MODULATION

First, the prototype was tested without TMC modulation techniques to assess general performance trends. The measurements of the PPC and dc-dc converter efficiencies were performed for the three dc microgrid voltages: $V_{DC} = 320$ V (Fig. 8), $V_{DC} = 350$ V (Fig. 9), and $V_{DC} = 380$ V (Fig. 10). The general efficiency trade-off is that converter performance is better at lower current in the voltage step-up mode, and higher current in the step-down mode. This is caused by higher (static) circulating energy when the dc-dc converter transfers energy from the CF to the VF side [34].

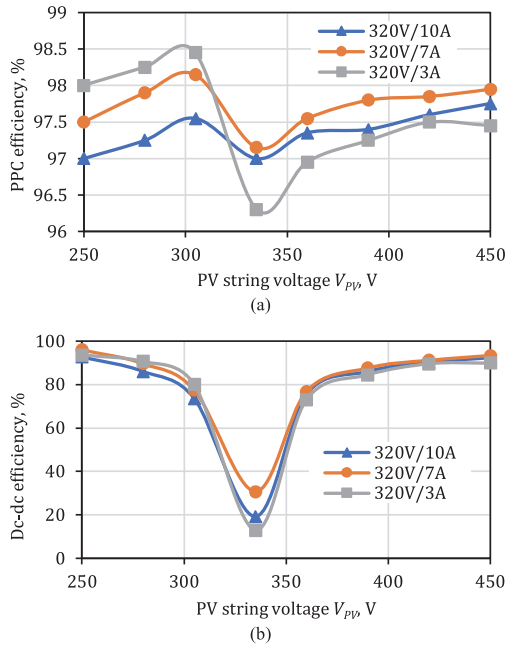

FIGURE 8. Efficiency measured with the baseline modulation at V_{DC} = 320 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

The dc-dc converter features minimum efficiency when PV string and dc microgrid voltages are equal, as could be expected from nearly zero processed power, as follows from Fig. 11. In this point, it operates with a phase shift angle of close to zero, as depicted in Fig. 12. The phase shift angle defines the dc gain, but have little dependence on the system power, only minor adjustment is needed to compensate for the increased conduction losses if the power rises. It linearly depends on the PV string voltage, while its sign defines the power transfer direction. This linearity would simplify the design of a control system, as it allows a typical PI controller to provide stable regulation.

The power processed by the dc-dc converter varies from nearly 0 W to almost 1500 W, while the PV string power

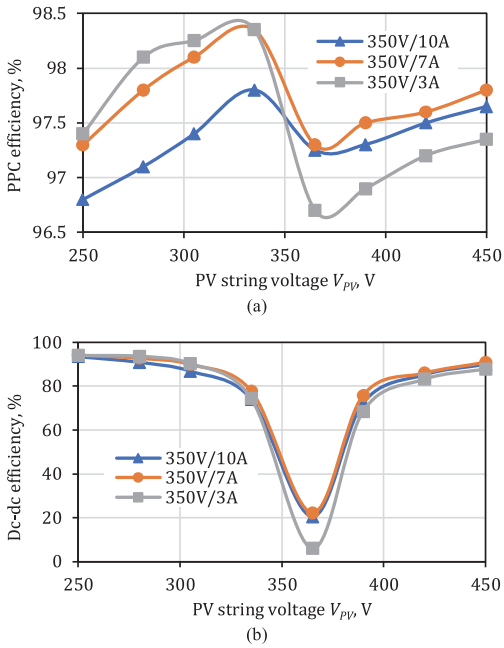

FIGURE 9. Efficiency measured with the baseline modulation at V_{DC} = 350 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

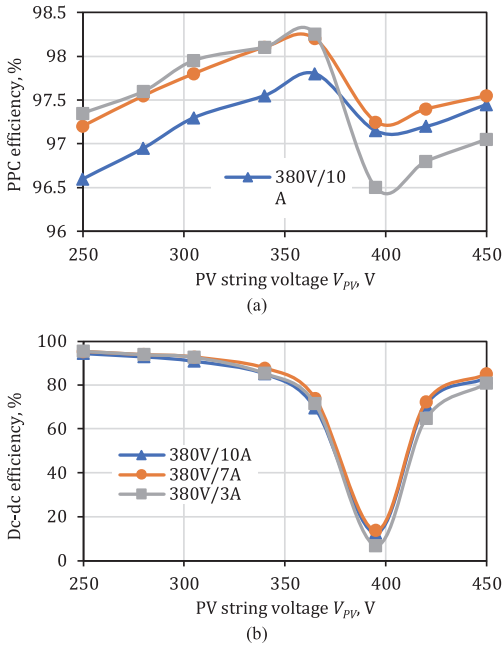

FIGURE 10. Efficiency measured with the baseline modulation at V_{DC} = 380 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

reaches up to 4.5 kW. The efficiency of dc-dc cell varies significantly, which, however, results only in a small drop in the PPC efficiency. Also, it is important to mention that

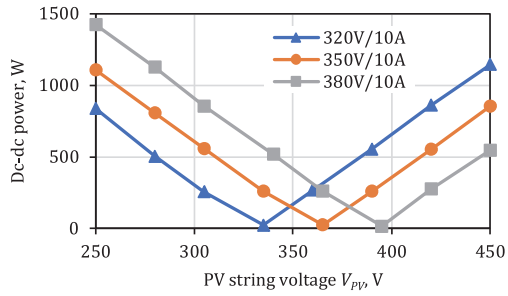

FIGURE 11. Experimentally measured active power processed by dc-dc converter plotted for three dc microgrid voltages across the PV string voltage range.

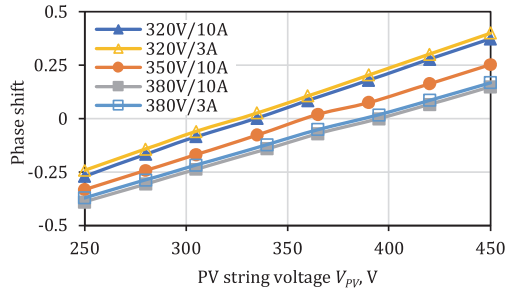

FIGURE 12. Experimental phase shift angle of the baseline modulation plotted in p.u. for five test conditions across the PV string voltage range.

the point of zero processed power is shifted from the $V_{PV} = V_{DC}$ condition due to voltage drop on the CF-side and SSCB transistors, wiring, and other ohmic losses in the converter. The dc-dc call must produce a small voltage to compensate for these resistances when the $V_{PV} = V_{DC}$.

C. PERFORMANCE EVALUATION OF THE PPC WITH TMC-VF MODULATION

The measurements of the PPC and dc-dc converter efficiencies were performed with the TMC-VF modulation for the three dc microgrid voltages: V_{DC} = 320 V (Fig. 13), V_{DC} = 350 V (Fig. 14), and V_{DC} = 380 V (Fig. 15). The general efficiency trade-off is similar to the baseline modulation at higher currents due to their similarity. The efficiency improved at low currents, where RMS current stress is low, and a reduction in transformer losses is more evident. The efficiency improvement over the baseline modulation could be observed. This results from the dc-dc cell operating in more favorable conditions, allowing higher overall efficiency and a smaller drop in efficiency ner zero partiality. On the other hand, it was found that current regulation near zero partiality is limited and could restrict PPC applicability.

The phase shift angle provides twice higher dc-dc gain with the TMC-VF modulation than the baseline modulation, as observed from Eqs. (5) and (6). This trend is confirmed experimentally, as can be observed in Fig. 16. As was

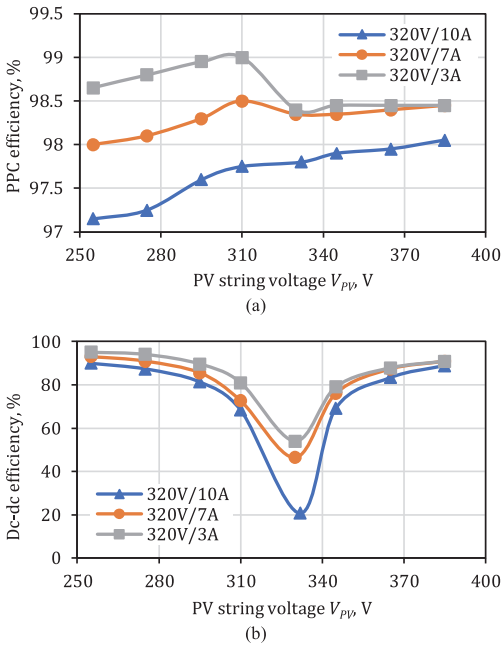

FIGURE 13. Efficiency measured with the TMC-VF modulation at V_{DC} = 320 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

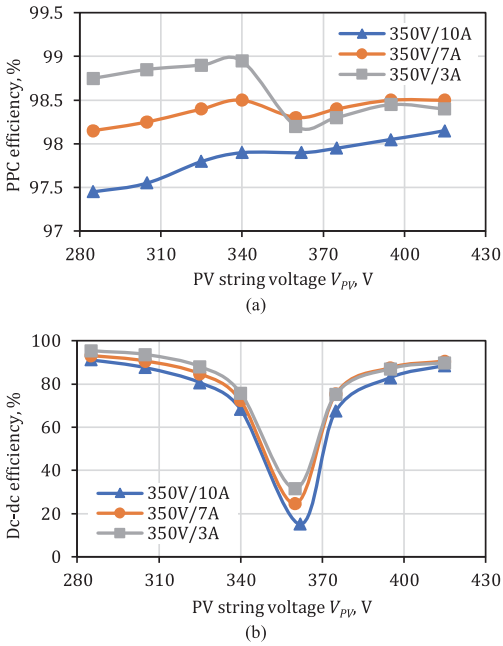

FIGURE 14. Efficiency measured with the TMC-VF modulation at V_{DC} = 350 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

mentioned, this modulation is feasible in the voltage range of the series port V_C, i.e., the difference between the PV string and dc microgrid voltages of ±60 V.

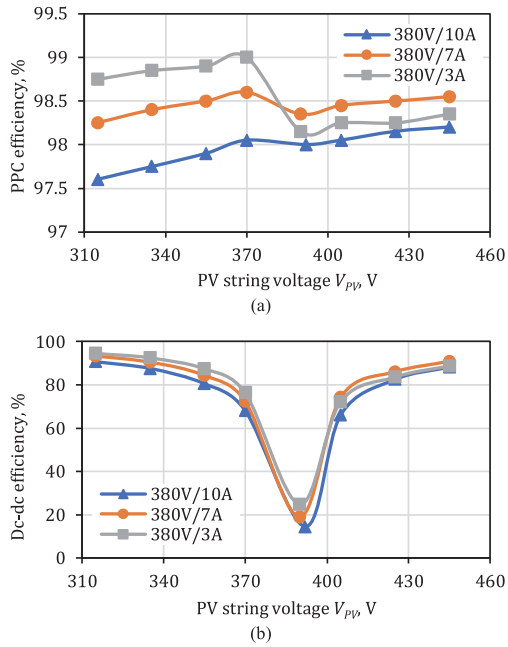

FIGURE 15. Efficiency measured with the TMC-VF modulation at V_{DC} = 380 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

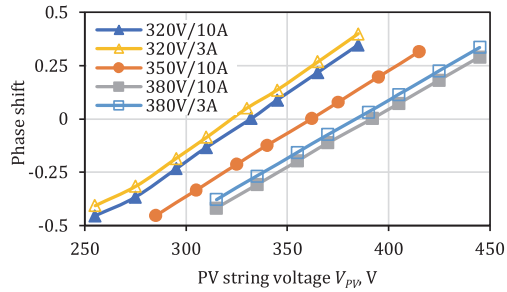

FIGURE 16. Experimental phase shift angle of the TMC-VF modulation plotted in p.u. for five test conditions across the PV string voltage range.

D. PERFORMANCE EVALUATION OF THE PPC WITH TMC-CF MODULATION

The TMC-CF modulation was also experimentally verified at three dc microgrid voltages: V_{DC} = 320 V (Fig. 17), V_{DC} = 350 V (Fig. 18), and V_{DC} = 380 V (Fig. 19). Generally, the efficiency rises when the PV string voltage increases. It follows the RMS current stress trend, defined mainly by the circulating energy. The efficiency is significantly lower in the step-up mode of the PPC due to energy transfer from the VF to the CF side. Compared to the baseline modulation, the efficiency is lower as this modulation employs a significant amount of circulating energy for current regulation. On the

other hand, this energy enables smooth current regulation near zero partiality.

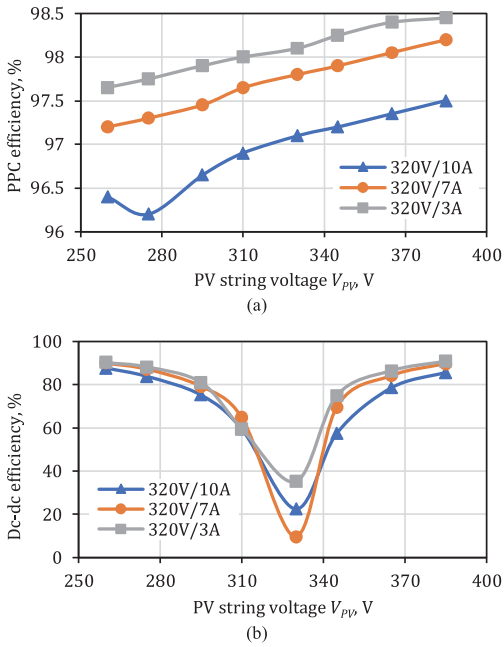

FIGURE 17. Efficiency measured with the TMC-CF modulation at V_{DC} = 320 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

To achieve this power flow direction, the circulating energy should be dominant. The duty cycle of the corresponding time interval, the main control variable in this mode, must be over 0.25. As a result of the reverse energy transfer from the VF to the CF side using the circulating energy, the RMS current of components increases significantly. In the step-down mode, the duty cycle of the reverse energy interval is below 0.25. As a result, the efficiency is higher. The correlation between the power loss and the reverse energy interval duration could be easily established by correlating its values from Fig. 20 and the measured efficiency curves from Figs. 17, 18, and 19. Despite the drawback of high conduction losses, this modulation features smooth behavior of the PPC efficiency curves. Also, it harnesses the circulating energy for current regulation near zero voltage at the series port. Similar to the TMC-VF modulation, the TMC-CF modulation could be applied only in the range of V_C between –60 V and +60 V.

E. COMPARISON OF MODULATION TECHNIQUES

First, to demonstrate fundamental differences between the studied modulation techniques, the experimental waveforms of the CF side current of the dc-dc converter, transformer current, and voltages across the transformer windings are shown in Figs. 21, 22, and 23 for the baseline, TMC-VF, and TMC-CF modulations, respectively. It is evident that the latter differs from the first two modulations by its operating principle and, consequently, its current/voltage waveforms.

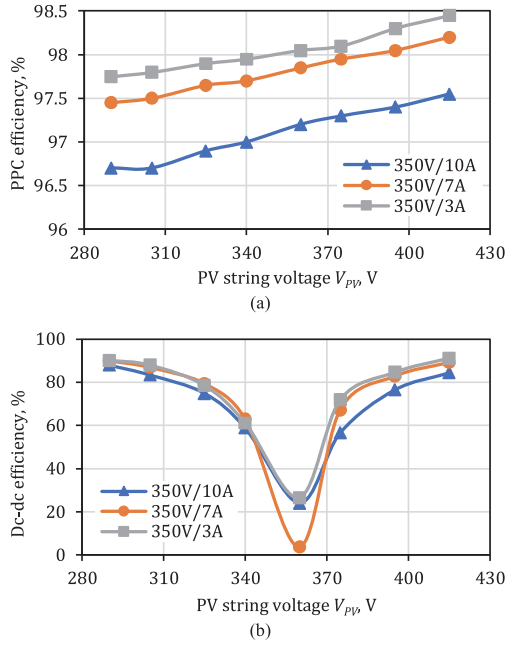

FIGURE 18. Efficiency measured with the TMC-CF modulation at V_{DC} = 350 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

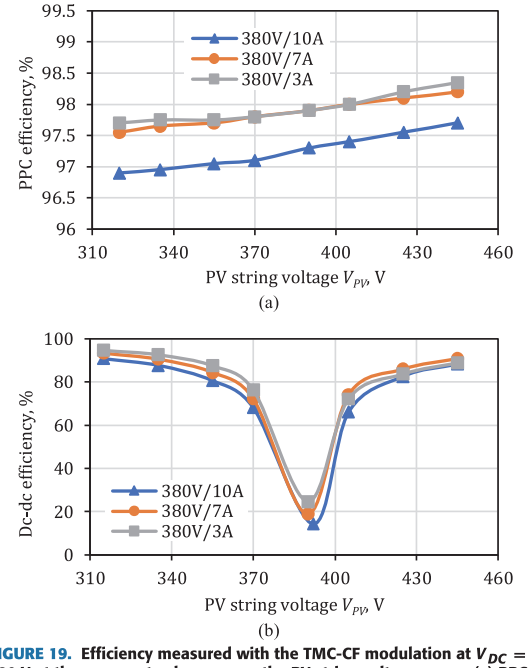

FIGURE 19. Efficiency measured with the TMC-CF modulation at V_{DC} = 380 V at three current values across the PV string voltage range: (a) PPC and (b) dc-dc efficiency.

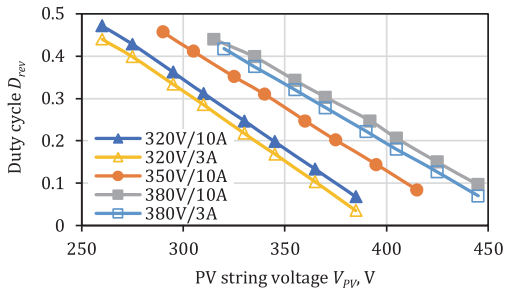

FIGURE 20. Experimental t_{REV} duty cycle of the TMC-CF modulation plotted for five test conditions across the PV string voltage range.

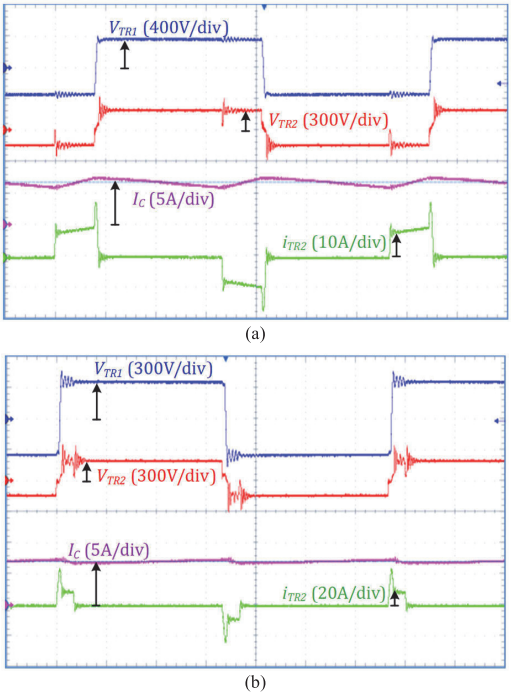

FIGURE 21. Experimental waveforms measured with the baseline modulation at the nominal dc microgrid voltage $V_{DC} = 350$ V and PV current of 7 A in (a) the step-up mode at $V_{PV} = 330$ V and (b) the step-down mode at $V_{PV} = 370$ V.

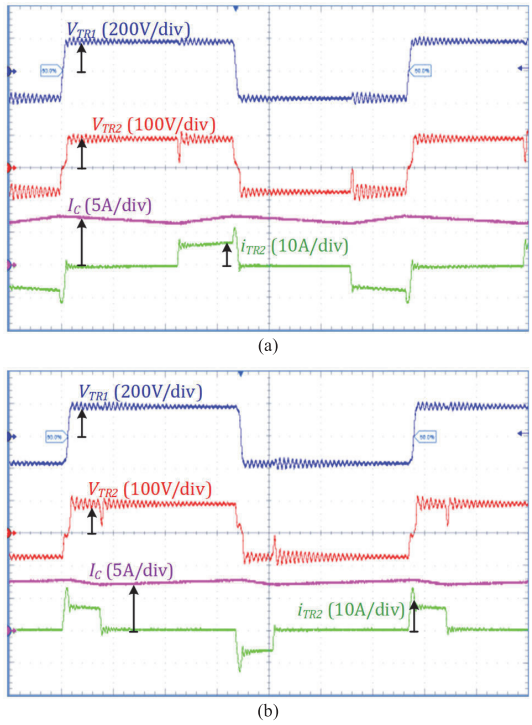

FIGURE 22. Experimental waveforms measured with the TMC-VF modulation at the nominal dc microgrid voltage $V_{DC} = 350$ V and PV current of 7 A in (a) the step-up mode at $V_{PV} = 330$ V and (b) the step-down mode at $V_{PV} = 370$ V.

First, the most obvious difference is in the swing of the voltage v_{TR2} between the baseline and TMC-VF modulations. As expected, the reduced voltage swing of the TMC-VF modulation causes, consequently, lower losses in the transformer core but higher losses in the transformer windings due to their higher RMS current. The baseline modulation features a high peak current in the transformer during the resonant soft-switching of the VF-side transistors, resulting from the higher voltage swing applied to the transformer winding. This phenomenon causes low efficiency of the baseline modulation at low loads.

The forward (from the CF to the VF side) and reverse energy transfer processes are clearly visible in the case of the TMC-CF modulation in Fig. 23. The reverse energy transfer interval is longer in the step-up mode and shorter in the step-down mode. This circulating energy results in high conduction losses in the components. Moreover, the effective operating frequency of the inductor L is equal to the switching frequency, which is twice as low as that of the other two modulations. This is caused by inductor charging only once a period, which happens at a much higher current slope resulting from the energy transfer from the VF to the CF side. As a result, the TMC-CF features a significant current ripple in the inductor L, which imposes a risk of high ac losses in the inductor windings.

The three modulations considered in this study could be compared in the V_C region of ± 60 V. Values of the efficiency difference between the TMC modulations and the baseline modulation are quantified in Fig. 24. TMC-VF always provides some increase in the PPC efficiency, which is more prominent in the step-down mode. In the step-down mode, the RMS currents are lower, which assists this increase in efficiency. In general, it features an efficiency trend similar to that of the baseline modulation. Considering their close

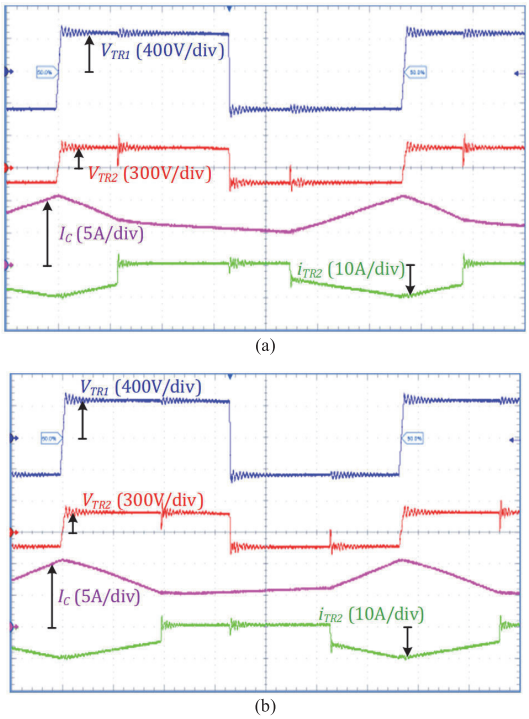

FIGURE 23. Experimental waveforms measured with the TMC-CF modulation at the nominal dc microgrid voltage $V_{DC} = 350$ V and PV current of 7 A in (a) the step-up mode at $V_{PV} = 330$ V and (b) the step-down mode at $V_{PV} = 370$ V.

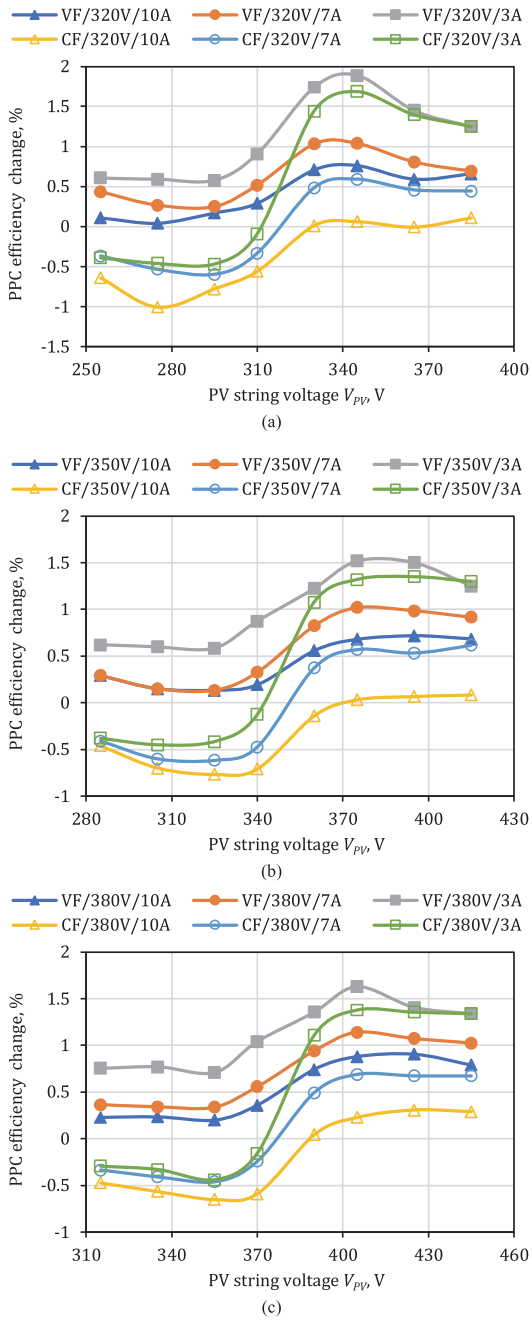

FIGURE 24. Experimental efficiency difference caused by the application of the TMC in the FV and the CF sides measured for three PV currents (3 A, 7 A, and 10 A) at three voltages of the dc microgrid: (a) 320 V, (b) 350 V, and (c) 380 V.

relations, both baseline and TMC-VF modulations demonstrate very similar voltage/current waveforms.

As expected, the TMC-CF modulation performs worse than the TMC-VF. It causes up to 1% of PPC efficiency drop in the step-up mode due to high circulating energy levels. This issue is diminished in the step-down mode, resulting in up to 1.7% efficiency improvement. Nevertheless, its performance regarding PPC efficiency is worse than TMC-VF can provide. Hence, the TMC-CF should be avoided in applications where efficiency is paramount. However, it will find its applications where high regulation performance near zero voltage at the series PPC port is required, even at the expense of a small drop in efficiency. Such an application could be a drooped-controlled battery energy storage, where small voltage variations cause sizable current variations.

Maximum power point tracking (MPPT) was implemented to demonstrate the benefits of TMC-CF modulation in terms of voltage regulation, as shown in Fig. 25 (a). In practice, the converter pre-charges the series capacitance to the maximum voltage difference and then initiates MPPT operation, as shown in Fig. 25 (b). A solar array simulator, Chroma 62150H-1000S, implemented synthetic tests with rapid changes in equivalent PV cell temperature (*Temp*) to achieve fast changes in the maximum power point voltage of a PV string at around 350 V. TMC-CF modulation enables MPPT with a smooth transition through the zero partiality

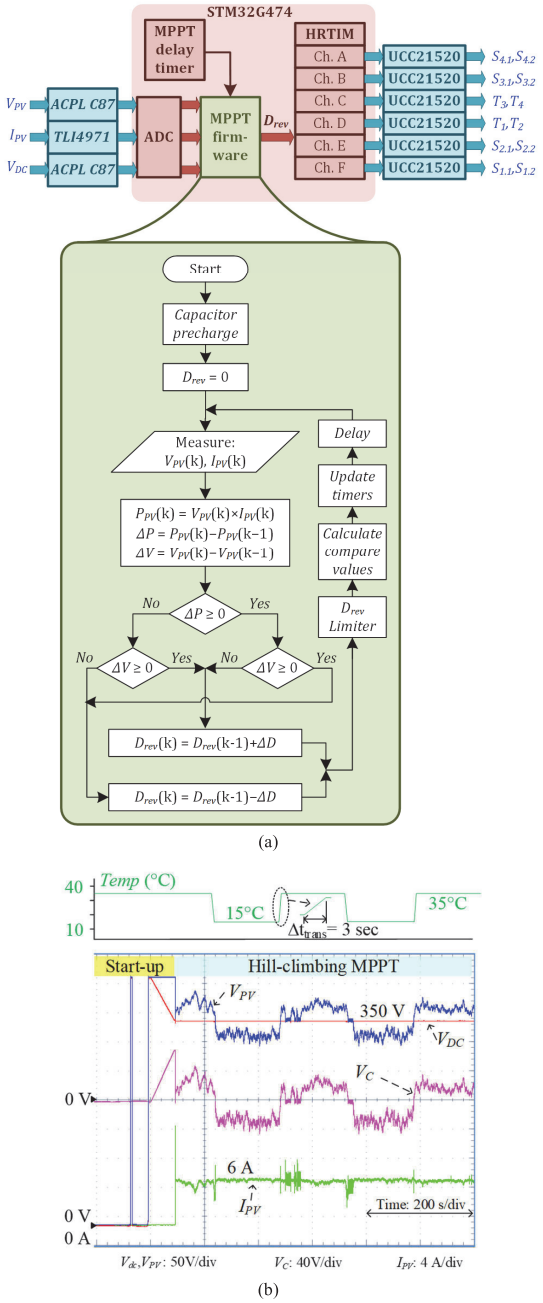

FIGURE 25. PPC operation with TMC-CF modulation: (a) implementation of the hill-climbing MPPT, and (b) PPC start-up and MPPT routine.

region, providing MPPT efficiency of roughly 99%. Six channels of high-resolution timer HRTIM was used for TMC-CF implementation, while generic embedded times defined the delay between MPPT perturbations. Used MOSFET drivers and current/voltage sensors are also indicated in the figure.

V. CONCLUSION

This study provides a comprehensive modeling of possible PV string configurations composed of 54-, 60-, and 66-cell PV modules, considering both hot and cold climates. It shows that a wide selection of available residential PV modules allows for restricting the PV string voltage range from 250 V to 450 V. At least 14 PV string configurations could fit this MPP voltage window. They range from 3 kW to 6 kW, covering the majority of residential rooftop installations. Combining this voltage range with the droop-control voltage range of ±30 V used in typical residential dc microgrids makes it possible to draw application requirements for partial power interface converters for PV string integrations in dc microgrids. Such an analysis has not been performed before. It yields that step-up/down PPC should be capable of operating in the ±130 V range of the series port and rated for 1.6 kW to cover the majority of residential rooftop PV string use cases. Such a PPC can perform best if its parallel port is connected to a dc microgrid.

A PPC was prototyped according to the derived application requirements. It achieves a peak efficiency of 99%. Nevertheless, its overall efficiency across the studied operating conditions is limited due to operating with relatively high partiality, i.e., the share of the active power processed by the isolated dc-dc cell. Recent research shows that topology morphing control can improve the performance of galvanically isolated dc-dc converters. It was proposed that PPCs could also benefit from this technique.

The applicability of the topology morphing control in PPCs was demonstrated in this study for the first time. Two topology morphing control techniques have been proposed to enhance the PPC efficiency in the ±60 V range of the series port voltage. The efficiency of the given PPC was improved by up to 1.9%. The case-study topology features soft switching of all semiconductor components, and efficiency improvement is associated with reduced conduction power losses.

Other PPC topologies and configurations should be studied regarding their feasibility according to the synthesized application requirements and applicability of the topology morphing control.

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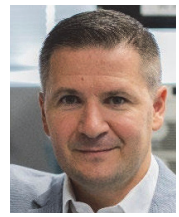

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Publication V

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Protection and Control Implementation for Bidirectional Step-Up/Down Partial Power Converter for Droop-Controlled DC Microgrids

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***Abstract*— Partial power converters enable the implementation of highly efficient dc-dc energy conversion systems. Step-up/down partial power converters show the highest potential for improving power density, efficiency, and implementation cost. Recent literature clearly shows that the most flexible implementations of these converters are based on galvanically isolated current-fed dc-dc converter topologies. On the other hand, these topologies are prone to overvoltage on semiconductors and can have poor current controllability at zero voltage in the series port. In practice, these partial power converters must implement multimode control, soft start, and protection of partial-voltage-rated semiconductors. This paper demonstrates these issues in a partial power converter and proposes implementation techniques to resolve them. The experimental verification demonstrates the effectiveness of the proposed techniques, suggesting that the partial power converters could be brought to industrial use.**

***Index Terms*— dc-dc converter, partial power converter (PPC), over-voltage protection, over current protection, open circuit protection, short circuit protection, soft start, under voltage protection.**

I. Introduction

RECENT research highlights that the residential sector is responsible for over 40% of global energy consumption and CO_2 emissions, making it a critical area for addressing climate change and reducing environmental impact. As a result, governments and international bodies are taking significant steps to mitigate the carbon footprint of the economic sectors using different measures, among which electrification is the most promising example [1]. In particular, the European Union (EU) has introduced ambitious regulations to steer the built environment towards zero-emission buildings by 2030 [2]. This initiative encompasses constructing new, energy-efficient buildings and retrofitting existing structures, with the ultimate goal of achieving climate neutrality by 2050 [3], [4]. Retrofitting older buildings is especially important, as the existing building stock is largely energy-inefficient and significantly contributes to emissions.

DC microgrids can reduce energy losses associated with multiple conversion stages, as conventional power systems experience up to 80% of their losses due to energy conversion processes [5]. Power electronic converters, especially dc-dc converters, play a crucial role in this transition [6]. These converters are essential components in various emerging energy technologies and applications that help reduce reliance on traditional energy sources. For instance, photovoltaic (PV) energy systems rely on dc-dc converters to optimize energy conversion and distribution. Similarly, battery energy storage systems (BESSs) require these converters to manage the charging and discharging processes efficiently, enabling better self-consumption of renewable energy generated on-site. Additionally, dc-dc converters are fundamental in LED drivers, improving energy efficiency in lighting systems, and in various household appliances such as heat pumps, which are becoming more energy-efficient because of advancements in power electronics [7]-[9]. The rising demand for dc-dc converters has driven significant research aimed at enhancing their performance. Key priorities include improving efficiency, reliability, and power density while reducing their costs. These advancements are making dc-dc converters more accessible for residential and industrial use. As sustainable energy solutions gain momentum, dc-dc converters become integral in various applications, including renewable energy systems [10].

Dc-dc converters could be broken down into full power converters (FPC) and partial power converters (PPC). FPCs handle the entire active power transfer between input and output, with their key performance indicators like efficiency, power density, and reliability matured over time [11]. As FPCs have reached the technological limits of their performance levels, PPCs attracted the attention of researchers to further improve system efficiency without increasing complexity or cost. Unlike FPCs, PPCs are designed to process only a portion of the total active power between input and output, allowing a significant amount of energy to bypass the converter along a nearly lossless path [12]. By minimizing the amount of processed power, PPCs can significantly reduce energy losses, thereby improving overall system efficiency.

Additionally, PPCs handle less power, enabling a more compact and power-dense design while utilizing conventional dc-dc topologies. This design approach avoids significant modifications to the converter's topology or modulation strategies, keeping the system relatively simple while delivering improved performance. PPC technology significantly benefits applications requiring high efficiency, reduced losses, and increased power density. Their high performance was previously justified for renewable energy and battery storage systems, offering improved performance

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without added complexity, making it a promising solution for future power electronics [13]. Current noticeable applications of PPCs are electric vehicles charging with power up to 300 kW [14], BESS applications [15]-[19] and connecting PV strings to inverters [20]-[23].

Despite the growing interest in PPCs, literature often overlooks the crucial aspect of system reliability, which can be significantly affected by unexpected fault events or practical issues. This oversight is particularly important because the series connection of input and output in these converters negates galvanic isolation, meaning they have no electrical separation. As a result, implementing precise protection measures becomes essential to safeguard the system against faults and ensure consistent operation. Moreover, while much of the literature highlights the advantages of step-up/down PPCs over traditional step-up or step-down converters, such as lower processing power requirements and higher efficiency, a notable gap exists in discussing the transition between these conversion modes [23]. The transition of the modes of PPCs, as shown in [20], can be critical, as it can introduce unique implementation challenges that may impact overall performance and reliability. Addressing these concerns is vital for the continued advancement of PPC technology in practical application, ensuring its benefits are fully realized in real-world systems.

An attempt to address practical implementation issues, such as the short-circuit (SC) and open-circuit (OC) faults in the PPCs, has been reported in [24]. The next steps were undertaken to demonstrate the implementations of droop control and protection algorithms in [24], [25]. This paper builds upon droop control implementation principles given in [25] and analyzes practical implementation issues, such as protection algorithms, based on the findings of [24]. Consequently, this paper thoroughly investigates and experimentally verifies various fault events that can occur in PPCs, particularly focusing on SC and OC faults. These faults can severely impact the reliability and performance of the system, so the paper not only identifies these potential issues but also proposes solutions that mitigate their effects. In addition to fault analysis, the paper addresses practical problems associated with converter mode change transients when the system shifts between step-up and step-down modes. These transients can introduce unique challenges, and the paper provides targeted solutions to manage these issues effectively. This paper also addresses the protection mechanisms for the PPC against under-voltage (UV), over-voltage (OV), and over-current (OCR) conditions.

The remaining sections are arranged as follows. Section II identifies the case study step-up/down PPC system. Next, Section III analyses associated faults and their potential consequences on system performance. This analysis offers insights into how protection issues impact operation, reliability, and efficiency if the system is designed for improved preparedness and response. Section IV presents simulation results that validate the proposed fault management and mode change transients handling methods, demonstrating their effectiveness across various scenarios. Section V presents the experimental validation of addressed problems and proposed solutions on an optimized PPC prototype. Finally, Section VI summarizes the key findings

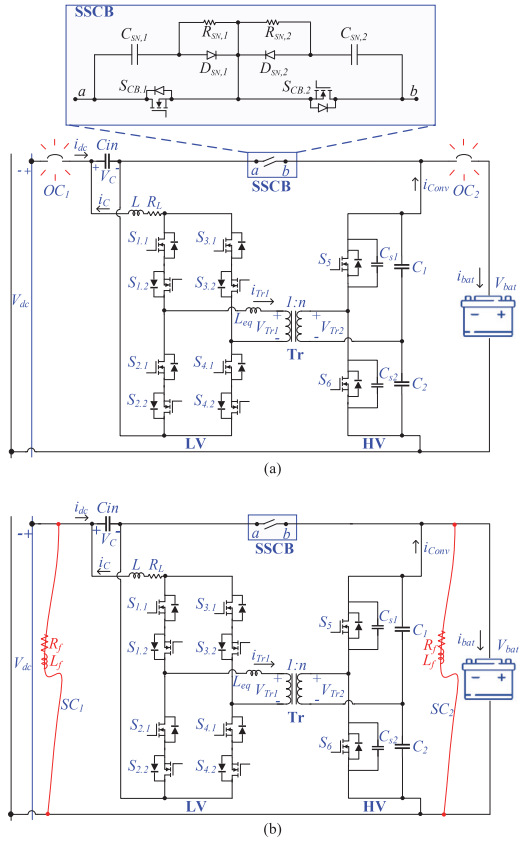

Fig. 1. Bidirectional step-up/down partial power converter with (a) OC faults and (b) SC faults.

and conclusions, emphasizing the importance of addressing fault events and mode change transient challenges in the design of partial power converters.

II. System Description

The bidirectional step-up/down partial power converter (PPC) is designed using a full-bridge current-source dc-dc converter at its core. This architecture provides flexibility in handling both step-up and -down voltage regulation operations, making it highly versatile in applications requiring bidirectional power flow. Detailed analysis of its various operational modes, topological configurations, and modulations can be found in [26]-[28].

Step-up/down PPCs demonstrate a more compact design, as the power-handling components can be downsized, leading to a more cost-effective solution and a lighter and more space-efficient converter. Moreover, the step-up/down PPC architecture further optimizes its performance, offering enhanced power density and improved scalability in multi-converter systems. This arrangement allows for parallel power processing at the input stage, which can be especially beneficial in applications where power sources with varying voltage levels need to be integrated or where energy storage systems are employed. The series connection at the output ensures that the desired voltage levels are maintained while distributing power more

TABLE I
PARAMETERS AND COMPONENTS OF THE EXPERIMENTAL PROTOTYPE

Component/Parameter	Symbol	Type/Value
HV Port Switches	S_5, S_6	G3R60MT07J
LV port switches	$S_{1,1}$ - $S_{4,2}$	BSC0403NS
SSCB switches	S_a, S_b	UF3SC065030B7S
Main inductor	L	CPER3231-820MC (2x82µH)
Transformer core	-	2 x EE42/21/15
Main transformer turns ratio	n_m	2.375:1
Main transformer leakage inductance	$L_{eq,m}$	1.2µH
Snubber transformer core	-	EILP32
Snubber transformer turns ratio	n_{sn}	2.22:1
Snubber transformer leakage inductance	$L_{eq,sn}$	350nH
Snubber diodes	D	STPSC2H065B-TR
RC snubber	-	50Ω – 2.1nF
HV port capacitors	C_1=C_2	R60IR51005040K / ECA2EHG100 (10‖10 = 20 µF)
HV port snubber capacitors	C_s	1.1 nF
Series capacitor	C	DCP4G056007GD4KSSD (60µF)

efficiently across multiple nodes. The architecture of PPC is depicted in Fig. 1, which illustrates the key elements. The parameters and components of the experimental prototype can be found in Table I.

As a result, the switching devices associated with the parallel, or high voltage (HV), port of the PPC typically handle only a small fraction of the total current, usually less than 20% of the overall current flow [33]. This significantly reduces the stress on these components, allowing for smaller, lower-rated devices to improve efficiency and reduce power losses. Since the HV port devices are responsible for processing only a portion of the power, they experience less wear out, which can enhance the reliability and longevity of the converter system. Additionally, the components in the series, or low voltage (LV), port experience reduced voltage stress, which is determined by the voltage difference between the input and output ports. This lower voltage stress allows for selecting components with lower voltage ratings, which are generally less expensive and more readily available. The combination of low current in the parallel port and reduced voltage stress in the series port means that components with lower current and voltage ratings can be used in the LV and HV ports of the converter, respectively.

III. POSSIBLE FAULTS FOR PPC

In conventional converter designs, severely overrated components are often used to achieve robustness to higher stresses, ensuring the system remains operational even under adverse conditions. This typically involves using components with higher voltage and current ratings than required for normal operation, providing a safety margin to mitigate the risk of converter failure. However, this approach is counterproductive when applied to PPCs. Overdesigning the components in a PPC reduces efficiency and negates the core benefit of the PPC technology – high efficiency. Nevertheless, many PPCs in the literature adopt high-voltage-rated components to enhance reliability under extreme conditions, as highlighted in [30]-[32]. This practice diminishes the inherent advantages of PPC technology, such as improved efficiency and compactness, since using full-

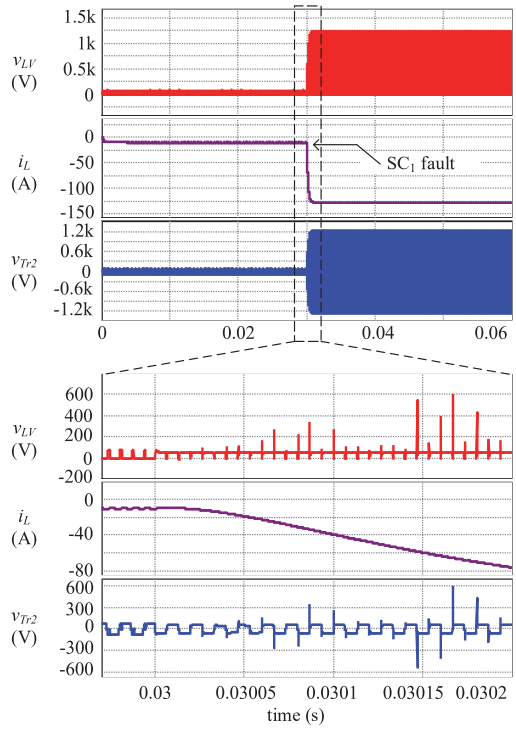

Fig. 2. Short circuit fault at input side (SC$_1$), during which the LV port voltage, inductor current, and transformer LV side voltage are shown.

voltage-rated components increase cost, size, and complexity. Therefore, rather than relying on overdesign, a more effective approach is to implement protection strategies that ensure safe PPC turn-off under faulty conditions. By employing this, PPCs can maintain their inherent benefits while still achieving reliability under adverse conditions.

To address these challenges, it becomes essential to implement adequate protection strategies to safeguard the converter during faulty conditions without overengineering its components. By focusing on ensuring safe operation with partial-voltage/current-rated devices, the system can still maintain the advantages of the PPC. These protection strategies must be designed to detect and respond to faults quickly and effectively, preventing catastrophic failure while preserving the converter's core functions. The ultimate goal of these protection mechanisms is to ensure the safety and functionality of the PPC regardless of input and output conditions, allowing the converter to operate dafely even when faced with fluctuating or adverse electrical environments. By doing so, the PPC can maintain its merits while ensuring reliable performance under various operating conditions.

A. Short Circuit (SC) Fault

Fig. 1 illustrates SC faults, labeled SC$_1$ and SC$_2$, on both the input and output sides of the given PPC. To account for the impact of the SC, it is modeled with an impedance comprising a 0.5 Ω resistance and a 0.5 µH inductance in series. Fig. 2 further demonstrates how the inductor current (i_L=i_C), LV series port voltage (V_{LV}=V_C), and transformer winding voltage (V_{Tr2}) behave under these conditions. During

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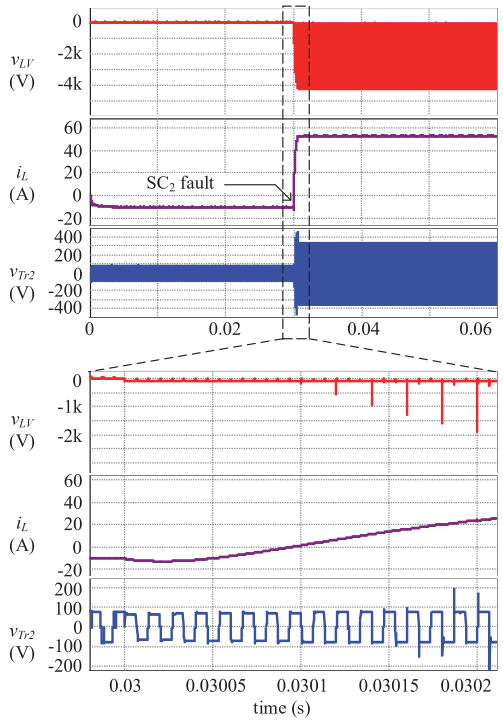

Fig. 3. LV port voltage, inductor current, and transformer LV side voltage during the short circuit fault at output side (SC$_2$) showing.

SC fault, the i_L increases and eventually peaks, but this is limited by the short circuit impedance and the equivalent series resistance (ESR) of the system components. It is worth noting that the PPC normally operates under soft-switching, specifically zero current switching (ZCS) in the LV port, during standard operation with maximum output current. This mode ensures efficient switching and minimal losses, as discussed in detail in reference [26]. However, when the output current is increased, the system is forced out of its soft-switching regime. In such cases, switching large inductive currents can lead to significant voltage spikes across the switches. Voltage spikes result from the rapid current changes (high di/dt) impacting the parasitic inductances.

These high voltage spikes create a significant risk of damaging the LV-port MOSFETs. When exposed to such spikes, the MOSFETs can experience breakdowns, leading to potential failures that could disrupt or completely halt the operation of the power converter. This failure type affects system reliability and introduces the possibility of costly repairs and downtime. A similar response is observed when a fault occurs on the HV port of the power converter, labeled SC$_2$ in Fig. 1. In this case, the fault triggers a significant surge in voltage, affecting other parts of the system. The simulations presented in Fig. 3 clearly show the magnitude of these voltage spikes, which can reach levels much higher than the voltage rating of the LV port switches. Hence, SC protection is essential for PPC implementation to protect the switches from high inductor current (short circuit current), compromising inductor saturation and causing high voltage spikes.

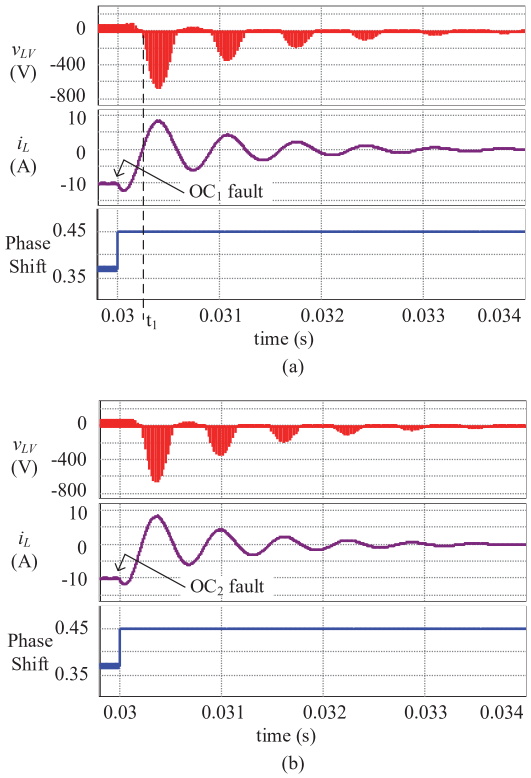

Fig. 4. Open circuit fault (a) at the input side (OC$_1$) and (b) the output side (OC$_2$) showing LV port voltage and inductor current.

B. Open Circuit (OC) Fault

Open circuit faults, much like SC faults, can occur on either the input or output sides of the PPC, referred to as OC$_1$ and OC$_2$ in Fig. 1. When such faults arise at both the input and output sides, a notable challenge emerges in oscillations at the LV port between the inductor (L) and capacitor (C). These oscillations can negatively impact the converter by creating voltage spikes across the LV port switches, possibly leading to switch breakdown. This issue is mainly linked to the PPC operating in a specific mode chosen from six possible modulation schemes, as referenced in [25]. All modulation schemes depend on the inductor current direction, and reversing it would result in voltage spikes on LV transistors. Hence, parasitic oscillations resulting in current i_L direction reversal cause interruption of the inductor current by PWM switching in the LV port, leading to voltage spikes.

This current flow disruption occurs due to the PWM applied to the LV port switches, interrupting the current, causing voltage surges. Therefore, managing these oscillations and ensuring proper protection against open circuit faults is crucial to prevent damage to the converter, particularly to avoid catastrophic switch failures due to excessive voltage stress.

This phenomenon is illustrated in Fig. 4(a), which depicts the behavior during OC$_1$ fault. After the fault occurs, there is a noticeable oscillation in the i_L, specifically when the current transitions from a negative to a positive value (at t$_1$ in Fig. 4(a)), and voltage spikes become apparent across the LV port.

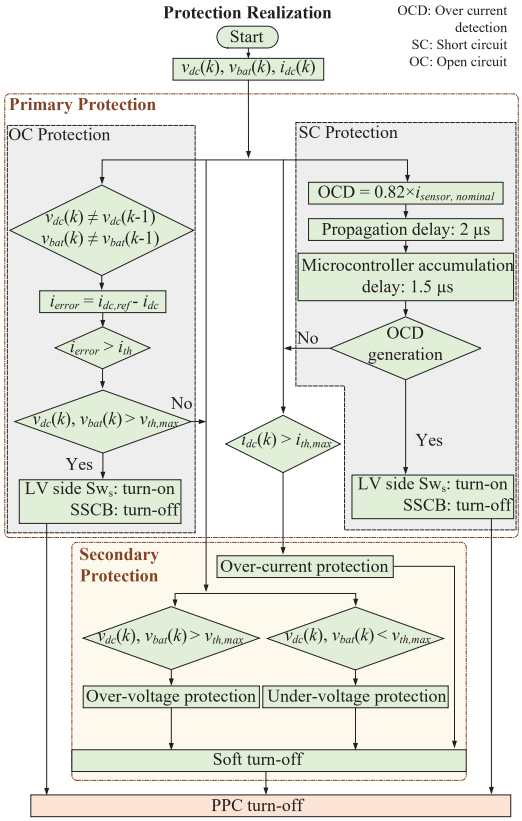

Fig. 5. PPC protection approach against SCs, OCs, over-currents, over-voltages, and under-voltages.

These spikes are particularly visible in the v_{LV} waveform. Simultaneously, the phase shift between the top and bottom switches of the LV port saturates at its maximum value. The conventional control, essential for regulating power flow and switch safety, becomes ineffective as it saturates, preventing further adjustment to mitigate voltage spikes. As a result, the risk of damage to the PPC components is imminent. A similar response can also be observed during OC_2 fault at the output side as shown in Fig. 4(b).

IV. Proposed Protection Method

This paper proposes effective and practical solutions to protect the PPC from SC and OC faults, which do not interfere with implementing the primary droop control.

A. Short Circuit Fault Clearance

Implementing a solid-state circuit breaker (SSCB) is essential for rapidly interrupting fault current and protecting the converter ports from overvoltages. SSCB can react within a few microseconds to prevent damage to sensitive components. Fig. 1 shows the SSCB configuration, which features two MOSFETs arranged in a back-to-back configuration, allowing for current flow in both directions, making it suitable for bidirectional dc applications [34]. The proposed SC fault protection methods are illustrated in Fig. 5 and are followed in the steps below.

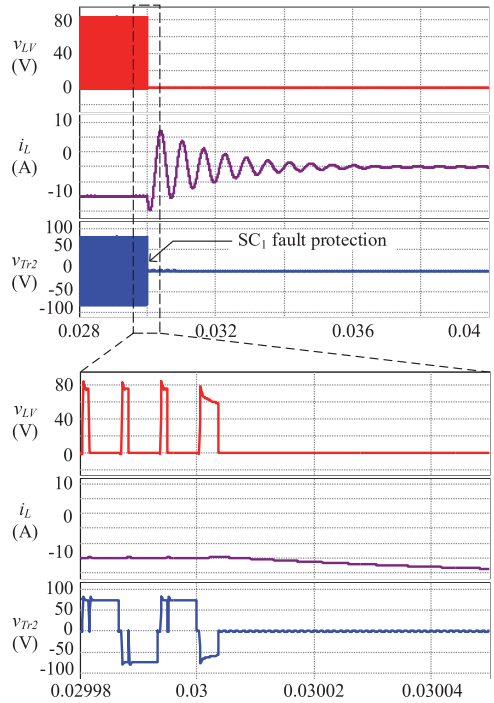

Fig. 6. Short circuit fault protection at input side (SC_1) showing LV port voltage, inductor current, and transformer LV side voltage.

Step 1: Data Acquisition from Current Sensor

A current sensor (Infineon TLI4971-A025T5-E0001) is integrated into the PPC for the series port current regulation, which is essentially the filtered inductor current. This sensor placement allows for the explicit regulation of current between two ports of the PPC. This sensor is essential for monitoring the current flow and ensuring it remains within safe operational limits. Real-time sensor data are used to maintain optimal performance and prevent damage from over-current conditions.

Step 2: Over-Current Detection

The TLI4971 sensor is equipped with over-current detection capabilities, which are used to initiate the protection strategy whenever necessary. This feature ensures that if the current exceeds predefined thresholds, the system can quickly respond to mitigate potential risks.

Step 3: Signal Generation and Timing

The next action is to generate a fast over-current signal (OCD) that activates at 0.82 of the nominal current (pre-programmed by the manufacturer). In this case, with a nominal current rating of 25 A, the over-current threshold is calculated as 0.82 × 25 A, resulting in 20.5 A. Once this threshold is exceeded, an SC fault operation is recognized, as the sensor will produce an over-current signal within a maximum of 2 µs.

Step 4: Connection to Microcontroller Delay

This prototype is designed to trigger an external interrupt event in a microcontroller (STM32G474VET6) as quickly as possible. By linking the sensor output directly to the microcontroller, the system ensures that it can respond to

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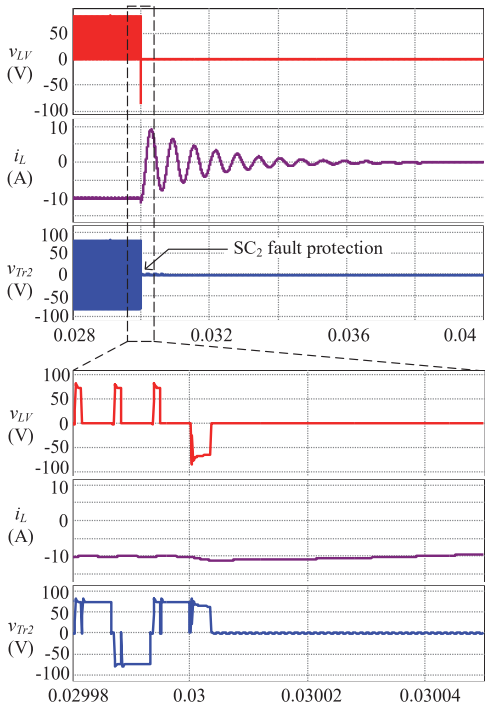

Fig. 7. Short circuit fault protection at output side (SC$_2$) showing LV port voltage, inductor current, and transformer LV side voltage.

over-current situations almost instantaneously, thereby enhancing the effectiveness of the proposed protection strategy. Effective fault management requires accounting for accumulated delays within the microcontroller and switch drivers. An additional delay of 1.5 µs is added to the initial sensor response time of 2 µs, resulting in a total delay of up to 3.5 µs before the protection routine is activated after a fault is detected. This response time is crucial for the reliability of the current-regulating system, enabling swift protective actions to safeguard the PPC from over-current damage.

Step 5: Trigger Fault Diagnosis

In addition to the action of SSCB interrupting the fault current, it is essential for the LV port switches must stop PWM operation and allow current flow to prevent voltage spikes. Therefore, the switches ($S_{1.1}$ - $S_{4.2}$) will be activated simultaneously upon receiving the turn-off command from the SSCB. As a result, after the SSCB disconnects and all the LV port switches are turned on, inductor-capacitor voltage-current oscillations are expected to occur within a series RLC circuit, which will be damped by the equivalent series resistance (ESR) of the components.

The SC fault protection simulation results are shown in Figs. 6 and 7 for the SC$_1$ and SC$_2$ faults, respectively. The fault clearance command sent to both the SSCB and the LV port switches effectively prevents voltage spikes across the LV port switches within approximately 25% of the switching cycle of the converter, given a switching frequency of 75 kHz. This fast and efficient fault protection is achieved by interrupting the current rise through the disconnected SSCB and turned-on LV port switches, causing parasitic resonance between the passive components. As a result, low-cost 150 V

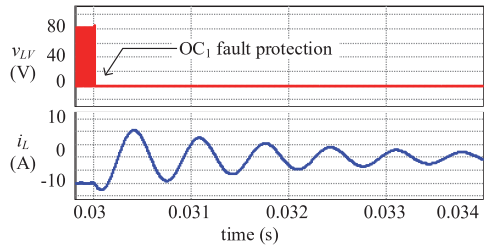

Fig. 8. Open circuit fault protection at the input side (OC$_1$) showing LV port voltage and inductor current.

Si MOSFETs with very low $R_{ds\text{-}on}$ can be used in the LV port, thereby optimizing the performance of the PPC.

B. Open Circuit Fault Clearance

During an OC fault, regulating either positive or negative current reference would result in voltage spikes caused by interrupting the inductor current i_L caused by the PWM operation of the LV port switches. Given that the parasitic oscillation frequency is approximately 1.6 kHz in the given prototype, which is determined based on the specific parameters of the converter, it becomes critically important to address and clear any faults within a very short time frame. Specifically, the fault must be cleared in less than half of one oscillation cycle, which equals roughly 312 µs. Therefore, the proposed OC protection approach is followed as below.

Step 1: Data Acquisition and Monitoring

First, the control system monitors system parameters such as i_{dc}, v_{dc}, and v_{bat} for any deviations or abnormal behavior during the operation of the converter. Also, it is acknowledged that an OC fault naturally interrupts the input-to-output current flow in the circuit.

Step 2: Analysis of Measured Signals

The next step is to compare the actual dc side current i_{dc} and reference current ($i_{dc,ref}$), considering that the reference current does not equal zero under normal operating conditions. In the case of an OC fault, the control system observes a significant difference between the measured current i_{dc} and the reference value $i_{dc,ref}$.

Step 3: Monitor Error Signal Fluctuations

The next step is to track the generated error signal (i_{error}). If this error signal becomes significant (i_{error} greater than i_{th}), it may indicate the presence of a fault. In this work, i_{th} is chosen as 10 A, which corresponds to relative error of 100% of the nominal current. A lower value can be selected if it corresponds to a significant relative error of the reference current tracking.

Step 4: Interpret Fault Conditions

The converging of two conditions (step 2 and step 3) should be interpreted as the occurrence of an OC fault.

Step 5: Trigger Fault Diagnosis

As the OC fault is detected, the protection routine is prioritized. As a result, the LV port switches are turned on continuously to reduce the overvoltages in the LV port caused by high di/dt through the inductor. After a while, the PPC enters a turn-off state when an RCD snubber in the SSCB dissipates the inductor energy. The result of the OC fault at the input side OC$_1$ is shown in Fig. 8.

V. Experimental Validation of the Proposed Protection Methods

To validate the proposed control-based protection approaches for a step-up/down PPC, an experimental prototype with a rated power of 4 kW (short overloads up to 5 kW) has been developed, as shown in Fig. 9. It comprises five boards: four power boards and one control board, allowing for flexible design, implementation, and maintenance. Thermal management is achieved using surface-mounted heatsinks attached to the MOSFET drain pads. Two bidirectional power supplies iTECH IT6000C emulate the battery and dc microgrid behavior. iTECH BSS2000 Pro software was used to emulate a battery pack.

OC and SC Fault Protection

The digital control board features an STM32G474 ARM Cortex-M4 microcontroller, capable of generating 12 PWM signals using six high-resolution dual-channel timers. This PPC prototype is tested under multiple SC and OC fault conditions. The developed control and protection methods easily distinguish the fault event from normal operation. Thus, the protection routine turns off the PPC appropriately to prevent it from being damaged by SC and OC faults. Fig. 10 shows the switching signals for LV and HV port MOSFETs along with the control signal for SSCB switches (*SSCB:* $S_{CB.2}$, *SSCB:* $S_{CB.2}$). The protection algorithm generates the trip signals for SSCB and stops the operation of LV port switches as an OC fault occurs at t_1 (as per flowchart shown in Fig. 5). As a result, the PPC is turned off safely.

Fig. 11 illustrates the current and voltages during the primary protection against OC_1. Before t_1, the PPC operates in normal step-down mode while v_{bat} and v_{dc} equal 335 V and 320 V, respectively, and $i_{dc} = 2$ A. When the OC_1 fault occurs at the instant t_1, the current i_{dc} drops to zero naturally. In this case, the i_{error} exceeds the i_{th} (set at 1 A). Hence, the protection sequence is executed rapidly, forcing the PPC to turn off. Consequently, the inductor current (related to i_{dc}) does not drop abruptly, avoiding overvoltages across LV switches. Thus, the PPC turns off safely during an OC fault.

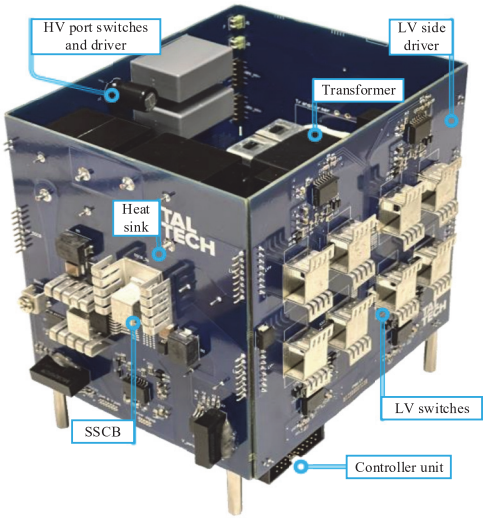

Fig. 9. 4 kW laboratory prototype of the step-up/down PPC.

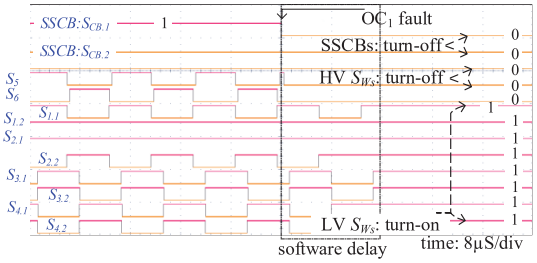

Fig. 10. Signal generation upon OC fault event.

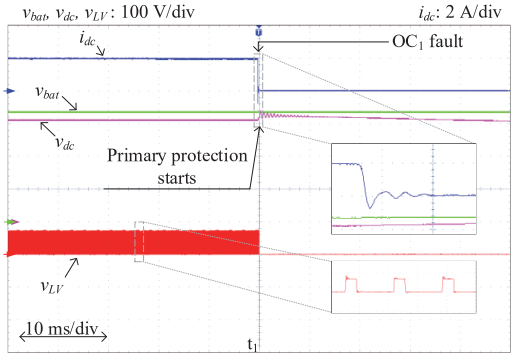

Fig. 11. Realization of primary protection during an OC fault (OC_1) at dc microgrid side.

This study also tested the secondary protection of the PPC to verify its effectiveness. Fig. 12 presents the case when the OC_1 fault is introduced at the instant t_1, and the primary OC protection is intentionally disabled to check the functionality of the secondary protection. The results show that the system switches to overvoltage protection when the primary protection fails. As the dc voltage (v_{dc}) exceeds the upper limit ($v_{dc,th,max} = 382$ V) a few seconds after the OC_1 fault, the PPC is turned off safely in the same manner at the instant t_2.

An SC fault protection realization is exhibited in Fig. 13. The PPC starts with normal operation where v_{dc} and v_{bat} are 320 V and 365 V, respectively. The SC_1 fault with fault resistance of $r_f = 16\ \Omega$ is introduced at the instant t_1 on the dc microgrid side. As the fault occurs, the current i_{dc} rises and reaches the maximum value of 150 A, defined by the value of r_f. When the i_{dc} crosses the OCD limit of 20.5 A (as per the sensor datasheet), the sensor generates the OCD signal (v_{OCD}), which can be observed in Fig. 13. It is worth mentioning here that the analog OCD signal and the digital OCD signal have some propagation delay. Considering the propagation and controller accumulation delay, the SC protection method turns off the PPC at t_2, 35 µs after the occurrence of the SC_1 fault. The low port voltage V_{LV} clearly shows that the LV port switches do not experience overvoltages across them, proving the effectiveness of the proposed control implementation techniques.

Fast and efficient fault protection is thus achieved by interrupting the rising current through SSCB disconnection and changing the PWM operation of the LV port switches to the continuous turn-on state. This creates a freewheeling path, allowing the inductor current to oscillate with the capacitor. As a result, low-cost 150 V MOSFETs with very low $R_{ds\text{-}on}$ and reverse recovery charge can be used in the LV port,

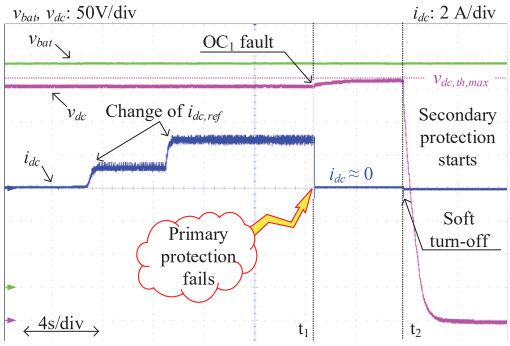

Fig. 12. Implementation of secondary protection for v_{dc}=350 V, v_{bat}=335, and i_{dc}=3 A.

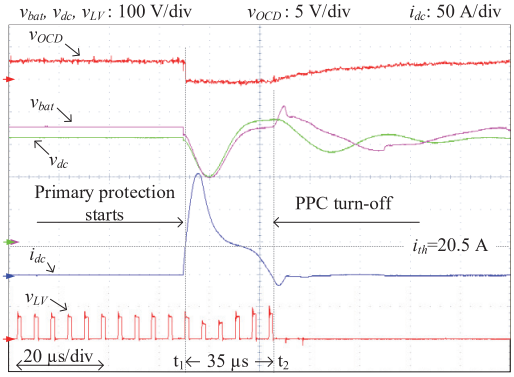

Fig. 13. Realization of primary protection during an SC fault (SC$_1$) at dc microgrid side.

enhancing the overall performance of the PPC. The experimental results demonstrate the effectiveness of the proposed SC and OC fault protection methods.

Soft Mode Transitions

The PPC operates as a four-quadrant dc-dc converter, where its performance is governed by the LV port current (i_{dc}) and voltage (v_{LV}). In different quadrants (Q$_{\rm I}$-Q$_{\rm IV}$), phase shift modulation (PSM) is typically used to regulate the system. However, in the Q$_{\rm II}$ and Q$_{\rm IV}$, PSM faces constraints, prompting the implementation of the flyback secondary modulated conversion (FBK-SMC) technique that uses circulating energy to control the inductor current. As a result, the converter operates in all quadrants properly, especially when the series voltage is zero, as noted in [25]. Fig. 14 exhibits the diagram of the mode/modulation selection and control structure of the PPC. The sign of reference current defines the current flow direction, while the operating quadrant is defined by the sign of the voltage difference (v_C) between input and output. If the current or voltage changes polarity, the converter shifts quadrants, requiring a new modulation for the switches.

To validate the dynamic functionality of PPC under the droop control curve, three tests were performed at battery voltages (v_{bat}) of 335 V, 350 V, and 365 V [35]. In Fig. 15, at 335 V, the PPC starts in the Q$_{\rm II}$ (discharge) during t_0-t_2. At t_1, as the dc voltage starts changing, the controller operates in droop control mode. As the v_{dc} increases, reaching a threshold

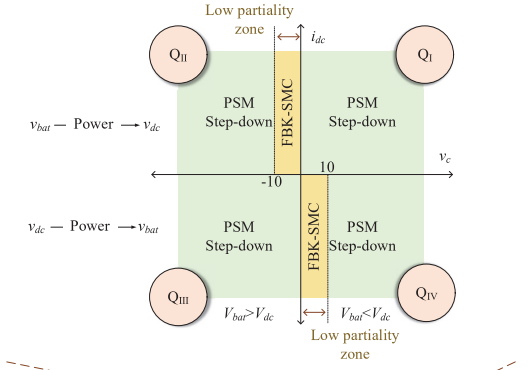

Fig. 14. Mode selection and control structure of PPC.

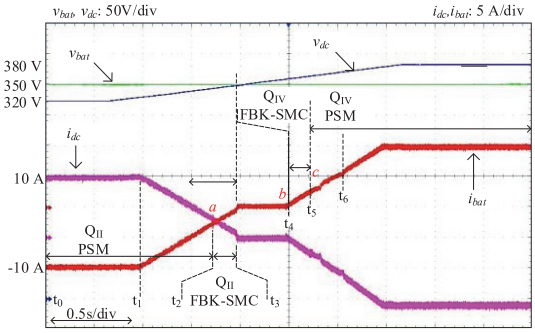

Fig. 15. PPC operating with current droop control for battery v_{bat} = 350 V and influence of the mode change transients.

($|v_c|$ < 10 V) at t_3, the operating mode shifts to Q$_{\rm II}$ with FBK-SMC (discharge) modulation, turning S_4 on and S_2 off continuously. During t_4-t_5, between 350 V and 355 V, all switches except the SSCB are turned off. At t_5, the PPC enters into Q$_{\rm IV}$ (charge) with FBK-SMC modulation. Later, at t_6, for 360 V < v_{dc} < 380 V, the PPC operates in the Q$_{\rm IV}$ (charge) with PSM. A practical challenge occurs during these shifts, as the microcontroller cannot instantly apply the new modulation.

The points where modes change, marked as *a*, *b* and *c* in Fig. 15, highlight the transients. Applying the required modulation takes 2-3 switching cycles, while the PWM signals cannot be controlled or predicted. An incorrect switching state can cause an SC across HV port capacitors via the transformer and LV switches, triggered by unintended activation of all LV side switches. As shown in Fig. 16, the inrush current is limited by leakage inductance, transformer resistance, and $R_{ds\text{-}on}$ of an HV MOSFET (less than 400 mΩ). This forbidden PWM state was faced frequently during the initial experimental tests. For example, Fig. 17 shows that the switch current $i_{S1.1}$ reaches over 400 A during mode change at t_1, potentially damaging this switch.

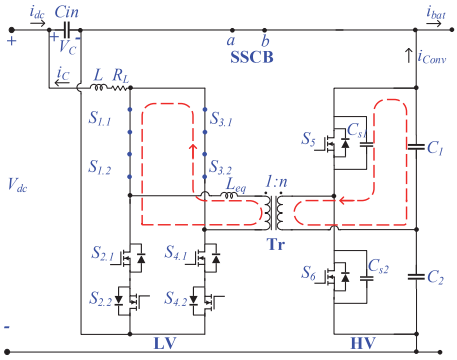

Fig. 16. Inrush current flowing through $S_{1.1}$ and transformer voltage during mode change transients when PWM is stuck in a forbidden state.

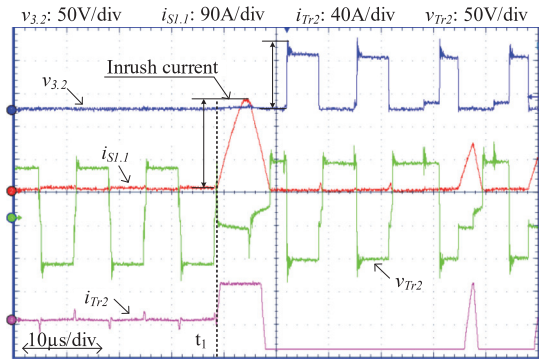

Fig. 17. Inrush current flowing through $S_{1.1}$ and transformer voltage during mode change.

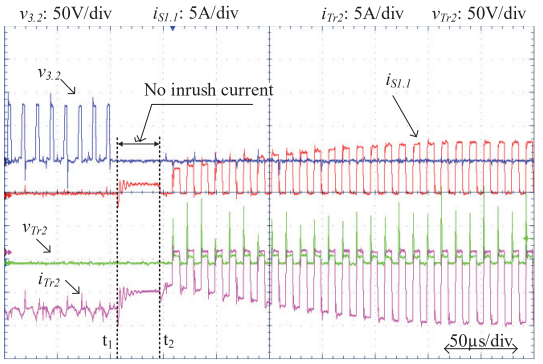

Fig. 18. Mitigation of inrush current during mode change transients.

Considering that the converter performance deteriorates significantly during such uncontrolled mode change transients, this paper also proposes a solution to overcome this and prevent damaging the LV semiconductor devices. To address inrush current during mode change transients, the HV port switches must be turned off while all LV port switches are turned on simultaneously. This allows for the dc side current i_{dc} flow without the need for active control. During this mode transition, the inductor current i_C is expected to reduce/increase by several magnitudes of its current ripple amplitude. With an inductor current ripple of around 0.3 A, the resulting decrease of 0.6 A in the dc side current i_{dc} (from a nominal 10 A) can be promptly managed by the PI controller after the new mode is activated. Also, this transient will be smoothed out by the capacitor C_{in}.

Fig. 18 proves that the proposed PWM signals blanking (t_1-t_2) effectively mitigates the inrush current in LV transistors during mode change transients. Hardware implementation required a monostable multivibrator, discrete logic, and a microcontroller triggering signal

VI. Conclusions

This paper highlights the implementation challenges of the step-up/down partial power converters. Special attention is paid to the short- and open-circuit faults at the input and output ports of the PPC. Without proper protection, the converter risks failure due to high voltage spikes at the LV port switches during faults. Microcontroller limitations also prevent instant switching pattern adjustments during PPC mode changes, causing forbidden PWM signals and associated inrush current in LV port switches. This paper also addresses these issues in the case study of partial power converter and suggests implementation techniques to resolve them.

The paper proposes fault detection using a current sensor with a 2 µs reaction delay and control variable monitoring. Fault clearance involves disconnecting the SSCB after 1.5 µs for short circuits and activating LV port switches after 25 µs for open circuits. The developed PPC prototype demonstrates stable and safe operation during faults.

High inrush currents in semiconductor components and the transformer were observed during mode/quadrant change transients. The main cause of this issue is circulating energy caused by PWM signals getting stuck in a forbidden state for several switching cycles during the mode change transients. A simple circuit employing a triggering signal from the microcontroller, a monostable multivibrator, and discrete logic components fully resolved this issue. This approach ensures smooth transitions between modes, preventing component faults. Experimental verification of these techniques confirms their effectiveness, showing that they successfully mitigate the identified issues. As a result, the proposed control system implementation enhances the reliability and performance of partial power converters, indicating their potential for industrial applications.

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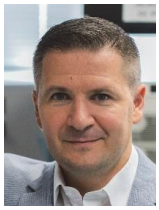

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High-Efficiency Partial Power Converter for Integration of Second-Life Battery Energy Storage Systems in DC Microgrids

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ABSTRACT This article presents a power electronic interface for battery energy storage integration into a dc microgrid. It is based on a partial power converter (PPC) employing a current-fed dc–dc topology. The article provides an analysis of application requirements and proposes an optimal second-life battery stack configuration to leverage all the benefits of the PPC technology. This converter can regulate current at zero series voltage between a battery stack and a dc microgrid using the topology morphing control. The article shows how the converter and its control system should be designed to operate in a droop-controlled dc microgrid. The experimental results demonstrate the converter's capability to operate under droop control, implementing both voltage step-up and -down regulation with a smooth transition between converter modes. The experimental efficiency reaches as high as 99.45%, demonstrating an efficient approach for second-life battery energy storage integration into dc microgrid.

INDEX TERMS Battery energy storage system (BESS), control, dc–dc converter, dc microgrid, partial power converter (PPC).

NOMENCLATURE

V_c	Series capacitor voltage.
V_{dc}	DC microgrid voltage.
V_b	Battery voltage.
I_c	Capacitor current.
I_{dc}	DC microgrid current.
G_{buck}	Voltage gain for buck mode.
G_{boost}	Voltage gain for boost mode.
t_{red}	Redistribution time.
φ_{buck}	Controlled phase shift for buck mode.
φ_{boost}	Controlled phase shift for boost mode.
f_{sw}	Switching frequency.
L_{eq}	Transformer leakage inductance.
D_{rev}	Control variable for flyback secondary modulated conversion.
n	Number of turns in the high-voltage side of the transformer.
V_{nom}	Nominal dc bus voltage.
R_{dr}	Droop coefficient.
$I_{dc,ref}$	DC bus reference current.
A_e	Effective cross-section of the core.
B_{max}	Maximum flux density.
Δi_L	Inductor current ripple.
V_{Tr}	Transformer voltage.
V_s	Switch voltage.

I. INTRODUCTION

Nowadays, buildings account for approximately 40% of carbon dioxide emissions globally. In response to this environmental impact, the EU Commission has enacted regulations mandating the transition toward zero-emission buildings (ZEBs) [1]. The interconnection of renewable energies, particularly photovoltaic (PV) panels installed on household rooftops, can facilitate a cost-optimal transition toward ZEBs

[2], [3]. Renewable energy resources and storage could be integrated using either a dc or an ac microgrid. Studies have demonstrated that implementing a dc microgrid can increase system efficiency by 15% due to removing the ac–dc conversion stages [4]. However, energy storage system (ESS) installation is unavoidable considering the rapid proliferation of renewable energy resources [5]. In order to improve the security, stability, and resilience of grid operations, utility-scale ESSs have emerged as a viable technology [6]. In [7], the economic viability of using battery storage as an energy source for a residential building was evaluated. Moreover, to improve PV self-consumption, Yu [8] presented a flexible load management model where second-life battery energy storage is designed.

The absence of an energy storage unit poses a significant challenge, as it hinders the ability to store excess energy generated during peak production periods and distribute it during periods of low or no generation. Its integration allows for effectively using renewable energy sources within a house, ensuring a reliable energy supply [9], [10], [11]. Implementation of a battery energy storage system (BESS) also offers a range of additional benefits, including providing sufficient inertia to stabilize the voltage profile of the dc microgrid [12], enabling peak power consumption shifting and energy arbitrage, and reducing distribution network losses through end-user self-consumption, especially during peak demand periods [13], [14]. However, the high capital cost of BESS (typically ranging from $250 to $300 per kWh) remains a major impediment to widespread installation in households [15], [16].

An alternative approach to address this cost challenge is the utilization of second-life electric vehicle (EV) batteries (SLBs). These batteries still retain 70%–80% residual capacity and, consequently, can reduce the capital cost by 15%–25%. Moreover, extending the battery utilization until the end of its life cycle can result in a total carbon emission reduction of 22%–51% [17]. This demonstrates the potential of repurposing EV batteries as a cost-effective and environmentally beneficial solution for residential energy storage. In terms of the battery technology, there can be different options, such as lithium cobalt oxide, lithium manganese oxide, lithium nickel manganese cobalt oxide (NMC), and lithium iron phosphate (LFP) [18].

The LFP technology offers several benefits, including improved safety and a reduced thermal runaway risk [19]. These batteries have a long expected life of more than 3000 discharge–charge cycles, and they possess high-power capability. It is argued that the shift of the EV industry toward LFP batteries makes a much stronger case for second-life applications compared to conventional NMC battery technology [20]. A key feature of LFP batteries is their consistently flat voltage profile, which persists even after degradation [21]. Nonetheless, the variability in the state of health among cells within a battery pack and the impedance mismatch between them make it impractical to use SLBs directly after disassembling from an EV [22]. Consequently, a cycle of observation based on specific criteria, including voltage analysis, residual capacity, and internal impedance analysis, is necessary. This systematic evaluation is crucial for selecting and repackaging suitable cells, ensuring their viability for installation in a household setting.

This article explores the integration of a second-life LFP battery into a dc microgrid using a partial power dc–dc converter (PPC) technology known for its notably high efficiency. This technology suits applications where galvanic isolation is not mandatory [23]. The PPCs presented in the literature often lack comprehensive examination and study concerning control mechanisms and limitations for system integration. Most PPC designs in the literature exhibit significant limitations, such as poor controllability near zero partiality, where the load and source voltages become equal [24], having startup inrush current when charging the series capacitor [25], etc.

The performance of full-power dc–dc converters is analyzed and validated across various droop control strategies. Meanwhile, partial power converters represent an innovative approach that enhances system efficiency and power density. This is accomplished by leveraging conventional galvanically isolated dc–dc converters without the need for intricate control algorithms. However, existing literature predominantly concentrates on improving efficiency within this domain. The practical concerns like transition between modes in step-up/down PPCs are neglected generally. Other factors like the inrush current of the series capacitor and the current controllability especially for battery energy storage applications are not fully covered. Therefore, an application-oriented PPC design is missing to close the gap in theoretical and the practical issues in the field of battery energy storage integration to the dc microgrid.

The topology employed in this article was introduced in [26] with detailed discussions of its advantages. This article undertakes a complete redesign of the converter to enhance its control and hardware performance. The optimized design incorporates low-resistance and low-voltage (LV) MOSFETs, aiming to elevate the converter's efficiency to higher levels. Additionally, the thermal and transformer designs are revised to minimize voltage overshoot across the switches and operate at lower temperatures.

The main contributions of this article are as follows.

1) This article has shown a novel approach to creating energy storage structures from used EV battery cells. This article also investigates the use of a PPC to integrate a second-life LFP battery into a dc microgrid.
2) This article proposes an optimized PPC design with an appropriate selection of semiconductor switches and the implementation of regenerative snubber and magnetics components to enhance converter efficiency.
3) The control strategy for the battery integration into a dc microgrid is implemented using linear droop control, a widely adopted, straightforward, and reliable control methodology for dc microgrids. The proposed PPC design can provide smooth current controllability

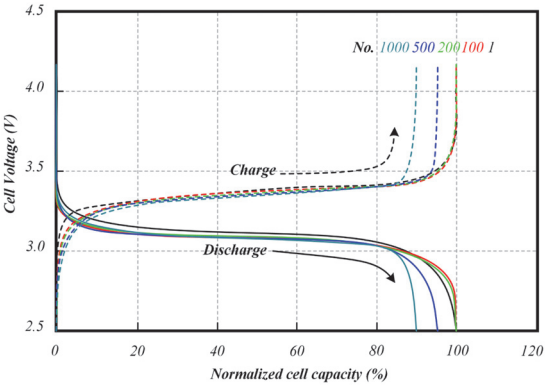

FIGURE 1. Charge–discharge profile of the $LiFePo_4$/graphite cells during cycling test with 1C rate [27].

at near-zero partiality, which is demonstrated for the first time in literature.

4) Soft switching (ZVS and ZCS) are also achieved to reduce the switch losses. Moreover, a soft start of PPC is also realized by using a solid-state circuit breaker (SSCB) and precharging the series capacitor at the startup time.
5) Experimental validation has also been carried out, and PPC peak efficiency of 99.45% was observed.

This article explores the droop control of a second-life LFP battery energy storage for residential applications. The rest of this article is organized as follows. Section II delves into the battery stack selection and briefly describes the case study PPC. Section III outlines the design guidelines necessary for the system's implementation. The experimental results are presented in Section IV. Finally, Section V concludes this article.

II. CASE STUDY SYSTEM DESCRIPTION

A. THE SECOND-LIFE LIFEPO$_4$ BATTERY STACK CONFIGURATION

Following the benefits of LFP batteries and the feasibility of utilizing the second-life automotive battery energy storage in residential applications, numerous research studies have been conducted to analyze and quantify the residual capacity and variations in the characteristics of these batteries after a specific number of charge–discharge cycles. One notable advantage of LFP batteries is their ability to maintain a stable voltage profile even after numerous charge–discharge cycles. In the referenced study on LFP batteries [27], electrochemical impedance spectroscopy was employed to investigate the degradation of the LFP/graphite Lithium-ion battery under various C-rates. The findings from 1C charge–discharge cycling over 1000 cycles are depicted in Fig. 1. The results reveal a consistently stable voltage profile, with the primary variation being a decrease in capacity (11% after 1000 cycles).

TABLE 1. Designed System Parameters

Parameter	Symbol	Value
Battery voltage	V_b	350 V(±30V)
DC microgrid voltage	V_{dc}	350 V(±30V)
Rated power	P_{reated}	4 kW
Rated power of the dc-dc stage	$P_{Conv\text{-}rated}$	750 W
Switching frequency	f_{SW}	75 kHz

Notably, this capacity decline occurs more rapidly during cycling at 2C and 5C rates (48% and 44.8%, respectively). One of the most significant differences between automotive and residential applications lies in the rate of battery degradation. In automotive systems, where fast chargers and extremely fast chargers (exceeding hundreds of kilowatts) are utilized, degradation tends to occur at an accelerated pace.

Conversely, residential applications typically operate at a much lower charge–discharge rate, commonly limited to 1C [27], [28]. In calculating the required capacity for selecting a second-life battery system for a house, this degradation rate must be considered to have a cost-effective ESS for a certain lifetime. According to the literature, the nominal voltage of the LFP cell is 3.2 V, which increases to 3.5 V for 90% of the state of charge (SoC) and decreases to 2.9 for 10% of SoC. Considering the advantage of the step-up/down PPCs, the nominal voltage of the battery stack and the dc microgrid must be equal [29], [30]. Therefore, to achieve a nominal battery voltage of 350 V in a residential dc microgrid, a series connection of 109 cells is required. Additionally, the voltage range of the battery is anticipated to fluctuate between approximately 320 and 380 V, taking into account SoC levels between 10% and 90% with corresponding battery cell voltage of 2.9 and 3.5 V, respectively. Determining the number of parallel cells in the system is influenced by factors, such as the residual capacity of each cell and the required energy storage capacity for household use. In the context of this article, a 109s1p arrangement of LFP cells is deemed suitable for the system. The parameters of the designed system are compiled in Table 1.

B. THE PPC CHARACTERISTICS AND MODULATION

This article employs the bidirectional step-up/down PPC first proposed in [26]. The PPC topology shown in Fig. 2 is based on a current-source full-bridge converter composed of a matrix inverter in the LV port and a voltage doubler rectifier in the high-voltage (HV) port. It offers distinctive advantages, including full-range soft-switching operation within its designed voltage regulation and power range. Furthermore, it exhibits limited stress on components, particularly in scenarios of low partiality where the series capacitor voltage V_C becomes zero ($V_{\text{dc}} = V_b$).

This converter can perform a soft start, unlike many other PPC converters [25]. It utilizes an SSCB to mitigate inrush current resulting from the charge of the series capacitor by

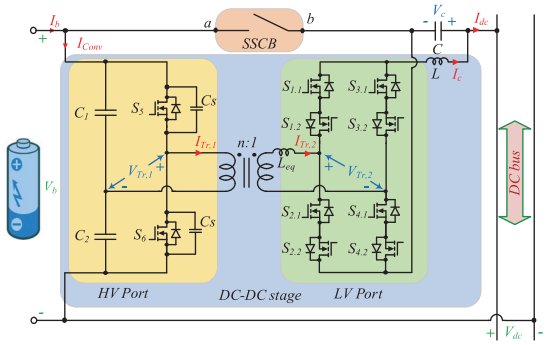

FIGURE 2. Bidirectional step-up/down (BDSUD) PPC integrating a battery energy storage into a dc microgrid.

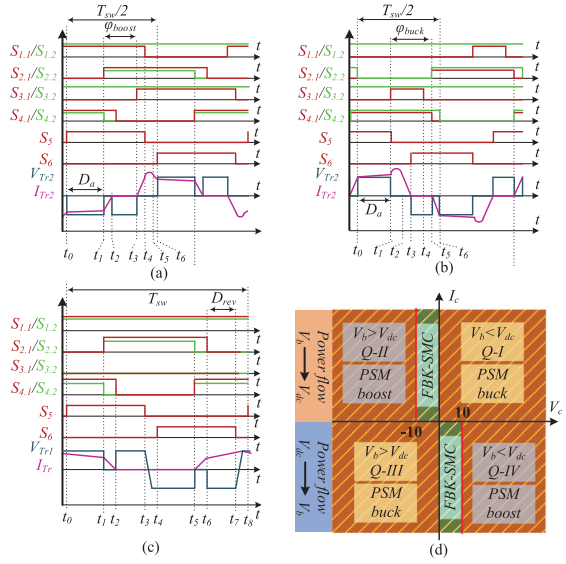

FIGURE 3. Control strategy and modulation of the PPC connected between battery and dc microgrid: (a) PSM boost modulation, (b) PSM buck modulation, (c) FBK-SMC modulation, and (d) utilization of modulation techniques within the four operation quadrants.

enabling precharging of this capacitor before the normal operation of the converter. Consequently, the soft start of the converter is achieved. Also, the SSCB ensures the safe operation of the BESS in case of dc microgrid faults. The LV port circuit is capable of generating bipolar voltage and regulating bidirectional current, operating as a four-quadrant converter. Irrespective of the power flow direction of the PPC, the power flow within the dc–dc stage can occur either from the HV port to the LV port or vice versa. The power flow direction is contingent upon the signs of the V_c and I_c. When the power flows from the HV to the LV port, the dc–dc stage functions as a buck converter, whereas in the opposite scenario, it operates as a boost converter. It is important to clarify that the terms "buck" and "boost" are used for the dc–dc stage, while "step-up" and "step-down" are employed for voltage conversion by the PPC. The control strategy of the converter relies on phase-shift modulation (PSM) for both the buck and boost modes of the dc–dc stage. A phase shift between the top and bottom switches of the LV port defines the voltage gain between the two ports, as illustrated in Fig. 3(a) and (b) for the boost and buck modes, correspondingly, for positive V_c values. Regardless of the mode, there is only one control variable that governs the LV side voltage and the dc microgrid current ($I_{\rm dc} = I_c$). For a comprehensive understanding of the operational principles, further details can be explored in [26]. The voltage gain equation for both cases can be written as follows:

$$G_{\rm buck} = \frac{V_c}{V_b} = \frac{\pi - \left(\varphi^{\rm buck} + \omega \cdot t_{\rm red}\right)}{2 \cdot \pi \cdot n} \tag{1}$$

$$G_{\rm boost} = \frac{V_b}{V_c} = \frac{2\pi n}{1 - 2f_{\rm sw}\left(\frac{\varphi_{\rm Boost}}{\pi} + \frac{2nL_{{\rm eq},m}(2I_{C({\rm max})} - I_C)}{V_b} + t_{\rm res}\right)} \tag{2}$$

where the $G_{\rm buck}$ and $G_{\rm boost}$ are the voltage gain of the buck and the boost mode of the dc–dc stage, respectively; the $t_{\rm red}$ is the redistribution time between LV port switches to allow them to turn OFF in ZCS condition (t_1–t_2 in the boost mode and t_5–t_6 in the buck mode); the $t_{\rm res}$ is the resonance time between the main transformer leakage inductance and the HV port switches snubber capacitors to fulfill ZVS turn-ON of HV port switches; the $f_{\rm sw}$ is the switching frequency and $\omega = 2\pi f_{\rm sw}$. It can be seen from (1) that for the buck mode, the voltage gain can approach nearly zero by increasing the phase shift in a way that $\varphi^{\rm buck} + \omega{\cdot}t_{\rm red} = \pi$. This signifies that the dc–dc stage can reduce the LV port voltage to almost zero, allowing for control of the converter at this critical point where V_c is becoming zero.

Conversely, in the boost mode, the voltage gain depends on the load, and the dc–dc stage may face limitations in boosting a very LV at the LV port. Given the parameters outlined in Table 1 for the designed converter, it is observed that the PPC becomes unstable when V_c falls below 10 V ($|V_c| < 10$ V) in the boost mode of the dc–dc stage, particularly when managing the maximum required load current of 4k W/320 V = 12.5 A. The instability arises from nearly zero energy stored in the capacitor C to charge the main inductor L at a very low-series voltage V_c. The operational quadrants of the PPC and the identified critical zones are illustrated in Fig. 3(d). It is noteworthy to highlight that the modulation signals depicted in Fig. 3 are designed.

A similar approach is employed for negative V_c values, with the only modification being the interchange of signals for the top and bottom switches in the symmetrical matrix LV port. As an example, changing the $S_{1,1}$ signal to $S_{2,2}$ would be part of this adaptation for negative V_c values. To address this challenge, a new modulation scheme called flyback secondary modulated conversion (FBK-SMC) is explicitly implemented in the critical zones within quadrants II and IV of the PPC

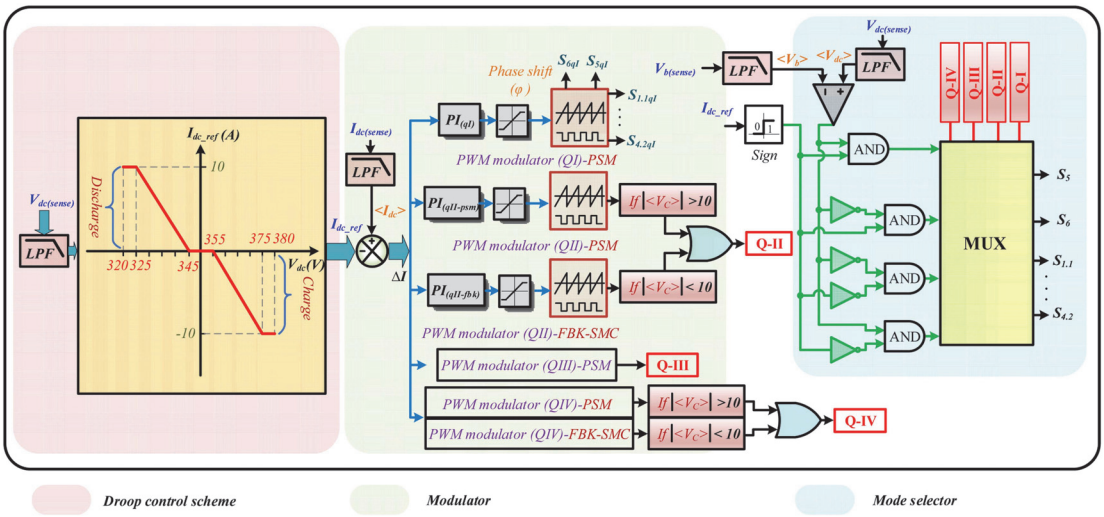

FIGURE 4. Control strategy and modulation of the PPC connecting battery energy storage to a dc microgrid.

operation, where the dc–dc stage acts as a boost converter. This modulation is depicted in Fig. 3(c), where one of the four quadrant switches is continuously turned ON (S_1), and the other one is continuously turned OFF (S_3). In this case, the modulation employs the reverse power flow from the HV port to the LV port in a specific time interval (D_{rev}) to charge the inductor L and extend the boost factor of the dc–dc stage. The details of this approach can be studied comprehensively from [31] and [32]. This approach enables the PPC to operate smoothly within this critical zone. The voltage gain of the dc–dc stage, in this case, can be determined as

$$G_{\text{boost}} = \frac{V_b}{V_c} = \frac{4 \cdot n}{1 - 4 \cdot D_{\text{rev}}}. \tag{3}$$

Operating with FBK-SMC modulation, the PPC will be less efficient due to higher energy circulation between the HV and the LV ports. However, the range in which this modulation is applied is very limited ($|V_c| < 10$ V) in comparison to the whole voltage regulation range of the PPC ($|V_c| < 60$ V), and it will be implemented only in two of the operation quadrants (II and IV) at a low power processed by the dc–dc stage. Therefore, the efficiency drop in this mode would have a negligible influence on the average efficiency of the converter.

Regarding system control, the conventional linear current droop control is typically implemented to govern the dc microgrid. Its use offers advantages, such as control simplicity and the absence of communication requirements between converter units. This simplicity enhances system robustness against communication issues and cyberattacks. The responsibility of maintaining the dc bus voltage within the specified range (320–380 V) lies with the battery energy storage. This voltage range corresponds to the NPR9090-2024 regulations [33] and the current/OS set of rules [34] currently used in dc buildings. Droop control becomes particularly crucial in islanded dc microgrids where the dc bus voltage stability is achieved by injecting or absorbing power from the dc microgrid depending on the dc microgrid voltage. This relationship is established through the definition of a droop coefficient, and the calculation of the droop coefficient is performed as follows:

$$V_{\text{dc}} = V_{\text{nom}} - R_{\text{dr}} I_{\text{dc}} \tag{4}$$

where $V_{\text{nom}} = 350$ V denotes the nominal dc bus voltage in the designed system and R_{dr} represents the droop coefficient, indicating the rate of current change in response to the voltage variation. The desired droop scheme is visually represented in Fig. 4.

The digital implementation of the proposed control method is based on a state machine contingent upon the measured current and voltage values. Following the measurement of the dc bus voltage, the dc bus reference current ($I_{\text{dc\_ref}}$) is generated from the droop curve. The state machine, based on a comparison between V_{dc} and V_b and the direction of the reference current ($I_{\text{dc\_ref}}$), decides and selects the appropriate operation mode from the six available modulations (three for discharge and three for charge process), as illustrated in Fig. 3(d). Subsequently, the state machine sets the PI controller parameters specific to the selected mode. The PI controller then converges to the required phase shift for each point based on the error generated by the difference between the measured and the reference current injected/drawn in/from the dc bus.

The calculated phase shift is applied to the compare values of a high-resolution timer, which generates the gating signals for all switches. All these processes are seamlessly executed through a logical procedure within the state machine, which operates solely based on the V_{dc}, V_b, and I_{dc} measurements. A simplified version of this procedure is visualized in Fig. 4.

III. DESIGN GUIDELINES

To meet the requirements of the entire system stated in the preceding section, two steps of design procedures must be followed. The initial step involves establishing a control design procedure to run the converter seamlessly across the whole operation range of the system, which is defined by the voltage variation range of the dc microgrid and the battery SoC. The subsequent design phase concentrates on the selection of the components and the converter parameter values to operate under the desired expectations.

A. CONTROL DESIGN

The PPC employs two types of voltage sensors. Two dedicated unipolar ACPL C87A sensors measure the battery and dc microgrid voltages. At the same time, a bipolar sensor ACPL C79B is used for the series capacitor voltage measurement, as it can measure both voltage polarities. The specific function of the series capacitor voltage sensor is to facilitate the soft start of the converter by precharging the series capacitor. This approach mitigates the inrush current during the converter startup, which might otherwise occur due to the high *dv/dt* on the series capacitor (in the case of a HV difference between the battery and the dc microgrid) [26]. The current sensor (TLI4971-A025T5-E0001) is used to implement the current control at the series port linked to the dc microgrid. To mitigate potential induced electromagnetic interference, a low-pass filter with a cutoff frequency of 1 kHz is incorporated at the output of all sensors. Additionally, a first-order low-pass filter within the software with the same cutoff frequency is applied to ensure nonoscillating voltage/current signals inside the microcontroller for the correct decision-making process.

The closed-loop control system relies on the PI controller to determine the phase shift for each mode according to the measured and the reference current. A feedforward control approach is employed to prevent any oscillation and instability during the mode change. This involves calculating the initial phase shift for the next mode based on measured battery and dc microgrid voltages and the I_{dc} value. To achieve this, the phase shift of the converter is computed for both the buck and boost modes of the dc–dc stage in the PSM, as well as for the FBK-SMC mode, described as follows:

$$\varphi_{\mathrm{buck}} = -0.5 + \frac{1.2305 \cdot |I_{\mathrm{dc}}|}{V_b} + \frac{2.4549 \cdot |V_c|}{V_b} - 357 \cdot 10^{-6} \cdot (|I_{\mathrm{dc}}| - 6) - 1.35 \cdot 10^{-6} \cdot V_b \quad (5)$$

$$\varphi_{\mathrm{boost}} = 0.044 + 0.014925 \cdot \left(\frac{\pi}{2} - arctg\left(\frac{26.125 \cdot |I_{\mathrm{dc}}|}{V_b}\right)\right) + \frac{4.75 \cdot |V_c| - 1.5675 \cdot |I_{\mathrm{dc}}| + 18.81}{2V_b} \quad (6)$$

$$D_{\mathrm{rev}} = 0.25 - \frac{2.375 \cdot |V_c|}{V_b} - \frac{0.78375 \cdot (24 - |I_{\mathrm{dc}})}{V_b} + 15 \cdot 10^{-4} \cdot (|I_{\mathrm{dc}}| - 3)\,. \quad (7)$$

The provided equations are derived from (1), (2), and (3) with adjustments that reflect the nonideality related to the equivalent series resistance of the converter components.

The state machine computes the initial phase shift of each mode and preloads it to the timer registers before the start of the next mode. This method ensures a seamless transition between the current and the next mode, minimizing oscillations in the output current. Additionally, it helps prevent excessive voltage stress and potential malfunctions in the converter.

B. HARDWARE DESIGN

To achieve the desired system behavior, meticulous selection and calculation of all hardware components and their parameters are essential. The following steps outline a comprehensive design approach for the PPC connected between the battery and the dc microgrid.

1) MAIN TRANSFORMER DESIGN

The isolation transformer is critical in this type of PPC to allow for the series connection of one of the dc–dc stage ports without creating a short-circuit of either the input or output source. Moreover, the turn ratio of the transformer determines the voltage regulation range between the battery and the dc microgrid. In the context of this application-oriented paper, the turn ratio is defined by the voltage variation of the $LiFePo_4$ battery and the dc microgrid concerning each other. As outlined in the prior section, this range is defined as 60 V. Adding a 10 V margin to account for any possible transients, the regulation range of 70 V is considered acceptable. The turn ratio must be calculated in the most critical operation point where the parallel port voltage is at the minimum voltage of 320 V and the series port operates at the maximum voltage of 70 V. This approach guarantees the correct operation of the PPC at higher parallel port voltage values (>320 V) while maintaining the maximum required partiality (maximum regulation range)

$$n_{m,\min} \geq \frac{V_{b,\min}}{2 \cdot D_{a,\max} V_{c,\max}} \quad (8)$$

$$V_{c,\max} = \left|V_{b,\min} - V_{dc,\max}\right| \quad (9)$$

in which n_m is the turn ratio of the main transformer and ($D_{a,\max} = 0.95$) is the maximum active energy transfer duty cycle of the dc–dc stage. This parameter is restricted by the current redistribution time between LV port switches (t_{red}) and the resonance time interval between LV and HV ports to fulfill the ZVS turn-ON of HV port switches [26].

Regarding the main transformer leakage inductance ($L_{\mathrm{eq},m}$), some constraints must be considered as follows.

1) Increasing the leakage inductance results in longer current redistribution and resonant time intervals for LV port switches. Consequently, this elongation shortens the active energy transfer state, decreasing $D_{a,\max}$ (undesirable).

2) Examining the voltage gain of the dc–dc stage in boost mode reveals that a higher leakage inductance contributes to a higher boost factor under similar conditions (desirable).
3) As given in [35], body diode reverse recovery affects the LV port switches during synchronous rectification, causing considerable voltage overshoot across them, which increases with increasing the $L_{eq,m}$ (undesirable).
4) Ultimately, a higher leakage inductance value induces more ringing on LV port switches, resulting in higher power loss (undesirable).

Considering all these limitations, the selection of leakage inductance is an optimization problem, which, however, is also subject to the practical limitations of the feasible transformer designs. Hence, an efficient regenerative snubber circuit must be employed [35]. Due to interactions between the main and the snubber transformer, they must be designed and implemented simultaneously to control the ratio between their leakage inductances.

The main transformer core is selected based on the maximum flux density (100 mT) to limit the core losses. The number of turns based on the maximum flux density can be derived from the following equation:

$$B_{\max} = \frac{V_{b,\max}}{4 \cdot n_1 \cdot f_{SW} \cdot A_e} \tag{10}$$

in which A_e is the effective cross-section of the core and n_1 is the number of turns in the HV side of the transformer.

2) SNUBBER TRANSFORMER AND CIRCUIT DESIGN

Similar to other current source converters, voltage oscillations and overshoots appear across the LV port switches due to resonant ringing between the MOSFETs' output capacitance (C_{oss}) and the main transformer's leakage inductance ($L_{eq,m}$). The overshoot is also increased due to MOSFETs' body diode reverse recovery. The relationship between the voltage overshoot across the LV port switches and converter parameters is expressed by the following equation provided in [35]:

$$v_{ds}(t) = n_m \cdot V_b/2 - (n_m \cdot V_b/2 \cdot \cos(\omega t) + i_0 \cdot \rho \cdot \sin(\omega t)) \cdot e^{-T_{ac}/4 \cdot \tau_{LK}} \tag{11}$$

where i_0 is the initial current of the leakage inductance that determines the switch body diode reverse recovery time; ρ is the characteristic impedance of the resonant circuit $\rho = (L_{eq,m}/C_{eq})^{0.5}$; ω is the resonance frequency of the circuit $\omega = (L_{eq,m} \cdot C_{eq})^{-0.5}$; C_{eq} is the overall parasitic capacitance of the circuit that includes C_{oss} of the mosfets and the winding capacitance of the main transformer; and τ_{LK} is the time constant of the *RLC* circuit. The voltage overshoot is nearly twice the steady-state blocking voltage of the MOSFETs when not accounting for the reverse recovery of the diodes. The practical effect of the reverse recovery charge being injected into the parasitic *RLC* network results in an almost voltage overshoot of 2.5 times the steady-state drain-source voltage of the switches. It is worth noting that the increase of the main transformer leakage inductance also increases the overshoot values by affecting ρ. These calculations have been performed using the converter parameters given in Table 1. Further details about the calculations can be studied from [35].

Implementing a snubber circuit is crucial to prevent overdesign with HV rating switches and allow for the use of cost-effective LV MOSFETs. However, utilizing a single *RC* snubber across the LV side of the transformer or an individual *RC* snubber for each switch can increase converter power loss, leading to an overall decrease in system efficiency. As proposed in [35], a regenerative snubber can be implemented to transfer overshoot energy to the HV side of the main transformer. This involves using an auxiliary transformer, smaller than the main transformer, and two diodes to form a passive voltage doubler circuit in the HV port of the converter. The turns ratio of this transformer (n_{sn}) must be lower than that of the main transformer to reverse bias the snubber circuit diodes and block power transfer during the normal steady-state operation of the converter. The correlation between these two values is detailed in [35]. When this turn ratio (n_{sn}) closely approaches the turn ratio of the main transformer (n_m), the rms current inside the snubber circuit increases, leading to higher losses in the snubber circuit.

Conversely, reducing n_{sn} below a certain threshold hinders the forward bias of the diode bridge during overshoot periods. Balancing these factors is crucial to optimize the performance of the system. In practice, maintaining n_{sn}/n_m between 0.85 and 0.95 is essential for achieving a tradeoff among the rms current of the snubber, the duration of the regenerative interval, and the reduction of voltage overshoot. This range allows for a balanced optimization of these factors in the system. Moreover, due to the parallel connection of the snubber circuit with the main transformer, the overall impedance of the snubber circuit in high-frequency oscillations must be lower than the main path to allow the current flow from the snubber circuit. This demands the leakage inductance of the snubber transformer to be at least one-third the value of $L_{eq,m}$.

To meet all these requirements, the main and snubber transformer must be designed considering both transformer parameters. Its core is to be selected based on (10) and considering $B_{\max} = 150$ mT, which is acceptable for planar magnetic design. In practice, the minimum leakage inductance of 350 nH was reached for the snubber transformer with EILP32 core set using the turn ratio of $n_{sn} = 40/18 = 2.22$. Therefore, the leakage inductance of the main transformer of 1.2 µH was implemented by rearranging the geometry of its windings to maximize the voltage clamping effect from the regenerative snubber. Moreover, to further decrease the voltage overshoot, a tiny *RC* snubber with 50 Ω resistance and 2.1 nF C0G ceramic capacitor is implemented across the LV side of the main transformer.

3) COMPONENTS SELECTION

The main inductor L and the HV port voltage doubler capacitors $C_1 = C_2 = C_{HV}$) are chosen based on the permissible

voltage and current ripple on both the battery side and the dc microgrid side. To further reduce the size of the converter, an off-the-shelf compact flat wound wire inductor is selected for use in the PPC. This necessitates minimizing the high-frequency current ripple in the inductor to mitigate power loss resulting from the high ac resistance of this inductor type. Therefore, the current ripple of the inductor is constrained to 5% of the nominal current. Elevating the frequency from 50 to 75 kHz, as compared to [26], will reduce the current ripple even further. In the HV port, electrolytic and film capacitors form voltage doubler capacitors. This approach aims to suppress both high- and low-frequency voltage ripple across the HV port, employing differences in the frequency behavior of film and electrolytic capacitors. The following equation can be used to determine the minimum values for the main inductor and HV port capacitors:

$$\Delta i_L = \frac{V_c \cdot (1 - D_a)}{4 \cdot L \cdot f_{\text{sw}}} \tag{12}$$

$$\Delta V_{\text{HV}} = \frac{P \cdot (1 - D_a)}{2 \cdot C_{\text{HV}} \cdot V_b \cdot f_{\text{sw}}}. \tag{13}$$

The inductor and capacitors are determined through calculations performed at the worst operation points where the current ripple and voltage ripple are maximum. In this case, it corresponds to converter operation at maximum partiality at the minimum HV voltage.

To select the switching devices, both voltage and current stress are considered. For the HV port switches, SiC MOSFET with a breakdown voltage of 650 V, the minimum voltage rating for SiC MOSFETs on the market, is selected. It is worth noting that the blocking voltage of the HV port switches is defined by the maximum battery voltage of 380 V. For the LV port switches, considerations extend beyond voltage–current stress. It becomes crucial to control the voltage overshoot induced by the parasitic resonance across their output capacitance and transformer leakage inductance. The body diode further amplifies this effect due to its reverse recovery charge injected in the parasitic resonant tank. To address these challenges, a MOSFET with specific characteristics is necessary, including low output capacitance (C_{oss}), low reverse recovery charge (Q_{rr}), and low ON-state resistance (to minimize conduction loss).

Simultaneously, the selected MOSFETs must withstand the voltage stress level at the LV port of the converter. After an extensive market search and experimental analysis of over 10 different MOSFETs within the 150–250 V breakdown voltage range, a 150 V Si MOSFET from Infineon is chosen for its optimally low ON-state resistance and reverse recovery charge.

The results obtained from the previous overshoot calculations indicate that the voltage overshoot across the LV port switches can be reduced from 2.5 times the steady-state voltage stress to 1.6 times by utilizing both regenerative snubbers and a tiny *RC* snubber. Consequently, with a maximum battery voltage of 380 V and a transformer turn ratio of 2.375, the overshoot is constrained to 120 V. This implementation effectively mitigates the overshoot, aligning with the specified system operating voltage ranges.

4) SSCB DESIGN

The SSCB is implemented to facilitate the soft start, which was demonstrated in [26]. Additionally, the SSCB aids in achieving current controllability at low current values. In this range, the controller may struggle to fully track the reference current, when the current flows from the HV port to the LV port, irrespective of the control mode. To address this, at low current values (<1 A), one of the series switches is turned OFF, and the SSCB changes to a turned-ON switch in series with a diode. This action blocks reverse current flow, ensuring it remains in the desired direction as defined by the droop control characteristic.

The SSCB was designed according to the guidelines given in [36]. It comprises two back-to-back MOSFETs with their sources connected and controlled individually by high-speed GPIO outputs of the microcontroller. Here, UCC21521, an isolated dual-channel gate driver, is used for all MOSFETs. Additionally, an *RCD* snubber and a metal-oxide varistor are installed across the drain-source terminals of each switch to protect them against overvoltage. The component values are taken from [36], since the voltage and power levels closely align with our application.

IV. EXPERIMENTAL RESULTS

To confirm the theoretical propositions and approaches, an experimental prototype is built with a rated power of 4 kW, capable of short overloads up to 5 kW. The prototype, depicted in Fig. 5(a), consists of five distinct boards—four power boards and one control board. This configuration offers flexibility in the design, implementation, and repair of the experimental setup. The thermal management is done by surface-mounted heatsinks that are directly attached to the drain pad of the surface-mounted MOSFETs.

To replicate the behavior of the battery and dc microgrid, two iTECH IT6006C and 6012C bidirectional power supplies are employed. These power supplies can generate various voltage and current functions at their output. Additionally, they can emulate the battery charge/discharge curve using iTECH BSS2000 Pro battery simulation software. The digital control board is centered around the STM32G474 ARM Cortex-M4 microcontroller, which is capable of providing 12 PWM signals with 6 dual-channel high-resolution timers. Fig. 5(b) illustrates a connection diagram of PPC with power sources. The efficiency measurements are conducted utilizing the Yokogawa WT1800 precision power analyzer. The parameters of the experimental prototype and components used can be found in Table 2.

To validate the effectiveness of thermal design, the prototype is preheated for 1 h at the rated power of 4 kW. The thermal images recorded by the FLUKE Ti10 thermal imager

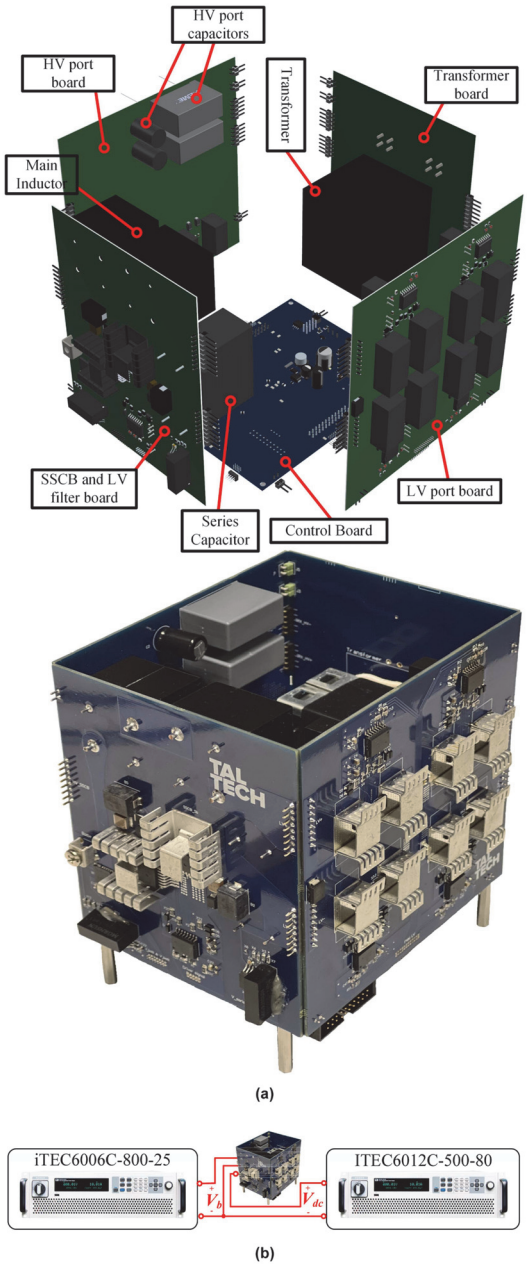

FIGURE 5. (a) Experimental prototype of the developed PPC. (b) Connection diagram.

TABLE 2. Parameters and Components of the Experimental Prototype

Component/Parameter	Symbol	Type/Value
HV Port Switches	S_5, S_6	G3R60MT07J
LV port switches	$S_{1.1}$ - $S_{4.2}$	BSC0403NS
SSCB switches	S_a, S_b	UF3SC065030B7S
Main inductor	L	CPER3231-820MC (2×82 µH)
Transformer core	-	2 × EE42/21/15
Main transformer turns ratio	n_m	2.375:1
Main transformer leakage inductance	$L_{eq,m}$	1.2 µH
Snubber transformer core	-	EILP32
Snubber transformer turns ratio	n_{sn}	2.22:1
Snubber transformer leakage inductance	$L_{eq,sn}$	350 nH
Snubber diodes	D	STPSC2H065B-TR
RC snubber	-	50 Ω–2.1 nF
HV port capacitors	$C_1 = C_2$	R60IR51005040K / ECA2EHG100 (10 ‖ 10 = 20 µF)
HV port snubber capacitors	C_s	1.1 nF
Series capacitor	C	DCP4G056007GD4KSSD (60 µF)

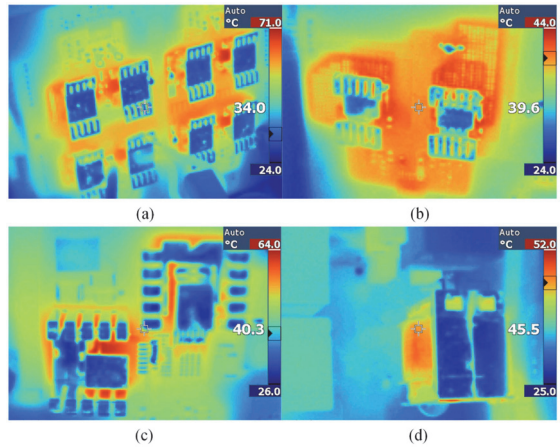

FIGURE 6. Thermal behavior of the PPC in maximum power (4 kW) after temperature stabilization (1 h). (a) LV port board. (b) HV port board. (c) SSCB switches. (d) Main transformer.

are shown in Fig. 6. They indicate that the maximum component temperature reaches 71 °C on the LV port board, which falls within the normal operation range of the switches. The temperature of the main transformer and other components is also acceptable.

To assess operation of the snubber circuit, three tests are executed. Initially, the PPC is tested without any snubber circuit to examine the maximum voltage overshoot across the LV port switches with a 10 A current flowing through the inductor. In this scenario, raising the HV port voltage to 250 V results in approximately 140 V voltage overshoot. For safety purposes, 140 V is considered to avoid any switch breakdown. Considering the voltage doubler in the HV port and the transformer turn ratio (1:2.375), the steady-state blocking voltage of the switches equals roughly 53 V. This indicates that the overshoot is 2.65 times higher than the steady-state blocking voltage level, reasonably close to the theoretical overshoot level (2.5 times), which also includes influence of the body diode reverse recovery. The result of this test is shown in

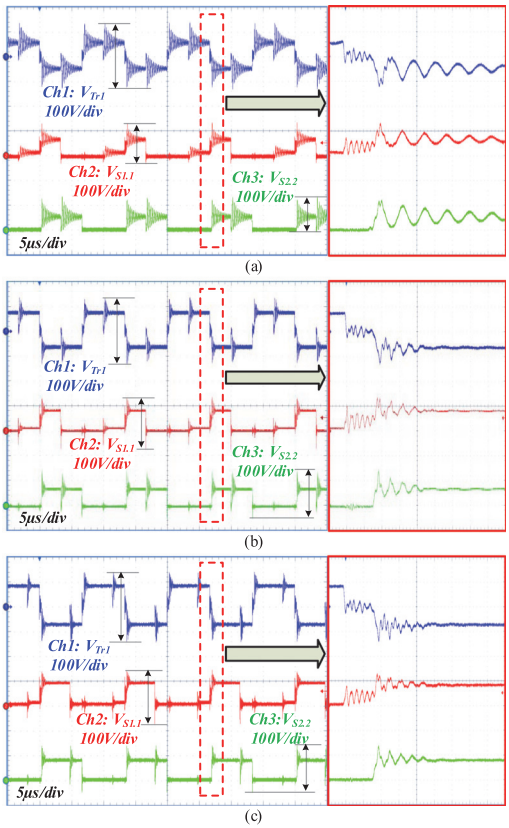

FIGURE 7. Voltage waveforms of main transformer LV side and two LV port switches ($S_{1.1}$ and $S_{2.2}$) drain-source (a) without snubber, (b) with regenerative snubber, and (c) with regenerative and RC snubber (50 Ω–2.1 nF).

Fig. 7(a). The steady-state blocking voltage and the level of overshoot are visible from the zoomed part on the right side of the figure. The regenerative snubber is implemented in the second step, and a similar test is performed. In this case to reach the 140 V across the drain-source terminals of the LV port MOSFETs, the HV port voltage must be increased to 330 V. In other words, following the same calculations, the voltage overshoot decreases to two times higher than the steady-state blocking voltage (70 V). The result of this step is depicted in Fig. 7(b).

Finally, the *RC* snubber was added alongside the regenerative snubber to allow the HV port voltage to increase to the required voltage range (max. of 380 V). As illustrated in Fig. 7(c), the voltage overshoot is approximately 130 V for 380 V at the HV port. This means the obtained voltage overshoot compared to the previous conditions has decreased to 1.6 times the steady-state blocking voltage (80 V). Hence, the 150 V MOSFETs can easily be utilized for the system under this operation condition. This result is essential for the PPC feasibility, as the market provides no suitable alternatives at higher rated voltage due to the excessive reverse recovery charge of Si MOSFETs. Notably, transitioning from a simple circuit in the initial step to a circuit with a regenerative snubber alters the voltage ringing frequency across the switches. This change is attributed to the parallel connection of the snubber transformer leakage inductance and the main transformer leakage inductance, which significantly decreases the overall inductance observed from the switch side. Consequently, this increases the observed parasitic resonance frequency.

In the resonant intervals (t_1–t_2) and (t_4–t_5), the energy accumulated in the transformer leakage inductance discharges the snubber capacitor of the turn OFF switch at the HV port. As the snubber capacitor discharges and its voltage reaches zero, its body diode conducts and the switches can be turned ON in ZVS condition. Fig. 8(a) exhibits voltage and current of HV port switch S_5. It can be observed that soft switching occurs during turn ON. Fig. 8(b) and (c) shows the ZVS turn ON and soft turn OFF assisted by snubber capacitor.

To verify the PPC functionality under the droop control curve presented in Fig. 4, three tests are conducted for three battery voltage levels (335, 350, and 365 V). The outcomes of these scenarios are depicted in Fig. 9(a)–(c) correspondingly. When $V_b = 335$ V, the PPC initiates its operation in the second quadrant (step down/discharge). As the dc microgrid voltage rises, the series capacitor voltage reaches the threshold level ($|V_c| < 10$ V) in the second quadrant, causing the dc–dc stage to change modulation to the FBK-SMC. This transition results in the continuously tuned-ON S_4 and turned-OFF S_2. Between $V_{dc} = 345$ and 355 V, all the switches turn OFF to block the current flow, except the SSCB needed to maintain the series capacitor always charged. In the range of 355 V $< V_{dc} <$ 380 V, the PPC works in the fourth quadrant (step-up/charge) with PSM modulation. It can be seen that all mode transitions are happening smoothly without a considerable current spike or oscillation. For the $V_b = 350$ V, almost a similar routine happens in Fig. 9(b), with the difference that in the discharge part of the droop scheme, the Q-I PSM mode is not used, and a new operation mode is introduced in the charge zone within the range of 355 V $< V_{dc} <$ 360 V. This new mode happens in the fourth quadrant of the PPC (step-up/charge) with FBK-SMC modulation (due to $|V_c| < 10$ V).

Last, the droop control test for $V_b = 365$ V is conducted, and the result is shown in Fig. 9(c). In this scenario, the PPC operates in the second quadrant with PSM modulation throughout the entire range of the discharge zone. For this battery voltage, a new mode occurs from $V_{dc} = 355$ to 365 V. Within this range, the PPC operates in the third quadrant (step-down/charge). For $V_{dc} > 365$ V, the FBK-SMC and PSM modulation will be applied until $V_{dc} = 375$ and 375 V $< V_{dc} <$ 380 V, respectively.

All three results demonstrate smooth mode transitions without significant current spikes or oscillations. Thus, the state machine effectively performs control strategy and mode selection, allowing seamless mode transitions within the droop control scheme.

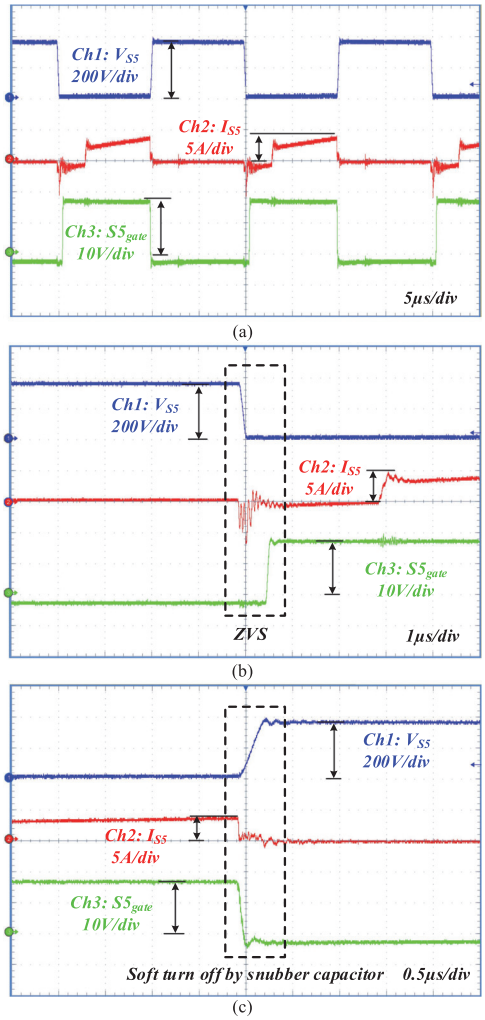

FIGURE 8. Soft switching of HV side switch S_5: (a) current, voltage, and control signal of the switch, (b) ZVS turn ON, and (c) soft turn OFF assisted by snubber capacitor.

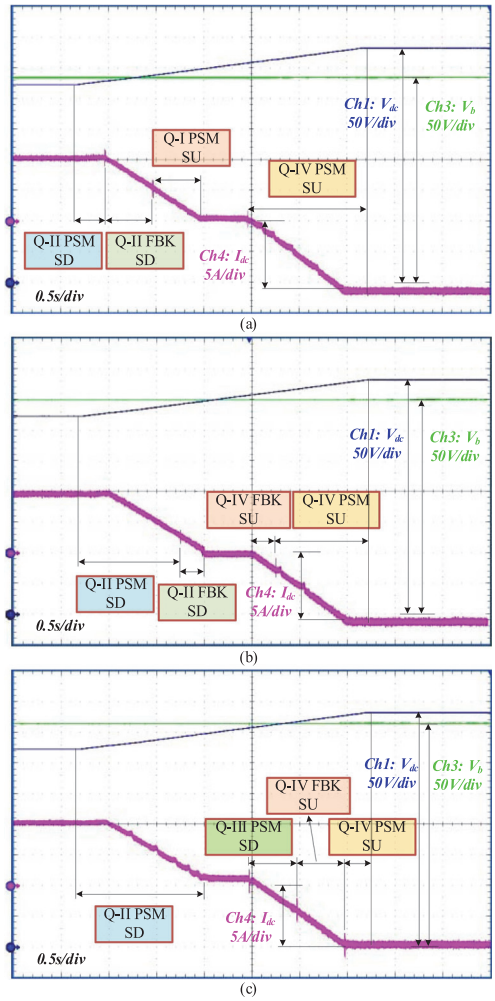

FIGURE 9. DC microgrid current under droop control for three different battery voltages. (a) $V_b = 335$ V. (b) $V_b = 350$ V. (c) $V_b = 365$ V.

The efficiency measurements are done both for the individual PPC operation in the different power levels varying from 1 to 4 kW with V_c changing from −60 to 60 V and during the droop control operation with three different battery levels. The results for both cases are shown in Figs. 10 and 11, respectively. The PPC reaches the maximum efficiency of 99.45% in 3 kW. Other than reaching high efficiency levels, the efficiency outputs are almost flat (>99%), especially for positive V_c values, as the PPC is working in the first quadrant.

Step-up/down PPCs process less power than step-up and step-down analogs, but they employ more components. The LV port of the dc–dc stage can operate bipolarly by applying

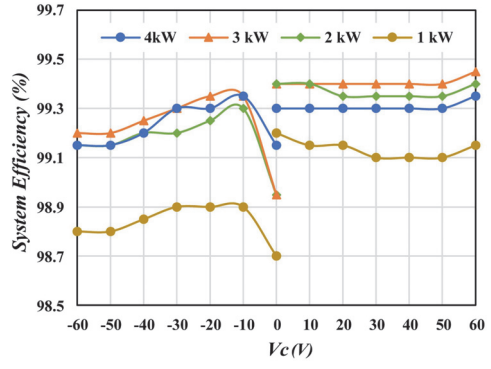

FIGURE 10. Experimental efficiency curves measured at four active power levels (1, 2, 3, and 4 kW) versus series capacitor voltage (−60 to 60 V).

TABLE 3. Parameters and Components of the Experimental Prototype

Ref.	Configuration	Voltage Range (V)		K_{pr} (%)	Nominal power (kW)	Efficiency (%)	Soft switching	Control Approach	Soft start
		V_{in}	V_{out}						
[37]	IPOS (step-up/down)	187–253	220	15	0.75	98.6–99.6	Not present	MPPT regulation	No
[38]	IPOS (step-up)	154–220	220	30	0.75	99	Not present	MPPT regulation	No
[39]	IPOS (step-up/down)	187–253	220	15	0.95	98.7–99.4	Not present	MPPT regulation	No
[40]	IPOS (step-up)	400	347–435	8	7.3	98.5–99.6	Not present	PI regulation	No
[41]	IPOS (step-up/down)	350	300–400	7	1.5	×	Partially present	Open loop voltage regulation	No
[42]	IPOS (step-up)	2–23	50–58	22	3.4	80–98.2	Not present	×	No
[43]	IPOS (step-down)	180–300	48	73	1.0	96	Present (During turn-on)	Voltage single closed loop control	No
Proposed work	IPOS (step-up/down)	320–380	335–365	17	4	98.7–99.45	Present	Current droop control	Yes

'×' = Not given

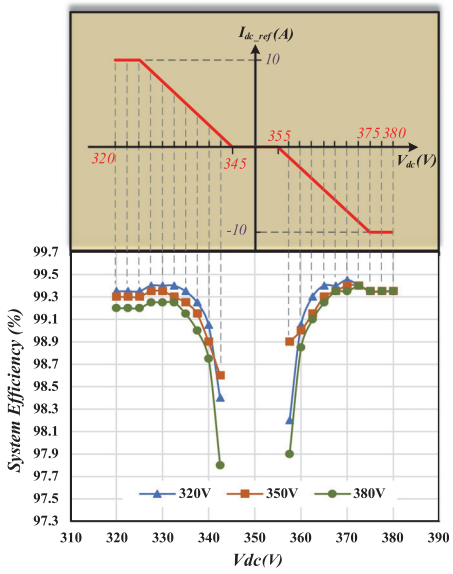

FIGURE 11. Efficiency measured at the different operation points of the droop curve at three battery voltage levels (V_b = 320 V, V_b = 350 V, and V_b = 380 V).

additional switches. Certain converters use diodes that add to the conduction power loss.

When it comes to achieving near-zero-voltage and soft start operation of the LV port, the current literature lacks clarity on how the claimed high efficiency and current controllability are obtained, aside from mentioning short-circuiting the LV port switches. Given the crucial nature of smooth operation in this context, it is essential to demonstrate the methodology for operating at this critical point for step-up/down PPCs. A comparative assessment of the proposed work with some existing PPC configurations [37], [38], [39], [40], [41], [42], [43] is given in Table 3. A unidirectional alternative, the converter from [40], has poor current control capabilities as it uses shoot-through duty cycle control, which is weakly dependent on the power level. This issue raises a question about effectiveness of this structure in battery energy storage applications. In [43], converter switches get turned ON under ZVS, but it does not provide any soft switching during turn-OFF. Additionally, this converter has higher diode conduction loss. These factors result in lower converter efficiency. The proposed work realized a current droop control and considered modulation gives a complete turn-ON ZVS while the snubber of the HV port offers a soft turn-OFF of switch. Moreover, optimized design and appropriate selection of components give a higher converter efficiency and experimental results guarantee the same.

V. CONCLUSION

The article has demonstrated a new approach to building energy storage using second-life battery cells from EVs. Based on the performed analysis, it is shown that building dc microgrids are currently being standardized for the nominal voltage of 350 V with ±30 V droop control band. Combined with the much-increased use of LFP batteries in EVs, it was proposed that building an LFP battery stack of 109 cells could be an optimal solution for the emerging 350 V building dc microgrids. This allows for the use of a highly efficient application-tailored PPC, as demonstrated in the article.

This article has utilized a topology proposed recently by the authors and demonstrated how to design it for the given applications and how the control systems could be implemented. As a result, the built prototype utilizes VA-rating-optimized semiconductors to reduce the cost of implementation. It

implements multimode control to enable full current controllability near zero partiality, which was not properly demonstrated in the prior literature. Despite avoiding costly high-end components, the prototype has achieved 99.45% peak efficiency, including auxiliary losses. It was proven capable of controlling the battery current according to linear droop control with a dead zone despite the need to perform operating mode transitions by changing the converter modulations. The topology morphing control utilized was enhanced by means of feedforward control that precalculates the theoretical control variable (phase shift) value before the mode transition happens. Afterward, a PI controller adjusts the small error caused by the losses in the real converter, which improves control dynamics as the control variable preset by the feedforward equations is very close to the needed value. When tested according to the droop control characteristic, the converter demonstrated efficiency levels of over 99% in most of the probable operating points.

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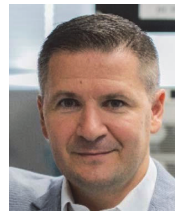

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