TTÜ INFOTEHNOLOOGIA TEADUSKOND
ARVUTITEHNIKA INSTITUUT
TEADSU- JA ARENDUSTEGEVUSE AASTAARUANNE 2013

1. Arvutitehnika instituudi struktuur

Arvutitehnika instituuti kuulub kaks uurimisgruppi:

- Tarkvaratehnika eriteemad (prof Ahto Kalja)
  Research group „Special topics of software engineering"
- Digitaalsüsteemide disain ja test (prof. Raimund Ubar)
  Research group "Design and test of digital systems"

2. Arvutitehnika instituudi teadustöö kirjeldus

2.1. Research group „Special topics of software engineering"

2.1.1. Description of the research work

Research group is involved in research on special topics of software engineering. Scientific activities include different areas of web information system studies and technologies, e-Government issues and software refactoring

2.1.2. Main research results

The best results of research group in year 2013 include the next row of investigations:

1. We have investigated and generalized the main lesson learned by developing Estonian e-Government Services (Kalja, Põld, Robal, Vallner, Viies).
2. We have concentrated on strategic web adaptations and showed that including indicators of user interest, such as the time spent on page, into methods of identifying popular portal pages based on access rate ranking is essential for improving such environments (Robal, Kalja).
3. We have provided a proof of concept to find 'smelly code' with the opportunity to help developers to fix these issues aided by today's integrated development environments, which have refactoring support built in (Põld, Robal, Kalja).

2.1.3. Five main publications of research group of the year 2013.

1. Kalja, Ahto; Põld, Janari; Robal, Tarmo; Vallner, Uuno; Viies, Vladimir (2013). Estonian eGovernment Services: lesson learned. In: PICMET '13 : Proceedings, Technology Management in the IT-Driven Services [July 28 - August 1, 2013, San Jose, California, USA]: (Toim.) Kocaoglu, D. F. et al.. Portland, Oregon, USA: PICMET, 2013, 562 - 568.
2. Robal, Tarmo; Kalja, Ahto (2013). Applying user domain model to improve Web recommendations. In: Databases and Information Systems VII : Selected Papers from the Tenth International Baltic Conference, DB&IS 2012: (Toim.) Caplinskas, A.; Dzemyda, G.; Lupeikiene, A.; Vasilecas, O.. Amsterdam: IOS Press, 2013, (Frontiers in Artificial Intelligence and Applications ; 249), 118 - 131.
3. Robal, Tarmo; Kalja, Ahto (2013). Managing knowledge in Web portals for improved customer loyalty and satisfaction. In: PICMET '13 : Proceedings, Technology Management in the IT-Driven Services [July 28 - August 1, 2013, San Jose, California, USA]: (Toim.) Kocaoglu, D. F. et al. Portland, Oregon, USA: PICMET, 2013, 1207 - 1216.
4. Põld, Janari; Robal, Tarmo; Kalja, Ahto (2013). On proving the concept of an ontology aided software refactoring tool. Caplinskas, A.; Dzemyda, G.; Lupeikiene, A.; Vasilecas, O. (Toim.). Databases and Information Systems VII : Selected Papers from the Tenth International Baltic Conference, DB&IS 2012 (84 - 94). Amsterdam: IOS Pres

5. Robal, Tarmo; Kruus, Helena; Kalja, Ahto (2013). Complementing ICT studies with learning objects on domain ontologies. In: Proceedings of the 24th Annual Conference on European Association for Education in Electrical and Information Engineering (EAEEIE): 24 th International Conference on European Association for Education in Electrical and Information Engineering 30-31 May 2013, Chania, Greece. (Toim.) G. M. Papadourakis . IEEE, 2013, 92 - 96.

2.2. Research group "Digital design and test"

2.2.1. Description of the research work

During the last decade the evolution of electronic systems has made a major leap and introduced new design paradigms like network-on-chips, multi- and many-core systems, ubiquitous and massively parallel computing, resulting in increasing dependency of society on electronics and hence, in increasing role of the reliability, testability and dependability of modern electronic systems.

The research group is conducting investigations and development of new methods in the fields of design verification, test, and dependability of digital systems and their components in line with International Technology Roadmap for Semiconductors. The research is targeting important quality factors like time-to-market, power consumption and speed of systems in design, performance and quality in verification and test, as well as fault tolerance and dependability of systems during their life-time.

The most important R&D results have been achieved in specific topics of diagnostic modeling of systems, fault simulation, automated design error diagnosis and debugging, test generation, built-in self-test, high-performance embedded test instrumentation and system-wide fault management for failure resilience.

The group is the leading partner of the Estonian research excellence centre CEBE which has the mission to improve the quality of life through technological innovations. The other two partners are Thomas Johann Seebeck Department of Electronics and Technomedicum. The research results of CEBE are related to the fields of design and test of embedded systems, biosignal processing, semiconductor technology and biomedical engineering including applications and commercial products.

The research group has published 30 papers, including 7 journal papers (1.1), 19 conference papers (3.1), and 3 PhD students (Reinsalu, Tšepurov, Aleksejev) have defended their theses in 2013.

2.2.2. Main research results in 2013

1. A new theory is being developed for diagnostic modeling of digital systems with high- and low level decision diagrams (DD). In this framework of research, **a new model of shared SSBDD (S3BDD) was developed which allows to reduce the complexity of the previous BDD models, to speed up simulation, and to minimize the complexity of fault modeling** by a novel approach of fault collapsing. The HLDD model, recently introduced by the research group, was further improved and used for automation of test program synthesis for testing of microprocessors . The main impact of the new theory is the possibility to transform logic level algorithms of diagnosis to higher system level ones with reduced complexity. Overview of the theory and new methods is presented in [5] and other papers.
2. **A new method and a scalable bug localization tool** together with a case study of pin-pointing real-world design bugs within a processor design project **was developed**. The tool has been implemented on top of a highly scalable HDL-centric open source framework zamiaCAD, developed recently in the international cooperation by the research team. The case study has been carried out on a real processor design ROBSY. The developments were supported by EU's FP7 research initiative DIAMOND which was

coordinated by the research team. The paper describing the approach is being published in the IEEE journal "Design and Test of Computers".

3. **A new method for locating design errors at the source-level of Register-Transfer Level (RTL)** hardware description language code using the High-Level Decision Diagram (HLDD) models **and correcting them by applying mutation operators was developed** [3]. The error localization is based on backtracing the mismatched and matched outputs of the design under verification on HLDDs. Experiments on a set of sequential RTL benchmarks show that the method is capable of locating the design errors injected with a high accuracy and a short run time. A majority of the errors injected in the experiments were identified as top suspects by the proposed diagnosis algorithm. It was shown that the mutation-based correction requires very small number of iterations and thus a short run-time.
4. **The first time it was shown how to prove the correctness of a digital circuit in the possible presence of multiple faults.** The traditional approach in testing of digital systems is the assumption of the presence of only a single fault. The novel idea of test groups was introduced and elaborated to cope with the problem of multiple fault mutual masking. The conditions were developed to prove that a test group is sufficient to avoid such a fault masking. A method was developed for generating test groups to avoid fault masking, and the goal is to verify the correctness of the circuit. Experimental research demonstrated the feasibility of the method and showed the ways to trade-off the test cost and robustness of the test regarding multiple faults. The results were described in two papers, including [5], and presented in 2 keynote speeches at international conferences.
5. **A new approach for assessment of diagnostic tests for automated hardware bugs localization was developed.** The method is based on calculating Hamming distances of sub-tests, it provides a measure of confidence in the localization results and allows to estimate the impact of the test on the quality of diagnosis. The approach is implemented as a part of an open-source hardware design and debugging framework zamiaCAD. Experimental results with an industrial processor demonstrate feasibility and effectiveness of the proposed approach.
6. One of the main reliability concerns in the nanoscale logic is the time-dependent variation caused by Negative Bias Temperature Instability (NBTI). It may increase the switching threshold voltage of pMOS transistors and as a result slow down signal propagation along the paths between flip-flops thus causing functional failures in the circuit. **A novel approach was proposed to identify NBTI-critical paths in respect of aging in nanoscale logic that is based on analyzing the combination of the three parameters**: delay-critical paths, gate input signal probability and the gate fan-out degree along the paths. The identified NBTI-critical paths can be used e.g. for introduction of aging sensors circuitry, rejuvenation stimuli generation, etc. The proposed approach was demonstrated on an industrial ALU circuit design.
7. Fault tolerance and fault management mechanisms (FMA) are necessary means to reduce the impact of soft errors and wear out in electronic devices. Typically, fault tolerance techniques assume certain limits in error rates when they are still applicable. Failure resilience goes beyond that by localizing and classifying faults into e.g. transient vs. permanent and critical vs. low-priority ones. **We have proposed a new general scalable fault management architecture based on the latest upcoming DFT standard IEEE P1687 IJTAG** [1]. The standard allows to create an efficient and regular network for handling fault detection information as well as to manage test and system resources as a system-wide background process during system operation.

8. **New techniques and algorithms for improving the performance of fault diagnosis by designing an optimized FMA for Systems on Chip were developed.** Novel methods for reducing fault
   detection latency and the time required for faulty resource localization have been proposed, which includes a formula for assessing the worst-case number of TCK cycles needed to perform fault diagnosis. The experimental results proved the feasibility of the proposed techniques showing logarithmic complexity of important FMA parameters with respect to the number of instruments in the SoC [1].
9. **The prerequisites for efficient application mapping on scalable Network-on-Chip (NoC) architectures were investigated** [4]. With XHiNoC a scalable mesh-based architecture has been built up in the recent years. The platform has been designed as 2D network with a memory interface for 3D DRAM stacking (via through-silicon vias). Essential for application mapping and system virtualization on a NoC-based platform are efficient distributed shared memory (DSM) coherence mechanisms and local memory architectures. Therefore efficient deadlock-free multicasting methods have been researched which are needed for memory coherence and message passing communication. Furthermore a design environment (GSNoC) for fast and cycle accurate simulation of 3D NoC systems with regular or sparse vertical links has been set up, in order to provide a quick validation of task mapping and scheduling methods. Adaptive routing methods on 3D NoCs have been researched and published.
10. **In the frame of the CEBE as a cooperation research with Biomedical Engineering Department (BME) novel algorithms were developed to increase the quality and accuracy of dialysis processes** [2]. In clinical practice, many events like patient blood pressure changes, needle displacement and concentrate depletion can trigger dialysis machine alarm, which will stop the treatment and give wrong information during optical dialysis dose monitoring. **The competences of BME in biosensorics and ATI in digital design and dependability formed the creative and synergetic basis for developing new competitive bioengineering solutions within optical dialysis monitoring**. The research results in test and diagnosis developed by RES allowed coping with the complexity of dependency problems in new innovative applications proposed by BME. New methods (AVRG, SMART and SIF) for accurate dialysis dose evaluation and extrapolation by means of Kt/V from online UV-absorbance measurements were proposed. The algorithms have a significantly positive effect on removal the disturbances and data visualization for the doctors showing substantial improvement on both chart readability and measurement precision. The output of the monitor has higher reliability and helps to avoid false prescriptions, and a high-quality medical care can be offered for the patients.

2.2.3. Five main publications of the year 2013

1. Jutman, Artur; Devadze, Sergei; Shibin, Konstantin (2013). Effective Scalable IEEE 1687 Instrumentation Network for Fault Management. IEEE Design & Test of Computers, 30 (5), pp. 26-35.
2. Karai, D. ; Fridolin, I. ; Kostin, S. ; Ubar, R. (2013). Accurate Dialysis Dose Evaluation and Extrapolation Algorithms during On-line Optical Dialysis Monitoring. IEEE Transactions on Biomedical Engineering, 60(5), pp. 1371 - 1377.
3. Raik, Jaan; Repinski, Urmas; Tšepurov, Anton; Hantson, Hanno; Ubar, Raimund; Jenihhin, Maksim. (2013). Automated design error debug using high-level decision diagrams and mutation operators. J. of Microprocessors and Microsystems, 37(4), pp. 505-513.

4. Samman, Faizal; Hollstein, Thomas; Glesner, Manfred (2013). Runtime Contention- and Bandwidth-Aware Adaptive Routing Selection Strategies for Networks-on-Chip. IEEE Transactions on Parallel and Distributed Systems, 24(7), pp. 1411 - 1421.
5. Ubar, Raimund (2013). Boolean Fault Diagnosis with Structurally Synthesized BDDs. In "Recent Progress in the Boolean Domain", Edited by Bernd Steinbach. Cambridge University Press, pp.302-331.

3. Loetelu struktuuriüksuse töötajate rahvusvahelistest tunnustustest

1. Raimund Ubar – Eesti Teaduste Akadeemia Nikolai Alumäe medal
2. Maksim Jenihhin - Boriss Tamme stipendiumikonkursi laureaat (määratud 2014, kuid 2013 tegevuse põhjal)
3. Kolme konverentsi parima artikli auhinnad:
   - H.Hantson, U.Repinski, J.Raik, M.Jenihhin, R.Ubar. Diagnosis and correction of multiple design errors using critical path tracing and mutation analysis. 13th IEEE Latin American Test Workshop, Quito, Ecuador, April 10-13, 2012. **Best Paper Award**.
   - R.Ubar, S.Kostin, J.Raik. Multiple Stuck-at-Fault Detection Theorem. The 15th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, Tallinn, Estonia, April 18-20, 2012. **Best Paper Award.**
   - T.Drenkhan, A.Tšepurov, T.Viilukas, J.Raik, A.Karputkin, M.Jenihhin, R.Ubar. Generating Directed Tests for C Programs using RTL ATPG. Workshop of High-Level and RTL testing (WRTLT-2013). **Best Paper Award.**
4. Kutsutud plenaarettekanded konverentsidele
   - R.Ubar. Fault Effect Reasoning in Digital Systems by Topological View on Low- and High-level Decision Diagrams. 4th IEEE Int. Workshop on Reliability Aware System Design and Test - RASDAT'13. Pune, India January 9-10, 2013. **Keynote talk**.
   - R.Ubar. Diagnostic Modeling of Digital Systems with Low- and High-Level Decision Diagrams. 14th IEEE Latin American Test Workshop, Cordoba, Argentina, April 2-4, 2013. **Keynote talk.**
   - R.Ubar. Topological Analysis of SSBDDs with Applications in Fault Diagnosis. Freiberg, 10th Int. WS on Boolean Problems Sept. 19-21, 2012, p. 1-16. **Keynote talk.**
   - G. Jervan. Design Methods for Dependable Many-Core Systems. Islamabad, Pakistan. 11th International Conference on Frontiers of Information Technology. December 16-18, 2013. **Invited talk.**

4. Loetelu struktuuriüksuse töötajatest, kes on välisakadeemiate või muude oluliste T&A- ga seotud välisorganisatsioonide liikmed

1. G. Jervan on IEEE vanemliige (ühtlasi ka Eesti sektsiooni aseesimees ja arvutiteaduste kapiitli esimees)
2. A.Jutman, R.Ubar ja G. Jervan on Euroopa Inseneerihariduse Assotsiatsiooni EAEEIE Nõukogu liikmed
3. R.Ubar ja G. Jervan on Ülemaailmse Testi Tehnoloogia Tehn. komitee TTTC liikmed
4. R.Ubar ja G. Jervan on Euroopa Testi Tehnoloogia Tehn. komitee ETTTC liikmed
5. R. Ubar on IEEE Computer Science Golden Core liige ja Harkovi Rahvusliku Raadiotehnika Ülikooli auprofessor

5. Aruandeaastal saadud T&A-ga seotud tunnustused (va punktis 3.2.3 toodud tunnustused), ülevaade teaduskorralduslikust tegevusest, teadlasmobiilsusest ning hinnang oma teadustulemustele.

1. 2013. a. Lisandunud uued projektid:
   - ICT COST Action IC1204 „TRUDEVICE – Trustworthy Manufacturing and Utilization of Secure Devices“ (2012-2016), juhtkomitee liige J. Raik, partnerid 20st riigist.
   - FP7-ICT-2013-11 STREP projekt BASTION: „Board and SoC Test Instrumentation for Ageing and No-Failure-Found“. Partnerid: Infineon, ASTER Technologies, Testonica Lab, University of Twente, Lund University, Hamm-Lippstadt, Politechnico di Torino. Projekti kestus: 1.01.2014-31.12.2016.
   - IUT19-01: „Usaldusväärsed mitmetuumalised arvutisüsteemid“. Teema juht: Jaan Raik.
2. Teaduskorralduslik tegevus
   - Artur Jutman oli rahvusvahelise konverentsi Nordic Test Forum 2013, Tallinnas, juhtkomitee liige ja peakorraldaja
   - G. Jervan oli konverentsi ReCoSoC 2013 programmikomitee juht; HiPEAC Computing Systems Week 2013 peakorraldaja.
   - P. Ellervee oli Norchip 2013 konverentsi korralduskomitee liige ja Baltic Electronics Conference 2012 ase-esimees.
   - Korraldati rahvusvaheline seminar BELAS'2013. Esimees: R.Ubar, Programmikomitee esimees: J.Raik, Suvekooli juhtkomitee esimees: M.Jenihhin.
   - Maksim Jenihhin on konverentsi LATW Publication Chair
   - Jaan Raik oli konverentsi "Design&Diagnostics of Electronic Circuits&Systems" DDECS'2013 aseesimees ja konverentsi „IEEE European Test Symposiumi - ETS'2013“ Student Activity sektsiooni esimees
   - Th.Hollstein oli konverentsi „Smart SysTech 2013: European Conference on Smart Objects, Systems and Technologies“ üldjuht.
   - R.Ubar oli konverentsi "East-West Design-and-Test Symposiumi" EWDTS'2013 aseesimees.
   - R. Ubar on Eesti TA uurija-professorite valimiskomisjoni liige
   - Loengutega välismaal esinesid A.Jutman (TU Darmstadt, TU Ilmenau), R.Ubar (TU Darmstadt, IIT Bombay), G.Jervan ja Th.Hollstein (Turku Ülikool)
   - G. Jervani külalisloengud Hiina ülikoolides: University of Science and Technology, Beijing, Zhejiang University of Science and Technology, Hangzhou, University of Shanghai for Science and Technology (kolm 2-päevast tutoriali).
   - G.Jervani loengute seeria Macau ja Hong Kongi ülikoolides.
   - Th. Hollsteini külalisloeng ülikoolis Ruhr-Universität Bochum.