THESIS ON INFORMATICS AND SYSTEM ENGINEERING C63

Analog Front End Components for Bio-Impedance Measurement: Current Source Design and Implementation

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Declaration:

Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for any academic degree.

/Argo Kasemaa/

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INFORMAATIKA JA SÜSTEEMITEHNIKA C63

Bioimpedantsi mõõteseadme analoogosa komponendid: vooluallika disain ja realisatsioon

ARGO KASEMAA

TTÜ
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ABSTRACT

The thesis describes the efficient CMOS technology based current source for bio-impedance measuring system and its layout realization with reduced circuit complexity. Square wave excitation current is preferred in energy constrained and embedded environment. It has been shown that by shortening the square waves, spectral purity of the excitation signals can be drastically improved. Further improvement can be achieved by introducing limited number of additional equally spaced current levels. The basic idea of such a solution is that by suitably adding several simple shortened pulses together some of the high energy harmonics are either further reduced or eliminated. This multilevel signal can be easily generated digitally and it enables simpler digital processing involving only additions and shifting. On the other hand required extra circuitry for multiple current levels should not eliminate main advantages of square wave excitation, such as reduced complexity and low consumption. Proposed solution improves the power consumption and reduces the complexity of the system as a whole compared to more generic approach. The current source output will be the shortened multilevel square wave signal. The output current value can be selected from range from 5 to 100μA. The main advantage of this method is greater efficiency because the overall power consumption is only about 1.5 times higher compared to the current flowing into the load and for measuring cycle only one or two pairs of switchable current mirrors will be activated to drive the H-bridge.

KOKKUVÕTE

Käesolev väitekiri kirjeldab CMOS tehnoloogial põhinevat vooluallikat, kui ühte osa bioimpedantsi mõõteseadmest, ja selle vähendatud keerukusega seadme realiseerimist ränikristallis. Energiatõhusates sardsüsteemides on eelistatud ergutusvooluks nelinurksignaali kasutamine. On tõestatud, et lühendatud nelinurksignaali puhul paraneb ergutussignaali spekter oluliselt. Lisaks on võimalik vähendada signaali spektris kõrgemate harmooniliste taset modifitseerides lühendatud nelinurksignaali: lisades sinna juurde astmeid või lõigates kolmenivoolisest signaalist tükke välja. Kogu sellise tegevuse põhiidee on see, et sellised lihtsad võtted võimaldavad signaali spektris kindlaid kõrgemaid harmoonilisi kas üldse välistada või nende taset oluliselt vähendada. Sellist mitmenivoolist signaali saab digitaalselt väga lihtsalt tekitada ja samuti on signaali töötlus kergem. Teisest küljest mitmenivoolise voolusignaali saamiseks vajalikud lisaahelad ei tohiks vähendada ergutusvooluks kasutatava nelinurksignaali eeliseid nagu seadme väiksem keerukus ja võimsustarve. Antud töös esitatud lahendus parandab energiatarvet ja vähendab süsteemi keerukust võrreldes tavapäraselt levinud lahendustega. Loodud vooluallika väljundiks on lühendatud nelinurksignaal ja väljundvoolu väärtusi saab valida vahemikust 5 kuni 100 μA-t. Põhiline eelis seisneb selles, et antud meetod tagab suurema energiatõhususe, sest üldine seadme voolutarve toiteallikast on umbest 1.5 korda suurem sellest voolust, mis kulgeb koormuses. Lisaks kasutatakse väljundiks oleva H-silla juhtimiseks ainult neid vooluallikaid, mida vajatakse vajaliku väljundvoolu saamiseks ning lülitatavaid vooluallikaid aktiveeritakse vaid lühikesteks mõõtetsükliteks.

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CONTENT

INTRODUCTION

The thesis presents the author's research work carried out during his PhD at the Department of Electronics of Tallinn University of Technology on the field of impedance measurement. This work gives a design overview of an efficient CMOS technology based current source realization and layout design. The current source layout design needs good matching, the geometry and temperature influence has been analyzed and the optimal geometrical structure will be suggested.

Measure by which system under investigation impedes alternating current (AC) flow can be used to characterize its properties. Measurement of low-level voltage response and its changes is usually conducted by using lock-in approach. Injecting known constant current and measuring the response voltage is generally preferred method. Classically sinusoidal excitation is used and Fast Fourier Transformation (FFT) or similar takes care of spectral separation. It enables determination of magnitude and phase of the complex response signal compared to the excitation signal, and gives relatively good insight into network under investigation. Measurement accuracy depends on the quality of the excitation signals, analog circuitry and on signal processing tools and algorithms. Energy and space constraints limit usage of analog components, and put sinusoidal signals and required signal processing solutions into unfavorable position. Replacing sinusoidal signals with their simpler square wave counterparts enables drastic reduction in energy consumption and complexity, but carries a penalty of energy loss and measurement errors introduced by high harmonic content. Systematic errors introduced by higher harmonics of simple square wave signals can be drastically reduced by slightly modifying the waveform. In case of shortening the excitation and reference signals by 30° and 18° respectively.

The three level shortened square waves' technique allows to reduce the higher harmonics, especially the lower end of higher harmonics. This multilevel signal can be easily generated digitally and it enables simple digital processing. An efficient CMOS technology based current source can be designed to work with such nontraditional waveforms. The current source consists of bias circuit, switchable current mirrors to select different current ranges and H-bridge current output stage. Proposed solution improves the power consumption and reduces the complexity of the system as a whole compared to more generic approach. The current source output will be the shortened multilevel square wave signal. The output current value can be selected from range from 5 to 100 μA. The main advantage of this method is greater efficiency because for measuring cycle only

one or two pairs of switchable current mirrors will be activated to drive the H-bridge.

Using discrete components a simple four bipolar transistor bridged circuit has been tested and implemented. This circuit showed relatively good results. The maximum working speed at maximum output current was up to 100 kHz, but at lower output currents not more than 10 kHz. In our case the goal was to improve the bridged circuit current source design and achieve speeds up to 1 MHz, also at lower output currents.

CHAPTER 1: DESCRIPTION OF THE PROBLEM

Introduction

In many cases we will regard our biological material, together with the necessary electrode arrangements, as an unknown "black box." By electrical measurement we want to characterize the content of the box (we do not have direct access to the key to open the lid!). We want to use the data to describe the electrical behavior, and perhaps even explain some of the physical or chemical processes going on in the box, and perhaps discern the electrode and tissue contributions. The description must necessarily be based on some form of model, for example, in the form of an equivalent electric circuit, mimicking measured electric behavior.

So said in their book [1] a basic problem is that always more than one model fit reasonably the measured electric behavior. The equivalent circuit is the tool of the electronic engineers and facilitates their interpretation of the results.

The black box may be assumed to "contain" the whole body, a part of the body, just an organ, or just a cell, together with the electrodes. The black box may be considered to contain the real tissue with electrodes for excitation and response measurement, or our model in the form of an electric network as a combination of lumped (discrete) electrical components. The network may be with two, three or four external terminals (cf. the number of electrodes used). A pair of terminals for excitation or recording is called a port.

The four external variables of a two-port black box are *v1* and *i1* (first port), *v2* and *i2* (second port), Fig. 1.1. There are four possible ratios: *v1/i1*, *v2/i2*, *v1/i2* and *v2/i1*. These ratios may be inverted so actually there are eight possible ratios. If the signals are sine waves, most of them have their special names.

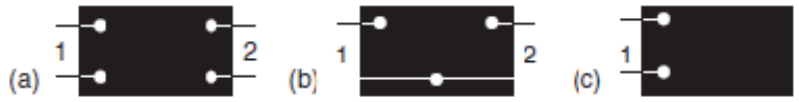


Fig. 1.1. Black boxes. The two boxes (a) and (b) allow for transfer parameters from one port to the other. Box (c) is a one-port, two-terminal box with only driving point parameters possible.

If a chosen ratio is current-to-voltage, the ratio is called admittance. It is measured in siemens (S), and can be obtained directly by reading current when a constant amplitude AC voltage is applied ($Y = i/v$). If the ratio is voltage-to-

current, the ratio is called impedance. It is measured in Ω, and can be obtained directly by reading voltage when a constant amplitude current is applied ($Z = v/i$). More detailed description of admitance and immitance can be found in [1].

Capacitive impedance can be written in its complex form as: $\dot{Z} = Re\dot{Z} + jIm\dot{Z}$, Fig. 1.2. Impedance of the simple series RC circuit can be expressed as $\dot{Z} = R + 1/j\omega C = R - j/\omega C$. When $Re\dot{Z} = R$, and $Im\dot{Z} = -1/\omega C$ are known at one frequency it is possible to calculate them, and consequently also impedance $\dot{Z}$ at any arbitrary frequency, since impedance values on complex plane draw strait line parallel to imaginary axis at the distance of R from it, starting at $-j\infty$ when $\omega = 0$ and ending at real axis at R when $\omega = \infty$.

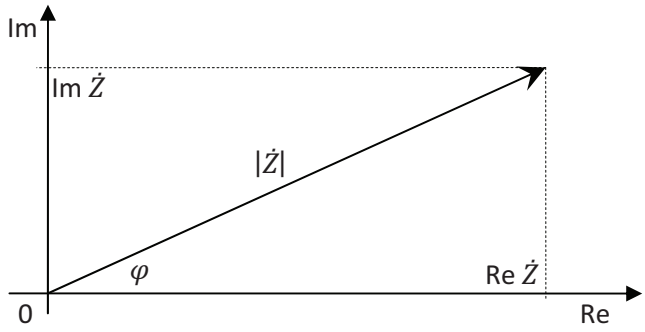


Fig. 1.2. The impedance vector and its real and imaginary parts.

Therefore the phase angle is negative. This means that the voltage as dependent variable is lagging the current, which is general rule in capacitively behaving circuit, since $i = C(du/dt)$. When drawing phasor diagram for capacitive circuit it is often convenient to mirror image over real axis, and therefore move image into first quarter. It is denoted by – sign near imaginary axis. Things get somewhat more complicated when three element circuit is considered, Fig. 1.3.

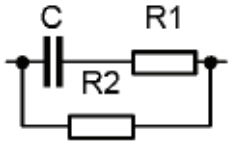


Fig. 1.3. Three element RC circuit, commonly used to discuss impedance of the tissue, also as Cole type A circuit.

In order to characterize circuit it is not enough anymore to make one measurement at single frequency. On phasor diagram frequency dependent impedance vector of the series connection of resistor and capacitor with parallel resistor is drawing a semicircular line, Fig. 1.4.

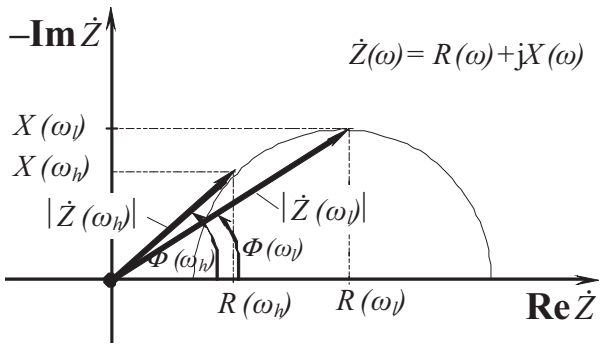


Fig. 1.4. The phasor diagram of the Fig. 1.3 circuit at two frequencies, low ω_l and high ω_h.

The frequency response of the three-component electrical equivalent in Fig. 1.3 can be expressed with acceptable accuracy through the impedances $\dot{Z}(\omega_l)$ and $\dot{Z}(\omega_h)$ that are measured at two frequencies: low and high. It is important to emphasize that the impedance variations at a decade or more of distant low and high frequencies (ω_l and ω_h) are also essentially different. Thus, the multisite and multifrequency bioimpedance information has a substantial diagnostic value.

Biological application

First explanation how the cellular structure of biological material can be connected with equivalent circuits can be contributed to Hugo Fricke and Sterne Morse [2]. As Kenneth Cole explains [3] “their measurements of the resistance and capacity of suspensions of red blood cells at various frequencies could accurately fitted to a circuit of type A (Fig. 1.3), where they thought of *R2* as due to the suspending medium, *R1* to interiors of the corpuscles, and *C* to the capacities at their surfaces”.

Drawing wider picture Herman P. Schwan says [4] “Fricke, Cole and Curtis laid the basis of our understanding of the β-dispersion. They did this by applying the relevant Maxwell equations to cell suspensions surrounded by membranes”.

Schwan himself laid the foundations for understanding of an α-dispersion, and γ-dispersion. Motivation behind existence of several distinct dispersions is based on a fact that different mechanisms are behind the behavior of biological material impedance at vastly different frequencies. Appearing between frequencies from millihertz to roughly some hundred hertz an α-dispersion being probably the most controversial, and needing further research and elaboration. As explained by Grimnes and Martinsen [1] it is mostly due to counter ion effects (perpendicular or lateral) near the membrane surfaces, active cell membrane effects and gated channels, intracellular structures (e.g. sarcotubular

system.), ionic diffusion, and dielectric losses (at lower frequencies the lower the conductivity). Maxwell–Wagner effects appearing in β-dispersion deal with processes at the interfaces between different dielectrics. If Fricke's model is extended towards increasing frequency smaller and smaller entities have their impact on the distribution from passive cell membrane capacitance, to intracellular organelle membranes, and protein molecule response. Whole β-dispersion can be observed from kilohertz to ca 100 MHz, and as explained is tightly related cellular and sub cellular structure of the biological materials. Lastly γ-dispersion from 100 MHz to 100 GHz is mostly due to dipolar mechanisms in polar media such as water, salts and proteins.

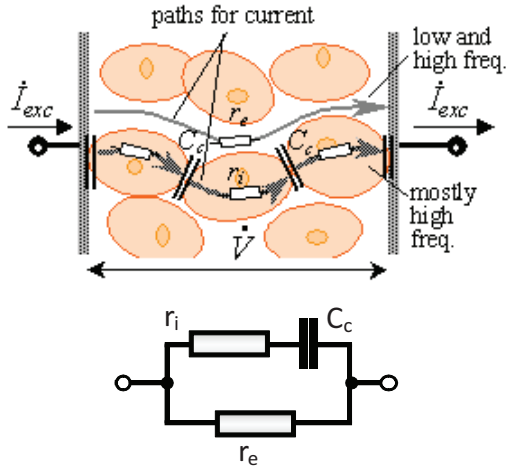


Fig. 1.5. Derivation of the impedance of the typical cellular tissue sample, where r_i is an intracellular resistance, r_c is an extracellular resistance, and C_c is capacitance between cellular membranes [5].

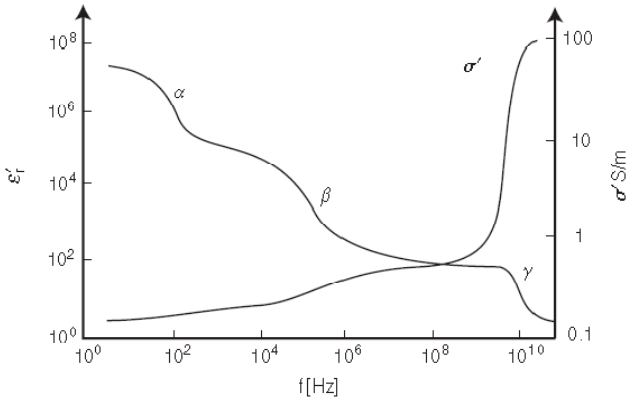


Fig. 1.6. Classical picture illustrating α, β, and γ dispersions of inphase conductivity and permittivity, as clearly separated Cole–Cole-like systems. Permittivity in biological materials typically diminishing with increasing frequency [1].

In spite of the long study of electrical properties of the biological materials Schwan while describing advanced methods for measurement still makes an important statement [4]: “The problem with most of these techniques is the complexity of the human body and its distribution of tissues of varying conductivity and permittivity, anisotropic properties at that. Even with sophisticated numerical techniques, it is almost impossible to do justice to this situation. The impedance signals received depend critically on this complex arrangement and simple models will not suffice”. In any case impedance of the human tissue varies largely both in frequency, and also depending which tissue and how is measured. Some indications for expected parameters can be found in literature, like [6]. Electrical impedance $\dot{Z}$ of biological objects or electrical bioimpedance (EBI) is measured with the aim to get information about the biological processes taking place inside the living organism. From the general point of view of the measurement, there is no significant difference between the EBI and other impedances, like the impedance of chemical cells, etc. But as biological objects are structurally complicated, the bioimpedance has also complicated equivalent circuit. Situation is further complicated by the fact, that it is possible to measure directly only the active and reactive components R and X of the complex impedance (or G and B of the complex admittance), which are mutually in quadrature. To be used for mathematical conversions R and X must be measured with required accuracy.

There is another factor which is rarely mentioned in connection with impedance of biological objects, but nevertheless affects measurement results – temperature. Any and all materials and substances change their electrical parameters as a function of temperature, and even though subject under investigation is ultimately a human, and therefore homoeothermic, keeping more or less stabile temperature, temperature still varies, and will influence measurement results. Even more when patient in unhealthy state is investigated. It warrants simultaneous temperature measurements in order to make comparison between different tests.

Theoretical background

The time constant

Immittance theory is based on sinusoidal excitation and sinusoidal response. In relaxation theory (and cell excitation studies) a step waveform excitation is used, and the time constant is then an important concept. If the response of a step excitation is an exponential curve, the time constant is the time taken to reach 63% of the final, total response. Let us, for instance, consider a series RC connection, excited with a controlled voltage step, and record the current response. The current as a function of time $I(t)$ after the step is: $I(t) = (V/R)e^{-t/RC}$, the time constant $\tau = RC$, and $I(\infty) = 0$.

However, if we excite the same series *RC* circuit with a controlled current step and record the voltage across the *RC* circuit, the voltage will increase linearly with time ad infinitum. Clearly the time constant is dependent not only on the network itself, but on how it is excited. The time constant of a network is not a parameter uniquely defined by the network itself. Just as immittance must be divided between impedance and admittance dependent on voltage or current-driven excitation, there are two time constants dependent on how the circuit is driven. The network may also be a three- or four terminal network. The time constant is then defined with a step excitation signal at the first port, and the possibly exponential response is recorded on the second port.

The step waveform contains an infinite number of frequencies, and the analysis with such non-sinusoids is done with Laplace transforms.

DC compared with a sine wave AC with $f \rightarrow 0$

When a sine wave frequency approaches 0 Hz, corresponding to a period of, for example, an hour of more, the signal may for a long time be regarded as a slowly varying DC. Strong DC polarization effects may have time to develop at the electrodes, and capacitive susceptance is very small according to $B = \omega C$.

In order to maintain linear conditions in electrolytic systems, the signal amplitude must be reduced to 0 as $f \rightarrow 0$. Except in the bulk of an electrolyte, DC conditions are therefore virtual unobtainable in electrolytic systems (cf. also the Warburg impedance concept). This is well illustrated with the logarithmic frequency scale, where both infinitely high and infinitely low frequencies are equally off scale and unattainable. With electronic (not ionic) conduction and ordinary resistors, perfect DC conditions represent no difficulty, and these can therefore only be idealized models of electrolytic systems.

Periodic waveforms, Fourier series of sine waves

A periodic waveform repeats itself exactly at regular time intervals (the period *T*). It is predictive: at any moment in the future we can foresee the exact value.

According to Fourier, any periodic waveform can be considered to be the sum of a fundamental sine wave of frequency $f_1 = 1/T$, and sine waves at certain discrete frequencies, the harmonics ($2f_1$, $3f_1$, $4f_1$, and so on). A periodic waveform is an idealized concept, the waveform is to have lasted and to last forever. At the time we start and stop it, other frequency components than the harmonics appear as transients.

The sine wave is a very special periodic waveform in the sense that it is the only waveform containing just one frequency: the fundamental frequency. Why has just the sine wave such special qualities?

It is derived from the circle, Fig. 1.7, it is the projection of a rotating radius (cf. the phasor). If the rotation is steady, the waveform is sinusoidal. A sinusoidal is characterized by its frequency f (Hz, periods per second) or the period $T = 1/f$ (second). Angular frequency ω must be used for trigonometric functions and to emphasize the relationship with the angle of the rotating radius. $\omega = 2\pi f = 2\pi/T$ is the number of rotations (in radians or degrees) per second. T is the time of one complete rotation. $\varphi = \omega t$ is the angle of rotation during the time t. A frequency independent phase shift or a reference value φ_0 may be added: $\varphi = \omega t + \varphi_0$.

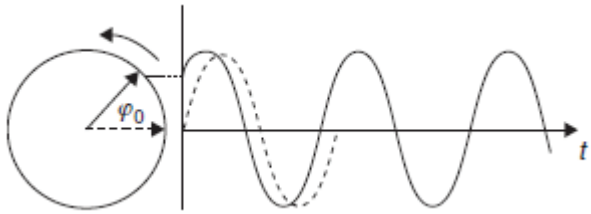


Fig. 1.7. The sine wave, with a reference sine wave stippled.

If the sine wave is symmetrical around 0, it has no DC component and is described by the equation:

$$v(t) = V_0 \sin(\omega t + \varphi_0)\,; \tag{1.1}$$

$$\int v dt = -V_0 \cos(\omega t + \varphi_0) = -V_0 \sin(90^\circ - \omega t - \varphi_0)\,; \tag{1.2}$$

$$dv/dt = V_0 \cos(\omega t + \varphi_0) = V_0 \sin(90^\circ - \omega t - \varphi_0)\,. \tag{1.3}$$

The time derivative as well as the time integral of a sine wave is also a sine wave of the same frequency, but phase-shifted 90°. The relationship between a sine wave and the circle is seen more directly in the complex notation of a radius r rotating around the origin in the Wessel diagram:

$$r(t) = r_0 e^{j\omega t + \varphi_0} = r_0 \left[\cos(\omega t + \varphi_0) + j \sin(\omega t + \varphi_0)\right]. \tag{1.4}$$

As the time derivative of an exponential is the same exponential, then $\partial(e^{j\omega t})/\partial t = j\omega e^{j\omega t}$. That is why integration and derivation in the equations describing the behavior of electrical circuits can be replaced by algebraic operations with the $j\omega$ instead of the $\partial/\partial t$. This is under the assumption that all signals are sine waves of the same frequency.

A phasor and a sine wave are given with respect to some reference sine wave. In Fig. 1.7 the reference is stippled, and the waveform of interest leads the reference by about 45°.

The peak value is called the amplitude V_0, φ is the phase angle. To define φ we must define a reference sine wave, for instance the known excitation signal. Although the mean value of a full period is 0, it is usual to quote the mean of half a period: $2V_0/\pi$. The RMS value is $V_0/\sqrt{2}$.

The sum of a fundamental sine wave and its harmonic components: Fourier series

A periodic waveform can be created by a sum of sine waves, each being a harmonic component of the sine wave at the fundamental frequency determined by the period.

This is illustrated Fig. 1.8(a), showing the sum of a fundamental and its third and fifth harmonic components. It indicates that uneven harmonic components may lead to a square wave, with a precision determined by the number of harmonic components included.

Fig. 1.8(c) shows the frequency spectrum of the waveform. It is a line or discrete spectrum, because it contains only the three discrete frequencies. Continuously repetitive waveforms have line spectra, their periodicity is composed only of the fundamental and its harmonic components.

Fourier formulated the mathematical expression for the sum of the fundamental and its harmonics. The condition is that a fundamental period of a waveform *f(t)* can be determined, and that the waveform *f(t)* is extended outside its defined interval so that it is periodic with period 2π:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos n\omega_1 t + b_n \sin n\omega_1 t), \tag{1.5}$$

where a_n and b_n are the amplitudes of each harmonic component n, a_0 is the DC component, and ω_1 the angular fundamental frequency defining the period 2π.

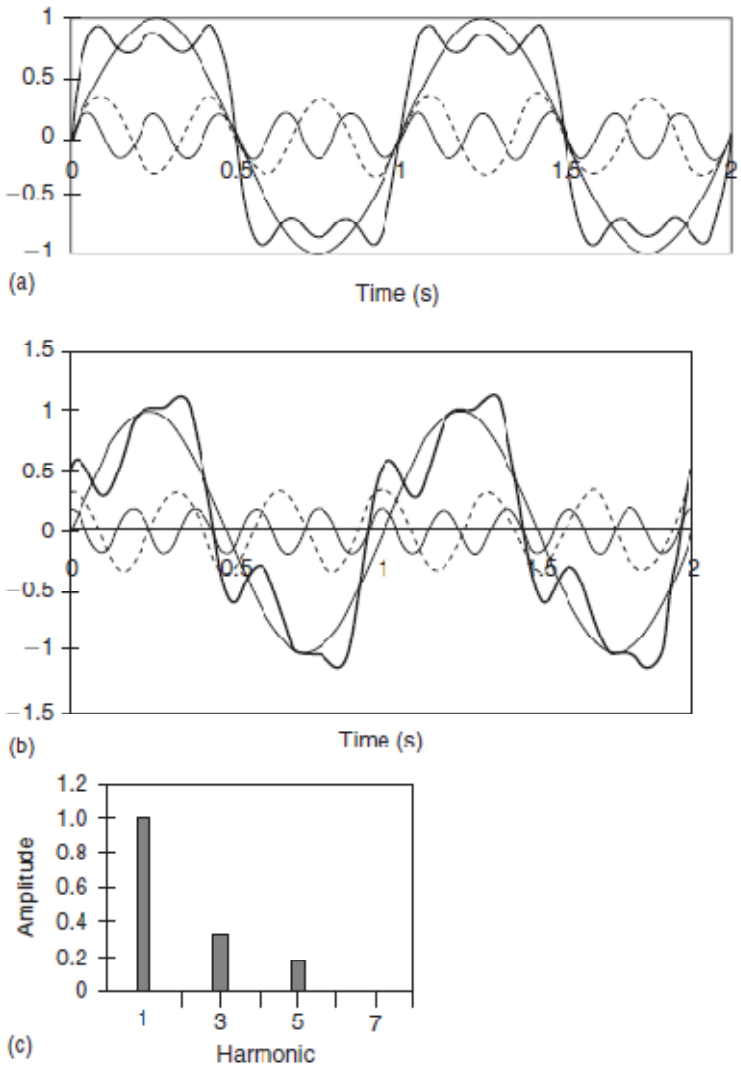


Fig. 1.8. Summation of harmonic sine waves, waveform dependence of phase relationships. Amplitude of fundamental sine wave = 1. Time domain: (a) in-phase harmonics, (b) phase-shifted harmonics. (c) Amplitude magnitude line frequency spectrum, equal for both cases [1].

According to the Fourier series eq. (1.5), any periodic waveform is the sum of a fundamental sinusoid and a series of its harmonics. Notice that in general each harmonic component consists of a sine and cosine component. Of course either of them may be zero for a given waveform in the time domain. Such a waveform synthesis (summation) is done in the time domain, but each wave is a component in the frequency domain. The frequency spectrum of a periodic

function of time *f(t)* is therefore a line spectrum. The amplitude of each discrete harmonic frequency component is:

$$a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t)\cos(n\omega_1 t)dt\,; \tag{1.6}$$

$$b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} f(t)\sin(n\omega_1 t)dt\,; \tag{1.7}$$

$$A_n = a_n + jb_n\,; \tag{1.8}$$

$$A_n = \sqrt{a_n{}^2 + b_n{}^2}\,; \tag{1.9}$$

$$\varphi = \arctan(b_n / a_n)\,. \tag{1.10}$$

Because the waveform is periodic, the integration can be limited to the period interval 2π as defined by ω_1. However, the number n of harmonic components may be infinite. The presentation of a signal in the time or frequency domain contains the same information; it is a choice of how data is to be presented and analyzed.

Problem description

Introduction to shortened square waveform signals

According to definition electrical impedance *Z*, or simply impedance, describes a measure of opposition to a sinusoidal alternating current (AC). In its complex form $\dot{Z} = \dot{V}/\dot{I} = R + jX$, and it is frequency dependent. It is therefore evident from definition that impedance can be, and in fact should be, measured with sinusoidal excitation current. For all practical signal processing tasks it is possible to state that any real signal can be constructed from sinusoids. In signal processing terms all non sinusoidal signals with fundamental frequency do have higher sinusoidal harmonics.

But before going any further is probably good to answer the question why it is useful to consider other then sinusoidal excitations. For a single frequency measurement simpler hardware and simpler signal processing, and ultimately lower cost and energy consumption can be the moving factors. While sinusoidal excitation is best by definition several alternative waveforms can be considered with acceptable results. Simplest alternative is square wave signal or signal which can be described by the Rademacher function (Fig. 1.9). One of the

therefore possible definitions of the Rademacher function $f_n(x)$ is the sign of $\sin(2^n\pi x)$, for a non-negative integer n. For $n = 1$ $\mathcal{R}(t) = \text{sign}(\sin(2\pi t))$, where $\mathcal{R}(t)$ denotes a Rademacher function.

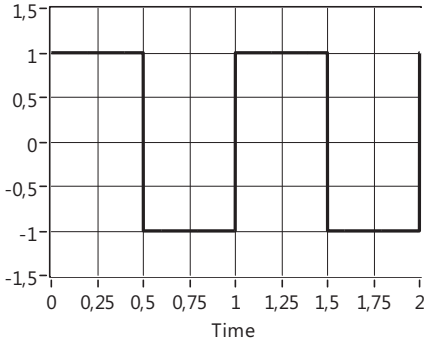


Fig. 1.9. The Rademacher function of n = 1, or just simply an odd square wave.

In order to see the difference between square wave and sinusoid it is convenient to consider the Fourier series of the square wave with amplitude 1. Since function is odd, i.e. $-f(x) = f(-x)$, Fourier series of the function will contain only sinusoidal members (frequency $f = \omega/2\pi$):

$$f(t) = \frac{4}{\pi}\sum_{n=1}^{\infty}\frac{\sin((2n-1)\omega t)}{2n-1} = \frac{4}{\pi}(\sin(\omega t) + \frac{1}{3}\sin(3\omega t) + \frac{1}{5}\sin(5\omega t) + \cdots). \tag{1.11}$$

Unfortunately severe problems appear if measurements with square waves are conducted. The measurement is no longer conducted on single well defined frequency, but instead produces results also on higher harmonics. It could be largely ignored if during signal processing multiplication is conducted with sinusoidal signals, unfortunately as it was discussed above, often it is accomplished with same rectangular signal instead, and energy form all the higher harmonics is summed to the fundamental, and becomes undistinguishable. Also spectral impact from non linearity's of the object (or apparatus) cannot be separated from desired response signal. Spectra resulting from such a multiplication can be seen on Fig. 1.13 with dotted line. There is another way of looking at how the errors appear [9]. Let's consider phase sensitivity characteristics of the synchronous demodulator (SD):

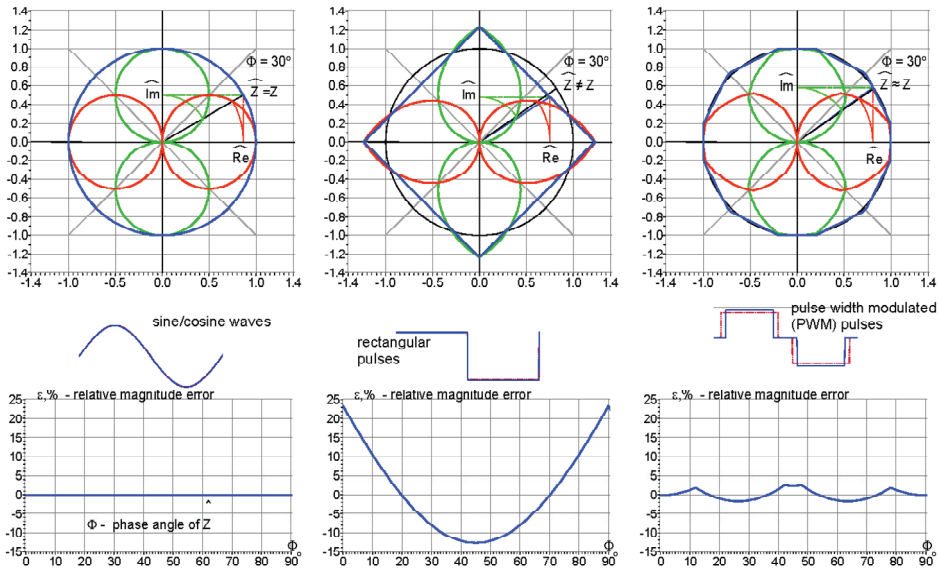


Fig. 1.10. Quality of synchronous demodulation in case of different signal waveform. From left to right sine wave, square wave, and modified square wave.

From Fig. 1.10 it is clear that synchronous demodulator produces different results in case of fully square wave system and in case of sinusoidal system. Fortunately there is very simple method for reducing errors introduced by higher harmonics.

Let's consider sum of two square waves with same frequency and amplitude, one of them shifted in phase by β degrees, and another $-\beta$ degrees. Such a double shift is preferable, since resulting function is again odd. In signal processing odd functions are more natural, because negative time is usually meaningless, and signals start at $t = 0$. Care must be taken that in many mathematical textbooks, and more importantly in different programs, even functions are considered instead.

Should the summary phase shift 2β be equal to the half period or odd multiply of half periods of any higher harmonic such a harmonic will be eliminated from the signal, since sum of to equal sinusoids with 180 degree shift is zero. Main difference with simple square wave is in appearing third level with zero value, so it is reasonable to call them shortened square waves. More generally spectra of these signals can be derived from Fourier series:

$$f(t) = \frac{4}{\pi}\sum_{n=1}^{\infty} \frac{\cos((2n-1)\beta)\sin((2n-1)\omega t)}{2n-1} = \frac{4}{\pi}(\cos\beta\sin(\omega t) + \frac{\cos 3\beta}{3}\sin(3\omega t) + \frac{\cos 5\beta}{5}\sin(5\omega t) + \cdots +). \quad (1.12)$$

Two of these shortened square waves are of special interest. In order to remove 3rd and 5th harmonics from the signal (as they cause most significant errors) 18 degree and 30 degree shifts are useful. First of them is void of 5th, 15th, etc harmonics, and second 3rd, 9th, 15th, etc. harmonics. Both of these three level signals with amplitude A are shown on Fig. 1.11. The third level does not introduce much added complexity from signal processing view. Both generation with digital logic, and also synchronous rectification with CMOS switches is straightforward [10].

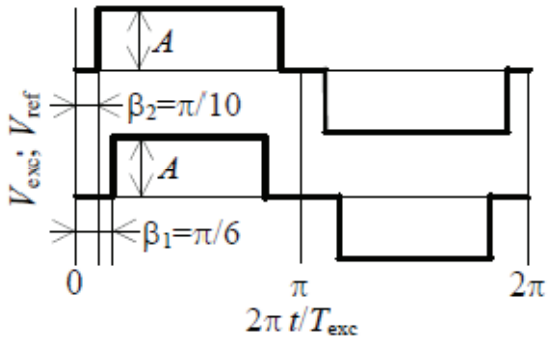


Fig. 1.11. 18 and 30 degree shortened signals with amplitude A [10].

If one of them is used as excitation signal and other as rectifying reference result will be much cleaner spectrally then it was with simple square waves, Fig. 1.13 white rectangles. These two waveforms were chosen, because complete elimination of certain harmonics was desired.

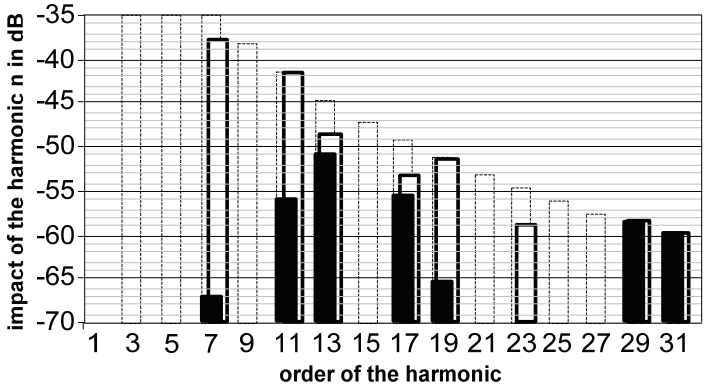


Fig. 1.13. Impact of the harmonics, in case of ordinary square wave (dotted line), simple shortened square wave (white boxes), and multilevel shortened square wave [11].

If 18 degree and 30 degree shortened signals are considered, then apparently there are still coinciding higher harmonics in both signals. Could the same summing procedure produce further improvement without much added

complexity, if more square waves are added together? The answer is yes. If third summed waveform is added into palette, namely 42 degrees shifted then combination of these three gives very promising results. Three interesting and still simple signals are considered as combinations of previously mentioned summed signals. First and most obvious is sum of 18, 30, and 42 degrees shortened signals with signs 1, –1, and 1. Resulting waveform is on Fig. 1.14, and spectra of the result is on Fig. 1.15. Result is already remarkably cleaner compared to simple square wave. It could be one of the candidates for use in demodulators, besides simpler 22.5 degree shortened square wave, when excitation is sinusoidal.

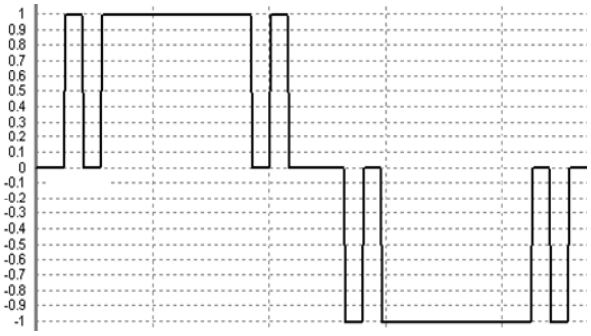


Fig. 1.14. Resulting waveform from summing of three shortened signals with weights 1, –1, and 1 [11].

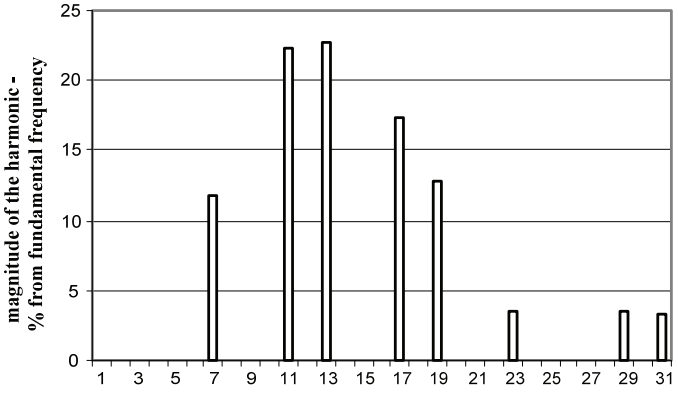


Fig. 1.15. Spectra of the signal on Fig. 1.14 [11].

If on the other hand excitation is also shortened square wave, then following pair of signals is suggested [12]. First of them is sum of all three components with coefficients 1, 1, and 1, Fig. 1.16. Spectra of this summed signal is on Fig. 1.17.

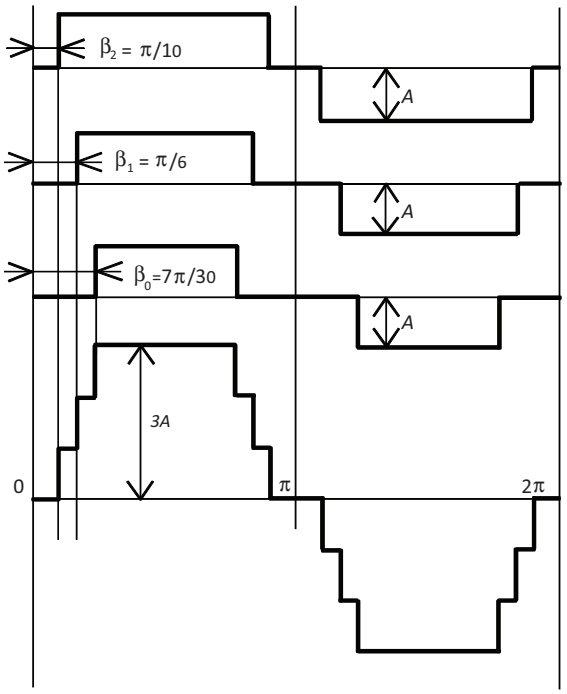


Fig. 1.16. Sum of three shortened waveforms with coefficients 1, 1, and 1 [11].

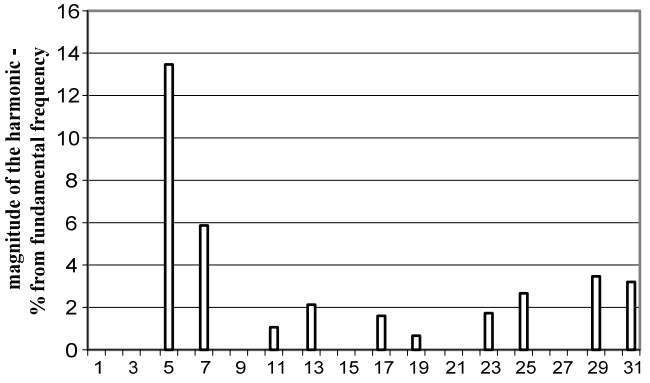


Fig. 1.17. Spectra of the signal on Fig. 1.16 [11].

Suitable counterpart summed with coefficients 2, –1, and 1 is on Fig. 1.18, and spectra on Fig. 1.19.

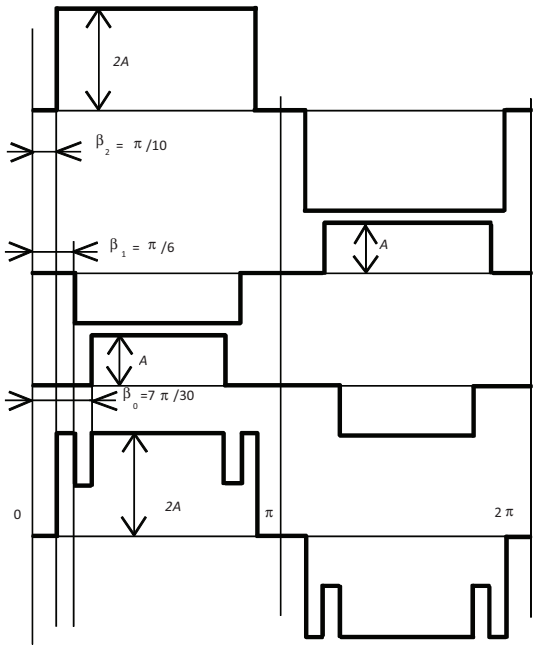


Fig. 1.18. Sum of three shortened waveforms with coefficients 2, –1, and 1 [11].

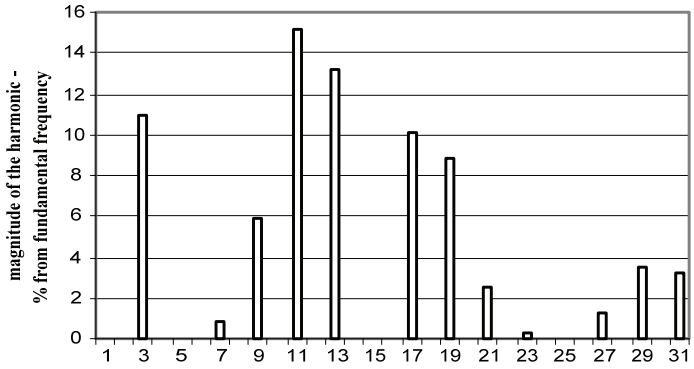


Fig. 1.19. Spectra of the signal on Fig. 1.18 [11].

Comparison of the multiplication results (Fig. 1.13) shows significant improvement over previous result. Nevertheless same clock speed penalty still applies as with simpler solution.

The basic measuring circuit

The basic measurement circuit needs a high output impedance and high frequency current source, which current is flowing into load, and the voltage response on the load is measured using high impedance differential amplifier. There are many different active current source designs. Usually they are based on operational amplifiers. One of the known designs from early sixties is Howland current source. It was invented by Bradford Howland from MIT around 1962 [14]. Historically it has been described as very clever circuit which is almost useless [15]. Nevertheless, several modifications of Howland circuit have been used successfully for impedance measurement [16], [17], [18] and many others. Second common type is the so called load in the loop circuit, where impedance under measurement is essentially placed in the feedback loop of an inverting amplifier, and the current in the load is proportional with the input voltage of the amplifier [19], [20], etc. General discussions on wide bandwidth current source parameters can found for example in [21], and discussions of the load in the loop circuits in [20]. Common to active current sources is a differential output [22] and the maximal achievable upper frequency limit is around 10 MHz in case of better circuits [23]. Output impedance while very good at lower frequencies, and can reach tens of mega ohms, will fall into few kilo ohm range at high frequencies, and the phase is shifted.

In our case we need for the measuring circuit a floating current source what can generate shortened square wave signal. The best solution seems to be the H-bridge configuration – four switched current sources are driving the load. Using discrete components a simple four bipolar transistor bridged circuit has been tested and implemented [24]. This circuit showed relatively good results. The maximum working speed at maximum output current was up to 100 kHz, but at lower output currents not more than 10 kHz.

In our case the intent was to improve the bridged circuit current source design and achieve speeds up to 1 MHz, also at lower output currents.

CHAPTER 2: DESIGN OF THE CIRCUIT

To design low power current exciter for generating shortened square waves different solutions can be used, but the simplicity of the electrical circuit is one major standpoint for the optimal circuitry solution. The solution with differential output seems to be therefore the most advantaged circuitry solution. But to realize the shortened square wave waveforms practically only one acceptable solution seems to be available: the switched current sources together with timing over the control unit will give the most advantageous result. Naturally the question rises, how the signal spectrum is influenced, if the turn-on and turn-off times for many current sources differ slightly from each other, or they are fully out of phase? Additionally it must be taken into account that also the on and off switching transition times of the current sources are influencing significantly the signal spectrum. Unfortunately such type of influence is almost impossible to calculate and predict, because it depends on switching speed and other factors. Therefore for the current source design we suppose that on and off switching time errors can be in the first approximation neglected in the control unit and the transition times are fast enough not to be counted. The transition time's influence to the spectrum will be measured afterwards. The results and discussion are presented in this chapter.

Design limitations

The replacement of sinusoidal signals in many practical cases can be solved using suitable approximations. The three levels shortened square waves' technique could be used. The basic idea of such a solution is that more equally spaced converting levels are introduced, and therefore higher harmonics, especially the lower end of higher harmonics, can be reduced. This multilevel signal can be easily generated digitally and it enables simple digital processing involving only additions and shifting. An efficient CMOS technology based current source can be designed to work with such nontraditional waveforms. The current source consists of circuit, switchable current mirrors to select different current ranges and H-bridge current output stage. In this case the use of H-bridge current output permits possibility to avoid the conventional instrumentation amplifier (simple buffer amplifier can be used), resulting a reduction of the whole measuring system complexity. Actually it means the connection of four current mirrors in bridge configuration. In such a simple structure we must take into consideration following limitations. All the design is made using National Semiconductor 0.5 μm CMOS technology.

The MOS transistor output current range is unfortunately limited, because of relatively low power supply and of need to keep the transistor in a strong inversion mode. To define the circuit limitations, a simplified H-bridge schematic will be used (Fig. 2.1) Using of p-channel MOS (PMOS) transistors, the higher threshold voltage V_{THP}, and the lower acting speed for used manufacturing technology will be achieved.

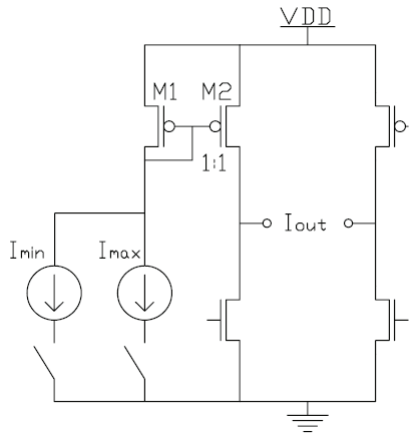


Fig. 2.1. H-bridge schematic.

If the current source with minimum current switches, the voltage drop on PMOS transistor M1 must be higher than the threshold voltage: $V_{SDmin} = V_{SGmin} > V_{THP}$. The maximum current from the switching current source gives the voltage drop on M1 which can be calculated as $-V_{SGmax} = VDD - 0.5\ V$, where the voltage 0.5 V is the minimum possible and reasonable voltage drop on current source and switch both. It means that by the power supply biasing VDD = 2.4 V results at the minimum value of V_{SGmin} could be equal to 1 V to keep the transistor in a strong inversion mode. The threshold voltage V_{THP} for PMOS transistors will be equal to –0.9 V for the used technology. The maximum value of V_{SGmax} calculates then 1.9 V. The defining question raises: what could be then the maximum value of ratio of the currents I_{max}/I_{min}?

To calculate roughly the MOS transistor drain current in saturation region a well know formula will be used e.g. [25]:

$$I_D = KP_p/2 \times W/L \times (V_{SG} - V_{THP})^2, \tag{2.1}$$

where KP_p is the transconductance parameter for p-channel MOS transistor, W is the channel width and L is the channel length. The first approximation can be done assuming that transconductance parameter and the ration of channel width and length are both constants. Setting in equation 2.1 for the transistor M1 the voltage V_{SG} possible values at 1 V and 1.9 V, then the current ratio I_{Dmax}/I_{Dmin} becomes equal to 100. From this result the conclusion can be made that

designing the circuit so that the strong inversion mode holds, then the minimal and maximal values of current sources I_{min} and I_{max} cannot differ more than 100 times. This is clearly true looking the transistor M1 from the diode side, but similar question raises looking the transistor M2.

The transistor M2 must be kept always in saturation region. This means that the differential resistance of the transistor M2 is high and the transistor is acting like a current source. But in case when the transistor M2 acts in linear region, then along the channel the inversion charge never decreases to zero value. But when the voltage $V_{SD} = V_{SG} - V_{THP}$, then the inversion charge under the gate will be equal to zero value, when $y = L$ (y is the length of inversion layer charge distribution along the channel). Working in saturation region means that $y < L$. Then the drain-source voltage is called (e.g. [25]):

$$V_{SD,\,sat} = V_{SG} - V_{THP}. \tag{2.2}$$

Equation (2.2) indicates a situation, when the channel charge becomes pinched-off at the drain-channel interface (long-channel MOSFETs). Our interest is keeping the voltage V_{SD} always higher than the voltage value $V_{SD,\,sat}$ to hold the transistor in the saturation region ($V_{SD} \geq V_{SG} - V_{THP}$). $V_{SD,\,sat}$ value can be called as a boundary value between triode and saturation region. In equations (2.1) and (2.2) we assume that the mobility does not vary with the voltage V_{SD}. In case, when the voltage drop at the transistor M1 is $V_{SD} = V_{SG} = 1$ V, the current source current value I_{min} is valid. This in turn means that the transistor M2 voltage $V_{SD,\,sat} = V_{SG} - V_{THP} = 0.1$ V. It means that if the power supply bias equals to value VDD = 2.4 V, then the maximum voltage drop (peak to peak value) on load impedance can reach the value 2.2 V because of two transistor in series situation (one n- and one p-channel CMOS transistor). When the voltage drop on transistor M1 is $V_{SD} = V_{SG} = 1.9$ V, then the current source current value I_{max} will be reached. In this case the transistor M2 biases as $V_{SD,\,sat} = V_{SG} - V_{THP} =$ 1 V and the maximum voltage drop at power supply VDD = 2.4 V (peak to peak value) can be only 0.4 V. From the previous discussions we can conclude that if the voltage drop $V_{SD} = V_{SG}$ on transistor M1 is changing between 1 to 1.9 V, then the minimum voltage drop V_{SD} on transistor M2 will be between 0.1 to 1 V. This happens of course then, when the difference between currents is 100 times. Such a large current difference indicates that the designed solution is valid almost for the solutions and applications, where the load impedance is low. In our case the load impedance is usually around 100 Ω and the currents not more than 500 μA, but the system must be able to measure also higher impedance values.

Unfortunately the current source, basing on four current mirrors in H-bridge configuration (Fig. 2.1), has some more limitations. First we have to mention is the output resistivity. Assuming that the MOSFET transistor behaves like a current source if it is operating in the saturation region (the analog design stage), we have to look more closely the output characteristics of MOSFET transistor (I_D dependence on V_{DS} voltage at the given V_{GS} value). In this case the output

current still depends slightly on voltage V_{DS}, when the transistor is in saturation. So, we can conclude that the MOS transistor equivalent model in saturation region can be described in a way that between source and drain of the transistor the ideal current source with parallel connected resistor r_o is placed. This resistor calculates, e.g. [25]:

$$r_0 = \left(\lambda \times I_{DS,sat}\right)^{-1}, \tag{2.3}$$

where λ is channel length modulation parameter and $I_{DS,\ sat} = I_D$ when $V_{DS} = V_{DS,\ sat}$. The parameter λ depends on the drain to source voltage, gate potential and channel length, e.g. [25]:

$$\lambda = L_{elec}^{-1} \times \left(dX_{dl}/dV_{DS}\right), \tag{2.4}$$

where L_{elec} is the so called electrical channel length (inversion layer charge distribution length along the channel). The electrical channel length of the MOSFET transistor defines as a difference between the physical channel length, neglecting lateral diffusion, and the depletion layer width X_{dl}, between the drain and the channel under gate oxide. The electrical channel length calculates, e.g. [25]:

$$L_{elec} = L - X_{dl}. \tag{2.5}$$

To understand how the electrical channel length L_{elec} differs from physical channel length L, the explanation is on Fig. 2.2.

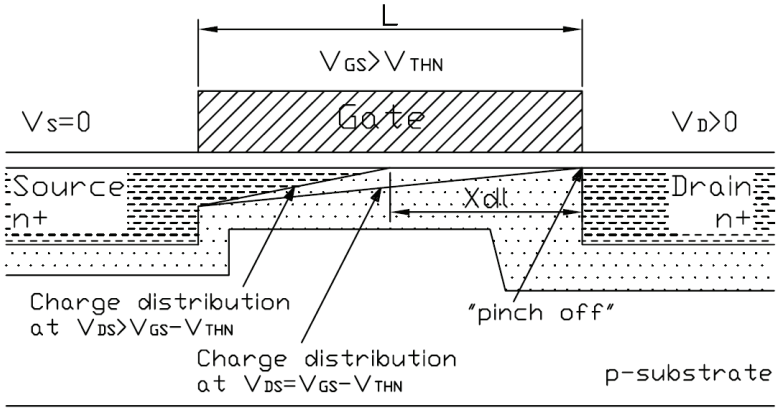


Fig. 2.2. The NMOS transistor in saturation regime.

Another limitation arises because the channel length modulation parameter λ is not a constant value. Additionally, we have to take into account that the exact output resistance values at different output (drain) currents and different source

to drain voltages can be calculated only in SPICE simulations. Taking into account all further described limitations the rough approximation for resistivity area can be estimated. For our concrete situation the channel length modulation parameter λ will be equalized for long channel design with the value 0.01 V^{-1}. For transistor M2 on Fig. 2.1 the output resistance r_o will be equal approximately to 20 MΩ at output current 5 μA, and approximately to 200 kΩ at output current 500 μA. It is clearly seen that about the hundred times difference is valid as we declared earlier.

Very important statement concludes from these further discussions. To improve the ideality of the current source the increase of the output resistivity must be done. Unfortunately increasing the output resistivity the introduction of cascoded current mirror technique is needed. But this technique leads us to a higher supply voltage, which is unacceptable for our design process and final solution as well.

The MOS transistor switching speed could be described through the transition frequency f_T. This is the frequency, where the current gain value of the MOSFET is equal to one. Transition frequency for PMOS transistors calculates, e.g. [25]:

$$f_T \approx g_m / 2\pi C_{gs} = 3\mu_p / 4\pi \times V_{SD,sat} / L^2 \quad . \tag{2.6}$$

This equation is fundamentally important. To increase the switching speed, the scale down of dimensions of the channel lengths must be done, and the higher voltage $V_{SD,\ sat}$ at the design process must be used. Referring to the previous text, the larger voltage $V_{SD,\ sat}$ could possibly be used, but this situation is in a clear contradiction with demand of decrease of the channel length. The shorter is the channel length the lower is the output resistivity of the current mirror transistors. From another point of view due to the non use of cascading technique it is impossible to realize the transistors with short channel length (the length of the channel must be as long as possible!). But high switching speed is needed because of switched current mirrors design, which means that the circuitry must be able to generate shortened square wave signals with frequencies up to 1 MHz. Consequently, the transition times must be as short as possible. To solve the problem a clear compromise must be done: the channel length should be about 4 times larger compared to its possible minimum value ($L \approx 4\lambda$).

The circuitry design is made basing on National Semiconductor 0.5 μm CMOS technology. Unfortunately, it gives one additional limitation to matching of current mirrors. For 1 to 1 ratio current mirrors the transistor channel area ($L \times W$) should not be less than 25 μm^2. This restriction leads to the layout situation, where the minimum size of transistors should be as L = 2 μm and W = 12.5 μm. This limitation increases the mirroring error with few percent. But we have to take into account that the smaller is the transistors channel area, the

bigger is the mirroring error. To get as good as possible matching of the current mirrors the transistors must be split, which means that the good choice for the schematic transistor is the solution with channel dimensions of L = 2 µm and W = 14 µm. And the split in layout (at least) gives us minimally two transistors with channel dimensions of L = 2 µm and W = 7 µm. Unfortunately this leads to the situation, where the current ratio about 1 to 8 is now inaccurate. This inaccuracy is arising from the fact, that one transistor must be geometrically matched with transistor, which is eight times larger. Even when the transistors are divided into two or four equal pieces (one transistor is giving 2 and the other one 16 equal size pieces), there is hard to find the best layout solution and the current error in current mirror is increasing. The current mirror transistor matching issues are discussed in the Chapter 3.

Actual design

The design of the current source chip contains 4×6 different current sources connected through switches to one H-bridge output stage. The current source as a black box is seen in Fig. 2.3. The current source needs two external bias signal pads to bias the inner circuitry current mirrors – V_{biasn} and V_{biasp}. For switching and combining the currents the 2×6 control inputs must be included (inputs C1 to C6 for getting positive output current and C1i to C6i for negative output current) and two inputs I_{off} and I_{off}i to switch the H-bridge off (third) state. Table 2.1 shows the possible output current generating scheme for switching all of the six current sources to get the maximum 100 µA output current.

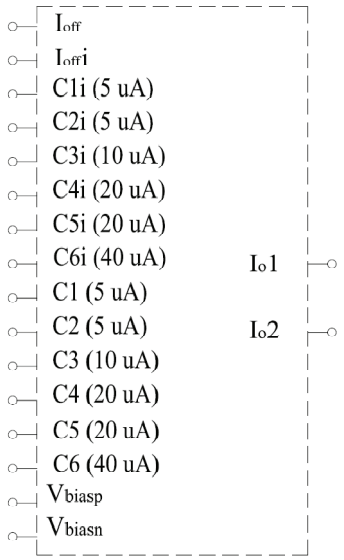


Fig. 2.3. Current source block diagram.

Table 2.1. Control signals and their current values.

Control signals	I_{out}
C1 and C1i	5 μA
C2 and C2i	5 μA
C3 and C3i	10 μA
C4 and C4i	20 μA
C5 and C5i	20 μA
C6 and C6i	40 μA

The schematic of the current source is given in Fig. 2.4. The V_{biasn} and V_{biasp} voltages are driving the current mirrors and afterwards the current is mirrored to 4×6 independent current sources. To achieve the simple current mirror ratio 1:1 the transistor matching error should stay ultimately below 2 %. To fulfill the demand for so small error the channel length of the transistor must be at least four times over the minimum strip dimensions (0.5 μm technology in our case) and the channel area ($L \times W$) must be larger than 25 μm^2. Unfortunately the higher is the mirrored current and primal current ratio the higher is the matching error. The current mirroring ratios over 1:8 are therefore not usable. The attempt was made to find the best optimum for transistor channel length and width ratios so, that the matching error at 1:1 ratio stays under 2 % and 1:8 ratio does not exceed 5 %. The "worst case" simulation results are shown in Fig. 2.10. The design and calculations show that the current error for all added currents did not exceed the 5 % level.

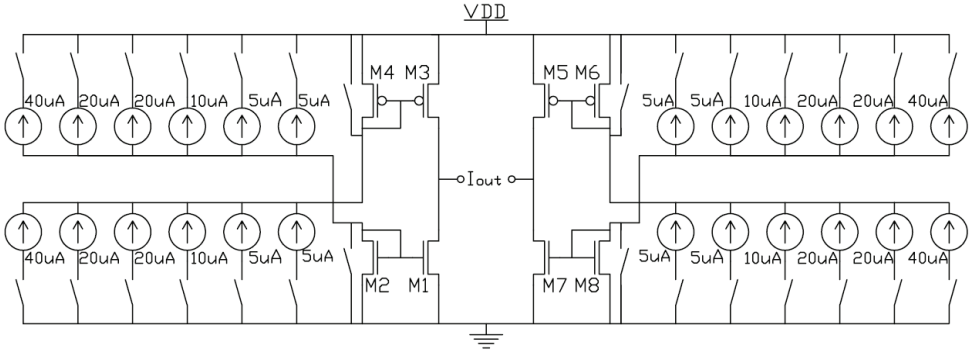


Fig. 2.4. Current source principial schematic.

There are two alternatives in the design process – first to connect the switching transistor source to power rail, or second to connect the current source transistor to power rail (VDD or GND). It is not important for series connection, because the outcome will be the same. But to decrease the peaks during the switching process the switching transistor sources must be connected to power

rail and the current source transistors must stay in “floating” position. In an opposite connection situation, where the switching transistors are floating, we will get much bigger current spikes at switching moments, which are undesirable phenomena. These spikes will generate only higher harmonics and are therefore they not important, but they could overload the measuring amplifier input or give a measuring error and must be therefore avoided. In this series contour the parasitic capacitances (drain to bulk, source to bulk, gate to source, etc.) presence must be taken into account as well (how to charge and discharge these capacitors). Actually, the full current source schematics would be much simpler, if the switches are “floating” (different conductivity transistors – p- or n-channel MOS transistors can be used to make the inversion operation). When the switching transistors are fixed to power rail, then we need additional invertors to drive the H-bridge current sources of opposite shoulder.

The actual circuitry for the current source solution is shown in Fig. 2.6. The difference in principal schematic (Fig. 2.4) and real schematic is that the bias circuit has the current mirror ratio 2:1. It means that all current sources C1 to C6 and C1i to C6i have a two times lower current value. The current mirrors in H-bridge have the current mirror ratio 1:2. This method helps to reduce the power consumption and has no significant effect on circuit overall speed. Of course, during the down and up mirroring the bias current and the current in H-bridge are different, but this is not a problem. More important is that the current ratios between different current sources will remain within allowable limits of error. This is important for generating multilevel signals (Fig. 1.18). The dimensions of H-bridge transistors channel for NMOS transistors are $L = 2.5$ µm and $W = 20$ µm and for PMOS transistors $L = 2.5$ µm and $W = 56$ µm. The H-bridge transistors form the complementary pair. For switched current source transistors the complementary condition is not essential. The dimensions of current source transistors for I_{min} were chosen for NMOS $L = 2.5$ µm and $W = 10$ µm and for PMOS $L = 2.5$ µm and $W = 20$ µm, respectively. The dimensions of current source transistors for I_{max} were chosen for NMOS $L = 2.5$ µm and $W = 80$ µm and for PMOS $L = 2.5$ µm and $W = 160$ µm, respectively. The dimensions of switching transistors were chosen for I_{min} and for NMOS transistors $L = 0.5$ µm and $W = 10$ µm, respectively; and for PMOS transistors $L = 0.5$ µm and $W = 20$ µm respectively. For I_{max} the dimensions were chosen for NMOS transistors $L = 0.5$ µm and $W = 80$µm and for PMOS transistors $L = 0.5$ µm and $W = 160$ µm respectively.

The test chip has been designed with the opportunity to use external bias voltage. The nominal bias voltage value was chosen to be 1.2 V. The low-power biasing circuitry solution is shown in Fig. 2.5.

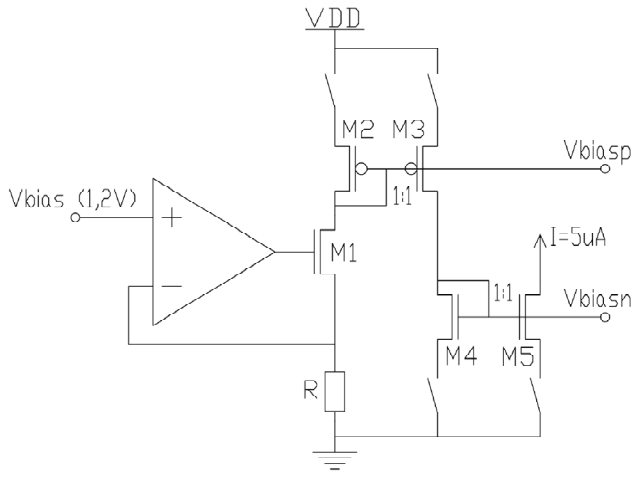


Fig. 2.5. Biasing circuit principial schematic.

The voltage to current conversion is realized using low-power operational amplifier, transistor M1 and resistor *R*. The weak point of this solution is the resistor *R* with nominal value about 240 kΩ. Unfortunately the used 0.5 μm technology gives for all resistors the positive temperature coefficients. Additionally the layout geometry dimension of the resistor becomes too big. The attempt to scale down the resistor area about 20 % leads us to the one long channel NMOS transistor with resistor *R* in series in case, when the transistor acts in linear regime. Then the resistor nominal value will be 190 kΩ (on Fig. 2.7 resistor R5 and transistor M61).

Results of the simulation comparing the 240 kΩ resistor (on Fig. 2.8 the dotted line) with the resistor of 190 kΩ in series with n-channel transistor are shown on Fig. 2.8 (at power supply voltage 3 V). The resistor in series with n-channel transistor gives the excellent output current stability in wide enough temperature range (from 0 to 40˚C), but only then, when the input biasing stays at 1.2 V. In this design there will be small current dependence from the power supply voltage. Changing the power supply voltage from 3 V to 5 V the bias circuit current through the resistor *R* is increasing 0.14 %, Fig. 2.9.

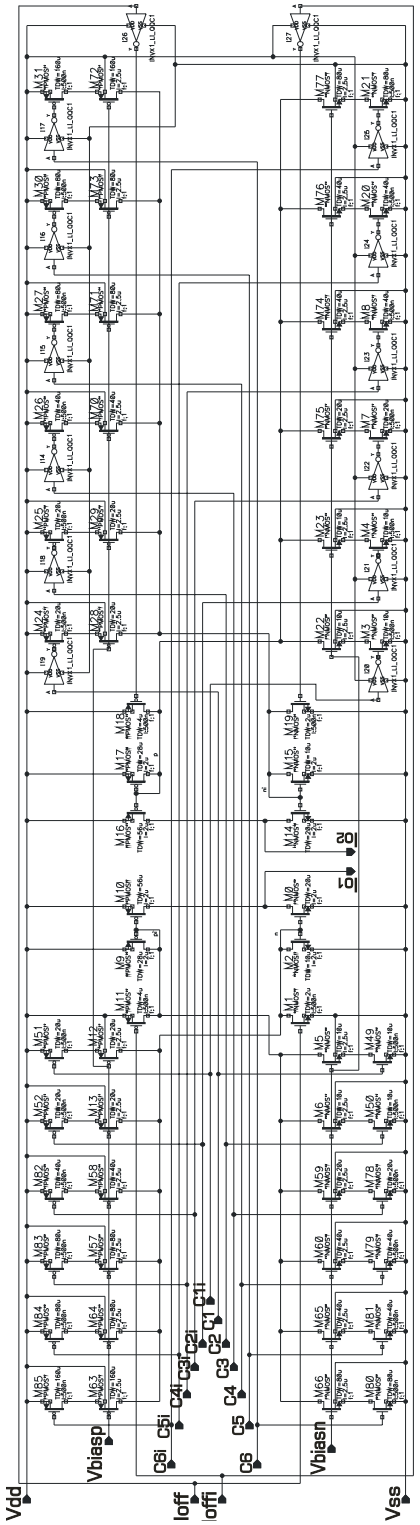


Fig. 2.6. Current source actual schematic.

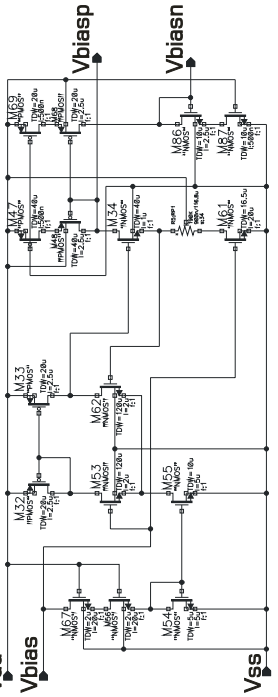


Fig. 2.7. Actual schematic of the biasing circuit.

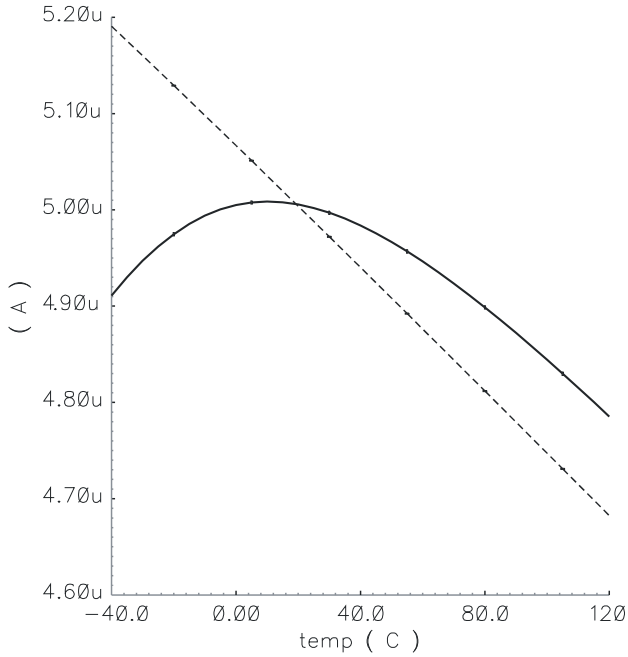


Fig. 2.8. The temperature dependence of the bias circuit transistor M34 drain current.

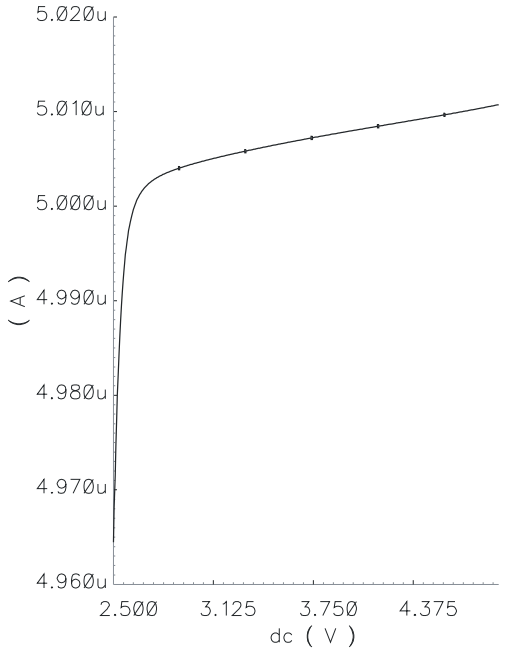


Fig. 2.9. Bias circuit transistor M34 drain current dependence from power supply voltage.

The initial simulation results showing only the working principle of the circuitry are shown in Fig. 2.10. The idea was not to create stepped sine wave, but to show the possible combinations of current sources. The simulations calculate only the threshold voltage, drain-to-source voltage and lambda mismatch. To get the accurate and trusted result, the layout has to be composed.

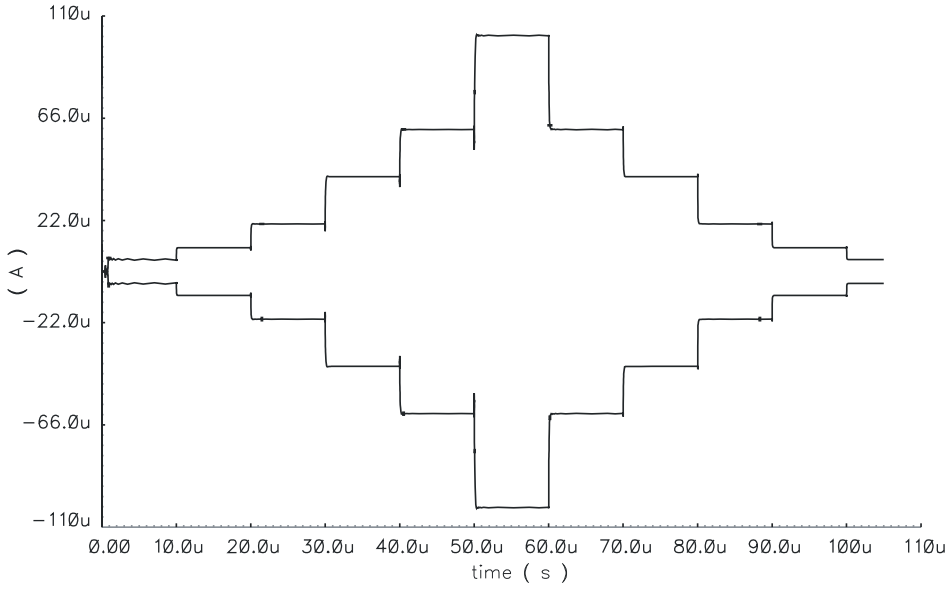
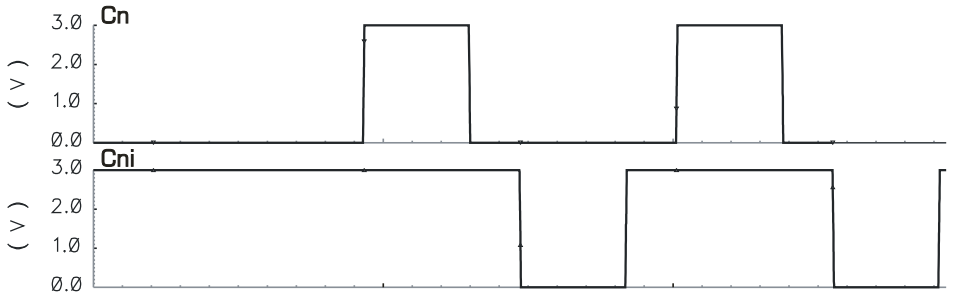


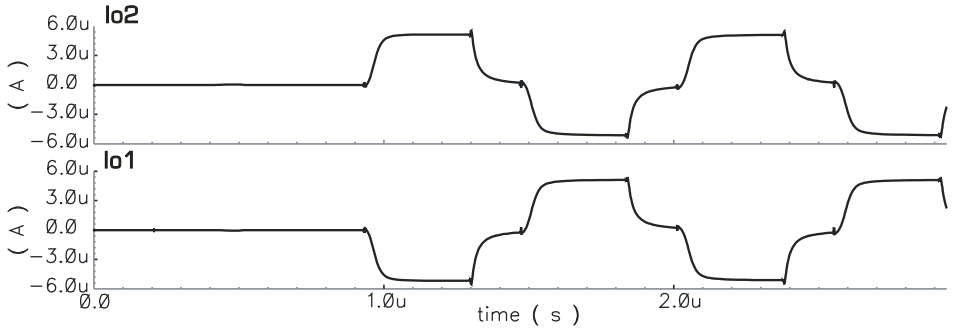
Fig. 2.10. Adding and subtracting independent current sources.

Let us explain the simulation results with 30° shortened square wave signal. The simulations show that at power supply voltage 3 V the current change at temperature corresponds with the graph presented in Fig. 2.7, but if we increase the power supply up to 5 V, then the H-bridge output current will rise approximately 5 %, and not 0.14 % as we expect and as the bias circuit should determine. Such an increase in current can be explained taking into the account the influence of the output resistance of current source transistors. To reduce dependency of power supply voltage, the cascoded current sources must be used. In our design we must just accept the increase in H-bridge output current as it produces.

The simulation results from Figs. 2.11 - 2.13 shows that the increase of pulse rising front time constant τ changes from 47 ns, at 5 μA, up to 22 ns, at 40 μA takes place. But in Fig. 2.14 quite another thing can be observed concerning the rise of the pulse fronts. For this difference the explanation concludes from the low power biasing circuit, which cannot hold the V_{biasn} and V_{biasp} voltages constant. Also the bias circuit operational amplifier speed limit decreases the maximum current source switching speed.



(a)



(b)

Fig. 2.11. (a) Control signals and (b) H-bridge output at 5 μA and 926 kHz.

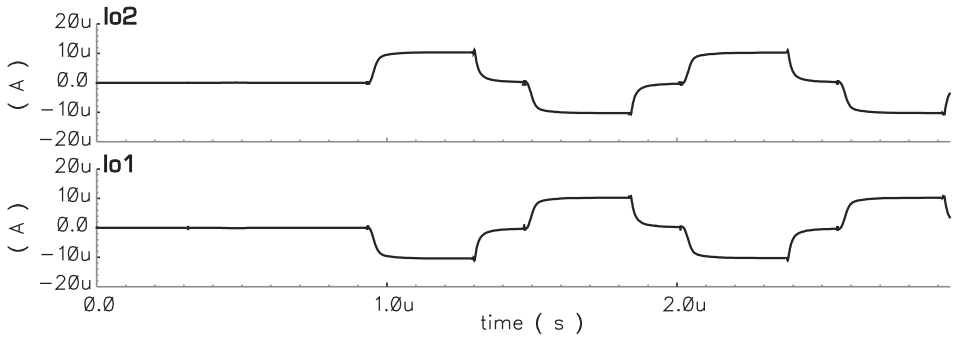


Fig. 2.12. H-bridge output at 10 μA and 926 kHz.

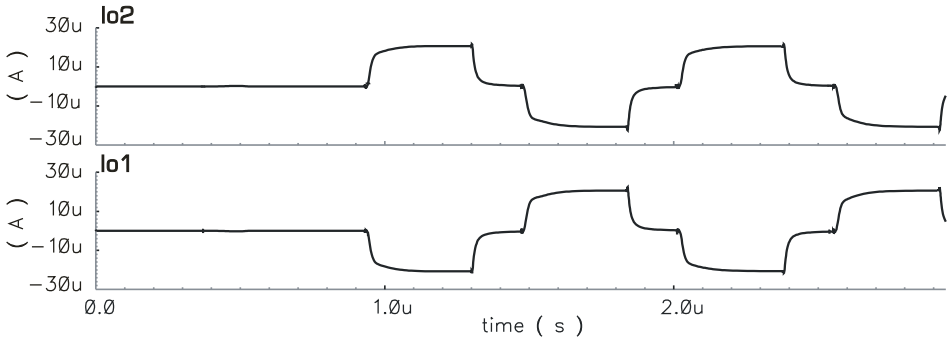


Fig. 2.13. H-bridge output at 20 μA and 926 kHz.

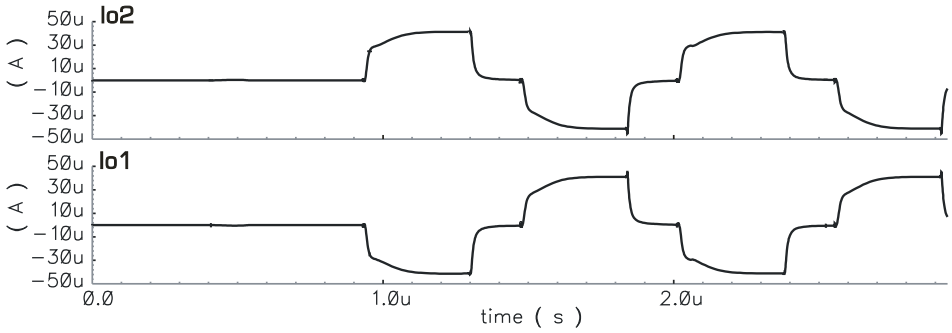


Fig. 2.14. H-bridge output at 40 μA and 926 kHz.

In Fig. 2.15 and Fig. 2.16 the 5 μA 30° shortened square wave signal spectrum at relative low speed (926 Hz) and high speed (926 kHz) are shown. The smoothened fronts at higher frequencies are lowering the higher harmonics level and the impact on main harmonic is less (the change is below 5 %).

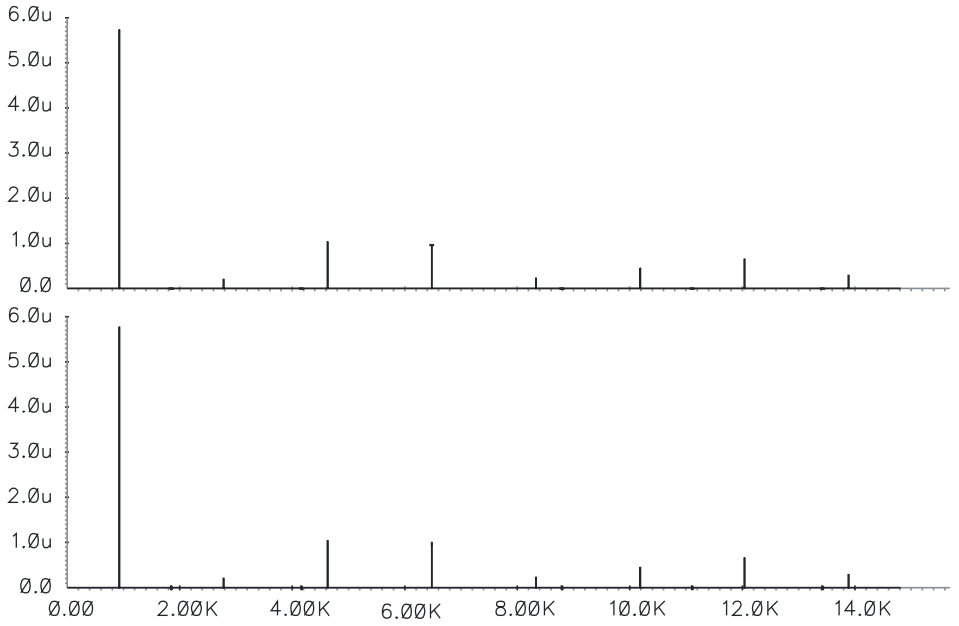


Fig. 2.15. 5 μA and 30° shortened square wave signal spectrum at 926 Hz (upper graph is the spectrum in case of ideal current source).

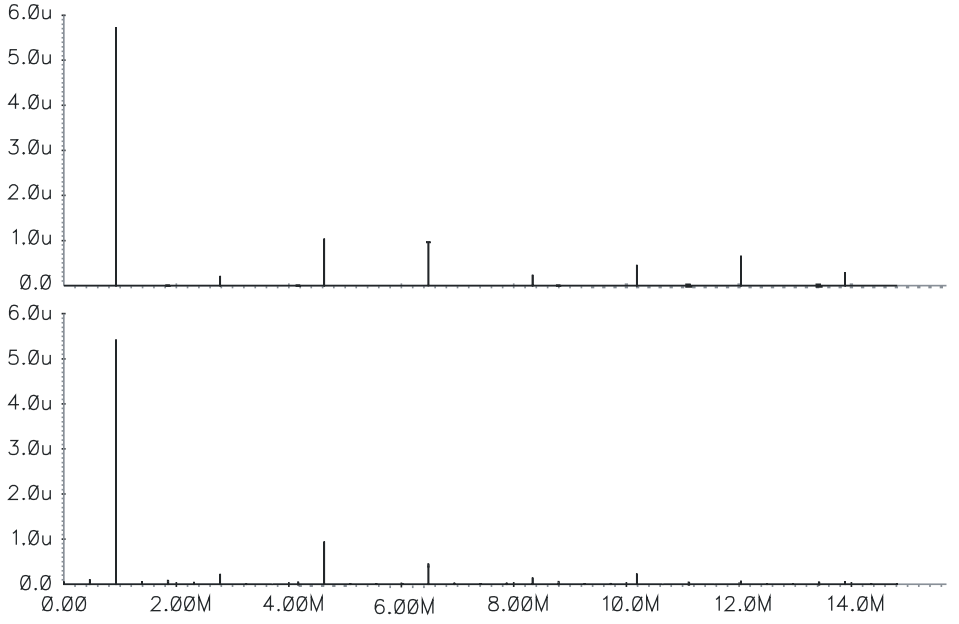


Fig. 2.16. 5 μA and 30° shortened square wave signal spectrum at 926 kHz (upper graph is the spectrum in case of ideal current source).

In Fig. 2.17 is a 40 μA and 30° shortened square wave signal spectrum at 926 kHz is shown. As one can see, on higher frequencies the picture is similar as we have seen at the 5 μA output signal, but the third harmonic level is increased. The simulations show also that the fifth harmonic level never changes.

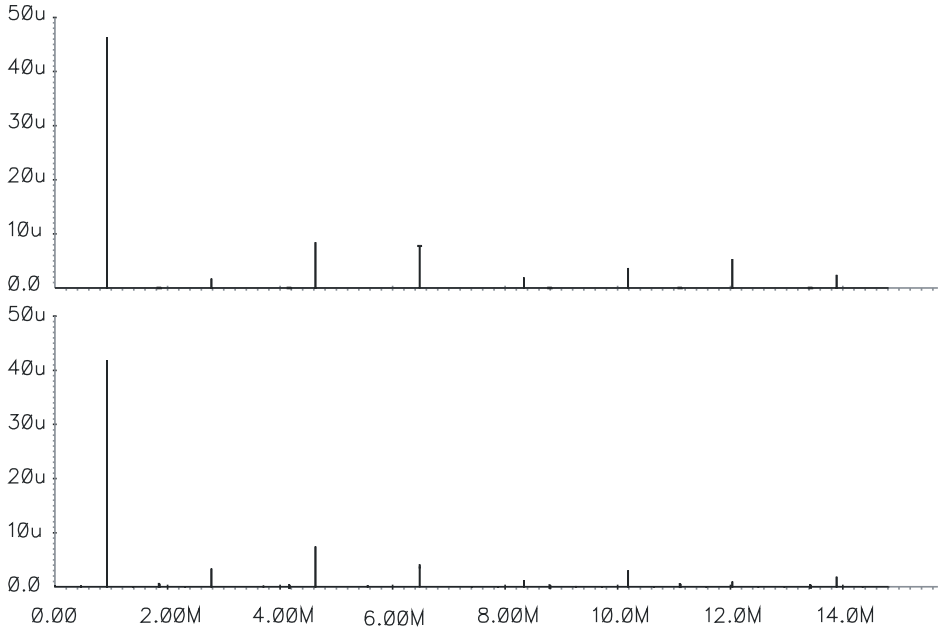


Fig. 2.17. 40 μA and 30° shortened square wave signal spectrum at 926 kHz (upper graph is the spectrum in case of ideal current source).

Taking into the account that there are no practical limitations from bias circuit, the current sources transistors rising front time constants are approximately equal to 10 ns (Fig. 2.18). The respective signal spectrum is shown in Fig. 2.19.

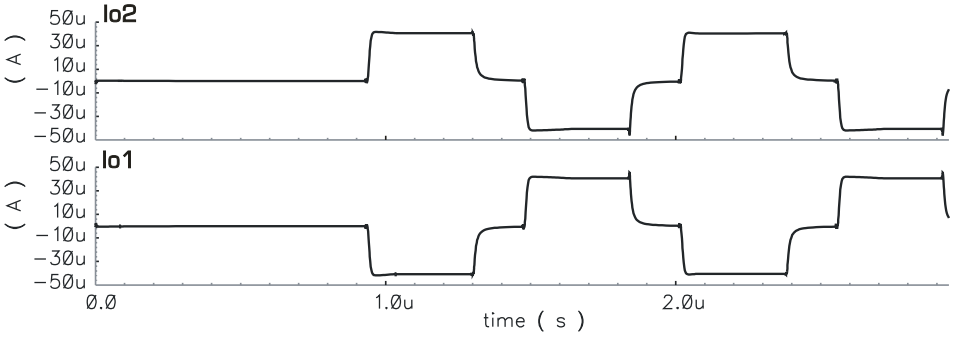


Fig. 2.18. H-bridge output at 40 μA and 926 kHz, when bias voltage levels stay constant.

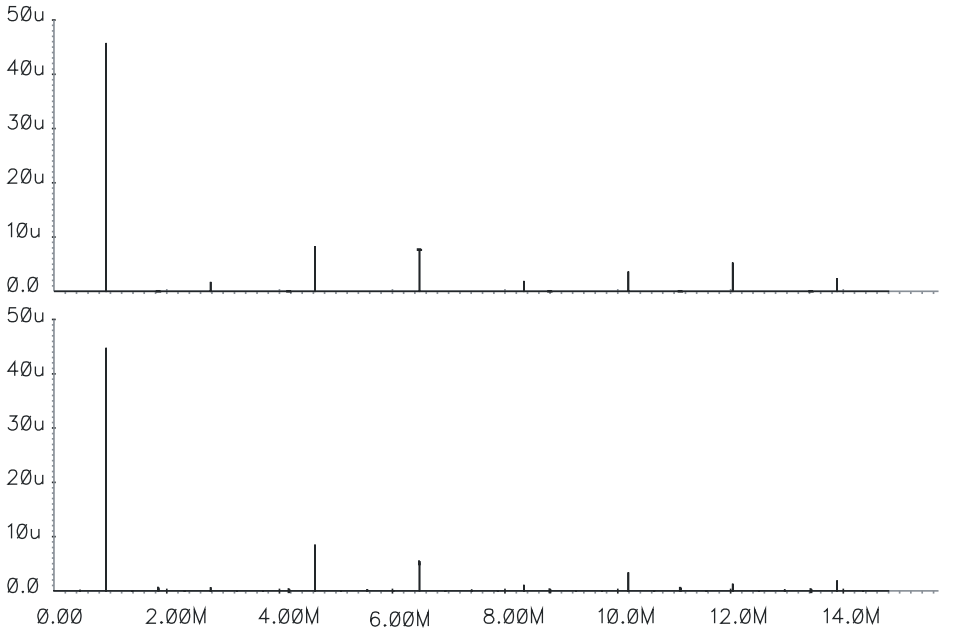


Fig. 2.19. Spectrum of Fig. 2.18 given signal (upper graph is the spectrum in case of ideal current source).

Conclusions

For generating shortened square wave current the simplest and optimal circuitry was used. Such a simple solution has pose many questions: how exact the output current will be and how big tolerances are accepted; does the switching give any glitches and how they will affect the measuring results; is the H-bridge output resistance high enough and at which frequency the output impedance is starting to influence the measuring results; and so on. The simulation results were showing relatively good results. Actually there are many parameters what the schematic simulations does not reveal. These parameters can be made worse or enhanced with layout. So the layout design is the critical part. If everything will turn out well there, then this simple current source circuit will give good results in real test chip measurements.

CHAPTER 3: DESIGN OF THE LAYOUT

Introduction

From the point of view of schematics full design of the current source looks relatively simple. The deceptive simplicity rises from developed circuit solution, where for example one row of current sources is giving the current to one side of H-bridge output. For this act the six current source and six switching regime transistors are described and also theoretically needed. Unfortunately the currents in the circuitry are different, and therefore we have to use in layout solution not twelve (6 + 6) transistors, but at least twenty transistors working in current source regime and twenty transistors in switch regime. Also we have to match all current source transistors, which usually mean the splitting of the transistors and this will double or even quadruple the number of transistors on chip surface. It means that if in schematics we have for example a transistor with channel length L = 2.5 μm and channel width W = 10 μm (channel area 25 μm^2), then in layout we have two transistors with dimensions L = 2.5 μm and W = 5 μm or four transistors with dimensions L = 2.5 μm and W = 2.5 μm (channel area 4×6.25 μm^2).

Generally there are two possibilities to match the devices on chip surface. It does not matter, are the elements resistors, capacitors or transistors; the same rules have to be followed. The realization is known as *interdigitated layout* or *common-centroid layout* solution [25].

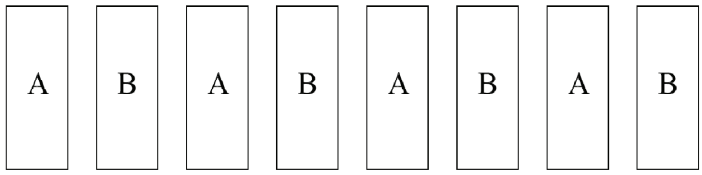
The general suggestions for matching

Interdigitated layout

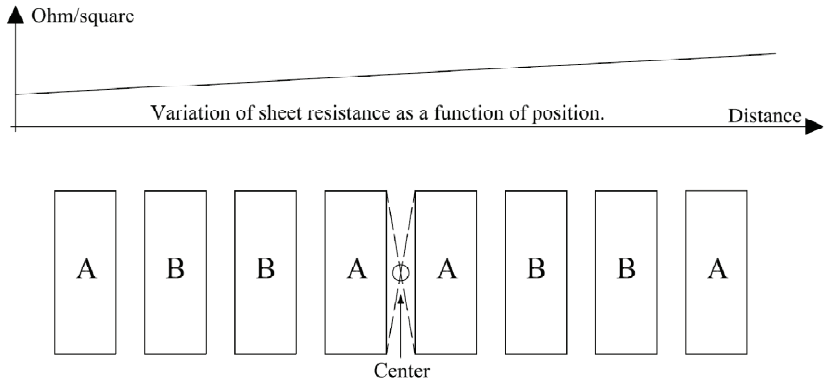
The matching between two different elements A and B can be improved if we split the elements into smaller pieces and using the layout shown in Fig. 3.1(a). These elements are said to be interdigitated. Process gradients, in this case changes in the *n*-well, n^+- or p^+-doping at different places on the die, are spread between the two devices A and B more evenly. We have to stress one important circumstance, if we need to match two devices: the orientation must be consistent between unit cells. As seen in Fig. 3.1(a) all the cells are laid out vertically. Essentially each element has the same parasitics over the whole array.

Common-centroid layout

Common-centroid (common center) layout helps to improve the matching between two elements. Considering the common-centroid layout shown in Fig. 3.1(b), one can follow those two elements A and B share the common center. If we consider, that the sheet resistance varies linearly on the overall value of each resistor, and assigning a normalized value to each unit element (resistor), we will get that (resistor) A has a value of 16 and (resistor) B has a value of 20. In ideal case they are of course equal. Looking to Fig. 3.1(b), the value of either element (resistor) A or B is 18. In other words, the use of a common center (ABBAABBA) will give better matching than the interdigitated layout (ABABABAB).



(a)



(b)

Fig. 3.1. Layout solutions: (a) interdigitated, and (b) common-centroid.

Typical causes of mismatch in current mirror

In analog design the circuit application is susceptible due the layout errors. In our design all the current sources are a part of one large current mirror, where from one so called bias transistor the current is mirrored into twelve transistors –

current sources. Because of this the design needs to be matched and therefore the layout design is extremely critical. For example, in basic current mirror, consisting of two transistors in Fig. 3.2, first-order process errors can cause the output current to be significantly different from the reference current. The process parameters like gate-oxide thickness, lateral diffusion, oxide encroachment and oxide charge density drastically affect on performance of the cells. These possible influences must be taken into account, when starting the layout design. It means that in the layout design must be used common-centroid layout rules as much as possible. In the following a short overview of first-order effects caused by the parameter variations is given.

Threshold voltage mismatch

In the current mirrors the values of threshold voltages of MOS transistors are critical to reach the overall accuracy. In basic current mirror, where only two transistors are used, the current mismatch can be calculated (higher order terms are ignored) as [25]:

$$\frac{I_{OUT}}{I_{REF}} \approx 1 - \frac{2\Delta V_{THN}}{V_{GS} - V_{THN}} = 1 - \frac{2\Delta V_{THN}}{V_{DS,sat}}, \tag{3.1}$$

where ΔV_{THN} is the mismatch or threshold voltage difference. Eq. (3.1) is quite revealing because it shows that if the voltage V_{GS} decreases, the difference in the mirrored currents increases due the threshold voltage mismatch. To attain high speed and to reduce the effects of threshold voltage mismatch, the gate drive voltage should be big enough (if it is too big, then we reach the triode region). Of course the drawback is a reduced output current range. All these problems were already taken into account in circuit schematics design in Chapter 2.

Drain to Source voltage and lambda

To obtain accurately generating currents the drain-to-source voltage has to be taken under specific observation. In simple two transistors current mirror solution the output current is equal to reference current only then, when both transistors have the same V_{DS} value. The current mismatch can be calculated as [25]:

$$\frac{I_{OUT}}{I_{REF}} = \frac{1 + \lambda_2 \cdot V_{OUT}}{1 + \lambda_1 \cdot V_{DS1}}, \tag{3.2}$$

where λ_1 and λ_2 are the transistors channel length modulation parameters, V_{DS1} is the drain-to-source voltage drop on first transistor and V_{OUT} is the voltage drop

on second transistor. Looking the Eq. (3.2) we can see, that even if we have the equal lambdas (both transistors in current mirror have the same size and the mirrored current ratio is 1:1) the drain-to-source voltage differences on both transistors will give about 1 to 2 % error in our case. This error is build into the schematics design and cannot be removed or improved over the layout design. The computer simulations of schematics show this error of 1 to 2 % and the simulation is taking into account the Eq. (3.2).

Layout techniques to improve matching

First rule is to use channel lengths as long as possible to improve matching. This concludes from the fact that the channel length modulation parameter λ has lesser effect on longer channel transistors (the longer the channel the smaller the channel length modulation parameter λ value is). In Chapter 2, it was discussed that the minimum channel length L should be at least 2 μm and the minimum channel area ($L \times W$) not less than 25 μm^2 for the used 0.5 μm CMOS technology. The maximum channel width W is defined by the guard ring rules. In used CMOS technology the maximum channel width is defined, for both the NMOS and PMOS transistors, to be 20 μm respectively. All transistors, which have large W/L ratio, are split into several parallel devices. The positive result of splitting the devices into several pieces, the smaller overall parasitic capacitance associated with the reverse-biased implant substrate diode.

In [25] and [27] the typical simple two-transistor current mirror layout is proposed and the solution is presented in Fig. 3.2. The transistors are split into four parts and the interdigitated layout solution is used.

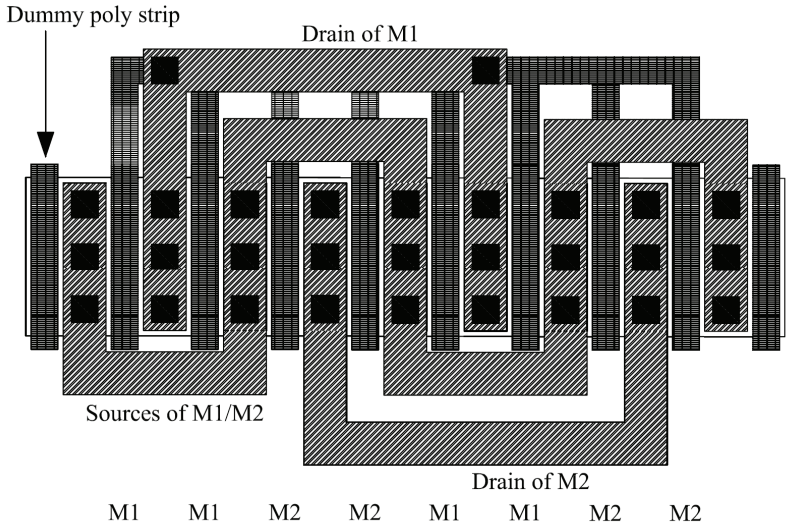


Fig. 3.2. Layout of a simple two NMOS transistor current mirror.

Unfortunately, obvious problems arise using such a solution. First, the guard ring is missing. The guard ring distance from source or drain of transistors is the most important geometrical parameter. Second, the drain to source distance of two separate transistors (distance between n^+ and n^+ implant in NMOS) must be equal to transistor source to guard ring or drain to guard ring distance (the distance is measured between n^+ and p^+ implants in NMOS). In this case the dummy poly strips are usually not necessary. Third, it is clear that all of the transistors must have the same orientation to achieve the necessary matching. Looking at Fig. 3.2, the first M1 transistor is orientated looking from left to right source-drain to the next M1 transistor drain-source. The next M2 transistor is again orientated from left to right source-drain to the next M2 transistor drain-source. So, this design is very compact, because the transistors share common drains and sources, but they do not have the same orientation. If we assume, that the first transistor M1 orientation is fixed (0°), then the next M1 orientation is rotated 180°. M2 transistor first part has again fixed (0°) orientation and second part is rotated again 180°. Unfortunately these nice literature suggestions cannot be used in the real layout design.

Practical solutions for current source layout

For the layout design the CADENCE design environment was used in combination of the NSC CMOS7_5v technology line data package. Although the designed circuitry is relatively simple, the layout becomes rather complicated. The most critical part in the layout design is the placement of the switchable current sources. Very good matching of the current sources must be achieved by the actual layout. Mismatch will result in failure of the whole current source design. Actually the circuit simulations do not show the matching error very accurately. The simulations take into account the fluctuations in drain-to-source voltage and lambda, but they do not show threshold voltage mismatch and transconductance parameter mismatch.

Fig. 3.3 shows the test chip layout in 0.5 μm CMOS technology with the used area of about 285×155 μm^2. The bias circuit for the current mirror is the core of the matched current source. Fig. 3.3 shows that the operational amplifier of the biasing circuit and voltage to current converting resistor are on the right side, and that the current mirrors what are biasing twelve NMOS and twelve PMOS transistor current sources (transistors M48, M68 and M86 on the Fig. 2.7) are moved directly to the middle of switched current sources. The transistors in the H-bridge are also split, in order to get a well matched compact block.

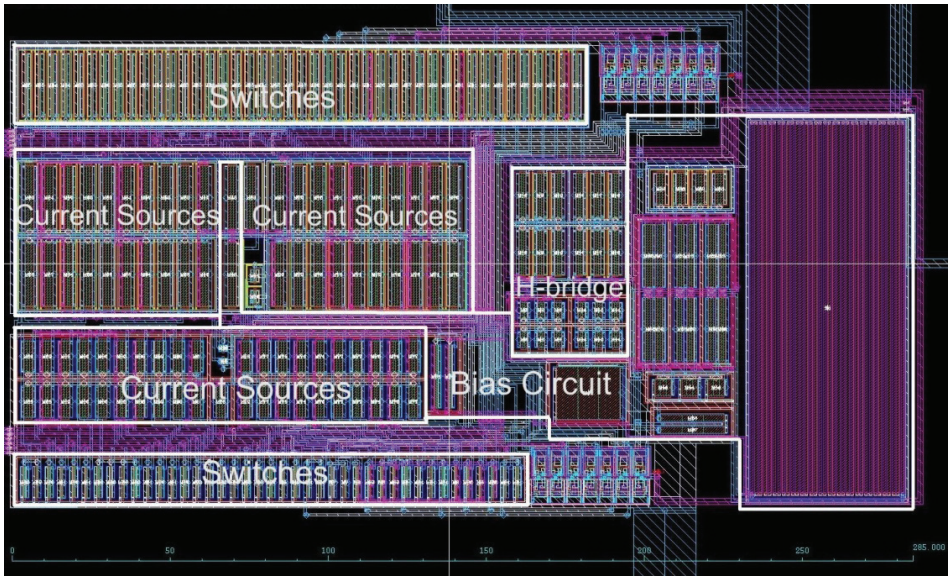


Fig. 3.3. Test chip layout.

Current source and switch transistors matching

Looking back to the schematics on Fig. 2.5 and 2.7, we can see, that there is only one NMOS transistor M86 which output voltage V_{biasn} is controlling all twelve current sources – C1 to C6 and C1i to C6i. It means, that the layout involves all together 41 NMOS transistors, including the bias transistor M86, in current source part and 41 NMOS transistors, including the bias transistor dummy switch transistor M87, in switching part. All the current source transistors have the same ratio *W*/*L*, and all the switching transistors have the same ration *W*/*L*, as seen in Fig. 3.4. The main question was, how do match one transistor with 40 transistors? Even splitting the transistors into smaller parts does not improve the results and complicates the whole layout. The decision was taken that the current sources C1 to C6 will be on left side and the current sources C1i to C6i will be on the right side. So the bias transistor M86 stays in the middle of the layout. And this will also give relatively good matching between current source C1 to C6 transistors and current source C1i to C6i transistors. Of course between left- and right-hand side transistors possibly the small mismatch could take place. This mismatch can affect the current output signal in such a way, that there will be differences in output current positive and negative amplitude values and this difference will cause even harmonics. This risk was taken and the real chip measuring results will show, if there is any problems with second and fourth harmonic in output signal (There will be even harmonics anyway, but their level will stay negligible).

For the matching of current source transistors the more accurate common-centroid layout solution was chosen. Because the current source transistors count is different there cannot be one common centroid point. In NMOS transistor current sources multiple groups and also multiple common centroid point's layout have been used. For example the current sources C4 and C5 are divided in two groups, see Fig. 3.4.

The switching transistors are also matched in the same way as the current source transistors.

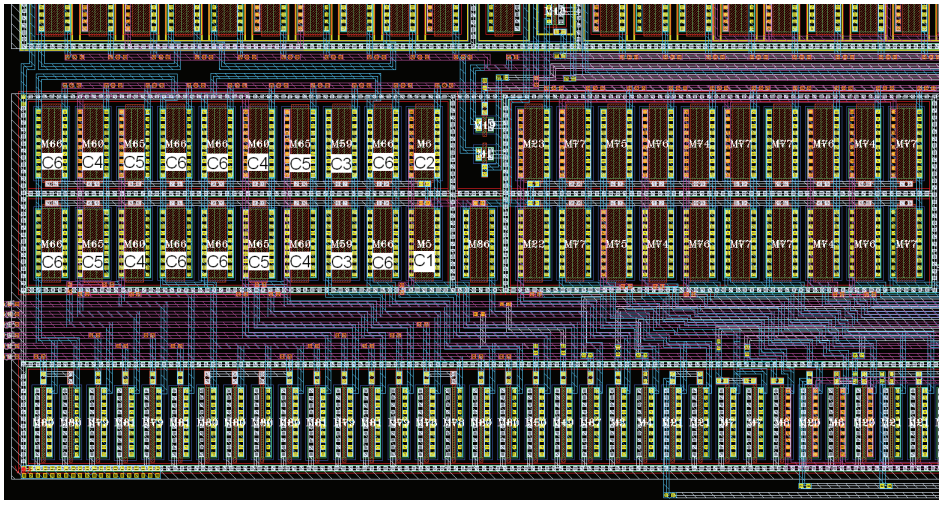


Fig. 3.4. Current sources C1 to C6 and C1i to C6i realized on NMOS transistors.

The counterpart for NMOS transistor current sources are the PMOS transistor current sources, Fig. 3.5. The PMOS current sources C1 to C6 and C1i to C6i are matched exactly the same way as the NMOS current sources on Fig. 3.4. In the middle are the bias circuit current mirror transistors M48 and M68 (see Fig. 2.7) giving the PMOS current sources control voltage V_{biasp}. The only difference is that the current sources C1 to C6 are on the right and current sources C1i to C6i are on the left side. On the top of current sources are the matched PMOS switching transistors.

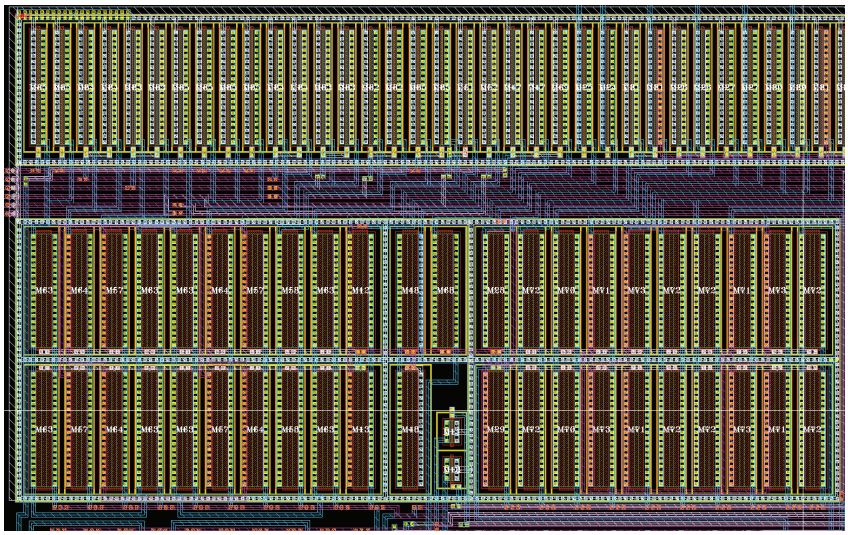


Fig. 3.5. Current sources C1 to C6 and C1i to C6i realized on PMOS transistors.

H-bridge output

The H-bridge current output stage was the simplest solution for matching. All transistors were divided into two parts and this gave a good and simple common-centroid type matching, as seen in Fig. 3.6.

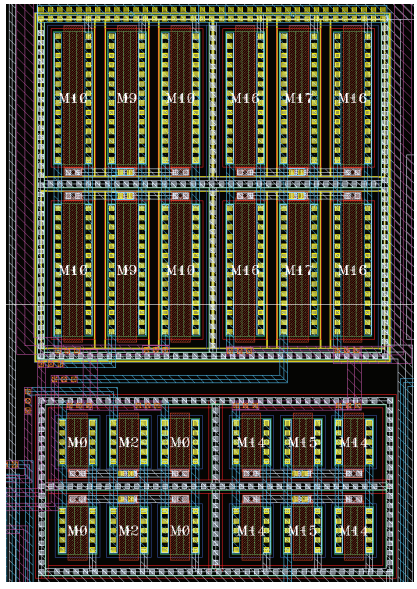


Fig. 3.6. Layout of the H-bridge.

Bias circuit

Bias circuit components were placed on free spots on layout, Fig. 3.7. Only blocks which have to be matched were put together to one bigger block. Looking into Fig. 3.7 we see on the right-hand side the 190 kΩ p diffusion type resistor R5, next to it we can see the bias circuit operational amplifier. In the middle is differential pair, on top of it the current mirror type dynamic load and on bottom the operational amplifier bias circuit with current mirror. Next to that block we can already see the H-bridge and below it is the transistor M61, which together with resistor R5 act as temperature compensated resistor. The bias circuit transistor M34 can be seen at the left down corner.

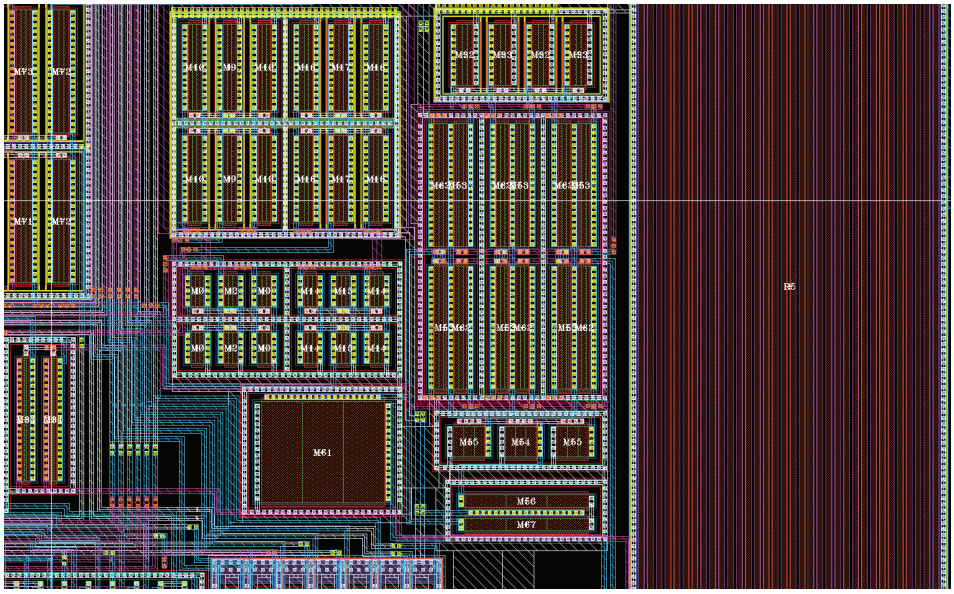


Fig. 3.7. Layout of the bias circuit components.

Conclusions

The current source layout came out as a quite compact and small device, using only area of about 285×155 μm^2. For test microchip it has given, that our layout design was not used area limited but contact ring limited. The contact ring makes a square with 5 contacts in each side, altogether 20 contacts. The overall chip area is about 1.2×1.2 mm^2. It means that most of the chip area was left empty and must be filled with metal fillers.

The layout design was challenging, because of the switched current sources. In many places was used standard matching solutions, like the bias circuit operational amplifier differential pair – two transistors which allows to use a

standard common-centroid matching solution. Also the H-bridge output transistors were very easy to match. It was a difficult task to mach all switched current source transistor, all together 24 current sources consisting of 80 separate transistors. This work was experimental and successfully accomplished as can seen from measuring results of test microchips. The measuring results are presented in the Chapter 4.

Fig. 3.8 shows the photography of the manufactured chip.

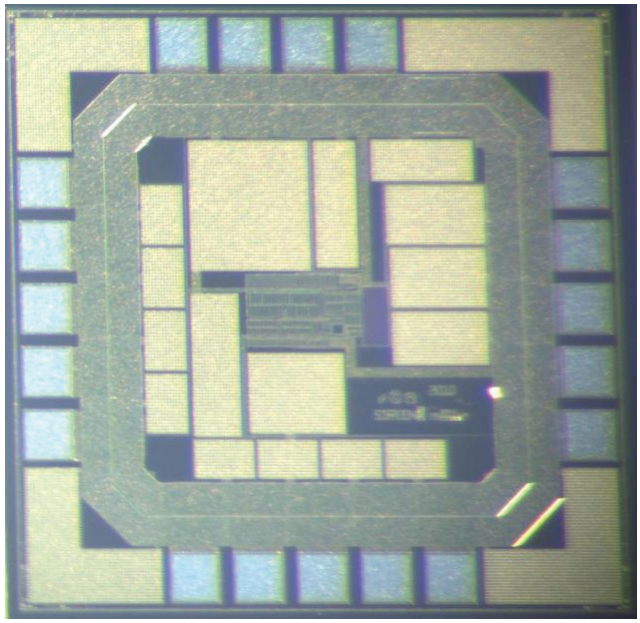


Fig. 3.8. The manufactured CMOS chip.

CHAPTER 4: MEASUREMENT RESULTS

Introduction

For testing of the manufactured current source demonstrators (chips) a simple printed circuit board (PCB) was designed. The manufactured chips are encapsulated into National Semiconductor LLP-20 (Leadless Leadframe Package) housing. The test PCB consists of one main board and of certain number of smaller DIP-20 (Dual In-line Package) PCB's, carrying the current source chip and ceramic capacitor for power supply bypass. Altogether all measurements were made using 10 current source chips.

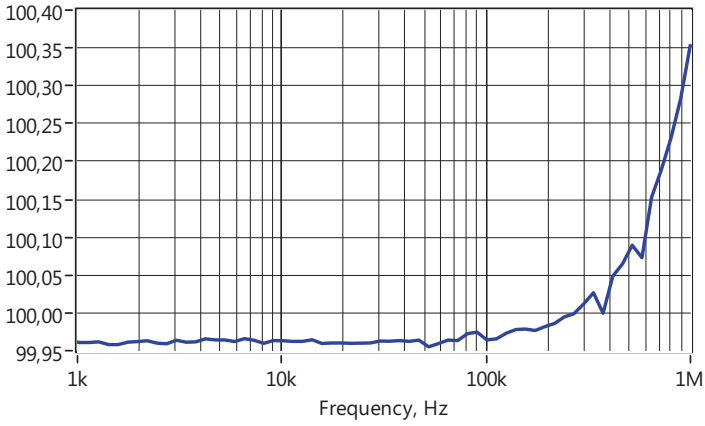
The current source chip needs two voltage sources – one for power supply and one constant voltage source for biasing (1.2 V). For this purpose an Agilent E3631A triple output power supply was used. To measure the chip current consumption the Agilent 3458A digital multimeter was used. The generation of the control signals for current sources chip (clips C1 to C6 and C1i to C6i) needs a flexible and high speed digital waveform generator. The National Instruments NI PXI-1042 general-purpose 8-slot chassis for PXI with NI PXI-6551 50MHz digital waveform generator card was chosen for experimental work. To measure the chip output response a LeCroy DA1855A stand-alone high-performance differential amplifier was used. The differential amplifier output signal was measured and analyzed using Agilent MSO8104A mixed signal oscilloscope.

To measure the chip output current the most important circuitry element is the load. The load is transferring the current to voltage and the voltage value can be measured using differential amplifier. For measurements two types of loads were used. First, the pure resistive load with value of 100 Ω was used, and secondly the combination of two resistors and one capacitor complex load was implemented. The last one is pretty similar to typical load of equivalent model of biological tissue discussed in Chapter 1.

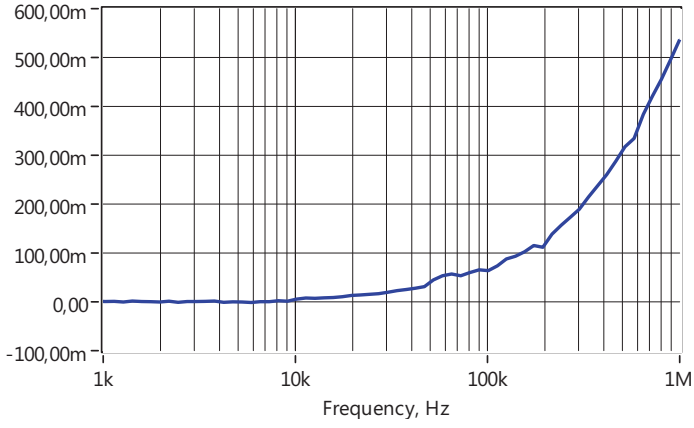
The 100 Ω metal film resistor is a perfect choice for the pure resistive load. The reason is that the values below 100 Ω for the resistors have an additional inductive component and the values of resistors over 100 Ω have an additional capacitive component. With other words, the impedance of low value resistors increases and the impedance of high value resistors decreases at higher frequencies. This information about resistors high frequency performance can be found in resistors datasheets, for example [Vishay, CHP, HCHP thick film high stability resistors datasheet (http://www.vishay.com/docs/52023/chp.pdf)]. Therefore the voltage on 100 Ω resistor should enough adequately show the current source chip output current response on different frequencies.

The magnitude and phase characteristics of an ordinary 1 % resistor were measured and the results are shown on Fig. 4.1. It was measured with the Wayne Kerr Electronics precision impedance analyzer 6500P. It is clearly seen that even an ordinary resistor behaves reasonably well for calibration within frequency range from 1 kHz to 1 MHz.

Therefore it can be clearly concluded, that measurements after the calibration are matching well within required accuracy limits (within 1 % of the selected full-scale range for each of the full-scale input impedance ranges) at different frequencies from kilohertz to megahertz.



(a)



(b)

Fig. 4.1. Ordinary 1 % metal film resistor characteristics, (a) magnitude characteristics of the 100 Ω resistor and (b) phase characteristics of the100 Ω resistor.

In major cases our activities focus on the question how the current source is acting together with the load (mimicking the biological tissue). This type of load

was discussed in chapter 1. The model of such a load consists of 100 Ω resistor with parallel contour – 100 Ω resistor in series with 10 nF capacitor (Fig. 4.2). To know how this type of load is acting applying the 30° shortened square wave current signal at higher frequencies a simple test circuitry for SPICE simulations was designed (Fig. 4.2). With the current source is connected a parallel resistor with value 1 MΩ what is equivalent to current source output resistance. The current source output resistance is depending from output current, the exact measured values can be found next in text from Table 4.2.

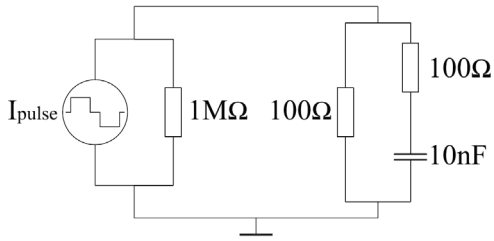
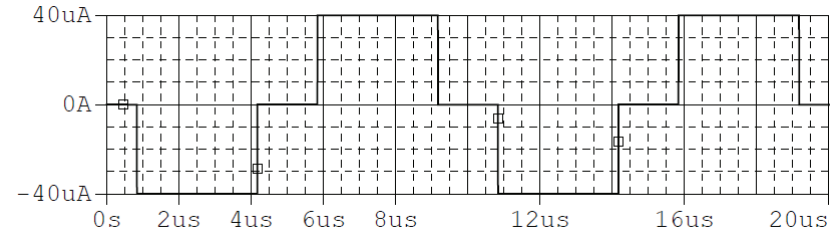
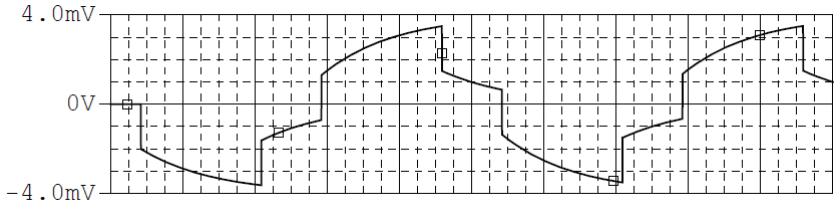


Fig. 4.2. Load (similar to biological tissue) model and SPICE test schematic.

The SPICE simulations show good performance of the current source chip with this type of load up to frequencies of 100 kHz. At higher frequencies the voltage drop on load decreases and the third harmonic level will increase slightly. The simulation results are shown on Fig. 4.3.



(a)



(b)

Fig. 4.3. The SPICE simulation results, (a) current from current source and (b) voltage response on biological tissue like load.

For the 30° shortened square wave signals the peak value of first harmonic should be about 1.102 times higher (usually the RMS value is used, and it is the peak value divided to √2) than the shortened square wave amplitude value. This assumption tells us that for the 30° shortened signal with the amplitude of 40 μA should give the first harmonic peak value approximately of 4.41 mV or RMS value of 3.12 mV on the load of 100 Ω. The SPICE simulations match (Fig. 4.4) with the spectrum peak values for the given signals presented on the Fig. 4.3. The capacitance counterpart in the load decreases the value of voltage response of the first harmonic about 24.5 %. Other harmonics values have decreased as: the 5^{th} 53.3, the 7^{th} 49.9, the 11^{th} 49.8, the 13^{th} 40.9, the 17^{th} 58.1 and the 19^{th} 45.1 %.

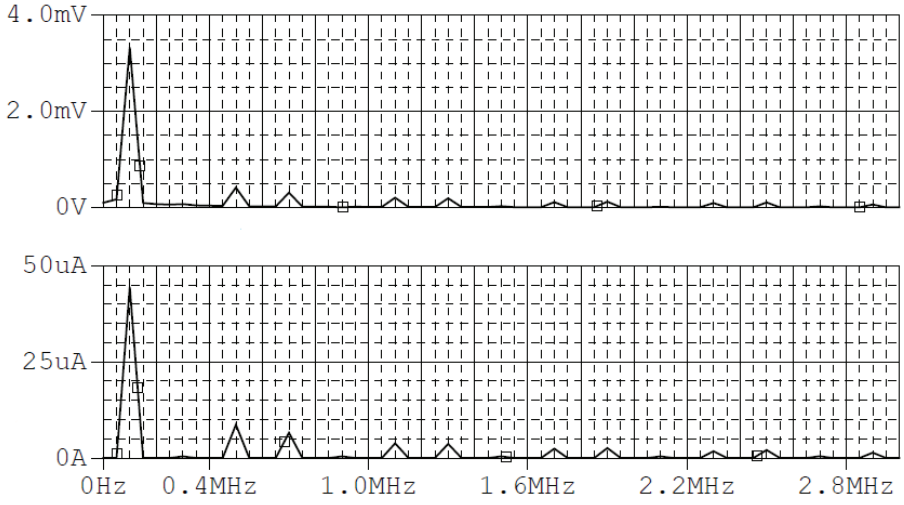


Fig. 4.4. Voltage and current signal spectral responses on biological tissue like load.

Measured signal spectrums and SPICE simulations are in a good agreement giving for the same type of load very alike results (see next in text: 24.5, 47.4, 52.4, 50.3, 56.3, 52.1 and 47.9 %).

Static values

The absolute minimum power supply voltage for the current source chip was measured to be equal to 2.4 V. The used CMOS process allows the maximum power supply voltage not higher than 5.5 V. The chips therefore were tested at supply voltage equal to 5 V. The average current consumption from power supply source for tested chips is shown in Table 4.1. In all measurements the load was taken equal to 100 Ω.

Table 4.1. Average current consumption of measured chips.

Selected current sources	At power supply 2.4 V	At power supply 3 V	At power supply 5 V
All current sources switched OFF	8.0 μA	9.6 μA	11.9 μA
C1 (5 μA)	15.1 μA	17.0 μA	19.8 μA
C3 (10 μA)	21.9 μA	24.3 μA	27.5 μA
C4 (20 μA)	35.4 μA	38.7 μA	42.8 μA
C6 (40 μA)	61.6 μA	67.5 μA	73.1 μA
∑C1,C6 (45 μA)	68.1 μA	74.7 μA	80.7 μA
∑C3,C6 (50 μA)	74.5 μA	81.9 μA	88.3 μA
∑C4,C6 (60 μA)	87.0 μA	96.1 μA	103.3 μA
∑C4,C5,C6 (80 μA)	117.6 μA	125.2 μA	133.7 μA
∑C1 to C6 (100 μA)	144.3 μA	153.6 μA	163.5 μA

The current consumption increase should be in the range of current increase through the bias circuit. But in reality the current consumption increases more rapidly. The reason concludes from the behavior of the current source transistors output resistance value: the output current depends on power supply voltage value, as we have discussed it in Chapter 2. In the saturation region the MOSFET transistor behaves like current source in parallel with a resistor. This resistive component is called the MOSFET output resistance. Looking from MOSFET output *I-V* curve, we can calculate the output resistance as:

$$r_{out} \approx \frac{\Delta U_{DS}}{\Delta I_D} \,. \tag{4.1}$$

The current source chips were measured at two different power supply voltages: at 3 V and at 5 V. To calculate the H-bridge output approximate resistance the $\Delta U_{DS} = 5\ V - 3\ V = 2\ V$ and the average $\Delta I_D = I_{out\ at\ 5\ V} - I_{out\ at\ 3\ V}$ values are taken from measured values in Tables 4.4 and 4.5 (assuming that there are two transistors connected in series and therefore we calculate the sum of these two resistances). From the measured values then the new results can be calculated: the current source output resistance will be equal to about 6 MΩ at 5 μA, and will be equal to about 400 kΩ at 100 μA output current (Table 4.2). These results are acceptable and almost match with the calculated results in Chapter 2, but we have to take into account that the output impedance will decrease at higher frequencies.

Table 4.2. Average current source output resistances.

Selected current sources	Average r_{out}, MΩ
C1 (5 μA)	6.09
C2 (5 μA)	6.27
C3 (10 μA)	3.60
C4 (20 μA)	1.84
C5 (20 μA)	1.81
C6 (40 μA)	0.95
∑C1,6 (45 μA)	0.86
∑C1,2,6 (50 μA)	0.77
∑C1,2,3,6 (60 μA)	0.65
∑C1,2,3,4,6 (80 μA)	0.49
∑C1 to 6 (100 μA)	0.39

Looking the data in Table 4.3 we can see, that only at minimum power supply the output currents are almost within the ±1 % range as expected. The only exception with up to 5 % tolerance is the 5 μA range. As the power supply voltage increases, so is increasing also the output current. The measured data in tables (Tables 4.3 - 4.5) show approximately the 10 % increase of the output current in all current ranges (at power supply increase from 2.4 V to 5 V). Actually the difference in output current about 0.5 μA at different voltages (at 2.4 V the output current is equal to 5 μA, and at 5 V the output current is equal to 5.5 μA) does not play the critical role in our solution. Important is the matching between the current sources C1 to C6 and that the positive and negative amplitude values of output signal differ not more than 4 % (the difference in positive and negative amplitudes gives even harmonics). When the difference is 4 % then the ratio of first and second harmonics is 100. When we calculate the matching error between current sources, then the average error is the highest at 10 μA range, and it is equal approximately to 4.5 % and is the smallest at 5 μA range, and it is equal approximately to 2.5 %. In other ranges the error lays around 3.3 %. The amplitude difference is the highest at 5 μA range, and it is equal approximately to 2.6 %, and is the lowest at 100 μA range, and it is equal approximately to 1.3 %.

Table 4.3. Test chip nr 5 output currents at 2.4 V.

Selected current sources	**IC5**	
	Pos. value (μA)	Neg. value (μA)
C1 (5 μA)	5.15	5.11
C2 (5 μA)	5.25	5.05
C3 (10 μA)	10.08	9.89
C4 (20 μA)	20.12	20.22
C5 (20 μA)	20.18	20.00
C6 (40 μA)	39.89	39.74
∑C1,6 (45 μA)	44.77	44.68
∑C1,2,6 (50 μA)	49.63	49.48
∑C1,2,3,6 (60 μA)	58.81	58.69
∑C1,2,3,4,6 (80 μA)	81.14	81.40
∑C1 to 6 (100 μA)	101.08	101.18

Table 4.4. Test chips output currents at 3 V.

Selected current sources	IC1		IC2		IC3		IC4		IC5	
	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)
C1 (5μA)	5.90	5.74	5.21	5.49	5.09	5.28	5.07	5.39	5.36	5.39
C2 (5μA)	5.78	5.70	5.35	5.52	5.09	5.34	5.17	5.33	5.52	5.35
C3 (10μA)	11.73	11.40	10.47	11.21	10.33	10.80	10.17	10.68	10.70	10.76
C4 (20μA)	23.01	22.61	21.15	21.92	20.59	21.51	20.66	21.35	21.45	21.77
C5 (20μA)	22.59	22.89	21.10	21.79	20.66	21.47	20.90	21.06	21.62	21.49
C6 (40μA)	45.29	45.58	41.73	44.02	41.51	42.21	42.23	42.00	43.23	43.16
∑C1,6 (45μA)	50.81	51.17	46.94	49.42	46.69	47.46	47.53	47.36	48.62	48.64
∑C1,2,6 (50μA)	56.14	56.73	52.15	54.75	51.75	52.72	52.72	52.55	54.03	53.93
∑C1,2,3,6 (60μA)	67.18	67.86	62.59	65.70	62.02	63.17	62.90	62.96	64.56	64.58
∑C1,2,3,4,6 (80μA)	88.82	89.43	83.35	86.92	82.82	84.37	83.85	84.09	86.18	86.43
∑C1 to 6 (100μA)	110.04	111.08	104.27	107.56	103.47	105.42	104.82	104.69	107.59	107.78
Selected current sources	**IC6**		**IC7**		**IC8**		**IC9**		**IC10**	
	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)
C1 (5μA)	5.53	5.67	5.12	5.31	5.38	5.60	5.32	5.45	5.38	5.16
C2 (5μA)	5.50	5.62	5.18	5.31	5.24	5.37	5.31	5.46	5.26	5.23
C3 (10μA)	10.29	10.83	10.35	10.40	10.39	10.70	10.32	10.71	10.55	10.08
C4 (20μA)	20.73	21.82	20.55	20.59	20.62	21.09	20.59	20.98	20.78	20.36
C5 (20μA)	20.73	21.82	20.72	20.68	20.83	21.11	20.77	21.10	21.16	20.69
C6 (40μA)	41.67	43.60	41.48	41.53	41.78	41.96	41.11	41.65	42.28	41.29
∑C1,6 (45μA)	47.05	48.93	46.62	46.87	47.20	47.32	46.30	46.93	47.56	46.43
∑C1,2,6 (50μA)	52.32	54.24	51.72	52.15	52.32	52.34	51.37	52.09	52.56	51.60
∑C1,2,3,6 (60μA)	62.44	64.52	61.96	62.38	62.45	62.55	61.27	62.35	62.80	61.54
∑C1,2,3,4,6 (80μA)	83.23	85.67	82.65	82.87	82.95	83.09	81.42	82.79	83.30	81.89
∑C1 to 6 (100μA)	103.90	106.48	103.35	103.28	103.52	103.50	101.57	103.02	104.02	102.24

Table 4.5. Test chips output currents at 5 V.

Selected current sources	IC1		IC2		IC3		IC4		IC5	
	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)
C1 (5μA)	6.20	6.16	5.54	5.92	5.45	5.71	3.21*	4.27*	5.74	5.71
C2 (5μA)	6.06	6.19	5.68	5.97	5.41	5.86	5.74	4.85	5.85	5.65
C3 (10μA)	12.05	12.04	11.02	11.87	10.88	11.48	10.89	11.09	11.25	11.20
C4 (20μA)	23.69	23.56	22.21	23.10	21.69	22.82	21.74	22.23	22.57	22.78
C5 (20μA)	23.42	23.93	22.33	22.54	21.75	23.01	22.01	21.92	22.59	22.50
C6 (40μA)	46.71	47.64	43.64	46.14	43.66	44.53	44.21	43.60	45.29	45.12
∑C1,6 (45μA)	52.42	53.42	49.05	51.71	49.11	50.00	45.21	49.27	50.91	50.79
∑C1,2,6 (50μA)	57.96	59.31	54.45	57.33	54.35	55.52	50.59	54.72	56.52	56.35
∑C1,2,3,6 (60μA)	69.39	70.89	64.97	68.48	65.05	66.43	61.33	65.47	67.44	67.33
∑C1,2,3,4,6 (80μA)	92.01	93.15	86.99	90.83	86.90	88.64	83.15	87.03	90.01	90.10
∑C1 to 6 (100μA)	114.26	115.74	108.99	110.39	108.49	110.93	105.58	108.59	112.28	112.49
Selected current sources	**IC6**		**IC7**		**IC8**		**IC9**		**IC10**	
	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)	Pos. value (μA)	Neg. value (μA)
C1 (5μA)	5.79	5.99	5.56	5.70	5.72	5.99	5.64	5.81	5.72	5.60
C2 (5μA)	5.75	5.94	5.54	5.64	5.64	5.83	5.63	5.81	5.60	5.57
C3 (10μA)	11.21	11.58	11.18	11.20	11.16	11.59	10.93	11.35	11.35	10.97
C4 (20μA)	22.35	23.26	22.20	22.15	22.20	22.71	21.80	22.22	22.25	21.99
C5 (20μA)	22.32	23.18	22.26	22.26	22.44	22.79	21.99	22.27	22.48	22.09
C6 (40μA)	44.61	46.32	44.31	44.26	44.72	44.93	43.33	43.92	44.73	44.00
∑C1,6 (45μA)	50.24	51.92	49.73	49.85	50.33	50.56	48.74	49.45	50.23	49.43
∑C1,2,6 (50μA)	55.70	57.52	55.03	55.34	55.68	55.86	54.02	54.86	55.51	54.79
∑C1,2,3,6 (60μA)	66.71	68.61	66.14	66.37	66.64	66.92	64.41	65.61	66.31	65.34
∑C1,2,3,4,6 (80μA)	88.58	90.75	87.92	87.87	88.19	88.47	85.73	87.08	88.20	86.95
∑C1 to 6 (100μA)	110.30	112.73	109.71	109.42	109.87	110.05	106.98	108.48	110.05	108.51

* The IC4 started to act weird at 5 V.

Dynamic values

The dynamic values were measured according to simulation results in Chapter 2. All measurements are made with power supply equal to 3 V. First we measured the behavior of the designed chip at relatively low frequencies (at 1 kHz), and at two different output current. To the current source output was connected the 100 Ω resistor and the measuring results are shown in Fig. 4.5 - 4.8. Because the voltage response on load resistor was measured, the Y-axis in next figures is showed in millivolts (mV), and not in microamperes. At low frequencies the 30° shortened square wave signal shape looks perfect and also the spectral responses (Fig. 4.6 and 4.8) are matching very well with the theoretical spectrums. Most important harmonics under inspection was the 5th and the 7th harmonics values. All spectral lines are RMS values (In chapter 2 the computer simulations give the peak values).

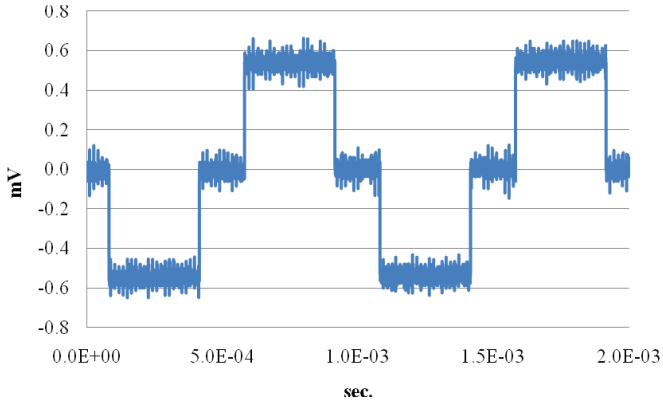


Fig. 4.5. Current source output at 5 μA and 1 kHz.

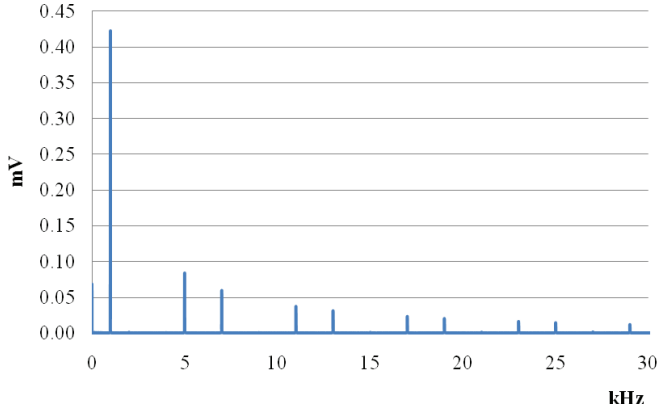


Fig. 4.6. 5 μA and 30° shortened square wave signal spectrum at 1 kHz.

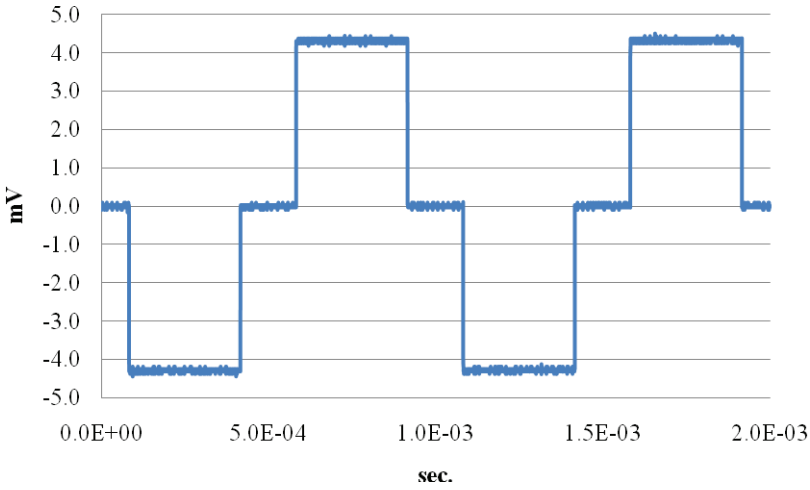


Fig. 4.7. Current source output at 40 μA and 1 kHz.

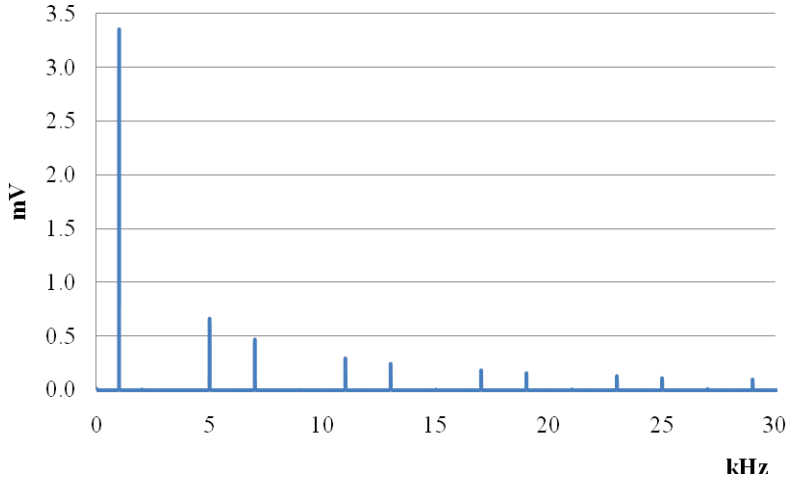


Fig. 4.8. 40 μA and 30° shortened square wave signal spectrum at 1 kHz.

As predicted, for the current source chip the absolute maximum working frequency is about 1 MHz, using the pure resistive 100 Ω load. The 5 μA output at 1 MHz is shown on Fig. 4.9. The output signal looks already like sine wave, but the spikes with attenuating oscillation and noise on the signal are also traceable.

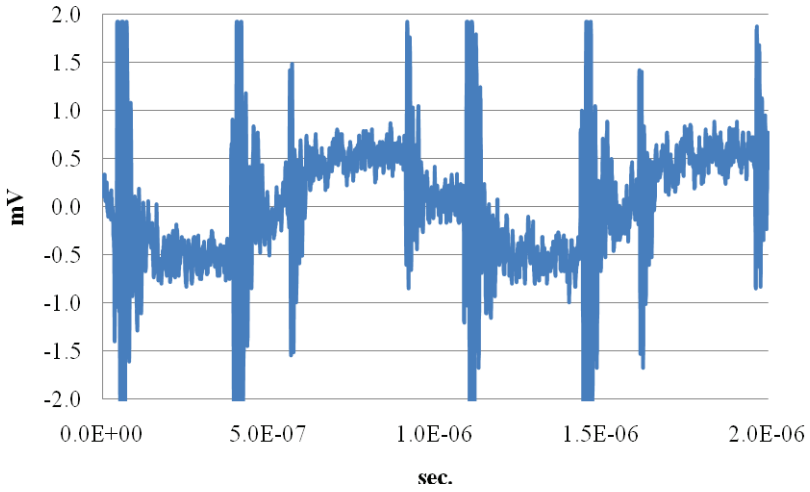


Fig. 4.9. Current source output at 5 μA and 1 MHz.

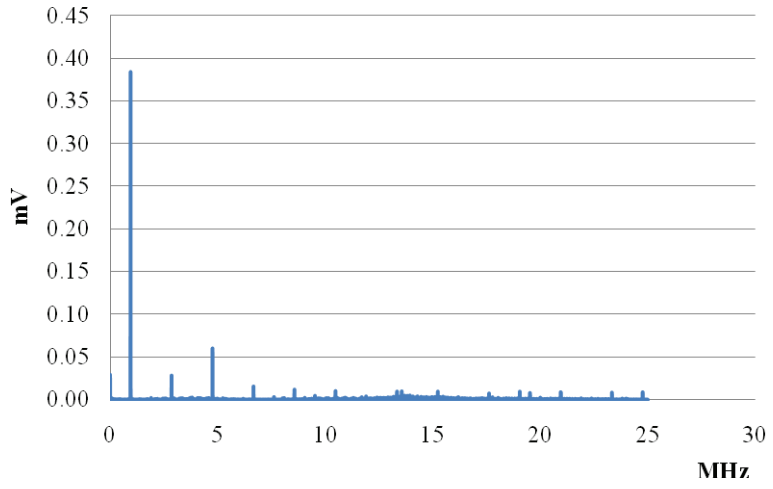


Fig. 4.10. 5 μA and 30° shortened square wave signal spectrum at 1 MHz.

Looking the spectral response on Fig. 4.10, then we see that the spikes have no influence on the first and on the fifth harmonics (all higher order harmonics are almost filtered out). The problem is, that we have third harmonic, which we cannot avoid. Also at higher output currents the shortened square wave signal is again recognizable (Fig. 4.11). The spectral response, shown in Fig. 4.12 has the similar form. Dominating are the fifth and the seventh harmonics and higher order ones are mostly filtered out. The third harmonic level is lower, but the

signal positive and negative amplitude must be uneven, because there are second and fourth harmonic in the spectrum.

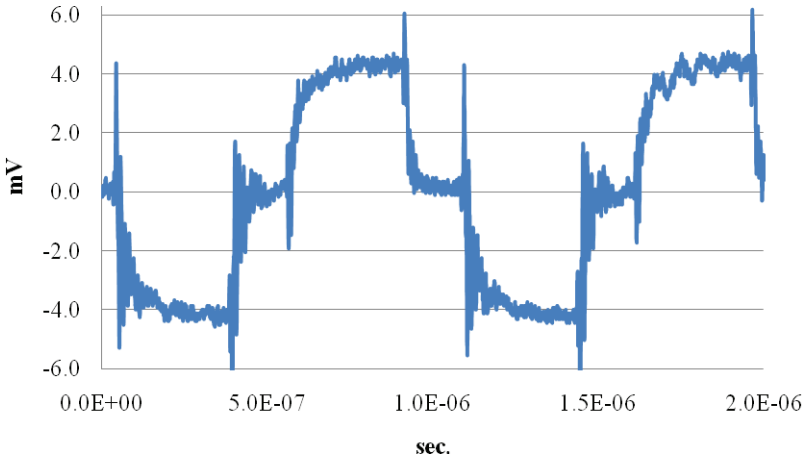


Fig. 4.11. Current source output at 40 µA and 1 MHz.

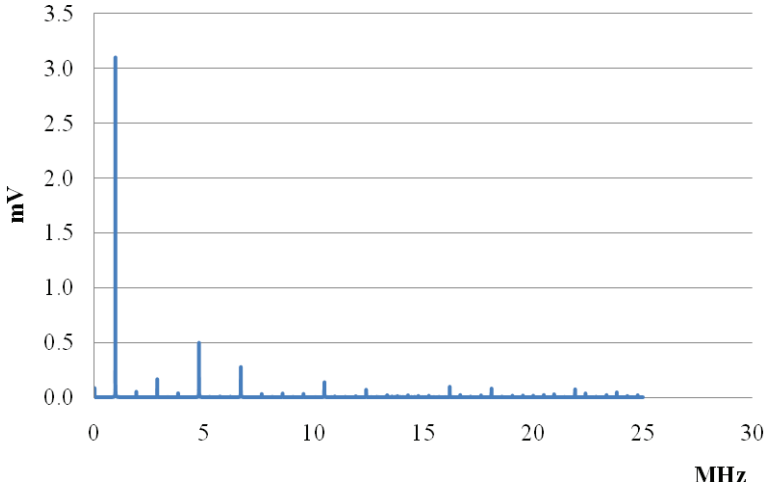


Fig. 4.12. 40 µA and 30° shortened square wave signal spectrum at 1 MHz.

As previously described in introduction we mostly want to know how the current source is acting together with loads mimicking the biological tissue. The simulation results was carried out on frequency 100 kHz and on two different output current 5 µA and 40 µA, the results are seen on Fig. 4.13 and Fig. 4.15. The spectral graphs are on Fig. 4.14 and 4.16. When the spectrum on Fig. 4.16 and the simulated spectrum on Fig. 4.4 are compared then can be seen that the spectral components are almost equal, only there is the third harmonic spike. In

simulation the capacitance counterpart in the load decreases the value of voltage response of the first harmonic about 24.5 %. Other harmonics values have decreased as: the 5th 53.3, the 7th 49.9, the 11th 49.8, the 13th 40.9, the 17th 58.1, and the 19th 45.1 %. Comparing it with measured results, the result is: 1st 24.5, 5th 47.4, 7th 52.4, 11th 50.3, 13th 56.3, 17th 52.1 and 19th 47.9 %.

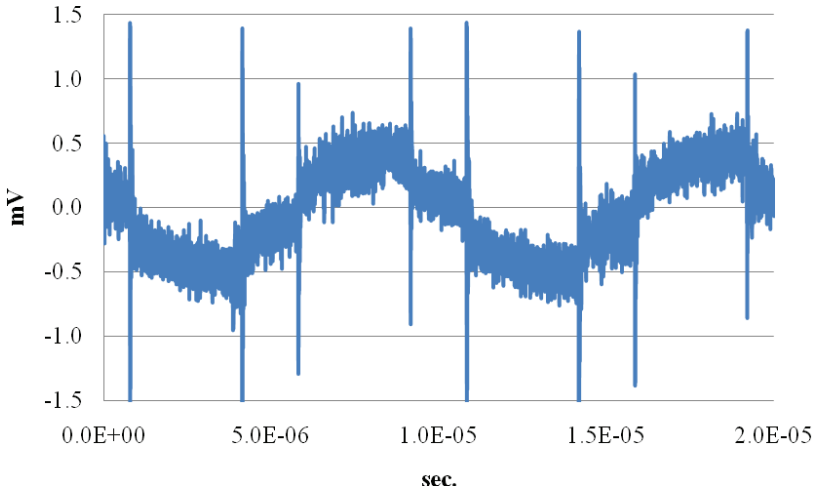


Fig. 4.13. Current source output to biological tissue like load at 5 μA and 100 kHz.

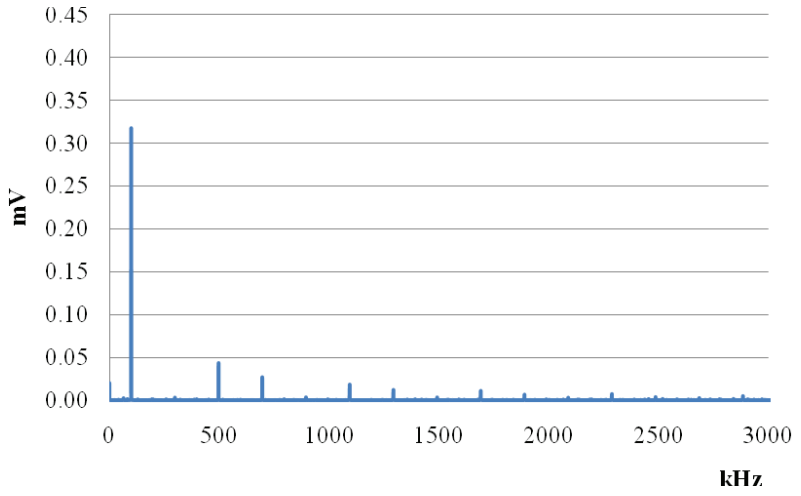


Fig. 4.14. 5 μA and 30° shortened square wave signal spectrum at 100 kHz.

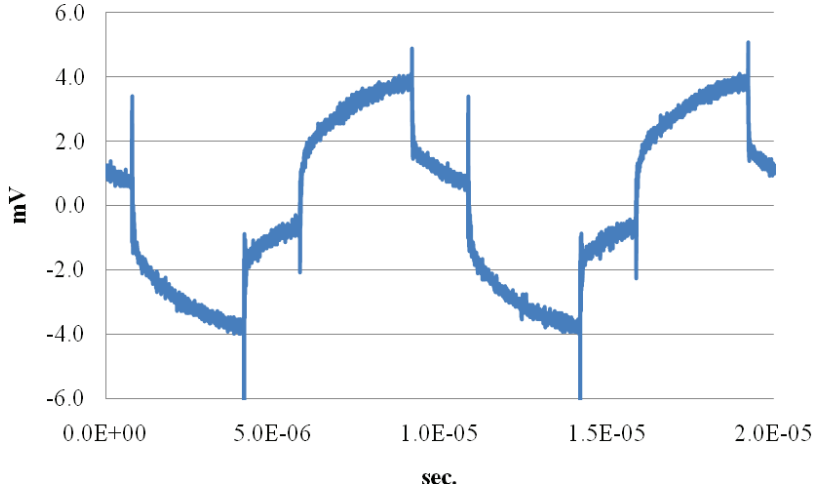


Fig. 4.15. Current source output to biological tissue like load at 40 μA and 100 kHz.

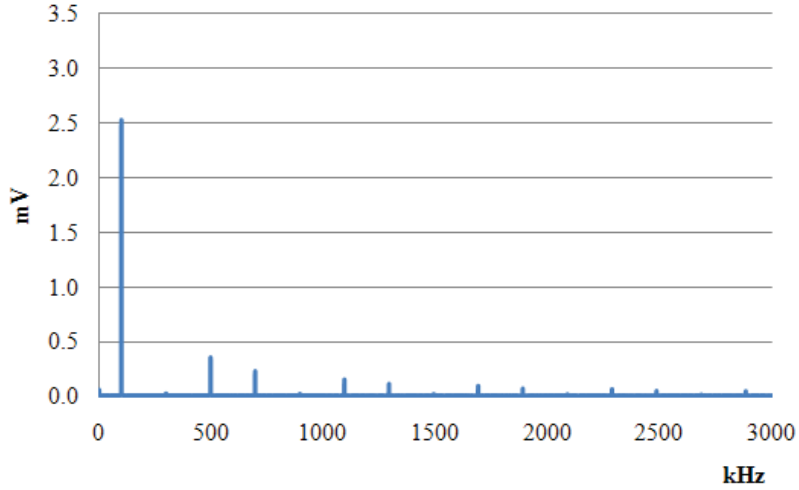


Fig. 4.16. 40 μA and 30° shortened square wave signal spectrum at 100 kHz.

Finally the current source chip was compared to its discrete component predecessor. Simplest four transistor circuit has been tested and implemented with good results [24]. Such a circuit (Fig. 4.17) is well suited for measurements with the aforementioned shortened square waves.

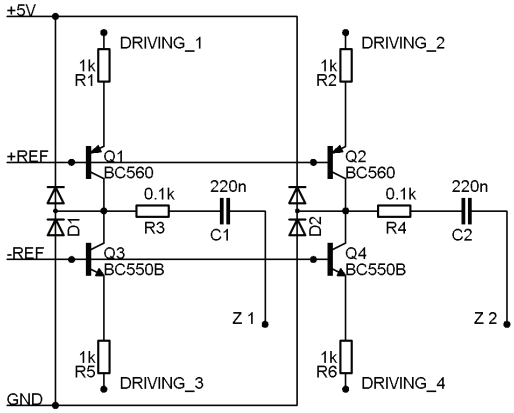


Fig. 4.17. Simplified schematics of the four transistors bridged V/I converter.

Inputs (Driving 1 - 4) are connected to the digital outputs of processor circuit, and impedance under investigation between electrodes Z1, and Z2. Practical tests show that such a simple design kit is functioning accurately at excitation frequencies from some tens of Hz up to 100 kHz with excitation currents from 1 µA to 1 mA. The only problem is that maximum frequency will be achieved only at 1 mA output current. This current source at 1.4 kHz with output current of about 250 µA into 100 Ω resistive load, measuring resulted in the waveform shown in Fig. 4.18. The problem is that the current source output response to input digital control signals (to generate a 30° shortened square wave signal at speed 100 kHz) is not anymore 30° shortened square wave, as we see in Fig. 4.19. There is a delay and the reason for this is unknown.

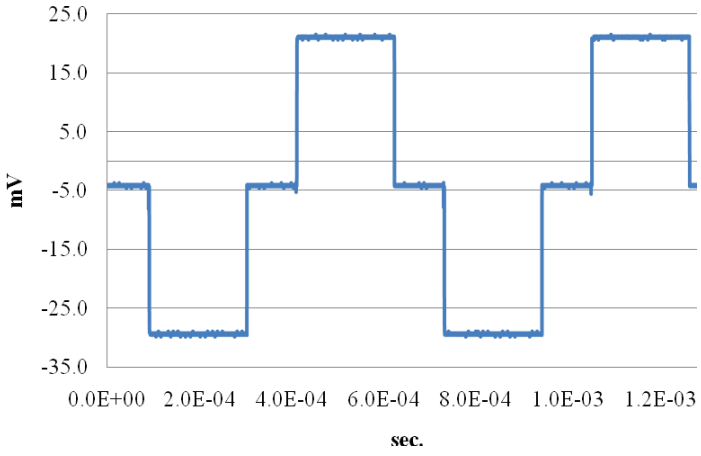


Fig. 4.18. Discrete component current source at 250 µA and 1.4 kHz.

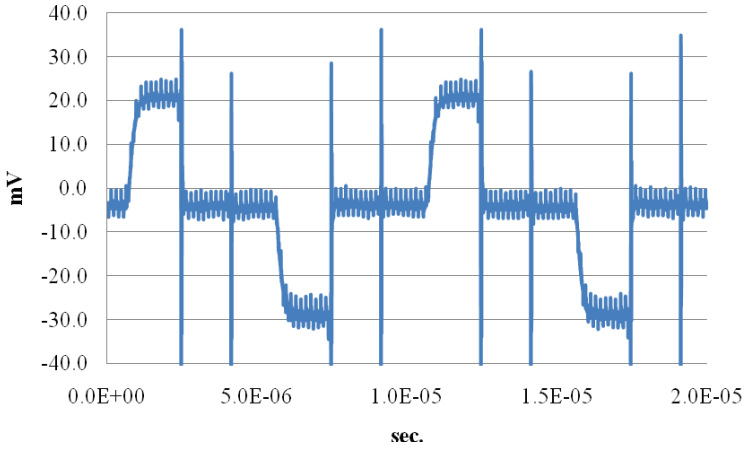


Fig. 4.19. Discrete component current source at 250 μA and 100 kHz.

Additional remark

The initial measurement system has some limitations and therefore more measurements had been done to better understand of the test chip behavior. During the dynamic measurements we discovered that if the input currents I_{OFF} and $I_{OFF}i$ are driving small switching transistors to discharge quickly the H-bridge current mirror transistors, the closing of the H-bridge transistors to third level (output signal zero level) at higher speed was expected. In reality it came out, that the output signal third harmonic level will increase, and therefore it is better to keep the I_{OFF} and $I_{OFF}i$ currents on their static value which holds the internal switching transistors steadily closed.

CONCLUSIONS

Present thesis summarizes author's research and engineering activities in the field of impedance measurement and analog chip design. Methods for fast and efficient impedance measurement have been investigated. The main goal of the research work was using specific, the shortened square wave signals technique, to design an efficient and simple current source for impedance measurements. This work bases strongly on previous work in the same field. The designed new current source has improved performance, higher speed and more precise pre-selected current values. The design and the realization of chips bases on technology offered by the National Semiconductor Estonia.

In the first chapter the theoretical bases for this work is discussed. Chapter gives an overview of a biological tissue like model and its impedance. A brief description of the signal theory and advantageous of shortened square wave signals and their spectral responses is presented as well.

The second chapter shows the CMOS process transistors limitations, which sets the limitations to our current source design. Still the high speed switched current source implementation was possible and the computer simulations were showing promising results.

Following novel and important results have been achieved:

1) Reduced circuit complexity and very simple schematic solution gives very good results: provide at high operating speed and very accurate output currents.
2) The current source is extremely effective:
   a) Thank to the current mirroring ratios the overall power consumption is only about 1.5 times higher compared to the current flowing into the load;
   b) The measuring cycles can be made short and in stand-by regime only the bias circuit consumes power.

In the third chapter the layout design and matching problems have been discussed. Because of the mirrored current from the bias transistor to many current source transistors, the matching is pretty difficult and complex.

Following new and important result is achieved:

3) Complexity of matching (mostly experimental) was recognized preliminarily in computer simulation. Important is that the measurements on manufactured chips affirm the good results

predicted by simulations. Thank to smart matching, the developed and designed chip solution insures all the most important parameters of the circuitry developed for current source.

The fourth chapter summarizes the real current source chips measuring results. First, the chips were functioning properly, but the measured currents gave a bit higher error than expected. The reason was very simple: the test system malfunctioned due to the wrongly configured control signals introducing the incorrect logical values. After redesign of the test system, all the measurement results with the predicted design and simulation results, and for the current source all frequencies from tenth of hertz up to 1 MHz, at all output currents are acceptable.

Achieved results should ultimately advance the art of impedance measurements, enhance medical diagnostics and decrease the costs in healthcare sector.

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List of authors' publications directly connected to the topic of dissertation (copies shown in Appendix)

Kasemaa, Argo; Annus, Paul (2008). CMOS current source for shortened square wave waveforms. In: Proceedings of the 11th Biennial Baltic Electronics Conference: 2008 International Biennial Baltic Electronics Conference (BEC2008) Tallinn, Estonia, October 6-8, 2008. , 2008, 119 - 120.

Kasemaa, Argo; Annus, Paul (2010). CMOS technology based current source with harmonic reducing properties. Electronics and Electrical Engineering, 143 - 146.

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APPENDIXES

Publication I

Kasemaa, Argo; Annus, Paul (2008). CMOS current source for shortened square wave waveforms. In: Proceedings of the 11th Biennial Baltic Electronics Conference: 2008 International Biennial Baltic Electronics Conference (BEC2008) Tallinn, Estonia, October 6-8, 2008. , 2008, 119 - 120.

CMOS current source for shortened square wave waveforms

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ABSTRACT: In many practical cases sinusoidal signals can be replaced with suitable approximations. Well-known alternative is the three level shortened square wave. By introducing more equally spaced levels, higher harmonics can be further reduced. This multilevel signal is easy to generate digitally and enables simple digital processing involving only additions and shifting. An efficient CMOS technology based current source can be designed to work with such waveforms. The current source consists of Beta-multiplier type biasing circuit, switchable current mirrors and H-bridge output stage. In this case the use of H-bridge output permits possibility to avoid the conventional instrumentation amplifier (simple buffer can be used), resulting a reduction of the whole measuring system complexity.

1. Introduction

Synchronous signal processing enables measurement of low-level signals with lock-in amplifiers, and is used in different network analyzers. Classically sinusoidal excitation is used, and Fast Fourier Transformation (FFT) or similar takes care of spectral separation. It enables determination of magnitude and phase of the response signal compared to the excitation signal, and gives relatively good results, depending on the quality of the excitation signal and signal processing algorithms. Situation changes dramatically in case of implantable devices, such as pacemakers. Both analog circuitry and digital signal processing tend to consume a lot of energy, and size of the device should be kept as small as possible. It is not necessary to measure with sinusoidal excitation current. Systematic errors introduced by higher harmonics of simple square wave signals can be drastically reduced by slightly modifying the waveform [1]. In case of shortening the excitation and reference signals by 30° and 18° (Fig. 1) errors can be reduced by order of magnitude in comparison with regular rectangular waves

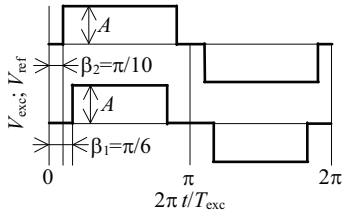

Fig.1 Shortened square wave pulses: 18° shortened three-level signal a), and 30° shortened three-level signal b)

Spectra of these signals can be expressed as the Fourier series of odd harmonics:

$$F(\omega t)=\frac{4A}{\pi}\left[\frac{\cos\beta}{1}\sin\omega t+\frac{\cos 3\beta}{3}\sin 3\omega t+...\right]=\frac{4A}{\pi}\left[\sum_{i=1}^{\infty}\frac{\cos(2i-1)\beta}{2i-1}\sin(2i-1)\omega t\right]$$

$$F(\omega t)=\frac{4A}{\pi}\left[\frac{\cos\beta}{1}\sin\omega t+\frac{\cos 3\beta}{3}\sin 3\omega t+...\right]=\frac{4A}{\pi}\left[\sum_{i=1}^{\infty}\frac{\cos(2i-1)\beta}{2i-1}\sin(2i-1)\omega t\right] \quad (1)$$

where A is the amplitude of the pulse signal. Synchronous demodulation is sensitive only to higher harmonics, which are existing simultaneously in both, the excitation and reference signals, such as 7th, 11th, 13th, 17th, 19th, 23rd, 29th, and 31th in case of 30°/18° shortened signals. Even better results can be achieved by using different suitable sums of such a waveforms together with introducing third 42° shortened three level square wave. When we sum three signals 18° shortened signal with + sign, 30° shortened signal with – sign, and 42° shortened signal with + sign new waveform is free from both the 3rd and 5th harmonics. Even 7th harmonic has been reduced by few % compared to square wave. Higher harmonics on the other hand are relatively high. It can be improved with changing the addition coefficients from 1, -1, 1 to 2, -1,1 [2]. Resulting waveform can be seen on Fig. 2. Appearing 3rd and 9th harmonics could pose a problem, however in case of suitably chosen signal pair it is possible to eliminate them from the multiplication result. One possible candidate for such a pairing signal is sum of 18°, 30° and 42° shortened signals with +1 coefficients.

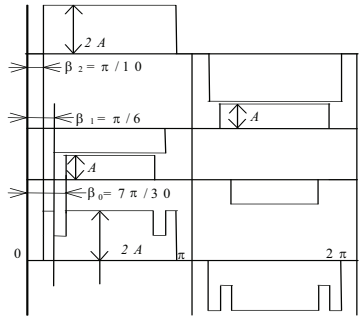

Fig.2 Sum of three shortened square wave pulses

Signal forming for excitation is similarly simple. It is worth noting here that compared to piecewise continuous approximations of sinusoidal signals using equal levels is much more feasible in digital domain of signal generation.

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2. CMOS Current Source

To utilize the shortened square wave waveform theory into practice, a low voltage and low power current exciter must to be designed. The aim was to design a flexible current source with output current range from 5 to 300µA and working with supply voltage range from 2,2 to 3V.

The current source consists of Beta-multiplier type biasing circuit, switchable current mirrors and H-bridge output stage. In this case the use of H-bridge output permits possibility to avoid the conventional instrumentation amplifier (simple buffer can be used), resulting a reduction of the whole measuring system complexity.

The MOS transistor output current range is unfortunately limited. Usually the output current range is one decade, when we are working at low power supply voltage region and want to stay in saturation region and strong inversion mode. To achieve at low voltage design the needed output range from 5 to 300µA, at least two different output current H-bridges must to be connected in parallel to sum the currents. In this design four different current sources are connected in parallel, Fig. 3. All output stages are biased from the same source (Vbiasn and Vbiasp) and each stage can be switched to give out two different current values, see Table 1. To switch between two current value control signals c1 and c2 are used. Also all stages can be switched separately off. At the moment there are twenty four control signals needed to control all four output stages (for testing purpose). The end version will only have two or three control signal inputs on each stage.

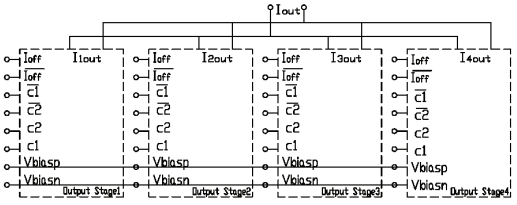

Fig.3 Current source block diagram.

Table 1

	c1	c2
Output stage 1	5 µA	20 µA
Output stage 2	10 µA	40 µA
Output stage 3	20 µA	80 µA
Output stage 4	40 µA	160 µA

The output stage schematic is given in Fig. 4. The Vbiasn and Vbiasp signals are driving current sources, transistors M1 to M4 and M19, M20, M23, M24. The currents are switched through transistors M5 to M8 and M17, M18, M21, M22 to current mirrors M9 to M12 and M13 to M16. The H-bridge can be switched off using transistors M25 to M28 or using control signals c1, $\bar{c}1$, c2 and $\bar{c}2$.

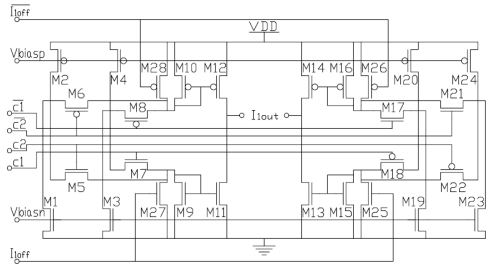

Fig.4 Output stage schematic.

The goal is to achieve at least ±1V output voltage at all current ranges with different load resistances. To get high speed, we need to use minimum channel lengths and design with a large $V_{DS,sat}$ [3]. The output transistors (M11 to M14) maximum $V_{DS,sat}$ can be 0,6V (at 2,2V Vdd). The transition frequency f_T can be calculated:

$$f_T \approx \frac{g_m}{2\pi C_{gs}} = \frac{3\mu_p}{4\pi} \cdot \frac{V_{DS,\,sat}}{L^2} \qquad (2)$$

The calculated PMOS transistors f_T at smallest possible current is 150MHz and highest 800MHz.

For good current mirror matching the long channel is preferred, also the longer channel increases the output resistance. Good compromise between channel length and speed can be L=2..4λ.

$$r_o = \frac{1}{\lambda I_{D,\,sat}} \quad \text{or} \quad r_o \propto \frac{L^2}{V_{DS,\,sat}^2} \qquad (3)$$

The calculated H-bridge transistors' output resistance at highest output current is around 600kΩ.

3. Conclusions

The design of an efficient CMOS technology based low power high speed current source has started. The CMOS technology to realize the microchip is not chosen yet, 0,35µm technology looks promising. The preliminary circuit calculations are made with using 0,6µm CMOS technology parameters.

4. Acknowledgement

The authors wish to thank the Estonian Ministry of Education and Research, the Estonian Science Foundation for the support of this research through the target oriented project SF0142737s06 and the research grant G7183, and the Competence Centre ELIKO for support as well.

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Publication II

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CMOS Technology based Current Source with Harmonic Reducing Properties

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Introduction

The replacement of sinusoidal signals in many practical cases can be solved using suitable approximations. The three level shortened square waves' technique could be used. The basic idea of such a solution is that more equally spaced converting levels are introduced, and therefore higher harmonics, especially the lower end of higher harmonics, can be reduced. This multilevel signal can be easily generated digitally and it enables simple digital processing involving only additions and shifting. An efficient CMOS technology based current source can be designed to work with such nontraditional waveforms. The current source consists of circuit, switchable current mirrors to select different current ranges and H-bridge current output stage. In this case the use of H-bridge current output permits possibility to avoid the conventional instrumentation amplifier (simple buffer amplifier can be used), resulting a reduction of the whole measuring system complexity.

This paper proposes an advanced solution for the shortened square wave CMOS current source with H-bridge current output. The analysis of the proposed system is given and new practical solutions for applications in portable devices are described. The proposed solution improves the power consumption and reduces the complexity of the system as a whole. The main advantage of this method is greater efficiency because of the fact that for measuring cycle only one or two pairs of switchable current mirrors will be activated to drive the H-bridge.

Shortened square waves

Synchronous signal processing enables measurement of low-level signals with lock-in amplifiers, and is used in different network analyzers. Classically sinusoidal excitation is used and Fast Fourier Transformation (FFT) or similar takes care of spectral separation. It enables determination of magnitude and phase of the response signal compared to the excitation signal, and gives relatively good results, depending on the quality of the excitation signal and signal processing algorithms. Situation changes dramatically in case of implantable devices, such as pacemakers. Both analog circuitry and digital signal processing tend to consume a lot of energy, and size of the device should be kept as small as possible. It is not necessary to measure with sinusoidal excitation current. Systematic errors introduced by higher harmonics of simple square wave signals can be drastically reduced by slightly modifying the waveform [1]. In case of shortening the excitation and reference signals by 30° and 18° (Fig. 1) errors can be reduced by order of magnitude in comparison with regular rectangular waves

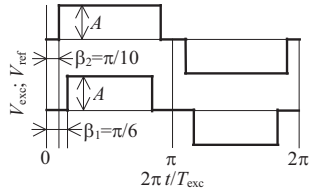

Fig. 1. Shortened square wave pulses: 18° shortened three-level signal (a); and 30° shortened three-level signal (b)

Spectra of these signals can be expressed as the Fourier series of odd harmonics

$$F(\omega t)=\frac{4A}{\pi}\left[\frac{\cos\beta}{1}\sin\omega t+\frac{\cos 3\beta}{3}\sin 3\omega t+\ldots\right]=\frac{4A}{\pi}\left[\sum_{i=1}^{\infty}\frac{\cos(2i-1)\beta}{2i-1}\sin(2i-1)\omega t\right], \quad (1)$$

where F is the Fourier spectra; A is the amplitude of the pulse signal, ω is the repetition frequency, β is measure of shortening in degrees and i is the number of the harmonic. Synchronous demodulation is sensitive only to higher harmonics, which are existing simultaneously in both, the excitation and reference signals, such as 7th, 11th, 13th,

17th, 19th, 23rd, 29th, and 31th in case of 30°/18° shortened signals. Better result is achievable using different suitable sums of waveforms together with introducing third 42° shortened three level square wave. When we sum three signals as 18° shortened signal with + sign, 30° shortened signal with – sign, and 42° shortened signal with + sign, the new waveform is free from both the 3rd and 5th harmonics. Even 7th harmonic is reduced compared to square wave. Higher harmonics however are still relatively strongly present. This situation can be improved by changing the addition coefficients from 1, -1, 1 to 2, -1, and 1 [2]. Resulting waveform is shown on Fig. 2. Appearing 3rd and 9th harmonics could pose a problem; however in case of suitably chosen signal pair it is possible to eliminate them from the multiplication result. One possible solution for such a specific pairing signal is the sum of 18°, 30° and 42° shortened signals with coefficient +1.

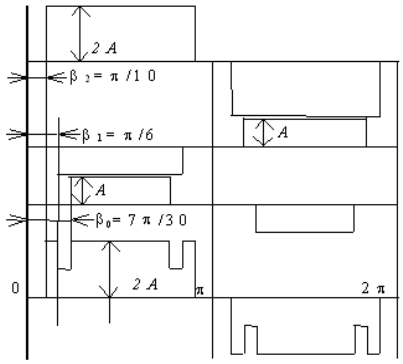

Fig. 2. Sum of three shortened square wave pulses

Signal forming for excitation is similarly simple as described earlier. It is worth noting here that a compared to piecewise continuous approximation of sinusoidal signals usage of equal levels is much more feasible in digital domain of signal generation.

CMOS Current Source

To utilize the shortened square waveform theory into practice, a low voltage and low power current exciter has to be designed. First the flexible current source with selectable output current in range from 5 to 500μA, and with supply voltage from 2.4 to 5V has been designed.

The core part of this current source will be the H-bridge output stage with multiple switchable current mirrors driving the output stage. Such realization of H-bridge output permits to use simple buffer amplifier, resulting a reduction of the whole measuring system complexity afterwards.

From the MOS transistor behavior we know that the output current range is limited. If we want to stay at minimum output current range in saturation region and strong inversion mode, then the H-bridge output transistor drain to source saturation voltage $V_{DS,\ sat}$ should not decrease below the four times thermal voltage V_T value. It means that at room temperature the minimum $V_{DS,\ sat}$ value should be about 100mV. On the other hand the $V_{DS,\ sat}$ cannot step over the 1V value due to the fact that the load impedance is about 100Ω (body tissue).

The MOS transistor drain current can be calculated [3–5]

$$I_D = \frac{KP}{2} \cdot \frac{W}{L} \cdot V_{DS,sat}{}^2, \qquad (2)$$

where the KP is the transconductance parameter, W is channel width, and L is channel length. In our case the $V_{DS,sat}$ is changing from 100mV to 1V. It means that the transistor drain current can change exactly from 5 to 500μA. The MOS transistor drain current changing interval is limited compared for example to the bipolar transistor collector current.

The next limiting factor is the single transistor output resistance r_O. To increase the output resistance and approximate the transistor output as an ideal current source, the cascode output stage must be introduced. Unfortunately the cascode output stage in H-bridge solution needs more than 3V power supply voltage. Therefore the test chip H-bridge output stage realization will use only single transistor solution.

Single transistor output resistance r_O can be calculated from formula [3]

$$r_O = \frac{1}{\lambda \cdot I_{DS,sat}}, \qquad (3)$$

where $I_{DS,sat}$ is the source drain saturation current and λ is the channel length modulation parameter. In this work the 0.5μm CMOS technology is used, where the channel lengths of output stage transistors are equal to 2μm. The λ value is approximately $0.01V^{-1}$. Using this data the single transistor output resistance at current level of 5μA will give the value of 20MΩ. At output current level of 500uA the 200kΩ output resistance will be calculated. Taking into the consideration that he output resistance below 1MΩ is undesirable; the current source test chip output current range should be in range from 5 to 100μA.

The current source required work frequency at 5μA output current should be at least 100 kHz. Single transistor transition frequency can be calculated as [3]

$$f_T \approx \frac{3KP \cdot V_{DS,sat}}{4\pi \cdot L^2 C'_{ox}}, \qquad (4)$$

where C'_{ox} is the oxide capacitance per unit area. In this work the C'_{ox} value is 1,75fF/μm^2, which is defined by used CMOS technology. The calculated minimum transition frequency for PMOS transistors is 146 MHz. This value gives the clear expectation that ON-OFF switching process of transistors with the 5μs time interval is enough to guaranty the fast enough slope rise and fall times for our application.

The design of the current source chip concludes with the 4x6 different current sources connected through switches to one H-bridge output stage. The current source as a black box is seen in Fig. 3. The current source needs two external bias signal pads to bias the inner circuitry – V_{biasn} and V_{biasp}. For switching and combining the currents

the 2x6 control inputs must be included (inputs c1 to c6 and their inversions) and two inputs to switch the H-bridge off (third) state. Table 1 shows the possible output current generating scheme for switching all of the six current sources to get the maximum 100µA output current.

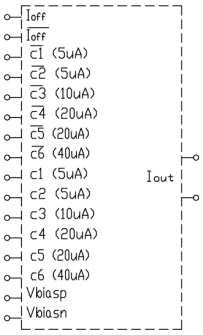

Fig. 3. Current source block diagram

Table 1. Possible output currents

Control signals	Iout
c1	5 µA
c2	5 µA
c3	10 µA
c4	20 µA
c5	20 µA
c6	40 µA

The schematic of the current source is given in Fig. 4. The V_{biasn} and V_{biasp} voltages are driving the current mirrors and afterwards the current is mirrored to 4x6 independent current sources. To achieve the simple current mirror ratio 1:1 the transistor matching error should stay ultimately bellow 2%. To fulfill the demand for so small error the channel length of the transistor must be at least four times over the minimum strip dimensions (0.5µm technology in our case) and the channel area (LxW) must be larger than 25µm^2. Unfortunately the bigger is the mirrored current and primal current ratio; the bigger is the matching error. The current mirroring ratios over 1:8 are therefore not usable. The attempt was made to find the best optimum for transistor channel length and width ratios so, that the matching error at 1:1 ratio stays under 2% and 1:8 ratio does not exceed 5%. The "worst case" simulation results are shown in Fig. 5. The design and calculations show that the current error for all added currents did not exceed the 5% level.

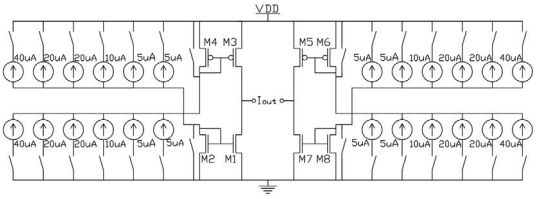

Fig. 4. Current source schematic

The current source simulation results in Fig. 5 exposit the H-bridge output current through the load. The resistors R7 and R8 were chosen equal to 1Ω in simulations and they are imitating the resistivity of the pad contacts. Load impedance, with low frequency value of 100Ω, is connected in series with this contact resistivity. In reality in most applications the load resistivity is complex and instead of resistivity the impedance must be handled.

Fig. 5 shows all the possible current values what can be generated and switching responses of the developed current source. When we are using the generated shortened square wave solutions, then only one certain current value like shown on Fig. 1, or two current values like on Fig. 2, will be used.

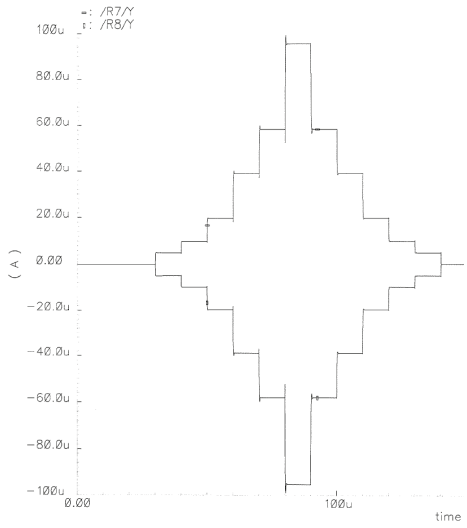

Fig. 5. Current source output current simulation results

The test chip is designed with the possibility to use external bias voltage. The nominal bias voltage value is chosen to be 1.2V. The low-power biasing circuitry solution is shown in Fig. 6.

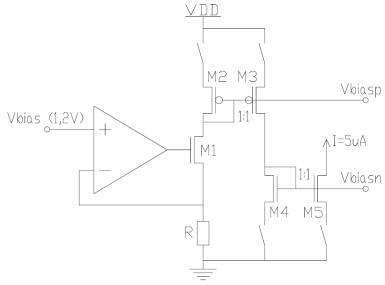

Fig. 6. Biasing circuit

The voltage to current conversion is realized using low-power operational amplifier, transistor M1 and resistor R. The weak point of this solution is the resistor R with nominal value 2400Ω. In used 0.5µm technology all resistors have unfortunately positive temperature coefficients. Additionally the lay-out geometry dimension of the resistor becomes too big. To scale down the resistor lay-out about 20% leads us to the one long channel NMOS transistor in series with resistor R, when the transistor is

working in linear region. The resistor nominal value will be then 190kΩ.

Results of the simulation comparing one 240kΩ resistor with 190kΩ resistor in series with n-channel transistor are shown on Fig. 7. The resistor in series with n-channel transistor gives the good output current stability in wide enough temperature range (from 0 to 40̊C), but only then when the input bias voltage stays at 1.2V.

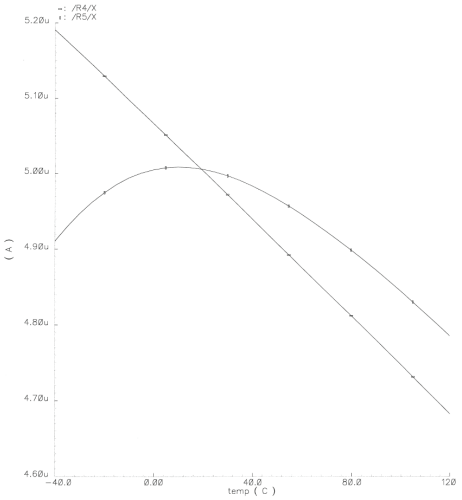

Fig. 7. Bias circuit output current temperature dependence simulations

Conclusions

The design of the CMOS technology based efficient low-power high speed current source has been made. The test chip layout has been made using NSC 0.5μm technology. The novel results are as follows:

- Reduced system circuit complexity and therefore smaller chip lay-out area.
- Greater efficiency, measuring cycles are short and in stand by regime only the bias circuit consumes power.

The next paper on this topic will include the realistic lay-out the whole designed circuitry and the experimental measurement results.

Acknowledgement

The present research work was supported by the company National Semiconductor Estonia, and by the Estonian Ministry of Education and Research (the target oriented project SF0142737s06), the Estonian Science Foundation (the research grants G7183 and G7243), and by the Foundation Archimedes and the European Regional Development Fund (Centre of Excellence CEBE; TK05U01).

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A. Kasemaa, P. Annus. CMOS Technology based Current Source with Harmonic Reducing Properties // Electronics and Electrical Engineering. – Kaunas: Technologija, 2010. – No. 10(106). – P. 143–146.

Multilevel higher harmonics reducing algorithm is proposed for digitally generated signal processing code involving only additions and shifting. An efficient CMOS technology based current source is designed to work with shortened square wave waveforms. The current source consists of biasing circuit, switchable current mirrors and H-bridge current output stage. The analysis of the proposed system is given and new practical solutions for applications in portable devices are described. The proposed solution improves the power consumption and reduces the complexity of the system as a whole. The main advantage of this method is greater efficiency because for measuring cycle only one or two pairs of switchable current mirrors will be activated to drive the H-bridge. Ill. 7, bibl. 5, tabl. 1 (in English; abstracts in English and Lithuanian).

A. Kasemaa, P. Annus. Srovės šaltinio harmonikų mažinimo ypatybės taikant KMOP technologiją // Elektronika ir elektrotechnika. – Kaunas: Technologija, 2010. – Nr. 10(106). – P. 143–146.

Pasiūlytas naujas daugiapakopis aukštesniųjų harmonikų mažinimo algoritmas. Jis sukurtas atlikus generuojamo signalo papildymus ir pakeitimus. KMOP technologijos pagrindu suprojektuotas srovės šaltinis, dirbantis su sutrumpintos stačiakampės formos signalais. Pateikta naujų pasiūlytos sistemos praktinio taikymo mobiliems įrenginiams būdų. Nors įdiegus šį pasiūlymą padidėja energijos sąnaudos, tačiau supaprastėja visa sistema. Pagrindinis šio metodo pranašumas – didesnis efektyvumas. Il. 7, bibl. 5, lent. 1 (anglų kalba; santraukos anglų ir lietuvių k.).

Publication III

Kasemaa, Argo; Rang, Toomas (2010). Low power CMOS current source for shortened wave signals. In: Proceedings of the 12th Biennial Baltic Electronic Conference BEC2010: IEEE 2010 12th Biennial Baltic Electronics Conference. (Toim.) T. Rang, P. Ellervee, M. Min. Tallinn: TTU Press, 2010, 89 - 92.

Low power CMOS current source for shortened square wave signals

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ABSTRACT: The paper gives short overview of an efficient CMOS technology based current source realization and layout design. The current source output will be shortened square wave signal [1],[2] and [3]. The output current value can be selected from range 5 to 100µA. The current source layout design needs good matching, the geometry and temperature influence has been analyzed and the optimal geometrical structure will be suggested.

1. Introduction

The replacement of sinusoidal signals in many practical cases can be solved using suitable approximations. The three level shortened square waves' technique allows to reduce the higher harmonics, especially the lower end of higher harmonics. This multilevel signal can be easily generated digitally and it enables simple digital processing involving only additions and shifting. An efficient CMOS technology based current source can be designed to work with such nontraditional waveforms. The current source consists of bias circuit, switchable current mirrors to select different current ranges and H-bridge current output stage. For impedance measuring the 8-channel switch mode synchronous detector will be used.

This paper proposes an advanced solution for the shortened square wave CMOS current source with H-bridge current output. The analysis of the proposed system is given and new practical solutions for applications in portable devices are described. The proposed solution improves the power consumption and reduces the complexity of the system as a whole. The main advantage of this method is greater efficiency because of the fact that for measuring cycle only one or two pairs of switchable current mirrors will be activated to drive the H-bridge.

2. CMOS Current Source

To utilize the shortened square waveform theory into practice, a low voltage and low power current exciter has to be designed. First the flexible current source with selectable output current in range from 5 to 100µA, and with supply voltage from 2.4 to 5V has been designed.

The design of the current source chip concludes with the 4x6 different current sources connected through switches to one H-bridge output stage. The current source as a black box is seen in Fig. 1. The current source needs two external bias signal pads to bias the inner circuitry current mirrors – Vbiasn and Vbiasp. For switching and combining the currents the 2x6 control inputs must be included (inputs c1 to c6 and their inversions) and two inputs to switch the H-bridge off (third) state. Table 1 shows the possible output current generating scheme for switching all of the six current sources to get the maximum 100µA output current.

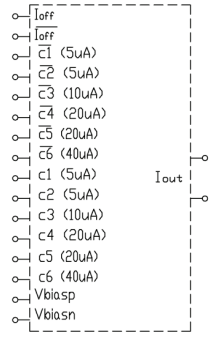

Fig.1. Current source block diagram

Table 1. Current sources

Control signals	Iout
c1	5 µA
c2	5 µA
c3	10 µA
c4	20 µA
c5	20 µA
c6	40 µA

The solution for current source is shown in Fig. 2. The Vbiasn and Vbiasp voltages are driving the current mirrors and afterwards the current is mirrored to 4x6 independent current sources. To achieve the simple current mirror ratio 1:1 the transistor matching error should stay ultimately bellow 2%. To fulfill the demand for so small error, the channel length of the transistor must be at least four times over the minimum strip dimensions (0.5µm technology in our case) and the channel area (LxW) must be larger than 25µm^2. Unfortunately the bigger is the mirrored current and

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primal current ratio; the bigger is the matching error. The current mirroring ratios over 1:8 are therefore not acceptable. The attempt was made to find the best solution for transistor channel length and width ratios so, that the matching error at 1:1 ratio stays under 2% and at 1:8 ratio does not exceed 5%.

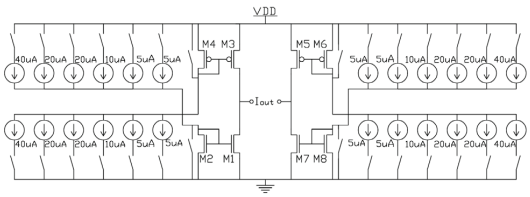

Fig.2. Current source schematic

The simulation results are shown in Fig. 3. The results are preliminary, because they show the working principle. The idea was not to create stepped sine wave; it was to show the possible combinations of current sources. The schematic simulation can calculate only the threshold voltage, drain-to-source voltage and lambda mismatch. To get the accurate and trusted result, the layout must be simulated.

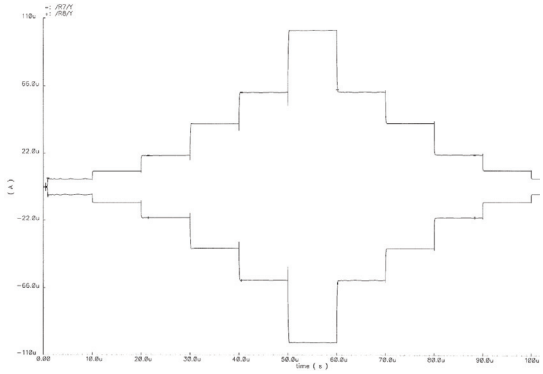

Fig.3. schematic simulation results

The test chip has been designed with the possibility to use external bias voltage. The nominal bias voltage value was chosen to be 1.2V. The low-power biasing circuitry solution is shown in Fig. 4.

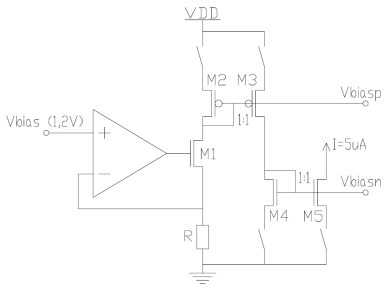

Fig.4. Biasing circuit

The voltage to current conversion is realized using low-power operational amplifier, transistor M1 and resistor R. The weak point of this solution is the resistor R with nominal value about 240kΩ. Unfortunately the used 0.5µm technology gives for all resistors the positive temperature coefficients. Additionally the lay-out geometry dimension of the resistor becomes too big. The attempt to scale down the resistor area about 20% leads us to the one long channel NMOS transistor with resistor R in series in case, when the transistor acts in linear regime. The resistor nominal value will be then 190kΩ.

Results of the simulation comparing one 240kΩ resistor with 190kΩ resistor in series with n-channel transistor are shown on Fig. 5. The resistor in series with n-channel transistor gives the excellent output current stability in wide enough temperature range (from 0 to 40˚C), but only then, when the input biasing stays at 1.2V.

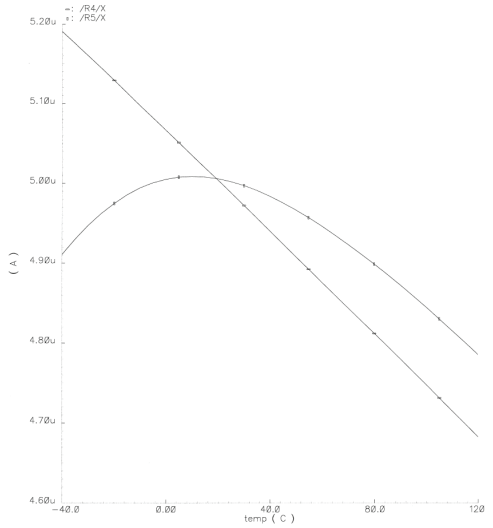

Fig.5. Bias circuit output current temperature dependence simulations

3. Layout design

For the layout design the CADENCE IC Design environment was used in combination of the NSC cmos7_5v technology line data package. Although the designed circuitry solution is relatively simple, the layout solution becomes rather complicated. The most critical part in layout design is the switchable current sources. By the layout realization the very good matching must be achieved; and if it will be not achieved, then the whole simple and flexible current source design will be a failure. Actually the circuitry simulations do not show the matching error very accurately, because we have to take into the account that the number of transistors in schematics and layout are different. For example 1:8 current mirrors with transistor switches in schematics is

solved with 4 transistors, but in layout at least 18 separated transistors must be used. All these separated transistors must be split at least to the same size of smallest transistor in the current mirror, or even 2 to 4 times smaller.

Fig. 6 shows the test chip layout in 0.5µm CMOS technology solution with the used area about 285x155µm. The bias circuit current mirror is the core of matched current sources. In fig. 6 one can see that the biasing circuit operational amplifier and voltage to current converting resistor are in the right, but the current mirrors (transistors M2 and M3 on the Fig. 4) are moved directly in the middle of switched current sources. In H-bridge also the transistors are split, to get well matched compact block.

Fig. 7 gives a magnified view from one part of switchable current sources to explain the transistors matching principle. From the bias circuit current mirror, on the left side, the current is mirrored to six different transistors (actually 20 on the lay-out), on the right. To get the 1:8 current ratio, the transistor is split to 8 transistors with same size as is the diode connected transistor in bias circuit. These 8 transistors are placed in three separately located groups. Between these groups are located current sources with 1:2, 1:4 and 1:4 current ratios.

The layout based improved simulation result was better then predicted (Fig. 8.). The only restriction is that the simulation doesn't take into account by the calculations the temperature differences around the chip area. But still the overall matching looks good and all current differences are below 1%. Looking the output current front rising and falling times we can estimate that the current source maximum operating frequency may reach up to 1MHz at all output currents.

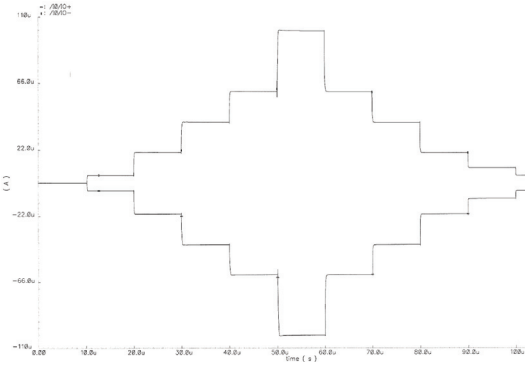

Fig.8. Layout simulation results

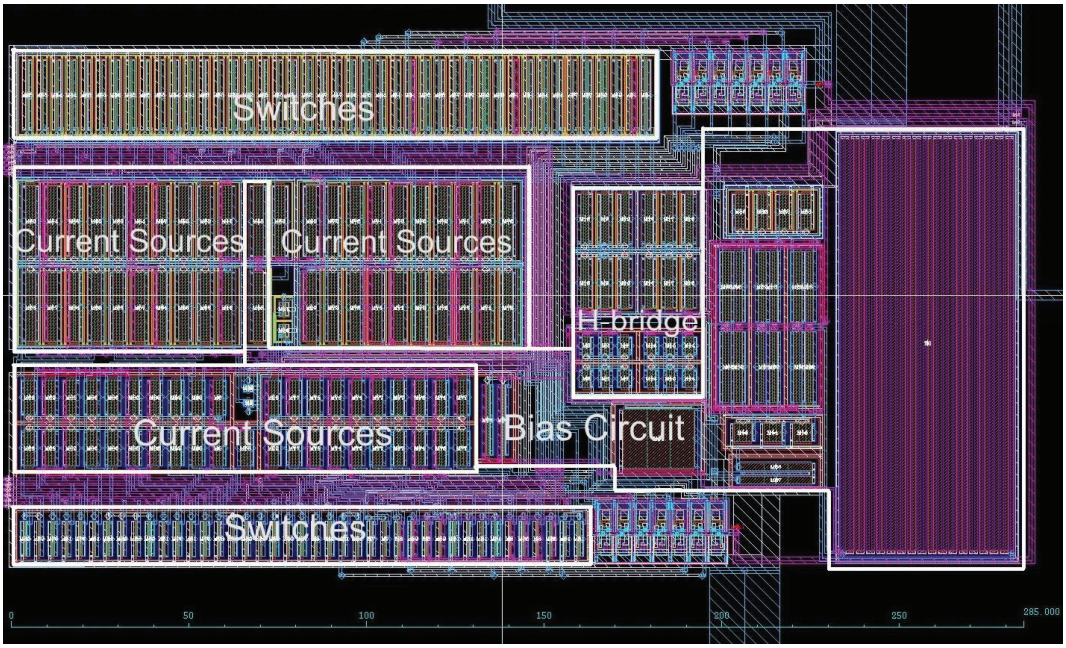

Fig.6. Test chip lay-out

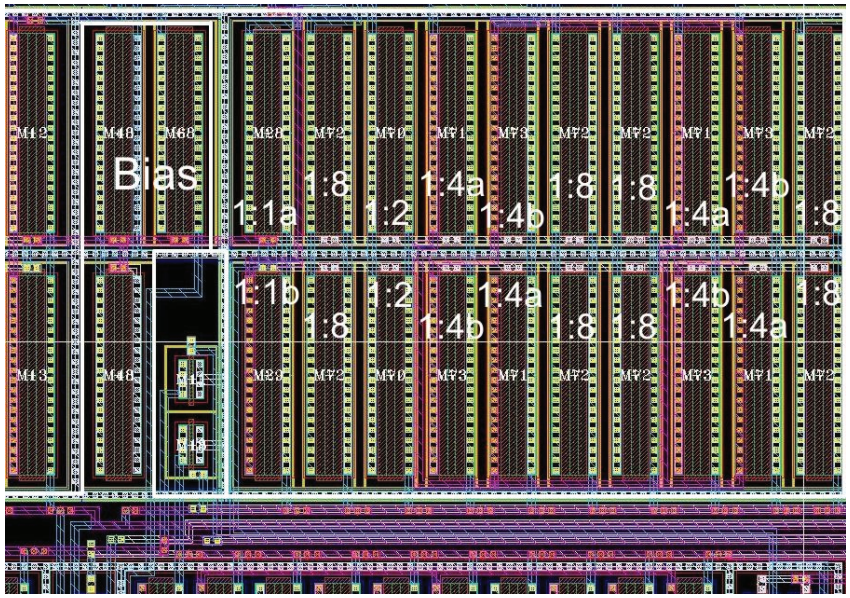

Fig.7. Current mirrors matching

4. Conclusions

The design of the CMOS technology based efficient low-power high speed current source has been made. The test chip layout has been developed using NSC 0.5µm technology. On base of experiments the following novel observations have been detected:

- Reduced system circuit complexity and therefore smaller chip lay-out area has been achieved.
- The efficiency of the circuitry has been improved, the measuring cycles are short and in stand-by regime only the bias circuit consumes power.

The test chip lay-out and simulation results look promising. The test chip has gone to fabrication and the experimental measurements can be made in near future.

5. Acknowledgement

The authors wish to thank the Estonian Ministry of Education and Research (the target oriented project SF0142737s06), the Estonian Science Foundation (the research grant G7183), and the Foundation Archimedes through the Centre of Excellence CEBE (TK05U01) for supporting the presented research work. Also we thank the NSC Estonia team for support and fabrication of the test chip.

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Publication IV

Kasemaa, Argo; Annus, Paul; Rang, Toomas (2011). CMOS low power current source with reduced circuit complexity. 9th IEEE International NEWCAS 2011 Conference. Bordeaux, France, June 26-29, 2011 (accepted for publication, ID 9101).

CMOS low power current source with reduced circuit complexity

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***Abstract*—The paper describes the efficient CMOS technology based current source for system identification and it's layout realization with reduced circuit complexity. Square wave excitation current is preferred in energy constrained and embedded environment. It has been shown that by shortening the square waves, spectral purity of the excitation signals can be drastically improved. Further improvement can be achieved by introducing limited number of additional equally spaced current levels. The basic idea of such a solution is that by suitably adding several simple shortened pulses together some of the high energy harmonics are either further reduced or eliminated. This multilevel signal can be easily generated digitally and it enables simpler digital processing involving only additions and shifting. On the other hand required extra circuitry for multiple current levels should not eliminate main advantages of square wave excitation, such as reduced complexity and low consumption. Proposed solution improves the power consumption and reduces the complexity of the system as a whole compared to more generic approach. The current source output will be the shortened multilevel square wave signal. The output current value can be selected from range from 5 to 100 µA. The main advantage of this method is greater efficiency because for measuring cycle only one or two pairs of switchable current mirrors will be activated to drive the H-bridge.**

I. INTRODUCTION

Measure by which system under investigation impedes alternating current (AC) flow can be used to characterize its properties. Measurement of low-level voltage response and its changes is usually conducted by using lock-in approach. Injecting known constant current and measuring the response voltage is generally preferred method. In case of biological matter it has added benefit of higher safety, due to strong limitation of the current level. Classically sinusoidal excitation is used and Fast Fourier Transformation (FFT) or similar takes care of spectral separation. It enables determination of magnitude and phase of the complex response signal compared to the excitation signal, and gives relatively good insight into network under investigation [1]. Measurement accuracy depends on the quality of the excitation signals, analog circuitry and on signal processing tools and algorithms. Situation changes dramatically in case of implantable devices, such as pacemakers. Energy and space constraints limit usage of analog components, and put sinusoidal signals and required signal processing solutions into unfavorable position. Both analog circuitry and traditional digital signal processing tend to consume a lot of energy, as well as require sizeable space on the die. Similar constraints apply in other areas as well. Monitoring the healing process in tissue transplants during the first hours and days is a key factor to successful reconstructive surgery. Visual inspection, the preferred method today, has serious flaws. Lack of qualified personnel can severely impair inspection efficiency, and together with uncertainty in interpretation of the observations could lead to late discovery of problems in transplanted muscle flaps. It may cause undesired or even fatal outcomes in place of the intended therapeutic effect of a treatment. Tissue impedance reflects well changes in tissue state such as the level of reperfusion and development of edema, which characterize the revivability or resuscitation of the tissue after transplantation. Energy constraints are of utmost importance since the device has to operate reliable over a longer period of time.

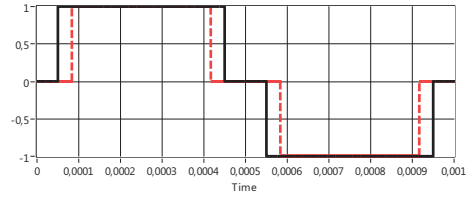

Figure. 1. Square wave signals shortened by 30° (dashed) and 18°.

Replacing sinusoidal signals with their simpler square wave counterparts enables drastic reduction in energy consumption and complexity, but carries a penalty of energy loss and measurement errors introduced by high harmonic content. Systematic errors introduced by higher harmonics of simple square wave signals can be drastically reduced by slightly modifying the waveform [2]. In case of shortening the excitation and reference signals by 30° and 18° respectively (Fig. 1), errors can be reduced by order of magnitude in comparison with regular rectangular waves. By weighted addition of three 18°, 30° and 42° shortened square waves spectral purity and measurement accuracy can be further improved [3] (Fig. 2).

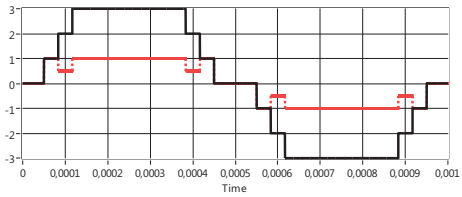

Figure. 2. Weighted sums of shortened square wave signals (18°, 30°, and42°), with coeficients 1, -0,5, 0,5 (dashed) and 1, 1, 1.

These multilevel signals can be easily generated digitally and enable simpler digital processing involving only additions and shifting. Unfortunately there are no off the self solutions for analog circuitry suitable for generation of described current signals. General digital to analog conversion techniques and solutions are both inefficient and consume relatively large die area. Therefore it is warranted to make a custom design for an efficient CMOS technology based current source, optimized to work with such nontraditional waveforms. The current source circuitry consists of switchable current mirrors to select different current ranges and H-bridge current output stage. On the chip the bias reference is used. This paper proposes an improved solution for the shortened square wave CMOS current source with H-bridge current output. The proposed solution improves the power consumption and reduces the complexity of the system as a whole. The main advantage of this method is greater efficiency because of the fact that during measurement cycle only limited number of pairs of switchable current mirrors will be activated to drive the H-bridge, and most of the consumed current is used to excite the system under investigation.

II. DESCRIPTION OF THE DESIGN PROBLEM

Differential current generator helps to solve problems posed by supply voltage and power constraints. Multiple, switched, constant current sources are chosen for multilevel shortened square wave generation. It is evident that inevitable timing uncertainties will influence spectral purity of the final shortened square wave current signal. Simulation has been performed in order to evaluate penalty paid because of timing errors. Also the switching transition time of current sources influence the signal spectrum. This type of influence is almost impossible to calculate and even predict, because it depends on switching speed and some other factors. At the preliminary current source design phase errors introduced by switching time differences will be ignored, and transition time's influence to the spectrum will be measured afterwards.

The MOS transistor output current range is unfortunately limited, because of relatively low power supply and because of the need to keep the transistor in a strong inversion mode. To describe circuit limitations a simplified H-bridge schematic will be used (Fig. 3.) By using *p*-channel MOS transistors, higher threshold voltage V_{THP}, and the lower acting speed for given manufacturing technology can be achieved.

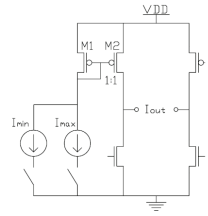

Figure. 3. The H-bridge schematics.

The MOS transistor drain current in saturation region is described by the well-known formula, [4]:

$$I_D = KP_p/2 \times W/L \times (V_{SG} - V_{THP})^2, \quad (1)$$

where KP_p is transconductance parameter for *p*-channel MOS transistor, W is channel width, and L is channel length. By using equation (1) and entering realistic values of 1 V and 1.9 V for the V_{SG} of the transistor M1, the current ratio I_{Dmax}/I_{Dmin} will be equal to 100. This is very important limitation for the described circuit, because the strong inversion mode for the transistor M1 can be realized only within the current values I_{min} and I_{max}, which cannot differ more than 100 times. At the same time transistor M2 must always stay in saturation region, in order to keep the resistivity of the transistor M2 high for it to act as a current source. No zero inversion charge can be observed along the channel, when the transistor M2 is in linear region. If $V_{SD} = V_{SG} - V_{THP}$, then the inversion charge under the gate at the point $y = L$ reaches the zero value, where y is the inversion layer charge distribution length along the channel. To keep the transistor M2 working in saturation region, y has to be kept smaller then L. The drain-source saturation voltage $V_{SD,sat} = V_{SG} - V_{THP}$, defines situation, when the channel charge becomes pinched-off at the drain-channel interface (on long-channel MOSFETs). V_{SD} voltage must be kept always bigger than the $V_{SD,sat}$ value to stay in saturation region ($V_{SD} \geq V_{SG} - V_{THP}$). $V_{SD,sat}$ value acts as a boundary value between triode and saturation region. It is safe to assume that the mobility of charge carriers does not vary with V_{SD}.

There are additional limitations for the H-bridge configuration (Fig. 3). The output resistance can be calculated as:

$$r_0 = (\lambda \times I_{DS,sat})^{-1}, \quad (2)$$

where the λ is channel length modulation, and $I_{DS,\,sat} = I_D$ when $V_{DS} = V_{DS,sat}$. The channel length modulation λ depends on the drain to source voltage, gate potential and channel length:

$$\lambda = L_{elec}^{-1} \times (dX_{dl}/dV_{DS}), \quad (3)$$

where L_{elec} is the electrical channel length (inversion layer charge distribution length in channel). The electrical channel length of the MOSFET is defined as a difference between the drawn (physical) channel length, neglecting lateral diffusion,

and the depletion layer width, X_{dl}, between the drain and the channel under gate oxide: $L_{elec} = L - X_{dl}$. The output resistance, as one of the most important parameters of the current source, could be increased by using cascaded current mirrors, but the unfortunate drawback is required higher supply voltage.

The speed of the MOS transistor is well described by the transition frequency f_T, which can be calculated as:

$$f_T \approx g_m / 2\pi C_{gs} = 3\mu_p / 4\pi \times V_{SD,sat} / L^2 . \qquad (4)$$

This equation is fundamentally important. To increase the speed strong decrease of the channel length is required, which leads to the larger $V_{SD,sat}$. On the other hand: the shorter the channel, the lower the current mirror transistors output resistance will be. This is a contradictory situation and demands careful compromise. Therefore channel of the transistor must be made as long as possible within speed posed constraints. High acting speed is needed, because switching current mirrors must be able to generate shortened square wave signals with fundamental frequencies up to 1 MHz, and so the transition times must be kept as short as possible. Suggested suitable compromise keeps the channel length at about 4 times over the minimum ($L = 4\lambda$) value. The design is made using National Semiconductor 0.5 µm CMOS technology.

III. Solution and Discussion

Final design of the current source chip includes 4x6 current sources connected through switches to one H-bridge output stage. The used NSC 0.5 µm CMOS technology has one additional limitation related to the current mirror matching. For 1 to 1 ratio current mirrors the transistor channel area (LxW) should not be less than 25µm^2. It means that the minimum size of the transistor should be L = 2 µm and W = 12.5 µm. To optimize the matching, the split L = 2 µm to W = 14 µm leads to layout solution where at least two transistors with channel dimensions L = 2 µm and W = 7 µm should be used.

Schematic of the current source is given in Fig. 4. Transistor matching error should stay ultimately below 2%, in order to achieve accurate mirroring ratio of 1:1. To fulfill the demand for so small error the channel length of the transistor must be at least four times over the minimum strip dimensions (0.5 µm technology in our case) and the channel area (LxW) must be larger than 25 µm^2. Unfortunately the bigger is the mirrored current and the primal current ratio; the bigger will eventually be the matching error. The current mirroring ratios over 1:8 are therefore not acceptable. Attempt was made to find the best optimum for transistor channel length and width ratios so that the matching error at 1:1 ratio stays under 2% and at 1:8 ratio does not exceed 5%. Calculations over final design show that the current error for all added currents does not exceed the 5% level.

The test chip has been designed with the possibility to use external bias voltage. The nominal bias voltage value was chosen to be 1.2 V. The low-power biasing circuitry solution is shown in Fig. 6.

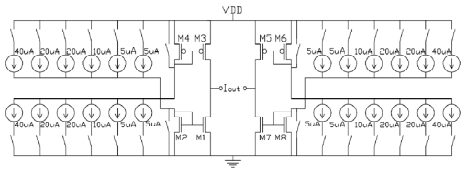

Figure. 4. Current source principial schematic.

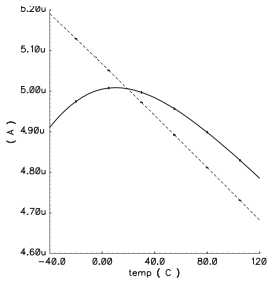

Figure. 5. Bias circuit output current temperature dependence simulations.

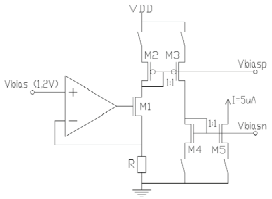

Figure. 6. Biasing circuit.

The voltage to current conversion is realized using low-power operational amplifier, transistor M1 and resistor R. The weak point of this solution is the resistor R with nominal value of about 240 kΩ. Unfortunately the used 0.5 µm technology gives positive temperature coefficients for all of the resistors. Additionally the lay-out size of the resistor becomes too big. However transistor acting in the linear regime can be used in the attempt to scale down the resistor area of about 20%, and it leads to one long channel n-MOS transistor with resistor R in series. The nominal value of the resistor will be 190 kΩ. Results of the simulation comparing one 240 kΩ resistor with 190 kΩ resistor in series with n-channel transistor are shown on Fig. 5. The resistor in series with n-channel transistor gives good output current stability in wide enough temperature range (from 0 to 40˚C), but only, when the input biasing stays at 1.2 V.

Simulation results for the developed circuit are shown in Fig. 7, where the 1 MHz 30° degree shortened square wave signals with the output levels of 5 µA and 40 uA are presented. The simulation shows that the actual switching speed could be even higher because the rising times are not limited by transistors of the switched current source, but by the bias circuitry itself. To increase the switching speed, the high speed operational amplifier must be implemented. This solution leads unfortunately to the increase of the supply current.

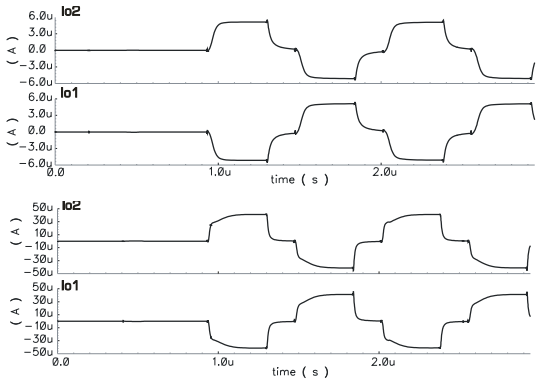

Figure. 7. Simulation results.

For the layout design the CADENCE design environment was used in combination of the NSC CMOS7_5v technology line data package. Although the designed circuitry is relatively simple, the layout becomes rather complicated. The most critical part in the layout design is the placement of the switchable current sources. Very good matching of the current sources must be achieved by the actual layout. Failure of doing so will result in failure of the whole current source design. Actually the circuit simulations do not show the matching error very accurately, because of the number of transistors in schematics and in layout are different. For example 1:8 current mirrors with transistor switches are schematically realized with 4 transistors, but in layout at least 18 separated transistors must be used. All these separated transistors must be split at least to the same size of smallest transistor in the current mirror, or even 2 to 4 times smaller.

Fig. 8 shows the test chip layout in 0.5 µm CMOS technology with the used area of about 285×155 µm^2. The bias circuit for the current mirror is the core of the matched current source. It can be seen on fig. 8 that the operational amplifier of the biasing circuit and voltage to current converting resistor are on the right side, and that the current mirrors (transistors M2 and M3 on the Fig. 6) are moved directly to the middle of switched current sources. The transistors in the H-bridge are also split, in order to get a well matched compact block.

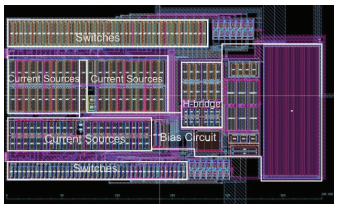

Figure. 8. Test chip lay-out.

Simulations based on this improved layout gave better results than predicted, but the circuit simulations don't take into account the temperature differences around the chip area and also all the fluctuations of parameters what are related to variation of process parameters, like gate oxide thickness, etc. The simulation results show overall excellent matching and all current differences are clearly below 1%.

The measurement result of the test chip is presented in Fig. 9. The current source load was chosen equal to 100 Ω with 1% metal film resistors. As predicted, the maximum useful working speed reaches the value 1 MHz and the matching error was in the range from 1.3 to 4.5%.

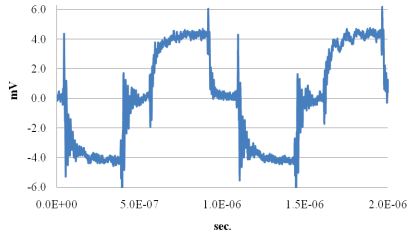

Figure. 9. 40 µA and 30° shortened square wave output signal at 1 MHz.

IV. Conclusions

The design of CMOS technology based efficient low-power high speed current source has been proposed. The test chip layout has been realized using NSC 0.5 µm technology. Following important results are achieved:

- Reduced circuit complexity and therefore smaller chip lay-out area;
- Greater efficiency, due to the fact that measuring cycles can be short and in stand by regime only the bias circuit consumes power;
- Original lay-out for matching of the current source transistors has been proposed and realized using available NSC technology.

Acknowledgement

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