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Bidirectional Isolated Current-Fed Soft-Switching Secondary-Modulated DC-DC Converters

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology, has not been submitted for any academic degree.

Roman Kosenko .....

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Contents

List of Publications

The present Ph.D. thesis is based on the following publications that are referred to in the text by Roman numbers.

[PAPER-I] Chub A., Kosenko R., Blinov A., Ivakhno V., Zamaruiev V., Styslo B., Full Soft-Switching Bidirectional Current-Fed DC-DC Converter, 2015 56th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON) (189–194). IEEE.

[PAPER-II] Blinov A., Kosenko R., Chub A., Vinnikov D., Bidirectional Soft Switching DC-DC converter for Battery Energy Storage Systems, 2018, IET Power Electronics.

[PAPER-III] Kosenko R., Husev O., Chub A., Full Soft-Switching High Step-Up Current-Fed DC-DC Converters with Reduced Conduction Losses. IEEE 5th International Confere`nce on Power Engineering, Energy and Electrical Drives (POWERENG), Riga, Latvia, 11-13 May, 2015. IEEE, 1–6.

[PAPER-IV] Ivakhno V., Zamaruiev V., Styslo, B.; Kosenko, R.; Blinov, A., Bidirectional Isolated ZVS DC-DC Converter with Auxiliary Active Switch for High-Power Energy Storage Applications. 2017 IEEE First Ukraine Conference on Electrical and Computer Engineering (UKRCON), May 29 – June 2, 2017..Kiev, Ukraine: IEEE, 589–592.

[PAPER-V] Kosenko R., Chub A., Blinov A., Full-soft-switching high step-up bidirectional isolated current-fed push-pull DC-DC converter for battery energy storage applications. Proceedings of the IECON2016 - 42nd Annual Conference of the Industrial Electronics Society, Florence (Italy), October 24-27, 2016: IECON 2016, Florence, Italy, 23-26 Oct. 2016. IEEE, 1–6.

[PAPER-VI] Kosenko R., Blinov A., Vinnikov D., Korkh O., Dual Inductor Current Fed Push-Pull DC-DC Converter with High Conversion Ratio, Scientific Journal of Riga Technical University Electrical, Control and Communication Engineering, 2018 (upcoming).

[PAPER-VII] Kosenko R., Blinov A., Korkh O., Experimental Verification of Two-Stage Power Converter With Current-Fed Soft-Switching Front-End for Battery Storage Applications, EPE'18 ECCE Europe, 2018.

[PAPER-VIII] Kosenko R., Blinov A., ChubA., Vinnikov D., Asymmetric Snubberless Current-Fed Full-Bridge Isolated DC-DC Converters, Electrical, Control and Communication Engineering, 2018.

[PAPER-IX] Blinov A., Kosenko R., Chub A., Vinnikov D., Bidirectional Soft Switching Current Source DC-DC Converter for Residential DC Microgrids, IECON 2018.

[PAPER-X] Blinov A., Kosenko R., Chub A., Vinnikov D., Snubberless Boost Full-Bridge Converters: Analysis of Soft Switching Performance and Limitations, International Journal of Circuit Theory and Applications, 2018.

[PAPER-XI] Kosenko R., Vinnikov D., Soft-Switching Current-FED Flyback Converter with Natural Clamping for Low Voltage Battery Energy Storage Applications. Technological Innovation for Smart Systems, 1: Doctoral Conference on Computing, Electrical and Industrial Systems; 03-05 May 2017. Lisbon, Portugal.

Author's Contribution to the Publications

The present PhD thesis is based on the following publications that are referred to in the text by Roman numbers.

[PAPER-I] Roman Kosenko co-authored the paper, synthesized the converter control algorithm and developed the simulation model in PSIM software.

[PAPER-II] Roman Kosenko co-authored the paper, developed a prototype converter and a control system for it; he was responsible for experimental study and co-authored writing.

[PAPER-III] Roman Kosenko is the main author of the paper, responsible for literature review, synthesized the converter topology and was responsible for the simulation study of the converter in PSIM software. He presented the paper at 2015 IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG).

[PAPER-IV] Roman Kosenko co-authored the paper, proposed the converter topology. He presented the paper at 2017 IEEE First Ukraine Conference on Electrical and Computer Engineering (UKRCON).

[PAPER-V] Roman Kosenko is the main author of the paper, synthesized the converter topology and modulation sequence, was responsible for the literature review, the prototype development and took part in the experimental study. He presented the paper at the 42nd Annual Conference of the Industrial Electronics Society (IECON2016).

[PAPER-VI] Roman Kosenko is the main author of the paper, synthesized the converter topology and modulation sequence; he was responsible for the literature review, submission and communication with editors, development of the experimental prototype and its experimental validation.

[PAPER-VII] Roman Kosenko is the main author of the paper, proposed the power converter concept; he was responsible for the development of the experimental prototype and the closed-loop control system for it, conducted the experimental study.

[PAPER-VIII] Roman Kosenko is the main author of the paper, was responsible for the literature review, submission and communication with editors, development of the experimental prototypes, control systems for them and their experimental validation.

[PAPER-IX] Roman Kosenko co-authored the paper, developed the prototype converter, and the control system for it, was responsible for the experimental study and co-authored writing.

[PAPER-X] Roman Kosenko co-authored the paper, took part in the development of the topologies assessment tool and simulation study in PSIM.

[PAPER-XI] Roman Kosenko is the main author of the paper, synthesized the converter topology and modulation sequence, was responsible for literature review, the prototype development and experimental study. He presented the paper at Technological Innovation for Smart Systems, 1: Doctoral Conference on Computing, Electrical and Industrial Systems (DoCEIS 2017).

List of Abbreviations

AC	Alternating Current
A-SMC	Asymmetrical Full-Bridge Secondary Modulated Converter
AUX-SMC	Full-Bridge Secondary Modulated Converter with Auxiliary Switch
BESS	Battery Energy Storage System
CF	Current-Fed
CFC	Current-Fed converter
CFVFC	Current-Fed Voltage-Fed converter
DC	Direct Current
DiPP-SMC	Dual Inductor Secondary Modulated Converter
EMI	Electromagnetic Interference
FB-SMC	Full-Bridge Secondary Modulated Converter
FBK-SMC	Flyback Secondary Modulated Converter
GI	Galvanic Isolation
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IS	Impedance-Source
ISC	Impedance-Source Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PCU	Power Conditioning Unit
PSM	Phase-Shift Modulation
PS-SMC	Phase Shifted Secondary Modulated Converter
PW-SMC	Pulse Width Secondary Modulated Converter
PWM	Pulse-Width Modulation
RES	Renewable Energy Source
RMS	Root Mean Square
SMC	Secondary Modulated Converter
SR	Series Resonant
SRC	Series Resonant Converter
ST	Shoot-Through
SiPP-SMC	Single Inductor Secondary Modulated Converter
TUT	Tallinn University of Technology
VDR	Voltage Doubler Rectifier
VF	Voltage-Fed
VFC	Voltage-Fed converter
WBG	Wide Bandgap
ZEB	Zero Energy Building
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Symbols

C_1, C_2	filter capacitor of the VDR
D_{REV}	duty-cycle of reverse energy transfer interval
D_{VF}	VF transistors duty-cycle
D_{CF}	CF transistors duty-cycle
I_g	grid current
I_{CF}	CF port current
I_{VF}	VF port current
$I_{TX,pr}$	primary winding current of the isolation transformer
$I_{TX,pr(av)}$	average current per half cycle of the resonant tank
$I_{TX,pr(m)}$	amplitude value of the current through the resonant tank
$I_{TX,sec}$	secondary winding current of the isolation transformer
L_{CF}	CF port inductor
L_{lk}	leakage inductance of the isolation transformer
n	transformer turns ratio of the isolation transformer
n_1	turns ration of the qZS coupled inductor
n_2	turns ratio of the isolation transformer
P	operating power
P_{CF}	CF port power
P_{VF}	VF port power
Q_{OSS}	output charge of a switch
$R_{DS(on)}$	drain-source on-state resistance
T_{SW}	switching period
T_x	isolation transformer
V_{DC}	DC-link voltage
V_G	gate voltage
V_{CF}	CF port voltage
V_{VF}	VF port voltage
V_{GS}	gate-source voltage
φ	phase shift angle

1 Introduction

1.1 Background

Current-fed (CF) converters are well-known and can be applied to all types of power electronic converters: DC-DC, AC-AC, AC-DC, DC-AC. Nevertheless, CF converters are not as widespread in the industry as their voltage-fed (VF) counterparts and are typically used in a few limited fields [1], [2].

Fig. 1.1 shows the generalized structure of the VF (a) and CF (b) galvanically isolated (GI) power converters. The VF converter uses a capacitor to stabilize the input voltage, while a typical CF converter uses an inductor to stabilize the input current. The CF converter (Fig. 1. b) generally consists of an input boost inductor, an inductor voltage overshoot clamping circuit, an input side inverter, an isolating transformer, an output side rectifier, and an averaging output filter.

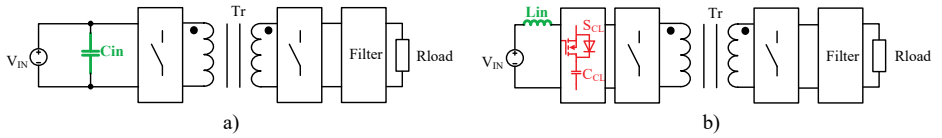

Fig. 1.1 Generalized block diagrams of the VF (a) and the (CF) GI converter.

Limited use of GI CF converters can be explained by several drawbacks that the VF converters lack, such as the requirement of additional circuits for the inductive voltage overshoots clamping. This voltage overshoot on the L_{in} at the turn-off of switches is caused by mismatch between the currents of an input inductor and a leakage inductance of an isolation transformer. The clamping circuit does not take part in the energy transmission process or converter step-up factor regulation; it is only used to provide voltage clamping and in some cases, soft-switching of the input side inverter switches. Another drawback of the CF converters is that they can have high inrush current during startup. This current is formed if the output filter capacitor is initially discharged and according to commutation laws, acts as short circuit. If not treated accordingly, the current amplitude can become significantly higher than the nominal value and can lead to the failure of semiconductor components.

Finally, the energy density of magnetic elements in CF converters is much lower as opposed to capacitors used as a filtering and storage element in VF topologies [3].

On the other hand, common advantages of the CF topologies are:

- CF converters are immune to the transformer saturation. Unlike in VF converters, the shoot-through state is allowed, while zero state is prohibited. This makes CF converters immune to the transformer saturation as the magnetizing current is reset during the shoot-through states [2].
- In applications like deep sea mining, long-distance energy transfer and other uses that have long supply wires, their parasitic inductance can be utilized instead or in addition to the dedicated magnetic element [1], [4].
- Lower RMS current stress of switches and easily achievable high partial load efficiency [5], [6].

- They require lower transformer kVA rating and turns ratio (in step-up applications). To get the same regulation range with a single stage converter, the isolating transformer turns ratio for the VF and CF will be different. CF converters are inherently boost-type converters. Therefore, the turns ratio can be reduced, allowing a more optimal design of the transformer as compared to the VF converter [7] and wider voltage regulation capabilities [8].
- Low input current ripple. Inherently CF topologies have an energy accumulating inductor at the input side, which results in smaller input current ripple as compared to the VF counterparts. This is important for interfacing with renewable energy sources, batteries and fuel cells to increase their lifetime and ensure operation at maximum power point [2],[8].

In recent years, numerous studies have focused on the development of the soft-switching CF GI converter topologies and led to the development of various clamping techniques using auxiliary networks or circuits as well as clampless solutions. At the same time, only a limited number of current-fed topologies with bidirectional functionality preserve soft-switching operation and the same high level of efficiency in both energy transfer directions. One type of converters that looks promising in this regard is the galvanically isolated current fed DC-DC secondary modulated converter (SMC) with reverse blocking switches. These types of power converters require an active rectifier and four-quadrant switches to achieve soft-switching operation. Comprehensive research of such SMC converters for low voltage industrial and consumer applications has been neglected, especially regarding the topologies other than full-bridge (FB). Novel current-fed DC-DC topologies with reduced switches count that employ bidirectional capability and soft-switching operation can show the benefits of SMC converters and increase the commercial acceptance of the CF converters as a group.

1.2 Motivation of the Thesis

This research was conducted according to the priority research program established in the Power Electronics Group of Tallinn University of Technology. These activities initiated in 2014 are aimed towards the synthesis of novel power electronics converter topologies and their enhanced control methods and further experimental verification for Electronic Power Distribution Networks (EPDNs). The research is conducted with a strong emphasis on industrial applications and market needs to achieve fast industrial approval of the technologies introduced and to increase their commercial potential. The direct support of this research was obtained in the form of the targeted financing research project SF0140016s11 of the Estonian Ministry of Education and Research. Additional financial sources were also used: grants PUT744 and PUT1680 from the Estonian Research Council. Research on power electronics converters for battery energy storage and prototype development was supported by the Prototron innovation development fund.

1.3 Aims, Hypothesis and Research Tasks

The technology of the CF converters is not as widely spread as VF in the industry despite their simultaneous development and much potential in various areas. The advantages and benefits of the PS-SMC class of CF converters are to be analyzed and studied.

The main aim of this Ph.D research is to synthesize and experimentally validate new topologies of GI CF converters with a reduced number of switches and soft-switching functionality in a wide operation range that will show the same level of performance as already existing full-bridge topologies. Moreover, the author aims to show the advantages of the presented novel PS-SMC topologies over existing solutions in bidirectional and renewable energy applications. The outcomes of this work are expected to develop the theory further and increase industrial awareness of the snubberless GI CF DC-DC converters.

Hypotheses:

- Existing modulation methods for galvanically isolated phase-shift secondary modulated current-fed converters (PS-SMC) could be enhanced to provide soft-switching operation and comparable performance in both energy transfer directions.
- A number of four-quadrant switches in full-bridge PS-SMC could be reduced while preserving soft-switching performance in both energy transfer directions.
- Energy transfer principle of the full-bridge PS-SMC applies to the topologies with a reduced number of switches such as push-pull and flyback.
- PS-SMC topologies with a reduced number of switches can achieve the level of performance and soft-switching capability comparable to the full-bridge PS-SMC.

Research Tasks:

- Synthesis of hierarchically structured classification of soft switching current-fed DC-DC converter topologies based on modulation techniques as a classification feature.
- Synthesis, analysis, and verification of the full-bridge PS-SMC topologies with reduced four-quadrant switches count.
- Analysis of the implementation possibilities of the PS-SMC topologies with reduced switches count.
- Analysis of application possibilities of the proposed PS-SMC.
- Development of the benchmarking methodology for the comparison of soft-switching DC-DC converters.

1.4 Research Methods and Instruments

The steady state mathematical analysis proposed in this thesis is based on the steady-state models derived using the volt-second balance in inductors and the charge balance in capacitors (Equations 1.1 and 1.2) [9],[10].

$$v_{L(av)} = \frac{1}{T_{sw}} \cdot \int_{0}^{T_{sw}} v_L(t) \cdot dt = 0 \quad , \tag{1.2}$$

where $v_{L(av)}$ is the average inductor voltage, T_{sw} is the switching period, and v_L is the instantaneous value of the inductor voltage.

$$i_{C(av)} = \frac{1}{T_{sw}} \cdot \int_{0}^{T_{sw}} i_C(t) \cdot dt = 0 \quad , \tag{1.3}$$

where $i_{C(av)}$ is the average capacitor current and i_C is the instantaneous value of the capacitor current.

Results of the steady state analysis were verified with the PSIM simulation software. For the estimation of the power losses, the Thermal module add-on along with physical models of the semiconductor devices was used.

In addition to the simulation study, experimental verification of all proposed topologies was performed with the different laboratory prototypes at the rated power from 100 W to 500 W. During tests, the prototypes were supplied by Elektro-Automatik EA-PSI 9080-60 and TDK-Lambda Genesys series (Gen 100, Gen 300 and Gen 600) DC power supplies and Keysight E4360A solar simulator. Converter output was loaded by the programmable DC electronic load Chroma 63204 or passive active-inductive load.

The experimental waveforms were acquired with the digital oscilloscope Tektronix MSO4034B equipped with Rogowski coil current probe PEM CWTUM/015/R, current probe Tektronix TCP0030A, and high-voltage differential voltage probes Tektronix P5205A. The efficiency of the converter was measured while it was supplied from a DC power supply in boost mode and TDK-Lambda GEN600-5.5 in buck mode. Efficiency measurements were carried out with a YOKOGAWA WT1800 high-precision power analyzer.

1.5 Contribution and Dissemination

This thesis addresses comprehensive research on the enhancement of the GI CF PS-SMCs with special emphasis on the synthesis of topologies with a reduced number of switches and auxiliary circuits. The autor has proposed five novel PS-SMC topologies that are focused on different applications. From the practical point of view, the competitiveness of the novel PS-SMCs was proven by the three industrial prototypes of the standalone battery energy storage systems based on three different topologies. Knowledge and results, both theoretical and experimental, obtained by the author's research effort have increased industrial awareness on soft-switching GI CF power converters.

This work contributes substantially to the further development of the soft-switching current-fed converters, particularly PS-SMCs. The research performed by the author in the field of CF converters was disseminated at 10 international conferences and 8 doctoral schools in the form of oral and poster presentations. A total number of papers published by the author in this field during the Ph.D. study is 18. Among them, 14 were published in conference proceedings, and 4 papers appeared in peer-reviewed journals. The author has been granted two Estonian utility models.

Findings described in this Ph.D. thesis are based on 11 papers attached and listed in the List of Author's Publications. Among them, 7 papers were reported at seven international conferences and workshops of IEEE. The other four papers have appeared in international peer-reviewed journals.

Utility models received:

- Utility model: Method for control of the current-fed bidirectional DC-DC converter; Owners: Tallinn University of Technology; Authors: Andrii Blinov, Andrii Chub, Roman Kosenko; Priority number: U201500037; Priority date: 11.05.2015.
- Utility model: Current-fed bidirectional DC-DC converter; Owners: Tallinn University of Technology; Authors: Andrii Blinov, Andrii Chub, Roman Kosenko; Priority number: U201500038; Priority date: 11.05.2015.

Scientific Novelties:

- State-of-the-art soft-switching current-fed DC-DC converters were systematized and classified based on clamping methods.
- Comprehensive mathematical model of the full-bridge PS-SMC that allows calculation of converter soft-switching operation boundaries was first developed.
- Five novel PS-SMC topologies including those with reduced four-quadrant switches count were synthesized and analyzed.
- Advantages of PS-SMC topologies in bidirectional applications are shown.
- Universal topology assessment tool for the selection of the most suitable topologies among those proposed for LiFePO4 battery interface converter was developed.

Practical Novelties:

- Five PS-SMC topologies were assessed and experimentally verified: two full-bridge PS-SMC topologies with reduced switches count, and three PS-SMC topologies.
- Five proposed PS-SMC topologies were built and experimentally validated.
- Three industrial prototypes of standalone battery energy storage systems based on the FB, DiPP and Asymmetrical PS-SMC topologies were assembled and experimentally verified.

- The application field of current-fed converters was extended to residential energy storage applications where PS-SMC is beneficial against voltage-fed converters.
- Performance assessment of PS-SMC topologies with the next generation wide bandgap semiconductor devices was performed.

1.6 Thesis Outline

Chapter 2 presents the state-of-the-art review of existing current-fed topologies and general classification of inductor voltage clamping methods.

Chapter 3 addresses five new soft-switching current fed topologies. Operation principle, benefits and drawbacks of each topology are described and analyzed.

Chapter 4 introduces the performance assessment tool that was developed. It allows direct comparison of power converter topologies regarding components loading conditions. The topologies proposed in Chapter 3 are compared using the assessment tool.

Chapter 5 presents an experimental validation of three topologies, including the reference topology, selected based on the theoretical comparison in the previous chapter. Converters prototypes were designed as and built as a front-end converter for the interface of the $LiFePO_4$ battery to the 400V DC-link as a part of AC battery storage system.

Chapter 6 provides generalizations, conclusions and description of future work and research directions.

2 Overview of CSC Clamping Methods

2.1 Types of Power Converter Topologies

There are three types of power converter topologies: voltage-fed (VF), current-fed (CF), and impedance source (ISC). ISCs are a new emerging technology that is not yet adopted by the industry, while VF and CF are already established.

Many of energy sources, like fuel cells and batteries, have low-voltage dc output and thus require a galvanically isolated dc-dc converter to interface them to the high-voltage utility grids and feed typical loads [12]. Voltage-fed (VF) dc-dc converters were a conventional approach in power electronics for decades. However, recently galvanically isolated current-fed (CF) dc-dc converters have proven to be a superior solution over VF counterparts for low-voltage high-current sources [2], [12]. Another recent trend is towards utilization of soft-switching techniques in dc-dc converters to achieve high power density and low cost [11]. Hence, soft-switching (SS) CF dc-dc converters are an important research topic.

Converters with transformers are often preferred due to reduced stresses on the components and better flexibility of application [13], [14]. Galvanically isolated dc-dc converters with a current-fed (CF) port became a strong competitor for the conventional voltage-fed (VF) converters in application areas with low input voltage and relatively high current, like photovoltaic energy generation, fuel cell or BESSs [15], [16]. Due to continuous input current of CF converters, more efficient operation of such systems could be achieved [17], [19].

Block diagram of a typical GI CF converter (Fig. 2.1) consist of an input boost inductor, inductor voltage overshoot clamping circuit, an input side inverter, an isolating transformer, an output side rectifier, and an averaging output filter.

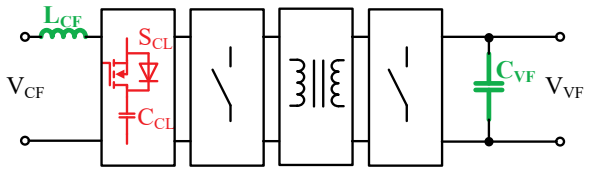

Fig. 2.1. Block diagram of a bidirectional CF GI converter.

The most obvious drawback of the CF dc-dc converters is the voltage overshoot on the L_{CF} at the turn-off of switches caused by mismatch between currents of an input inductor and a leakage inductance of an isolation transformer. For this reason, they require the clamping circuit. Clamping circuit does not take part in the energy transmission process or the converter step-up factor regulation but is only used to provide voltage clamping and in some cases soft-switching of the input side inverter switches. There are numerous different types of the clamping circuits, each with its unique set of features as well as clampless topologies. In the clampless topologies, the input side inverter with a specific control algorithm can deal with inductor voltage overshoots without any additional circuits.

2.2 State-of-the-Art Clamping Methods for CFC

Generalized classification of the clamping methods for GI CF converters is shown in Fig. 2.2.

2.2.1 Snubber assisted clamping methods

Passive snubber clamping

Historically, first attempts to suppress inductor voltage overshoots were made with passive snubbers - auxiliary circuits that included diodes and capacitors. Additional examples of a converter with passive snubbers are shown in [16],[20],[21]. An example of the bidirectional converter with a passive snubber is shown in [PAPER-III]. Drawbacks of converters with a passive snubber are limited operation range and additional losses on snubber elements.

Active snubber clamping

Active snubbers are a next step in the development of clamping circuits that adds active switches instead of diodes to the passive snubber circuits. Active snubbers solve the problem of voltage overshoot in a wide operation range and they are also used to create zero voltage switching (ZVS) conditions for main transistor switches.

For FB converters, active clamp circuit (ACC) was introduced in [22]. Active clamping circuit for a bidirectional FB converter was introduced in [23]. By utilizing active clamp and phase shift control, the converter reaches high peak efficiency in both directions of the power flow.

The drawback of ACC is that it raises the peak current through the CF-side switches and the transformer higher than the input current, which together with circulating capacitor energy results in increased conduction losses [22], [24]. Various methods have been used to address this issue at the cost of increased component count, for example, by incorporating a more complex snubber [25], or by using an auxiliary converter as an active clamping circuit [26]-[29].

2.2.2 Snubberless clamping methods

Some of the existing topologies can be attributed to clampless topologies [30]-[32]. Those feature clamping and soft switching of semiconductor devices without a separate dedicated circuit. This can be achieved by forcing the current redistribution between the CS transistors and it is typically attained in two different ways: by utilizing resonant circuit or by using an active rectifier at the voltage source (VF) side.

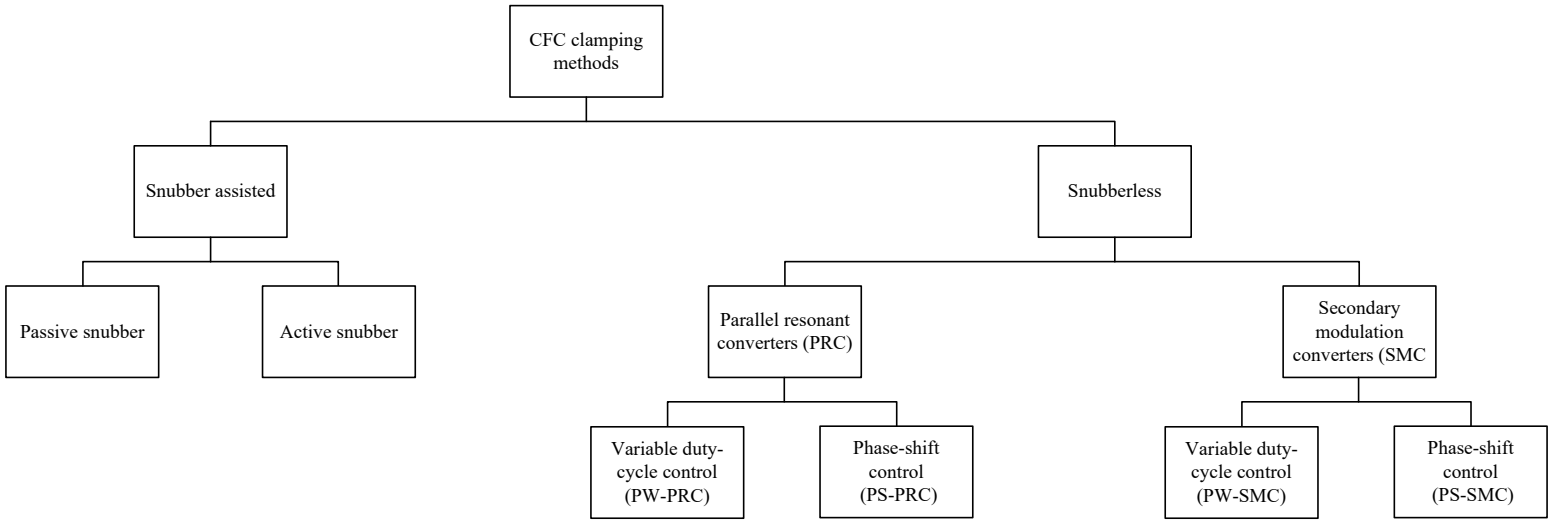

Fig. 2.2. Clamping methods of CF GI converters.

Resonant clamping converters

The first approach takes advantage of equivalent parasitic inductance of the circuit in the form of the transformer leakage inductance that is used to form a resonant circuit together with a relatively small, typically external, capacitor. As a result, the topology changes to either a series or a parallel resonant current source converter (PRC). The latter topology is usually preferred due to wider regulation possibilities [33], [34]. PRCs can feature either variable frequency pulse width- or phase-shift-modulation.

Variable-frequency control resonant converters (F-PRC)

In this group, transistor modulation sequence is based on the constant duty-cycle of the CF and VF switches. Topologies in this group achieve clamping with either passive or synchronous active rectification on the VF side.

One of examples is a resonant converter with symmetrical PWM control; symmetric parallel resonant CFC (S-PRC) is shown in [33]. This converter features constant on-time control of the CF stage, passive VF rectifier and regulation is achieved using frequency variation. A drawback of this topology is that energy circulation is drastically increased at low power and a significant switching frequency variation range occurs with load change.

Variable duty-cycle control resonant converters (PW-PRC)

Another possibility to achieve SS and voltage clamping without additional circuits is to use impulse commutation that employs local resonance during switching transients [30]. This approach utilizes parasitic elements for resonance commutation, but it is associated with high peak current stress of the input side switches.

The clamping method that uses secondary side active switches and is based on the resonance effect between the leakage inductance and the drain-to-source capacitance of the primary side MOSFET is presented in [35]. The method was successfully applied to different bidirectional converters [36], [37]. The main difficulties are associated with component parameter mismatch, nonlinearity of practical components, significant oscillations and the need for frequency variation to achieve robust clamping and soft-switching in the wire regulation range.

Phase-shift control resonant converters (PS-PRC)

Converters with such control have constant duty-cycle of CF and VF switches with constant switching frequency. Regulation is achieved by variation of the phase-shift angle between CF switches diagonals or by the variation of the phase-shift between CF and VF sides. An example topology is the phase-shift parallel-resonant CFC (PS-PRC) topology [38]. A main drawback of this converter is that the voltage gain depends heavily on the power level, growing more than 1.5 times as the power drops to 10% of the nominal voltage that was analyzed and shown in [PAPER-X].

Secondary Modulated Converters

This approach involves implementation of an active rectifier to form a secondary-modulated converter (SMC). SMCs use an active rectifier to force the primary currents of the input side switches to change direction and achieve clamping and soft switching for semiconductors. The idea to use HV switches to achieve clamping of the CF side was first proposed in [39]. Typical SMC converters have one CF and one VF port; thus, in some papers, bidirectional SMCs are addressed as current-voltage-fed (CVF) converters. Due to the inherited boost capability of the CF side, SMC converters are typically used with CF port on the low-voltage side and VF port on the high-voltage side. Accordingly, bidirectional converter operation with energy transfer from CF to VF port will be referred to further as a boost operation mode and vice versa, energy transfer from the VF to CF port will be called buck mode.

The advantage of SMCs lies in constant frequency modulation for both symmetric and phase-shift versions and higher degree of freedom when choosing VF side lossless snubber capacitors.

Variable duty-cycle control (PW-SMC)

PW-SMC converters achieve output power/voltage regulation by altering the duty-cycle of the transistor control signals while maintaining the constant phase-shift between the control signals. This enables manipulation of the leakage inductance current to achieve zero-current switching (ZCS) conditions at the input side and zero-voltage switching (ZVS) conditions at the output side with snubber capacitors. In addition, PW-SMC features inherent bidirectional operation capability.

The PW-SMCs control method for the half-bridge CF converter was introduced in [40], and was later applied to a family of bidirectional converters [32],[41],[45]. The method is based on active clamping by VF side active switches and allows achieving ZVS of all switches without additional clamping circuits. The proposed algorithm was first applied to a converter with half-bridge at the VF side in [48]. To control the topology effectively, leakage inductance of the transformer should be precisely dimensioned (possibly by an external inductor). The main advantage of PW-SMC is that it offers a low number of switches. The main drawback of existing PW-SMC topologies is that it has increased energy circulation and CF switches exhibit relatively high peak currents, especially during light load operation [34].

Phase-shift control (PS-SMC)

The converter consists of the CF full-bridge inverter at the low-voltage input side, the VF half-bridge inverter with snubber capacitors at the high-voltage output side, which operates as an active voltage double rectifier (VDR) in boost mode.

PS-SMC regulates output power/voltage by changing the phase-shift between the CF inverter diagonals or diagonals and the VF rectifier or both, while the duty cycles of the switches are kept constant.

In this group, all transients in all semiconductor components are soft-switching (SS), which is achieved along with natural clamping at the CF side. Another advantage of the PS-SMC is minimal energy circulation from the output side to the input side, which is a usual drawback of many SS techniques. It requires utilization of diodes in series with the switches at the CF side to achieve bidirectional voltage blocking feature of the switch.

Utilization of diodes in series with switches results in unidirectional power flow in the converter. A converter with four-quadrant switches at the CF side proposed in [47] can utilize the synchronous phase-shifted modulation to achieve bidirectional power transfer with FSS in the both directions. There are no commercial fully controllable bidirectional switching (four-quadrant switching) devices and only a few commercial models of the reverse blocking IGBT devices have a structure of series connection of IGBT and diode. At this level of technology, for a competitive high-efficiency converter, reverse blocking switches must be realized as a counter-series connection of the two discrete transistors.

Therefore, the main drawback of the PS-SMC is the increased number of semiconductors at the CF port and high conduction losses.

2.3 Summary of Chapter 2

This chapter reviewed existing clamping methods for GI CF converters. The main conclusions are as follows:

- Snubber assisted clamping methods cannot ensure inductive voltage overshoot clamping in a wide operation range. Additionally, clamping circuit increases circulation energy and power losses.
- Resonant clamping methods allow clamping without additional power circuits but suffer from limited regulation range. Regulation range and efficiency heavily depend on the resonant circuit design. It is possible either to get high efficiency in a narrow operation range or good efficiency in a wider range.
- PW-SMC has a minimal number of components and allows clamping and soft-switching without auxiliary circuits. A drawback is that the peak current through the CF side switches remains the same at all power levels, which leads to significant efficiency drop at low power.
- PS-SMC allows both clamping and soft-switching of CF and VF transistors in a wide operation range with a relatively simple control strategy (only-phase shift value is regulated). But PS-SMC has higher number of switches in the CF side. So far, this group was represented mainly by FB topologies and with the requirement of four-quadrant switches, which has led to a high number of transistors and increased conduction losses in the CF side.

3 Novel Galvanically Isolated Bidirectional Soft-Switching Current-Fed DC-DC Converters

The full-bridge topology (FB-SMC) introduced in [PAPER-I] was chosen as the baseline topology for the evaluation of novel phase-shift modulated converters as they are based on the same soft-switching principle. A mathematical model and modulation sequence deadtime calculations are presented in [PAPER-II]. FB PS-SMB topology that has four four-quadrant (4Q) switches is shown in Fig. 3.1. Waveforms for energy transfer direction from the CF to VF port are shown in Fig. 3.2. A detailed description of switching intervals and modulation sequence for the reverse energy transfer is shown in [PAPER-II].

Depending on the application, instead of bidirectional 4Q switches (Fig. 3.3. (b-d)), reverse blocking two-quadrant (2Q) switches (Fig. 3.3. (e-g)) can be used to decrease the number of controlled semiconductors. 4Q switch realization with two MOSFETs in a common source configuration (Fig. 3.3. b) is preferable as it has the lowest conduction losses, particularly in low voltage applications. In high voltage low current systems, where the bidirectional functionality is not needed as the reverse blocking, IGBT switches (Fig. 3.3.) can be applied, since they feature improved on-state characteristics as compared to similarly rated IGBT and series diode configurations. The idea of soft-switching is that due to the phase-shift between the CF and VF port they are forcing ZCS and ZVS commutation in each other [PAPER-II].

Soft-switching range is limited by the recharge rate of the VF transistors by the CF-side current at the minimum input current (low input power at high input voltage) during switching interval f) from low-power side of operation region and by the CF transistors current drop rate at maximal input current (high input power at low input voltage) during switching intervals c) and e) from the high-power side of the operation region.

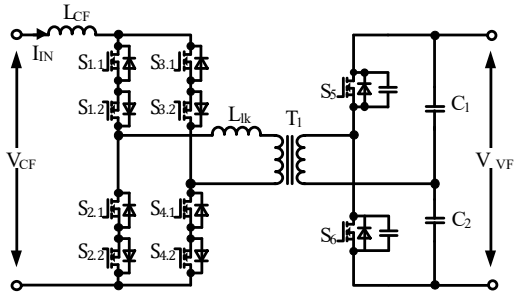

Fig. 3.1. FB-SMC topology.

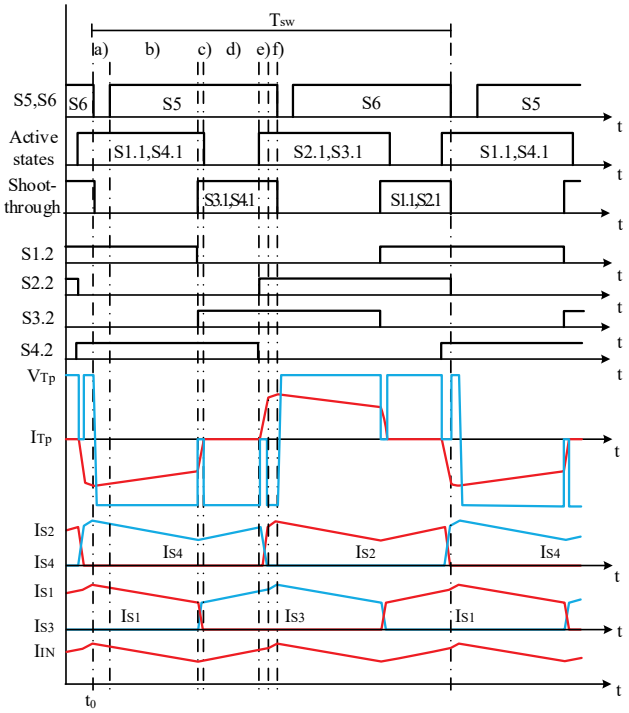

Fig. 3.2. Operational diagrams of the proposed converter topology with four four-quadrant switches.

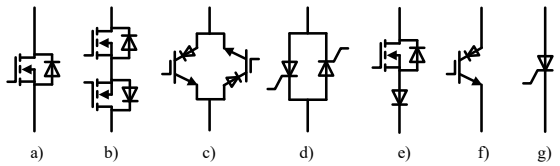

Fig. 3.3. 2Q (a), 2Q reverse blocking (e-g) and 4Q (b-d) switches.

Voltage gain factor can be expressed as [PAPER-III]:

$$G_{CF-VF} = \frac{N_S}{N_P} \cdot \frac{2}{1-(2 \cdot t_c + 2 \cdot t_d + 2 \cdot t_e + 4 \cdot t_f)/T_{SW}}, \quad (3.1)$$

where T_{sw} is the converter switching period, N_P and N_S are the number of the turns of the primary and secondary windings, t_c, t_e, t_f is the duration of the switching intervals c), e) and f) accordingly (Fig. 3.2.).

The simplified Gain factor can be expressed by the equation:

$$G_{CF-VF} = \frac{N_S}{N_P} \cdot \frac{2}{1-D_S-2D_{REV}}, \quad (3.2)$$

where $D_S = 2 \cdot (t_c + t_d + t_e) / T_{SW}$ is the shoot-through duty cycle; $D_{REV} = 2 \cdot t_f / T_{SW}$ is the duty cycle of the reverse reactive energy transfer interval.

Among the advantages of the FB-SMC converter are:

- bidirectional energy transfer is possible [PAPER-I];
- all semiconductors operate under soft-switching conditions in both energy transfer directions [PAPER-II];
- soft-switching is achieved in a relatively wide operation range [PAPER-II];
- self-clamping of the CF inductor voltage [PAPER-II];
- no passive snubbers are required, soft-switching is achieved with the help of parasitic equivalent output capacity of the VF transistors and phase-shifter modulation algorithm [PAPER-I];
- it is possible to achieve both polarities of voltage on the CF port in VF to CF energy transfer direction [PAPER-VI];
- peak current of the switches and the transformer never exceeds the input current. This leads to minimized energy circulation [PAPER-X].

A significant disadvantage of the FB-SMC topology is a high number of switches at the CF side. Taking into account that the proposed converter topology acts as a step-up converter in the energy transfer direction from the CF to the VF port with 1:1 transformer, the most reasonable applications will be with low voltage CF and high voltage VF port. As a result, a high number of switches at the low voltage/high current side leads to high conduction losses, and so the power stage efficiency can be lower than in other full-bridge CF and VF topologies.

A distinctive feature of FB-SMC is that the regulation of the output voltage is done by varying of the shoot-through duty-cycle (D_s) that is achieved by changing the phase-shift between CF side diagonals. At the same time, the duty cycles of the CF-port transistors (D_{CF}), VF-port transistors (D_{VF}) and the phase shift between CF- and VF-ports (D_{rev}) are selected at the design stage [PAPER-II] and remain there throughout the whole operation range. Alternatively, regulation can be achieved by varying D_{rev}, while D_s and other duty-cycles are fixed. However, this approach demonstrated lower efficiency and higher transformer losses due to the increased reactive energy circulation [48].

3.1 Topology with Auxiliary Active Switch

To decrease the number of switches in the CF-port, the topology with an auxiliary active switch (AUX-SMC) was proposed Fig. 3.4. It uses the same principle of phase-shifted modulation as the FB-SMC to achieve soft-switching operation but has one additional 4Q switch instead in series with the transformer winding instead of all CF-side switches being four-quadrant. The topology was first introduced in [PAPER-III], and the reverse operation mode was presented in [PAPER-IV]. Modulation sequence and generalized waveforms for AUX-SMC in CF to VF energy transfer mode are shown in Fig. 3.5.

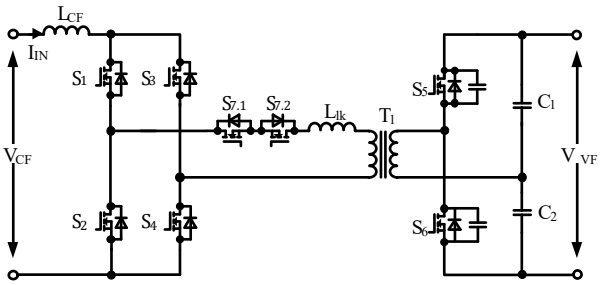

Fig. 3.4. AUX-SMC topology.

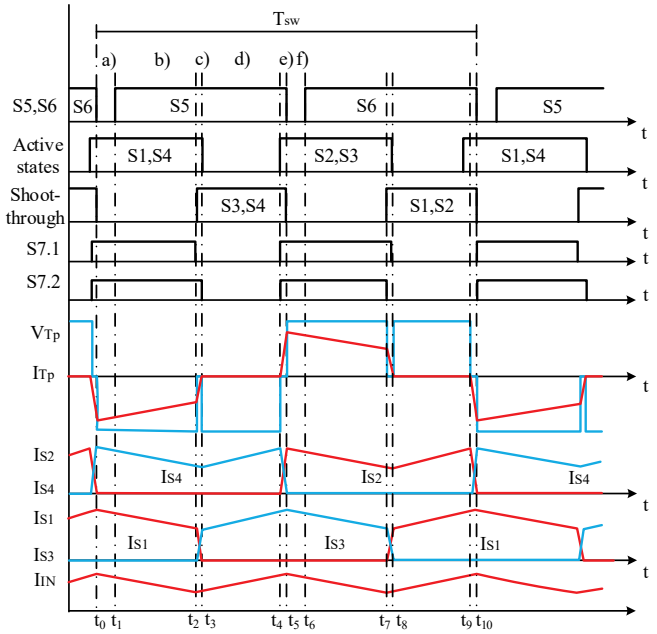

Fig. 3.5. Operational diagrams of the proposed converter topology with a single four-quadrant switch.

Voltage gain factor can be expressed as [PAPER-III]:

$$G_{CF-VF} = \frac{N_S}{N_P} \cdot \frac{2}{1-(2 \cdot t_c + 2 \cdot t_d + 2 \cdot t_e)/T_{SW}} \tag{3.3}$$

where t_c, t_d, t_e – the duration of the switching intervals c, d and e accordingly (Fig. 3.5).

This topology has the benefits and drawbacks of the FB-SMC topology while the number of switches and control signals is lower. Nevertheless, the topology has a significant control limitation. As seen from the operating waveforms of Figs. 3.5 and 3.2, one switching interval is absent. In the FB-SMC topology it served as an additional safety interval to extend the soft-switching range towards low current (minimal power at maximum input voltage) at the cost of increased circulation energy at high input current (the highest power at minimum input voltage). Without the possibility to adjust this interval, the soft-switching range is more limited compared to FB-SMC due to the increased VF transistors parasitic capacitor recharge time at the low input current.

3.2 Asymmetric FB topology

Another way to decrease the number of switches in FB-SMC was proposed in [PAPER-IIX]. Asymmetrical full-bridge phase-shifted converter (A-SMC) aims to add the advantage of consistent VF transistor C_{eq} recharge rate to the phase-shifted SMC that was previously available only in PW-SMCs [PAPER-IX]. A-SMC topology is shown in Fig. 3.6, generalized waveforms for CF to VF energy transfer direction in Fig. 3.7.

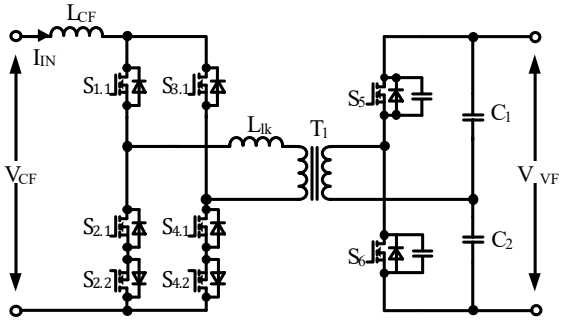

Fig. 3.6. A-SMC topology.

Voltage gain factor can be expressed as [PAPER-IIX]:

$$G_{CF-VF} = \frac{N_S}{N_P} \cdot \frac{2}{1-2 \cdot (t_{2-3} + t_{1-6(\min)})/T_{SW}} \tag{3.4}$$

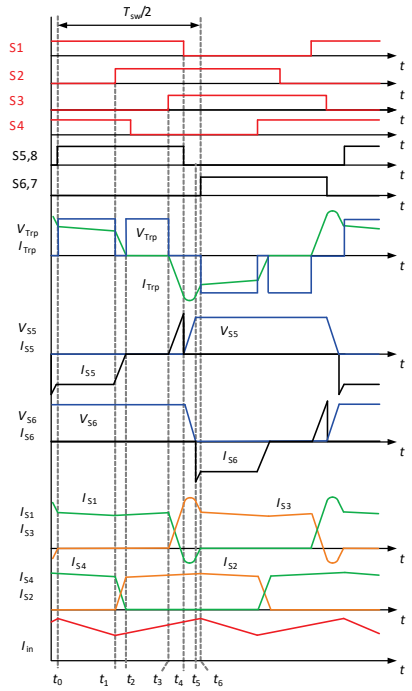

Fig. 3.7. Generalized waveforms of A-SMC.

Usage of two 2Qv switches and the modulation sequence of FB-SMC allowed extending soft-switching range down to zero power (no load operation) while having lower switch count. In FB-SMC, it was limited by the slow recharge of the VF transistor equivalent output capacitance when the CF current was low. In A-SMC with proper design, the peak current of the top CF transistors is always higher than the input current ($t_{4\text{-}5}$) [PAPER-IIX], and this peak does not depend on the power value. Recharging of capacitor C_{eq} takes place when the current is at its peak value. Thus, the capacitor recharge time is constant and unaffected by the converter operating point.

A drawback of A-SMC, as compared to FB-SMC, is that it is non-symmetrical, which leads to non-equal loss distribution among CF semiconductors. In VF to the CF energy transfer direction it is not possible to get both polarities of the voltage on the CF port; the peak value of the CF transistors current is always high and thus they suffer from increased conduction losses at light loads. Another disadvantage is that precise dimensioning of leakage inductance is necessary to avoid unreasonably high energy circulation.

3.3 Single Inductor Push-Pull

A-SMC and AUX-SMC both have fewer switches than FB-SMC, but still, a total number of transistors is higher than in most competing CF topologies like active-clamp and PW-SMC [PAPER-IIX]. That is why the author tried to extend the proposed soft-switching algorithm to topologies with low switches count. Among such topologies, the first is a single-inductor push-pull secondary modulated converter (SiPP-SMC). The topology is shown in Fig. 3.8. Generalized waveforms in the CF to VF energy transfer direction are shown in Fig. 3.9. Switching intervals and the reverse energy transfer mode are shown in [PAPER-V].

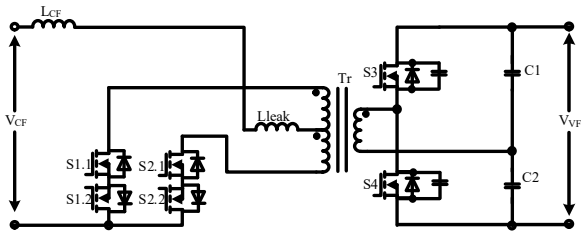

Fig. 3.8. Generalized waveforms of SiPP-SMC.

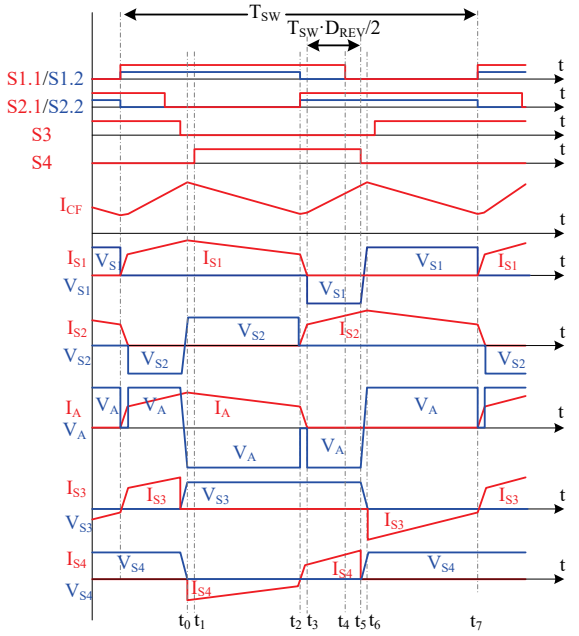

Fig. 3.9. Generalized waveforms of SiPP-SMC for the forward operation mode.

SiPP-SMC has many of the benefits of the FB-SMC, at the same time, it has significantly lower switches count.

Among the drawbacks of SiPP-SMC are:

– three winding transformer is required, which makes it generally bulkier and more complex in design as opposed to the two-winding transformer in the presented topologies;

- two times higher steady-state voltage stress across the CF switches compared to the FB-SMC converter with the same parameters and transformer turns ratio;
- increased energy circulation, especially at higher gain values, because the regulation is done by varying the duration of the reactive energy transfer interval.

Voltage gain factor can be expressed as [PAPER-V]:

$$G_{FRW} = \frac{V_{VF}}{2nV_{CF}} = \frac{1}{1-2\cdot D_{REV}}, \tag{3.5}$$

3.4 Dual Inductor Push-Pull

Another topology with low-switches count is the dual inductor push-pull SMC topology (DiPP-SMC) introduced in [PAPER-VI]. The topology and generalized waveforms are shown in Figs. 3.10. and 3.11 respectively. Due to the configuration of the switching stage, modulation sequence currents through the inductors reach their peak value with a phase-shift of 180 degrees between each other. Furthermore, at any given instance of time, one of the input inductors is accumulating the energy, and another one is releasing it. As the converter input current is equal to the sum of the input inductor currents, the converter never operates in discontinuous conduction mode.

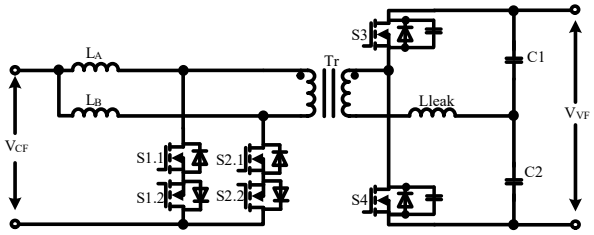

Fig. 3.10. DiPP-SMC topology.

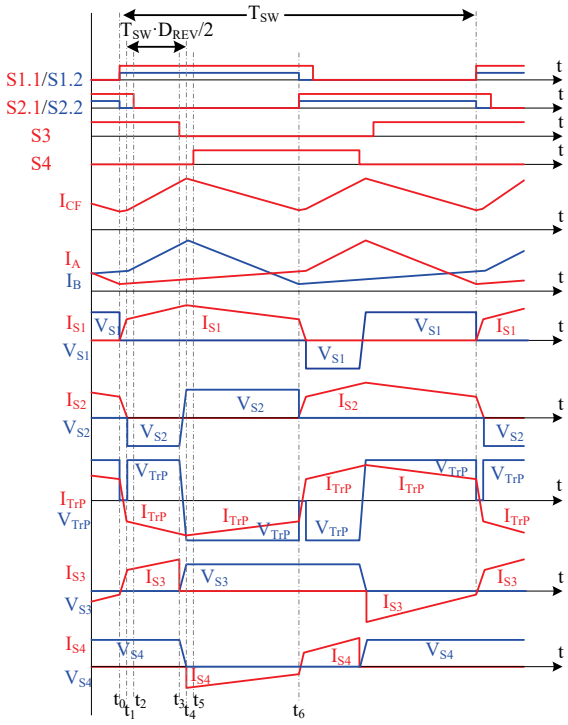

Fig. 3.11. Generalized waveforms of DiPP-SMC.

The voltage gain of DiPP is expressed as:

$$G_{CF-VF} = \frac{N_S}{N_P} \cdot \frac{2}{1-4 \cdot D_{REV}}, \tag{3.6}$$

DiPP-SMC topology has the following advantages compared to FB-SMC:

- two times higher minimal gain, so the transformer turns ratio will be lower than in FB-SMC and SiPP-SMC;
- two-winding transformer is required unlike the SiPP-SMC;
- immune to the discontinuous current mode.
- The disadvantages of the DiPP-SMC:
- doubled steady-state voltage stress on the CF transistors;
- increased number of magnetic components (two inductors);
- increased energy circulation, since the output voltage is regulated by varying the duration of the reactive energy transfer interval.

3.5 Flyback SMC

Further development of the DiPP-SMC topology revealed that it is redundant and can operate even at failure of one of the inductors. The topology obtained from DiPP-SMC by removing one of the CF inductors (Fig. 3.12.) was presented as a flyback secondary modulated converter (FBK-SMC) in [PAPER-XI]. The extra benefit of this topology as compared to the DiPP-SMC is the reduced number of magnetic elements.

The drawback of this converter is that input current ripple is higher and its frequency is two times lower than in other PS-SMC topologies (I_{CF} waveform in Fig. 3.13.).

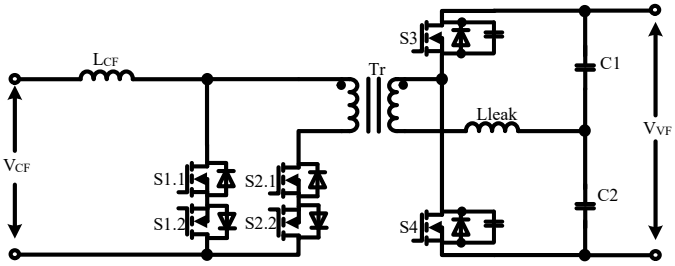

Fig. 3.12. FBK-SMC topology.

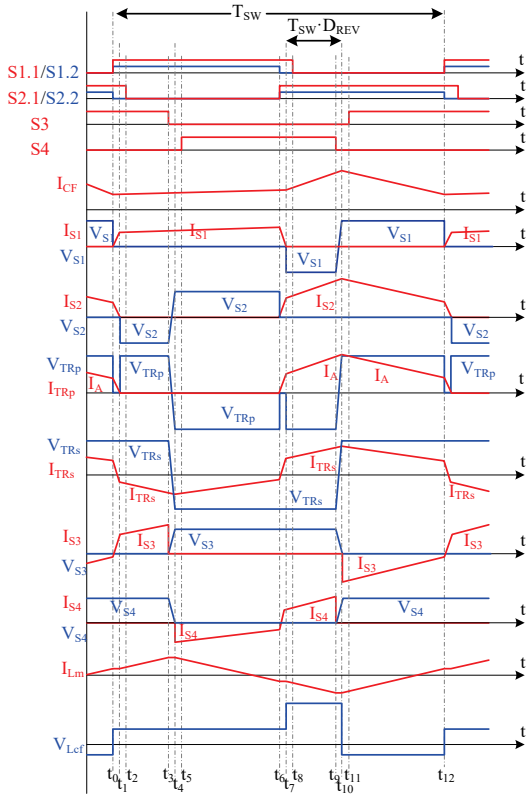

Fig. 3.13. Generalized waveforms of FBK-SMC in the forward operation mode.

Generalized waveforms of FBK-SMC are shown in Fig. 3.13. Description of control intervals is presented in [PAPER-XI]. Voltage gain in the CF to VF energy transfer direction is expressed as:

$$G_{CF-VF} = \frac{N_S}{N_P} \cdot \frac{2}{1-4 \cdot D_{REV}}, \tag{3.7}$$

Operation in the VF to CF energy transfer direction has not been discussed in paper, but in general, it is similar to DiPP-SMC. Generalized waveforms in this mode are shown in Fig. 3.14.

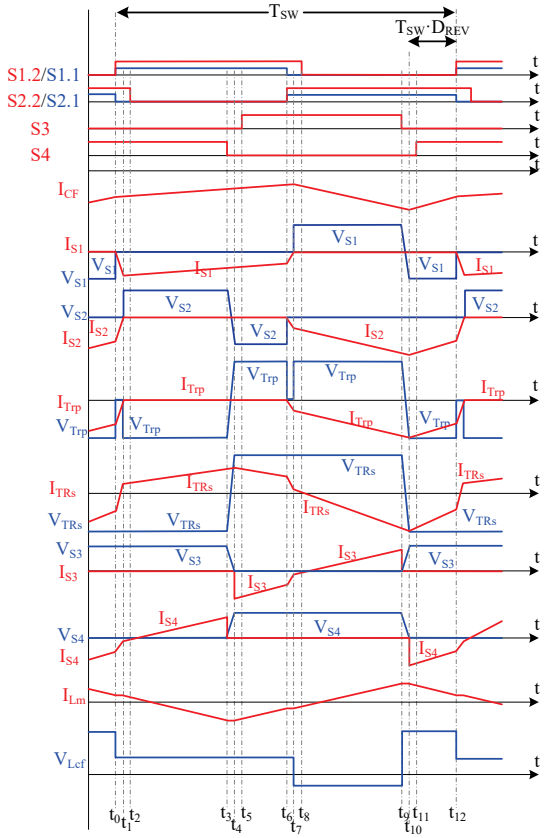

Fig. 3.14. Generalized waveforms of FBK-SMC in the reverse operation mode.

Interval 1 ($t_0 < t < t_1$). At the instant t_0, the switch S2.1 is turned off. The body diode (BD) of S2.1 conducts the current. The 4Q switch S1 is turned on with ZVS, assisted by the transformer leakage inductance. The transformer current I_{TRp} is redistributing between the 4Q switches, from S2 to S1, and changes its sign. Transformer primary voltage drops to zero.

Interval 2 ($t_1 < t < t_2$). At the instant t_1, current through the 4Q switch S2 drops to zero, causing the BD of S2.1 to turn off naturally. From this instant, the switch S2.2 can be switched off with ZCS. The inductor L_{CF} feeds the load. Transformer-magnetizing inductance starts accumulating energy from C4 through S4. This interval is needed to

ensure that the current through S2 drops to zero in the whole converter operation range.

Interval 3 ($t_2 < t < t_3$). Switch S2.2 is turned off with ZCS at the instant t_2. Processes in this interval are similar to the previous one. This interval is needed to separate switching transitions in CF and VF sides and in most cases it can be omitted.

Interval 4 ($t_3 < t < t_4$). The switch S4 turns off with snubber-assisted (C2) soft-switching at the instant t_3. This results in recharging of the snubber capacitors: C2 from zero to V_{VF} and C1 from V_{VF} to zero.

Interval 5 ($t_4 < t < t_5$). At the instant t_4, the transformer voltage polarity is changed, causing BD of S3 to turn on. Energy accumulated in the transformer magnetizing inductance Lm is transferred to C3. This interval is needed to ensure that snubber capacitors are recharged and should be optimized to minimize the BD conduction losses.

Interval 6 ($t_5 < t < t_6$). At the instant t_5 S3 turns on with ZVS. Energy transfer from Lm to C3 continues with reduced conduction losses.

Interval 7 ($t_6 < t < t_7$). At the instant t_0, the switch S1.1 is turned off. The body diode (BD) of S1.1 conducts the current. The 4Q switch S2 is turned on with ZVS, assisted by the transformer leakage inductance. Processes are analogical to those on interval 1.

Interval 8 ($t_7 < t < t_8$). At the instant t_1, current through the 4Q switch S2 drops to zero, causing the BD of S1.1 to turn off naturally. Energy transfer interval is started. Energy is transferred through the transformer from VF to CF terminal. L_{CF} starts accumulating energy.

Interval 9 ($t_8 < t < t_9$). S1.2 is turned off with ZCS at the instant t_8. Energy transfer interval continues.

Interval 10 ($t_9 < t < t_{10}$). The switch S3 turns off with snubber-assisted (C1) soft-switching at the instant t_9.

Interval 11 ($t_{10} < t < t_{11}$). At the instant t_{10}, the transformer voltage polarity is changed, causing BD of S4 to turn on. Reverse energy transfer interval is started. Energy accumulated in L_{CF} is transferred to the load and to the C4 through the transformer.

Interval 12 ($t_{11} < t < t_{12}$). At the instant t_{11}, S4 turns on with ZVS. Reverse energy transfer continues with reduced conduction losses. Duration of intervals 11 and 12 defines the converter gain factor. It is expressed by the equation:

$$G_{CF-VF} = \frac{N_P}{N_S} \cdot 0.5 - 2 \cdot D_{REV}, \quad (3.8)$$

3.6 Summary of Chapter 3

Five new topologies were proposed: two full-bridge with a different configuration of 4Q switches (AUX-SMC and A-SMC) and three with a reduced number of switches (SiPP-SMC, DiPP-SMC, FBK-SMC). In industrial applications, converter efficiency is a trade-off of components cost and quality. In soft switching converters, two mains sources of losses are semiconductor conduction losses and losses in magnetic components. In the case of step-up power converters, conduction losses on the low voltage (high current) side are defining. With the development of the semiconductor technology, prices of the state-of-the-art transistor silicon transistors are low. As was shown in [44], it is unreasonable to use expensive emerging wide-bandgap GaN transistors in PS-SMCs; they will not give efficiency gain but only better size/weight characteristics with higher switching frequencies. At the same time, to improve converter efficiency by the reduction of the losses in magnetic components it is needed to use exotic and expensive magnetic materials. Thus, the increased static semiconductor losses because of the higher number of switches in PS-SMC converters are not so critical as they allow a decrease in the losses in magnetic elements by decreasing the circulating energy [PAPER-II], [PAPER-X].

The topologies proposed are sharing some common features, such as:

+ PS-SMC by nature – regulation is achieved by variation of the phase shift between CF and VF ports while the duty-cycle of all switches remains the same;
+ Active rectifier (VF port) enables bidirectional power transfer;
+ Soft-switching operation in both directions;
+ Soft-switching operation in a wide regulation range;
+ Voltage clamping of the CF port inductor voltage;
+ No snubbers are required;
+ Immune to transformer saturation (flux runaway).

4 Application-Specific Design of GISS Bidirectional DC-DC Converters for Energy Storage Applications

An experimental prototype was designed for interfacing of the eight-cell $LiFePO_4$ battery into the 400V DC-bus as a part of battery energy storage system (BESS). The converter was designed to cover the whole voltage range of the battery. The voltage of the eight-cell $LiFePO_4$ battery varies in a range of 20-30 V. One of distinguished features of the $LiFePO_4$ batteries is that the output voltage remains almost constant on a level of 25.6 V in a range of approximately 20-80% of its nominal capacity. LFP battery charge and discharge curves are shown in Fig. 4.1a. Hence, the interface converter should be optimized for this operation voltage.

The nominal operational voltage of the selected battery is 25.6 V. During normal operation, the voltage of the battery should not drop below 20 V and rise above 30 V to avoid deep discharge and overcharge conditions. The battery charge and discharge curves at maximum rate are shown in Fig. 4.1b.

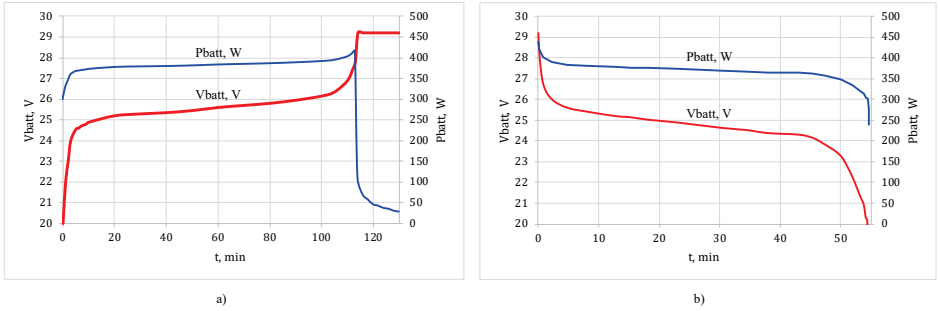

Fig. 4.1. 8-cell LiFePO4 battery charge a) and discharge b) profiles.

4.1 Full-Bridge SMC topology

FB-SMC is used as a baseline topology to assess topologies with reduced switches count. BESS storage based on the FB-SMC topology is described in detail in [PAPER-VII]. In this research, a grid inverter is not taken into account as it is the same for all compared systems.

General parameters of the prototype are presented in Table 4.1. The parameters of the semiconductor devices are listed in Table 4.2. The experimental converter prototype in Fig. 4.2 is controlled by the STM32F334R8T6 microcontroller. The input and output current are measured by ACS716 and ACS712 current sensors respectively. The voltages are measured with the isolated operational amplifier AMC1200. All the sensors were connected to the ADC converter integrated into the microcontroller through the active analog filters. VF side transistors are controlled with ACPL-P346 drivers. CF side transistors are controlled with ADUM3221 dual channel galvanically isolated drivers. Usage of such drivers allows us to minimize components count as only one driver and isolated supply are needed to drive the bidirectional 4Q switch.

All the experimental waveforms were acquired with the digital oscilloscope Tektronix MSO4034B equipped with Rogowski coil current probe PEM CWTUM/015/R, current probe Tektronix TCP0030A, and high-voltage differential voltage probes Tektronix P5205A. Efficiency of the converter was measured while it was supplied from a DC power supply Elektro-Automatik EA-PSI 9080-60 in the charge mode and from TDK-Lambda GEN600-5.5 in the discharge mode. Efficiency measurements were carried out with a YOKOGAWA WT1800 high-precision power analyser.

TABLE 4.1. OPERATING PARAMETERS OF THE EXPERIMENTAL CONVERTER

Parameter	Symbol	Value
Converter power rating, W	P	500
Input voltage, V	V_{CF}	20-30
DC-bus voltage, V	V_{DC}	400
Switching frequency DC-DC, kHz	f_{SW}	50
Switching frequency DC-AC, kHz	f_{SW}	20
Transformer turns ratio (Ns /Np)	N	33/6
Transformer magnetizing inductance, uH	L_{TX_m}	930
Transformer leakage ind., nH	L_{leak}	430
Inductance of boost inductor, uH	L_{CF}	100
Capacitance of filter capacitor, uF	C_1,C_2	2.2
Capacitance of DC-link capacitor, uF	C_3	150

TABLE 4.2. TYPES AND PARAMETERS OF SEMICONDUCTOR DEVICES USED

Component	Type	Specifications
S1.1 – S4.2	Infineon BSC035N10NS5	V_{DS}=100 V; $R_{DS(on)}$=3.5 mΩ I_D=100 A, t_{rr}= 62 ns, Q_{rr}=122 nC
S5 – S11	Infineon: IPP65R225C7	V_{DS}=650 V; $R_{DS(on)}$=225 mΩ I_D=41 A, t_{rr}=890ns, Q_{rr}=600 nC

Duty cycles required for the soft-switching operation were in a range of 50-500 W input power and 20-30 V CF-side voltage was calculated by the methodology proposed in [PAPER-II]. For the prototype DVF=0.47 and DCF=0.516. Visual representation of the soft-switching range and the converter operation area is shown in Fig. 4.3. Converter operating area is marked as a shaded rectangle. Power stage efficiency measurement results are shown in Table 4.3. Measurements were carried out in all the assessment tool points, an additional point at 25% of the nominal power was added to smoothen out the efficiency graphs that will be shown at the end of this chapter. Negative power represents converter operation in the discharge mode (energy is transferred from CF- to VF-side) while positive power corresponds to the charge mode.

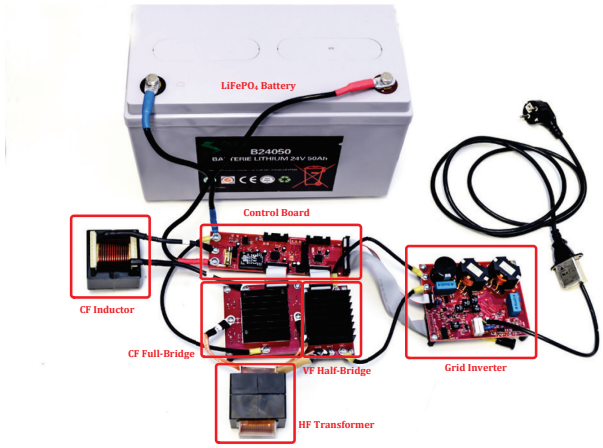

Fig. 4.2. Experimental prototype of FB-SMC.

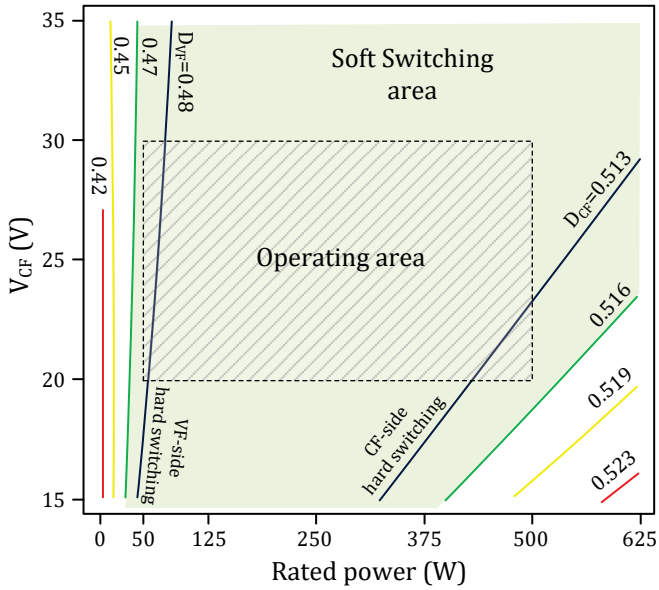

Fig. 4.3. FB-SMC soft-switching operation range.

TABLE 4.3. FB-SMC POWER STAGE EFFICIENCY MEASUREMENTS

Pin, %	Pin, W	Vcf, V		
		20	25	30
		Eff., %	Eff., %	Eff., %
-100	-500	92.9	94.6	95.6
-70	-350	94.3	95.4	96.7
-40	-200	96.2	97.0	97.6
-25	-125	96.7	97.2	97.4
-10	-50	95.2	96.1	96.0
10	50	94.2	94.6	94.9
25	125	95.7	96.4	96.7
40	200	95.6	96.7	97.1
70	350	94.4	96.0	96.6
100	500	92.9	94.7	95.9

4.2 Asymmetric FB SMC topology

A-SMC parameters and components used are the same as for FB-SMC (Tables 4.1 and 4.2). The soft-switching range and its dependence on the transistors duty-cycles are shown in Fig. 4.4. As seen from the comparison of Figs. 4.3 and 4.4, A-SMC has the same soft-switching range border at high power as the FB-SMC, but it can operate under soft-switching conditions down to zero power. Results of the efficiency measurements of the A-SMC power stage are shown in Table 4.4.

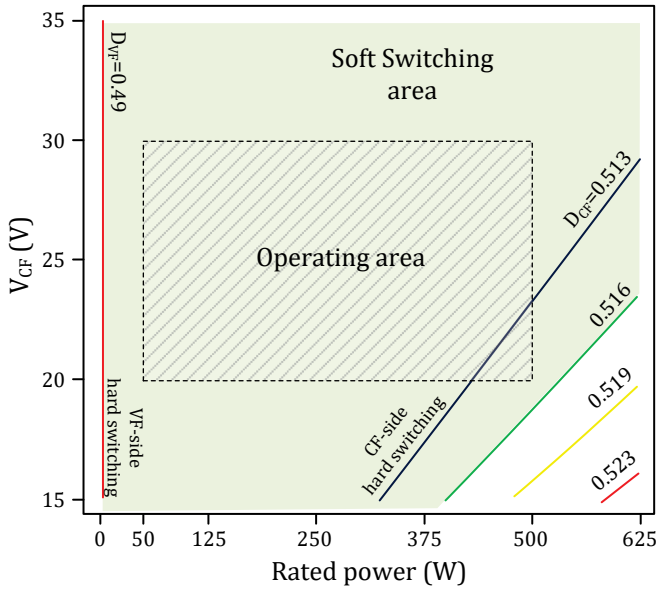

Fig. 4.4. A-SMC soft-switching boundaries.

TABLE 4.4. A-SMC POWER STAGE EFFICIENCY

Pin, %	Pin, W	Vcf, V		
		20	25	30
		Eff., %	Eff., %	Eff., %
-100	-500	91.7	94.3	95.4
-70	-350	93.4	95.3	95.8
-40	-200	94.4	95.4	95.7
-25	-125	93.7	94.2	94.4
-10	-50	87.8	88.0	87.9
10	50	90.5	91.0	90.6
25	125	94.3	95.0	95.3
40	200	94.9	95.8	96.0
70	350	93.2	95.1	95.8
100	500	91.2	93.9	95.0

4.3 Dual Inductor Push-Pull SMC topology

For an experimental verification of DiPP-SMC, main converter parameters are the same as for FB-SMC. Still, due to the doubled minimal gain factor of DiPP-SMC, the transformer with two times lower turns ratio is required. Parameters of the transformer and input inductors are shown in Table 4.5. Moreover, CF transistors suffer from increased steady-state voltage stress due to the reflected transformer voltage; so, their voltage rating should be higher. CF transistors with the parameters closest possible to those of FB-SMC but increased operating voltage were selected, their parameters are shown in Table 4.6. The dependency of the soft switching range of the converter on the the values of boundary duty cycles calculated is shown in Fig. 4.5. According to the calculations, to ensure soft-switching in the whole operation area, CF duty cycle should be 0.51 or higher and VF duty cycle should be 0.46 or lower. These values were used in transistor modulation sequences during the experiments.

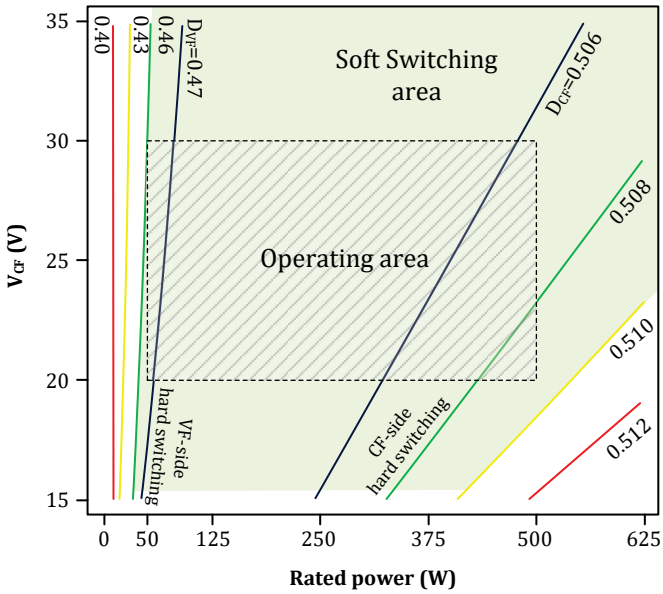

Fig. 4.5. Converter soft-switching boundaries.

TABLE 4.5. PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter / Component	Symbol	Value
Primary side inductor, µH	L_A, L_B	44
Transformer turns ratio	N_2/N_1	22:8
Transformer magnetizing inductance, mH	L_{TX_m}	3
Equivalent TX leakage inductance, µH	L_{leak}	10

TABLE 4.6. SEMICONDUCTOR COMPONENTS OF THE EXPERIMENTAL DIPP-SMC PROTOTYPE

Component	Type	Specifications
S1.1 – S2.2	Infineon IPB048N15N5	V_{DS}=150 V; $R_{DS(on)}$=4.8 mΩ I_D=120 A, t_{rr}= 60ns, Q_{rr}=83 nC
S3 – S4	Infineon: IPP65R225C7	V_{DS}=650 V; $R_{DS(on)}$=225 mΩ I_D=41 A, t_{rr}=890ns, Q_{rr}=600 nC

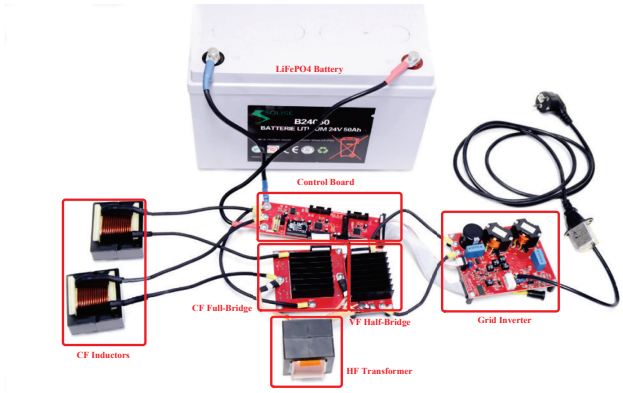

Fig. 4.6. Experimental DiPP-SMC prototype.

TABLE 4.7 DIPP-SMC POWER STAGE EFFICIENCY.

Pin, %	Pin, W	Vcf,V		
		20	25	30
		Eff., %	Eff., %	Eff., %
-100	-500	94.30	95.90	96.30
-70	-350	95.30	96.50	96.40
-40	-200	96.10	96.70	96.20
-25	-125	95.70	96.10	95.10
-10	-50	93.00	92.70	90.00
10	50	92.98	91.00	86.60
25	125	96.15	95.70	94.44
40	200	96.20	96.30	96.30
70	350	95.40	96.20	96.40
100	500	94.30	95.32	96.00

4.4 Experimental results

For the ease of comparison, the measured power stage efficiency for both energy transfer directions is visually represented in Figs. 4.7- 4.9 for different voltage levels.

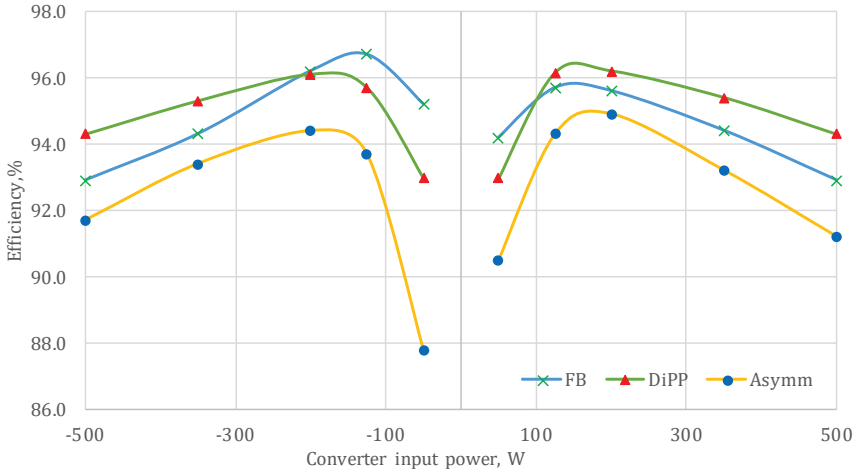

Fig. 4.7. Comparison of converter efficiency at Vcf=20 V.

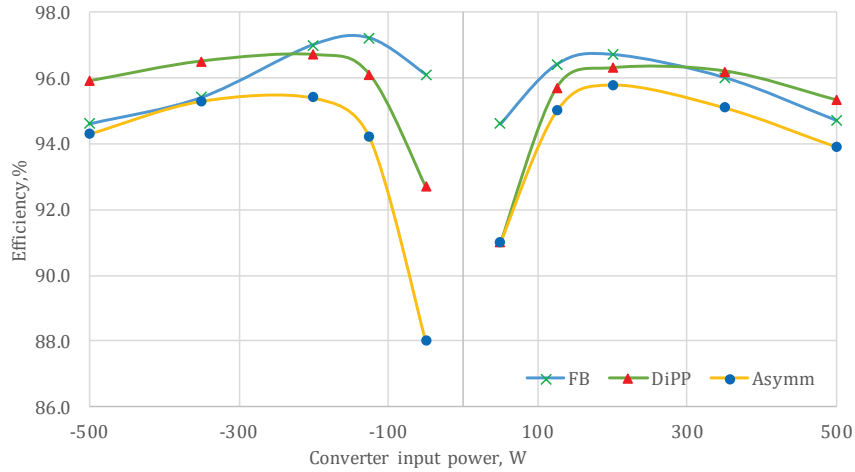

Fig. 4.8. Comparison of converter efficiency at Vcf=25 V.

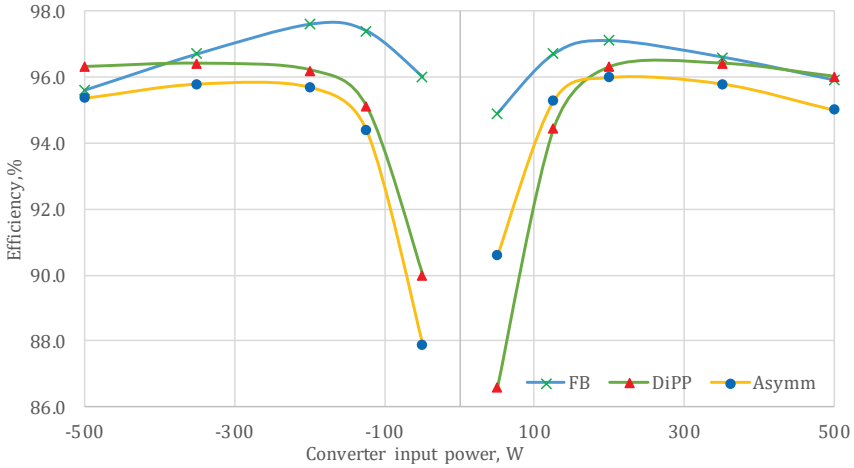

Fig. 4.9. Comparison of converter efficiency comparison at Vcf=30 V.

4.5 Summary of Chapter 4

In this chapter, application-oriented design of three SMC converters was discussed. Current-fed soft-switching GI converters in low voltage BESS application can give a significant advantage over voltage fed counterparts as they allow continuous battery charge and discharge current and decrease transformer size and turns ratio because of inherited voltage step-up capability. More of that soft-switching operation of proposed converters in the whole operation range is a significant benefit in this high-current application that places the proposed converters in the same line with industry approved soft-switching VF dual active bridge converters.

Three experimental converters with the same parameters were developed to justify the applicability of SMC converters for BESS:

- All three converters showed an efficiency higher than 95% in the middle of the operation range, close to the nominal battery voltage, V_{CF}=25 V (Fig. 4.1) and power higher than 25% of that rated.
- It was proven by the theoretical and experimental data that SMC converters with reduced switches count preserve benefits and operation range of the full-bridge based SMC topologies.
- It was shown that the SMC topology with reduced switches count DiPP-SMC is able to achieve higher power stage efficiency at high power.
- A-SMC and DiPP-efficiency drop at low power level predicted by the assessment tool in Chapter 3 was proven by the experimental data.

5 Performance Assessment of Bidirectional Current-Fed DC-DC Converters

5.1 Definition of Comparison Criteria

There is a variety of GI CF topologies and clamping methods. Since each application has its specific requirements and optimization priorities, the choice of the most suitable topology for a particular application requires comparison according to certain criteria. The initial tool for the assessment and comparison of topologies was presented in [PAPER-X]. It was performed by evaluating two parameters: cumulative RMS current in the CF side (primary inverter) (sum of RMS currents in all switches) and RMS transformer primary current, both normalized to the RMS input current. In the scope of [PAPER-X], the difference in secondary currents between the analyzed converters was found to be relatively small, and thus the analysis of the rectifier currents was omitted. This approach allowed to evaluate and compare different current source isolated full bridge converters. However, the methodology has a limited scope and cannot be used to adequately compare converter topologies others than full-bridge based.

Author's proposal for the improvement of the assessment tool is described below. It is extended to allow us to evaluate and compare not only the full-bridge topologies but also the topologies with different switch count such as half-bridge and push-pull or even VF and CF converters within the same application mission profile.

A general galvanically isolated converter consists of five functional blocks, as shown in Fig. 5.1: input energy storing element (capacitor, inductor or both), primary inverter, isolating transformer, secondary rectifier, output filter.

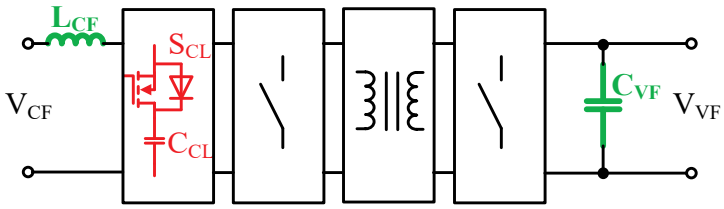

Fig. 5.1. The generalized structure of the galvanically isolated converter.

For the analysis, certain assumptions were defined. All the components were considered lossless, the input inductor current ripple (or, in the voltage source topology, input capacitor voltage ripple) and the output voltage ripple were negligible and transformer magnetizing inductance infinitely large. For this reason, the input energy storing element and the output filter were not taken into consideration in the scope of this evaluation. The converters were investigated for the capability of soft switching and stabilization of the output voltage with 1:2 input voltage and 10% to 100% load variations. For comparison, the equivalent inductance and capacitance parameters were chosen such that the converter's input inverter should be capable of providing exactly 1.1 voltage gain at a maximum input voltage and maximum power, while the transformer turns ratio and switching frequency were assumed the same. The parameters of all topologies under the evaluation were derived using these design constraints.

The evaluation was performed using three normalized quantities that represent the loading conditions of the primary inverter, isolation transformer and secondary rectifier.

Primary inverter loading conditions are represented as a ratio between the cumulative RMS current in primary semiconductors ($I_{Sp(RMS)}$) multiplied by the steady-state voltage stress across semiconductors at the input side ($V_{Sp(DC)}$) and the product of the input current (I_{in}) by the input voltage (V_{in}):

$$V_{SpN} \cdot I_{SpN} = \frac{\sum_{\substack{Switch \\ Primary}} I_{Sp(rms)} \cdot V_{Sp(DC)}}{I_{in} \cdot V_{in}} . \quad (5.1)$$

Transformer loading conditions are represented by a ratio between the product of the cumulative RMS transformer primary current ($I_{TXp(RMS)}$) by a transformer steady-state primary voltage and the product of the input current by the input voltage:

$$V_{TXpN} \cdot I_{TXpN} = \frac{\sum_{\substack{Winding \\ Primary}} I_{TXp(rms)} \cdot V_{TXp(DC)}}{I_{in} \cdot V_{in}} . \quad (5.2)$$

Secondary rectifier loading conditions are represented as a ratio between the cumulative RMS current in secondary semiconductors ($I_{Ss(RMS)}$) multiplied by the steady-state voltage stress across semiconductors to a product of the output current (I_{out} by the output voltage (V_{out}):

$$V_{SsN} \cdot I_{SsN} = \frac{\sum_{\substack{Switch \\ \text{Sec}ondary}} I_{Ss(rms)} \cdot V_{Ss(DC)}}{I_{out} \cdot V_{out}} . \quad (5.3)$$

In [PAPER-X], loading conditions of the secondary part were not considered because in the scope of that study they were similar for all reviewed converter topologies. The inclusion of this parameter to the assessment tool allowed us to evaluate and compare topologies with different secondary rectifier stages and to assess the impact of reactive energy in a circuit for appropriate topologies. Addition of normalized voltage stress, on the other hand, allowed us to compare topologies with different transformer turns ratios and switches configuration.

5.2 Converter Evaluation Operation Points

In the proposed approach, the operation region of a particular application is divided by the operation voltage and power. This approach provides a set of points that are representing different converter operation conditions, starting from minimal operation power at maximal input voltage up to the nominal power at the lowest input voltage (Fig. 5.2).

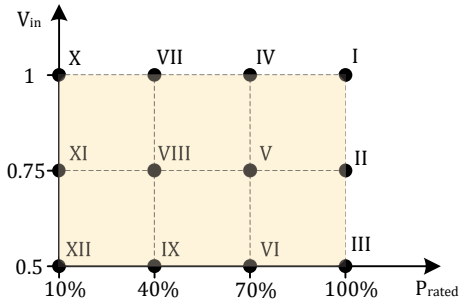

Fig. 5.2. Operating points selected for evaluative comparison of case study converters.

For each operation point, the normalized voltage-current loading condition quantities of all converters were measured. In the scope of this work, those quantities were obtained with software models done in "PSIM Simulation Software".

The results were grouped and represented in the form of circular diagrams. Such diagrams allow us to see the behavior of the topology in a whole operation range at a glance and quickly define its weak and strong points.

5.3 Limitations of the Performance Assessment Tool

The proposed assessment tool was designed for the evaluation of power stages of different power converter topologies. However, it has some limitations as it does not take into account circuit parasitic elements, control system complexity, magnetic elements design complexity or dynamic characteristics of the converter. Those parameters should also be considered during the assessment for a specific application and design limitations, as it was shown in [PAPER-X].

5.4 Assessment of Proposed Topologies

The proposed topologies were assessed with a converter assessment tool. As an application for the analysis, a $LiFePO_4$ battery energy storage system was used with a battery connected to the current-fed port. Converter nominal power was 500 W, output voltage 400 V, the input voltage was changing in a range from 20 to 30 V (operation range of the 8-cell $LiFePO_4$ battery). As all the converters are bidirectional, they will be assessed in both energy transfer directions. To distinguish the test points in different energy transfer directions, positive and negative operation power was used. Positive power corresponds to the converter input power when the energy is transferred from the voltage-fed to the current-fed port (battery charging mode). Negative power corresponds to the converter input power when the energy is transferred from the current-fed to the voltage-fed port (battery discharge mode).

Operation range was divided evenly by four power and three voltage levels, as shown in Fig. 5.3.

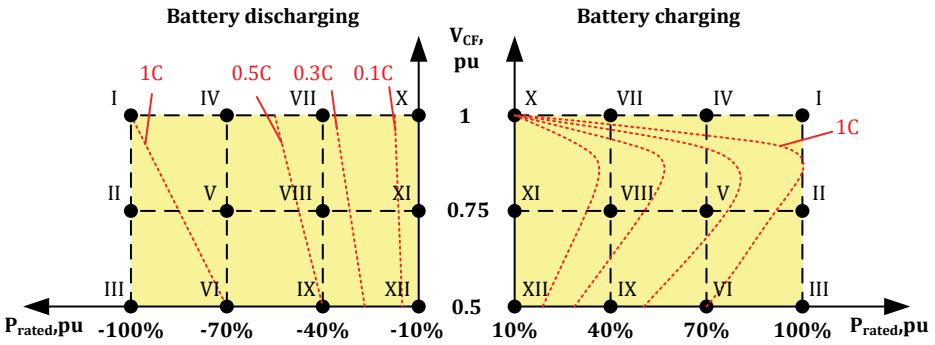

Fig. 5.3. Test points distribution over the operation range.

For clarity, the battery charge and discharge curves are shown in the figure by a red line. In the battery, energy storage system charging and discharging can be performed at any reasonable power lever below nominal, and not always at maximum power. In Fig. 5.3, the nominal charging curve with the current value in the constant current charging mode equal to the battery capacity is marked by the symbol “1C”. Charging and discharging can occur at each and any power and voltage level combination depending on the application. For example, to maximize the usage of renewable energy, the battery will be charged at any rate depending on available energy from renewable sources and will be discharged at maximum rate to support the local microgrid or at low rate during a night to support household equipment. On the other hand, when buying and selling energy from the grid, both charge and discharge will take place at maximum rate.

For each converter in each operation point, the cumulative current-voltage stresses were measured with the PSIM simulation software. The diagrams produced help to compare the static stresses on different components between converters in both forward (discharging) and reverse (charging) operation modes.

Comparison of cumulative CF transistors loading conditions ($V_{SpN}I_{SpN}$) is shown in Fig. 5.4. It is seen that AUX-SMC and A-SMC topologies have an advantage over other topologies across the whole range, except for low power; this advantage is explained by the lower number of switches in those topologies. For the A-SMC topology, increased stress at low power is explained by the form of current through top transistor peak value that is independent of the power (peak value is the same for high and low power). Increased stress in the AUX-SMC topology is explained by the limitations in the modulation sequence explained earlier in this chapter. High input loading conditions of the FB-SMC topology are explained by the high number of switches in it, so even with decreased transistors, current stress multiplied by the number of switches gives a relatively high cumulative loading-condition value. SiPP-SMC and DiPP-SMC, on the other hand, both have two times lower number of switches than FB-SMC, but the voltage stress across transistors is two times higher; so the cumulative CF transistors loading-conditions are on the same level across the whole operation region in both transfer directions.

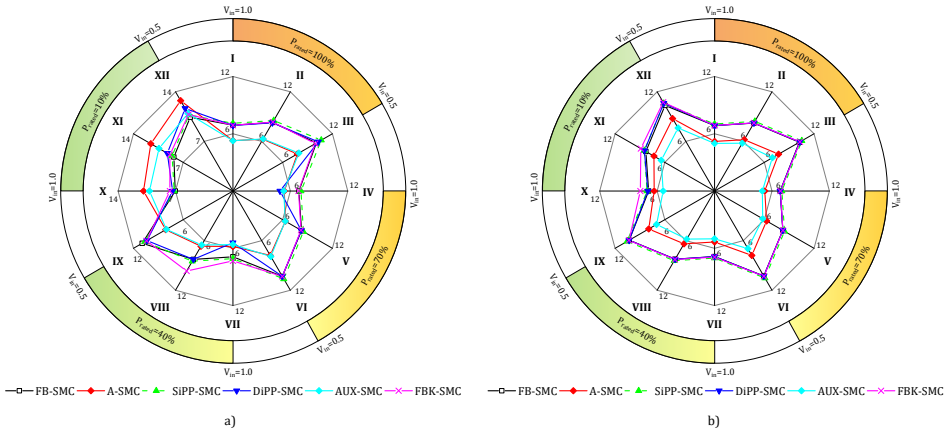

Fig. 5.4. Loading conditions of CF transistors in forward a) and reverse b) operation modes.

Loading conditions ($V_{SsN}I_{SsN}$) of the VF transistors (Fig. 5.5) of FB-SMC, AUX-SMC, and A-SMC topologies have approximately equal VF transistors loading conditions. On the other hand, SiPP-SMC and DiPP-SMC have higher VF transistors loading-conditions due to the use of the reactive energy for regulation that causes increased RMS current through VF transistors. It becomes even more obvious at low power when the reactive energy transfer interval is longest.

Transformer loading conditions ($V_{TXpN}I_{TXpN}$) are shown in Fig. 5.6. A-SMC has transformer loading conditions slightly higher than in FB-SMC, and the difference increases towards low power because the VF transistors current spike during the reactive energy transfer interval (Fig. 3.7. $t_{5\text{-}6}$) becomes relatively higher than average current. AUX-SMC has the same value as FB-SMC in the forward operation mode but much higher in reverse, this is due to the different control principle in the reverse mode [PAPER-IV]. The best topology regarding transformer-loading conditions is the DiPP-SMC, it is only lagging at low power due to the increased reactive energy circulation.

As mentioned in Chapter II, in topology selection, many parameters should be considered. No universal guidelines are available on how to treat these parameters or how to define with one parameter that has higher priority because it is highly dependent on the specific application. Some of these general properties of the presented topologies are shown in Table 5.1.

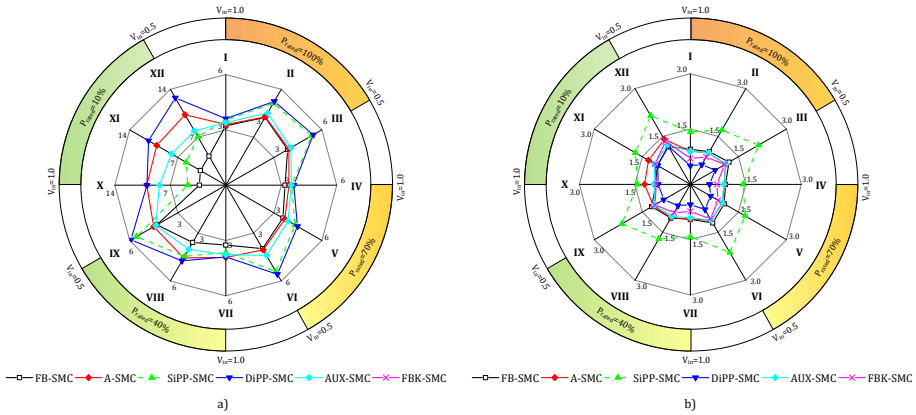

Fig. 5.5. Loading conditions of VF transistors in boost a) and buck b) operation modes.

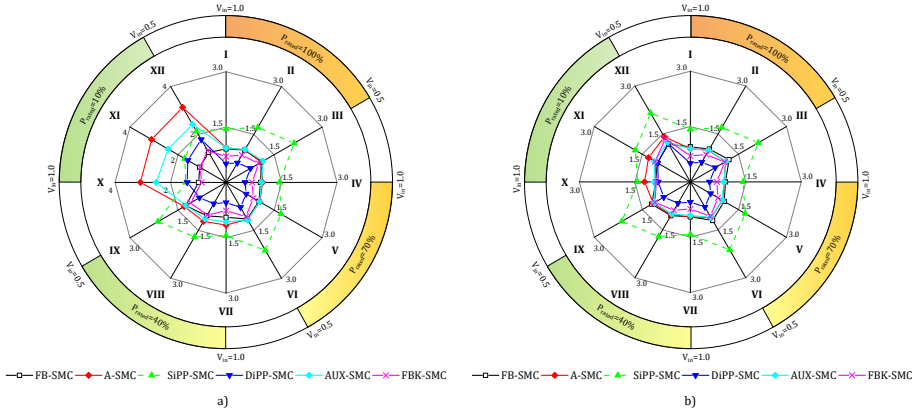

Fig. 5.6. Loading conditions of a transformer in boost (a) and buck (b) operation modes.

For comparison of the assessment tool and the experimental results, the efficiency values are plotted in Fig. 5.7 for the discharge mode and in Fig. 5.8 for the charge mode in the same style as loading-conditions. Distribution of the operation points is shown in Fig. 5.3.

TABLE 5.1. GENERAL PROPERTIES OF SELECTED SNUBBERLESS CONVERTERS

Topology	2Q Switches	4Q(RB)* switches	Control signals count	Ref.	Soft-Switching range	Transformer turns ratio
FB-SMC	2	4	10(6*)	II	normal	$\frac{V_{out}}{2 \cdot V_{in}}$
AUX-SMC	4	1	8	IV	limited	$\frac{V_{out}}{2 \cdot V_{in}}$
A-SMC	4	2	8(6*)	IX	extended	$\frac{V_{out}}{2 \cdot V_{in}}$
SiPP-SMC	2	2	6(4*)	V	normal	$\frac{V_{out}}{2 \cdot V_{in}}$ dual,
DiPP-SMC	2	2	6(4*)	VI	extended	$\frac{V_{out}}{4 \cdot V_{in}}$
Flyback-SMC	2	2	6(4*)	XI	normal	$\frac{V_{out}}{4 \cdot V_{in}}$

* switches used are depending on application requirements

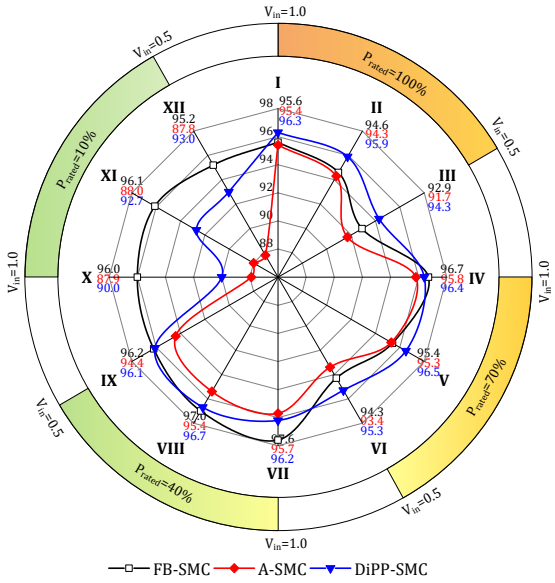

Fig. 5.7. Comparison of efficiency in the discharge mode.

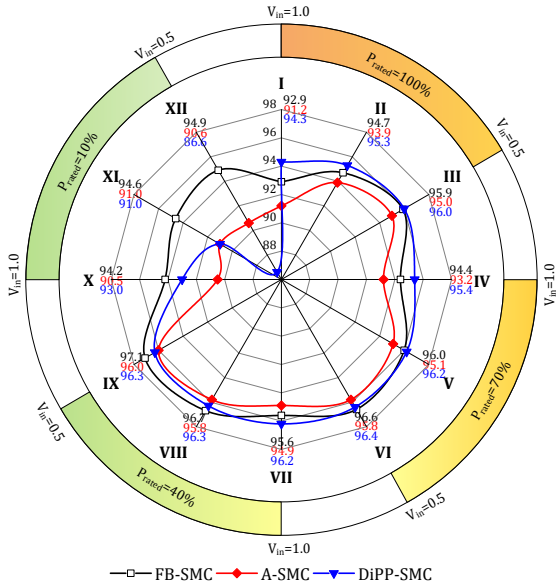

Fig. 5.8. Comparison of efficiency in the charge mode.

After the data analysis, it is clear that the DiPP-SMC topology has the highest efficiency at the power levels above 50% of the nominal while at lower power, FB-SMC takes the lead. It correlates with significantly lower transformer loading conditions in DiPP-SMC at high power (Fig.3.18).

Loading conditions of the transformer are increasing rapidly in the text points X, XI and XII in A-SMC because of the increased RMS-value of the transformer current due to the current spike described in Chapter 3. Increased transformer loading in DiPP-SMC in those points is explained by the increased circulation due to the voltage regulation principle used. Experimental results show that at lower power level, the impact of the loading conditions of the transformer is more significant than the loading conditions of the switches for soft-switching SMC topologies.

Efficiency curves of the power stage correlate perfectly with the loading conditions of the VF transistors (Fig. 3.17); the lower the loading-conditions, the higher the efficiency.

5.5 Summary of Chapter 5

The assessment tool proposed takes into account stresses on all key parts of the power converter and can be used as a universal tool for the evaluation of power converter topologies. Despite having certain limitations, it can be used to assess the performance across the operation range in the most probable operation points. Due to the intuitive graphical representation of the results, it is useful for a quick generalized comparison and can be used as one of the steps in the choice of the most suitable solution for a target application.

Experimentally measured efficiency curves and results of the theoretical assessment tool are in good correlation. This correlation proves the efficacy of the proposed assessment tool for benchmarking of SS CF converters topologies.

According to the assessment tool, there is no superior topology in all aspects, but it is expected that A-SMC will have better power stage efficiency as it has lower semiconductors loading condition. Also, the DiPP-SMC topology is competitive with full-bridge based topologies because of reduced switch count and smaller transformer and loading conditions of it.

6 Conclusions and Future Work

6.1 Conclusions

The results of this PhD thesis fully satisfy the aims and prove the hypothesis advanced by the author.

Substantial work was performed towards the synthesis of new CF PS-SMC topologies in order to show the versatility of this type of voltage clamping, Within this research work, the author has shown that the proposed clamping method could be utilized not only in full-bridge but also in other switching stages, like half-bridge, push-pull, and flyback.

However, it should be noted that on the current level of semiconductor technology, no commercial single-die four-quadrant switches are available. Their implementation requires a series connection of two transistors that inevitably leads to increased conduction losses and an increased number of control signals. This may decrease the attraction of the full-bridge variants of the proposed PS-SMC for industrial applications. The paper [PAPER-X] shows a comparison of the proposed full-bridge converter to existing topologies with other types of voltage clamping. Moreover, it was shown that even despite a higher number of switches, proposed topology could compete performance-wise with existing solutions.

The FC PS-SMC topologies were justified as an effective approach to clamping inductive voltage overshoots while providing high efficiency and flexibility regarding applications due to a variety of switching stage configuration.

As the main results of this thesis, the author claims the following:

- ✓ Two variants of PS-SMC topologies with the FB CF switching stage with reduced switches count were described. It was experimentally proven that they have all the features of the reference topology and comparable efficiency that is slightly higher at full load and slightly lower during partial load operation as compared to the reference FB PS-SMC topology.
- ✓ Three PS-SMC topologies with reduced switches count were synthesized (SIPP-SMC, DIPP-SMC, FBK-SMC).
- ✓ It was theoretically shown and experimentally verified that PS-SMC topologies with reduced switches count preserve advantages of FB PS-SMC, such as bidirectional operation, inductive voltage overshoots clamping and soft-switching of all transistors in a wide operation range regarding load and voltage regulation.
- ✓ Benchmark methodology was developed for the assessment and comparison of soft-switching DC-DC converters for a specific application.

Taking into account theoretical and practical results obtained by the author, it can be concluded that DC-DC PS-SMC topologies can beat existing voltage-fed solutions regarding performance and features in renewable energy and zero-energy building applications.

6.2 Future Work

This research work has raised a few questions about PS-SMC.

The most critical one is the application of A-SMC topology in a single stage DC-AC battery storage system with the CF-side facing the AC-grid. As was shown, A-SMC is a FB based topology capable of soft-switching and clamping in a wide-range starting from zero power. At this moment, the limiting factor is that it requires 2 two-quadrant and 2 four-quadrant switches at the CF-side but the position of those switches is changing depending on the grid voltage polarity, so only four-quadrant switches are appropriate. This can be solved by switching the altering switching stage to accommodate a central-tapped transformer and a modified modulation sequence.

Another research task is the development of alternative control methods that will allow us to decrease the number of switching transistors, widen the operation range towards low-power range and get higher part-load efficiency. For example, this work has already started with A-SMC shown in [PAPER-VIII] that presents a fusion of PWM-SMC and PS-SMC clamping methods.

A further question is the extension of the converter regulation range by topology morphing and multi-mode control at various power/voltage levels to achieve the best performance. The proposed converters allow us to achieve this, as some of them are sharing common elements of the switching stage structure. For example, FB-SMC (Fig. 3.1) can be controlled as A-SMC (Fig. 3.6) with two transistors constantly conducting by those extending FB-SMC operation range towards a low power region. Moreover, at low voltage, on the CF port FB-SMC can be reconfigured to FBK-SMC (Fig. 3.12) with one of the top four-quadrant switches constantly conducting and another constantly blocking the current. As a result, higher step-up factor and minimized number of actively switching semiconductors can be achieved. The topic of the research, in this case, is the determination of conditions for the operation mode switching of the topology and smooth transition in the control system [47]. As a special case of reconfiguration of the power converter topology, the fault-tolerant operation can be considered. For example, at failure (either short-circuit or open-circuit) of one or few semiconductors in the FB-SMC topology, it can still operate as A-SMC, FBK-SMC or in extreme cases, as PWM-SMC or partially hard-switching converter topology, at a cost of decreased efficiency and functionality in some cases. Important tasks for this research are to determine faulty transistors and to adjust appropriate autonomous modulation sequence by the converter control system.

Finally, it is required to address the synthesis of interleaved and multi-phase PS-SMC topologies for improved power for high power applications. A similar study was already carried out by the author in [48]-[50] for FB-SMC topology, but additional research for topologies with a reduced number of switches is needed.

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Roman Kosenko

Abstract

Bidirectional Isolated Current-Fed Soft-Switching Secondary-Modulated DC-DC Converters

There are two main types of well-established industry-accepted DC-DC converters. A voltage-fed converter is a conventional approach for power conversion in a broad range of applications. Limited use of GI CF converters can be explained by their drawbacks, which the VF converters lack, such as the requirement of additional circuits for the inductive voltage overshoots clamping.

Numerous recent studies have focused on the development of the soft-switching CF converter topologies that have led to the development of various clamping techniques using auxiliary networks or circuits as well as clampless solutions. At the same time, there is a limited number of current-fed topologies with bidirectional functionality that preserve soft-switching operation and the same high level of efficiency in both energy transfer directions.

Snubberless voltage clamping methods for the bidirectional CF converters are the topic of current interest. The existing clamping methods were studied and classified. State-of-the-art topologies representing each group of SMCs were compared regarding design complexity and current stresses.

The aim of the doctoral thesis is to study bidirectional soft-switching DC-DC converters that accommodate snubberless clamping methods. Special attention was paid to the development of the topologies with a reduced number of switches. Five novel SMC topologies were proposed, analyzed and experimentally verified.

A universal assessment tool for application-oriented power converter topologies was developed. The assessment tool was used for comparison of all proposed topologies with a reference FB-SMC based on the simulation data. By the results of this comparison, DiPP-SMC and A-SMC topologies were selected for implementation as a front-end converter for the battery energy storage industrial prototype. Experimental data on the industrial prototype performance have proven the reliability of the proposed assessment tool.

This work also has a substantial practical value, as the application-oriented design of the proposed DIPP-SMC and A-SMC topologies for battery energy storage system was carried out and three industrial prototypes were built.

The theoretical and practical results of the work are a substantial contribution in the field of the bidirectional isolated soft-switching DC-DC converters. The proposed assessment tool is not limited to current-fed converters and can be used for a selection of the most suitable power converter topology for a specific application. Practical results obtained by the author show the benefits of the PS-SMCs topologies and increase industrial awareness and attraction of the isolated CF DC-DC converters.

Kokkuvõte

Isoleeritud kahesuunalised voolutoitelised pehmelülituse ja sekundaarmodulatsiooniga alalisvoolumuundurid

Tööstuses kasutatakse kaht erinevat alalispingemuunduri skeemilahendust. Pingetoiteline alalispingemuundur on tavapäraseks lahenduseks suures hulgas praktilistes lahendustes. Voolutoitelisi alalispingemuundureid kasutatakse samas oluliselt vähem. See on seletatav lisanõudmistega voolutoitelistele jõupooljuhtmuunduritele, nagu erilülitused induktiivsuse põhjustatud ülepingete neutraliseerimiseks.

Lähiaastatel on paljud uuringud keskendunud voolutoiteliste jõupooljuhtmuundurite pehmelülitusele, nende summutusahelate parendamisele ning üldse ilma summutusahelateta voolutoiteliste muundurite skeemilahendustele. Samal ajal on väga vähe kahesuunalisi voolutoiteliste muundurite skeemilahendusi, mis kasutaks pehmelülitust ning millel oleks sama kõrge kasutegur mõlemasuunalisel energia ülekandemisel.

Antud doktoritöö põhiliseks uurimisallikaks on summutusahelateta ülepingete mahasurumise meetodid kahesuunalistes voolutoitelistes alalispingemuundurites. Olemasolevaid summutusmeetodeid uuriti ja klassifitseeriti. Igat summutusmeetodit kasutavat kaasaegset skeemilahendust analüüsiti ja võrreldi neid omavahel, lähtudes skeemi keerukusest ja komponentidele langevatest koormustest. Erilist tähelepanu pöörati vähendatud lülituselementide arvuga skeemilahenduste arendamisele. Töös pakuti välja viis erinevat skeemilahendust, mida analüüsiti ning mida prooviti ka katseliselt järgi.

Teoreetiliste uuringute kõrval arendati välja rakenduspõhine metodoloogiline tööriist jõupooljuhtmuundurite skeemilahenduste hindamiseks, mida kasutati kõigi väljapakutud skeemilahenduste simulatsioonipõhisel uurimisel. Uurimistulemuste põhjal valiti DiPP-SMC ja A-SMC skeemilahendused energiasalvesti akut teenindava muunduri tööstuslike prototüüpide aluseks. Prototüüpide katsetamisel saadud info kinnitab arendatud tööriista poolt väljastatud andmete õigsust ja selle kasutatavust.

Doktoritöö praktilist väärtust tõstavad kolm DiPP-SMC ja A-SMC skeemilahenduse põhjal valminud rakenduslikku seadmeprototüüpi.

Antud töö teoreetilised ja praktilised tulemused annavad märgatava panuse kahesuunaliste, isoleeritud ning pehmelülitust kasutavate alalispingemuundurite arengusse. Loodud metodoloogilise tööriista kasutusala ei ole piiratud vaid voolutoiteliste jõupooljuhtmuundurite skeemilahenduste hindamisega vaid on kasutatav kõigile pooljuhtmuunduritele rakenduseks sobivaima skeemilahenduse leidmiseks. Doktoritöö praktilised tulemused näitavad PS-SMC skeemilahenduse eeliseid ning parendavad valmisolekut voolutoiteliste alalispingemuundurite praktiliseks kasutamiseks tööstuses.

Appendix

[PAPER-I] Chub A., Kosenko R., Blinov A., Ivakhno V., Zamaruiev V., Styslo B., Full Soft-Switching Bidirectional Current-Fed DC-DC Converter, 2015 56th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON) (189−194). IEEE.

Full Soft-Switching Bidirectional Current-Fed DC-DC Converter

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***Abstract* – The focus is on a switching control strategy for the galvanically isolated bidirectional current-fed dc-dc converter. The converter under study employs the current-fed full-bridge stage at the low-voltage side and the voltage-fed half-bridge stage at the high-voltage side. The current-fed side of the converter utilizes four-quadrant switches comprised of two MOSFETs each. The switching sequence proposed enables soft-switching operation of all switches in both directions of energy transfer for a wide range of dc voltage gain and load variations. Moreover, it features natural clamping and thus eliminates voltage overshoot at the turn-off of switches at the current-fed side. Full zero-current switching is achieved in the current-fed side, while full zero-voltage switching is accommodated in the voltage-fed side. Theoretical predictions were verified with simulations in PSIM 9.**

***Keywords* – current-fed converter, dc-dc converter, bidirectional converter, soft-switching, ZVS, ZCS.**

I. Introduction

Extensive research in power electronics has been stimulated recently by the rapid penetration of renewable and alternative energy systems, battery storages and electric vehicles (EV) in industrial as well as residential applications [1]. Many energy sources, like fuel cells and batteries, have low-voltage (LV) dc output and thus require galvanically isolated dc-dc converter for interface with the high-voltage (HV) DC link of a utility grid converter or feed typical loads [2]. Voltage-fed (VF) converters were a conventional approach in power electronics for decades. Recent reports have proved that galvanically isolated current-fed (CF) dc-dc converters are a superior solution over VF counterparts for LV high-current energy sources [3], [4]. Another recent trend is towards utilization of soft-switching in dc-dc converters to achieve high power density and low cost [2]. Hence, soft-switching (SS) CF dc-dc converters are an important research topic.

The most obvious drawback of the galvanically isolated CF dc-dc converters is the voltage overshoot at the turn-off of switches caused by mismatch between currents of an input inductor and a leakage inductance of an isolation transformer. First, passive snubbers were used to suppress that voltage overshoot [5]. Further application of active clamping circuits together with properly designed magnetizing inductance have shown a possibility to avoid the voltage overshoot and achieve SS in a wide range of loads [6]. Another possibility to achieve SS and voltage clamping without additional circuits is to use impulse commutation that employs local resonance during switching transients [7], [8]. This approach utilizes parasitic elements for resonance commutation, but it is associated with high peak current stress of the input side switches.

The newest SS techniques for CF dc-dc converters employ an active rectifier at the output side [9]-[11]. All techniques in this group were described for converters with CF switching stage at the input and VF switching stage at the output. Switching sequences of the input and the output sides are synchronized. This enables manipulation of the leakage inductance current to achieve zero-current switching (ZCS) conditions at the input side and zero-voltage switching (ZVS) conditions at the output side with snubber capacitors. In this group of SS techniques, the separated commutation shows only SS transients in all semiconductor components, i.e. full soft-switching (FSS) is achieved along with natural clamping of the CF side [12]-[14]. Another advantage of the separated commutation is minimal energy circulation from the output side to the input side, which is a usual drawback of many SS techniques. Moreover, in separated commutation techniques, the output switches conduct most of the time and thus improve the efficiency. However, it requires utilization of diodes in series with the switches at the CF side to achieve bidirectional voltage blocking feature of the switch.

Utilization of diodes in series with switches results in unidirectional power flow in the converter. Previously, the separated commutation was described for energy transfer from the VF side to the CF side [12], [13], and from the CF to the VF side [14]. The converter with four-quadrant switches at the CF side proposed in [15] (Fig. 1) can utilize the separated commutation to achieve bidirectional power transfer with FSS in both directions. The converter consists of the CF full-bridge

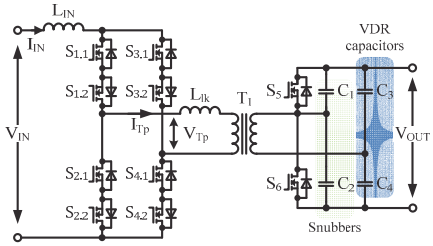

Fig. 1. The bidirectional current-fed dc-dc converter [15].

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inverter at the LV input side, the VF half-bridge inverter with snubber capacitors at the HV output side, which operates as an active voltage doubler rectifier (VDR) in the forward direction. They are coupled by the isolation transformer T_1 with leakage inductance L_{lk}. The FSS CF dc-dc converter is a new promising technology for EVs [16]. It steps up voltage in the forward mode and steps it down in the reverse mode.

The aim of this paper is to present switching control strategy utilizing the separated commutation strategy for both energy transfer directions. Special attention is paid to the delays between control signals of the switches within the four-quadrant switches. Design guidelines for the converter can be used from [12]-[15]. The paper is the first full description of switching control for the full soft-switching galvanically isolated bidirectional current-fed dc-dc converter. Earlier papers have described either partial SS [9] or have overlooked switching control strategy for reverse operation [11].

II. Forward Operation of the Converter

This section describes the operational principle of the converter for energy transfer from the LV CF side to the HV VF side. Idealized voltage and current waveforms with control sequence are shown in Fig. 2 for a single switching period T. Equivalent circuits that describe converter operation for forward energy transfer are shown in Fig. 3. The operation of

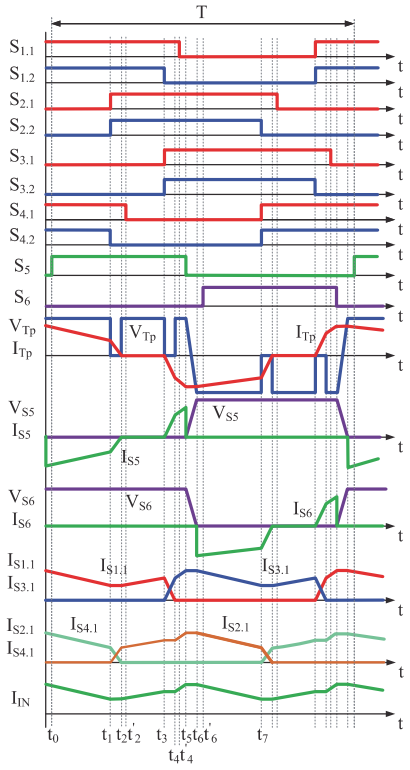

Fig. 2. Operation principle of the converter for the forward energy transfer.

the converter is described further for half of the switching period, since processes during each half of the period are similar. Eleven time intervals and equivalent circuits are used.

Interval 1 ($t < t_0$, Fig. 3*a*). The converter is in active state. The energy is transferred from the input side to the output side. The body diode (BD) of the switch S_5 conducts the transformer current. At instant t_0, S_5 can be turned on at ZVS. Input current is decreasing.

Interval 2 ($t_0 < t < t_1$, Fig. 3*b*). The switch S_5 turns on at ZVS at the instant t_0. The converter is in active state, when the output capacitor C_3 is charging, while C_4 is discharging to feed the load. The input current is still falling – discharge of L_{IN}.

Interval 3 ($t_1 < t < t_2$, Fig. 3*c*). At the beginning of this interval, switches $S_{2.1}$ and $S_{2.2}$ turn on at ZCS, assisted by the leakage inductance, while $S_{4.2}$ turns off. The BD of $S_{4.2}$ conducts the current. The leakage inductance current is decreasing. The input current is redistributing from the four-quadrant (4Q) switch S_4 to S_2. The BD of $S_{4.2}$ is used to prevent sign change of the leakage inductance current. At the instant t_2, this BD of $S_{4.2}$ turns off naturally, and it switches to reverse biased state forced by the output voltage applied to it through the isolation transformer T_1.

Interval 4 ($t_2 < t < t'_2$, Fig. 3*d*). At this interval, transformer current is zero, and the switch $S_{4.1}$ does not conduct any current. At the same time, the BD of $S_{4.2}$ is reverse biased by the output voltage applied through the isolation transformer T_1. Hence, the switch $S_{4.1}$ can be turned off at ZCS, which happens at the instant t'_2. From the instant t_2, the converter is in the shoot-through state, when the input inductor is charging.

Interval 5 ($t'_2 < t < t_3$, Fig. 3*e*). During this time interval, the converter is in the conventional shoot-through state, which duration defines the dc voltage gain in the input side. The 4Q switches S_1, S_2 are short circuiting the front-end inverter, while the output capacitors C_3, C_4 feed the load.

Interval 6 ($t_3 < t < t_4$, Fig. 3*f*). At the beginning of this interval, switches $S_{3.1}$ and $S_{3.2}$ turn on at ZCS, assisted by the leakage inductance, while $S_{1.2}$ turns off. The BD of $S_{1.2}$ conducts the current. The leakage inductance current is increasing up to the I_{IN} instantaneous value. It is reached at the instant t_4, which results in reverse biasing of the BD of $S_{1.2}$. The input current changes slightly during this short interval, and it is redistributed between 4Q switches: from S_1 to S_3. The switch S_5 conducts forward current.

Interval 7 ($t_4 < t < t'_4$, Fig. 3*g*). At this interval, energy is transferred in the reverse direction through the switch S_5, which results in the rise of the input current and the leakage inductance current – charging of the inductances L_{IN} and L_{lk}. The switch $S_{1.1}$ does not conduct any current and thus can be turned off at ZCS, which happens at the instant t'_4.

Interval 8 ($t'_4 < t < t_5$, Fig. 3*h*). It is similar to the previous one. It has to be minimized due to energy circulation from the output to the input side. The interval ends with the turn-off of the switch S_5. It is very short and used to separate switching transients at the input and output sides in time.

Interval 9 ($t_5 < t < t_6$, Fig. 3*i*). The switch S_5 turns off at the instant t_5. This results in recharging of the output snubber capacitors C_1, C_2 with the transformer current from 0 to V_{OUT}

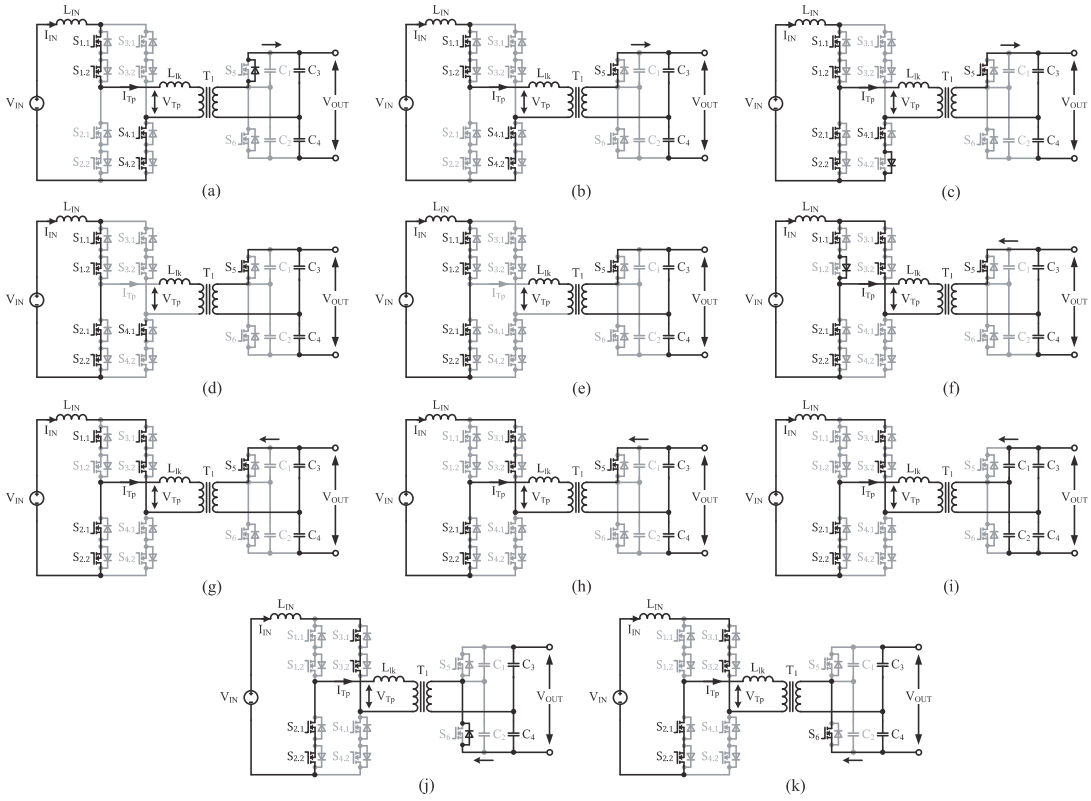

Fig. 3. Equivalent circuits of the converter for the forward energy transfer.

and from V_{OUT} to 0, respectively. At the instant t_6, BD of S_6 starts conducting the transformer current naturally at ZVS.

Interval 10 ($t_6 < t < t'_6$, Fig. 3*j*). The converter switches to the active state at the instant t_6. Energy is transferred from the input side to the output side. Input current is decreasing. Switch S_6 can be turned on at ZVS at any moment after t_6.

Interval 11 ($t'_6 < t < t_7$, Fig. 3*k*). The interval is starting at the instant t'_6 when the switch S_6 is turned on. Active state at this interval is similar to the previous one (interval 10) with a difference at the output side where S_6 conducts current.

III. Reverse Operation of the Converter

Operation of the converter for reverse energy transfer is similar to that in the case of the forward energy transfer. The operating principle is described in Fig. 4. Further description of the operation principle is supported with equivalent circuits shown in Fig. 5. Only half of the switching period T is described as in the previous section. Description of the operation principle is separated into ten time intervals.

Interval 1 ($t < t_0$). The converter is in active state. The equivalent circuit is similar to that in Fig. 3*k* with a difference in the sign of currents due to reverse energy transfer. Also, currents of the CF inverter switches and I_{IN} are negative.

Interval 2 ($t_0 < t < t_1$, Fig. 5*a*). The switch S_6 turns off at ZVS at the instant t_0. This results in recharging of snubber capacitors C_1 and C_2 by the transformer current from V_{OUT} to 0 and from 0 to V_{OUT}, respectively. At the instant t_1, BD of S_5 starts conducting the transformer current naturally at ZVS.

Interval 3 ($t_1 < t < t'_1$, Fig. 5*b*). Energy is circulating from the input (V_{OUT}) to the output (V_{IN}) side. The output current (I_{IN}) remains negative, while its absolute value is decreasing. Switch S_5 can be turned on at ZVS at any moment after t_1.

Interval 4 ($t'_1 < t < t_2$, Fig. 5*c*). The interval is starting at the instant t'_1 when the switch S_5 is turned on. Energy is still circulating from the input to the output side, while the output current (I_{IN}) and the leakage inductance current are decreasing by the absolute value. This interval is very short and used to separate switching transients in the input and output sides.

Interval 5 ($t_2 < t < t_3$, Fig. 5*d*). At first, switches $S_{1.1}$ and $S_{1.2}$ turn on at ZCS, assisted by the leakage inductance, while $S_{3.1}$ turns off. The BD of $S_{3.1}$ conducts the current, until it prevents sign change of that current. The leakage inductance current is decreasing down to zero. Zero level is reached at the instant t_3, which results in reverse biasing of the BD of $S_{3.1}$. The input current changes slightly during this short interval, while it is redistributed between 4Q switches: from S_3 to S_1. The switch S_5 conducts reverse current.

Interval 6 ($t_3 < t < t'_3$, Fig. 5*e*). At this interval, the transformer current is zero, and the switch $S_{3.2}$ does not conduct any current. Hence, it can be turned off at ZCS, which happens at the instant t'_3. From the instant t_3, the converter is in the zero state, when the output inductor (L_{IN}) is discharging, and the BD of $S_{3.1}$ is reverse biased by the output voltage applied through the isolation transformer T_1.

Interval 7 ($t'_3 < t < t_4$, Fig. 5*f*). The converter is in the zero state. The 4Q switches S_1, S_2 are closing the output current loop, allowing the inductor L_{IN} feed the load.

Interval 8 ($t_4 < t < t_5$, Fig. 5*g*). At the beginning of this interval, switches $S_{4.1}$ and $S_{4.2}$ turn on at ZCS, assisted by the leakage inductance, while $S_{2.1}$ turns off. The BD of $S_{2.1}$ conducts the current. The leakage inductance current is increasing by the absolute value. The output current (I_{IN}) is redistributing from the four-quadrant (4Q) switch S_2 to S_4. At the instant t_2, this BD of $S_{2.1}$ of turns off naturally, and it switches to reverse biased state forced by the output voltage applied to it through the isolation transformer T_1.

Interval 9 ($t_5 < t < t'_5$, Fig. 5*h*). Starting from the instant t_5, the switch $S_{2.2}$ does not conduct any current and can be turned off at ZCS. This happens at the instant t'_5. The converter is in active state, when the capacitor C_3 feeds the load through the isolation transformer T_1.

Interval 10 ($t'_5 < t < t_6$, Fig. 5*i*). At this time interval, the converter is in active state. Processes are similar to those of the previous interval. The difference is that the switch $S_{2.2}$ is turned off, which has no influence on the operation.

Figs. 2 and 4 show that the operation of the converter in the forward and reverse modes is quite similar. Both modes maintain FSS and natural clamping. The difference is in the sequence order of the processes. The processes are in reverse order for the reverse energy transfer mode as compared to the switching sequence of the forward energy transfer mode. The duty cycle of all switches is around 0.5. The voltage step-up is performed in the forward more by means of shoot-through

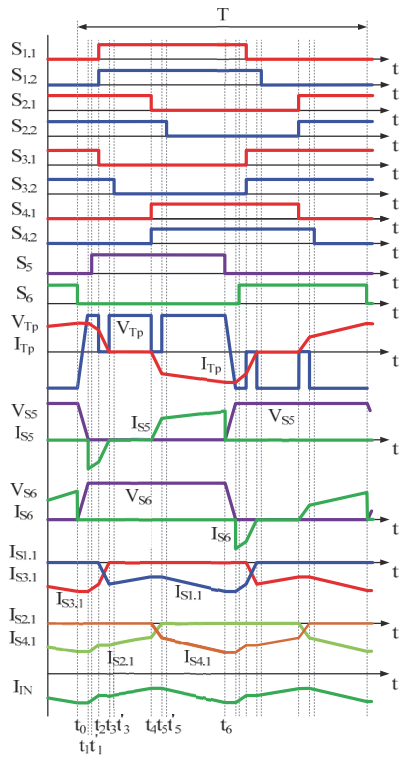

Fig. 4. Operation principle of the converter for the reverse energy transfer.

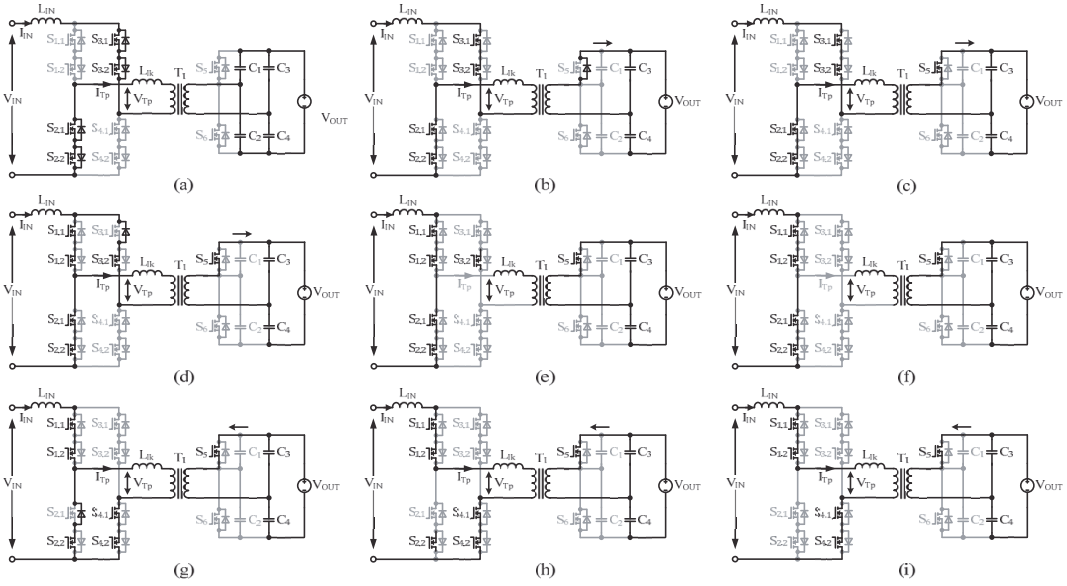

Fig. 5. Equivalent circuits of the converter for the reverse energy transfer.

states of the CF bridge. The shoot-through states are generated using phase shift between control signals of CF top and bottom switches. The phase shift can be leading or lagging.

IV. Simulation Results

Simulation study of the converter was performed in PSIM 9 software. Parameters of the model implemented are shown in Table I. First, the forward operating mode was studied. Voltage and current waveforms obtained (Fig. 6) are consistent with theoretical predictions. The most obvious difference is that the time intervals of SS transients and reverse energy circulation are very short. Hence, some of them are not easy to identify, but they have to be minimized to avoid their parasitic effects. Delay between turn-off instants of the switches within each 4Q switch is also shown.

Simulation parameters were selected to show the operation of the converter with a supercapacitor (SC). The SCs can be used for support of DC bus in DC microgrids and EVs in the case of voltage sag or swell caused by excessive power consumption or generation, respectively. Converters for SCs are a demanding application, since SC can be fully discharged without damage, while the utilization of stored energy is mostly limited by an interface converter [17]. However, SC store only 25% of the rated energy when it is discharged to half of the rated voltage. Hence, tradeoff between converter operation range, i.e. SC energy utilization, and realization cost has to be achieved. Two practical scenarios of interaction between DC bus and SC based energy storage were modeled:

a) In the forward mode, the converter supplies power of 220 W from a charged a SC to support DC bus with nominal voltage of 400 V during voltage sag down to 350 V;

b) In the reverse energy transfer mode, the converter charges slowly a partially discharged SC from the DC bus after its voltage is restored to the nominal level. The converter consumes a power of 50 W from DC bus for slow charging.

Simulation results for the reverse energy transfer (Fig. 7) are also in good agreement with the theoretical predictions.

TABLE I

Parameters Used for Simulation Study

Parameter	Value
L_{IN}	15 µH
Switching frequency	100 kHz
Transformer turns ratio	3.5
C_1, C_2	265 pF
C_3, C_4	1 µF
Forward voltage dc gain	30V/350V
Reverse voltage dc gain	400V/15V
L_{lk}	380 nH

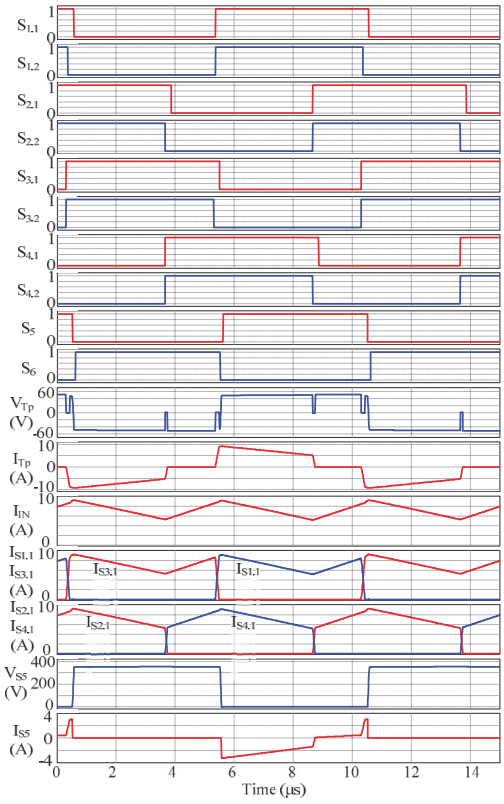

Fig. 6. Simulation waveforms of the converter for the forward energy transfer.

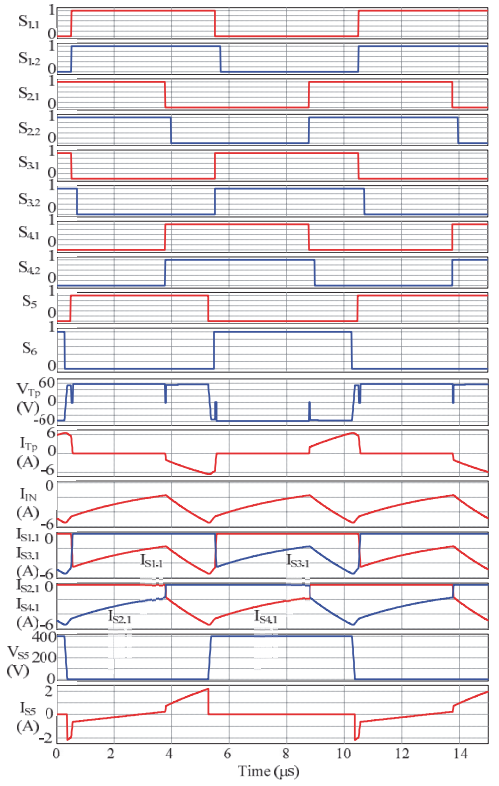

Fig. 7. Simulation waveforms of the converter for the reverse energy transfer.

V. Conclusions

The switching control strategy presented enables full soft-switching with natural clamping in the galvanically isolated bidirectional current-fed dc-dc converter for both energy transfer directions and a wide range of dc voltage gain and load variations. The operation principle and switching sequences were described for both energy transfer directions, not reported before for other similar converters. Our simulation study has justified theoretical predictions. Full ZCS was achieved in the current-fed side, while full ZVS is accommodated in the voltage-fed side. Design guidelines were avoided, since they can be reused from [12]-[15].

Acknowledgements

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Abstract: The study introduces a bidirectional dc–dc converter with current- and voltage-fed (VF) ports that features soft switching in both buck and boost operating modes. The converter can be used for integration of low-voltage DC sources, such as batteries into a dc bus of considerably higher voltage or a dc link of a grid side inverter. Zero current switching, assisted with the leakage inductance of the isolation transformer, can be achieved at the current-fed side along with zero voltage switching of the VF side, assisted by snubber or intrinsic capacitances of the transistors. Soft switching can be maintained over a wide range of voltage and power levels, regardless of the energy transfer direction. Converter operation is described and theoretical findings were verified with experimental results obtained by means of a 300 W prototype operating at a switching frequency of 100 kHz and designed for integration of a 24 V battery into 400 V dc bus. The converter proposed is compared in terms of efficiency to other competing soft-switching full-bridge topologies implemented with the same components.

1 Introduction

Massive introduction of dispersed energy generation systems imposes new challenges of grid stability due to the intermittent nature of the renewable energy sources, which is especially challenging in remote locations [1, 2]. Fuel cell or battery-based energy storage systems (BESSs) is an attractive solution for both residential and commercial applications. They can improve electricity supply security and electricity peak demand shaving, particularly when they are an integral part of a microgrid with a high-level control functionality [3, 4].

Galvanically isolated dc–dc converters with a current-fed (CF) port are a strong competitor for the conventional voltage-fed (VF) converters in low voltage and relatively high current applications, such as photovoltaic, fuel cell or BESS [5–8]. Due to the continuous input current of CF converters, the more efficient operation of such systems could be achieved [9–11]. Moreover, the inherent boost capability allows simplified design requirements of an isolation transformer [12] and wider voltage regulation capabilities [13]. Other advantages include lower RMS current stress of the switches and easily achievable high partial load efficiency [14–17]. Although the VF dc–dc converters received increased attention in the research and industry during the last decades, further improvements and soft switching possibilities for CF converters continue to be addressed [18–20].

Galvanically isolated CF topologies require clamping to avoid voltage overshoot across the semiconductor switches. Some soft-switching CF dc–dc converters utilise passive clamp circuits or diodes in series with inverter switches [19], which causes significant losses in applications of interest with relatively high input currents. Active clamp circuit (ACC) was introduced in [21] for full-bridge converters, together with shifted control method; symmetrical control method was proposed in [22]. The ACC does not only solve the problem of voltage overshoot, but it is also used to create zero voltage switching (ZVS) conditions for main transistor switches. For high step-up applications, half-bridge acting as a voltage doubler rectifier (VDR) circuit was proposed in [23]. The bidirectional full-bridge version was introduced in [24]. By utilising ACC and phase shift control, the converter reaches high peak efficiency in both directions of power flow. Bidirectional configuration with half-bridge voltage source part is introduced in [25] (Fig. 1*a*). It cannot utilise the same phase-shift method; therefore, it is proposed as hard-switched when operating in the buck mode. Partial soft switching by using duty cycle shift (DCS) control [26] together with synchronous rectification (SR) could be applied to improve this situation. On the other hand, the ACC causes the peak current through the CF-side switches and a transformer higher than the input current, which together with circulating capacitor energy results in increased conduction losses [21, 27]. Various methods have been used to address this issue at the cost of the increased component count and complexity [28, 29].

A new snubberless secondary modulation-based (SMB) control method for the half-bridge CF converter was introduced in [30], which was later applied to a family of bidirectional converters [31–33]. The method is based on active clamping by secondary side active switches and allows achieving ZVS of all switches without additional clamping circuits. This algorithm was first applied to a converter with half-bridge at the voltage source side in [34] (Fig. 1*b*). To control the topology effectively, the leakage inductance of the transformer should be precisely dimensioned (possibly by an external inductor). In addition, the topology switches exhibit relatively high peak currents, especially during light load operation [32]. A variation of this method that is based on the resonance effect between leakage inductance and drain-to-source capacitance of the MOSFET is presented in [35]. The method was successfully applied to different bidirectional converters [36, 37]. The main difficulties are associated with component parameter mismatch, non-linearity of practical components, significant oscillations and the need for variable frequency control.

This study introduces a galvanically isolated dc–dc converter utilising four-quadrant switches in the CF side and half-bridge in the VF side with a novel control principle. In contrast to alternatives with half-bridge (acting as a voltage doubler/divider) described above, it features minimised circulating power, low peak current and constant switching frequency with soft switching maintained in both boost and buck modes of operation. The converter operation and switching algorithms in both the buck and the boost modes are described in the next section. Section 3 focuses on various design constraints, gain characteristics and soft-switching conditions and limitations. Section 4 analyses the experimental waveforms and compares characteristics of various topologies.

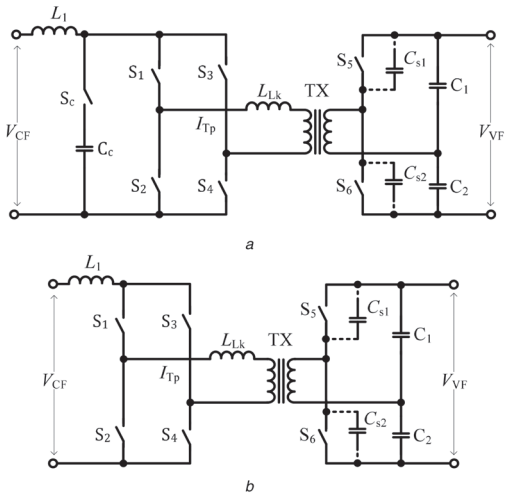

Fig. 1 *Bidirectional dc–dc converter topology*
(a) With an active clamp circuit [25], ***(b)*** Secondary-modulation based [34]

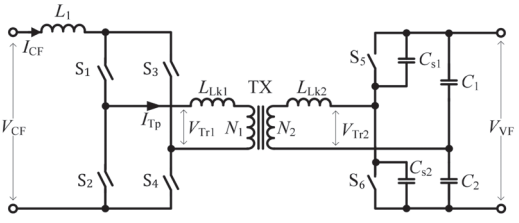

Fig. 2 *Proposed bidirectional dc–dc converter topology*

2 Topology description

Many modern power electronics applications with low voltage sources benefit from the continuous input current at the CF terminal of a converter [9–11]. Therefore, in this study, the CF is considered to operate at much lower voltage than that of the VF terminal. The converter topology in Fig. 2 features CF terminal where a low voltage source V_{CF} can be connected and high-voltage VF terminal V_{VF} coupled by an isolation transformer TX. The full bridge at the CF side is used for this study to demonstrate an increased degree of freedom in switching state selection, allowing lowered energy circulation at the expense of higher component count. In addition, CF full-bridge converters have demonstrated higher efficiency than their half-bridge and push–pull counterparts in similar applications [24]. The half-bridge at the VF side allows the use of filter capacitors with lower voltage ratings and the transformer with lower leakage inductance and twice smaller turns ratio, improving the regulation capabilities. During the operation with the switching control method proposed, the voltage of negative polarity is applied to power semiconductors at the CF terminal; therefore, they need to possess bidirectional voltage blocking capability. For this case study, the four-quadrant switches in the CF side are realised by two MOSFETs in a common source configuration. Depending on the power flow direction, one of these transistors operates in synchronous rectification mode and blocks the current when the negative voltage is applied, thereby the switch features thyristor-like natural commutation. As a result, low circulating power along with soft switching in a wide regulation range is achieved. The bidirectional converter proposed eliminates voltage overshoots typical for CF converters without additional clamping circuits. Therefore, it can be referred to the naturally clamped converter family introduced recently [31, 33, 34].

2.1 Voltage step-up (boost) mode

This section addresses the operating modes and estimation of their durations. In the evaluation, the components are considered lossless and the influence of the transformer magnetising inductance is neglected.

During the step-up mode, the energy is transferred from the CF to the VF terminal. Transistors $S_{1.2}$, $S_{2.2}$, $S_{3.2}$ and $S_{4.2}$ operate as diodes (with SR) and the VF part acts as a synchronous VDR. Generalised waveforms of the converter are presented in Fig. 3. The following intervals could be distinguished during the switching half-period:

t_0-t_1 [t_d]: S_5 turns off, while four-quadrant switches S_2 and S_3 conduct. Snubber capacitors C_{s1} and C_{s2} are recharged (Fig. 4*a*). The voltage polarity of the transformer starts to change its sign and the input inductor and magnetising currents reach the amplitude value when the transformer instantaneous voltage crosses zero. S_1 should be turned off before this instant. The duration of this interval is largely dependent on the value of capacitors $C_{s1} = C_{s2} = C_s$ and the operating power and could be estimated by

$$t_{0-1} = t_d = N \cdot \frac{2 \cdot C_s \cdot V_{VF}}{\left(I_{L1avg} + \Delta i_{L1}/2\right)} \tag{1}$$

where $I_{L1avg} = P_{rated}/V_{CF}$ is the average CF-side current, $P_{rated}$is the converter rated power, Δi_{L1} is the input current ripple, and $N = N_2/N_1$is the transformer turns ratio.

t_1-t_2 [t_a]: The voltage across the transformer reaches the amplitude value and the active state starts. The power is transferred through the switches S_2, S_3 and the body diode of S_6, which could be turned on now to reduce conduction losses (Fig. 4*b*). By the end of this interval, the input current reaches a minimum value. The active state is the controlled parameter that defines the converter gain; the following expression could be used for the first approximation of the required duration:

$$t_{1-2} \simeq t_{a(est)} = N \cdot \frac{V_{CF}}{V_{VF}} \cdot \frac{1}{f_{sw}} \tag{2}$$

t_2-t_3: The shoot-through state is started with the switches $S_{4.1}$ and $S_{4.2}$ being turned on and $S_{2.2}$ turned off. The switch $S_{2.2}$ current is redirecting current into its body diode (Fig. 4*c*). Current redistributes from S_2 to S_4 with di/dt limited by the leakage inductance of the TX referred to N_2. The TX voltage V_{Tr1} drops to zero. The duration of this interval is determined by the circuit parameters and is estimated by

$$t_{2-3} = \frac{1}{N} \cdot \frac{2 \cdot L_{Lkeq2} \cdot \left(I_{L1avg} - \Delta i_{L1}/2\right)}{V_{VF}} \tag{3}$$

where equivalent leakage inductance can be calculated as follows: $L_{Lkeq2} = L_{LK2} + L_{LK1}\,(N_2/N_1)^2$.

t_3-t_4: When the current of $S_{2.2}$ drops to zero, its body diode becomes reverse biased and exhibits reverse recovery and associated voltage overshoot. Reverse recovery losses are minor in practice since they depend on the current slope [38] that is limited by the transformer leakage inductance. The clamping process is finished and the transistor $S_{2.1}$ could be now turned off with zero current switching (ZCS) (Fig. 4*d*). The shoot-through state continues and the energy is being accumulated in the inductor. The duration of this interval is dictated by the duration of the active state.

t_4-t_5: $S_{1.1}$ and $S_{1.2}$ are turned on and $S_{3.2}$ is turned off (Fig. 5*a*). The input current redistributes from S_1 to S_3 with di/dt limited by the leakage inductance of the TX referred to V_{Tr2} and the TX voltage V_{Tr1} drops to zero (in the manner similar to that during the time interval t_2-t_3). The duration is estimated by

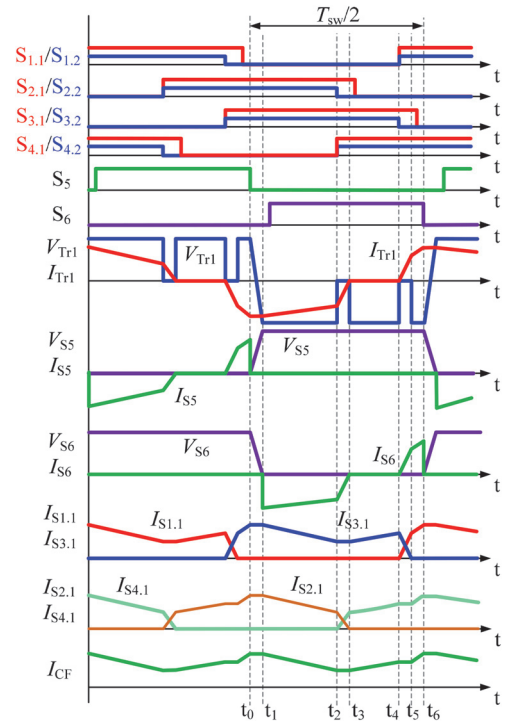

Fig. 3 *Idealised operational waveforms of the converter during the boost mode*

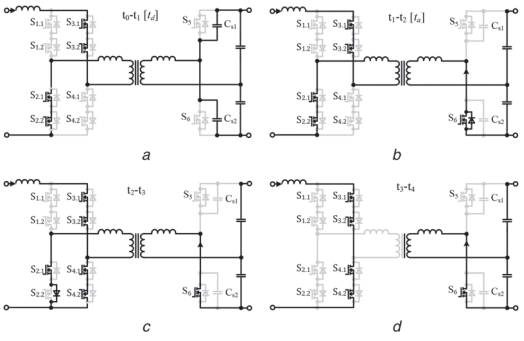

Fig. 4 *Converter switching states in the boost mode of operation (part 1)*

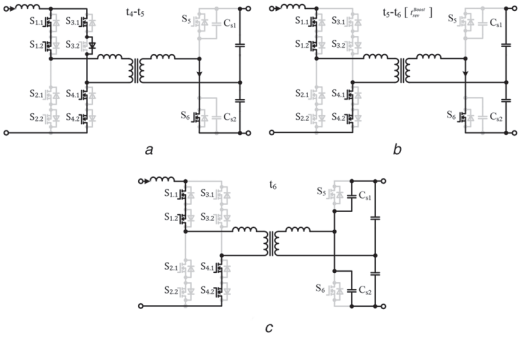

Fig. 5 *Converter switching states in the boost mode of operation (part 2)*

$$t_{4-5} = \frac{1}{N} \cdot \frac{2 \cdot L_{Lkeq2} \cdot (I_{L1avg} + \Delta i_{L1}/2)}{V_{VF}} \quad (4)$$

t_5-t_6 [t_{rev}]: When the current of $S_{3.2}$ drops to zero, it becomes reverse biased and exhibits reverse recovery with small power losses and associated voltage overshoot. The clamping process is finished and the transistor $S_{3.1}$ could be turned off with ZCS (Fig. 5*b*). The shoot-through state is finished and the interval of energy return starts and continues until S_6 is turned off at t_6 (Fig. 5*c*). The duration of this interval (t_{rev}) is a controlled parameter and should generally be minimised in order to reduce energy circulation in the circuit. The interval t_2–t_5 is the resulting duration of the shoot-through state t_s, which determines the gain regulation of the converter. The switching processes then repeat in the similar way for the second half-period.

2.2 Voltage step-down (buck) mode

During this mode of operation, the energy is transferred from the VF to the CF terminal. The top transistors $S_{1.1}$, $S_{2.1}$, $S_{3.1}$ and $S_{4.1}$ operate as diodes (with SR) and the VF part acts as a half-bridge inverter with the duty cycle of transistors close to 0.5. Operational waveforms are presented in Fig. 6. The following intervals could be distinguished during the switching half-period:

t_0-t_1 [t_d]: S_5 turns off while S_1 and S_4 conduct. Snubber capacitors C_{s1} and C_{s2} are recharged (Fig. 7*a*). The voltage polarity of the transformer starts to change its sign and the output inductor and magnetising currents reach the amplitude value when the transformer instantaneous voltage crosses zero. The duration of this interval is largely dependent on the value of the capacitors C_{s1} and C_{s2} and the load.

t_1-t_2 [t_{rev}]: The transformer voltage reaches the amplitude value when the snubber capacitors are recharging. The body diode of S_6 conducts the current and the interval of energy return starts. Transistor S_6 could be turned on (with ZVS) to reduce conduction losses (Fig. 7*b*). The interval (t_{rev}) is a controlled parameter that should be minimised in order to reduce energy circulation in the circuit.

t_2-t_3: $S_{1.1}$ is turned off, while $S_{3.1}$ and $S_{3.2}$ are turned on at t_2 (Fig. 7*c*). The voltage across the inductor drops to V_{CF} and the process of energy return is finished. Current redistributes from S_1 to S_3 with di/dt limited by the leakage inductance of the TX. The TX voltage V_{Tr1} drops to zero as the current starts to freewheel through L_1, S_4, transformer winding N_2 and S_3.

t_3-t_4: When the current of $S_{1.1}$ drops to zero, its body diode becomes reverse biased, the clamping process is finished and the transformer voltage rises to the amplitude value. $S_{1.2}$ could be turned off with ZCS (Fig. 7*d*). The freewheeling state continues and the inductor maintains the current in the CF side.

t_4-t_5: The end of the freewheeling interval is initialised by the turn off of $S_{4.1}$ and turn on of $S_{2.1}$ with $S_{2.2}$ (Fig. 8*a*). The current starts to redistribute from S_4 to S_2, limited by the leakage inductance of the TX and the transformer voltage V_{Tr1} drops to zero.

t_5-t_6 [t_a]: When the current of $S_{4.1}$ drops to zero, its body diode becomes reverse biased and the freewheeling state is finished. The transformer voltage rises to the amplitude value and $S_{4.2}$ could be turned off with ZCS (Fig. 8*b*). The converter operates in the active state and the power is delivered through semiconductor switches S_2, S_3 and S_6. This state continues until S_6 is turned off (Fig. 8*c*) and after that the processes repeat in a similar way for the second half-period.

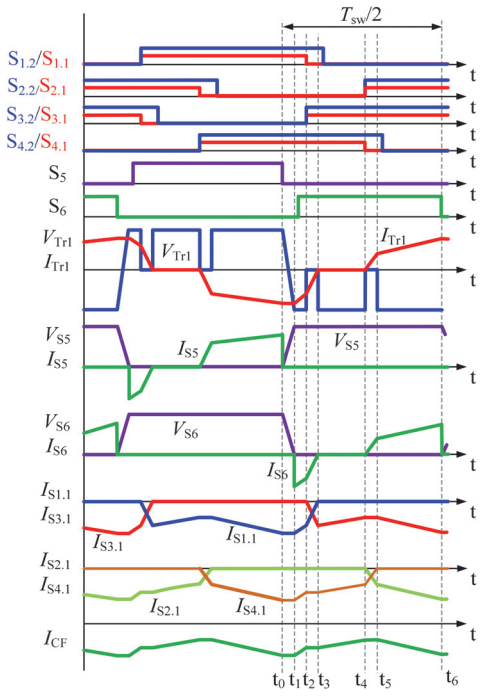

Fig. 6 *Idealised operational waveforms of the converter during the voltage step-down mode*

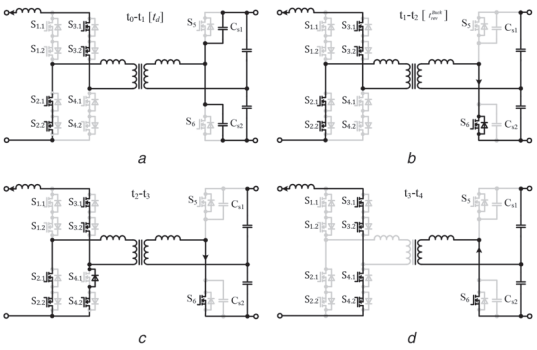

Fig. 7 *Converter switching states in the buck mode of operation (part 1)*

3 Estimation of the operating parameters

3.1 Voltage step-up (boost) mode

The converter could provide a reliable soft-switching operation assuming that the switching parameters take into account critical operating points. The first of such parameters is the maximum duty cycle of the VF-side transistors. The equivalent parallel capacitance of these switches has to be recharged to ensure ZVS, which reduces the maximum allowable duty cycle. To estimate the $D_{VF(max)}$, the interval t_d (1) has to be considered

$$D_{VF(max)} = \frac{1}{2} - t_d \cdot f_{sw} \tag{5}$$

In the general form, the maximum duty cycle of the VF-side transistors could be expressed as

$$D_{VF(max)} = \frac{1}{2} - N \cdot \frac{2 \cdot C_s \cdot V_{VF} \cdot f_{sw}}{(I_{L1avg} + \Delta i_{L1}/2)} \tag{6}$$

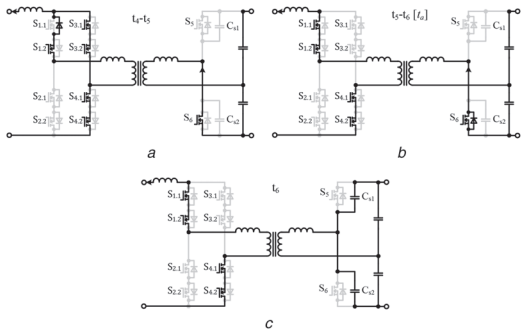

Fig. 8 *Converter switching states in the buck mode of operation (part 2)*

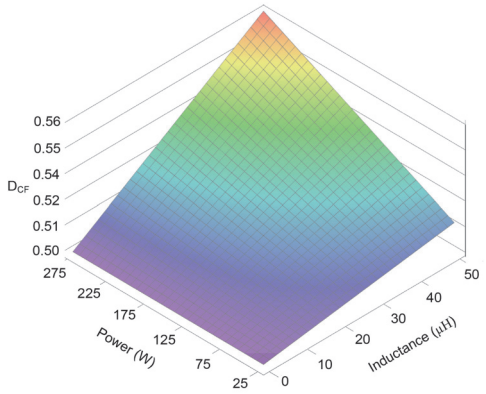

Fig. 9 *Minimum required duty cycle for CF-side switches for different power and L_{Lkeqs} values (V_{CF} = 24 V, V_{VF} = 400 V, N = 6, L_1 = 45 μH f_{sw} = 100 kHz)*

where C_s is the equivalent capacitance of the VF-side transistor.

Another parameter that has to be taken into account is the minimum duty cycle of top low voltage switches $S_{1.1}$, …, $S_{4.1}$, which has to be always slightly higher than 0.5 to allow the current redistribution between opposite CF bridge arms with di/dt limited by the transformer leakage inductance. The interval $t_{4\text{-}5}$ (4) has to be considered to estimate the resulting $D_{CF(min)}$

$$D_{CF(min)} = \frac{1}{2} + t_{4-5} \cdot f_{sw} \tag{7}$$

In the general form, the minimum duty cycle of CF switches could be estimated by

$$D_{CF(min)} = 0.5 + \frac{1}{N} \cdot \frac{L_{Lkeq2} \cdot (V_{CF}^2 + 8 \cdot L_1 \cdot P_{rated} \cdot f_{sw})}{4 \cdot L_1 \cdot V_{CF} \cdot V_{VF}} \tag{8}$$

The example of dependencies plotted in Figs. 9 and 10 shows that the critical point for VF switches occurs at low load and high equivalent capacitance, while for CF switches, at high load and equivalent inductance. These tendencies will be maintained in systems with other specifications.

The third parameter to be determined is the minimum phase shift value D_{offset} between the switching of the CF and VF sides. In the boost mode, it depends on the duration of the interval $t_{4\text{-}5}$ (4) (phase shift value between control signals of the CF and VF sides) and can be estimated after choosing actual operating values of D_{CF} and D_{VF} by

$$D_{offset}^{Boost} \geq D_{CF(min)} - \frac{D_{VF} + D_{CF}}{2} \tag{9}$$

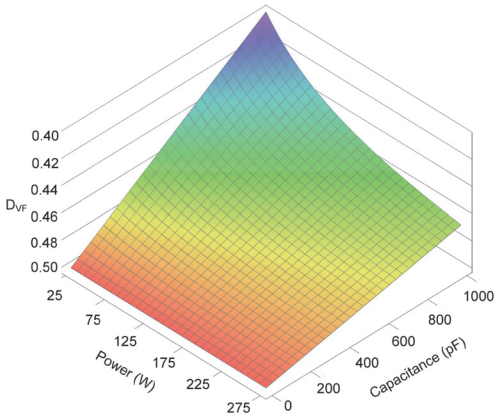

Fig. 10 *Maximum allowed duty cycle for VF-side switches for different power and C_s values (V_{CF} = 24 V, V_{VF} = 400 V, N = 6, f_{sw} = 100 kHz)*

where D_{VF} and D_{CF} are the chosen values of duty cycles that correspond to the conditions from (6) and (8). D_{offset} can significantly influence the gain factor of the converter since together with $D_{CF(min)}$ it affects the resulting interval of the energy return ($t_{5\text{-}6}$):

$$t_{5-6} = t_{rev}^{Boost} = \frac{1}{f_{sw}} \cdot \left(\frac{D_{VF} - D_{CF}}{2} + D_{CF} - D_{CF(min)} + D_{offset}^{Boost} \right) \quad (10)$$

The duration of the converter active state t_a could be estimated by considering the volt-second balance of the input inductor, which (neglecting the influence of leakage inductance) could be described as follows:

$$\begin{aligned} &(V_{CF} - V_{Tr1}) \cdot t_a + V_{CF} \cdot \left(\frac{1}{2f_{sw}} - t_{rev} - t_d - t_a \right) \\ &+ (V_{CF} + V_{Tr1}) \cdot t_{rev} = 0 \end{aligned} \quad (11)$$

Assuming that $V_{Tr1} = V_{VF}/2N$, the t_a could be then expressed in a general form by the following equation:

$$\begin{aligned} t_a &= \frac{2\left[t_{rev} \cdot \left(V_{CF} + \frac{NV_{VF}}{2} \right) - V_{CF} \cdot \left(t_d + t_{rev} - \frac{1}{2f_{sw}} \right) \right]}{V_{VF}} \\ &= t_{rev} + \frac{NV_{CF} \cdot (1 - 2f_{sw} \cdot t_d)}{V_{VF} \cdot f_{sw}} \end{aligned} \quad (12)$$

The resulting converter gain could be calculated from

$$G_{CF} = N \cdot \frac{2}{D_a - D_{rev}^{Boost}} \quad (13)$$

Assuming that $t_a = T_{sw}/2 - (t_s + t_{rev} + t_d)$, converter gain could be expressed as

$$G_{CF} = N \cdot \frac{2}{1 - D_s - D_d - 2 \cdot D_{rev}^{Boost}} \quad (14)$$

where $D_s = 2t_s/T_{sw}$ is the duration of shoot-through state, $D_d = 2t_d/T_{sw}$ and $D_{rev} = 2t_{rev}/T_{sw}$.

The theoretical values of normalised gain (G_{CF}) obtained from (14) are presented in Fig. 11. As shown, the parameter D_{rev} could be potentially utilised for the adjustment of the gain factor. In the practical circuit, the converter will have a minimum normalised gain higher than two (due to VDR), which is determined by the

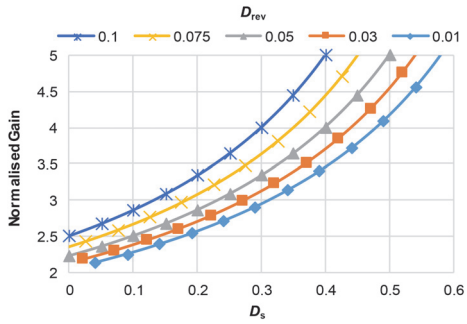

Fig. 11 *Theoretical voltage gain for a converter operating in the voltage step-up mode*

leakage inductance of the transformer, the equivalent capacitance of the VF-side switches and the operating frequency.

3.2 Voltage step-down (buck) mode

The CF-side inductance value considering the continuous conduction mode and $L = V \cdot dt/di$ could be approximated as

$$L_1 \geq \frac{t_{a(est)} \cdot V_{CF}^2}{P_{rated} \cdot k_L} \cdot \left[\frac{1}{2 \cdot f_{sw} \cdot t_{a(est)}} - 1 \right] \quad (15)$$

where $t_{a(est)}$ is derived from (2), k_L is the relative input current ripple and P_{rated} is the rated power of the converter.

The capacitance of VF-side capacitors (considering $C = i \cdot dt/dv$) can be estimated as follows:

$$C_{1,2} = \frac{P_{rated}}{2 \cdot V_{VF}^2 \cdot f_{sw} \cdot k_V} \quad (16)$$

where k_V is the relative voltage ripple of the voltage V_{VF} (in the case of the stand-alone system).

Unlike the boost mode, the minimum phase shift value between the switching of CF and VF sides is influenced by t_d (1) and, as a result, by the $D_{VF(max)}$ (6) value

$$D_{offset}^{Buck} \geq \frac{D_{CF} + D_{VF}}{2} - D_{VF(max)} \quad (17)$$

The resulting interval of energy return in the buck mode can be obtained from

$$\begin{aligned} t_{rev}^{Buck} &= t_{1-2} = \frac{1}{f_{sw}} \cdot \left(\frac{1 - D_{CF} - D_{VF}}{2} + D_{offset}^{Buck} \right) - t_d \\ &= \frac{2 \cdot \left(D_{offset}^{Buck} + D_{VF(max)} \right) - D_{CF} - D_{VF}}{2 \cdot f_{sw}} \end{aligned} \quad (18)$$

The converter gain in the buck mode is estimated from

$$\begin{aligned} G_{VF} &= \frac{1}{2 \cdot N} \cdot \left(D_a - D_{rev}^{Buck} \right) = \frac{1}{2 \cdot N} \cdot \\ &\left(1 - D_s - D_d - 2 \cdot D_{rev}^{Buck} \right) \end{aligned} \quad (19)$$

where $D_{rev}^{Buck} = 2t_{rev}^{Buck}/T_{sw}$.

As shown in Fig. 12, the gain characteristic in this mode is linear but different from that of the voltage step-up mode. The converter gain is controlled by adjusting the relative durations D_{rev} and D_s. This can be achieved easily by varying the phase shift between switches S_2 and S_4 relative to other topology switches, as presented in Fig. 13.

The resulting characterisation of soft-switching limits of the case study converter based on (6) and (8) is presented in Fig. 14.

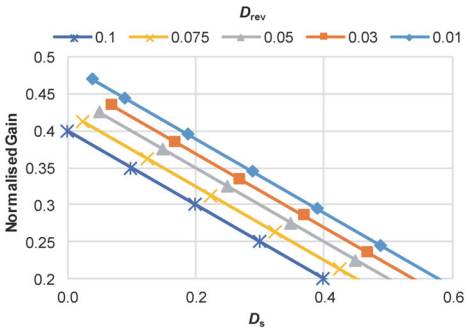

Fig. 12 *Theoretical voltage gain for a converter operating in the voltage step-down mode*

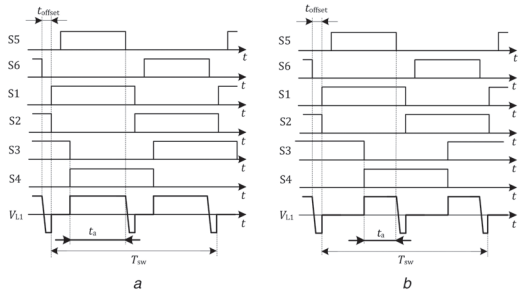

Fig. 13 *Generalised control signals at*
(a) Maximum and, ***(b)*** Minimum active state duration

Evidently, the soft-switching range could be adjusted by varying switch duty cycles. At the same time, a very wide soft-switching area chosen will lead to decreased converter regulation capabilities and performance (assuming constant duty cycles) at other operating points. As long as design constraints described in (6), (8) and (9) or (17) are met, the converter will operate under soft-switching conditions without additional adjustments. Hence, the duty cycles should be selected such that a range defined by converter operating limits is within soft-switching area highlighted in Fig. 14. Based on the depicted characteristics, it can be observed that $D_{CF} = 0.54$ and $D_{VF} = 0.47$ are sufficient to provide soft-switching operation for 20–30 V input voltage and 50–350 W power range. The converter designed for soft-switching operation should not work below the minimum power P_{min}. Therefore, seamless transition between boost and buck modes should be avoided to maintain operating conditions of semiconductors within design limits and avoid discontinuous conduction mode. However, this peculiarity does not limit the converter application in dc microgrids, where dc bus signalling approach [39] is used for autonomous operation and energy sources are expected to operate with dead-zone regarding the dc bus voltage [40].

4 Experimental verification and analysis

This section presents the following: experimental verification of feasibility of the soft-switching method proposed, verification of theoretical dc voltage gain characteristics, performance assessment of the converter proposed in low-voltage energy storage applications, comparison of the converter proposed with competing soft-switching CF full-bridge topologies using the same magnetic and semiconductor components.

A 300 W prototype (Fig. 15) was assembled to study the feasibility of the soft-switching method and assess the performance of the topology. The parameters of the converter are listed in Table 1. The isolation transformer and CF side inductor were produced utilising conventional approaches for low cost manufacturing. This design enables performance verification with moderate leakage inductance, common for industrial designs.

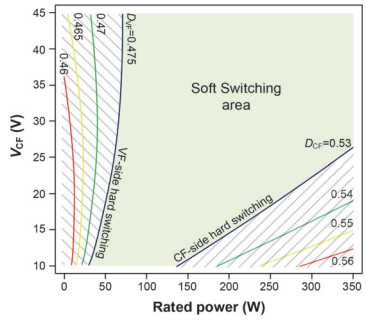

Fig. 14 *Soft-switching limits of the proposed converter values (V_{CF} = 24 V, V_{VF} = 400 V, C_s = 270 pF, N = 6, L_{Lkeqs} = 25 μH, f_{sw} = 100 kHz)*

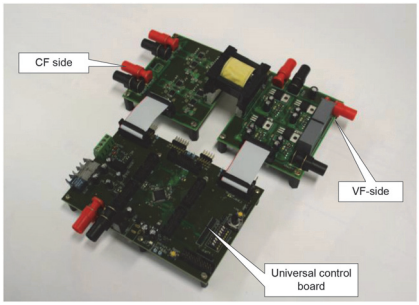

Fig. 15 *Photo of the prototype converter*

Table 1 Parameters and components of the prototype

Parameter	Symbol	Value
CF-side voltage	V_{CF}	20–30 VDC
VF-side voltage	V_{VF}	400 VDC
switching frequency	f_{sw}	100 kHz
CF-side inductor	L_1	30 μH/13 turnsRM14/3C95
VF-side capacitors	C_1, C_2	2 μF
transformer turns ratio	N_2/N_1	48:8/ETD34/3C95
equivalent TX leakage inductance	L_{lkeq2}	22 μH
rated power	P_{rated}	300 W
CF transistors	S_1–S_4	FDMS86181
VF transistors	S_5, S_6	STP18N60DM2
microcontroller		STM32F334R8T6
CF transistor drivers		ADUM3221
VF transistor drivers		ACPL-P346

Transformer optimisation can decrease leakage inductance considerably [41, 42], which, however, could result in increased engineering and production costs. Ten independent PWM channels were used to control the topology. Since CF-side switch pairs are in a common-source configuration, only one isolated power supply and one dual-channel driver chip could be applied to provide driving signals for two transistors that form the four-quanrant switch. The total power consumed by the auxiliary circuits at 100 kHz was around 2.7 W.

The converter operation was tested in both directions of the power flow. Similar to other CF converters, the start-up process with a discharged output capacitor in the boost mode requires limitation of the inrush current. Typical measures to solve this problem can potentially be applied [43, 44]. The start-up process is not emphasised in this research since it is assumed that the capacitors C_1 and C_2 at the VF terminal of the converter are connected to pre-charged dc link or dc bus. The experimental

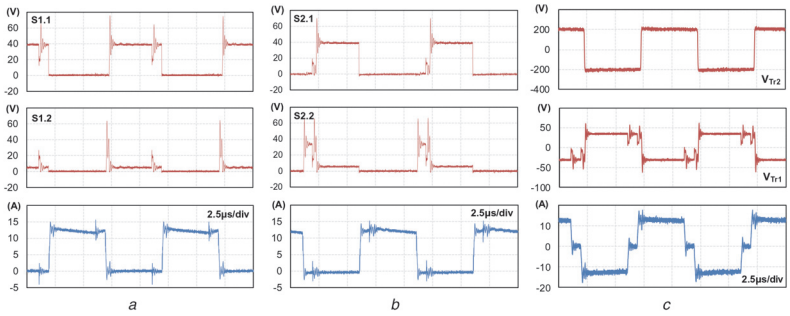

Fig. 16 *Experimental switching waveforms in the voltage step-up mode of*
(a) Transistors $S_{1.1}$ and $S_{1.2}$; ***(b)*** $S_{2.1}$ and $S_{2.2}$; ***(c)*** Transformer TX

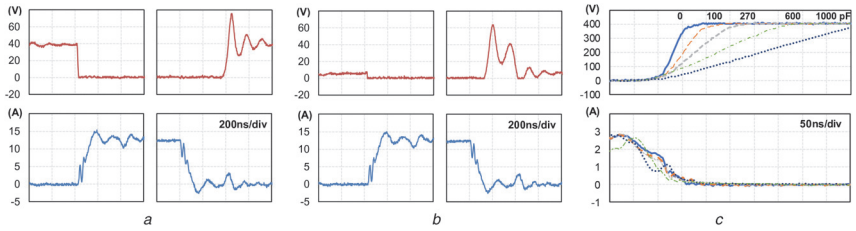

Fig. 17 *Experimental transient waveform showing*
(a) Turn-on and ZCS of transistor S1.1; ***(b)*** Reverse bias of the $S_{1.2}$ body diode; and ***(c)*** Turn-off waveforms of S5 with various snubber capacitors

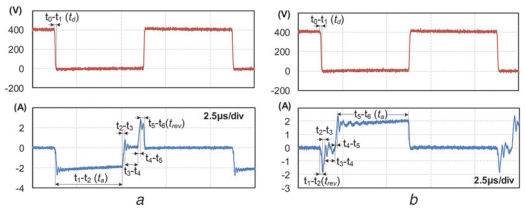

Fig. 18 *Experimental switching waveforms of transistor S_5 with corresponding operating intervals shown:*
(a) Voltage step-up mode and ***(b)*** Voltage step-down mode

waveforms showing the steady-state operation are presented in Figs. 16–18. As it could be observed in Fig. 18, the operation of the converter in the voltage step-down mode is similar to that in the voltage step-up mode. In both modes, the magnetising current is low and has a minor influence on the processes in the converter. The observed voltage overshoots in the current-source transistors generated during the reverse recovery process of the body diodes result in remarkable voltages across the devices but cause no second order effects, such as an avalanche or a dynamic turn on. These overshoots could be reduced by PCB layout optimisation or application of small RC or RCD snubbers across the power semiconductor switches, minimisation of conduction time of the MOSFET body diode and further circuit and layout improvements [45]. Such voltage spikes caused by the reverse recovery process are typical and frequently observed in soft-switching CF converters presented recently [32, 46, 47]. Moreover, no signal filtering was used during measurements by means of isolated differential voltage probes and Rogowski coil-based current sensors that are known for exaggerating oscillations of the measured signals due to capacitive coupling, probe induced ground loops and common mode currents [48, 49]. During the experiments, the voltage spikes were tolerable and no extra damping circuits were used.

As shown in Figs. 17*a* and *b*, the experimental results are in agreement with the estimations and demonstrate the ZCS turn-off of the CF-side switches. The ZVS turn-on of the VF-side transistor is depicted in Fig. 18. Turn-off waveforms of S_5 with various snubber capacitances (Fig. 17*c*) demonstrate the reduction of dv/dt from 7.5 V/ns without external snubber to 1 V/ns with 1 nF snubber. The turn-off energy, in this case, was reduced from 5 to 1.5 μJ, resulting in negligible overall semiconductor switching losses in the topology.

The characteristics and performance of the converter proposed were compared quantitatively and qualitatively with alternative CF topologies operating at a constant switching frequency (see Table 2). As compared to other converters, the proposed topology features the least transistor peak current stress and requirements on the isolation transformer VA rating. The competing converters were assembled using the same magnetic and semiconductor components as the converter proposed to an achieve objective comparison (Table 1). The capacitor for the active clamp converter was chosen according to [27]. During the buck operation mode, both active clamp and SMB-HB [34] were assumed to operate as a DCS converter with SR. The efficiencies were measured with Yokogawa WT1800 power analyser and the results are summarised in Fig. 19. The obtained efficiency values of the competing topologies are comparable or higher than those reported in the previously published papers, where they were in the range of 89–94% [13, 31–33, 47, 50–52] for CF converters and 86–93% for the VF DAB-based converter in [53]. As can be observed, the efficiency of SMB-HB and active-clamp converter drops significantly at light load operation in the step-up mode, while the case study topology features high efficiencies at a wide load range. In contrast to the competitors, during the step-up mode, the proposed converter reached a higher power stage efficiency at most operating points (up to 95.9%). Nevertheless, at full power, the SMB-HB converter operates close to its nominal operating point

Table 2 Qualitative and quantitative comparison of competing topologies (V_{CF} = 20 V, V_{VF} = 400 V, P_{rated} = 300 W f_{sw} = 100 kHz)

Parameter	Topologies			
	VF DAB [63]	Active clamp [25]	SMB-HB [34]	Proposed (Fig. 2)
voltage conversion type	step-down		step-up	
transformer turns ratio N_2/N_1	16		6	
LV side filtering and aux. passive components	bulky capacitor	bulky inductor and aux. capacitor	bulky inductor	bulky inductor
LV side transformer peak and (RMS) current, A	27.4 (20.2)	23.2 (12.7)	48.6 (21.5)	15.9 (12.9)
transformer minimum VA rating	610	500	730	440
number of LV side switches	4	5	4	8
steady-state voltage stress of LV transistors, V	30	39	34	34
LV transistor peak and (RMS) current, A	27.4 (14.3)	23.2 (10.2)	32.2 (13.2)	15.9 (10.6)
clamp transistor peak and (RMS) current, A	N/A[a]	8.8 (4.1)	N/A	N/A
cumulative VA rating of LV side switches, p.u.	1.00	1.12	1.05	1.68
soft switching in LV side switches	ZVS turn-on/off	ZVS turn-on, hard turn-off at lower current	snubbered ZVS/ZCS turn-on/off (with small reverse recovery losses)	
number of HV side switches	4		2	
voltage stress of HV side switches, V	400			
HV transistor peak and (RMS) current, A	1.89 (0.96)	3.9 (1.5)	8 (2.5)	3 (1.6)
cumulative VA rating of HV side switches	1.00	0.79	1.30	0.83
soft switching in HV side switches	ZVS turn-on/off	synchronous rectification	ZVS turn-on, snubbered turn-off	ZVS turn-on, snubbered turn-off
relative total VA semiconductor rating, p.u.	1.00	0.96	1.17	1.28
number of gate driver power supplies	6	6	5	6
number of low-side driver ICs (channels)	6: 4 × 1-channel and 2 × 2-channel	6: 5 × 1-channel and 1 × 2-channel	5: 4 × 1-channel and 1 × 2-channel	6: 2 × 1-channel and 4 × 2-channel
circulating power	high	low	high	low
transformer series inductance	high (external)	low (integrated)	high (external)	low (integrated)
range of soft switching	limited at light loads		wide (load adaptive)	

[a]N/A – not applicable.

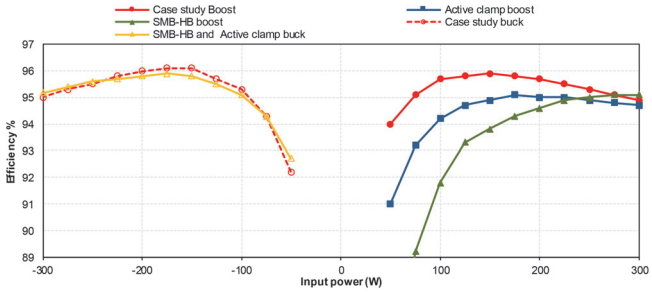

Fig. 19 *Experimental power stage efficiencies of converter topologies: case study, active clamped [25], SMB-HB [34] (V_{VF} = 400 V, V_{CF} = 28 V)*

with minimal energy circulation and surpasses the case study converter in efficiency thanks to its reduced number of CF-side switches.

The characteristics of the analysed converters in the step-down mode are comparable at most power levels. The case study converter features higher partial load efficiency, while at minimal and maximal loads, it is slightly lower. Fig. 20 presents the converter efficiency with varying V_{CF} (20–30 V), which is a typical voltage range for lithium iron phosphate (LFP) batteries that are becoming popular in energy storage applications [54, 55].

The power loss breakdown shown in Fig. 21 was estimated by typical analytical approaches using datasheet characteristics and open- and short-circuit tests of the transformer [56]. The experimentally obtained efficiency was used to define the total loss of 15.3 W. It could be observed that losses in semiconductors account for 28% of the total power loss. At the same time, the majority (around 60%) of losses come from power dissipation in magnetic components, which shows the path for further efficiency improvement. The comparison of analytical voltage gain characteristics derived in Section 3 with experimental values in both buck and boost modes is presented in Fig. 22. As shown, experimental results are in agreement with the theoretical estimations.

Realisation of bidirectional capability for the CF switches presently requires a connection of at least two commercial devices, which has a negative impact on the converter silicon utilisation and cost. From Table 2, it follows that the proposed converter requires 28% more VA switch rating than the DAB converter. The full potential of the topology and control method can be realised by applying discrete bidirectional switches. Samples of such devices are manufactured and reported for Si [57, 58], SiC [59, 60] and GaN [61, 62] semiconductor technologies.

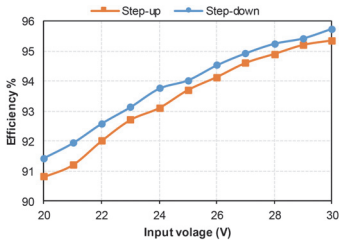

Fig. 20 *Efficiency of the case study converter power stage at different CF-side voltage levels*

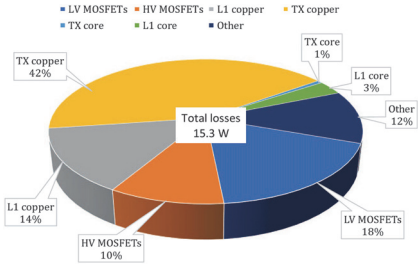

Fig. 21 *Power loss (P_{total} = 15.3 W) breakdown at V_{VF} = 400 V, V_{CF} = 28 V, P_{input} = 300 W*

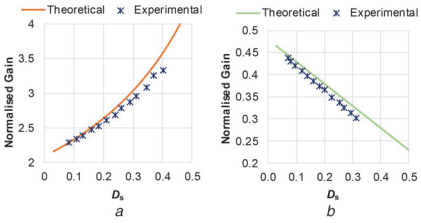

Fig. 22 *Theoretical and experimental voltage gain for a converter operating in the*
(a) Voltage step-up mode; and ***(b)*** Voltage step-down mode

5 Conclusions

This paper introduces a bidirectional current-fed dc–dc converter that features soft switching in both the voltage step-up and step-down operating modes. The switching control method, steady-state analysis and design aspects of the converter are presented. The prototype converter with a rated power of 300 W was assembled and tested considering future application to residential battery energy storages. The experimental test results prove feasibility of the soft-switching method in the proposed converter. Stable soft-switching operation is maintained with a wide variation of the CF-side voltage and power levels; moreover, the current stress on the switches never exceeds the input current. Throughout the operation, low circulating power and constant switching frequency was maintained. Peak power stage efficiency of 95.9% in the boost mode and 96.2% in the buck mode were achieved for the power stage of the prototype converter utilising cost-optimised magnetic components that contribute majority of power losses, while the CF switches correspond to only 18%, regardless their increased number. Minimisation of turn-off losses at the voltage-fed side by use of capacitive snubbers was shown. Furthermore, it was demonstrated that unlike other bidirectional topologies with CF terminal, the efficiency of the converter proposed does not strongly depend on the energy transfer direction. Experimental efficiency evaluation was performed for the converter proposed and existing competitive soft-switching current-fed topologies using the same set of industry manufactured magnetic components and generic off the shelf Si semiconductor components. The results obtained prove better performance of the proposed concept in low voltage applications. Given the realisation method of four-quadrant switches, the obvious disadvantage of the topology is a high VA rating and number of commercial transistors required, resulting in low silicon utilisation. This, however, does not result in a dramatic increase of cost of driving circuits, since four-quadrant switches feature transistors in common source configuration and enable use of a single isolated power supply and two-channel low-side driver per four-quadrant switch. The approach introduced could be considered as an alternative that enables relaxed cooling requirements for systems where low power losses at a wide power range are desired for both directions of power flow.

6 Acknowledgment

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Full Soft-Switching High Step-Up Current-Fed DC-DC Converters with Reduced Conduction Losses

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***Abstract*— Two variants of the full soft-switching high step-up DC-DC converter are proposed. The main advantage of the converters is the minimized conduction losses by the use of the four-quadrant switches and a specific control algorithm. Simulation was performed to verify the principle of operation and to estimate the losses.**

***Keywords*— DC-DC power converters, photovoltaic systems, soft switching, step-up, isolated**

I. Introduction

The concept of the full soft-switching high step-up current-fed DC-DC converter (Fig. 1) is discussed and verified in different works [1]-[6]. The main advantage of these converter topologies is the soft-switching operation of all transistors: Zero-Current Switching (ZCS) in the input side and Zero-Voltage Switching (ZVS) in the output side. This places it in line with the resonant converters but without their typical disadvantages: additional passive elements, varying switching frequency, and considerable circulating power. The main drawback of this converter topology lies in the additional conduction losses caused by series diodes in the front-end inverter stage. In the low-voltage applications with relatively high current, the input conduction losses exceed all other losses of the converter and significantly limit its maximum efficiency [1]. These diodes are needed to achieve soft-switching of inverter switches by limiting energy flow between the inverter and the rectifier during shoot-through states [2]. So the originally proposed topology is not well suited for low-voltage applications, particularly for solar photovoltaic.

There are many different approaches to minimize switching losses in current-fed topologies [7]-[9], but most of them require additional switches or passive elements. A soft-switching snubberless naturally clamped current-fed full-bridge converter is presented in [10]. Snubber capacitors play a key role in that topology. At the same time, full soft-switching operation is not the case in this topology, since the transistors on the primary side have hard turn-on due to discharging of the snubber capacitors through transistors.

The main goal of this paper is to present two different approaches to minimize conduction losses in soft-switching high step-up current-fed DC-DC converter [1] while maintaining soft-switching of all power switches. Proposed topologies are analyzed in terms of efficiency and control strategies.

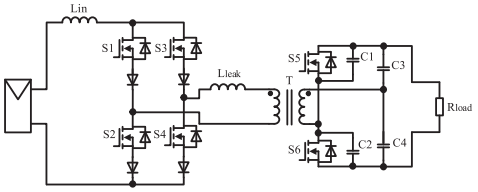

Fig. 1. Full soft-switching high step-up DC-DC converter

II. Losses Reduction Approaches

One of the approaches to overcome this drawback is reported in [11]; it uses the resonant network and varying switching frequency. Another approach that requires no additional passive components and has stable switching frequency is to replace the diodes by active switches.

A. Implementation with Four Four-Quadrant Switches

The most obvious solution to minimize conduction losses is to replace diodes with the fully-controlled switches, i.e., reverse-blocking switches in the inverter stage are replaced by the four-quadrant switches (Fig. 2). However, such approach has the drawback of a higher cost and control circuit complexity.

Figs. 3 shows the switching states of the proposed topology, the solid black lines indicates current path while the gray one indicates inactive parts of the circuit. Fig. 4 shows idealized voltage and current waveforms. During the switching period, the operation of the converter is symmetrical and thus only one-half of it will be discussed.

At the moment t_0, switches S1.1, S1.2, S4.1, S4.2, S5 are conducting, C2 is discharged, while C1 is charged to V_{Ts}. The switching half-period includes the following intervals:

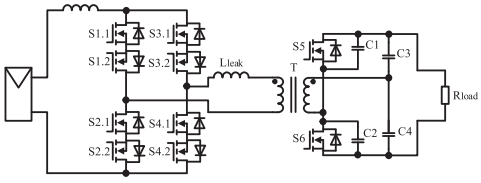

Fig. 2. Proposed converter topology with four four-quadrant switches.

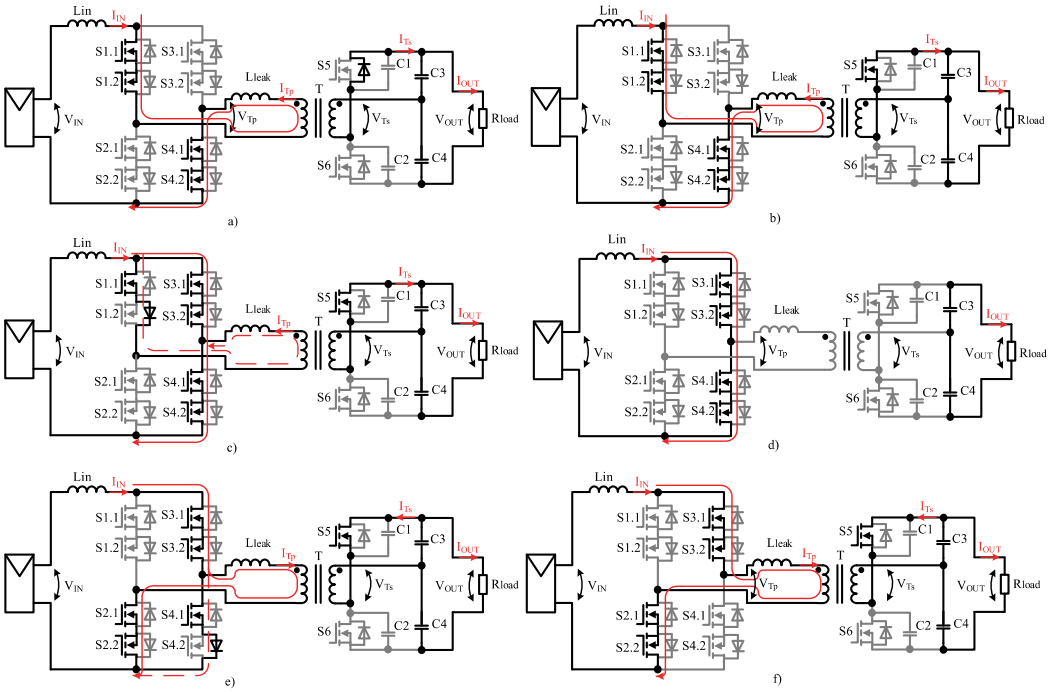

Fig. 3. Switching states of the proposed converter topology with four four-quadrant switches.

a) Switch S2.2 can be turned off at ZCS. S6 is turned off, C2 is charging to V_{OUT} with I_{Ts} and C1 is discharging, snubber soft turn-off of the switch S6 occurs. When the voltage across C2 reaches V_{Ts} and C1 is fully discharged, the freewheeling diode of S5 opens, starting the energy transfer to the load. This process is characterized by conduction losses in the freewheeling diode. Duration of this interval must be longer than the capacitor recharge interval to ensure that all transient processes on snubber capacitors are finished.

b) Switch S5 is turned on, current flow is transferred from the freewheeling diode to the switch itself, so the conduction losses are minimized. The energy transfers from the source to the load. The duration of this interval determines the mean output voltage of the converter.

c) Switch S1.2 is turned off, current is flowing through its freewheeling diode. S3.1 and S3.2 are turned on. The transformer leakage inductance acts as a snubber for S3.1 and S3.2, limiting the current rise. The voltage V_{Tp} drops to zero. I_{IN} decreases and is redistributed between S1.1, S1.2 and S3.1, S3.2. The L_{in} starts accumulating energy. After I_{IN} has been fully transferred to S3.1 and S3.2, the freewheeling diode of S1.2 is closing with natural commutation, preventing shorting of primary winding.

d) S1.1 is turned off with ZCS. This interval could be used for the regulation of the input voltage when it varies.

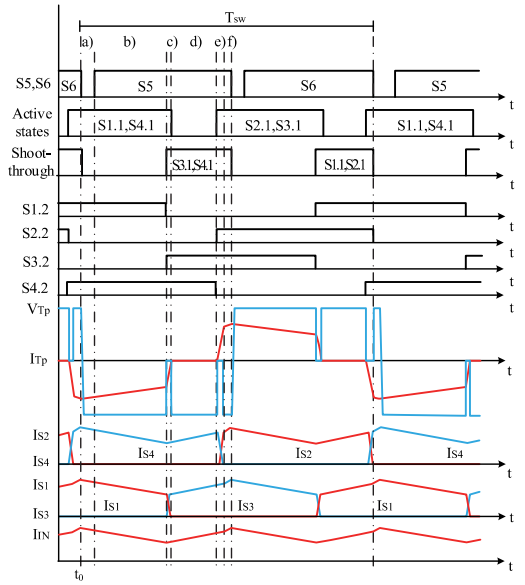

Fig. 4. Operational diagrams of the proposed converter topology with four four-quadrant switches.

e) S4.2 is turned off, current is transferred to its freewheeling diode. S2 is turned on with the transformer leakage inductance acting as a snubber. The voltage V_{Tp} drops to zero. I_{Tp} starts increasing due to the shoot-through state of the inverter switches. The current I_{TS} is flowing back to the transformer through the open S5, thus forcing I_{IN} to redistribute between S4 and S2.

f) After I_{IN} has been fully transferred to S2.1, S2.2, the current through S4.1 and S4.2 equals to zero and the freewheeling diode of S4.2 is closing with natural commutation, preventing shorting of the primary winding.

The energy from the load through the opened S5 is transferred back to the source, L_{in} accumulating energy from both, power source and load capacitor C3.

The process is repeated in a similar way for the second half-period.

As it seen from the diagrams, control signals of the additional switches slightly differ from the main. The reason is to prevent shorting at the intervals of current redistribution and, at the same time, to ensure minimal conduction losses during shoot-through and energy transfer intervals. The minimal duration of the intervals c) and e) is determined not just by the leakage inductance but also by the load and the source parameters which can vary significantly in PV applications. Therefore, they made slightly longer than the current redistribution time. Smaller time interval will lead to cutting off the non-zero current through the transformer winding, which will lead to high switching losses or even semiconductor damage due to the voltage overshoot. Longer time interval is not critical due to the current flow limitation in the other direction by freewheeling diodes.

Proposed converter with four four-quadrant switches does not require precise adjustment of durations of switching intervals and can maintain soft-switching in dynamic modes. This is the main benefit of proposed topology before another variant which has lover conduction losses but requires precise adjustment of duration of switching intervals [10].

Overall, the operational diagrams of the proposed topology are the same as in the reference topology [1].

B. Implementation with a Single Four-Quadrant Switch

Another technique to minimize conduction losses is the topology with a four-quadrant switch in series with the transformer primary winding, as shown in Fig. 5.

Fig. 6 shows the idealized voltage and current waveforms. The switching states for this topology are shown in Fig. 7, the solid black lines indicates current path while the gray one indicates inactive parts of the circuit.

At the moment t_0, the snubber capacitor C2 is charged to V_{OUT} and C1 is discharged: S1.1, S1.2, S2.1, S2.2, S4.1, S4.2, S7.1, S7.2 are conducting, C2 is discharged, C1 is charged to V_{Ts}. The switching half-period includes the following intervals:

a) Energy transfers from the load to the source through the freewheeling diode of S5. This process is characterized by conduction losses in this diode. Duration of that interval must

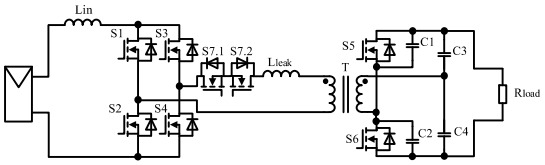

Fig. 5. Proposed converter topology with a single four-quadrant switch.

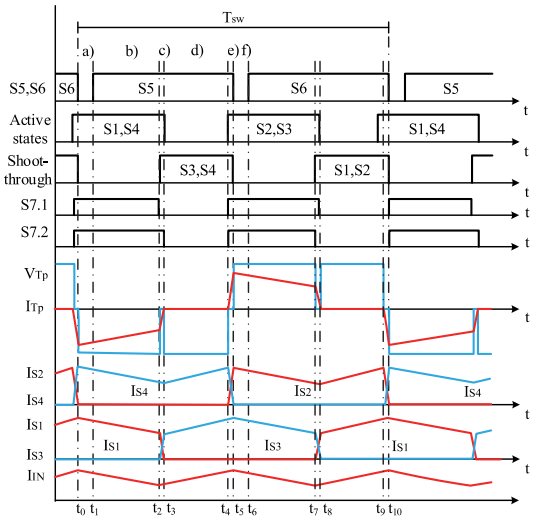

Fig. 6. Operational diagrams of the proposed converter topology with with a single four-quadrant switch.

be longer than the capacitor recharge interval to ensure that all transient processes on snubber capacitors are finished.

b) S5 is turned on with ZVS, current flow is transferred from the freewheeling diode to the switch itself. The energy transfers from the source to the load.

c) S7.1 is turned off, current is transferred to its freewheeling diode. S3.1 and S3.2 are turned on with the transformer leakage inductance acting as a snubber. The voltage V_{Tp} drops to zero. I_{IN} is redistributed between S1.1, S1.2 and S3.1, S3.2 due to the current flowing from the load. After I_{IN} has been fully transferred to S3, the freewheeling diode of S7.1 is closing with natural commutation, preventing shorting of transformer primary winding. S1 is still open but not conducting. The L_{in} starts accumulating energy.

d) S1 is turned off with ZCS. This interval could be used for regulation of the input voltage when it varies.

e) S2.1, S2.2, S7.1, S7.2 are turned on, with the transformer leakage inductance acting as a snubber.

f) S5 is turned off with the capacitor C1 acting as a snubber. On this interval, the snubber capacitor C1 is charged to V_{OUT}, and C2 is discharged: energy is transferred to the load through the freewheeling diode of S6. The process is repeated similarly to intervals a-e) for the second half-period

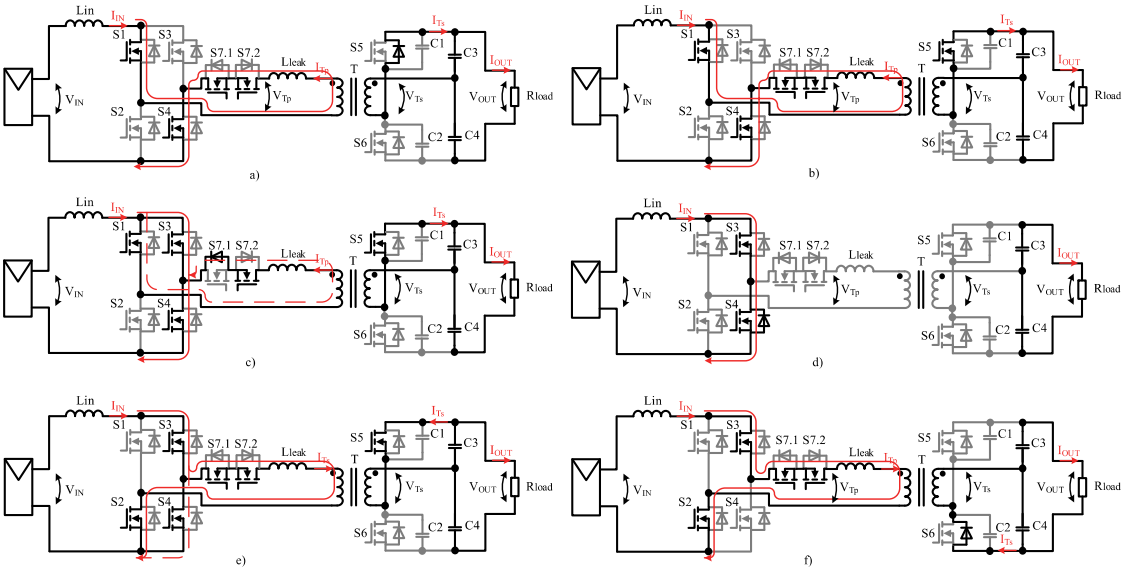

Fig. 7. Switching states of the proposed converter topology with a single four-quadrant switch.

Simulated transitions on all switches are shown in Fig. 8.

Both of these proposed converter topologies have similar operation principle as they are derived from the same topology [1]. Some main parameters of both topologies will be listed in the next chapter.

III. Design Guidelines

This section provides guidelines for the selection of the converter parameters. To simplify the analysis it is assumed that the passive components are lossless and the transformer magnetizing inductance is large enough and therefore the magnetizing current is negligible. Most of the converter parameters are calculated similarly to those in the reference topology [1] and [2], and thus they are not listed here.

The equation for the output voltage for both converter topologies is the same, as their operation principles are similar.

The output voltage can be expressed as:

$$V_{out} = 2 \cdot V_{Ts} = 2 \cdot V_{Tp} \cdot \frac{N_S}{N_P}, \quad (1)$$

where "2" is the DC voltage gain of the voltage doubler rectifier stage, V_{Tp} and V_{Ts} are the voltages across the transformer primary and secondary windings, respectively, N_P and N_S are the number of the turns of the primary and secondary windings.

The amplitude value of the transformer primary voltage is

$$V_{Tp} = V_{IN} \cdot \frac{T_{SW}}{T_{SW} - 2 \cdot t_+}, \quad (2)$$

where T_{sw} – the converter switching period, V_{IN} - the converter input voltage, t_+ – the duration of the switching intervals when L_{in} is accumulating energy.

Taking into account (2), the output voltage of the converter with four four-quadrant switches is

$$V_{out} = \frac{N_S}{N_P} \cdot \frac{2 \cdot V_{IN}}{1 - (2 \cdot t_c + 2 \cdot t_e + 4 \cdot t_f)/T_{SW}}, \quad (3)$$

where t_c, t_e, t_f – the duration of the switching intervals c), e) and f) accordingly. Each interval is repeated two times during switching period and on the interval *f*, the boost inductor L_{in} is accumulating energy from both, power source and load capacitor C3 (Fig. 4).

The output voltage of the converter with a single four-quadrant switch is

$$V_{out} = \frac{N_S}{N_P} \cdot \frac{2 \cdot V_{IN}}{1 - (2 \cdot t_c + 2 \cdot t_e)/T_{SW}} \quad (4)$$

where t_c, t_e – the duration of the switching intervals c and e accordingly (Fig. 6).

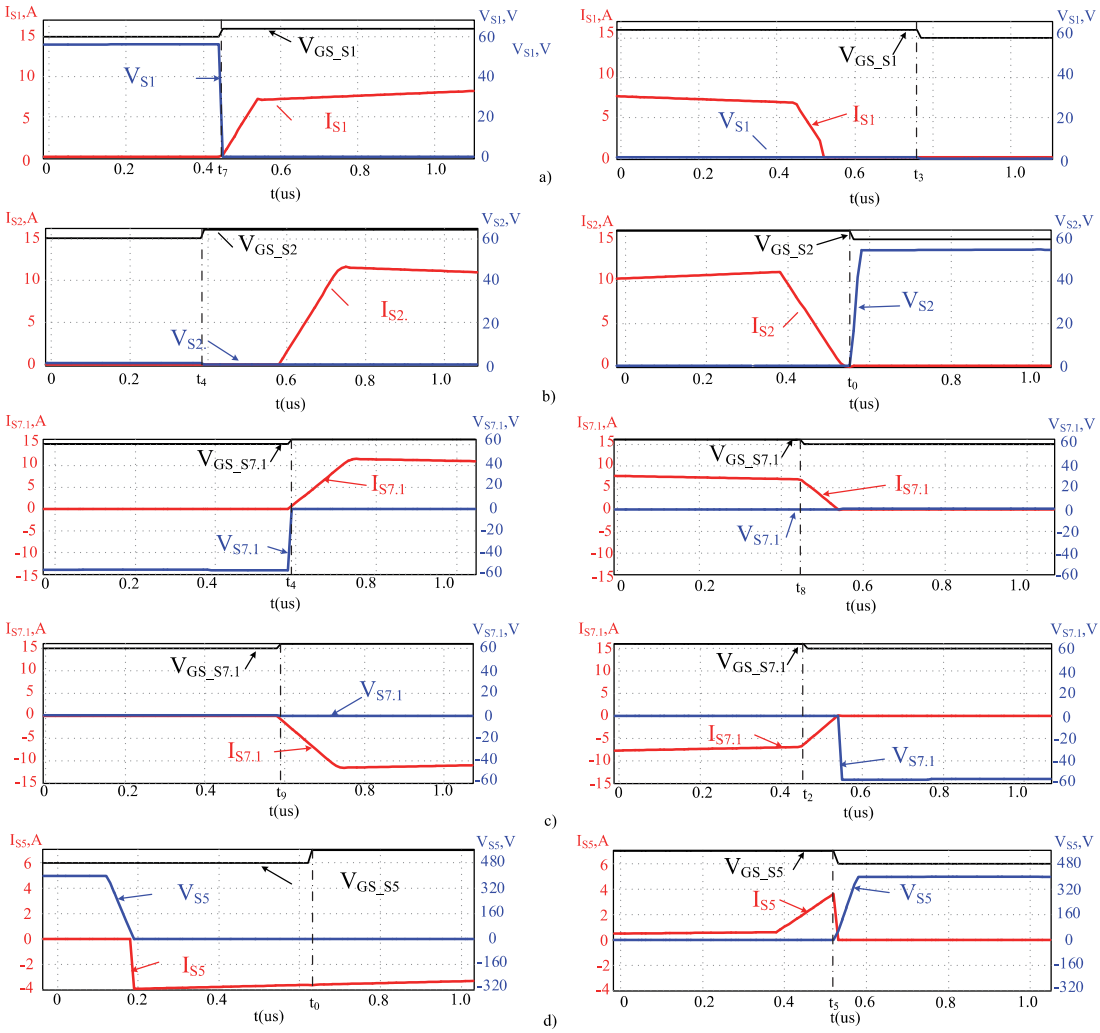

Fig. 8. Simulated voltage and current waveforms of S1 (a), S2 (b), S7.1 (c), S5 (d) for the proposed converter topology with a single four-quadrant switch

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As seen from (3) and (4) the output voltage is almost the same for both topologies, which means that the duty cycle and so the current and voltage ripple will be on the same level. Assuming this the proposed converter topologies can be compared in terms of efficiency with the same parameters of the passive elements.

IV. Efficiency Estimation

Both converter topologies were simulated by means of PSIM software with parameters in Table I for semiconductor components shown in Table II. Simulated working diagrams match exactly the theoretical ones shown in this paper. Total losses in the converter were calculated with the methodology proposed in [1], [2].

The simulation results are shown in Table III.

TABLE I. Converter Operational Parameters

Parameter	Symbol	Value
Input voltage, V	V_{IN}	30
Output voltage, V	V_{OUT}	400
Switching frequency, kHz	f_{SW}	100
Transformer turns ratio	N_S/N_P	3.5
Output capacitance, uF	C3, C4	1
Snubber capacitance, pF	C1, C2	265
Input inductance, uH	L_{in}	15
Leakage inductance, uH	L_{leak}	0.76
Rated power, W	P_{out}	275

TABLE II. SEMICONDUCTOR COMPONENTS

Parameters	Inverter transistors	Rectifier transistors
	Si4190ADY	IPA60R190P6
V_{DS}, V	100	650
I_D,A(t=25°C)	18.4	20,2
$R_{DS(on)max}$, mΩ	8,8	190
$Q_{g,typ}$,nC	20,7	37
C_{OSS},pF	695	76

TABLE III. ESTIMATION OF THE CONVERTER TOTAL LOSSES

Losses (W)	Reference topology	Four four-quadrant switches	Single four-quadrant switch
Inverter stage transistor switching	0.4	0.8	0.6
Inverter stage transistor conduction	2.8	5.6	4.2
Inverter stage diodes conduction	11.2	0	0
Rectifier stage transistor switching	0	0	0
Rectifier stage transistor switching	1.2	1.2	1.2
Rectifier stage diodes conduction	0.6	0.6	0.6
Total losses:	16.2	8.2	6.6
Efficiency (%):	94.1	97.0	97.6

CONCLUSIONS AND FUTURE WORK

The proposed converters allow soft-switching of the both inverter and rectifier switches without any auxiliary passive elements and clamping circuits.

As seen from simulation results, the topology with a single four-quadrant switch has higher efficiency than the topology with four four-quadrant switches, but at the same time, it has few disadvantages that could affect the final choice of topology:

- Step-up factor is slightly lower than in the topology with four four-quadrant switches;
- The switching interval *e* (and the symmetrical interval in another half-period) must be of strictly right duration, which is equal to the time of current redistribution between switches S4 and S2. The shorter duration of this interval will result in high switching losses and, in extreme cases, can lead to damage of the switch S4. The significantly longer duration will result in current increase through the switch S2 and eventually may result in the boost inductor saturation.
- The original topology and the topology with four four-quadrant switches does not have the problem with the longer duration of this switching interval and so they have lower requirements to the control system in dynamic mode. This means that proposed converter with four four-quadrant switches allows robust soft-switching commutation, which is hard to achieve in galvanically isolated current-fed DC-DC converters.

The main disadvantage of the topologies is the presence of four switches in series in the inverter stage on the path of the current flow during the energy transfer interval. This leads to the conduction losses higher than in the conventional phase-shifted full-bridge topology. Nevertheless the switching losses are lower due to the introduced soft-switching. It means that switching frequency could be increased while maintaining the efficiency at acceptable level.

Future work will be devoted to the experimental verification of the proposed converters and further control algorithm optimization.

ACKNOWLEDGEMENT

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Bidirectional Isolated ZVS DC-DC Converter with Auxiliary Active Switch for High-Power Energy Storage Applications

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***Abstract* — This paper describes topology and control algorithm of a bidirectional isolated converter with controlled semiconductors at the voltage-fed and current-fed parts. A bidirectional switch connected in series with the transformer winding at the current-fed side features zero-current switching and allows achieving zero-voltage-switching of transistors at the voltage-fed side by utilising leakage inductance of the isolated transformer. The topology is proposed for high power battery or fuel cell systems. The proposed ideas are verified with simulations in MATLAB and evaluation prototype.**

Keywords — Bidirectional power flow; ZVS; ZCS; DC-DC power converters; snubbers

I. INTRODUCTION

In the field of isolated DC-DC converters the full-bridge, half-bridge or push-pull topologies with controlled switches in the primary part and uncontrolled rectifiers in the secondary are widely used [1]-[4] (Fig. 1). The galvanic isolation and output filtering are achieved by an isolation transformer and LC filter. The power semiconductor devices in such basic systems are typically hard-switched, which results in considerable dynamic losses, especially at high switching frequencies. Those can be limited by applying dissipative or non-dissipative passive or active circuits [5]. Alternatively, special control algorithms or other topology modifications may be applied to achieve zero voltage (ZVS) or zero current switching (ZCS) of the main power semiconductor devices [6]-[10]. The application of controlled switches in the rectifier part allows to transfer power in the reverse direction.

This paper analyses the topology presented in [11] (Fig. 2), where the power transfer from current-fed (CF) to voltage-fed (VF) side is described. This work focuses on operation mode where the energy is transferred from the VF to the CF terminal. For high-power systems, the IGBTs can be used as the main switching devices. The topology features soft-switching operation of power semiconductor devices. However, the drawback lies in increased number of switching devices at the CF side.

II. OPERATION OF THE CONVERTER

The case study converter topology depicted in Fig. 2 differs from the conventional one by an additional bidirectional reverse blocking (RB) switch, connected in series with the transformer winding w_2. The switching processes during one half-period of power transfer from VF to CF side are presented in Fig. 3 and

Fig. 6. The following switching states can be distinguished:

t_0-t_1: VT1, VT3, VD4 together with VD5 and VD8 are conducting (Fig. 3a). During this interval $u_d/2>u_{w1}$, the capacitor C1 is discharged, C2 is charged to $u_d/$ and the currents i_d, i_L are increasing.

t_1-t_2: at t_1 the transistor VT1 is turned off with *du/dt*, limited by snubber capacitors C1 and C2 (Fig. 3b). By the end of the interval the transformer voltage Utr2 drops to zero, and the voltage across snubber capacitors becomes equal to ud/2.

t_2-t_3: The transformer voltage U_{tr1} changes its sign and the diodes VD6-VD7 become forward biased and their current starts increasing, while the current of VD5 and VD8 decreases (Fig. 3c).

t_3-t_4: At t_3 the snubber capacitors are completely recharged and the transformer voltage reaches the amplitude value. The diode VD2 becomes forward biased and starts returning the energy stored in the leakage inductance to the input (Fig. 3d). From here the transistor VT2 could be turned on with ZVS.

t_4-t_5: the current through VD6 and VT3 decays to zero and the energy return is finished. The transformer voltage U_{tr2} rises from zero to the amplitude value and the currents through diodes VD5-VD8 becomes equal to half of the value of i_L (Fig. 3e).

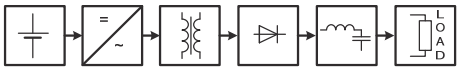

Fig. 1. Generalised structure of an isolated DC-DC converter with a high-frequency isolating transformer.

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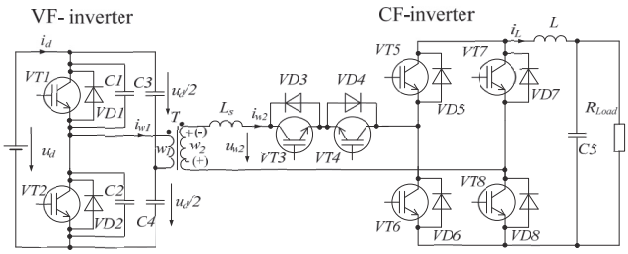

Fig. 2. The bidirectional current-fed dc-dc converter with a single four-quadrant switch in series with the transformer winding 2.

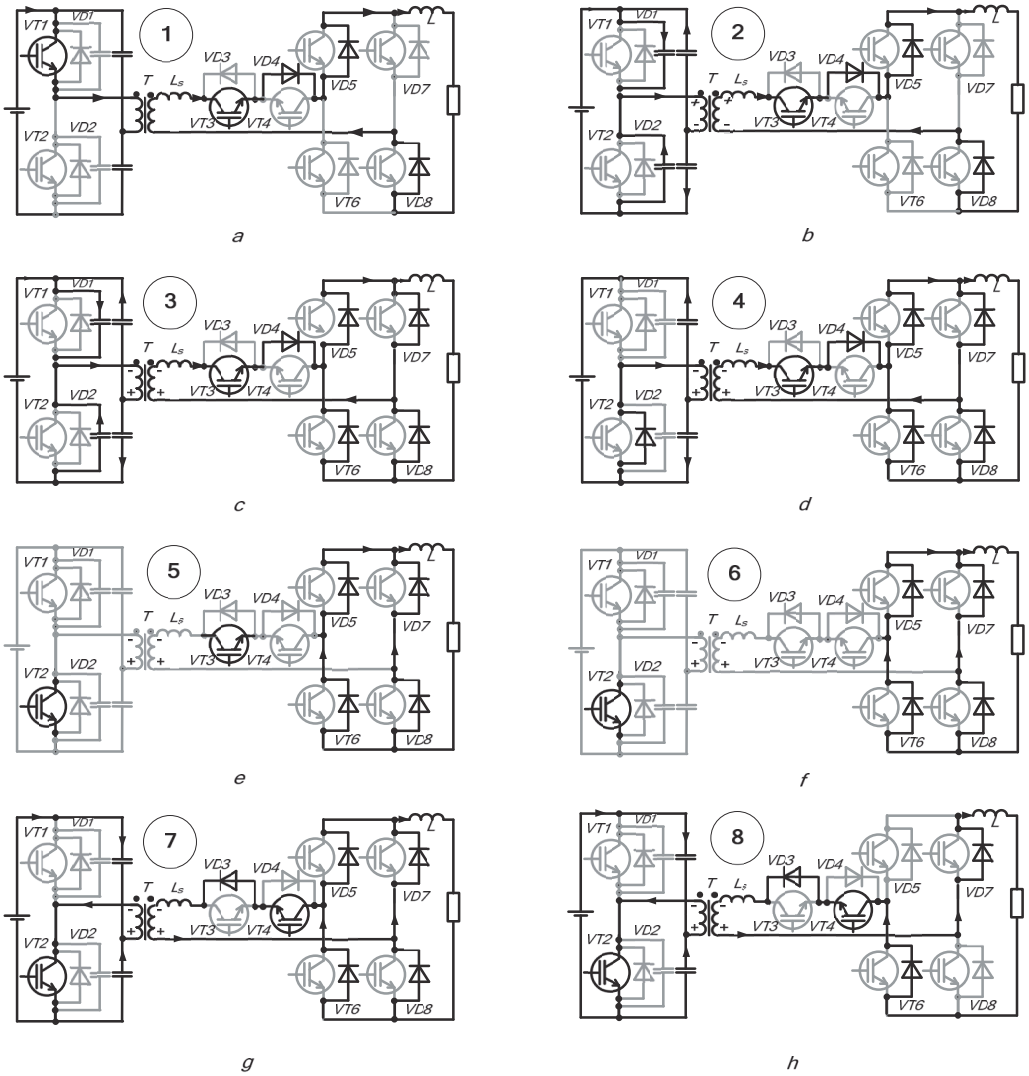

Fig. 3. Converter switching states during power transfer from VF to CF side.

t_5-t_6: the transistor VT3 could be turned off with ZCS at any time during this interval, therefore the maximum duty cycle duration of the auxiliary switch could be increased to 0.5. The current i_L is decreasing, while freewheeling through VD5-VD8, L and the load (Fig. 3f).

t_6-t_7: the transistor VT4 is turned on (Fig. 3g). The transformer voltage U_{w2} drops to zero while the output current redistributes to VD6 and VD7 with *di/dt* limited by transformer leakage inductance.

t_7-t_8: the diodes VD5 and VD8 become reverse biased and the diodes VD6 and VD7 are now conducting full output current (Fig. 3h). The transformer voltage U_{tr2} rises to amplitude value. The i_L is rising and the processes repeat similarly for the next operating half-period.

The presented algorithm shows that VF switches feature ZVS turn-on and snubber capacitor-assisted turn-off. The auxiliary switch features ZCS turn-off, while *di/dt* at turn-on is limited by the leakage inductance of the transformer.

The advantage of the topology lies in minimised energy circulation: unlike the dual active bridge [12] or RB active rectifier converters [13], where the energy return is a controlled parameter, only the energy stored in the leakage inductance is being returned to the source. The operating principle of the converter is close the topology with half-controlled full-bridge rectifier, where one arm consists of controlled RB devices, while another one is based on diodes [14]. However, in contrast to the case study topology, it does not allow bidirectional power flow.

IV. Simulation Results

In order to verify the presented operating principles, the simulation model was created in MATLAB software. The simulation parameters are listed in Table I. The waveforms are presented in Figs 4. As it could be observed, the simulation results are in agreement with the estimations.

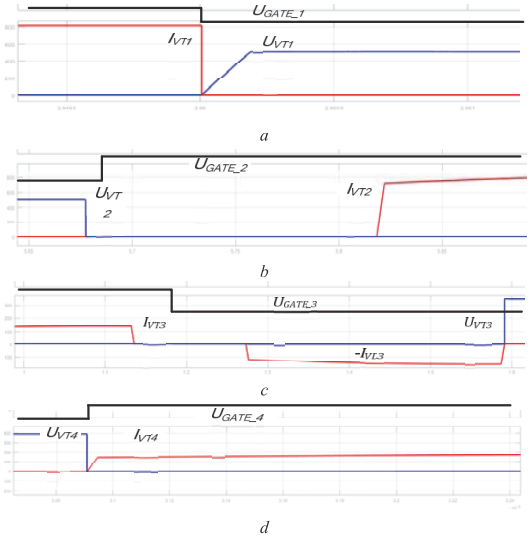

Fig. 4. Simulated voltage and current waveforms of VT1 (a) , VT2 (b), VT3 (c), VT4 (d) for the proposed algorithm for converter with a single four-quadrant switch

TABLE I. Parameters of the Converter

Parameter	Symbol	Value
CF-side voltage	V_{CF}	150 VDC
VF-side voltage	V_{VF}	3300 VDC
Switching frequency	f_{sw}	1000 Hz
CF side inductor	L	1 mH
VF-side capacitors	C_1, C_2	30 nF
Transformer turns ratio	N_s/N_p	1:1
Load resistance	R_{Load}	10 Ohm

IV. Experimental Results

For verification the converter control algorithm its physical model has been developed. The model allows to analyse the processes of commutation of power switches.

Turn-on / turn-off processes of VT1 –VT4 is shown on fig. 5 (a,b) and fig. 5 (c ,d) respectively. At fig. easily verified, that commutations of switches are at ZVS and ZCS modes.

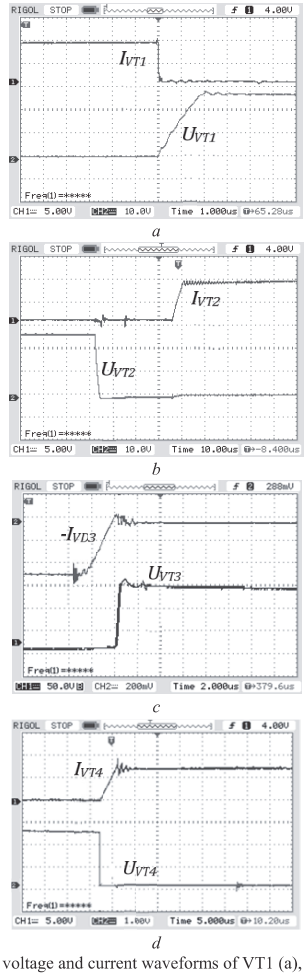

Fig. 5. Simulated voltage and current waveforms of VT1 (a), VT2 (b) , VT3 (c) and VT4 (d)

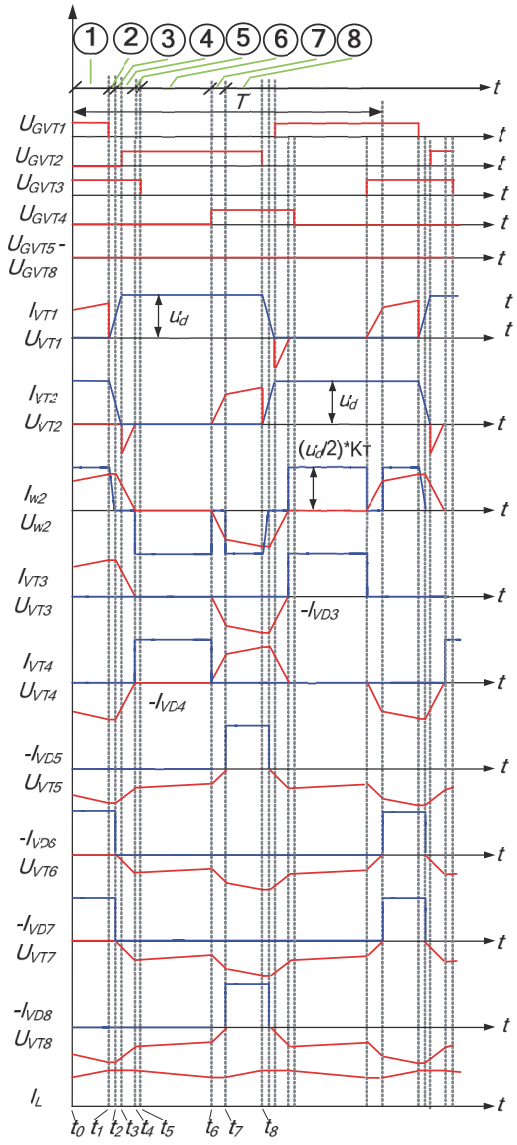

Fig. 6. Operation principle of the converter for the energy transfer from VF to CF side

V. Conclusions:

The paper presents DC-DC converter with CF and VF terminals. The auxiliary bidirectional switch connected in series with the transformer winding at the CF side enables soft switching of power semiconductor devices. As a result, dynamic losses are reduced and higher operating frequencies could be achieved. The possibility to transfer power in both directions allows the topology to be applied in high power battery or fuel-cell applications.

The converter operation are verified with computer simulations and physical model, which prove the functionality of the presented system.

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Full-Soft-Switching High Step-Up Bidirectional Isolated Current-Fed Push-Pull DC-DC Converter for Battery Energy Storage Applications

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***Abstract*—This paper presents topology of a novel bidirectional current-fed push-pull DC-DC converter with galvanic isolation. The control algorithm proposed enables full-soft-switching of all transistors in a wide range of the input voltage and the input power and does not require snubbers or resonant switching to be employed. The converter features active voltage doubler rectifier, which is controlled by the switching sequence synchronous to that of the input-side switches. As a result full-soft-switching operation at fixed switching frequency is achieved. First, operation principle for the energy transfer in the both directions, forward and reverse, was described. Then, experimental prototype of rated power 300 W was built. Experimental results obtained are in good agreement with the theoretical steady-state analysis.**

Keywords—current-fed dc-dc converter; bidirectional converter; soft-switching; ZVS; ZCS; push-pull converter; switching control method, naturally clamped

I. INTRODUCTION

Rapid development of power electronics applications is evident in recent years due to numerous challenges imposed on the modern electric energy generation and distribution systems [1]. Among them, technology of the residential battery energy storage systems (BESSs) have attracted a lot of attention recently due to wide adoption of residential solar photovoltaic (PV) and wind systems [2]-[5]. Residential BESSs mitigate problem of time shift between energy generation and consumption in the households, and decrease sensitivity of the whole system to an intermittent nature of the renewable energy sources [6]. At the same, it can results in minimized electricity bill and higher electricity supply security if active demand-side management and smart grid elements are employed.

Development of battery technologies brought on the market small scale BESSs aimed for households with energy capacity up to 10 kWh. There are several examples available or emerging to the market: Tesla Powerwall (6.5 kWh), BYD EPS-1500 (2.4 kWh), JLM Energy Energizr-100 (8.8 kWh), Enphase AC Battery (1.2 kWh), Samsung SDI AIO (3.6 kWh), etc. Residential BESSs can have rated power as low as 300 W for supply of critical appliances, while they usually support modular approach that allows easy system scalability. Many of available small BESSs contains lithium iron phosphate ($LiFePO_4$) type of batteries that is characterized by high safety, long lifetime, low cost and high number of recharging cycles [7]-[9]. Those batteries are usually low voltage sources and thus require interface converter whether a BESS has AC or DC output.

Current-fed (CF) converters are known for low input current ripple and, consequently, good compatibility with batteries and fuel cells [10], [11]. However, galvanically isolated CF converters were previously depreciated in favor voltage-fed (VF) converters, like dual active bridge (DAB) and similar topologies [10]. DAB become popular due to high efficiency, good scalability, and soft-switching operation [12]. Combination of those features was previously complicated in case of CF converters. However, recent developments demonstrate new CF converter topologies that combines those features. Soft-switching is important to achieve high efficiency and power density. In case of galvanically isolated CF converters soft switching can be achieved with active clamping [13]-[14], resonant switching [15], active snubber that enables resonance during switching transients only [16], utilization of parasitic resonance [17] and other methods. However, these methods usually require additional components, complicated control system tuning, variable switching frequency, etc.

New class of soft-switching galvanically isolated CF converters was developed recently. It is based on active control of the secondary side switches synchronously to the primary side switches [18]-[24]. It is especially advantageous in bidirectional converters where active switches are always present in the secondary side and thus no additional components are required. Special switching sequence is used for shaping of the isolation transformer current, which results in soft-switching operation of semiconductors. This new class of converters contains only several push-pull topologies despite the fact that push-pull converters show superior performance in BESS and PV applications due to low number of switches within the input current loop [25]-[27].

This paper presents a new galvanically isolated CF push-pull DC-DC converter derived from the full-bridge converter presented in [24]. The main disadvantage of the full-bride

baseline topology is high number of switches at the CF side, where four switches are always present in the input current loop, which is also observed in several others soft-switching CF converters [16], [22]. The proposed push-pull converter allow reduction of number of switches at the input side from eight to four, while their increased voltage stress is not a serious issue in BEESs considering low operating voltage of the corresponding lithium iron phosphate batteries. The push-pull converter proposed is intended for low-power residential BESSs.

II. Forward Operation Mode of the Converter

The proposed converter topology is shown in **Error! Reference source not found.**. It consists of the CF push-pull switching stage in the input low-voltage side and the active voltage doubler rectifier (half-bridge in the reverse operation mode) in the output VF side. The converter features soft-switching operation of all semiconductor components in a wide range of the input voltage and power, while provides natural clamping of the input CF side switches. Galvanic isolation allow interfacing of low-voltage batteries to the DC bus with much higher operating voltage or to the utility grid. Converter maintains soft-switching properties in bidirectional operating mode and provide continuous current at the battery terminals connected to the CF port of the converter. The main drawback is high number of switches even though it was reduced when compared to the full-bridge counterpart, which results in additional conduction and driving losses. Voltage step-up is performed by means of energy circulation intervals, which are usually minimized in the full-bridge counterpart due to additional losses when compared with conventional PWM shoot-through control. The parasitic output capacitance (C_{OSS}) of the switches S_3, S_4 can be used as snubber capacitors C1-C2.

This section describes the forward operation mode, i.e. then the power is transferred from terminal V_{CF} to V_{VF}. In this mode bottom transistors of current-fed four-quadrant (4Q) switches (S1.2 and S2.2) operate as diodes. Generalized current and voltage waveforms for this operation mode are shown in Fig. 2. It is evident that converter operation can be described in six unique time intervals within half the switching period T_{SW}.

Interval 1 ($t_0 < t < t_1$, Fig. 3a). At the instant t_0 the voltage across transformer reaches amplitude value and the BD (body diode) of S4 starts conducting the transformer current, power delivery mode is started. This interval is necessary to ensure that the snubber capacitors are completely recharged and should be optimized to minimize BD conduction losses.

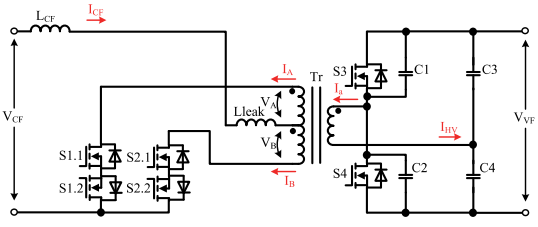

Fig. 1. Full-soft-swithicng CF push-pull converter proposed.

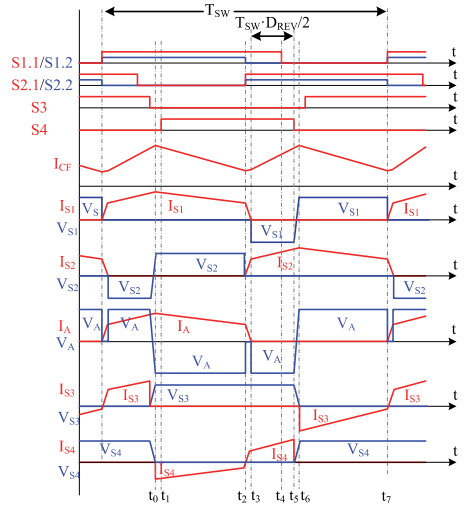

Fig. 2. Generalized waveforms for the forward operation mode.

Interval 2 ($t_1 < t < t_2$, Fig. 3b). Transistor S4 is turned on with ZVS at the instant t_1, power delivery mode continue. Energy is transferred to VF terminals through 4Q switch S1, transformer winding A and transistor S4.

Interval 3 ($t_2 < t < t_3$, Fig. 3c). Switch S1.2 is turned off. The body diode (BD) of S1.2 conducts the current. 4Q switch S2 is turned on with ZVS, assisted by the transformer leakage inductance. The transformer winding A current decreases while winding B current increases. Input current redistributes from 4Q switch S1 to S2. Transformer primary winding voltage drops to zero due to flux cancellation from both windings. At the instant t_2 converter goes to shoot-through state (both 4Q switches S1 and S2 conduct), the input inductor starts accumulating the energy.

Interval 4 ($t_3 < t < t_4$, Fig. 3d). At the instant t_3 transformer winding A current drops to zero causing BD of S1.2 to turn off. Starting from this interval S1.1 does not conduct any current and can be switched off with ZCS. The input inductor accumulates the energy from CF terminals and output capacitors C3, C4 through transistor S4 and transformer Tr. The energy is transferred in reverse direction from VF to CF side for the additional voltage-step-up.

Interval 5 ($t_4 < t < t_5$, Fig. 3e). At the instant t_4 switch S1.1 is turned off with ZCS. The energy is transferred in the same way as during Interval 4

Interval 6 ($t_5 < t < t_6$, Fig. 3f). The transistor S4 turns off with snubber-assisted soft-switching at the instant t_5. Voltage across C2 changes from zero to V_{VF} and across C1 from V_{VF} to zero. Transformer voltage polarity is changed.

Interval 7 ($t_6 < t < t_7$). This interval is similar to the interval 1. At the instant t_5 BD of S3 starts conducting the transformer current, starting the energy delivery interval. Processes are repeated in the same way for the second half of the switching period.

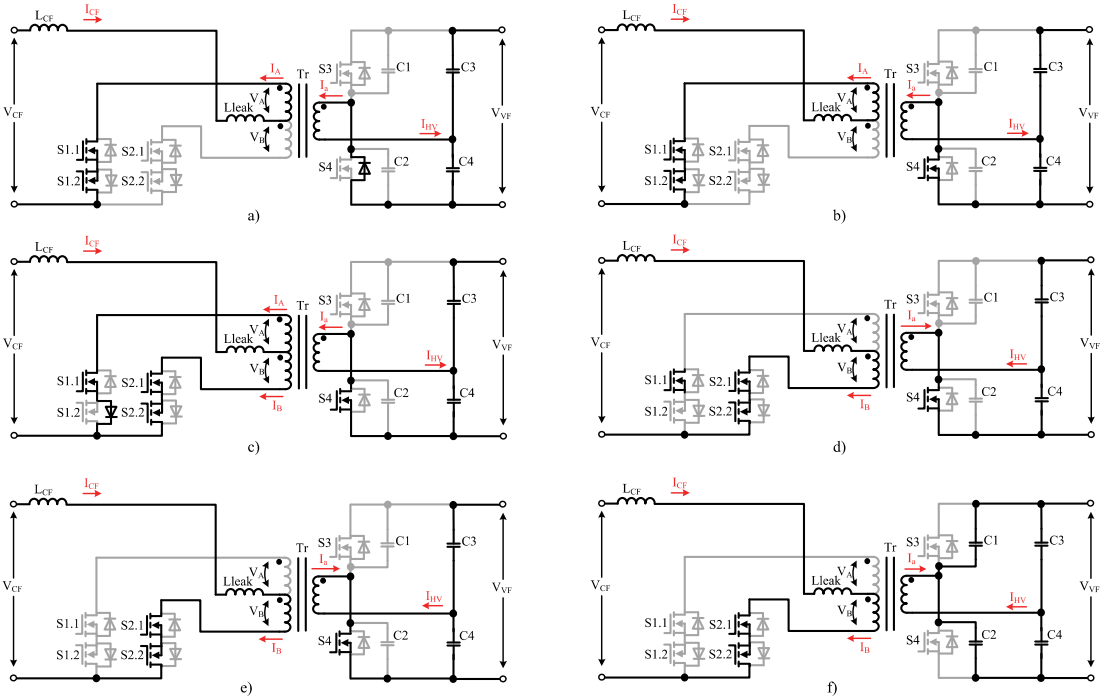

Fig. 3. Equivalent circuits for the forward operation mode.

The duration of snubber recharge (interval 6) and current redistribution (interval 3) intervals is negligibly small as compared to energy transfer intervals 2 and 4-5. Simplified equation for the normalized DC voltage gain of the converter in the forward operation mode (Fig. 4) can be expressed as:

$$G_{FRW} = \frac{V_{VF}}{2nV_{CF}} = \frac{1}{1-2\cdot D_{REV}}, \quad (1)$$

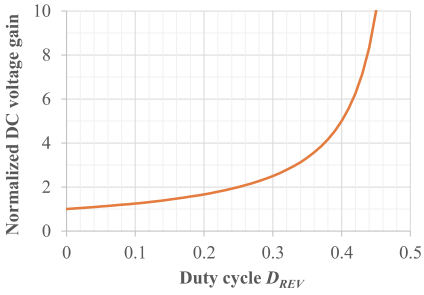

Fig. 4. Normalized DC voltage gain in the forward operation mode.

III. Reverse Operation Mode of the Converter

This section describes the reverse operation mode, when the power is transferred from terminals V_{VF} to V_{CF} as show in Fig. 5. This operation mode can be used for battery charging in BESS. In this mode top transistors of current-fed side four-quadrant (4Q) switches (S1.1 and S2.1) operate as diodes.

Interval 1 ($t_0 < t < t_1$, **Error! Reference source not found.**a). At the instant t_0 current through 4Q switch S2 drops to zero causing BD of S2.1 to turn off naturally. Power delivery mode starts. Starting from this instant transistor S2.2 can be switched off with ZCS. Energy is transferred through transistor S4 and 4Q switch S1. This interval is necessary to ensure that the current through S2 equals zero before the time instant t_1.

Interval 2 ($t_1 < t < t_2$, **Error! Reference source not found.**b). Switch S2.2 turned off with ZCS at t_0. Energy is transferred to V_{CF} terminals from the VF side through transistor S4, transformer winding A and 4Q switch S1.

Interval 3 ($t_2 < t < t_3$, **Error! Reference source not found.**c). The transistor S4 turn off with snubber-assisted soft-switching at the instant t_2. This results in recharging of snubber capacitors C2 from zero to V_{VF} and C1 from V_{VF} to zero.

Interval 4 ($t_3 < t < t_4$, **Error! Reference source not found.**d). At the instant t_3 the transformer voltage polarity is

changed causing and BD of S3 to turn on. The load current flow direction is maintained by L_{CF}. Reverse energy transfer mode is started (energy is

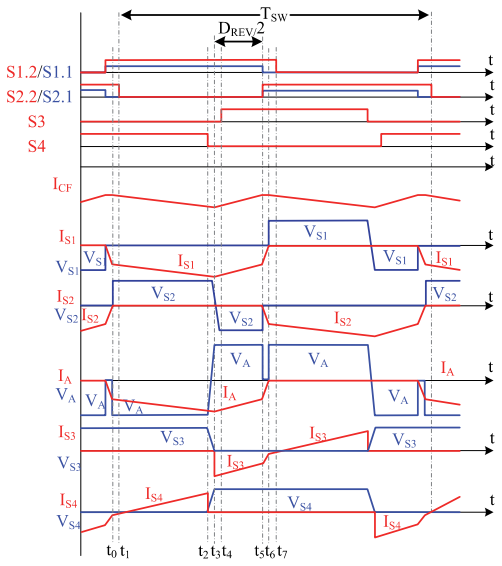

Fig. 5. Generalized waveforms for the reverse operation mode.

transferred from CF to VF terminals). This interval is needed to ensure that snubber capacitors are recharged and should be optimized to minimize BD conduction losses.

Interval 5 ($t_4 < t < t_5$, **Error! Reference source not found.**e). At the instant t_4 S3 turns on with ZVS. Energy stored in L_{CF} is transferred back to terminals V_{VF}. Duration of this interval determines converter voltage step-down factor.

Interval 6 ($t_5 < t < t_6$, **Error! Reference source not found.**f). At the instant t_5 switch S1.1 is turned off. The body diode (BD) of S1.1 conducts the current. 4Q switch S2 is turned on with ZVS, assisted by the transformer leakage inductance. The transformer winding A current is decreasing while winding B current increasing. Input current is redistributing from 4Q switch S1 to S2. Transformer primary windings voltage drops to zero due to flux cancellation effect.

Interval 7 ($t_6 < t < t_7$). This interval is similar to the interval 1. At the instant t_6 current through 4Q switch S1 drops to zero, causing BD of S1.1 to turn off. Starting from this instant S1.2 can be switched off with ZCS. Power delivery mode is started. Energy is transferred through transistor S3 and 4Q switch S2. This interval is needed to ensure that the current through S1 always drops to zero at any operating point. Process repeated analogically for the second half-period. Simplified equation the normalized DC voltage gain of the converter in the reverse operation mode (**Error! Reference source not found.**) can be expressed as:

$$G_{FRW} = \frac{2nV_{CF}}{V_{VF}} = 1 - 2 \cdot D_{REV} . \quad (2)$$

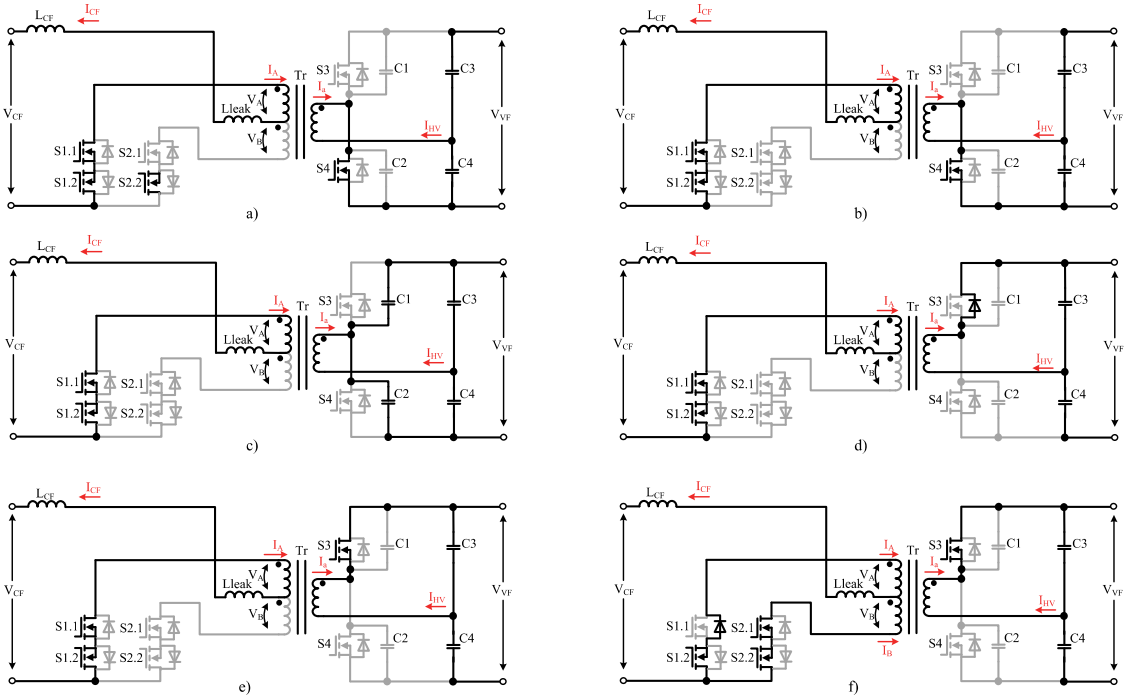

Fig. 6. Equivalent circuits for the reverse operation mode.

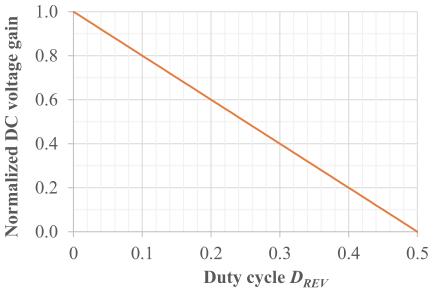

Fig. 7. Normalized DC voltage gain in the reverse operation mode.

IV. Experimental Results

Experimental prototype was design for interfacing of the $LiFePO_4$ batteries into DC-microgrid. It also can be used as a frontend DC-DC converter in AC-storage system. Converter operation range covers full range of LiFePO4 battery operation, starting from full charge to deep discharge. Proposed converter total losses are determined mostly by the conduction losses and losses in magnetic components. Low efficiency at low input voltage is caused by higher current and high voltage step-up required to maintain the constant output power.

The main operation parameters of the prototype are presented in Table I. Table II describes the main parameters of semiconductor devices utilized in this study. Two critical operating points described in Table III were tested. The converter efficiency is higher when the normalized DC voltage gain is closer to unity. It goes down to 93.3% (by 3%) when the normalized DC voltage gain of the converter is increased by factor of 1.5. It means that converter efficiency does not exceed 3% variations and can be considered flat within the operating range of a $LiFePO_4$ at the rated power. Moreover, reverse operation mode provide the same efficiency values as that in the forward mode in the corresponding operating point.

TABLE I. Operating Parameters of the Experimental Converter

Parameter	Symbol	Value
Converters power rating, W	P	300
Input voltage, V	V_{CF}	20-30
Output voltage, V	V_{VF}	400
Switching frequency, kHz	f_{SW}	100
Transformer turns ratio (Np/Ns)	n	6
Transformer magnetizing inductance, mH	L_{TX_m}	3.4
Transformer secondary leakage ind., uH	L_{TX_leak}	8
Inductance of boost inductor, uH	L_{CF}	16
Capacitance of filter capacitor, uF	C_3, C_4	2.2
Capacitance of snubber capacitor, pF	$C_1 – C_6$	265

TABLE II. TYPES AND PARAMETERS OF SEMICONDUCTOR DEVICES USED

Component	Type	Specifications
CF MOSFETs	Infineon BSC035N10NS5	V_{DS}=100 V; $R_{DS(on)}$=3.5 mΩ I_D=100 A, t_{rr}= 62 ns, C_{OSS}=770pF
VF MOSFETs	ROHM SCT2120AF	V_{DS}=650 V; $R_{DS(on)}$=120 mΩ I_D=29 A, t_{rr}=33 ns, C_{OSS}=90pF

TABLE III. FORWARD OPERATION TEST RESULTS

Parameters	Test point	
Input voltage, V	20	30
Input current, A	15	10
Normalized DC voltage gain, (V_{VF}/(2nV_{CF}))	1.67	1.11
Efficiency, %	93.3	96.3

Voltage and current of semiconductor components captured during experimental study are shown in Figs. 8-10. They correspond to the converter operating in the forward mode when V_{CF} = 25 V and the input power equals 300 W. Soft-switching operation of the switches is evident and thus steady-state analysis presented above is confirmed.

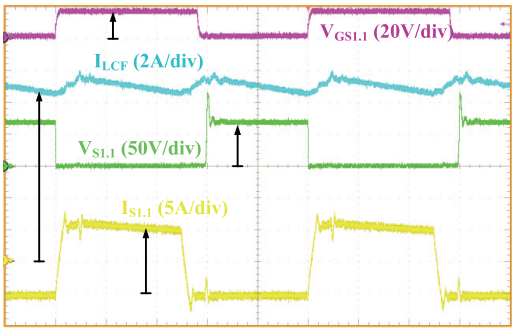

Fig. 8. Experimental current and voltage waveforms of the switch S1.1.

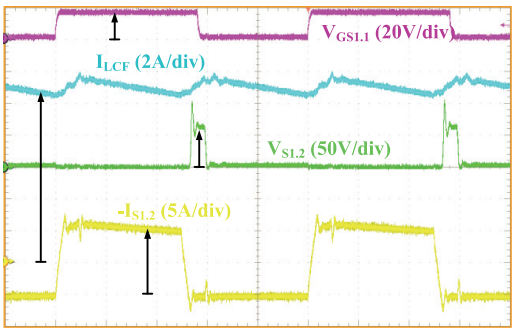

Fig. 9. Experimental current and voltage waveforms of the switch S1.2.

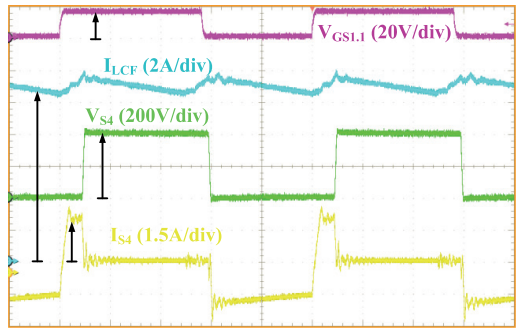

Fig. 10. Experimental current and voltage waveforms of the switch S4.

CONCLUSIONS

A novel bidirectional galvanically current-fed push-pull converter with galvanic isolation was proposed. It features full-soft-switching operation of all semiconductor components, while its DC voltage gain is higher than in traditional current-fed converters due to utilization of the circulating energy for the input voltage step-up. Moreover, it does not require any clamping circuits, since the novel control algorithm proposed features natural clamping of the switches at the current-fed side. Despite relatively high number of semiconductor components, it show peak efficiency of 96.3%. Efficiency of the converter almost does not depend on energy transfer direction in the same operating point. Soft-switching operation with continuous current at the current-fed side makes the converter proposed suitable for residential battery energy storage systems. Further research will be directed towards experimental verification of the converter performance with lithium iron phosphate battery.

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Dual Inductor Current Fed Push-Pull DC-DC Converter with High Conversion Ratio

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***Abstract* – This paper presents an isolated bidirectional current fed DC-DC converter with high conversion ratio for battery energy storage systems. The converter features low voltage battery-side terminal that acts as dual inductor push-pull stage in the boost mode and current doubler rectifier in the buck mode. Similarly, high-voltage terminal acts as voltage doubler rectifier or half-bridge inverter. The phase shift modulation method proposed utilises transformer leakage inductance and transistor parasitic capacitances to enable soft-switching of all semiconductors in a wide range of the input voltage and power. This is achieved without requirement of external snubbers or resonant circuits and complex multi-mode modulation strategies. Operation principle for both energy transfer directions is described and component design guidelines are presented. The converter operation is verified with 500 W experimental prototype.**

***Keywords* – dc-dc power converters, zero current switching, zero voltage switching, soft switching.**

I. Introduction

Increased electricity generation from the renewable energy sources changes the principle of electric grid architecture from centralised to widely distributed generation [1]. Installation of various energy storage systems enables higher self-consumption and utilization of renewable energy sources as well as provision of ancillary services for the grid, including reactive power supply, voltage and frequency support, operational reserve capability, peak shaving, support of intentional electrical islands, optimised management of solar cycles, power oscillation damping, etc [2]. In private residential applications, battery-based energy storage systems (BESSs) are usually utilised [3][4][5]. The power of such BESSs varies in the range from hundreds of Watts up to several kW and they are typically equipped with relatively low voltage batteries [6][7][8]. Therefore, an interface converter with high voltage conversion ratio is required. Converters with transformers are often preferred due to reduced stresses on components and galvanic isolation [9]. Such systems generally utilise two-stage power conversion: combination of step-up bidirectional DC-DC converter and grid side DC-AC inverter. This configuration includes intermediate DC-link that can be used for interconnection of renewable energy sources [10].

For bidirectional DC-DC power conversion, voltage source DC-DC converters [11], such as dual active bridge (DAB) topology is a reliable and widely adopted solution, which can provide soft switching for semiconductors and high efficiency [12]. On the other hand, such converters are susceptible to core saturation, have increased transformer and semiconductor rms currents and require complex modulation strategy to maintain soft switching under wide range of operating conditions [13].

In recent years, current-fed (CF) converters that are aimed to solve mentioned drawbacks are proposed [14]-[22]. Those include soft switching converters with active clamp circuit [15][16], resonant switching [17][18], active snubber [19][20], secondary side modulation [21][22] etc. Another advantage of CF converters lies in low input current ripple; therefore, they are referred as reliable solutions for battery and fuel cell interfacing [23][24].

For low voltage and relatively low power systems push-pull converters are popular due to their increased gain and low number of active devices [25]. Comparison between two CF push-pull DC-DC converter types (single inductor and dual inductor) was presented in [26]. The benefits of dual inductor converter are: reduced voltage across the main switches, lower current stress on the inductors, reduced RMS current ripple of the output capacitor, smaller size of the transformer and each of the input inductors.

Several soft switching dual inductor push-pull converter topologies have been proposed. The first group utilises active and passive circuits at the input side and passive rectifier. The converter with active clamp proposed in [15] provides ZVS for primary semiconductors and constant operating frequency. On the other hand, it requires additional semiconductor components and ZVS is lost at light loads. The advantages of circuit in [27] lie in low number of active devices and simple output part, but it requires variable frequency for gain regulation. The second group is using active rectifier to create soft switching conditions at the input side and possesses inherent bidirectional operation capability. The converter presented in [28] utilises secondary side modulation to force the current redistribution at the input side and provide ZCS conditions. On the other hand, such solution exhibits high circulating energy in the switches and transformer when operating at low input voltages and light loads. The method was extended in [29] wit multi-mode control to additionally provide ZVS for the input devices and improve gain. On the other hand, it suffers from hard switching transients and insufficient utilization of rectifier transistors.

A phase-shift modulation bidirectional dual inductor current fed push-pull (DIPP) converter was proposed in [30]. The advantage of the solution lies in high conversion ratio and soft switching of all semiconductors for both directions of power flow. The results presented in [30] are comprehensively extended including more theoretical analysis, simulation, and experimental results. The converter prototype was designed to meet the application parameters of residential energy storage

system based on 25.6 V Lithium Iron Phosphate ($LiFePO_4$, LFP) battery. The operation principle of the converter for both directions of power flow is presented in Section II, followed by case study design procedure in Section III. The experimental verification and performance analysis are presented in Section IV to verify the operation of the proposed solution.

II. Description of Operation

The proposed converter topology is shown in Fig. 1. It consists of the CF dual inductor push-pull switching stage at the input low-voltage side and the active voltage doubler rectifier at the output voltage-fed (VF) side. The converter features soft-switching operation of all semiconductor components in a wide range of the input voltage and power, while providing natural clamping of the input CF side switches. Galvanic isolation allows interfacing of low-voltage batteries to the DC bus with much higher voltage rating. Converter maintains soft-switching properties in bidirectional operating mode and provides continuous current at the battery terminals that are connected to the CF terminal of the converter. One of the goals of this paper is to show that this converter is competitive to the full-bridge counterpart [31] with the similar phase-shift modulation algorithm while the number of active components is reduced compared to it. Despite the fact that the number of switches is higher than in some other current fed dual inductor push-pull converters proposed topology features natural clamping of voltage overshoots on L_A and L_B and so does not require additional active clamping circuits. Output voltage regulation is achieved by controlling the duration of energy return intervals (when part of the energy is transferred from the output to the input terminal). Another feature is that the parasitic output capacitance of the switches S_3, S_4 can be used as snubber capacitors C1-C2 so there is no need in external snubbers. Turn off losses of S_3 and S_4 can be reduced with the help of lossless snubber capacitors.

In the boost operation mode the bottom transistors of the current-fed four-quadrant (4Q) switches (S1.2 and S2.2) operate as diodes during the transient intervals. In the buck operation mode the converter topology can be regarded as the VF isolated half-bridge with current doubler rectifier at the secondary side. In this mode top transistors of 4Q switches operate in synchronous rectification mode.

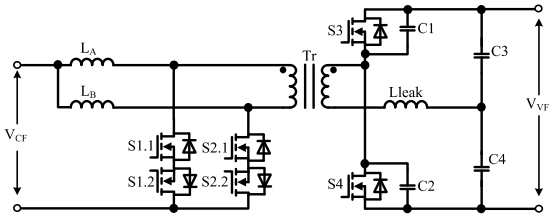

Fig. 1. Phase shift modulated dual inductor current fed push-pull converter.

A. Boost operation mode

This section describes the boost operation mode, when the energy is transferred from the current fed port (battery) to the voltage fed port (DC-bus). Generalized waveforms for this operation mode are shown in Fig. 2. The energy conversion process in boost operation mode can be described by the six intervals within a half of the switching period T_{SW}.

Interval 1 ($t_0 < t < t_1$, Fig. 2.). At the instant t_0 switch S2.2 is turned off. The body diode (BD) of S2.2 conducts the current. 4Q switch S1 is turned on with ZVS, assisted by the transformer leakage inductance. The inductor L_A is accumulating energy from the input through the 4Q switch S1. The inductors L_B is accumulating energy from current fed port through S1 and transformer primary winding. Switch S3 is still turned on and thus forces the transformer primary winding current redistribution between the 4Q switches, from S2 to S1.

Interval 2 ($t_1 < t < t_2$, Fig. 2.). At the instant t_1 current through S2 drops to zero causing BD of S2.2 to turn off naturally. Starting from this instant the converter is in reverse energy transfer mode (form VF to CF terminal). The inductor L_A is accumulating energy from CF terminal, while L_B is accumulating energy from the both CF and VF terminals. The switch S2.1 is not conducting current and can be turned off with ZCS. The duration of this interval should be long enough to ensure that current has sufficient time to redistribute in the whole converter operation range.

Interval 3 ($t_2 < t < t_3$, Fig. 2.). Switch S2.1 is turned off with ZCS. Processes in this interval are similar to the previous one and its duration defines the converter gain factor.

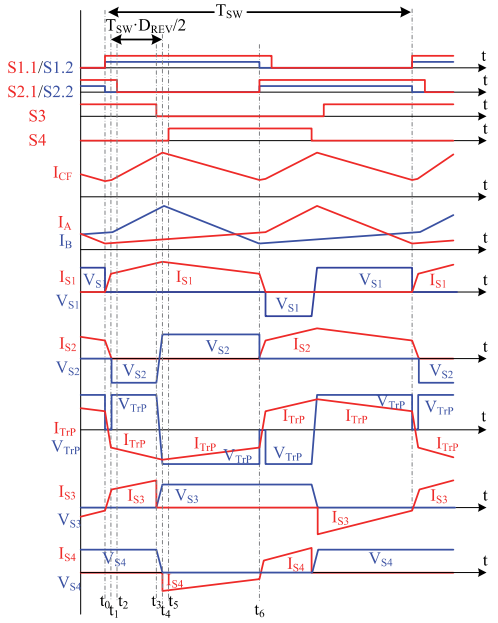

Fig. 2. Generalized waveforms in boost operation mode.

Interval 4 ($t_3 < t < t_4$, Fig. 2.). At the instant t_3 the switch S3 is turned off with capacitive snubber-assisted soft-switching.

This results in recharging of snubber capacitors C1 from zero to V_{VF} and C2 from V_{VF} to zero. The voltage polarity of the transformer windings is changed.

Interval 5 ($t_4 < t < t_5$, Fig. 2.). At the instant t_4 BD of the switch S4 starts conducting the transformer current and the power delivery mode starts. Energy stored in the inductor L_B is transferred to the VF terminal through the 4Q switch S1 and BD of the switch S4. This interval is required to ensure that the snubber capacitors will have enough time to recharge in whole converter operation range and should be optimized to minimize BD conduction losses.

Interval 6 ($t_5 < t < t_6$, Fig. 2.). The switch S4 is turned on with ZVS at the instant t_5. Energy is transferred from CF to VF terminal through 4Q switch S1 and switch S4. Afterwards the similar processes repeat for another half-period.

DC voltage gain of the CF part can be expressed as follows:

$$F_{REV} = \frac{V_{VF}}{2nV_{CF}} = \frac{1}{1-2\cdot(D_{REV} + t_{0-1} + t_{4-5} + t_{5-6})}, \quad (1)$$

where n is the transformer turns ratio, 2 is the voltage gain of the voltage doubler, D_{REV} is the duty cycle of the reverse energy transfer interval in boost mode (Fig. 2.), $t_{0\text{-}1}$ is the duration of the current redistribution interval (interval 1), $t_{4\text{-}5}$ is the duration of the snubber recharge interval (interval 5), $t_{5\text{-}6}$ is the duration of the inductor L_B energy release interval (D_A).

B. Buck operation mode

This section describes the reverse operation mode, when the power is transferred from VF to CF terminals (Fig. 3). This operation mode can used for battery charging in BESS.

Interval 1 ($t_0 < t < t_1$, Fig. 3.). At the instant t_0 the switch S2.1 is turned off. The body diode (BD) of S2.1 conducts the current. The 4Q switch S1 is turned on with ZVS, assisted by the transformer leakage inductance. The transformer current I_{TRp} is redistributing between the 4Q switches, from S1 to S2, and changes its sign. Transformer primary voltage drops to zero. The inductors L_A and L_B releasing the energy to the load.

Interval 2 ($t_1 < t < t_2$, Fig. 3.). At the instant t_1 current through the 4Q switch S2 drops to zero causing the BD of S2.1 to turn off. Power delivery mode starts. From this instant the switch S2.2 can be switched off with ZCS. Energy is transferred through the switch S4 and the 4Q switch S1 from VF to CF terminal. This interval is needed to ensure that the current through S2 drops to zero.

Interval 3 ($t_1 < t < t_2$, Fig. 3.). At the instant t_1 current through the 4Q switch S2 drops to zero causing the BD of S2.1 to turn off. Power delivery mode starts. From this instant the switch S2.2 can be switched off with ZCS. Energy is transferred through the switch S4 and the 4Q switch S1 from VF to CF terminal. This interval is needed to ensure that the current through S2 drops to zero.

Interval 4 ($t_2 < t < t_3$, Fig. 3.). Switch S2.2 is turned off with ZCS at the instant t_2. Power delivery mode continues.

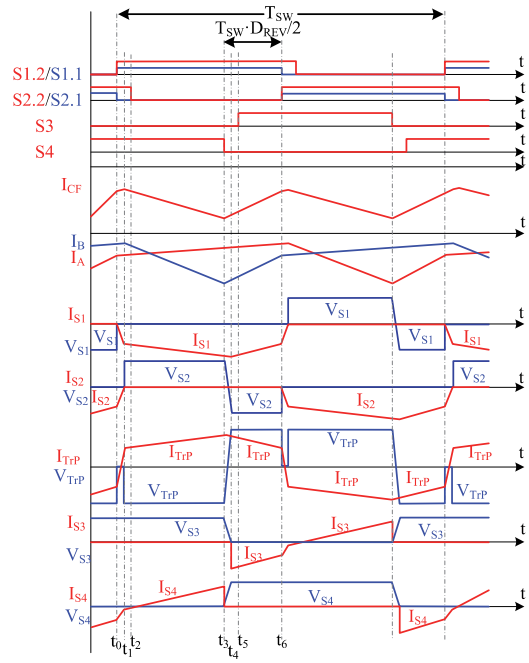

Fig. 3. Generalized waveforms in the buck operation mode.

Interval 5 ($t_3 < t < t_4$, Fig. 3.). The switch S4 turns off with capacitive snubber-assisted soft-switching at the instant t_3. This results in recharging of the snubber capacitors: C2 from zero to V_{VF} and C1 from V_{VF} to zero. Reverse energy transfer mode starts. The load current is maintained by L_A through 4Q switch S1. Energy accumulated in the inductor L_B is transferred from CF to VF terminal.

Interval 6 ($t_4 < t < t_5$, Fig. 3.). At the instant t_4 the transformer voltage polarity is changed causing BD of S3 to turn on. Power delivery mode starts, energy is transferred from VF to CF terminal. In this mode, the load current is the sum of the currents I_A and I_B. This interval is needed to ensure that snubber capacitors are recharged and should be optimized to minimize the BD conduction losses.

Interval 7 ($t_5 < t < t_6$, Fig. 3.). At the instant t_5 S3 turns on with ZVS. Reverse energy transfer mode continues with reduced conduction losses.

Similar to the boost operating mode, the equation for the normalized DC voltage gain of the converter operating in the reverse operation mode can be simplified to:

$$F_{REV} = \frac{2nV_{CF}}{V_{VF}} = 1-2\cdot(D_{REV} + t_{0-1} + t_{4-5} + t_{5-6}), \quad (2)$$

where D_{REV} is the duty cycle of the reverse energy transfer interval in buck mode (Fig. 3.), $t_{0\text{-}1}$ is the duration of the current redistribution interval (interval 1), $t_{3\text{-}4}$ is the duration of the snubber recharge (interval 5) interval, $t_{2\text{-}3}$ is the duration of the active energy transfer through transformer (interval 4).

III. Converter Design Aspects

Experimental prototype was designed for interfacing of the eight-cell $LiFePO_4$ battery into the 400V DC-bus. The converter was designed to cover the voltage range of the through the whole charge cycle.

The voltage of the of the eight-cell $LiFePO_4$ battery varies in a range of 20-30V. One of distinguished features of the $LiFePO_4$ batteries is that the output voltage remains almost constant on a level of 25.6V in a range of approximately 20-80% of its nominal capacity. LFP battery charge and discharge curves are shown in Fig. 5. Hence, the interface converter should be optimized for this operation voltage.

General parameters of the prototype are presented in Table I. The parameters of the semiconductor devices are listed in Table II. The experimental converter prototype in Fig. 4. is controlled by the STM32F334R8T6 microcontroller. The input and output current were measured by ACS716 and ACS712 current sensors, respectively and the voltages were measured with the isolated operational amplifier AMC1200. All the sensors were connected to the ADC converter integrated into the microcontroller through the active analog filters. CF side transistors are controlled with ADUM3221 dual channel galvanically isolated drivers. VF side transistors are controlled with ACPL-P346 drivers.

All the experimental waveforms were acquired with the digital oscilloscope Tektronix MSO4034B equipped with Rogowski coil current probe PEM CWTUM/015/R, current probe Tektronix TCP0030A, and high-voltage differential voltage probes Tektronix P5205A. Efficiency of the converter was measured while it was supplied from a DC power supply Elektro-Automatik EA-PSI 9080-60 in boost mode and from TDK-Lambda GEN600-5.5 in buck mode. Efficiency measurements were carried out with YOKOGAWA WT1800 high-precision power analyser.

TABLE I: PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

PARAMETER / COMPONENT	SYMBOL	VALUE
Input voltage	V_{CF}	20-30
Output voltage, V	V_{VF}	400
Switching frequency, kHz	f_{sw}	50
Primary side inductor, µH	L_A, L_B	44
Capacitance of the filter capacitor, uF	C_3,C_4	2.2
Capacitance of the snubber capacitor, pF	C_1,C_2	313
Equivalent capacitance (at TX primary), nF	C_{eq}	10
Transformer turns ratio	N_2/N_1	3.5:1
Transformer magnetizing inductance, mH	L_{TX_m}	3
Equivalent TX leakage inductance, µH	L_{leak}	10
Rated power, W	P_{rated}	500

TABLE II: SEMICONDUCTOR COMPONENTS OF THE EXPERIMENTAL PROTOTYPE

Component	Type	Specifications
S1.1 – S2.2	Infineon BSC093N15NS5	V_{DS}=150 V; $R_{DS(on)}$=9.3 mΩ I_D=87 A, t_{rr}= 49ns, C_{OSS}=604pF
S3 – S4	Infineon: IPP65R225C7	V_{DS}=650 V; $R_{DS(on)}$=225 mΩ I_D=41 A, t_{rr}=890ns, $C_{O(tr)}$=313pF

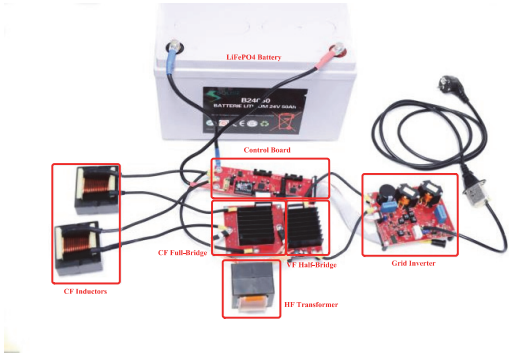

Fig. 4. Experimental converter prototype.

To ensure soft-switching operation of DC-DC converter with this mission profile the operating duty-cycles were pre-defined. The minimal CF side transistors duty cycle (D_{CF}) is determined by the maximal CF port current and can be calculated as follows:

$$D_{CF(min)}=0.5+\frac{1}{N}\cdot\frac{L_{Lkeq2}\cdot\left(V_{CF}^2+8\cdot L_1\cdot P_{rated}\cdot f_{sw}\right)}{4\cdot L_1\cdot V_{CF}\cdot V_{VF}}, \quad (3)$$

where $N=N_2/N_1$ is the transformer turns ratio, $L_{Lkeq2}=L_{Lk2}+L_{Lk1}\cdot N^2$ is the transformer equivalent leakage inductance, P_{rated} is the converter rated power, L_1 is the input inductance value.

The maximal VF side transistors duty cycle (D_{VF}) is limited by the transistors equivalent output capacitance and minimal CF side current. Maximal D_{VF} can be calculated as follows:

$$D_{VF(max)}=\frac{1}{2}-N\cdot\frac{2\cdot C_s\cdot V_{VF}\cdot f_{sw}}{\left(I_{L1avg}+\Delta i_{L1}/2\right)}, \quad (4)$$

where C_s is the equivalent VF-side switch capacitance, $I_{L1avg}=P_{rated}/V_{CF}$ is the average input current, Δi_{L1} is the input current ripple.

The phase shift between the CF and VF control signals in the boost and buck modes is determined by

$$D_{offset}^{Boost}\geq D_{CF(min)}-\frac{D_{VF}+D_{CF}}{2}, \quad (5)$$

$$D_{offset}^{Buck}\geq\frac{D_{CF}+D_{VF}}{2}-D_{VF(max)}, \quad (6)$$

where D_{CF} and D_{VF} are the actual duty cycles of the transistors at the CF and VF sides, respectively.

The interval of energy return in the boost and buck modes is estimated by

$$t_{rev}^{Boost}=\frac{1}{f_{sw}}\cdot\left(\frac{D_{VF}-D_{CF}}{2}+D_{CF}-D_{CF(min)}+D_{offset}^{Boost}\right), \quad (5)$$

$$t_{rev}^{Buck}=\frac{2\cdot\left(D_{offset}^{Buck}+D_{VF(max)}\right)-D_{CF}-D_{VF}}{2\cdot f_{sw}}, \quad (6)$$

Based on equations (3) and (4), the dependency of the soft switching range of the converter on the boundary duty cycles

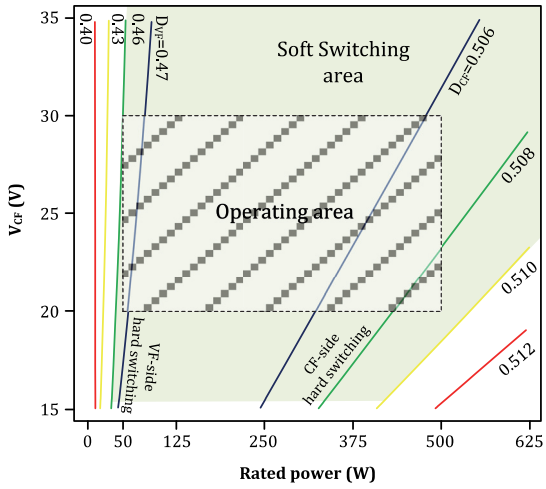

Fig. 5. Converter soft-switching boundaries

values was calculated (Fig. 5.). Converter operating area is marked as a shaded rectangle. According to the calculations, to ensure soft-switching in the whole operation area, CF duty cycle should be 0.51 or higher and VF duty cycle should be 0.46 or lower. These values were used in transistor modulation sequences during experiments.

IV. Experimental Verification

Transient waveforms of the transistor S1.1 turn-on and turn-off processes are shown in Fig. 6. and Fig. 7,respectively. These waveforms correspond to operation point with V_{CF}=20V and P_{CF}=500W, that has the highest current in the CF side transistors. It is clear that the slope of the current resultsi in soft switching conditions for the CF transistor with a given duty-cycle (0.51). This proves that the equation (3) is valid.

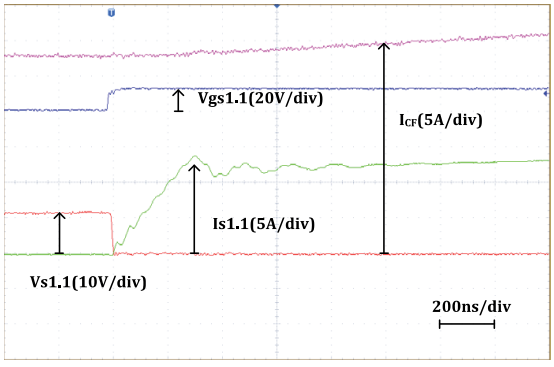

Fig. 6. S1.1 current and voltage and driving waveforms during the transistor turn-on in boost mode(V_{CF}=20 V, P_{CF}=500 W).

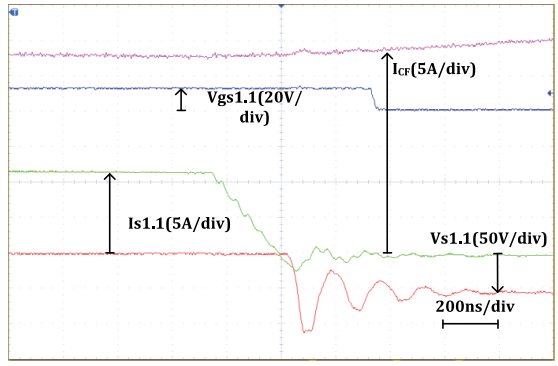

Fig. 7. S1.1 current, voltage and driving waveforms during the transistor turn-off in boost mode (V_{CF}=20 V, P_{CF}=500 W).

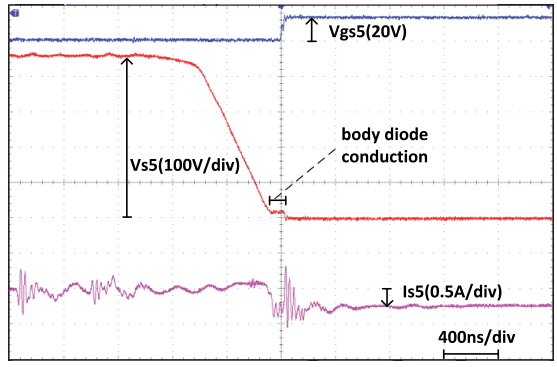

Fig. 8. S5 current, voltage and driving waveforms during transistor turn-on (V_{CF}=30 V, P_{CF}=50 W).

Steady-state waveforms of the transistor S5 turn-on process are shown in Figs 8. Those waveforms show the second critical point that represents the operating mode with the lowest current in the CF transistors (V_{CF}=30 V, P_{CF}=50 W). In this mode, the most critical switching transition is the turn-on of the VF side transistors. The transistor should not be turned on earlier than its output capacitor will be discharged and the body diode will start conducting. As can be seen the calculated VF transistors duty cycle value of 0.46 produces enough deadtime for the equivalent output capacitance of the transistor to fully discharge before switching it on. The small safety interval where the diode is conducting as shown in Fig. 8. This experiment proves that the equation (4) is valid.

The converter operating waveforms at nominal voltage (V_{CF}=25.6 V) are shown in Fig. 9. and Fig. 10. They correspond to generalized theoretical waveforms presented in Section II.

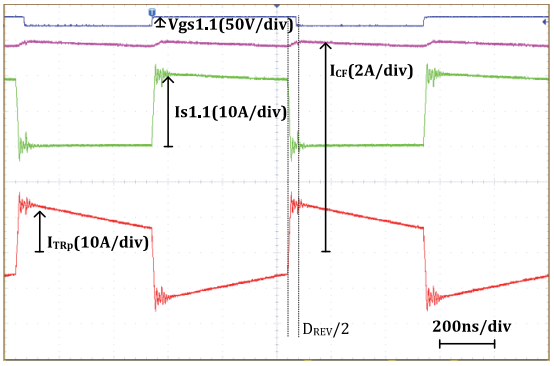

Fig. 9. Waveforms of the input current and transformer current in boost mode,(V_{CF}=25.6 V, P_{CF}=500 W).

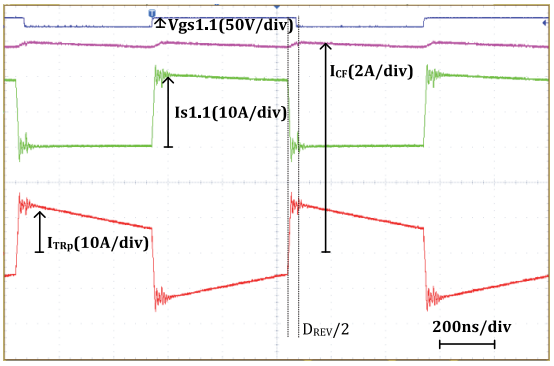

Fig. 10. Waveforms of the current fed port current and transformer primary voltage and current in boost mode,(V_{CF}=25.6 V, P_{CF}=500 W).

Fig. 11. shows the efficiency of the converter. The right half plane represents the discharge mode (energy transfer from CF to VF port) while the left one corresponds to the battery charging mode (energy transfer from VF to CF port). As can be seen, the DC-DC stage reaches its peak efficiency at around 150 W in both transfer directions. Efficiency drop toward lower voltage and higher power levels happens due to the increased conduction losses on the semiconductors. Efficiency drop towards the low power can be explained by the increased contribution of the circulating energy in the converter. As this interval remains the same for all power and voltage levels, so it is somewhat

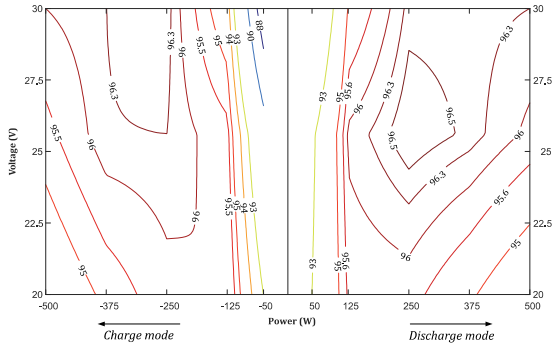

Fig. 11. Experimental converter efficiency

redundant at the low power levels. This can be addressed with the optimized control strategy that will adjust D_{VC} and D_{CF} on the fly and incorporates variable DC-bus voltage level to achieve maximum performance over the whole operation range.

One of the advantages of the proposed topology is that it can operate even without load at the voltage fed port in boost mode which is uncommon for current fed topology. This improves handling of fault states and beneficial in applications that have fast changing load or require hot-swap power module replacement. This advantage is not achievable in other topologies with a similar phase-shift modulation such as full bridge current fed [31].. It is possible because the current circulating between CF side inductors through the transformer is helping to recharge parasitic snubber capacitors of the VF side transistors (interval 4 in the boost mode) as shown in Fig. 13. and Fig. 14. Even though currents in the current fed inductors are significant they are phase shifted and compensating each other so average current at the CF terminal is zero. In this operation mode soft-switching in the VF side transistors is lost but is due to the low current it will not damage converter. During experiments it was measured that the converter dissipates around 3W of power due to this circulating current in case of no-load operation.

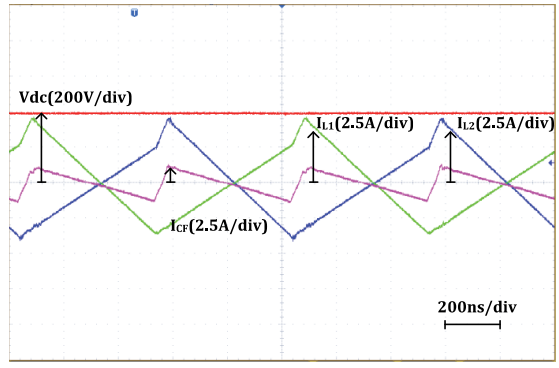

Fig. 13. Input currents waveform in boost mode at no load operation.

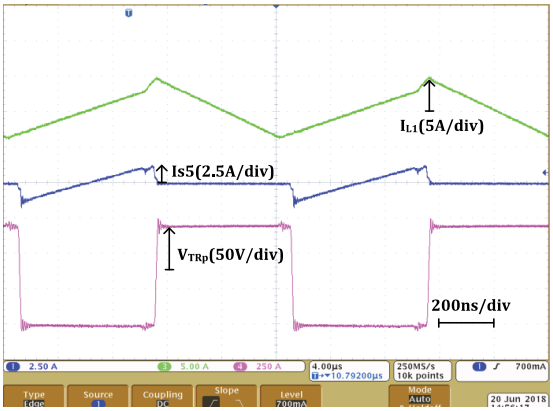

Fig. 14. Waveforms of the transformer input voltage and current through S5 in boost mode at no load operation.

V. Conclusions

An isolated bidirectional dual inductor current fed push-pull DC-DC converter for battery energy storage systems was analysed and experimentally verified. The proposed converter features phase shift modulation method that utilises transformer leakage inductance and transistor parasitic capacitances to enable soft-switching of all semiconductors in a wide range of the input voltage and power. The experiments shown that converter preserves soft-switching operation in a range of input power from 50 to 500 W and current fed port voltage from 20 to 30V. This confirms the viability of the proposed design approaches.

The converter demonstrated peak efficiency of 95.9% and 95.3% at maximum power at 25.6V in the boost and buck modes respectively. The peak efficiency is higher than 96.3% in both bodes at approximately half power. Additional benefit of the proposed topology is that it can safely operate with no load in boost mode.

Acknowledgment

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[PAPER-VII] Kosenko R., Blinov A., Korkh O., Experimental Verification of Two-Stage Power Converter With Current-Fed Soft-SwitchingFront-End for Battery Storage Applications, EPE'18 ECCE Europe, 2018.

Experimental Verification of Two-Stage Power Converter with Current-Fed Soft-Switching Front-End for Battery Storage Applications

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Keywords

«Current-fed», «dc-ac converter», «bidirectional converter», «soft-switching», «ZVS», «ZCS», «battery», «switching control method», «naturally clamped»

Abstract

This paper presents a two-stage power system that consists of a novel bidirectional current-fed DC-DC converter module for interfacing with lithium iron phosphate battery, followed by a single-buck inverter for grid interface. Additional benefit of the proposed two-stage converter lies in the intermediate DC-link between two stages that allows connection of other energy sources, such as PV. The proposed converter offers galvanic isolation, high voltage step-up factor and power factor correction. The operation principle and control system structure of the case study converter are described. Due to the accommodation of a special phase-shift modulation algorithm, the proposed front-end converter features natural voltage clamping and soft-switching of all semiconductor devices without additional components such as snubbers and clamping circuits. Parameters of the converter were estimated in accordance with residential battery energy storage system requirements. A 500W prototype converter was developed to validate theoretically estimated characteristics of the converter, including the soft-switching range, transfer function and design constraints. Experimental waveforms as well as efficiency for both charge and discharge operation modes are presented and analysed.

Introduction

Many countries are introducing new legislation towards energy saving technologies in residential and small commercial buildings. For example, the directive 2010/31/EU demands from EU states to minimize environmental footprint of new buildings and introduces new requirements to all new buildings commissioned after the year 2020 to be nearly zero energy buildings [1]. As a result, residential buildings of the future have to balance their energy consumption with energy production. Aside from implementation of new materials in construction to minimize energy consumption in buildings, electricity generation from the renewable and alternative energy sources (like wind, photovoltaic (PV), fuel cells, etc.), another important and convenient way is to achieve nearly-zero energy consumption goal. Also, such buildings are expected to perform the demand side management functions, like peak shaving, valley filling, load shifting, prioritizing of loads, etc. [2]. Hence, a paradigm shift is expected in the electric grid architecture from a centralized to an extremely dispersed generation pattern. As a result, residential energy storages will be in great need within the nearest future. Recently, residential battery energy storage systems (BESSs) have been often recommended in combination with rooftop solar PV installations [3]. This market is growing and provides numerous products at different power levels and technologies from such companies as Tesla, Sonnen, Enphase and others.

There are two types of residential BESSs (RBESSs): single-stage and multi-stage systems. The single-stage systems have higher efficiency and power density but are limited in functionality. RBESSs are usually based on low voltage batteries for better safety. Therefore, they generally utilize multi-stage power conversion: the step-up bidirectional DC/DC converter and the grid side DC/AC inverter.

Multi-stage systems are costlier but can offer many additional features. For example, presence of DC-link in the system allows effective decoupling of double grid frequency ripple, correcting the form and power factor of consumed grid current. Additionally, intermediate DC-link bus allows to connect additional energy sources such as photovoltaics. Due to the popularity of PV in residential installations and DC nature of PV modules, they can be easily integrated to such systems. This approach can easily justify additional cost of a multi-stage system by sharing a grid inverter between the battery and the PV energy sources.

As for battery chemistry for a RBESS Lithium Iron Phosphate ($LiFePO_4$, LFP) batteries are a very promising option. They are currently under comprehensive research and development due to very good characteristics for such applications: high safety and long lifetime. The results shown in [4] demonstrate superior temperature stability of LFP chemistry as compared to other Li-ion battery technologies, although special attention is required to protect cells against overcharge and short-circuit. Another property of LFP batteries is open circuit voltage that remains almost constant when state-of-charge ranges from 20 to 80%. In addition, there is an apparent hysteresis between charging and discharging voltages. As a result, an accurate estimation of the state of charge is quite complicated and possible methods are addressed in [5]-[9]. Other notable topics of research include lifetime estimation models [10],[11] and fast charging techniques [12][14]. The feasibility of LFP battery integration in stand-alone photovoltaic systems is evaluated in [13] and proposed as viable for storage systems up to 1 kWh. In [15] the influence of low frequency current ripple caused by grid-side inverter is evaluated. According to the results, even extreme current ripple values had a minor influence on the battery performance.

The converter proposed in this paper is based on a novel soft-switching current-fed front-end converter and a single-buck grid inverter. It allows bidirectional energy transfer, high voltage step-up factor, soft-switching in all semiconductors, and active power factor correction that make it a good candidate for a residential BESS based on a low voltage battery. This paper is focused on the control strategy and performance evaluation of the proposed front-end converter as an interface for a low voltage battery. In our research, this converter will be a part of the microgrid with the additional PV power port connected to the DC-link.

Converter Control System Description

The converter consists of two stages connected to the intermediate DC-link (Fig. 1.). The first stage is a current-fed (CF) soft-switching converter [23] that incorporates bidirectional switches. The second stage is a single-buck inverter. This paper is focused on the control strategy and performance evaluation of the proposed front-end converter as an interface for a low voltage battery. The converter here will be a part of the microgrid with the PV power port connected to the DC-link. Thus, it will interconnect residential DC-bus, BESS, PV and the AC distribution grid. Different renewable energy sources and energy storage devices, such as photovoltaic panels, wind turbine fuel cells and batteries, could be connected to the DC-grid [6-8]. This allows most optimal utilization of power electronics as there will be common grid inverter for multiple DC sources and energy storage. This paper analyses a system with a single battery connected to the DC-bus.

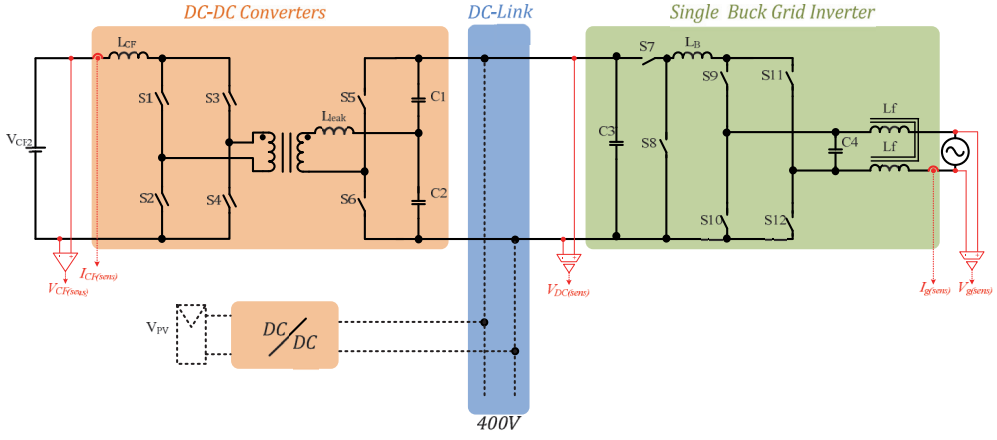


Fig. 1. Two-stage converter topology.

Simplified control system diagram for the discharge mode is shown in Fig. 2a. The control system of the grid side inverter incorporates SOGI PLL to generate the output voltage synchronous to the grid voltage. Proportional-resonant regulator (PR) regulates converter output voltage to achieve output current with low total harmonic distortion. Protective state-machine block is constantly monitoring the battery and grid parameters and if one of them goes beyond the acceptable level, the converter will be immediately switched off.

A simplified control system diagram for the charge mode is shown in Fig. 2b. In the charge mode, SOGI block controls the grid side inverter; thus, it acts as a controlled synchronous rectifier with boost functionality.

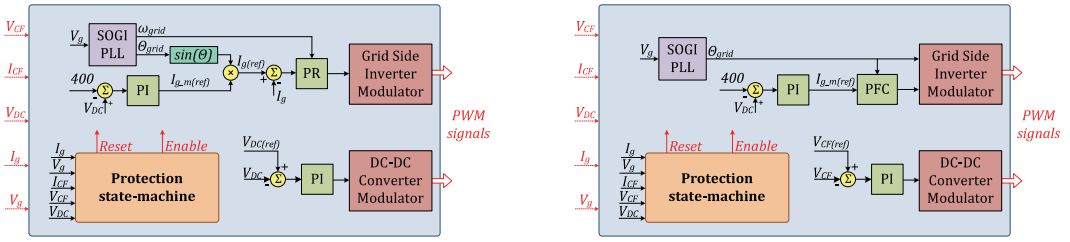


Fig. 2. Control system structure in the discharge a) and charge b) modes.

Control sequence of the front-end DC-DC converter was described in [23]. This sequence enables soft-switching of all transistors in a wide range of the input voltage and power. The converter features an active voltage doubler rectifier, which is controlled by the switching sequence synchronously to he input-side switches. The DC-bus represented by the capacitor C3 is operated at constant voltage.

Control sequence of the grid side inverter in the discharge mode is shown in Fig. 3a. Sine wave modulation is done by switch S_7. Switches S_9-S_{12} act as unfolder, changing the output voltage polarity twice per grid period. In such approach, only one switch is working at high frequency (20 kHz) and all the others are switched with grid frequency. This allows us to minimize switching losses and increase total system efficiency.

The control sequence of the charge mode is shown in Fig. 3b. In this mode, the grid inverter is working as a controlled rectifier. S7 is switched off. Switches S_{10} and S_{12} are modulated as synchronous rectifier according to the grid voltage angle calculated by a single order general integrator phase-locked loop (SOGI PLL) algorithm. S8 is modulated by PFC controller to provide an additional boost of the grid voltage to obtain the DC-link voltage of 400 V.

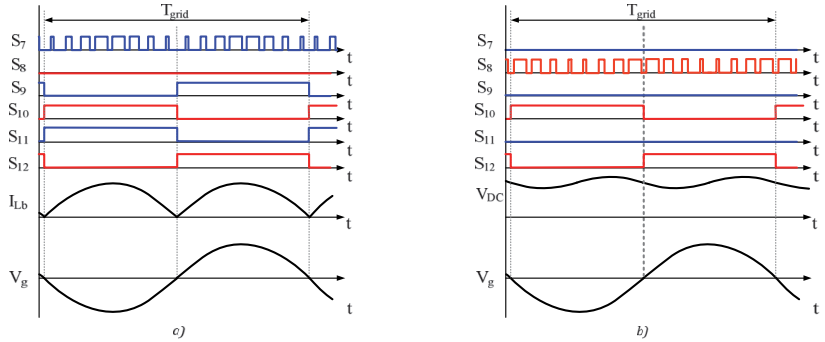


Fig. 3. Generalized waveforms of the grid inverter in the discharge a) and charge b) modes.

Experimental Results

A. Experimental setup

Experimental prototype was designed for interfacing of the $LiFePO_4$ batteries into the AC-grid. The converter was designed to cover the voltage range of the eight-cell $LiFePO_4$ battery, starting from the full charge to the deep discharge.

The experimental converter prototype is shown in Fig. 4 consists of the control board, the full bridge high frequency inverter, the controlled voltage-doubler rectifier and grid side inverter boards.

The parameters of the semiconductor devices are listed in Table I. General operation parameters of the prototype are presented in Table II. One of the main goals was to build a cost-effective system, therefore, traditional low-cost silicon semiconductor switches were used. The converter is controlled by the STM32F334R8T6 microcontroller from STMicroelectronics. The input and output current were measured by ACS716 and ACS712 current sensors, respectively. The input and output voltages were measured with the isolated operational amplifier AMC1200. All the sensors were connected to the ADC converter integrated into the microcontroller through the active analog filters.

All the experimental waveforms were acquired with the digital oscilloscope Tektronix MSO4034B equipped with Rogowski coil current probe PEM CWTUM/015/R, current probe Tektronix TCP0030A, and high-voltage differential voltage probes Tektronix P5205A. For efficiency measurements of the converter stages, it was fed from a DC power supply TDK-Lambda GEN600-5.5, Elektro-Automatik EA-PSI 9080-60 and utility grid in different tests. Power stage efficiency was measured with YOKOGAWA WT1800 power analyser.

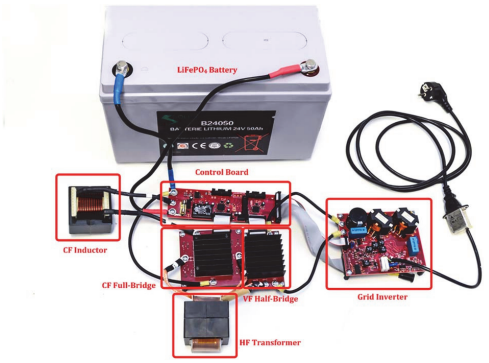


Fig. 4. Experimental converter prototype.

TABLE I: Types and Parameters of Semiconductor Devices Used

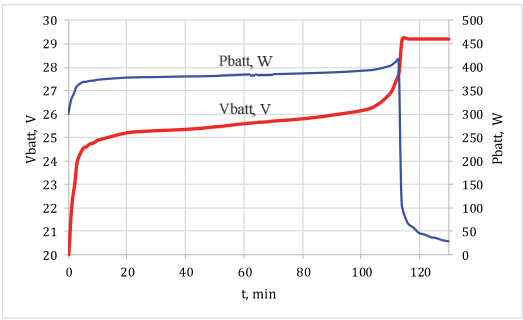
Component	Type	Specifications
S1.1 – S4.2	Infineon BSC035N10NS5	V_{DS}=100 V; $R_{DS(on)}$=3.5 mΩ I_D=100 A, t_{rr}= 62 ns, C_{OSS}=770pF
S5 – S11	Infineon: IPP65R225C7	V_{DS}=650 V; $R_{DS(on)}$=225 mΩ I_D=41 A, t_{rr}=890ns, $C_{O(tr)}$=313pF

Table II: Operating parameters of the experimental converter

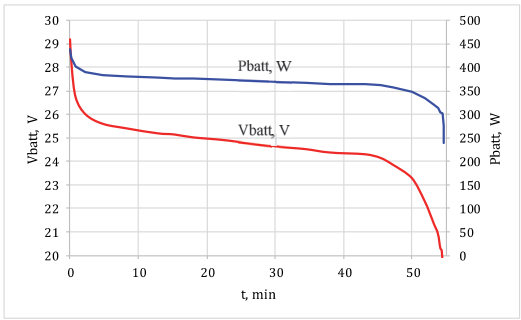
Parameter	Symbol	Value
Converter power rating, W	P	500
Input voltage, V	V_{CF}	20-30
DC-bus voltage, V	V_{DC}	400
Output RMS voltage, V	V_G	230
Switching frequency DC-DC, kHz	f_{SW}	50
Switching frequency DC-AC, kHz	f_{SW}	20
Transformer turns ratio (Ns /Np)	N	33/6
Transformer magnetizing inductance,	L_{TX_m}	930
Transformer leakage ind., nH	L_{leak}	430
Inductance of boost inductor, uH	L_{CF}	100
Capacitance of filter capacitor, uF	C_1,C_2	2.2
Capacitance of DC-link capacitor, uF	C_3	150

B. Test profile and definition of the operating parameters

The nominal operational voltage of the selected battery is 25.6 V. During normal operation, the voltage of the battery should not drop below 20 V and rise above 30 V to avoid deep discharge and overcharge conditions. The battery charge and discharge curves at n are shown in Fig. 5. In the systems with the demand-side control, the battery is typically charged at the maximal possible rate in order to keep the battery energy storage system always ready to support the grid with the minimal idle time. The discharge of the battery, on the other hand, can be done at any possible rate depending on the energy demand.



a)



b)

Fig. 5. 8-cell LiFePO4 battery charge a) and discharge b) profiles.

To ensure soft-switching operation of DC-DC converter with this mission profile the modulation sequence duty-cycles was calculated. The minimal CF side transistors duty cycle (D_{CF}) is determined by the maximal CF port current and can be calculated as follows:

$$D_{CF(min)}=0.5+\frac{1}{N}\cdot\frac{L_{Lkeq2}\cdot\left(V_{CF}^2+8\cdot L_1\cdot P_{rated}\cdot f_{sw}\right)}{4\cdot L_1\cdot V_{CF}\cdot V_{VF}}, \quad (1)$$

where $N=N_2/N_1$ is the transformer turns ratio, $L_{Lkeq2}=L_{Lk2}+L_{Lk1}\cdot N^2$ is the transformer equivalent leakage inductance, P_{rated} is the converter rated power, L_1 is the input inductance value

The maximal VF side transistors duty cycle (D_{VF}) is limited by the transistors equivalent output capacity and minimal CF side current. Maximal D_{VF} can be calculated as follows:

$$D_{VF(max)}=\frac{1}{2}-N\cdot\frac{2\cdot C_s\cdot V_{VF}\cdot f_{sw}}{\left(I_{L1avg}+\Delta i_{L1}/2\right)}, \quad (2)$$

where C_s is the equivalent VF-side switch capacitance ($C_{O(tr)}$ in device datasheet), $I_{L1avg}=P_{rated}/V_{CF}$ is the average input current, Δi_{L1} is the input current ripple.

The phase shift between the CF and VF control signals in the boost and buck modes is determined by

$$D_{offset}^{Boost}\geq D_{CF(min)}-\frac{D_{VF}+D_{CF}}{2}, \quad (3)$$

$$D_{offset}^{Buck}\geq\frac{D_{CF}+D_{VF}}{2}-D_{VF(max)}, \quad (4)$$

where D_{CF} and D_{VF} are the actual duty cycles of the transistors at the CF and VF sides, respectively.

The interval of energy return in the boost and buck modes is estimated by

$$t_{rev}^{Boost}=\frac{1}{f_{sw}}\cdot\left(\frac{D_{VF}-D_{CF}}{2}+D_{CF}-D_{CF(min)}+D_{offset}^{Boost}\right), \quad (5)$$

$$t_{rev}^{Buck}=\frac{2\cdot\left(D_{offset}^{Buck}+D_{VF(max)}\right)-D_{CF}-D_{VF}}{2\cdot f_{sw}}, \quad (6)$$

Based on equations (1) and (2), the dependency of the soft switching range of the converter on the boundary duty cycles values was calculated (Fig. 6.). Converter operating area is marked as a shaded rectangle with two critical points highlighted by a circle. According to calculations, to ensure soft-switching in the whole operation area, CF duty cycle should be 0.515 or higher and VF duty cycle should be 0.47 or lower. For an experimental verification, values of D_{CF}=0.53, D_{CV}=0.46 were chosen. These duty-cycles provide an additional safety margin; as a result, the regulation range decreases and the amount of energy circulation are insignificant.

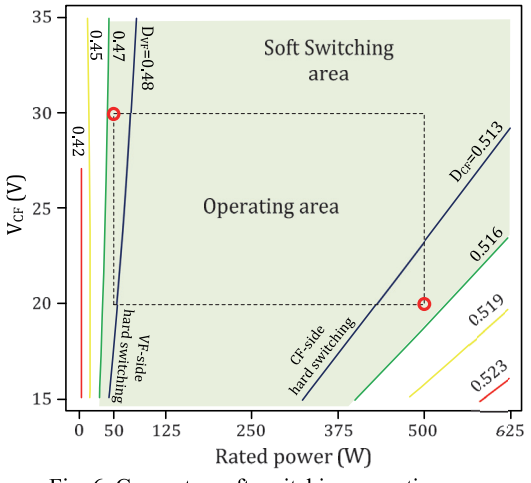


Fig. 6. Converter soft-switching operation range.

The theoretical DC-DC converter gain in the discharge mode can be expressed by [23]:

$$G_{CF} = N \cdot \frac{2}{1 - D_s - D_d - 2 \cdot D_{rev}}, \quad (7)$$

where D_S – CF side shoot-through duty-cycle, D_d – duty cycle of the VF transistor output capacitor recharge interval, D_{rev} – duty cycle of phase-shift interval, 2 – voltage doubler gain, N -transformer turns ratio, $D_d = 2 \cdot t_d / T_{sw}$, T_{sw} – switching period duration, t_d – duration of the recharge interval of the VF transistor output capacitor.

The theoretical DC-DC converter gain in the charge mode can be expressed by:

$$G_{VF} = \frac{1}{2 \cdot N} \cdot \left(1 - D_s - D_d - 2 \cdot D_{rev}\right), \quad (8)$$

C. Steady-state operating waveforms

Transient waveforms of the transistor S1.1 turn-on process are shown in Fig. 7. Those waveforms are acquired in the first critical point of the operating area. This point is V_{CF}=20V, P_{CF}=500W and it corresponds to the operating mode with the highest current through the CF side transistors. The slope rate of the CF side transistor current is 78.1 A/us, which gives the rise time of 320 ns four times per switching period [23] or 1280 ns in total. In other words, this leads to the duty-cycle loss of 0.064 on the CF side switches. This slope should be added to limits the duty-cycle of CF transistor to ensure that current has time to fall down to zero in one converter leg and grow to input current in another leg by those preserving soft-switching transition [23]. The 320 ns slope added to 50% duty-cycle modulated signal will give the minimal duty-cycle of CF transistor at 50 kHz of 0.516. This is close to the calculated value 0.515 and proves that equation (1) is valid.

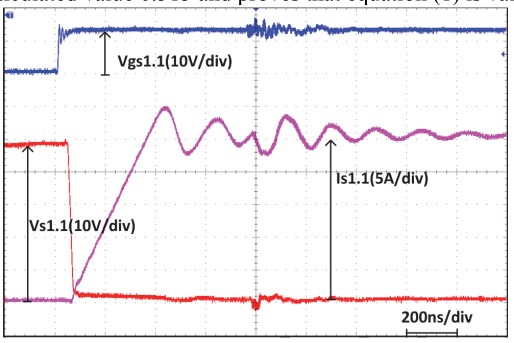


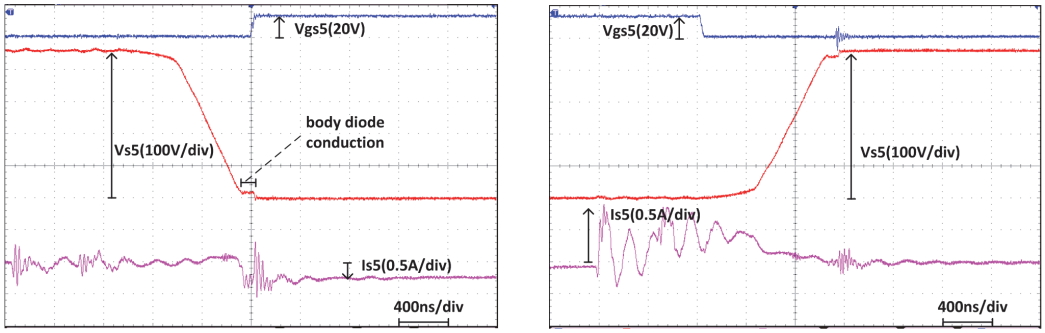
Fig. 7. S1.1 current and voltage and driving waveforms during the transistor turn-on (V_{CF}=20 V, P_{CF}=500 W).

Steady-state waveforms of the transistor S5 turn-on and turn-off process are shown in Figs. 8a. and 8b, respectively. Those waveforms show the second critical point that represents the operating mode with the lowest current in the CF transistors (VCF=30 V, PCF=50 W). In this mode, the most critical switching transition is the turn-on of the VF side transistors [5]. The transistor should not be turned on earlier than its output capacitor will be discharged and the body diode will start conducting. At the given parameters, the recharge rate of the output capacitors of the VF side transistors is 1375 V/us. This gives a slope of 320 ns, as can be seen in Fig. 8. This slope is present on both turn-on and turn-off transitions and thus the maximal VF transistor duty-cycle at 50 kHz switching frequency with a measured slope should not be higher than 0.47 to prevent VF transistors from short-circuiting VF port during those slopes [23]. This critical duty cycle is close to the calculated value (0.47) and proves that equation (2) is valid.

As shown in Fig. 8, a duty cycle selected for experimental verification D_{VF}=0.46. In the most critical point of the operating area (VCF=30 V, PCF=50 W), the equivalent output capacitor of the transistor S5 has enough time to recharge. After recharging, the body diode of the transistor S5 starts conducting and only then S5 is turned on with ZVS. The interval when the current is flowing through the body diode acts as a safety margin introduced in the modulation sequence to ensure robust ZVS of VF side transistors at the low power. At the higher operating power, the discussed slope rate will increase.

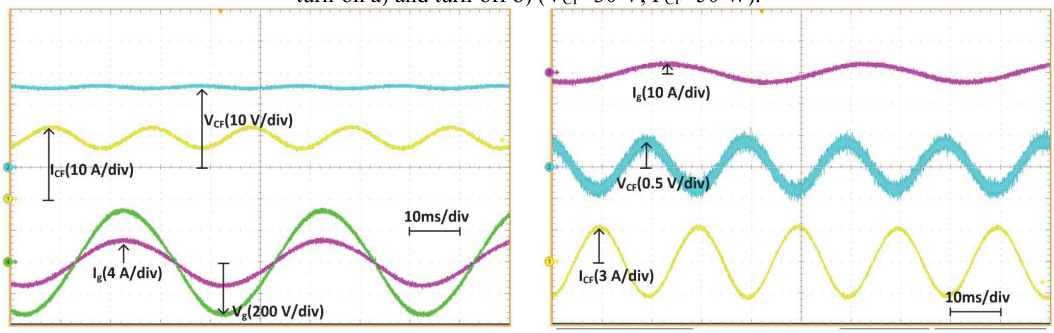
Input and output current and voltage waveforms in discharge mode are shown in Fig. 9. Waveforms for the charge mode are shown in Fig. 9b. AC-components of voltages and current of the converter in the discharge mode with V_{CF}=25.6V are shown in Fig. 9. Input current ripple is 30% and DC-bus voltage ripple is 6%.

Grid voltage and the current consumed from the grid by the inverter in the charge mode are shown in Fig. 10. As seen from the waveforms, the converter proposed has power factor correction and boost functionality to charge the DC-link up to 400 V from the 230 V grid. The figures show that the DC-bus voltage ripple is 5%. Fig. 10b. demonstrates that the quality of the current consumed by the inverter is much better than in passive rectifiers but still is not sinusoidal. Further improvement of the quality of the consumed current requires additional tuning of the PR regulator.



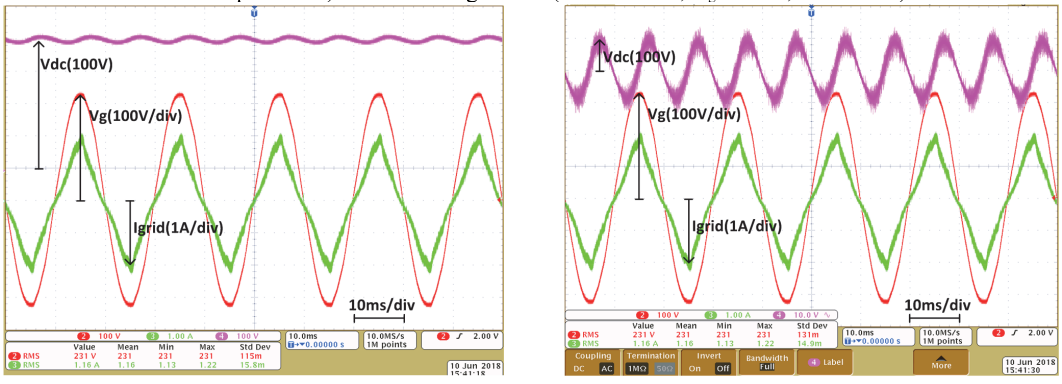
a) *b)*

Fig. 8. S5 current and voltage and driving waveforms during transistor turn-on a) and turn-off b) (V_{CF}=30 V, P_{CF}=50 W).



a) *b)*

Fig. 9. Waveforms of the converter input and output currents and voltages a) and their AC-components b) in the discharge mode (V_{DC} = 400 V, V_g=230 V, P = 500 W).



a) *b)*

Fig. 10. Waveforms of the converter output current and voltage and DC-link voltage a) and their AC-components b) in the charge mode (P=250 W).

D. Power stage performance characterization

Fig. 11. shows the efficiency of the DC-DC stage. The right half plane represents the discharge mode (CF to VF port) while the left one corresponds to the transfer direction of the battery charging energy (VF to CF port). As can be seen, the DC-DC stage reaches its peak efficiency at around 150 W in both transfer directions. Efficiency drop toward lower voltage and higher power levels happens due to the increased conduction losses on the semiconductors. Efficiency drop towards the low power can be explained by the increased contribution of the reactive energy transfer interval on the circulating energy in the converter. As this interval remains the same for all power and voltage levels, so it is somewhat redundant at the low power levels. This can be addressed with the optimizer control strategy that will adjust D_{VC} and D_{CF} on the fly and incorporate variable DC-link voltage level to achieve maximum performance over the whole operation range. The efficiency of the grid inverter is shown in Table III.

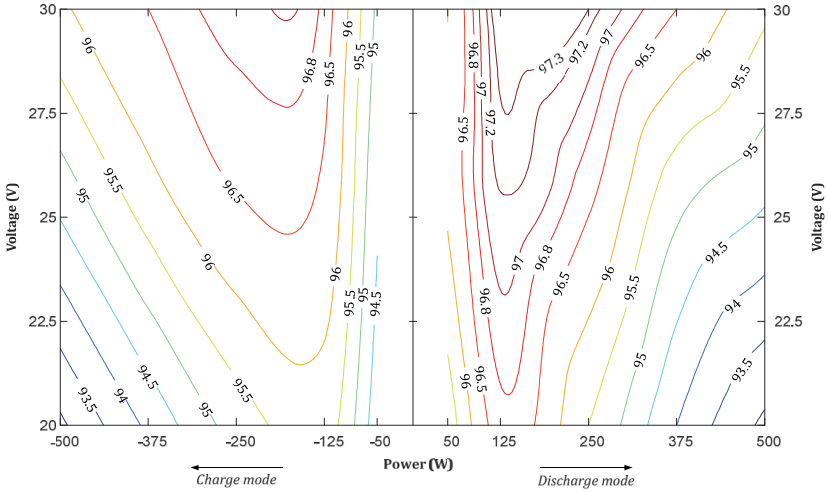


Fig. 11. Front-end DC-DC converter efficiency.

Fig. 12. compares the theoretical and experimental gain of the DC-DC converter, a) and b) for the discharge and charge modes, accordingly. The experimental gain is lower than that of theoretical and this difference increases with the power increasing. As the power grows and the voltage drops difference in theoretically precalculated and actual gain starts to grow. The reason is that the calculated gain does not take into account differences in the transformer parasitic capacitance in the equivalent output capacity of the VF transistors from sample to sample and the input current ripple is assumed to be zero. Additionally D_{CFmin} D_{VFmax} and t_{rev} modulation variables remains constant in all operating range. Close to the border of operating range those values are becoming significantly different from calculated values and thus affects the performance and gain of the converter. For example, in the point of the maximal CF side current (VCF=20 V, PCF=500 W) the actual interval of energy return t_{rev} is smaller than precalculated modulation variable, because the output capacitors of VF transistors are recharged faster with higher current in the circuit. This leads to the situation when excess time left in the energy return interval increases the converter.

Table III: Grid inverter efficiency measurements

Vdc, V	Vg, V	Pin, W	Discharge mode		Charge mode	
			m_index	η,%	m_index	η,%
400	230	500	0.830	98.3	0.810	97.7
400		375	0.824	98.6	0.735	97.6
400		250	0.805	98.8	0.401	97.4
400		125	0.685	99.0	0.252	96.1
400		50	0.430	98.5	0.140	93.5

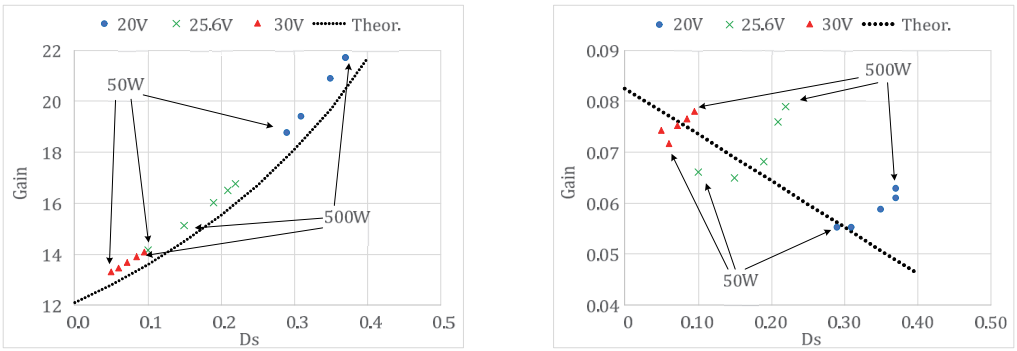


Fig. 12. Experimental and theoretical gain in the discharge (a) and charge mode (b).

Conclusion

A two-stage bidirectional DC-AC converter with a novel galvanically isolated current-fed front-end topology for residential battery storage applications was analysed. Conventional current-fed converters exhibit high voltage spikes at the end of the shoot-through state. The proposed converter features phase-shift modulation that provides clamping and soft switching of all semiconductors under a wide range of power and voltage levels. This is achieved without complex multi-mode modulation techniques and with low energy circulation. The presented control system and theoretical estimations were verified with the converter prototype that is intended to interface 25.6 V LFP battery with the grid. The experiments confirmed the viability of the proposed design approaches.

The experimental front-end stage demonstrated the efficiency of 95.6% and 95.9% at maximum power in the discharge and charge modes, respectively. The peak efficiency was over 97% at approximately half power in both modes. The second DC-AC stage is based on the single-buck inverter acting as a PFC rectifier when transferring power in the reverse direction. Due to only one semiconductor device operating with high switching frequency, the DC-AC stage reached the efficiency of 98.3% at maximum power and the whole system demonstrated the efficiency over 94.0% and 93.7% in the discharge and charge modes, respectively. Additional benefit of the two-stage converter lies in the presence of the intermediate DC-link between two stages, which allows connection of other energy sources, such as PV, to enable battery charging, avoiding DC-AC conversion stages.Further research will be directed towards battery state of charge and capacity estimation, active decoupling and PFC with harmonic compensation not addressed in the current study. In addition, soft start procedure that pre-charges the DC-link capacitor by the grid inverter is under development.

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Asymmetric Snubberless Current-Fed Full-Bridge Isolated DC-DC Converters

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***Abstract* – This paper presents two isolated current-fed full-bridge DC-DC converters that can be used to interface a lower voltage source into a DC bus of higher voltage. The first topology uses a resonant circuit to force current redistribution between low-voltage-side transistors and a passive rectifier. The second topology utilizes an active rectifier with secondary modulation to achieve the same goal. The resonant circuit can be formed by using transformer leakage inductance and the parasitic capacitances of the switches. The converters feature soft switching of semiconductors over a wide range of operating conditions. This is achieved with decreased energy circulation when compared to existing topologies with symmetric control and with fewer semiconductors than in those with phase-shift control. The topologies can be implemented in renewable, supercapacitor, battery, fuel cell, and DC microgrid applications. Steady-state operation and design aspects of the converters are presented and verified experimentally with 400 W prototypes.**

***Keywords* – DC-DC power converters; Soft switching; Zero-current switching; Zero-voltage switching.**

I. Introduction

Power electronic systems with a variable gain are required to interface different renewable energy sources or storage systems into the microgrid [1]. Converters with transformers are often preferred due to reduced stresses on the components and better flexibility of application [2], [3]. A significant portion of the past and present research that is related to isolated DC-DC converters is focused on voltage-fed dual-active-bridge (DAB) topologies [4]–[6]. These converters feature good regulation capabilities and soft switching over a wide range of operating conditions with advanced multi-mode digital control algorithms. At the same time, isolated current-fed (CF) converters could be beneficial due to their inherent boost capability, low input current ripple, reduced energy circulation, reduced requirements regarding the isolation transformer and simpler control system [7]–[9]. The present study is focused on full-bridge-type topologies due to their flexibility and scalability, making them suitable for a wide range of applications with various voltage and power levels. A common drawback of isolated CF topologies is related to voltage overshoots across primary transistors due to the leakage inductance of practical transformers. This issue is usually solved by applying a RCD snubber [10], the active clamp circuit introduced in [11] or solutions without snubbers, by utilizing the parasitic parameters of the circuit [14]–[17]. The latter approach is advantageous due to the reduced number of components required and the soft switching provided for power switches in the topology.

Existing snubberless (also referred to as “clampless”) converters can utilize the symmetric [12], [13] control algorithm or the phase-shift one [14]–[17]. In phase shift control, the primary switches need to have the reverse-blocking capability. Given the typical realization of this function (with a series diode or an anti-series switch), it leads to a remarkable increase in the total number of primary semiconductors and their power losses. On the other hand, at some operating points, symmetric topologies have excessive energy circulation and increased current stress on the primary switches and the transformer. In addition to the existing solutions, the present paper proposes two asymmetric topologies that combine the properties of both approaches and could provide an improved weighted performance, particularly if the converters have to operate under a wide range of input voltage and power levels. In this paper, operation with a full-bridge rectifier is assumed; however, the voltage-doubler rectifier can be applied for both converters as well. The operation principle of the topologies is described in Section II, design guidelines are presented in Section III and the experimental results are demonstrated in Section IV.

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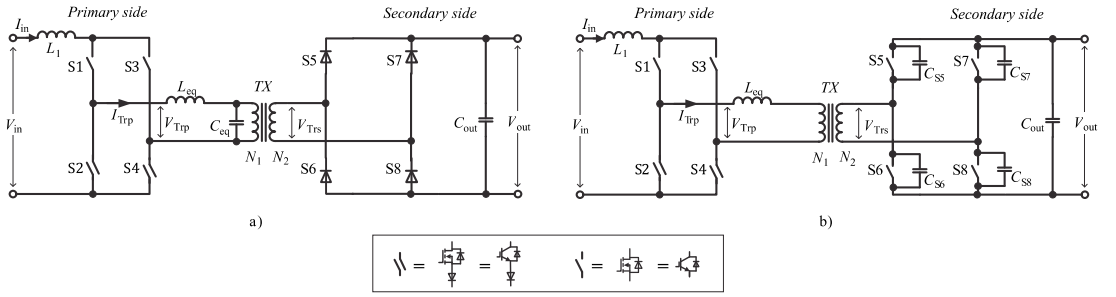

Fig. 1. Topology of the asymmetric converters proposed: ARPC (a), ASMB (b).

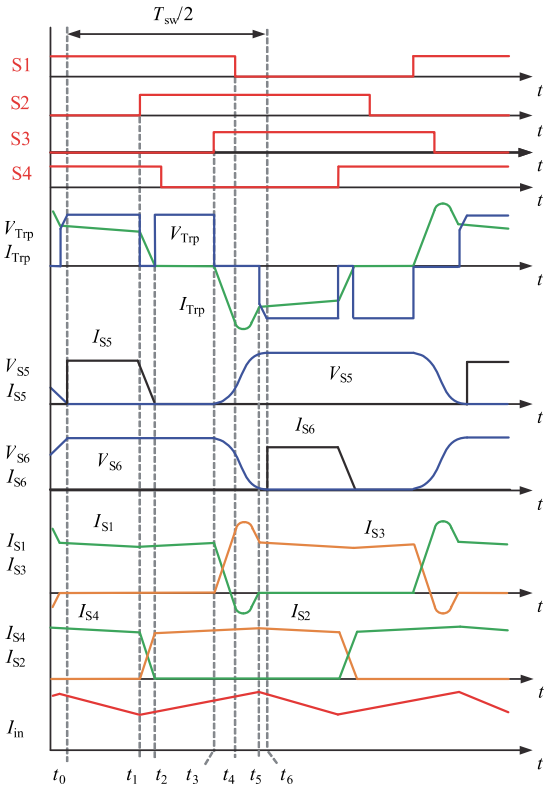

Fig. 2. Idealized operating waveforms of APRC with a passive rectifier.

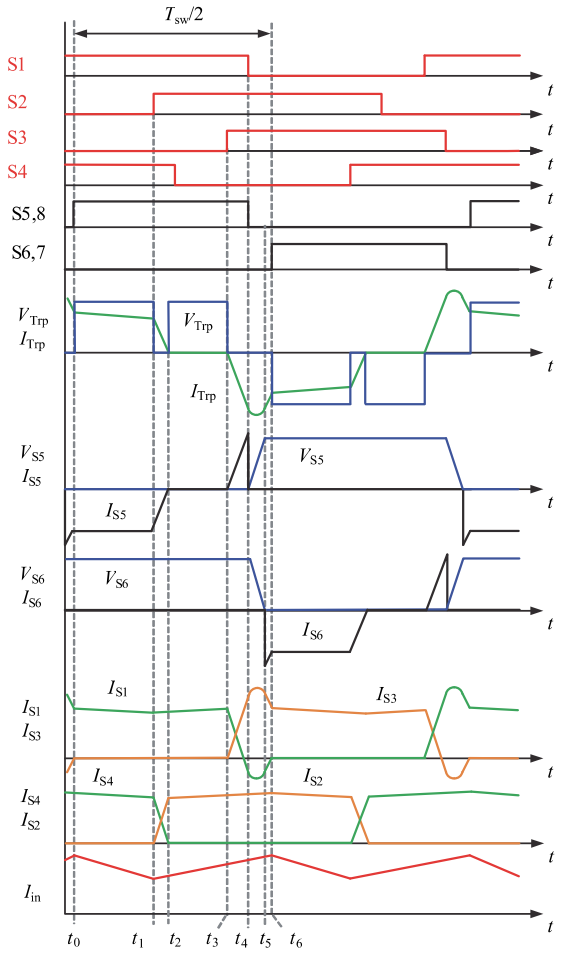

Fig. 3. Idealized operating waveforms of ASMC with an active rectifier.

II. Description of Operation

The converter topologies proposed are shown in Fig. 1. As can be observed, they feature two reverse-conducting and two reverse-blocking devices at the primary side. The asymmetric parallel resonant converter (APRC) topology can be implemented with a passive rectifier (Fig. 1a). It utilizes a resonant tank formed by L_{eq} and C_{eq} to redistribute current between the top transistors. The asymmetric secondary modulation-based converter (ASMC) topology in Fig. 1b has an active rectifier that is used to force the currents to change direction and achieve the same goal. The equivalent capacitor across the transformer primary winding can be formed by the intrinsic capacitances of the rectifier switches (C_{S5}–C_{S8}) and/or separately. Similarly, the equivalent inductance can represent the leakage inductance of the transformer reflected to the primary winding or by an additional inductor in series to the primary winding. Both topologies operate at a constant switching frequency and regulate output voltage by phase-shift between the top and bottom switches. The operation of the converters presented in Figs. 2 and 3 can be described by six switching modes for each half-period $T_{sw}/2$.

A. The APRC Topology

t_0–t_1: switches S1 and S4 are turned on and the other ones are turned off. The converter is in the active state and the power is transferred to the output through switches S1, S4 and diodes S5 and S8. At the end of this interval, the input current reaches the minimum value.

t_1–t_2: S2 is turned off and the active state is finished. The current of S2 rises, while the current of S4 decreases linearly with di/dt, caused by the equivalent leakage inductance. The currents of S5 and S8 as well as the transformer current decrease with the same slope. The input inductor voltage polarity is reversed and its current starts to increase, while the transformer primary voltage is zero.

t_2–t_3: the current of S2 reaches the input current level and the transformer primary voltage rises to the amplitude value. The converter is in the shoot-through state with S1 and S2 conducting while the input inductor is energized. S4 could be turned off with ZCS.

t_3–t_4: S3 is turned on and the resonant process is started. Capacitor C_{eq} starts to recharge and, as a result, the S1 current decreases and the S3 current increases (Fig. 2).

t_4–t_5: when the resonant current becomes higher than the input current, the soft switching condition is satisfied; the body diode of S1 starts to conduct and the transistor channel can be turned off with ZCS. The currents at the primary side reach the amplitude value when the capacitor voltage crosses zero and, as the capacitor C_{eq} voltage polarity changes, starts to decrease back to the value of the input current.

t_5–t_6: the currents at the input side are equal to the input current and the recharging of capacitor C_{eq} continues. When C_{eq} and the transformer voltages reach the amplitude value, rectifier switches S6 and S7 become forward-biased and start to supply the current to the output. From t_6 the converter active state starts and the processes are then repeated for another switching half-period.

B. The ASMC Topology

The first three modes are equivalent to those in APRC.

t_0–t_1: switches S1 and S4 are turned on and the other ones are turned off. The converter is in the active state and the power is transferred to the output through switches S1, S4 and MOSFETs S5 and S8. At the end of this interval, the input current reaches the minimum value.

t_1–t_2: S2 is turned off and the active state is finished. The current of S2 rises, while the current of S4 decreases linearly with di/dt, caused by the equivalent leakage inductance. The currents of S5 and S8 as well as the transformer current decrease with the same slope. The input inductor voltage polarity is reversed and its current starts to increase, while the transformer primary voltage is zero.

t_2–t_3: the current of S2 reaches the input current level and the transformer primary voltage rises to the amplitude value. The converter is in the shoot-through state with S1 and S2 conducting while the input inductor is energized. S4 could be turned off with ZCS.

t_3–t_4: S3 is turned on and the current of S3 rises, while the current of S1 decreases linearly with di/dt, caused by equivalent leakage inductance. This mode is analogous to the interval t_1–t_2 (Fig. 3).

t_4–t_5: since S1 is a reverse-conducting device, after decreasing to zero, the current starts to flow through its body diode, changing with the same slope, while the current through S3 rises above the input current. Thus, the soft switching condition is satisfied and S1 can be turned off with ZCS, along with S5 and S8. The equivalent capacitor recharges and the transformer voltage changes its polarity.

t_5–t_6: capacitor C_{eq} is recharged, the transformer secondary voltage reaches the amplitude value and the body diodes of S6 and S7 become forward-biased. The current through S1 returns back to zero with the same di/dt, and the current of S3 and the transformer primary current become equal to the input current. From t_6, the converter active state is started, hence S6 and S7 can be turned on to avoid excessive losses in the body diodes. The processes are then repeated for another switching half-period.

C. Design Aspects

1. The APRC converter

For APRC, soft switching is achieved if peak transformer primary current $I_{P(res)}$ is larger than input inductor current I_{in}.

$$I_{P(res)} = \frac{V_{out}}{nZ_r} \geq I_{in}, \tag{1}$$

where V_{out} is the output voltage, n is the transformer turns ratio and Z_r is the impedance of the resonant circuit:

$$Z_r = \sqrt{\frac{L_{eq}}{C_{eq}}}, \tag{2}$$

where L_{eq} is the inductance of the equivalent circuit (largely determined by transformer leakage inductance) and C_{eq} is the equivalent capacitance, which can be represented by the intrinsic capacitance of the rectifier semiconductor and/or an external capacitor.

To satisfy the soft switching criteria for a wide range of conditions, the resonant circuit should be designed around minimal input voltage at full load. The required impedance of the resonant tank Z_r, should be chosen according to

$$Z_r = \sqrt{\frac{L_{eq}}{C_{eq}}} \le \frac{V_{out}}{nI_{P(res)}} = \frac{V_{in(min)}V_{out}}{nP_{max}}, \quad (3)$$

where P_{max} is the maximum power of the converter. The required resonant frequency is estimated by

$$f_r = \frac{f_{sw}}{1-\frac{n}{G_{min}}}, \quad (4)$$

where f_{sw} is the converter switching frequency and G_{min} is the desired minimum converter voltage gain. The resonant frequency is calculated from

$$f_r = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}}. \quad (5)$$

From (3)–(5), the equation for the required equivalent inductance L_{eq} is obtained from

$$L_{eq} = \frac{Z_r}{2\pi f_r}. \quad (6)$$

The associated resonant capacitance can then be derived from (3).

The duty cycle of the switches should be higher than 0.5 to avoid open circuit of the input inductor and for S2 and S4, it can be approximated as

$$D_{S2,S4}^{min} \ge \frac{1}{2} + \frac{nL_{eq}P_{max}}{V_{in}V_{out}}. \quad (7)$$

For the other pair of switches (S1 and S3), the required duty cycle is estimated from

$$D_{S1,S3} = \frac{1}{2} + \frac{f_{sw}}{4f_r}. \quad (8)$$

The gain of this converter is not sensitive to load variations and is estimated from

$$G = \frac{n}{1-f_{sw}\left(\frac{1}{f_r}+2t_{2-3}\right)}. \quad (9)$$

2. The ASMB Converter

For the ASMB converter, the duty cycle of the switches can be calculated from (8) for the minimum possible input voltage and the maximum power level. It should be noticed that a longer duty cycle would lead to an increased peak current at the primary side and excessive energy circulation. In the ideal case, the peak current of the converter should be equal to maximum possible input current $I_{in(max)}$, and the switch duty cycle is obtained by

$$D = \frac{1}{2} + \frac{nI_{in(max)}L_{eq}f_{sw}}{V_{out}}, \quad (10)$$

where $I_{in(max)} = P_{max}/V_{in(min)}$.

The minimum total duration of the shoot-through state (t_1–t_6) is then estimated from

$$t_{1-6(min)} = \frac{2\left[L_{eq}\left(nI_{in(max)}\right)^2 + C_{eq}V_{out}^2\right]}{nI_{in(max)}V_{out}}. \quad (11)$$

As shown, both L_{eq} and C_{eq} increase the resulting minimum duration of the shoot-through state. Therefore, they should be carefully selected to have the desired regulation capabilities of the converter. The converter gain can be then estimated from

$$G = \frac{1}{1-2f_{sw}\left(t_{2-3}+t_{1-6(min)}\right)}. \quad (12)$$

3. Generalizations

Unlike in other topologies with phase shift control, the peak current of the top transistors is higher than the input current, which offers a specific advantage. From the operational waveforms and equations presented it follows that the recharging of capacitor C_{eq} takes place when the current is at its peak value, which is higher than the maximum input current. Thus, the capacitor recharge time is constant and unaffected by the converter operating point and operation at light load does not affect converter gain or require adjustments to the control strategy. Since only top transistors exhibit such an increased current, the total energy circulation through semiconductors at low-load conditions can be lower than that of the topologies with symmetric control. While the APRC topology requires lesser number of active switches, the ASMB provides a larger degree of freedom when choosing the value of C_{eq}. Moreover, if the input current value is known, the implementation of digital control to adjust the duty cycles of the switches would allow a significant reduction of the circulating energy.

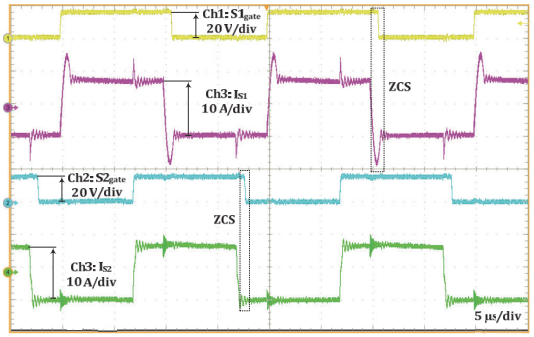

Fig. 4. Experimental waveforms of an APRC converter: Ch1 – S1 gate voltage, Ch2 – S2 gate voltage, Ch3 – S1 current and Ch4 – S2 current.

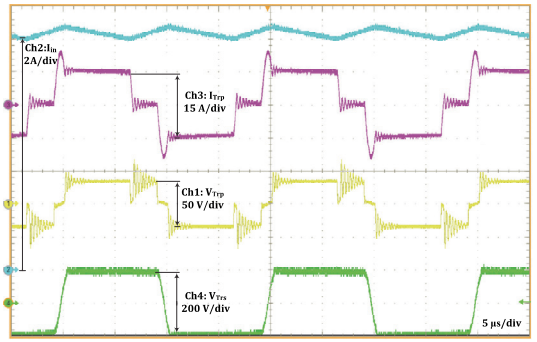

Fig. 5. Experimental waveforms of an APRC converter: Ch1 – V_{Trp}, Ch2 – I_{in}, Ch3 – I_{Trp} and Ch4 – V_{Trs}.

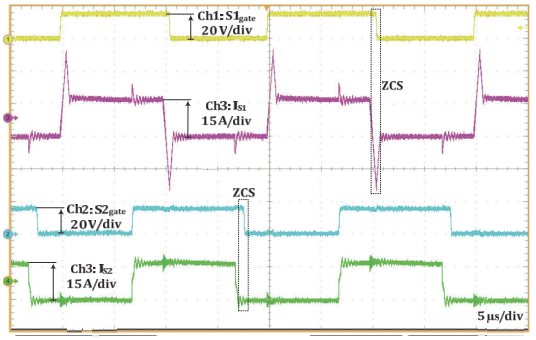

Fig. 6. Experimental waveforms of an ASMC converter: Ch1 – S1 gate voltage, Ch2 – S2 gate voltage, Ch3 – S1 current and Ch4 – S2 current.

III. Experimental Verification

To validate the proposed converters, an experimental prototype with a rated power of 400 W was assembled and both topologies were tested with the same hardware. Synchronous MOSFETs instead of series diodes were applied in the primary part to reduce conduction losses. The parameters and components used are listed in Table I.

TABLE I

Parameters and Components of the Experimental Prototype

Parameter/component	Symbol	Value
Input voltage, DC	V_{in}	20–30 V
Output voltage, DC	V_{out}	400 V
Switching frequency	f_{sw}	50 kHz
Primary side inductors inductance	L_1	100 µH
Equivalent capacitance (at TX primary winding)	C_{eq}	10 nF
Transformer turns ratio	N_2/N_1	13 : 1
Equivalent TX leakage inductance	L_{eq}	0.8 µH
Rated power	P_{rated}	400 W
Primary-side transistors	S1–S4	FDMS86181
Secondary-side transistors	S5–S8	STP18N60DM2
Microcontroller	–	STM32F334R8T6
Primary-side transistor drivers	–	ADUM3221
Secondary-side transistor drivers	–	ACPL-P346

The experimental waveforms for the APRC topology at $V_{in} = 24$ V are presented in Figs. 4 and 5. As shown in Fig. 4, top switch S1 is turned off when the resonant current is flowing through its body diode, resulting in ZCS. Bottom switch S2 is turned off when its current is taken over by S4, which also results in ZCS. All the primary switches turn on with reduced di/dt and, as a result, the turn-on losses diminish. The input current waveform in Fig. 5 shows that the converter continues to be in the shoot-through state during the resonant period, while the transformer secondary winding changes polarity.

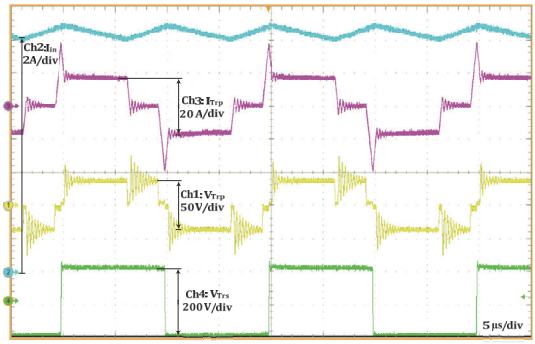

Fig. 7. Experimental waveforms of an ASMC converter: Ch1 – V_{Trp}, Ch2 – I_{in}, Ch3 – I_{Trp} and Ch4 – V_{Trs}.

The measurement results of ASMC at $V_{in} = 24$ V are shown in Figs. 6 and 7. During the experiments, the converter was operating with a very small value of C_{eq} and, as a result, the t_4–t_5 interval is minor. Similar to the APRC topology, the top transistors turn off when their body diode conducts, while the bottom ones – after the current drops to zero, resulting in ZCS for all the primary semiconductors. From Fig. 7 it can be observed that the transformer secondary voltage changes polarity when its current is at the peak value and, since C_{eq} could be small for this converter, the process takes significantly less time. During the laboratory experiments, the power stage of ARPC reached an efficiency of 96.4 % and that of ASMC – 96.6 % at an input voltage of 30 V.

The experimental results are in agreement with theoretical estimations for both topologies and therefore it can be concluded that the claims presented in the previous sections have been confirmed.

IV. Conclusion

This paper introduced two isolated soft-switching asymmetric current-fed DC-DC converters with a passive rectifier and an active one. The proposed topologies can be applied in systems where a high gain and/or galvanic isolation are required, such as fuel cells, batteries, DC microgrids and other applications. The converters have two reverse-blocking devices and two reverse-conducting ones at the primary side and utilize phase-shift control with a constant switching frequency. Their main aim is to reduce the problem of high circulating energy encountered in existing symmetric topologies and the high conduction losses present in topologies with phase-shift control.

The experimental results showed a peak power stage efficiency of 96.4 % and 96.6 % for the ARPC and ASMC topologies, respectively. That proves that the topologies proposed allow achieving a comparable level of efficiency – while having a lower switch count than other existing topologies with a phase-shift control algorithm and lower current stress than the topologies with a symmetrical modulation control algorithm.

Future research will focus on the detailed analysis of the presented topologies and their comparison with other existing solutions, designed with the same constraints and requirements.

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Bidirectional Soft Switching Current Source DC-DC Converter for Residential DC Microgrids

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***Abstract*—This paper presents a novel asymmetric bidirectional isolated DC-DC converter topology with current source and voltage source terminals. The topology can be implemented in renewable, supercapacitor, battery and dc microgrid applications. It features two bidirectional and two reverse-conducting switches in the current-source bridge side. Thanks to special control algorithm it provides soft switching of all semiconductors under wide range of operating conditions with low energy circulation. This is achieved without any dedicated snubbers or clamp circuits. The converter theoretical performance at various operating conditions is assessed and compared with other competitive solutions in terms of rms current stress on the transformer and semiconductors. Steady-state operation and design aspects of the converter are presented and verified experimentally with 500 W prototype.**

Keywords— dc-dc power converters; bidirectional power flow; soft switching; zero current switching; zero voltage switching; batteries.

I. INTRODUCTION

Isolated current source DC-DC converters (CSCs) are an attractive alternative to voltage source ones in dc microgrid applications for interfacing relatively low voltage sources, such as fuel cells, photovoltaics or batteries [1]-[3]. Among different current source topologies, full bridge converters with single input inductor (boost full bridge, BFB) are receiving high attention due to their scalability and modularity, making them suitable for wide range of applications: from relatively low voltage [4],[5] to high voltage/high power ones [6],[7].

The isolated CSCs usually feature auxiliary circuits, such as snubbers or clamps, to prevent voltage spikes across current source side (CS) semiconductor devices, caused by leakage inductance of practical transformers [8]. At the same time, some of the existing topologies can be attributed to snubberless [9]-[12]. These converters provide clamping and soft switching of semiconductor devices without a separate dedicated circuit, by special control algorithms, by utilising parasitic parameters of the circuit. This can be achieved by forcing the current redistribution between the CS transistors and typically is attained in two different ways: by utilising resonant circuit [9],[10] or by using active rectifier at the voltage source (VS) side [11],[12].

The first approach takes advantage of equivalent parasitic inductance of the circuit (mainly determined by transformer leakage inductance), that is used to form a resonant circuit together with a relatively small, typically external, capacitor. As a result, the topology changes to either series or parallel resonant current source converter (PRC). The latter topology is preferred due to wider regulation possibilities [14]. PRCs can feature either variable frequency pulse width- or phase-shift-modulation. The advantages of phase shift modulation include reduced energy circulation and constant switching frequency; however, the CS switches need to possess reverse blocking (RB) capability, which, in practice, requires series connection of devices and leads to increased conduction losses [15]. Another disadvantage lies in limited capability to regulate output voltage at light loads [10].

The second approach involves implementation of active rectifier to form a secondary-modulated converter (SMC) that forces the current redistribution between top transistors at the CS side to achieve clamping and soft switching. This approach was adopted to both symmetric (S-SMC) [11] and phase shift control (PS-SMC) [12]. As in the case of PRC, the phase shift control features reduced energy circulation, but requires the CS switches to feature RB capability. The advantage of SMCs lies in constant frequency modulation for both symmetric and phase-shift versions and higher degree of freedom when choosing VS-side lossless snubber capacitors. In addition, S-SMC features inherent bidirectional operation capability and PS-SMC can achieve that using four quadrant switches at the CS side. At the same time, the S-SMC has increased energy circulation, particularly at partial load and requires RC snubbers to reduce voltage stress on the CS transistors [13], while PS-SMC requires increased number of semiconductors and thus has increased conduction losses.

Current paper will present asymmetric secondary-modulated converter (A-SMC) topology that aims to combine properties of both S-SMC and PS-SMC and could provide improved weighted performance, particularly if the converter has to operate under wide range of input voltage and power levels.

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Table I
PARAMETERS AND REQUIREMENTS OF THE ANALYSED SYSTEM

Parameter	Symbol	Value
Minimum CS-side voltage	$V_{CS(min)}$	20 VDC
Maximum CS-side voltage	$V_{CS(max)}$	40 VDC
VS-side voltage	V_{VS}	480 VDC
Switching frequency	f_{sw}	50 kHz
Transformer turns ratio	n	1:5.5
Minimum CS gain (V_{CF}=40 V)	G	1.10·n
Rated power	P_{rated}	500 W
Operating power	P	50…500 W

II. CHARACTERISATION OF EXISTING TOPOLOGIES

Current section is devoted to assessment of the performance of the proposed A-SMC and its comparison with existing solutions. All of the competing converters feature bidirectional operation capability, with low and high voltage ports at the current- and voltage-source sides, respectively. The topologies are characterised by software models in terms of normalised rms current of the isolation transformer I_{TXN} and normalised cumulative rms current of the semiconductors I_{SN}: In the analysis the components are considered lossless and the influence of the CS current ripple negligible.

$$I_{TXN} = \frac{I_{TX(rms)}}{I_{CS}}, \tag{1}$$

$$I_{SN} = \frac{\sum_{\text{Switch}}^{\text{Primary}} I_{S(rms)}}{I_{CS}}, \tag{2}$$

where I_{CS} is the rms CS side current.

This approach allows to evaluate the requirements to key power components and potential performance at various operating conditions. For better representation of results, the topologies should meet the same case study operating parameters (Table I).

A. Symmetric secondary-modulated converter (S-SMC)

The full bridge S-SMC with reverse conducting transistors and symmetric control was presented in [11] (Fig. 1). The CS switches are operated with duty cycles (D) higher than 0.5, while the VS switches are turned on during the shoot-through state. This allows their current to change direction and forces the current redistribution across the CS-side transistors with di/dt limited by equivalent circuit inductance L_{eq}.

In the general form, the converter gain (G) can be expressed by the following

$$G = \frac{V_{VS}}{V_{CS}} = \frac{n}{1-D}, \tag{3}$$

where n is the transformer turns ratio, V_{CS} and V_{VS} are converter current source side and voltage source side voltages, respectively.

The soft switching criteria for CS switches is satisfied when peak current (I_{peak}) at the CS side becomes higher than I_{CS}. The I_{peak} is estimated by

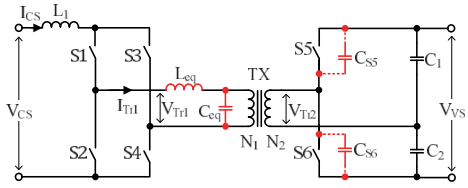


Fig. 1. S-SMC topology with reverse conducting switches at the CS side and active voltage doubler rectifier at the VS side [11].

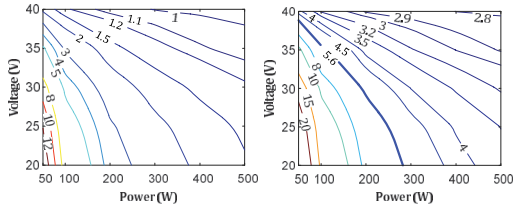


Fig. 2. Normalised transformer N_1 winding rms current I_{TXN} (a) and total CS switch I_{SN} (b) rms currents of S-SMC, operating in the boost mode (L_{eq}=1.45 µH, C_{eq}=0 nF).

$$I_{S(peak)} = \frac{I_{CS}}{4} + \frac{V_{VF} - 2 \cdot V_{CS} \cdot n}{16 \cdot L_{eq} \cdot f_{sw} \cdot n}, \tag{4}$$

where f_{sw} is the converter switching frequency.

The VS switches turn on with ZVS and their turn-off losses can be limited by equivalent capacitance C_{eq}, generally formed by snubber capacitors C_{s5} - C_{s6}. This imposes certain converter design constraints, as both L_{eq} and C_{eq} limit the minimum gain, particularly at full CS voltage and load conditions. In the current study it is assumed that the C_{eq} is negligible and the converter is capable of providing 10% CS-side voltage gain at maximum CS voltage and rated load conditions (Table I). The L_{eq} is calculated as

$$L_{eq} \le \frac{V_{in(max)} \cdot V_{out} \cdot \left(1 - \frac{1}{G}\right)}{8 \cdot n \cdot f_{sw} \cdot P_{rated}} \tag{5}$$

The characterisation of the converter in the boost mode (Fig. 2) shows that the converter features low circulating energy at maximum load and CS voltage, but the dependency on power and CS voltage decrease is high. As a result, the converter has very high energy circulation at minimum power and CS voltage.

B. Phase-shifted secondary-modulated converter (PS-SMC)

The converter topology shown in Fig. 3 was presented in [12]. Unlike the S-SMC, the topology utilises phase shift control and reverse blocking devices at the CS side.

The CS transistors always operate with duty cycles slightly higher than 0.5:

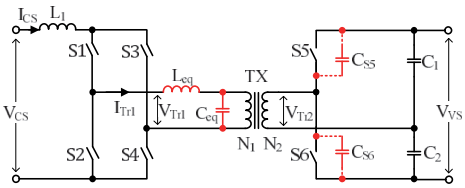


Fig. 3. PS-SMC topology with bidirectional switches at the CS side and active rectifier at the VS side [12].

$$D_{CS} = \frac{1}{2} + \frac{2 \cdot n \cdot I_{CS} \cdot L_{eq} \cdot f_{sw}}{V_{VS}}, \tag{6}$$

The peak current of the switches never exceeds the I_{CS} current and its rms value can be estimated by

$$I_{S(rms)} = I_{CS} \cdot \sqrt{D_{CS}} \approx 0.7 \cdot I_{CS}, \tag{7}$$

Thanks to active switches in the rectifier, the PS-SMC is forcing the current transition between the transistors S1 and S3 and achieves ZCS. The current transition between S2 and S4 is achieved naturally. Similar to S-SMC, the C_{eq} in this topology serves the purpose of reducing *dv/dt* across the turning-off rectifier transistor. The minimum gain of the converter is determined by four transient intervals: two linear current transitions between transistors S1-S3 and S2-S4, interval of energy return and capacitor recharge time. Taking into account both L_{eq} and C_{eq}, the minimum duration of the shoot-through state is calculated by

$$t_{st(min)}^{LC} = \frac{n \cdot \left(4 \cdot L_{eq} \cdot {I_{CS}}^2 + C_{eq} \cdot {V_{VS}}^2\right)}{I_{CS} \cdot V_{VS}} \tag{8}$$

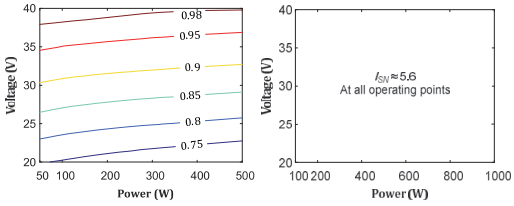
As it could be observed, the duration depends on the load current and at low load conditions the regulation capability of the converter could be diminished due to increased recharge time of the C_{eq}. This problem can be mitigated by applying semiconductors with low output capacitance, such as GaN-based transistors [16],[17]. The interval of energy return is derived as

$$t_{rev} = \frac{2 \cdot L_{eq} \cdot n \cdot \left(2 \cdot I_{CS(max)} - I_{CS}\right)}{V_{VS}} \tag{9}$$

The resulting minimal converter gain is estimated by

$$G = \frac{2}{1 - 2 \cdot f_{sw} \cdot \left(t_{st(min)}^{LC} + 2 \cdot t_{rev}\right)}, \tag{10}$$

The normalised transformer current of the PS-SMC is depicted in Fig. 4a. The transformer winding N_1 current does not have any circulating energy and is well utilised at all operating points. While the individual CS switch rms current is relatively low (Fig. 4b), the cumulative rms current is increased due to high number of devices in the CS part:



(a) (b)

Fig. 4. Normalised transformer I_{TXN} (a) and total primary switch I_{SN} (b) rms currents of A-SMC, operating with case study power and voltage range (L_{eq}=430 nH, C_{eq}=0 nF).

$$I_{SN} = \frac{\sum_{1}^{8} I_{S(rms)}}{I_{CS}} \approx 5.6, \tag{11}$$

The analysis shows that both existing SMCs have certain drawbacks and there is no clearly superior solution. The S-SMC can demonstrate high peak efficiency; however, the performance deteriorates at non-optimal operating point due to high circulation energy in the topology. At the same time, the PS-SMC features reduced current stresses and minor energy circulation. On the other hand, since it requires bidirectional switches at the CS side (typically realised by two discrete devices), the total conduction losses in semiconductors are increased and the resulting silicon utilisation is relatively low.

III. Proposed Asymmetric Converter

The asymmetric secondary modulated converter (A-SMC) proposed in this paper aims to combine the properties of existing solutions and provide improved weighted performance, particularly if the converter has to operate under a wide range of CS voltage and power levels. The operation with voltage doubler rectifier is assumed; however, the full-bridge rectifier can be applied as well. The converter topology is presented in Fig. 5, featuring two reverse-conducting and two bidirectional blocking devices at the CF side. The active rectifier is used to force the currents to change direction and achieve the soft switching of semiconductors. The equivalent capacitor across the transformer N_1 winding can be formed by intrinsic capacitances of the rectifier switches (C_{S5}-C_{S6}) and/or separately. Similarly, the equivalent inductance can represent leakage inductance of the transformer reflected to N_1 or by additional inductor in series to the N_1 winding.

A. Description of operation in the boost mode

The topology operates at the constant switching frequency and regulate output voltage by phase-shift between the top and bottom switches. The modulation principle of the converter is presented in Fig. 6a and can be described by six switching modes for each half-period $T_{sw}/2$. The transistors S2.2 and S4.2 can be turned-off or operate in the synchronous rectification mode to reduce conduction losses. In the analysis all the are considered lossless and the transformer magnetising inductance infinitely large.

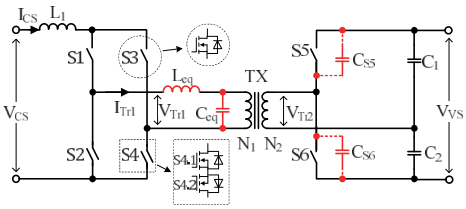


Fig. 5. Proposed bidirectional asymmetric secondary modulated converter topology with two conventional and two bidirectional switches in the CF side.

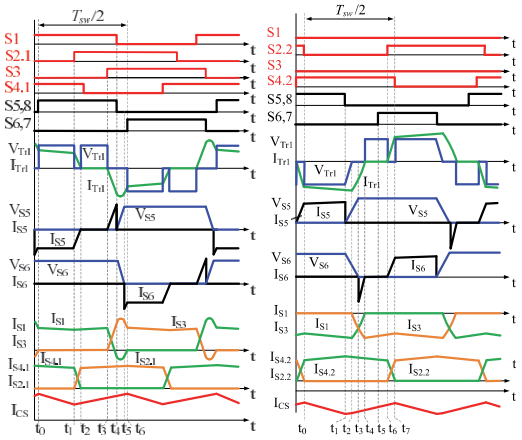


Fig. 6. Operating waveforms of bidirectional A-SMC: boost mode (a), buck mode (b).

t₀-t₁: Switches S1 and S4.1 are turned on and the other ones are turned off. The converter is in the active state and the power is transferred to the output through switches S1, S4 and the body diodes of transistors S5 and S8, which can be turned on with ZVS to reduce on-state losses. At the end of this interval, the I_{CS} reaches a minimum value.

t₁-t₂: S2 is turned off and the active state is finished. The current of S2 rises, while the current of S4 decreases linearly with *di/dt* limited by L_{eq}. The currents of S5 and S8 as well as transformer current decrease with the same slope. The CS inductor voltage polarity is reversed and its current starts to increase, while the V_{Tr1} is zero.

t₂-t₃: The current of S2 reaches input current level and the V_{Tr1} rises to the amplitude value. The converter is in the shoot-through state with S1 and S2 conducting while the L_1 inductor is energised. S4 could be turned off with ZCS.

t₃-t₄: S3 is turned on and the current of S3 rises, while the current of S1 decreases linearly with *di/dt*, limited by L_{eq}. This mode is analogous to the interval t_1-t_2 (Fig. 6b).

t₄-t₅: Since S1 is a reverse conducting device, after decreasing to zero, the current starts to flow through its body diode, changing with the same slope, while the current through S3 rises above the input current. Thus, the soft switching condition is satisfied and S1 can be turned off with ZCS, along with S5 and S8. The equivalent capacitor recharges and the V_{Tr2} changes its polarity.

t₅-t₆: C_{eq} is recharged, the V_{Tr2} reaches the amplitude value and the body diodes of S6 and S7 become forward biased. The S1 current returns back to zero with the same *di/dt*, and the current of S3 and the I_{Tr1} becomes equal to the input current. From t_6, the starts the converter active state, hence S6 and S7 can be turned on to avoid conduction losses in the body diodes. The processes are then repeated for another switching half-period.

B. Description of operation in the buck mode

In the buck mode the topology represents voltage source converter with inductive output filter. The converter modulation principle is similar to the one of phase-shifted active rectifier presented in [18] and thus not analysed in detail in the current paper. The minor difference lies in the configuration of the reverse blocking switches S2 and S4. In the proposed topology they are located in different bridge legs and, unlike in [18], the duty cycle of the transistors should always be above 0.5 in order to avoid open-circuit condition of the inductor L_1. The generalised switching waveforms for the buck mode are presented in Fig. 6b. The transistors S1, S3, S2.1 and S4.1 can be kept turned-off or operate in the synchronous rectification mode to reduce conduction losses.

C. Design aspects

The soft switching of A-SMC is achieved if the peak current in the CS side I_{peak} is larger than the CS inductor current I_{CS}. The duty cycle of the switches is calculated assuming minimum CS voltage and maximum power level (maximum possible I_{CS}). It should be noticed, that longer duty cycle would lead to increased peak current in the CS side and excessive energy circulation. In the ideal case, the peak current of the converter should be equal to maximum possible CS current $I_{CS(max)}$, and the switch duty cycle is derived by

$$D = \frac{1}{2} + \frac{2 \cdot n \cdot I_{CS(max)} \cdot L_{eq} \cdot f_{sw}}{V_{out}}, \qquad (12)$$

where $I_{CS(max)} = P_{rated} / V_{CS(min)}$.

Neglecting the influence of C_{eq}, the minimum total duration of the shoot-through state (t_1-t_6) is estimated from

$$t^{L}_{1\text{-}6(min)} = \frac{4 \cdot n \cdot L_{eq} \cdot I_{CS(max)}}{V_{VS}}. \qquad (13)$$

In the case C_{eq} is significant, the duration $t_{4\text{-}5}$, cannot be ignored. This duration can be estimated by

$$t_{4\text{-}5} = \frac{\frac{\pi}{2} - arctg\left(\frac{n \cdot I_{peak} \cdot Z_r}{V_{VS}}\right)}{\pi \cdot f_r}. \qquad (14)$$

where $Z_r = \sqrt{L_{eq} / C_{eq}}$ and $f_r = 1/\left(2 \cdot \pi \cdot \sqrt{L_{eq} \cdot C_{eq}}\right)$.

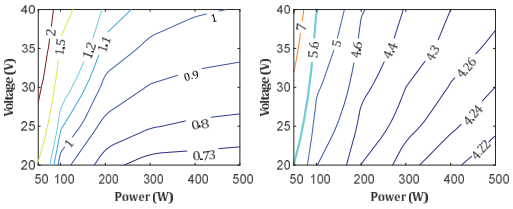


Fig. 7. Normalised transformer I_{TXN} (a) and total primary switch I_{SN} (b) rms currents of A-SMC, operating with case study power and voltage range.

Resulting shoot-through state duration can be then estimated by

$$t_{1\text{-}6}^{LC} = t_{1\text{-}6(min)}^{L} + t_{2-3} + t_{4-5}\,. \tag{15}$$

As shown, both L_{eq} and C_{eq} increase the resulting minimum duration of the shoot-through state. Therefore, they should be carefully selected to have the desired regulation capabilities of the converter. The converter gain can be then estimated from

$$G = \frac{2}{1 - 2 \cdot f_{sw} \cdot \left(t_{2\text{-}3} + t_{1\text{-}6}^{LC}\right)}. \tag{16}$$

Different from PS-SMC, the peak current of the top transistors in A-SMC is higher than the I_{CS}, which offers a specific advantage. From the operational waveforms and equations presented it follows that the capacitor C_{eq} recharge takes place when the current is at its peak value, which is equal or higher than the maximum rated CS current. As a result, the capacitor recharge time is constant and unaffected by the converter operating point and operation at light load does not affect converter gain or require adjustments to the control strategy. Thus, the A-SMC provides a larger degree of freedom when choosing the C_{eq} value when compared to PS-SMC. Since only top transistors exhibit such increased current, the total energy circulation through semiconductors and transformer at low load conditions is lower than that of the S-SMC, as shown in Fig. 7. From these graphs it could also be observed that the highest energy circulation occurs at high CS voltage and low load condition.

IV. Experimental Verification

To validate the proposed converter, a scaled experimental prototype with rated power of 500 W was assembled and tested. The components and parameters of the prototype are presented in Table II. Synchronous rectification was applied to reduce conduction losses.

The experimental waveforms for the boost mode at V_{CS}=24 V are presented in Figs. 8-10. During the experiments, the converter was operating with a very small value of C_{eq} and, as a result, the interval t_4-t_5 is minor and the slopes of the circulating current are linear.

As shown in Fig. 8, the top transistors turn off when their body diode conducts, while the bottom ones – after the current drops to zero (Fig. 9), resulting in ZCS for all the CS semiconductors. All the CS switches turn on with reduced *di/dt* and, as a result, their turn-on losses are decreased.

TABLE II

Parameters and Components of the Experimental Prototype

Parameter / Component	Symbol	Value
CS voltage	V_{CS}	20-40 VDC
VS voltage	V_{VS}	480 VDC
Switching frequency	f_{sw}	50 kHz
CS side inductor	L_1	100 µH
Equivalent capacitance (at N_1)	C_{eq}	5 nF
Transformer turns ratio	N_2/N_1	5.5:1
Equivalent TX leakage inductance	L_{eq}	430 nH
Rated power	P_{rated}	500 W
Primary side transistors	S_1-S_4	BSC035N10NS5
Secondary side transistors	S_5-S_6	STP18N60DM2
Microcontroller	-	STM32F334R8T6

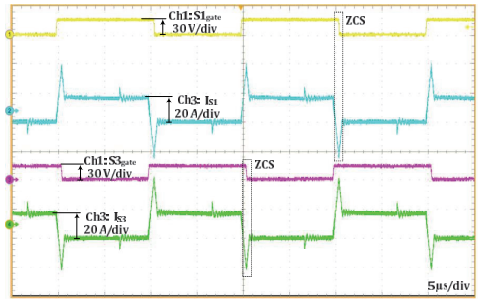


Fig. 8. Experimental waveforms of ASMC converter: Ch1 – S1 gate voltage, Ch2 – S1 current, Ch3 – S3 gate voltage and Ch4 – S3 current.

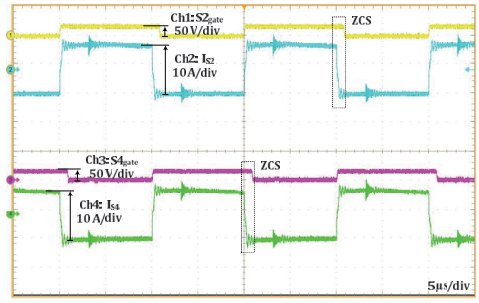


Fig. 9. Experimental waveforms of ASMC converter: Ch1 – S2 gate voltage, Ch2 – S2 current, Ch3 – S4 gate voltage and Ch4 – S4 current.

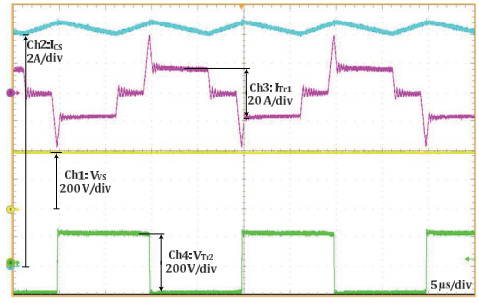


Fig. 10. Experimental waveforms of ASMC converter: Ch1 – V_{VS}, Ch2 –I_{CS}, Ch3 – I_{Tr1} and Ch4 – V_{Tr2}.

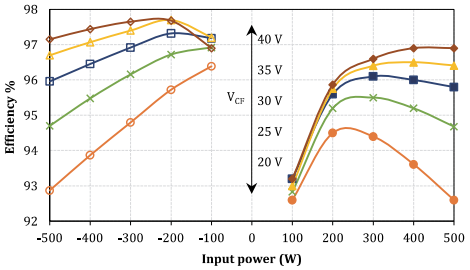


Fig. 11. Experimental efficiency of the converter power stage at different CS-side voltage levels in buck mode (negative) and boost mode (positive).

The CS current waveform in Fig. 10 shows that the converter continues to be in the shoot-through state when I_{Tr1} is above its steady-state value. The V_{Tr2} changes polarity when transformer current is at its peak value and the process takes relatively short time.

The converter power stage efficiency depicted in Fig. 11 was measured at various CS voltage levels in both buck and boost operation modes. At rated power the prototype reached maximum efficiency of 96.9% and 97.1% in the boost and buck mode, respectively. The experimental results are in agreement with the estimations and, therefore, it can be concluded that the analysis presented in previous sections is verified and confirmed.

V. Conclusions

This paper introduced bidirectional isolated soft switching asymmetric current-fed dc-dc converter with an active rectifier. Proposed topology can be applied in systems where high gain and/or galvanic isolation is required, such as fuel cell, battery, dc microgrid and other applications. The converter has two bidirectional and two reverse conducting devices at the CS side and utilise phase-shift control with constant switching frequency. The topology is aimed to reduce the problem of high circulating energy in existing symmetric topologies and high conduction losses of topologies with phase-shift control. It was shown, that for the proposed solution, both values are moderate, which would result in better weighted performance over a range of possible operating points. Steady-state operation and design aspects of the topology proposed are presented and verified experimentally.

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Snubberless Boost Full-Bridge Converters: Analysis of Soft Switching Performance and Limitations

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Keywords:	DC-DC power conversion, Power electronics, Pulse width modulated power converters, Switched mode power supplies, Current

Snubberless Boost Full-Bridge Converters: Analysis of Soft Switching Performance and Limitations

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***Abstract*—This paper analyses current-fed (current source) isolated dc-dc converters that are proposed for various renewable energy and dc microgrid applications, such as photovoltaic, fuel cell or energy storage systems. The studied current-fed (boost) full-bridge converters achieve clamping and soft switching without dedicated external auxiliary circuits, such as snubbers or clamps. Selected snubberless topologies designed with common criteria are analysed at different operating conditions. The relation between the rms input current and the isolation transformer primary current as well as the cumulative rms current of primary semiconductors is proposed for converter characterization. This approach shows advantages, drawbacks and limitations of the solutions analysed and can be extended or applied to other topology types. The results of this study can be used as a universal tool for performance assessment of snubberless converters without auxiliary circuits for particular operating conditions in various systems.**

***Index Terms*— power electronics, pulse width modulated power converters, DC-DC power conversion, switched mode power supplies, current.**

Nomenclature

I_{in}	input current (A)
$I_{in(max)}$	maximum input current (A)
$I_{S(peak)}$	peak switch current (A)
$I_{S(rms)}$	primary switch rms current (A)
I_{SN}	cumulative primary switch rms current (A)
$I_{TX(rms)}$	transformer primary rms current (A)
I_{TXN}	normalized transformer primary current (A)
V_{in}	input voltage (V)
$V_{in(min)}$	minimum input voltage (V)
$V_{in(max)}$	maximum input voltage (V)
V_{out}	output voltage (V)
P_{rated}	rated power (maximum) (W)
L_{eq}	equivalent inductance (H)
C_{eq}	equivalent capacitance (F)
Z_r	impedance of the resonant circuit (Ω)
f_{sw}	switching frequency (Hz)
f_r	resonant frequency (Hz)
G	converter primary side (normalized) voltage gain
n	transformer turns ratio
D	primary switch duty cycle
t_{st}	duration of shoot-through state (s)

I. Introduction

Isolated current-source dc-dc converters (CSCs) are attracting increased attention due to their advantages over the voltage-source counterparts in renewable, storage and dc microgrid applications where the dc input associated with lower voltage and high current is interfaced with a dc output of considerably higher voltage [1][2][3][4]. In this case, the continuous input current facilitates optimal operation of batteries, fuel-cells, and other energy sources sensitive to the input current ripple [6][7][8][9]. However, due to imperfect magnetic coupling of windings, practical transformers have some of the flux not linking the other

windings. This leakage flux can be represented as additional equivalent (leakage) inductance in series with a transformer winding. As a result, the CSCs typically require clamping at the input side to avoid voltage overshoot across the semiconductor switches due to mismatch between input inductor and transformer currents when the boosting interval is finished. Different methods exist for solving this problem; however, most of those include additional passive or active circuits [10][11][12] or auxiliary dc-dc converters [13][14][15][16][17]. Many of those methods additionally provide extra features, like soft switching of semiconductors and soft starting capability. Soft-switching CSC topologies have been proven to outperform their voltage-source counterparts due to a wider soft-switching range over the power and the input voltage variations, lower rms current of semiconductors, low input current ripple, lower turns ratio of the transformer, resulting in smaller parasitic elements, higher part-load efficiency, simpler requirements to the isolation transformer design, etc [18][19][20][21].

At the same time, a number of CSC topologies exist that feature clamping and soft-switching without auxiliary circuits. In general, these can be attributed to resonant [22][23][24][26][25][27] and secondary-modulated ones (also referred to as snubberless) [28][29][30][31]. Although this assumption is not strictly defined and various interpretations are possible, in the present study, the authors assume that clamping in such systems is achieved without a separate dedicated passive or active circuit. Instead, it is achieved with special control principles, by utilizing equivalent inductance and capacitance present in the circuit. Those can be determined by parasitic parameters of the practical components (transformer leakage inductance and intrinsic capacitances of the transistors) or by using relatively small additional passive components. Such approach generally brings another advantage – soft switching operation of semiconductor devices. At the same time, clamping and soft switching impose certain conditions and design criteria to be met in order to ensure successful operation within the desired range of conditions. The equivalent inductance and capacitance values should be dimensioned to maintain required operating mode, along with additional limitations on switching timings of semiconductors, particularly for systems with a wide range of voltage and load variations. Some of the control principles proposed are quite flexible and can be adopted to different topologies. However, in the current analysis, only full-bridge topologies with single input inductor (boost full-bridge) are considered for evaluation due to their scalability and modularity, making them suitable for a wide range of applications: from relatively low voltage [32][33] to high voltage/high power ones [34][35] [36].

General properties of the selected topologies are summarized in Table I. In this study, parallel resonant converters (PRCs) are considered due to their wider soft switching operation range than that of CS series resonant converters [23]. The topologies could be classified based on the proposed control method: symmetrical (S-PRC and S-SMC) [26][30] or phase-shift (PS-PRC, PS-SMC, A-PRC and A-SMC) [27][29][31] and type of the rectifier: passive (PRC-type) or active with secondary modulation (SMC-type). PRCs rely on resonance between equivalent inductance and capacitance of the circuit, while SMCs use an active rectifier, to force the primary currents of the input side switches to change direction and achieve clamping and soft switching for

semiconductors. Phase shift control requires that the CS switches should possess reverse voltage blocking capability. Assuming practical realization possibilities of this property (series diode or anti-series switch), it could lead to poor utilization of semiconductor devices. On the other hand, topologies with symmetric control have additional energy circulation and current stress on the CS switches and the transformer. Asymmetric parallel resonant (A-PRC) and secondary modulation based (A-SMC) converters [31] combine the properties of both groups to achieve better weighted performance over a wide range of operating conditions, however, their peak efficiency is limited.

As it follows, all the concepts referred to possess various advantages and limitations and careful analysis is necessary to choose the most suitable topology for a particular application and operating conditions. However, the converters were presented by different research groups with various design approaches and targeted specific application areas, while the analytical estimations and experimental results are often delivered for particular hardware components. Therefore, the existing study does not allow effective comparison of the existing solutions and assessment of their capabilities side-by-side, using the same criteria.

TABLE I

GENERAL PROPERTIES OF SELECTED SNUBBERLESS CONVERTERS

Topology	Total Switches	Active switches	Control method		Rectifier Type		Frequency		Reference	Figure
			Symmetric	Phase-shift	Passive	Active	Variable	Constant		
S-PRC	8	4	•		•		•		[26]	Fig. 1
PS-PRC	12	4		•	•		(•)*		[27]	Fig. 3
PS-SMC	12	8		•		•		•	[29]	Fig. 6
S-SMC	8	8	•			•		•	[30]	Fig. 8
A-PRC	10	4		•	•			•	[31]	Fig. 11
A-SMC	10	8		•		•		•	[31]	Fig. 13

*combined phase-shift and frequency modulation is proposed in the current study to extend soft switching range

The aim of the present research is to analyse existing snubberless current-fed dc-dc topologies and assess their advantages and limitations using a common approach. Despite extensive research in this field, proper characterization, comparison, and justification of application capabilities have not been addressed and this paper aims to fill this gap. The design and comparison criteria applied to selected topologies are defined, followed by the derivation of equations and design parameters for each topology and corresponding characterization. The universal tool proposed in Section IV is proposed for assessment and comparison of the characteristics of different converters to choose the most suitable topology depending on its most probable operating point or other design preferences. Finally, obtained results are generalized in the conclusions.

II. Definition of comparison criteria

For the purposes of the current study, a generalized approach for comparison of topologies was used. However, certain assumptions and common criteria had to be defined. In the analysis, the components are considered lossless, the current ripple of the input inductor is negligible and the transformer magnetizing inductance is infinitely large. The converters are investigated for their capability of soft switching and stabilization of the output voltage during 1:2 input voltage and 10% to 100% load variations. For comparison, the equivalent inductance and capacitance parameters were chosen such that the converters CS stage should be capable of providing exactly 10% gain at full input voltage and desired power range, while the transformer turns ratio and base switching frequency were assumed to be the same. The voltage across semiconductors at the input side was not taken into account, as steady-state voltage stress is equal for all the converters analysed in the present study. It is equal to V_{out}/n.

The equations presented in the paper allow for optimized selection of parameters, considering the case study operating range and gain criteria. The maximum possible equivalent inductance that satisfies the criteria was chosen for each topology. It should be noticed that practical systems are usually designed with a certain safety margin to ensure desired operation conditions considering voltage drop in the components and possible transient or overload conditions. The exact selection of such margin depends on the practical components, application peculiarities and designer's choice. In the current analysis, safety margin was not included and the converters were dimensioned for an ideal case or borderline conditions.

The authors evaluated selected topologies in terms of the ratio between the rms input and the rms transformer primary current (I_{TXN}) as well as between the rms input and the cumulative rms current in primary semiconductors (I_{SN}) obtained with software models.

$$I_{TXN} = \frac{I_{TX(rms)}}{I_{in(rms)}}, \tag{1}$$

$$I_{SN} = \frac{\sum_{\substack{Switch \\ Primary}} I_{S(rms)}}{I_{in}}. \tag{2}$$

The I_{SN} estimation was made assuming that the reverse blocking devices are formed by two identical semiconductors connected in anti-series. This can be justified by the fact that in practical low voltage systems, synchronous MOSFETs are usually applied instead of diodes, while in higher voltage systems, the IGBTs and similarly rated diodes usually have comparable voltage drop. This approach allows a generalized converter comparison and assessment of theoretical performance and limitations for the same conditions and using common criteria, without narrowing down to a particular component or application peculiarities.

In the soft-switching CSC topologies analysed, the secondary part is generally of relatively higher voltage and thus its current is low and, consequently, its influence on the overall losses should not be significant, especially considering state-of-the-art SiC device characteristics. Moreover, the difference in secondary currents between the analysed converter was found to be relatively small and thus the analysis of the rectifier currents was omitted, as the input side losses are considered to be dominant.

III. Comparison of topologies

This section presents topologies selected for comparison and a brief description of their operation. The equations presented describe the characteristics and limitations of the converters and show derivation of the variables that are necessary for the current study. Each topology is analysed in terms of normalised current stress on the primary semiconductors and isolation transformer, followed by brief generalization.

A. Symmetric parallel-resonant CSC (S-PRC)

The symmetric parallel resonant CSC was proposed for fuel cell and PV applications in [24] and [25]. Full bridge version of the topology (S-PRC) is presented in Fig. 1 [26]. It uses symmetrical control and a passive rectifier. The modulation is based on the constant on-time control of the input stage and the regulation is achieved using frequency variation.

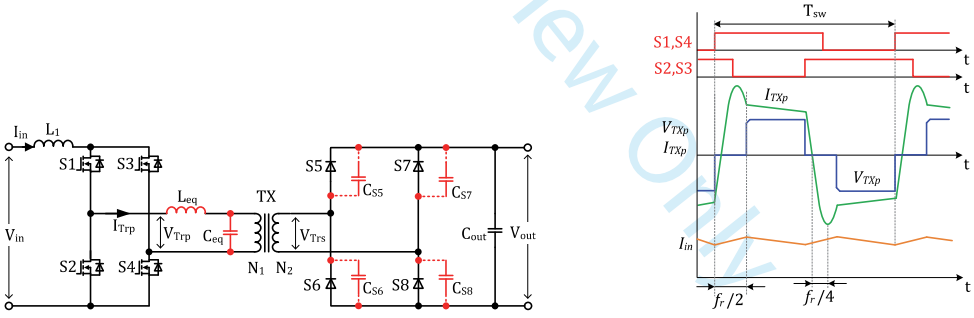


Fig. 1. S-PRC topology with reverse conducting switches at the primary and uncontrolled rectifier at the secondary side (a), generalized operating principle (b) [26].

For this topology, soft switching is achieved if the peak transformer primary (or input side switch) current $I_{S(peak)}$ is larger than the input inductor current.

$$I_{S(peak)} = \frac{V_{out}}{n \cdot Z_r} \geq I_{in}\,, \tag{3}$$

where V_{out} is the output voltage, n is the transformer turns ratio. The impedance of the resonant circuit Z_r is calculated by

$$Z_r = \sqrt{\frac{L_{eq}}{C_{eq}}}, \tag{4}$$

where L_{eq} is the equivalent circuit inductance (includes transformer leakage inductance) referred to the input side and C_{eq} is the equivalent capacitance, which can be represented by the intrinsic capacitance of the rectifier semiconductors and/or external capacitor(s).

To satisfy the soft switching criteria, the resonant circuit should be designed around minimum input voltage at full load. The required Z_r value should be chosen according to

$$Z_r = \frac{V_{out}}{n \cdot I_{S(peak)}} = \frac{V_{in(min)} \cdot V_{out}}{n \cdot P_{rated}}. \tag{5}$$

For a given switching frequency and gain, the required resonant frequency is calculated by

$$f_r = \frac{f_{sw}}{1 - 1/G}, \tag{6}$$

where f_{sw} is minimum switching frequency and G is the normalized voltage gain (G= 1.1 is assumed for the present study).

For this converter, the resonant process takes approximately 1/2 of resonant frequency f_r that is calculated by

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{eq} \cdot C_{eq}}}. \tag{7}$$

From (5)-(7), the equation for the required equivalent inductance can be derived

$$L_{eq} = \frac{Z_r}{2 \cdot \pi \cdot f_r}. \tag{8}$$

The associated resonant capacitance can then be calculated as

$$C_{eq} = \frac{L_{eq}}{Z_r^2}. \tag{9}$$

The gain of this converter G is not sensitive to load variations and is estimated from

$$G = \frac{V_{out}}{n \cdot V_{in}} = \frac{1}{1 - f_{sw} / f_r}. \tag{10}$$

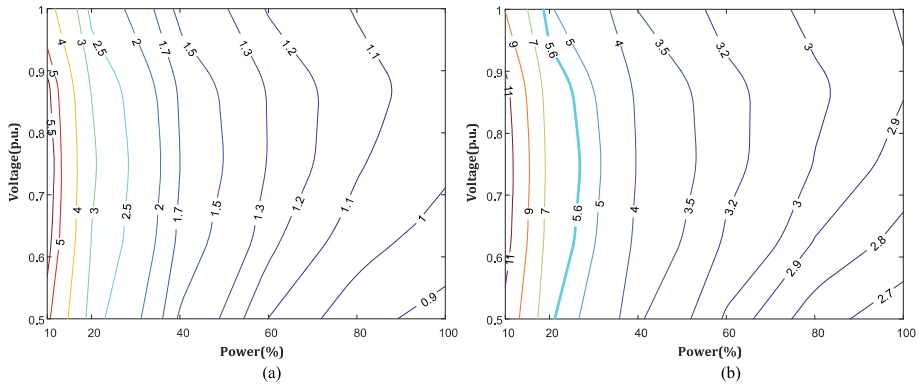


Fig. 2. Normalized transformer I_{TXN} (a) and total primary switch I_{SN} (b) rms currents of S-PRC, operating with case study power and voltage range.

Fig. 2 shows that the converter features low amount of energy circulation at full load, while dependency on the input voltage is relatively weak. Both transformer and primary transistor rms currents are very low at full load. However, as the power decreases, the energy circulation increases and at the lowest power, the transformer rms current is over 5, while the total transistor is over 10 times higher than the rms input current. To stabilize the output voltage at the case study operating conditions (1:2 voltage variations and 10~100% load change), the switching frequency of S-PRC has to be regulated in the range of 1:6, which makes it relatively difficult to achieve optimized magnetic component design.

B. Phase-shift parallel-resonant CSC (PS-PRC)

The phase-shift parallel-resonant converter (PS-PRC) topology proposed for high voltage dc applications in [27] and [36] (Fig. 3). It utilizes phase-shift control with constant switching frequency. The topology requires input side switches to have reverse blocking capability. Similar to the S-PRC presented above, it features the resonant circuit formed by L_{eq} and C_{eq} and a passive diode bridge rectifier with an output filtering capacitor.

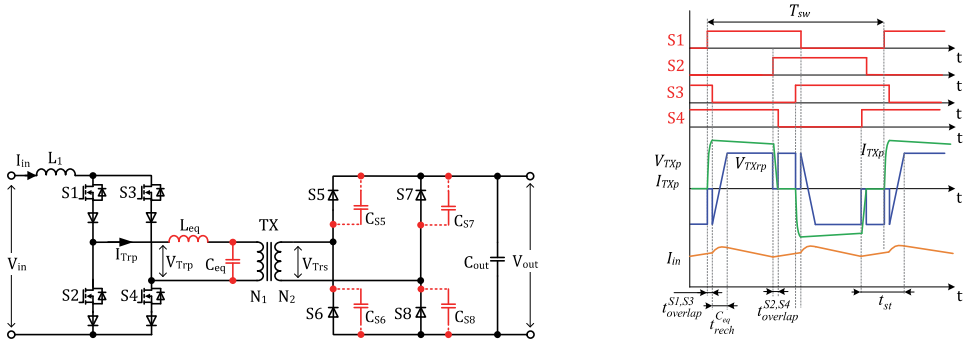


Fig. 3. PS-PRC topology with reverse blocking switches at the primary and uncontrolled rectifier at the secondary side[27].

The minimum gain of the converter is determined by three transient intervals: linear current transition between transistors S2 and S4, resonant current transition between transistors S1 and S3 and capacitor recharge time. The equations below are presented in general form to determine borderline conditions for the required G.

The time for linear transition between bottom devices S2 and S4 is calculated from

$$t_{overlap}^{S2,S4} = \frac{n \cdot I_{in} \cdot L_{eq}}{V_{out}}, \tag{11}$$

where I_{in} is the input current of the converter.

The resonant transition time between top devices S1 and S3 is estimated by

$$t_{overlap}^{S1,S3} = \frac{\arcsin\left(\frac{I_{in} \cdot n \cdot Z_r}{V_{out}}\right)}{2 \cdot \pi \cdot f_r}, \tag{12}$$

where Z_r is the impedance of the resonant circuit formed by L_{eq} and C_{eq}, which is calculated from (3). By the end of this interval, the remaining voltage across C_{eq} is

$$v_{C_{eq}} = V_{out} \cdot \cos\left(2 \cdot \pi \cdot f_r \cdot t_{overlap}^{S1,S3}\right). \tag{13}$$

The capacitor recharge interval is calculated from

$$t_{rech}^{C_{eq}} = \frac{\left(V_{C_{eq}} + V_{out}\right) \cdot C_{eq}}{n \cdot I_{in}}. \tag{14}$$

For the desired minimum gain, the total duration of the shoot-through state can be then estimated by the following:

$$t_{st(min)} = t_{overlap}^{S1,S3} + t_{overlap}^{S2,S4} + t_{rech}^{C_{eq}} = \frac{G-1}{2 \cdot G \cdot f_{sw}}. \tag{15}$$

By solving (11)-(15), the required equivalent inductance can be derived. From (14) it follows that capacitor recharge time is inversely proportional to the input current. Hence, at light load conditions, the recharge time as well as the converter gain are significantly increased. To ensure 1.1 voltage gain at 10% power, the resonant frequency should be more than two orders of magnitude higher than the switching frequency. In real systems it is, in general, not feasible and difficult to achieve, assuming practical application of parasitic parameters. Therefore, the parameters of the resonant circuit are instead calculated for 1.1 normalized gain, at full input voltage and full power. The converter gain characteristics depicted in Fig. 4 show that the converter will have problems with output voltage regulation at light loads. To operate at lower power levels, the authors propose to apply variable switching frequency control. The required switching frequency to provide desired voltage gain can be estimated from

$$f_{sw} = \frac{G-1}{2 \cdot G \cdot t_{st(min)}} \tag{16}$$

and the resulting characteristics are shown in Fig. 5a.

The input side switch rms current is not dependent on the operating point and is calculated by

$$I_{S(rms)} = I_{in} \cdot \sqrt{D} \approx 0.7 \cdot I_{in} . \tag{17}$$

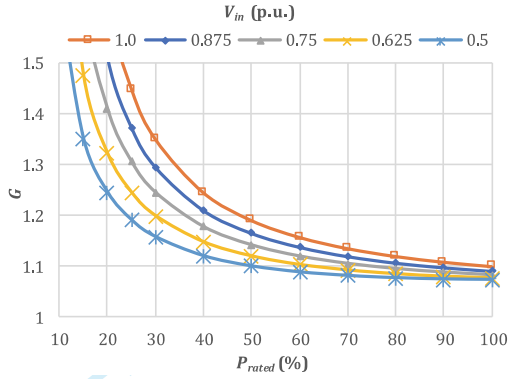
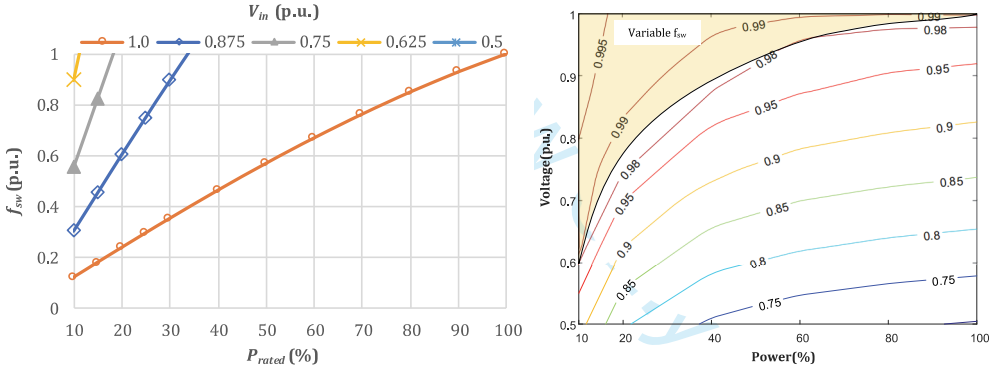


Fig. 4. Normalized gain G vs input voltage and power (L_{eq} is estimated for 100% load and voltage).



(a) (b)

Fig. 5. Switching frequency at different input voltages (a) and normalized transformer current I_{TXN} (b) in the case study operation range with marked variable f_{sw} area.

As it follows from (17), thanks to the phase-shift control and constant duty cycle, the rms current of any switch is always low. The transformer primary current has no circulating energy and is well utilized at all operating points due to combined phase-shift and frequency control (Fig. 5b). On the other hand, as the total number of semiconductor devices at the input side is increased by a factor of 2 as compared to S-PRC, the cumulative rms current of CS switches calculated by (2) is relatively high:

$$I_{SN} = \frac{\sum_{1}^{8} I_{S(rms)}}{I_{in(rms)}} \approx 5.6; \tag{18}$$

This value is constant over the input voltage and power variation range. Therefore, it is taken for reference in this study and depicted in bold for I_{SN} of other converters for better visibility. Another drawback of the converter is a rather complex dual-mode control with a wide range (up to 1:10 at maximum input voltage and minimum load) frequency modulation (Fig. 5a) to guarantee soft switching operation conditions for required power and voltage ranges, which complicates achieving electromagnetic compatibility.

C.Phase-shift secondary modulation-based CSC (PS-SMC)

The converter topology shown in Fig. 6 was presented in [29] for PV applications, initially featuring synchronous voltage doubler rectifier. Similar to the PS-PRC, the topology utilizes phase shift control and reverse blocking devices at the CS side. The peak current of the switches never exceeds the input current and its rms value can be estimated by (17). However, thanks to active switches in the rectifier, the PS-SMC does not depend on the resonant capacitor to create soft switching condition for the top transistors S1 and S3. Instead, this is achieved by modulating the rectifier and forcing the current transition between the transistors actively. The C_{eq} in this topology serves the purpose of reducing dv/dt across the turning-off rectifier transistor and its size the can be dimensioned with higher degree of freedom when compared to the PS-PRC. In some cases, the influence of the capacitor could be neglected, particularly considering the new generation of power transistors, such as GaN high-electron-mobility transistors (HEMTs), which have minor parasitic capacitance and turn-off losses.

The minimum gain of the converter is determined by four transient intervals: linear current transition between transistors S1 and S3, linear current transition between transistors S2 and S4, interval of energy return and, if present, capacitor recharge time.

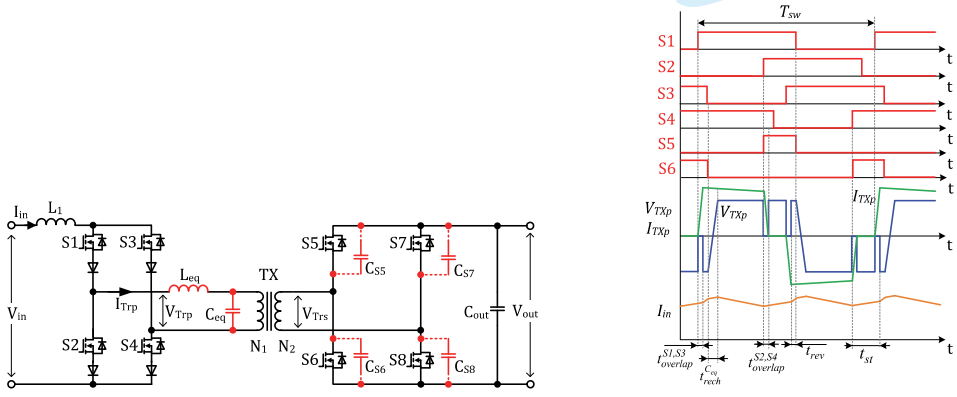


Fig. 6. PS-SMC topology with reverse blocking switches at the primary and active rectifier at the secondary side (a), generalized operating principle (b) [29].

Assuming an ideal case when t_{rev} is zero at maximum input current (at minimum input voltage and full load), the t_{rev} at actual input current is

$$t_{rev} = \frac{L_{eq} \cdot n \cdot (I_{in(max)} - I_{in})}{V_{out}}. \tag{19}$$

The minimum duration of the shoot-through state (ignoring input current ripple) is

$$t_{st(min)}^{L} = t_{overlap}^{S1,S3} + t_{overlap}^{S2,S4} = \frac{2 \cdot n \cdot I_{in} \cdot L_{eq}}{V_{out}}. \tag{20}$$

If C_{eq} is considered, then its recharge interval is added to the duration of the shoot-through t_{st}, since the average voltage across the input inductor during this time is equal to V_{in}. In this case, the minimum duration of the shoot-through state is

$$t_{st(min)}^{LC} = \frac{2 \cdot \left[(I_{in} \cdot n)^2 \cdot L_{eq} + C_{eq} \cdot {V_{out}}^2 \right]}{n \cdot I_{in} \cdot V_{out}}. \tag{21}$$

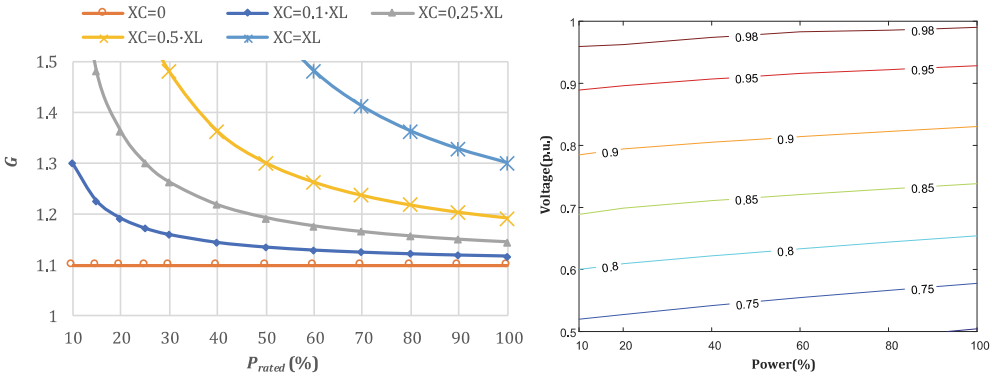
The normalized converter gain is calculated from

$$G = \frac{1}{1 - 2 \cdot f_{sw} \cdot \left(t_{st(min)}^{LC} + 2 \cdot t_{rev} \right)}. \tag{22}$$

The maximum leakage inductance value could be estimated for the desired voltage gain using the following equation:

$$L_{eq} \le \frac{V_{out} - \frac{V_{out}}{G}}{4 \cdot n \cdot f_{sw} \cdot I_{in(max)}}. \tag{23}$$

Equation (21) shows that similar to PS-PRC, the minimum gain of PS-SMC increases with a decrease in load and an increase of C_{eq}. Its influence on various values of C_{eq} is depicted in Fig. 7a. As shown, without the capacitor, the converter provides constant gain despite load variation and could operate with its basic phase-shift control algorithm. On the other hand, especially for significant values of C_{eq}, more complex control strategy would be required. Otherwise, the topology shares advantages and drawbacks of PS-PRC: the transformer is well utilized (Fig. 7b) and while the primary switch rms current is low, the cumulative rms current is increased due to the high number of devices in the CS part (18).



(a) (b)

Fig. 7. Normalized G vs. power and C_{eq} when L_{eq} is chosen for 100% load and voltage (a); normalized transformer current I_{TXN} (b) at the case study operation range.

D.Symmetric secondary modulation-based CSC (S-SMC)

The secondary modulation technique for LL-type current-source converter was introduced in [28] for energy storage interface in fuel cell vehicle applications. The full-bridge full bridge version of symmetrically controlled secondary modulated CSC (S-SMC) was presented in [30]. Similar to PS-SMC, the secondary modulated rectifier is used to create soft switching condition for the CS switches. It utilizes traditional reverse conducting transistors with antiparallel diodes at the CS side. At the same time, it keeps the advantages of the PS-SMC: constant switching frequency operation and certain degree of freedom when selecting C_{eq}, which is also used to reduce dv/dt across the turning-off rectifier transistor. As in the case of S-PRC, the soft switching condition is satisfied if the peak voltage of the CS transistors and transformer primary is higher than the input voltage. Thus, the energy circulation at certain operating points is increased. On the other hand, this brings an advantage: since C_{eq} recharges with increased current, the recharge time does not affect the resulting converter gain as much as in the case of PS-PRC and PS-SMC at low power levels.

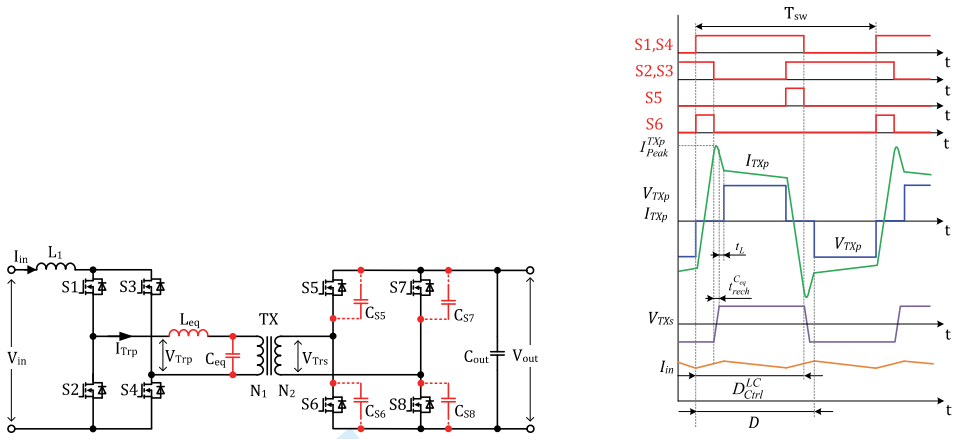


Fig. 8. S-SMC topology with reverse conducting switches at the primary and active rectifier at the secondary side (a), generalized operating principle (b)[30].

The equivalent duty cycle of the switches for the S-SMC is estimated by

$$D = 1 - \frac{n \cdot V_{in}}{2 \cdot V_{out}} = 1 - \frac{1}{2 \cdot G}. \tag{24}$$

For this topology, the value of L_{eq} should be dimensioned for full input voltage and load. Neglecting the influence of C_{eq}, its value for the desired minimum normalized gain (G=1.1) can be estimated by

$$L_{eq} \le \frac{V_{in(max)} \cdot V_{out} \cdot \left(1 - \frac{1}{G}\right)}{4 \cdot n \cdot f_{sw} \cdot P_{rated}}. \tag{25}$$

Taking into account the influence of the leakage inductance, the actual duty cycle of the switches is calculated by

$$D_{Ctrl}^{L} = D - t_L = \frac{3}{4} - \frac{n \cdot \left(V_{in} - 4 \cdot I_{in} \cdot L_{eq} \cdot f_{sw}\right)}{4 \cdot V_{out}} \le D. \tag{26}$$

The peak current of the CS transistors is derived by

$$I_{S(peak)} = \frac{I_{in}}{2} + \frac{V_{out} - V_{in} \cdot n}{8 \cdot L_{eq} \cdot f_{sw} \cdot n}. \tag{27}$$

As shown, the peak primary transistor current depends on both the input voltage and power levels. Ideally, it is equal to the input current at full input voltage and full load condition. The peak current through the transformer primary is the sum of currents of CS switches

$$I_{Peak}^{TXp} = I_{Peak}^{SwL} + \left(I_{Peak}^{SwL} - I_{in}\right). \tag{28}$$

Due to the relatively high peak current of the transformer (28), the capacitor recharge time is reduced significantly and for $X_C << X_L$ is approximated by

$$t_{rech}^{C_{eq}} = \frac{2 \cdot n \cdot C_{eq} \cdot V_{out}}{I_{Peak}^{TXp}}. \tag{29}$$

Similar to the PS-SMC, the voltage across the input inductor during the C_{eq} recharge time is equal to the input voltage. Taking into account the influence of both L_{eq} and C_{eq}, the duty cycle of the transistors is calculated by

$$D_{Ctrl}^{LC} = D_{Ctrl}^{L} - t_{rech} \cdot f_{sw}. \tag{30}$$

The minimum shoot-through time of the converter is

$$t_{st(min)} = t_{Ctrl} + \left(t_{Ctrl} - t_{overlap}^{S2,S4}\right) + t_{rech}^{C_{eq}} = \frac{2 \cdot D - 1}{f_{sw}} - \frac{2 \cdot I_{in} \cdot L_{eq} \cdot n}{U_{out}} + \frac{2 \cdot n \cdot C_{eq} \cdot V_{out}}{I_{Peak}^{TXp}}. \tag{31}$$

Considering both L_{eq} and C_{eq}, the output voltage is estimated by

$$V_{out}^{LC} = \frac{n \cdot V_{in}}{2 \cdot f_{sw} \cdot \left(t_{overlap}^{S2,S4} - t_{rech}^{C_{eq}}\right) + 3 - 4 \cdot D}. \tag{32}$$

The data obtained with (32) are depicted in Fig. 9, showing the corresponding changes of the converter gain for various values of C_{eq}, which is linear for all the conditions analysed. With variable duty cycle, the converter can to a certain point negate the influence of L_{eq} and C_{eq}.

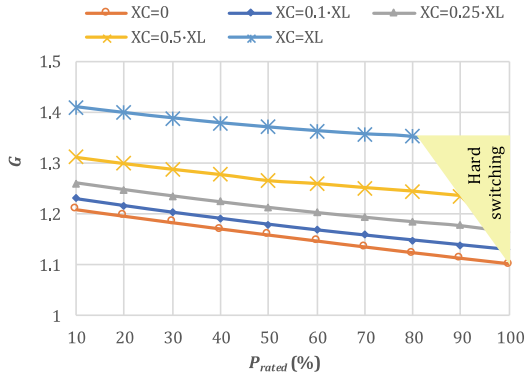
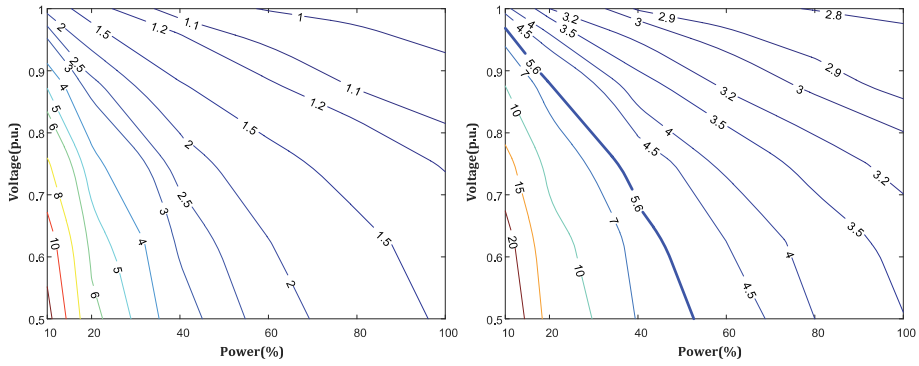


Fig. 9. Normalized G vs. power and C_{eq} when D is constant and L_{eq} is chosen for 100% load and voltage.



(a) (b)

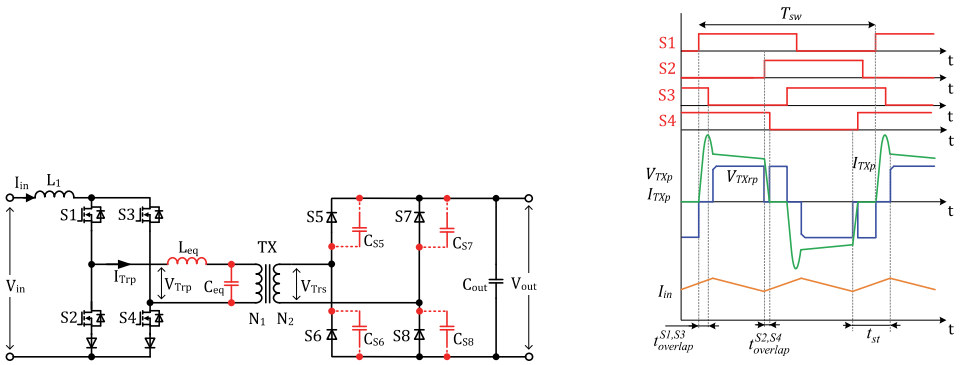
Fig. 10. Normalized transformer I_{TXN} (a) and total primary switch I_{SN} (b) rms currents of S-SMC, operating with case study power and voltage range.

Fig. 10 shows that the converter features low circulating energy at full load and full input voltage, but the dependency on the power decrease is very high. While both the normalized currents of the transformer and the primary transistor are very low at full load and maximum input voltage, at a decrease of any of them, the energy circulation increases and, at the minimum power of 10% power and lowest input voltage, the transformer rms current is over 20, while the total transistor is over 10 times higher than the rms input current.

E. Asymmetric parallel-resonant CSC (A-PRC)

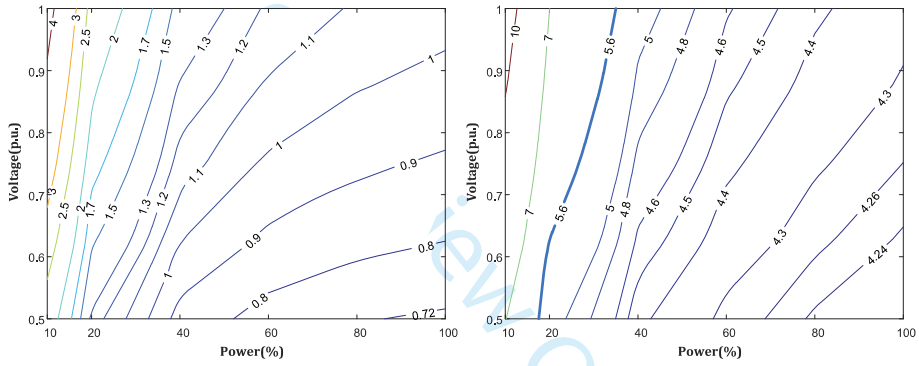
The asymmetric parallel resonant converter (A-PRC) concept proposed in [31] aims to reduce the negative impact of increased energy circulation of CSCs with symmetric control and increased conduction losses in converters with phase-shift control. In the A-PRC, the two top switches are reverse conducting devices, while the two bottom switches provide reverse blocking. The A-PRC features a passive rectifier and the output is regulated by phase-shift control. The resonant circuit is used to create soft switching condition for the top devices, while the bottom ones commutate naturally. As a result, during the resonant period, the current is circulating only through top devices, while the transformer energy circulation and the number of devices are moderate.

To provide soft switching operation, the peak resonant current should be higher than the maximum input current. The resonant frequency is calculated by (7) and the resonant circuit parameters by (8) and (9). Unlike the PS-PRC, the resonant capacitor recharges faster with increased current and the converter gain is not increased at light loads. Therefore, unlike other parallel resonant converters described in this study, the A-PRC can provide desired regulation capability with the phase-shift control only.



(a) (b)

Fig. 11. APRC topology with uncontrolled rectifier at the secondary side (a), generalized operating principle (b) [31].



(a) (b)

Fig. 12. Normalized transformer I_{TXN} (a) and total primary switch I_{SN} (b) rms currents of A-PRC, operating with case study power and voltage range.

The characteristic in Fig. 12a shows that both the transformer and the primary switches have moderate current stress with A-PRC. When compared to S-PRC, the current circulation in the transformer is generally slightly lower. However, the I_{SN} is higher for all cases, except for very light load condition (Fig. 12b). On the other hand, these I_{SN} values are lower than or comparable to those of PS-PRC for the load above 20%.

F. Asymmetric secondary-modulated CSC (A-SMC)

Similar to A-PRC, the asymmetric secondary modulation-based converter (A-SMC) shown in Fig. 13 features two reverse conducting and two reverse blocking devices in the primary side. However, thanks to the active rectifier at the secondary side, it does not rely on a resonant circuit to create soft switching condition for the top devices. Therefore, a certain degree of freedom when selecting the C_{eq} is present, as in the case of S-SMC.

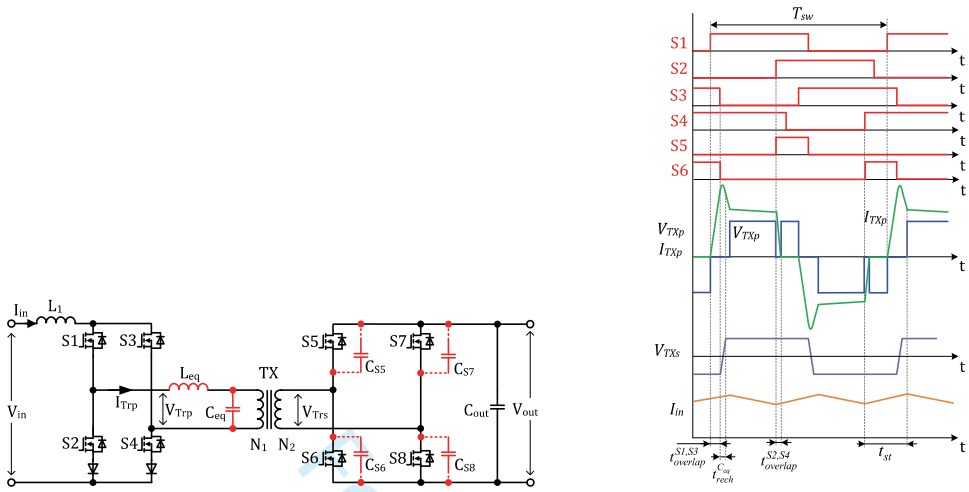


Fig. 13. Topology with active rectifier at the secondary side (a), generalized operating principle (b) [31].

The maximum leakage inductance is calculated by (25). In the ideal case, the peak current of the top switches and the transformer primary are equal to the maximum input current. The peak is diminished at the minimum input voltage and full load and its duration is

$$t_{peak} = \frac{2 \cdot n \cdot \left(I_{in(max)} - I_{in} \right) \cdot L_{eq}}{V_{out}}. \tag{33}$$

The minimum duration of the shoot-through state is

$$t_{st(min)}^{L} = \frac{2 \cdot n \cdot I_{in(max)} \cdot L_{eq}}{V_{out}}. \tag{34}$$

The C_{eq} is always recharged with maximum input current and including its recharge time, the minimum shoot-through state duration is estimated from

$$t_{st(min)}^{LC} = \frac{2 \cdot \left[L_{eq} \cdot \left(n \cdot I_{in(max)} \right)^2 + C_{eq} \cdot {V_{out}}^2 \right]}{n \cdot \left(n \cdot I_{in(max)} \right) \cdot V_{out}}. \tag{35}$$

As shown in Fig. 15, the recharge time of C_{eq} is independent of the converter power. Therefore, unlike PS-SMC, it can be designed for a relatively large C_{eq} and its output voltage regulation capability is not diminished at light loads. According to Fig. 15, the converter characteristics are slightly superior, but otherwise very close to those of A-PRC.

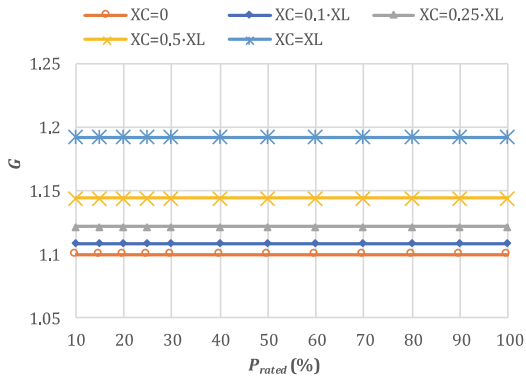


Fig. 14. Normalized gain vs power and C_{eq} when L_{eq} is chosen for 100% load and voltage for G=1.1.

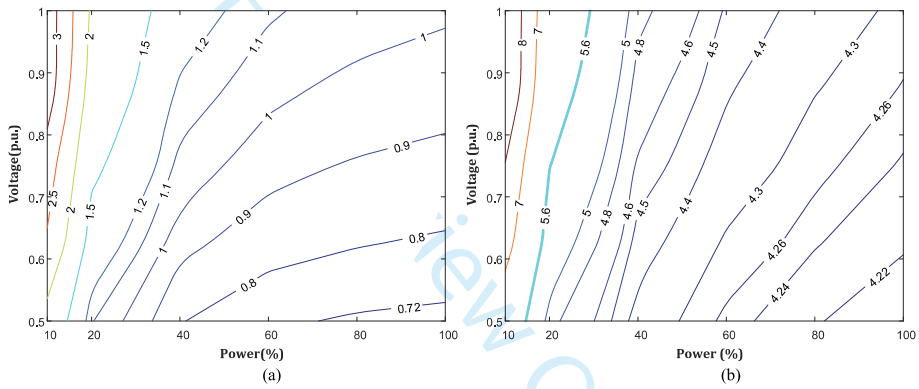


Fig. 15. Normalized transformer I_{TXN} (a) and total primary switch I_{SN} (b) rms currents of A-SMC, operating with case study power and voltage range.

IV. Comparative analysis and discussion

The analysis in the section above showed that among presented snubberless converters and criteria selected for the present study, each topology features certain drawbacks and no distinctly superior solution exists. This section describes devoted to evaluative comparison and analysis of investigated topologies. The data presented previously are represented using common graphs that can be further used as universal tools for topology selection according to the most probable operating region of a particular application.

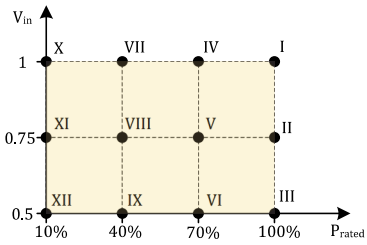


Fig. 16. Operating points selected for evaluative comparison of case study converters.

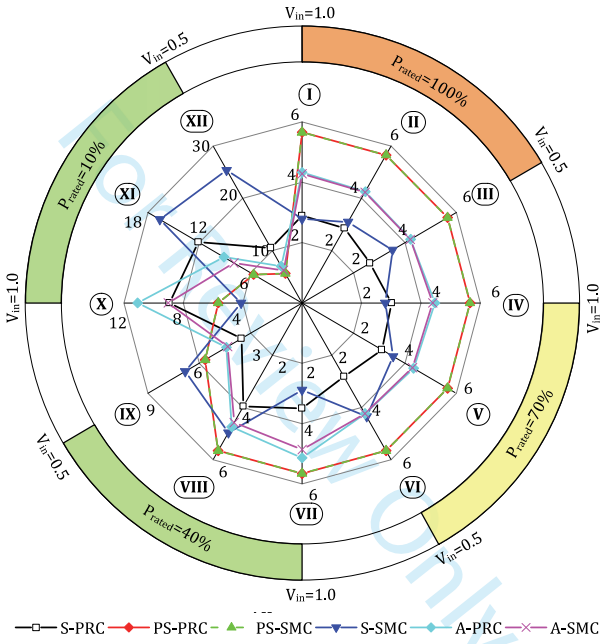


Fig. 17. Comparative graph showing I_{SN} of case study converters at chosen operating points.

The tool describing the total normalized primary semiconductor current I_{SN} of the topologies compared, depicted in Fig. 17, is based on twelve data points marked in Fig. 16. The performance of all converters analysed could be evaluated at a glance by comparing the corresponding encircled areas. As anticipated, the phase-shift topologies have high I_{SN} and thus the silicone utilization is low at most of the operating points selected (they are outperforming other solutions only at lowest power ratings). On the other hand, the symmetric topologies are generally superior at high load conditions and the S-PRC converter has relatively low I_{SN} for most of the points analysed.

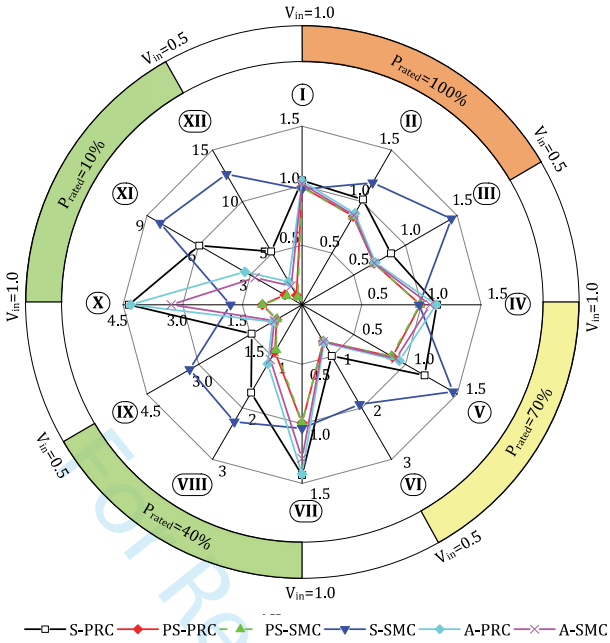


Fig. 18. Comparative graph showing I_{TXN} of case study converters at chosen operating points.

The normalized transformer primary current I_{TXN} for operating points marked in Fig. 16 is shown in Fig. 18. As expected, the performance of phase-shift topologies is clearly superior: both symmetric topologies have significantly higher rms current of the transformer, especially at low input voltage and at low power conditions. The asymmetric topologies show average performance in terms of both I_{SN} and I_{TXN}, with A-SMC having a slight advantage over A-PRC at some operating points.

Additionally, the converters can be compared in terms of relative leakage inductance requirements. The characteristics presented in Fig. 19 show that S-SMC can satisfy case study criteria with the highest L_{eq} value, while the PS-PRC converter still has the strictest equivalent inductance requirements, even despite the multi-mode control method proposed. It should be noticed that if the secondary-modulated converters feature remarkable equivalent capacitance, the maximum allowable L_{eq} value will decrease substantially.

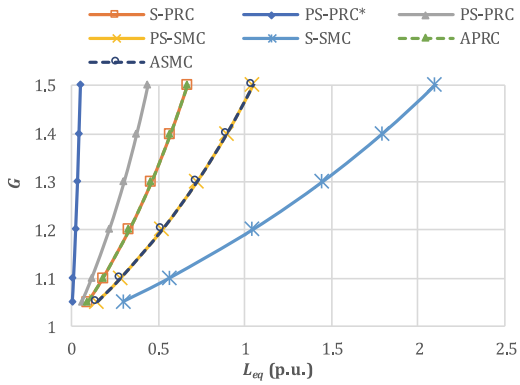


Fig. 19. Relative maximum L_{eq} vs. G for analysed converter topologies for case study design criteria (XC=0, U_{in}=1.0, P_{rated}=100%.);

*the values assuming constant f_{sw}.

On the example of S-SMC in Fig. 17, it is shown that the topology has low I_{SN} at one voltage level (V_{in}=1.0). Taking into account inherent bidirectional operation capability, this topology can be recommended for storage systems with small voltage variations, like lithium-iron-phosphate (LFP) battery-based energy storage applications. On the other hand, the PS-PRC and PS-SMC having the lowest I_{TXN} (Fig. 18) can be recommended for applications that aim for the lowest isolation transformer requirements, such as high-power systems where magnetic component costs are significant [38], or for the systems that process most of the power at low power conditions. For a more general representation, various parameters and properties of topologies analysed are summarized in Table II, where the control complexity is estimated empirically, taking into account design constraints, number of controlled semiconductors and complexity of control, while the transformer and the switch current values are presented in relative terms over the selected input voltage range.

TABLE II

EVALUATIVE COMPARISON OF SELECTED SNUBBERLESS CONVERTERS

Topology	Reference	Total (Active) switches	Transformer current (p.u.)		Primary switch current (p.u.)		Design/control complexity
			Full load	Low Load	Full load	Low Load	
S-PRC	Fig. 1 [26]	8(4)	0.83	0.70	0.50	0.70	moderate/high
PS-PRC	Fig. 3 [27]	12(4)	0.71	0.13	1.00	0.36	high/very high
PS-SMC	Fig. 6 [29]	12(8)	0.71	0.11	1.00	0.36	low/moderate
S-SMC	Fig. 8 [30]	8(8)	1.00	1.00	0.56	1.00	low/low
A-PRC	Fig. 11	10(4)	0.74	0.43	0.75	0.58	moderate/moderate
A-SMC	Fig. 13	10(8)	0.72	0.35	0.76	0.55	low/moderate

V. Conclusions

Focus was on the analysis of snubberless current source isolated full bridge converters. In such topologies, the clamping and soft switching are provided without dedicated external circuits, such as active or passive clamps. Instead, this is achieved by using parasitic parameters of the circuit or by relatively small external components. Based on this assumption, six reported topologies were selected for the analysis. The parameters of the topologies were derived using common design constraints to provide clamping and soft switching operation at a wide range of operating conditions. The analytical equations derived can be used to calculate the parameters of the circuit for various applications.

The analysis showed that symmetric topologies have low energy circulation in primary semiconductors at high power levels, while for phase-shift topologies, the normalized switch current is always constant. The symmetric topologies have, in general, better characteristics at higher power levels. The S-PRC topology has low dependence of the circulating energy on the input voltage variation, while the S-SMC features small dependency on load at maximum input voltage. On the other hand, at light load operation, the symmetric snubberless topologies have high energy circulation in both transformer primary and semiconductors. At minimum power, the cumulative normalized primary switch current in symmetric converters is higher than that of the phase-shift and asymmetric ones, despite a lower number of semiconductor devices applied.

The estimation of the transformer current showed that the phase-shift topologies are superior at nearly all the operating conditions analysed and other topologies can reach comparable values only at a few operating points. The symmetric topologies feature the highest transformer primary current, especially at low loads. At the same time, asymmetric converters have relatively low transformer currents at high loads and at low input voltages.

It can be concluded that among the converters analysed, there is no clearly superior solution. The symmetric converters have the potential to reach the highest silicone utilization at a limited operation range; the phase-shift topologies have the lowest isolation transformer requirements, while the asymmetric converters are average in both and can provide better weighted performance if the converter has to operate at a wide range of continuously changing conditions.

The results and methods presented can be used as a universal tool for analysis at the selection of an optimal snubberless boost full bridge topology, based on the most probable operating point of the particular design. The proposed solution can be further extended to include other potential boost full bridge converters or applied to other converter types, such as LL-type (half-bridge) current-source converters.

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Soft-Switching Current-FED Flyback Converter with Natural Clamping for Low Voltage Battery Energy Storage Applications

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Abstract. This paper introduces a new galvanically isolated current-fed step-up dc-dc converter intended for high voltage gain applications. The converter have fully-controllable voltage doubler rectifier, with control signals synchronous to that of the inverter switches. The proposed converter can regulate output voltage within wide range of the power and input voltage variations. Proposed converter does not require snubbers or resonant switches and with proposed control sequence ensures switches operation under soft-switching conditions in all transient states. Soft-switching in semiconductors allows achieving high efficiency. Moreover, the input side current is continuous. The operating principle for the energy transfer from the current-fed to voltage-fed side is described, design guidelines along with experimental verification of the proposed converter are shown in this paper. The converter proposed can be used as a front-end converter for grid connected battery storage.

Keywords: Current-fed converter · Soft-switching · Flyback converter · ZVS · ZCS · Switching sequence · Clampless · Energy storage

1 Introduction

New trends in European Union green energy policy encourage use of distributed power generation sources [1]. For more efficient use of alternative energy sources in residential applications it is preferable to include battery energy storage (BES) to those systems [2–5]. Battery energy storage systems (BESS) are used as buffer to store exceeded energy so that later it can help to suppress grid shortages or even inject power to the grid in case of high electric energy demand. This helps to minimize the impact of renewable power generation sources on electric grid stability [6].

BESSs in residential installations have power rating up to 8 kW. Battery chemistry for battery energy storage also varies significantly. In recent years lithium iron phosphate (LiFePO4) batteries are preferable for residential usage as they have one of the highest safety and reliability characteristics among lithium batteries. Another important feature is that they can preserve nominal capacity even after few thousands of discharge-charge cycles [7–9].

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For connecting the BESS to the AC-grid the additional inverter stage is used. The intermediate DC-link of the system is traditionally formed by different voltage-fed (VF) DC-DC converters [10, 11]. One of the most reliable and widely used solution is dual active bridge (DAB) converter as they have soft switching capability and thus high operational performance [12]. Soft-switched current-fed (CF) converters with soft-switching capability is a topic of interest in recent years. Among them there are converters with additional clamping circuits [13, 14], with resonant-assisted transition [15], and others additional circuits [16, 17]. Additional advantage of current-source converters is continuous input current. This places them as preferable choice for battery powered applications [10, 11].

Fully-controllable switches at the rectifier side of isolated CF converters brings new challenges and benefits [18–26]. This paper introduces CF flyback DC-DC converter with novel regulation1 algorithm. This algorithm has duration of transient switching intervals that is constant in a whole operation range and so ensures soft switching across that range. High efficiency can be achieved due to minimizer dynamic losses even at relatively high operational frequencies.

2 Relationship to Smart Systems

Nowadays smart systems are used in all major sectors of human life such as healthcare, safety, automotive and environment. Typical smart system consist of diverse components that are usually physically organized in different physical nodes. And with the rapidly increasing interest in the concept of the Internet of things all those nodes and even entire systems have to be operating and connected to each-other all the time without any interruptions. To ensure this the most critical smart-systems accommodates backup battery-based power supplies. Battery energy storage in household is used to accumulate energy from renewable energy sources when it is not used or from the grid when it has a lowest price. After battery is charged it can be used when it is required by user or when grid is under heavy load and requires additional power. This means that battery energy storage together with smart learning system with energy demand tracking as a part of smart house can increase stability of local power supply system and decrease yearly average grid power usage. So a major research direction of power electronics in smart systems is the development of high-efficiency robust power converters for battery-storage.

3 General Description

Topology of the discussed converter is shown in Fig. 1. It can be considered as derivation of the CF dual-inductor push-pull topology [25] proposed earlier. It consists of the CF inverter with four-quadrant (4Q) switches at the input side and the controllable rectifier at the output VF side. Isolating transformer introduces additional step-up needed to interface low-voltage sources to the high voltage DC-link. Converter provides low level of ripple CF terminal that is faced to battery. By controlling the duration of the reactive energy circulation interval regulation of output voltage is achieved.

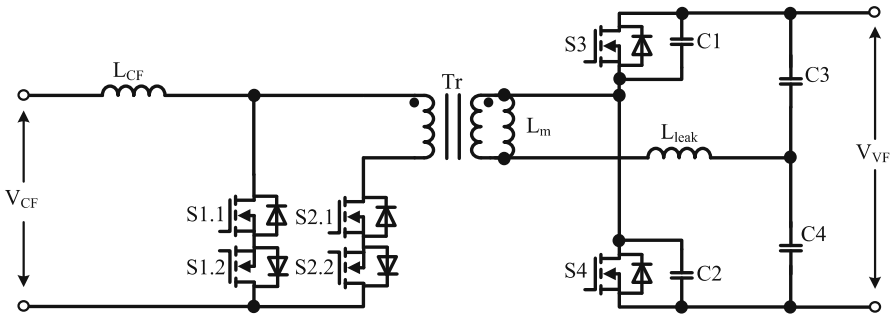

Fig. 1. Proposed converter topology.

Full soft-switching CF flyback converter topology can be used as interface power converter for connecting battery to the DC-grid or as the first conversion stage in AC-grid connected battery storage. In such applications the proposed topology and proposed control algorithm have the following distinguish features:

- High voltage gain that allows to use transformers with lower turns ratio to connect low voltage 12 V and 24 V batteries to a standard 400 V DC-grid.
- Current-fed terminal that ensures that the battery is operating with continuous input current. This allows increasing battery elements lifetime.
- Natural clamping of input inductor is achieved with the special control algorithm without any additional active or passive elements.
- Soft-switching is achieved in all switching elements through the wide operation range in both energy transfer directions.
- Reduced number of semiconductor devices as compared to the full-bridge boost converter (FSS-IFBBC) [24], and the same number of switches that in the dual inductor push-pull converter [25] and CF push-pull converter [26] that are using same control algorithm.
- High transformer utilization factor due to the double-ended operation with one part of the switching period (t0–t7) proposed topology operates similar to the flyback converter and during the other part (t7–t12) it operates similar to the forward converter.
- Transformer flux runaway protection capability without use of RCD snubbers or additional transformer windings.

During operation the transistors S1.2 and S2.2 are controlled synchronously to S1.1 and S2.1 and are turned off (acting like diodes) for transient intervals.

4 Converter Operation

This section describes converter operation with power flow from V_{CF} to V_{VF} terminal. Generalized control algorithm and simulated waveforms presented in Fig. 2. Switching period with the proposed control algorithm consists of twelve time intervals that are described in details further.

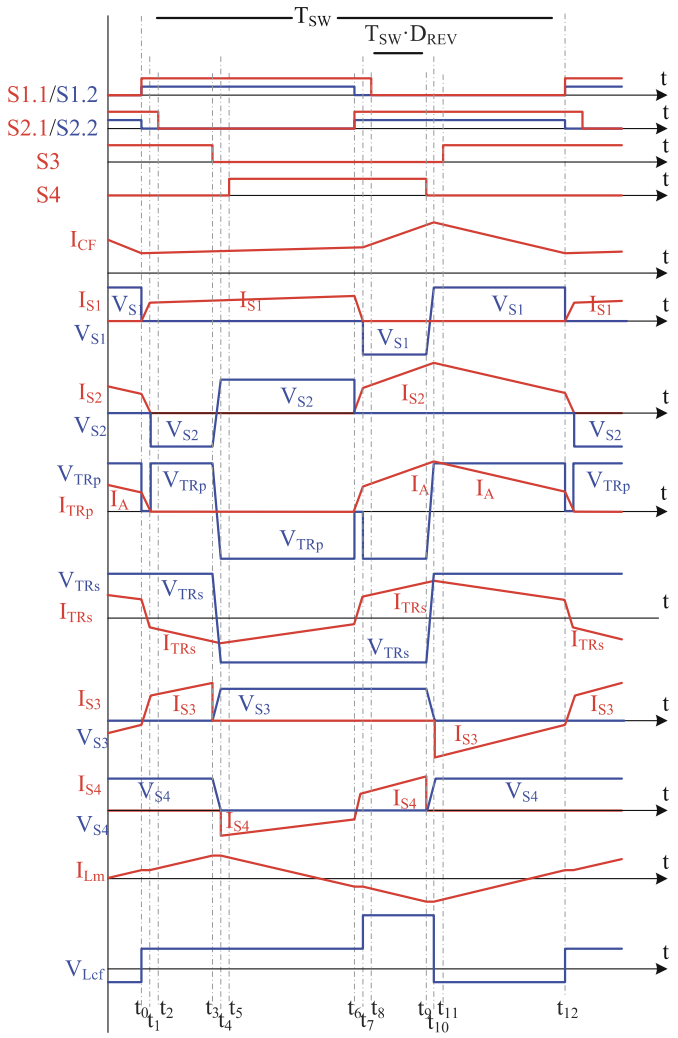

Fig. 2. Simulated operation waveforms.

Interval 1 ($t_0 < t < t_1$). Interval starts with turn off of switch S2.2. Current is been redirected to the body diode (BD) of S2.2. S1 with assistance of the transformer leakage inductance L_{leak} is turned on under soft-switching conditions. Leakage inductance acts like a snubber by slowing down current rise in S1 to separate voltage fall and current rise and thereby to minimize switching losses. The inductor L_{CF} is storing energy. Switch S3 is kept on forcing the inverter side transformer current to transfer from S2 to S1.

Interval 2 ($t_1 < t < t_2$). Interval starts after S2 current reaches zero and BD of S2.2 is turned off naturally. Inductor L_{CF} is storing energy from CF terminal. Transformer-magnetizing inductance starts accumulating energy from C3 through S3. The duration of this interval is calculated so that the current through S1 will have sufficient time to drop to zero at minimal input voltage at nominal power.

Interval 3 ($t_2 < t < t_3$). Interval starts with turning off switch S2.1 under ZCS conditions. Interval is needed to separate switching transitions in CF and VF sides and in most cases it can be omitted.

Interval 4 ($t_3 < t < t_4$). Switch S3 is turned off with soft-switching assisted by snubber capacitor C1. Capacitor C1 is charging from zero to VVF and C2 is discharged from VVF to zero. The transformer output The voltage polarity at the transformer output is changed.

Interval 5 ($t_4 < t < t_5$). Interval begins when the transformer current starts flowing through BD of S4. This interval is a part of power delivery mode from CF to VF terminal. Energy accumulated in the transformer magnetizing inductance L_M is delivered to the output terminal through the BD of S4. Interval duration is Duration of this interval is calculated so that it is equal to the snubber capacitor recharge time in point of the minimal operational power. In this case soft-switching will be achieved in the whole operation range while the conduction losses across BD will be minimized.

Interval 6 ($t_5 < t < t_6$). During this interval S4 turned on at ZVS conditions. Energy accumulated in L_M is delivered to the VF terminal through switch S4.

Interval 7 ($t_6 < t < t_7$). Switch transients on this interval are analogical to those **on interval 1**. 4Q switch S2 is turned on with soft-switching assisted by L_{leak}.

Interval 8 ($t_7 < t < t_8$). Interval is analogical to **interval 2**. At the beginning of interval current through S2 reaches zero by those forcing BD of S2.1 to turn off naturally. Reverse energy transfer interval is started. LCF accumulating energy from VF (C4 through S3 and Tr) and CF terminals.

Interval 9 ($t_8 < t < t_9$). During this interval S2.1 turned off under ZCS conditions. Processes in converter are analogical to **interval 8**. Duration of intervals 8 and 9 defines the converter gain factor.

Simplified converter voltage gain factor can be derived analogically to [25] and is expressed as follows:

$$F_{FRW} = \frac{V_{VF}}{2nV_{CF}} = \frac{2}{1 - 4 \cdot D_{REV}}, \tag{1}$$

where n is the transformer turns ratio.

Interval 10 ($t_9 < t < t_{10}$) and **Interval 11** ($t_{10} < t < t_{11}$). Are analogical to intervals 4 and 5 accordingly. Starting from instant t_{10} energy is delivered to transferred from the input to the output terminal through the transformer and body diode of S4 like in classical forward DC-DC converter.

Interval 12 ($t_{11} < t < t_{12}$). At the instant t_{11} switch S4 is turned on under ZVS conditions. Current is transferred from BD to switch thereby decreasing conduction losses.

5 Experimental Results

For the experimental study converter was designed to operate with a 4-cell $LiFePO_4$ battery was selected. Experimental prototype design parameters are shown in Table 1. Semiconductor devices parameters used are shown in Table 2.

Table 1. Converter parameters

Parameter	Decsignator	Value
Nominal power, W	P	100
CF voltage, V	V_{CF}	10–15
VF voltage, V	V_{VF}	400
Operation frequency, kHz	f_{SW}	100
Transformer turns ratio (Np/Ns)	N	1:6
Magnetizing inductance, mH	L_{TX_m}	3.4
Transformer secondary leakage ind., uH	L_{TX_leak}	8
Inductance of input inductors, uH	$L_{A, LB}$	44
Capacitance of output filter, uF	C_3, C_4	2.2
Capacitance of snubber, pF	C_1, C_2	265

Table 2. P semiconductor devices parameters

Component	Device	Parameters
CF MOSFETs	Infineon BSC035N10NS5	V_{DS} = 100 V; $R_{DS(on)}$ = 3.5 mΩ I_D = 100A, t_{rr} = 62 ns, C_{OSS} = 770 pF
VF MOSFETs	Infineon IPB60R190C6	V_{DS} = 650 V; $_{DS(on)}$ = 190 mΩ I_D = 59 A, t_{rr} = 430 ns, COSS = 85pF

Experimental data is shown in Table 3. The difference in theoretical and experimental voltage gains can be explained by the assumptions and simplifications used in theoretical equation.

Table 3. Experimental results forward operation

VCF, V	DREV	Theoretical gain	Experim. gain	Losses, W	η, %
10	0.104	3.42	3.33	7.89	92.11
11	0.086	3.05	3.03	6.29	93.71
12	0.069	2.77	2.78	5.39	94.61
13	0.051	2.51	2.56	4.53	95.47
14	0.033	2.31	2.38	3.81	96.19
15	0.017	2.15	2.22	3.66	96.34

6 Conclusions

A novel current-fed flyback converter was proposed and analyzed. One of the main features of proposed converter is that all semiconductors are operating under soft-switching conditions at all switching transients. Also proposed converter due to utilization of the circulating energy features higher DC voltage gain than in traditional current-fed converters. Moreover, due to the special control algorithm it futures natural clamping

of input inductor convertor does not require any additional clamping circuits. Peak power stage efficiency during experimental verification reached 96.34%. Converter switching frequency can be increased without significant efficiency drop thanks to the soft-switching operation. This allowing to decrease size and price of magnetic components and so the price of BESS in general.

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Educational institution	Graduation year	Education (field of study/degree)
Chernihiv National University of Technology	2013	Master of Science (with honors)
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3. Language competence/skills (fluent; average, basic skills)

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Ukraine	Native
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Period	Organization	Position
2016 –	Ubik Solutions OÜ	Software Engineer
2014 –	Tallinn University of Technology	Junior Researcher
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5. Honors & Awards

- 2016, Roman Kosenko, Best Poster Session Award - 5th International Doctoral School of Energy Conversion and Saving Technologies (IDS-ECST), Klapkalnciems, Latvia, May 27-29
- 2016, Roman Kosenko, IES Student Paper Travel Award, 10th International Conference on Compatibility, Power Electronics and Power Engineering, 29.06-01.07, Bydgoszcz, Poland
- 2015, Roman Kosenko, Diploma for High Level of Scientific Report and Practical Value of the Work -International Scientific-Technical Conference "Power Electronics and Energy Efficiency 2015", Kharkiv, Ukraine
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7. Grants & projects

- New Converter Topologies and Control Methods for Electronic Power Distribution Networks
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- New Power Quality Improvement Techniques for Distributed Generation Systems
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- High-Performance Impedance-Source Converters
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   - Aktiivsete elektrijaotusvõrkude muundurite topoloogiad ja juhtimismeetodid
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