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Research, Design and Implementation of Galvanically Isolated Impedance-Source DC-DC Converters

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology, has not been submitted for any academic degree.

Andrii Chub ……...

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ENERGEETIKA. ELEKTROTEHNIKA. MÄENDUS D79

Galvaaniliselt isoleeritud impedantsallikaga alalispingemuundurite uurimine, süntees ja rakendamine

ANDRII CHUB

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KIRJASTUS

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Andrii Chub

LIST OF ABBREVIATIONS

AC	Alternating Current
CCM	Continuous Conduction Mode
CS	Current-Source
CSC	Current-Source Converter
DC	Direct Current
EMI	Electromagnetic Interference
EPDN	Electronic Power Distribution Network
ESR	Equivalent Series Resistance
GI	Galvanically Isolated
GI ISC	Galvanically Isolated Impedance-Source DC-DC Converter
JFET	Junction Gate Field-Effect Transistor
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IqZSFPPC	Interleaved quasi-Z-Source-Fed Push-Pull Converter
IS	Impedance-Source
ISC	Impedance-Source DC-DC Converter
ISN	Impedance-Source Network
MIC	Module Integrated Converter
MLPE	Module Level Power Electronics
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
PCB	Printed Circuit Board
PCU	Power Conditioning Unit
PEC	Power Electronic Converter
PMSG	Permanent Magnet Synchronous Generator
PSM	Phase-Shift Modulation
PV	Photovoltaic
PWM	Pulse-Width Modulation
qZS	quasi-Z-Source
qZSC	Galvanically Isolated quasi-Z-Source DC-DC Converter
qZSI	quasi-Z-Source Inverter
qZSN	quasi-Z-Source Network
qZSSRC	Galvanically Isolated quasi-Z-Source Series Resonant DC-DC Converter
RES	Renewable Energy Source
RMS	Root Mean Square
RPM	Rotations Per Minute
SR	Series Resonant
SRC	Series Resonant Converter
ST	Shoot-Through
TUT	Tallinn University of Technology

VDR	Voltage Doubler Rectifier
VS	Voltage-Source
VSC	Voltage-Source Converter
VSI	Voltage-Source Inverter
WBG	Wide Bandgap
WT	Wind Turbine
ZCS	Zero Current Switching
ZEB	Zero Energy Building
ZS	Z-Source
ZSI	Z-Source Inverter
ZVS	Zero Voltage Switching

LIST OF SYMBOLS

$C_1 \ldots C_4$	capacitors of the qZS network
C_b	DC blocking capacitor
$C_{f1} \ldots C_{f2}$	filter capacitor of the VDR
C_r	resonant capacitor
$D_1 \ldots D_2$	qZS network diodes
D_A	duty cycles of an active state
$D_{r1} \ldots D_{r4}$	diodes of the VDR
D_{ST}	duty cycle of a shoot-through state
G	DC voltage gain
G_{norm}	normalized DC voltage gain
f_{qZS}	operating frequency of the qZSN
f_r	resonant frequency
f_{SW}	switching frequency
I_{CqZ}	qZSN capacitor current
I_{DC}	DC-link current
I_{D1}	qZSN diode current
I_g	grid current
I_{IN}	input current
I_S	switch current
$I_{TX,pr}$	primary winding current of the isolation transformer
$I_{TX,pr(av)}$	average current per half cycle of the resonant tank
$I_{TX,pr(m)}$	amplitude value of the current through the resonant tank
$I_{TX,sec}$	secondary winding current of the isolation transformer
L_1, L_2	inductors of the qZS network
L_3	tertiary winding inductance of the qZS coupled inductor
L_{f1}, L_{f2}	inductors of the grid side filter
L_{IN}	input inductor
L_{lk}	leakage inductance of the isolation transformer
L_m	magnetizing inductance of the isolation transformer
L_r	resonant inductor
n	transformer turns ratio of the isolation transformer
n_1	turns ratio of the qZS coupled inductor in the Gi ISCs with combined energy transfer
n_2	turns ratio of the isolation transformer in the Gi ISCs with combined energy transfer
P	operating power of a lossless converter
P_{IN}	input power
P_{OUT}	output power
P_r	power dissipated in the resonant tank
Q_g	total gate charge of a switch
Q_{OSS}	output charge of a switch
$R_{DS(on)}$	drain-source on-state resistance

R_g	gate resistance
R_{ld}	load resistance
R_r	resistance of the resonant circuit
S	main switch of the single-switch switching stage
$S_1 \ldots S_4$	inverter switches
S_{qZS}	switch of the synchronous qZSN
T	switching period
T_1	ISN coupled inductor in ISC with combined energy transfer, coupled inductor in couple-inductor-based ISC and isolation transformer in transformer-based ISC
T_2	isolation transformer in ISC with combined energy transfer
t_A	active state time duration
t_{off}	OFF-state time duration
t_{on}	ON-state time duration
T_{qZ}	coupled inductor of the coupled qZSN
t_{ST}	shoot-through state duration
TX	5-winding qZS coupled inductor
t_Z	zero state time duration
V_1	voltage of the qZSN imaginary DC-link
V_C	capacitor voltage
V_{CqZS}	qZSN capacitor voltage
V_{DC}	voltage of a common DC-bus
V_{dc1}	variable DC link voltage
V_{dc2}	stable DC link voltage
$V_{DC(\text{peak})}$	peak DC-link voltage
V_{D1}	qZSN diode voltage
V_{DS}	maximum drain-source voltage of MOSFET
V_F	forward voltage drop of a diode
V_G	gate voltage
V_{GS}	gate-source voltage
V_g	grid voltage
V_{IN}	input voltage
$V_{IN,\,min}$	minimum input voltage
$V_{IN,\,nom}$	nominal input voltage
V_{L1}	qZSN inductor voltage
V_{PV}	voltage of a PV module
V_{OUT}	output voltage
V_{RRM}	maximum repetitive peak reverse voltage
V_S	switch voltage
$V_{TX,pr}$	primary winding voltage of the isolation transformer
$V_{TX,sec}$	secondary winding voltage of the isolation transformer
φ	phase shift angle
η	efficiency of a converter

1 INTRODUCTION

The impedance-source converters are a novel line of investigation in the field of power electronics. The first impedance-source (IS) inverter proposed by Prof. F. Z. Peng in 2002 was introduced to overcome the limitations of the existing current- and voltage-source inverters [12]. This is a novel electric energy conversion technology that was supposed to be an alternative to existing approaches. The IS converters can be distinguished from the current- and voltage-source counterparts by means of an IS network (ISN) that is usually added at the input terminals. In general, an ISN consists of capacitor(s), inductor(s), and diode(s)/switch(es), which are connected in a special configuration. In case of inverters, an ISN enables any switching state, which makes the resulting inverter withstand the shoot-through (shortening all leg switches) or open states that are forbidden for either the current- or the voltage-source converters. Moreover, such switching flexibility allows considerable extension of the input voltage regulation range, which is desirable in many modern applications.

The IS networks can be applied to all types of electric energy conversion: DC-DC, DC-AC, AC-DC, and AC-AC to enhance performance of the existing solutions. Among them, the galvanically isolated (GI) IS DC-DC converters (ISC) which could become an enabling technology for modern power electronics applications such as renewable and alternative energy systems.

1.1 Galvanically Isolated Impedance-Source DC-DC Converters – A Novel Technology of Electric Energy Conversion

The first GI ISC was introduced in 2009 [13]. It was derived naturally from the Z-source (ZS) inverter by adding an isolation transformer, followed by a rectifier and a filter at the inverter output terminals. On the other hand, the derivation can be seen as adding an ISN between the input terminals and the inverter bridge [PAPER-I]. The first GI ISCs were based on ZS inverters and thus their application range was limited because of discontinuous input current. During last five years, numerous ISNs were applied in GI ISCs to improve the performance of the traditional ZS network. The quasi-Z-source (qZS) network derived from the ZS network quickly overtook a major position in this field, since it has all the advantages of the ZS network and introduces continuous input current [14].

The GI ISC is a technology alternative to the existing GI voltage-source (VS) and current-source (CS) converters, since it combines all their major features while adding extra benefits. Figure 1.1 shows the generalized block diagrams of the single-phase full-bridge converter for the three approaches. They are similar in structure, but the input side realization differs considerably: capacitors are used as an energy storage in the VS converters (VSCs) and inductors in the CS converters (CSCs), while the IS converter utilizes both

inductor(s) and capacitor(s) combined with diodes and/or switches. This allows higher DC voltage gain of the ISCs as compared to the CSCs. Also, the ISCs feature voltage step-down properties similar to those of the VSCs, when the averaging filter (e.g., *LC*) is introduced at the output side. A comprehensive comparison between CSCs, VSCs, and ISCs was performed by the author in [PAPER-I]. An important advantage of the ISC over its competitors is the flexibility of control, since it has no limitations of switching states, while CSCs cannot withstand open states, and VSCs suffer from shoot-through states.

It is known that the VSCs and CSCs can realize only a buck or a boost function, correspondingly. The regulation range can be extended if an additional converter or a switching stage is introduced to achieve buck-boost functionality [15]-[16]. For example, a converter for the renewable energy applications often has the boost converter at the input to adopt the widely changing input voltage.

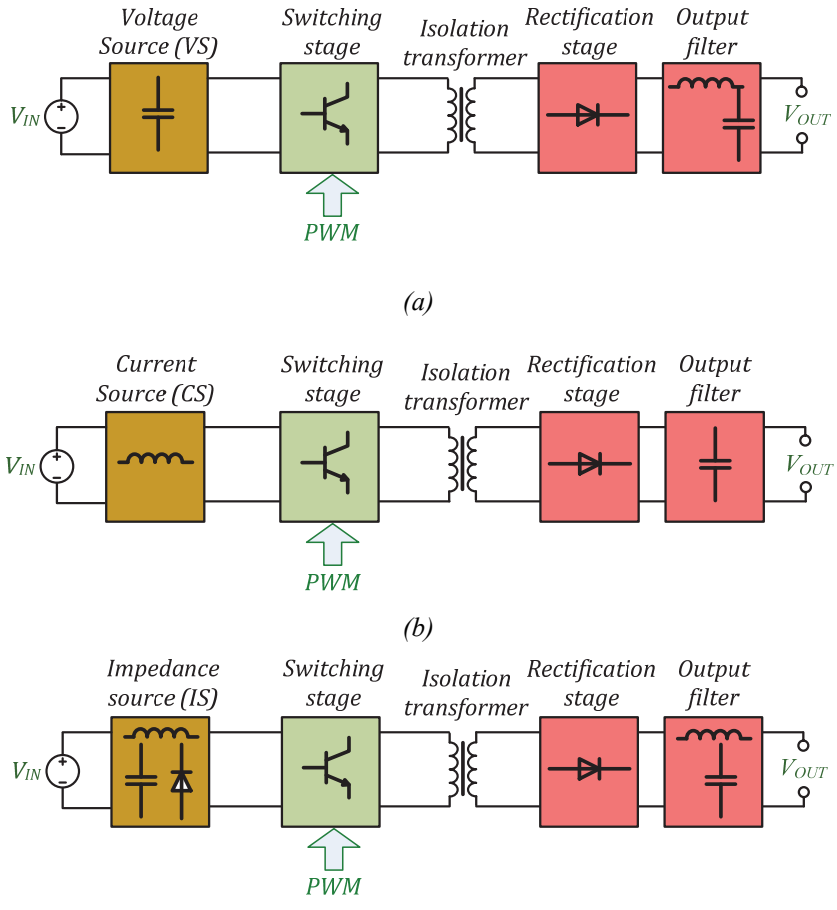


Figure 1.1 Generalized block diagrams of the VS (a), CS (b) and IS (c) GI DC-DC converters [PAPER-I].

The ISCs allow both the buck and boost functions using a single switching stage owing to the utilization of the shoot-through states for the voltage step-up, and zero states together with an averaging output filter for the voltage step-down. Another useful feature is an easy implementation of the bidirectional power transfer. Usually, it requires replacement of the diode(s) of the ISN with a switch. As a result, the ISN will operate as a filter during the reverse power flow [17]. This proves that the ISC technology is a versatile solution that corresponds to the demands of modern power electronics applications.

ISC operation with an averaging filter is similar to that of VSCs. It can be illustrated using the qZS converter as an example. Obviously, the duty cycle of the VSC switches never exceeds 0.5 when the ISC allows it to be increased up to 0.75 in the ideal case, which is usually limited to 0.65 to achieve acceptable efficiency [18]. Hence, the ISCs extend the regulation range of the VSCs (doubled range in the case of a qZS converter), as shown in Figure 1.2*a*. The voltage step-up principle of the ISCs (of their voltage-fed type, most widely used) is similar to that of the CSCs. The isolation transformer voltage is stabilized through the control of the shoot-through state duration. However, the influence of the shoot-through duty cycle is higher on the DC voltage gain of the ISCs (see Figure 1.2*b*) than that of the CSCs, since its normalized DC voltage gain is calculated as follows [48]:

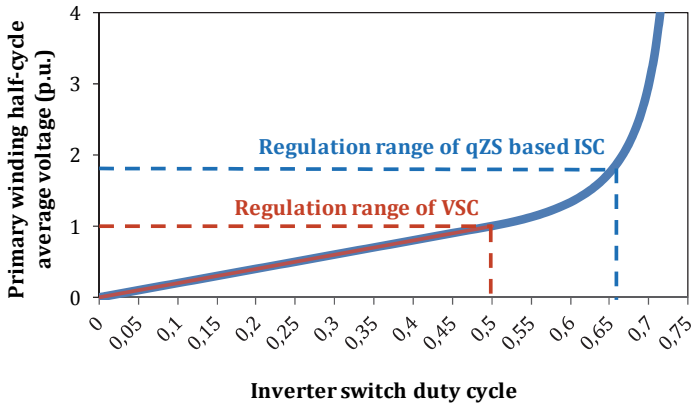
$$G_{norm} = \frac{V_{OUT}}{2 \cdot n \cdot V_{IN}} = \frac{1}{1 - 2 \cdot D_{ST}}, \tag{1.1}$$

where n is the isolation transformer turns ratio, and D_{ST} is cumulative duty cycle of the shoot-through states over the switching period. As a result, in the ISCs, the transformer transfers energy from the input to the output side during at least half of the switching period, not allowing narrow voltage pulses possible in the CSCs. Also, the ISCs avoid voltage clamping circuits needed in the CSCs.

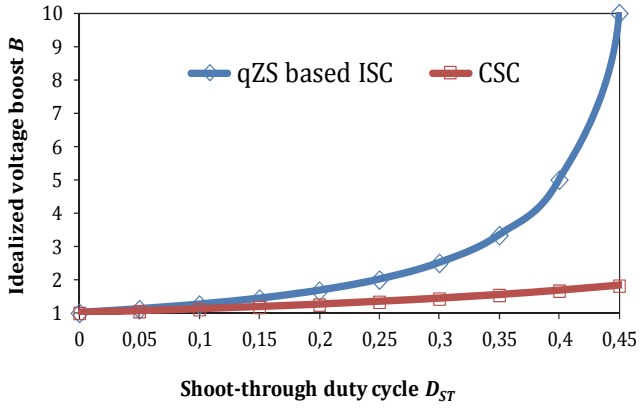
Resulting from the discussion above, it can be concluded that the GI ISCs are an independent class of converters alternative to the VSCs and CSCs. At proper implementation, significant benefits of the ISC over the traditional GI VSCs and CSCs can be shown. The most prominent features are regulation flexibility, power circuit versatility and inherent reliability [PAPER-I]. However, the ISN increases the complexity of the ISCs and can limit their efficiency, which is crucial for commercial success of this technology.

1.2 Motivation of the Thesis

Power electronics plays an extremely important role in human advancement even though it is not obvious and therefore undervalued sometimes. Switching power supplies are used with almost any consumer or industrial equipment. Recently, power electronics has penetrated into the applications of energy generation and distribution since outdated approaches cannot satisfy recent challenges imposed by increased dispersion and intermittent nature of modern energy generation units. The latest advances in this field are within the



(a)



(b)

Figure 1.2 Half-cycle average voltage of the primary winding of the isolation transformer as a function of the inverter switch duty cycle for the qZS-based ISC and the VSC (a) and idealized voltage boost factor B as a function of the shoot-through duty cycle D_{ST} for the qZS-based full-bridge ISC and the corresponding CSC [PAPER-I].

integration of the renewable and alternative energy sources into the power systems of the residential and small commercial buildings. Small renewable energy sources usually have output voltage well below the distribution grid voltage. In some cases, like photovoltaic (PV) module strings, they can be cascaded, but this approach limits the performance and scalability of the system. Therefore, parallel grid integration of the individual energy sources and storages has become a popular trend due to the high scalability of this approach and, consequently, good acceptance by the residential market [19]-[22]. However, high voltage step-up requires an efficient GI DC-DC converter with a wide input voltage range. If properly designed, the GI ISCs are able to satisfy all demands of a modern small-scale low-voltage renewable and alternative energy system.

Prior to this research, the GI ICSs were justified for fuel cell and small permanent magnet synchronous generator (PMSG) based wind turbines [24]-[25]. However, those reports are scarce and mostly limited to the same qZS full-bridge DC-DC converter. This is because of a limited number of the GI ISC topologies. In order to achieve best performance in each application, different topologies are required. In the author's opinion, the family of the GI ISCs is not limited to the full-bridge topologies since many other topologies, like half-bridge, push-pull or single-switch, can be introduced. A greater variety of topologies will allow us to select an ISC topology and tailor it for a particular application. However, this requires additional research.

This thesis research was conducted according the priority research program established in the Power Electronics Group of Tallinn University of Technology. The aim has been to synthesize novel power electronic converter topologies and their enhanced control methods and to verify them further experimentally in application to Electronic Power Distribution Networks (EPDNs). This research activity was initiated in cooperation with industrial partners from Estonia (Estel Elektro, 4Energia, Ubik Solutions, MS Balti Trafo, Clifton) and Norway (Vardar Eurus) in 2010. The studies have strong emphasis on industrial applications and market needs to achieve fast industrial approval of the technologies introduced and to increase their export potential. This research was supported by the targeted financing research project SF0140016s11 of the Estonian Ministry of Education and Research. Additional financial sources were as follows: grants PUT744 and PUT633 from the Estonian Research Council, project VE554 provided by the European Center for Power Electronics. Research related to power electronic converters for a resource efficient building was supported by the Estonian Centre of Excellence in Zero Energy and Resource Efficient Smart Buildings and Districts, ZEBE, grant 2014-2020.4.01.15-0016 funded by the European Regional Development Fund. Industrially oriented research on residential renewable energy systems was conducted in cooperation with Estonian enterprise Ubik Solutions Ltd. within the framework of the projects Lep13069, LEP15006 and Lep16005. Cooperation was supported by the project Va16021 between Estonian and Polish Academies of Science.

This PhD project is important for Estonian and European economy and applied science since it introduces new converter topologies that can improve energy conversion performance in the most challenging applications, like residential and small commercial PV systems or micro wind turbines. These technologies are already in great demand to satisfy Energy Performance of Buildings Directive introduced by the European Commission and to hit the European 20-20-20 targets by the year 2020.

1.3 Aims, Hypothesis and Research Tasks

The technology of the GI ISCs has not been accepted by industry yet although abundant research has been conducted, which is evident from

hundreds of published papers [23]. The advantages of this technology are still to be recognized, considering concerns about efficiency, power density and reliability imposed by an increased number of passive components.

The main aim of this PhD research was to synthesize and experimentally validate new topologies of the GI ISCs that show one or several of the following properties: reduced number of switches, reduced number of passive components, improved voltage step-up characteristics, high utilization of magnetic components combining their functionality, simple design and low cost of realization. Moreover, the author aims to show that the GI ISCs are a versatile technology that can be used in renewable and alternative energy systems to resolve limitations of the existing solutions based on VS and CS converters and to reduce the number of conversion stages. The outcomes of this thesis are expected to substantially advance the emerging field of the galvanically isolated impedance-source DC-DC converters and their application to renewable and alternative energy generation systems that enable new standards of living.

Hypotheses:

✦ Due to the different principles of energy transfer from the input to the output side, the GI ISCs cannot be treated in the same way as the corresponding IS inverters, where an IS network is used as a basic classification feature. In the GI ISC, the magnetic component(s) that transfers energy from the input side to the output side has to be used as a classification feature, while a particular IS network utilized is less important for the fundamental operation principle.

✦ Prior to this work, mostly the GI ISCs with the full-bridge switching stage were known. However, the switching stages with a reduced number of switches, like the push-pull, the half-bridge or the single-switch, can be applied to make the GI ISC technology more attractive in applications where the full-bridge switching stage could be avoided due to input voltage range or realization cost constraints.

✦ The GI ISCs utilize either isolation transformers or coupled inductors for energy transfer from the input to the output side. Both of these types of magnetic components can be applied simultaneously to achieve combined energy transfer with improved voltage step-up performance of the converter.

✦ The GI ISCs can improve energy performance and/or cost of realization of highly demanding renewable and alternative power generation systems intended for buildings with nearly zero energy consumption, a rapidly increasing demand within the following five years.

Research tasks:

✦ synthesis of hierarchically structured classification of the GI ISC topologies based on the type of magnetic component(s) transferring energy from the input to the output side as a basic classification feature;

✦ synthesis, analysis and verification of the GI ISC topologies with a reduced number of switches;

✦ analysis of implementation possibilities of the combined energy transfer and synthesis of corresponding ISC topologies;

✦ analysis of applicability of topologies proposed for renewable and alternative power generation systems;

✦ experimental evaluation of topologies selected for the integration of the renewable and alternative energy sources into residential and small commercial power systems.

1.4 Research Methods and Instruments

The mathematical analysis of the concepts proposed in this thesis is generally based on steady-state models derived using the traditional volt-second balance in inductors and the charge balance in capacitors (Eqs. (1.2) and (1.3)).

$$v_{L(av)} = \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} v_L(t) \cdot dt = 0 , \tag{1.2}$$

where $v_{L(av)}$ is the average inductor voltage, T_{sw} is the switching period and v_L is the instantaneous value of the inductor voltage.

$$i_{C(av)} = \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} i_C(t) \cdot dt = 0 , \tag{1.3}$$

where $i_{C(av)}$ is the average capacitor current and i_C is the instantaneous value of the capacitor current.

Results of the steady state analysis were verified with the PSIM simulation software with add-on "Thermal Module" to estimate the semiconductor power losses. Experimental verification was performed with the laboratory prototypes of different rated power from 250 W to 1300 W. The converters were supplied by DC power supplies from TDK-Lambda Genesys series (Gen 100, Gen 300 and Gen 600) or the solar array simulator Keysight E4360A and loaded by the programmable DC electronic load Chroma 63204 or passive load.

The experimental waveforms were captured with digital oscilloscopes Tektronix DPO7254 and MDO4034B-3 in conjunction with the AC/DC current measurement probes Tektronix TCP0030, Rogowski coil current probe PEM CWTUM/015/R, and HV differential voltage probes Tektronix P5205A. Several test-benches were created for the experimental study of the designed power electronic converters. Such test-benches for tests of power electronic converters intended for PV and variable speed micro wind turbines are shown in Figures 1.3 and 1.4, correspondingly.

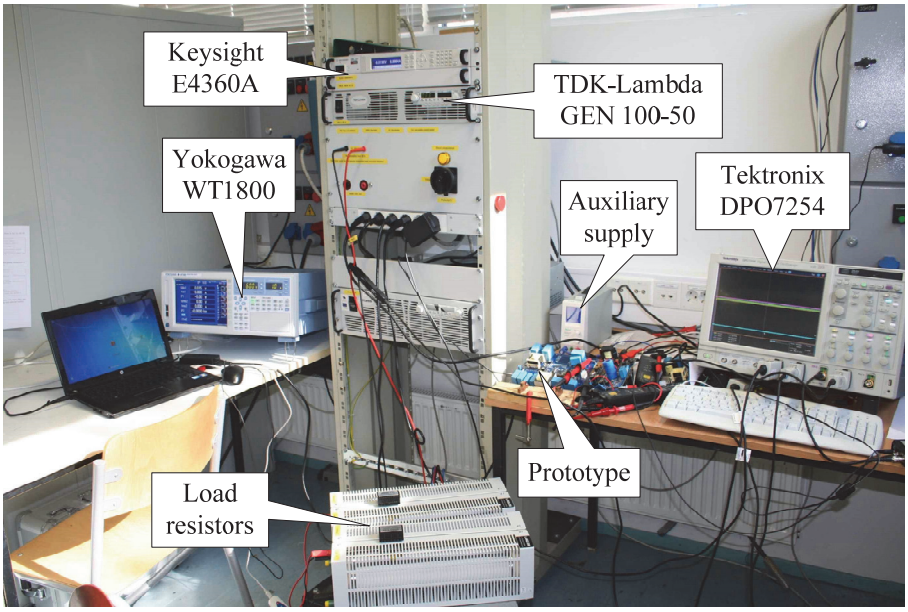


Figure 1.3 Photo of the test-bench used for the experimental study of PV module integrated converters.

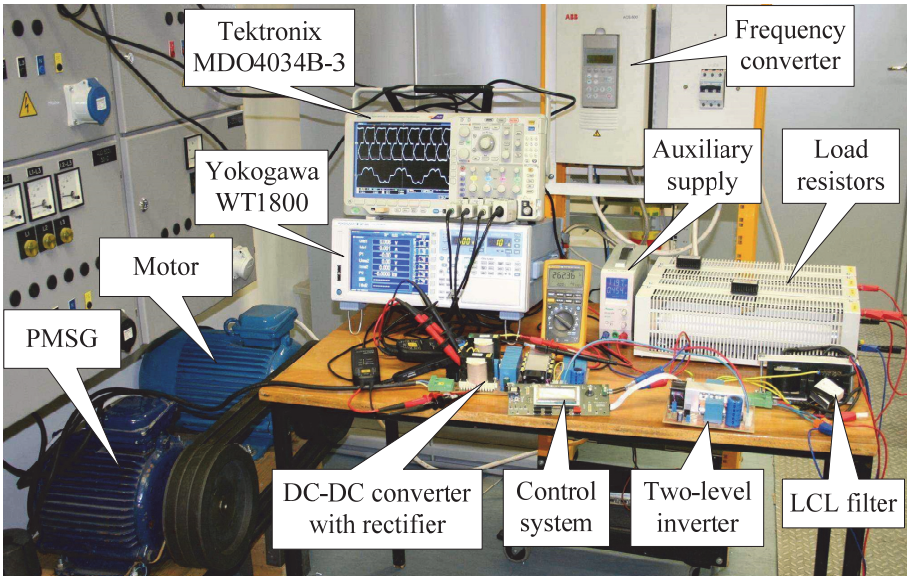


Figure 1.4 Photo of the test-bench used for the experimental study of the power conditioning unit intended for variable speed permanent magnet synchronous generator (PMSG) based micro wind turbines.

Experimental efficiency values of the converters were calculated as a ratio between the input and output powers (Eq. (1.4)), measured by the precision power analyzer Yokogawa WT1800:

$$\eta = \frac{P_{OUT}}{P_{IN}} \cdot 100\% = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} \cdot 100\% , \quad (1.4)$$

where P_{IN} is the input power, V_{IN} is the input voltage, P_{OUT} is the output power, V_{OUT} is the output voltage, and I_{OUT} is the output current.

1.5 Contribution and Dissemination

This thesis was intended as a pioneering research to enhance the family of GI ISCs with special emphasis on the classification and synthesis of topologies with reduced number of switches and/or passive components that suit well for renewable and alternative energy systems. The author has proposed numerous novel ISC topologies that can be tailored for different renewable and alternative energy applications to improve energy harvesting performance, efficiency, cost of realization, power density, etc. Knowledge obtained by the author advances this research field towards realization of the full potential of the ISC technology. The significant results gained in the application-oriented topics strengthen the position of the ISC technology further in the applied power electronics, targeted to industrial approval. The results obtained in this thesis contain both scientific and practical novelties.

Scientific novelties

- ✦ systematization and comparative analysis of the state-of-the-art GI ISC topologies and synthesis of versatile classification that can be also used as a derivation tool for new GI ISC topologies;
- ✦ synthesis, mathematical analysis and experimental validation of twelve novel types of the GI ISC topologies, five of which belong to a new class of GI ISCs introduced by the author;
- ✦ mathematical analysis and experimental validation of five existing topologies of GI ISCs: transformer-based full-bridge converter with synchronous rectification, with resonant switching (two topological variations), and two coupled-inductor-based push-pull converters.

To emphasize the contribution of this PhD research in the development of the GI ISCs area, the classified existing and proposed topologies are shown in Figure 1.5. The following color schemes of highlighting are used: topologies derived by the author are highlighted in yellow; blue color indicates the topologies that were investigated by the author and proposed by other researchers. White area denotes the topologies proposed by other researchers, the author did not contribute to these studies.

Practical novelties

- ✦ Four GI ISCs with a reduced number of switches were assessed as low-cost solutions for PV applications: two qZS asymmetrical half-bridge DC-DC converters, a qZS symmetrical half-bridge DC-DC converter and a qZS single-switch DC-DC converter.

✦ High-performance multi-mode quasi-Z-source series resonant DC-DC converter with a novel buck-boost control principle was experimentally validated for photovoltaic module level power electronics applications, where it can outperform all existing competitors.

✦ Single-switch quasi-Z-source DC-DC converter with a synchronous qZS network was experimentally validated as a low-cost PV module integrated converter for residential applications.

✦ Coupled-inductor-based quasi-Z-source single-switch DC-DC converter was proposed and verified experimentally as a novel intermediate stage of the power conditioning unit for residential variable speed wind turbines with a permanent magnet synchronous generator.

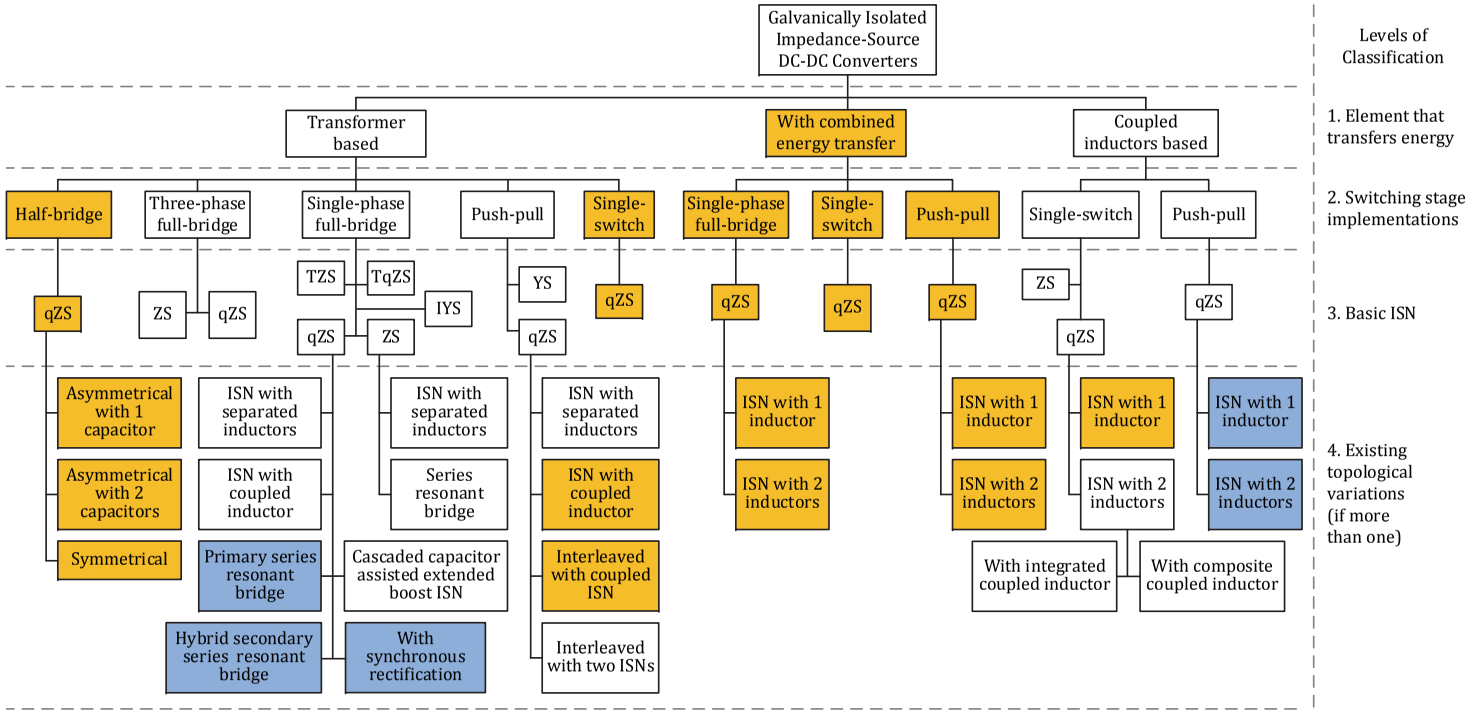
✦ Test power profile that simulates operation conditions with the generic 60-, 72- and 80-cell silicon PV modules with emphasis on the operation with 60-cell PV modules was proposed. It can be used as a novel performance assessment tool for PV module level power electronic systems.

✦ Detailed design guidelines were proposed for quasi-Z-source converters. They emphasize reduced input current ripple due to interaction between input wiring inductance and qZS coupled inductor, elimination of discontinuous conduction mode with synchronous rectification in the qZS network and superiority of a voltage doubler rectifier in voltage step-up converters.

The design guidelines for the quasi-Z-source GI DC-DC converters were described by the author in [5], [PAPER-IX]. Practical outcomes are already implemented in several products under development in the Estonian industrial company Ubik Solutions Ltd.

This thesis work contributes substantially to the advancement of the emerging field of the ISCs. Author's research in the field of GI ISCs was disseminated in **13** international conferences and **9** doctoral schools in the form of oral and poster presentations. Total number of author's papers published in this field is **28**, including **16** published in conference proceedings and **12** papers in peer-reviewed journals. In addition, the author has co-authored **2** manuscripts on qZS converters for PV applications and **1** manuscript on micro wind turbine applications, which are under current consideration in IEEE journals. Author had been granted **1** Latvian patent and **2** Estonian Utility Models. Also, the author has co-authored **1** book chapter "Wind energy systems" in the book "Power Electronic Converters and Systems: Frontiers and applications" published recently by IET [1].

Findings described in this PhD research thesis are based on **11** papers attached and listed in the List of Author's Publications. Among them, **6** papers were reported at **5** international conferences and workshops of IEEE, and **1** paper will be reported at IECON'2016 in October 2016. Another **4** papers have appeared or expected to appear in international peer-reviewed journals, of which one is under consideration, and two papers have been published or accepted for publication in the IEEE Transactions on Power Electronics.



qZS: quasi-Z-source; ZS: Z-source; TZS: trans-Z-source; TqZS: trans-quasi-Z-source; YS: Y-source; IYS: improved Y-source; ISN: impedance source network.

Figure 1.5 Proposed classification of the GI ISCs [PAPER-I].

2 STATE-OF-THE-ART IN GI ISCs

Section 1.2 clearly showed flexibility and numerous advantages of GI ISCs for emerging distributed generation applications. Roughly thirty topologies of GI ISCs were identified by the author in [PAPER-I]. However, earlier there was no clear understanding of how those numerous topologies can be organized into groups and classified. This section presents a brief overview of the GI ISCs, proposes a feature for classification and the resulting classification.

2.1 Feature Selection for Classification. Definition of Transformer and Coupled Inductor

Recently, several reviews and classifications for ISNs have been reported by the author and other researchers [2], [23]. However, in [PAPER-I] the author concludes that the ISN cannot be used as a classification feature for the GI ISCs. An ISN defines the operation range and many features of a converter derived, while it fails to define the essence of the energy transfer principle. Moreover, the number of ISNs is rising constantly. For example, after a review of ISNs presented in [23], numerous new types were proposed: sigma-Z-source network [26], a whole new family of magnetically coupled ISNs [27], split-source inverter concept [28], L-Z-source network [29], Z-source networks with switched Z-impedance [30]. In addition, a new class of active ISNs which contain controlled switch(es) was introduced recently in order to achieve higher efficiency, lower component count, and improved voltage step-up performance [31]-[36]. Moreover, almost any ISN can be modified further using different available techniques. The most popular are implementation of switched-inductor and switched-capacitor cells [3], [4], [37], or different voltage lift techniques available [38]. Both of those techniques can improve voltage step-up performance of a ISN considerably. Many of the ISNs feature discontinuous input current, which limits their application in high power or renewable energy systems. The input current shape of an ISNs can be improved when the LC- or the C- filter is utilized [39]-[44]. Hence, the type of the ISN cannot be used as the major classification feature because of the high flexibility of this term and numerous types of ISNs reported.

Typically, a GI converter contains a magnetic component that provides galvanic isolation and performs energy transfer from the input to the output side [PAPER-I]. There are only two basic types of magnetically coupled components used in power electronics: transformers and coupled inductors. It means that only three types of GI converters can be identified theoretically based on the energy transfer principle: transformer-based, coupled-inductor-based, and with combined energy transfer when both types of magnetic components are utilized [PAPER-I]. Hence, the first level in the classification can be based on the energy transfer principle. This classification feature is also advantageous over the type of the switching stage since it provides fewer classes, simplifying the

hierarchical structure. Moreover, some switching stages, like the single-switch switching stage, are applicable for any type of energy transfer within the IS converters reviewed in [PAPER-I]. At the same time, it is impossible to apply each energy conversion type to any type of a switching stage.

The classification (Figure 1.5) proposed by the author in [PAPER-I] is based on the operation mode of the magnetic component(s) that transfer(s) energy from the input to the output side. However, it is required to define the transformer and the coupled inductor properly in order to devise a clear classification. Author proposes to use a well-established approach when a magnetic component with two or more windings is considered as a transformer which features zero average flux in the core. A sketch of transformer voltage and typical wave shapes of a flux is shown in Figure 2.1*a* for real transformer, where magnetizing inductance cannot be omitted. In the given case, the core flux is changing linearly during energy transfer with a slope proportional to the voltage and inversely proportional to the transformer magnetizing inductance. Voltage pulses could be asymmetrical as long as volt-second balance and zero average flux are maintained.

A magnetic component with several windings can be considered as a coupled inductor if it features non-zero average core flux, as shown in Figure 2.1*b*. Transformers and coupled inductors differ substantially in their amount of energy stored in the core. However, coupled inductors also maintain volt-second balance in a steady state, while the winding voltage shape can be either asymmetrical or symmetrical.

The properties of magnetically coupled elements described above are well known [45]. Transformers and coupled inductors look superficially similar, while they operate in different modes and thus require different design. Transformers are usually more compact than coupled inductors since their core

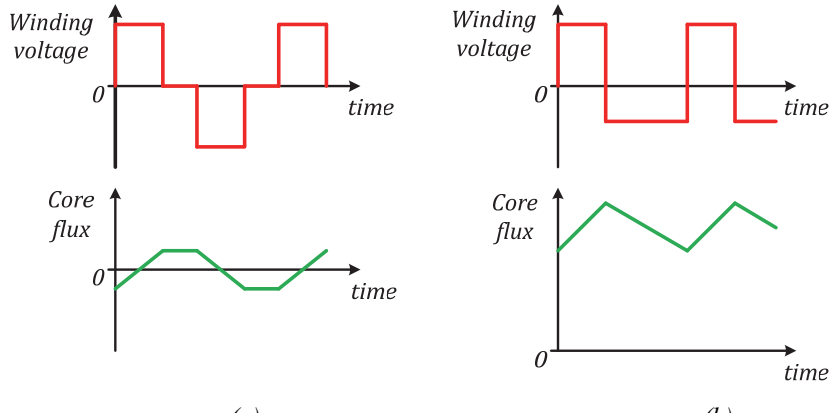


Figure 2.1 Sketches of typical waveshapes of the winding voltage and consequent core flux of: a transformer (a) and a coupled inductor (b) [PAPER-I].

either contains no air gap or a small air gap is introduced deliberately to withstand possible imbalance of the core flux, i.e. voltage during regulation or start-up. Coupled inductors feature a large air gap, which enables high average rated flux. It leads to a larger size of coupled inductors and higher values of the leakage inductances than those of transformers. Both types of magnetic components can be utilized within a converter for energy transfer [46]. The sections following will describe the principles of classification of the GI ISCs based on the type of the magnetic component that transfers energy.

2.2 Fundamentals of the Transformer-Based GI ISCs Class

Development of the transformer-based GI ISCs class by the introduction of the transformer-based ZS GI three-phase full-bridge DC-DC converter was initiated by the Power Electronics Group of Tallinn University of Technology in 2009 [47]. The basic operation principle of the transformer-based GI ISCs is illustrated at high level of abstraction in Figure 2.2. This class of converter topologies was derived from conventional VS and CS counterparts by insertion of an ISN between input terminals and a switching stage instead of a capacitor/inductor. Use is made of typical switching stages: full-bridge, half-bridge, push-pull, etc. Addition of an ISN enables a wide variety of switching states, while some of them are prohibited in VSCs or CSCs. The switching stage employs shoot-through and open states for buck-boost voltage/current regulation using an ISN. A generalized functional scheme shows feedback from the switching stage to the ISN. It means that operating conditions of the ISN depend on the switching control sequence employed by the switching stage. Hence, proper switching sequence enables flexible control of the switching stage input voltage/current parameters. A distinctive feature of this GI ISCs class is the operation of a switching stage: it is connected to the ISN and the transformer. Hence, a switching stage processes all the operating power, which is transferred from the input to the output side during active states.

The transformer-based qZS GI single-phase full-bridge DC-DC converter (Figure 2.3*a*) proposed in [48] is the most extensively studied topology among the GI ISCs [PAPER-I]. Moreover, it is the most typical converter in this class and is thus used to illustrate a general principle. In the given case, the converter is controlled by the symmetrical overlap of active states [49], [50]. Hence, the switching period T consists of two active states (intervals 1 and 3) and two shoot-through states (intervals 2 and 4) of the cumulative duty cycle D_A and

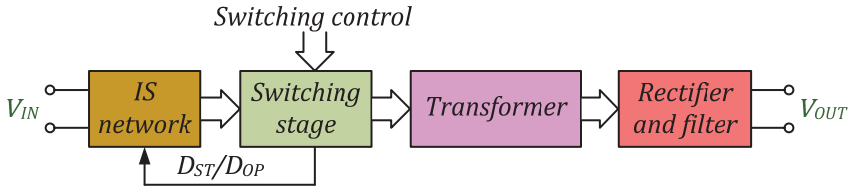


Figure 2.2 Generalized functional scheme of the transformer-based GI ISCs class.

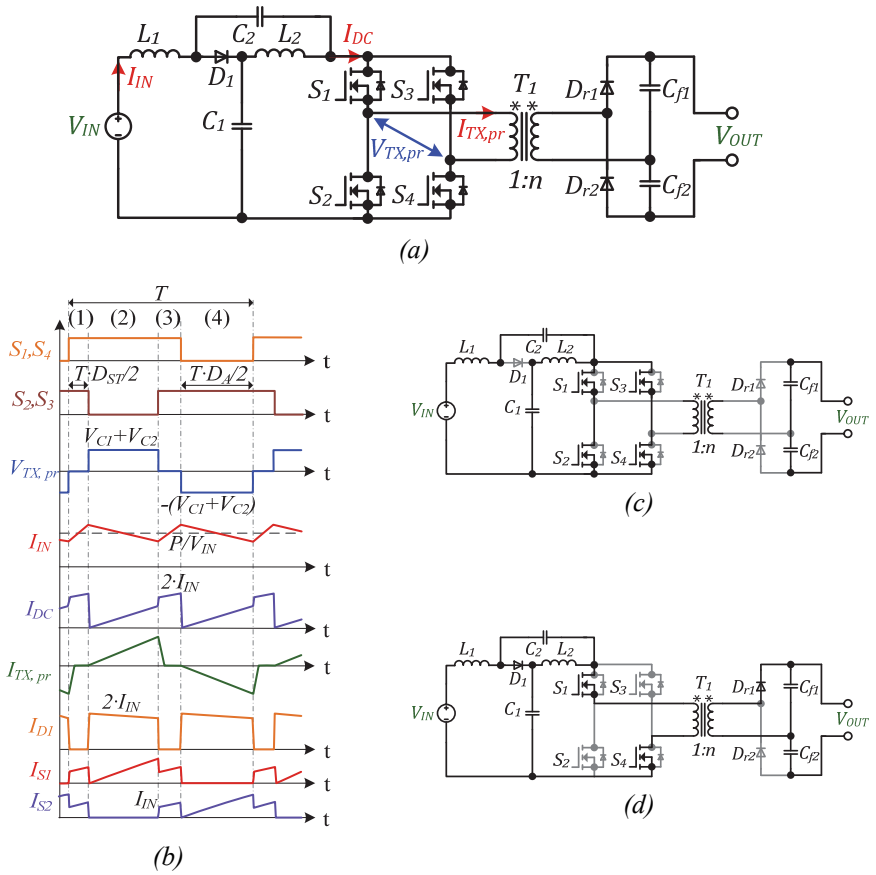


Figure 2.3 Transformer-based qZS GI single-phase full-bridge DC-DC converter [48]: topology (a), sketch of idealized operating waveforms (b), equivalent circuit for the shoot-through state (c), and for the one of active states (d).

D_{ST}, respectively, as shown in Figure 2.3*b*. Equivalent circuits for shoot-through and active states are shown in Figure 2.3*c* and Figure 2.3*d*, accordingly.

During the shoot-through state, energy from the input and the qZS capacitors is stored into the qZS inductors and thus voltage step-up is performed. During the active state, energy is transferred from the qZS inductors and the input terminals to the output side, while the qZS capacitors are charging. Input power P is processed by the qZSN with twofold switching frequency. The rising rate of the transformer current is defined by the leakage inductance. Combination of a step-up transformer with the turns ratio n, a voltage doubler rectifier with constant DC voltage gain that equals two, and symmetrical overlap PWM results in the following DC voltage gain adjustable by the shoot-through duty cycle D_{ST} [48]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n}{1 - 2 \cdot D_{ST}}. \tag{2.1}$$

This converter is based on a single-phase qZS inverter and can be extended to three-phase in order to be able to handle higher powers [48]. All the ISCs derived from the corresponding IS full-bridge inverters have the same structure of the topology and thus can be generalized into a single functional scheme shown in Figure 2.4. More generalized functional schemes can be derived for other types of the GI ISCs classified by the switching stage they employ [PAPER-I]. Those functional schemes do not depend on the type of the ISN and thus can be used as a derivation tool for the GI ISCs that belong to the wide class of transformer-based GI ISCs.

2.3 Fundamentals of the Coupled-Inductor-Based GI ISCs

The first converter from the class of coupled-inductor-based GI ISCs based on the push-pull switching stage was presented in [51]. Its comprehensive analysis for continuous conduction mode (CCM) and discontinuous conduction mode (DCM) was reported in [PAPER-VI]. The operation principle of this GI ISCs class is different from that of the transformer-based class. The basic operation principle of the coupled-inductor-based GI ISC is shown at high level of abstraction in Figure 2.5. It is evident that topologies within this class are simpler than those of transformer-based GI ISCs. Presently, only single-switch and push-pull topologies are known within this class of the GI ISCs. In this type of converters, a switching stage is placed at the output terminals of an ISN and

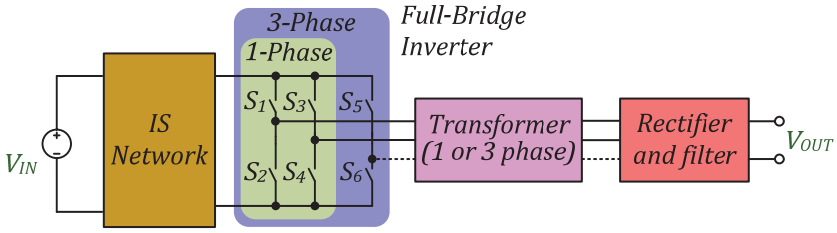


Figure 2.4 Generalized functional scheme of the transformer-based GI ISCs with the full-bridge switching stage [PAPER-I].

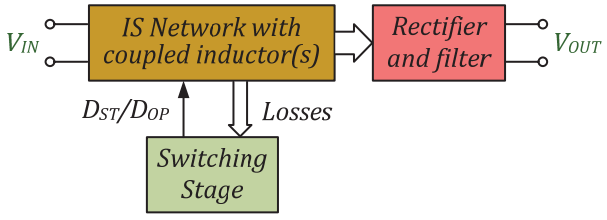


Figure 2.5 Generalized functional scheme of the coupled-inductor-based GI ISCs class.

performs short-circuiting, which results in conditions equivalent to the shoot-through state of the transformer-based GI ISCs. Combining shoot-through and open states of the cumulative duty cycle D_{ST} and D_{OP}, respectively, the switching stage controls the DC voltage gain within an ISN. At the same time, the switching stage consumes a small fraction of the converter power in the form of semiconductor power losses. Another inherent feature of the coupled-inductor-based GI ISCs is the presence of at least one magnetically coupled component within an ISN, which can transfer energy from the input side to the output side, while serving as an inductor within an ISN that stores energy in from of the core magnetic flux. However, output current ripple will be transferred to the input side, increasing current ripple within an ISN.

Coupled-inductor-based GI qZS single-switch DC-DC converter shown in Figure 2.6*a* was first proposed by the author in [PAPER-VIII] and later justified for residential wind turbines in [PAPER-XI]. It is the simplest topology within the class of the coupled-inductor-based GI ISCs. It contains only a single magnetic component T_1, a single switch S_1, two diodes, and four capacitors. Figure 2.6*b* shows a sketch of idealized operating waveforms that explains its operation principle. The switch S_1 short-circuits the qZS network (qZSN) with the duty cycle D_{ST}, while the converter is in the active state during another part of the switching period T. Equivalent circuits for both of the operating states are shown in Figure 2.6*a* and *b*. Operation of the qZSN is similar to that in the transformer-based GI ISCs with difference in currents. The magnetizing current of the coupled inductor T_1, which refers to the input side (I_{LM}), features the same behavior as in the transformer-based converters. At the same time, a tertiary winding with N_{sec} turns is used for energy transfer from the input side to the output side. The energy transfer takes place during the entire switching period.

In the given converter, the leakage inductances of the coupled inductor T_1 define the current slope in the tertiary winding [PAPER-VIII]. The ratio of the output winding current slopes for the shoot-through and active states depends on the shoot-through state duty cycle D_{ST} due to the volt-second balance. This topology is rather simple and intended for low power applications. The converter features relatively high input current ripple and thus could be paralleled in order to minimize the input current ripple [5]. Moreover, this topology has two times lower DC voltage gain than the transformer-based full-bridge GI ISCs [PAPER-VIII]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{n}{1 - 2 \cdot D_{ST}}. \tag{2.2}$$

There are few coupled-inductor-based single-switch GI ISCs available. Their main operation principle does not depend on the type of the ISN and thus can be generalized into a single functional scheme shown in Figure 2.7. Further derivations of similar ISCs can be performed by applying different types of ISNs to that generalized functional scheme [PAPER-I].

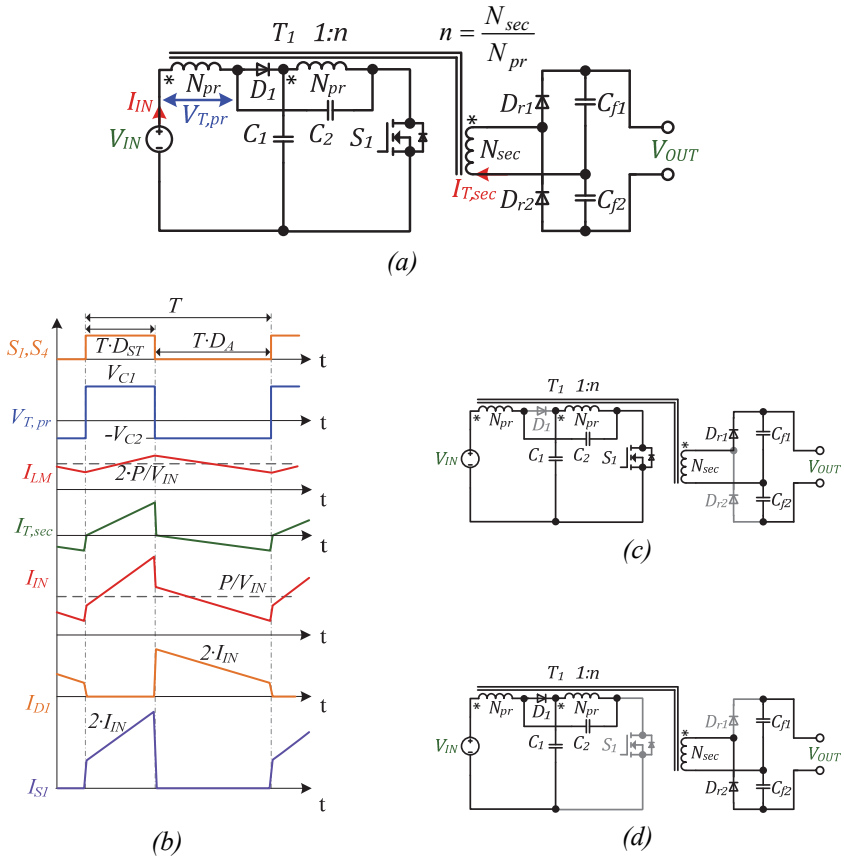


Figure 2.6 Coupled-inductor-based qZS GI single-switch DC-DC converter [PAPER-VIII]: topology (a), sketch of idealized operating waveforms (b), equivalent circuit for the shoot-through state (c), and for the active states (d).

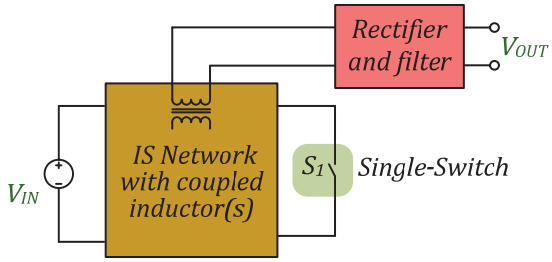


Figure 2.7 Generalized functional scheme of the coupled-inductor-based GI ISCs with a single switch [PAPER-I].

2.4 Classification of Existing Topologies, Recent Development Trends, and Prospective Research Directions

GI ISC topologies were reviewed comprehensively by the author in [PAPER-I]. More than thirty state-of-the-art basic topologies were identified in that paper, while there are many more known GI ISCs. There are topologies not covered by that review, since they are derivatives of the topologies reviewed. Hence, they were considered as topological variations of the main principle and thus omitted. Their derivation from the basic topologies can be connected to paralleling of the basic topologies with magnetic coupling between ISNs or without it [52], [53]. Moreover, basic topologies can be cascaded into a parallel-series electric energy conversion system [PAPER-VII], [10], [54]. The basic topologies can be extended further through an active output stage in order to achieve bidirectional power transfer capabilities [55], [56].

The derived classification of the GI ISCs (Figure 1.5) can be separated into four parts. First, converters without highlight are not related to the author's research and were mostly derived before starting this research or by other research groups. Second, topologies highlighted with orange color were derived and studied by the author and are covered in this thesis. Third, the author has made some contribution to the development of the topologies highlighted in blue, while they were not proposed by him. This contribution is mostly within application related research of particular topologies to identify their advantages in the given case. It is worth mentioning that two topologies were added into this classification after publication of [PAPER-I]. Out of them, an improved YS network was presented recently in [42]-[43], while the qZS push-pull topology with two ISNs presented in [57] is missing in [PAPER-I]. However, the fact that those topologies can be easily adopted by the classification proposed proves its versatility.

The classification of the GI ISCs proposed has a four-level hierarchical structure. The first level is occupied by the main classification feature – type of magnetic component(s) that is (are) used for galvanic isolation and transfers energy from the input to the output side. There are three classes of GI ISCs: transformer-based, coupled-inductor-based, and converters with combined energy transfer. The latter was introduced recently in [PAPER-IV] by the author. The second level of classification is defined by a switching stage utilized in a particular GI ISC. Not all types of switching stages can be applied to all the classes of GI ISCs. Hence, this level of classification follows the type of the magnetically coupled components utilized.

At the second level of classification, topologies have a similar physical structure and thus they can be generalized into basic structures at a low level of abstraction. The half-bridge switching stage has two possible implementations and thus requires two generalized structures to be drawn for symmetrical and asymmetrical implementation of the GI ISCs. Moreover, transformer-based single-phase and three-phase full-bridge converters have the same generalized structure, since the only difference is in the number of phases. They can be extended to multiphase full-bridge GI ISCs as well. [PAPER-I] covers ten

generalized functional schemes that can be used for classification as well as for derivation of new topologies.

The third level of the classification features the type of ISN applied to a particular GI ISC. This level is decoupled from the previous one, since different types of ISNs can be applied to the generalized functional schemes proposed. This is one of the further research directions possible in the field of GI ISCs, since one or two ISNs were applied before to nine out of the ten generalized functional schemes. It is required to study numerous ISCs in order to identify their performance in different applications. For example, magnetically coupled ISNs seem to be of no use in many DC-DC converter applications, while they could be advantageous in applications with very low input voltage as a competitive solution to the GI ISCs with combined energy transfer [PAPER-I].

The fourth level of the classification contains different topological variations of the same energy transfer principle. It is evident that transformer-based single-phase full-bridge GI ISCs are the most advanced group of topologies, mostly due to natural transition of ideas and best practice from the field of IS inverters. Hence, this group features numerous topological variations, mostly related to the implementation of magnetic integration in an ISN, resonant switching, and synchronous rectification.

The classification reveals several obvious directions for the future research in the field of GI ISCs. The first is application of different ISNs to the generalized functional schemes proposed. The second is application of different switching stages [PAPER-I]. For example, the class of GI ISCs with combined energy transfer does not feature any half-bridge topologies and thus this topic requires additional research. The third possibility is derivation of topological variations with improved performance, like in the case of transformer-based single-phase full-bridge GI ISCs. This thesis covers author's research work focused on the derivation of novel GI ISC topologies with simplified switching stages, which is one of the research directions for further development. Moreover, a new class of the converter derived by the author combines transformers and coupled inductors for energy transfer. This area is still offering wide research possibilities, in particular to uncover application ranges and feasibility of numerous ISNs for DC-DC converters.

The field of GI ISCs is relatively new. Thus, the best practice of VS and CS DC-DC converter implementation can be also adopted there. Special attention is usually paid to the improvement of the efficiency and power density. First, implementation of the resonant switching that utilizes parameters of the isolation transformer was proven to be beneficial in the class of the transformer-based GI ISCs [58]. The transformer-based hybrid full-bridge qZS converter with secondary series resonance (SR) studied by the author in [PAPER-IX] has the best input voltage range among known PV module integrated converters. This is a good example of how a combination of ISCs features, best features of existing SR converter control principles with soft-switching in a wide range, and best practice of DC-DC converters implementation results in a superior

application-tailored performance. Synchronous rectification is also one of the common techniques utilized in high efficiency DC-DC converters.

Another promising research direction is to utilize emerging wide bandgap semiconductor materials in power electronic converters. Their performance depends on an application, especially on the switch blocking voltage required. In the switching stages where blocking voltage is higher than 650 V, silicon carbide (SiC) devices have proved a preferable solution [59]-[64] that enables high switching frequency together with high efficiency. Gallium Nitride (GaN) is advantageous over Si counterparts at lower voltages, especially in high frequency converters due to their superior switching performance and low driving losses [65]-[71]. The wide bandgap power semiconductors enable MHz-level switching frequencies and thus impose new requirements on the PCB design [72]. In modern power electronics applications a converter operates with a relatively low voltage (up to 100 V) and power at the input and much higher voltage (usually up to 600 V) at the output side. In this case, full-GaN GI ISCs can reveal all benefits of the topology supported with best-in-class power semiconductor components. The application of SiC devices can be of great interest for high power GI ISCs.

2.5 Summary

This chapter has presented the fundamentals and classification of the state-of-the-art GI ISCs. The classification feature was identified by the author, which resulted in the classification of GI ISCs derived. Classes of transformer-based and coupled-inductor-based GI ISCs were described in general, with brief examples of the most typical topologies. Recent research trends and prospective research directions were identified. Author sees the main conclusions as follows:

- ✦ The GI ISCs can be classified by means of the magnetically coupled component that transfers energy from the input to the output side.
- ✦ The classification proposed is versatile since it can adopt easily new and existing GI ISCs. Moreover, it can be used as a derivation tool for new GI ISC topologies.
- ✦ The GI ISCs family can be extended at higher level through the application of conventional switching stages to one of the three converter classes where those switching stages were not applied before.
- ✦ There is an extremely wide area of research on the GI ISCs connected with the study of feasibility and advantages from the application of a certain ISN out of the rapidly growing number of ISNs.
- ✦ The GI ISCs feature the best qualities of VS and CS DC-DC converters and thus they can benefit from the adoption of the best realization practices of VS and CS converters, which include resonant switching, synchronous rectification, magnetic integration, digital control, etc.
- ✦ Additional research is required in order to assess the application fields that can benefit from the implementation of wide bandgap power semiconductors in the GI ISCs taking into account possible cost penalties.

The main conclusions above describe a limited number of possibilities defined by the author as the most promising in the modern power electronics component market. Some experimental technologies, like PCB embedded magnetics or photonic power electronics, were rejected by the author intentionally because of their poor market availability. Author is targeting a wide industrial acceptance of GI ISCs technology, i.e. solutions to be adopted in industry or those close to industrial approval and thus available off-the-shelf. GaN high electron mobility transistors (HEMTs) are a good example of the latter, since they have become accessible off-the-shelf and are used in the first products available on the market recently. Hence, they can be regarded as a technology that has entered industrial practice.

3 NOVEL TOPOLOGIES AND IMPLEMENTATION CHALLENGES OF GI ISCs

GI ISC topologies known before this research work were limited. Most of them were derived from the corresponding IS inverters and thus belong to the class of the transformer-based GI ISCs. Both VS and CS DC-DC converter families feature topologies with a reduced number of switches, like half-bridge, push-pull, single-ended topologies (flyback), etc. Therefore, focus in this chapter is on the derivation of GI ISCs with a reduced number of switches. The aim is to derive converters competitive in low-power and/or low-voltage applications with the VS and CS counterparts. In some cases, they could provide higher efficiency, power density, and/or low cost of realization.

Further, this chapter describes practical implementation issues of the GI ISCs. The following methods of DC-DC converter improvements were studied: synchronous rectification, application of wide bandgap semiconductors, series-parallel cascading of modules, and resonant switching. These improvements are all widely utilized in industrial VS and CS converters, while benefits from their application to the GI ISCs were unclear before.

3.1 Transformer-Based Topologies with Reduced Number of Switches

It has been of paramount importance to reduce the number of switches in topologies intended for low input voltage and/or power applications, or to minimize the cost of realization [73]. Half-bridge and push-pull switching stages are used widely for transformer-based converters. Half-bridge converters are preferred because of their simple structure [74]-[77]. However, this switching stage has twofold voltage step-down, which is beneficial in applications where the input voltage is higher than the output voltage. Moreover, they are used also in low power step-up DC-DC converters [76]. The operation principle of a push-pull converter is close to that of a full-bridge, while it requires two times fewer switches with two times higher blocking voltage and an additional input side winding within an isolation transformer [78]-[81]. As a result, push-pull converters provide high efficiency in applications with relatively low voltage and high current at the input, where the number of switches within the input current loop influences the converter performance directly. This section describes briefly author's findings regarding the derivation of transformer-based half-bridge, push-pull and single-switch GI ISC topologies presented in [PAPER-II], [PAPER-III], [PAPER-V], [PAPER-VII]. Symmetrical and two types of asymmetrical half-bridge GI ISCs, two types of push-pull GI ISCs, and single-switch GI ISCs are described briefly below in general terms, with examples based on a qZS network selected as a basis for the description of the general operation principles of the GI ISCs.

3.1.1 Symmetrical Half-Bridge GI ISC Topology

Before this research work, no half-bridge GI ISC topologies were available. The half-bridge non-isolated ZS converter was proposed recently in [82] as an electronic ballast for fluorescent lamps. It performs power factor correction (PFC) on the grid side using rectifier diodes as part of the ZS network, while it supplies the lamp with the high-frequency voltage. Another topology of the half-bridge ZS converter was proposed in [83]. It features flexible control of negative and positive magnitudes of the output AC voltage. It suits well for electroplating applications instead of more complicated topologies. Hence, half-bridge ISCs can provide high performance when tailored for an application. There are three transformer-based half-bridge GI ISC topologies proposed by the author. Among them, the symmetrical half-bridge features the simplest derivation and operation principle similar to that of the multilevel IS inverter.

The transformer-based qZS GI symmetrical half-bridge DC-DC converter shown in Figure 3.1 was first presented in [PAPER-III]. It contains two qZSNs connected in a mirror configuration at the neutral node *n*. Switches S_1 and S_2 perform shoot-through in order to step up the input voltage when it varies. The converter is in one of the two active states during the remaining time when the power is transferred from the input to the output side. The input current remains continuous over the entire input voltage range if the qZS inductors are properly dimensioned. The concept of the symmetrical half-bridge GI ISCs was generalized into a functional scheme (Figure 3.2) presented in [PAPER-I]. It is simple to design and control while its performance is limited. It regulates the input voltage only in the boost mode, which limits its application range. Moreover, a high number of passive components imposes realization cost penalties. Nevertheless, this complicated topology with a reduced number of switches can be advantageous in solar PV applications. Neutral node *n* can be used to connect two separated PV modules, which is highly demanded in residential PV installations. Thereby, the regulation range of the converter has to be extended somehow to adopt the wide voltage range of a PV module.

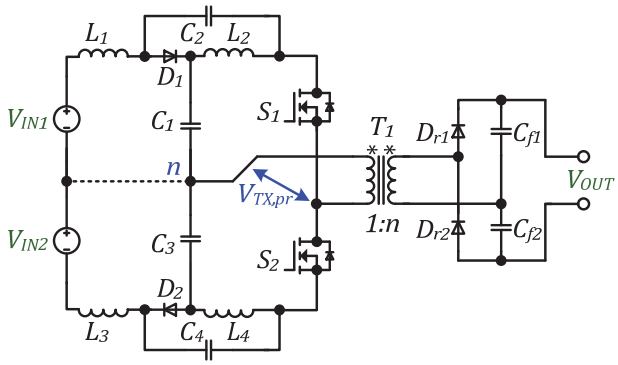


Figure 3.1 Transformer-based qZS GI symmetrical half-bridge DC-DC converter [PAPER-III].

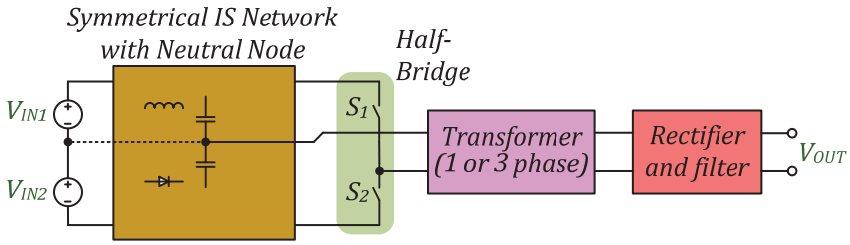


Figure 3.2 Generalized functional scheme of the transformer-based symmetrical half-bridge GI ISCs [PAPER-I].

General principle of the transformer-based symmetrical half-bridge GI ISCs was applied recently to the switched-boost type of active ISNs in [35]. The converter proposed there totally corresponds to the input side of the generalized functional scheme (Figure 3.2), which corroborates the classification proposed by the author in [PAPER-I]. The transformer-based symmetrical half-bridge GI ISCs, as well as most of other simplified topologies, require an isolation transformer with two times higher turns ratio than that of the full-bridge topologies from this class. This results from the two times lower DC voltage gain, similar to that of the coupled-inductor-based converters (Eq. (2.2)) [PAPER-III]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{n}{1 - 2 \cdot D_{ST}}. \tag{3.1}$$

The symmetrical half-bridge GI ISC topology proposed requires further research on advanced control techniques and further topology modification in order to achieve voltage step-down functionality. Subsequently, it can be adopted in residential PV applications, however, the price could be still of a concern.

3.1.2 Asymmetrical Half-Bridge Topologies

Further research of half-bridge GI ISCs was concentrated on the minimization of passive component count. Two concepts of transformer-based asymmetrical half-bridge GI ISCs shown in Figure 3.3 were presented in [PAPER-II]. Both topologies contain a single ISN similar to the full-bridge GI ISCs and provide a reduced number of switches. They were derived from the current-fed half-bridge CSCs through replacing of the input inductor with an ISN (qZSN in the given case). They differ from the symmetrical counterpart not only by the configuration of the ISN but also by the voltage applied to the transformer, which is also asymmetrical.

Both transformer-based asymmetrical half-bridge GI ISCs feature the input voltage step-up in the input stage. It depends on the operating duty cycle of the switch S_2, which performs short-circuiting of the qZSN output terminals, while the switch S_1 is controlled complementary with dead-time [PAPER-II]. Hence, the duty cycle of the switch S_2 is always lower than 0.5, which results in asymmetrical voltage that supplies the isolation transformer. The blocking

capacitor C_b is necessary in order to avoid saturation of the isolation transformer T_1. These simplified asymmetrical half-bridge GI ISC topologies feature the same DC voltage gain and voltage stress of semiconductor components as the much more complicated symmetrical counterpart [PAPER-II]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{n}{1 - 2 \cdot D_2}, \tag{3.2}$$

where D_2 is the duty cycle of the switch S_2.

Derivation of the asymmetrical half-bridge GI ISCs was a quality leap towards simple high-performance transformer-based GI ISCs with a reduced number of switches. The basic topology shown in Figure 3.3*a* was further simplified to minimize the number of passive components, as shown in Figure 3.3*b*. That simplified asymmetrical half-bridge topology contains one capacitor fewer in the switching stage, which, however, results in higher voltage stress of the remaining capacitors. Both concepts of the transformer-based asymmetrical half-bridge GI ISCs can be generalized in the form of a functional scheme with minor variations in the switching stage, as shown in Figure 3.4.

Asymmetrical half-bridge topologies described in this section solve some of the issues of their symmetrical counterpart, e.g. the high number of passive components. However, DC voltage gain is still two times lower than that of the transformer-based full-bridge GI ISCs, which is a usual characteristic of the half-bridge switching stage. Moreover, the additional blocking capacitor with high rated RMS current (in modern low-voltage applications) is required in series with the transformer primary winding, which, however, can be utilized

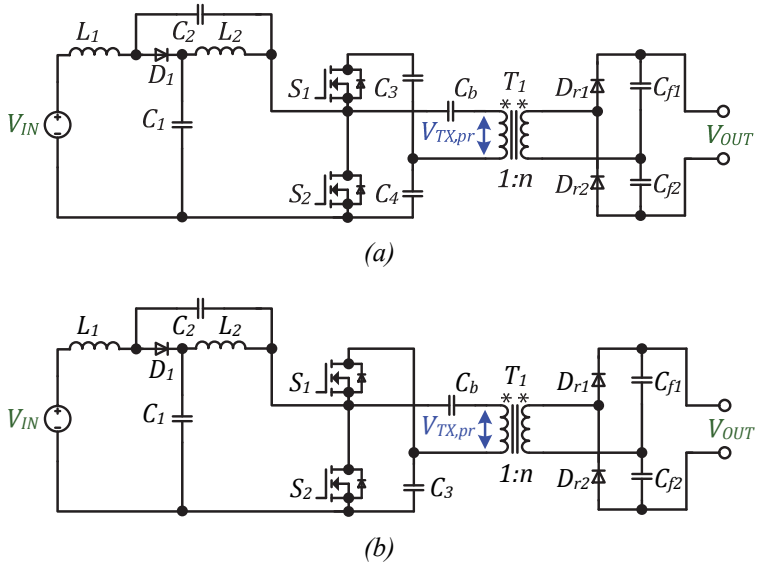


Figure 3.3 Transformer-based qZS GI asymmetrical half-bridge DC-DC converters: with two (a) and a single capacitor (b) in the switching stage [PAPER-II].

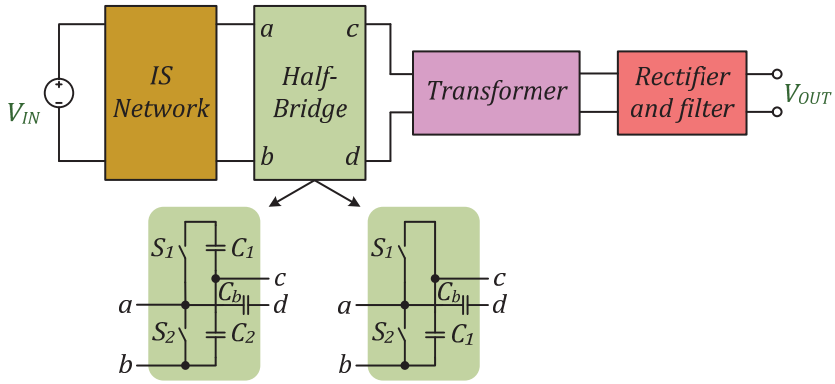


Figure 3.4 Generalized functional scheme of the transformer-based asymmetrical half-bridge GI ISCs [PAPER-I].

for resonant switching. In the author's opinion, application of resonant switching with enhanced control, like constant on-time control in this case, will enable acquisition of all the benefits of the asymmetrical half-bridge converters. However, these topologies have one major drawback inherited from the half-bridge CSCs, i.e. they cannot withstand shoot-through states due to the presence of the DC-link capacitor(s).

3.1.3 Push-Pull Topologies

Two groups of the transformer-based asymmetrical half-bridge GI ISCs were proposed above. However, they require an isolation transformer with an increased turns ratio, which results in undesirably high parasitic elements and either a high number of passive components or a blocking capacitor in series with the transformer primary winding. Hence, half-bridge topologies can be recommended only for low power applications due to their rather limited voltage step-up performance. Another promising solution is to utilize the push-pull switching stage in the transformer-based GI ISCs. It features twofold increase of the voltage stress when compared to the full-bridge counterpart. However, in low-voltage applications with input voltage less than 50 V, this voltage stress causes no severe shortage of efficiency since MOSFETs with very low on-state resistance can be still used. Moreover, push-pull switching stage requires no high-side driving circuits like those in the full-bridge and half-bride switching stages. As a result, the push-pull switching stage can be of a great benefit in applications with relatively low input voltage and high current, especially considering that it features the lowest number of semiconductor components within the input current loop [PAPER-I].

In [PAPER-VII] the author presents a novel group of transformer-based GI ISCs that utilize the push-pull switching stage (Figure 3.5). They were derived from single- and double-inductor GI push-pull CSCs [80]. Both topologies are based on the ISNs with tightly coupled inductors to achieve higher power density. The transformer-based GI push-pull qZS DC-DC converter

(Figure 3.5*a*) provides performance similar to that of its full-bridge counterparts. Reduced number of semiconductor components comes with the price of an additional transformer winding. Moreover, voltage stress of the switches is increased twofold as compared to that of the full-bridge switches, which is an acceptable drawback for low-voltage applications. Voltage step-up depends on the shoot-through duty cycle in the same manner as in the transformer-based full-bridge GI ISCs. Shoot-through is performed by a symmetric overlap of switches' control signals, similar to CS push-pull converters. If the transistors feature similar voltage drop and input windings contains the same number of turns, conditions that appear in the isolation transformer are called "magnetic short-circuit" [84]. During the shoot-through state, both input windings operate with the same voltage compensating each other, which results in a constant magnetic core flux during that time interval, i.e. flux cancellation appears. This topology is able to withstand transformer flux imbalance due to the current limiting nature of the qZSN. Thus, in practice it is not required to have the properties of the switches in complete compliance. Therefore, at balanced operation, the DC voltage gain depends on the switch operating duty cycle D_A as follows [PAPER-VII]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n}{3 - 4 \cdot D_A}, \tag{3.3}$$

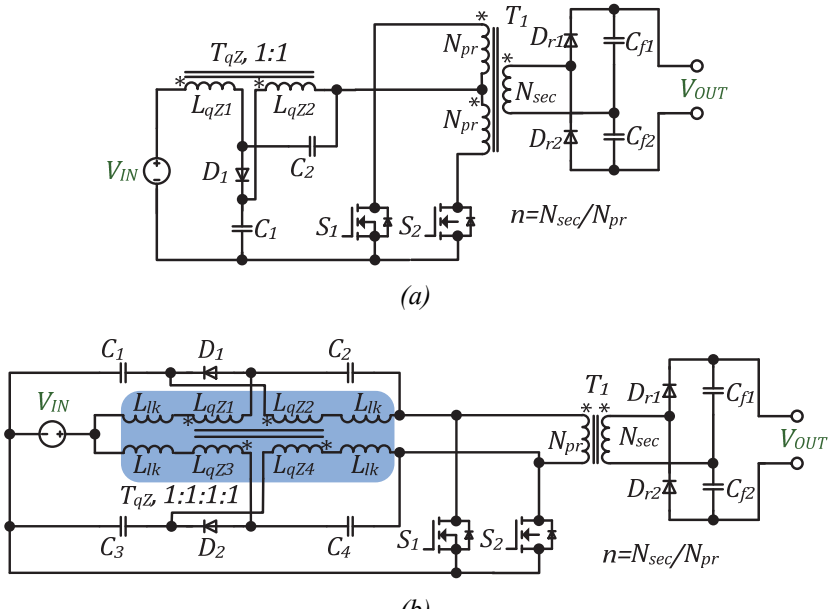


Figure 3.5 Transformer-based qZS GI push-pull DC-DC converters with: ISN that contains a coupled inductor (a) and interleaved with a coupled ISN (b) [PAPER-VII].

where D_A is the duty cycle of the switches S_1 and S_2 that are controlled with interleaving. It means that both of the switches always operate with a duty cycle in the range from 0.5 to 0.75, which results in the converter operation in the boost mode. It is worth mentioning that a similar topology with a non-coupled qZSN was proposed in [84] simultaneously with the author.

The family of the CS push-pull converter contains also a double-inductor topology, which is commonly known as L-type half-bridge (Figure 3.5*b*). Author has derived the transformer-based qZS GI interleaved push-pull topology from the double-inductor CS push-pull converter in [PAPER-VII]. From the CS counterpart, it inherits reduced voltage stress of only two switches, which is equal to that of the corresponding full-bridge GI ISCs. Moreover, this topology can avoid DCM operation, at the same time, careful design of the isolation transformer is required to dimension its magnetizing inductance properly [80]. However, this converter can be also designed with two independent ISNs, as proposed in [57], where a similar approach was published simultaneously with [PAPER-VII].

The DC voltage gain of the interleaved push-pull topology is similar to that of the corresponding bridge topology:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n}{1 - 2 \cdot D_A}. \tag{3.4}$$

In the interleaved qZS push-pull topology proposed by the author (Figure 3.5*b*), an important step towards a minimized double-qZSN was achieved by the use of magnetic coupling of the two qZSNs. The coupled qZSN obtained as a result contains a four-winding coupled inductor with a complicated design illustrated in Figure 3.6. In practice, it can be represented as two gapped two-winding coupled inductors (highlighted in blue color) that contain tight coupling in between. Obviously, the central core branches (highlighted in green) handle the differential flux of those two inductors. Hence, current ripple in the windings of the coupled inductors is reduced considerably

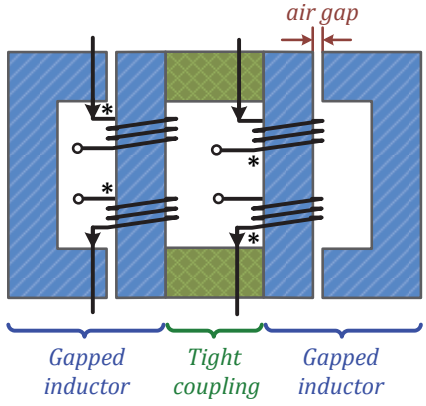


Figure 3.6 Four-winding coupled inductor for an interleaved qZS push-pull converter.

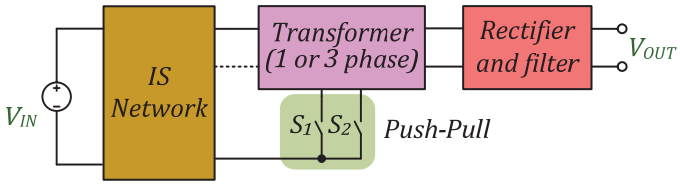


Figure 3.7 Generalized functional scheme of the transformer-based push-pull GI ISCs [PAPER-I].

down to roughly half of the input current ripple if the central core branches feature tight coupling without air gap [10]. This design of a coupled inductor was analyzed in detail for parallel operation of qZS converters in [85], where the operation of the coupled inductor is similar to that in the interleaved qZS push-pull converter, but four magnetic components are used instead of one.

The new class of the transformer-based push-pull GI ISCs was derived in this section. These converters feature higher DC voltage gain than that of their half-bridge counterparts. Hence, these topologies are suitable for low input voltage applications, like battery chargers or interface converters for low power solar PV. Both types of the transformer-based push-pull GI ISCs can be generalized in the form of a functional scheme shown in Figure 3.7 [PAPER-I]. This concept can be further extended to three-phase push-pull switching stage for high power applications. The non-interleaved push-pull topology is simpler to design and thus is more attractive for industrial product use.

3.1.4 Single-Switch Topology

The transformer-based asymmetrical half-bridge was derived from the CS boost half-bridge converter that gained popularity in renewable applications due to its simplicity and high performance [86], [87]. As the half-bridge switching stage is not the simplest one and suffers from shoot-through states, its further reduction to the single-switch in the GI CS DC-DC converters is required to avoid the capacitors that clamp the inductor voltage when the top switch creates necessary current path while supplying the isolation transformer with voltage. Usually, single-switch GI CS DC-DC converters require either additional diodes or transistors in order to shape the input current properly and simultaneously transfer energy to the output side [88], [89]. However, many of ISCs, for example qZSC, not only limit the output current of an ISN, but also stabilize its output voltage and thus require no additional voltage clamping [90]. As a result, the author has concluded that single-switch topologies can be implemented within the class of transformer-based GI ISCs without additional components. Moreover, the author assumes that single-switch topologies will perform at least as well as asymmetrical half-bridge topologies.

The single-switch GI ISCs were proposed by the author in [PAPER-V], where the qZS single-switch topology shown in Figure 3.8 is presented. It was derived from the non-isolated single-switch ISC by adding the isolation transformer with a rectifier in parallel with the switch. As a result, the isolation

transformer is fed with the unipolar high-frequency voltage that equals zero when the switch S_1 performs shoot-through [PAPER-V]. The qZSN feeds the transformer with the voltage ($V_{C1} + V_{C2}$), thus forcing the blocking capacitor C_b to be charged up to the average voltage that equals V_{C2}. Therefore, the output capacitors of the voltage doubler rectifier are asymmetrically charged by the asymmetrical voltage supplied to the isolation transformer. It means that single-switch GI ISCs feature the same operating voltages of the transformer and output capacitors as asymmetrical half-bridge GI ISCs. Hence, it can be concluded that single-switch topologies are a more favorable solution than the corresponding half-bridge counterparts due to a lower number of semiconductor components and consequently, lower losses, price, and auxiliary power used for driving. The DC voltage gain is also similar to that of the half-bridge GI ISCs [PAPER-V]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{n}{1 - 2 \cdot D}, \tag{3.5}$$

where D is the duty cycle of the switch S_1.

Close similarity between asymmetrical half-bridge and the single-switch GI ISCs can be explained by applying another derivation principle to the single-switch topology. It is evident that the single-switch GI ISC (Figure 3.8) can be derived from an asymmetrical half-bridge GI ISC with a single capacitor in the switching stage (Figure 3.3*b*) simply by short circuiting the DC link capacitor C_3 and removing switch S_1 from the circuit, leaving its nets open. It is evident that the operation of the ISN, the isolation transformer, and the voltage doubler rectifier are exactly the same in those two classes of GI ISCs according to the results of [PAPER-II] and [PAPER-V]. Therefore, the single-switch topologies are a better alternative to the half-bridge counterparts and suits well for low power applications, since they have a minimal number of passive components and only a single low-side switch that requires no isolated driving circuit.

The single-switch GI ISCs can be generalized in the form of a functional scheme as any other GI ISC. The functional scheme shown in Figure 3.9 differs from that proposed by the author in [PAPER-I]. The latter did not reveal the essence of the single-switch GI ISCs as clearly as the updated functional scheme shown here does. Apart from low power applications, the transformer-based single-switch GI ISCs can be also recommended for modular solutions,

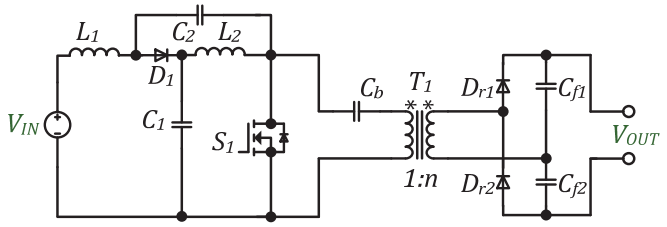


Figure 3.8 Transformer-based qZS GI single-switch DC-DC converter [PAPER-V].

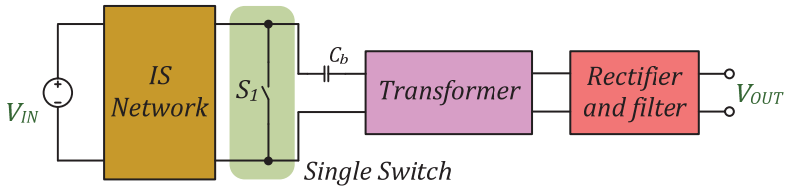


Figure 3.9 Generalized functional scheme of the transformer-based single-switch GI ISCs [PAPER-I].

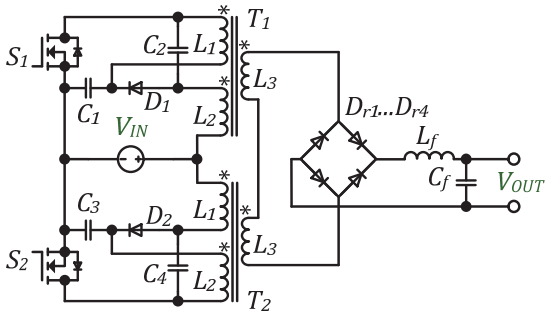
where the rated power of a single cell is usually limited by several hundreds of watts.

3.2 Simple Coupled-Inductor-Based Topologies

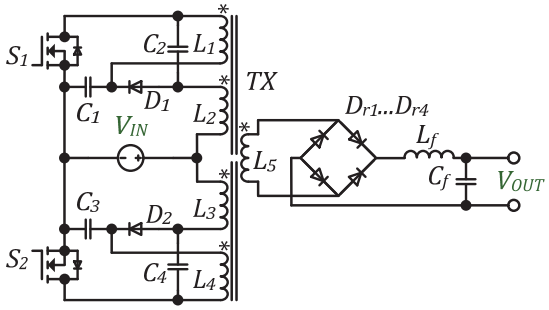
Previous sections discussed author's contribution in the class of the transformer-based GI ISCs that contain discrete magnetic components with dedicated functionality – they are either inductors that store energy or transformers that transfer energy. However, low power applications are known to benefit from simpler topologies where magnetic components combine those functions. For example, a flyback converter stores energy at one part of the switching period and releases it to the load during the remaining time interval. This section describes author's contribution to the class of the coupled-inductor-based GI ISCs. This class of the ISCs along with some facts from the history of its development was reviewed in Section 2.3.

3.2.1 Push-Pull Topologies

As it was mentioned before, the class of the coupled-inductor-based GI ISCs was initiated by the Power Electronics Group of Tallinn University of Technology when the push-pull topology was proposed in [51]. That paper presents two coupled-inductor-based push-pull GI ISC topologies, which are both shown in Figure 3.10. The first topology (Figure 3.10*a*) was not proposed by the author, while author's contribution to this topology is presented in [PAPER-VI], where a detailed analysis is presented for CCM and DCM and corroborated with the experiments. This topology can be represented as two coupled-inductor-based qZ GIS single-switch converters that are connected in parallel at the input side, while secondary side windings are connected in series. The output side windings share the same diode bridge rectifier and LC-filter that feeds the load. Therefore, this topology cannot be treated exactly as an input-parallel-output-series power conversion system composed of two single-switch converters. It features only low-side switches and thus provides low auxiliary power consumption as well as simple control and driving. Conventional interleaved control of switches with the common duty cycle D is used to control the output voltage according to the following expression for the DC voltage gain [PAPER-VI]:



(a)



(b)

Figure 3.10 Coupled-inductor-based qZS GI push-pull DC-DC converters with an ISN that contains two (a) and one (b) coupled inductor [51].

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n \cdot D}{1 - 2 \cdot D}, \tag{3.6}$$

where D is the duty cycle of the switches S_1, S_2 and thus it cannot exceed 0.5.

The topology discussed has shown a good performance in residential wind power systems based on permanent magnet synchronous generators (PMSGs) [8]. Therefore, it can be recommended for applications with a wide input voltage range and relatively high maximum input voltage. It is possible to integrate this push-pull topology further if a complicated magnetic component is applied, as shown in Figure 3.10*b*, where a five-winding coupled inductor is used. The author proposes a magnetic design shown in Figure 3.11 to realize a simplified push-pull topology with the five-winding coupled inductor. Air gaps positions minimize coupling between the two pairs of the primary windings (L_1, L_2 and L_3, L_4), while they have good coupling with the output side winding L_5.

Both push-pull converters can be generalized into the same functional scheme shown in Figure 3.12 [PAPER-I]. This type of coupled-inductor-based GI ISCs was implemented up to the power level of several kilowatts and showed quite high performance. However, the most beneficial power range is several hundred watts, when those converters combine simple structure and high efficiency with a small volume of magnetic components needed. Author's

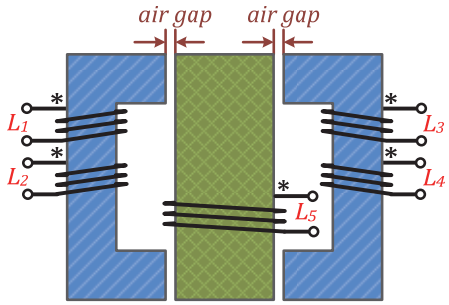


Figure 3.11 Five-winding coupled inductor for the coupled-inductor-based qZS GI push-pull DC-DC converter with a single coupled inductor.

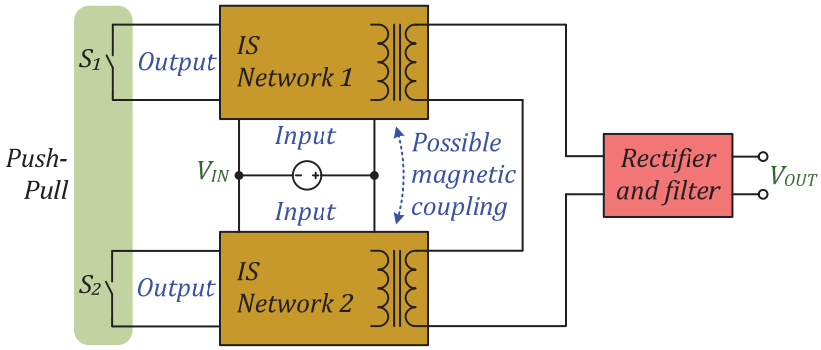


Figure 3.12 Generalized functional scheme of the coupled-inductor-based push-pull GI ISCs [PAPER-I].

contribution here is a comprehensive analysis of converter operating modes presented in [PAPER-VI], while an additional extensive study is needed to define the application range of this concept.

3.2.2 Single-Switch Topology

The simplest topology in the class of single-switch coupled-inductor-based GI ISCs was proposed by the author in [PAPER-VIII] and then studied for DC bus integration of residential PMSG based wind turbines in [PAPER-XI]. Its topology shown in Figure 2.6 was described in Section 2.3 along with its generalized functional scheme (Figure 2.7). It contains only one magnetic component that simultaneously serves as the energy storage element and the isolating element that transfers energy from the input to the output side. This topology features relatively high input current ripple as a result of minimization of magnetic component count. Nevertheless, this topology features DC voltage gain similar to its push-pull counterpart described above [PAPER-VIII]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n \cdot D}{1 - 2 \cdot D}, \tag{3.7}$$

where D is the duty cycle of the switch S_1.

This converter competes with the single-switch converter proposed in [91], where the input inductor is left unchanged and the secondary side is coupled with the second inductor of the qZSN. The latter approach definitely allows lower input current ripple at the cost of an additional magnetic component. In this application, a coupled inductor serves several purposes and thus is treated as an integrated component realized by the use of a single magnetic core. However, it can be realized as a composite component that contains a discrete inductor and a transformer connected in parallel to this inductor, as was proposed in [92]. Therefore, the topology presented in [92] may look like a new transformer-based converter, but it is just a topological variation of the converter presented in [91] and it differs from the latter only by the realization of the coupled inductor. The single switch converter proposed by the author in [PAPER-VIII] is an attractive alternative to topologies presented in [91], [92]. Higher input current ripple can be tolerated by many applications or easily mitigated by an input capacitor if the power level is around a few hundred watts, where such topologies usually prove most beneficial.

3.3 Topologies with Combined Energy Transfer

CSCs contain inductors at the input side, similar to many ISNs. Back in the 1990s, a new concept of input inductor utilization in the GI CSCs was presented: an additional winding can be added to the input side inductor for energy transfer to the output side [93], [94]. Moreover, it can be utilized for soft start-up of a GI CSC, which has always been an issue in many applications [95]. Author proposed to apply this concept to GI ISCs in [PAPER-IV], [PAPER-X]. As a result, a new class of GI ISCs with combined energy transfer was established. These converters feature two ways of energy transfer from the input to the output side: through the isolation transformer and through the coupled inductor placed in an ISN, as shown in Figure 3.13. This generalized functional scheme combines features of schemes shown in Figure 2.2 and Figure 2.5. Hence, additional voltage step-up can be obtained using a coupled inductor added. All known topologies are based on the corresponding transformer-based counterparts and thus feature the same type of the input switching stage. The following sections will describe several types of converters from this class differing by the switching stage used. These converters are rather complicated to design as compared to their main competitors – GI ISCs with magnetically coupled ISN [PAPER-I].

3.3.1 Full-Bridge Topologies

Full-bridge switching stage is most commonly used among different ISCs. The generalized qZS topology from this class shown in Figure 3.14 is quite similar to its transformer-based counterpart, while two additional windings are contained in the input side inductor [PAPER-IV]. At the input side, the coupled inductor T_1 may include both qZSN inductors depending on the application.

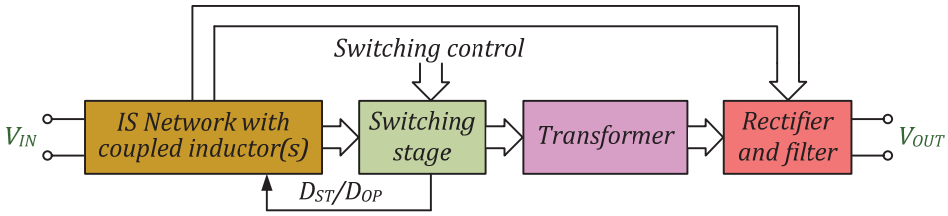


Figure 3.13 Generalized functional scheme of the class of GI ISCs with combined energy transfer.

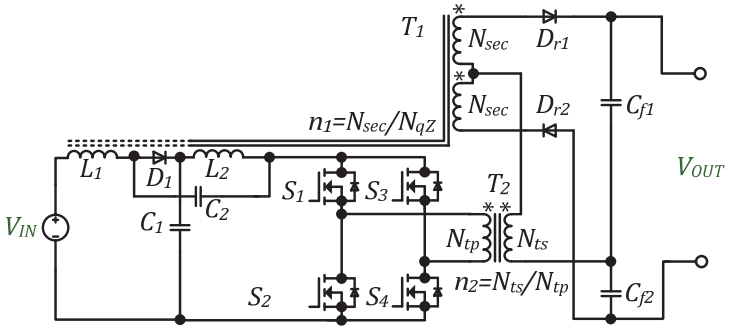


Figure 3.14 qZS GI full-bridge DC-DC converters with combined energy transfer [PAPER-IV].

Full magnetic integration in the qZSN will result in a relatively high input current ripple that can be compensated by an input capacitor, while a discrete qZS inductor used at the input terminals allows a considerable decrease of the input current ripple. Two secondary windings are used in the coupled inductor in order to maintain symmetrical operation of the Voltage doubler rectifier (VDR). Energy transfer through the coupled inductor uses two times higher operating frequency of the qZSN, which results in a possibility to supply the same additional voltage to the output side for both positive and negative half-waves of the isolation transformer T_2. This converter can utilize the same control principle as the corresponding transformer-based ISC due to the synchronized behavior of the coupled inductor and the isolation transformer [PAPER-I]. Finally, DC voltage gain is higher owing to the coupled inductor [PAPER-IV]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot (n_1 \cdot D_{ST} + n_2)}{1 - 2 \cdot D_{ST}}. \tag{3.8}$$

Generalized functional scheme shown in Figure 3.15 is quite similar to that of the corresponding full-bridge converter (Figure 2.4) [PAPER-I]. It is evident that the switching stage transfers energy through the isolation transformer and at the same time, defines the operating mode of the ISN, thus controlling energy transfer through the coupled inductor. In the given case, the construction of the coupled inductor allows the use of the same VDR without any modifications.

3.3.2 Push-Pull Topologies

Push-pull topologies of the GI qZS converter with combined energy transfer (Figure 3.16) derived by the author in [PAPER-IV] are very similar to those with the full-bridge switching stage described above. Here, the push-pull switching stage reproduces the same conditions as the full-bridge while suffering two times higher voltage stress caused by an additional input-side winding [PAPER-IV], [PAPER-V]. These topologies also save the possibility to avoid high current ripple at the input at the cost of a discrete inductor separated from the coupled inductor T_1. Similar to the corresponding transformer-based ISCs, these topologies can be recommended for low voltage applications, or very low voltage if the coupled inductor is properly designed in order to ensure a sufficient increase of the DC voltage gain. The reduced number of switches and the additional input side winding of the isolation transformer T_2 allow the same DC voltage gain to be maintained as that of full-bridge counterparts described above [PAPER-IV]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot (n_1 \cdot D_{ST} + n_2)}{1 - 2 \cdot D_{ST}}. \tag{3.9}$$

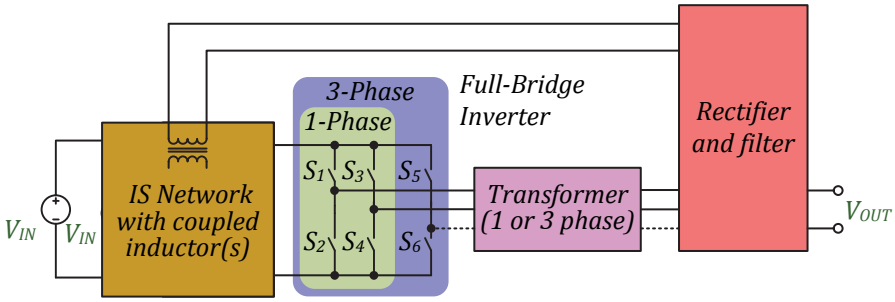


Figure 3.15 Generalized functional scheme of the full-bridge GI ISCs with combined energy transfer [PAPER-I].

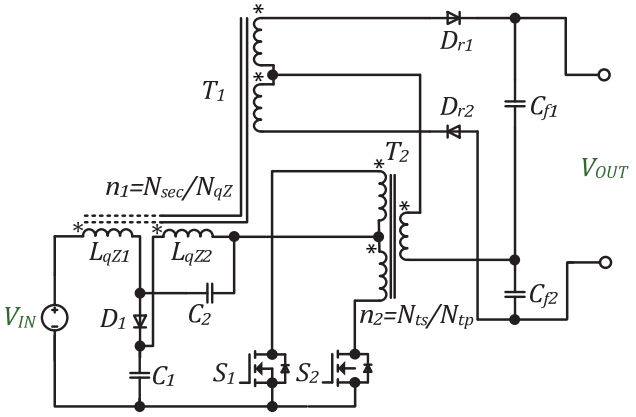


Figure 3.16 qZS GI push-pull DC-DC converters with combined energy transfer [PAPER-IV].

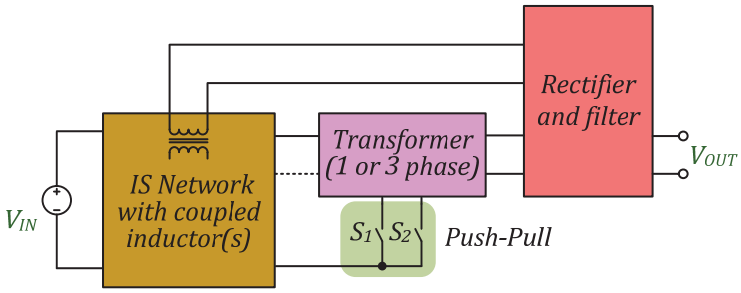


Figure 3.17 Generalized functional scheme of the push-pull GI ISCs with combined energy transfer [PAPER-I].

Topologies of the push-pull GI ISC with combined energy transfer can be generalized in the form of a functional scheme that does not depend on the type of the ISN used, similar to the previous converters [PAPER-I]. The functional scheme shown in Figure 3.17 is quite similar to that of the corresponding transformer-based topologies (Figure 3.7). High DC voltage gain and low number of switches in the input current loop justifies the use of these ISCs in applications with very low input voltage and high input current, where extreme values of the DC voltage gain cannot be satisfied by the isolation transformer solely [PAPER-I].

3.3.3 Single-Switch Topologies

The single-switch qZS GI DC-DC converter (Figure 3.18) was derived as an enhanced topological variation of the transformer-based single-switch DC-DC converter in [PAPER-V]. In this topology, the input winding voltage of the isolation transformer T_2 is equal to that of the coupled inductor input winding. As a result, only one output winding is utilized in the coupled inductor. Here again, the input inductor can be either integrated into the coupled inductor or not depending on the requirements to the input current ripple. In the ideal case, the DC voltage gain of this converter can be calculated as follows [PAPER-V]:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{n_1 + n_2}{1 - 2 \cdot D}, \tag{3.10}$$

where D is the duty cycle of the switch S_1, n_1 is the turns ratio of the coupled inductor T_1, and n_2 is the turns ratio of the isolation transformer T_2.

Evidently, DC voltage gain (Eq. (3.10)) is up to two times lower than that of the full-bridge or push-pull converters from the same class. A generalized functional scheme for single-switch GI ISCs with combined energy transfer shown in Figure 3.19 is quite similar to that shown in Figure 3.9, which can be expected. This topology can be recommended for low-power applications with low input voltage, where the cost of realization can be an important issue [PAPER-IV], [PAPER-V]. The generalized scheme presented in Figure 3.19 differs from that in [PAPER-I] due to the modifications made for clarification, similar to those in Figure 3.9.

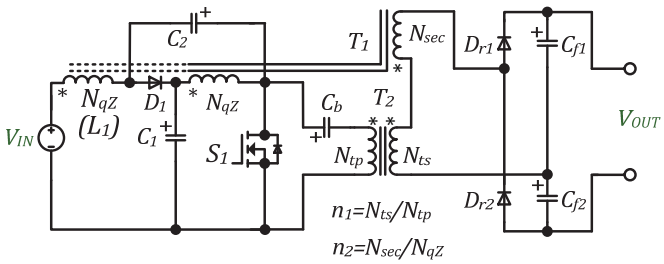


Figure 3.18 qZS GI single-switch DC-DC converters with combined energy transfer [PAPER-IV].

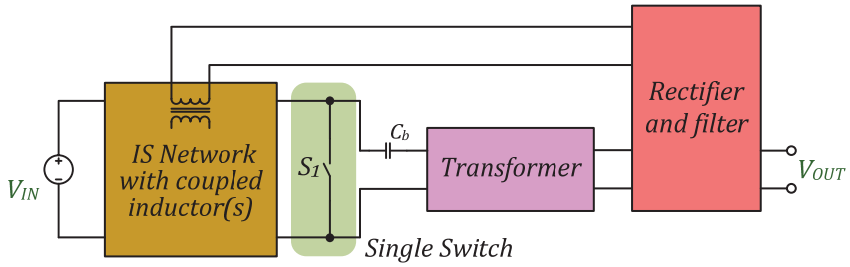


Figure 3.19 Generalized functional scheme of the single-switch GI ISCs with combined energy transfer [PAPER-I].

3.4 Implementation Challenges of GI ISCs

High performance of the GI ISCs can be revealed in real applications only if the best practice from modern DC-DC converters is implemented in design. This section describes the following promising possibilities of performance enhancement studied by the author:

- ✦ selection of the proper rectifier;
- ✦ wide bandgap semiconductors enabling high switching frequency operation;
- ✦ implementation of series-parallel modular power electronic systems;
- ✦ reduction of semiconductor power losses by use of synchronous rectification and resonant switching.

3.4.1 Influence of Rectifier and Filter Topologies on Converter Performance

Author studied the influence of the rectifier topology on the performance of GI ISCs for a wide power and voltage range in [5]. The results showed clearly that half-wave rectifiers can ensure good efficiency and low cost of realization and thus can be recommended for low power applications. However, they provide lower DC voltage gain and can suffer from high voltage stress due to parasitic oscillations during the freewheeling interval. Therefore, they require higher turns ratio of the isolating magnetic component and careful design to

ensure reliability. Bridge rectifiers are usually combined with an *LC*-filter and thus perform averaging of the rectified voltage, which results in a limited range of operation and higher turns ratio of an isolating magnetic component. Voltage multiplier rectifiers show best performance due to an effective combination of the current limiting nature of the ISNs and inductorless realization of the output filter. VDR is the most advantageous among voltage multiplier rectifiers, since it has the lowest conduction losses for many real world applications [9]. Rectifiers with higher gain can be used only in specific applications, where extremely high DC voltage gain cannot be satisfied by the isolating magnetic component solely or when the voltage stress of the rectifier semiconductors is high.

There are two types of VDR: bridge and Greinacher, shown in Figure 3.20*a* and *b*, correspondingly. The bridge type has potentially higher efficiency due to its lower current stress of components. However, the Greinacher VDR can be advantageous in topologies with secondary series resonance, where the capacitor C_1 can be used as a resonant capacitor, while C_2 can be a bulky power decoupling capacitor [PAPER-IX]. At the same time, a bridge VDR requires an additional capacitor for power decoupling and it can provide slightly imbalanced resonant frequencies of the positive and negative half-waves of the transformer current. Usually, the VDR is implemented using SiC Schottky barrier diodes (SBDs) in order to minimize switching losses and thus achieve high switching frequency. The SiC SBDs have relatively high conduction losses that can be justified if high switching is required. Hence, the VDR provides the best performance in most of the voltage step-up applications and is widely used among the existing GI ISCs.

3.4.2 Benefits from Application of Wide Bandgap Semiconductors in High-Voltage High-Frequency IS Converters

Most of the GI ISCs are hard-switching and thus require careful assessment of semiconductor power losses. Today's commonly used switching frequency is 100 kHz and higher, which requires semiconductors with superior characteristics. Silicon Carbide (SiC) and Gallium Nitride (GaN) are the most advanced technologies on the market of wide bandgap (WBG) power semiconductors. Some GI ISC topologies cannot be realized without WBG

Figure 3.20 Voltage doubler rectifiers: bridge type (a) and Greinacher type (b) [5].

semiconductors. For example, an experimental study reported by the author in [7] shows that high voltage (1200 V devices are used) hard-switching GI ISCs with high switching frequency are not feasible without SiC SBDs, since fast Si diodes with soft recovery feature up to ten times higher semiconductor power losses. Utilization of SiC MOSFETs instead of their Si counterparts allows an efficiency improvement of up to 5% in the given case despite 100 kHz switching frequency. Improvements were achieved mostly due to considerably lower conduction losses [7]. GaN devices were not widely utilized in GI ISCs, but they were already justified for IS inverters intended for module level power electronics (MLPE) applications [96]. Experimental efficiency of qZS inverters with GaN switches were reported at the level of 98% at 100 kHz switching frequency. Moreover, it was predicted in the same study that synchronous rectification with a GaN switch can result in a peak efficiency of 99%. It can be concluded that WBG semiconductors can improve the performance of GI ISCs considerably.

3.4.3 Advantages of Synchronous Rectification and Resonant Switching

Synchronous rectification is a popular method to improve efficiency in topologies where a diode is placed at the low voltage side. Authors of [97] predicted an efficiency rise of 2% in GI qZS converters for photovoltaic applications by means of simulations in PSIM software. Experimental verification performed by the author in [6] and [9] proves this statement. However, synchronous rectification within the ISN shows much better performance than that in the output side VDR. Synchronous VDR requires more expensive SiC MOSFETs for better performance, while additional switching losses and driving power almost diminish benefits of synchronous rectifications. Hence, utilization of the synchronous qZSN is compulsory if high efficiency is of a concern, while the synchronous VDR does not provide sufficient efficiency rise to justify additional costs of SiC MOSFETs and their driving circuits. Moreover, the synchronous rectification has yet another substantial benefit that is not connected to the efficiency improvement. The ISCs are known for their dangerously high DC voltage gain when they reach DCM [98], [99]. However, the synchronous switch creates a path for the inductor negative current flow and thus forces the ISN to operate similar to CCM; even the inductor current(s) has negative values before the shoot-through mode is started [100].

Resonant switching is another popular approach for efficiency improvement that allows switching losses reduction. This method suits well for the transformer-based class of GI ISCs. Author did not implement resonant switching in the GI ISCs that was first performed in [58]. Author's contribution is in practical design guidelines formulated in [PAPER-IX]. First, it is more reasonable to integrate a resonant inductor in the isolation transformer in order to minimize parasitic oscillations and conduction losses. Second, it is more reasonable to place a resonant tank at the high voltage side in order to minimize conduction losses in resonant capacitor(s). Third, capacitors of the bridge VDR

can be used as resonant capacitors, while the resonant frequency will not be influenced by the bulky output power decoupling capacitor. Those recommendations together with the synchronous rectification in the qZSN are used for the PV module integrated converter based on the hybrid series-resonant transformer-based full-bridge GI qZS DC-DC presented in [PAPER-IX] and thus can achieve superior performance.

3.4.4 Parallel-Series Modular Systems

Modular power electronic systems usually contain several basic cell modules connected in parallel-series configuration. The GI ISCs can also benefit from such advantages of those systems as (N+1) redundancy, easy scalability, simple thermal design, improved DC voltage gain, reduced manufacturing cost, etc. [PAPER-VIII]. Earlier, input-series-output-parallel connection of the qZS GI DC-DC converters was tested in [54]. Author's attention was concentrated on the input-parallel-output-series (IPOS) connection of the GI ISCs, since this configuration suits better for modern applications, like renewable and alternative energy systems, or battery energy storages [PAPER-I]. In those systems, easy scalability and redundancy is of high importance. Moreover, such connections allow lower DC voltage gain requirements from a single module and consequently increase total energy conversion efficiency, since critical operating points with extreme duty cycles are avoided. On the other hand, alleviated requirements imposed on the converter DC voltage gain range enable the use of simple topologies like those with a single switch. A simulation study performed by the author in [10] shows that two low-cost transformer-based GI qZS single-switch DC-DC converters connected in the IPOS configuration can achieve performance close to that of the full-bridge counterpart in the boost mode with the same turns ratio of the isolation transformer [PAPER-I], [PAPER-VIII]. Hence, IPOS systems can be regarded as an emergent trend in the field of GI ISCs that requires further research to identify their advantages in different modern applications.

3.5 Summary

This chapter described new topologies of the GI ISCs and their implementation challenges. It has covered mostly the contribution of the author to the field of the GI ISCs through the synthesis of new topologies and their analysis. Major conclusions from this chapter are as follows.

✦ The transformer-based symmetrical half-bridge GI ISCs can provide good performance in a limited number of applications due to the high number of passive components. However, it seems to be a promising solution for dual PV module integration, which requires further experimental verification.

✦ The transformer-based asymmetrical half-bridge GI ISCs provide the same functionality as the corresponding single-switch topology while contain twice as many switches and can be damaged by the shoot-through states. Therefore, the transformer-based single-switch GI ISCs will dominate over the asymmetrical half-bridge topologies in most of the applications. On the other hand, the half-bridge topologies can be advantageous in designs where converter parasitic inductances cannot be minimized and thus inherent voltage clamping capabilities of the half-bridge will be a substantial benefit.

✦ The DC voltage gain of the transformer-based half-bridge and single-switch GI ISCs is twice lower than that of the corresponding full-bridge topologies.

✦ The transformer-based push-pull converters can provide a low number of switches in the input current loop and keep the DC voltage gain equal to the of the corresponding full-bridge topologies. However, this approach has several drawbacks against the full-bridge GI ISCs, like increased VA rating of the isolation transformer and twice higher voltage stress of the switches, or utilization of complicated double ISN with magnetic coupling that allow the voltage stress to be the same as in the corresponding full-bridge converters without influencing the DC voltage gain.

✦ The coupled-inductor-based topologies are a low cost alternative to the transformer-based converters that can be utilized in low power systems, while the design of their magnetic components can be a complicated task due to hybrid functionality.

✦ The combined energy transfer is easily achieved if a GI ISC contains both the isolation transformer and coupled inductors. This concept is based on the corresponding transformer-based converters and thus utilizes the same switching stages. However, only the single-switch topologies with combined energy transfer seem to be attractive due to simpler realization.

✦ In order to achieve the best performance, if feasible, the following realization methods should be applied to the GI ISCs: synchronous rectification in the ISN, resonant switching, cascading for high voltage step-up, and utilization of the WBG semiconductors.

4 APPLICATION-ORIENTED DESIGN OF GI ISCs

4.1 Emergent Power Electronics Applications in Low Power Residential and Small Commercial Energy Systems

The Europe's 20-20-20 goals (energy efficiency increase by 20%, reduction of CO_2 emissions by 20%, and 20% renewables by 2020) require significant re-configuration of the European electricity grid, which would transform it to a "Smart Grid". That would involve major changes both in the high-power grid infrastructure and in the consumer energy management areas.

In accordance with the Energy Performance of Buildings Directive, all new buildings commissioned must be nearly zero energy buildings after December 2020 (2018 for public buildings). The concept of nearly zero energy (Figure 4.1) requests the building to possess a superior energy performance: very low (or zero) amount of energy consumed should be generated mainly by the renewable sources, including the ones located on-site or nearby [101]. The energy consumed should cover the typical needs associated with the building: heating, cooling, hot water, lighting, appliances and other needs. The energy sources considered renewable are: hydro, geothermal, solar, tide (wave), wind, biomass, and heat pumps.

A number of various concepts and examples for both public and residential nearly zero energy buildings exist, such as EnergyFlexHouse©, Primary School Hohen Neuendorf, ValaGard©, Minergie©-A, etc. In total, there are more than 300 existing buildings that claim to feature the nearly zero energy concept.

The availability of renewable energy sources varies significantly from region to region, e.g. in the Northern European market, heat pumps and biomass technologies prevail, while in Southern Europe, solar thermal systems promise highest potential. Besides, the actual performance of the systems could vary significantly throughout the year. Buildings that rely only on PV for energy generation could have excess of energy in summer and high demand during the winter. On the other hand, buildings that have PV combined with other units, like heat and power (CHP), wind turbine, or fuel cell (Japan's ENE-FARM program) would have a more continuous generation and consequently better match of supply and demand. This, however, may not be cost-effective over the expected lifecycle. The widespread introduction of described innovations will help the EU countries to meet the 2020 targets for CO_2 reduction.

Additionally, increased number of energy generating points would potentially allow increased energy supply security, since it will reduce dependency on a single power generating facility or power line. At the same time, energy generation from a high number of systems will significantly complicate energy system management and require new approaches to be developed that would ensure an optimal use of the energy available. One of the key components of such systems are power electronic converters, which interface parts of the energy system and possess the energy between them.

An example of the next generation residential system with DC-coupling is presented in Figure 4.2. Individual converters in such power electronic systems are usually low power (up to 2 kW) and have to correspond to a large number of requirements, including high reliability, efficiency, functionality, electromagnetic compatibility (EMC), etc. At the same time, these emerging applications open wide possibilities for development and spread of power electronic systems and impose various challenges for the designers in order to obtain highest possible benefits from these new technologies.

Among potential solutions, topologies featuring ISNs are the promising candidates as interface converters for renewable energy applications. They fit exceptionally well to the nature of such applications (PV, PMSG, fuel cell), which results in a significant variation of voltage and power generated. Galvanic isolation requirement could be easily fulfilled, as most qZS-based topologies utilize a transformer or a coupled inductor for energy transfer. In addition, qZS-based converters have continuous input current, which is highly desirable, as it affects positively the long-term reliability and lifetime of RES. All experimental studies in this thesis were performed with the qZS converter due to its continuous input current and inherent DC-rail voltage clamping [90].

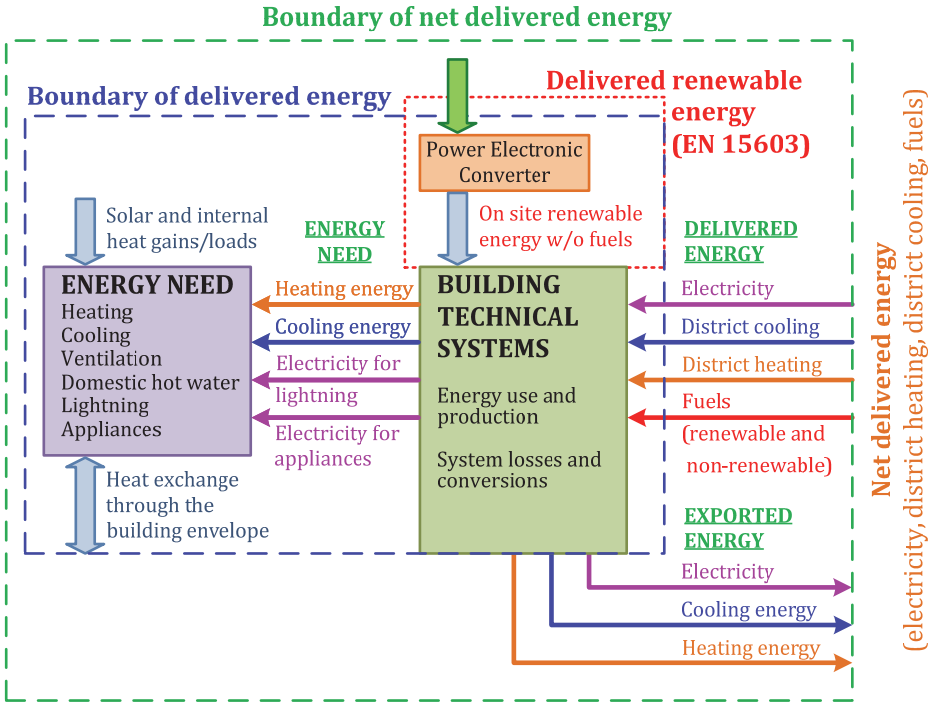
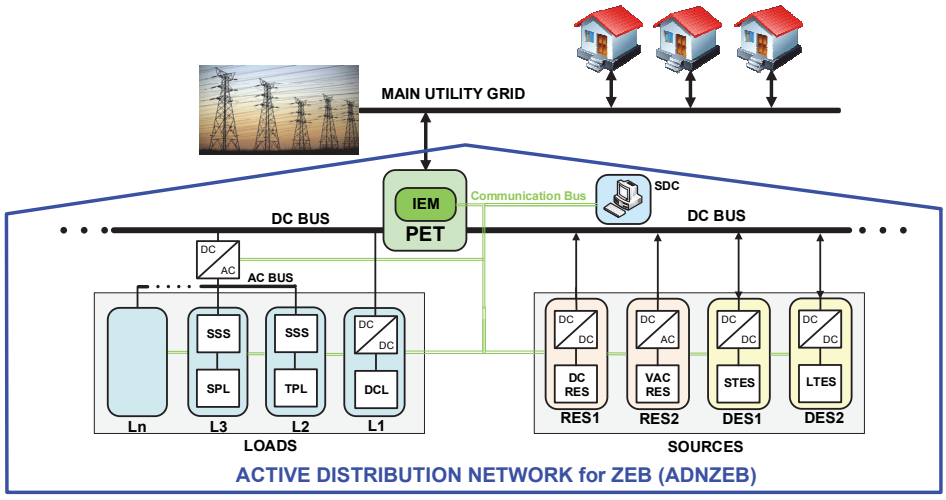


Figure 4.1 Concept of net zero energy buildings and small communities [102].



PET – Power electronic transformer (*solid-state* or *intelligent transformer*)
IEM – Intelligent energy management
SDC – Supervision and diagnostics center
SSS – Solid-state switch
RES – Renewable energy source
DES – Distributed energy storage
DCR – DC RES (photovoltaics, fuel cells)

VACR – Variable AC RES (wind turbine, hydro)
STES – Short-term energy storage (batteries, supercapacitors, flywheels)
LTES – Long-term energy storage (hydrogen buffer)
L – Load
SPL – Single-phase loads
TPL – Three-phase loads
DCL – DC loads

Figure 4.2 Next generation active distribution network of the zero energy buildings.

4.2 Quasi-Z-Source Based Microconverter – A New Photovoltaic Module Level Power Electronic Interface

Module Level Power Electronics (MLPE) is one of the promising topics in the area of PV applications. The main purpose of MLPE is to achieve operation of every individual PV module in the Maximum Power Point (MPP) to ensure the highest possible energy yield despite shaded conditions and other challenges of residential applications. It can be achieved by means of buck-boost control.

The focus of the application is PV modules connected in parallel, where each module is equipped with an integrated converter (MIC). Outputs of each MIC are connected in parallel to the common DC bus of the PV power system. MIC should preferably be a self-powered, high efficiency isolated step-up DC-DC converter with autonomous control for tracking the MPP locally. Considering these aspects, the GI quasi-Z-source series resonant DC-DC converter (qZSSRC) is presented as a candidate topology for PV MLPE applications (Figure 4.3) [PAPER-IX]. This converter is based on a topology presented in Figure 2.3 and consists of a qZSN (L_1, L_2, C_1, C_2, S_{qZS}), full-bridge inverter ($S_1 \ldots S_4$), step-up isolation transformer TX and VDR (D_{r1}, D_{r2}, C_{f1}, C_{f2}). At its secondary side, the converter has a series resonant tank formed by the leakage inductance of the isolation transformer and the VDR capacitors. The output capacitance C_f is used for the output voltage filtering.

As was shown, some modifications were introduced to the original topology [11] for performance improvement. Firstly, synchronous MOSFET was

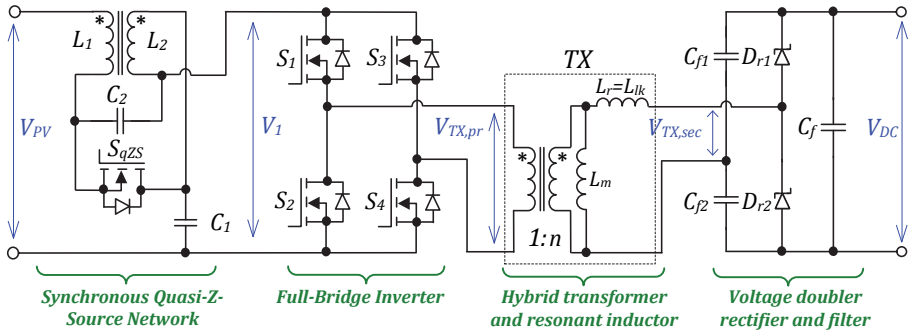


Figure 4.3 Galvanically isolated series resonant full-bridge quasi-Z-source DC-DC converter (qZSSRC) topology.

introduced in the qZSN to reduce conduction losses. Secondly, the discrete inductors in the qZSN were replaced by a coupled inductor for higher power density and for further reduction of the input current ripple. Thirdly, the proposed converter contains an integrated series resonant tank at the secondary side formed by capacitors C_{f1}, C_{f2} and leakage inductance of the isolation transformer referred to the secondary winding L_{lk}.

The MIC uses a multi-mode operation to optimize performance under various operating conditions [11], [PAPER-IX]. The qZSSRC can combine basic phase-shift modulation (PSM) and shoot-through PWM for buck and boost operating modes, respectively. In the boundary between these modes, the converter operates in a normal mode as a series resonant converter (SRC) at its resonant frequency [11]. Idealized control variables of the proposed qZSSRC operating within the input voltage range from 0.5·to 1.5 $V_{PV(MPP)}$ (panel output voltage at MPP) reported in [PAPER-IX] are shown in Figure 4.4. The normal mode corresponds to the MPP of the PV module at the most common operating conditions [11]. In this mode, the duty cycle of the inverter switches is close to 0.5, the switch S_{qZS} is always conducting and the qZSSRC operates identical to the traditional SRC at the resonant frequency [11], [PAPER-IX].

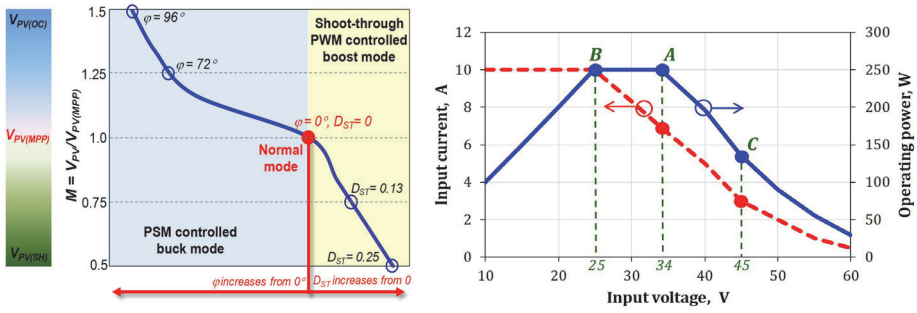


Figure 4.4 Operating modes with ideal control variables (a) and load profile of the qZSSRC (b) [PAPER-IX].

If the input voltage is higher than nominal, the converter starts operation in the buck mode [11]. In this mode, the qZSSRC could be treated as the SRC operating at the resonant frequency with the PSM control, where the output voltage is controlled by the phase shift angle φ between the inverter legs [11].

If the input voltage is lower than the nominal, the converter operates in the boost mode, similar to the traditional qZS converter [11], [48]. The output voltage is controlled by the shoot-through state duration, when all the switches of the inverter bridge are turned on simultaneously. The switching frequency of the qZSSRC in the boost mode is fixed to the resonant frequency.

For the experimental verification of the concept, the prototype of the MIC based on the qZSSRC topology has been developed (Figure 4.5). General specifications of the prototype are: input voltage 10-60 VDC (34 V nominal), output voltage 400 VDC, switching frequency 110 kHz, operating power 25-300 W. The components used were: Infineon BSC035N10NS5 (S_1...S_4, S_{qZS}), CREE C3D02060E (D_{r1}, D_{r2}), microcontroller ST STM32F334, $L_1 = L_2 = 22$ µH, $C_1 = C_2 = 26.4$ µF, $C_{f1} = C_{f2} = 43$ nF, $C_f = 100$ µF, $L_{lk} = 24$ µH, $L_m = 1$ mH, $n = 6$ [PAPER-IX]. The prototype was designed to operate with the power profile shown in Figure 4.4*b*, to represent the operation conditions of the MLPE converters powered by the 60-cell PV modules [11].

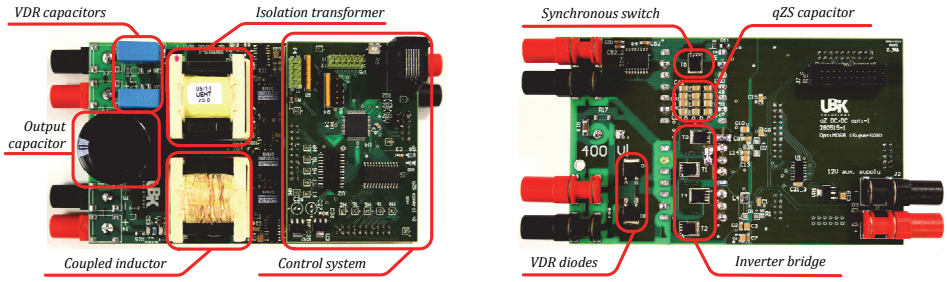


Figure 4.5 Top (a) and bottom (b) views of the 300 W MIC prototype of the qZSSRC [PAPER-IX].

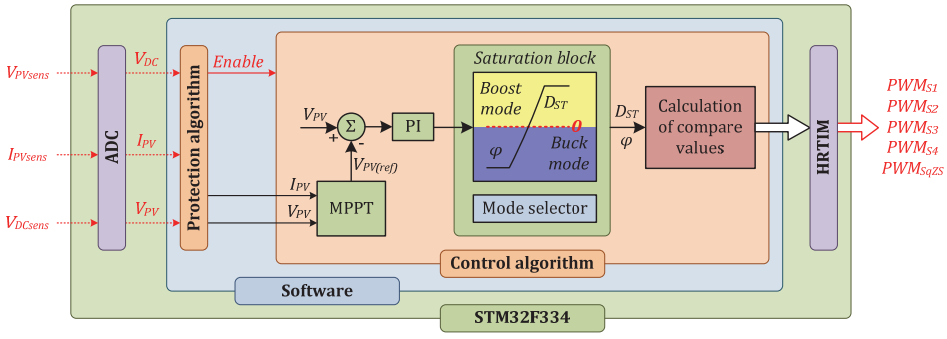


Figure 4.6 Block diagram of the control system developed for the qZSSRC converter [PAPER-IX].

Figure 4.6 presents a simplified block diagram of the developed MIC control system. MPP tracking algorithm calculates the reference input voltage V_{PV}. Error between the reference and measured input voltages is sent to the PI controller. Saturation block featuring the mode selector provides smooth transition between various operating modes. Positive values of the PI controller output determine the shoot-through duty cycle, while negative ones determine the phase shift angle. They define the compare values of the high resolution timer (HRTIM), which generates control signals for the converter transistors.

The control system proposed is relatively simple, as it does not control the output DC-link voltage. It is assumed that distributed generation applications have the DC-link voltage maintained by the inverter, energy storage or another power consuming system connected to the output terminals of the converter. Therefore, the experimental analysis was performed with the electronic DC load operating in the constant voltage mode. If the DC-link voltage level exceeds the defined limits, the protection algorithm will stop operation of the MIC.

The experimentally obtained variables of the qZSSRC converter for different input voltage V_{PV} levels are shown in Figure 4.7 and the experimental efficiency curves corresponding to the PV test profile (Figure 4.4*b*) are presented in Figure 4.8. The peak efficiency of 97.4% was achieved at the nominal input voltage when the converter was operating in the normal mode [PAPER-IX]. When the input voltage was lower than 34 V, the converter operated in the boost mode. The efficiency dropped to 87% at the maximum voltage step-up when the input voltage $V_{PV} = 10$ V (input power of 100 W). According to Figure 4.7, the shoot-through duty cycle in this operating point has the value of 0.41 and the converter reaches the maximum DC voltage gain of 40.

At low loads (according to the profile in Figure 4.4*b*), the converter has a considerable efficiency drop. To improve the performance, cycle skipping modulation was introduced. By optimizing the number of skipped cycles, up to 10 % efficiency improvement was achieved at low operating power, as shown in Figure 4.9 for the normal and the buck modes. Moreover, DCM with

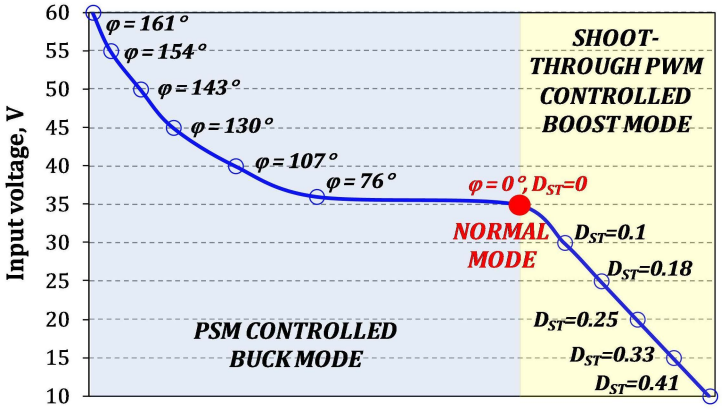


Figure 4.7 Experimental control variables of the qZSSRC converter [PAPER-IX].

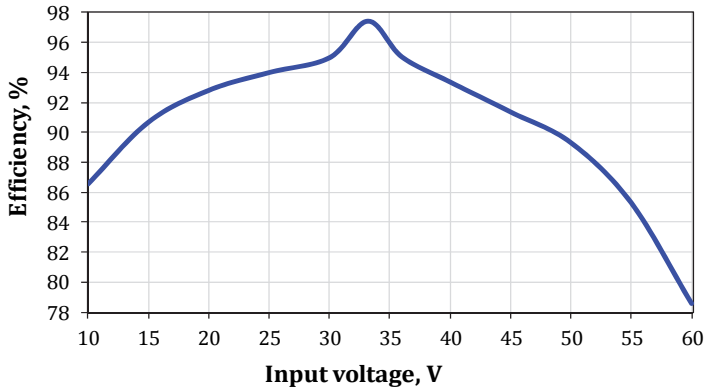


Figure 4.8 Experimental efficiency of the converter qZSSRC according to the power profile from Figure 4.4 [PAPER-IX].

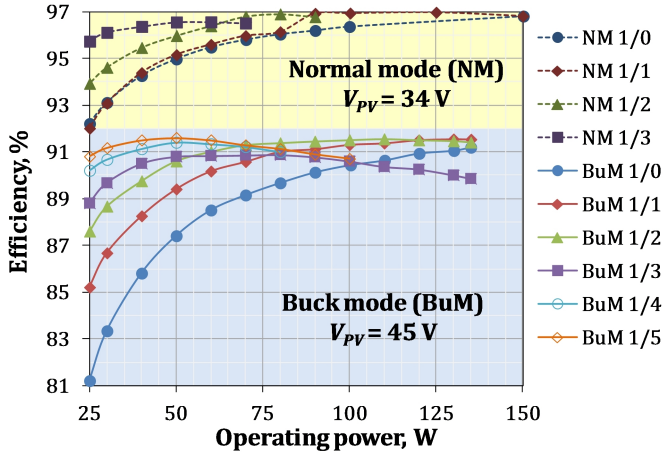


Figure 4.9 Light-load efficiency of the qZSSRC for different cycle-skipping modulation parameters (1/0 - no cycle skipping, 1/1 - one applied and one skipped, etc.) [PAPER-IX].

dangerously high voltage step-up can be avoided at light load if the synchronous ISN is utilized [100].

4.3 Low Cost Quasi-Z-Source Photovoltaic Module Integrated Converter Based on the GI Single-Switch qZS Converter

The previous section described a high performance PV MIC converter. To reduce the cost of realization while sacrificing a wide input voltage range, the author proposed a simplification of the full-bridge MIC in [PAPER-X] to the single-switch topology shown in Figure 4.10. From here on, this simplified MIC will be regarded as a single-switch MIC, despite the presence of two switches, since the switch *S* defines the operating state. It is based on the transformer-

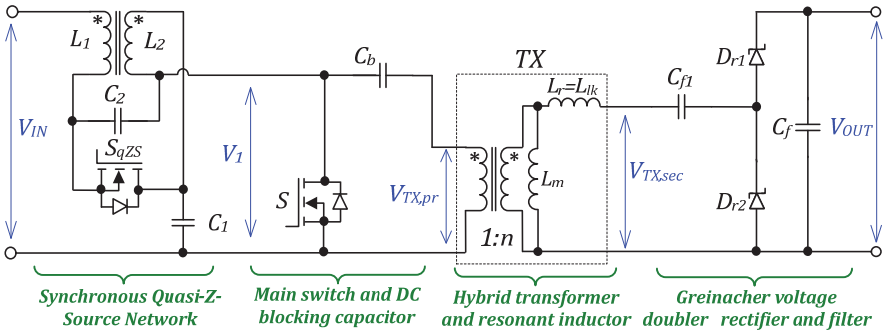


Figure 4.10 Galvanically isolated single-switch qZS MIC topology.

based single-switch GI ISC proposed by the author (Figure 3.8). Its DC voltage gain is two times lower than that of the full-bridge qZS MIC. Therefore, it has limited input voltage range due to operation in the boost mode only.

The single-switch MIC requires only two control channels that operate complementary with small dead-time. The converter utilizes a blocking capacitor C_b and thus can achieve resonant operation inherently due to its interaction with the isolation transformer leakage inductance. Its operating principle is explained in the form of a sketch of the idealized current and voltage waveforms shown in Figure 4.11. The dead-time is required to avoid short-circuiting of the qZS capacitors [6]. Its duration is defined by the process of the leakage inductance energy recuperation to the output side, i.e. until its current hits zero level and active state with the resonant current can be started. Leakage inductance and resonance enable soft-switching behavior of the VDR diodes. In this case, the Greinacher VDR was utilized for easier tuning of the series resonance, as explained in Section 3.4.1.

A prototype shown in Figure 4.12 was designed for 60-cell silicon PV modules and thus rated for 250 W. In this case, the input voltage range is limited to the range from 20 V to 40 V. Therefore, this converter cannot operate under partial shading conditions, while it can still track local MPP within the predefined MPP tracking (MPPT) range from 31 V to 37 V, which is typical for 60-cell PV modules. Most of the components in the prototype and in the previous converter are the same, only some values of the equivalent resonance tank differ. Also, the switching frequency was decreased to 60 kHz to limit switching losses and improve thermal performance of the switches that need to handle the full converter power. Evidently, the considerably simplified MIC is capable of handling the power of 250 W, where full-bridge qZS converters were utilized before. This allows considerable reduction of the realization cost and improved reliability, since the MIC contains fewer components.

Verification of the single-switch qZS MIC was performed according the P-V and I-V profiles of a typical 60-cell PV module that are shown in Figure 4.13 for the irradiance of 1000 W/m^2. Experimental results obtained are listed in Table 4.1 to describe the performance of the MIC when it reaches the MPP around 31 V, starting from the open circuit voltage of 38 V. The simplified

converter has lower efficiency than its full-bridge counterpart, reaching only 95.3%, which is high enough for operation in the boost mode only.

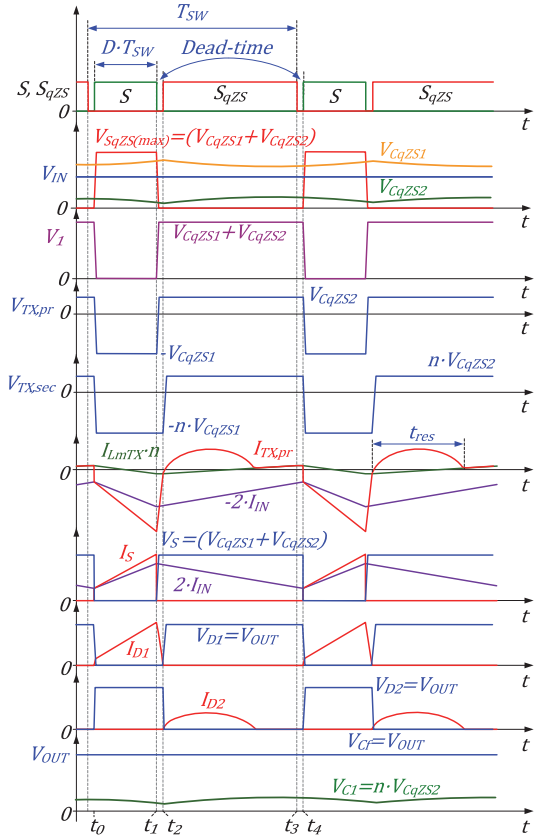


Figure 4.11 Sketch of the idealized current and voltage waveforms of the transformer-based single-switch qZS DC-DC converter [PAPER-X].

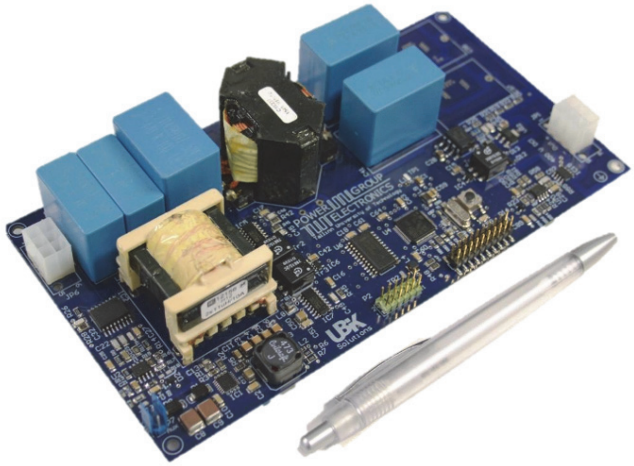
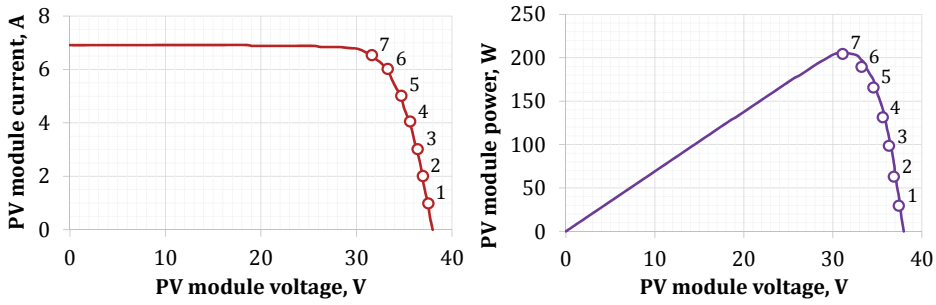


Figure 4.12 Developed 250 W prototype of the single-switch qZS MIC [PAPER-X].

Performance of the incremental conductance MPPT method implemented within the MIC was verified during the start-up transients captured by the oscilloscope (test-bench is shown in Figure 1.3). Figure 4.14 shows that this MIC can reach the MPP in five seconds using the MPPT frequency of 5 Hz. The single-switch MIC suits well for the residential PV applications and provides high static MPPT efficiency of 99.5%.



(a) *(b)*

Figure 4.13 Case study PV profiles.

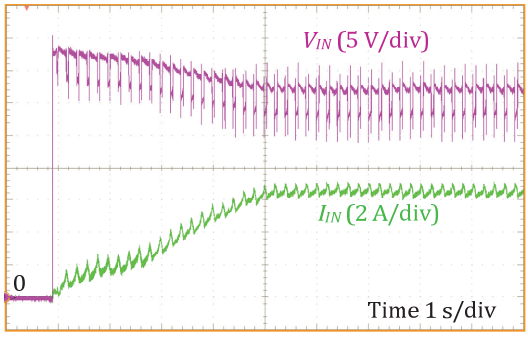


Figure 4.14 Input voltage and current during startup and the MPPT process.

Table 4.1. Measured efficiencies and duty cycle values

Operating points			**Measured values**	
Point nr.	*PV module voltage, V*	*PV module power, W*	*Duty cycle D*	*Efficiency, %*
1	37.2	37.2	0.2	92
2	36.2	72.4	0.21	94.8
3	35.2	105.6	0.22	95.3
4	34.2	136.8	0.23	95.3
5	33.2	167.5	0.24	95.2
6	32.2	193.2	0.25	95.1
7*	31.2	205	0.26	94.8

*Corresponds to the maximum power point

4.4 Galvanically Isolated Power Conditioning Unit for Residential PMSG Based Wind Turbines with a Coupled-Inductor-Based Single-Switch QZS Converter

Residential variable speed wind turbines (WTs) have become widely acceptable owing to remarkable technology advances. However, many of them are based on low voltage multi-pole PMSGs driven by a wind rotor directly. This technology is highly reliable, light weight, and used mostly for battery charging. Integration of small low-voltage WTs into the distribution grid is not popular because of numerous challenges, like requirement of high voltage step-up, a wide PMSG voltage variation (up to 1:5) that is proportional to the rotational speed of a WT, and a drastic variation of the generator output power. Author's brief review in [PAPER-XI] shows that existing state-of-the-art solutions are very complicated, like use of active generator side rectifiers, full-bridge isolated converters, and even electric energy conversion in four stages. According to the author's opinion, small wind energy conversion systems can benefit from the implementation of coupled-inductor-based GI ISCs.

In [PAPER-XI] the author proposed a residential variable speed PMSG based wind energy conversion system shown in Figure 4.15. Electric energy is converted by the novel GI power conditioning unit (PCU). It is much simpler than the existing solutions and therefore can make the technology of residential WTs more attractive for consumers. According to the author, the GI DC-DC converter stage should be implemented in a modular structure, which will reduce the production cost of cells and increase overall system redundancy. The proposed power level of a single cell is 500…600 W, i.e. the smallest WTs require a single cell only, while larger residential WTs need several cells within the PCU.

A 1.3 kW PCU with a two-cell DC-DC converter was implemented for the case study WT. Rated power requires the GI DC-DC stage to contain two cells. The experimental prototype was realized according to the schematic from Figure 4.16, as shown in Figure 4.17. First, the experimental prototype was tested in the 1:10 input voltage range (40…400 V) to prove that it suits a wide variety of small WTs. It utilizes 1:1:1 coupled inductors (caused by relatively high maximum PMSG output voltage of the case study WT) and SiC devices only to achieve high efficiency at 100 kHz switching frequency. Regardless of the hard-switching operation of the converter, the maximum efficiency of nearly 94% was achieved at 400 W constant input power (limited by maximum input current at the minimum input voltage of 40 V), as described in [PAPER-XI]. Hence, the proposed GI DC-DC converter for small WTs is a novel technology, enabling simple integration of these WTs into the distribution grid of residential and small commercial buildings.

Major experimental results were obtained using the characteristics of the case study 8-pole PMSG based WT described in Figure 4.18 using the test-bench shown in Figure 1.4. Five operating points were selected for experimental verification. The maximum WT power of 1275 W corresponds to the fifth

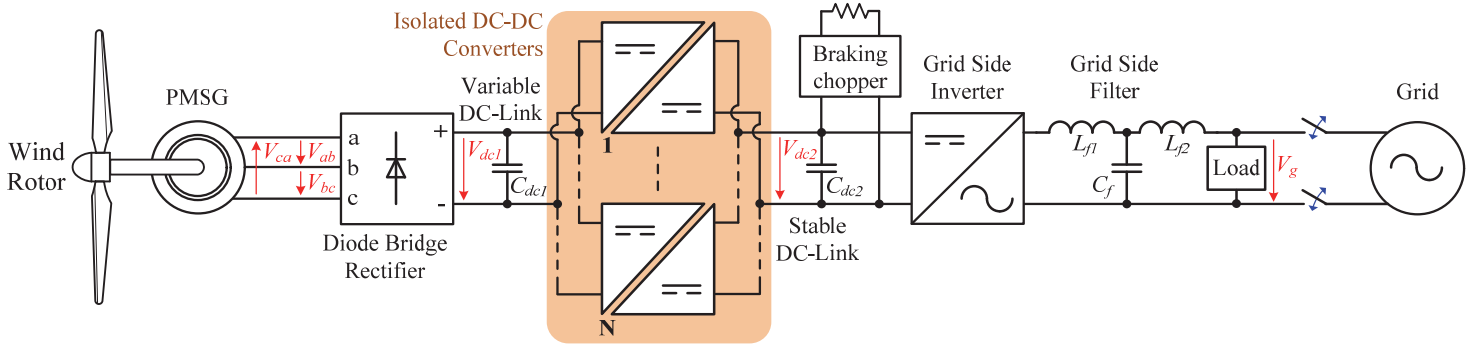


Figure 4.15 Proposed residential variable speed PMSG based wind energy conversion system with GI three-stage PCU that utilizes modular converter based on the coupled-inductor-based qZS GI single-switch converter topology.

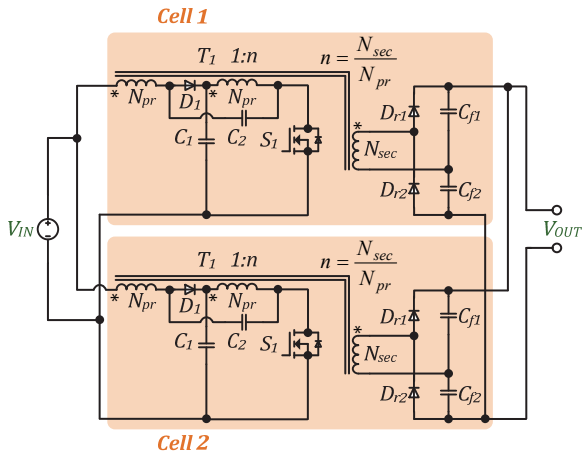


Figure 4.16 Topology of a GI coupled-inductor-based qZS DC-DC converter stage composed of two cells.

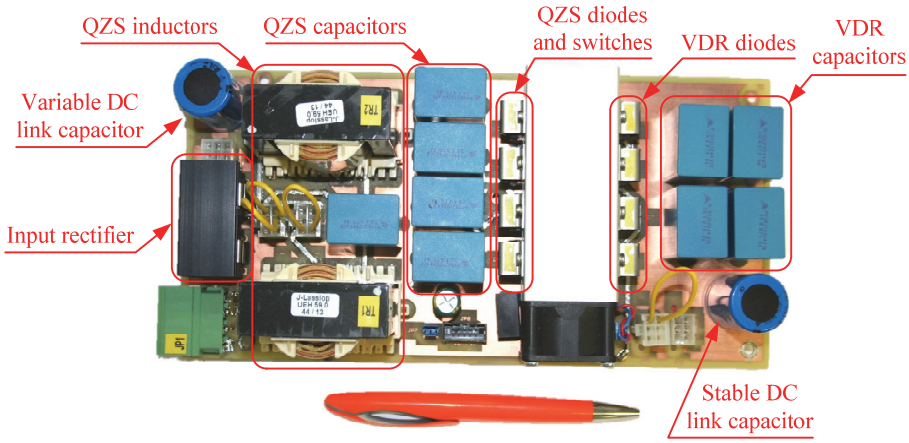
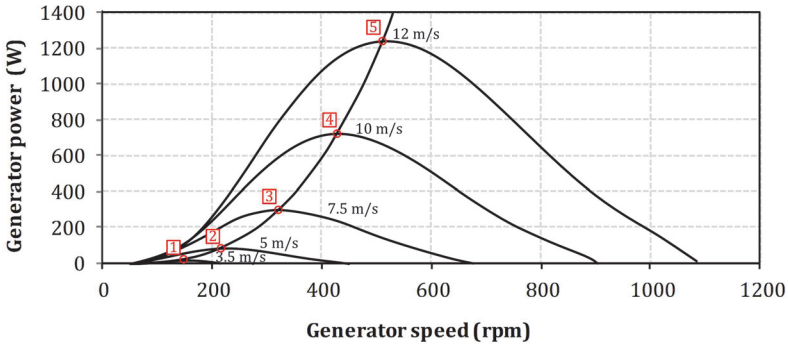
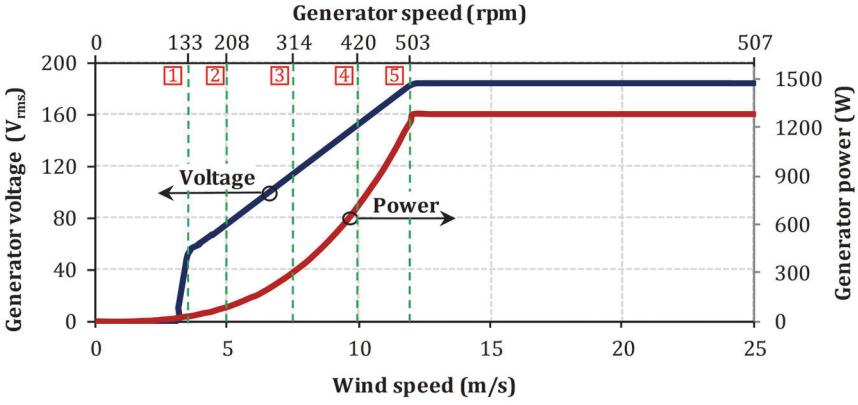


Figure 4.17 Prototype of the two-cell GI qZS DC-DC converter.

operating point. The input and output voltage and current of the PCU corresponding to the maximum input power are shown in Figure 4.19. Obviously, the diode bridge rectifier used results in the distorted PMSG phase current. However, this has minor influence on the annual energy yield [103]. The grid-side inverter produces output voltage and current with low distortions, which justifies proper selection of the grid side filter components. The stable DC-link features voltage ripple with frequency twice higher than that of the inverter output voltage, but the second DC-link capacitance is sufficient to suppress its amplitude. The DC-DC stage was able to stabilize the second DC-link voltage regardless of severe changes of the input power and voltage.

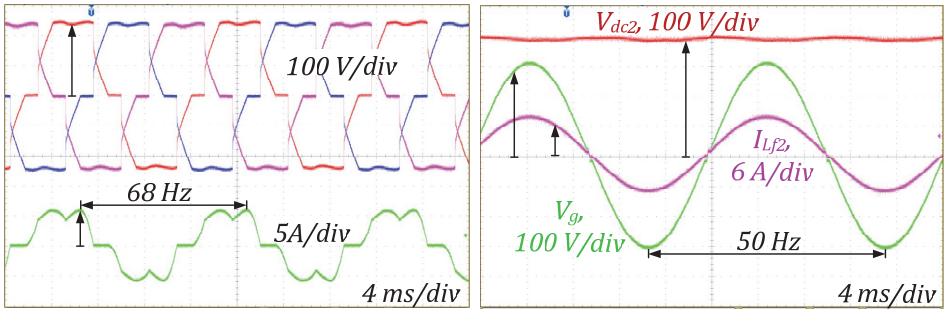


(a)



(b)

Figure 4.18 Characteristics of the given PMSG based WT: optimal torque curve (a) and dependence of the PMSG line-to-line voltage and output power on the wind speed (b).



(a) *(b)*

Figure 4.19 Experimental voltage and current waveforms: generator output line-to-line voltages (top) and phase current (bottom) (a) and the stable DC link voltage (top) and inverter current and voltage (bottom) (b).

Efficiency curves were measured with the power analyzer for three electric energy conversion stages: PMSG side rectifier, DC-DC converter, and inverter. Usually, this information is left out of most of the reports on PCUs for residential WTs. The results of the experimental efficiency measurements are shown in Figure 4.20. Evidently, the diode bridge rectifier that operates at the WT frequency has the highest efficiency. The efficiency of the grid side inverter is higher than that of the DC-DC stage, which was expected, considering galvanic isolation. The resulting PCU efficiency reaches the peak value higher than 90%, which is a high enough for the three stage electric energy conversion.

Regarding to thermal issues, special attention was paid to semiconductor power losses of the DC-DC stage. At the maximum input power, its cumulative semiconductor power losses exceed 45 W out of 70 W total power loss, the breakdown of which is shown in Figure 4.21. As a result, it was decided to use common compact heatsink with active cooling and 1.1 K/W thermal resistance to improve the converter power density.

It can be concluded that the PCU proposed suits well for residential variable speed PMSG based WTs and allows capital cost reductions.

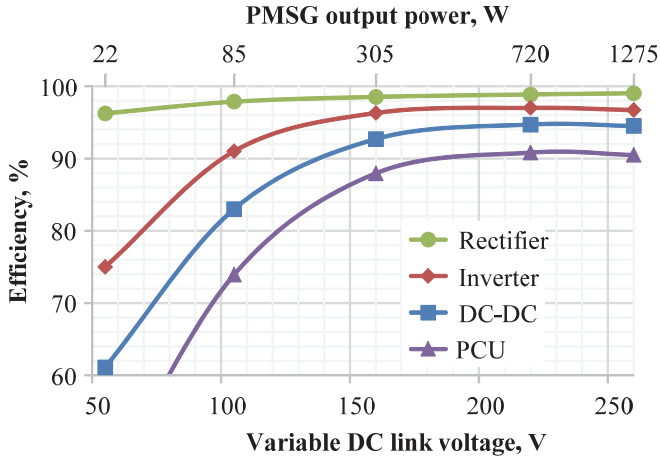


Figure 4.20 Efficiency measurement of the PCU and its parts.

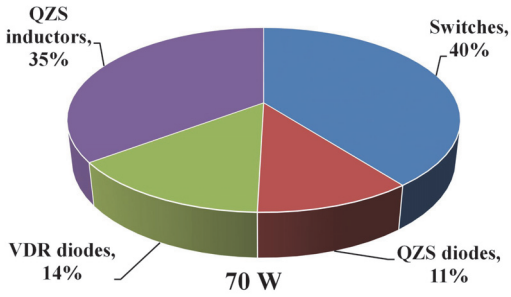


Figure 4.21 Power loss breakdown on the DC-DC converter at the maximum power (operating point 5).

4.5 Summary

In this chapter, application-oriented design of GI ISCs was discussed. First, the range of applications where GI ISCs can make a significant change in the current technology was identified. It involves integration of small renewable and alternative energy sources into power systems of residential and small commercial buildings as a part of the global shift towards zero energy buildings. Considering the latest regulations introduced by the European Commission and other national and international level regulators, technologies enabling micro power generation from renewable and alternative energy sources will be of a rapidly increasing demand in the next five years. Author anticipates that the technology of GI ISCs will become one of the key solutions to speed up a wide acceptance of small renewable or alternative energy sources at household and small community levels and consequently, to improve the security of the electrical power supply.

Three demonstrators with different sets of requirements were developed by the author to justify the technology of the GI ISCs as a versatile solution.

✦ The transformer-based GI full-bridge qZS DC-DC converter was improved by the use of synchronous rectification, resonant switching, and the novel buck-boost control principle [PAPER-IX]. Results of the experimental evaluation justified this topology as a new high-performance photovoltaic module level power electronic interface that can easily resolve the issue of partial shading, enabling global MPPT. The converter proposed facilitates galvanically isolated topologies move towards traditional application ranges of the non-isolated power optimizers, where conventional GI CSCs and VSCs were avoided due to the limited input voltage range.

✦ In PV module level applications where the cost of realization is more important than high performance, the single-switch topologies can be utilized within a module integrated converter [PAPER-X]. It is difficult to achieve peak efficiency well over 95% with those converters since only the boost mode is available for the input voltage regulation. They easily track local MPP within the predefined range, but cannot reach global MPP in the case of partial shading. Hence, they can be regarded as a low-cost solution with acceptable performance similar to that of numerous existing solutions.

✦ The coupled-inductor-based converters can be a simple solution for applications where high current ripple inherent to those topologies will not limit their performance. The single-switch topology with a single coupled inductor was proven to simplify power conditioning units, reduce their cost, number of electric energy conversion stages, and, consequently, increase reliability. The modular design of the GI DC-DC stage proposed by the author was justified for residential directly driven variable speed PMSG based WTs in [PAPER-XI].

5 CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

The results of this PhD thesis fully satisfy the aims set and prove the hypotheses formulated by the author. The GI ISCs were identified as a novel family of the GI DC-DC converters that combines major features of the existing VSCs and CSCs while providing an extended input voltage and load regulation range. The review paper published by the author in [PAPER-I] introduced those findings to the field of power electronics in order to start discussion and increase awareness among researchers and engineers regarding the technology of the GI ISCs. Within this research work, the author has shown that the GI ISCs can utilize well known switching stages, like full-bridge, half-bridge, push-pull, single-switch, etc. that are widely used in the traditional CSCs and VSCs. This allowed the introduction of a new classification of the GI ISCs based on the type of magnetic component that transfers energy from the input to the output side. This classification differs from those proposed for the IS inverters where the ISN type is used as a major classification feature. Moreover, the classification proposed can be used as a powerful tool to derive new GI ISC topologies with predefined features.

Substantial work was performed to synthesize new GI ISC topologies in order to show versatility of this technology, underline its importance and numerous possibilities for the future research in this field. Author anticipates that a higher variety of topologies will inevitably result in increased performance of solutions based on the GI ISCs. This is because more degrees of freedom will be available for converter design, allowing tailoring of the converter for particular applications, taking into account the power level, input voltage range, price constraints, etc. For example, symmetrical half-bridge topologies suit well for the integration of a PV panel that contains two PV modules, which is a common task in residential installations, while it seems to be less attractive for most of the applications. Though this work could not fill all the research gaps in the area, it is a significant leap in the development of the GI ISC family. This research organizes and significantly increases existing knowledge in this field and, consequently, shows numerous possibilities for the future research in this field. A novel class of converters with combined energy transfer was identified through the classification and structuring of existing knowledge in this field. Generally speaking, this work has introduced the terminology and tools for the further development of the GI ISC field.

The GI ISCs were justified as a promising technology for the integration of the small scale renewable and alternative energy sources into the power systems of residential and small commercial buildings, supporting in this way the zero energy building concept. The three case studies performed show that a high variety of topologies, among which many were introduced by the author, allow researchers and engineers to find a solution based on the GI ISCs that satisfies numerous design requirements and provides additional benefits over the

existing solutions. The transformer-based GI ISCs have shown good performance in PV applications while the coupled-inductor-based topologies are capable of operating in WT applications with severe changes of the input voltage and power.

As the main results of this thesis research, the author claims the following:

1. The galvanically isolated impedance-source DC-DC converters were distinguished and justified as a new electric energy conversion technology that is an alternative to the existing voltage-source and the current-source counterparts.
2. The author has derived a versatile classification of the galvanically isolated impedance-source DC-DC converters based on the type of magnetic components that transfer energy from the input to the output side. It clearly reflects the essence of the energy conversion principle and can be used as a unique tool for the derivation of new topologies tailored for the given application.
3. The novel class of the galvanically isolated impedance-source DC-DC converters with combined energy transfer derived can be characterized by energy transfer from the input side to the output side performed by means of the coupled inductors and the isolation transformers simultaneously. It substantially extends the family of the galvanically isolated impedance-source DC-DC converters and introduces a new principle of the electric energy conversion.
4. The author has introduced **12** novel topologies of the galvanically isolated impedance-source DC-DC converter, i.e. **12** novel electric energy conversion methods alternative to the full bridge converters that were dominating this field before the work performed by the author. Example topologies were derived using the quasi-Z-source network.
5. It was shown theoretically and experimentally that the technology of the galvanically isolated impedance-source DC-DC converters can substantially improve the performance of the existing solutions. It extends the input voltage regulation range, minimizes the number of the electric energy conversion stages, improves withstandability to harsh EMI environments, and avoids discontinuous conduction mode with extreme voltage step-up when the synchronous impedance-source network is utilized.
6. The author has studied and selected guidelines for practical implementation of the galvanically isolated impedance-source DC-DC converters that enable their maximum performance. The most promising are the following: coupled inductors and synchronous rectification in the impedance-source networks, voltage doubler rectifier in the voltage step-up converters, the resonant switching, parallel-series cascading of the standardized power electronics modules, use of the quasi-Z-source network due to its inherent self-clamping capabilities, etc.

Taking into account theoretical and practical results obtained by the author, it can be concluded that the GI ISC can be one of the technologies enabling smart zero energy buildings for eco-friendly, sustainable future of humanity.

5.2 Future Work

This research work has extended the family of the GI ISCs considerably. Therefore, numerous questions were raised with the introduction of new classes and groups of topologies within this family. One of the most important questions for any power electronic converter is to identify applications that can benefit from the particular converter topology. The GI ISCs introduce at least three different classes of ISCs, which can be confusing when searching for a solution tailored for the particular application. Therefore, extensive application-oriented research is required to clarify the performance of the GI ISCs in different applications. This thesis has already introduced several high performance solutions that will be adopted by industry, but it is not sufficient for an overall approval of the GI ISC technology by the industry in general.

Identification of the three classes of GI ISCs should be followed by studies of the application of different ISNs since they influence some key features of the resulting converter. For example, the ZS and qZSNs provide many similar features, while only the qZS ensures the continuous input current. Moreover, numerous active ISNs, like switched boost concept and its derivatives, were introduced recently as a better alternative to the qZSN. They feature less passive components, but require more semiconductor components, which could be a disadvantage in applications with relatively high input current, like integration of PV modules or fuel cells.

The proposed classification of the GI ISCs seems to have room for improvement at the second level, where the switching stages are placed. For example, there are no half-bridge GI ISCs with combined energy transfer, while their derivation from the corresponding transformer-based topologies could be feasible, like in the case of the full-bridge or the push-pull switching stages.

There are also practical issues in the GI ISCs to be resolved. The concept of the GI ISCs with combined energy transfer requires extensive experimental evaluation and comparison with the corresponding transformer-based GI ISCs. Also, reliability of the GI ISCs has to be studied since they contain an increased number of passive components and/or semiconductor devices. It is known that failures of capacitors are a major contributor to the reliability of power electronic converters, followed by PCB and semiconductor components issues [104]. It is not evident which approach is more reliable: use of a traditional qZSN or active ISNs with a reduced number of passive components, but an increased number of semiconductors. It is required to answer all of those practical questions before industry will accept the GI ISC technology.

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LIST OF AUTHOR'S PUBLICATIONS

The present PhD thesis is based on the following publications that are referred to in the text by Roman numbers.

[PAPER-I] A. Chub, D. Vinnikov, F. Blaabjerg and F. Z. Peng, "A Review of Galvanically Isolated Impedance-Source DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2808-2828, April 2016.

[PAPER-II] D. Vinnikov, A. Chub and L. Liivik, "Asymmetrical quasi-Z-source half-bridge DC-DC converters," *Proc. 9th International Conference on Compatibility and Power Electronics (CPE)*, Costa da Caparica, 2015, pp. 369-372.

[PAPER-III] D. Vinnikov, A. Chub, O. Husev, and J. Zakis, "Quasi-Z-source half-bridge DC-DC converter for photovoltaic applications," *Proc. 2015 IEEE International Conference on Industrial Technology (ICIT)*, Seville, 2015, pp. 2935-2940.

[PAPER-IV] A. Chub, D. Vinnikov, and T. Jalakas, "Galvanically isolated quasi-Z-source DC-DC converters with combined energy transfer for renewable energy sources integration," *Proc. 2015 IEEE International Conference on Industrial Technology (ICIT)*, Seville, 2015, pp. 2896-2900.

[PAPER-V] A. Chub and D. Vinnikov, "Single-switch galvanically isolated quasi-Z-source DC-DC converter," *Proc. 2015 IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG)*, Riga, 2015, pp. 582-586.

[PAPER-VI] A. Chub, O. Husev, A. Blinov, and D. Vinnikov, "CCM and DCM Analysis of Quasi-Z-Source Derived Push-Pull DC/DC Converter," *Informacije MIDEM-Journal of Microelectronics Electronic Components and Materials*, vol. 44, no. 3, pp. 224−234, 2014.

[PAPER-VII] A. Chub, O. Husev, D. Vinnikov, and F. Blaabjerg, "Novel family of quasi-Z-source DC/DC converters derived from current-fed push-pull converters," *Proc. 2014 16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe)*, Lappeenranta, 2014, pp. 1-10.

[PAPER-VIII] A. Chub, O. Husev, and D. Vinnikov, "Input-parallel output-series connection of isolated quasi-Z-source DC-DC converters," *Proc. 2014 Electric Power Quality and Supply*

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[PAPER-IX] D. Vinnikov, A. Chub, L. Liivik, and I. Roasto, "High-Performance Quasi-Z-Source Series Resonant DC-DC Converter for Photovoltaic Module Level Power Electronics Applications," *IEEE Trans. Power Electron.*, accepted for publication.

[PAPER-X] D. Vinnikov, A. Chub, and E. Liivik, "Single-Switch Galvanically Isolated Step-Up DC-DC Converter for Photovoltaic Applications," *IECON'2016*, accepted for publication.

[PAPER-XI] A. Chub, O. Husev, D. Vinnikov, and A. Blinov, "Novel Galvanically Isolated Power Conditioning Unit for Micro Wind Turbine Applications," *submitted for consideration to IEEE Trans. Ind. Electron*.

AUTHOR'S OWN CONTRIBUTION TO THE PUBLICATIONS

Author's contribution to the papers in this thesis:

[PAPER-I] Andrii Chub as the main author of the paper has provided the literature review, synthesized the classification and co-authored writing.

[PAPER-II] Andrii Chub co-authored the paper, synthesized the converter topology, and was responsible for the experimental study of the prototype developed by him. He presented the paper at 9th International Conference on Compatibility and Power Electronics (CPE), June 2015, Costa da Caparica, Portugal.

[PAPER-III] Andrii Chub co-authored the paper, synthesized the converter topology, and was responsible for the experimental study of the prototype developed by him. He presented the paper at 2015 IEEE International Conference on Industrial Technology (ICIT), March 2015, Seville, Spain.

[PAPER-IV] Andrii Chub is the main author of the paper, responsible for the literature review and the simulation study in PSIM software. He had a major role in writing, and presented the paper at 2015 IEEE International Conference on Industrial Technology (ICIT), March 2015, Seville, Spain.

[PAPER-V] Andrii Chub is the main author of the paper, responsible for the literature review and the simulation study in PSIM software, development of the experimental prototype and its testing. He had a major role in writing, and presented the paper at 2015 IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (POWERENG), May 2015, Riga, Latvia.

[PAPER-VI] Andrii Chub is the main author of the paper, responsible for the literature review, submission and communication with editors, the simulation study in PSIM software, development of the experimental prototype and its testing.

[PAPER-VII] Andrii Chub is the main author of the paper, responsible for the literature review and the simulation study in PSIM software. He had a major role in writing, and presented the paper at 2014 16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe), August 2014, Lappeenranta, Finland.

[PAPER-VIII] Andrii Chub is the main author of the paper, responsible for the literature review and the simulation study in PSIM software, development of the experimental prototype and its testing. He had a major role in writing, and presented the paper at 2014 Electric Power Quality and Supply Reliability Conference (PQ) June 2014, Rakvere, Estonia.

[PAPER-IX] Andrii Chub co-authored the paper, synthesized the converter topology and its design guidelines, and was responsible for the experimental study of the prototype developed by him.

[PAPER-X] Andrii Chub co-authored the paper, synthesized the converter topology, and was responsible for the experimental study of the prototype developed by him. He will present the paper at 42nd Annual Conference of the IEEE Industrial Electronics Society (IECON'2016), October 2016, Florence, Italy.

[PAPER-XI] Andrii Chub is the main author of the paper, responsible for the literature review, submission and communication with editors, the simulation study in PSIM software, development of the experimental prototype and its testing.

ABSTRACT

This PhD thesis is dedicated to the development of the novel field in power electronics – galvanically isolated impedance-source DC-DC converters. It was shown that these converters can be characterized by beneficial features of both the current-source and voltage-source converters, while avoiding their drawbacks. Therefore, the GI ISCs were justified as a new technology of electric energy conversion alternative to the existing CSCs and the VSCs.

The existing GI ISCs were broadly categorized into two classes: the transformer-based and the coupled-inductor-based according to the magnetic components that transfer energy from the input to the output side. As a result, a versatile classification was synthesized and a novel class of the GI ISCs was introduced – converters with combined energy transfer that utilize both the isolation transformers and the coupled inductors for energy transfer from the input to the output side. Five novel topologies were synthesized within this novel class. Moreover, seven other topologies from the transformer-based and the coupled-inductor-based classes were synthesized and analyzed. These results contribute substantially to the development of the field of the GI ISCs. Availability of different GI ISC topologies with different sets of features allows the GI ISCs to be applied to a wider range of applications.

Implementation challenges of the GI ISCs were discussed. According to the author's opinion, the synchronous rectification along with resonant switching can improve the efficiency of the GI ISCs limited by additional components of the ISN. The voltage doubler rectifier was justified as the superior solution for the voltage step-up GI ISCs. Moreover, cascading of converters can improve DC voltage gain and redundancy of the whole system. Also, wide bandgap semiconductors were pointed out as a major possibility to implement highly efficient high-frequency GI ISCs.

This work has also a substantial practical value since it introduces three examples of the application-oriented design of GI ISCs (intended for zero energy buildings):

- ✦ high performance PV microconverter with an ultra-wide input voltage range comparable to that of much simpler non-isolated power optimizers, which, consequently, can withstand even complicated cases of partial shading;
- ✦ low-cost PV microconverter based on the transformer-based single-switch qZS topology, which features limited input voltage range;
- ✦ novel galvanically isolated power conditioning unit for the residential variable speed PMSG based WTs.

The theoretical and practical results contribute substantially to the field of the GI ISCs and can be used as a knowledge base for further developments in this field. Practical results obtained by the author advertise the benefits of the GI ISC technology and make it attractive for the industry.

KOKKUVÕTE

Käesolev doktoritöö on pühendatud galvaaniliselt isoleeritud impedantsallikaga alalispingemuundurite (GI IA APM) arendamisele, mis kuuluvad uudsesse jõuelektroonika valdkonda. Doktoritöös selgub, et seda tüüpi muunduritel on nii pinge- kui ka vooluallikaga muundurite kasulikud omadused. Seetõttu on GI IA APM-te kasutamine elektrienergia muundamises õigustatud alternatiiviks olemasolevatele pinge- ja vooluallikaga muunduritele.

Olemasolevad GI IA APM-te topoloogiad saab sõltuvalt energia ülekandmiseks kasutatavatest magnetilistest komponentidest jagada kahte klassi: trafol põhinevateks ning sidestatud induktoril põhinevateks. Doktoritöö tulemusena sai välja töötatud selliste muundurite mitmekülgne klassifikatsioon ning sai loodud uus GI IA APM-te klass – kombineeritud elektrienergia ülekandega muundurid, milles on kasutatud nii trafosid kui ka sidestatud induktoreid elektrienergia ülekandmiseks. Uude klassi sai doktoritöö jooksul sünteesitud viis uudset muundurite topoloogiat. Lisaks nendele, sai doktoritöö jooksul sünteesitud seitse uut topoloogiat juba eksisteerivatesse trafol ning sidestatud induktoril põhinevatesse klassidesse. Need tulemused annavad suure panuse GI IA APM-te arendamisesse. Oma kasulike omaduste tõttu sobivad GI IA APM-te topoloogiad väga mitmesugustesse rakendusvaldkondadesse.

Doktoritöös arutletakse GI IA APM-te rakendamisega seotud väljakutsete üle. Autor leiab, et sünkroonne alaldamine ning jõupooljuhtlülitite resonants-lülitamine võimaldavad tõsta GI IA APM-te kasutegurit, mis on nendes muundurites kasutavate lisakomponentide tõttu piiratud. Doktoritööst selgub, et parimaks topoloogiaks pinget tõstvate galvaaniliselt isoleeritud impedantsallikaga tüüpi muundurite seast on pingekordisti. Lisaks sellele, võimaldaks muundurite kasutamine jadaühenduses suurendada seadmete pingetõstmisvõimet ning tõsta kogu süsteemi töökindlust. Laia keelutsooniga pooljuhtide kasutamine võimaldaks GI IA APM-tes saavutada kõrget kasutegurit ning lülitussagedust.

Käesolevale doktoritööle annab märkimisväärse praktilise väärtuse GI IA APM-te disain kolmele rakendusvaldkonnale (võimalik kasutada null-energia ehitistes):

- ✦ suure jõudlusega ning väga laia sisendpinge vahemikuga mikrovaheldi päikesepaneelidele, mis on võimeline taluma ka järsku osalist varjutust;
- ✦ ühe-jõupooljuhtlüliti ning trafo põhine qZS topoloogia odavatele päikesepaneele teenindavatele mikromuunduritele;
- ✦ uudne, püsimagnetgeneraatoritel töötavatele tuuleturbiinidele mõeldud, galvaaniliselt isoleeritud muundur.

Doktoritöö teoreetilised ja praktilised tulemused annavad olulise panuse GI IA APM-te valdkonna edasisele arendamisele. Autori poolt saadud praktilised tulemused toovad välja GI IA APM-te tehnoloogilised eelised ning muudavad selle tehnoloogia atraktiivseks ka tööstusele.

ELULOOKIRJELDUS

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Tšernigivi Riiklik Tehnoloogiaülikool, Tööstuselektroonika Instituut	2008	Bakalaureuse kraad (kiitusega)
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Keel	Tase
Ukraina keel	Kõrgtase
Vene keel	Kõrgtase
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Eesti keel	Algtase

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Töötamise aeg	Tööandja nimetus	Ametikoht
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2013 - Diplom kõrgel tasemel teadusliku aruande ja töö praktiliste väärtuste eest rahvusvaheliselt konverentsilt (18th International Scientific-Technical Conference "Power Electronics and Energy Efficiency)
2013 - Kõige aktiivsema osaleja auhind rahvusvahelisel konverentsil (54th Int. Scientific Conference on Power and Electrical Engineering)
2013 - Parima artikli eest tänukiri rahvusvaheliselt konverentsilt (IECON2013)
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6. Teadustöö põhisuunad:

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ETF9350 - Elektersõidukite kiirlaadimiseks kasutatavate uudsete kahesuunaliste muunduritopoloogiate ja juhtimisalgoritmide uurimine ja väljatöötamine
ETF8687 - Intelligentne trafo – talitlusrežiimide analüüs
ETF8538 - Kvaasi-impedantsallikaga alalis- ja vahelduvpingemuundurid
PUT744 - Pehmelülitusega galvaaniliselt isoleeritud alalispingemuundurite uus perekond
Va16021 - Jõuelektroonika muundur kui energiaruuter aktiivsete jaotusvõrkude jaoks
LEP15006 - PV rakendustele mõeldud moodul integreeritud muundurite uurimine ning väljatöötamine
Lep16005 - Järgmise põlvkonna päikeseenergia rakenduse otstarbeks moodul integreeritud muundurite uurimine, arendamine ja optimeerimine
Lep13069 - Taastuvenergeetika rakendustele mõeldud progressiivsete jõuelektroonika muundurite uurimine ja väljatöötamine - tootmiseelsete näidiste (demonstraatorite) kokkupanek ja katsetamine
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2. Education

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Chernihiv State Technological University	2008	Bachelor degree (cum laude)
Chernihiv Secondary School No 30	2004	Secondary education

3. Language competence/skills (fluent; average, basic skills)

Language	Level
Ukrainian	Native
Russian	Native
English	Fluent
Estonian	Beginner

4. Professional employment

Period	Organization	Position
2014 –	Tallinn University of Technology	Junior researcher
2013 – 2014	Tallinn University of Technology	Engineer
2010 – 2012	Chernihiv Branch of Ukrtelecom JSC	Hardware Engineer
2009 – 2009	Chernihiv State Technological University	Research Engineer
2006 – 2008	Chernihiv State Technological University	Laboratory Assistant

5. Honors and awards

2015 - Best Paper Award Certificate - IEEE 5th International Conference on Power Engineering, Energy and Electrical Drives (PowerEng'2015)
2015 - IEEE-IES Student Travel Scholarship - 2015 IEEE International Conference on Industrial Technology (ICIT'2015)
2014 - Diploma for the Composition and Presentation of the Best Paper - 14th Biennial Baltic Electronics Conference (BEC'2014)
2013 - Diploma for High Level of Scientific Report and Practical Value of the Work - 18th International Scientific-Technical Conference "Power Electronics and Energy Efficiency"
2013 - Most Creative Participant Award in the Section of Power and Electrical Engineering, Subsection of Electrical Engineering - 54th International Scientific Conference on Power and Electrical Engineering
2013 - Certificate of Appreciation for Best Paper in session SS19.4 of 39th Annual Conf. of the IEEE Industrial Electronics Society (IECON'2013)
2009 - Scholarship of the Cabinet of Ministers of Ukraine
2008 - Scholarship of the President of Ukraine
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7. Current grants & projects

SF0140016s11 - New Converter Topologies and Control Methods for Electronic Power Distribution Networks
VEU15033 - Innovation in Intelligent Management of Heritage Buildings
ETF9350 - Research and Development of New Converter Topologies and Control Methods for Fast Charging of Electric Vehicle
ETF8538 - Quasi-Impedance Source DC/DC and AC/AC Converters
ETF8687 - Intelligent Transformer – Analysis of Operating Modes
PUT744 - New Family of Full Soft-Switching Isolated DC/DC Converters
Va16021 - Power Electronic Transformer - An Energy Router For Active Distribution Grids
LEP15006 - Research and Development of Module Integrated Converters (MICs) for Photovoltaic (PV) Applications
Lep16005 - Research, Development and Optimization of the Next-Generation Photovoltaic Module Integrated Converters
Lep13069 - Research and Development of Advanced Power Electronic Converters for Renewable Energy Systems (Demonstrators)
PUT633 - New Power Quality Improvement Techniques for Distributed Generation Systems

APPENDIXES

[PAPER-I] A. Chub, D. Vinnikov, F. Blaabjerg and F. Z. Peng, "A Review of Galvanically Isolated Impedance-Source DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 2808-2828, April 2016.

A Review of Galvanically Isolated Impedance-Source DC–DC Converters

Andrii Chub, *Student Member, IEEE*, Dmitri Vinnikov, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*, and Fang Zheng Peng, *Fellow, IEEE*

***Abstract*—Impedance-source converters, an emerging technology in electric energy conversion, overcome limitations of conventional solutions by the use of specific impedance-source networks. Focus of this paper is on the topologies of galvanically isolated impedance-source dc–dc converters. These converters are particularly appropriate for distributed generation systems with renewable or alternative energy sources, which require input voltage and load regulation in a wide range. We review here the basic topologies for researchers and engineers, and classify all the topologies of the impedance-source galvanically isolated dc–dc converters according to the element that transfers energy from the input to the output: a transformer, a coupled inductor, or their combination. This classification reveals advantages and disadvantages, as well as a wide space for further research. This paper also outlines the most promising research directions in this field.**

***Index Terms*—DC–DC power converters, galvanic isolation, impedance-source (IS) converters, renewable energy sources.**

I. Introduction

RESEARCH in the field of impedance-source converters (ISCs) was initiated by the invention of the Z-source (ZS) inverter based on the ZS network [1]. ZS inverters (ZSIs) are able to provide buck–boost functionality by the single switching stage and improved reliability due to the inherent short-circuit immunity. These advantages urge active research in the field of impedance-source inverters. Recent ten years have seen a growing number of studies published in this area. The impedance-source (IS) technology was applied to all four basic converter types: dc–dc, ac–ac, dc–ac, and ac–dc. IS converters are applied in a very broad area from modern energy generation systems (renewable and alternative) to dc circuit breakers and electronic loads [2]. Impedance-source network (ISN) is the key element of any converter in this group. It consists of inductors, capacitors, and diodes (or switches). Any basic ISN can be represented as a two-port network that allows improved reliability, dc voltage (or current) gain, and provides immunity to shoot-through and open states. A number of novel ISNs have been proposed to improve the performance, cost, and reliability of IS converters [2].

A wide penetration of energy sources with low output voltage, like PV panels or fuel cells, has stimulated research into isolated step-up dc–dc converters with a wide input voltage variation range. They are intended to integrate low-voltage energy sources to the common dc link with much higher operating voltage. In this case, a magnetic element is used not only for galvanic isolation but also to define the dc gain range. Input voltage variations can be compensated at the controlled step-up stage inside the converter. The dc gain of this step-up stage is usually within the range from one to three. This range is selected to keep the efficiency of the controlled step-up stage within an acceptable range, while a major voltage step-up may occur at the isolation magnetic element with high efficiency.

The IS galvanically isolated dc–dc converters were reported as a suitable solution to interface low-voltage renewable or alternative energy sources [2], [3]. They have a wide input voltage and load regulation range that allows a better use of the energy source. Other advantages of the IS galvanically isolated dc–dc converters include the possibility of converterless integration of the short-term energy-storages (batteries) [4], bidirectional operation capability [5]–[7], and the inherent short-circuit protection. Converterless energy storage integration could be provided through direct connection of a battery in parallel with an ISN capacitor [8]. However, an additional bidirectional converter [9] can be used to enhance the operation range of the converter.

The aim of this paper is to review and systematize the state-of-the-art IS galvanically isolated dc–dc converters to fill the gap in the classification proposed in [2]. Section II presents a generalized comparison of the ISC technology with the voltage-source convertors (VSC) and current-source converters (CSC). Next, developments in the research of the IS galvanically isolated dc–dc converters are outlined. Then, the emerged IS galvanically isolated dc–dc converters, which have several hierarchical levels, are classified and their possible future research directions are indicated.

II. General Comparison With Voltage-Source and Current-Source DC–DC Converters

In contrast to the classical voltage-source and current-source converters (VSC and CSC, correspondingly), the ISC features an alternative power conversion approach, which combines both the advantages of the VSC and CSC and offers some extra benefits. This section explains the essence of the IS galvanically

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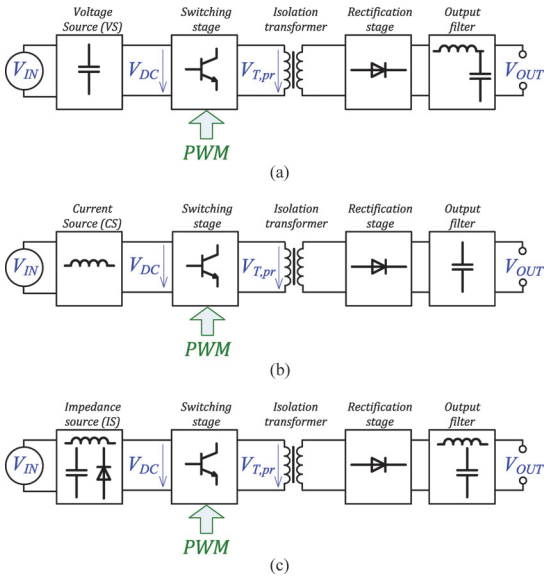

Fig. 1. Generalized block diagrams of (a) voltage-source, (b) CS, and (c) IS galvanically isolated dc–dc converters.

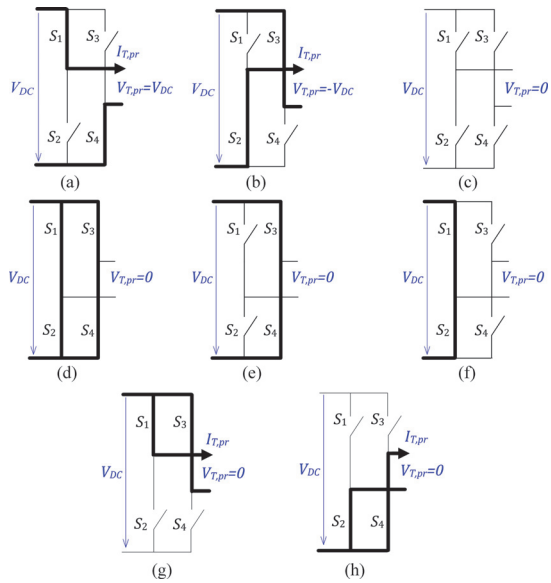

Fig. 2. Typical switching states of the single-phase inverter: (a) and (b) two active states, (c) one unstable state $V_{T,\mathrm{pr}} < V_{\mathrm{DC}}$, (d)–(f) three shoot-through states, and (g) and (h) two zero states.

isolated dc–dc converters in brief and compares them in general terms with the VSC and the CSC.

The generalized block diagrams of the three approaches are shown in Fig. 1. To simplify the discussion, the switching stage is represented by the single-phase full-bridge inverter followed by the isolation transformer and the diode rectifier with an output filter. Thereby, the inverter is controlled by a symmetrical pulse width modulation (PWM) [10].

The traditional VSC [see Fig. 1(a)] performs only the buck function of the input voltage by the variation of the duty cycle of the primary inverter switches. The VSCs are typically equipped with the output *LC* filter, which has an averaging effect on the applied pulsating voltage. In the traditional (square wave) PWM control, the duty cycle of the switches in the inverter bridge could vary between 0 and 0.5, thus providing minimum and maximum output voltage of the converter, correspondingly. Therefore, the switching period of the VSC typically consists of the combination of the active states [see Fig. 2(a) and (b)] and zero states [see Fig. 2(g) and (h)]. Since the VSC has the capacitive energy-storage element, it is very sensitive to the cross conduction of the switches in the inverter legs. Such short-circuit can easily destroy the converter; therefore, a dead time is typically introduced to eliminate the possibility of cross conduction at the duty cycles close to their maximum. Resulting from its simple realization and control, in the galvanically isolated dc–dc power conversion, the VSC is the most popular recent approach.

The CSC [see Fig. 1(b)] is characterized by the presence of the inductive storage element, which forms a current source (CS) on the dc side. In contrast to the VSC, the primary side of the CS galvanically isolated dc–dc converters performs the boost function only, i.e., the amplitude value of $V_{T,\mathrm{pr}}$ [see Fig. 1(b)] will always be higher than the input voltage. Therefore, shoot-through [see Fig. 2(d)–(f)] and active states [see Fig. 2(a) and (b)] are combined in the control of the primary inverter, and the duty cycle of inverter switches is typically higher than 0.5. The CS inverters have no open-circuit immunity, which means that at every time instant at least one loop with two devices conducting has to be ensured. Similarly to the VSC, the CS galvanically isolated dc–dc converters can be used in the bidirectional applications without significant hardware modifications. In the bidirectional power flow, the input inductor behaves as a first-order low-pass filter, thus suppressing the high-frequency ripple.

Since the VSC and CSC can realize either a buck or a boost function, an additional switching stage is necessary to widen the input voltage regulation range of these converters. For example, in renewable energy applications with widely changing input voltage, the VS galvanically isolated dc–dc converter is typically equipped with a boost converter (BC).

Traditionally, the BC is implemented before the main VSC [11]. In some cases, the BC is integrated in the secondary stage of the main VSC [12]. A similar approach can be adopted for the CSC, where the buck functionality is realized by the help of the additional step-down converter.

The ISC combines the main properties of the VSC and CSC, allowing both the buck and boost functions within the single switching stage. The ISN can be short- or open-circuited without any damages of the dc–dc converter. Therefore, all switching states illustrated in Fig. 2 can be realized with the ISC. Depending on the application, the ISC can be built either with a capacitive or an *LC* output filter [13]. As with the VSC and the CSC, the IS isolated dc–dc converter assures a bidirectional

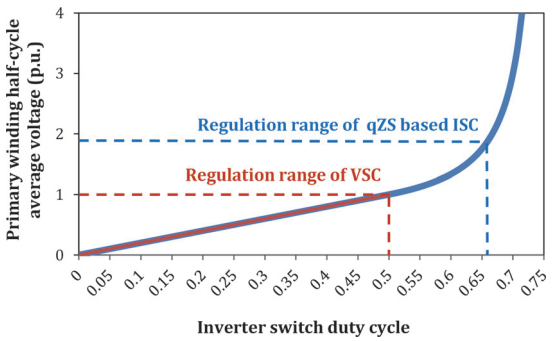

Fig. 3. Half-cycle average voltage of the primary winding of the isolation transformer as a function of the inverter switch duty cycle for the qZS-based ISC and the VSC.

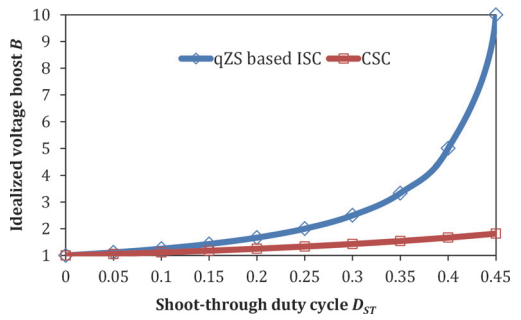

Fig. 4. Idealized voltage boost factor B as a function of the shoot-through duty cycle D_{ST} for the qZS-based ISC and the CSC.

power flow if the diode of the ISN is replaced by a bidirectionally conducting unidirectionally blocking switch. During the reversed power flow, the ISN operates as a low-pass filter and suppresses the high-frequency ripple without any reconfigurations [5]. Therefore, it justifies the ISC regarded as a versatile topology for applications in which a wide range of input voltage and load regulation is essential.

Fig. 3 shows a possibility of extending the regulation range for the traditional VSC by the use of the quasi-Z-source (qZS) network and a modified control algorithm [10]. Since it was assumed that the VSC has an output *LC* filter, the half-cycle average voltage values of the primary winding of the isolation transformer referred to the input voltage are compared for both approaches. For the qZS-based ISC, the operation duty cycle of the inverter switches can be theoretically extended from 0.5 to 0.75. However, in practical applications, the duty cycle values higher than 0.65 are not commonly recommended since they will lead to high conduction losses and a drastic decrease in the efficiency of the converter [14]. Hence, the ISC has nearly twice wider input voltage regulation range than that of the VSC.

With regard to its operation principle, the ISC is quite similar to the CSC, since both of them use the shoot-through switching states to step up the input voltage. In both approaches, the amplitude voltage of the primary winding of the isolation transformer ($V_{T,\mathrm{pr(peak)}}$) depends on the shoot-through duty cycle D_{ST}

$$D_{\mathrm{ST}} = \frac{t_{\mathrm{ST}}}{T} \tag{1}$$

where t_{ST} is the cross conduction time of the switches in the inverter bridge and T is the switching period. The idealized voltage boost across the inverter bridge in the qZS-based ISC is [15]

$$B_{\mathrm{qZS-ISC}} = \frac{V_{T,\mathrm{pr(peak)}}}{V_{\mathrm{IN}}} = \frac{1}{1-2\cdot D_{\mathrm{ST}}}. \tag{2}$$

In the case of the CSC, the idealized voltage boost is [16]

$$B_{\mathrm{CSC}} = \frac{V_{T,\mathrm{pr(peak)}}}{V_{\mathrm{IN}}} = \frac{1}{1-D_{\mathrm{ST}}}. \tag{3}$$

Results from the comparison of idealized voltage boost properties show that the voltage step-up capability of the ISC for the same shoot-through duty cycle D_{ST} is higher than that of the CSC (see Fig. 4). The twofold input voltage gain typical of the power conditioners for renewable energy sources is obtained with D_{ST} equal to 0.25 and 0.5 for the qZS-based ISC and the CSC, respectively. Since the duty cycles of the shoot-through and active states are interdependent in both topologies ($D_A = 1 - D_{\mathrm{ST}}$), this will result in higher RMS current in the isolation transformer of the CSC for the same operating conditions due to a shorter active state duty cycle D_A, which is used for transfer of the same amount of energy as in the ISC. Moreover, the ISCs have a narrower regulation range of the shoot-through duty cycle. The energy transfer in the boost mode during the active state is never less than half of the switching period. It leads to a better transformer utilization and absence of short current pulses with high amplitude, which is quite common for the CSCs regulated in a wide range. The input voltage gain of the ISC can be further improved by the cascading of the ISNs [17].

Since the operating principles are similar, the CSC faces a disadvantage of inductive overvoltages across the inverter bridge, which may lead to additional clamping circuits to be applied [18], [19]. Another issue of the CSC, the inrush current during the start-up at low output voltage, requires auxiliary start-up circuits to be implemented [20]. As a result, the introduction of these necessary auxiliary circuits significantly increases the complexity of the CSC, which finally makes it less attractive than the ISC.

Resulting from the discussion above, the main properties of the VSC, CSC, and ISC are compared in Table I. If properly implemented, the ISC may provide significant benefits over the two traditional isolated dc–dc power conversion approaches because of its regulation flexibility, power circuit versatility, and inherent reliability. On the other hand, in contrast to the popular VSC approach, the ISN will lead to higher complexity and to challenges related to efficiency, which is crucial for commercial success of the ISC technology.

TABLE I
COMPARISON OF MAIN PROPERTIES OF THE VSC, CSC, AND ISC

Property	VSC	CSC	ISC
Voltage boost	No	Yes	Yes
Voltage buck	Yes	No	Yes
Short-circuit immunity	No	Yes	Yes
Open-circuit immunity	Yes	No	Yes
Energy-storage element	One capacitor	One inductor	At least one capacitor and one inductor
Cascading of energy-storage elements	No	No	Yes
Realization and control simplicity	Simple	Complicated	Moderate

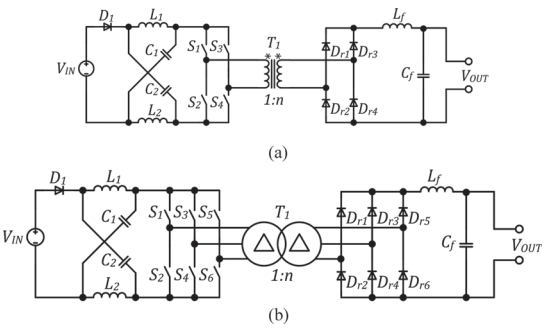

Fig. 5. State-of-the-art (a) ZSI-based single-phase and (b) three-phase galvanically isolated dc–dc converters [13], [21].

III. DEVELOPMENT OF THE IS GALVANICALLY ISOLATED DC–DC CONVERTERS

A. First Topologies

Originally, the ISC topologies can be broadly categorized as voltage fed or current fed. In terms of their simple practical realization and control, in a majority of applications, the voltage-fed approach is most popular today. The first voltage-fed IS-based galvanically isolated dc–dc converter [see Fig. 5(a)] reported in 2009 was derived from the classical voltage-source full-bridge isolated dc–dc converter by adding a ZS network to its input terminals [13]. Further improvement of the topology [see Fig. 5(b)] was connected with the modification in the intermediate high-frequency ac link, where the single-phase transformer was replaced by a three-phase one to achieve a higher power density [21]. These topologies were intended for the grid integration of low-voltage high-current fuel cells with rated power up to 10 kW.

The first IS galvanically isolated dc–dc converters presented in Fig. 5 were based on the voltage-fed ZSI; therefore, they suffered from the discontinuous input current during the shoot-through operation mode. Further progress on the IS galvanically isolated dc–dc converters was achieved by the introduction of the qZS network, which ensured a continuous input current [22]. Special shoot-through control methods used with the parasitic elements of the power circuit have led to the soft-switching qZS dc–dc converter [23].

B. Recent Development Trends

Focus today is on the efficiency and power density optimization of the IS dc–dc converters. A shift to resonant bridge with series resonant (SR) circuit, which utilizes the leakage inductance of the transformer, was proposed in [24]. This allows a considerable reduction of losses leading to a switching frequency rise and power density improvement.

Another possibility is synchronous rectification in the ISN. Preliminary results reported in [25] show the reduction of the losses in the qZS network by replacing the qZS diode with the MOSFET. It allows an efficiency rise by 2% within the qZS network. Active rectification is also possible at the voltage doubler rectifier (VDR) side. If all semiconductor components within the converter are active (e.g., MOSFETs), higher efficiency both in the VDR and IS stages as well as the controllable bidirectional operation can be achieved [26]. However, synchronous rectification requires more switches and driving circuits, as well as a complex control system with dead time implementation to avoid short-circuits [27].

New materials use is a popular trend in the modern power electronics industry. New magnetic materials can reduce the size of the ISN. Also, the new widebandgap semiconductors, like SiC and GaN, allow further loss reduction along with the switching frequency rise. GaN MOSFETs have shown good performance at the low voltage side in the PV microconverters [28]–[32]. Their utilization allows higher switching frequency; however, attention should be paid to the gate driver design and minimization of parasitic elements of the power circuit [33]–[35]. As modern SiC MOSFETs have proved their performance in high-voltage applications [36]–[40], they can be used in the synchronized VDR on the high voltage side. An appropriate selection of new widebandgap semiconductors and analysis of the benefits achieved along with economic concerns require additional research and development of new design guidelines.

C. Status of Progress

Since 2009, a number of new topologies of the IS galvanically isolated dc–dc converters have appeared, which can broadly be classified into three main groups according to the component which transfers energy from the input to the output side:

1) transformer based;
2) coupled inductor based;
3) with combined energy transfer.

The classification (see Fig. 6) is based on the operation mode of the component (components) that transfers energy from the input to the output side. In this paper, the transformer is any magnetic element that has two or more windings and operates with zero average core flux. Typical wave shapes of voltage across the winding and the core flux are shown in Fig. 7(a). During the energy transfer, the constant voltage is applied to a winding and the flux is changing with a slope that depends on the winding voltage amplitude and magnetizing inductance reflected to the same winding. Fig. 7(a) shows symmetrical

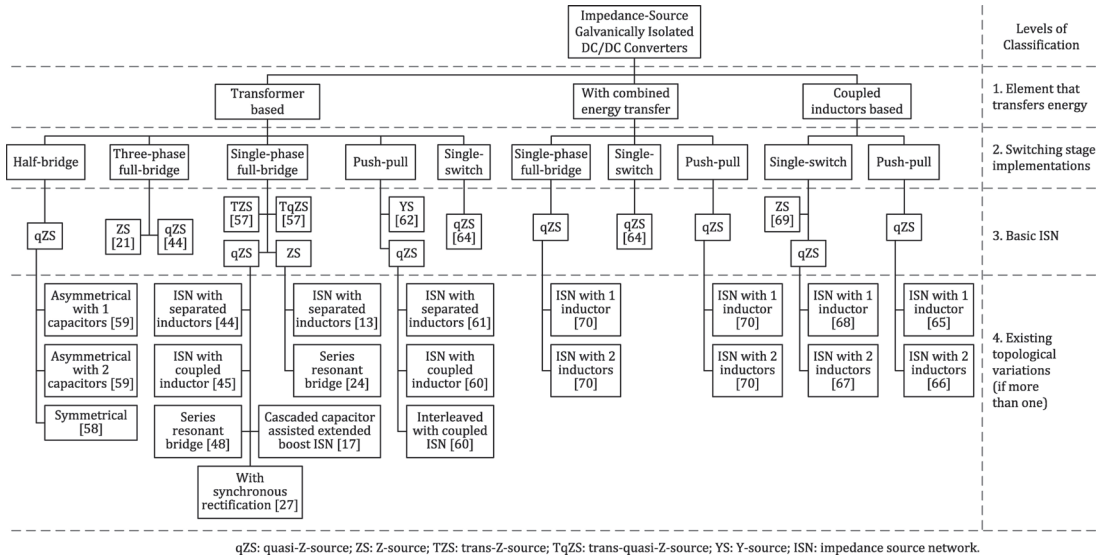

Fig. 6. Classification of the state-of-the-art IS galvanically isolated dc–dc converters.

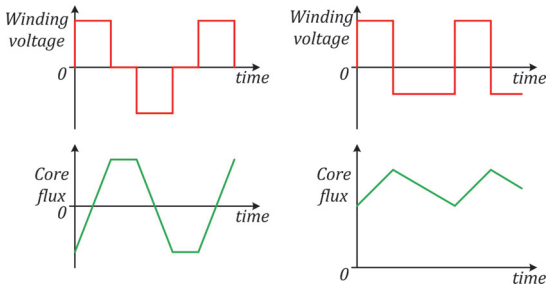

Fig. 7. Typical wave shapes of the winding voltage and core flux of: (a) transformer and (b) coupled inductor.

voltage pulses, even though they can also be asymmetrical. In this case, the volt–second balance as well as the zero average flux in the core must be maintained.

The term "coupled inductor" refers to a magnetic component with several windings and nonzero average core flux. The main difference of the coupled inductor and the transformer is in its functionality—a coupled inductor permanently stores a substantial amount of energy in the core. Fig. 7(b) shows an example of the voltage across the winding and the core flux of the coupled inductor. In a steady state, the volt–second balance must be maintained, while the voltage can either be symmetrical or asymmetrical.

The distinctive features of magnetically coupled elements are well known [41]. Despite superficial similarities between transformers and coupled inductors, these elements operate in different modes. Their construction is also different. The transformers are usually compact since the air gap in the core is small, or they are produced without it, to withstand the small unbalance of the core during regulation. Coupled inductors have to be designed with an air gap to ensure high average rated flux. Also, they are bulky and have higher leakage inductances than the transformers.

In the transformer-based IS dc–dc converters, the transformer transfers energy and ensures isolation, while inductors of the ISN only store the energy. In the coupled-inductor-based IS dc–dc converters, the coupled inductor(s) is usually a part of the ISN, and it serves not only for the energy transfer but also for the energy storage. The IS isolated dc–dc converters with combined energy transfer use both types of magnetically coupled components for energy transfer from the input to the output side.

IV. Transformer-Based IS Galvanically Isolated DC–DC Converters

This class of the ISC contains topologies that use a transformer for galvanic isolation and energy transfer. They can be divided into five basic groups:

1) with single-phase full-bridge switching stage;
2) with three-phase full-bridge switching stage;
3) with half-bridge switching stage;
4) with push–pull switching stage; and
5) with a single switch.

The first two categories can be merged into one with the full-bridge switching stage.

A. Converters With Full-Bridge Switching Stage

A generalized functional scheme for this group is shown in Fig. 8. The input part of the converter between the input terminals and the transformer is the basic structure of the IS inverter,

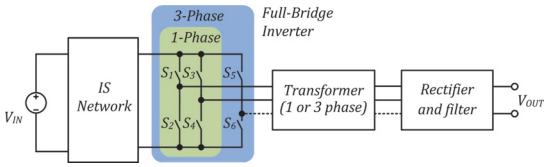

Fig. 8. Generalized functional scheme of the transformer-based IS galvanically isolated dc–dc converters with the full-bridge switching stage.

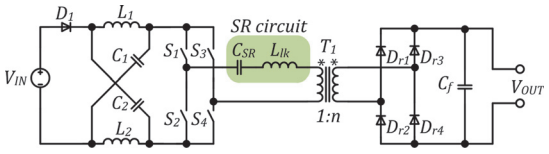

Fig. 9. ZS-based galvanically isolated SR full-bridge dc–dc converter [24].

which can have either one or three phases. These dc–dc converters consist of an IS inverter, a transformer, a rectifier, and a filter. The turns ratio n of the isolation transformer defines the range of the dc voltage gain. In this case, the ISN serves for adjusting the voltage across the transformer windings when the input voltage varies.

1) Z-Source: ZS-based converters utilize the ZS network that consists of two capacitors C_1, C_2, two inductors L_1, L_2, and a diode D_1 as shown in Fig. 5(a). The converter shown in the figure is historically the first in this group. It is based on the single-phase ZSI [13]. This converter has inherited advantages like buck–boost regulation and improved reliability and drawbacks like high component stress and discontinuous input current from the ZSI. The discontinuous input current substantially limits the application possibilities and performance of this converter. For example, it can be used with renewable energy sources, but it requires an additional filter at the input, which increases the system cost, volume, and failure rates. Also, bidirectional operation is possible in a symmetrical configuration [42], but it still has all the drawbacks of the ZSI, and the application range of such solutions is uncertain. The three-phase implementation of this converter is analyzed in [21]. In addition, an application with a distributed ZS network is discussed in [43].

The ZS-based converter with a single-phase full-bridge switching stage can easily use SR circuit in series with a transformer as shown in Fig. 9 [24]. The leakage inductance of the transformer could serve as a part of the resonance circuit, thus improving power density. In this case, the SR converter has a narrow regulation range in the frequency domain and improved buck–boost features. With the voltage buck–boost capability, the switching frequency range of ZS-based converter can be minimized to achieve higher efficiency over the entire input voltage and load variation. The converter still has a drawback of the circulating energy, while it is considerably minimized as compared to the conventional SR full-bridge converter. The reason is a narrower switching frequency regulation range. Another drawback lies in the discontinuous input current.

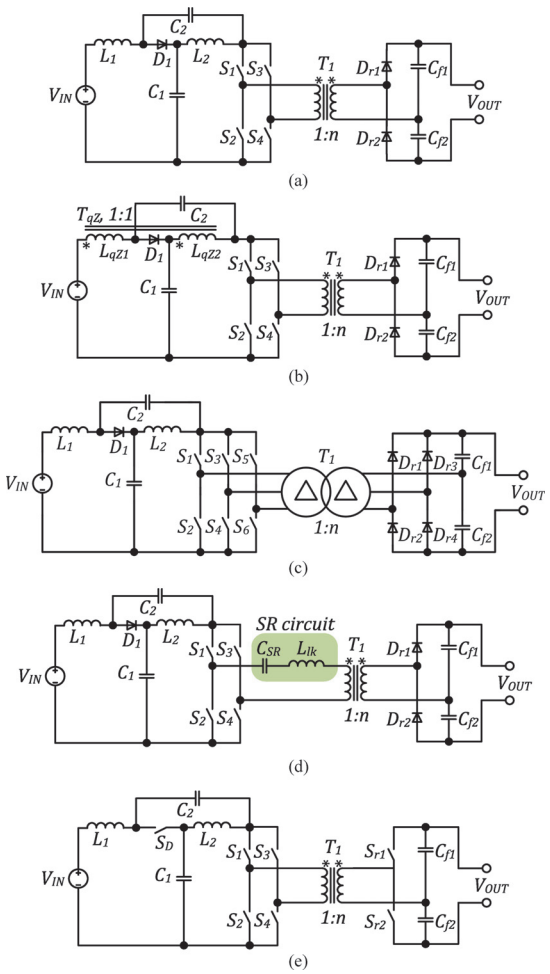

Fig. 10. qZS-based galvanically isolated full-bridge dc–dc converter with: (a) ISN with separated inductors [44], (b) ISN with coupled inductor [45], (c) with three-phase intermediate high-frequency ac link [44], (d) with SR bridge [48], and (e) with synchronous rectification [27].

2) Quasi-Z-Source: The quasi-Z-source inverter (qZSI) family was proposed in [15]. The qZSI has inherited all the advantages of the ZSI, but it has lower component stress and continuous input current. The single-phase and the three-phase qZS-based galvanically isolated dc–dc converters are proposed in [44]. Two implementations of the single-phase qZS-based ISC are shown in Fig. 10(a) and (b). In the first case, the qZS network contains the inductors L_1 and L_2 and capacitors C_1 and C_2. It is advisable to implement the qZS network with the single-coupled inductor T_{qz} [see Fig. 10(b)] in order to improve power density [45]. Advantages inherited from the qZSI make this converter a superior solution for modern distributed energy generation systems. Additional benefits are gained with the use of the VDR based on diodes D_{r1}, D_{r2} and capacitors

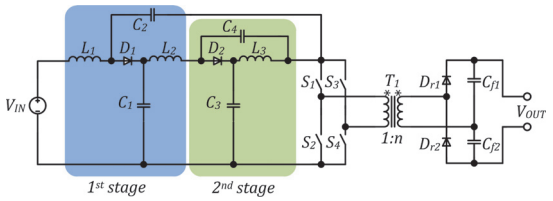

Fig. 11. Cascaded CAEB two-stage qZS-based galvanically isolated full-bridge dc–dc converter [17].

C_{f1}, C_{f2}. It is recommended to use the VDR for any step-up converter in the transformer-based group. It enables the use of the transformer with a reduced turns ratio n, which leads to lower transformer parasitic elements. The topology has demonstrated its good performance in the fuel cell applications and permanent magnet synchronous generator (PMSG)-based wind turbines [46], [47]. It is recommended to implement the topology with the three-phase intermediate high-frequency ac link [see Fig. 10(c)] for high-power applications [44].

The qZS-based galvanically isolated dc–dc converter has attracted attention of researcher because of the numerous advantages of the qZS network in power conversion. Several topological variations have been derived to further improve this topology. SR bridge to be used within this converter [see Fig. 10(d)] is proposed in [24] and discussed in [48]. Advantages of this converter are similar to those of the SR ZS converter (see Fig. 9), while it features continuous input current. When operating in the buck mode, the circulating energy could be an issue. Therefore, additional research and elaboration of detailed design guidelines are required. Also, the light-load operation may limit controllability as an inherent drawback of SR converters. Furthermore, the possible range of soft switching must be analyzed. Another possible improvement of the reference qZS-based full-bridge topology is the use of synchronous rectification. The improved topology with solely fully controlled switches shown in Fig. 10(e) allows more than 2% higher efficiency [27] because of minimized conduction losses in the qZS semiconductor element that is the major contributor of its losses [25], [49]. It can also provide the bidirectional operation without additional circuits. Moreover, the use of active VDR may result in a soft-switching operation, like in the dc–dc converters presented in [50]–[52]. Thus, additional research is required.

Another alternative to improve the qZS-based topology is to employ a cascaded qZS network. An inverter with the cascaded qZS network is proposed in [53] to further improve the step-up performance. Diode assisted and capacitor assisted families of cascaded qZS topologies have been analyzed.

Capacitor-assisted topologies have better voltage step-up performance and fewer semiconductor elements than those of the diode assisted. Therefore, the capacitor-assisted extended boost (CAEB) topologies were applied to the qZS-based galvanically isolated dc–dc converter in [17]. This topology with two qZS stages is shown in Fig. 11. Cascaded two-stage implementation of the qZS network contains two times more components and can provide a higher step-up than the ordinary qZS-based converter with the same shoot-through duty cycle. The purpose of the solution was to improve transformer utilization by narrowing the shoot-through duty cycle regulation range. In practice, additional components bring in losses and additional volume that cannot be compensated by the improvements in the transformer operation mode. The cascaded converter cannot overcome the simple qZS-based approach by its overall performance mostly due to the increased losses.

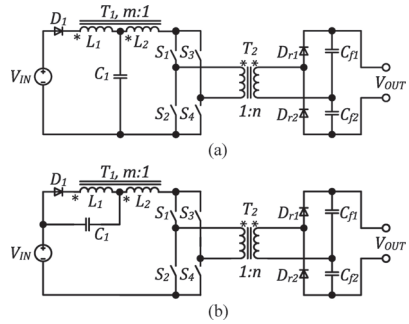

Fig. 12. (a) TZS-based and (b) TqZS-based galvanically isolated full-bridge dc–dc converters [57].

The review of the ISNs in [2] shows that only some ISNs can provide continuous input current, which is needed in most of the modern power electronics applications for distributed generation. The qZS network has a superior region of continuous input current. There are several ZS-based ISNs that have coupled inductors (with nonunity turns ratio), which influence the dc gain factor by their turns ratio m, for example: Γ-Z-source [54], trans-Z-source (TZS) [55], and Y-source (YS) [56]. They usually have discontinuous input current. Such converters have better step-up performance than the conventional ZS or qZS. In the case of the transformer-based IS galvanically isolated dc–dc converters, these networks allow dc voltage gain to be distributed between the transformer (defined by n) and the coupled inductor (defined by m). This leads to distributed parasitic elements and better switching performance.

3) Trans-Z-Source: TZS-based galvanically isolated dc–dc converter family was proposed in [57]. It consists of the TZS-based single-phase dc–dc converter and the trans-quasi-Z-source (TqZS)-based single-phase dc–dc converter shown in Fig. 12. Three-phase implementation can be easily derived from a single-phase design. In these converters, the dc voltage gain of TZS or TqZS networks depends not only on the shoot-through duty cycle but also on the turns ratio m of the coupled inductor T_1. The IS network contains fewer passive elements: one capacitor C_1, coupled-inductor T_1, and diode D_1. Both converters have discontinuous input current. Experimental verification has shown that the TqZS-based galvanically isolated dc–dc converter has lower start-up current than that of the TZS inverter based. In the future, it is required to establish the application range and detailed design guidelines of those converters.

B. Converters With Half-Bridge Switching Stage

In contrast to the full-bridge counterparts, the half-bridge IS galvanically isolated dc–dc converters feature a reduced number

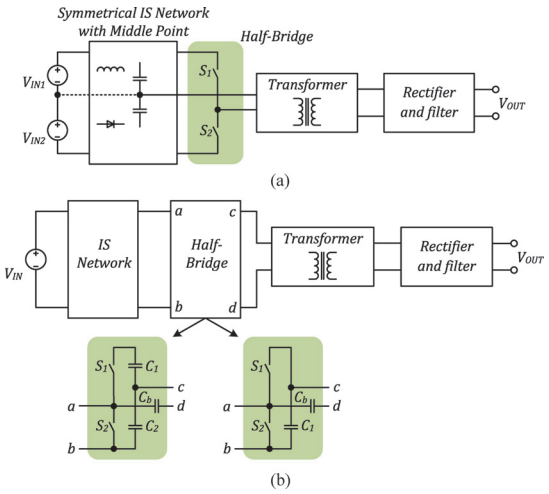

Fig. 13. Generalized functional schemes of the transformer-based IS galvanically isolated dc–dc converters with half-bridge switching stage: (a) symmetrical and (b) asymmetrical.

of switching elements. The IS galvanically isolated dc–dc converters with a half-bridge switching stage can be broadly classified into symmetrical and asymmetrical topologies. Symmetrical topologies [see Fig. 13(a)] require a symmetrical ISN structure, which must have a middle point. The half-bridge switching stage supplies a transformer with bipolar pulses of the same magnitude, and the dc blocking capacitor is generally avoided. Symmetrical converters can operate either with a single or two input voltage sources connected to the middle point of the ISN. The output voltage of the converter is controlled by the variation of the shoot-through duty cycle of the inverter similarly to the IS dc–dc converters with the full-bridge switching stage.

Asymmetrical converters can have the half-bridge switching stage of two types: with single or two capacitors [see Fig. 13(b)]. The high-side and the low-side transistors of the half-bridge inverter are driven complementary, and the dc blocking capacitor is typically required to prevent the possible saturation of the isolation transformer. The difference between the switching stages lies within the dc-link implementation and connection of the transformer to the dc link. The configuration with a single capacitor can be obtained from that with two capacitors if the top capacitor in the dc link is short circuited. The low-side transistor S_2 performs shoot-through states for dc voltage gain regulation on both types of the asymmetrical half-bridge IS galvanically isolated dc–dc converters.

1) Quasi-Z-Source: All the existing half-bridge IS galvanically isolated dc–dc converters are based on the qZS network. The symmetrical qZS half-bridge dc–dc converter (see Fig. 14) has two identical qZS networks with a neutral node n between the capacitors C_1 and C_3 [58]. Mirror connection of two qZSNs enables the symmetrical structure of the ISN. Each qZS network needs to handle half of the converter rated power. The voltage stress of the half-bridge switches equals the sum of the capacitor voltages on both qZS networks.

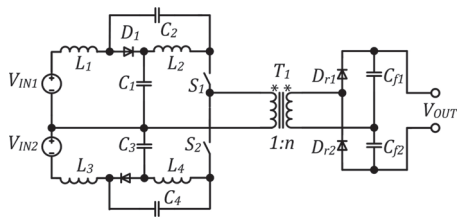

Fig. 14. qZS-based galvanically isolated symmetrical half-bridge dc–dc converter [58].

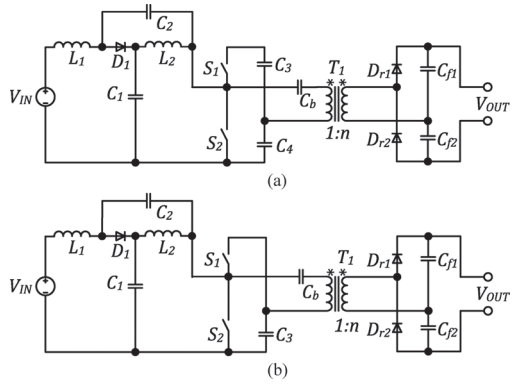

Fig. 15. qZS-based galvanically isolated asymmetrical half-bridge dc–dc converters: (a) with two capacitors and (b) with a single capacitor in the switching stage [59].

The half-bridge ISC can be simplified considerably by the implementation of the asymmetrical half-bridge concept (see Fig. 15) [59]. In that case, the high-side and the low-side switches of the half-bridge inverter are driven complimentary, and the energy is transferred through the isolation transformer TX by the asymmetrical pulses. It leads to unequal voltages across the VDR capacitors C_{f1} and C_{f2} [see Fig. 15(a)] and also requires the dc blocking capacitor C_b in series with the primary winding of the isolation transformer to prevent its possible saturation. If properly realized, the SR circuit formed by the dc blocking capacitor and primary winding leakage inductance of the isolation transformer could result in the soft switching of the half-bridge inverter switches.

The asymmetrical half-bridge topology can be simplified further by the reconfiguration of the switching stage as shown in Fig. 15(b). In general, the operating principle of the modified topology remains the same. Minimized component count will lead to higher voltage stress of the primary side capacitors C_3 and C_b. Therefore, the capacitor C_3 must be specified for the operating voltage equal to the amplitude value of the intermediate dc-link voltage. The blocking capacitor C_b needs to withstand higher dc voltage because the half-bridge switching stage supplies the transformer with unipolar voltage pulses in contrast to bipolar in the topology shown in Fig. 15(a).

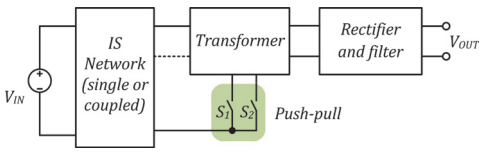

Fig. 16. Generalized functional scheme of the transformer-based IS galvanically isolated dc–dc converters with the push–pull switching stage.

In several cases, the qZS-based galvanically isolated asymmetrical half-bridge dc–dc converters can be considered as a cheaper alternative to the transformer-based ISC with a full-bridge switching stage. However, as compared to the full-bridge-based converter, the asymmetrical half-bridge topologies have only one shoot-through state per switching period. Therefore, the qZS network operates with the frequency equal to the switching frequency, and its passive components have double values as compared to those of the full-bridge counterpart.

C. Converters With Push–Pull Switching Stage

A generalized functional scheme of this group is shown in Fig. 16. This group has several advantages over the full-bridge-based converters, such as lower number of switches, simpler control, and lower conduction losses in low input voltage applications. However, the full-bridge counterparts can provide higher output power levels due to the higher number of switches. Usually, the switches work interleaved to improve the input current ripple.

1) Quasi-Z-Source: The qZS-fed push–pull converter (qZSFPPC) family has been proposed recently [60]. It is derived from the current-fed push–pull converter family by replacing the input inductor with the qZS network. Such family could be derived for almost any ISN, but almost none of them have continuous input current. This family includes the qZSFPPC and the interleaved qZS-fed push–pull converter (IqZSFPPC) that both are shown in Fig. 17. They have fewer switches than the full-bridge IS-based converters, while they provide similar performance.

The qZSFPPC [see Fig. 17(a)] employs a qZS network with a coupled inductor. It has the operation principle quite similar to that of the qZS-based full-bridge converter. The qZS-based galvanically isolated push–pull dc–dc converter with a separated inductor (see Fig. 18) is described in [61]. Its differences from the qZSFPPC lie in simpler implementation of the qZS network and worse utilization of the VDR. The IqZSFPPC [see Fig. 17(b)] contains a magnetically coupled qZS network, which can be represented as two qZS networks with full magnetic coupling within the coupled inductor T_{qZ}. In the IqZSFPPC, the leakage inductances of the coupled inductor define the input current ripple, while the magnetizing inductance defines the current ripple in the windings. This dependence implies a complicated design of the magnetic component for the IqZSFPPC.

The control principle of these converters is quite similar to the reference current-fed push–pull converter family except for the duty cycle regulation range, because of the improved voltage step-up performance. The leakage inductances are not taken into account in [60] and [61]. This means that, in practice, these converters will utilize active or passive clamping at the input side. Nevertheless, these converters are recommended for low input voltage and high input current applications because the input current loop contains only one power switch, which may assure lower conduction losses. The IqZSFPPC has more passive elements, but they are rated for lower current or voltage stress. Therefore, the final power densities of the noninterleaved and the interleaved converters can be close to each other.

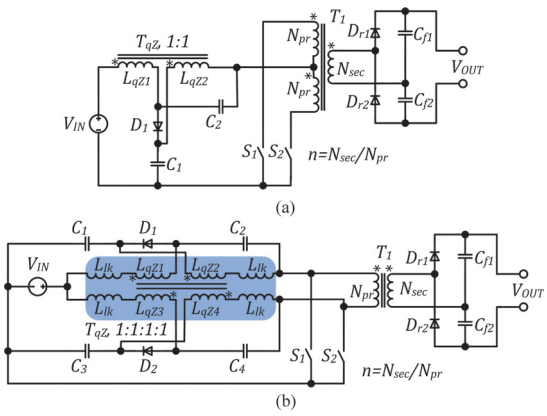

Fig. 17. qZSFPPC family [60]: (a) qZSFPPC with coupled inductors and (b) IqZSFPPC.

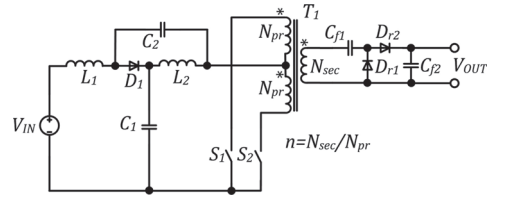

Fig. 18. qZS-based galvanically isolated push–pull dc–dc converter with separated inductors [61].

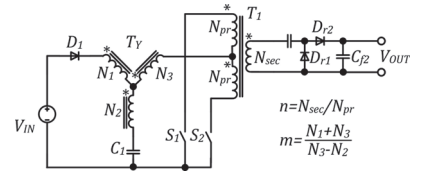

Fig. 19. YS-based galvanically isolated push–pull dc–dc converter [62].

2) Y-Source: Recent designs of IS converters are using the novel YS network [2]. A YS converter in the group of transformer-based IS galvanically isolated dc–dc converters with the push–pull switching stage is shown in Fig. 19 [62]. The YS network consists of the capacitor C_1, the coupled

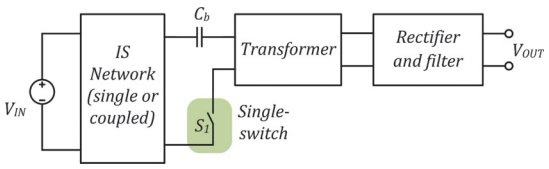

Fig. 20. Generalized functional scheme of the transformer-based galvanically isolated IS dc–dc converters with a single switch.

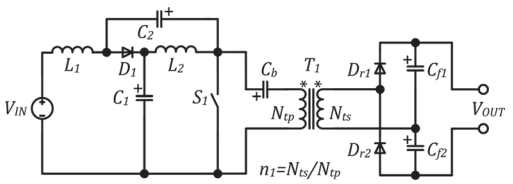

Fig. 21. qZS-based transformer-based IS galvanically isolated single-switch dc–dc converter [64].

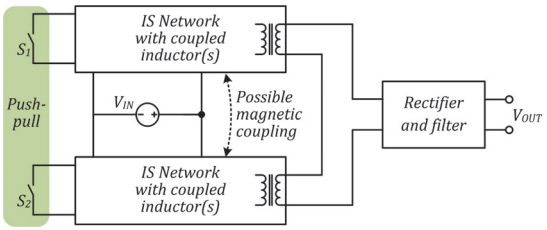

Fig. 22. Generalized functional scheme of the coupled-inductor-based galvanically isolated IS dc–dc converters with the push–pull switching stage.

inductor T_Y, and the diode D_1. That network is regarded under the group of IS networks with coupled inductors. In this case, the coupled inductor T_Y has three windings, which give some level of freedom during the design of this converter because the characteristic value *m* depends nonlinearly on the turns number of each winding. This value defines the step-up characteristic of the YS network. Also, the converter utilizes the Greinacher VDR, while the bridge VDR is commonly used and has slightly better performance [3].

According to the reports, the performance of the YS network converter is close to that of the TZS network. In addition, it suffers from voltage overshoots caused by the leakage inductances of the coupled inductor due to discontinuous input current [63] like other ISNs with a coupled inductor. Moreover, the three-winding coupled inductor is more complicated to design and more expensive than the two-winding inductor used in the TZS network. The closed-loop control of the YS-based converters and their application possibilities need comprehensive coverage. To compare the YS network with other ISNs with coupled inductors (TqZS, Γ-Z-source, etc.), analysis and experiments are required to evaluate practical application possibilities and overall performance of the YS network-based converters. From the sources available, it seems to have a good performance and versatility for inverters, while in dc–dc applications its advantages may be less apparent.

D. Converters With a Single Switch

A generalized functional scheme of this group is shown in Fig. 20. Simplest in the class of transformer-based converters, it has only one switch, and, thus, is intended for the low-power and low-voltage applications. Due to its simplicity, the ISN operates at the switching frequency of the switch. This group of converters has been proposed recently as a concept, and it needs further study to identify application possibilities and limitations imposed by the simplified switching stage.

1) Quasi-Z-Source: This group contains only one converter—the qZS-based single-switch IS converter shown in Fig. 21. Derived from a single-switch nonisolated qZS dc–dc converter [64], it comprises the qZS network, power switch S_1, isolation transformer T_1, dc blocking capacitor C_b, and VDR. Blocking capacitor is required to avoid saturation since the transformer is fed with unipolar voltage pulses. The power switch S_1 performs shoot-through states for the qZS network. The qZS network feeds the transformer T_1 with unipolar voltage pulses with varying magnitude and duty cycle. It results in unequal voltage over VDR capacitors C_{f1} and C_{f2}. Average value of the transformer input voltage is equal to the voltage across capacitor C_2, while the magnitude of the imaginary dc link is equal to the sum of qZS capacitors voltages. It means that VDR capacitors are charged to the values of the qZS capacitors voltages reflected to the output. Resonant soft switching could be achieved if the blocking capacitor is properly adjusted to form a SR circuit with the leakage inductance of the isolation transformer T_1. Advantages of that converter lie in low-power and low-voltage applications since it contains only one power switch. The switch can suffer from high current stress at a wide voltage regulation due to the short conduction state at the low dc voltage gain, since the topology requires nonzero switch duty cycle for normal operation. Additional research is required here.

V. Coupled-Inductor-Based IS Galvanically Isolated DC–DC Converters

This class of the ISC contains topologies that use a coupled inductor as a part of the ISN, as well as for the galvanic isolation and energy transfer from the input side to the output side. Those converters are not as numerous as the previous one. The first topology appeared in the literature at the beginning of 2012 [65]. During the last three years, several new converters from this class have been proposed. They can be divided into two main groups:

1) with push–pull switching stage;
2) with a single switch.

A. Converters With Push–Pull Switching Stage

This group consists of two push–pull-based converters that could be organized into one family based on the commonly used qZS network. A generalized functional scheme for this group is shown in Fig. 22.

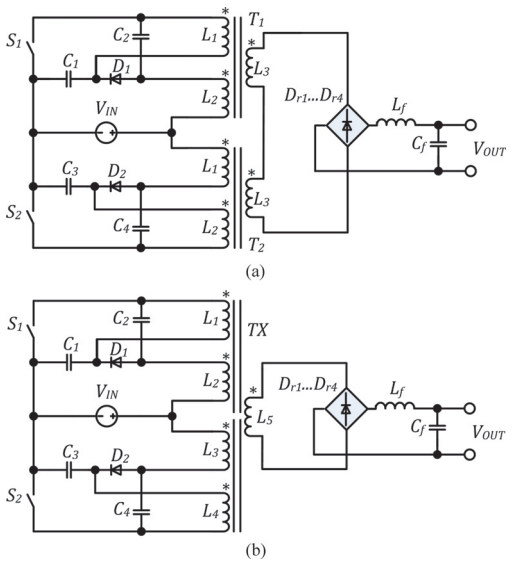

Fig. 23. qZS-based galvanically isolated push–pull dc–dc converters: (a) with two coupled inductors and (b) with a single-coupled inductor [65], [66].

1) Quasi-Z-Source: The qZS derived push–pull dc–dc converter with two coupled inductors is reported in [65] and analyzed in [66]. It consists of two qZS networks: C_1, C_2, T_1, D_1 and C_3, C_4, T_2, D_2 as shown in Fig. 23(a). Three-winding coupled inductors T_1 and T_2 provide galvanic isolation and store energy in the form of equivalent magnetizing current (i.e., flux through the core of the coupled inductors). The turn-on state of the transistors corresponds to the shoot-through behavior of the IS inverter. This converter shows good performance in wind power applications due to its wide feasible input voltage regulation range, especially for PMSG-based wind turbines. It can be also envisioned as two single-switch converters connected in parallel at the input and in series at the output, where they are sharing a common output rectifier and a filter. At low step-up, this converter transfers energy in the narrow pulses with high current amplitude, which is the main drawback that limits the practical regulation range. Flat efficiency curve at high switching frequency can be achieved in the "full-SiC" implementations [40].

Further improvement in the group of push–pull-based converters is possible through magnetic coupling of qZS networks [65]. Full coupling between T_1 and T_2 should be avoided because it leads to self-compensation of windings, and such converter is infeasible. Partial coupling is a good option that leads to a single-coupled inductor implementation of the push–pull-based topology. The qZS derived push–pull dc–dc converter with a single-coupled inductor is shown in Fig. 23(b). This topology reported in [65] looks promising, but neither studies of the design of the coupled inductor *TX* nor full design guidelines have been provided.

Both converters use a diode bridge rectifier with an output *LC* filter. These topologies require careful design to avoid high-voltage oscillation over the rectifier diodes and tertiary windings of the coupled inductors. They may appear in the topology with two-coupled inductors during the freewheeling state, when voltages across L_5 and L_6 compensate each other.

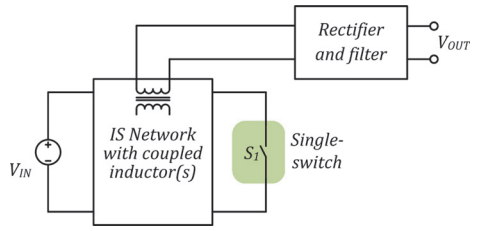

Fig. 24. Generalized functional scheme of the coupled-inductor-based galvanically isolated IS dc–dc converters with a single switch.

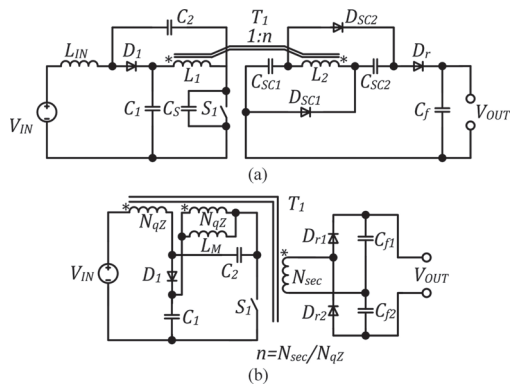

Fig. 25. qZS-based galvanically isolated coupled-inductor-based single-switch dc–dc converters: (a) with two inductors [67] and (b) with a single inductor [68].

B. Converters With a Single Switch

This group contains three recently proposed converters based on the typical qZS and ZS networks. A generalized functional scheme for this group is shown in Fig. 24.

1) Quasi-Z-Source: qZS-based single-switch converter with two inductors within the ISN has been reported in [67]. In the qZS network, the second inductor is replaced with a coupled inductor T_1 as shown in Fig. 25(a). The magnetizing inductance reflected to the primary winding serves as the part of the qZS network along with $L_{\rm IN}$ to store the energy. Inductor T_1 also provides galvanic isolation and energy transfer to the output. The output part contains the switched capacitor cell $D_{\rm SC1}$, $D_{\rm SC2}$, $C_{\rm SC1}$, $C_{\rm SC2}$ for additional voltage step-up and the rectifier D_r with the filter capacitor C_f. The output side utilizes leakage inductance of the coupled inductor as a part of the rectifier that limits the current ripple. The main advantage is that the output current ripple is reflected to the inductance L_1 in the qZS network, but does not influence the input current with low ripple. On the other hand, such implementations require two magnetic components.

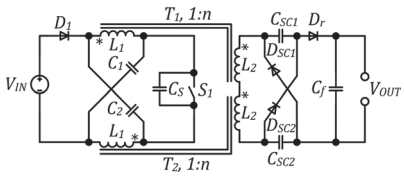

Fig. 26. ZS-based galvanically isolated single-switch dc–dc converter [69].

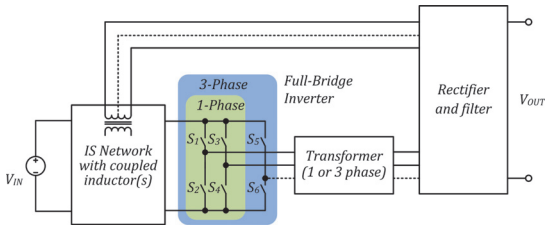

Fig. 27. Generalized functional scheme of the galvanically isolated full-bridge IS dc–dc converters with combined energy transfer.

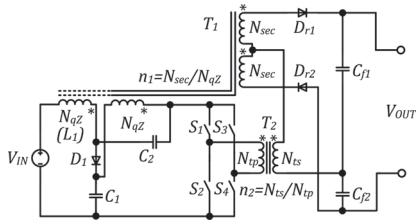

Fig. 28. qZS-based galvanically isolated full-bridge dc–dc converter with combined energy transfer [70].

Another single-switch qZS-based dc–dc converter shown in Fig. 25(b) has been derived from the qZS push–pull dc–dc converter with two coupled inductors [see Fig. 23(a)] [3], [68]. It contains only one magnetic component. In contrast to the previous qZS converter, this converter has continuous input current with higher ripple, because the reflected output current ripple is shared between the primary windings of the coupled inductor T_1. It also utilizes the bridge VDR, which provides continuous output capacitor current (only one of them charges simultaneously) and low component count. Here, the slight drawback with higher input current ripple can be neglected when the converter operates in a high step-up mode and couples the low and high voltage sides. This converter shows good performance in a wide input voltage range [68].

2) Z-Source: Another converter in this group was derived in the same manner as the qZS-based single-switch converter with two inductors [69]. Both inductors of the single-switch ZS isolated dc–dc converter are coupled to maintain a symmetrical structure of the ZS network as shown in Fig. 26. In contrast to the conventional ZS network, the current in the ZS inductors has higher ripple due to the reflection of the output current to the input side. The leakage inductance of secondary windings serves as a filter in the output side. The input current is discontinuous. As compared to single-switch qZS converters, this converter has higher stress of the elements. This topology can be improved by magnetic coupling of coupled inductors T_1 and T_2. Full coupling seems to be the best choice. In this case, the ZS network would be based on the three-winding coupled inductor that carries two times higher flux. The feasibility of such systems needs to be investigated with the VDR, which also seems to be a superior solution for the IS isolated dc–dc converters.

Coupled-inductor-based converters are more complicated to design than transformer-based converters. They have shown good performance in wind energy applications, where the input voltage varies most of all. This class of converters contains several topologies. Many novel topologies can be derived with other ISNs that have not been applied yet.

VI. IS Galvanically Isolated DC–DC Converters With Combined Energy Transfer

The latest trend of the ISCs is to use the combined energy transfer principle. Converters of this class contain coupled inductors and transformers, which allows magnetically coupled components to be used for energy transfer, and, thus, a better dc voltage gain is the result. Coupled inductors of the ISN contain additional winding(s) for energy transfer to the output side. Several secondary windings are connected to the rectifier and filter at the output side. They provide additional output voltage, and, thus, improve the voltage step-up operation of the ISC. First topologies were proposed in [70]. This class presents the same categories at the second level of classification as the transformer-based converters because of similar switching stages. All the converters reported in [64] and [70] are based on the qZS network and represent three basic groups:

1) with single-phase full-bridge switching stage;
2) with push–pull switching stage;
3) with a single switch.

This solution is versatile because the dc voltage gain and energy transfer distribution between the magnetic elements could be defined by two turns ratios.

A. Converters With Full-Bridge Switching Stage

This group of converters can be described by the generalized functional scheme shown in Fig. 27. The concept is based on the combination of the transformer-based converters with the full-bridge switching stage and a coupled-inductor-based converter with a single switch. Switching stage could be implemented using a single-phase and a three-phase configuration. The single-phase configuration seems to be simpler and more attractive in practice.

1) Quasi-Z-Source: The qZS ISC shown in Fig. 28 was proposed in [70]. The coupled-inductor T_1 in the qZS network contains two additional windings connected in series with the output winding of the isolation transformer T_2. Each secondary

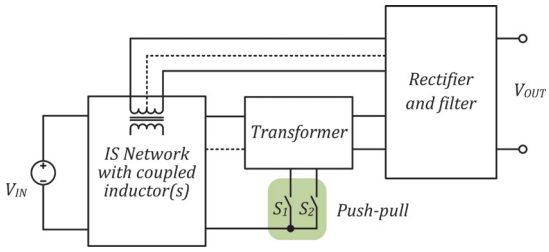

Fig. 29. Generalized functional schemes of the galvanically isolated IS push–pull dc–dc converters with combined energy transfer.

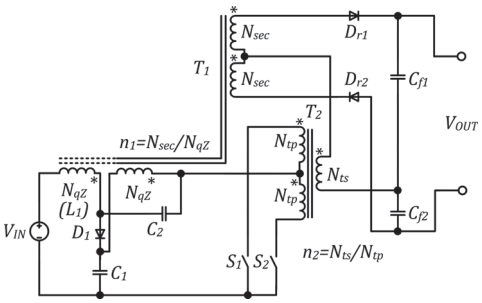

Fig. 30. qZS-based galvanically isolated push–pull dc–dc converter with combined energy transfer [70].

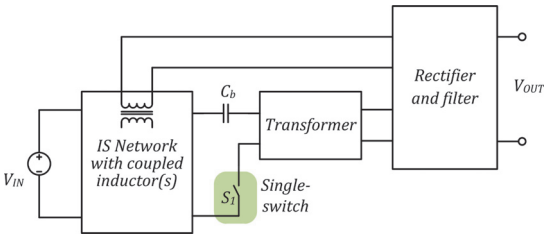

Fig. 31. Generalized functional scheme of the galvanically isolated IS single-switch dc–dc converters with combined energy transfer.

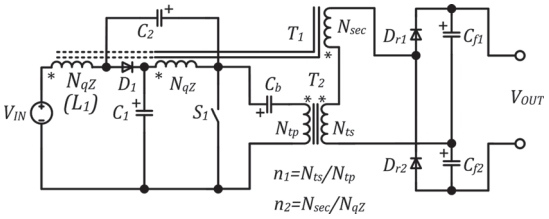

Fig. 32. qZS-based galvanically isolated single-switch dc–dc converter with combined energy transfer [64].

winding feeds the VDR together with the secondary winding of the transformer T_2 during active state in the inverter bridge. The proposed connection of the output windings allows the use of a single VDR. Filter capacitors are charged symmetrically. The voltage of the capacitors C_{f1} and C_{f2} is equal to the sum of the capacitors C_1 and C_2 voltage reflected through the transformer T_2 and the voltage of the capacitor C_2 reflected through the coupled inductor T_1. This topology has two variations: when input inductor is part of T_1, and when it is discrete. In the first case, the input inductor is implemented as the fourth winding of the T_1 with N_{qZ} turns number. Another option is to use a discrete inductor L_1 at the input along with a three-winding coupled inductor in the qZS network. The first topology with a single magnetic component in the IS network is simpler, but has higher input current ripple. The other one with two magnetic components in the qZS network is more complicated, but the input current has lower ripple.

B. Converters With Push–Pull Switching Stage

This group is also based on the combined features of the coupled-inductor topologies with a single switch with those of the transformer-based topologies with a push–pull switching stage (see Fig. 29). Converters within this group operate similarly to those from the previous group.

1) Quasi-Z-Source: Only two topologies based on the qZS network exists in this group (see Fig. 30) [70]. Voltages of the output windings are similar to the previous case. Topological variations are revealed in the implementation of the input inductor. It can be used as a fourth winding of T_1 with a N_{qZ} number of turns, or as a discrete inductor L_1. The input current ripple is higher in the first case, while the second case requires more passive elements.

C. Converters With a Single Switch

Further simplification of the switching stages has led to IS galvanically isolated single-switch dc–dc converters with combined energy transfer. The generalized functional scheme is shown in Fig. 31. It is derived by combining a transformer-based and a coupled-inductor-based single-switch converter. Overall performance of these converters is limited by the power processing capabilities of a single switch.

1) Quasi-Z-Source: The qZS-based converter from this group is an improved transformer-based single-switch topology presented in [64]. The qZS network allows a simple integration of the output windings as shown in Fig. 32. It is achieved due to equal voltages across the input windings of the coupled inductor T_2 and isolation transformer T_1. Here, coupling of the input inductor is also optional. In the simplest case, when a coupled inductor is placed instead of the right qZS inductor, the current ripple of the output windings will be reflected to the qZS network through T_2. It means that the relation between the turns ratios n_1 and n_2 requires additional research to avoid possible discontinuous conduction mode in the input winding of the inductor T_2. The main drawback of this topology is the limited power rating of a single switch, especially when it suffers from high current pulses at the low dc voltage gain. It requires nonzero switch duty cycle to provide voltage at the output.

ISCs topologies with combined energy transfer are brand new and have not been verified experimentally. Furthermore, only qZS-based converters have been proposed in this group. Further research could focus on the application of different ISNs to this concept, as well as on the analysis of the influence of the parasitic components and experimental verification for certain case study systems. It will help to define their overall performance and application range.

VII. Classification and Comparison of IS Galvanically Isolated DC–DC Converters

All the reviewed topologies can be considered as basic topologies. Many other converters could be derived from them by parallel connection of basic topologies without magnetic coupling [71], or with magnetic coupling between ISNs [71], [72]. These basic topologies could be used in different parallel–series energy conversion systems [68], [73]. The implementation of the secondary side with active switches allows bidirectional operation of basic topologies [26], [42].

A. Classification of IS Galvanically Isolated DC–DC Converters

To clarify the derivation process and show the potential gray areas, the existing converters were classified. The reason is that in the classification of ISNs in [2], the essence of the IS dc–dc electric energy conversion remains uncovered and some topologies are neglected. Use of ISNs as the main factor of classification is not a benefit due to their spreading high variety. For example, two novel passive ISNs have been proposed recently: L-Z-source [74] and sigma-Z-source [75]. Also, active ISNs are becoming popular [76], [77]. Moreover, most of the ISNs can be further modified using switched-inductor and switched-capacitor cells [78] or voltage-lift technique [79] to improve the voltage step-up characteristic, or using passive LC- [80], [81] or C-filers [82] to achieve continuous input current. Hence, ISN could not be used as a major factor for classification.

The first level in the classification is based on the energy transfer principle: energy could be transferred from the input to the output side through a transformer, coupled inductor, or based on the combined energy transfer principle. This factor has advantages over the switching stage type since it contains fewer groups, and, thus, results in a better hierarchical structure. Also, the single-switch switching stage is applicable for any type of energy conversion within the IS converters reviewed, while it is impossible to apply each energy conversion type to any type of switching stage.

The second level of classification is based on the implementation of the switching stage. The third level of classification shows the ISNs applied to the basic structures shown in Figs. 8, 13, 16, 20, 22, 24, 27, 29, and 31. The fourth level is used to indicate topological variations of the basic principle defined by the previous three levels. The classification of the state-of-the-art IS galvanically isolated dc–dc converters is shown in Fig. 6. The first two levels define only ten basic principles. Only one or two ISN types were applied to nine of them. This provides further research space for applications of other ISNs.

The converters based on the single-phase qZSI have been studied most extensively. This group has the widest topological variations. The single-phase IS inverter-based group contains more topologies than other groups. The reason is that this derivation principle is natural and the simplest. Numerous IS inverters have been comprehensively investigated. Many of these results could be reused in the dc–dc converter design. The classification proposed shows wide prospects for research of new IS galvanically isolated dc–dc converter topologies on the third and fourth level of the classification. Focus should be on the utilization of ISNs and their topological variations. Furthermore, an extension of the classification at the second level is possible. The application of different switching stages in the class of ISC with combined energy transfer is the most obvious.

Therefore, it is concluded that the proposed classification is versatile, and could be used as a basis for future derivation and systematization of novel IS galvanically isolated dc–dc converters.

B. Control, Application Possibilities, and General Comparison of the IS Galvanically Isolated DC–DC Converters

Table II summarizes all the reviewed basic topologies from the family of IS galvanically isolated dc–dc converters. Thirty topologies are compared according to the number of passive and semiconductor components, and maximum switch duty cycle. In addition, advantages and drawbacks are pointed out. Special attention has been paid to dc voltage gain in the boost mode, since this mode is most common in the reported case study systems. All the expressions are provided for lossless idealized converters. Basic strategies of switching control for the topologies reviewed are shown in Fig. 33 and referenced in Table II to explain the dc voltage gain expressions. In the topologies with symmetrical PWM control, like full-bridge or push–pull, maximum duty cycle of a switch could be related to any switch in the switching stage. Otherwise, it is related to a switch that generates the shoot-through states at the output terminals of an ISN—switch S_2 in the case of the asymmetrical half-bridge IS galvanically isolated dc–dc converters. Maximum duty cycle of a switch depends also on the type of the ISN, especially in the case of the magnetically coupled ISN, where the turns ratio m defines the operation range of the duty cycle referred to the switching period T.

The simple switching control strategies shown in Fig. 33 describe the basic operation of the topologies reviewed. The single-phase full-bridge topologies can be controlled with the symmetrical overlap strategy [see Fig. 33(a)]. It fits also the majority of push–pull converters and symmetrical half-bridge converters since they require only control of two switches S_1 and S_2 with the same sequence. Apparently, the operating frequency of the ISN as well as the frequency of the input current ripple is twice the transistor switching frequency. It could be extended to a three phase as shown in Fig. 33(b), the three-phase bridge operates without zero states, while additional shoot-through states are added at the switching transitions of each leg. It results in sixfold operation frequency of the ISN and high utilization of

TABLE II
COMPARISON OF BASIC TOPOLOGIES OF THE IS GALVANICALLY ISOLATED DC–DC CONVERTERS

TOPOLOGY	MAXIMUM DUTY CYCLE OF A SWITCH	DC VOLTAGE GAIN IN BOOST MODE (CONTROL)	NO. OF SC*		NO. OF MC*			NO. OF C*	PROS (+) AND CONS (-)
			D*	S*	L*	CL*	TR*		
TRANSFORMER BASED									
qZS symmetrical half-bridge converter [58] (Fig. 14)	0.75	$\frac{n}{(1-2\cdot D_S)}$ (Fig. 33*a*)	4	2	4	0	1	6	+ double input possibility + low number of switches + continuous input current - high number of passive components - high voltage stress of switches
qZS asymmetrical half-bridge converter with 1 capacitors [59] (Fig. 15*b*)	0.5 (S_2 on Fig. 15)	$\frac{n}{(1-2\cdot D)}$ (Fig. 33*c*)	3	2	2	0	1	6	+ low number of components + continuous input current - DC blocking capacitor is needed - uneven loading of switches - high voltage stress of switches
qZS asymmetrical half-bridge converter with 2 capacitors [59] (Fig. 15*a*)			3	2	2	0	1	7	
qZS single-switch converter [64] (Fig. 21)	0.5	$\frac{n}{(1-2\cdot D)}$ (Fig. 33*e*)	3	1	2	0	1	5	+ low number of components + continuous input current - DC blocking capacitor is needed - high stress of a switch
ZS three-phase full-bridge converter [21] (Fig. 5*b*)	0.75	$\frac{2\cdot n}{(1-2\cdot D_S)}$ (Fig. 33*b*)	7	6	3	0	1	3	+ better power density - limited performance due to LC filter - discontinuous input current - high number of SCs
qZS three-phase full-bridge converter [44] (Fig. 10*c*)			5	6	2	0	1	4	+ better power density + continuous input current - high number of SCs
TZS single-phase full-bridge converter [57] (Fig. 12*a*)	$0.5+\frac{1}{2\cdot(1+m)}$	$\frac{2\cdot n}{(1-(1+m)\cdot D_S)}$ (Fig. 33*a*)	3	4	0	1	1	3	+ high voltage step-up at the input stage + low number of passive components - high voltage stress of switches - discontinuous input current
TqZS single-phase full-bridge converter [57] (Fig. 12*b*)			3	4	0	1	1	3	
ZS single-phase full-bridge converter with separated inductors [13] (Fig. 5*a*)	0.75	$\frac{n\cdot(1-D_S)}{(1-2\cdot D_S)}$ (Fig. 33*a*)	5	4	3	0	1	3	- discontinuous input current - limited performance due to LC filter
ZS single-phase series resonant full-bridge converter [24] (Fig. 9)	0.75	$\frac{n}{(1-2\cdot D_S)}$ (Fig. 33*a*)	5	4	3	0	1	4	+ resonant soft switching + high power density - complicated control - discontinuous input current
qZS single-phase full-bridge converter with separated inductors [44] (Fig. 10*a*)	0.75	$\frac{2\cdot n}{(1-2\cdot D_S)}$ (Fig. 33*a*)	3	4	2	0	1	4	+ continuous input current - relatively high number of PCs*
qZS single-phase full-bridge converter with coupled inductor [45] (Fig. 10*b*)	0.75		3	4	0	1	1	4	+ continuous input current + magnetically integrated ISN - relatively high number of PCs*
qZS single-phase series resonant full-bridge converter [48] (Fig. 10*d*)	0.75		3	4	3	0	1	5	+ continuous input current + resonant soft switching - variable frequency control
qZS single-phase full-bridge converter with synchronous rectification [27] (Fig. 10*e*)	0.75 (S_1…S_4) 1.0 (S_D) 0.5 (S_{r1}…S_{r2})		0	7	2	0	1	4	+ low losses and high power density + continuous input current - high number of SCs - lower reliability
Cascaded CAEB qZS single-phase full-bridge converter [17] (Fig. 11)	2/3	$\frac{2\cdot n}{(1-3\cdot D_S)}$ (Fig. 33*a*)	4	4	3	0	1	6	+ continuous input current + high voltage step-up at the input stage - high number of passive components
YS push-pull converter [62] (Fig. 19)	$\frac{(1+m)}{2\cdot m}$	$\frac{2\cdot n}{(1-m\cdot D_S)}$ (Fig. 33*a*)	3	2	0	1	1	3	+ high voltage step-up at the input stage + low number of components + magnetically integrated ISN - complicated design of ISN - discontinuous input current - high voltage stress of switches - three-winding transformer

TOPOLOGY	MAXIMUM DUTY CYCLE OF A SWITCH	DC VOLTAGE GAIN IN BOOST MODE (CONTROL)	NO. OF SC*		NO. OF MC*			NO. OF C*	PROS (+) AND CONS (-)
			D*	S*	L*	CL*	TR*		
qZS push-pull converter with separated inductors [61] (Fig. 18)	0.75	$\frac{2 \cdot n}{(1-2 \cdot D_S)}$ (Fig. 33a)	3	2	2	0	1	4	+ low number of SCs + continuous input current - high voltage stress of switches - three-winding transformer
qZS push-pull converter with coupled inductor [60] (Fig. 17*a*)	0.75		3	2	0	1	1	4	+ low number of SCs + continuous input current + magnetically integrated ISN - high voltage stress of switches - three-winding transformer
Coupled qZS interleaved push-pull converter [60] (Fig. 17*b*)	0.5	$\frac{2 \cdot n}{(1-2 \cdot D)}$ (Fig. 33*d*)	4	2	0	1	1	6	+ low number of SCs + continuous input current - complicated design of ISN - high voltage stress of switches - high number of passive components
COUPLED INDUCTOR BASED									
ZS single-switch converter [69] (Fig. 26)	0.5	$\frac{2 \cdot n \cdot (1+D)}{(1-2 \cdot D)}$ (Fig. 33*e*)	4	1	0	2	0	6	+ single switch - discontinuous input current - high number of semiconductor components
qZS single-switch converter with a single inductor [68] (Fig. 25*b*)	0.5	$\frac{n}{(1-2 \cdot D)}$ (Fig. 33*e*)	3	1	0	1	0	4	+ single switch + high magnetic integration + continuous input current
qZS single-switch converter with two inductors [67] (Fig. 25*a*)	0.5	$\frac{2 \cdot n \cdot (1+D)}{(1-2 \cdot D)}$ (Fig. 33*e*)	4	1	1	1	0	6	+ single switch + continuous input current - high number of components
qZS push-pull converter with a single inductor [66] (Fig. 23*b*)	0.5	$\frac{2 \cdot n \cdot D}{(1-2 \cdot D)}$ (Fig. 33*d*)	6	2	1	1	0	5	+ continuous input current + high magnetic integration of ISN - limited performance due to LC filter - high number of components
qZS push-pull converter with two inductors [65] (Fig. 23*a*)	0.5		6	2	1	2	0	5	+ continuous input current - limited performance due to LC filter - high number of components
WITH COMBINED ENERGY TRANSFER									
qZS single-phase full-bridge converter with a single inductor [70] (Fig. 28)	0.75	$2 \cdot \frac{n_1 \cdot D_S + n_2}{(1-2 \cdot D_S)}$ (Fig. 33*a*)	3	4	0	1	1	4	+ high magnetic integration of ISN + additional voltage step-up + continuous input current - complicated design of CL - high input current ripple
qZS single-phase full-bridge converter with two inductors [70] (Fig. 28)			3	4	1	1	1	4	+ additional voltage step-up + continuous input current - complicated design of CL
qZS push-pull converter with a single inductor [70] (Fig. 30)			3	2	0	1	1	4	+ high magnetic integration of ISN + additional voltage step-up + continuous input current - complicated design of CL - high input current ripple
qZS push-pull converter with two inductors [70] (Fig. 30)			3	2	1	1	1	4	+ additional voltage step-up + continuous input current - complicated design of CL
qZS single-switch converter with a single inductor [64] (Fig. 32)	0.5	$\frac{(n_1+n_2)}{(1-2 \cdot D_S)}$ (Fig. 33*e*)	3	1	0	1	1	5	+ high magnetic integration of ISN + additional voltage step-up + continuous input current - high stress of a switch - high input current ripple
qZS single-switch converter with two inductors [64] (Fig. 32)	0.5		3	1	1	1	1	5	+ additional voltage step-up + continuous input current - high stress of a switch

*SC – semiconductor component; MC – magnetic component; D – diode; S – switch; L – inductor; CL – coupled inductor; TR – transformer; C – capacitor; PC – passive component.

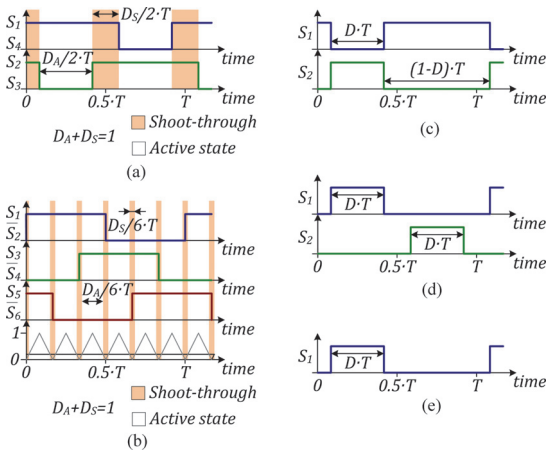

Fig. 33. Simplified switching control strategies for: (a) single-phase full-bridge, symmetrical half-bridge, and majority of push–pull topologies, (b) three-phase full-bridge topologies, (c) asymmetrical half-bridge topologies, (d) interleaved push–pull topologies, and (e) single-switch topologies.

the isolation transformer in high-power applications. Overlap of switches control signals is not required in interleaved topologies, transformer-based interleaved push–pull and coupled-inductor-based push–pull, since switches perform short-circuiting of the ISN output terminals directly. In this case, interleaved control [see Fig. 33(d)] with 180° phase shift results in lower input current ripple and ISN operating frequency doubling. Asymmetrical half-bridge topologies require asymmetrical control [see Fig. 33(c)], while single-switch topologies utilize simple control [see Fig. 33(e)] where the duty cycle of the switch is limited (see Table II). These topologies with reduced number of switches have reduced operating frequency of the ISN, which is equal to the transistor(s) switching frequency.

The converters reviewed reveal their advantages in applications where a wide input voltage regulation range is required. Recent areas mostly include renewable and alternative energy applications. Usually it means low-voltage input and handling relatively high current. Most of the ISNs have a diode that results in relatively high losses at the input side. Maximum reported peak efficiency is in the range of 96%–97% [24], [61], [62]. It is mostly measured without voltage step-up at the input side, i.e. at maximum rated input voltage. Regulation range is usually limited with an efficiency drop and is often within the range 1:3 for simpler ISNs and a slightly wider range for those magnetically coupled. At maximum voltage step-up, i.e., minimum rated input voltage, the efficiency could drop to 85%, depending on the application and the hardware used. This trend is the same for transformer-based and coupled-inductor-based converters, and, thus, the efficiency of converters with combined energy transfer is in the same range too. Recently several approaches, like series resonance and synchronous rectification, have been proposed to reduce power loss. Synchronous rectification in the ISN is most advantageous among the results reported. Further efficiency improvement could be achieved with soft switching in power switches. Efficiency optimization is a crucial issue for power electronics systems and further studies of IS converters are required. Apparently, there is still a room for improvement in the new field of IS dc–dc converter technology.

Application possibilities for IS dc–dc converters need further examination, since reports on case study systems are scarce. In most of the examples available, emerging applications of the single-phase full-bridge qZS converter are numerous. However, it is not an appropriate conclusion that ISCs can be used only with low-voltage input. Application examples that contain experimental verification are described below for all the applications reported.

The area of *wind energy* has benefited from two different types of IS converters. It is one of the most demanding renewable energy applications due to a wide range of output voltage variations of the wind turbine, especially for those based on PMSG. The transformer-based qZS full-bridge dc–dc converter has been used together with an active rectifier in the interface converter for residential PMSG-based wind turbines with a rated power of 1.3 kW [47]. The total voltage gain of the interface converter was distributed between the input side active rectifier and the qZS converter. The active rectifier was used to stabilize the first dc-link voltage at low wind speeds at the level of 150 V, while uncontrolled rectification was performed at higher wind speeds when the generator is able to provide dc-link voltage higher than 150 V. The qZS converter was used to stabilize the second dc-link voltage, which feeds the grid-side inverter at the level of 250 V. It means that the transformer-based qZS full-bridge converter was operating at a voltage boost lower than twofold, which is within the recommended range of 1:3. Application of the coupled-inductor-based qZS push–pull converter together with the uncontrolled six-pulse three-phase diode rectifier to exactly the same wind turbine was described in [83]. The qZS converter there covers the whole operating voltage range of the wind turbine from 65 to 259 V in the boost mode only. Hence, the coupled-inductor qZS push–pull converter has shown an ability to operate in the range of 1:4. Its operation in the range from 40 to 400 V is described in [3], where efficiency higher than 90% was achieved for the 1:4 input voltage range from 100 to 400 V at the maximum input current. High efficiency at the switching frequency of 100 kHz was assured by the SiC devices, which are essential to realize the high-frequency high-voltage IS converters [40]. The coupled-inductor topology has used nearly the same inductance in the qZS network (1 mH) as the transformer-based counterpart, while the input current ripple was higher due to the different operating principle, but this is not a weighty disadvantage since the dc-link capacitor on the generator side decouples current ripple from the generator. However, the design and operation principle of the coupled-inductor-based qZS topology is more complicated, and, thus, more efforts may be required to build such systems.

Photovoltaic power generation systems are also an attractive area of application for the IS dc–dc converters. For example, a microconverter realized with the transformer-based qZS symmetrical half-bridge topology was proposed in [58] for integration of single or two PV panels into the common dc bus. The concept was verified for operation at constant input current 5 A

and input voltage range from 30 to 58 V, i.e., the rated power is 300 W. Such operating conditions with constant input current are common for PV maximum power point trackers when the input voltage of the converter changes with the PV panel temperature, while the input current remains nearly constant at the same irradiation. The obtained efficiency was around 92% at the switching frequency 100 kHz, since no optimization of losses was involved.

Fuel cells are more demanding than photovoltaic and wind turbine applications. They provide maximum output power at the minimum output voltage, while renewable applications usually provide maximum output power at the maximum output voltage. An industrial converter based on the galvanically isolated qZS full-bridge dc–dc converter is proposed for proton exchange membrane fuel cells with power up to 8 kW in [84]. It was created in cooperation between the Tallinn University of Technology and industrial partners. The grid-connected interface performs energy conversion in two stages. The first stage contains two qZS full-bridge converters that operate in parallel with interleaved control and stabilize dc-link voltage at the level of 600 V. Stable voltage is used to supply the grid-side three-phase inverter at the second stage. The input voltage range is from 35 to 64 V, while the input current can reach up to 230 A. The peak efficiency achieved was around 96%.

Power factor corrector (PFC) based on the galvanically isolated qZS full-bridge topology with rated power of 1 kW was proposed in [85]. It supplies load with 380 V dc voltage from 230 V/60 Hz grid voltage, which is rectified by a single-phase bridge diode rectifier. The PFC was designed to operate with 20% input current ripple at the switching frequency of 50 kHz, which results in the 1 mH value of qZS network inductors. This allowed 4.4% of grid current THD to be achieved at full power with an efficiency of 93%.

All the examples for application described above prove high versatility of the IS dc–dc electric energy conversion technology. It can handle different levels of power and input voltage. However, not all of the topologies reviewed in this paper were verified experimentally. Only a few of them were used in practical applications reviewed above. It means that more application oriented research is required to find out applications advantageous for each class of the converters reviewed and define their limitations. As for now, the qZS full-bridge topology was applied to most of the emerging applications and can be selected by engineers to minimize risks regarding the implementation of new topologies in the industrial products.

The main tendency for topology selection at the required power level is the same as for conventional VSCs and CSCs; more complicated topologies with higher number of switches, like full-bridge, fit better for high power applications. For example, push–pull topologies could be used up to medium power levels or for high-current applications, where the number of switches increases the conduction losses. Low power applications benefit from simple topologies, like that with a single switch. Among the three proposed classes of converters, the transformer-based converters cover the whole power range, while they have a simple design procedure. As for now, the coupled-inductor-based converters have been tested only for low power applications (up to 1.5 kW), and, thus, cannot be recommended for higher power levels. The converters with combined energy transfer have not been reported for any applications. They seem to be useful for different power ranges due to the possibility to utilize various switching stage types, but this is not proven yet. Also, they could be applied where a wide input voltage regulation range is necessary if experimental verification proves theoretical predictions. According to design complexity, the transformer-based converters are the simplest, while the coupled inductor based could take more efforts. In terms of design, the converters with combined energy transfer could be most complicated, since it is required to design both an isolation transformer and a coupled inductor and select the right proportion between their turns ratios, while better dc voltage gain could be achieved.

The application of magnetically coupled ISNs, like qTZS or Γ-source, in dc–dc converters needs a separate coverage. They have high performance in inverter use due to high dc voltage gain that leads to smaller loss of the modulation factor control range. This feature is not essential for dc–dc converters in most of the cases, since the main voltage step-up is usually obtained with a transformer and an output rectifier. The ISN is mostly used to adjust the transformer voltage when the input voltage varies. However, the magnetically coupled ISNs could be advantageous in specific applications. For example, the YS push–pull converter could be beneficial in applications with very low input voltage and relatively high input current. In this case, the transformer design could be complicated if a simpler ISN is used. The input voltage could be preadjusted with the YS network up to an acceptable level, while the push–pull switching stage provides low conduction losses with high input current.

In Table II, the converters reviewed are compared on the basis of the qZS full-bridge topology with separated inductors mostly due to their continuous input current, which is highly demanded for emerging applications. They have no obvious disadvantages revealed from the comparison with other converters. Their disadvantages, like relatively low efficiency and higher number of components as compared to VSCs and CSCs, are common for all converters from this review and balanced with improved regulation range and reliability. Data in Table II prove that the basic topology selected could be a preferable solution for emerging applications.

VIII. Conclusion

The modern renewable energy market requires versatile power electronics solutions. The review in this paper reveals that the qZS-based galvanically isolated dc–dc converters can be further developed as the basic power electronics building blocks for dispersed generation systems.

The proposed classification of the isolated IS dc–dc converters shows numerous gaps in this field mostly related to the application of certain ISN to the generalized topology structure or application of another switching stage to a certain energy transfer principle. It could be concluded that converters from the transformer-based class are simpler to design, more

flexible, and have a wider application range. Coupled-inductor-based topologies are more complicated to design and control and less effective, but they show better performance where a wide voltage regulation range is needed. They are required only in some applications with wide input voltage variations, for instance, in PMSG-based wind turbines. The converters with combined energy transfer proposed recently require extensive research.

Numerous further research areas are indicated in this paper. Ten generalized functional schemes proposed can be used to understand the derivation process of the IS galvanically isolated dc–dc converter topologies or as a derivation tool.

Finally, it is concluded that broadly, the qZS-based converters have advantages over other IS topologies for emerging applications. Further directions to improve those converters were discussed. Main directions for future research are the resonant implementations, active rectification in the input and the output sides, bidirectional operation, and also the use of new materials and semiconductors, which might give a new paradigm of converter design.

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Asymmetrical Quasi-Z-Source Half-Bridge DC-DC Converters

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***Abstract*— This paper presents a novel quasi-Z-source half-bridge DC-DC converter family derived by a combination of the single-switch qZS DC-DC converter and the half-bridge galvanically isolated DC-DC converter. The novel topologies have only two active switches and are a cheaper alternative to the galvanically isolated quasi-Z-source DC-DC converters with a full-bridge switching stage. Such promising features as circuit simplicity, low cost, high efficiency, and high reliability are attributed to the new alternative solution. A 200W prototype was assembled and tested. Simulation and experimental results are presented to verify the step-up performance of the topology.**

Keywords*— *impedance-source converters, DC-DC power converters, galvanic isolation, renewable energy sources

I. INTRODUCTION

The quasi-Z-source (qZS) full-bridge DC-DC converter (Fig. 1) is a new emerged topology of the galvanically isolated step-up DC-DC converters [1]. Its specific properties, such as continuous input current, wide input voltage and load regulation range, increased reliability and inherent soft-switching properties, have contributed to the popularity of the topology in the renewable energy applications as power conditioners for the fuel cells [2], PV panels [3] and residential wind turbines [4]. Since its appearance in 2009, increasing research efforts in the field of qZS DC-DC converters have been made. New approaches, such as cascaded qZS-network [5], advanced shoot-through control methods [6], synchronous rectification [7], and resonant power conversion [8], are targeting improved step-up performance and efficiency of the baseline topology. Moreover, two new topologies of the magnetically coupled qZS DC-DC converters with reduced number of switches were developed: the qZS push-pull converter [9] and the symmetrical qZS half-bridge DC-DC converter [3] (see Fig. 1). Both topologies have two transistors in their switching stage, which leads to reduced complexity of the switching stage and its simpler control.

In contrast to the push-pull counterpart, the symmetrical qZS half-bridge DC-DC converter features twice reduced voltage stress of the transistors and a two-winding isolation transformer. In addition, the converter could be supplied either from one or two input voltage sources. However, to ensure the symmetrical structure of the impedance source network, mirror connection of two identical qZS networks is required. That seems to be the main drawback of the symmetrical qZS half-bridge DC-DC converter since it uses twice more passive components and is more costly and less efficient than the traditional full-bridge qZS DC-DC converter.

This paper proposes an asymmetrical qZS half-bridge DC-DC converter with its experimental validation. The novel topology was derived by the combination of the single-switch qZS DC-DC converter and the half-bridge galvanically isolated DC-DC converter. The structure of this topology is simpler than that of the symmetrical qZS half-bridge DC-DC converter since it is based on a single qZS network.

II. ASYMMETRICAL QUASI-Z-SOURCE HALF-BRIDGE DC-DC CONVERTER

A. General description

The proposed step-up DC-DC converter has the qZS network, two switches and two capacitors on the low-voltage input side, a step-up isolation transformer and a Voltage Doubler Rectifier (VDR) on the high-voltage output side (Fig. 2*a*).

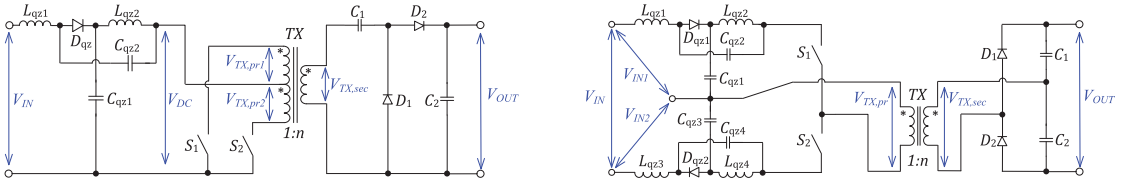

Fig. 1. State-of-the-art qZS galvanically isolated DC-DC converters with reduced switch count: qZS push-pull DC-DC converter (a) and symmetrical qZS half-bridge DC-DC converter (b).

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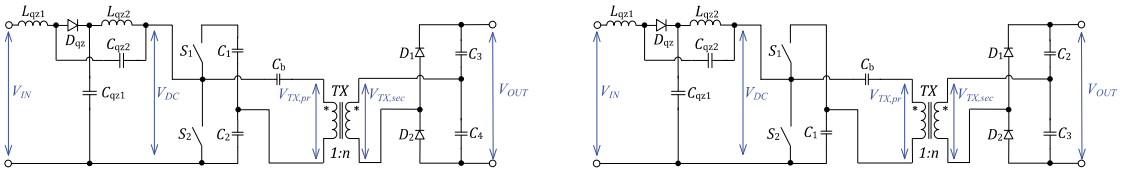

Fig. 2. New asymmetrical qZS half-bridge DC-DC converters: with two (a) and single (b) capacitor in the half-bridge switching stage.

The qZS network is composed from two inductors (L_{qz1} and L_{qz2}), two capacitors (C_{qz1} and C_{qz2}), and a diode (D_{qz}). To prevent the saturation of the isolation transformer *TX*, DC blocking capacitor C_b is added in series with the primary winding of the isolation transformer.

B. Generalized Operating Principle

In the proposed topology (Fig. 2*a*), the high-side (S_1) and the low-side (S_2) switches of the half-bridge inverter are driven complimentary without dead time (Fig. 3).

In the converter, the switch S_2 performs shoot-through for DC voltage gain regulation similarly to other qZS derived topologies [10], therefore the amplitude value of the intermediate DC-link voltage V_{DC} could be represented as

$$V_{DC} = \frac{V_{IN}}{1-2\cdot d_2} = B\cdot V_{IN}, \qquad (1)$$

where V_{IN} is the input voltage of the converter, d_2 is the duty cycle of S_2 and B is the input voltage boost factor (B=1/(1-2·d_2)). The half-bridge capacitors C_1 and C_2 are

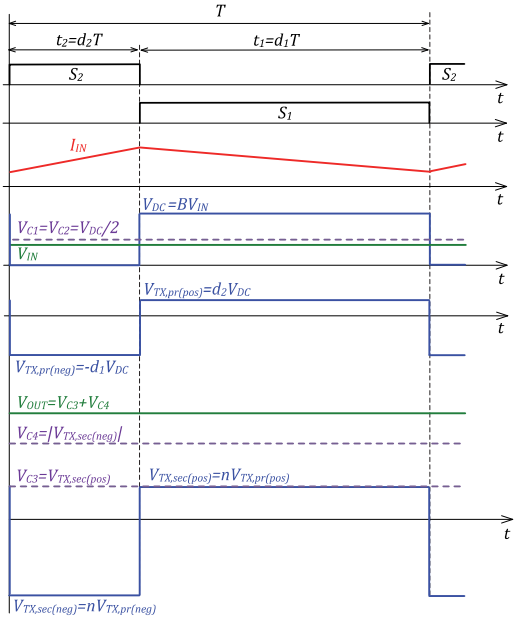

Fig. 3. Control principle and idealized operating waveforms of the proposed converter.

equally charged to half of the V_{DC} value each. The energy is transferred through the isolation transformer *TX* by the asymmetrical pulses, which leads to unequal voltages across the VDR capacitors C_3 and C_4 (Fig. 3). The output voltage of the proposed topology is directly regulated by the variation of the duty cycle of S_2:

$$V_{OUT} = \frac{V_{IN}\cdot n}{1-2\cdot d_2}, \qquad (2)$$

where n is the turns ratio of the isolation transformer.

If inductors L_{qz1} and L_{qz2} are properly dimensioned [11], the qZS network will maintain the continuous input current, thus reducing the stress of the input voltage source. As compared to the galvanically isolated qZS DC-DC converter with the full-bridge switching stage [1], the proposed converter has only one shoot-through state per switching period. Therefore, the qZS-network operates with the frequency equal to the switching frequency and its passive components have double values as compared to those of the full-bridge counterpart.

C. Topology Modification Possibility

The proposed asymmetrical half-bridge topology could be simplified further by the reconfiguration of the switching stage. In that case, the upper capacitor of the half-bridge switching stage should be short-circuited, as shown in Fig. 2*b*. The general operating principle of the modified topology remains the same. Minimization of components count will lead to higher voltage stress of the primary side capacitors. Capacitor C_1 should be dimensioned for the operating voltage equal to the amplitude value of the intermediate DC-link voltage V_{DC}. The blocking capacitor C_b needs to withstand higher DC voltage because the half-bridge switching stage supplies the transformer with unipolar voltage pulses in contrast to bipolar in the previous topology.

III. Simulation and Experimental Study

To verify the step-up performance of the proposed topology, the numerical simulations were performed in the PSIM environment. Generalized simulation parameters are presented in Table I. Fig. 4 shows that the converter ensures the demanded gain of the input voltage (V_{IN} = 25 V and V_{DC} = 62 V) and continuous input current with peak-to-peak ripple of 6 A. The amplitude voltage values of the positive and negative cycles of the isolation transformer's primary winding can be calculated as follows:

$$V_{TX,pr(pos)} = d_2 V_{DC} \approx 19V, \quad V_{TX,pr(neg)} = -((1-d_2)V_{DC}) \approx -43V. \qquad (3)$$

TABLE I
SIMULATION PARAMETERS OF THE QZS HALF-BRIDGE DC-DC CONVERTER

Parameter	Symbol	Value
Input voltage, V	V_{IN}	25
Average input current, A	I_{IN}	8
Output voltage, V	V_{OUT}	240
Duty cycle of S_2 (shoot-through duty cycle)	d_2	0.3
Switching frequency, kHz	f_{sw}	100
Transformer turns ratio	n	4
Capacitance of qZS capacitors, µF	C_{qz1}, C_{qz2}	26.4
Inductance of qZS inductors, µH	L_{qz1}, L_{qz2}	23
Capacitance of half-bridge capacitors, µF	C_1, C_2	100
Capacitance of the DC blocking capacitor, µF	C_b	5.5
Capacitance of VDR capacitors, µF	C_3, C_4	2.2

As it was previously predicted, the VDR capacitors are charged to different voltages, which could be estimated by

$$V_{C3} = d_2 V_{DC} n \approx 76V\,, \quad V_{C4} = (1-d_2) V_{DC} n \approx 172V\,. \qquad (4)$$

Finally, the output voltage is the sum of the voltages of C_3 and C_4, which properly matches the theoretical prediction. The simulation results show the sine wave current of the primary winding of the isolation transformer. This effect is caused by the series resonant circuit formed by the DC blocking capacitor C_b and primary winding leakage inductance of the isolation transformer. By proper utilization of those elements the soft switching could be achieved for the half-bridge inverter switches.

To validate the proposed topology, the 200 W prototype converter was assembled in accordance with the schematic in Fig. 2*a* and technical specifications in Tables I and II.

TABLE II
GENERAL SPECIFICATIONS OF SEMICONDUCTORS USED IN THE EXPERIMENT

Component	Type	Specifications
S_1, S_2	Vishay Si4190ADY	V_{DS}=100 V; $R_{DS(on)}$=8.8 mΩ I_D=18.4 A, Q_g=20.7 nC, R_g=2.2 Ω
D_{qz}	Vishay V60D100C	V_{RRM}=100 V; V_F=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_1, D_2	CREE C3D02060E	V_{RRM}=600 V; V_F=1.8 V $I_{F(AV)}$=4 A

The qZS network was built on low-profile SMD inductors Vishay IHLP-6767GZ (two 47 uH inductors in parallel for each qZS inductor). The isolation transformer was wound on the ETD34 core made from ferrite N87 and its leakage inductance referred to the primary was 0.35 µH. Chip multilayer ceramic capacitors SMD1210 2.2 µF 100 V from Murata were used to assemble the qZS network and the voltage doubler rectifier (12 units connected in series for each qZS capacitor and 9 units connected in 3x3 matrix configuration for the VDR capacitors).

As seen from Fig. 5, the experimental waveforms are matching the theoretical predictions and the simulation study. The topology features the demanded step-up performance, continuous input current and sine wave current of the primary winding of the isolation transformer. Due to losses in components, the converter has slightly lower DC voltage gain which was also influenced by the leakage inductance of the isolation transformer. Measured voltage across VDR capacitors was 70 V and 155 V in contrast to 76 V and 172 V estimated in (3).

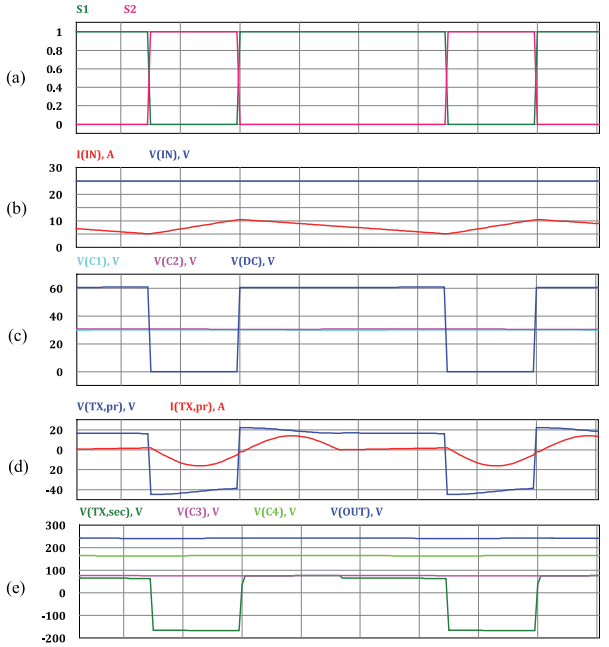

Fig. 4. Simulation results of the proposed topology: gating signals of switches (a), input voltage and current (b), voltages of half-bridge capacitors and intermediate DC-link voltage (c), voltage and current of the primary winding (d) and secondary winding voltage, voltages of VDR capacitors and output voltage of the converter (e).

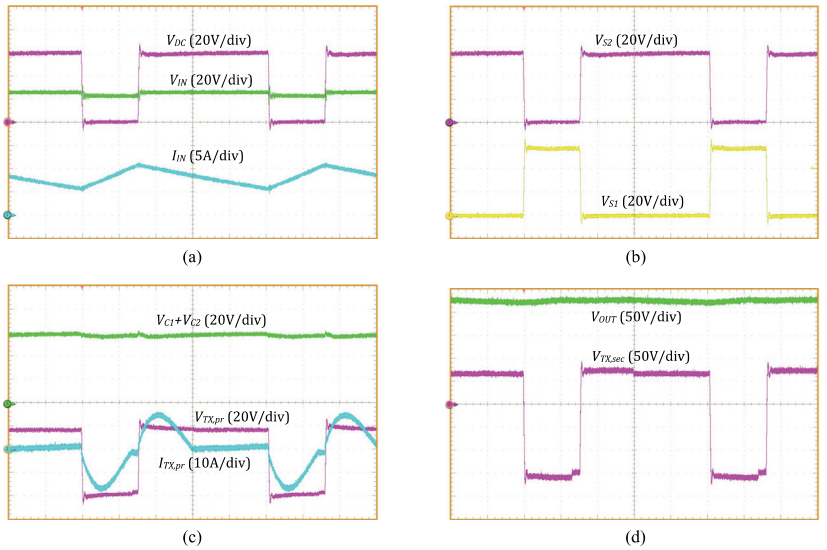

Fig. 5. Experimental waveforms of the proposed topology: input voltage, input current and intermediate DC-link voltage (a), operating voltages of switces (b), summarized voltage of the half-bridge capacitors, voltage and current of the primary winding (c) and secondary winding voltage and output voltage of the converter (d).

IV. Conclusions and Future Work

This paper proposed a novel galvanically isolated asymmetrical qZS half-bridge DC-DC converter, a new member of the galvanically isolated impedance source DC-DC converter family. It was derived by the combination of the single-switch qZS DC-DC converter and the half-bridge galvanically isolated DC-DC converter. The converter features simple control due to reduced switch count and continuous input current in the CCM operation. If properly realized, the series resonant circuit formed by the DC blocking capacitor and primary winding leakage inductance of the isolation transformer will result in the soft switching of the half-bridge inverter switches.

To validate the proposed topology, the experimental prototype with a rated power of 200 W was assembled and tested. Experimental results have verified all the theoretical assumptions and computer simulations. Voltage stresses of the capacitors and transistors all conformed to the theoretical predictions.

Further research will be directed towards the analysis of the resonant switching processes and resulting soft switching performance of the proposed converter.

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Quasi-Z-Source Half-Bridge DC-DC Converter for Photovoltaic Applications

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***Abstract*—This paper presents a novel quasi-Z-source half-bridge galvanically isolated DC-DC converter intended for the photovoltaic applications. The topology could be envisioned as an alternative to the boost half-bridge DC-DC converter but the benefit of its symmetric structure reduces the threat of transformer saturation due to the dc flux. The proposed converter features the continuous input current and could be used either with one or two input voltage sources.**

Keywords— impedance-source converters, DC-DC power converters, galvanic isolation, renewable energy sources

I. Introduction

The impedance-source (IS) galvanically isolated DC-DC converter was proposed in [1] as an alternative power conversion approach for the renewable energy applications, in particular, for PV power systems. In general, the new topology was derived from a classical voltage source full-bridge isolated DC-DC converter by adding a passive IS network (ISN) to its input terminals. The IS network is a two-port passive circuit that consists of capacitors, inductors and diodes in a special configuration. It could be short- or open-circuited without any damages of the main DC-DC converter. Therefore, the IS DC-DC converter combines the basic properties of the voltage source and current source converters, allowing both the buck and boost functions within the single switching stage. Thanks to this unique property, the IS galvanically isolated DC-DC converters are also known as converters for a wide input voltage and load regulation range.

According to the topology of the ISN, the existing IS DC-DC converters could be categorized as Z-Source [1, 2], quasi-Z-Source [3], Trans-Z-Source [4], Trans-quasi-Z-source [4], and Y-source based converters [5]. The quasi-Z-Source (qZS) approach has gained its popularity fast in the renewable energy applications since it features the continuous input current during the shoot-through operation mode and reduced component stresses.

In the switching stage realization, the dominant solution is the full-bridge inverter, which could be realized in a single- or three-phase configuration [3]. The IS DC-DC converter with the push-pull switching stage [6, 7] is characterized with the reduced number of transistors with performance close to the full-bridge counterpart. However, in this topology the transistors must block twice the dc link voltage, therefore their voltage stress is twice higher than in the full-bridge switching stage.

We propose the novel qZS half-bridge galvanically isolated DC-DC converter as an alternative approach to the IS DC-DC converters with a reduced number of switches. In contrast to the push-pull counterpart, it features twice reduced voltage stress of the transistors and a two-winding isolation transformer. The topology is positioned as a power conditioning unit for PV applications with single- or dual-input functionality.

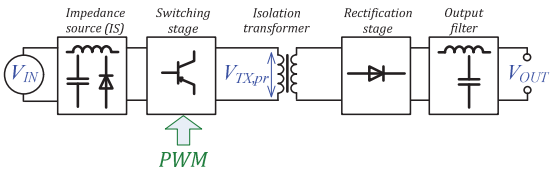


Fig. 1. Generalized block diagram of the impedance source galvanically isolated DC-DC converter.

II. qZS Half-Bridge DC-DC Converter

A. Derivation and general description

Fig. 2 shows the generalized power circuit layout of the proposed qZS half-bridge DC-DC converter. It is based on two identical qZS networks with a neutral node *n* between the capacitors C_1 and C_3. Mirror connection of two qZS networks enables the symmetrical structure of the impedance source network. The topology could be used either with one or two input voltage sources. By help of the voltage doubler rectifier (VDR) the high voltage gain is realized with the optimal turns ratio of the isolation transformer *TX*.

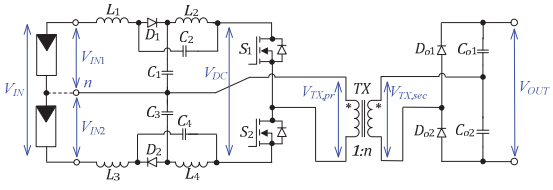


Fig. 2. Power circuit layout of the qZS half-bridge DC-DC converter.

The output voltage of the converter is controlled by the variation of the shoot-through duty cycle of the inverter stage similarly to the qZS full-bridge DC-DC converter discussed in [8]. We examine here the topology with a single input voltage source V_{IN}, therefore the primary winding voltage of the isolation transformer can have three different levels: $-B(V_{IN}/2)$, 0, and $+B(V_{IN}/2)$, where B is the boost factor of the inverter defined as $B=V_{DC}/V_{IN}$.

B. Steady State Analysis

Similarly to any other qZS based galvanically isolated DC-DC converter, the shoot-through states in our topology are generated by the cross-conduction of both switches of the inverter leg (Fig. 3). The switching period in the continuous conduction mode (CCM) consists of two shoot-through states (with a total duration t_S) and two active states (with a total duration t_A), and can be generally expressed as

$$\frac{t_A}{T}+\frac{t_S}{T}=D_A+D_S=1, \tag{1}$$

where D_A is the duty cycle of the active states, D_S is the duty cycle of the shoot-through states and T is the switching period. The converter is controlled by the symmetrical pulse width modulation (PWM), therefore the active and shoot-through states within one switching period are evenly split into equal intervals of half the duration.

It is seen from Fig. 3 that the proposed topology has three main operating states in the CCM: shoot-through state, positive active state and negative active state.

Shoot-through state $[t_0 < t < t_1$ *and* $t_2 < t < t_3]$*:* Shoot-through states are generated by the cross-conduction of S_1 and S_2. The shoot-through state is used to boost the magnetic energy stored in the qZS inductors $L_1...L_4$ without short-circuiting the capacitors $C_1...C_4$. This increase in inductive energy, in turn, provides the boost of voltage seen on the transformer primary winding during the active states of the converter. The equivalent circuit of the converter in this state is presented in Fig. 4*a*. During this state the voltage across the isolation transformer is zero.

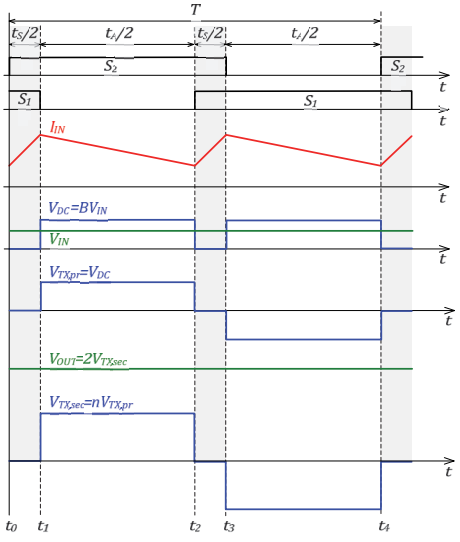


Fig. 3. Control principle and idealized operating waveforms of the proposed topology.

Positive active state $[t_1 < t < t_2]$*:* During this state, the switch S_2 is conducting, thus resulting in a positive voltage $V_{TX,pr}$ across the primary winding of the isolation transformer. The equivalent circuit of the converter in this state is presented in Fig. 4*b*. It is seen that only the bottom qZS network (C_3-C_4-D_2-L_3-L_4) maintains the power transfer to the output. At the same time, as the inductor L_2 is not involved in the power flow, it charges the capacitor C_2.

Negative active state $[t_3 < t < t_4]$*:* Switch S_1 is conducting, thus resulting in a negative voltage $V_{TX,pr}$ across the primary winding of the isolation transformer. The equivalent circuit of the converter in this mode presented in Fig. 4*c* is similar to that of the positive active state.

Taking into account that the qZS-network is symmetrical, we can assume that

$$L_1=L_3, \qquad L_2=L_4, \tag{2}$$

$$C_1=C_3, \qquad C_2=C_4. \tag{3}$$

Correspondingly, the voltages are

$$v_{L1}=v_{L3}, \qquad v_{L2}=v_{L4}, \tag{4}$$

$$V_{C1}=V_{C3}, \qquad V_{C2}=V_{C4}. \tag{5}$$

The sum of the capacitor voltages defines the peak value of the DC-link voltage:

$$V_{DC}=V_{C1}+V_{C2}+V_{C3}+V_{C4}, \tag{6}$$

where V_{C1}, V_{C2}, V_{C3}, V_{C4} are the average voltages across the capacitors over one switching period. At steady state the average voltage of the inductors over their operating period is zero and the dc voltages of the capacitors can be found from the voltage balance across the inductors:

$$V_{C1}=V_{C3}=\frac{V_{IN}(1-D_S)}{2(1-2\cdot D_S)}, \quad V_{C2}=V_{C4}=\frac{V_{IN}\cdot D_S}{2(1-2D_S)}. \tag{7}$$

The boost factor of the qZS network can be expressed as follows:

$$B=\frac{V_{DC}}{V_{IN}}=\frac{V_{C1}+V_{C2}+V_{C3}+V_{C4}}{V_{IN}}=\frac{1}{1-2\cdot D_S}. \tag{8}$$

The gain factor of the proposed converter is expressed as follows:

$$G=\frac{V_{OUT}}{V_{IN}}=\frac{n}{1-2\cdot D_S}, \tag{9}$$

where n is the turns ratio of the isolation transformer.

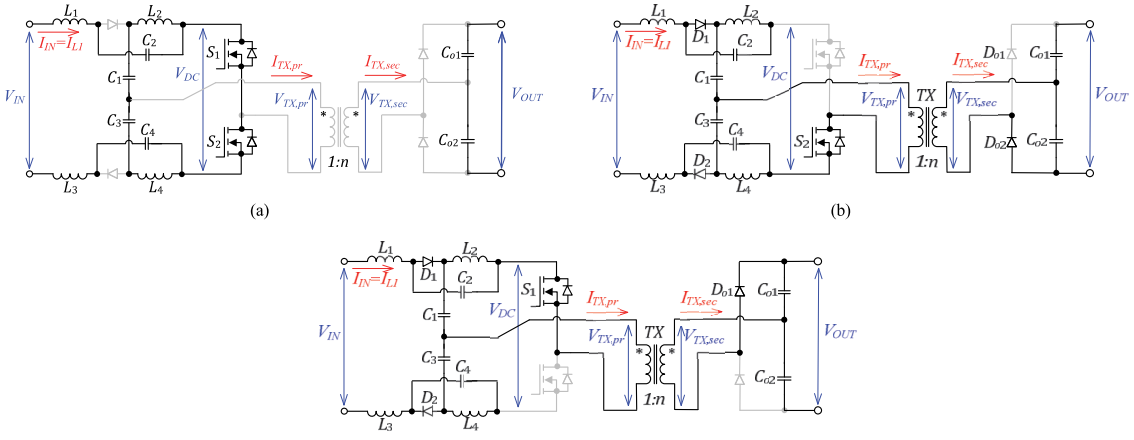


Fig. 4. Equivalent circuits of the proposed topology for its main operation states: shoot-through (a), positive active state (b) and negative active state (c).

C. Component Stresses and General Design Guidelines

The main purpose of the capacitors of the qZS network is to absorb the current ripple and limit the voltage ripple across the inverter. The voltage ripple across the capacitor can be roughly calculated by

$$\Delta V_C = \frac{I_{L,av} \cdot t_S}{2 \cdot C}, \tag{10}$$

where $I_{L,av}$ is the average current through the qZS inductor, C is the capacitance and t_S is the total duration of the shoot-through states over the operating period. In the proposed topology the shoot-through time is evenly split into two intervals of half the duration (Fig. 3) and the qZS network operates with the frequency twice higher than the fundamental frequency of the isolation transformer. Assuming that $C_1 = C_3$ the capacitance needed to limit the peak-to-peak voltage ripple by K_C could be calculated as

$$C_1 = C_3 \geq \frac{P \cdot D_S \cdot (1-2D_{S(\max)})}{f \cdot K_C \cdot V_{IN(\min)}^2 \cdot (1-D_{S(\max)})}, \tag{11}$$

where P is the power rating of the converter, f is the switching frequency, $V_{IN(min)}$ is the minimum value of the input voltage, $D_{S(max)}$ is the shoot-through duty cycle value corresponding to the minimum input voltage, and K_C is the desired peak-to-peak voltage ripple across the capacitor ($K_C = \Delta V_C / V_C$).

Capacitance values for capacitors C_2 and C_4 could be found similarly:

$$C_2 = C_4 \geq \frac{P \cdot (1-2D_{S(\max)})}{f \cdot K_C \cdot V_{IN(\min)}^2}. \tag{12}$$

The inductors in the qZS network will limit the current ripple through the switches during the shoot-through states. Peak-to-peak current ripple through the inductors can be calculated by

$$\Delta I_{L1} = \int_0^{\frac{T \cdot D_S}{2}} \frac{dI_{L1}}{dt} \cdot dt = \int_0^{\frac{T \cdot D_S}{2}} \left(\frac{V_{IN} + V_{C2} + V_{C4}}{2 \cdot L} \right) \cdot dt. \tag{13}$$

The average current through the inductors is equal to the average input current. In order to maintain the CCM operation of the converter, the input current ripple ΔI_{IN} should be smaller than the average input current I_{IN}. Therefore, the minimal inductance value of the qZS inductors where no discontinuous conduction mode (DCM) occurs is

$$L \geq \frac{V_{IN(\min)}^2 \cdot (1-D_{S(\max)}) \cdot D_{S(\max)}}{4 \cdot f \cdot (1-2 \cdot D_{S(\max)}) \cdot K_L \cdot P}, \tag{14}$$

where K_L is the desired peak-to-peak input current ripple of the converter ($K_L = \Delta I_{IN} / I_{IN}$).

To provide correct operation of the voltage doubler rectifier (VDR) and ensure the voltage doubling effect, the capacitors C_{O1} and C_{O2} (Fig. 2) should be properly dimensioned. In order to limit the peak-to-peak voltage ripple on these capacitors by K_{CO}, the capacitance of each capacitor should be

$$C_{01} = C_{02} \geq \frac{P \cdot D_S}{2 \cdot f \cdot K_{CO} \cdot V_{OUT}^2}. \tag{15}$$

The voltage and current stresses on the semiconductors for the ideal system are summarized in Table I.

TABLE I
VOLTAGE AND CURRENT STRESSES OF SEMICONDUCTORS

Component	Maximum Voltage	Average Current
Diodes of the qZS network (D_1, D_2)	$\frac{V_{OUT}}{2 \cdot n}$	$\frac{P}{V_{IN}}$
Transistors of the half-bridge inverter (S_1, S_2)	$\frac{V_{OUT}}{n}$	$\frac{P}{V_{IN}}$
Diodes of the voltage doubler rectifier (D_{O1}, D_{O2})	V_{OUT}	$\frac{P}{V_{OUT}}$

III. Simulation Study

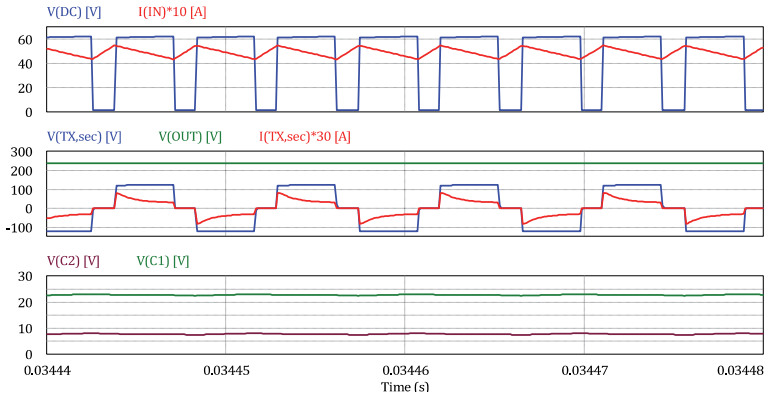
The proposed approach was validated by the computer simulations in the PSIM environment. In the qZS based topologies, the properties of semiconductors have direct impact on the step-up performance of the converter [9], therefore we used accurate models of the semiconductors based on the device datasheet values. To simplify the analysis, the ideal models of passive components (inductors, capacitors and isolation transformer) were used. The simulation parameters and generalized specifications of semiconductors are presented in Tables II and III, respectively. Two operating points corresponding to the maximum and minimum input voltages were studied. In both cases the average input current was kept at its maximum value (5 A). This approach is common for the PV oriented converters, because the PV panel behaves similarly to the current source with the limited output voltage. As shown in Fig. 4, the objects of our study were the input voltage boost properties, input current ripple, quality of the output voltage, and voltage stresses of the qZS capacitors.

TABLE II
Simulation Parameters of the qZS Half-Bridge DC-DC Converter

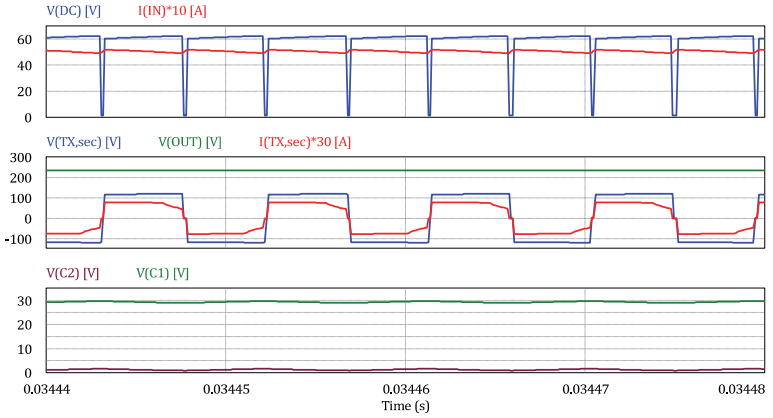
Parameter	Symbol	Value
Input voltage range, V	V_{IN}	30…58
Maximum input current, A	I_{IN}	5
Output voltage, V	V_{OUT}	240
Switching frequency, kHz	f_{sw}	110
Operating frequency of qZS-network, kHz	f_{qZS}	220 ($2 \cdot f_{sw}$)
Transformer turns ratio	n	4
Capacitance of qZS capacitors, µF	$C_1 \ldots C_4$	26.4
Inductance of qZS inductors, µH	$L_1 \ldots L_4$	24
Capacitance of output capacitors, µF	C_{O1}, C_{O2}	2.2
Converter power rating, W	P	300

TABLE III
General Specifications of Semiconductor Components Used in Simulations and Experiments

Component	Type	Specifications
S_1, S_2	Infineon IPP600N25N3	V_{DS}=250 V; $R_{DS(on)}$=60 mΩ I_D=25 A, Q_g=22 nC, R_g=2.5 Ω
D_1, D_2	Vishay V60D100C	V_{RRM}=100 V; V_F=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_{o1}, D_{o2}	CREE C3D02060E	V_{RRM}=600 V; V_F=1.8 V $I_{F(AV)}$=4 A



(a)



(b)

Fig. 4. Simulation results of the proposed topology at the minimum (a) and maximum (b) input voltages.

In the first operating point with the input voltage of 30 V, the shoot-through duty cycle was set to 0.27 to obtain the desired output voltage. Fig. 4*a* shows that the qZS network ensures the demanded twofold gain of the input voltage (V_{IN} = 30 V and V_{DC} = 60 V) and continuous input current. As predicted by Eq. (6), the amplitude value of the V_{DC} equals the sum of the capacitor voltages of the qZS network. Furthermore, the voltage doubler rectifier provides the demanded voltage doubling effect of the peak voltage of the secondary winding of the isolation transformer, thus ensuring the ripple-free output voltage of 240 V at the power close to 150 W.

Next, the topology was tested with the maximum input voltage (58 V). The shoot-through duty cycle was reduced to 0.05 and the converter operated with the minimal input voltage boost factor (*B* close to 1). As shown in Fig. 4*b*, the operating voltage of the qZS capacitor C_2 (and, consequently, C_4) was decreased almost to zero, while the voltage of C_1 (and C_3) reached its maximum value. It was found that the converter was still maintaining the continuous input current, ensuring the ripple-free output voltage of 240 V at the rated power.

IV. Experimental Results

To verify the proposed topology experimentally, the 300 W prototype converter (Fig. 5) was assembled in accordance with the schematic in Fig. 2 and technical specifications in Table II.

Each qZS network contains the coupled inductor built on the EFD25 core made from N87 ferrite material with the resulting magnetizing inductance of 12 µH. The isolation transformer was wound on the ETD34; its magnetizing inductance was 30.8 µH and leakage inductance referred to the primary was 0.35 µH. Chip monolithic ceramic capacitors SMD1210 2.2 µF 100 V from Murata were used to assemble the qZS network and the voltage doubler rectifier (12 units connected in series for each qZS capacitor and 9 units connected in 3x3 matrix configuration for the VDR capacitors). The types and generalized specifications of the semiconductors are presented in Table III. The prototype was built on the 250 V Si MOSFETs, thus without optimization for the high efficiency.

The experimental setup was supplied from two PV simulators Agilent E4360A connected in series. Each PV simulator produced half of the input voltage of the converter, therefore the string connection of two PV panels was emulated.

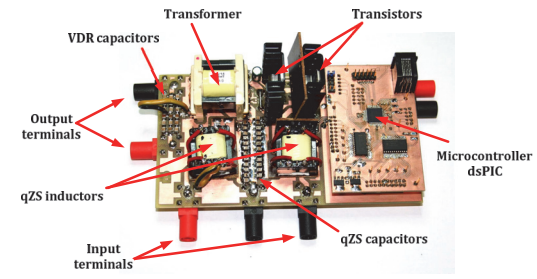


Fig. 5. Experimental prototype (165 mm x 90 mm).

Waveforms measured at the minimum input voltage V_{IN} = 30 V are shown in Fig. 6*a*. Shoot-through duty cycle near 0.3 was used to compensate the losses in the system and to achieve 240 V at the output terminals. Oscillations across transformer windings were observed during the shoot-through states, which is a common behavior of the half-bridge converters caused by the resonance between the transformer leakage inductance and the parasitic capacitance of the semiconductor components [10]. These voltage oscillations are reflected to the qZS diodes D_1 and D_2 that are reverse biased during the shoot-through states.

Waveforms measured at the maximum input voltage V_{IN} = 58 V are shown in Fig. 6*b*. Experimental results obtained somewhat differ from the simulation study (Fig. 4*b*) mainly due to the influence of the leakage inductance of the coupled inductors of the qZS networks and the leakage inductance of the transformer. High number of passive components leads to undesirable oscillations in the qZS network at the operation modes with a DC voltage gain close to unity. For example, these parasitic oscillations have been observed in the input current, as shown in Fig. 6*b*. In both cases the efficiency was limited by 92 %, which is mostly caused by the high on-state resistance of the MOSFETs.

V. Conclusions and Future Work

In this paper the qZS half-bridge DC-DC converter was proposed as a new member of the impedance source galvanically isolated DC-DC converter family. To obtain the symmetrical structure, two identical qZS networks were mirror-connected. Each qZS network needs to handle half of the converter rated power. The topology could be used either with one or two input voltage sources. It has simple control due to reduced switch number and features the continuous input current in the CCM operation.

To validate the proposed topology, the experimental prototype with a rated power of 300 W was assembled and tested. Experimental results have verified all the theoretical assumptions. Voltage stresses of the capacitors and transistors all conformed to the theoretical predictions; however, waveforms of currents were influenced by the parasitic oscillations in the prototype. At the same time, the average values of the currents were not influenced.

Further research will be directed towards the analysis of the resonant processes within the converter and elaboration of the detailed design guidelines. In addition, the operation in the dual input mode with two input voltage sources connected through the common neutral node will be studied.

Acknowledgment

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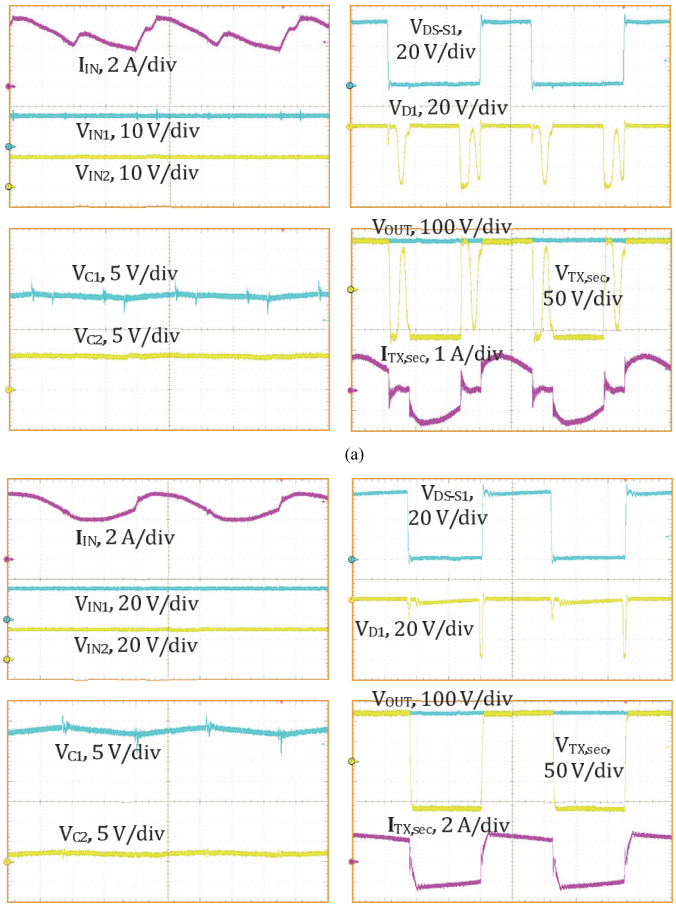

Fig. 6. Experimental results of the proposed topology at the minimum (a) and maximum (b) input voltages.

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Galvanically Isolated Quasi-Z-Source DC-DC Converters with Combined Energy Transfer for Renewable Energy Sources Integration

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***Abstract*—This paper presents a novel class of quasi-Z-source galvanically isolated DC-DC converters intended for the integration of low voltage renewable energy sources into a DC microgrid. These converters combine characteristics of the transformer based and the inductor based impedance-source galvanically isolated DC-DC converters. They feature the continuous input current essential for photovoltaic applications. Two types of the quasi-Z-source based converters are presented within the proposed class: with the full-bridge and the push-pull switching stage. Also, two possible variations of coupling in the impedance-source network are described for both converter types.**

Keywords—impedance-source converters, DC-DC power converters, galvanic isolation, renewable energy sources

I. INTRODUCTION

Recent reports indicate a finite supply of fossil fuels, while energy consumption is growing. This imposes new challenges for energy generation, conversion and delivery, which link to the rapid penetration of renewable and alternative energy sources and energy storages. Power electronics has become a key technology in emerging energy applications like dispersed energy generation [1], [2]. The concept of integration of the renewable and alternative energy sources into the DC microgrid has become popular in energy harvesting and distribution. DC microgrids could also be a part of complicated smart grids [3] - [5].

The DC microgrid technology has been adopted for shipboard and aircraft power systems, supply of data centers and other sensitive industrial loads [6] - [8]. It is also a promising solution for the future small power grid of household or small community levels [9], [10]. Such small power grids could comprise renewable and alternative energy sources, and battery energy storage systems. Also, many consumer electronic devices could avoid the AC-DC energy conversion stage at the input, and be fed through a single-stage internal high efficient DC-DC converter from a common DC bus. This solution shows superior possibilities for an efficient energy consumption, but requires high performance energy converters to connect the system to the main AC grid, as well as to integrate energy generation and storage units [2], [11]. The DC microgrids are more advantageous as most of the internal energy sources and storage systems have the DC input/output. For example, the DC microgrid concept provides higher efficiency of energy conversion than the AC microgrid in household energy systems based on rooftop (or building-integrated) photovoltaic (PV) power and battery energy storage system [8].

Integration of a PV panel to the residential DC microgrid with high conversion efficiency could be very complicated due to possible partial shading. It leads to a wide variation of voltage and power on a maximum power point. Panel-integrated converter could be used to provide individual maximum power point tracking for each PV panel and ensure high energy yield under partial shading [12]. An appropriate power electronics converter has to be able to operate in a wide voltage and power range to provide low start-up power and partial shading compensation. To integrate low-voltage energy sources with the DC output, like a PV panel, the galvanically isolated DC-DC converter is needed. As a solution, current source topologies have been preferred over voltage source topologies due to inherent continuous input current. An alternative solution proposed recently is the impedance-source converters (ISCs) [13], [14]. They utilize common blocks with voltage and current source converters and specific two port impedance-source network (ISN) at the input. The ISN allows voltage step-up on the input stage, and makes an ISC immune to shoot-through and open states in the switching stage.

All existing galvanically isolated impedance-source (IS) DC-DC converters have been classified into transformer and coupled inductor based according to the element that transfers energy from the input to the output side [15]. This paper proposes a new class of the ISCs that features combined energy transfer: using both a coupled inductor and a transformer. Four topological variations described below are using two basic switching stage types: full-bridge inverter and push-pull. The proposed energy conversion principle is described here with only one type of ISN – quasi-Z-source (qZS) network, because only this type has continuous input current within a wide input voltage regulation range. This makes it particularly suitable for the integration of the low-voltage DC source into the DC microgrid.

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II. Isolated Impedance-Source Converters with Combined Energy Transfer

The proposed principle of combined energy transfer adds a third class to the second level of the ISC classification in [15]. In general, the principle combines features of transformer based ISCs and coupled inductor based ISCs with a single switch. It means that it commonly uses switching stage generic for the transformer based ISCs. Here we are showing only two switching stages that are widely used: full-bridge inverter and push-pull. Another switching stage could be utilized to expand the proposed class of ISCs. A similar principle was already adopted in current source converters [16] - [18]; however, researchers have shown no particular interest in the principle.

A. Full-Bridge Switching Stage

A generalized functional scheme of this group of ISCs is shown in Fig. 1. The concept combines features of the coupled inductor based converter with a single switch and the transformer based converters with the full-bridge switching stage. Coupled inductors of the ISN contain additional winding(s) used for energy transfer to the output side. They provide additional output voltage and improve DC voltage step-up capabilities of the ISC. Switching stage could be implemented using a single-phase and a three-phase configuration. The single-phase configuration seems to be simpler and more attractive in practice.

Application of the generalized functional scheme to the qZS ISC with single-phase full-bridge switching stage is shown in Fig. 2. The proposed full-bridge ISC topology utilizes only one voltage doubler rectifier (VDR) at the output side, which is highly advisable in the ISCs [19]. The ISN contains a single inductor or two inductors depending on the coupling of the input inductor. It could be either a winding of the coupled inductor T_1 with N_{qZ} turns, or a discrete inductor L_1. The output

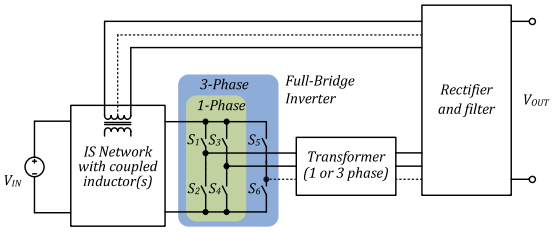

Fig. 1. Generalized functional scheme of the galvanically isolated full-bridge IS DC-DC converter with combined energy transfer.

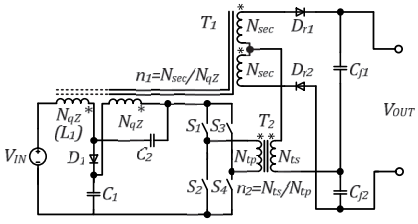

Fig. 2. qZS based galvanically isolated full-bridge DC-DC converter with combined energy transfer.

windings with N_{sec} turns are connected in series with the output winding of the isolation transformer T_2 with N_{ts} turns. Voltage could be regulated using a symmetrical overlap method where shoot-through is created by overlapping active states.

Only one of the output windings of the coupled inductor T_1 will conduct current simultaneously. It means that the current of the winding N_{ts} will be reflected from the output side to the input side through the coupled inductor T_1 with turns ratio n_1. It follows that the input current will increase ripple when the input inductor is a part of T_1, because each input winding of the coupled inductor T_1 will receive half of the reflected output winding current. When the input inductor is a separate inductor L_1, all current of the output winding is reflected to a single input winding of the T_1 with N_{qZ} turns. The second coupling type looks more promising for PV applications, since it has low input current ripple while combined energy transfer is satisfied. Neither does it influence capacitor voltages in the qZS network, while current ripple will be different from that of the conventional qZS network. This topology will be described in detail in the next section.

B. Push-Pull Switching Stage

The push-pull switching stage is an alternative solution for the full-bridge switching stage. It has a reduced number of switches, but requires twice higher blocking voltage of the switches. The push-pull switching stage fits applications with low-voltage and high-current at the input. In this case higher blocking voltage of the switches is not a concern, while conduction losses could be reduced because the input current loop contains only one power switch.

In contrast to the previous full-bridge ISC, the push-pull switching stage does not influence the operation of the qZS network. It provides the same voltage at the output winding

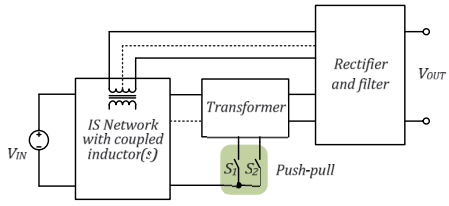

Fig. 3. Generalized functional schemes of the galvanically isolated IS push-pull DC-DC converter with combined energy transfer.

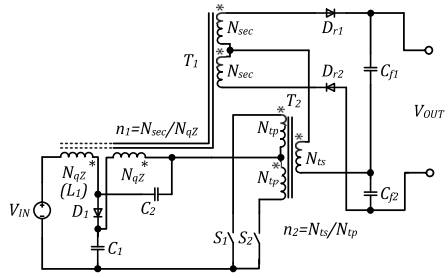

Fig. 4. qZS based galvanically isolated push-pull DC-DC converter with combined energy transfer.

of the transformer T_2 with N_{ts} turns. During an equivalent active state, only one switch is conducting, while both of them should be conducting during an equivalent shoot-through state. During the equivalent shoot-through state, the input windings of the transformer T_2 compensate each other and provide short-circuit of the DC link. Operation principle of the push-pull switching stage with the isolation transformer T_2 improves the core flux balance to avoid saturation.

III. Steady State Analysis of Isolated Single-Phase Full-Bridge ISC with Combined Energy Transfer

This section analyzes operation in the steady state of the galvanically isolated single-phase full-bridge ISC with combined energy transfer shown in Fig. 5. This topology has been derived as a superposition of the converters proposed in [14] and [20]. It has low input current ripple due to discrete implementation of the input inductor. The steady state analysis is performed with an assumption that the proposed ISC operates in the continuous conduction mode at the input. An example of steady state analysis of the ISC with combined energy transfer is shown here. The topology selected is based on the most proven converter among the existing transformer based galvanically isolated qZS DC-DC converters. The ISC topology analyzed is especially appropriate for a PV panel integration into the DC microgrid since it meets all requirements. The other three ISC topologies proposed in this article have a similar operation principle and could be analyzed in the same way.

The control principle of the ISC analyzed in this section is shown in Fig. 6. The full-bridge switching stage is controlled with a symmetric overlap of the active states of the transistors. Zero state is avoided in control because it has minor influence on the operation of the converter. DC voltage step-up is controlled through adjusting of the shoot-through duty cycle D_S. The shoot-through state appears two times per switching period that leads to twofold operation frequency of the qZS network. The switching period T consists only of active and shoot-through states:

$$D_A + D_S = 1. \tag{1}$$

Implementation of the combined energy transfer has minor influence on the voltage values within the qZS network. From the voltage-second balance it is possible to obtain values of the capacitors' voltages that are common for the qZS network:

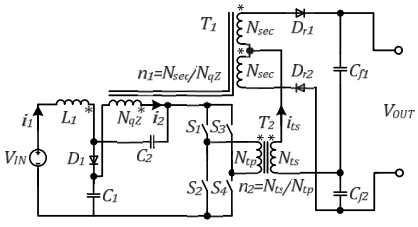

Fig. 5. Power circuit layout of the qZS galvanically isolated single-phase full-bridge ISC with combined energy transfer.

$$V_{C1} = \frac{V_{IN} \cdot (1 - D_S)}{(1 - 2 \cdot D_S)}, \tag{2}$$

$$V_{C2} = \frac{V_{IN} \cdot D_S}{(1 - 2 \cdot D_S)}. \tag{3}$$

As seen from Fig. 6, the switching period of the proposed topology could be separated into four intervals: two identical shoot-through state intervals and two active state intervals with an opposite polarity of the transformer T_2 voltage.

Active state with positive voltage across the input winding of the transformer T_1 occurs during the interval $[t_1;t_2]$. Positive voltages across output windings of T_1 and T_2 are summed and applied to the VDR. The diode D_{r1} is in a conducting state, while D_{r2} is reverse biased; the output capacitor C_{f2} charges. The equivalent circuit of the converter is shown in Fig. 7*a*. The voltage (V_{C1}+V_{C2}) is applied to the input winding of the transformer T_1, while only voltage V_{C2} is applied to the input winding of the coupled inductor T_2. Another active state with negative transformer input voltage occurs during an interval $[t_3;t_4]$. It is quite similar to the previous one, as shown by its equivalent circuit in Fig. 7*b*.

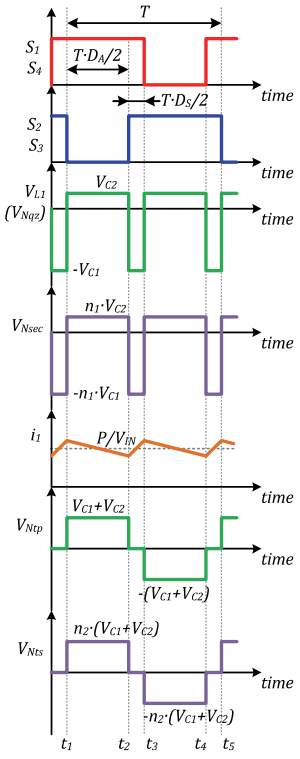

Fig. 6. Control principle and idealized operating waveforms of the proposed topology.

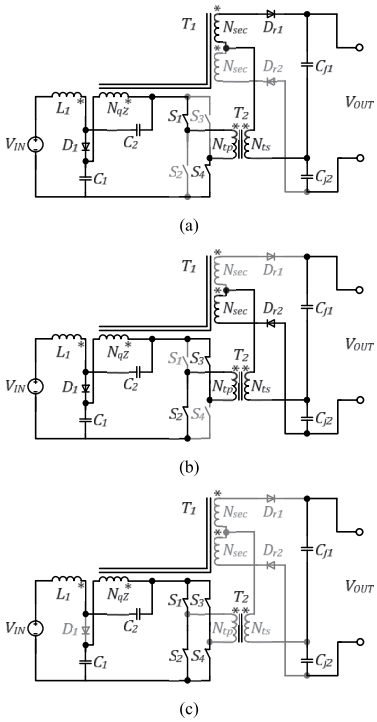

Fig. 7. Equivalent circuits of the proposed topology for: shoot-through states during [t_2;t_3] and [t_4;t_5] (a), and active state during [t_1;t_2] (b) and [t_3;t_4] (c).

The shoot-through state occurred during the time intervals [t_2;t_3] and [t_4;t_5]. It is generated by the cross-conduction of all four switches. During the shoot-through state, the magnetic energy stored in the qZS network magnetic components increases, which is essential for the voltage step-up. The equivalent circuit of the converter in the shoot-through state is shown in Fig. 7*c*. During that state, the voltage across the isolation transformer is zero, while negative voltage is applied to the windings of the coupled inductor T_1. Output capacitors feed the output load.

Idealized DC voltage gain of the converter could be easily calculated considering the waveforms from Fig. 6 and (1)-(3):

$$G = \frac{V_{OUT}}{V_{IN}} = 2 \cdot \frac{n_1 \cdot D_S + n_2}{(1 - 2 \cdot D_S)}. \quad (4)$$

Equation (4) shows that the proposed converter has higher DC voltage gain than the basic one proposed in [14], while it will feature the same input current if the input inductors are equal. However, the proposed converter requires more complicated magnetic components to achieve that improvement. DC voltage gains of the proposed topology and the basic topology from [14] are shown in Fig. 8 for the case $n_1 = 3$ and $n_2 = 3$. The same transformer is assumed to be used in the basic converter.

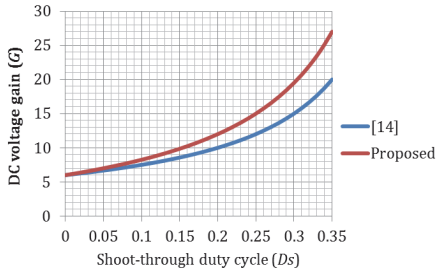

Fig. 8. Comparison of DC voltage gain for $n_1 = 3$ and $n_2 = 3$.

IV. Simulation Study

The proposed ISC converter topology was verified by the computer simulations in the PSIM environment. Parameters used in the model are shown in Table I. High step-up mode has been modeled to verify our theoretical predictions. To achieve that, the model was adjusted to provide 400 V output voltage with 15 V input voltage and 125 W input power. This low voltage and relatively high current could be achieved with a typical PV panel under partial shading conditions [12].

Simulation results shown in Fig. 9 prove our theoretical predictions. It is shown that the voltage of the VDR capacitor is higher than the voltage across the output winding of the transformer T_2. The difference equals the output voltage of the coupled inductor T_1. Also, it is shown that the current of the output winding of T_1 is reflected to the input side, while an imaginary current of the magnetizing inductance is equal to the input current since it is equal to the input inductance.

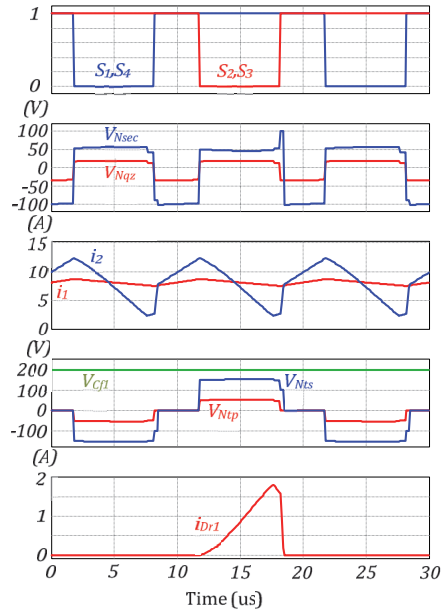

Fig. 9. Simulation results.

TABLE I. MODEL PARAMETERS

qZS nework	
Capacitors C_1, C_2	26.4 uF
Input inductor L_1	24 uH
Forward voltage drop of diode D_1	0.5 V
Coupled inductor T_1	
Magnetizing inductance	24 uH
Leakage inductance of the primary winding	0.2 uH
Leakage inductance of the secondary windings	3 uH
Turns ratio n_1	3
Transformer T_2	
Magnetizing inductance	30 uH
Leakage inductance of the primary winding	0.1 uH
Leakage inductance of the secondary windings	1.5 uH
Turns ratio n_2	3
Single-Phase Full-Bridge Switching Stage	
$R_{DS(ON)}$ resistance of the MOSFETs	30 mOhm
Switching frequency of each transistor	50 kHz
Voltage Doubler Rectifier	
Capacitors C_{f1}, C_{f2}	2.2 uF
Forward voltage drop of the diodes Dr_1, Dr_2	1.5 V

V. CONCLUSIONS

As compared to basic transformer based topologies, the new class of galvanically isolated impedance-source DC-DC converters proposed has shown improved voltage step-up characteristics. One of the proposed topologies comprehensively analyzed provides good performance for PV panel integration into the DC microgrid. This paper opens a new broad area of research on galvanically isolated impedance-source DC-DC converters with combined energy transfer. The most important topics to be investigated are: optimization of the ratio between n_1 and n_2, continuous conduction mode boundaries, application range, control issues, etc. The approach proposed extends the overall performance of the basic transformer based impedance-source topologies with a complex coupled inductor in the impedance-source network and with no additional components.

ACKNOWLEDGMENT

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Single-Switch Galvanically Isolated Quasi-Z-Source DC-DC Converter

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***Abstract*— A novel galvanically isolated quasi-Z-source DC-DC converter with a single switch is presented. It is derived from the conventional single-switch nonisolated quasi-Z-source DC-DC converter. The new topology is within the transformer based class of the galvanically isolated impedance-source DC-DC converters, while existing topologies are solely within the coupled inductor based class. This simple solution features low cost, high efficiency and reliability that suits low power or low-voltage applications. Theoretical predictions were verified with simulation in PSIM and experimentally with a 200 W prototype. The topology is further improved using the combined energy transfer principle.**

Keywords*— *impedance-source converters, DC-DC power converters, galvanic isolation, renewable energy sources.

I. INTRODUCTION

Research on galvanically isolated impedance-source (IS) DC-DC converters has been initiated with the full-bridge converter derived from the Z-source (ZS) inverter [1]. The ZS network has discontinuous input current [2]-[3] and thus does not suit well for emerging applications, like renewable energy systems. The quasi-Z-source (qZS) network is an asymmetrical derivative of the ZS network that has inherited all advantages of the ZS network, while it features continuous input current [2]. Among galvanically isolated IS DC-DC converters, the full-bridge qZS DC-DC converter proposed in [4] (Fig. 1) has been most widely studied [5]. Its applications are numerous due to the wide input voltage and load regulation range, improved reliability, continuous input current, and soft-switching possibilities with modified control algorithms. Nevertheless, the full-bridge converter could be an excessive solution for small power or low-voltage high-current applications due to the high number of semiconductor elements and cost issues.

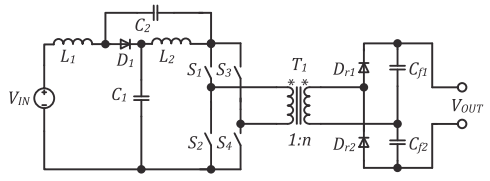

Fig. 1. qZS based galvanically isolated full-bridge DC-DC converter

There are IS DC-DC converter topologies with reduced number of switches that could be used in low power or low-voltage applications. To simplify the topology, the full-bridge switching stage could be replaced with that of push-pull. Such converters were described in [6] and [7]. They comprise only two switches that are connected to the common ground. The main drawbacks of that solution are: two times higher voltage stress of switches and an additional primary winding of the transformer. The full-bridge switching stage could be replaced with that of the symmetrical half-bridge, but it requires a more complicated IS network with a higher number of passive elements [8]. Another possibility is to use single-switch topologies. Different single-switch topologies have shown high performance in PFC [9] and low power applications [10], electronic lamp ballasts [11], renewable energy systems [12], and low-voltage applications [13].

There are three main classes of galvanically isolated IS DC-DC converter topologies depending on the element that transfers energy from the input to the output side: transformer based, coupled inductor based, and with combined energy transfer [5]. Single-switch topologies are present only in the class of the coupled-inductor based IS converters. In these converters, inductors in the IS network serve as energy storage and as elements that transfer energy from the input to the output side. The qZS converter from this class is shown in Fig. 2*a*. It has shown wide input voltage regulation at an acceptable efficiency [14], [15]. This topology was derived from the conventional nonisolated single-switch qZS converter shown in Fig. 2*b*. Low number of elements results in a relatively high input current ripple and complicated design of the coupled inductor T_1. Nonisolated IS DC-DC converter topologies could also provide high voltage step-up [16], but isolated solutions seem to be more efficient and safe when the input and the output voltage differ to a great extent.

A new single-switch galvanically isolated qZS DC-DC converter is proposed and experimentally verified in this paper. It was derived from the conventional single-switch qZS converter (Fig. 2*b*). In this case qZS inductors are used only as energy storage elements and, therefore, they ensure continuous input current with low ripple. Discrete transformer performs galvanic isolation and energy transfer. The topology proposed could be classified as the simplest in the class of transformer based galvanically isolated IS DC-DC converters.

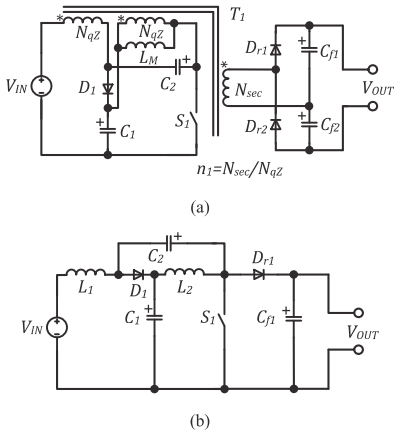

Fig. 2. qZS single-switch DC-DC converters: galvanically isolated coupled inductor based with a single inductor (a) and conventional nonisolated (b).

II. Single-Switch Quasi-Z-Source DC-DC Converter

A. Topology Description

The proposed step-up qZS DC-DC converter is shown in Fig. 3. It comprises: a qZS network that consists of inductors L_1, L_2, capacitors C_1, C_2, and diode D_1; power switch S_1; DC blocking capacitor C_b; isolation transformer T_1, Voltage Doubler Rectifier (VDR) composed from diodes D_{r1}, D_{r2} and capacitors C_{f1}, C_{f2}. A blocking capacitor in series with the primary winding of the transformer is required to isolate the DC component of the transformer input voltage, thus avoiding the transformer saturation.

B. Generalized Operating Principle

Operating principle of the topology described in Fig. 4 contains two switch states during the switching period T:

1) Off-state during $[t_1;t_2]$: diode D_1 is conducting, qZS inductors are discharging, while qZS capacitors are charging; diode D_{r1} is conducting, diode D_{r2} is reverse biased; capacitor C_{f1} is charging, while C_{f2} is discharging with the load current.

2) On-state during $[t_2;t_3]$: diode D_1 is reverse biased, qZS inductors are charging, while qZS capacitors are discharging; diode D_{r2} is conducting, diode D_{r1} is reverse biased; capacitor C_{f2} is charging, while C_{f1} is discharging with the load current.

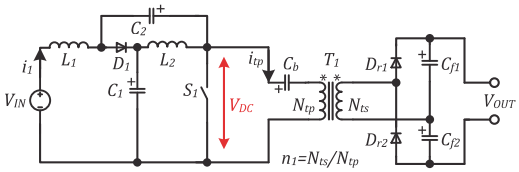

Fig. 3. Single-switch galvanically isolated qZS DC-DC converter

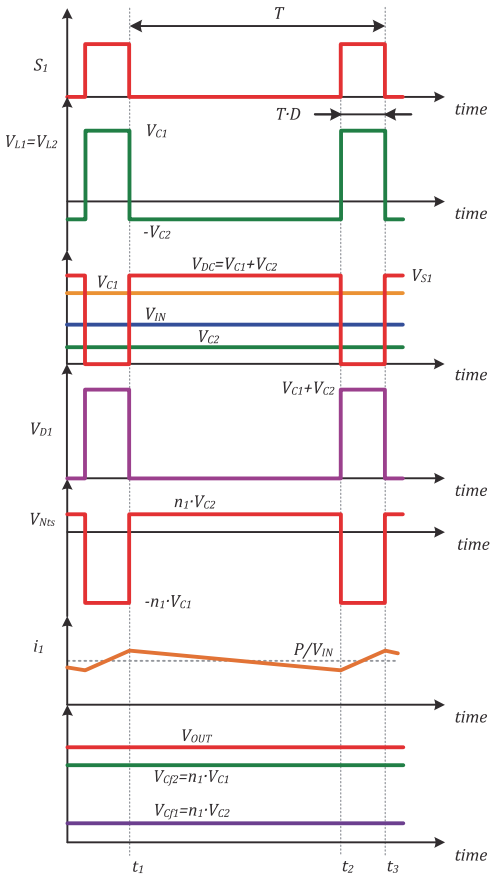

Fig. 4. Idealized current and voltage waveforms of the proposed converter

The duty cycle D defines DC voltage gain. It is equivalent to the shoot-through state in the full-bridge qZS DC-DC converter [4]. Peak value of the intermediate DC-link voltage V_{DC}, i.e. voltage stress of the switch S_1 and diode D_1, could be calculated as

$$V_{DC} = \frac{V_{IN}}{1-2\cdot D} = B\cdot V_{IN}, \qquad (1)$$

where V_{IN} is the input voltage of the converter, D is the duty cycle of S_1, and B is the input voltage boost factor (B=1/(1-2·D)). Unipolar pulsating voltage V_{DC} supplies the primary winding of the transformer T_1 with turns ratio $n_1 = N_{ts}/N_{tp}$. Operation principle of the converter strongly depends on the voltages of the qZS capacitors:

$$V_{C1} = \frac{V_{IN}\cdot(1-D)}{1-2\cdot D}; V_{C2} = \frac{V_{IN}\cdot D}{1-2\cdot D}. \qquad (2)$$

From Fig. 4 and (2) it can be concluded that the average voltage of the V_{DC}, i.e. voltage of the capacitor C_b, equals V_{C1}. It means that the primary winding of the transformer is supplied with non-symmetrical AC voltage with the positive peak value equal to V_{C2} and the negative peak value equal to $-V_{C1}$. Asymmetrical voltage results in the asymmetrical voltage across the VDR capacitors, similar to the qZS capacitors:

$$V_{Cf1} = n_1 \cdot V_{C2} = \frac{n_1 \cdot V_{IN} \cdot D}{1-2 \cdot D}, \tag{3}$$

$$V_{Cf2} = n_1 \cdot V_{C1} = \frac{n_1 \cdot V_{IN} \cdot (1-D)}{1-2 \cdot D}. \tag{4}$$

From (2)-(4) we can find the DC voltage gain:

$$G = \frac{V_{IN}}{V_{OUT}} = \frac{n_1}{1-2 \cdot D}. \tag{5}$$

The proposed converter can operate with continuous current within a wide range of voltage and load if inductors are properly dimensioned [17]. As compared to the full-bridge qZS DC-DC converter, the topology proposed has two times lower operating frequency of the qZS network, and two times lower DC voltage gain. This will lead to two times higher values of qZS components if the same voltage and current ripple is maintained. Also, the isolation transformer requires two times more turns in the secondary winding to maintain the same DC voltage gain. Thus, the converter proposed is simple and cheap in its implementation as compared to other transformer based galvanically isolated IS DC-DC converters.

C. Topology Improvement Possibility

The converter proposed requires higher turns ratio n_1 than that of the full-bridge reference topology. It usually results in higher leakage inductance and secondary winding capacitance, and complicated design of the transformer. Implementation of novel combined energy transfer principle recently proposed for galvanically isolated IS DC-DC converters could improve the performance of the proposed topology [18]. The improved topology shown in Fig. 5 was derived by replacement of the inductor L_2 with the coupled inductor T_2 with turns ratio n_2. Secondary windings of T_1 and T_2 are connected in series since the voltages of their primary windings are equal. Required turns ratio could be distributed between the two magnetic elements and thus it will decrease parasitic parameters, or improve the DC voltage gain of the converter. This modification will result in higher current ripple in the second qZS inductor (T_2), which could be limited within an acceptable range if $n_1 > n_2$. DC voltage gain of the improved topology with combined energy transfer could be calculated as:

$$G = \frac{(n_1 + n_2)}{1-2 \cdot D}. \tag{6}$$

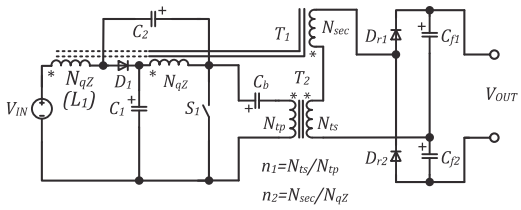

Fig. 5. Single-switch galvanically isolated qZS DC-DC converter with combined energy transfer

Moreover, the input inductor L_1 could be replaced with an additional winding of the coupled inductor T_1 with N_{qZ} turns, as shown in Fig. 5.

III. Simulation and Experimental Study

First, theoretical results on the DC voltage gain and the general operating principle were verified with simulation software PSIM. Simulation parameters selected on the basis of the parameters of the experimental prototype build are presented in Table I.

Simulation results are shown in Fig. 6. Input voltage equal to 25 V and duty cycle $D = 0.3$ should have resulted in 250 V

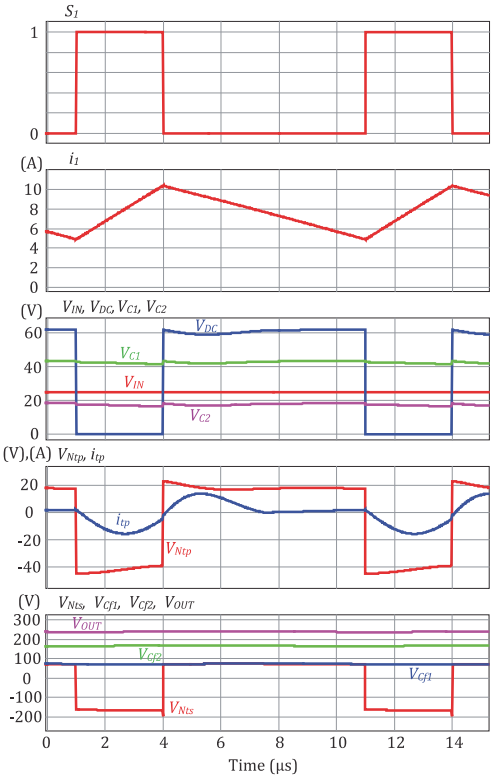

Fig. 6. Simulation results of the proposed topology

at the output and V_{DC} = 62.5 V. Output voltage obtained in the simulation is slightly lower (V_{OUT} = 240 V) due to the influence of the transformer leakage inductance. Capacitors of the VDR are charged asymmetrically, as it was predicted analytically. Input current ripple is roughly 6 A. Also, voltages of qZS capacitors correspond to the values calculated from (2): V_{C1} = 43.75 V and V_{C2} = 18.75 V. In most of applications, the regulation range required is not more than 1:3. This corresponds to triple voltage step-up on the input qZS network. Higher boost factor will lead to low efficiency; therefore, in practice the duty cycle is limited to D ≤ 0.33. Then, the voltage of the capacitor C_2 is always lower than the input voltage.

Real isolation transformers have some leakage inductance. It can form series resonant circuit with the blocking capacitor C_b. Simulation results showed that series resonance was achieved, since the current of the transformer primary winding is sinusoidal. This means that soft-switching commutation of the switch S_1 could be achieved if resonant circuit is properly designed, preferably with no additional elements.

Further verification was done experimentally. A small-scale experimental prototype with a rated power 200 W was designed and assembled in accordance with the schematic shown in Fig. 3. All parameters correspond to the nomenclature are stated in Tables I and II.

The qZS network is based solely on SMD components. The qZS inductors were implemented with low-profile SMD inductors IHLP-6767GZ from Vishay: two 47 uH inductors in parallel for each qZS inductor. The isolation transformer is custom made using the ETD34 core of N87 ferrite from Epcos. Measured leakage and magnetizing inductances correspond to the data in Table I. The qZS capacitors were implemented with the parallel connection of multilayer ceramic capacitors. Each qZS capacitor comprises twelve capacitors with capacitance 2.2 µF rated for voltage 100 V in SMD1210 case from Murata. The same capacitors were used in series-parallel connection 3x3 to obtain 2.2 µF capacitance of each VDR capacitor. All diodes are Schottky diodes: Si based in the low-voltage input side and SiC based in the high-voltage output side.

Measured waveforms of voltages and currents in the experimental prototype are shown in Fig. 7. The topology proposed features continuous input current and wide input voltage regulation by performing step-up to the required DC link voltage (in the experiment B = 2.5). Moreover, series resonance was achieved in the primary winding of the transformer that ensures soft-switching of the output VDR diodes. Slight difference between the simulated and the measured output voltage was observed: 230 V in contrast to 240 V obtained during the simulation study, while theory predicts 250 V. It is caused mostly by power losses in converter components and the influence of leakage inductance of the isolation transformer. Series resonant frequency in the prototype slightly differs from that in the simulation model mostly due to capacitance variations of the C_b under the DC bias. Experimental waveforms are in good agreement with the theoretical and simulation results.

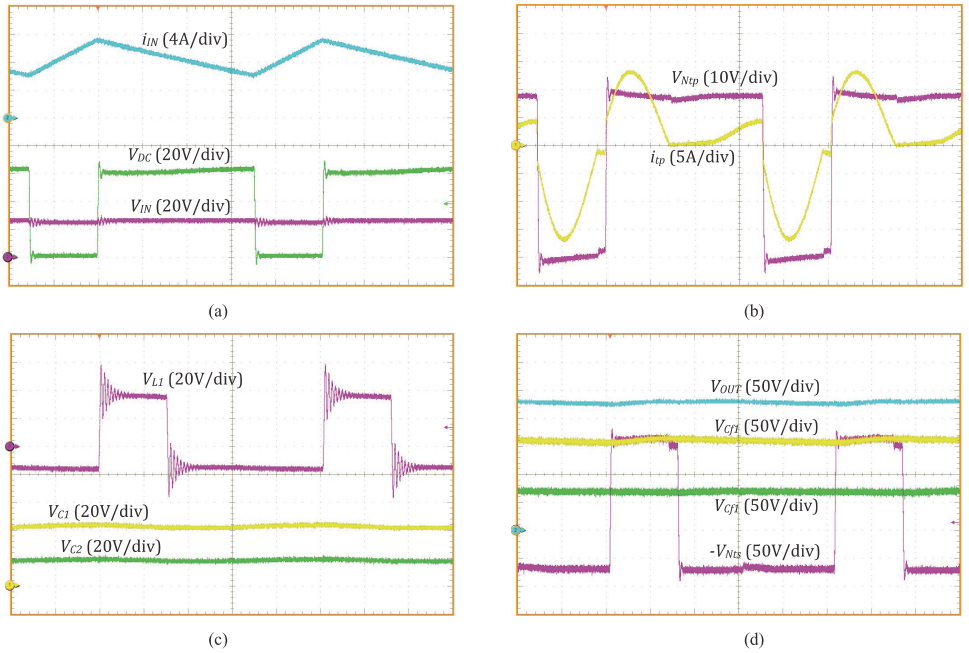

Fig. 7. Experimental waveforms of the proposed topology: input voltage, input current and intermediate DC-link voltage (a), voltage and current of the transformer primary winding (b), voltage of the qZS inductor, and qZS capacitors (c), and voltage of the transformer secondary winding, voltages of the VDR capacitors and output voltage of the converter (d) in time scale 2 µs/div.

TABLE I.
SIMULATION PARAMETERS OF THE QZS SINGLE-SWITCH DC-DC CONVERTER

Parameter	Symbol	Value
Input voltage, V	V_{IN}	25
Average input current, A	I_{IN}	8
Output voltage, V	V_{OUT}	240
Duty cycle of S_1	D	0.3
Switching frequency, kHz	f_{sw}	100
Transformer turns ratio	n	4
Transformer magnetizing inductance, µH	-	30.8
Transformer leakage inductance, µH	-	0.3
Capacitance of qZS capacitors, µF	C_1, C_2	26.4
Inductance of qZS inductors, µH	L_1, L_2	23
Capacitance of the DC blocking capacitor, µF	C_b	5.5
Capacitance of VDR capacitors, µF	C_3, C_4	2.2

TABLE II.
SPECIFICATIONS OF SEMICONDUCTORS USED IN THE EXPERIMENT

Component	Type	Specifications
S_1	IR IRFB4610PBF	V_{DS}=100 V; $R_{DS(on)}$=11 mΩ I_D=52 A, Q_g=90 nC, R_g=1.5 Ω
D_1	Vishay V60D100C	V_{RRM}=100 V; V_F=0.66 V $I_{F(AV)}$=2x30 A (common cathode)
D_{r1}, D_{r2}	CREE C3D02060E	V_{RRM}=600 V; V_F=1.8 V $I_{F(AV)}$=4 A

CONCLUSIONS

The converter proposed extends the family of the galvanically isolated impedance source DC-DC converters by adding a new switching stage type into the two classes of converters: the transformer based and that with combined energy transfer with small modification. Other impedance-source networks could be utilized based on the proposed principle of topological derivation.

The converter requires only one control channel and a single transistor driving circuit. It has inherited the continuous input current and a wide input voltage and load regulation range from the qZS converters. It features two times lower DC voltage gain and operating frequency of the qZS network as compared to the full-bridge or push-pull qZS DC-DC converters. Therefore, it requires two times higher qZS component values and transformer turns ratio. Moreover, the series resonance is achievable by use of the DC blocking capacitor and the leakage inductance of the isolation transformer's primary winding.

In the experimental verification, the prototype with a rated power of 200 W was used. It has corroborated the theoretical and simulation results. The converter proposed suits for low power or low-voltage applications, where the price of implementation or the number of switches is crucial.

Further research will focus on the analysis of the resonant switching processes and possibilities of soft switching in semiconductor elements of the proposed converter.

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CCM and DCM Analysis of Quasi-Z-Source Derived Push-Pull DC/DC Converter

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Abstract: This paper presents a steady state analysis of the operation modes of the quasi-Z-source (qZS) derived push-pull DC/DC converter topology. It was derived by the combination of the qZS network and coupled inductors. The output stage of the converter consists of a diode bridge rectifier and an LC-filter. This topology provides a wide regulation range of the input voltage and galvanic isolation. These features fit the requirements for the integration systems of renewable energy sources, such as PV panels, variable speed wind turbines, and fuel cells. A converter can operate in continuous (CCM) and discontinuous conduction mode (DCM). Switching period is divided into four and six intervals for CCM and DCM, respectively. Equivalent circuits and analytical expressions for each interval are presented. The DC gain factor for each mode is derived. To simplify our analysis, coupled inductors were substituted with a model that consists of an ideal transformer and magnetizing inductance. Leakage inductances are neglected because the coupling coefficient in this topology should be close to unity. In DCM the converter operation depends on the active duty cycle and the duty cycle of the zero current condition. Two solutions are possible for the DC gain factor in DCM. It is theoretically impossible to achieve the unity DC gain factor in DCM if the turns ratio of coupled inductors is equal to or more than one. The proposed topology was simulated with PSIM software in two operating points. Experimental verification proves our theoretical and simulation results.

Keywords: DC/DC converter, quasi-Z-source converter, galvanic isolation, renewable energy, steady state analysis.

Analiza CCM in DCM Push-Pull DC/DC pretvornika z impedančnim prilagodilnim vezjem

Izvleček: Članek opisuje statično analizo delujočih stanj push-pull DC/DC pretvornika z impedančnim prilagodilnim vezjem (qZS). Izveden je s kombinacijo qZS omrežja in sklopljenih tuljav. Izhodna stopnja pretvornika je sestavljeno iz diodnega usmerniškega mostiča in LC filtra. Topologija omogoča široko regulacijsko območje in galvansko ločitev. Lastnosti ustrezajo zahtevam integriranih sistemov obnovljivih virov energije, kot so PV moduli, vetrne turbine s spremenljivo hitrostjo in gorivne celice. Pretvornik lahko deluje v neprekinjenem (CCM) ali prekinjevalnem (DCM) prevodnem režimu. Perioda preklapljanja je razdeljena na štiri ali šest intervalov za CCM oziroma DCM. Predstavljeno je ekvivalentno vezje in analiza za vsak interval ločeno. Za vsak način je izračunano faktor DC ojačenja. Za poenostavljeno analizo so bili, za sklopljene tuljave, uporabljeni modeli z idealnim transformatorjem in magnetno induktivnostjo. Uhajalne induktivnosti so zaradi enotnosti koeficienta enotnosti v tej topologiji zanemarjene. Pri DCM je delovanje odvisno od aktivnega obratovalnega ciklusa in obratovalnega ciklusa pri ničelnem toku. Možni sta dve rešitvi za DC ojačenje pri DCM. Teoretično je nemogoče doseči enotno ojačenje pri DCM če je razmerje ovojev sklopljenih tuljav večje ali enako ena. Predlagana topologija je bila simulirana s programskim paketom PSIM v dveh točkah delovanja. Ekperimentalen preizkus potrjuje teorijo in rezultate simulacij.

Ključne besede: DC/DC pretvornik, impedančno prilagodilno vezje, galvanska ločitev, obnovljivi viri, statična analiza

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1 Introduction

Quasi-Z-source inverters (qZSIs) providing logical improvement of Z-source inverters were proposed in 2008 [1]. QZSIs extend the family of single stage buck-boost inverters. The concept of the QZSI provides improved reliability due to high EMI withstandability, wide input voltage regulation possibility, and continuous input

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current. These features make the qZSI appropriate for the realization of renewable energy systems (PV panels, fuel cells, wind turbines, etc.) [2]-[5] and electric vehicle applications [6]. Output voltage of the renewable energy sources (RES) usually is by far lower than grid voltage. An intermediate DC/DC converter can be used for voltage stabilization when high step-up is needed for RES integration into the grid [7-9]. DC/DC qZSI-based converters have been widely used because of their good performance as voltage matching converters that interconnect the RES and the grid-tied inverter [10]-[12].

The recent push-pull converter derived from the quasi-z-source (qZS) concept is shown in Fig. 1 [13]. This topology has ample opportunities for DC gain regulation [14]. Continuous input current can be achieved in a wide range even for the discontinuous conduction mode (DCM) in branches. The converter contains small component count and only two active switches that lead to a simple control circuit. Topology derivation is based on the combination of two qZS networks implemented with two three-winding coupled inductors.

The converter utilizes two qZS networks: C_1, C_2, D_1, TR_1 and C_3, C_4, D_2, TR_2, as shown in Fig. 1. Three-winding coupled inductors TR_1 and TR_2 provide galvanic isolation and store energy in the form of equivalent magnetizing current (i.e. field in the core of the coupled inductors). Transistors T_1 and T_2 work interleaved. The turn-on state of the transistor corresponds to the shoot-through behavior of the qZS network. Capacitors of the qZS network transfer part of the stored energy to the coupled inductor and the output load during the equivalent shoot-through state. Voltage across the primary windings can be described similarly to that of the conventional qZS network. Current in the primary windings of the coupled inductors differs from the current in the conventional qZS network due to the energy transfer process in the coupled inductors. From the input side the converter looks like two independent branches. These branches are connected in series by means of secondary windings. Summarized voltage of the secondary windings $v_S(t)$ is applied to the diode bridge rectifier $D_3 \ldots D_6$. Rectified voltage feeds the output load with the rectified voltage through the LC-filter L_f, C_f. The frequency of the current ripple of the input current and the output inductor current is twice higher than the switching frequency of the transistors. Voltage regulation is achieved by the adjusting of the turn-on state (active) duty cycle of the transistor.

The aim of this article is to present an analytical description for possible operation modes of the qZS derived push-pull converter. Like most of step-up switching power converters, the investigated topology can operate in the continuous conduction mode (CCM) and DCM. In DCM the transistors and diodes of the qZS networks suffer from high voltage stress. DCM occurs at low DC gain and low input power. The DC gain characteristic depends strongly on the operation mode. This paper is based on our earlier preliminary version [15] and includes substantially revised theoretical analysis and additional experimental results, not presented there.

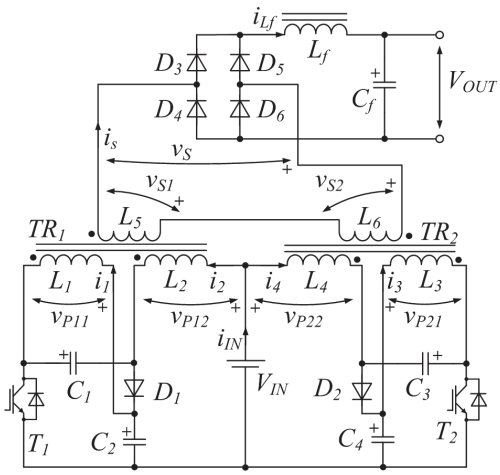

Figure 1: qZS-derived push-pull converter topology.

Several assumptions should be made for our further analysis. In this topology a coupled inductor should have the coupling coefficient close to unity. Primary windings should have an equal number of turns N_{12}. It means that in each qZS network voltages across the primary windings are equal: $v_{P11}(t) = v_{P12}(t)$, $v_{P21}(t) = v_{P22}(t)$. The secondary winding utilizes N_3 turns. The turns ratio $k = N_3/N_{12}$ defines the minimum achievable DC gain. Voltage across the secondary winding depends on the turns ratio and the voltage of the primary windings: $v_{S1}(t) = k \cdot v_{P11}(t)$, $v_{S2}(t) = -k \cdot v_{P21}(t)$, $v_{S1}(t) + v_{S2}(t) = v_S(t)$. In this case coupled inductors can be substituted with a simplified model that consists of the magnetizing inductance L_M reflected to one of the windings and an ideal transformer with N_{12}:N_3 primary to secondary turns ratio. Also, in any mode currents in the primary windings of each coupled inductor are equal: $i_1(t) = i_2(t)$, $i_3(t) = i_4(t)$. Let us assume that the voltage ripple of all capacitors in the converter is well below the corresponding average voltage. These assumptions and the symmetry of branches result in equal average voltages across the capacitors: $V_{C1} = V_{C3}$, $V_{C2} = V_{C4}$. Let us assume that the current of the filter inductor $i_{Lf}(t)$ is continuous in any mode. None of the losses are considered in this article. It means that the input power P and the output power are equal: $I_{OUT} = I_{Lf} = P/V_{OUT}$. The lower case letter of the voltage and the current corresponds to an instantane-

ous value, and the upper case letter or angle brackets correspond to an averaged (or constant in some cases) value. The input power is represented as P. For the symmetry operation of the branches, each of them should operate at half of the rated power: $I_4 = I_2 = P/(2 \cdot V_{IN})$.

2 Circuit Steady-State Analysis in CCM

Current and voltage waveforms for an idealized converter in CCM are shown in Fig. 2. The figure shows that the switching period of the converter T can be divided into four time intervals: two equal active intervals during which only one of the transistors is turned on (i.e. active states with the time duration t_A each) and two inactive intervals when both transistors are not conducting (i.e. zero state, t_0 each):

$$\frac{t_A}{T} + \frac{t_0}{T} = D_A + D_0 = 0.5. \tag{1}$$

where D_A is the duty cycle of an active state and D_0 is the duty cycle of a zero state. It is clear from (1) that $D_A < 0.5$ and $D_0 < 0.5$. In CCM, as well as in DCM, the current $i_{Lf}(t)$ has a double switching frequency ripple. Also, in both modes $i_{Lf}(t)$ always rises during active states and falls during a zero state.

Figure 3a shows the equivalent circuit of the converter for the time interval *t1-t2* when the transistor T_1 is turned on, diode D_1 is blocked and D_2 is conducting. Equations (2)-(6) describe the behavior of the converter during this time interval.

$$v_{C1}(t) = v_{C2}(t) - V_{IN}, \tag{2}$$

$$v_{C2}(t) = v_{P11}(t) = L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \tag{3}$$

$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) + k \cdot i_{Lf}(t)\right), \tag{4}$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \tag{5}$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C2}(t) + v_{C3}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right), \tag{6}$$

where $v_{C1}(t)$, $v_{C2}(t)$, $v_{C3}(t)$, $v_{C4}(t)$ are the capacitor voltages, $v_{S1}(t)$ and $v_{S2}(t)$ are the voltages of the corresponding secondary windings of the transformer, $v_S(t)$ is the summarized voltage of the secondary winding applied to the rectifier, $i_1(t)$, $i_2(t)$, $i_3(t)$, $i_4(t)$ are the currents of the corresponding primary windings of the transformer, L_M is the magnetizing inductance of the coupled inductors, k is the turns ratio of the coupled inductors, and $i_{Lf}(t)$ is the current of the filter inductor L_f.

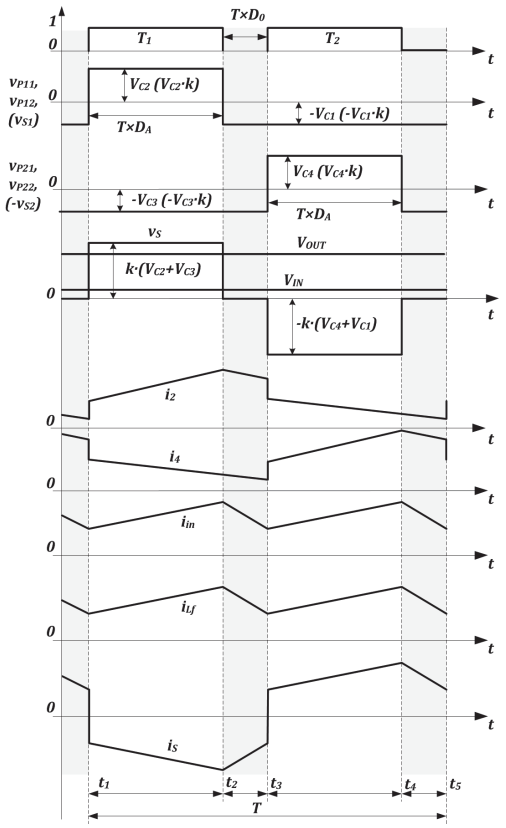

Figure 2: Generalized converter voltage and current waveforms during the operation in CCM.

During the interval t_2-t_3 both transistors are not conducting, diodes D_1 and D_2 are conducting. The equivalent circuit of the converter is depicted in Fig. 2b. Equations (7)-(11) describe the operation of the converter for that time interval. Summarized voltage of the secondary windings $v_S(t)$ is equal to zero if the voltage ripple of the qZS capacitors is negligible.

$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \tag{7}$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \tag{8}$$

$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) + k \cdot i_{Lf}(t)\right), \tag{9}$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \tag{10}$$

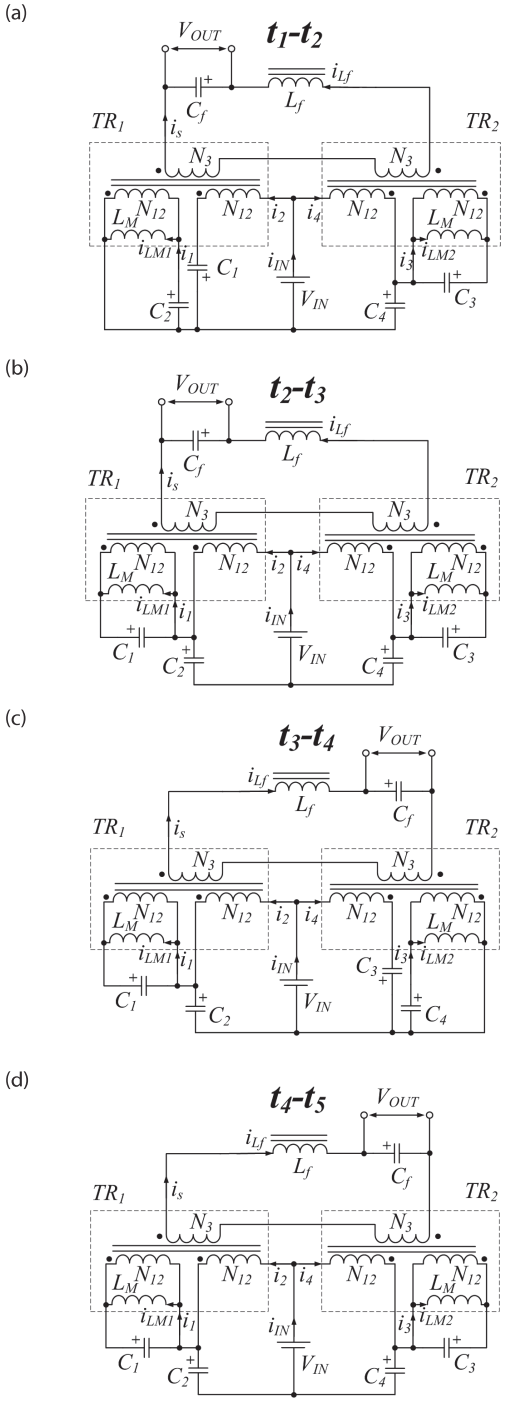

Figure 3: Equivalent circuits of the investigated converter in CCM.

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C3}(t) - v_{C1}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right) \approx 0. \quad (11)$$

Figure 2c depicts the equivalent circuit of the converter for the time interval t_3-t_4 when the transistor T_2 is turned on, the diode D_2 is reverse based and D_1 is conducting. Equations (12)-(16) define the operation of the converter during the time interval t_3-t_4:

$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) + k \cdot i_{Lf}(t)\right), \quad (12)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (13)$$

$$v_{C3}(t) = v_{C4}(t) - V_{IN}, \quad (14)$$

$$v_{C4}(t) = v_{P21}(t) = L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (15)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(-v_{C1}(t) - v_{C4}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) - 2 \cdot k \cdot i_{Lf}(t)\right). \quad (16)$$

During the interval t_4-t_5 both transistors are switched off, diode D_1 and diode D_2 are conducting. The equivalent circuit for the fourth interval is shown in Fig. 2b. Equations (17)-(21) define the behavior of the converter for the time interval t_4-t_5. Summarized voltage of the secondary windings $v_S(t)$ is equal to zero if the voltage ripple of the qZS capacitors is negligible. The fourth interval differs from the second in the direction of the current $i_{Lf}(t)$ via the secondary windings, i.e. $i_S(t)$ has an opposite sign.

$$v_{C1}(t) = -v_{P11}(t) = -L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) + k \cdot i_{Lf}(t)\right), \quad (17)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (18)$$

$$v_{C3}(t) = -v_{P21}(t) = -L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = -L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (19)$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \quad (20)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C3}(t) - v_{C1}(t)\right) = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - i_3(t) - i_4(t) + 2 \cdot k \cdot i_{Lf}(t)\right) \approx 0. \quad (21)$$

At the time moments t_1, t_3 and t_5 currents in the primary windings change by step:

$$\Delta i_2(t_1) = -\Delta i_4(t_1) = k \cdot i_{Lf}(t_1),$$

$$\Delta i_4(t_3) = -\Delta i_2(t_3) = k \cdot i_{Lf}(t_3),$$

$$\Delta i_2(t_5) = -\Delta i_4(t_5) = k \cdot i_{Lf}(t_5).$$

This step change could be explained by the change of the direction of the current $i_s(t)$. Also, these steps are equal because $i_{Lf}(t_1) = i_{Lf}(t_3) = i_{Lf}(t_5)$. These steps are not reflected in the input current because the steps of currents $i_2(t)$ and $i_4(t)$ compensate each other.

According to the voltage-second balance principle, the average voltage across the primary winding of the coupled inductor over one switching period equals zero. That can be used for the calculation of the average voltage across the qZS capacitors:

$$V_{P11} = \langle v_{P11}(t) \rangle = \frac{1}{T}\int_0^T v_{P11}(t)dt = 0, \quad (22)$$

$$V_{P21} = \langle v_{P21}(t) \rangle = \frac{1}{T}\int_0^T v_{P21}(t)dt = 0. \quad (23)$$

In order to solve Eqs. (22) and (23) we need to assume that the voltage across the capacitors is close to the average value over the switching period:

$$v_{C1}(t) \approx \langle v_{C1}(t) \rangle = V_{C1}, \quad (24)$$

$$v_{C2}(t) \approx \langle v_{C2}(t) \rangle = V_{C2}, \quad (25)$$

$$v_{C3}(t) \approx \langle v_{C3}(t) \rangle = V_{C3}, \quad (26)$$

$$v_{C4}(t) \approx \langle v_{C4}(t) \rangle = V_{C4}. \quad (27)$$

The following expressions are right for all the intervals according to Eqs. (24)-(27) and (2)-(21):

$$V_{C2} = V_{IN} + V_{C1}, \quad (28)$$

$$V_{C4} = V_{IN} + V_{C3}. \quad (29)$$

$$V_{C1} = V_{C3}, \quad (30)$$

$$V_{C2} = V_{C4}. \quad (31)$$

From Eqs. (22)-(31) it is easy to find expressions for the capacitor voltages:

$$V_{P11} = V_{C2} \cdot D_A - V_{C1} \cdot (1 - D_A) =$$
$$= D_A \cdot (V_{IN} + V_{C1}) - V_{C1} \cdot (1 - D_A) = 0,$$

$$V_{C1} = V_{C3} = \frac{D_A}{1 - 2 \cdot D_A} V_{IN}, \quad (32)$$

$$V_{C2} = V_{C4} = \frac{1 - D_A}{1 - 2 \cdot D_A} V_{IN}. \quad (33)$$

Using Eqs. (1)-(33) and considering all the abovementioned assumptions, the summarized voltage of the secondary windings of the coupled inductors could be analytically expressed for each time interval:
Time interval t_1-t_2:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot (V_{C2} + V_{C3}). \quad (34)$$

Time interval t_3-t_4:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = -k \cdot (V_{C1} + V_{C4}). \quad (35)$$

Time intervals t_2-t_3 and t_4-t_5:

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot (V_{C3} - V_{C1}) = 0. \quad (36)$$

In CCM the output voltage of the converter can be expressed as

$$V_{OUT} = \frac{1}{T}\int_0^T |v_{S1}(t) + v_{S2}(t)| \cdot dt =$$
$$= k \cdot \frac{2}{T}\int_0^{T \cdot D_A} (V_{C3} + V_{C2}) \cdot dt = \frac{N_3}{N_{12}} \cdot \frac{2 \cdot D_A}{1 - 2 \cdot D_A} \cdot V_{IN}. \quad (37)$$

The resulting DC voltage gain of the proposed DC/DC converter is

$$G = k \cdot \frac{2 \cdot D_A}{1 - 2 \cdot D_A}. \quad (38)$$

In Fig. 4 the DC voltage gain of the converter (38) is depicted as a function of an active state duty cycle for different turns ratios of the coupled inductors. As is seen, a very wide regulation range of the DC voltage gain could be achieved for the lossless system. Also, high step-up can be reached using coupled inductors with a high turns ratio. In real systems the DC voltage gain of the step-up converter usually is seriously influenced by the losses in the components, especially in semiconductors.

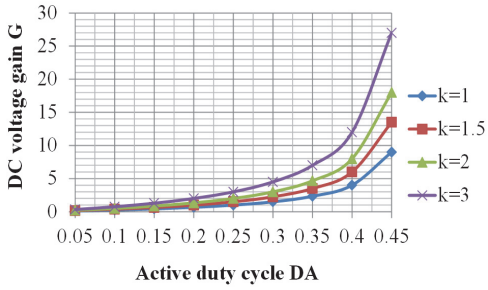

Figure 4: DC voltage gain G as a function of the active state duty cycle D_A for the proposed DC/DC converter operated in CCM.

3 Circuit Steady-State Analysis in DCM

In general, the converter operation mode is considered as DCM when the input current falls to zero. However, in the investigated topology, DCM will be considered as a mode when the current in the primary winding of the coupled inductor drops to zero. In DCM the input current can still remain continuous. Typical waveforms

for DCM are shown in Fig. 5. Two additional equivalent circuits that are needed for the analysis of DCM are shown in Figs. 6a and 6b. These figures correspond to the time intervals t'_1-t_2 and t'_3-t_4, respectively. During other time intervals converter operation is the same as for CCM. If the duty cycle of the DCM state γ less than the D_0 converter operation is almost similar to CCM.

Figure 6a shows the equivalent circuit of the converter during the time interval t'_1-t_2 when the transistor T_1 is turned on, diode D_1 is reverse based, and diode D_2 is not conducting. This mode is possible only if $\gamma > D_0$. Voltage is applied to the diode D_2: $v_{D2}(t) = v_{C3}(t) + \alpha$, where $\alpha = v_{P21}(t)$. Voltage α is constant during this time interval. Equations (39)-(43) describe the operation of the converter during this time interval when $i_3(t) = i_4(t) = 0$.

$$v_{C1}(t) = v_{C2}(t) - V_{IN}, \quad (39)$$

$$v_{C2}(t) = v_{P11}(t) = L_M \cdot \frac{di_{LM1}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - k \cdot i_{Lf}(t)\right), \quad (40)$$

$$v_{P21}(t) = v_{P22}(t) = \alpha = k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt}, \quad (41)$$

$$v_{C4}(t) = V_{IN} + v_{C3}(t), \quad (42)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(v_{C2}(t)\right) - k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt} = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(i_1(t) + i_2(t) - 2 \cdot k \cdot i_{Lf}(t)\right) \approx V_{C2} - \alpha. \quad (43)$$

Figure 6b shows the equivalent circuit of the converter for the time interval t'_3-t_4 when the transistor T_2 is conducting, the diode D_1 is not conducting, and the diode D_2 is reverse based. Voltage is applied to the diode D_1: $v_{D1}(t) = v_{C3}(t) + \alpha$, where $\alpha = v_{P11}(t)$. Equations (44)-(48) describe the behavior of the converter over this time interval considering that $i_1(t) = i_2(t) = 0$.

$$v_{P11}(t) = v_{P12}(t) = \alpha = k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt}, \quad (44)$$

$$v_{C2}(t) = V_{IN} + v_{C1}(t), \quad (45)$$

$$v_{C3}(t) = v_{C4}(t) - V_{IN}, \quad (46)$$

$$v_{C4}(t) = v_{P22}(t) = L_M \cdot \frac{di_{LM2}(t)}{dt} = \\ = L_M \cdot \frac{d}{dt}\left(i_3(t) + i_4(t) - k \cdot i_{Lf}(t)\right), \quad (47)$$

$$v_S(t) = v_{S1}(t) + v_{S2}(t) = k \cdot \left(-v_{C4}(t)\right) + k \cdot L_M \cdot \frac{di_{Lf}(t)}{dt} = \\ = k \cdot L_M \cdot \frac{d}{dt}\left(-i_3(t) - i_4(t) + 2 \cdot k \cdot i_{Lf}(t)\right) \approx -V_{C4} + \alpha. \quad (48)$$

3.1 DCM mode 1

If the duty cycle of the DCM state is less than the duty cycle of the zero state ($0 < \gamma < D_0$), the operation of the converter will remain unchanged. In this case the behavior of the converter could be described by Eqs. (2)-(6).

3.2 DCM mode 2

In case the duty cycle of the DCM state lies in the range $D_0 < \gamma < 0.5$, the average voltage of the qZS capacitors and the DC voltage gain of the converter should be recalculated. It can be done using Fig. 5, taking into account (22)-(31), and assuming that α is equal to zero in order to simplify the calculations:

$$V_{P11} = V_{C2} \cdot D_A - V_{C1} \cdot (1 - D_A - \gamma + D_0) = \\ = D_A \cdot (V_{IN} + V_{C1}) - V_{C1} \cdot (1.5 - \gamma - 2 \cdot D_A) = 0,$$

$$V_{C1} = V_{C3} = \frac{2 \cdot D_A}{3 - 2 \cdot \gamma - 6 \cdot D_A} V_{IN}, \quad (49)$$

$$V_{C2} = V_{C4} = \frac{3 - 2 \cdot \gamma - 4 \cdot D_A}{3 - 2 \cdot \gamma - 6 \cdot D_A} V_{IN}. \quad (50)$$

The output voltage of the converter operated in DCM when $D_0 < \gamma < 0.5$ can be expressed as

$$V_{OUT} = \frac{1}{T} \int_0^T \left| v_{S1}(t) + v_{S2}(t) \right| \cdot dt \approx \\ \approx k \cdot \frac{2}{T} \left(\int_0^{T \cdot (0.5 - \gamma)} \left(V_{C2} + V_{C3}\right) \cdot dt + \int_{T \cdot (0.5 - \gamma)}^{T \cdot D_A} V_{C2} \cdot dt \right) = \\ = \frac{N_3}{N_{12}} \cdot \frac{8 \cdot D_A \cdot (1 - \gamma - D_A)}{3 - 2 \cdot \gamma - 6 \cdot D_A} \cdot V_{IN}. \quad (51)$$

The resulting DC voltage gain of the proposed DC/DC converter is

$$G = k \cdot \frac{8 \cdot D_A \cdot (1 - \gamma - D_A)}{3 - 2 \cdot \gamma - 6 \cdot D_A}. \quad (52)$$

In the DCM, when $\gamma = 0.5$ each branch consumes current only during $T/2$. In this case, time t_1 equals t'_1, and time t_3 equals t'_3. The input current of the converter is in the boundary conduction mode and reaches zero twice per switching period at the time moments t_1 and t_3. Current steps occur due to the change of the sign of the current $i_S(t)$ at the same time moments.

The condition $\gamma > 0.5$ is theoretically possible when the converter needs to operate at very low input power compared to the rated power value. This mode corresponds to the discontinuous input current. It should be avoided because of high overvoltage across the power semiconductor components. This mode could be avoided practically due to the losses in the converter. Also, renewable energy systems usually require high step-up at low power, or do not require ultra-light-load operation. On the other hand, in this mode the converter needs enormous inductance at the output filter

to satisfy the assumption about the continuous inductor current.

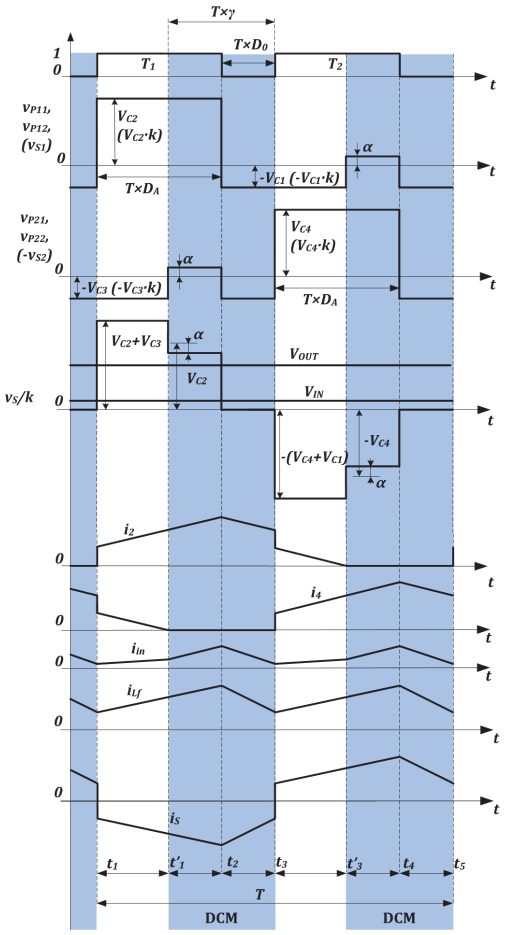

Figure 5: Generalized converter voltage and current waveforms during the operation in DCM.

4 Experimental Verification

Theoretical assumptions were verified by means of modeling. The model was rated for the power of 600 W in compliance with the topology shown in Fig. 1. Component values and given modeling conditions are listed in Table I. Simulation results are shown in Figs. 8 and 10. In the first case, the model of the converter operates in CCM (input voltage of 70 V and D_A = 0.43), while in the second modeling, the converter operates in DCM (input voltage of 250 V and D_A = 0.25).

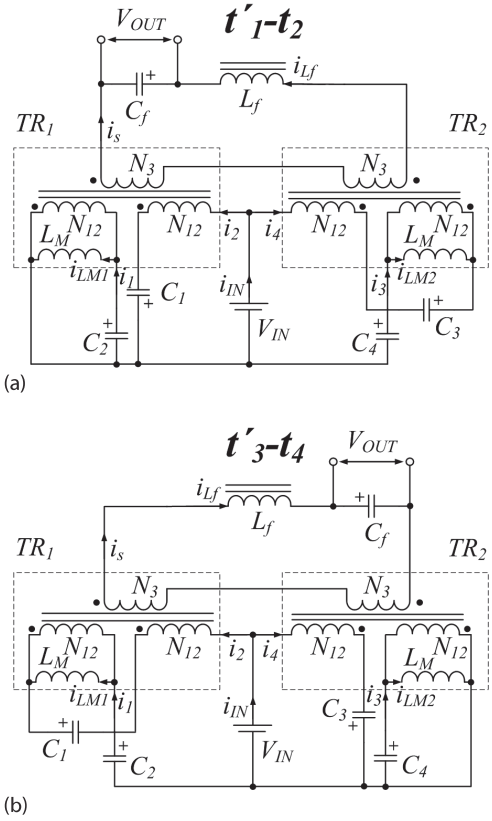

Figure 6: Additional equivalent circuits of the investigated converter for DCM.

Theoretical and simulation results were verified using a 600 W laboratory prototype, which is shown in Fig. 7. It was assembled in compliance with schematics in Fig. 1. Experimental waveforms including the input voltage are presented in Figs. 9 and 11. In the case of 70 V at the input, the converter operates in CCM. For CCM, experimental results are in good agreement with the theoretical assumption. On the other hand, when the input voltage equals 250 V, and the converter operates in DCM, the parasitic parameters in the experimental prototype cause major oscillations. Distinctions between the experimental and simulated waveforms are considerable.

Figure 12 shows experimentally measured curve of active state duty cycle D_A versus input voltage and DC voltage gain for constant output voltage 400 V and output power 600 W. CCM is achieved for input voltage below 150 V DC. Converter operates in DCM when input voltage is higher than 150 V DC. Measured curve has higher non-linearity in DCM, as it was expected.

Table 1: Operating Parameters and Passive Component Values of the Converter

Main operating parameters	Value
Minimal input voltage VIN, min	70 V
Maximal input voltage VIN, max	250 V
Desired output voltage VOUT	400 V
Nominal power P	600 W
Switching frequency fsw=1/T	100 kHz
Turns ratio of the isolation transformers N3:N12	1:1
Passive component values	
Capacitance value of the capacitors C1...C4	60 µF
Magnetizing inductance of the isolation transformers LM	1 mH
Inductance of the filter inductor Lf	1 mH
Capacitance of the filter capacitor Cf	220 µF

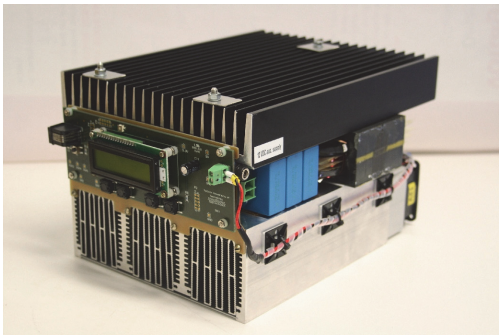

Figure 7: Converter prototype used for experimental verification.

5 Conclusions

The paper has presented a steady state analysis of the operation of the qZS derived push-pull DC/DC converter in the continuous and discontinuous conduction mode. The mathematical analysis provides a general solution for waveforms and values of voltage and current in the passive components. Some differences between the theoretical results and the simulation and experimental results are related to an idealized model (losses in components, leakage inductance are neglected). The converter reveals that the behavior in DCM is complicated. The DCM state duty cycle appears when half of the current ripple through the primary winding, defined by the magnetizing inductance, surpasses an average primary winding current defined by the load power. This mode of operation could occur at the gain factors closer to unity. This topology is a good solution

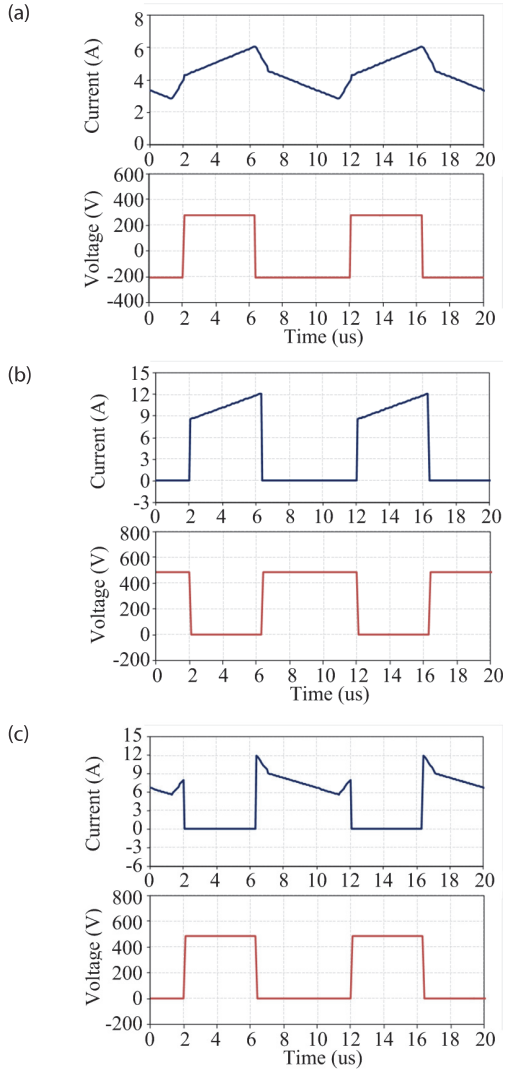

Figure 8: CCM simulated waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 70 V

for the integration of a variable voltage variable speed small wind turbine. In this case the converter operates with a lower gain at a higher power. This condition combined with the features of the converter could ensure operation in CCM in a wide range of power

The mathematical analysis was verified by means of the simulation software and the experimental prototype. As shown, the results are in good agreement with the theoretical predictions.

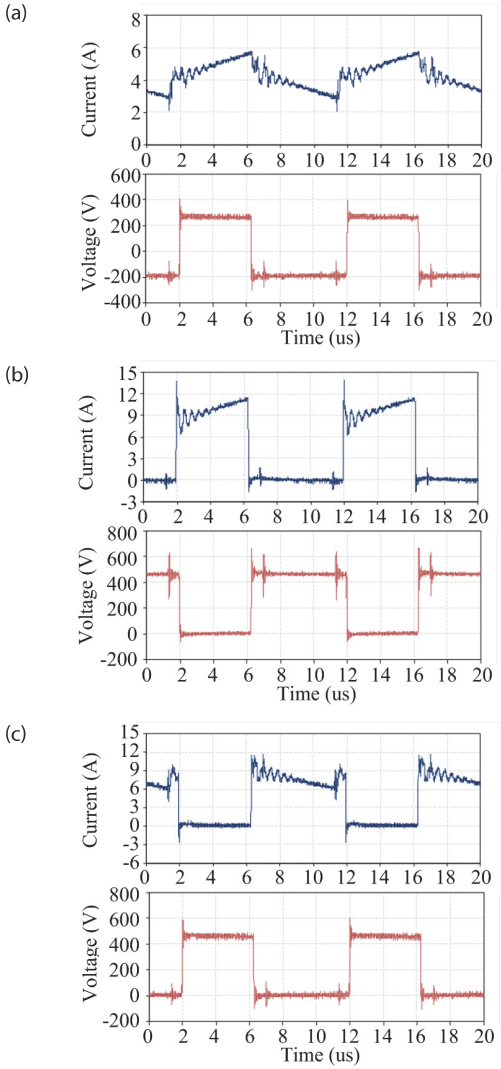

Figure 9: CCM experimental waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 70 V.

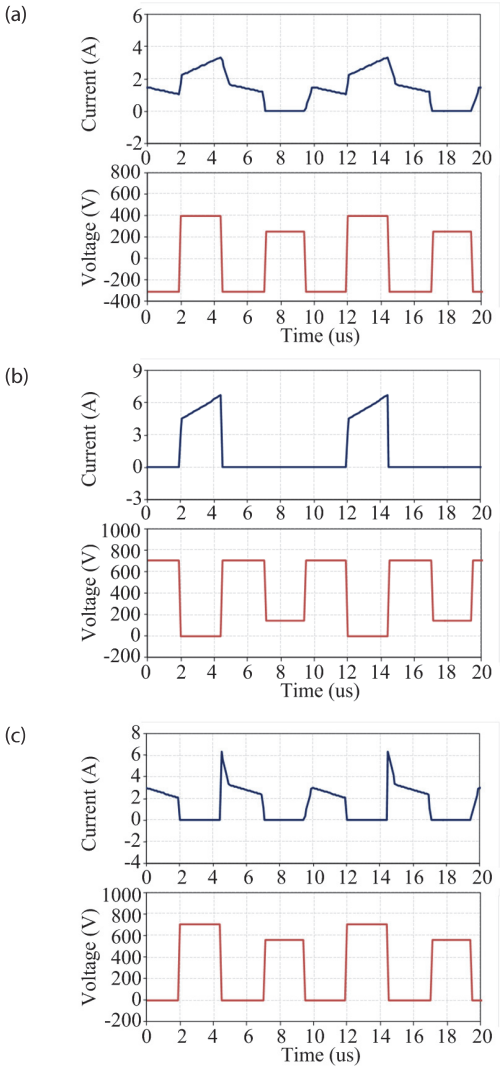

Figure 10: DCM simulated waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 250 V.

6 Acknowledgments

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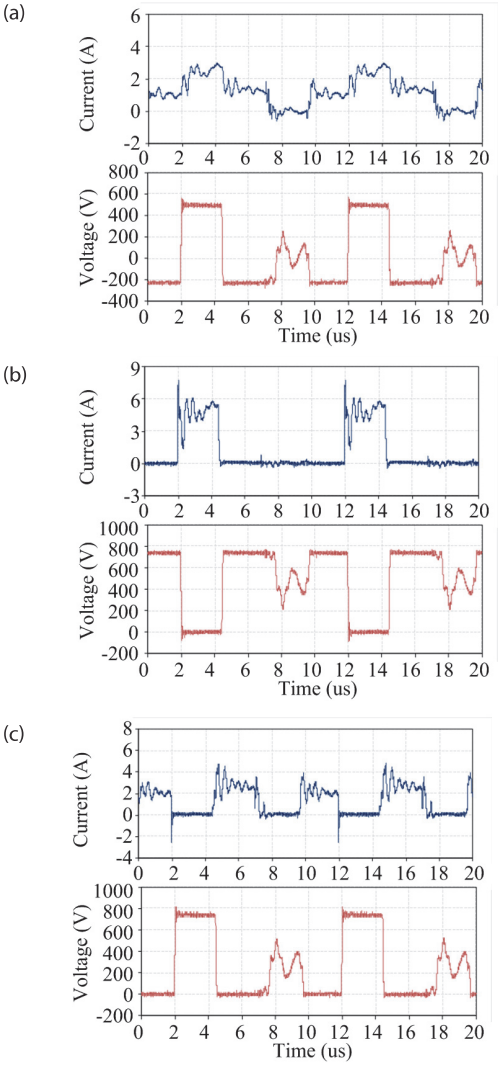

Figure 11: DCM experimental waveforms of the transformer primary (a), transistor (b) and qZS diode (c) at 600 W with the input voltage of 250 V.

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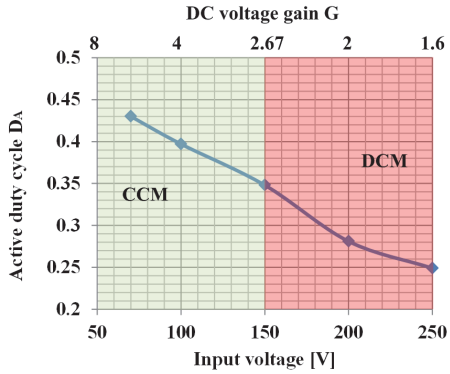

Figure 12: Experimentally measured active state duty cycle D_A versus input voltage and DC voltage gain.

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Novel Family of Quasi-Z-Source DC/DC Converters Derived from Current-Fed Push-Pull Converters

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Keywords

«DC power supply», «Emerging topology», «Interleaved converters», «Modulation strategy», «Renewable energy systems».

Abstract

This paper is devoted to the step-up quasi-Z-source dc/dc push-pull converter family. The topologies in the family are derived from the isolated boost converter family by replacing input inductors with the quasi-Z-source network. Two new topologies are proposed, analyzed and compared. Theoretical predictions are verified by means of simulations.

Introduction

Today renewable energy is a main trend of modern energy industry [1]. Fast growing and deep penetration of Renewable Energy Sources (RES) raises new challenges for energy conversion applications [2]. New converter topologies are needed for efficient interfacing into the power distribution grid of low voltage intermittent RES, like PV panels, fuel cells, etc. Quasi-Z-source DC/DC converters are reported as a suitable solution for RES applications [3]. They were derived from Quasi-Z-Source Inverters (qZSIs). QZSIs are the result of the improvement of Z-source inverters that have continuous input current and lower element stresses [4], [5].

A family of isolated current-fed push-pull converters consists of a current-fed push-pull converter and a two-inductor isolated boost converter shown in Fig. 1*a* and 1*b*, respectively [6],[7]. Previously they were used in power factor correction, telecommunication and battery charging applications [8]. Continuous input current and flux self-balancing also fit the requirements for energy use from RES. Typically the transformer performance is poor if a variation of the DC voltage gain factor is used because the power is transferred from the input to the output through the isolation transformer in narrow pulses. Fast growth of RES and electric transportation industries has shifted the researchers' attention to isolated current-fed push-pull topologies. Novel multi-phase [9] and soft-switching [10] - [11] current-fed push-pull converters have been recently proposed. This means that further research in this field is required.

These topologies can be improved with the implementation of quasi-Z-source (qZS) networks instead of input inductors. Also, the qZS principle enables improvement of the inrush current, which is a typical problem of the isolated current-fed push-pull converter family [6],[7]. The topologies proposed are shown in Fig. 2. All the inductors in the qZS networks are coupled in order to decrease the number

of bulky magnetic elements and current ripple, which leads to the increase of power density and efficiency. Output rectifier stage is implemented with the voltage doubler rectifier (VDR). This approach allows a decrease of the turns ratio of the isolation transformer and thus diminishes winding parasitic parameters [1].
Focus in this paper is on a novel power circuit topology family to be implemented for the front-end DC/DC converter in renewable energy applications. These topologies were derived from current-fed push-pull converters by the implementation of the quasi-Z-source networks instead of input inductors. The operation principle of the two proposed topologies is described and compared.

Proposed Converters

Fig. 2*a* shows the Quasi-Z-Source-Fed Push-Pull Converter (QZSFPPC), which contains the coupled inductor L_{qZ} with a magnetizing inductance L_M, capacitors C_1, C_2, a qZS diode D_{qZ}, two active switches T_1, T_2, a transformer TR_1 and a VDR based on diodes D_{r1}, D_{r2}, and capacitors C_{f1}, C_{f2}. To simplify the analysis, the equivalent circuit of the coupled inductor takes only the magnetizing inductance into account [12]. The isolation transformer TR_1 is substituted with the conventional equivalent circuit. It includes an ideal transformer, a magnetizing inductance L_{MT}, and two leakage inductances L_{lT}.
Early-access papers [13] and [14] appeared simultaneously with the review process of this article. They describe a converter that is very similar to the QZSFPPC. That converter has different implementation of the output voltage doubler stage. The bridge voltage doubler rectifier used in the QZSFPPC can provide slightly higher efficiency [15]. This article provides a more comprehensive analysis of current ripples in the steady state, while [14] is a more of an experimental study. Moreover, the QZSFPPC and the converter from [14] are further modifications of the converter proposed in [3] derived by replacing the bridge switching stage with the push-pull switching stage.
Fig. 2*b* shows the Interleaved Quasi-Z-Source-Fed Push-Pull Converter (IQZSFPPC), the topology of which is based on two magnetically coupled qZS networks. This coupling of the qZS networks is called a coupled qZS network. The IQZSFPPC contains a coupled inductor L_{qZ} presented with four equivalent leakage inductances L_{lk}, an ideal transformer, and a magnetizing inductance L_M, capacitors $C_1 \ldots C_4$, qZS diodes D_{qZ1}, D_{qZ2}, two active switches T_1, T_2, a transformer TR_1 and a VDR based on diodes D_{r1}, D_{r2}, and capacitors C_{f1}, C_{f2}. In this case the leakage inductances of the coupled inductor L_{qZ} define the current ripple and cannot be neglected [16]. Magnetizing inductance, i.e. coupling ratio, defines the current ripple in the windings. An equivalent circuit of the isolation transformer TR_1 consists of an ideal transformer, a magnetizing inductance L_{MT}, and a leakage inductance L_{lT}. The IQZSFPPC topology contains a considerably higher number of components, but voltage or current stresses are lower than those of the QZSFPPC. Therefore, the power density of both converters could be close.

Operation Principle and Steady State Analysis of the Proposed Converters

Both of the proposed topologies have the flux balancing in the isolation transformer and an ideal model of the transformer can be used for the steady state analysis. The leakage inductance should be considered when it is necessary to analyze the currents in the transformer windings and the output rectifier. To simplify the analysis, all the leakage inductances are assumed equal to L_{lk}. For the steady

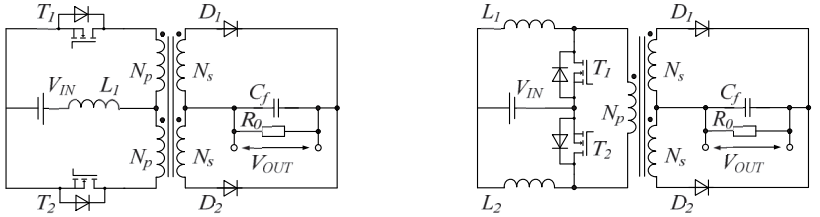

Fig. 1 – Isolated current-fed push-pull converter family: a) current-fed push-pull converter and b) two-inductor isolated boost converter.

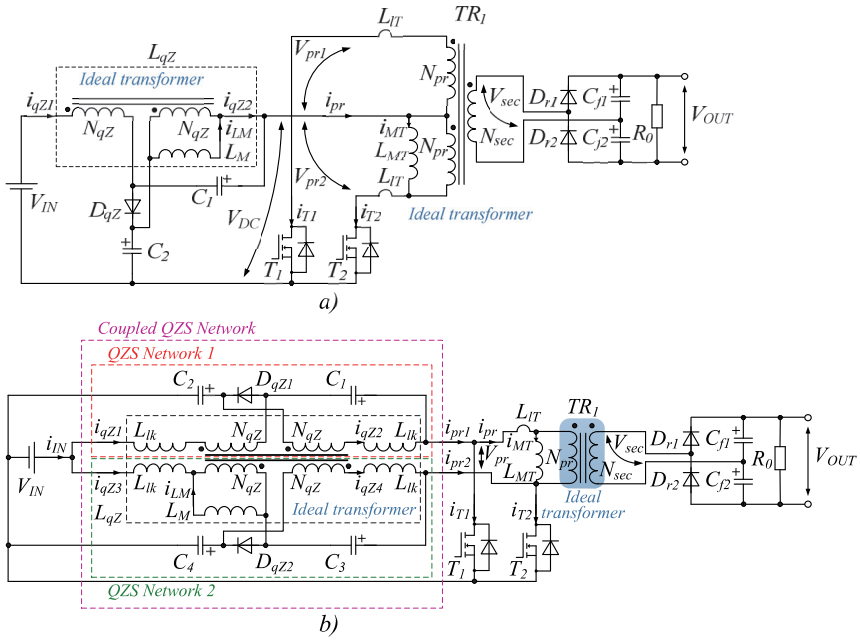

Fig. 2 – Topologies of the proposed quasi-Z-source-fed push-pull converter family: a) quasi-Z-source-fed push-pull converter and b) interleaved quasi-Z-source-fed push-pull converter.

state analysis the isolation transformer TR_1 is substituted with an ideal transformer due to the flux balance in the core: $L_{MT} \to \infty$, $L_{lT} \to 0$.

Operation Principle of the Proposed Quasi-Z-Source-Fed Push-Pull Converter

The switching period of the QZSFPPC can be separated into four intervals, as shown in Fig. 3*a*. The transistors work interleaved. Each of them is turned on during an active duty cycle $D_A > 0.5$. The converter works as a conventional push-pull if $D_A < 0.5$. Buck mode behavior depends on the real transformer leakage inductances. Converter steps up the input voltage if $D_A > 0.5$. In this case the gate signals of the transistors are overlapped during the duty cycle D_S twice per switching period $T = 1/f_{SW}$. During the time $D_S \cdot T$ the core flux remains constant. The ampere-turns of the primary windings cancel each other. Therefore it operates in the conditions equal to the conventional shoot-through mode in qZS inverters. This article analyzes only the boost mode of the QZSFPPC. As it can be seen from the waveforms, the input current and the output rectifier have twice higher frequency than the switching frequency f_{SW}. Also, the same current flows in both windings of the coupled inductor: $i_{qZ1} = i_{qZ2}$. The primary winding current is always composed of the switches' currents: $i_{pr} = i_{T1} + i_{T2}$. For further analysis, the transformer turns ratio is assigned to n:

$$n = \frac{N_{sec}}{N_{pr}}.$$

During the time interval $[t_1;t_2]$ the transistor T_1 is switched off, T_2 is switched on. An equivalent circuit is shown in Fig. 4*a*. The currents in the coupled inductor windings are falling. Part of the energy stored in the qZS network is discharged to supply the load through the transformer. The voltage V_{DC} is applied to both primary windings of the transformer. V_{DC} is equal to half of the output voltage reflected from the output. The current of the transistor T_2 is equal to the reflected current of the secondary winding, which is equal to the current of the diode D_{r1}. The slope of this current in real applications will be defined by the leakage inductance of the transformer TR_1. The input current of the primary windings i_{pr} equals to the current of the transistor T_2. Blocking voltage of the transistor T_1 equals the reflected output voltage. At the instant t_1 the transistor current i_{T2} changes from the maximum input current value I_{qZ1max} to half of that level.

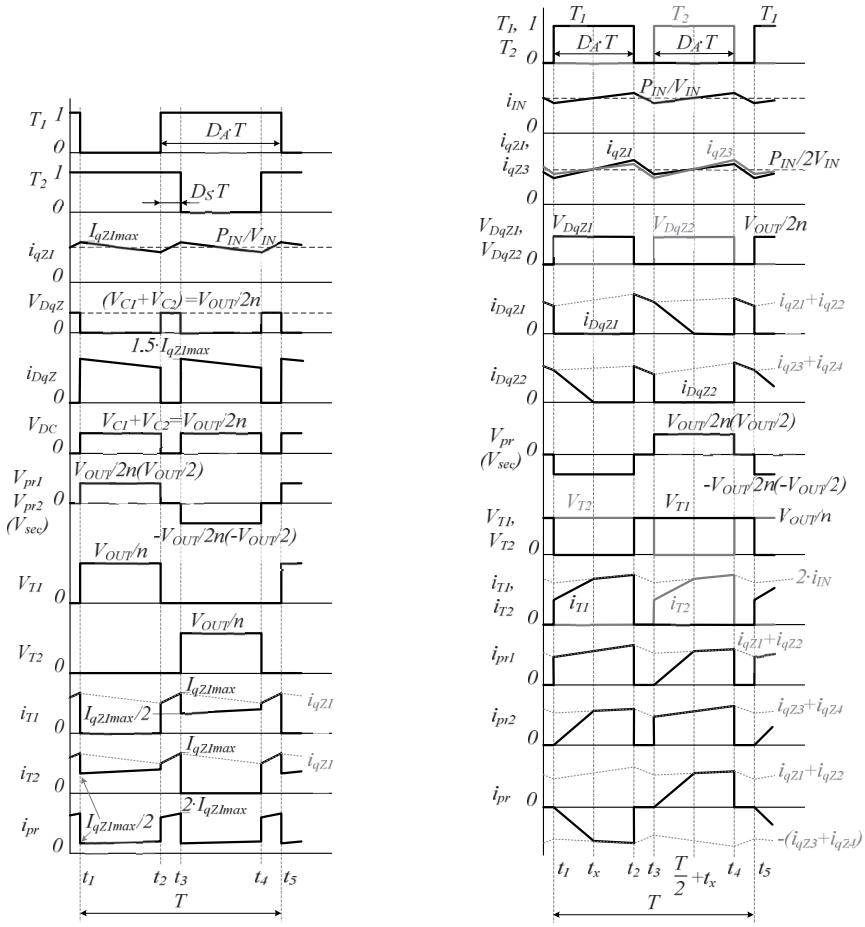

Fig. 3 – Current and voltage waveforms for the proposed converters: a) QZSFPPC and b) IQZSFPPC.

In this assumption we neglect the leakage inductances of the transformer TR_1. It means that at the moment t_2 the current i_{qZ2} is shared equally between the capacitor C_1 and the primary winding of the transformer TR_1 (i.e. capacitor C_{f1} reflected to the primary winding). It follows that the transformer input current i_{pr} decreases four times at the moment from $2 \cdot I_{qZ1max}$ to $I_{qZ1max}/2$ and the current of the qZS network diode reaches the maximum value equal to $1.5 \cdot I_{qZ1max}$.

Within the interval $[t_2;t_3]$ the transistor T_1 is switched on and T_2 is switched on, i.e. they are overlapped. An equivalent circuit is shown in Fig. 4*b*. During that interval the qZS network operates equivalent to the shoot-through mode, and it is called the equivalent shoot-through mode. The currents in the coupled inductor are rising. The QZS network is charged from the input supply. Voltage V_{DC} is equal to zero. Nothing is applied to both primary windings of the transformer. Current is flowing through both transistors. Fluxes in the primary winding are compensating each other. Currents of the transistor T_1 and T_2 are equal to the input current i_{qZ1}. Diodes of the output rectifier and diode D_{qZ} are reverse biased. Capacitors C_{f1} and C_{f2} supply the load. The input current of the primary windings i_{pr} equals the double input current (magnetizing current of the coupled inductor). That time interval is totally equal to the interval $[t_4;t_5]$.

For the time interval $[t_3;t_4]$ the transistor T_1 is switched on, T_2 is switched off. An equivalent circuit is shown in Fig. 4*c*. The currents in the coupled inductor fall and supply the load. Voltage V_{DC} is applied to both primary windings of the transformer. V_{DC} is equal to the negative half of the output voltage

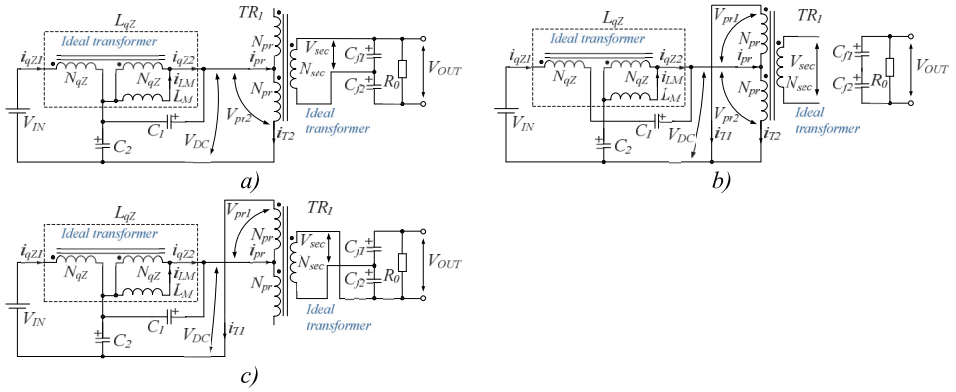

Fig. 4 – Equivalent circuits of the QZSFPPC for time intervals: a) [t_1;t_2], b) [t_2;t_3] and [t_4;t_5], c) [t_3;t_4].

reflected from the output. The current of the transistor T_1 is equal to the reflected current of the secondary winding, which is equal to the current of the diode D_{r2}. Here the slope of this current will be defined by the leakage inductance of the transformer. The input current of the primary windings i_{pr} equals the current of the transistor T_1. The blocking voltage of the transistor T_2 equals the reflected output voltage.

The duty cycle of the equivalent shoot-through mode is $D_S = (D_A - 0.5)$. Taking into account the double frequency of the equivalent shoot-through states and the implementation of the VDR, it is easy to calculate the DC gain factor:

$$\frac{V_{OUT}}{2 \cdot n} = \frac{1}{(1 - 2 \cdot 2 \cdot (D_A - 0.5))} \cdot V_{IN} = \frac{1}{3 - 4 \cdot D_A} \cdot V_{IN}\ ;\ B = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n}{3 - 4 \cdot D_A}. \quad (1)$$

Equation (1) shows that the QZSFPPC operates in the step-up mode in the active duty cycle D_A range from 0.5 to 0.75. This means that the duty cycle of the negative and positive half waves of the secondary winding lies in the range from 0.25 (for the maximum duration of the equivalent shoot-through state) to 0.5 (for the unity DC gain factor). Reference topology shown in Fig. 1*a* has a range that is two times wider – from 0 to 0.5. From this point of view, transformer utilization of the QZSFPPC is better with a wide voltage regulation.

The average values of the voltages and currents in the qZS network:

$$V_{C1} = \bar{v}_{C1} = \frac{2 \cdot D_A - 1}{3 - 4 \cdot D_A} \cdot V_{IN}\ ;\ V_{C2} = \bar{v}_{C2} = \frac{2 \cdot (1 - D_A)}{3 - 4 \cdot D_A} \cdot V_{IN}\ ;\ I_{qZS} = \bar{i}_{qZS1} = \bar{i}_{qZS2} = \frac{P_{IN}}{V_{IN}}\ ; \quad (2)$$

where P_{IN} is the input power of the converter.

Ripple and peak value of the current in the qZS network:

$$\Delta I_{qZS} = \frac{(2 \cdot D_A - 1) \cdot (1 - D_A) \cdot V_{IN}}{2 \cdot f_{SW} \cdot (3 - 4 \cdot D_A) L_M}\ ; \quad (3)$$

$$I_{qZS1\max} = I_{qZS} + \frac{\Delta I_{qZS}}{2} = \frac{P_{IN}}{V_{IN}} + \frac{(2 \cdot D_A - 1) \cdot (1 - D_A) \cdot V_{IN}}{4 \cdot f_{SW} \cdot (3 - 4 \cdot D_A) L_M}. \quad (4)$$

Voltage stress across the output rectifier diodes equals the output voltage. The average voltage of the output capacitor is equal to half of the output voltage. Voltage stress across the transistors equals the reflected output voltage.

Operation Principle of the Proposed Interleaved Quasi-Z-Source-Fed Push-Pull Converter

In the case of the IQZSFPPC, the switching period consists of six intervals, as shown in Fig. 3*b*. The transistors are working interleaved. Each of them is turned on during the active duty cycle $D_A < 0.5$. There are two instants which totally depend on the leakage inductance of the real transformer TR_1: t_x and $T/2+t_x$, where T means the switching period of the converter: $T = 1/f_{SW}$. This converter operates only in the step-up mode. In the IQZSFPPC waveforms of the input current, currents in the windings of the coupled inductor L_{qZ} and the output rectifier have twice higher frequency than the switching

frequency f_{SW} due to the interleaved transistor control and coupling of two qZS networks. Also, the same current flows in the pairs of windings: $i_{qZ1} = i_{qZ2}$, $i_{qZ3} = i_{qZ4}$. The coupled qZS network is implemented with one coupled inductor L_{qZ}, two diodes D_{qZ1}, D_{qZ2}, and four capacitors $C_1 \ldots C_4$. The proposed coupled impedance network can be used as two independent qZS networks with four inductors (or two two-winding coupled inductors), which work at the switching frequency. Coupling of four inductors on one core results in a reduced current ripple and volume due to twice higher working frequency ($2 \cdot f_{SW}$). Fig. 3*b* shows the amplitude envelopes for the current waveforms. The following inequalities and equations are correct over the switching period:

$$i_{DqZ1}(t) \le i_{qZ1}(t) + i_{qZ2}(t);\ i_{DqZ2}(t) \le i_{qZ3}(t) + i_{qZ4}(t);\ i_{T1}(t) \le 2 \cdot i_{IN}(t) = \sum_{j=1}^{4} i_{qZj}(t);$$

$$i_{T2}(t) \le 2 \cdot i_{IN}(t) = \sum_{j=1}^{4} i_{qZj}(t);\ i_{pr1}(t) \le i_{qZ1}(t) + i_{qZ2}(t);\quad i_{pr2}(t) \le i_{qZ3}(t) + i_{qZ4}(t);$$

$$i_{pr1}(t) = i_{qZ1}(t) + i_{qZ2}(t) - i_{DqZ1}(t);\ i_{pr2}(t) = i_{qZ3}(t) + i_{qZ4}(t) - i_{DqZ2}(t);$$

$$(i_{qZ3}(t) + i_{qZ4}(t)) \le i_{pr}(t) \le i_{qZ1}(t) + i_{qZ2}(t).$$

For further analysis, the variables are changed:

$$n = \frac{N_{sec}}{N_{pr}},\ p = \frac{L_M}{L_{lk}},$$

where n is the turns ratio of the transformer TR_1, and p is the coupling ratio of the inductor L_{qZ}.

Within the time interval $[t_1;t_2]$ the transistor T_1 is switched on, T_2 is switched off. Equivalent circuits are shown in Figs. 5*a* and 5*b*. Currents in the coupled inductor are rising. Energy from the input is stored in the coupled qZS network. At the same time the coupled qZS network transfers energy to the load through the transformer TR_1. Voltage across the primary winding is equal to half of the output voltage reflected from the output. Reflected output voltage is applied to the transistor T_2. Until t_x the following expressions are valid: $i_{pr1}(t) = i_{qZ1}(t) + i_{qZ2}(t)$; $i_{pr2}(t) \le i_{qZ3}(t) + i_{qZ4}(t)$; $i_{pr}(t) = -i_{pr2}(t)$. After t_x the expressions are changing: $i_{pr1}(t) = i_{qZ1}(t) + i_{qZ2}(t) = 2 \cdot i_{qZ1}(t)$; $i_{pr2}(t) = i_{qZ3}(t) + i_{qZ4}(t)) = 2 \cdot i_{qZ3}(t)$; $i_{pr}(t) = -(i_{qZ3}(t) + i_{qZ4}(t)) = -2 \cdot i_{qZ3}(t)$.

The idealized waveforms shown in Fig. 3*b* describe the most general case when $t_x < t_2$, and the current $i_{DqZ2}(t)$ is discontinuous. In a real circuit, depending on the operation mode, we can observe a situation when the current $i_{DqZ2}(t)$ is continuous during the time interval $[t_1;t_2]$. In such a case the converter behavior within that time interval can be described with the equations shown for the interval $[t_1;t_x]$.

During the interval $[t_2;t_3]$ both transistors are switched off. An equivalent circuit is shown in Fig. 5*c*. The currents in the coupled inductor L_{qZ} are falling. The coupled qZS network does not supply the load. No current flows to the transformer. The winding currents of L_{qZ} are charging the qZS capacitors: $i_{C1}(t) = i_{qZ2}(t)$; $i_{C2}(t) = i_{qZ1}(t)$; $i_{C3}(t) = i_{qZ4}(t)$; $i_{C4}(t) = i_{qZ3}(t)$. Zero voltage is applied to the primary winding of the transformer TR_1. In each qZS diode pairwise sums of the currents of the coupled inductor L_{qZ} are flowing: $i_{DqZ1}(t) = i_{qZ1}(t) + i_{qZ2}(t)$; $i_{DqZ2}(t) = i_{qZ3}(t) + i_{qZ4}(t)$. The reflected output voltage is applied to both transistors, and that time interval is dually similar to the interval $[t_4;t_5]$.

The behavior of the converter during the interval $[t_3;t_4]$ is symmetrically equivalent to the interval $[t_1;t_2]$: the transistor T_2 is turned on, T_1 is turned off. Equivalent circuits are shown in Figs. 5*d* and 5*e*. Currents in the two qZS networks that form the coupled qZS network are pairwise mirror images of each another. For example, the current $i_{qZ1}(t)$ has the same behavior at the interval $[t_1;t_2]$ as the current $i_{qZ3}(t)$ at the interval $[t_3;t_4]$.

Taking into account the implementation of VDR at the output it is easy to calculate the DC gain factor:

$$\frac{V_{OUT}}{2 \cdot n} = \frac{1}{(1 - 2 \cdot D_A)} \cdot V_{IN};\ B = \frac{V_{OUT}}{V_{IN}} = \frac{2 \cdot n}{1 - 2 \cdot D_A}. \qquad (5)$$

From here it follows that the IQZSFPPC operates in the step-up mode within the active duty cycle D_A range from 0 to 0.5. This means that the duty cycle of the negative and the positive half waves of the secondary winding lies in the range from 0 to 0.5. It is the same range as in the reference topology shown in Fig. 1*b*. In the proposed topology the duty cycle of transformer pulses is shorter at the same DC gain factor. The main advantage is shorter turn-on states of the transistors, i.e. more than 0.5 shorter duty cycles. Nevertheless, in the proposed topology transistors operate with twice higher current stress.

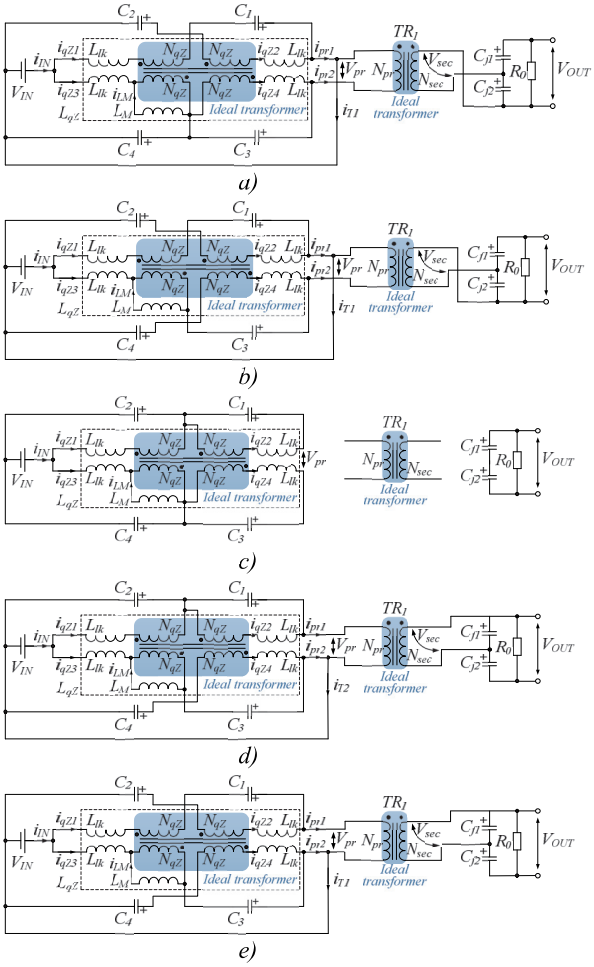

Fig. 5 – Equivalent circuits of the IQZSFPPC for time the intervals: a) $[t_1;t_x]$, b) $[t_x;t_2]$, c) $[t_2;t_3]$ and $[t_4;t_5]$, c) $[t_3;T/2+t_x]$, d) $[T/2+t_x;t_4]$.

Average values of voltages and currents in the qZS network and average input current are as follows:

$$V_{C1} = V_{C3} = \frac{D_A}{1-2\cdot D_A}\cdot V_{IN};\ V_{C2} = V_{C4} = \frac{1-D_A}{1-2\cdot D_A}\cdot V_{IN}; \tag{6}$$

$$I_{qZS} = \bar{i}_{qZS1} = \bar{i}_{qZS2} = \bar{i}_{qZS3} = \bar{i}_{qZS4} = \frac{P_{IN}}{2\cdot V_{IN}};\ I_{IN} = \bar{i}_{IN} = \frac{P_{IN}}{V_{IN}}. \tag{7}$$

where P_{IN} is the input power of the converter. All the currents of the coupled inductor have equal average value and achieve the same peak value. Ripple and peak value of the current in the qZS network and at the input:

$$\Delta I_{qZS} = \frac{V_{IN}\cdot D_A}{L_{lk}\cdot f_{SW}}\frac{(1-D_A)+2\cdot p\cdot(1-2\cdot D_A)}{(1+4\cdot p)\cdot(1-2\cdot D_A)}; \tag{8}$$

$$I_{qZS1\max} = I_{qZS} + \frac{\Delta I_{qZS}}{2} = \frac{P_{IN}}{2V_{IN}} + \frac{V_{IN}\cdot D_A}{L_{lk}\cdot f_{SW}}\frac{(1-D_A)+2\cdot p\cdot(1-2\cdot D_A)}{2\cdot(1+4\cdot p)\cdot(1-2\cdot D_A)}; \tag{9}$$

$$\Delta I_{IN} = \frac{V_{IN}\cdot D_A}{L_{lk}\cdot f_{SW}}; \tag{10}$$

$$I_{IN\max} = I_{IN} + \frac{\Delta I_{IN}}{2} = \frac{P_{IN}}{2V_{IN}} + \frac{V_{IN} \cdot D_A}{2 \cdot L_{lk} \cdot f_{SW}}. \quad (11)$$

From expressions (8)-(11) it follows that the input current ripple depends only on the value of leakage inductances of the coupled inductor. Also, the ratio of magnetizing and leakage inductances defines the ripple of currents in the coupled inductor windings. The following inequality is correct for the above-mentioned ripples regardless of the coupling coefficient: $\Delta I_{qZS} \geq \Delta I_{IN}/2$. This topology requires specific design of the coupled inductor. Voltage stress across the output rectifier diodes equals the output voltage. The average voltage of the output capacitors equals half of the output voltage. Voltage stress across the transistors equals the reflected output voltage.

DC gain characteristics for the QZSFPPC and the IQZSFPPC are shown in Fig. 6 for $n = 1$.

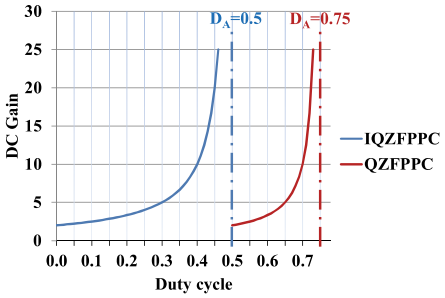

Fig. 6 – DC gain characteristics of the proposed converters.

Simulation Results

Simulations by means of PSIM software were done to verify theoretical assumptions. Parameters of the implemented models are presented in Table I. In the simulation study leakage inductances of the isolation transformer are practically avoided due to their low value (1 uH).

Our simulation results are shown in Fig. 7. Special attention was paid to the influence of the magnetizing inductance of the isolation transformer TR_1. The simulation shows that the magnetizing current should be included to the equations of the current envelopes where it is needed. This current has even higher influences on the operation principle of the IQZSFPPC. Magnetizing inductance of the coupled inductor in the QZSFPPC and the leakage inductance of the coupled inductor in the IQZSFPPC are equal. The input current ripple of the QZSFPPC is two times lower than in the IQZSFPPC because the qZS network inductors of the QZSFPPC are coupled. This behavior was expected. In general, simulation waveforms proved our theoretical results in total. The main difference is in the magnetizing current of the isolation transformer TR_1.

Table I: Parameters for simulation

Parameter	Value	Parameter	Value	Parameter	Value
$C_1 \ldots C_4$	15 uF	L_{lT}	1 uH	P_{IN}	300 W
C_{f1}, C_{f2}	15 uF	L_{MT}	1 mH	V_{IN}	80 V
L_M (QZSFPPC)	200 uH	n	1	V_{OUT}	400 V
L_M (IQZSFPPC)	500 uH	p	2.5	D_A (QZSFPPC)	0.651
L_{lk} (IQZSFPPC)	200 uH	f_{SW}	50 kHz	D_A (IQZSFPPC)	0.303

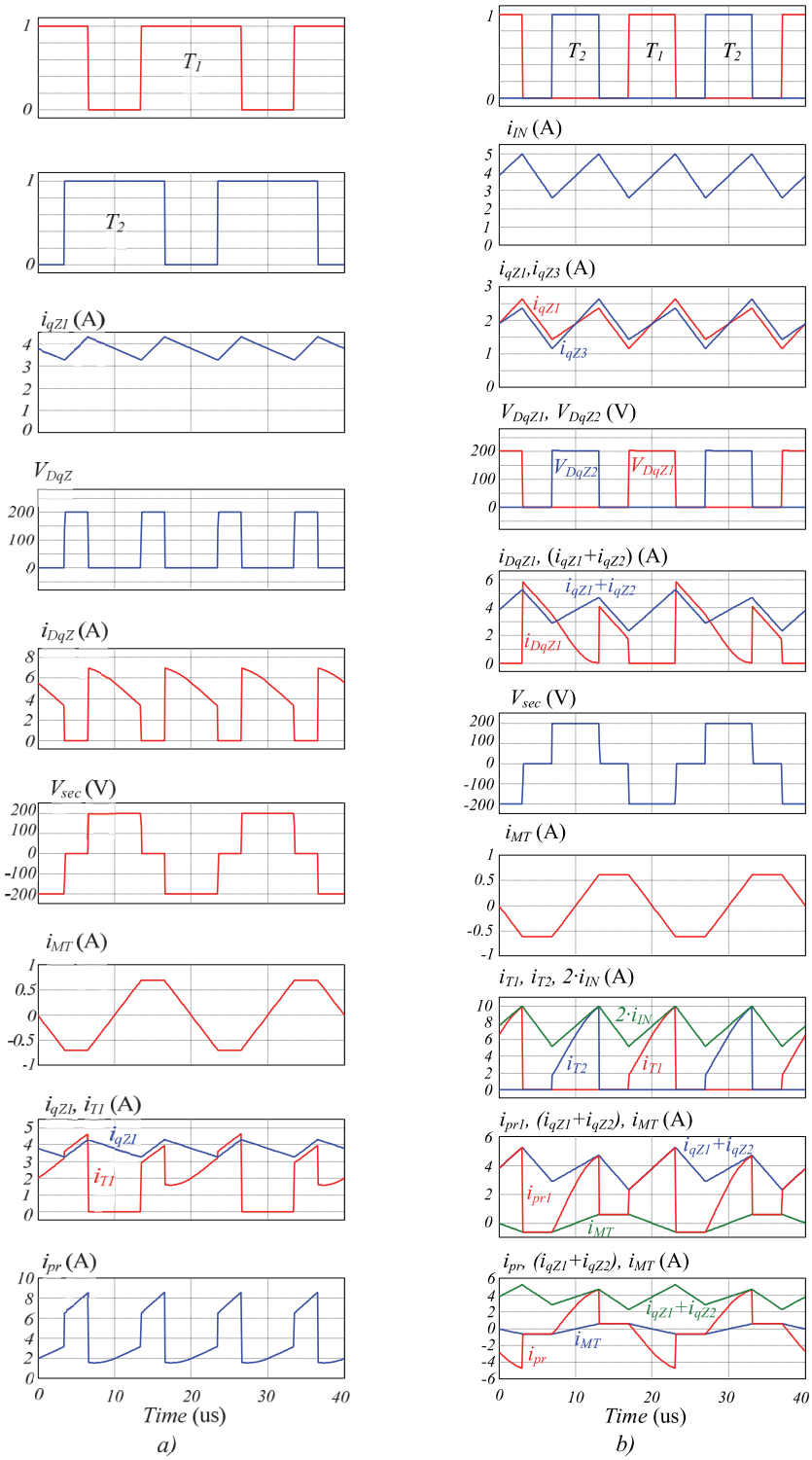

Fig. 7 – Simulation results of the proposed converters: a) QZSFPPC and b) IQZSFPPC.

Conclusions

This paper has presented a novel family of the quasi-Z-source DC/DC converter. It was derived from the current-fed push-pull converters, also known as isolated boost converters. By replacing the input inductors with magnetically coupled qZS networks, as compared to the reference topologies, the step-up capability was improved. The proposed topologies can be applied to a wide variety of applications, like renewable energy systems, battery energy storage systems, alternative energy sources, etc. Main expressions describing the work of the converter are presented. Simulations performed proved the theoretical analysis of the operation modes.

The focus of future research is on further magnetic integration of the proposed topologies and on the soft-switching and active clamping techniques, which are necessary to decrease the switching losses and to eliminate the influence of the isolation transformer leakage inductances.

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Input-Parallel Output-Series Connection of Isolated Quasi-Z-Source DC-DC Converters

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***Abstract*—This paper proposes an input-parallel-output-series (IPOS) power system based on the isolated qZS DC-DC converter. Reported as a solution for the integration of renewable energy sources into the medium voltage grid, such power systems can also be used to integrate low voltage energy sources into a 230V/400V grid. We examined the basic switching stage with three different rectifier topologies whereas the steady state analysis was made for each topology. Criteria for our comparison were implementation complexity and current and voltage stress of the components. An experimental prototype of the proposed IPOS power system composed of two converters was built at a rated output power of 400 W. DC gain characteristics and efficiency curves are presented. The experimental waveforms for the input voltage 80 V and the output voltage 400 V were measured.**

***Index Terms*—DC-DC power converters, quasi-Z-source converters, rectifiers, input-parallel output-series connection.**

I. Introduction

Modular architecture of power systems has been a subject of intensive research for more than 20 years [1]–[9]. Typically, a series-parallel conversion system utilizes multiple standardized converters that are connected in parallel or series at the output and input sides [6]. There are four possible architectures depending on the module interconnection form: input-parallel-output-parallel (IPOP), input-series-output-parallel (ISOP), input-series-output-series (ISOS), and input-parallel-output-series (IPOS), as shown in Fig. 1. Connection of several converters into one conversion system provides the following advantages: possibility to use commercial-off-the-shelf converters, faster design process of the small scale modules, ease of thermal design of the system, improved reliability because of reduced electrical and thermal stresses, easy system scalability, higher reliability with implementation of n+1 redundancy, smaller input and output filters due to interleaved control of converters, reduced manufacturing cost and time, etc. [6], [10]. Low voltage/current stress of the basic converter enables the use of faster semiconductor devices and higher switching frequency that leads to smaller system size and high overall efficiency.

Mixed architecture can incorporate advantages of several configurations into one system. For example, the high power density DC-DC power system proposed in [11] uses the IPOS connection of converters with internal ISOP architecture. As a result, an efficiency of 98% was obtained.

IPOP architecture is widely adopted in the industry [6]. It is used in point-of-load converters, on-board multiphase voltage regulator modules, and in telecommunication power supplies. In these applications, converters supply high-current loads with low voltage. Also, modules with a rated power 200–300 W can have switching frequency in a MHz range and improved thermal design [12].

ISOP configuration fits applications where the output voltage is rather low, while the input voltage is relatively high. It meets the requirements of electric power systems for a high-speed-train [13] and industrial drives [6]. Also, it is applicable in renewable energy systems [14]. Lower input voltage enables the utilization of low-$R_{DS(ON)}$ MOSFETs and high switching frequency. This ensures flat efficiency characteristics in a wide range of input voltages [15].

ISOS systems can be used for interfacing two high/medium voltage levels in electric power conversion systems [16].

Conventional applications of the IPOS architecture are fabrication equipment for the semiconductor industry, X-ray and ultrasound equipment, electrostatic precipitators, and drivers for ion thrusters [5], [6], [17]. In each of them a relatively low voltage source supplies a high voltage load. In some cases such architecture allows the use of common output filters for several converters [18].

The rapidly growing renewable energy market has shifted researchers' attention to the IPOS energy conversion systems. IPOS cascading of basic converters can be used for the integration of a low voltage renewable energy source into the medium voltage grid [8], [9]. An IPOS system with different types of converters suits for photovoltaic applications. In [7] an IPOS converter utilizes a full-bridge LLC resonant converter as a highly efficient full power dc transformer, and a flyback converter as a low power photo-voltaic regulator. This system has high efficiency at the full input voltage range and low costs due to the combination of advantages of converter topologies and IPOS architecture.

Quasi-Z-source (qZS) converters show high performance in renewable energy systems [19], [20]. Previously, ISOP power systems based on isolated qZS DC-DC converters have been proposed for distributed generation [14]. This paper investigates the IPOS connection of three topological variations of the converter shown in Fig. 2. The topology was derived from the qZS push-pull converter presented in [21]. Three possible rectifiers for the output stage need to be analyzed and experimentally verified in order to estimate the converter performance in the IPOS configuration. Like any IPOS power system, the proposed qZS-based converter

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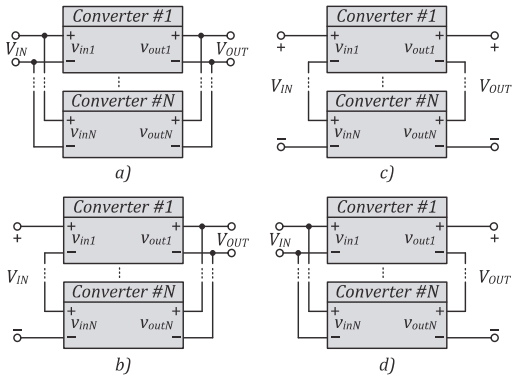

Fig. 1. Four architectures of the series-parallel conversion system: a) IPOP, b) ISOP, c) ISOS, and d) IPOS.

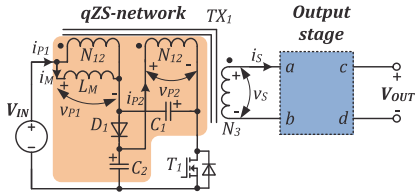

Fig. 2. General schematic of the isolated qZS DC-DC converter.

can be controlled with a uniform voltage distribution control scheme [22], when each converter operates as a voltage-controlled current source, or with simpler common-duty-ratio control [10]. In any case, the control system should provide interleaved control to decrease the input current ripple and the output voltage ripple.

II. Overview of the Converter Topology

The investigated converter shown in Fig. 2 is derived from the qZS push-pull converter presented in [21]. It combines the basic cell of the single switch non-isolated qZS converter and the coupled inductor. The main part of the converter is a qZS network. It consists of a coupled inductor TX_1, a diode D_1 and capacitors C_1, C_2. The coupled inductor integrates the functions of energy storage and a high frequency isolation transformer. It is shown as an equivalent circuit that contains an ideal transformer and a magnetizing inductance L_M due to the unity coupling coefficient. Primary windings of the coupled inductor contain N_{12} turns. The secondary winding that is coupled with the output stage contains N_3 turns. It transfers energy from the input to the output. Energy is stored in the magnetic field of the coupled inductor, i.e. magnetizing current, and in the qZS capacitors. The basic topology enables regulation of the output voltage in a wide range of the input voltage in the continuous conduction mode [23]. This makes it suitable but not limited to the integration of a variable-speed wind turbine into a medium voltage grid.

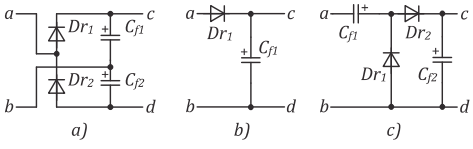

Fig. 3. Rectifiers selected for comparison: a) VDR1, b) HWR, c) VDR2.

Three rectifier topologies were selected for our comparative analysis: Fig. 3a shows the voltage-doubler rectifier (VDR1), Fig. 3b – the half-wave rectifier (HWR), and Fig. 3c – the Greinacher voltage-doubler rectifier (VDR2) [24]. One of the topologies is to be selected as the basis of a typical module for the proposed IPOS qZS-based system.

The converter investigated has one transistor. Idealized waveforms of winding voltages are shown in Fig. 4, where T is the switching period, and V_{C1} and V_{C2} are the voltage values of the qZS capacitors C_1, C_2, respectively. The qZS capacitors voltage is considered close to constant over the switching period. During the active cycle, the transistor is turned on. Regardless of the rectifier topology, voltages across qZS capacitors depend only on the input voltage V_{IN} and the duty cycle of the active state D_A:

$$V_{C1} = \frac{D_A}{1-2\cdot D_A} V_{IN}; \quad (1)$$

$$V_{C2} = \frac{1-D_A}{1-2\cdot D_A} V_{IN}; \quad (2)$$

$$k = \frac{N_3}{N_{12}}; \quad (3)$$

where k is the turns ratio of coupled inductors, $0 \le D_A \le 0.5$. Equations (1)–(3) are similar to those of the conventional qZS converter. Since the output rectifier defines the energy transfer process from the input to the output, the current waveforms of the converter strongly depend on the used rectifier circuit.

The following equations describe the IPOS power system in the steady state by means of average values:

$$V_{INsys} = V_{IN}; \quad (4)$$

$$I_{INsys} = N \cdot I_{IN}; \quad (5)$$

$$V_{OUTsys} = N \cdot V_{OUT}; \quad (6)$$

$$I_{OUTsys} = I_{OUT} = \frac{P}{V_{OUT}}; \quad (7)$$

$$P_{sys} = N \cdot P; \quad (8)$$

where V_{INsys}, I_{INsys}, V_{OUTsys}, I_{OUTsys}, P_{sys} are average values of the input voltage, input current, output voltage, output current and the output power of the IPOS power system; V_{IN}, I_{IN}, V_{OUT}, I_{OUT}, P are average values of the input voltage, input current, output voltage, output current and the output power of the single module; N is the number of modules included in the IPOS power system. These equations are correct for any IPOS where the control system equalizes operation conditions of the modules.

Steady state analysis was selected to evaluate and compare the three proposed topological variations of the converter.

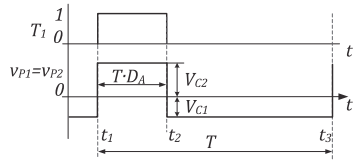

Fig. 4. Idealized waveforms of the primary windings voltage.

Analysis by average values is an appropriate method because averaged input/output parameters of a module are strictly tied with averaged input/output parameters of the IPOS power system in (4)–(8). In this analysis the lower case letters correspond to instantaneous values, and the upper case letters correspond to averaged or constant values.

III. Steady State Analysis of the Converter

In our analysis leakage inductances of the coupled inductor were not considered, but their influence was taken into account in the idealized waveforms shown in Fig. 5. Because of the same reason, the duty cycle in the output stage is designated as D' to differentiate duty cycles in the input and the output parts. Symmetry of the qZS network is important for simpler analysis. Primary windings of the coupled inductor contain an equal number of turns. For symmetry, qZS capacitors too should be equal: $C_1 = C_2 = C$. In this case $i_{P1}(t) = i_{P2}(t) = i_P(t)$. Voltages across all the capacitors in any of the three configurations of the converter are assumed constant in the steady state. Due to symmetry of the qZS network, we can make the following substitution: $v_{P1}(t) = v_{P2}(t) = v_P(t)$. The average current of the primary windings is equal to the average input current for any rectifier topology:

$$I_P = \frac{1}{T}\int_{t_1}^{t_3} i_P(t)dt = I_{IN} = \frac{P}{V_{IN}}. \quad (9)$$

A. Analysis of the Converter with the Voltage-Doubler Rectifier

The voltage-doubler rectifier is a high performance solution for step-up converters [19]. The VDR1 topology consists of two diodes Dr_1, Dr_2, and two output filtering capacitors C_{f1}, C_{f2}. Output capacitors are connected in series. Energy is transferred from the input side to the output during the whole switching period. Idealized waveforms of the currents and voltages of the VDR1 rectifier are shown in Fig. 5a. Short delays between the processes in the input and output stages are neglected in the following description.

During the time interval $[t_1;t_2]$, transistor T_1 is turned on, and voltage V_{C2} is applied to the primary windings of the coupled inductor. At this interval, diode D_1 is reverse biased. Reverse voltage of D_1 equals $(V_{C1} + V_{C2})$. At the output, diode Dr_1 is conducting, and diode Dr_2 is reverse biased with the output voltage. Current i_S charges the capacitor C_{f1}. During this interval, $i_{Dr1}(t) = i_S(t)$ and $v_S(t) = V_{Cf1}$. In an idealized case, $V_{Cf1} = k \cdot V_{C2}$, but in a real converter $V_{Cf1} \le k \cdot V_{C2}$ due to the influence of leakage inductances. Capacitor C_{f2} is discharging with the output current.

In the time interval $[t_2;t_3]$, transistor T_1 is turned off, and voltage of the primary windings changes at the moment t_2 to the value $v_P(t) = V_{C1}$. At this interval, diode D_1 is conducting. At the output, diode Dr_2 is conducting, and diode Dr_1 is reverse biased with the output voltage. Current i_S changes direction and starts charging the capacitor C_{f2}. During this interval, $i_{Dr2}(t) = -i_S(t)$ and $v_S(t) = V_{Cf2}$. For an idealized case $V_{Cf2} = k \cdot V_{C1}$, but in a real converter it changes to inequality $V_{Cf2} \le k \cdot V_{C1}$ as a result of the influence of leakage inductances. The output current discharges the capacitor C_{f1}.

During both of the intervals, one of the rectifier diodes is conducting, the other one is reverse biased. In this rectifier voltage, oscillations on the reverse biased diode do not occur because the diode is always clamped to the output voltage through the conducting diode.

A short delay occurs between the turn-off (or turn-on) of the transistor and the actual change of the voltage on the secondary winding due to energy saved in the leakage inductances. During that delay the current in the secondary winding falls to zero, and energy from the leakage inductance charges one of the output capacitors. Only after the end of that process, the output rectifier changes its state. Processes of the same nature can be observed in any of the three selected rectifiers. In the analysis those delays are neglected.

Average currents of the rectifier diodes are equal to the output current, and thus the average current of the secondary winding is equal to zero:

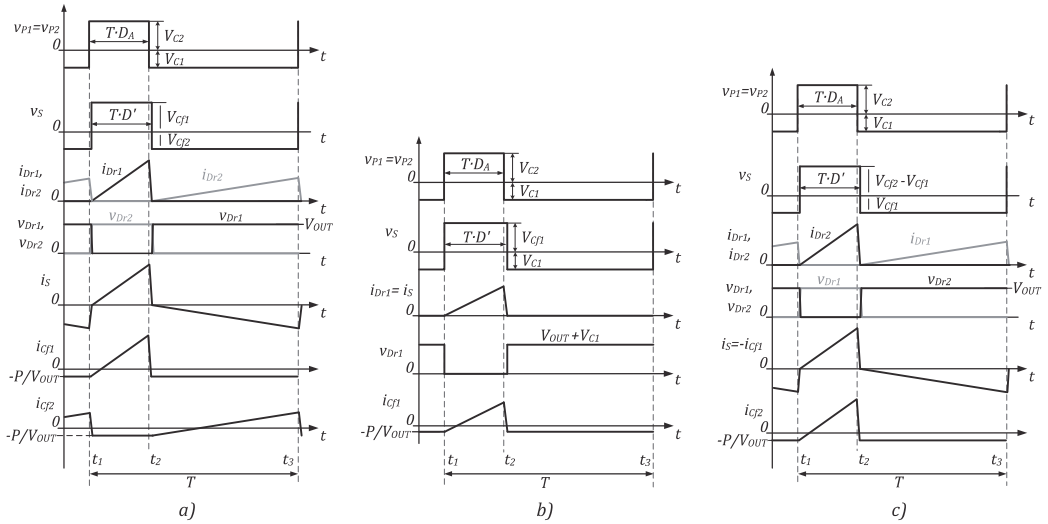

Fig. 5. Idealized waveforms of currents and voltages of the basic converter for the three selected rectifiers: a) VDR1, b) HWR, c) VDR2.

$$I_{Dr1} = \frac{1}{T}\int_{t_1}^{t_3} i_{Dr1}(t)dt = \frac{1}{T}\int_{t_1}^{t_2} i_S(t)dt = \frac{P}{V_{OUT}}; \quad (10)$$

$$I_{Dr2} = \frac{1}{T}\int_{t_1}^{t_3} i_{Dr2}(t)dt = \frac{1}{T}\int_{t_2}^{t_3} |i_S(t)|dt = \frac{P}{V_{OUT}}; \quad (11)$$

$$I_S = \frac{1}{T}\int_{t_1}^{t_3} i_S(t)dt = I_{Dr1} - I_{Dr2} = 0. \quad (12)$$

Taking into account (1)–(3), an ideal DC gain factor of the VDR1 topology is as follows:

$$G_{VDR1} = \frac{V_{OUT}}{V_{IN}} = \frac{k\cdot(V_{C1}+V_{C2})}{V_{IN}} = \frac{k}{1-2D_A}. \quad (13)$$

Taking into account (13), the DC gain of the IPOS power system implemented with the isolated qZS converter based on the VDR1 rectifier is as follows:

$$G_{VDR1sys} = \frac{V_{OUTsys}}{V_{INsys}} = \frac{N\cdot V_{OUT}}{V_{IN}} = \frac{N\cdot k}{1-2D_A}. \quad (14)$$

B. Analysis of the Converter with the Half-Wave Rectifier

Half-wave rectifier was selected for our comparative study because it is a cheap and simple solution. It consists of a diode Dr_1 and an output filtering capacitor C_{f1}. Energy transfer from the input side to the output occurs only during the active cycle, when transistor T_1 is switched on. Idealized waveforms of currents and voltages of the HWR rectifier are shown in Fig. 5b. The short delays shown in the figure are neglected in the following analysis of the idealized case.

In the time interval $[t_1;t_2]$, transistor T_1 is turned on, and voltage $v_P(t) = V_{C2}$. At this interval the qZS diode D_1 is reverse biased with voltage $(V_{C1} + V_{C2})$. Rectifier diode Dr_1 is conducting. Current i_S charges the capacitor C_{f1}. During that interval $i_{Dr1}(t) = i_S(t)$ and $v_S(t) = V_{Cf1}$. In an idealized case $V_{Cf1} = k\cdot V_{C2}$, but influenced by the leakage inductances of the coupled inductor, this equality changes into inequality $V_{Cf1} \le k\cdot V_{C2}$.

During the time interval $[t_2;t_3]$, transistor T_1 is turned off, and voltage of the primary windings changes at the moment t_2 to the value $v_P(t) = V_{C1}$. At this interval, diode D_1 is conducting. After a short delay, diode Dr_1 switches to the reverse biased state. Voltage applied to Dr_1 is equal to the sum of the output voltage and the secondary winding voltage: $(V_{OUT} + V_{C1})$. In a real converter, voltage across Dr_1 will oscillate during that interval. Voltage oscillations will occur as a result of the resonance process between the nonlinear parasitic capacitance of the diode Dr_1 and the leakage inductance of the secondary winding. During that interval, $i_{Dr2}(t) = i_S(t) = 0$ and $v_S(t) = k\cdot V_{C1}$. The output current discharges the capacitor C_{f1}.

Average current of the rectifier diodes and the secondary winding are equal to the output current:

$$I_{Dr1} = \frac{1}{T}\int_{t_1}^{t_3} i_{Dr1}(t)dt = I_{OUT} = \frac{P}{V_{OUT}}; \quad (15)$$

$$I_S = \frac{1}{T}\int_{t_1}^{t_3} i_S(t)dt = I_{OUT} = \frac{P}{V_{OUT}}. \quad (16)$$

Taking into account (1)–(3), the ideal DC gain factor of the HWR rectifier is as follows:

$$G_{HWR} = \frac{V_{OUT}}{V_{IN}} = \frac{k\cdot V_{C2}}{V_{IN}} = k\cdot\frac{1-D_A}{1-2\cdot D_A}. \quad (17)$$

Taking into account (17), the DC gain of the qZS IPOS power system based on the HWR rectifier is as follows:

$$G_{HWRsys} = \frac{V_{OUTsys}}{V_{INsys}} = \frac{N\cdot V_{OUT}}{V_{IN}} = N\cdot k\cdot\frac{1-D_A}{1-2\cdot D_A}. \quad (18)$$

C. Analysis of the Converter With the Greinacher Voltage-Doubler Rectifier

Greinacher voltage-doubler rectifier is another possible implementation of the voltage-doubler rectifier [24]. It was selected as a VDR1 competitor topology. It consists of two diodes Dr_1, Dr_2, and two output filtering capacitors C_{f1}, C_{f2}. Unlike VDR1 topology, in this rectifier only one capacitor C_{f2} supplies the output load directly. Capacitor C_{f1} serves as an intermediate energy storage element. This rectifier has the same voltage and current shapes at the terminals a-b and provides the same voltage at the terminals c-d as in the VDR1 topology. Idealized waveforms of currents and voltages of the VDR2 rectifier are shown in Fig. 5c. Short delays between the processes in the input and output stages are neglected in the following description.

During the time interval $[t_1;t_2]$, transistor T_1 is turned on. Processes in the coupled inductor and qZS network are similar to the processes in the VDR1 topology during the same time interval. At the output, diode Dr_2 is conducting, and diode Dr_1 is reverse biased with the output voltage. Current i_S charges the capacitor C_{f2} and discharges the capacitor C_{f1}. During that interval, $i_{Dr2}(t) = i_S(t)$ and $v_S(t) = (V_{Cf2} - V_{Cf1})$. In an idealized case $(V_{Cf2} - V_{Cf1}) = k\cdot V_{C2}$, but in a real converter $(V_{Cf2} - V_{Cf1}) \le k\cdot V_{C2}$ due to the influence of leakage inductances.

In the time interval $[t_2;t_3]$, transistor T_1 is turned off, $v_P(t) = V_{C1}$, and diode D_1 is conducting. At the output, diode Dr_1 is conducting, and diode Dr_2 is reverse biased with the output voltage. Current i_S changes its direction and starts charging the capacitor C_{f1}. During that interval, $i_{Dr1}(t) = -i_S(t)$ and $v_S(t) = V_{Cf1}$. In the ideal case $V_{Cf1} = k\cdot V_{C1}$, but in a real converter $V_{Cf2} \le k\cdot V_{C1}$ because of the influence of leakage inductances. The output current charges the capacitor C_{f1}.

During both intervals the reverse biased rectifier diode is clamped to the output voltage through the conducting rectifier diode. No voltage oscillations occur in the rectifier.

Equations (10)–(12) are also correct for the VDR2 rectifier. The ideal DC gain factor of the VDR2 topology is similar to the DC gain of the VDR1 rectifier:

$$G_{VDR2} = G_{VDR1} = G_{VDR} = \frac{k}{1-2D_A}. \quad (19)$$

The DC gain of the IPOS power system implemented with the isolated qZS converter based on the VDR1 rectifier is as follows, taking into account (13):

$$G_{VDR2sys} = G_{VDR1sys} = G_{VDRsys} = \frac{N\cdot k}{1-2D_A}. \quad (20)$$

Both of the voltage double rectifier topologies have the same ideal DC gain. In general, the topology VDR2 has

higher voltage and current stresses of the output capacitors than the VDR1 rectifier. It follows that VDR1 should have slightly higher efficiency and DC gain than VDR2 in the real prototype. This hypothesis needs to be experimentally verified. The prototype of the proposed IPOS power system comprising two converters would be sufficient for our verification. In the next section, all the three topologies will be compared based on the key parameters.

IV. Comparison of the Converter Configurations

All the investigated topologies were compared for the number of elements, possible parasitic oscillations, voltage and current stresses of elements. TABLE I. presents the data used for our comparison. We used here the duty cycle of the output stage D' instead of D_A, and V_{OUT}. This approach is more practical because of the influence of parasitic elements that change the relations between the input and output values depending on the operation mode of the converter.

As it follows from the table, all the topologies allow the IPOS connection of the converters. The step-up characteristic of the half-wave topology is worse than that of the topologies based on the voltage-doubler rectifier. In addition, the HWR topology suffers from the parasitic voltage oscillations at the output and does not utilize both half-waves of the voltage across the secondary winding. The VDR1 topology looks slightly better than VDR2 due to lower voltage and current stresses of the rectifier elements. Both voltage-doubler topologies fully utilize the output voltage of the secondary winding. Moreover, they do not suffer from voltage oscillations thanks to the inherited reverse voltage clamping of the rectifier diodes.

Averaged magnetizing current of the coupled inductor is another important parameter for a comparative analysis. In voltage-doubler topologies, average current of the secondary winding is zero. It leads to a high average magnetizing current $I_{M\text{-}VDR}$, taking into account (10)–(12):

$$I_{M-VDR} = I_{Dr1} + I_{Dr2} - I_S = \frac{2 \cdot P}{V_{IN}}. \quad (21)$$

In the half-wave rectifier, the current of the secondary winding is unipolar, i.e. it contains a DC component. This leads to the lower magnetizing current of the coupled inductor for the HWR topology $I_{M\text{-}HWR}$, taking into account (15)–(16):

$$I_{M-HWR} = I_{Dr1} + I_{Dr2} - I_S = \frac{2 \cdot P}{V_{IN}} - \frac{P}{V_{OUT}}. \quad (22)$$

Lower average magnetizing current of the HWR topology can be considered as an advantage. From a practical point of view, a coupled inductor for the HWR rectifier should have smaller size than a coupled inductor for the VDR1 or VDR2 rectifiers. This means that the HWR topology has a smaller elements number, and can have higher efficiency due to reduced losses in the elements. Implementation of a snubber for the diode Dr_1 can increase reliability due to damping of oscillations, as predicted, but it will lower the efficiency. Also, output voltage ripple is higher in the half-wave rectifier.

Idealized DC gain characteristics of the converter for voltage-doubler rectifier topologies and for the half-wave rectifier topology are shown in Fig. 6 for $k = 1$. Topologies based on the voltage-doubler are bound to have higher DC gain at the same duty cycle of the active state.

TABLE I. Major Parameters of the Converter Configurations

Parameter	Component	Rectifier topology		
		VDR1	*HWR*	*VDR2*
Half-wave (HW) or full-wave (FW)	N/A*	FW	HW	FW
Number of diodes		2	1	2
Voltage oscillations across diodes		No	Yes, with overshoot	No
Number of capacitors		2	1	2
Average current	Dr_1	$\frac{P}{V_{OUT}}$	$\frac{P}{V_{OUT}}$	$\frac{P}{V_{OUT}}$
	Dr_2		N/A	
Maximum current	Dr_1	$\frac{2}{D'} \cdot \frac{P}{V_{OUT}}$	$\frac{2}{D'} \cdot \frac{P}{V_{OUT}}$	$\frac{2}{1-D'} \cdot \frac{P}{V_{OUT}}$
	Dr_2	$\frac{2}{1-D'} \cdot \frac{P}{V_{OUT}}$	N/A	$\frac{2}{D'} \cdot \frac{P}{V_{OUT}}$
Voltage stress	Dr_1	V_{OUT}	$(V_{OUT} + V_{C1})$[1]	V_{OUT}
	Dr_2	V_{OUT}	N/A	V_{OUT}
	C_{f1}	$(1-D') \cdot V_{OUT}$	V_{OUT}	$D' \cdot V_{OUT}$
	C_{f2}	$D' \cdot V_{OUT}$	N/A	V_{OUT}
Average magnetizing current	TX_1	$\frac{2 \cdot P}{V_{IN}}$	$\frac{2 \cdot P}{V_{IN}} - \frac{P}{V_{OUT}}$	$\frac{2 \cdot P}{V_{IN}}$

*N/A- not applicable.

[1] steady state value, voltage overshoot with higher magnitude is possible.

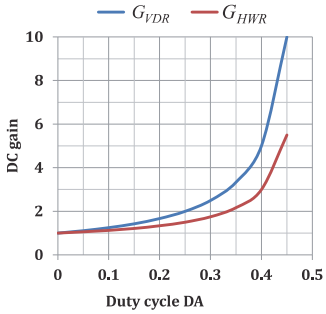

Fig. 6. Ideal DC gain factors of the converter.

V. Experimental Results

An experimental prototype of the proposed IPOS power system was built. It contains two isolated qZS DC-DC converters, at the total rated power of 400 W, i.e. 200 W per module. To verify theoretical predictions, the system was tested with three different output rectifiers. The switching frequency selected was equal to 100 kHz. Converters were controlled with common-duty-ratio control [10] with added interleaving. The coupled inductors' magnetizing inductance was 1 mH and the leakage inductance 30 μH and 15 μH in the primary and secondary windings, respectively. The turns ratio of the coupled inductors was $k = 1$. Metallized polypropylene film capacitors 60 μF/800 V were used in the rectifiers and in the quasi-Z-source network of the converter. All the semiconductor components were SiC-based; and the experiments were performed under constant output voltage of 400 V, i.e. 200 V per module, and constant output power of 400 W, i.e. 200 W per module. Measurement results of the DC gain characteristic are summarized in Fig. 7. Measured characteristics were compared with ideal ones expressed in (14), (18), (20), assuming $N = 2$, $k = 1$.

Measured DC gain characteristics of the VDR1 and the VDR2 rectifiers were equal, but lower than the ideal one, as shown in Fig. 7a. The measured DC gain characteristic of the HWR rectifier was also considerably lower than the ideal one, as shown in Fig. 7b. As it was predicted, the HWR topology has a lower DC gain characteristic than the voltage-doubler topologies, as shown in Fig. 7c.

The investigated converter was considered as a pure boost converter. In practice, DC gain characteristics show buck-boost behavior. Buck mode for the HWR was within D_A range [0;0.2], and within the range [0;0.165] for VDR1 and VDR2. Measurements were performed in the range of the input voltage of 40 V to 400 V in order to verify the buck behavior of the converter. The input voltage of 400 V corresponds to the DC gain 0.5 of a single converter in the implemented IPOS power system ($N = 2$). This happens not only because of losses and influence of the leakage inductances, but also due to narrow control impulses. In this mode output diodes transfer energy during a short time. In an ideal case, qZS capacitors charge output capacitors till the equalization of voltages between the input and output parts. When D_A is a low qZS, capacitors cannot transfer enough energy to the output capacitors within a narrow current impulse. Neither is the leakage inductance sufficient in this case to form a small LC-filter with output capacitors. It provides an output voltage close to an average voltage instead of peak value, which is expected. Also, at low D_A the behavior of the three rectifiers is almost similar, because the magnitude of the negative half wave of the voltage v_S is close to zero.

Oscilloscope Tektronix DPO7254 with two current probes (Tektronix TCP0030) and two voltage probes (Tektronix P5205A and P5210A) was used for the efficiency measurement. Instantaneous input (or output) power was obtained by the multiplication of the measured input (or output) current and voltage. Efficiency is the ratio of the average measured output power to the average measured input power. The efficiency measured is shown in Fig. 8. The converter with the HWR rectifier shows high efficiency in a wide range of input voltage. In terms of reliability and efficiency, the VDR2 topology shows slightly better performance than the other topologies. The HWR topology has higher efficiency at high input voltage due to a smaller number of semiconductor components and lower voltage overshoot in this range. Snubber was not used in the HWR topology in order to measure voltage overshoot across diode Dr_1. It is shown in Fig. 9. D_A and V_{C1} decrease with the rise of the input voltage. Reverse voltage of diode Dr_1 in the HWR topology in the steady state equals $V_{OUT} + V_{C1}$. This value decreases with the input voltage rise at the constant output voltage. Voltage overshoot decreases with the steady state value.

Experimental waveforms for $V_{IN} = 80$ V, $V_{OUT} = 400$ V and $P_O = 400$ W are shown in Fig. 10. The converter operates in the continuous conduction mode. Measured waveforms confirm our assumptions about parasitic oscillations in the HWR rectifier. Also, they prove our theoretical analysis. All the waveforms are close by shape to those predicted in section three. Slope of any current is defined not only by real leakage and magnetizing inductances, and by the operation mode of the converter.

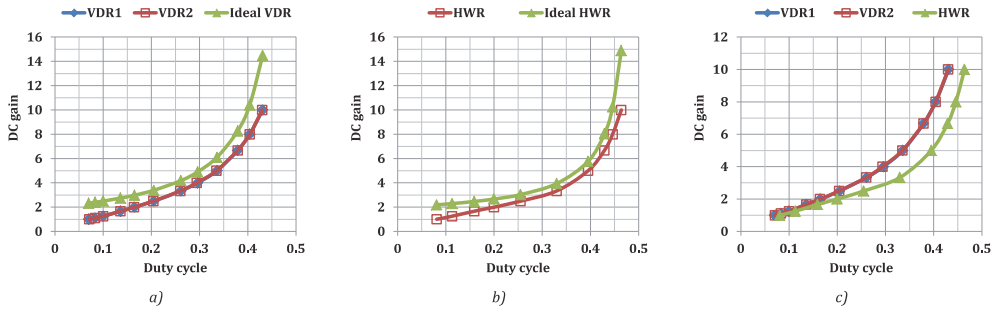

Fig. 7. DC gain characteristics: a) VDR1, VDR2 measured and ideal, b) HWR measured and ideal, c) measured for for all the three topologies.

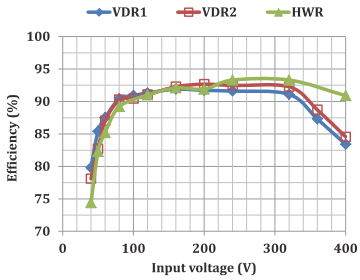

Fig. 8. Measured efficiency versus input voltage.

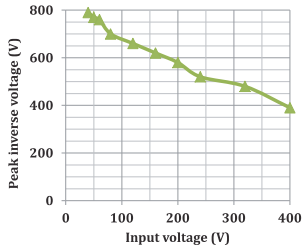

Fig. 9. Peak inverse voltage across diode Dr_1 in the HWR topology versus the input voltage.

In the experiment we used a coupled inductor with a relatively high magnetizing inductance, which results in low magnetizing current ripple. In this case the AC component of the primary windings current i_P is close by form to the current of the secondary winding multiplied by 0.5.

All the currents and voltages in Fig. 10 marked with the subscript "$_{SYS}$" belong to the input and the output of the whole ISOP system. Our experiment shows that the input current ripple of a single module is lower for a converter with the HWR rectifier than for voltage-doubler-based rectifiers. On the contrary, the input current ripple of the proposed qZS-based ISOP power system is lower with modules based on voltage-doubler rectifiers. This can be explained by the current slope compensation between the modules: when the current of one module is rising, the current of the other module is falling. Differences in these slopes result in the system input current ripple.

VI. Conclusion

Theoretical and experimental analysis of the isolated qZS DC-DC converter shows that two rectifier topologies suit for the IPOS power system: the half-wave rectifier and the Greinacher voltage-doubler rectifier. The first selection provides a simple solution, but it requires a snubber for the output diode. Usually, a snubber would slightly decrease the total efficiency. In any case the converter with a HWR

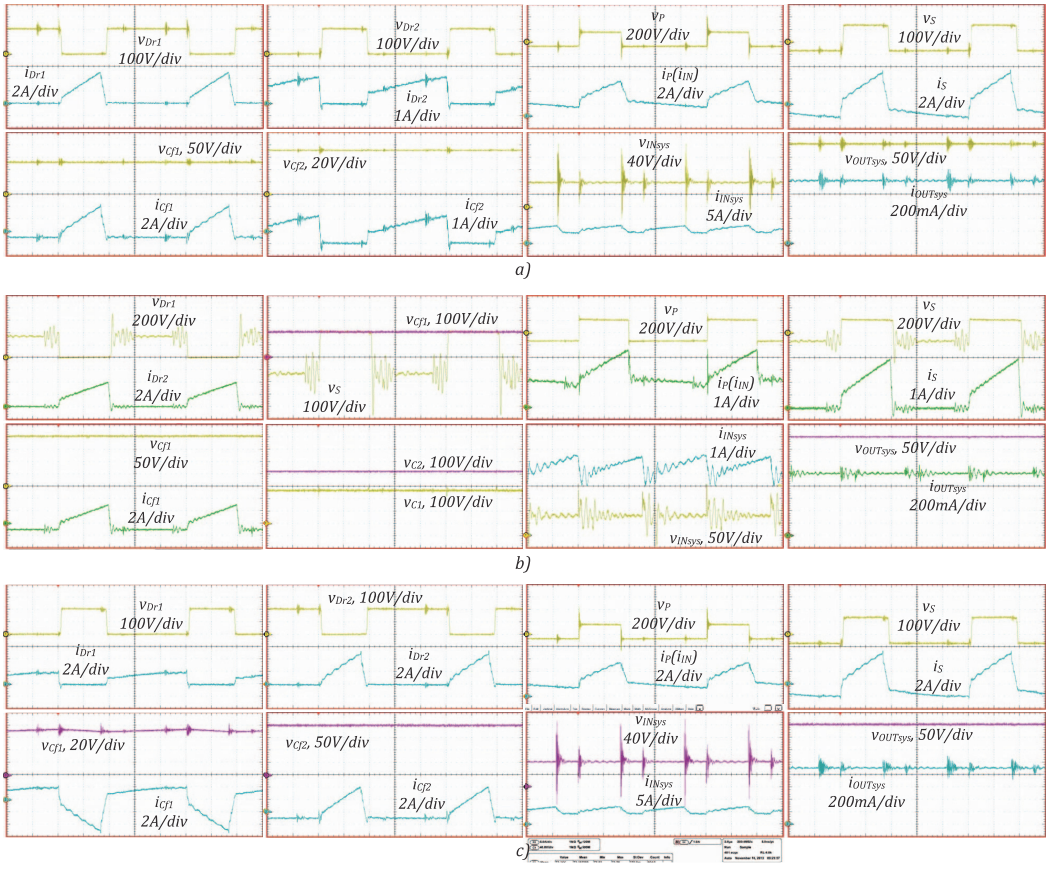

Fig. 10. Experimental waveforms of voltages and currents in the converter with: a) VDR1, b) HWR, and c) VDR2 rectifiers, in time scale 2 μs/div.

rectifier still has the lowest price of implementation. The converter with a VDR2 rectifier has high reliability and slightly higher efficiency than VDR1. The difference in the efficiency is in the range of 1%. Conversely, the advantage derived from the VDR2 rectifier instead of VDR1 is not obvious because the difference is within the measurement accuracy. At higher powers, VDR1 can have higher efficiency than VDR2 because it has lower current and voltage stresses of the output capacitors. This advantage makes VDR1 a preferable topology for the proposed IPOS system.

In general, introduction of the qZS IPOS power system is suitable but not limited for the integration of renewable energy sources with a wide range of output voltages, like variable-speed-variable-voltage wind turbines.

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[PAPER-IX] D. Vinnikov, A. Chub, L. Liivik, and I. Roasto, "High-Performance Quasi-Z-Source Series Resonant DC-DC Converter for Photovoltaic Module Level Power Electronics Applications," *IEEE Trans. Power Electron.*, accepted for publication.

High-Performance Quasi-Z-Source Series Resonant DC-DC Converter for Photovoltaic Module Level Power Electronics Applications

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***Abstract*— This paper presents the high-performance quasi-Z-source series resonant DC-DC converter as a candidate topology for the PV module level power electronics applications. The converter features a wide input voltage and load regulation range thanks to the multi-mode operation, i.e. when the shoot-through pulse-width modulation and phase-shift modulation are combined in a single switching stage to realize the boost and buck operating modes, respectively. Our experiments confirmed that the proposed converter is capable of ensuring ripple free 400 V output voltage within the six-fold variation of the input voltage (from 10 to 60 V). The converter prototype assembled achieved a maximum efficiency of 97.4%, which includes the auxiliary power and control system losses.**

Keywords*— *resonant converter; DC/DC converter; quasi-Z-source converter; renewable energy; solar photovoltaic; module level power electronics; module integrated converter (MIC)

I. INTRODUCTION

Module Level Power Electronics (MLPE) is a topic of growing interest in the solar photovoltaic (PV) applications. The idea of MLPE is to allow operation of each PV module in the Maximum Power Point (MPP) and therefore, to ensure the best possible energy harvest. Generally, the MLPE concepts could be classified as the full-power and partial-power processing converters [1]. The full-power MLPE concepts could be categorized as those connecting PV panels in series and in parallel. The first group is mostly represented by the PV power optimizers, which are typically realized with the non-isolated boost [2] and buck-boost converters [1]. The main focus of this paper is on the full-power converters for the parallel connection of PV modules. In this approach, each PV panel is equipped with a microconverter (*μCON*) with outputs connected in parallel to the central DC bus of the PV power system (Fig. 1*a*). *μCON* is a self-powered high efficiency step-up DC-DC converter with galvanic isolation that operates with autonomous control and is integrated to the PV panel for tracking the MPP locally. The galvanic isolation is essential to reduce ground leakage currents and grid current total harmonic distortion [3]. As seen from Fig. 1*a*, the central inverter feeds PV power to the grid.

The microinverter (*μINV*) concept presented in Fig. 1*b* allows parallel connection of PV modules at the grid side [4].

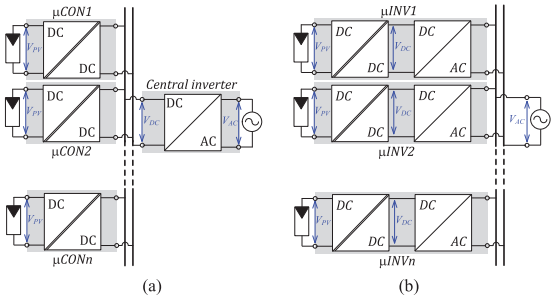

Fig. 1. Full-power converters for the parallel connection of PV modules: microconverters (*μCON*) with common DC bus (a) and microinverters (*μINV*) with grid side connection (b).

In that case, each PV module features direct AC connectivity since *μINV* integrates both the galvanically isolated step-up DC-DC converter and the grid-tied inverter. This concept is common now in residential and small commercial PV power systems mostly because of its expandability as well as simplicity of installation and maintenance.

Both of the approaches discussed (Fig. 1) usually require the DC-DC converter, which must ensure high step-up ratio of the input voltage, maximum power point tracking, at the same time, providing high conversion efficiency. To analyze the technology trends in this field, the state-of-the-art galvanically isolated step-up DC-DC converter topologies for MLPE applications are discussed in Section II. Section III proposes the novel galvanically isolated series resonant quasi-Z-source DC-DC converter as a candidate topology for MLPE applications. Section IV analyzes the multi-mode operation principle of the proposed converter. Further, Sections V and VI present the selected design guidelines and analysis of experimental results. Finally, conclusions are drawn in Section VII.

II. RECENT ADVANCES IN GALVANICALLY ISOLATED DC-DC CONVERTERS FOR MLPE APPLICATIONS

For the last 20 years, the MLPE application was an object of increased research interest all over the world. An insight to the MLPE technology trends is given in several review

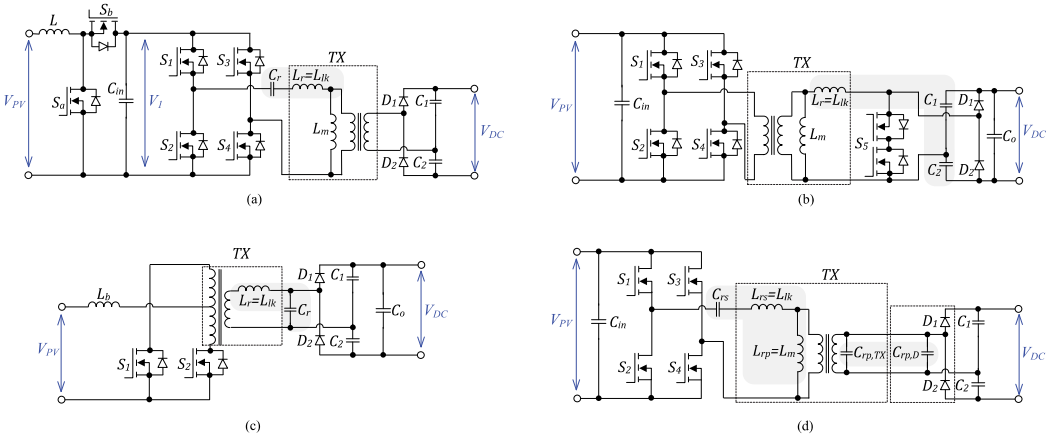

Fig. 2. State-of-the-art DC-DC converters for MLPE applications: double stage topology combined from a front-end synchronous boost converter and series resonant converter (a), double stage topology combined from a series resonant converter and a back-end boost converter based on the bi-directional AC switch (b), single stage approach based on the parallel resonant current-fed push-pull converter (c), and single-stage multiresonant converter (d).

papers [1], [5]-[7]. Except the efficiency, power density, reliability and per-watt-price issues, one of the recent challenges in the design of a good MLPE system is a wide input voltage regulation range. A high-efficiency DC-DC converter with extended input voltage regulation range will support the implementation of the global MPP tracking algorithms, which can substantially improve the energy yield from the PV module under the partial shading conditions [8]. The majority of commercial microinverters today feature the minimum level of the MPP voltage in the range from 22 V [9] to 27 V [10]. To feed power to the grid in European conditions, the grid-side DC-link voltage should be around 400 V, therefore the maximum DC voltage gain of these converters ($G = V_{DC} / V_{PV}$ according to Fig. 1) lies in the range from 14.8 to 18.2. A further decrease of the MPP voltage, for example, to 10 V, could bring the performance level of the microinverters to that of the PV power optimizers [11]. Next, emerging topologies of the high step-up galvanically isolated DC-DC converters for MLPE applications are discussed.

Generally, the high step-up galvanically isolated DC-DC converters for MLPE applications can be categorized as those with a double stage or with a single stage power conversion. In the first case, the front-end boost converter pre-regulates the varying voltage of the PV module to a certain constant voltage level so that the input inverter stage of the high step-up DC-DC converter operates with a near-constant duty cycle. To enhance the efficiency of the double stage conversion approach, the combination of a synchronous boost converter with a series resonant DC-DC converter was proposed in [12]. Such a combination (Fig. 2*a*) resulted in the efficiency close to 97% at a power level of 200 W and it features a wide input voltage regulation range from 15 to 45 V. Another approach called *hybrid series resonant and PWM boost converter* [13] contains a combination of a full-bridge series resonant DC-DC converter with a back-end boost converter based on the bi-directional AC switch (Fig. 2*b*). Thanks to its hybrid structure, the converter is able to regulate the input voltage in a range from 15 to 60 V by using the simple fixed-frequency PWM control and maintaining relatively high efficiency over the entire input voltage and load regulation range.

In a single stage DC-DC power conversion, the primary inverter should operate within a wide input voltage range and optimization of the efficiency could become an issue. Here different approaches were developed to achieve better performance. The simplest structure based on two interleaved flyback converters was proposed by Enphase Energy [14] and due to its overall simplicity, could still be referred to as one of the most popular power conversion approaches for MLPE systems. However, due to its single-ended nature, the main disadvantages of the flyback topology are poor utilization of the isolation transformer and a need for active clamp circuits to minimize the voltage stress of the main switches in the conditions of wide input voltage and load regulation.

To enhance the performance of a single stage DC-DC power conversion approach, it seems more feasible to implement double-ended topologies such as full-bridge, half-bridge or push-pull. For example, the soft-switching current-fed push-pull converter proposed in [15] (Fig. 2*c*) comprises only two switches and allows the non-isolated gate drivers to be used. Thanks to the parallel resonance between the leakage inductance of the isolation transformer and the resonant capacitor C_r, the transistors are turned on and off at the zero-voltage and zero-current conditions. The diodes of the voltage doubler rectifier are also turned off at the zero current, which finally results in a peak efficiency of 96.6% and input voltage regulation range of 20 to 40 V.

Another original approach to the single-stage DC-DC power conversion for MLPE applications was discussed in [16]. The proposed multi-resonant full-bridge DC-DC converter (Fig. 2*d*) features the series and parallel resonant tanks formed by the leakage and magnetizing inductances of the isolation transformer, respectively. The parallel capacitance C_P is a sum of the parasitic capacitances of the rectifying diodes $C_{rp,D}$ and the isolation transformer $C_{rp,TX}$. In this topology, the resonant tank optimized carefully leads to a

peak efficiency of 96% and the input voltage range from 20 to 35 V. To regulate the input voltage, the frequency control is used and the switching frequency is changed in a range from 215 to 268.5 kHz.

The performance of the state-of-the-art DC-DC converter topologies for MLPE applications is compared in Table I. As can be seen, the "best-in-class" converters feature a three- to almost four-fold input voltage regulation range with the peak efficiency of 97%. Further, generalizations regarding the technology development trends in the MLPE systems could be as follows:

- Resonant power conversion is an important attribute of the modern galvanically isolated DC-DC converters for PV applications since it allows the soft-switching of semiconductors and could help improve the power density of the converter by increasing the switching frequency. The most popular type of resonance used is the series resonant with the maximum possible utilization of the parasitic elements of the circuit, i.e. leakage inductance of the transformer.
- Voltage doubler rectifier (VDR) is typically used in the secondary side of the converter to reach higher DC voltage gain at a given transformer turns ratio. Furthermore, the VDR enables realization of the integrated series resonant tank at the secondary side of the converter, i.e. when the leakage inductance of the isolation transformer is used as a resonant inductor and capacitors of the VDR are used as resonant capacitors.
- Implementation of the wide-bandgap semiconductors enables the peak efficiencies to be well over 97%. It seems to be most feasible to use SiC Schottky Barrier Diodes (SBD) in the VDR with the output voltages over 380 VDC since they feature extremely low reverse recovery charge, which results in the low switching losses and higher efficiency. Moreover, the high operating junction temperature of the SiC SBD is especially important in terms of the high thermal stress and reliability requirements applied to the MLPE systems. To improve the efficiency further, GaN transistors could be implemented; however, it could also impose some cost penalties, especially in the current situation when the per Watt prices of the MLPE systems are ramped down.

III. Galvanically Isolated Quasi-Z-Source Series Resonant DC-DC Converter

In this paper, the galvanically isolated quasi-Z-source series resonant DC-DC converter (qZSSRC) is examined as a candidate topology for PV MLPE applications (Fig. 3). The converter consists of the qZS network (L_{qZS1}, L_{qZS2}, C_{qZS1}, C_{qZS2}, S_{qZS}), a full-bridge inverter ($S_1 \ldots S_4$), a step-up isolation transformer TX and the voltage doubler rectifier (D_1, D_2, C_1, C_2). At its secondary side, the converter has a series resonant tank formed by the leakage inductance of the isolation transformer and the VDR capacitors. The output filter capacitance C_f is used for the output voltage filtering as well as to buffer the double line frequency voltage ripple caused by a grid side inverter.

TABLE I. Performance Comparison of New Emerged High Step-Up DC-DC Converters for MLPE Applications

Fig. [ref]	P_{max} (W)	V_{PV} (V)	V_{DC} (V)	Peak eff. (%)	Type of resonance
2*a* [12]	275	15…45	400	97	Series
2*b* [13]	300	15…55	320	97.4	Series
2*c* [15]	244	20…35	700	96	Parallel
2*d* [16]	250	20…40	400	96.6	LLCC

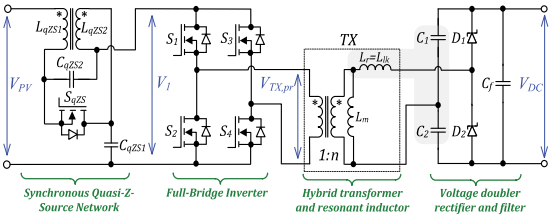

Fig. 3. Generalized topology of the galvanically isolated series resonant quasi-Z-source DC-DC converter (qZSSRC).

To improve the performance, a number of modifications were introduced to the baseline qZSSRC topology, which was originally proposed in [17]. First, to reduce the conduction losses in the input stage of the converter, the concept of the synchronous qZS-network was implemented [18], [19]. In the original qZS-network [20], a diode is needed to avoid short-circuiting of the capacitors C_{qZS1} and C_{qZS2} during the shoot-through states. In the synchronous qZS-network (Fig. 3), the n-channel MOSFET S_{qZS} is placed instead of the diode and is synchronized with the inverter switches such that it conducts only during the active states of the inverter. To prevent conduction of the S_{qZS} during the shoot-through states, a dead-time is introduced before its turn on and off transients.

Another important modification of the qZS-network is the implementation of a coupled inductor instead of two discrete inductors in the traditional approach [20]. This modification resulted in both higher power density of the converter and an extra benefit from using the input (PV side) wiring inductance for further reduction of the input current ripple of the converter. The qZSSRC topology proposed combines numerous advantages of the voltage-fed and current-fed converters, while utilizing the best practice of the full-bridge impedance-source converter implementation [21].

As compared to the baseline qZSSRC topology, the proposed converter contains the fully integrated series resonant tank at the secondary side (secondary resonance). On the one hand, the capacitors of the VDR which are charged and discharged in parallel, form the resonance capacitor with an equivalent capacitance value C_r:

$$C_r = C_1 + C_2, \tag{1}$$

where C_1 and C_2 are the capacitance values of VDR capacitors. On the other hand, the series resonant tank is formed by the leakage inductance of the isolation transformer referred to the secondary winding (L_{lk}); therefore, the resonant frequency can be defined as:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{L_{lk}\cdot C_r}} = \frac{1}{2\pi}\sqrt{\frac{1}{L_{lk}\cdot (C_1 + C_2)}}. \tag{2}$$

It should be noted that the second resonance frequency also exists due to the magnetic integration of the resonant inductor:

$$f_{r2} = \frac{1}{2\pi}\sqrt{\frac{1}{(L_{lk}+L_m)\cdot C_r}}, \quad (3)$$

where L_m is the magnetizing inductance of the isolation transformer referred to the secondary winding. Typically, the leakage inductance of the transformer is below 2 % of the value of the magnetizing inductance [12] and the resonance frequencies f_r and f_{r2} differ by a factor of 10.

The integrated resonant tank implemented enables avoiding the size and cost penalties associated with the use of external resonant elements. The secondary side of the proposed converter could be further simplified by the implementation of the Greinacher voltage doubler rectifier (Fig. 4). In that case, the first capacitor of the VDR acts as a resonant capacitor C_r and the second operates as a buffer of the double line voltage ripple from the grid side inverter. However, in this VDR configuration, the capacitors have different voltage stresses. In addition, the current stresses are also different since their capacitance values differ by more than 10 times, which is caused by their different functions.

IV. Multi-Mode Operating Principle of the qZSSRC

To extend the input voltage regulation range without serious efficiency penalties, the proposed MIC uses a multi-mode operation. Due to the unique properties of the qZS network, the qZSSRC is capable of combining the shoot-through pulse-width modulation (PWM) and ordinary phase-shift modulation (PSM) for the realization of the boost and buck operating modes, respectively. Moreover, in the boundary between these modes, the converter operates in a normal mode as a pure series resonant converter (SRC) at the resonant frequency. Fig. 5 shows an example of idealized control variables of the proposed qZSSRC operating within the input voltage range from $0.5\cdot V_{PV(MPP)}$ to $1.5\cdot V_{PV(MPP)}$. Next, the operating principle of the converter in these three modes is analyzed in detail.

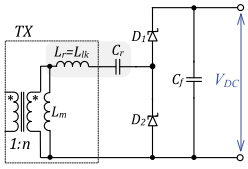

Fig. 4. Greinacher voltage doubler rectifier as an alternative option for the qZSSRC secondary side.

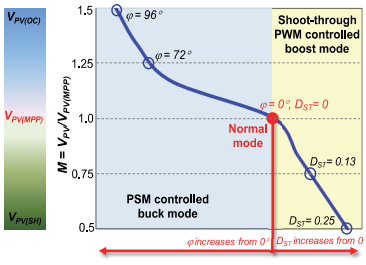

Fig. 5. An example of operating modes and idealized control variables of the multi-mode qZSSRC.

In order to simplify the analysis of the operating modes of the converter, the following assumptions were made:

- the converter features no power dissipation in the elements;
- MOSFET switches are ideal except for their body diodes and output capacitances;
- output filtering capacitance C_f is large enough so that the DC output voltage V_{DC} can be considered as ripple-free;
- the transformer is composed of an ideal transformer with turns ratio 1:n, a magnetizing inductance L_m and a leakage inductance L_{lk}, both referred to the secondary winding;
- C_f is much larger than the VDR capacitors C_1 and C_2, and, therefore, has no influence on the resonance process;
- VDR capacitors C_1 and C_2 have equal capacitance values and their sum is represented as C_r.

A. Normal Mode

According to Fig. 5, the normal mode corresponds to the maximum power point of the PV module at the most common operating conditions. In this operating point, the duty cycle of the inverter switches is close to 0.5 after the dead-time deduction. The switch S_{qZS} is constantly conducting and the operation of the qZSSCR is similar to that of the traditional SRC operating at the resonant frequency. The steady-state waveforms of the qZSSRC operating in the normal mode are presented in Fig. 6.

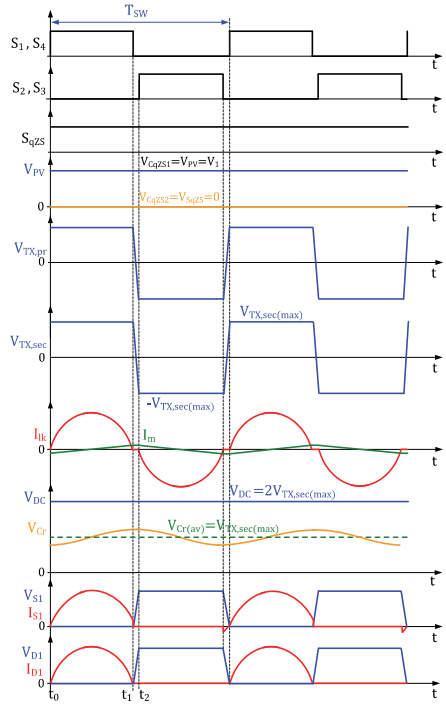

Fig. 6. Steady-state waveforms of the qZSSRC operating in the normal mode.

Next, the operation principle of the qZSSRC in the normal mode is analyzed for the positive half-cycle:

[$t_0 < t < t_1$, Fig. 8*a*]: switches S_1 and S_4 are turned on and input voltage V_{PV} is applied to the primary winding of the isolation transformer. Since the switching frequency is equal to the resonant frequency ($f_{SW} = f_r$), the current of the L_{lk} and the voltage of the parallel combination of C_1 and C_2 fully resonate, which results in almost pure sinusoidal waveforms. The current of the magnetizing inductance L_m linearly increases to its maximum value:

$$i_{Lm(p)} = \frac{V_{PV} \cdot n \cdot T_{sw}}{4 \cdot L_m}. \quad (4)$$

At the instant t_1, when the resonant current reaches zero, the switches S_1 and S_4 are turned off and the VDR diode D_1 turns off at zero current switching (ZCS). The magnetizing current, which is still present in the switches S_1 and S_4, could be considered as relatively small; therefore, it is assumed that S_1 and S_4 are also commutated in the near-ZCS conditions.

[$t_1 < t < t_2$, Fig. 8*b*]: switches S_1 and S_4 are turned off and the qZSSRC features dead-time of the inverter during this time interval. The magnetizing inductance of the isolation transformer charges the output capacitances of S_1 and S_4 and, at the same time, discharges the output capacitances of S_2 and S_3. If the dead-time and magnetizing inductance of the isolation transformer are correctly dimensioned, the drain-source voltages of S_2 and S_3 will reach zero before the beginning of the next resonance half-cycle. Therefore, it could be stated that at t_2, the switches S_2 and S_3 will be turned on under the zero-voltage switching (ZVS) conditions. In practice, the minimum dead-time required depends on the operating point and ambient temperature. Hence, it has to be selected large enough in order to discharge capacitors to zero voltage, or even force corresponding body diodes to the conduction state before the instant t_2, as shown in Fig. 8*c*, regardless of the operating point.

In the normal mode, the voltage stresses of the qZS capacitors are as follows:

$$V_{CqZS1(normal)} = V_{PV}\,;\; V_{CqZS2(normal)} = 0\,. \quad (5)$$

The average voltage of the VDR capacitors is half the output voltage and their voltage ripple could be found as:

$$\Delta v_{Cr(normal)} = \frac{P \cdot T_{sw}}{4 \cdot V_{DC} \cdot C_r}, \quad (6)$$

where P is the operating power of the converter. The normalized voltage gain of the qZSSRC in the normal mode could be expressed by (7) and is similar to that of the traditional SRC operating at the resonant frequency:

$$G_{normal} = \frac{V_{DC}}{2 \cdot n \cdot V_{PV}} = 1\,. \quad (7)$$

B. Buck Mode

When the input voltage is higher than the predefined nominal value, the converter starts to operate in the buck mode. In this mode, the qZSSRC could be regarded as a SRC with the PSM control, i.e. when the output voltage is controlled by the phase shift angle φ between the two inverter legs at the resonant frequency ($f_{SW} = f_r$). Fig. 7 shows the steady-state waveforms of the converter in the buck mode.

[$t_0 < t < t_1$, Fig. 9*a*]: switches S_1 and S_4 are turned on and input voltage V_{PV} is applied to the primary winding of the isolation transformer. The current of the L_{lk} and the voltage of the parallel combination of C_1 and C_2 start to resonate and the magnetizing current linearly increases to its maximum value:

$$i_{Lm(p)} = \frac{V_{PV} \cdot n \cdot T_{sw}}{2 \cdot L_m} \times \frac{\varphi}{360}. \quad (8)$$

[$t_1 < t < t_2$, Fig. 9*b*]: at t_1, the switch S_4 turns off with ZVS and the converter enters the dead-time interval. Since the resonance was suddenly interrupted, the currents are still present in the leakage and magnetizing inductances of the isolation transformer. They discharge the output capacitance of S_3 while charging the output capacitance of S_4. This will ensure the ZVS turn-on of S_3 at the instant t_2. Its body diode could be conducting at t_2 if the dead-time is over-dimensioned.

[$t_2 < t < t_3$, Fig. 9*c*]: at t_2, the switch S_3 turns on at the ZVS conditions and the converter enters the zero state, when the primary winding of the isolation transformer is shorted by the top transistors of the inverter bridge (S_1 and S_3). The voltage of the isolation transformer is zero and the magnetizing current remains unchanged at its maximum value (8).

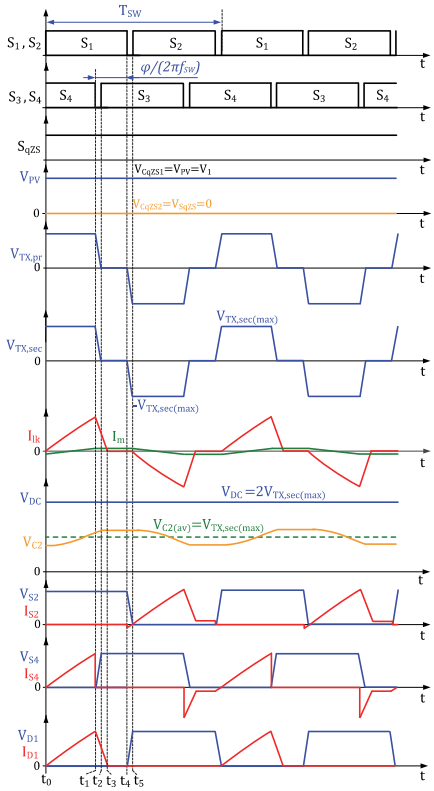

Fig. 7. Steady-state waveforms of the qZSSRC operating in the buck mode.

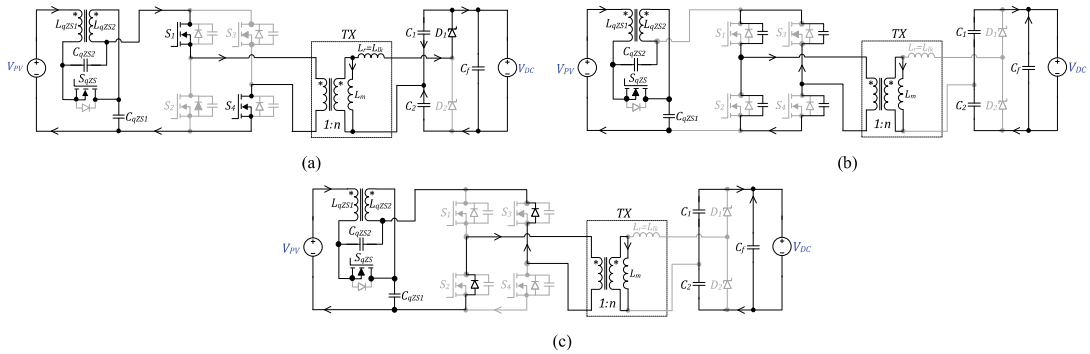

Fig. 8. Generalized equivalent circuits of the qZSSRC operating in the normal mode: $t_0 < t < t_1$ (a), $t_1 < t < t_2$ (b), and directly before the instant t_2 (c).

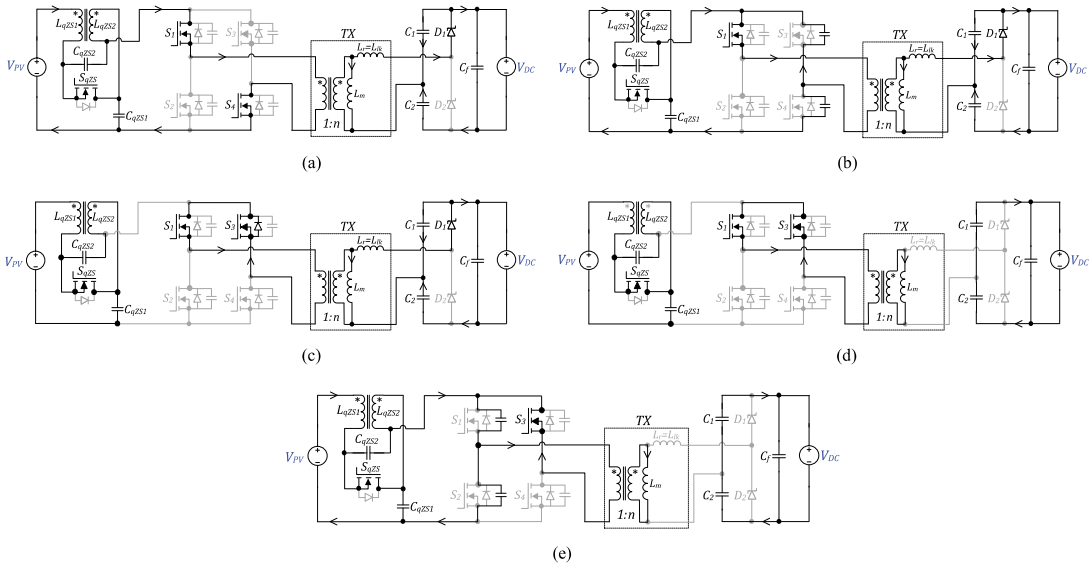

Fig. 9. Generalized equivalent circuits of the qZSSRC operating in the buck mode: $t_0 < t < t_1$ (a), $t_1 < t < t_2$ (b), $t_2 < t < t_3$ (c), $t_3 < t < t_4$ (d) and $t_4 < t < t_5$ (e).

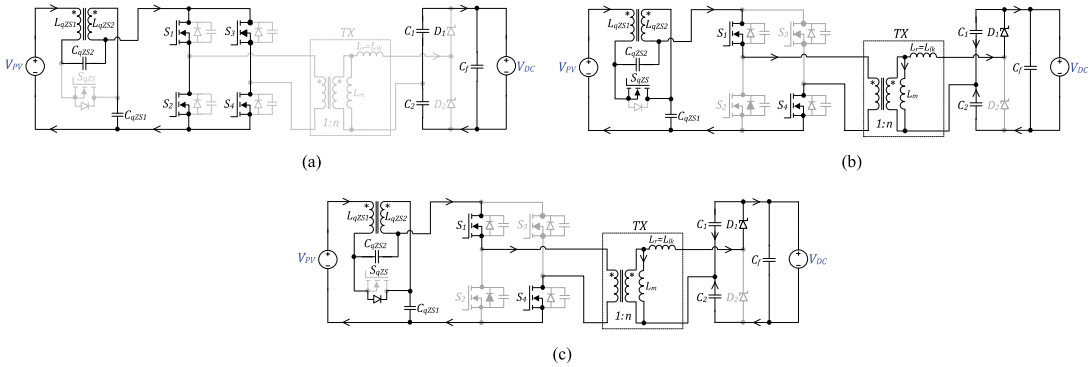

Fig. 10. Generalized equivalent circuits of the qZSSRC operating in the boost mode: $t_0 < t < t_1$ (a), $t_1 < t < t_2$ (b) and during the dead-time of the S_{qZS} (c).

[$t_3 < t < t_4$, Fig. 9*d*]: at t_3, the current through the leakage inductance decreases to zero and the converter enters the discontinuous conduction mode (DCM). During DCM, the leakage inductance current remains zero and the power is not transferred from the input to the output side. Thanks to DCM, the VDR diodes feature ZCS, while the switch S_1 – near-ZCS.

[$t_4 < t < t_5$, Fig. 9*e*]: at t_4, the switch S_1 turns off and the converter enters the dead-time interval. The current through the leakage inductance is still zero; therefore, the S_1 features near-ZCS combined with ZVS (due to magnetizing current) turn-off. The magnetizing current charges the output capacitance of S_1 while discharging the output capacitance of S_2. When the output capacitance of S_2 is fully discharged, its body diode starts conduction, which results in the ZVS turn on of the S_2 at the time instant t_5. Next, the converter enters the negative half-cycle, when the negative input voltage V_{PV} is applied to the primary winding of the isolation transformer.

In the buck mode, the voltage stresses of the qZS capacitors are similar to those in the normal mode. The normalized voltage gain of the qZSSRC in the buck mode is similar to that of the traditional SRC with PSM control at the resonant frequency [23]:

$$G_{buck(DCM)} = \frac{V_{DC}}{2nV_{PV}} = 0.5\left[A\left(\frac{2}{\pi Q}-1\right)+\sqrt{\left(\frac{2}{\pi Q}-1\right)^2 A^2 + A\frac{8}{\pi Q}}\right], \quad (9)$$

where

$$A = 0.5 - 0.5\cos\left[\pi\left(1-\frac{\varphi}{180}\right)\right], \quad (10)$$

$$Q = \frac{8\pi f_{SW} L_{lk}}{R_L}. \quad (11)$$

Fig. 11 shows that the normalized voltage gain of the qZSSRC strongly depends on the Q-factor of the resonant tank and the phase shift angle φ. It is important to notice that at Q-factors equal or higher than one, the converter starts operating with the continuous current through the resonant network and its regulation characteristic becomes more flat [24].

C. Boost Mode

If the input voltage drops below the predefined nominal level, the converter starts to operate in the boost mode similar to the traditional qZS converter [20]. The output voltage is controlled by the duration of the shoot-through state t_{ST}, i.e.

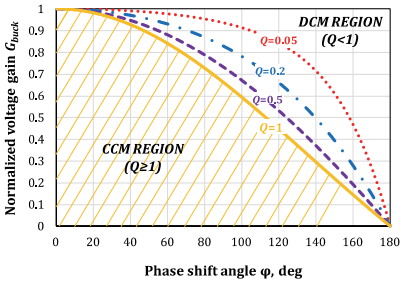

Fig. 11. Normalized voltage gain of the qZSSRC as a function of the phase shift angle φ for the different Q-factors of the resonant network.

when all the switches of the inverter bridge are simultaneously turned on. Shoot-through states are generated by increasing the duty cycle of the switches over 0.5, which causes the active states of the top (S_1, S_3) and the bottom (S_2, S_4) switches to overlap with each other [22]. The switching frequency of the qZSSRC in the boost mode remains fixed to the resonant frequency. The inverter switches are controlled without dead-time and the steady-state waveforms are shown in Fig. 12.

[$t_0 < t < t_1$, Fig. 10*a*]: at t_0, all four switches of the inverter bridge are turned on and the converter enters the shoot-through state. The switch S_{qZS} is turned off before the instant t_0 and its body diode is reverse-biased. The voltage stresses of the qZS capacitors could be estimated by:

$$V_{CqZS1(boost)} = \frac{V_{PV}(1-D_{ST})}{1-2D_{ST}};\ V_{CqZS2(boost)} = \frac{V_{PV}D_{ST}}{1-2D_{ST}}; \quad (12)$$

$$D_{ST} = \frac{t_{ST}}{T_{SW}}. \quad (13)$$

During the shoot-through state, the currents of the qZS inductor will linearly increase to their maximum value:

$$I_{LqZS(\max)} = I_{PV} + \frac{V_{PV}D_{ST}}{4L_{qZS}f_{SW}} \cdot \frac{1-D_{ST}}{1-2D_{ST}}, \quad (14)$$

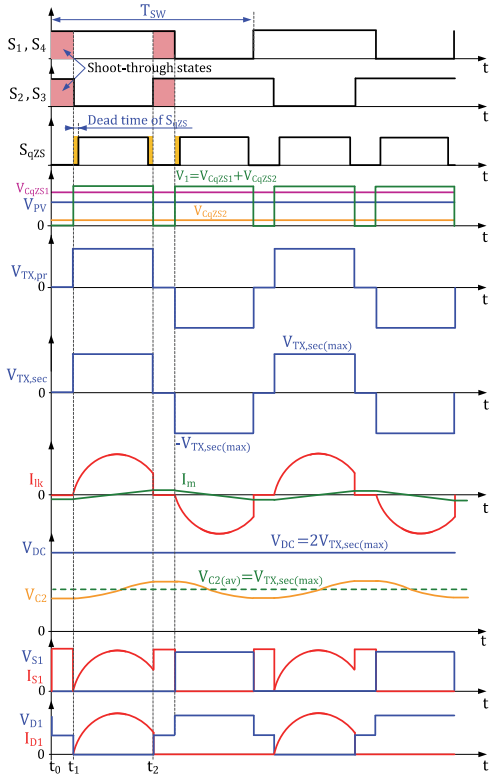

Fig. 12. Steady-state waveforms of the qZSSRC operating in the boost mode.

where I_{PV} is the average input current of the converter and L_{qZS} is the magnetizing inductance value of the qZS inductor.

[$t_1 < t < t_2$, Fig. 10*b*]: at t_1, the switches S_2 and S_3 are turned off, the synchronous switch S_{qZS} is turned on after dead-time and the active state begins. Diagonal switches S_1 and S_4 are conducting and the stepped-up voltage from the qZS network is applied to the primary winding of the isolation transformer:

$$V_{TX,pr(\max)} = V_{CqZS1} + V_{CqZS2} = \frac{V_{PV}}{1-2D_{ST}}. \quad (15)$$

Similar to the normal mode, the current of the L_{lk} and the voltage of parallel combination of C_1 and C_2 start resonating. The qZS inductor current is linearly decreasing to minimum:

$$I_{LqZS(\min)} = I_{PV} - \frac{V_{PV} D_{ST}}{4L_{qZS} f_{SW}} \cdot \frac{1-D_{ST}}{1-2D_{ST}}. \quad (16)$$

At the instant t_2, the switches S_2 and S_3 are turned on, while the switch S_{qZS} turns off before that instant. The resonance ends early and the converter enters the second shoot-though state similar to [$t_0 < t < t_1$]. It is seen from Fig. 12 that in the boost mode, the inverter switches are always hard switched, while the VDR diodes feature the near-ZCS operation.

In order to prevent the damage of the circuit, which could be caused by the simultaneous conduction of the inverter transistors and synchronous switch S_{qZS} during the shoot-through states, a dead-time is introduced before the turn on and off transients of the S_{qZS}, as shown in Fig. 12. During the dead-time, the body diode of the S_{qZS} is conducting and the equivalent circuit of the converter during that time period is shown in Fig. 10*c*. This state enables safe transition from the shoot-trough to the active state and should be longer than the control signal propagation delay of the inverter switches.

The normalized voltage gain of the qZSSRC in the boost mode depends directly on the shoot-through duty cycle D_{ST}:

$$G_{boost} = \frac{V_{DC}}{2nV_{PV}} = \frac{1}{(1-2D_{ST})}. \quad (17)$$

It is seen from Fig. 13 that for the threefold input voltage regulation range, the shoot-through duty cycle should vary in the range from 0 to 0.33. However, in real systems, the practical voltage gain in the boost mode could be seriously affected by the losses in the primary side of the converter where the major part is formed by the conduction losses of semiconductors [25].

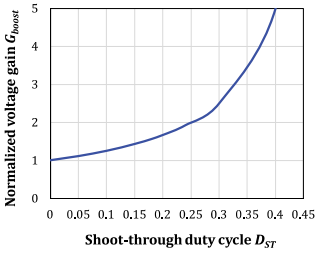

Fig. 13. Normalized voltage gain of the qZSSRC in a boost mode.

V. Converter Design and Control Considerations

A. Magnetically Integrated Quasi-Z-Source Network

To improve the power density, the proposed qZSSRC features the magnetically integrated qZS network, which is based on the coupled inductor with unity turns ratio. The highest current ripple through the coupled inductor occurs in the boost mode at the minimum input voltage, when the shoot-through duty cycle reaches its maximum value. Fig. 14 shows the equivalent circuit of the synchronous magnetically integrated quasi-Z-source network.

Usually, the qZS network is considered symmetrical and therefore, the leakage inductances are omitted from the design guidelines [26]. In real systems, the parasitic inductance of interconnection wires between the PV module and the converter (L_w) contributes to the input winding leakage inductance L_{lk1}, which results in different current ripples of the winding currents I_1 (i.e. I_{PV}) and I_2:

$$\Delta I_1 = \frac{V_{PV(\min)} \cdot L_{lk1^*} \cdot D_{ST(\max)} \cdot (1-D_{ST(\max)})}{f_{SW} \cdot (L_{lk1^*} \cdot L_{lk2} + L_{Mi} \cdot (L_{lk1^*} + L_{lk2})) \cdot (1-2 \cdot D_{ST(\max)})}; \quad (18)$$

$$\Delta I_2 = \frac{V_{PV(\min)} \cdot L_{lk2} \cdot D_{ST(\max)} \cdot (1-D_{ST(\max)})}{f_{SW} \cdot (L_{lk1^*} \cdot L_{lk2} + L_{Mi} \cdot (L_{lk1^*} + L_{lk2})) \cdot (1-2 \cdot D_{ST(\max)})}, \quad (19)$$

where L_{lk1^*} is the effective leakage inductance of the input winging of the coupled inductor (L_{lk1^*}=L_{lk1}+L_w), $V_{PV(min)}$ is the minimum input voltage value of the converter, and $D_{ST(max)}$ is the corresponding maximum shoot-through duty cycle.

Generally, Eqs. (18) and (19) are an extended version of Eqs. (14) and (16), since they will provide the same results if leakage inductances are equal and converge to zero. Moreover, the current ripple ratio depends inversely proportional on the leakage inductances ratio, as shown in Fig. 15. However, the mismatch of the leakage inductance has only slight influence on the current of the magnetizing inductance L_{Mi}, as shown by the following expression for the maximum magnetizing current $I_{LMi(max)}$:

$$I_{LMi(\max)} = \frac{2 \cdot P}{V_{PV(\min)}} + \frac{V_{PV(\min)} \cdot D_{ST(\max)} \cdot (1-D_{ST(\max)})}{2 \cdot f_{SW} \cdot \left(\frac{L_{lk1^*} \cdot L_{lk2}}{L_{lk1^*} + L_{lk2}} + L_{Mi} \right) \cdot (1-2 \cdot D_{ST(\max)})}. \quad (20)$$

Typically, the values of leakage inductances are considerably smaller than the magnetizing inductance value, even when considering parasitic inductance of interconnection wires. Hence, the simplified equation can be used for the dimensioning of the coupled inductor:

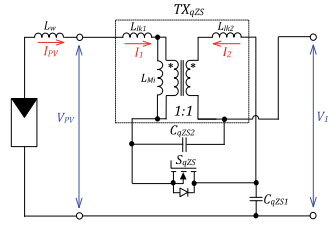

Fig. 14. Equivalent circuit of the magnetically integrated qZS network.

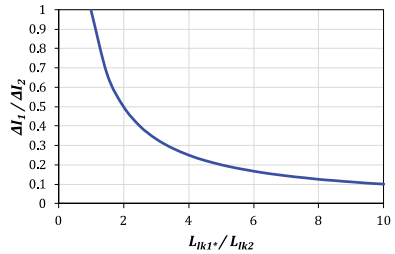

Fig. 15. Current ripple ratio as a function of the leakage inductance ratio.

$$I_{LMi(\max)} \approx \frac{2 \cdot P}{V_{PV(\min)}} + \frac{V_{PV(\min)} \cdot D_{ST(\max)} \cdot (1 - D_{ST(\max)})}{2 \cdot L_{Mi} \cdot f_{SW} \cdot (1 - 2 \cdot D_{ST(\max)})}. \quad (21)$$

Due to the high current ripple in the qZS network, voltage ripple of the qZS capacitors (ΔV_{CqZS}) has the highest value in the boost mode at the minimum input voltage:

$$\Delta V_{CqZS} = \Delta V_{CqZS1} = \Delta V_{CqZS2} \approx \frac{P \cdot D_{ST(\max)}}{C_{qZS} \cdot f_{SW} \cdot V_{PV(\min)}}, \quad (22)$$

where C_{qZS} is the capacitance of the qZS capacitors. It is evident that they feature the same absolute value of the voltage ripple, while their relative ripple is different. Average voltages of the qZS capacitors depend on the operating mode of the converter and can be found in Section III.

B. Integrated Series Resonant Tank

To improve power density, the proposed converter contains a fully integrated series resonant tank at its secondary side (Fig. 3), which is formed t leakage inductance referred to he secondary winding (L_{lk}) of the isolation transformer and the parallel combination of the VDR capacitors ($C_1 + C_2$). One of distinguishing features of the proposed converter is that due to the discontinuous current through the resonant network, it enables the ZCS of the inverter switches and VDR. Therefore, the critical value of the L_{lk} when the converter still maintains DCM, could be found from (11) as follows:

$$L_{lk(cr,DCM)} < \frac{V_{DC}^2}{8\pi P f_{SW}}. \quad (23)$$

In high-frequency low-power transformers, the maximum value of the leakage inductance is significantly smaller than the critical value set by (23) since it is strictly limited by the physical design of the transformer. On the other hand, smaller values of L_{lk} will lead to higher currents through the isolation transformer, which will result in increased current stresses of the semiconductors.

To maintain the resonance, the values of VDR capacitors could be selected by:

$$C_1 = C_2 = \frac{1}{8 L_{lk} \pi^2 f_{SW}^2}. \quad (24)$$

Since the discussed converter has its maximum efficiency in the normal mode, special attention should be paid to the proper selection of the dead-time. During the dead-time, the parasitic output capacitances of the inverter switches are charged and discharged by the magnetizing current of the transformer, which results in the robust full ZVS and near-ZCS operation of the inverter switches. The minimal value of the dead-time could be found by:

$$T_D \geq \frac{8 L_m f_{SW} C_{oss}}{n^2}, \quad (25)$$

where C_{oss} is the parasitic output capacitance of the main switches.

C. Multi-Mode Control Principle

As described in Section III, the proposed converter features multi-mode operation to ensure the wide input voltage and load regulation. In the boost mode, the shoot-through PWM is used for the regulation of the output voltage. In the normal mode, the shoot-through states are eliminated and the converter operates as a typical voltage-fed SRC featuring fixed DC voltage gain. In the buck mode, the output voltage is controlled by the PSM at the resonant frequency. The carrier-based control signal generation of the proposed converter is shown in Fig. 16.

The control system requires a microcontroller, which utilizes the floating-point core or unit and enhanced PWM peripheral. It should contain High Resolution Timer (HRTIM) peripheral, which can generate at least 10 PWM signals in order to achieve the maximum performance. Eventually, the HRTIM should be made of at least four 16-bit up-counters with synchronous auto-reload (further they are called units), while each of them should feature at least four compare registers. Clock frequency should be high enough in order to achieve acceptable PWM resolution to set short intervals, like dead-time, properly. For a converter with the switching frequency around 100 kHz, PWM clock frequency is recommended to be higher or equal to 200 MHz.

Control signals of switches S_1 and S_2 are controlled by the timer unit *C* and the corresponding compare values *C.CMP1…C.CMP4*. Signals of switches S_3 and S_4 are controlled by the timer unit *D* and the corresponding compare values *D.CMP1…D.CMP4*. Control signal of the synchronous switch S_{qZS} is generated by the timer unit *E* and it is based on the compare values *E.CMP1…E.CMP4*. All timer channels are synchronized and therefore, only one counter sawtooth signal is shown in Fig. 16. Generally, every control signal requires only two compare values: one for setting it to logical "1" and the other for resetting to logical "0". However, the control signal of the S_{qZS} has the double switching frequency as compared to other control signals. This means that it requires four compare values per switching period.

Calculation of the compare values is unified, since they are defined by the same equations in all operating modes. There is one main difference between the operating modes: in the boost mode, the phase-shift value φ is equal to zero (Fig. 16*a*), while the shoot-through duty cycle D_{ST} is zero in the buck mode (Fig. 16*b*). Moreover, the synchronous switch S_{qZS} is always turned on in the buck and normal modes. Hence, all the compare values of the timer unit *E* are ignored and its output is forced to the logical "1". Basically, the normal mode can be

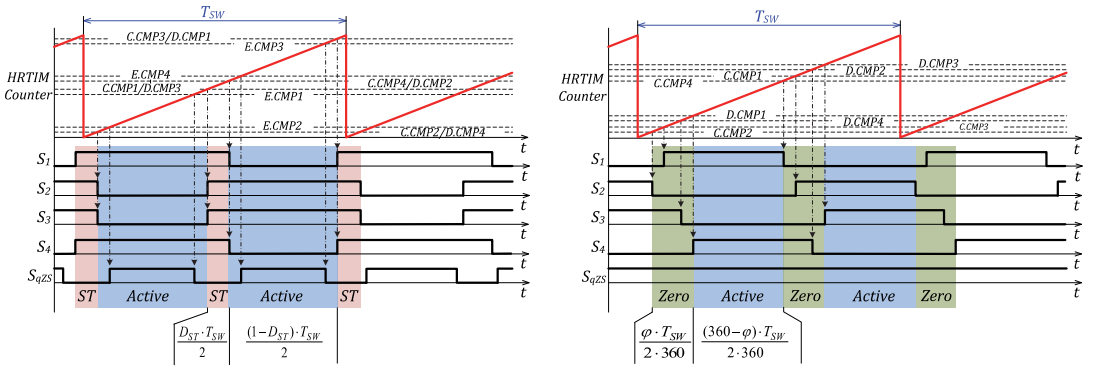

Fig. 16. Generalized principle of the control signal generation in the boost (a) and the buck (b) modes.

considered as the buck mode with zero phase-shift. For simplicity of explanation, all compare values and the sawtooth signal are normalized to be within the range from 0 to 1, as shown in Fig. 16.

If the calculated compare value is higher than 1 or is negative, it has to be shifted to the next or the previous sawtooth period, correspondingly. Expressions for the calculation of the compare values are presented in Table II. They are taking into account the following relative dead-time values: *dt_T* –the qZS inverter transistors dead-time, *dt_D_on* –the transistor S_{qZS} turn-on dead-time, *dt_D_off* – the transistor S_{qZS} turn-off dead-time.

VI. Experimental Verification

A. Description of the Prototype

For the experimental verification of the proposed concept, the prototype of the wide input voltage range PV microconverter based on the qZSSRC topology has been developed (Fig. 18). General specifications of the prototype are listed in Table III.

The converter was designed to operate within the input voltage range from 10 to 60 V and with the power profile shown in Fig. 17. This power profile was specially synthesized in order to simulate the operation conditions of MLPE converters powered by the 60-cell PV modules [27].

TABLE II. Expressions for Calculation of the Compare Values

C.CMP1	$0.5+dt\_T-\frac{D_{ST}}{4}$	*D.CMP3*	$0.5-\frac{\varphi}{360}+dt\_T-\frac{D_{ST}}{4}$
C.CMP2	$\frac{D_{ST}}{4}-dt\_T$	*D.CMP4*	$1-\frac{\varphi}{360}+\frac{D_{ST}}{4}-dt\_T$
C.CMP3	$dt\_T-\frac{D_{ST}}{4}$	*E.CMP1*	$0.5-\frac{D_{ST}}{4}-dt\_D\_off$
C.CMP4	$0.5+\frac{D_{ST}}{4}-dt\_T$	*E.CMP2*	$0.5+\frac{D_{ST}}{4}+dt\_D\_on$
D.CMP1	$1-\frac{\varphi}{360}+dt\_T-\frac{D_{ST}}{4}$	*E.CMP3*	$1-\frac{D_{ST}}{4}-dt\_D\_off$
D.CMP2	$0.5-\frac{\varphi}{360}+\frac{D_{ST}}{4}-dt\_T$	*E.CMP4*	$\frac{D_{ST}}{4}+dt\_D\_on$

The control system of the converter was realized on the ST STM32F334 microcontroller, which utilizes the Cortex-M4 core with a floating-point unit and enhanced PWM peripheral.

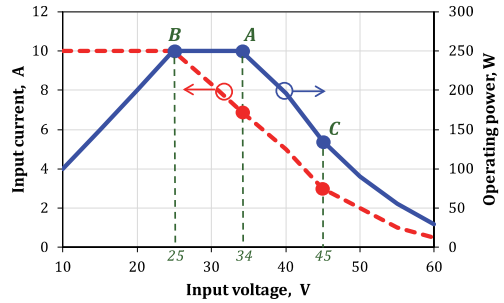

Fig. 17. Input current and operating power of the experimental prototype as functions of the input voltage.

TABLE III. General Specifications of the Experimental Prototype

Operating parameters	
Input voltage range, V_{PV}	10…60 V
Nominal input voltage, $V_{PV,nom}$	34 V
Maximal input current, I_{PV}	12 A
Output voltage, V_{DC}	400 V
Switching frequency, f_{SW}	110 kHz
Dead-time of inverter switches	120 ns
Dead-time of synchronous switch	45 ns
Operating power range	25…300 W
Components	
$S_1...S_4$, S_{qZS}	Infineon BSC035N10NS5
D_1, D_2	CREE C3D02060E
L_{qZS1}, L_{qZS2}	22 µH
C_{qZS1}, C_{qZS2}	26.4 µF
C_1, C_2	43 nF
C_f	100 µF
L_{lk}	24 µH
L_m	1 mH
n	6

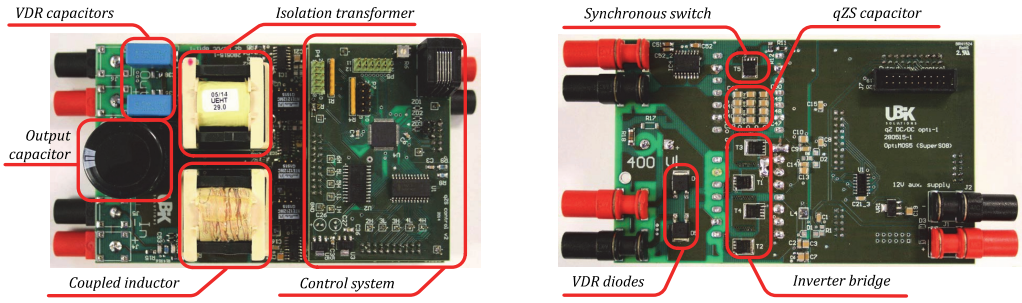

Fig. 18. Top (a) and bottom (b) views of the 300 W experimental prototype of the wide input voltage range PV microconverter based on the qZSSRC topology.

A simplified block diagram of the control system developed for the proposed converter is shown in Fig. 19. The input voltage sensor is non-isolated, however, the input current and output voltage sensors feature galvanic isolation. This architecture of the measurement subsystem results from the design of the control system that has common zero potential with the input side of the converter. Output signals of the sensors are then converted into a digital form using an integrated 12-bit analog-to-digital converter (ADC) of the microcontroller.

Software control algorithm is executed only when the protection algorithm reports that the measured values are within the safety range. Maximum power point tracking algorithm calculates the reference input voltage $V_{PV(ref)}$. Error between the reference and measured values of the input voltage is applied to the input of the PI controller. Saturation block with a mode selector allows smooth transition between the operating modes of the converter. Positive values of the PI controller output define the shoot-through duty cycle, while negative values determine the phase shift angle. Shoot-through duty cycle and phase shift angle define the compare values of the high resolution timer (HRTIM), which is employed in the microcontroller. Equations for the calculation of the compare values are shown in Table II. The HRTIM generates control signals for the converter transistors. The physical output signals of the HRTIM are forwarded to the gate drivers of the corresponding transistors.

The proposed control system is quite simple since it does not control the DC-link voltage. In many distributed generation applications, the DC-link voltage is balanced by the power consumption of the load, i.e. inverter, energy storage, etc. Hence, the experimental study was performed by using the electronic DC load in the constant voltage mode. If the DC-link voltage exceeds the limits defined for the normal operation, the protection algorithm will disable the converter operation.

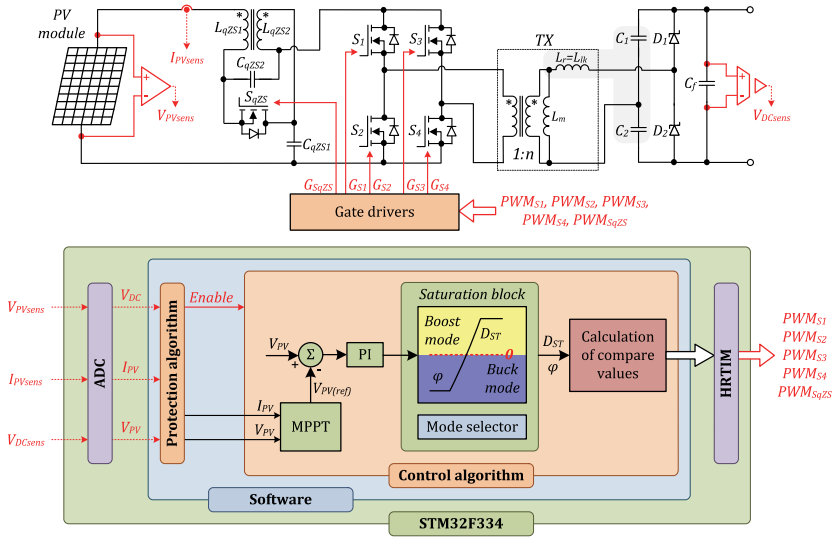

Fig. 19. Block diagram of the control system developed for the proposed converter.

B. Experimental Results

Steady-state operating waveforms of the experimental multi-mode qZSSRC are presented in Figs. 20-22. To acquire the operating waveforms, the digital phosphor oscilloscope Tektronix DPO7254 equipped with the Rogowski coil current probe PEM CWTUM/015/R, current probe Tektronix TCP0030A and high-voltage differential voltage probes Tektronix P5205A were used. The converter was supplied by the PV panel simulator Keysight E4360 and loaded by the programmable DC electronic load Chroma 63204.

First, the converter was tested in the normal mode at $V_{PV} = 34$ V and $P = 250$ W (point *A* in Fig. 17). The switching frequency was equal to the resonant frequency and the current through the isolation transformer has pure sinusoidal waveform (Fig. 23*c*). As a result, the inverter switches (Fig. 23*d*) and VDR diodes (Fig. 23*e*) are all operating under ZCS. Moreover, the inverter switches feature ZVS in addition to the near-ZCS due to magnetizing current recharging parasitic output capacitances. As can be seen from Fig. 23*c*, the synchronous switch S_{qZS} is constantly conducting, the voltage of capacitor C_{qZS2} is zero and the voltage of the capacitor C_{qZS1} equals the input voltage.

Steady-state waveforms of the proposed converter in the buck mode with 45 V input and an operating power of 135 W are shown in Fig. 24 (point *C* in Fig. 17). To step-down the input voltage, the phase shift angle between the two inverter legs was set to 130°. The operating waveforms (Fig. 24*c*) reveal that the current through the isolation transformer is discontinuous. As a result, the VDR diodes are all operating under the full ZCS. Inverter switches in the leading leg (S_1 and S_2) feature ZCS turn on and near-ZCS combined with ZVS turn-off, which is supported by the magnetizing current of the isolation transformer. Switches in the lagging leg of the inverter are characterized by full ZVS operation, which is ensured by the proper selection of the dead-time duration.

Finally, the converter was tested in the boost mode with 25 V input and an operating power of 250 W (point *B* in Fig. 17). To step-up the input voltage, the shoot-through duty cycle was set to 0.18. The experimental waveforms show that in the boost mode (Fig. 25*e*) the inverter MOSFETs are hard switched, however, the VDR diodes feature ZCS.

Fig. 20 shows the experimentally obtained control variables of the proposed converter. It was confirmed that the converter is capable of ensuring the ripple-free 400 V output voltage within the six-fold input voltage variation (from 10 to 60 V). Moreover, the converter features almost ripple-free continuous input current within the entire range of the input voltage and load variations due to influence of the input wires inductance.

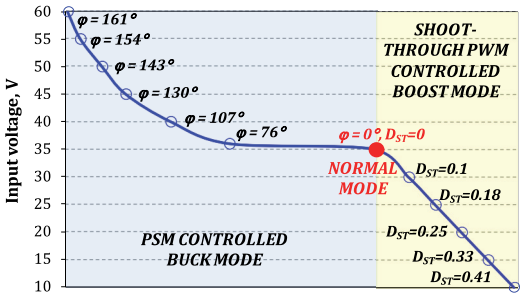

Fig. 20. Experimental control variables of the proposed converter.

Fig. 21 shows the efficiency curve of the experimental prototype, which was measured by the precision power analyzer Yokogawa WT1800. The efficiency curve incorporates all losses in the converter, including those of auxiliary power and the control system. As it was predicted, the peak efficiency (97.4 %) was achieved at the nominal input voltage when the converter operates in the normal mode and has the full soft-switching operation when near-ZCS and ZVS conditions are ensured. The efficiency drops to 87% in the boost mode when the converter operates at 100 W in the conditions of minimal input voltage and rated current ($V_{PV} = 10$ V, $I_{PV} = 10$ A). According to Fig. 20, the shoot-through duty cycle in this operating point has the maximum value of 0.41 and the converter demonstrates the maximum DC voltage gain of 40 ($G = V_{DC} / V_{PV}$ according to Fig. 1).

As it is seen from Fig. 17, the converter features maximum power in the voltage range from 25 to 34 V. Fig. 22 shows the efficiency curves as functions of the operating power acquired in the selected operating points within the maximum power range. The converter was also tested with the peak power of 300 W, which imposed no serious efficiency penalties. The peak efficiency obtained is within the target power range from 200 to 250 W.

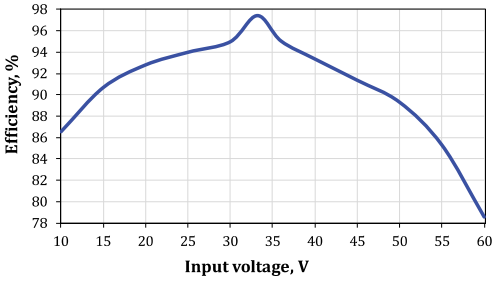

Fig. 21. Experimental efficiency of the proposed converter measured according to the power profile from Fig. 17.

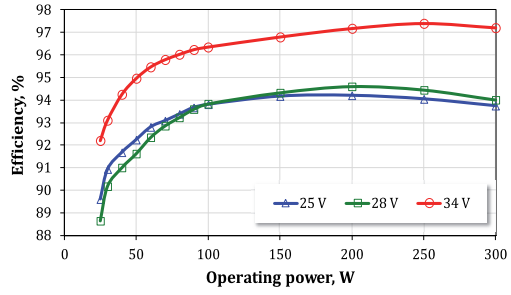

Fig. 22. Experimental efficiency of the proposed converter in the maximum power point range.

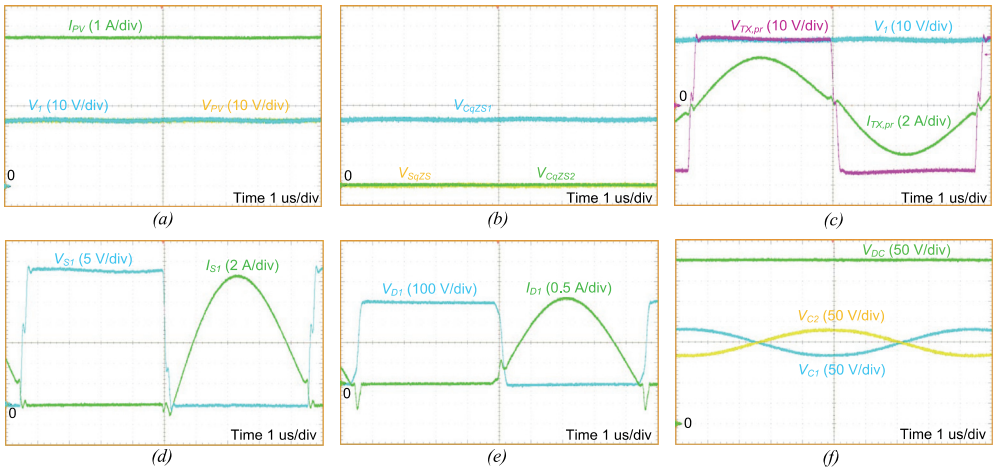

Fig. 23. Experimental waveforms of the qZSSRC in the normal mode at $V_{PV} = 34$ V and $P = 250$ W: input voltage, input current, and intermediate DC-link voltage (*a*), voltages of qZS capacitors and voltage of the switch S_{qZS} (*b*), intermediate DC-link voltage and isolation transformer primary winding voltage and current (*c*), voltage and current of switch S_1 (*d*), voltage and current of diode D_1 (*e*), voltages of VDR capacitors and output voltage of the converter (*f*).

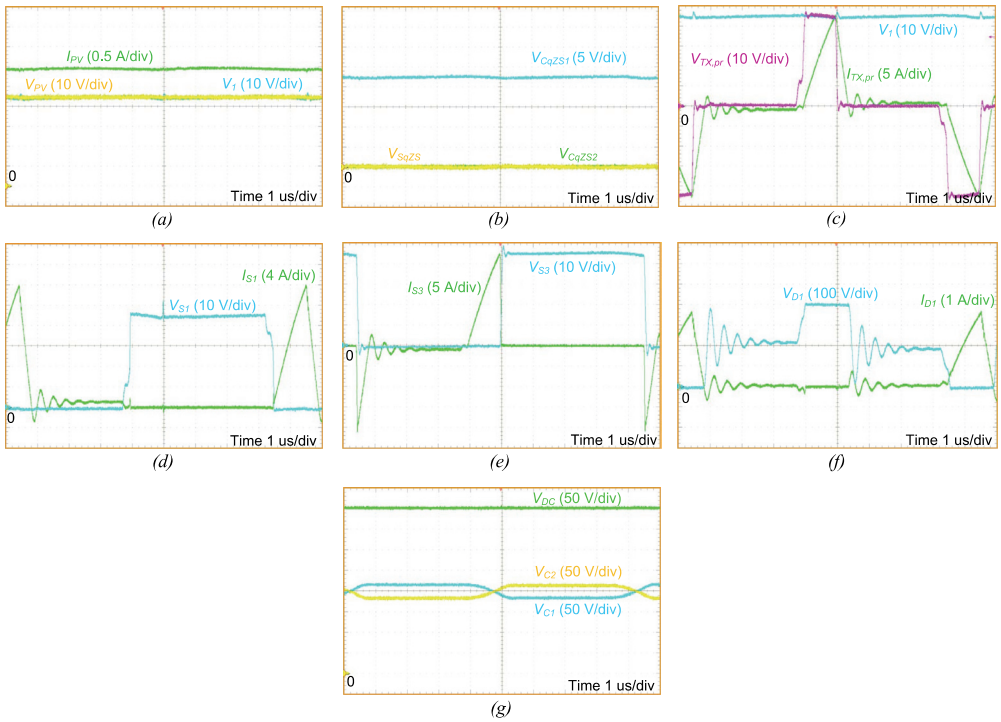

Fig. 24. Experimental waveforms of the qZSSRC in the buck mode at $V_{PV} = 45$ V, $P = 135$ W and $\varphi = 130°$: input voltage, input current, and intermediate DC-link voltage (*a*), voltages of qZS capacitors and voltage of the switch S_{qZS} (*b*), intermediate DC-link voltage and isolation transformer primary winding voltage and current (*c*), voltage and current of switch S_1 (*d*), voltage and current of switch S_3 (*e*), voltage and current of diode D_1 (*f*), voltages of VDR capacitors and output voltage of the converter (*g*).

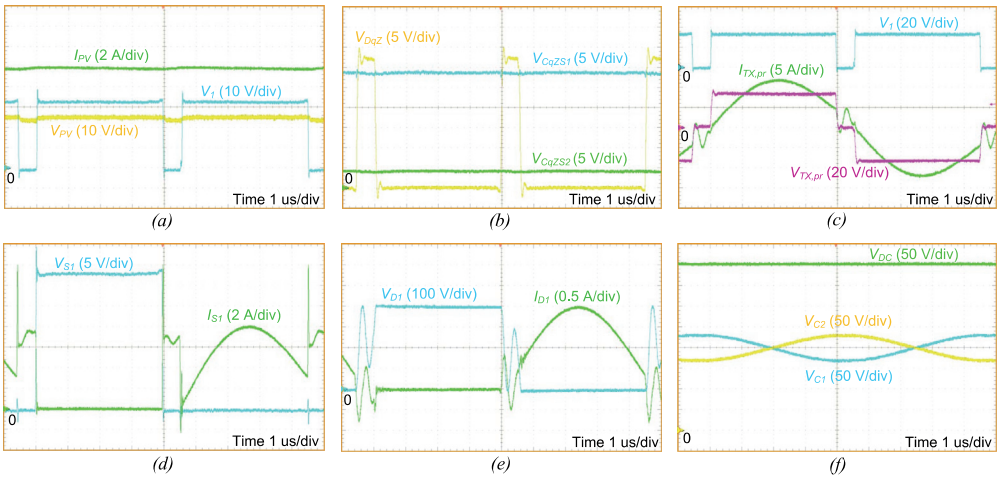

Fig. 25. Experimental waveforms of the qZSSRC in the boost mode at V_{PV} = 25 V, P = 250 W and D_S=0.18: input voltage, input current, and intermediate DC-link voltage (*a*), voltages of qZS capacitors and voltage of the switch S_{qZS} (*b*), intermediate DC-link voltage and isolation transformer primary winding voltage and current (*c*), voltage and current of switch S_1 (*d*), voltage and current of diode D_1 (*e*), voltages of VDR capacitors and output voltage of the converter (*f*).

As mentioned above, the proposed converter was specially designed for wide input voltage and load variations. According to the test profile presented in Fig. 17, the converter's operating power decreases gradually when the input voltage rises above 34 V. This operation range is mostly intended for the start-up of a PV module from the open circuit voltage. Moreover, even at the nominal operating voltage (V_{PV} = 34 V) and at the part-load conditions (P < 150 W), the converter turns from the normal to the buck mode, which results in a remarkable efficiency drop (red line in Fig. 22). Hence, modifications of the control algorithm should be adopted in order to improve the part- and light-load efficiency in the input voltage range from 34 to 60 V. Among numerous available techniques, the cycle or pulse skipping modulation is widely adopted in different applications, including PV systems [28]-[31]. The main idea is to force the converter into the idle mode when all switches are turned off, for several switching periods after one switching period of normal operation.

The experimental study was performed for two operating points: V_{PV} = 34 V and V_{PV} = 45 V. In the first case, the converter turns from the normal mode to the buck mode when the operating power decreases below 150 W. In the second case, the converter is in the buck mode at any operating power. Efficiency improvement resulted from the application of the cycle skipping modulation is shown in Fig. 26. In the figure, different modulations are designated as 1/Y, where Y is the number of skipped switching periods, when the converter is in the idle mode. It means that 1/0 corresponds to modulation without cycle skipping, while 1/5 corresponds to modulation that skips five switching periods after a single switching period of the operation. This results in decreased switching and magnetic losses at part- and light-load operation. However, at switching frequencies of around 100 kHz, skipping of more than five cycles is not recommended in order to avoid audible frequency range.

It is apparent from Fig. 26 that for each input voltage value, it is possible to draw an envelope over the efficiency curves with an efficiency variation of roughly 1% within the operating power variation range of 25 to 150 W. At V_{PV} = 34 V, points on the envelope correspond to the pure normal mode with skipping of one, two or three cycles depending on the instantaneous operating power, while other points employ PSM with a small phase shift angle. Operation in the normal mode at all power levels results in an efficiency improvement of up to 4%, while maintaining the output voltage of 400 V ± 1%. In the second case, the envelope of efficiency curves corresponds to PSM with skipping of two cycles in the range of the operating power of 75 to 150 W, while at the lower operating powers, the PSM with skipping of five cycles has to be adopted. This enables an efficiency improvement roughly by 10% at the minimum operating power.

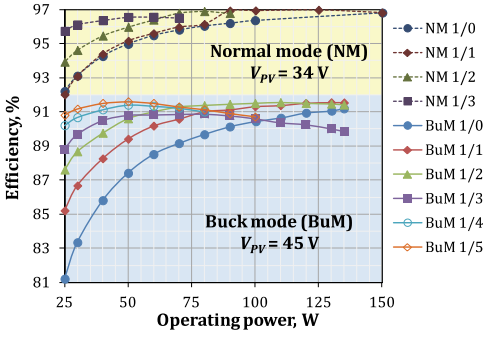

Fig. 26. Part- and light-load efficiency improvement of the proposed converter by the use of the cycle-skipping technique.

Part- and light-load efficiency improvement can be achieved over the entire operating range of the converter if the similar experimental study is performed for the rest of the operating points. It will result in a map of optimal number of skipped cycles for each possible operating point, which, in turn, will help to achieve a more flat efficiency curve of the converter.

VII. Conclusions

This paper has introduced a novel single-stage galvanically isolated high step-up DC-DC converter for the photovoltaic MLPE applications. Thanks to the multi-mode operation, the proposed quasi-Z-source series resonant DC-DC converter with synchronous quasi-Z-source network and series resonant tank integrated to the secondary part of the converter features a wide input voltage and load regulation range. Moreover, the proposed topology achieves high efficiency through the full-ZCS of the VDR diodes over the entire operating range, and depending on the operating mode, ZVS and/or ZCS of the primary side switches.

The multi-mode operation principle of the proposed converter was described along with steady-state waveforms and analysis of operating states. Next, selected design guidelines were presented for the integrated magnetic components and realization of the control system. To verify the theoretical assumptions, the experimental prototype was assembled and tested. It was confirmed that the proposed converter is capable of ensuring the ripple free 400 V output voltage within the six-fold variation of the input voltage (from 10 to 60 V). Moreover, it features the continuous input current over the entire voltage and load variation range without adding the buffering capacitors to its input terminals. The converter prototype based on the generic Si MOSFETs and SiC SBDs achieves the maximum efficiency of 97.4% in the nominal mode and at the rated power of 250 W. It was also shown how the part- and light-load efficiency of the proposed converter can be improved considerably by the use of the cycle skipping modulation technique.

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Single-Switch Galvanically Isolated Step-Up DC-DC Converter for Residential Photovoltaic Applications

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***Abstract*—In this paper the modified single-switch galvanically isolated quasi-Z-source DC-DC converter was proposed and evaluated as a candidate topology for the photovoltaic module-level power electronics applications. The operation principle of the converter was explained by the help of the steady-state analysis. For the verification of theoretical assumptions and evaluation of the performance of the proposed concept the 200 W experimental prototype of photovoltaic microconverter was assembled and tested.**

Keywords— DC/DC converter, quasi-Z-source converter, solar photovoltaic, module integrated converter (MIC)

I. INTRODUCTION

In last decade the concept of module integrated converter (MIC) has increasingly gaining its popularity in residential and small-commercial photovoltaic (PV) installations due to such important benefits as possibility of individual PV module oriented design, module-level maximum power point tracking (MPPT) and performance monitoring, simple installation and maintenance, etc. However, one of the important issues of the MIC approach is the complexity of the power circuit and, therefore, higher per watt costs as compared to those of the traditional string inverters.

Generally, the MIC is the self-powered DC-DC converter responsible for not only for the tracking the maximum power point but also for the stepping up the varying output voltage of the PV module to some certain stabilized DC voltage level. For example, the output voltage of MIC in European conditions should be around 400 V, which is essential for the grid-tied inverter to feed power to a single-phase AC grid. Therefore, the PV MICs could be characterized by the DC voltage gain ($G = V_{OUT} / V_{IN}$) over 15, which is the main difference between them and PV power optimizers, where the DC gain is typically limited by 10 [1]. To achieve the high DC gain values the PV MICs are traditionally based on the galvanically isolated DC-DC converters, where the high-frequency isolation transformer ensures the desired voltage elevation with high efficiency [2].

From big variety of the topologies recently developed for MIC applications the full-bridge (FB) DC-DC converters are dominant since they feature such important benefits as enhanced control flexibility, best possible transformer utilization factor and high power throughput. To further maximize the efficiency of the FB DC-DC converters for PV applications different approaches were proposed such as advanced zero-voltage and zero-current switching techniques [3]-[4], implementation of resonant switching with the maximum possible utilization of the parasitic elements of the circuit [5]-[6], topology morphing control [7], etc. As a result, the peak efficiency of the modern PV MICs based on the FB DC-DC converter topology has exceeded the 98% including the auxiliary power and control system losses [8].

The full-bridge MIC topologies are characterized by the presence of at least four controlled switches with associated driving peripherals, which add extra costs and complexity to the system. This issue has motivated the research in the field of MICs with reduced number of switches, which resulted in appearance of different topologies ranging from more complex current-fed half-bridge boost [9]-[10] and push-pull converters [11] to the single-ended ones such as flyback [12] or single-switch current-fed converters [13]. Moreover, the number of high-performance single-switch DC-DC converters was recently proposed for the renewable energy applications, from which the single-switch quasi-Z-source DC-DC converter (Fig. 1) could match the requirements of the low-cost PV MIC [14].

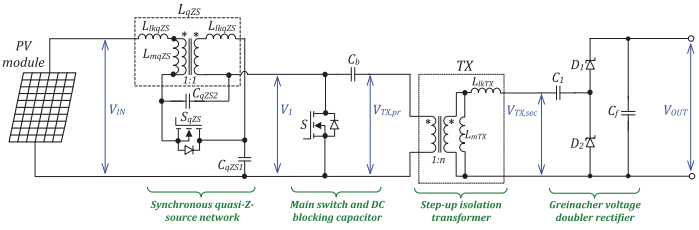

Fig. 1. Generalized circuit structure of the proposed single-switch galvanically isolated step-up DC-DC converter for photovoltaic applications.

The single-switch quasi-Z-source DC-DC converter (SSqZSC) was derived from the full-bridge quasi-Z-source DC-DC converter (FBqZSC [15]) by the simplification of the switching state, where the inverter bridge was replaced by a single switch. In contrast to the FBqZSC, which could operate either in a buck or in the boost mode, the SSqZSC can perform only the boost function of the input voltage. However, the SSqZSC requires only one control channel and a single transistor driving circuit, and features the continuous input current and a wide input voltage and load regulation range typical for the family of the galvanically isolated quasi-Z-source (qZS) converters [16].

In this paper the qZSSRC was first evaluated as a candidate topology for the PV module-level power electronics applications. To enhance the efficiency several modifications were introduced to the baseline topology of the SSqZSC proposed in [14]. For example, the concept of synchronous qZS-network was implemented to decrease the conduction losses in the primary side of the converter [17]-[18]. Moreover, the series resonant tank formed by the DC blocking capacitor C_b, capacitor of the voltage doubler rectifier C_1 and the leakage inductance of the isolation transformer *TX* was utilized to achieve the ZCS turn-off of the output diodes.

II. Operation Principle of the SSQZSC

As it is shown in Fig. 1 the primary (low-voltage) side of the proposed single-switch galvanically isolated step-up DC-DC converter consists of the main switch *S*, DC blocking capacitor C_b and qZS-network formed by the coupled inductor *L*, capacitors C_{qZS1} and C_{qZS2} and synchronous switch S_{qZS}. The secondary (high-voltage) side is based on the Greinacher voltage doubler rectifier (GVDR), where the capacitor C_1 is used as a part of the resonant tank and output filtering capacitor C_f is connected in parallel with the load. The low- and high-voltage sides are connected through the step-up isolation transformer *TX* with the turns ratio *n*.

The generalized operation principle of the SSqZSC with synchronous qZS-network is explained in Fig. 2. The output voltage is controlled by the duty cycle *D* of the main switch *S*. The switch S_{qZS} is synchronized with the main switch and, therefore, conducts current only during the OFF-state of the *S*. To prevent damage of the circuit, the dead-time is added before the turn-ON and turn-OFF transients of the S_{qZS}, as shown in Fig. 2. During the OFF-state of the *S* the qZS-network supplies the primary winding of the isolation transformer *TX* with unipolar voltage pulses with duration $T_{SW}\cdot(1\text{-}D)$. The blocking capacitor C_b is charged up to the voltage $V_{Cb} = V_{CqZS1}$, which results in the bipolar balanced voltage across the transformer primary winding. The average voltage values of the qZS capacitors could be calculated as follows:

$$V_{CqZS1} = \frac{V_{IN}\cdot(1-D)}{1-2\cdot D}, \quad (1)$$

$$V_{CqZS2} = \frac{V_{IN}\cdot D}{1-2\cdot D}, \quad (2)$$

where V_{IN} is the input voltage of the converter and *D* is the duty cycle of the main switch *S*.

According to Fig. 2 the switching period of the SSqZSC can be separated into four intervals:

[$t_0 < t < t_1$]: the main switch *S* is turned on, while the S_{qZS} is turned off and converter enters the operation state similar to the shoot-through state of the FBqZSC [15]. The switch *S* handles the double input current from the qZS-network as well as the current of the transformer.

[$t_1 < t < t_2$]: the main switch *S* is turned off and converter enters the dead-time. During the dead-time, the body diode of the synchronous switch is conducting therefore to maximize the efficiency of the converter the dead-time should be set as short as possible but long enough to avoid the short-circuit of the qZS capacitors. Usually, it is set in the range from 50 ns to 100 ns [17].

[$t_2 < t < t_3$]: the converter enters the active state, where the positive voltage is applied to the primary winding of the isolation transformer and energy is transferred to the output. The series combination of C_b, C_1 and L_{lkTX} start to resonate. The resonant inductor current I_{Lr} has enough time to drop to zero, which results in the ZCS turn-off of the diode D_2 at the time instant t_3. The synchronous switch S_{qZS} is conducting thus reducing the static losses in the primary side of the converter.

[$t_3 < t < t_4$]: the converter again enters the dead-time period, but its operation is totally similar to the previous time interval. The main difference is that the body diode of S_{qZS} takes over the current of the synchronous switch after it is turned off at the time instant t_3.

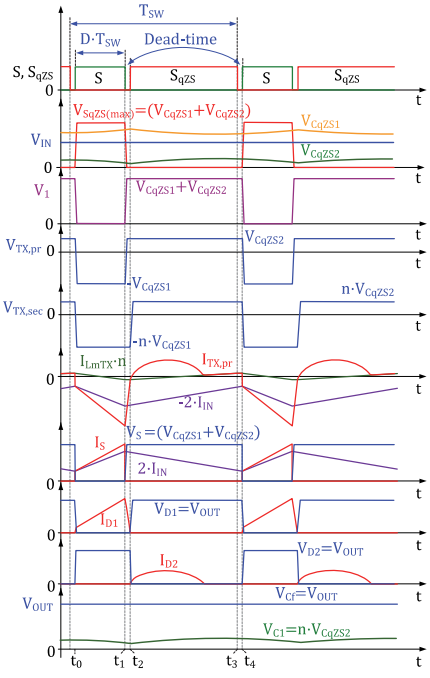

Fig. 2. Idealized steady-state current and voltage waveforms of the SSqZSC with synchronous qZS-network.

In the SSqZSC the isolation transformer operates with the bipolar voltage equal to that of the qZS inductor. The average voltage of the capacitor C_1 is proportional to the average voltage of the qZS C_{qZS2}, while the voltage stress of the C_f equals to the output voltage of the converter:

$$V_{C1} = n \cdot V_{CqZS2} = \frac{n \cdot V_{IN} \cdot D}{1-2 \cdot D}, \quad (3)$$

$$V_{Cf} = V_{OUT} = \frac{n \cdot V_{IN}}{1-2 \cdot D}, \quad (4)$$

where n is the turns ratio of the isolation transformer and V_{OUT} is the output voltage of the converter.

The normalized DC voltage gain of the SSqZSC could be calculated as follows:

$$G = \frac{V_{OUT}}{2 \cdot n \cdot V_{IN}} = \frac{1}{2 \cdot (1-2 \cdot D)}. \quad (5)$$

III. Determination of Duty Cycle Limit and Length of the Resonant Period

In the PV applications the maximum duty cycle will always correspond to the minimum input voltage of the converter, which is defined by the operating conditions of the PV module:

$$D_{\max} = \frac{1}{2} \cdot \left(1 - \frac{n \cdot V_{IN,\min}}{V_{OUT}}\right). \quad (6)$$

After the calculation of a maximum duty cycle the maximum duration of the resonant process within the operation state [$t_2 < t < t_3$] in Fig. 2 could be estimated as follows:

$$T_{res,\max} = T_{SW}\left(1 - D_{\max}\right). \quad (7)$$

The length of the resonant half-wave is defined by the parameters of the resonant tank and could be found by:

$$T_{res} = \pi \sqrt{\frac{L_{lkTX} C_b C_1}{C_b + n^2 C_1}}, \quad (8)$$

where C_1 is the capacitance value of the VDR capacitors, C_b is the capacitance value of the DC blocking capacitor, L_{lkTX} is the leakage inductance of the isolation transformer referred to the secondary and n is the turns ratio of the isolation transformer.

IV. Experimental Results

In order to verify the presented theoretical assumptions the experimental prototype of the PV MIC was assembled and tested. The converter was designed for the operation with the 60-cell polycrystalline silicon PV module Naps Saana 250 [19]. It features the peak power of less than 200 W at the normal operating cell temperature (NOCT = 45°C) and irradiance of 800 W/m^2. Therefore, the experimental prototype was designed for 200 W rated power. Tests of the prototype were performed according to the characteristics shown in Fig. 3, which correspond to the Saana 250 PV module operating at the temperature of 45°C and irradiance of 800 W/m^2. The generalized specifications of the prototype are presented in Table I. The Infineon BSC035N10NS5 MOSFETs with Analog Devices ADuM3223 drivers were used in the primary side for the main and synchronous switches. The GVDR was realized on the SiC Schottky diodes Wolfspeed C3D02060E. The control system of the converter was realized on the ST STM32F334 microcontroller, which is based on the Cortex-M4 core with a floating-point unit. The photograph of the experimental prototype is presented in Fig. 4.

Tests of the converter performance were performed in seven points shows in Fig. 3 in the MPPT range in the given case, where the point 7 corresponds to the maximum power point. Efficiency of the converter measured in this seven point is presented in Table II. Power consumption of the control system and driving circuits equal to 1.1 W were taken into account, since auxiliary power supply fed from the input voltage was implemented within the prototype.

TABLE I. Specifications of the Experimental Prototype

Parameter	Symbol	Value
Minimal input voltage, V	$V_{IN,min}$	20
Maximal input voltage, V	$V_{IN,max}$	40
MPPT range, V	V_{MPP}	31…37
Output voltage, V	V_{OUT}	400
Switching frequency, kHz	f_{sw}	60
Magnetizing inductance of qZS inductor, µH	L_{mqZS}	12
Leakage inductance of qZS inductor, µH	L_{lkqZS}	0.6
Turns ratio of qZS inductor	n_{qZS}	1
Magnetizing inductance of transformer, mH	L_{mTX}	1
Leakage inductance of transformer, µH	L_{lkTX}	9
Turns ratio of transformer	n	6
Capacitance of qZS capacitors, µF	C_{qZS1}, C_{qZS2}	22
Capacitance of DC blocking capacitor, µF	C_b	47
Capacitance of GVDR capacitors, µF	C_1, C_f	3

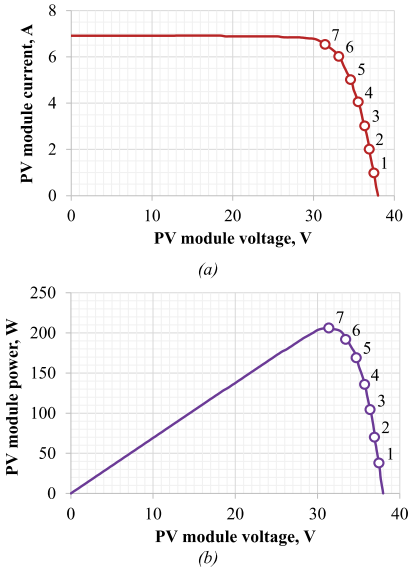

Fig. 3. Selected I-V (a) and P-V (b) characteristics of the PV module.

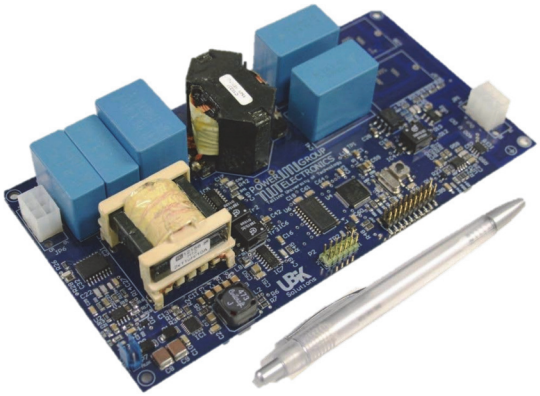

Fig. 4. The 200 W prototype of the PV MIC based on the SSqZSC topology.

TABLE II. VALUES OF THE MEASURED EFFICIENCY AND DUTY CYCLE

Operating points			Measured values	
Point nr.	***PV module voltage, V***	***PV module power, W***	***Duty cycle D***	***Efficiency, %***
1	37.2	37.2	0.196	92
2	36.2	72.4	0.208	94.8
3	35.2	105.6	0.22	95.3
4	34.2	136.8	0.231	95.3
5	33.2	167.5	0.242	95.2
6	32.2	193.2	0.253	95.1
7*	31.2	205	0.26	94.8

*Corresponds to the maximum power point

The key waveforms of the experimental prototype are presented in Fig. 5. The converter was tested in the operating point nr.7 with minimal input voltage. To step-up the input voltage to the desired 400 V at the output the duty cycle D was set to 0.26. It is seen from Fig. 5*a* that the proposed converter features the continuous input current with the 45% peak-to-peak ripple. The average voltages of the qZS capacitors C_{qZS1} and C_{qZS2} are 48 V and 17.8 V, which is in a good agreement with Eqs. (1) and (2). The main switch S is operating in the hard switching conditions (Fig. 5*b*); however, the output diodes feature the ZCS turn-off (Fig. 5*d* and *e*). The voltage stresses of the capacitors C_b, C_1 and C_f are 48 V, 102 V and 400 V, which conforms the validity of the steady-state analysis. The measured length of the resonant process (Fig. 5c) was around 9 μs, which corresponds to that obtained theoretically by the help of Eq. (8).

Values of the duty cycle measured experimentally (Table II) and calculated using Eq. (6) are shown in Fig. 6. The plotted curves are almost linear and lie close to each other. As a result of linear regulation characteristic, control of this PV MIC can be implemented using simple PI controller that is driven by error signal dependent on the reference value of the input voltage obtained from a MPPT algorithm. The MPPT algorithm based on the fixed-step incremental conductance method were utilized in this study. The low-cost Allegro ACS716 current sensor were used for the input current measurement, while measuring the input voltage with voltage divider and Microchip MCP6022 operating amplifier. The output voltage was sensed by the TI AMC1200B precision isolation amplifier to maintain the isolation barrier between the input and output sides. All analog signals obtained from the current and voltage sensors were converted into the digital form by help of the internal 10-bit ADC converter of the microcontroller.

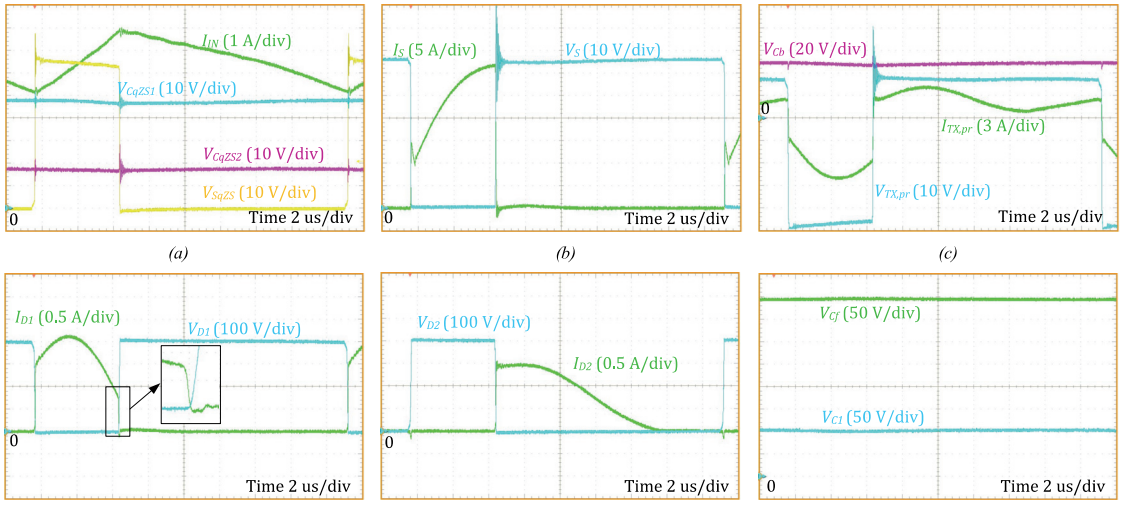

Fig. 5. Experimental waveforms of the proposed converter at V_{IN} = 31 V, P = 200 W, D=0.26 and V_{OUT} = 400 V: input current, voltages of qZS capacitors and voltage of the switch S_{qZS} *(a)*, voltage and current of main switch S *(b)*, voltage of DC blocking capacitor and isolation transformer primary winding voltage and current *(c)*, voltage and current of diode D_1 *(d)*, voltage and current of diode D_2 *(e)*, voltages of GVDR capacitors *(g)*.

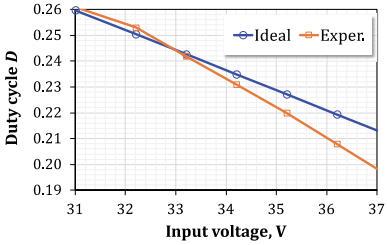

Fig. 6. Comparison of ideal and experimental regulation characteristics of the proposed converter.

Start-up test with MPPT was performed according to characteristics from Fig. 3 in order to verify the converter performance. A solar array simulation Agilent E4360A emulating the Saana 250 PV module in the given operating conditions was used to supply the prototype. The prototype was loaded by the programmable DC electronic load Chroma 63204 in constant voltage mode (400 V). As shown in Fig. 7 the prototype starts MPPT right after the module is connected to the input. Evidently, the MPPT frequency is 5 Hz, and converter reaches the maximum power point in five seconds. In this case, voltage step of the MPPT algorithm was increased intentionally to make the MPPT process more evident. The static MPPT efficiency measured is fairly high and equals to 99.5%.

V. Conclusons and Future Work

This paper introduces a novel single-switch galvanically isolated quasi-Z-source DC-DC converter. It was successfully evaluated as a PV module integrated converter. The converter possesses several advantages. First of all, ZCS turn-off of the voltage doubler rectifier diodes was achieved due to series resonance operation. Second, synchronous rectification allow to reduce conduction losses in the input side considerably at the cost of additional switch and driving circuit. Third, the converter features linear control characteristics and thus require simple control system. These modifications employed in the proposed topology enable peak operating efficiency of 95.3% taking into account auxiliary losses. Tests with real PV module I-V curve show high MPPT dynamic performance and static MPPT efficiency of 99.5%. Therefore, the converter proposed can be regarded as a low-cost high performance PV module integrated converter. Future work will be aimed to further efficiency improvement and comprehensive assessment of MPPT performance in a wide input voltage range.

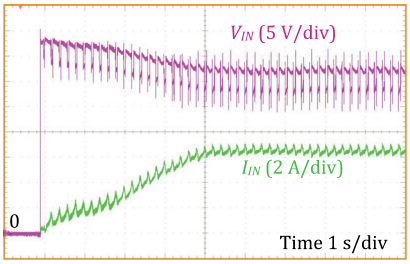

Fig. 7. Input voltage and current during startup and MPPT process.

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[PAPER-XI] A. Chub, O. Husev, D. Vinnikov, and A. Blinov, "Novel Galvanically Isolated Power Conditioning Unit for Micro Wind Turbine Applications," *submitted for consideration to IEEE Trans. Ind. Electron*.

Novel Galvanically Isolated Power Conditioning Unit for Micro Wind Turbine Applications

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Andrei Blinov, *Member, IEEE*, Dmitri Vinnikov, *Senior Member, IEEE*

***Abstract*—This paper presents a novel power conditioning unit (PCU) for micro wind turbine applications. It features simple generator side rectifier, galvanic isolation with simple DC-DC converter proposed, and single-phase full-bridge inverter at the grid side. Variable speed micro wind turbines based on permanent magnet synchronous generator (PMSG) are being increasingly often used in residential and small commercial buildings, despite their relatively low output voltage. Therefore, they can be used easily for battery charging, while their grid integration requires PCU with galvanic isolation. Most of available PCUs do not provide galvanic isolation, or use for that complicated topologies or four stage energy conversion. The proposed DC-DC converter utilized in this study allows reducing complexity of the PCU. Steady state analysis performed for the converter shows its capability to regulate voltage in a wide range that suits for micro wind turbines. The prototype build for integration of 1.3 kW PMSG based micro wind turbine shows good performance over the entire 1:5 range of the wind turbine output voltage. Detailed study of efficiency and power losses is performed according to the wind turbine power profile.**

***Index Terms*—micro wind turbine, isolated power conditioning unit, quasi-Z-source converter, single-switch converter**

I. INTRODUCTION

SMALL scale wind energy conversion systems have become a rising trend recently due to increased demand for green and secure electricity supply, especially in remote areas, which resulted in more than one million installed units all around the world [1]-[3]. Nowadays, more than 250 producers sell small Wind Turbines (WTs) that are usually limited to 100 kW power according to different national and international regulations [4],[5]. The small WTs with rated power up to 40 kW dominate in the market, however, the average power of a small WTs installed all around the globe is about 1 kW [4]-[6]. There are special feed-in tariffs introduced by many countries for small WTs that make micro WTs with rated power up to 3 kW an attractive solution for residential buildings and small communities in most of the countries [1], [7].

Despite their relatively high price, the multi-pole low-speed Permanent Magnet Synchronous Generators (PMSGs) are a dominant technology used in variable speed micro WTs due to small volume, high reliability and efficiency, self-excitation and brushless design [2], [8]-[10].

Usually, a small PMSG is directly driven by three- or multi-blade horizontal wind rotor with high torque in order to avoid mechanical parts (i.e. gearbox) that suffer from wearing. Residential micro WTs of sub-kW level can generate output voltage as low as several tens of volts, which also varies in a wide range due to variable speed operation [11]. This makes them suitable for battery charging, but they require galvanically isolated grid interface converter.

There are numerous concepts of power conditioning units for small WTs that are mostly oriented towards applications with rated power well above that of micro WTs. The latter is usually limited by standard household electric network: 11 kW for three-phase connection to 400 V distribution greed, and more commonly 5.75 kW for single-phase connection to 230 V distribution grid [7]. Generally, Power Conditioning Unit (PCU) for small PMSG based WTs is nonisolated and based on: back-to back converters [12]-[13]; combination of diode bridge rectifier and dc-dc converter at the generator side and traditional voltage source inverter at the grid side [14]-[16]; combination of the diode bridge rectifier and an impedance source inverter that includes functions of voltage regulation and thus avoids dc-dc converter [17]-[19]; etc.

Many works discuss proper selection of the generator side converter for PMSG based WTs. The most common solutions are diode bridge, its combination with the boost dc-dc converter, switched mode rectifier that utilizes phase inductance of the PMSG, semi-bridge rectifier and traditional two-level active rectifier composed of fully controlled power semiconductors [20]-[23], and other more complicated active rectifier topologies [24]-[26]. Advantages of active rectifiers fed by PMSG WTs were widely advertised, especially at high wind speeds, while combination of diode bridge rectifier and a dc-dc converter seems to be simple and attractive alternative with good tradeoff between cost and performance, since the PMSG does not require additional excitation [27]-[28]. In many residential WT installations, especially in urban areas, the average wind speed is rather low. In this conditions the annual energy yield could be increased by 1% only, when the active rectifier is used with kW level PMSG based WT instead of diode bridge rectifier with a dc-dc converter [29]. Therefore, it can be concluded that the latter is the preferable solutions in micro WT applications, also, due to easy implementation of galvanic isolation at the dc-dc stage.

Galvanic isolation is needed in micro WT applications to enable required high voltage step-up that cannot be performed by the boost converter due to practical limitations [30]. However, the topic of isolated PCUs for micro WTs is underrepresented in periodicals considering rapid rising of this market, while major efforts are made towards high performance control of existing non-isolated PCUs, which do not suit well for micro WTs. The galvanic isolation is a

favorable feature for residential wind energy conversion systems that increases their safety. There are few galvanically isolated PCUs proposed for small WTs:

- in [31] a diode bridge rectifier is followed by the full-bridge voltage source dc-dc converter that feeds two-level full-bridge grid side inverter;
- in [32] and [33] active rectifiers supply phase-modulated high-frequency isolated dual LCL dc-ac converter that shapes current, which is injected into the grid through unfolder;
- in [9] and [34] an active rectifier operates in tandem with quasi-Z-source full-bridge dc-dc converter to supply the grid side inverter with stable voltage;
- in [35] the WT microinverter performs isolated energy conversion in four stages in the following: diode bridge rectifier, non-isolated boost converter, galvanically isolated flyback converter the shape sinusoidal current, unfolder that injects current into the grid.

Evidently, existing solutions are either based on isolated full-bridge dc-dc converters that are an excessive solution for sub-kW power levels, or based on a single-ended converter that require four stages of energy conversion, which, in turn, will results in efficiency limitations. Clearly, there is a need for simpler approach that is better tailored for micro WTs. This work is dedicated to a novel galvanically isolated modular single-switch quasi-Z-Source (qZS) dc-dc converter intended for micro WT applications. Its utilization in PCU for micro WTs enables low cost of realization, three stages of energy conversion despite single-switch nature of a converter, simple control, and modular realization.

II. Power Conditioning Unit with Galvanic Isolation

The proposed PCU for micro WTs is shown in Fig. 1. Its structure is similar to the traditional PCUs based on diode bridge rectifier followed by the boost converter. However, in this PCU, a novel galvanically isolated dc-dc converter is utilized. Generally speaking, several standardized dc-dc converters can be connected in parallel in order to achieve required power level.

The inverter and diode bridges can be scaled for different power level using pin-to-pin compatibility of power devices (and modules) rated for different current and standard dimensions of heatsinks. At the same time, galvanically isolated dc-dc converters and grid side filters utilize custom magnetic components and thus have limited scalability. They could be designed for standardized power levels in order to reduce production costs with modular design. Typical variable speed PMSG based micro WTs feature wide output voltage reaching one to five voltage ratio [34], [36]. Therefore, standardized converter should be optimized for even wider input voltage range considering existing products available on the market. Power rating of such converters depends on the market demand, but power around 500-600 W seems to be advantageous, since it corresponds to the half of the average installed power and results in reasonable number of modules for micro WT rated up to few kW.

The single-switch dc-dc converter proposed is an enabling technology for residential wind energy conversion system, allowing simple design of the PCU and high energy yield. It is analyzed in details in the following section. The PCU proposed does not require any control of the generator side rectifier, while the grid-side inverter should inject power into the grid from the stabilized second dc-link, for example, by using the direct power control [2]. The braking chopper with resistor both rated for at least the same power as the given WT are required for safe operation of the PCU. However, it is not considered in this paper, since it can be purchased as a ready to use device produced for electric drives or similar applications. The intermediate galvanically isolated single-switch qZS dc-dc converter proposed can be controlled in the same way as conventional boost converter. For example, it can perform maximum power point tracking based on iterative search with the switch duty cycle as the direct reference. This is possible, since this converter features input resistance dependence on the switch duty cycle (idealized case) similar to that in the boost converter [37]:

$$R_{IN} = \frac{(1-2\cdot D_S)^2}{n^2}\cdot R_{LD}\,, \tag{1}$$

where R_{IN} is the equivalent input resistance, D_S is the switch duty cycle, n is the turns ratio of the coupled inductor, and R_{LD} is the equivalent load resistance. More insight on the dc-dc converter operation is provided in the next section. Further detailed experimental study of the converter with a WT will be performed.

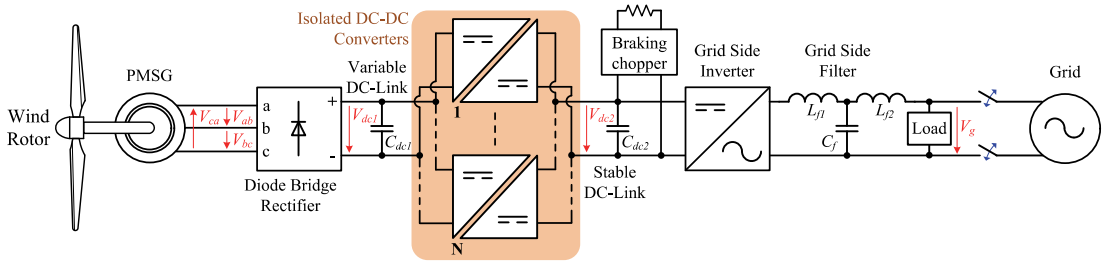


Fig. 1. Proposed variable speed PMSG based wind energy conversion system with three-stage PCU based on the isolated DC-DC converter(s).

III. Operation Principle of the Coupled-Inductor-Based DC-DC Converter

The galvanically isolated single-switch qZS converter proposed belongs to the class of a coupled-inductor based impedance-source converters, where inductor at the input side combine functions of energy storage and energy transfer from the input to the output side [38].

Fig. 2*a* illustrates investigated topology. It contains qZS network with a 3-winding coupled inductor (L_1, L_2, L_3), diode D_{qZ} and capacitors C_1, C_2, switch S_{qZ} and voltage doubler rectifier (VDR) with D_{r1} and D_{r2} along with dc-link capacitors C_3 and C_4.

At the same time, the Fig. 2*b* shows equivalent circuits of the coupled inductor where N_1 and N_2 are number of turns of the primary side and secondary side windings of the coupled inductor correspondently. In a very general case it is represented by means of magnetizing inductance L_M and ideal transformer. I combines two functions: store energy as a port of the qZS network, and transfers energy from the input to the output side.

In order to estimate the operation principle of the proposed topology the steady state analysis is performed. The Continuous Conduction Mode (CCM) of the input current of the dc-dc stage is assumed.

A. CCM steady state analysis

Fig. 3 shows the idealized operation waveforms. It shows the voltage and currents in the coupled inductor, and currents in the secondary side.

The operating period of the galvanically isolated single-switch qZS dc-dc converter in the CCM and in ideal case may be divided into two time intervals and can be represented by means of two equivalent circuits. First of all, there are several additional assumptions, which were taken into account. The conduction losses resistances R_L are shown on the primary side, since current on the primary side is larger. The location of magnetizing inductance L_M does not play any significant role. For more quality analysis the leakage inductance L_L is taken into account in this model. This leakage inductance prevents instantaneous switching on the secondary side between diodes D_{r1} and D_{r2}. As a result, this topology should be represented by means of four equivalent circuits that are shown in Fig. 4 that correspond the time diagram illustrated in the Fig. 3.

Fig. 4*a* shows the equivalent circuit of the shoot-through (ST) state. Transistor S_{qZ} and diode D_{r1} are conducting. It corresponds to the ST conduction mode.

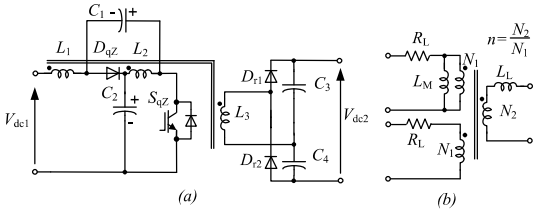


Fig. 2. Investigated topology of the single-switch isolated qZS based dc-dc converter (a) and equivalent circuit of coupled inductor (b).

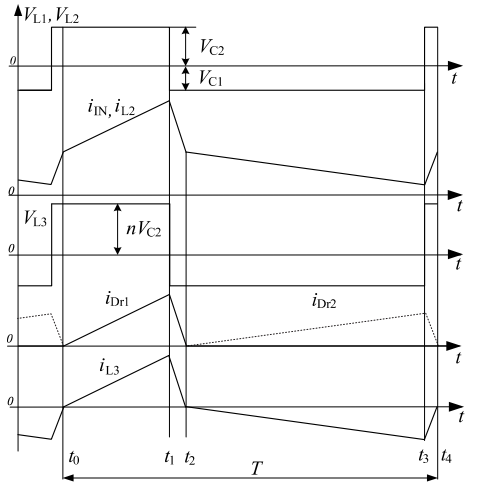


Fig. 3. Idealized waveforms of the proposed isolated single-switch dc-dc converter.

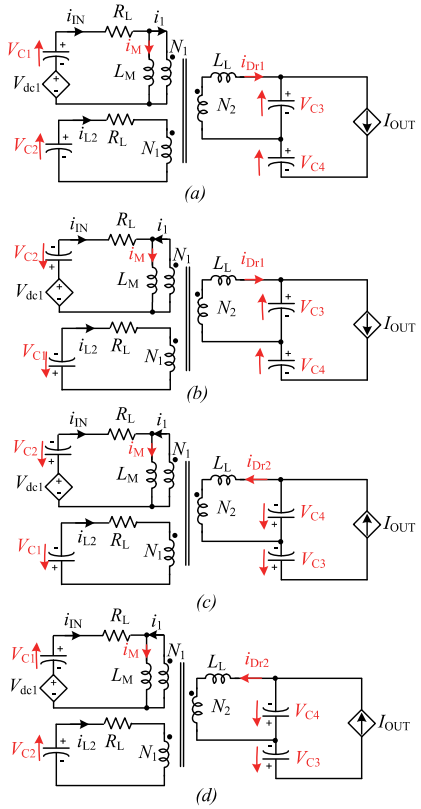


Fig. 4.Equivalent circuits of the single-switch qZS dc-dc converter.

This state can be described by means of differential equations:

$$\begin{cases} L_M \dfrac{di_M}{dt} = V_{C1} + V_{dc1} + C_1 \dfrac{dV_{C1}}{dt} R_L; \\ L_L \dfrac{di_{Dr1}}{dt} = n \cdot V_{C2} + n \cdot C_2 \dfrac{dV_{C2}}{dt} R_L - V_{C3}; \\ C_1 \dfrac{dV_{C1}}{dt} = -i_M - n \cdot i_{Dr1} - C_2 \dfrac{dV_{C2}}{dt}; \\ R_L C_2 \dfrac{dV_{C2}}{dt} = L_M \dfrac{di_M}{dt} - V_{C2}; \\ C_3 \dfrac{dV_{C3}}{dt} = i_{Dr1} - I_{OUT}; \\ C_4 \dfrac{dV_{C4}}{dt} = -I_{OUT} \end{cases} . \quad (2)$$

At the time instant t_1, the transistor S_{qZ} is turned off and diode D_{qZ} starts to conduct. At the same time, the diode on the secondary side continues conducting the leakage inductance current until it drops to zero. The equivalent circuit for this time interval (Fig. 4*b*) can be described with differential equations as follows:

$$\begin{cases} L_M \dfrac{di_M}{dt} = -V_{C2} + V_{dc1} - C_2 \dfrac{dV_{C2}}{dt} R_L; \\ L_L \dfrac{di_{Dr1}}{dt} = -n \cdot V_{C1} - n \cdot C_1 \dfrac{dV_{C1}}{dt} R_L - V_{C3}; \\ C_1 R_L \dfrac{dV_{C1}}{dt} = -L_M \dfrac{di_M}{dt} - V_{C1}; \\ C_2 \dfrac{dV_{C2}}{dt} = i_M + n \cdot i_{Dr1} - C_1 \dfrac{dV_{C1}}{dt}; \\ C_3 \dfrac{dV_{C3}}{dt} = i_{Dr1} - I_{OUT}; \\ C_4 \dfrac{dV_{C4}}{dt} = -I_{OUT} \end{cases} . \quad (3)$$

At the instant t_2 the diode D_{r2} starts to conduct as shown in Fig. 4*c*. Finally, at the instant t_3 the transistor S_{qZ} turns on again, while the secondary side voltages are lagging due to influence of the leakage inductance (Fig. 4*d*). Differential equations similar to Eqs. (2)-(3) can be derived for the equivalent circuits shown in Fig. 4*c* and *d*, but they are not shown for simplicity. In the ideal case, the leakage inductance converges to zero. As a result, the operation principle of the converter can be explained by means of the first (t_1-t_0) and the third (t_3-t_2) time intervals and their equivalent circuits. The capacitor voltages can be found from the volt-second balance of the coupled inductor windings over one switching period:

$$V_L = \frac{1}{T}\int_0^T v_L(t)dt = 0 . \quad (4)$$

Taking into account the conditions above, the voltages across the capacitors can be obtained as:

$$V_{C3} = \frac{n \cdot V_{dc1} \cdot (1 - D_S)}{(1 - 2 \cdot D_S)}, \quad (5)$$

$$V_{C4} = \frac{n \cdot V_{dc1} \cdot D_S}{(1 - 2 \cdot D_S)}, \quad (6)$$

where the D_S is the duty cycle of the ST state. It can be seen that the voltages across VDR capacitors are not symmetrical and depend on the operation point.

The final equation for the boost factor can be obtained:

$$B = V_{C4} = \frac{V_{C3} + V_{C4}}{V_{dc1}} = \frac{n}{(1 - 2 \cdot D_S)} . \quad (7)$$

B. Influence of the leakage inductance and conduction losses

It is evident that in the real experimental setup the output voltage depends on the leakage inductance L_L.

Neglecting conduction losses, the duration of time intervals that correspond to the VDR current drop to zero can be defined as:

$$\Delta t_{21} = t_2 - t_1 = \frac{I_{peak\_Dr1}}{V_{C3} + n \cdot V_{C1}} \cdot L_L , \quad (8)$$

$$\Delta t_{43} = t_4 - t_3 = \frac{I_{peak\_Dr2}}{V_{C4} + n \cdot V_{C2}} \cdot L_L , \quad (9)$$

where I_{peak_Dr1} and I_{peak_Dr2} are peak currents of the VDR diodes D_{r1} and D_{r2}, correspondently. The main conclusion from these equations is that these time intervals are proportional to the leakage inductance. Applying the voltage balance across inductors and taking into account all time intervals the boost characteristic can be found as a function of the leakage inductance L_L and winding resistance R_L. In particular, Fig. 5*a* shows dependence of the boost factor B as a function of the cumulative parasitic duty cycle D_P:

$$D_P = \frac{\Delta t_{21} + \Delta t_{43}}{T} , \quad (10)$$

which, in turn, is proportional to the leakage inductance.

Fig. 5*b* shows the boost factor B as a function of conduction losses (R_L). It can be seen that the increase of leakage inductance along with conduction losses will result in the decrease of the boost factor.

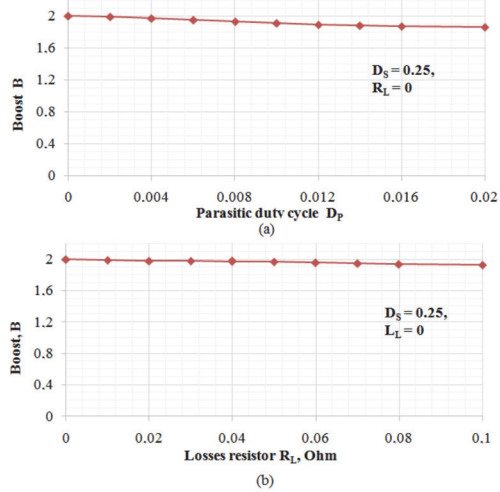


Fig. 5. The boost factor as a function of the D_P (a) and R_L (b).

IV. Experimental Results

The dc-dc converter prototype was build and tested using one to ten input voltage range to justify its performance. Then a PCU based on the dc-dc converter proposed was verified according to power profile of the case study WT.

A. Performance assessment of the prototype

The experimental prototype shown in Fig. 6 was built for rated power of 1.3 kW for a PMSG based micro WT that is described in the following subsection. It consists of two proposed galvanically isolated single-switch qZS dc-dc converters. The prototype can be fed either by dc voltage from separated input or from three-phase ac voltage through the embedded diode bridge rectifier. The first option was used to study performance of the isolated dc-dc stage. The prototype is capable to stabilize the output voltage at the level of 400 V, while the input voltage varies within the 1:10 voltage range from 40 V to 400 V. All tests in this subsection were performed at the 400 W power level due to limitation of the input current at the minimum input voltage. All semiconductor components utilized in the PCU are listed in Table II.

The switches in the prototype are controlled with interleaving and common duty cycle. They operate at 100 kHz, which results in the 200 kHz equivalent operating frequency of the prototype. This converter is a hard-switching converter and thus impose high demands on semiconductors, especially diodes, considering the switching frequency. Only SiC devices were utilized in the dc-dc converter stage due to their superior switching performance, low switching losses and gradually decreasing price [39], [40]. For example, the last (third) generation of 900 V SiC MOSFETs launched recently by CREE is a real competitor to Si devices due to considerable price reduction.

Results of the prototype efficiency measurement at the constant operating power of 400 W are shown in Fig. 7. The lowest efficiency corresponds to the extreme value of the boost factor, since the input voltage is stepped up by ten times. The prototype utilizes coupled inductors with unity turns ratio, while higher values should be used for voltages lower than 80 V. The duty cycle of the switches changes in the wide range nearly reaching the theoretical limit $D_S = 0.5$ (Fig. 8). The steady state voltage and current waveforms are shown in Fig. 9 for $V_{IN} = 80$ V. They are in good agreement with theoretical operating principle described above. Moreover, utilization of two converters within the prototype and their interleaved control result in reduction of the prototype input current ripple ($I_{IN(conv)}$) and, consequently, its frequency is twice the switching frequency. It can be concluded that due to its superior voltage regulation capabilities, simple topology and control the proposed galvanically isolated single-switch qZS dc-dc converter can be used as a power electronics building block for variable speed PMSG based micro WTs.

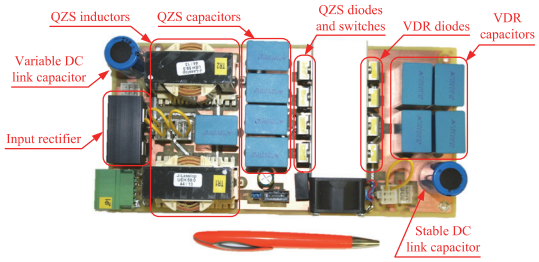


Fig. 6. Developed 1.3 kW prototype composed of two qZS converters.

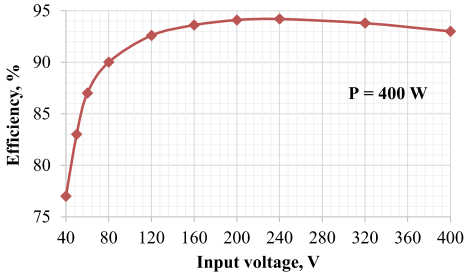


Fig. 7. Efficiency measured at the constant operating power.

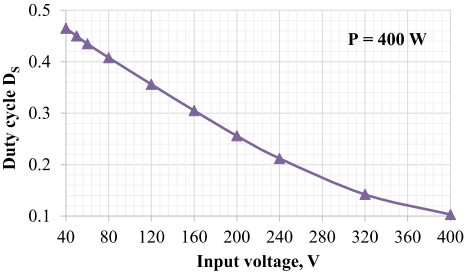


Fig. 8. Duty cycle of the switches at the constant operating power.

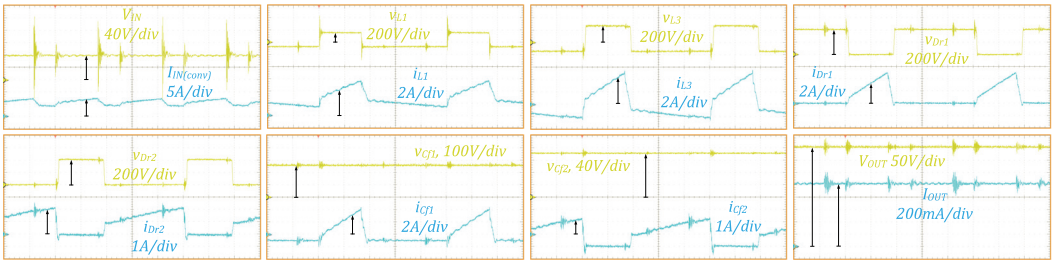


Fig. 9. Experimental voltage and current waveforms in time scale of 2 μs/div.

TABLE I
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value
Input voltage range, V_{IN}	*40…400 V*
Maximal input current, I_{IN}	*10 A*
Output voltage, V_{OUT}	*400 V*
Switching frequency, f_{SW}	*100 kHz*
Turns ratio of the qZS coupled inductors, n	*1:1:1*
Magnetizing inductance of the qZS coupled inductors, L_M	*1 mH*
Leakage inductance of the qZS inductors referred to the output side, L_L	*15 μH*
qZS and VDR capacitors, C_1…C_4	*3 μF*

B. Description of case study system

Further experimental study was performed using test-bench shown in Fig. 10. A PMSG designed for variable speed micro WTs were driven by induction motor. Speed control of induction motor was performed by means of ABB frequency converter from ACS 600 family. Parameters of the test-bench are listed in Table III. The dc-dc converter stabilizes the second dc-link voltage at 400 V that feeds the inverter. The two-level inverter used was implemented with a low frequency (50 Hz) leg based on low saturation voltage Si IGBTs with SiC antiparallel diodes, and a high frequency (50 kHz) leg based on SiC MOSFETs, as described in Table II. The generator-side rectifier was realized with two typical diode bridge rectifiers for lower cost, i.e. one leg was not used. The micro WT under study was designed for operation within the wind speed range from 3.5 m/s to 25 m/s and average wind speed of 5.5 m/s (Fig. 11). At wind speed of 12 m/s the WT reaches synchronous operation at the constant speed and constant power limited

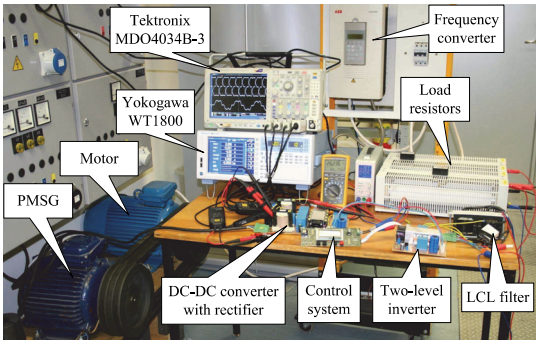


Fig. 10. Test-bench of a small wind energy conversion system.

TABLE II
SEMICONDUCTOR DEVICES USED IN PCU

Device	Type
Generator side rectifier	*Taiwan Semiconductor GBU606 (2 items)*
DC-DC converter, switches	*CREE C2M0160120D*
DC-DC converter, qZS diodes	*CREE C4D10120D*
DC-DC converter, VDR diodes	*CREE C4D10120D*
Inverter, low frequency leg switches	*Infineon IGW30N65L5*
Inverter, low frequency leg antiparallel diodes	*CREE C3D04060A*
Inverter, high frequency leg switches	*CREE C2M0160120D*

TABLE III
PARAMETERS OF TEST-BENCH EQUIPMENT

Parameter	Value
PMSG	
Number of phases	*3*
Number of poles	*8*
Phase inductance	*5 mH*
Phase resistance	*1.2 Ω*
DC link capacitors	
Variable DC link capacitance	*150 μF*
Stable DC link capacitance	*1000 μF*
LCL filter	
Inductor L_{f1}	*600 μH*
Capacitor C_f	*0.47 μF*
Inductor L_{f2}	*200 μH*

by pitch or stall control. Below this range WT does not operate, while it must be stopped above 25 m/s for safety reasons by short-circuiting PMSG windings. Obviously, converter has to operate in ultra-wide range of The PMSG voltage and power.

C. Operation of the PCU with the case study WT

The PCU implemented in the test-bench was studied using five operating point shown in Fig. 11. In the case of 5.5 m/s average wind speed, major annual energy yield correspond to variable wind turbine operation in the range of wind speed 6 m/s and 12 m/s [9]. Efficiency measurements for three electric energy conversion stages and total efficiency of the PCU are presented in Fig. 12. Apparently, the diode bridge has the highest efficiency, the inverter reaches 97% peak efficiency, and the dc-dc converter reaches almost 95% peak efficiency. Efficiency of the both inverter and dc-dc converter drops significantly at the operating point 1 due to high voltage

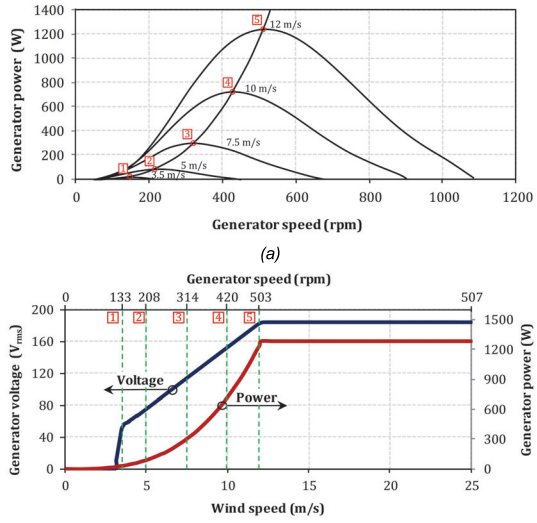


Fig. 11. Characteristics of the case study variable speed PMSG based WT: optimum torque curve (a) and dependence of the PMSG line-to-line voltage and output power on the wind speed.

step-up and low operating power. However, the PCU efficiency is higher than 80% in the range of maximum annual energy yield and reaches nearly 91% at the high PMSG powers, which is rather high considering three stage energy conversion and challenging operating conditions. Operation of the PMSG side rectifier and inverter are shown in Fig. 13*a* and *b*, correspondingly. The PMSG phase current corresponds to nature of the three-phase diode bridge rectifier, while the PMSG voltage is distorted due to high phase inductance. Using efficiency measurement results and measurements of voltage and current power losses in dc-dc converter semiconductor devices can be estimated.

D. Assessment of the dc-dc converter losses

Additional measurements were performed to estimate semiconductor power loss in the dc-dc converter. First, the duty cycle was measured experimentally in order to define the dc-dc converter control characteristic shown in Fig. 14. Then, the semiconductor power losses were measured in all five operating points. Semiconductor power losses are illustrated in details in Figs. 12-14. Evidently, the dc-dc converter demonstrates the highest losses at the fifth operating point at the maximum input power. In SiC MOSFETs the switching losses dominate over the conduction losses. SiC diodes feature relatively low power losses enabling operation at high switching frequency [41]. The power loss breakdown (Fig. 18) shows that semiconductors generate almost 65% of the total power losses, while another 35% is caused by the power dissipation in the qZS coupled inductors. This means that a common heatsink should be rated for dissipating of up to 50 W of power losses.

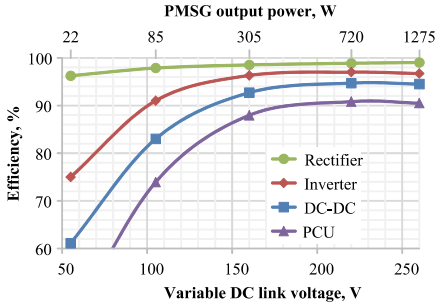
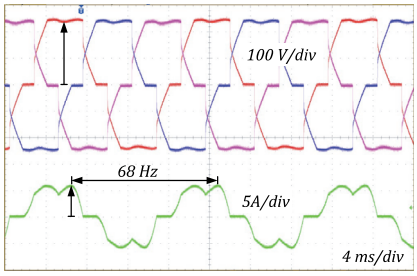
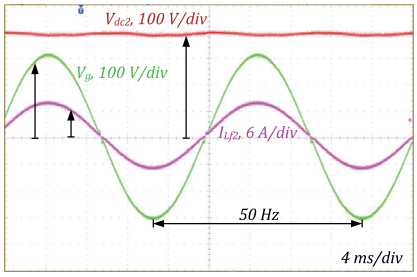


Fig. 12. Efficiency measurement of the PCU and its parts.



(a)



(b)

Fig. 13. Experimental voltage and current waveforms: generator output line-to-line voltages (top) and phase current (bottom) (a) and the stable DC link voltage (top) and inverter current and voltage (bottom) (b).

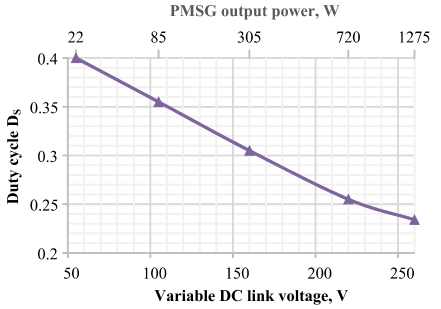


Fig. 14. Duty cycle of the DC-DC converter switches.

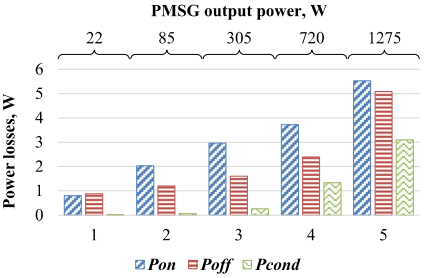


Fig. 15. Semiconductor power losses of a DC-DC converter switch: turn-on (*Pon*), turn-off (*Poff*), and conducting (*Pcond*).

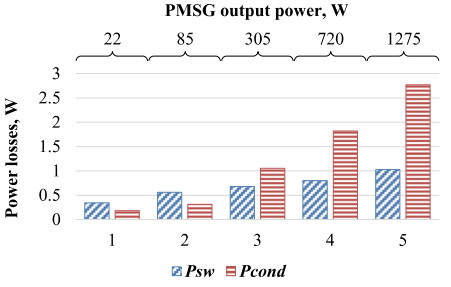


Fig. 16. Semiconductor power losses of a dc-dc converter qZS diode: switching (*Psw*) and conducting (*Pcond*).

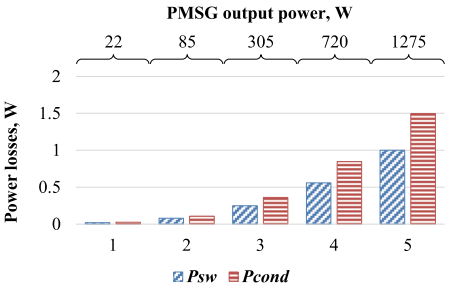


Fig. 17. Semiconductor power losses of a dc-dc converter VDR diode: switching (*Psw*) and conducting (*Pcond*).

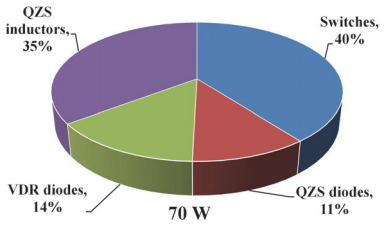


Fig. 18. Power loss breakdown on the dc-dc converter at maximum power (operating point 5).

V. Conclusions

This paper proposes a novel galvanically isolated power conditioning unit aimed for variable speed micro wind turbines based on the permanent magnet synchronous generator. This unit enables grid integration of sub-kW residential wind turbines into the distribution grid. Usually, reports on small scale wind energy conversions systems are dedicated to the enhanced control methods. However, performance of a power electronics converter used is often overlooked, especially proper analysis of the efficiency and losses according to operating profile of a corresponding wind turbine. The proposed approach does not require any changes of the conventional control systems. Therefore, this paper pays special attention to energy conversion performance by means of the efficiency and power losses.

The galvanically isolated power conditioning unit proposed in this paper is based on a novel modular quasi-Z-source dc-dc converter composed of typical single-switch power electronics modules. The design proposed can decrease manufacturing costs for power levels up to several kW. The 1.3 kW experimental prototype based on dc-dc converter composed of two modules was build for the case study wind turbine. It shows capability to cover the entire operating range of the corresponding wind turbine. It reaches almost 91% peak efficiency despite 1:5 voltage and more than 1:50 power variations, which usually complicates the design of the PCU for high efficiency. The approach proposed allows either reduction of number of energy conversion stages from four to three or avoiding complicated isolated topologies, like full-bridge. Experimental study of power losses was performed in order to estimate heatsink requirements. Losses in the switches and in the qZS coupled inductors are close to each other dominates over other losses in the prototype built. The experimental results obtained justify the power conditioning unit proposed for the given application. Future research will be directed towards study of reliability and packaging issues of the proposed concept.

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