THESIS ON POWER ENGINEERING,
ELECTRICAL ENGINEERING, MINING ENGINEERING D43

Research and Development of High-Power High-Voltage DC/DC Converters

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Declaration:
Hereby I declare that this doctoral thesis, my original investigation and achievement, submitted for the doctoral degree at Tallinn University of Technology has not been submitted for any academic degree.

Tanel Jalakas.....

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ENERGEETIKA. ELEKTROTEHNIKA. MÄENDUS D43

Võimsate kõrgepingeliste alalispingemuundurite uurimine ja välmimine

TANEL JALAKAS

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Contents

Introduction

Improvements in materials and semiconductor technology as well as in power electronics can make new generation of power electronics devices more compact, more reliable, cheaper and improve their efficiency. State of the art high voltage isolated gate bipolar transistors (HV IGBTs) have their blocking voltage up to 6.5 kV and current limit to 750 A. New high-voltage IGBTs enable simple two-level inverters to be implemented in high-voltage converter systems, instead of several series connected transistors or converter stages. New high-voltage semiconductor switches and topologies could be used in a wide variety of applications, like VAR compensators, transmission line converters, rolling stock traction converters and auxiliary power supply converters. The rolling stock is one of the most demanding power electronics applications. The requirements dictated by rough environment, safety and reliability are high.

Auxiliary power supply converters are one of the basic systems in rolling stock applications, interfacing the HV contact line with lower voltage secondary systems. The auxiliary power supply consists of several stages. The first stage converter is a step-down DC/DC front end converter (FEC) that lowers 3 kV DC catenary voltage to 350 V DC voltage. Next stages of auxiliary power supply are various DC/DC and DC/AC converters with input voltage 350 V DC. Those converters provide a wide range of output voltages for different on-board systems of a vehicle, like ventilation systems, compressors, lighting, control system, communication equipment and batteries (Figure 1). New auxiliary power supplies are not only needed for new vehicles but also for retrofitting of old ones.

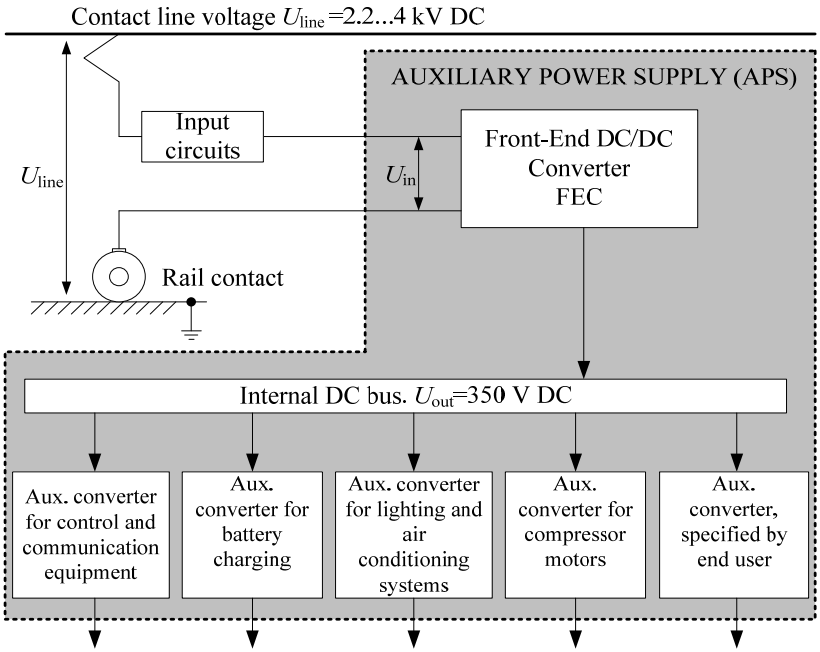

Figure 1 Auxiliary power supply

In cooperation between Tallinn University of Technology, Department of Electrical Drives and Power Electronics and Estonian company Estel Electro Ltd., 2006 a project "Power converters for onboard equipment of electrical transport", financed by Enterprise Estonia was launched. This doctoral thesis is based on the research, done during this project.

Field of interest of the current doctoral thesis is shown in Figure 2. The FEC of APS can be divided into the control and communication the and power electronics stage. The objectives of this thesis involve the research and analysis of various topologies, components, design issues and future research possibilities associated with the HV IGBT based FEC power electronics stage. The proposed DC/DC converter is based on HV 6.5 kV IGBTs and half-bridge inverter topology.

The control and communication stage of FEC along with research and development of control hardware and algorithms of the proposed converter are handled in detail in the doctoral thesis of PhD Indrek Roasto "Research and development of digital control system and algorithms for high power, high voltage isolated DC/DC converters".

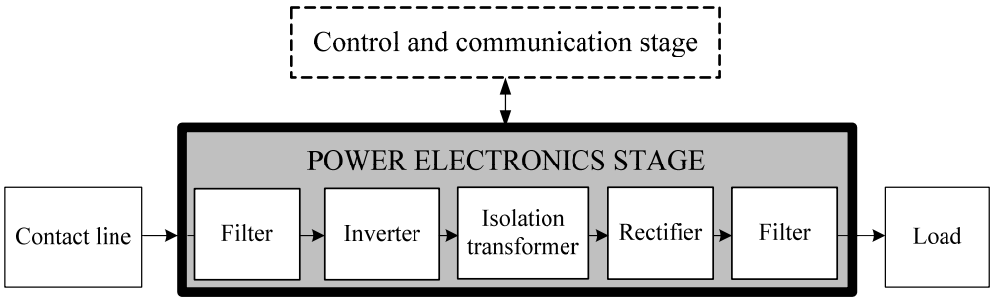

Figure 2 Field of interest of current doctoral thesis

Given research was financed by Enterprise Estonia supported contract "Power converters for onboard equipment of electrical transport", Tallinn University of Technology financial support (BF110) and two grants G7425 and G8020.

The main aim of the investigations is to transfer the modern know-how on this important field of engineering to Estonia and use that knowledge in research and study process of Tallinn University of Technology.

The General Hypothesis of the Research

The high-voltage insulated gate bipolar transistor (high-voltage IGBT) is a new promising power device for high-voltage high-power (> 20 kW) applications. Due to increased voltage blocking capability, the new high-voltage (> 2 kV) IGBT can serve as a good replacement for GTO and IGCT thyristors in medium or medium-to-high power applications. The implementation of high-voltage IGBTs can improve power density, integrity, controllability and reliability of power electronics converters for such demanding applications as rolling stock.

Thesis Objectives

The main objective of the thesis is to develop and validate topologies and design methods for high-voltage IGBT based power electronic converters.

General objectives of the thesis were:

1. analysis of user requirements and standards covering power electronic converters for high-demand applications i.e. rolling stock;
2. research and analysis of the recent state of the art technologies and development trends;
3. research and analysis of operating properties of high-voltage IGBTs;
4. comparative analysis of full- and half-bridge two-level voltage source inverters in high-voltage applications;
5. comparative analysis of two- and three-level voltage source inverters in high-voltage applications;
6. comparative analysis of topologies and components of energy efficient high-power rectifier;
7. comparative analysis of high-voltage transient protection methods;
8. research and development of high-voltage high-power (> 2 kV; > 20 kW) iron powder core isolation transformer;
9. research and development of EMI suppression methods on high voltage DC/DC converters;
10. research and development of thermal management issues of high-voltage IGBTs and rectifier diodes;
11. elaboration of design guidelines for product development;
12. elaboration of proposals for post-doctoral studies.

Scientific Novelty

The scientific novelties of the thesis are:

1. systematization of the state of the art converter topologies, materials and components used in rolling stock power electronics applications;
2. development and classification of performance requirements for power electronic converters used in rolling stock;
3. feasibility study of full- and half-bridge two-level voltage source inverters in high-voltage high-power (> 2 kV; > 20 kW) applications;
4. feasibility study of two- and three-level voltage source inverters in high-voltage high-power (> 20 kW) applications;
5. feasibility study of topologies and components of energy efficient high-power (> 20 kW) rectifier;
6. analysis of magnetic core saturation reasons of high-power (> 20 kW) iron powder core transformers and elaboration of saturation avoidance methods;
7. development of thermal models of high-voltage IGBT based converters;
8. development of EMI suppression methods in high-voltage IGBT based converters;
9. study of methods for efficiency improvement by use of soft switching features in the three-level neutral point clamped half-bridge inverter.

Practical Outputs

The practical outputs of the thesis are:

1. designed and developed high-power and high-voltage step-down DC/DC converter for traction applications based on two-level half-bridge topology;
2. designed and developed high-power and high-voltage step-down DC/DC converter for traction applications based on three-level neutral point clamped half-bridge inverter and current doubler rectifier;
3. simulation models of step-down DC/DC converters and components;
4. design guidelines for cooling systems of high-voltage IGBT based converters;
5. design guidelines for high-power (> 20 kW) iron powder core transformers;
6. design guidelines for high-voltage high-power (> 2 kV; > 20 kW) DC/DC converters;
7. two Estonian Utility Models (EE00824U1 and EE00687U1);
8. implementation of research results in the study process in Tallinn University of Technology.

Results of this work have been published in various international scientific conference proceedings (Estonia, Latvia, Lithuania, Poland, Germany, Slovenia, Slovakia, Portugal, Spain, Italy, Greece and England). 8 articles have been published in the international database of the Institute of Electrical and Electronics Engineers IEEE Xplore. 2 articles have been published in scientific journals. The developed power converter has also two Estonian Utility Model Certificates EE00824U1 and EE00687U1. In the course of the research and development cooperation between company Estel Elektro Ltd. and Tallinn University of Technology, Department of Electrical Drives and Power Electronics was established. Information exchange has also been conducted with companies Infineon and IXYS.

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Tallinn Tanel Jalakas
June 2010

Abbreviations

APLC – active power line conditioner
APS – auxiliary power supply
CCMLI – cascaded cell multilevel inverter
CDR – current doubler rectifier
DC/DC – direct current
DVR – dynamic voltage restorer
EMC – electromagnetic compatibility
EMI – electromagnetic interference
FB – full-bridge
FEC – front-end converter
FRED – fast recovery epitaxial diode
FWD – freewheeling diode
GDT – gas discharge tube
GTO – gate turn-off thyristor
HB – half-bridge
HP – high power
HV – high voltage
IGBT – isolated gate bipolar transistor
IGCT – integrated gate-commutated thyristor
MG – motor generator
MOS – metal oxide varistor
NPC – neutral point clamped
PWM – pulse-width modulation
SCR – silicon controlled rectifier
SELV – safety extra low voltage
TSPD – thyristor surge protection device
TVS – transient voltage suppressors
ZCS – zero current switching
ZVS – zero voltage switching

Symbols

A_C	isolation transformer core loss factor
B_m	isolation transformer operating flux density
C_B	capacitance of IGBT module T2
C_{res}	resonant capacitance of output rectifiers snubber
C_{sn}	frequency halving capacitance
C_{IGBT}	capacitance of IGBT module
C_O	output filter capacitance
C_{Tr}	isolation transformer primary windidng capacitance
D	duty cycle
d	distance between busbar conductor plates
d_{cond}	diameter of conductor
D_{max}	maximum duty cycle
D_{min}	minimum duty cycle
E_S	energy, stored in L_{TS}
f_{osc}	frequency of parasitic oscillations after IGBT turn-off
f_{sw}	switching frequency
I_C	IGBT collector current
$I_{Cav,FB}$	average IGBT collector current in FB inverter
$I_{Cav,HB}$	average IGBT collector current in HB inverter
I_{C1}	half-bridge capacitor C1 current
I_{C2}	half-bridge capacitor C2 current
I_{CT}	ringing effect current
$I_{C\ max\ 3l}$	maximum collector current of one inverter IGBT
I_{Co}	compensating current
$I_{C\text{-}on}$	IGBT collector current during turn-on
$I_{C\text{-}off}$	IGBT collector current during turn-off
$I_{Crms,FB}$	IGBT collector current RMS value in FB inverter
$I_{Crms,HB}$	IGBT collector current RMS value in HB inverter
$I_{C\ T1}$	top IGBT collector current
$I_{C\ T2}$	bottom IGBT collector current
$I_{C\ RMS\ max\ FB}$	maximum RMS value of collector current of IGBT of FB inverter
$I_{C\ RMS\ max\ HB}$	maximum RMS value of collector current of IGBT of HB inverter
$I_{F\ rd}$	output rectifier diode forward current
$I_{F\ rd\ av}$	average value of output rectifier diode forward current
$I_{F\ rd\ amp}$	amplitude value of output rectifier diode forward current
$I_{FW\ B}$	freewheeling diode current
I_{in}	converter input current
I_L	APLC load current
I_{Lo}	output inductor current
ΔI_{Lo}	output inductor current ripple
$I_{Lo\ rms}$	output inductor current RMS value
$I_{leak\ d}$	rectifier diode leakage current
I_{out}	FEC output current
I_S	APLC source current

I_{su}	surge current flowing through the varistors
$I_{Tr\ p}$	transformer primary current
$I_{Tr\ p\ amp}$	primary current amplitude value of isolation transformer
$I_{Tr\ s}$	transformer secondary current
I^*_{v}	varistor current
k_{add}	added losses factor
k_g	airgap coefficient
k_t	temperature coefficient of transformer winding resistance
k_U	window utilization factor
l	length of busbar conductor
L_{bus}	stray inductance of busbar system
L_c	internal inductance of DC-link capacitors
l_{cond}	length of conductor
L_{IGBT}	IGBT module internal inductance
L_M	main inductance of an isolation transformer
L_{mec}	stray inductance of contacts
L_O	inductance of output filter inductor
L_{res}	stray inductance of output rectifier
L_s	commutation loop stray inductance
L_{TS}	primary winding stray inductance of an isolation transformer
$L_{TS\ S}$	secondary winding stray inductance of an isolation transformer
m	number of the analyzed layer
N_p	primary turns number of an isolation transformer
N_s	secondary turns number of an isolation transformer
n_{tr}	number of IGBT modules in common heatsink
P_{CDR}	current-doubler rectifier total power loss
$P_{condIGBT}$	IGBT conduction power loss
P_{FBR}	full-bridge rectifier total power loss
P_{FWDC}	conduction power loss of integrated freewheeling diode
P_{FWDR}	reverse recovery power loss of integrated freewheeling diode
P_i	power loss in output filter inductor
P_{in}	input power of converter
$P_{leak\ diode}$	rectifier diode leakage power loss
$P_{loss\ FWD}$	power loss of the integrated freewheeling diode
$P_{loss\ IGBT}$	power loss of the one IGBT
$P_{loss\ inv}$	power loss of the input inverter
$P_{loss\ off\ diode}$	rectifier diode turn-off power loss
$P_{loss\ d\ module}$	rectifier diode module power loss
$P_{loss\ rectifier}$	output rectifier power loss
$P_{offIGBT}$	IGBT turn-off power loss
P_{onIGBT}	IGBT turn-on power loss
P	rated power of the FEC
$P_{rec\ rd}$	recovery power loss of the rectifier diode
P_{sn}	output rectifier snubber loss
P_t	isolation transformer rated power
P_{tr}	isolation transformer rated power
$Q_{rr\ rd}$	reverse recovery charge of the rectifier diode

Q_{rrFWD}	FWD reverse recovery charge
$R_{\text{AC,m}}$	AC resistance of the m-th layer
R_{C}	magnetic resistance of the core material of the isolation transformer
$R_{\text{DC,m}}$	DC resistance of m-th layer
$R_{\text{EKV DC}}$	isolation transformer equivalent load resistance
R_{LE}	equivalent load resistance
R_{LO}	output inductor active resistance
R_{m}	IGBT module lead resistance
R_{S}	active resistance of isolation transformer secondary winding
R_{sn}	output rectifier snubbers damping resistance
$R_{\text{tch d module}}$	thermal resistance between rectifier diode module case and heatsink
R_{tha}	thermal resistance between heatsink and surrounding environment
$R_{\text{tha rec}}$	thermal resistance between rectifier heatsink and environment
R_{thch}	common thermal resistance between IGBT module and heatsink
$R_{\text{tjc rdiode}}$	thermal resistance between rectifier diode junction and case
$R_{\text{thjc IGBT}}$	thermal resistance between IGBT semiconductor junction and case
$R_{\text{thjc FWD}}$	thermal resistance between FWD junction and transistor module case
$R_{\text{thjc diode}}$	thermal resistance between FWD junction and transistor module
S_{FB}	inverter switch stress for the FB topology
S_{HB}	inverter switch stress for the HB topology
S_{m}	cross-section of the magnetic core of the isolation transformer
t	time
$t_{\text{d max}}$	maximum dead-time
T^*	minimum time period between two voltage surges
T_{a}	ambient temperature
ΔT_{ch}	temperature rise between case and heatsink
t_{cond}	IGBT conduction time
t_{FW}	duration of freewheeling impulse
T_{h}	measured temperature of the heatsink
ΔT_{ha}	temperature rise between heatsink and surrounding environment
$\Delta T_{\text{jc IGBT}}$	temperature rise between the IGBT junction and module case
$\Delta T_{\text{jc FWD}}$	temperature rise between the FWD junction and module case
$T_{\text{j rd}}$	temperature of diode semiconductor junction
t_{off}	IGBT turn-off time
t_{on}	duration of inverter active cycle
t_{rr}	reverse recovery time
T_{sw}	duration of switching period
ΔT_{tr}	transformer temperature rise
t_{Uoff}	IGBT collector-emitter voltage rise time
U_{C1}	HB capacitor voltage
$U_{\text{CE max}}$	maximum collector-emitter voltage of IGBT in 2-level inverter
$U_{\text{CE\_max\_3l}}$	maximum collector-emitter voltage of IGBT in a three-level HB inverter
$U_{\text{CE-off}}$	IGBT collector-emitter voltage at turn-off
$U_{\text{CE-on}}$	IGBT collector-emitter voltage at turn-on
U_{change}	rapid line voltage change
U_{Co}	APLCcompensating voltage

U_{dip}	line voltage dip
U_{FB}	active switch utilization for the FB topology
U_{FIGBT}	forward voltage drop of IGBT
$U_{F\ RD}$	forward voltage drop of output rectifier diode
U_{HB}	active switch utilization for the HB topology
U_{in}	FEC input voltage
$U_{in\ var}$	line voltage variation
ΔU_L	line voltage disturbance
U_{line}	catenary line voltage
$U_{linemin1}$	lowest permanent line voltage
$U_{linemin2}$	lowest non permanent line voltage
$U_{linemax1}$	highest permanent line voltage
$U_{linemax2}$	highest non-permanent line voltage
$U_{linemax3}$	highest long term overvoltage
$U_{line\ n}$	nominal catenary line voltage
U_{LO}	output inductor voltage drop
$U_{n\ in}$	FEC nominal input voltage
$U_{n\ out}$	FEC nominal output voltage
U_{out}	FEC output voltage
$U_{out\ inv\ amp\ FB}$	amplitude value of FB inverter output voltage
$U_{out\ inv\ amp\ HB}$	amplitude value of HB inverter output voltage
$U_{out\ ripple}$	allowed maximum voltage ripple
$U_{ov\ lt}$	long term overvoltage
$U_{prI\ rms}$	primary winding RMS voltage at the fundamental frequency
U_{siov}	minimum protection voltage of input varistors
$U_{T1\ CE\ amp}$	top IGBT collector-emitter voltage
$U_{Tr\ p}$	primary voltage of an isolation transformer
$U_{Tr\ p\ amp}$	primary amplitude voltage of an isolation transformer
$U_{Tr\ p\ rms}$	primary RMS voltage of an isolation transformer
$U_{Tr\ s}$	secondary voltage of an isolation transformer
$U_{Tr\ s\ amp}$	secondary amplitude voltage of an isolation transformer
$U_{Tr\ s\ rms}$	RMS value of the transformer secondary voltage
$U_{T2\ CE\ amp}$	bottom IGBT collector-emitter voltage
V_M	minimum core volume of an isolation transformer
$V_{m,i}$	minimum required core volume of an output inductor
W	maximum energy in the varistor
Z_{HFE}	impedance of an isolation transformer at high frequency
Z_m	magnetic impedance of the core material of the isolation transformer
Z_p	impedance of the primary winding of the isolation transformer
Z_S	impedance of the secondary winding of the isolation transformer
α	heat irradiation coefficient
δ	depth of wire skin effect
μ	absolute magnetic permeability of the conducting material
η	efficiency of the inverter
ρ	resistivity
ω	angular frequency

1. Analysis of Performance Requirements

Auxiliary power supply (APS) is one of the basic systems used in rolling stock. It provides power to every electrical system and equipment on a railway vehicle, including those that are critical to its safety and operability.

APS cosists of several energy conversion stages. 2.2 kV DC to 4 kV DC from contact line is lowered to 350 V DC in the front end converter (FEC). The FEC supplies with 350 V DC lighting system, radio and communication equipment, compressor motors, ventilation and air conditioning systems, battery chargers, passenger information system power supply and control system power supply [2] (Figure 2). A failure within FEC would render the whole vehicle non-operational, resulting in a financial loss, operational problems to the railway and discomfort to passengers [1].
The suitability of any product depends to a substantial extent on the quality of the specification on which the product design is based. Prior to the development of any power electronic product for the rolling stock, all the major design requirements and specific considerations must be analyzed. Such FEC design requirements need to be divided to two distinct parts: factors related to the end-user and limitations concerning the specific area of use.

Factors which are becoming increasingly important to meet the aspirations of end-users are as follows:

- *low cost of ownership*: total life cycle costs mean that in addition to the initial price, maintenance and running costs must also be cut down. Failures and time for repairs must be minimized to provide the highest possible availability so that a given service can be provided with fewer vehicles [3].
- *Small overall dimensions*: space on the vehicle is scarce as more and more equipment has to be fitted to provide the onboard facilities of a modern railroad vehicle.
- *Low weight*: minimizing vehicle weight reduces the track wear and lowers propulsion costs.
- *Low noise level*: audible noise must be minimized to prevent annoyance to passengers. This applies to sound both inside and outside the vehicle.

It means that to meet the presented objectives, it is necessary to use the simplest circuits, consistent with achieving the required performance, thereby minimizing the cost and complexity. But another aspect is that technical and design issues crucial to the procurement of a reliable and maintainable product have to be considered and addressed within the main body by the reference to the main technical standards and specifications for the rolling stock. The main standard for power electronics for railway applications, EN50155, draws on requirements that are defined in other specifications and standards. Performance standards are defined for practically every facet of a railway's operational environment, including shock, vibration, extended temperature range, humidity, salt, fog, voltage fluctuations, electric safety and many more (Table 1). The standards are defined so that

electronics in rail cars will be able to operate 24 hours a day for 30 years, or approximately 250,000 hours [4]. These comprehensive performance requirements are needed because the failure of an electronic assembly in a passenger train could bring human lives to danger.

Table 1 List of European standards applied to railway power electronics applications

EN50155	The main standard for railway systems
EN 50163	Supply voltages for traction systems
EN 61287	Characteristics of power converters, installed on board of rolling stock
EN 61287	Electric safety
EN 60529	
EN 60077	
EN 50124	Isolation requirements
EN 50121	Electromagnetic interference
EN 55011	
IEC 60605	Reliability
EN 61373	Mechanical reliability (shock, vibration, temperature etc.)

Drawn from the standards and norms presented above, the main criteria that influence the design of the auxiliary power supply for the rolling stock may be determined:

1. compliance with supply voltage requirements;
2. compliance with a high variety of loads;
3. compliance with electric safety requirements;
4. compliance with physical requirements;
5. compliance with electromagnetic interference requirements.

1.1 Supply Voltage

Supply voltage requirements for FEC are defined by the standard EN 50163. This standard describes all variables of the supply voltage in the electric traction system. Supply voltage is defined by the few parameters, presented in Table 3. The supply voltage range given in EN50163 could be simply described by the parameters: nominal contact line voltage U_{line_n}, highest permanent line voltage $U_{linemax1}$, highest non permanent line voltage $U_{linemax2}$, lowest permanent voltage $U_{linemin1}$ and lowest non permanent voltage $U_{linemin2}$ in Table 2 [5].

Table 2 Nominal voltages and their permissible limits, given in EN 50163

Parameter	Value
Lowest non permanent voltage, $U_{linemin2}$ (kV DC)	2
Lowest permanent voltage, $U_{linemin1}$ (kV DC)	2
Nominal voltage, $U_{line\ n}$ (kV DC)	3
Highest permanent voltage, $U_{linemax1}$ (kV DC)	3.6
Highest non permanent voltage, $U_{linemax2}$ (kV DC)	3.9

Table 3 Definition of supply voltage parameters in traction system

No.	Parameter	Description
1	Linevoltage, U_{line}	Potential at vehicles current collector or elsewhere on the contact line measured between the contact line and the return circuit.
2	Nominal line voltage, U_{line_n}	Designated voltage value for electric traction system
3	Highest permanent line voltage, $U_{linemax1}$	Maximum value of the line voltage likely to be present indefinitely
4	Highest non permanent line voltage, $U_{linemax2}$	Maximum value of the line voltage likely to be present as highest non permanent voltage for a limited period of time.
5	Highest long term overvoltage, $U_{linemax3}$	Voltage defined as the highest value of long term overvoltage for duration over 20 ms (This value is independent of frequency).
6	Lowest permanent line voltage, $U_{linemin1}$	Minimum value of the line voltage likely to be present indefinitely
7	Lowest non permanent line voltage, $U_{linemin2}$	Minimum value of the line voltage likely to be present as the highest non permanent voltage for a limited period of time.
8	Long term overvoltage, U_{ov_lt}	Overvoltage higher than $U_{linemax2}$ lasting more than 20 ms.
9	Line voltage variation, U_{in_var}	Increase or decrease of line voltage normally due to variation of the total load of a distribution system or a part of it.

For the optimization of the FEC it is necessary to know the characteristics of the specific catenary supply system. The EN50163 standard requires that failure-free operation of electronics must be guaranteed with supply voltages between 70 and 120 percent of the nominal voltages defined in the specification (Table 2). Transient voltage fluctuations between 60 and 130 percent of nominal must not cause a fault [5]. The EN50163 standard states that continuous failure-free operation of the APS must be guaranteed within the limits of the supply voltage, which are presented in Figure 3. Power interruptions cannot cause any malfunction of the equipment. But the real situation is much more complex than it can be expected from the above definition. The first field questions are derived from its dynamic features, self-impedance, transients, noise, etc. Measurements of the catenary voltage waveform at the input of the auxiliary power supply device were performed. The railway supply systems across Estonia are according to the Soviet GOST standards that are

setting much harder design criteria to the power electronics devices designed for railway use.

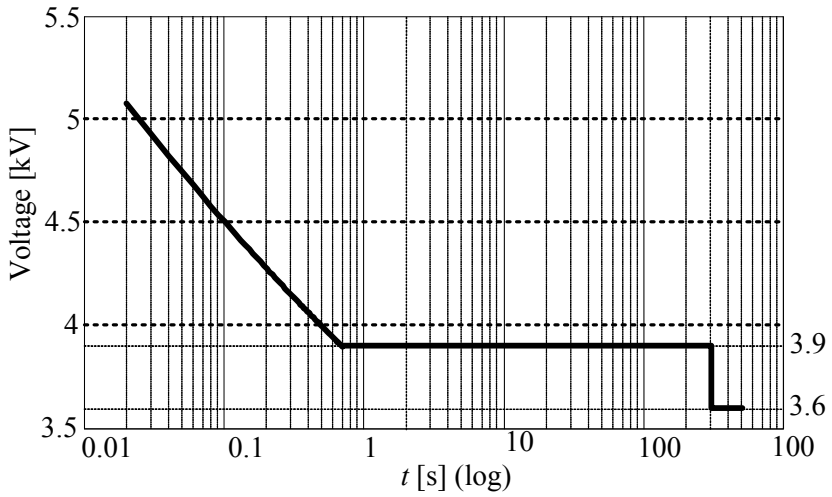


Figure 3 By EN50163 accepted 3 kV DC catenary overvoltages in logarithmic timescale

The Figure 4 represents the real voltage fluctuations in contact line of electric railway that were recorded in the Estonian electric railway line between the towns of Tallinn and Paldiski. The measured values in Figure 4 show that the catenary voltage does not comply to the EN standards. The supply voltage fluctuations exceed the limiting values. Due the long supply lines, the voltage drop can be quite high, especially in winter, when the train's heating systems are operating at full capacity.

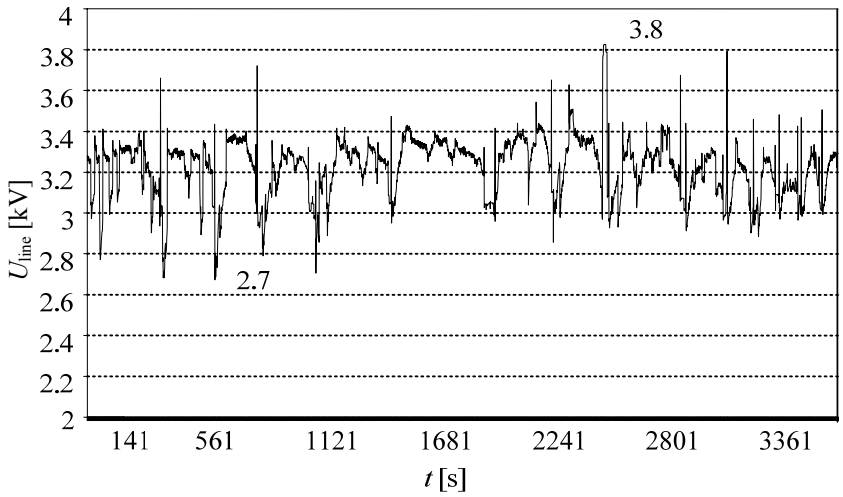


Figure 4 Measured contact line voltage profile

The measurements have shown that the catenary voltage changes between 2.7 kV DC and 3.8 kV DC (Figure 4). The long-term measurements have shown

that in some quite rare occasions the catenary voltage can change from 2.5 kV DC to 3.9 kV DC, exceeding standard maximal short-term catenary voltage limits. On the Figure 5 the appearance probabilities for different catenary supply voltages, in real traction conditions are presented. The Figure 5 also reveals that the line voltage is 3.3 kV DC with the highest probability of 34 %.

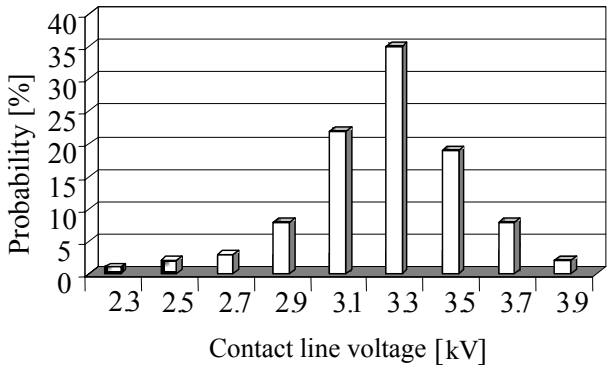


Figure 5 Histogram of the measured contact line fluctuations

Table 4 shows the standardized supply voltage fluctuations and the measured values.

Table 4 Measured supply voltage fluctuations

Standard	**Nominal voltage** U_{line_n} (kV DC)	**Lowest permanent voltage** $U_{linemin2}$ (kV DC)	**Highest non permanent voltage** $U_{linemax2}$ (kV DC)
Former USSR standard GOST	3	2.4	4
General European standard EN50163	3	2	3.9
Measurements	3.3	2.7	3.8
Combined design requirements	3.3	2.2	4

The FEC capable of operating in those conditions must have input voltage range from U_{in_min} = 2.2 kV to U_{in_max} = 4 kV DC, the measured nominal voltage of the supply line is 3.3 kV DC; over 300 volts higher than standards allow, therefore the nominal input voltage of the FEC must be U_{n_in} = 3.3 kV DC .

1.2 Dynamic Performance

The main objective of the APS and FEC is stable operation despite voltage fluctuations on the primary side and variation of loads on its secondary side. To

optimize the power characteristics of the developed FEC it is necessary to analyze its loads in different operational conditions. FEC has several types of loads: battery charging device, radio and communication equipment, lighting system, compressors, control system, ventilation and air conditioning system, passenger information system etc. (Figure 1).

Voltage fluctuations of the auxiliary low-voltage DC bus, such as may occur during the start-up of the auxiliary power supply apparatus, shall be limited to the range of –5 % and +5 % of the nominal FEC output voltage found in Table 5. These fluctuations will not exceed 0.1 s in duration. This means that the FEC needs a very short response time on variations of loads. Low-voltage DC power supply output overvoltages, such as may occur in the case of failure of the low-voltage power supply control systems, will be limited to 40 % above the nominal Auxiliary DC-bus voltage of the APS (specified in Table 5), and will not exceed one second in duration [2]. The requirements of the output power and output voltage quality are set by end-user requirements (Table 5 and Table 6).

Table 5 Allowed output voltage fluctuations of FEC

Parameter	Value
Nominal APS output voltage, U_{n_out} (V DC)	350.0
Minimal short-term voltage, U_{out_min} (V DC)	332.5
Maximal short-term voltage, U_{out_max} (V DC)	367.5

Table 6 Output parameters of FEC required by end-user

Parameter	Value
Rated power of the converter, P (kW)	50
Output current, I_{out} (A)	142
Maximum output voltage ripple, U_{out_ripple} (%)	5
Maximum output current ripple, I_{out_ripple} (%)	10

Load current of the auxiliary DC-bus could vary in a very wide range (up to 140 A) in different operation modes of a train. In an ideal case, the design of the FEC must be coordinated such that peak loads can be supplied by the FEC without reducing its output voltage below the minimum. Care must also be taken to ensure that the charging system will replenish the battery during normal operating runs of the vehicle.

1.3 Electric Safety

The main specific feature of the FEC for the railway rolling stock is that the input and output sides of the developed FEC need to be galvanically separated. The requirement for safety isolation depends on the integrity of the interconnections between the output of the power supply and the safety isolation provided by the load. Furthermore, it should be noted that voltages guaranteed to remain below 60 V DC are classed as safety extra low voltage (SELV) and precautions to protect the user are far less stringent. Reference should be made to the international

standard IEC 950 and European norms EN 60950 and EN 50155. But if the load has inherent safety isolation, then the need to introduce a further safety isolation barrier at the power supply in question is not required [2].

There are very different voltage levels on the primary side (up to 3.9 kV DC) and on the secondary side (350 V DC) of the FEC. Therefore, the input and output sides of the converter need to be galvanically isolated to meet the standards presented above. Usually to provide the necessary I/O galvanic separation power transformers are used. In view of all the requirements, a simplified block-diagram of a typical DC/DC auxiliary converter for rolling stock can be presented (Figure 6).

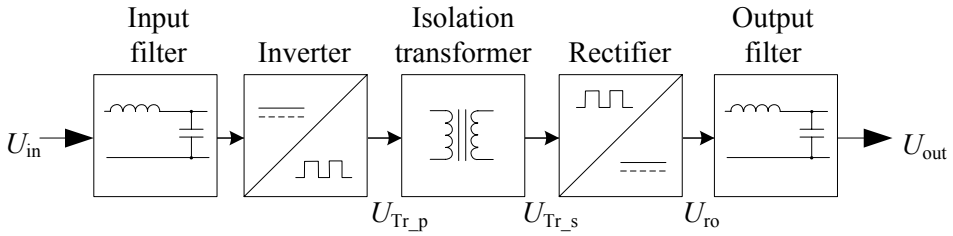


Figure 6 Simplified block diagram of a typical FEC for the 3 kV DC rolling stock

Since there is a need of the isolation transformer certain adjustments are to be made in the design of the power circuit of the FEC. As mentioned above, one of the criteria of a FEC is its compactness and low weight. However, it is a well known that the transformer is the main contributor in the size of any switching-mode power supply since it contributes about 25 to 30 % of the overall volume and more than 30 % of the overall weight [6]. In order to design small and compact electric power supplies, it is essential to reduce the size of the isolation transformer. The best way to achieve this is to employ high frequency excitation of transformer, although the used high-voltage semiconductors set limits to maximum switching frequency.

Another important issues of keeping the whole device electrically safe for operators are the isolation strength of the used materials and right construction of high voltage circuits. According to normative EN 50124 Annex D the minimum required insulation voltage for the system that has nominal voltage above 3 kV DC is 3.6 kV DC and according to normative EN 61287 Annex A the isolation of any part of high voltage circuit of the auxiliary power supply that has 3.6 kV DC rated insualtion voltage must withstand at least 15 kV DC voltage impulse (Table 7) [7]. The devices have overvoltage categories from OV1 to OV4. Because the FEC is connected to the overhead line through the additional surge arresting resistor and protected by metal oxide varistors, the FEC is rated to category OV2 (Table 8) [7].

Table 7 Rated impulse voltages for circuits powered by the contact line

Rated insulation voltage (kV DC)		**Rated impulse voltage (kV DC)**			
From ≥	Up to <	OV1	OV2	OV3	OV4
3	3.7	12	15	25	30
3.7	4.8	15	18	30	40

Table 8 Rated impulse voltages for circuits powered by the contact line

Category	Explanation
OV1	Circuits not connected to a power system Circuits being operated indoor (low voltage circuits)
OV2	Circuits not directly connected to the contact line and protected against overvoltages (power electronics circuits protected additionally by filter or inherently protected by components like varistors e.t.c)
OV3	Circuits directly connected to the contact line and not exposed to atmospheric overvoltages
OV4	Lines outside buildings protected only by inherent protection

All circuits that have voltage exceeding of SELV must be protected by device casing or safety barriers according to EN 60529 [8]. Also the vehicle and on-board devices grounding must be done according to normative EN 60077 [9] to ensure safety of servicing personnel and passengers in case of a faulty device.

1.4 Reliability

Reliability is one of the crucial aspects in the design of FEC. The failure of FEC can cause the failure of critical systems of rolling stock like brakes. The reliability requirements of FEC are mostly fulfilled by selecting proper components, topology and mechanical design. FEC must be able to operate for 24 hours daily for 30 years with minimum 250,000 hours of mean time between failures [10]. The reliability requirements are divided into two groups:

- electrical reliability;
- mechanical reliability.

1.4.1 Electrical Reliability

In service the components of FEC may endure short-term periods when the input voltages or output currents may exceed maximum allowed values. The mean time between failures and the overall reliability of the whole device is influenced by the ability of all components to continue normal functioning after the optimal working conditions are restored. Influence of overvoltages can be reduced by using protective devices (metal oxide varistors etc.), reasonably over-dimensioning switching devices and capacitors, using corresponding isolation materials in the isolation transformer.

Input voltage of FEC may vary from 2.2 kV DC to 4 kV DC (Table 4) and the maximum input voltage spike may be 6 kV DC and have duration of 20 μs. In normative EN 61287 [11] it is stated also that step change of line voltage within specified limits, light load operation, step change of load and short supply interruption may not harm the components of FEC and disturb the normal operation of the device. EN 61287 also states that the short circuit of output may not cause permanent damage to FEC.

1.4.2 Mechanical Reliability

Components used on rolling stock also must be qualified under the applicable mechanical standards. Moreover, they must be installed in such a way that ventilation is not obstructed and the mechanical mounting system must accommodate the shock and vibration inherent in rail cars. The overall internal temperature of FEC must not exceed the allowed highest temperature value of any component, used in the device. In addition to shock, the EN50155 main railway standard also defines vibration and temperature for a specific frequency range. Electronic assembly or component must be tested at resonant frequency (if present) for a period of 15 minutes and additionally at 50 Hz for two minutes in all three directions [4]. Also the rolling stock electrical equipment must withstand mechanical shocks, that are characterized by short duration and high acceleration. Typical shock and vibration values in real service are given in standard EN 61373 [12].

The EN50155 standard defines different classes of operating temperatures, but railway systems typically require the complete industrial temperature range of -40°C to +85°C [6]. To meet the temperature requirements of EN50155, tests are conducted for six hours at the highest temperature in the range and for two hours at the lowest point. Operation is also tested at points between either extreme. Humidity tests are similar to temperature tests. For example, electronics are subjected to 55°C at 95 to 100 % humidity for 10 hours. Following those tests, the functioning and insulation strength of electronics is tested again [4]. The shock, vibration, temperature and relative humidity limits, the FEC and its all internal components must withstand are listed in Table 9.

Table 9Limiting values for mechanical parameters according to EN50155

Parameter	Value
Vibration, (G)	1 at 10 Hz ... 150 Hz
Shock, (G/msec)	15
Outside temperature, (°C)	-40...+50
Inside temperature, (°C)	-40...+85
Temperature change rate , (°C/sec)	3
Relative humidity, (%)	≤ 75 % yearly average

When the end-user has specified a reliability level, the norm IEC 60605 may be used as a guide to monitor the performance of device and analyze the possible reliability and mintainability of rolling stock equipment.

1.5 EMC and EMI

With the increasing introduction of high-power electronic equipment, together with complex microcontrollers and a multitude of other electronic devices being installed on rail vehicles, electromagnetic compatibility (EMC) within the rail environment has become a critical issue in every aspect of the design and implementation of rail vehicle and rail-associated apparatus. This has subsequently led to the mandatory requirement that all new railway applications must be tested for compliance with

the European standard EN50121 [13]. The presented standard addresses some main aspects of the railway system that EMC concerns:

1. the effect of the railway system on the surrounding environment;
2. the effect of the railway system on signalling and communications equipment; and the ability of railway equipment and related apparatus to remain unaffected by the inherently severe environment within which it is intended to operate [14].

The electromagnetic interference (EMI) can reach from rolling stock apparatus to the surrounding systems through particular interfaces, called ports e.g. DC power port, earth port, signal and communication port shown in Figure 7 [15].

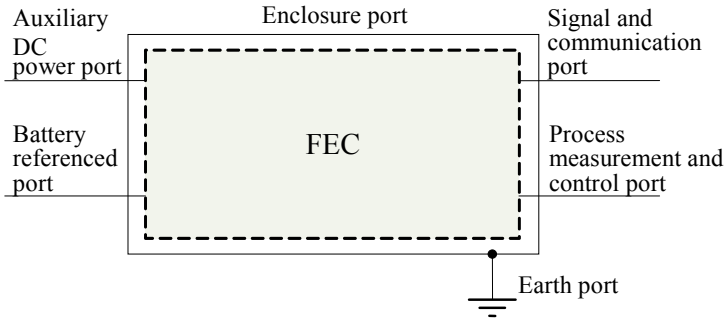


Figure 7 Main categories of electromagnetic interference ports

As the main focus of this thesis is on power circuit of FEC, the most important ports are auxiliary DC power port, earth port and device enclosure port. The limits of both conducted and radiated emissions of above mentioned ports are given in Table 10 and in Table 11 [15].

Table 10 Emission limits of auxiliary DC power ports according to EN 50121

Port	Basic standard	Frequency range	Limits
Auxiliary supply DC port	EN 50121	9 kHz to 150 kHz	No limits
		150 kHz to 500 kHz	99 dBμV quasi-peak
		500 kHz to 30 MHz	93 dBμV quasi-peak

Table 11 Emission of enclosure port according to EN 50121

Port	Basic standard	Frequency range	Limits
Auxiliary supply DC port	EN 55011	30 MHz to 230 MHz	40 dBμV quasi-peak (measured at 10m distance)
		230 MHz to 1 GHz	47 dBμV quasi-peak (measured at 10m distance)

Simple snubber circuits allow cost efficient solution of some serious EMI problems. But to completely minimize the overshoot and ringing effects it's necessary to pay

attention that the isolation transformer used in converter should be designed to reduce stray inductance to prevent some parasitic loops between it's secondary side and diode rectifier. Also the overall design of power stages must be kept as compact as possible, avoiding long wire loops with high parasitic inductance.

1.6 Generalizations

The end user requirements and the requirements from various normatives form the basic data to rely, when beginning to construct a FEC of APS for rolling stock. The normatives regulate safety and quality related aspects. End-user requirements specify the application field and several output parameters for FEC. Basic data about performance requirements of an FEC are submitted in Table 12. Those requirements set strict limits to construction, power circuit topology, materials and technical solutions to guarantee safe and reliable operation in demanding environment of rolling stock.

Table 12 Generalized performance requirements of FEC for rolling stock use

Parameter	Basic standard	Value
Input parameters		
Minimum input voltage of FEC,U_{in_min} (kV DC)	EN 50163	2.2
Nominal input voltage of FEC, U_{n_in} (kV DC)		3.3
Maximum input voltage of FEC, U_{in_max} (kV DC)		4
Output parameters		
Minimum output voltage, U_{out_min} (V)	Specified by end-user	332.5
Nominal output voltage, U_{n_out} (V)		350.0
Maximum output voltage, U_{out_max} (V)		367.5
Maximum output voltage ripple, (%)		5
Rated power of the converter, P (kW)		50
Output current, I_{out} (A)		142
Maximum output voltage ripple, U_{out_ripple} (%)		5
Maximum output current ripple, I_{out_ripple} (%)		10
Electric safety parameters		
Rated insulation voltage, (kV DC)	EN 50124	3.6
Rated impulse voltage, (kV DC)		15

Input voltage requirements for FEC are regulated by basic standard EN 50163. The input voltage of FEC may vary between 2.2 kV DC and 4 kV DC with nominal input voltage 3.3 kV DC. Output parameters are specified by the end-user. Required output voltage is 350 V DC with maximum allowable deviation from nominal value 5 %. Required ratedoutput power is 50 kW and the according output current is 142 A. EN 50124 sets requirements for rated isolation voltage and required impulse voltage (3.6 kV DC and 15 kV DC accordingly). The measurements of line voltage values in Estonian electric railway system have shown that catenary voltage can exceed 3.6 kV DC in long term. So the required rated isolation voltage would be even higher (4.6 kV DC). Parameters that define mechanical reliability are regulated by the normative EN 50155 (Table 13). FEC must be able to withstand shock 15 G/ms, vibration up to 1 G and temperature from -40 °C to 50 °C. EMI level is limited to 93 dBµV (Table 14).

Table 13 Limiting values for mechanical parameters

Limiting values for mechanical parameters		
Vibration, (G)	EN 50155	1 at 10 Hz ... 150 Hz
Shock, (G/msec)		15
Outside temperature, (°C)		-40...+50
Inside temperature, (°C)		-40...+85
Temperature change rate, (°C/sec)		3
Relative humidity, (%)		≤ 75 % yearly average

Table 14 EMC and EMI

EMC and EMI		
EMC emissions at frequency range 150 kHz to 500 kHz, (dBµV)	EN 50121	99 quasi-peak
EMC emissions at frequency range 500 kHz to 30 MHz, (dBµV)		93 dBµV quasi-peak

2. Analysis of State of the Art and Development Trends

2.1 Historical Survey

In terms of history, new materials, topologies, switching elements and control methods in power electronics mark the evolution. Figure 8 represents the classification of auxiliary power supplies used in rolling stock. The main focus is on the conversion technology and semiconductor switch type. First auxiliary power supplies used in rolling stock were motor-generators (rotary converters) (Figure 9). Because of their robustness and relatively simple construction, these devices are still widely used in electric trains.

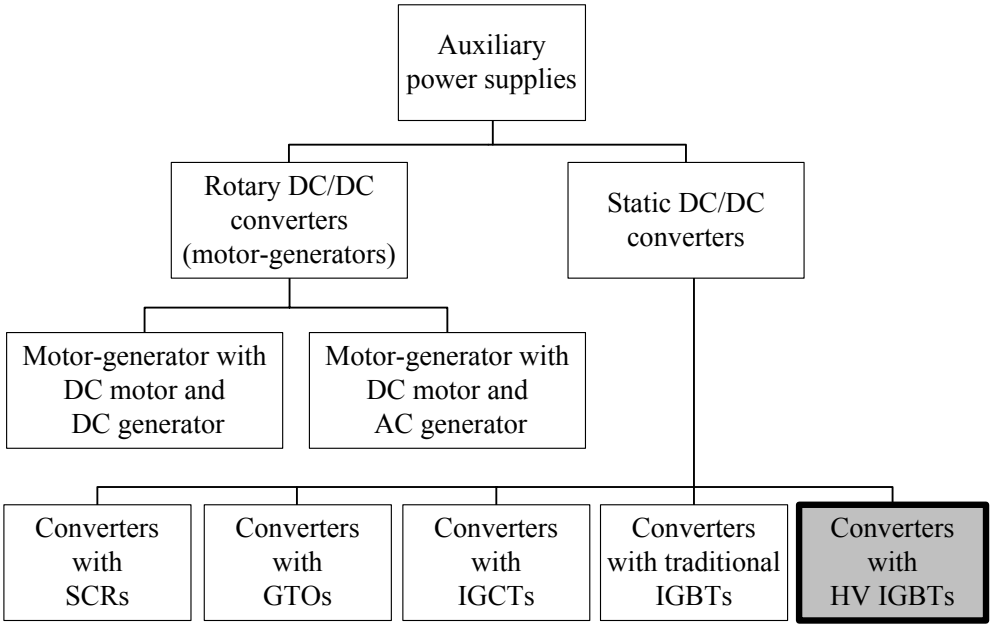


Figure 8 Classification of auxiliary power supplies

Early motor-generators included a DC motor and a DC generator, later the devices had a DC motor but an asynchronous AC generator with a semiconductor rectifier that ensured higher efficiency and reliability of those converters. Motor-generators ДК-604В are still in wide use in electric trains ЭР2, ЭР2Р, ЭР6 and also in other models throughout former Soviet countries. The first converters widely used for rolling stock that had no moving parts began to appear after a thyristor (SCR, Silicon Controlled Rectifier) was commercially introduced in 1957 by the General Electric (Figure 9). In year 1974 began the former Kalinin Plant (nowadays Estel Elektro Ltd.) in the Soviet Union launched the production of thyristor based converters for railway use [16].

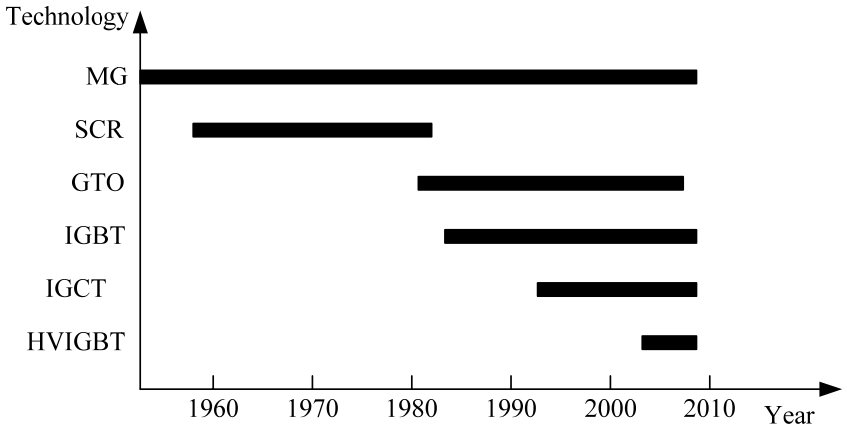


Figure 9 Historical use of different voltage conversion technologies in rolling stock

GTO (Gate Turn – Off thyristor) was the next advancement in power electronics. GTOs made it possible to use higher switching frequencies, new control methods made control and thyristor firing systems simpler. Next generation of thyristors were IGCTs (Integrated Gate-Commutated Thyristor), first released by ABB in 1993.

Insulated Gate Bipolar Transistors (IGBTs) were introduced in 1968 when Yamagami was granted the Japanese patent S47-21739. The theory was successfully proven in practice in 1979 when B. J. Baliga experimented with Vertical Channel Metal Oxide Semiconductor Gated Thyristors [17]. IGBTs introduced in the early 1980s had slow switching speed and limited voltage range. In 1983 an IGBT with increased switching frequency and blocking voltage that could be used in variety of power electronics devices was commercially introduced. German company Transtechnik Gmbh produced an experimental static converter in 1984 using IGBTs. Production of non latch-up type IGBTs with good capability of withstanding short-circuit was launched in 1985 by Toshiba company. In 2004 Estonian company Estel started manufacturing RTA37 auxiliary power supplies for rolling stock that used IGBTs as switching elements.

Around the year of 2000 the IGBTs with 4.5 kV and 6.5 kV blocking voltage were introduced to power electronics specialists [18] [19] but it was some years later that those IGBTs were available for engineers.

2.2 Topologies

In accordance with Figure 6, the FEC could be divided into two separate parts: inverter-stage and rectifier-stage. Specific norms for rolling stock cancel out many single switch transformerless DC/DC converter topologies (flyback, boost, Čuk, single-switch forward), leaving only the isolated DC/DC converter designs. The possible topologies for inverter-stage are shown in Figure 10.

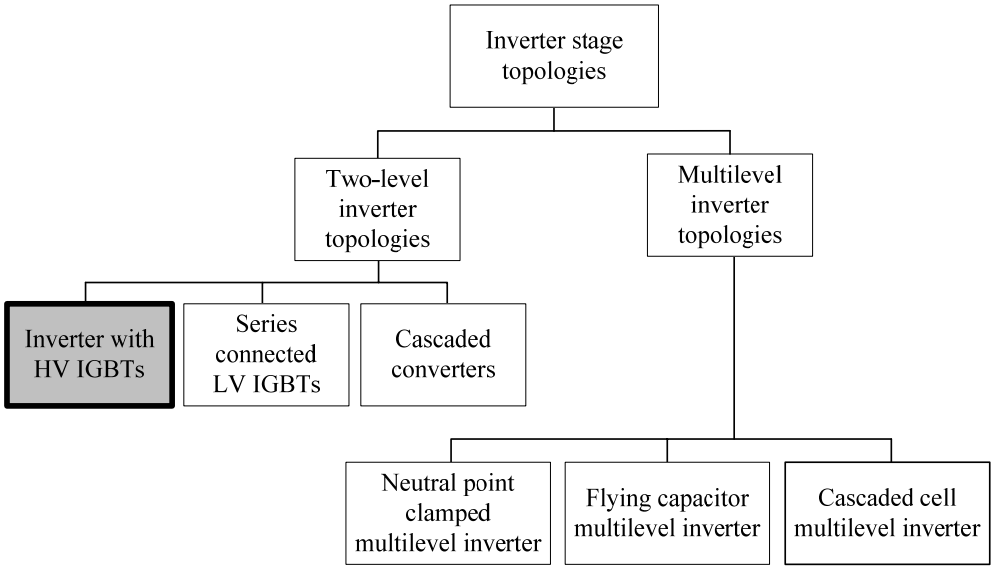


Figure 10 Classification of inverter stage topologies

The rectifier stage of front end converter of an APS could be realized using full-bridge, center-tapped or current doubler rectifier topologies (Figure 11).

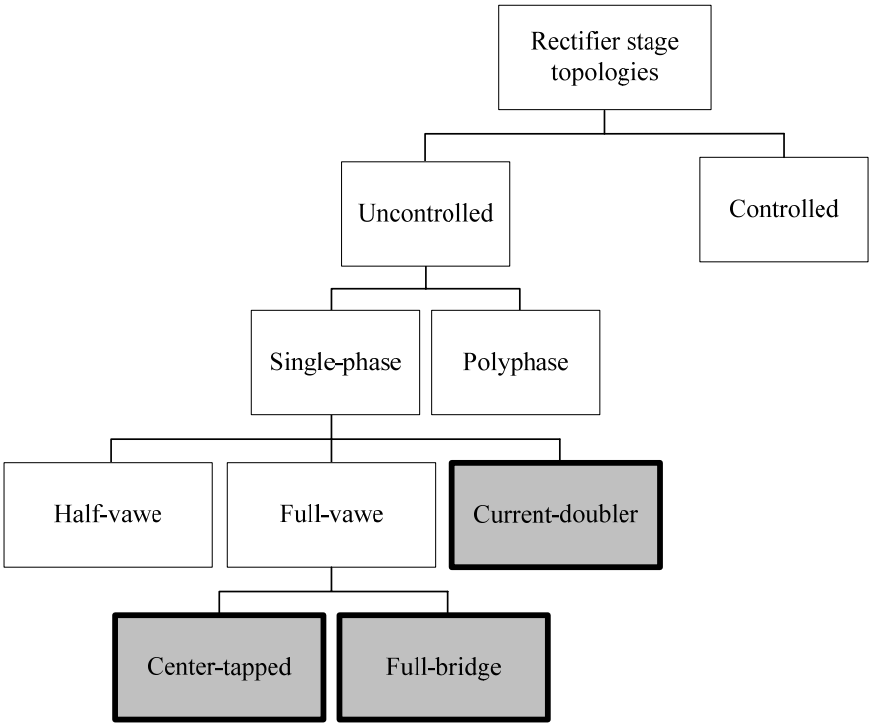


Figure 11 Classification of rectifier stage topologies

2.2.1 Two-Level Topologies with HV IGBTs

The simplest topologies for inverters are two-level topologies. It can be used two-level full-bridge or two-level half-bridge inverter topology (Figure 12).

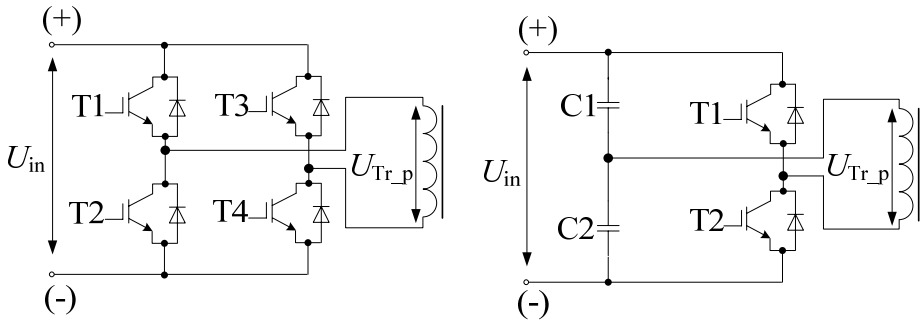


Figure 12 Two-level inverter topologies: full-bridge (a) and half-bridge (b)

Two-level inverters could be realized either with high voltage switching elements (6.5 kV IGBTs) or by using multiple switching elements in series configuration. The two-level half-bridge input inverter topology with 6.5 kV IGBTs has some significant advantages, like simple power stage design and simple control system; however, it has some serious disadvantages too. The main disadvantages of the two-level half-bridge design are: high switching losses of 6.5 kV IGBTs, low switching frequency and relatively high price of HV IGBTs.

2.2.2 Two-Level Topologies with Series Connected Switches

Connecting IGBTs in series allows fast high-power/high-voltage semiconductor switches with operating voltages of several kilovolts to be realized. Depending on the blocking voltage of transistors to be connected in series (1.2 kV, 1.7 kV, 3.3 kV or others), the total number of interconnected IGBTs varies from 6 to 2 [20] (Figure 13). The operating voltage across the whole series circuit is higher than the real voltage blocking capability of each single IGBT and must be shared between them. Due to unequal and variable IGBT-parameters (i.e. collector-emitter capacitance, leakage current, switching delays and storage times) and with real gate drive circuits for each single element (with unmatched delay times and supply voltages), voltage sharing of the whole switch is not balanced across all the elements. The transient (during turn-on and turn-off) and static (in off-state) divergent collector-emitter voltages introduce a risk of element destruction due to voltage and power dissipation stress [21], [22], [23], [24], [25]. All this leads to auxiliary voltage-balancing circuits to be implemented on the high-voltage primary inverter, increasing the complexity and decreasing the overall reliability of the designed system.

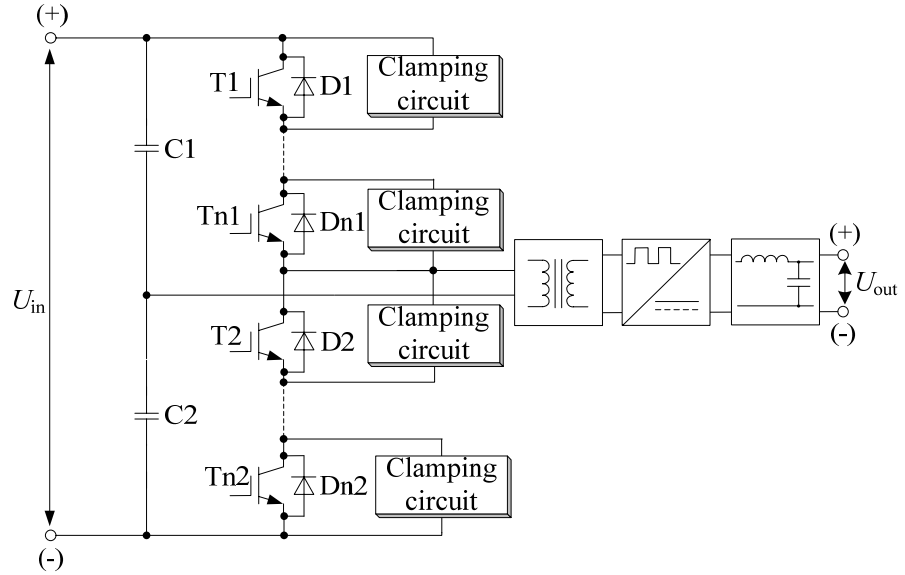


Figure 13 Two-level converter with series connected IGBTs

2.2.3 Multilevel Topologies

To overcome the problems related to two-level inverter topologies the multilevel (levels n>2) inverter topology can be implemented [21], [22]. For instance, the three-level topology fixes some problems, like high voltage spikes and high switching losses, but the system is more complex, as there are complimentary components added to the system [26]. There are two general topologies for a three-level inverter:

1. neutral point clamped multilevel inverter (NPC) (Figure 14, b);
2. cascaded cell multi-level inverter CCMLI [27] (Figure 15);
3. flying capacitor multilevel converter (Figure 14, a).

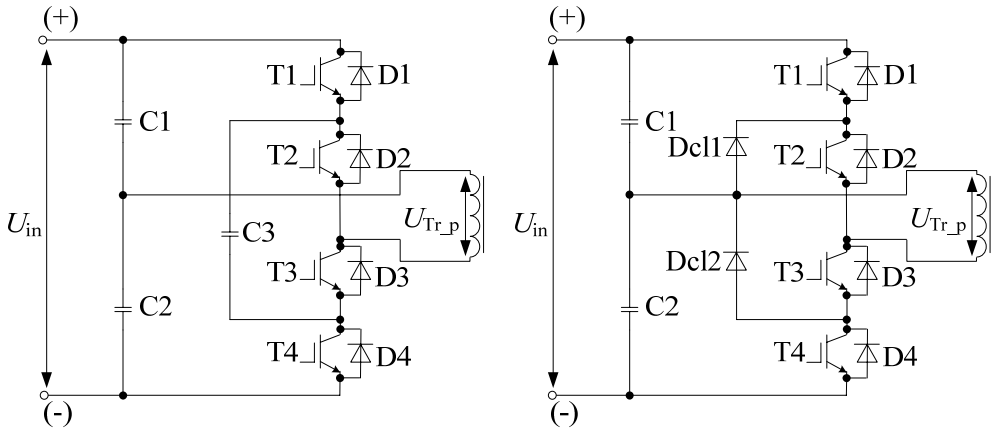


Figure 14 Flying capacitor (a) and neutral point diode clamped (b) three-level half-bridge inverter topologies

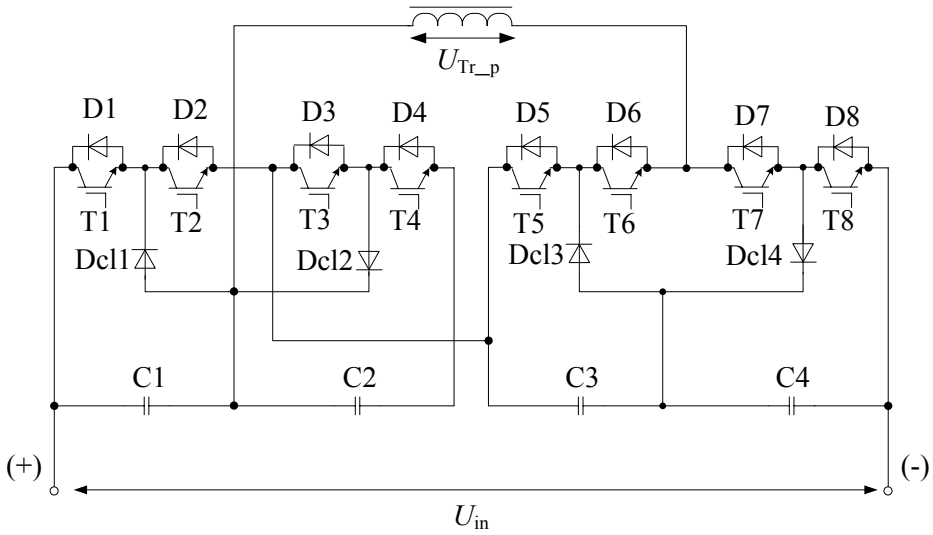


Figure 15 Cascaded cell multilevel inverter

The flying capacitor multilevel inverter, as shown in Figure 14 (a), has the smallest component count but high voltage bipolar thin film capacitors are expensive and can easily fail when exposed to strong vibration and extreme temperatures. The neutral point diode clamped three level inverter has two clamping diodes instead of the capacitor. The diodes are relatively inexpensive and reliable components when compared with capacitors, thus the neutral point clamped topology presented in Figure 14 (b) will be more advantageous in this application. It is also possible to use a mixed solution of neutral point diode clamped flying capacitor multi-level inverter that incorporates good properties of the both topologies.

The cascaded cell multi-level converter topology, shown in Figure 15 is well suited for use in systems with high input voltages but the inverter stage and the control system of the converter are complex.

2.2.4 Multiconverter Topologies

Another possibility to achieve high-voltage blocking is the cascaded converter topology (Figure 16) [28]. In that case, a number of identical two-level isolated DC/DC converters are connected in series at their inputs to achieve the desired voltage blocking capability of primary inverters. The number of cascaded converters depends of the voltage blocking capability of IGBTs used in primary inverters. Output leads of these converters are connected in parallel, thus the output current is distributed between the converters. It gives an extra opportunity to use secondary rectifier diodes with the reduced operation current and implement higher switching frequencies. Another advantage of cascaded converter topology is the effect of “distributed magnetic cores”, i.e. using a number of isolation transformers instead of one bulky unit enables a more compact and space-saving design of a power converter. The same assumption applies to the output filter chokes as well.

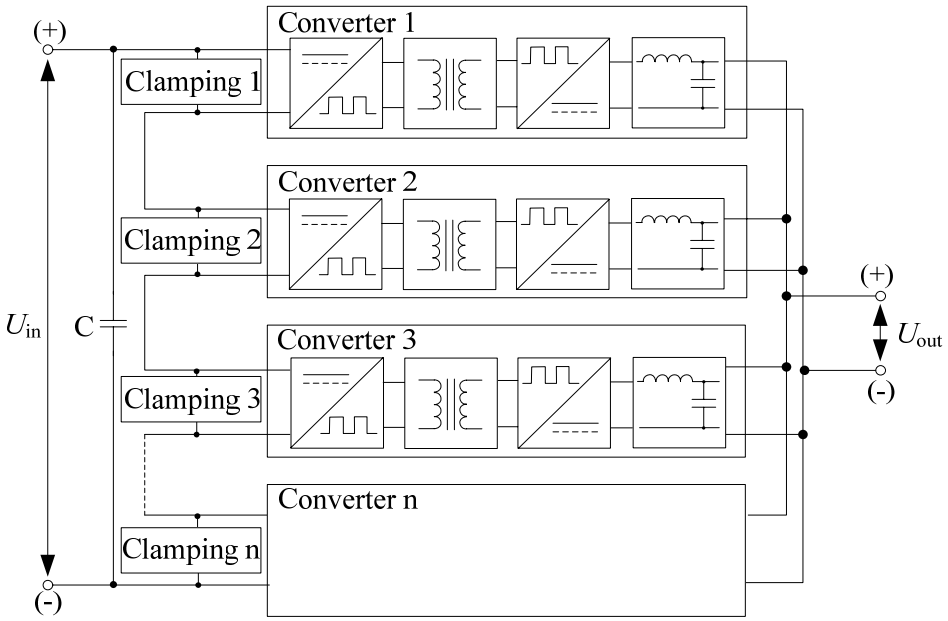


Figure 16 Example of APS with n cascaded converters

Multilevel topology combines some serious disadvantages like: increased number of components, decreased long-term reliability, increased complexity of control and protection circuits, increased dimensions and weight of the converter.

2.2.5 Rectifier Stage Topologies

A variety of rectifier topologies are used today in switch-mode power supplies. It is well understood that certain secondary-side topologies are less desirable in the specific railway applications [29]. Rectifier-stage designs usable in FEC are: center-tapped full-bridge [31] [32] [33], full-bridge [30], and current-doubler [34] rectifier topologies shown in Figure 17 (a), (b) and (c), respectively.

Center-Tapped Full-Wave Rectifier

Figure 17 (a) illustrates a center-tapped full-wave rectifier. A full-wave center-tapped rectifier is commonly used in high current, low voltage applications. Since there is only one diode forward voltage drop in the circuit at each conduction period [35] but the power rating of the transformer has to be about 30% greater in comparison with a full-wave bridge transformer.

Full-Bridge Rectifier

A topology of a full-bridge rectifier (Figure 17, b) is most cost-effective because it requires a lower VA-rated transformer than a center-tapped rectifier. As a drawback, more diodes are required than in the center-tapped circuit. Also the full-bridge rectifier suffers a slight performance disadvantage as well as an additional voltage drop.

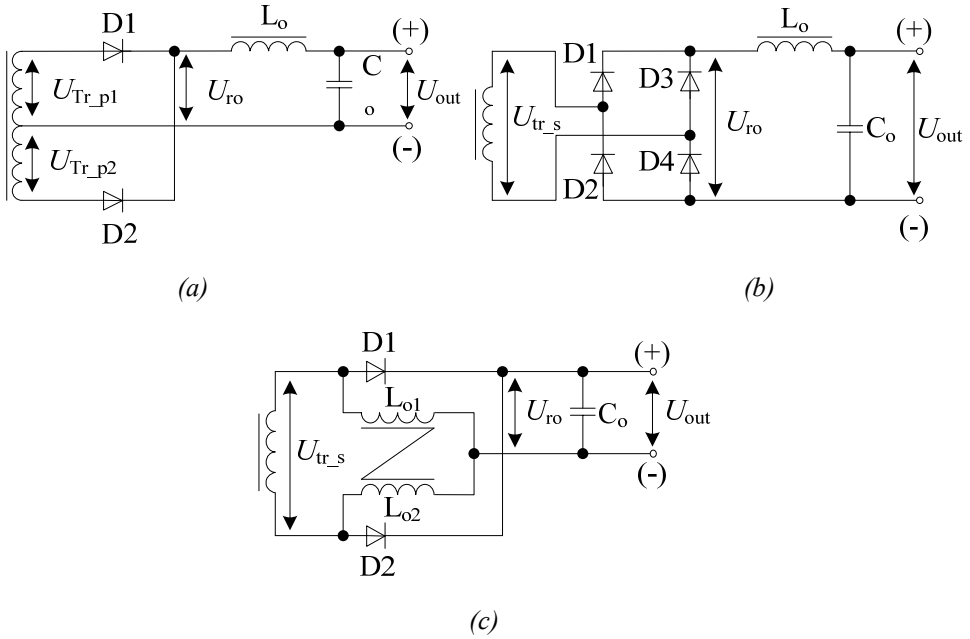


Figure 17 Center-tapped (a), full-bridge (b) and current-doubler (c) rectifier topologies

Current-Doubler Rectifier

The current-doubler rectifier (Figure 17, c) provides an alternative rectification technique to the center-tapped topology [36] [37]. The advantages of the current doubler rectifier stage are: lower loss in the power transformer due to the lower secondary current, simpler mechanical structure for the output transformer, lower output capacitance required for the same voltage ripple [38]. Operation of the primary side of the transformer is unchanged [39]. The drawback of this topology is the need for two separate output inductors.

Table 15 gives a side-by-side comparison of these three rectifier topologies.

Table 15. Evaluative comparison of different rectifier topologies

Parameter	**Value**		
	Center-tapped rectifier	Full-bridge rectifier	Current doubler rectifier
Rectifier output voltage, U_{ro}	$U_{Tr\_p\_amp1,2}$ - U_{F_rd}	$U_{Tr\_p\_amp}$ - $2U_{F\_rd}$	$U_{Tr\_p\_amp}/2$ - U_{F_rd}
Maximum required repetitive reverse voltage, U_{RRM}	$2U_{ro}+U_{F\_rd}$	$U_{ro}+2U_{F\_rd}$	$2U_{ro}+U_{F\_rd}$
Average value of diode forward current I_{F_rd} (av)	I_{out}(av)/2	I_{out}(av)/2	I_{out}(av)/2
Number of diodes	2	4	2

Table 16 shows the rectifier topology related changes of the isolation transformer and the output filter.

Table 16 Rectifier topology related changes of the isolation transformer and the output filter

Parameter	Value		
	Center-tapped rectifier	Full-bridge rectifier	Current doubler rectifier
Number of transformer secondary windings	2	1	1
Relative number of transformer secondary turns	1+1	1	1·2
Number of filter inductors	1	1	2
Number of filter capacitors	1	1	1

The criteria of comparison are: rectifier output amplitude voltage (U_{ro}) in relation to the secondary amplitude voltage (U_{Tr_p}) of the transformer, maximum required repetitive reverse voltage (U_{RRM}) of the diode in relation to rectifier output amplitude voltage, average diode current (I_{F_rd}) in relation to output current (I_{out}). The forward voltage drop (U_{F_RD}) of the diode was considered for comparison.

The center tapped rectifier has the smallest amount of rectifier diodes but needs more complicated and expencive transformer design. The full-bridge rectifier has the highest diode count but involves only one inductor and simple design of the transformer secondary winding. The current doubler rectifier (CDR) outclasses center tapped and full bridge rectifier topologies by better output parameters but needs two bulky filter inductors. For the output rectification of high-voltage switch-mode converters the full-bridge topology is the best choice. Although it has more diodes than the center-tapped, the diodes are not very expensive in comparison with the more complex center-tapped transformer required for center-tap rectification. A full-bridge rectifier outpaces the current-doubler in terms of two times smaller number of output filter inductors as well as in terms of two times lower per diode repetitive reverse voltage per diode, which gives an extra opportunity for a more compact design. Thus, the full-bridge full-bridge rectifier topology was selected to be implemented in the secondary side of the FEC.

2.3 Components and Materials

2.3.1 IGBTs

Converters based on the IGBT technology for the catenary voltages of 3.3 kV DC are only possible with IGBTs with the blocking voltage not lower than 6.5 kV [40]. Today's conventional IGBTs are basically available in 1.2 kV and 1.7 kV configurations up to currents 2.4 kA [40]. In the case of IGBTs with the blocking voltage lower than 6.5 kV, the multi-level inverter topologies are used (Figure 14)

[41]. However, the multi-level topologies have an increased component count, which could lead to low reliability and efficiency. Another way of coping with high blocking voltage demands is the series connection of lower-voltage IGBTs to a high-voltage switch in the two-level inverter topology (Figure 19) [42], [43], [44], [45]. Depending on the voltage blocking capability of the single transistors to be connected in series (1.2 kV, 1.7 kV, 3.3 kV or others), the total number of interconnected IGBTs varies from 6 to 2, as shown in Table 17.

As the converter must be able to operate in the extended supply voltage limits, (U_{in}=4 kV DC), so the number of IGBTs selected for the series connection must be coordinated to keep the nominal DC-link voltage level for each IGBT in accordance with the voltage class of the IGBT. In such a way combined high-voltage switch can operate with U_{in}=3.6 kV DC (±20 %). Table 15 provides an overview of operating voltages of different IGBT types and their minimal required number to combine a high-voltage switch with the 6.5 kV voltage blocking capability.

Table 17 Different candidate IGBTs for a high-voltage switch

IGBT type	**Nominal value of U_{in}, (kV DC) (± 20%)**	**Max. blocking voltage U_{CE_max}, (kV DC)**	**Min. number of series connected to a HV switch**
1.2 kV IGBT	0.6	1.2	6
1.7 kV IGBT	0.9	1.7	4
3.3 kV IGBT	1.8	3.3	2
6.5 kV IGBT	3.3	6.5	1

The 6.5 kV IGBT modules (INFINEON, ABB, IXYS, DYNEX, etc.) recently implemented are mainly designed for the two-level inverters with 3.3 kV input voltage. A single IGBT must have the voltage blocking capability two times the nominal catenary voltage level. Such transistors enable series connection of IGBTs to be avoided, achieving higher efficiency, power density and reliability compared to the combined HV switch designs. 6.5 kV IGBT modules are available in three basic configurations: with 200 A, 400 A, 600 A and 750 A collector current capabilities.

Realization Possibilities of a High-Voltage Switch

As shown in Table 17 a series combination of lower voltage switches is needed (2, 4 or 6 single IGBTs) (Figure 18 and Figure 19). Thus, the most economical and technically feasible solution will be implementation of dual IGBT (half-bridge) modules (Figure 19). The IGBT parameter mismatch in that case tends to be minimal.

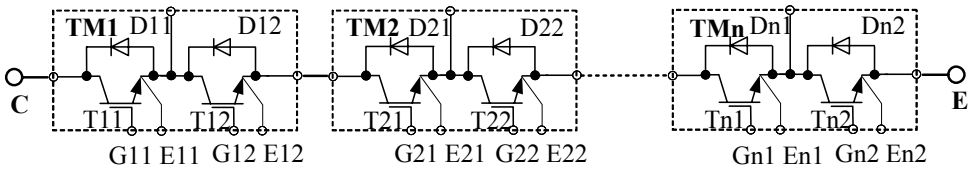


Figure 18 Interconnection of conventional IGBTs (1.2 kV and 1.7 kV IGBT half-bridge modules) [40]

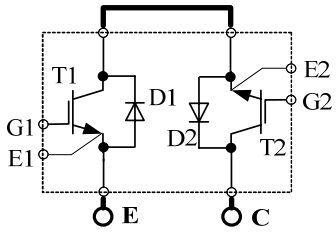


Figure 19 3.3 kV dual IGBT module [40]

The analysis below relies on the following IGBTs:

- Infineon 1.2 kV, 200 A half-bridge IGBT module FF200R12KE3,
- Infineon 1.7 kV, 200 A half-bridge IGBT module FF200R17KE3,
- Infineon 3.3 kV, 200 A dual IGBT module FF200R33KF2C,
- Infineon 6.5 kV, 200 A single IGBT module FZ200R65KF2.

Despite such advantages of power converters with single 6.5 kV IGBTs like simplicity and reliability, their overall design involves several limitations. These are mostly related to the specific properties of a single 6.5 kV transistor. Figure 20 shows the typical values of the turn-on delay time t_{d_on}, rise time t_r, turn-off delay time t_{d_off}, and fall time t_f for IGBTs with different voltage classes.

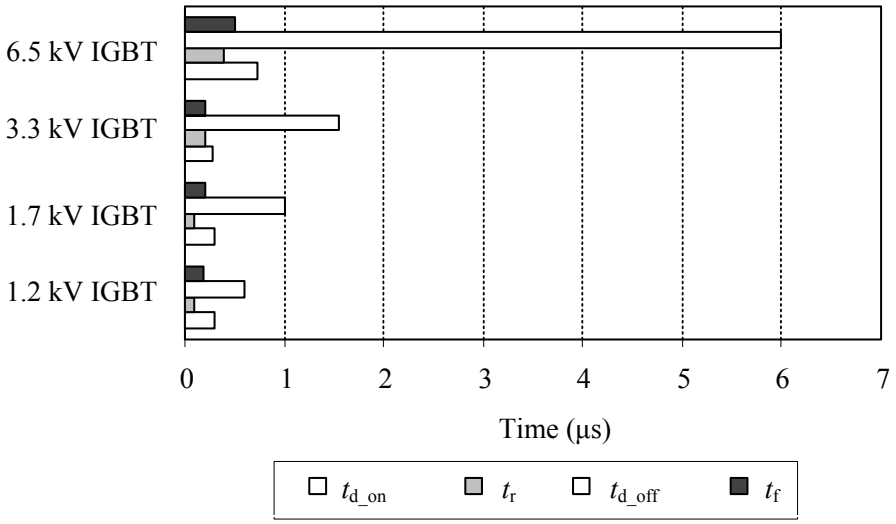


Figure 20 Comparison of turn-on and turn-off times of different IGBT types [40]

As seen from Figure 20, the turn-on (t_{d_on}) and turn-off (t_{d_off}) times of the 6.5 kV IGBT are much higher as compared to the 1.2 kV and 1.7 kV IGBT and even to another representative of the HV-IGBT class - the 3.3 kV IGBT. Table 18 outlines an overview of basic characteristic values of the investigated IGBTs. High collector-emitter voltage drop of 6.5 kV IGBTs predicts high conduction losses. Although the 1.2 kV, 1.7 kV and 3.3 kV IGBTs may have sufficient blocking voltage in series configuration, they lack the isolation strength and so additional isolation is needed to provide required isolation strength for HV operation of IGBTs (Table 19).

Table 18 Basic characteristic values of investigated IGBTs

Type of IGBT	**Collector-emitter voltage drop, (V)**	**IGBT thermal resistance, R_{thJC}/R_{thCH} (K/W)**	**FWD thermal resistance, R_{thJC}/R_{thCH} (K/W)**	**Stray inductance module, (nH)**
1.2 kV IGBT FF200R12KE3	2.0	0.12/ 0.01	0.20/ 0.01	20
1.7 kV IGBT FF200R17KE3	2.4	0.10/ 0.033	0.16/ 0.052	20
3.3 kV IGBT FF200R33KF2C	4.3	0.057/ 0.049	0.11/ 0.093	58
6.5 kV IGBT FZ200R65KF2	5.3	0.033/ 0.024	0.063/ 0.047	25

Table 19 Insulation voltage of investigated HV IGBTs

Type of IGBT	**Insulation voltage, (kV)**
1.2 kV IGBT, FF200R12KE3	2.5
1.7 kV IGBT, FF200R17KE3	3.4
3.3 kV IGBT, FF200R33KF2C	6.0
6.5 kV IGBT, FZ200R65KF2	10.2

Comparative Evaluation of Different High-Voltage Switch Solutions

To compare devices of the same power and voltage ratings, six 200 A, 1.2 kV IGBTs (three HB modules), four 200 A 1.7 kV IGBTs (two HB modules) and two 200 A 3.3 kV IGBTs (one dual module) were virtually connected in series forming a combined 200 A 6.5 kV switch (Figure 19). This combined high-voltage switch solution was further compared with the single 200 A 6.5 kV IGBT module.

On-State and Dynamic Analysis

As compared to their low-voltage counterparts, the turn-on of the 1.7 kV, 3.3 kV and 6.5 kV IGBTs takes considerably longer time as compared to the 1.2 kV IGBT.

This is basically limited by the Safe Operating Area (SOA) of the freewheeling diode, which determines the maximum current rise and voltage gradient of the IGBT during inductive commutation [46]. Also there are structural changes of the IGBT chip to reduce the ratio between short-circuit current and rated current to values between 3 (3.3 kV IGBT) and 5 (6.5 kV IGBT). As a consequence, gate-emitter and the Miller capacitance are increased [47], [48]. In combination with the demands on the gate resistor, this extends switching times and results in increased turn-on losses.

Table 18 shows the collector-emitter voltage drop for the different IGBTs investigated. Due to the sum of voltage drops in series connection, as the number of series devices increases, the total collector-emitter voltage drop as well as the freewheeling diode voltage drop and total on-state power loss will increase.

Technical and Economic Feasibility

Figure 21 features installation surface area requirements for different high-voltage switch solutions. It is obvious that the implementation of a single 6.5 kV IGBT results in smaller baseplate areas than the total baseplate areas of the combined HV switches. As dual IGBT modules are used, six 1.2 kV IGBTs result in three modules, four 1.7 kV IGBTs result in two modules and two 3.3 kV IGBTs result only in one module that is in size comparable with a 6.5 kV single IGBT module. Moreover, at their maximum performance, combined switch solutions require more powerful heatsinks to extract extra losses. Although the base plate size and weight of a twin 3.3 kV IGBT module and a 6.5 kV module are equal the more complicated driver circuit must be used with a dual 3.3 kV IGBT module. Thus, the use of single 6.5 kV modules instead of the series-connected devices seems more attractive when the space constraints of IGBT installation are determinative.

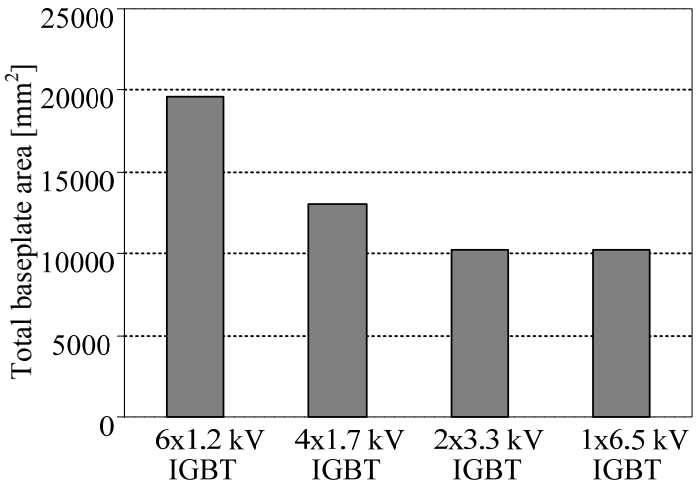


Figure 21 Comparison of installation area requirements for different high-voltage switch solutions

By the help of series connected 1.2 kV IGBT modules or single 200 A 6.5 kV IGBT module the total weight of a combined 200 A 6.5 kV switch could be reduced by

10 % as compared to HV switch solutions with series connected 1.7 kV and 3.3 kV IGBT modules, respectively (Figure 22).

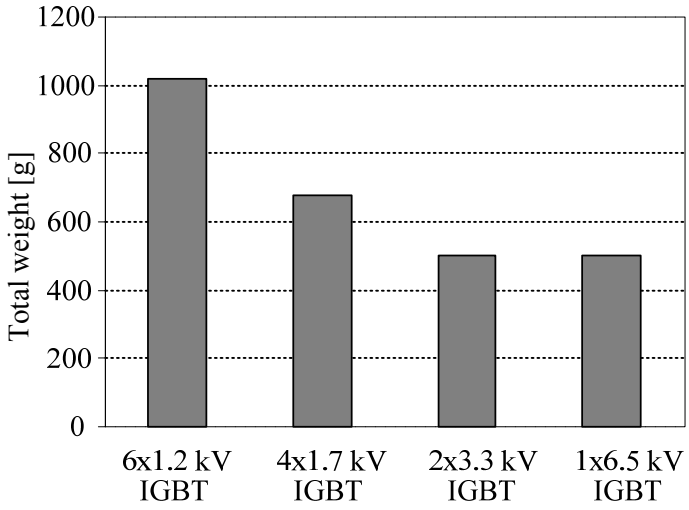


Figure 22 Total weight comparison of different high-voltage switch solutions

Figure 23 shows a comparison of total prices for different high-voltage switch solutions. Due to its relative novelty and recent high manufacturing costs, the 6.5 kV IGBT technology has lower competibility than other IGBT types in the high-voltage switch configuration.

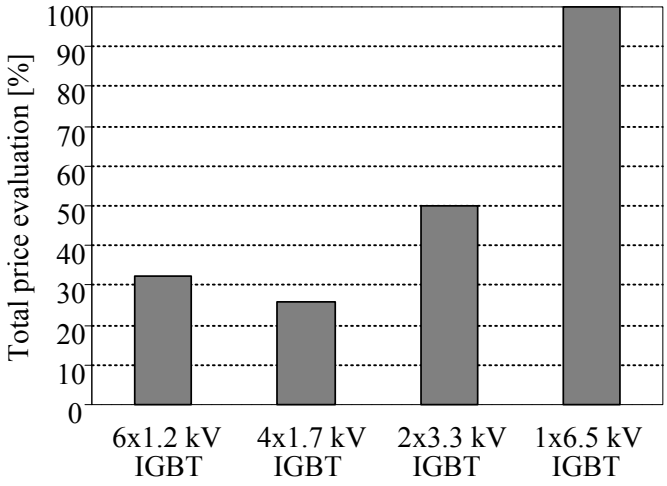


Figure 23 Total price evaluation of the different high-voltage switch solutions

One of the key-issues in the development of the combined HV switch is to ensure static and dynamic voltage sharing across the series connected IGBTs. Static voltage balancing can be achieved relatively easily by the connection of high resistance resistors in parallel with each IGBT.

The methods for dynamic voltage balancing can be divided into two groups: power circuit side (passive snubbers, voltage clamping circuits, resonant tanks etc.), and the gate side. Solutions on the power device side involve power scheme complication, resulting in increased weight and price of the final device. In [49] it is shown that voltage fall in transistors turn-off can be controlled by a central auxiliary circuit that guarantees a uniform turn-off transient for all the series devices. However, parameter mismatch of the series connected IGBTs during the off-state will cause unbalanced steady-state voltage distribution and the additional device side snubber or gate side control is still required [50].

The transient and static divergent collector-emitter voltages introduce a risk of element destruction due to the voltage and power dissipation stress [51] [52]. All this leads to auxiliary voltage-balancing circuits to be implemented on the high-voltage primary inverter.

Generalizations
Single 6.5 kV IGBT-based converters provide an excellent reliability due to the minimal required component number, simple power circuit and control system. Drawbacks are their high cost and high losses of 6.5 kV IGBTs. In some applications, like three-level neutral point clamped inverters, 3.3 kV IGBT dual modules provide a cost effective alternative.

2.3.2 Gate Drivers

In order to switch IGBTs on and off specialized IGBT gating circuits are used. High-voltage IGBT gate drivers must have the following abilities:

- high output power,
- galvanic isolation,
- built-in short circuit protection,
- status feedback,
- high switching frequency.

Drivers that are suitable for switching 6.5 kV IGBTs have the output power of 6 to 8 W [53]. According to specific requirements the isolation of gate drivers used in FEC with nominal input voltage of 3 kV DC must withstand at least 15 kV DC voltage surges and 4 kV DC in long term. The driver power supply must be galvanically isolated and the connection between the control system and the gate driver realized with a fiberoptic link. To prevent the damage in the case of short circuit a fast acting short circuit protection must be built into the gate driver.

To cope with high switching frequency requirements IGBT gate driver circuits must be able to maintain switching frequencies up to 50 kHz. The signal propagation delay is a crucial element in high frequency driven power electronic systems. Several high-voltage IGBT drivers that implement signal delays time from input to output less than 300 ns are available on the market.

One crucial external component is the gate resistor, as shown in Figure 24, (a) [54]. The external resistor determines the turn-on and turn-off time of the IGBT by limiting the gate switching current. To choose different turn-on and turn-off times for the IGBT, asymmetrical gate resistor could be used, as shown in Figure 24 (b). In IGBT drivers that operate at higher frequencies, the resonant switching is could be used to reduce losses dissipated in the driver circuit. The energy needed to switch the IGBT flows from the resonant inductor to the gate capacitance [55].

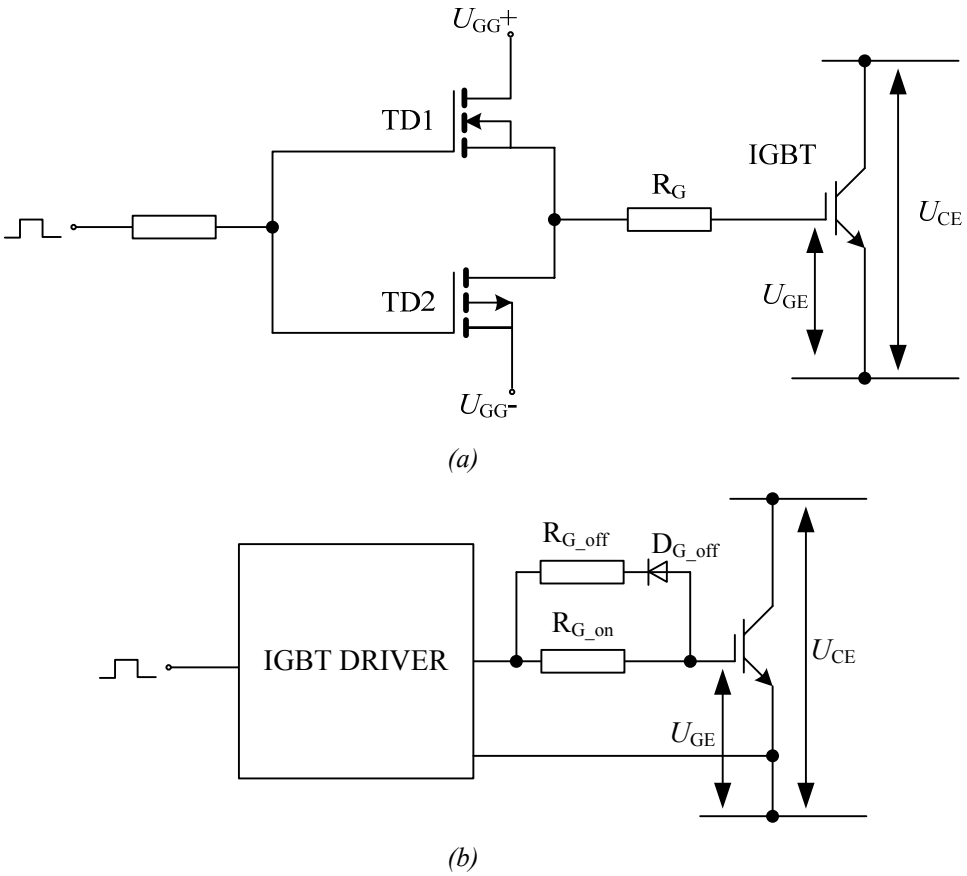


Figure 24 Typical IGBT gating circuit (a), asymmetrical gating circuit (b)

The state of the art high voltage gate drivers must have: high output power, high galvanic isolation, high switching speed, small signal propagation delay, short circuit protection, status feedback, and highly customisable peripheral circuits that could be fitted with rolling stock applications.

2.3.3 DC-Link and Filter Capacitors

In high-voltage power circuits mainly electrolytic and metalized film capacitors are used. Other types of capacitors like tantalum and ceramic capacitors have either too low voltage ratings or small capacitance. In the inverter of FEC capacitors must sustain voltage up to 4 kV DC (Table 4). In the output filter the amplitude value of voltage reaches 795 V. Inverter capacitors must tolerate relatively high voltage and

filter capacitors must have high capacitance to reduce voltage ripple in the converters output.

Electrolytic Capacitors

Electrolytic capacitors are common in power electronic equipment because they have high capacitance and are relatively inexpensive. Unfortunately tend electrolytic components tend to lose their capacitance over time. The highest rated voltage of electrolytic capacitors is limited with 500 V. Also, the effective series resistance (ESR) of an electrolytic capacitor is high, leading to high losses and temperature rise inside the capacitor. High temperature causes the liquid electrolyte inside the capacitor to evaporate through the seals of capacitor casing. At temperatures lower than - 40 °C the liquid electrolyte begins to crystallize leading to a rise in the effective series resistance [56]. Despite of all these disadvantages the electrolytic capacitor is still usable in the output filter of FEC due to its high current handling capacity and high capacitance.

Metalized Film Capacitors

Metalized film capacitors consist of thin metalized polymer foil. The foil material is usually either polyester, polypropylene, polycarbonate or polystyrene. As there is no liquid electrolyte in metalized film capacitors they also lack some of the problems common to electrolytic capacitors, like internal corrosion, electrolyte dry-up and electrolyte leakage. Metalized film capacitors have higher service lifetime, their capacitance does not change significantly over time, they have lower effective series resistance and their voltage rating is higher. But the overvoltages and overtemperatures degrade the polymer film [57]. Due to relatively low capacitance it is needed to connect several capacitors in parallel. In Table 20 metalized film and electrolytic capacitors are compared.

Table 20 Comparison of capacitors

Parameter	Capacitor type	
	Metalized film capacitor	**Electrolytic capacitor**
Capacitance	high	low
Volume	high	medium
ESR	medium	high
Price	high	low
Aging	slow	fast
Leakage current	low	high
Current handling capacity	medium	high
Voltage limit	high	low

Generalizations

Metalized film capacitors are suitable for use in FEC inverter circuits, because this capacitor type has slower aging, lower ESR, smaller volume, lower leakage current and high voltage rating. To achieve similar voltage ratings with electrolytic capacitors, several devices must be connected in series. The electrolytic capacitors are cheaper, have better current handling capacity and have high capacitance but

they are less reliable and have low voltage limit (500 V). Electrolytic capacitors could be used in circuits that have relatively low voltages but need high capacitance, like the output filter of FEC.

2.3.4 Rectifier Stage Diodes

The rectifying elements strongly influence the efficiency and the performance of the whole converter. Diodes used in the rectifier must have sufficiently high forward current and repetitive reverse voltage ratings. The forward voltage drop must be as low as possible to keep the rectifier power loss at low level. The switch boundary on-state times and the corresponding amplitude values of the rectifier output voltages U_{ro} are shown in Table 21.

Table 21 Values of U_{ro} for different operation points

Parameter	Value at U_{in_min}	Value at U_{in_max}
Converter input voltage, U_{in} (kV DC)	2.2	4
Duty cycle, D	0.80	0.44
Amplitude value of, U_{ro} (V DC)	438	795

The output rectifier diodes for the converters with a wide input voltage range must satisfy two basic criteria:

- maximum possible repetitive reverse voltage U_{RRM};
- maximum possible average forward current I_{F_rd} and minimized forward voltage drop U_{F_rd}.

To analyze the strengths and weaknesses of different type rectifier diodes that could be used in the output rectifier of FEC, general specifications of on-market available diode types are compared in Table 22, (based on the production of company IXYS).

Table 22 Evaluative comparison of different rectifier diode characteristics [35]

Parameter	Silicon diode	Silicon Schottky diode	SiC Schottky diode	GaAs Schottky diode	FRED diode
Maximum repetitive reverse voltage U_{RRM}, (V)	1600...2200	200	1200	600	1800
Forward voltage drop, U_{F_rd}, (V)	1.2...2.2	0.3...0.7	1.5	1.7	0.6...1.8
Reverse recovery time, t_{RR}, (ns)	500...15000	25	20	20	40...450
Maximum forward current, I_{F_rd}, (A)	56...1800	200	11	38	180...453

The widely used common silicon rectifier diode has good voltage and current ratings. However, a high recovery time cancels their benefits in high frequency applications. Thus, the Schottky diodes or fast switching diodes (fast recovery, ultrafast recovery, etc.) have remarkable benefits [58]. Both of the diode types have low voltage drops in the on-state condition. For instance, the 0.3…0.7 V voltage drop of a Schottky diode (Table 22) and about 0.6 to 1.8 V voltage drop of fast recovery epitaxial diodes can improve the efficiency of the rectifier stage by 15 to 35 %. Also, Schottky diodes have very fast reverse recovery times and negligible switching losses needed for a high-frequency rectification. SiC-based diodes have high forward voltage drop U_{F_rd} = 1.5...5 V that cancels other advantageous properties, like improved switching dynamics and high possible operation temperatures [59] [60]. Schottky barrier diode is extremely sensitive to temperature because of its high leakage characteristics over entire operating range. The PN junction diode (typically Fast Recovery Epitaxial Diode, FRED) has lower leakage at higher temperatures than the Schottky diode but the forward voltage is somewhat higher. For power supply designers, efficiency is a very undesirable trade-off for thermal stability [61]. Thus, for the high-frequency operation with voltages about 1 kV to 1.1 kV (transient overvoltages) and output currents of about 100 A, fast recovery diodes must be used.

2.3.5 Magnetic Components

The main magnetic components in FEC are the isolation transformer and the output filter inductor. In the input side, the primary voltage amplitude value can be up to 4 kV AC (Table 4), depending of the inverter topology. There are four basic types of inductors and power transformer that could be used in FEC (Figure 25).

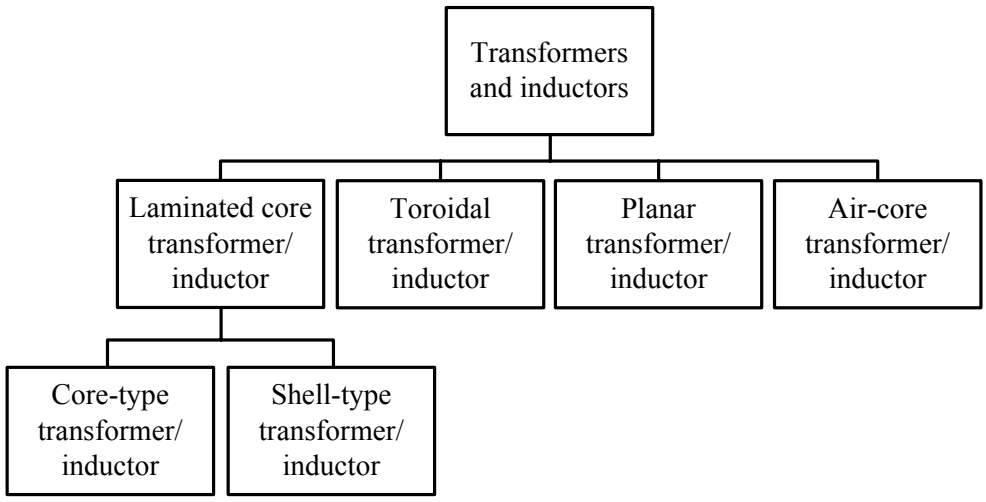


Figure 25 Basic transformer and inductor types

The isolation between primary and secondary windings and between windings and the core must withstand those voltage and short impulses up to 15 kV DC (Table 7). In the secondary side the voltage amplitude is 2.22 times lower but the output current is accordingly higher. High current in the secondary winding of the isolation transformer and in the output filter inductor demands a low active resistance of

windings. The switching frequency is in the range from 1 kHz to 2 kHz. At that frequency the skin effect in windings is the factor that must be acknowledged with [62]. As the magnetic components are the bulkiest details in the whole device that volume is in correlation with the frequency, so higher frequencies are more favorable.

Laminated Core Transformer

Laminated core is the most common core type of transformer that can be either shell or core type. The core of shell type transformer is constructed in most cases using E and I shape steel parts, steel core surrounding windings [63] (Figure 26, a). The shell type transformer is built, using L shaped steel details and there are windings around both sides of the core (Figure 26, b). Core type transformers are easier to isolate and the cooling is also somewhat better but shell type transformers have smaller dimensions and are more cost effective. Shell type cores are mostly used in small electronic devices and core type transformers in high voltage and high power systems.

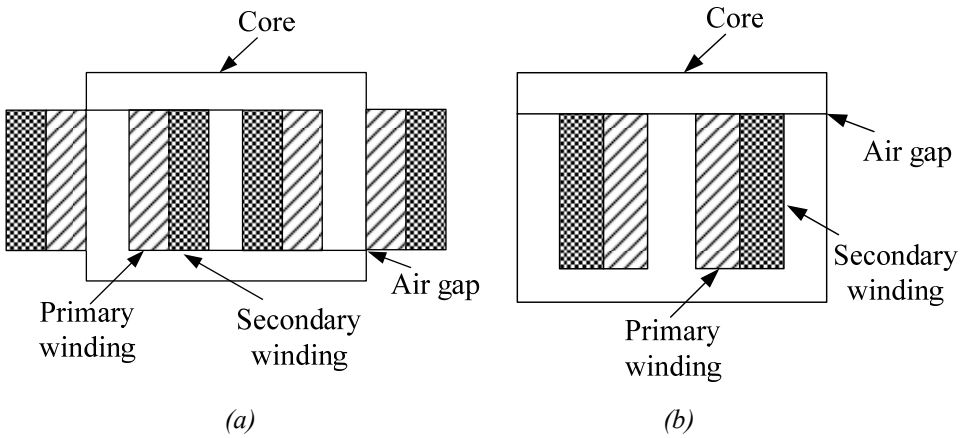


Figure 26 Core type laminated core transformer (a), shell type laminated core transformer (b)

Core type transformer can also be tape wound cut – C – type core where magnetic core is constructed from metal tape instead of thin L shaped details (Figure 27).

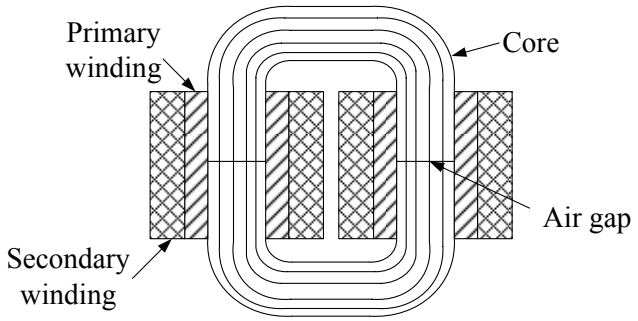


Figure 27 Tape wound cut - C core

Toroidal Transformer

As the windings of a toroidal transformer cover the core more evenly than laminated steel E, I and L cores a toroidal transformer can operate at higher flux density when compared with other types of transformers [63] (Figure 28). Also the covering winding of a toroidal transformer has a screening effect, reducing the radiated magnetic field. Toroidal transformers are more compact, less noisy and more efficient.

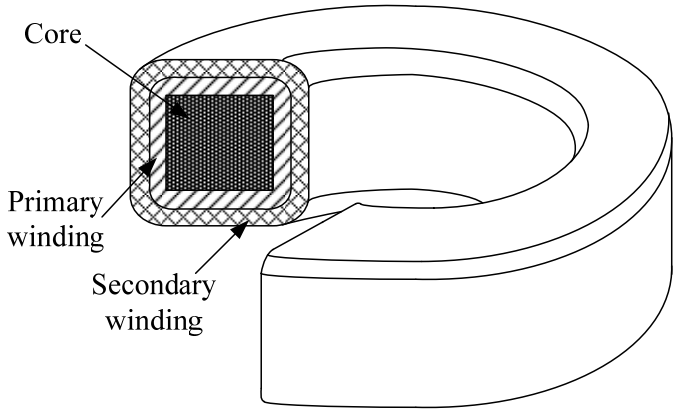


Figure 28 Cross section of toroidal transformer

The cores of toroidal transformers are either powder or ribbon wound cores. Powder cores are manufactured from very fine particles of magnetic materials that are coated with inert insulation to minimize eddy currents and form an air gap that is distributed evenly along the whole core [64]. Ribbon wound core consists of long magnetic metal alloy ribbon that is placed around the round form. The main disadvantage of a toroidal transformer is the cooling of the magnetic core that limits its maximum output power.

Planar Transformer

The planar transformers (Figure 29) are mostly used in small electronic assemblies as they are taking up much less space than conventional magnetic devices.

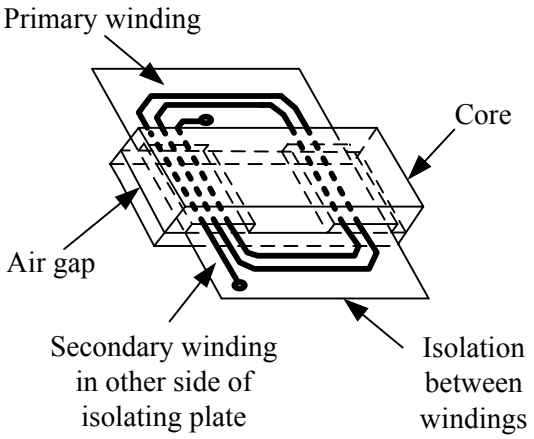


Figure 29 Planar transformer

The latest developments have introduced planar transformers with relatively high power (≤ 150 kW) and high voltage ratings (≤ 10 kV DC). Large surface area is good for cooling the transformer windings but the leakage inductivity can be 50 times higher when compared with a similar toroidal transformer [65]. The leakage inductivity is reduced by heavily interleaving primary and secondary windings but interleaving increases the capacitance coupling between primary and secondary windings.

Air-Core Transformers

Air-core transformers do not have a ferromagnetic core. Air core transformers have no losses due to core hysteresis but they have very high leakage inductivity and they are completely unsuitable for power electronics applications. Air-core transformers are used mostly in radio-frequency devices due to their high frequency range [66] [67]. In Table 23 the possible transformer and inductor types are compared based on five parameters.

Table 23 Comparision of different transformer and inductor types

Type	Leakage inductivity	Size	Current capability	Voltage regulation	Cooling
Laminated core	Low	Medium	High	Good	Good
Toroidal	Low	Medium	Medium	Good	Medium
Planar	Medium	Small	High	Good	Good
Air-core	High	Big	Low	Low	Good

Leakage inductance is quite low for laminated core and toroidal transformers. High leakage inductance of planar transformers is normally reduced by interleaving windings but the heavy interleaving increases capacitive coupling between the primary and secondary winding. Planar transformers are the smallest ones but also the toroidal transformers are compact. All designs have quite good current capability except for the air core transformers. Also voltage regulation of air-core transformers is very low and the secondary voltage drops too much if load is applied thus making air-core transformers and inductors unsuitable for use in the proposed applications. Cooling is a problem for toroidal transformers because the windings are enclosing the whole core, preventing heat exchange with the surrounding environment. When analyzing all advantages of a toroidal transformer, like compact size, high efficiency, low EMI ratings, low leakage inductivity and good voltage regulation, the toroidal transformer can be considered as a suitable isolation transformer type for use in FEC. High currents (> 100 A) in the output filter of FEC require better cooling that makes a laminated core a good choice. Planar transformers may be the key elements for future power electronics devices where high power density and small size are required.

Magnetic Materials

The values of magnetic materials like permeability $\mu_{\text{н}}$, saturation and magnetic induction B_{sat} of the magnetic core material are essential for maximal weight-space optimization of the transformer. In Table 24 different soft magnetic materials are

compared. The basic choice of the core material for these frequency ranges are iron, steel and Permalloy. Permalloy has quite good magnetic properties but also a high value of magnetostriction. Another drawback of Permalloy is associated with its softness because flat particles are liable to be deformed by stresses induced during milling, also resulting in a loss of magnetic properties. Ferrites are not considered for such high-power low-frequency operation because of their relatively low permeability and saturation magnetic induction [68].

Table 24 Magnetic properties of some soft magnetic materials

Material	**Magnetic induction, B_{sat} (T)**	**Magnetic permeability, $\mu_н$ (H/m)**	**Maximum permeability, μ_{max} (H/m)**
Permalloy	0.70...0.75	14000...50000	60000...300000
Silicon steel	2	200...600	3000...8000
Ferrites	0.18...0.40	100...6000	3000...10000
Iron	2.16	250	7000
Gammamet	0.8...1.12	7000...20000	40000...600000

Alternative to permalloy, iron and ferrites cores are Gammamet toroidal magnetic core made from 25 μm thick ribbon of soft magnetic nanocrystalline alloy on Fe-basis [68].

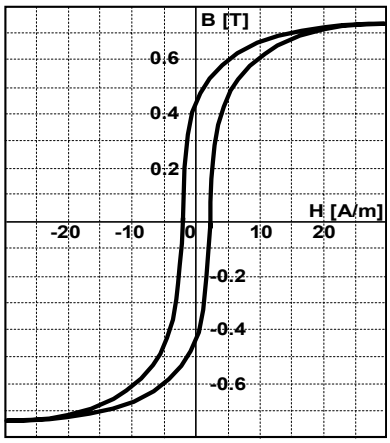


Figure 30 B-H loop of the Gammamet GM14DC core

From the product range of Gammamet Inc. most suitable magnetic core model is Gm14DC. Advantages of the selected toroidal magnetic cores Gm14DC are: high initial permeability and very low core losses [68]. Physical and magnetic parameters of Gm14DC magnetic cores are presented in Figure 30 and Table 25.

Table 25 Typical properties of GM14DC core

Parameter	**Value**
Saturation magnetic induction, B_{sat} (T)	0.8
Initial permeability, $\mu_н$ (H/m)	20000
Maximum permeability, μ_{max} (H/m)	50000

Winding Technologies

Different winding technologies and winding strategies can influence the DC and AC resistance, leakage inductance and current capability of magnetic components. At higher switching frequencies special type foil and litz wire windings are used to reduce skin effect and proximity effect losses [64]. Skin effect is the situation when the current density of the alternating current is higher close to the surface of the conducting material. When the switching frequency rises, the AC resistance of windings will also rise. The AC resistance of the conductor R_{AC} is calculated as follows:

$$\delta = \sqrt{\frac{2\rho}{\omega \cdot \mu}}, \tag{1}$$

$$R_{AC} = \frac{\rho}{\delta} \cdot \left(\frac{l_{cond}}{\pi \cdot (d_{cond} - 2\delta)} \right), \tag{2}$$

where: δ is the skin depth, ρ is the resistivity of the conducting material, μ is the absolute magnetic permeability of the conducting material, ω is the angular frequency of current, l_{cond} is the length of the conductor and d_{cond} is the the diameter of the conductor.The proximity effect is caused by the electromagnetic field around every single wire that induces eddy currents in nearby conductors altering the overall distribution of the current flowing through the winding of the transformer or the inductor, increasing the ac resistance and losses of the whole winding. The AC resistance caused by the proximity effect can be calculated using the Dowell method. In the Dowell method the round conductor with diameter d_{cond} is replaced by the rectangular one that must have the width of $\sqrt{\pi}\, d_{cond}/2$ and height h and the conductor is divided into layers. The AC resistance of the conductor R_{ac} is calculated as follows [49]:

$$R_{AC,m} = R_{DC,m} \cdot \frac{\xi}{2} \cdot \left[\frac{\sinh \cdot \xi + \sin \xi}{\cosh \cdot \xi - \cos \xi} + (2m-1)^2 \cdot \frac{\sinh \cdot \xi - \sin \xi}{\cosh \cdot \xi + \cos \xi} \right], \tag{3}$$

where ζ is:

$$\xi = \frac{\sqrt{\pi}}{2} \cdot \frac{d_{cond}}{\rho}, \tag{4}$$

where $R_{AC,m}$ is the AC resistance of the m-th layer, $R_{DC,m}$ is the DC resistance of the m-th layer and m is the number of the analyzed layer. Skin effect and proximity effect can be calculated separately. In the isolation transformer of FEC foil windings could also be used, where the wire is replaced by thin copper foil that is wound around the core. Foil windings have better parameters than other winding types but are also hard to manufacture and repair. Mechanical defects of conducting foil edges and small particles that are trapped between conducting and isolating foil may cause turn to turn faults requiring specialized technology for transformer manufacture [69]. An alternative to hard-to manufacture foil winding is litz-wire

winding, where one solid wire is replaced by many isolated parallel wires, increasing effectively the wire surface and reducing AC resistance.

Winding Strategies

Not only the winding type but also the position of winding wires has an effect on the overall performance of a transformer. Leakage inductance of a transformer is lowered by interleaving the primary and secondary windings. In Figure 31 three different winding strategies of the transformer with a toroidal core are shown. In Figure 31 (a) the windings are not interleaved, causing high leakage inductance. The winding shown in (b) has somewhat lower leakage inductance and AC resistance as the windings are lightly interleaved.

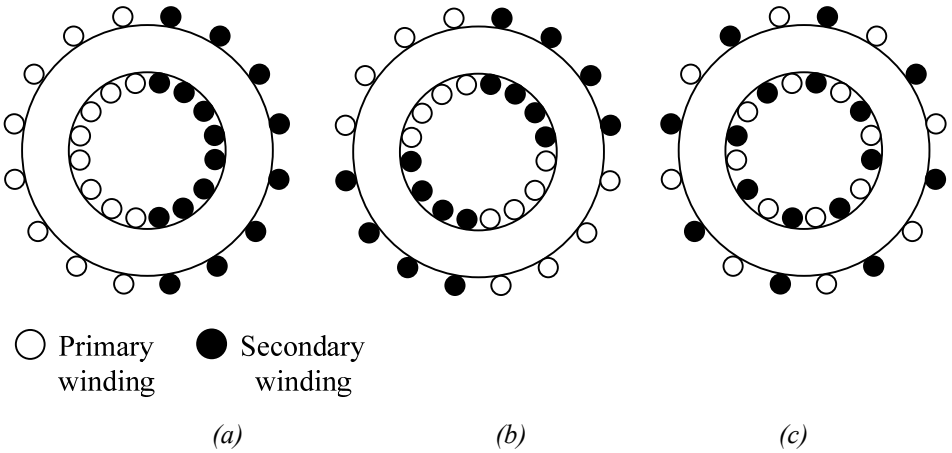


Figure 31 Winding strategies: non interleaved winding (a), interleaved winding (b), heavily interleaved winding (c)

Winding strategy shown in Figure 31, c) has the lowest leakage inductance and AC resistance. Studies show that at higher frequencies AC resistance can differ 2 % and leakage inductance around 90 % when structures a) and c) are compared [70]. At medium frequencies (1 kHz to 2 kHz) the differences are not so great but still evident. Totally interleaved windings (Figure 31, c) result in the smallest leakage inductance but are also the most expensive and the hardest to manufacture.

Generalizations

Most suitable transformer type for use as isolation transformer in FEC is the toroidal core transformer with interleaved windings and with soft magnetic nanocrystalline alloy on Fe-based core material. As the foil windings are hard to manufacture with the toroidal core, the litz wire windings may used instead. As the cooling capability of the core type, laminated core transformers are better than toroidal type devices, it is plausible to use this core type in output filter inductors.

2.3.6 Protection Devices

The protection devices usable in rolling stock converter systems with nominal voltage up to 4 kV DC can be divided into two groups: crowbar devices and clamping devices [71] (Figure 32).

The crowbar type protection devices generate a short circuit when the input voltage exceeds the breakdown voltage of the protection device. On some occasions a crowbar device may not turn off when the voltage returns to the nominal value and the short circuit is not removed until the input voltage of the converter is switched off. The crowbar devices must be installed along with additional overcurrent protection devices (fuses etc.). Crowbar-type short-circuiting protective devices, usable in the input circuit of FEC are: Gas Discharge Tube (GDT) and Thyristor Surge Protection Device (TSPD).

The clamping type overvoltage protection devices shunt the excessive voltages, when the input voltage exceeds the breakdown potential of the clamping device. The clamping protective devices can shunt several overvoltage impulses without disturbing normal operation of the whole converter. Clamping-type short-circuiting protective devices are: Metal Oxide Varistor (MOS) and Transient Voltage Supressor (TVS).

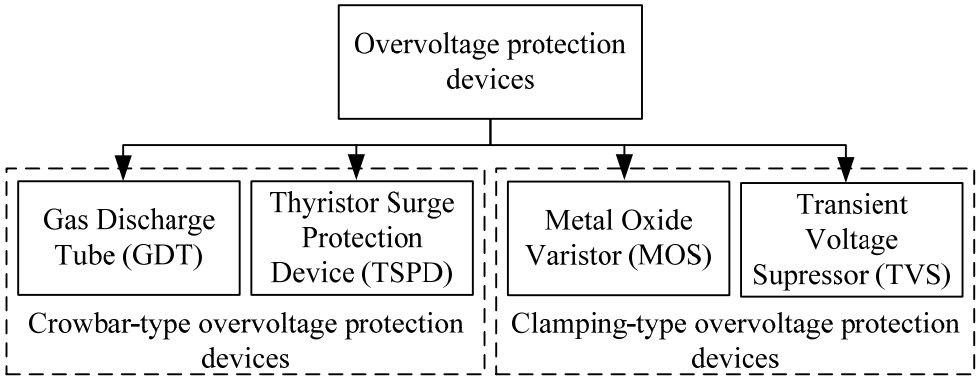


Figure 32 Classification of overvoltage protection devices

Gas Discharge Tubes

Gas discharge tubes (GDT) are protection devices that rely on the noble gas breakdown in overvoltage condition. The internal construction and typical voltage – current characteristics of the GDT are shown in Figure 33.

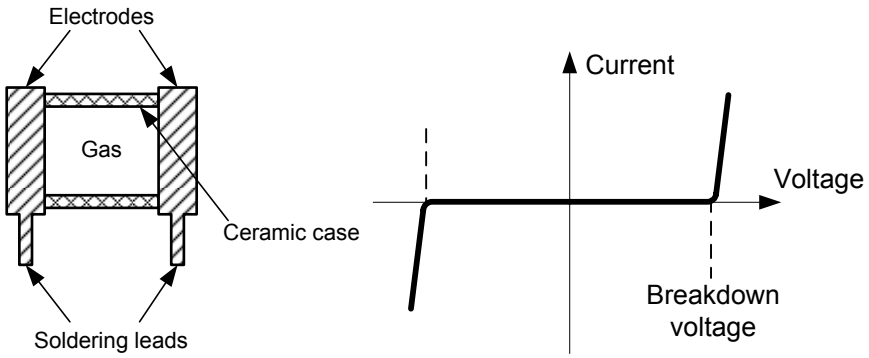


Figure 33 Internal construction of gas discharge tube (a) and typical voltage – current characteristics of GDT (b)

High voltage potential difference between the internal electrodes of the GDT ionizes the gas in the tube and forms a conductive plasma channel, short circuiting the GDT. Due to hysteresis in the breakdown voltage characteristics, the electric arc may not turn-off when the voltage across GDT returns to normal value. GDTs have high current handling capacity but they are quite slow as compared to other surge protection devices [72].

Thyristor Surge Protection Devices

Thyristor surge protection devices (TSPD) are based on a pair of intertwined bipolar transistors (Figure 34, a) [72]. TSPD consists of four layers n and p doped silicon that forms three junctions J1, J2 and J3. Layers P2, N2 and P1 form pnp transistor and N2, P1 and N1 form the npn transistor (Figure 34, b). In normal conditions the junction J2 blocks the current flow through TSPD. When the voltage potential between TSPDs anode and cathode exceeds the breakdown voltage of reverse biased junction J2 (Figure 34, c), the current begins to flow through N2 and P1 layers that form the bases for both transistors, turning them on and dramatically lowering the internal resistance of TSPD.

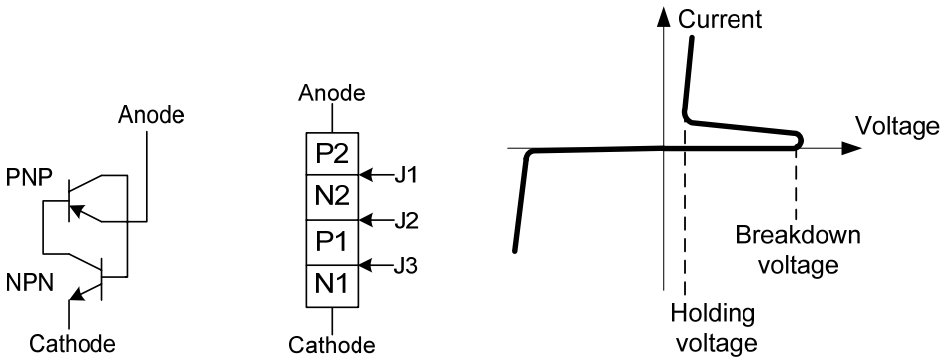


Figure 34 Thyristor Surge Protection Device circuit (a), TSPD physical layout (b) and typical voltage – current characteristics of TSPD (c)

To ensure bipolar function of the TSPD, two anti-parallel thyristors are used (Figure 35).

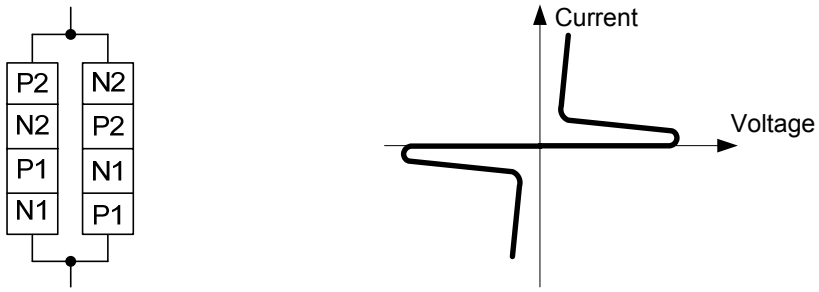


Figure 35 Bipolar TSPD (a) and typical voltage – current characteristics of bipolar TSPD (b)

In many aspects the TSPD is similar to the GDT. The TSPD has good current handling capability, its breakdown voltage accuracy is better than that ofGDT and TSPDs have more compact design than GDTs [72]. To turn the TSPD off after voltage surge, the voltage across TSPDs terminals must drop lower than the holding voltage (Figure 34, b). There are available also controllable TSPDs available that require additional control system to turn them off after the high voltage spike.

Metal Oxide Varistors

Metal oxide varistors (MOS) are voltage dependent, semiconductor resistors. The semiconductor material used in the varistor is a metal-oxide, i.e. ZnO (Zinc oxide) [73]. Metal oxide is in a granular form and the granules, touching each other form a matrix of parallel, serious and anti-parallel small diodes that conduct when high voltage is applied across them, reducing rapidly the resistance across the leads of a varistor. Figure 36 is shows a simplified cross section of a typical metal oxide varistor along with the typical voltage – current characteristics of a metal oxide varistor.

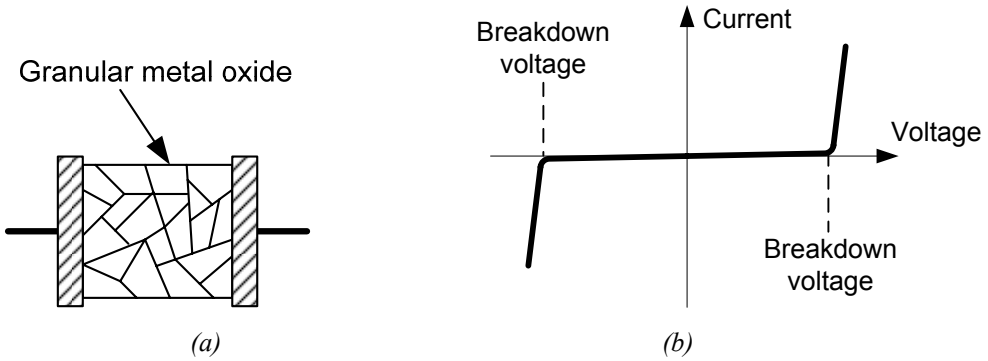


Figure 36 Cross section of metal oxide varistor (a), typical voltage – current characteristics of metal oxide varistor (b)

The properties of the varistor are determined by the grain size, the nature of the matrix material between the grains, the thickness of the ceramic and the attachment of leads to the ceramic [72]. The varistors have a good current handling capability, are inexpensive and can be implemented for a wide variety of voltages and have small outside dimensions. The negative sides of MOS are the low breaking voltage accuracy (± 10 %) and the wearout of the varistor [74].

Transient Voltage Suppressors

Transient Voltage Suppressors are basically avalanche and zener diodes designed to handle the high current requirements for surge suppression [72]. TVS devices are fast, compact and accurate but have lower current handling capacity than other overvoltage protection devices. In the case of voltage surge much energy is dissipated internally in TVS device lowering the value and duration of the maximum allowed current flowing through TVS. Typical voltage – current characteristics of a unipolar transient voltage supressor are shown in Figure 37.

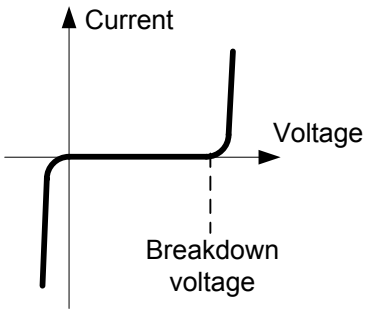


Figure 37 Typical voltage – current characteristics of transient voltage suppressor

Generalizations
Possible overvoltage protection devices, usable in FEC are compared in Table 26.

Table 26 Comparision of overvoltage protection devices

Type	Current Capability	Size	Voltage accuracy	Wearout	Breakdown voltage
Gas discharge tube	High	Large	Low	No	High
Thyristor surge protection device	Medium	Small	Medium	No	Low
Metal oxide varistor	Medium	Small	Medium	Yes	Medium
Transient Voltage Suppressor	Low	Small	High	No	Low

As thyristor surge protection devices and transient voltage suppressors have maximum breakdown voltages under 400 V [75] and so are they unsuitable for use in high-voltage equipment.

The breakdown voltages of Metal Oxide Varistors and Gas Discharge Tubes are higher than those of above mentioned protection devices (the company EPCOS produces MOVs with breakdown voltage up to 1.1 kV and GDTs with breakdown voltage up to 5.5 kV) [76]. Therefore metal oxide varistors are suitable for overvoltage protection in the high voltage circuit of FEC but means of overcurrent protection must be used along with MOVs (thermal fuses etc.). For better protection a MOV along with a GDT could be used.

2.4 Cooling and Packaging

2.4.1 Cooling Methods

Cooling methods feasible to be used in mass production for rolling stock power converters with the output power of 50 kW are: passive cooling, forced air cooling

and liquid cooling. Other cooling methods that use heat pipe, peltier effect, phase change or liquefied gasses are too expensive and difficult to manufacture and use, or have a cooling effect too weak.

Passive Cooling.
As the simplest, cheapest and most reliable of all the cooling methods, the passive cooling is most desirable for rolling stock applications where high reliability is required. The negative side of passive cooling systems is the need for large heatsinks that are exposed to the environment outside the device. The effectiveness of heatsink is improved when the air is moved by force with ventilators through the cooling fins of heatsink.

Forced Air Cooling
Forced air cooling is up to 70 % more effective than passive cooling, providing the same cooling power with less volume. Forced air cooling systems can dissipate much more loss power to the surrounding air but they are also noisy and require regular maintenance. Energy needed to drive ventilators reduces overall efficiency of the whole power supply.

Liquid Cooling
A liquid cooling system provides effective means to build very compact power stages of inverters and extract much heat from the system. A liquid cooling system also enables to place the majority of the cooling system outside the device to a thermally good position. Thermal resistance of the liquid cooling system is greatly influenced by the heatsink material (copper, aluminium) and the cooling liquid used (water, glycol, deionized water, dielectric fluids, polyalphaolefin, oil) [77]. The downside of liquid cooling is high complexity and low reliability.

Table 27 Thermal resistance limits for different cooling methods

Cooling system type	**Thermal resistance, R_{tha} (K/W)**	**Volume, (cm^3)**
Passive, convention heatsink	$56 \cdot 10^{-3}$	$24 \cdot 10^{3}$
Forced air cooled heatsink	$11 \cdot 10^{-3}$	$28 \cdot 10^{3}$
Liquid cooling system	$5 \cdot 10^{-3}$	$15 \cdot 10^{3}$

In Table 27 [78] the limits of the thermal resistance R_{tha} between the heatsink and air along with the approximate volumes of cooling systems are shown. Conventional passive heatsinks tend to have too high thermal resistance to be effective when the power loss is exceeding several kilowatts. Forced air cooled heatsinks can have more than five times lower thermal resistance between the surrounding air and the heatsink making it attractive to cool power converters. The liquid cooling system has superior cooling abilities but is expencive, maintenance intensive and complex to use in the demanding rolling stock applications. The implementation of the liquid cooling system is feasible when higher power loss is needed to be dissipated.

2.4.2 Busbars and Modular Design

In high-voltage, high power inverters the turn-off surge voltages can reach dangerous values. Those voltage surges are created by the energy that is stored in stray inductance of mechanic components (busbar system, DC-link capacitors, screw terminals etc.). The surge voltage U_{ces} appearing in IGBT turn-off is estimated with the following equations [29]:

$$U_{ces} = U_{in} + (L_s \cdot \frac{dI_C}{dt}), \tag{5}$$

$$L_s = L_{bus} + L_c + L_{mec} + L_{IGBT}, \tag{6}$$

where L_s is the commutation loop stray inductance, dI_c/dt is the change rate of IGBT collector current, I_c is the IGBT collector current, L_{bus} is the stray inductance of the busbar system, L_c is the internal inductance of DC-link capacitors, L_{mec} is the stray inductance of mechanical contacts (screw terminals) and L_{IGBT} is the internal stray inductance of IGBT module. U_{ces} may not exceed the maximum allowed voltage rating for inverter IGBTs or DC-link capacitors under any circumstances or those devices could be damaged or destroyed.

To keep the stray inductance low, a copper sheet busbar system could be used. The mutual inductance between flat stacked conductors with even width can be expressed as follows [79]:

$$L_{bus} = 0.22l \cdot \left[\ln(\frac{l}{d} + \sqrt{1 + \frac{l^2}{d^2}}) - (\frac{d}{l} + \sqrt{1 + \frac{d^2}{l^2}}) \right], \tag{7}$$

where l is the length of the busbar conductor (in cm), d is the distance between busbar conductors. By using high-voltage isolation materials the distance d could be significantly reduced.

2.5 Generalizations

Most suitable topology for the input inverter of FEC of an APS is a two-level inverter layout with 6.5 kV IGBTs. The inverter topology could be half- or full-bridge. To reduce inverter power losses, voltage surges and oscillations at transistor turn-off, more complicated a three-level neutral point diode clamped inverter could be used with series connected 3.3 kV IGBTs. The whole FEC can be constructed only as an isolated DC/DC converter, where the input and output are galvanically isolated by the transformer, because of the strict safety requirements for high-voltage power electronics equipment for rolling stock. For an output rectifier it is feasible to use a full-bridge, or current doubler rectifier with fast FRED diode modules. To limit the temperatures of semiconductor elements (IGBTs and diodes) forced air cooling provides good balance between reasonable cooling power and moderate complexity. For an isolation transformer the toroidal core can be used with litz wire and partially interleaved windings. For output filter components more conventional inductor constructions could be used like: laminated steel core

inductors with rectangular shape copper bar windings. Due to the required high voltage rating the best solution for DC-link capacitors is metalized film type capacitors, electrolytic capacitors with greater capacitance are well suited to filter the output of the front end converter. To keep the overvoltages, occurring at transistor turn-off as low as possible, all components in the inverter circuit must be connected, using low inductance busbars. Surge voltages from the contact line can be neutralized, using metal oxide varistors, combined with gas discharge tubes. Suitable technical solutions are outlined in Table 28.

Table 28 State of the art technical solutions to be used in the front end converter of an APS

Inverter	
General topology	Isolated DC/DC
Inverter topology	Two-level with HV IGBTs
Switching element	6.5 kV IGBT with built-in FWD
DC-link capacitor type	Metalized film
Overvoltage protection	
Secondary overvoltage protection device	Gas discharge tube (optional)
Primary overvoltage protection device	Metal oxide varistor
Inverter cooling system	
Cooling system type	Forced air cooling
Rectifier	
Rectifier topology	Full-bridge
Rectifier diode	FRED
Rectifier cooling system	
Cooling system type	Air cooling
Magnetic components	
Isolation transformer type	Toroidal
Isolation transformer windings	Litz wire, partially interleaved
Output filter inductor type	Laminated steel, core type core

3. Research and Development of Two-level Catenary-fed Isolated DC/DC Converters with HV IGBTs

3.1 Operation Principles of High-Voltage Full- and Half-Bridge Inverter Topologies

6.5 kV IGBT transistors make it possible to use simple two-level inverter topology in FEC. The most widespread topologies are full- and half-bridge topologies. Full-bridge (FB) inverter consists of four transistors that are controlled alternately (top transistor T1, bottom transistor T2 and top transistor T3 along with bottom transistor T4) forming two bridge arms, as shown in Figure 38 (b). The half-bridge inverter (HB) consists of the top transistor T1 and the bottom transistor T2 and two series connected capacitors C1 and C2, forming the bridge arms as shown in Figure 38 (a). HB topology is a simplified form of a FB inverter where two expensive high-voltage transistors are replaced with capacitors. Also the control system is simplified as there are only two IGBT drivers and two control channels needed for the HB inverter.

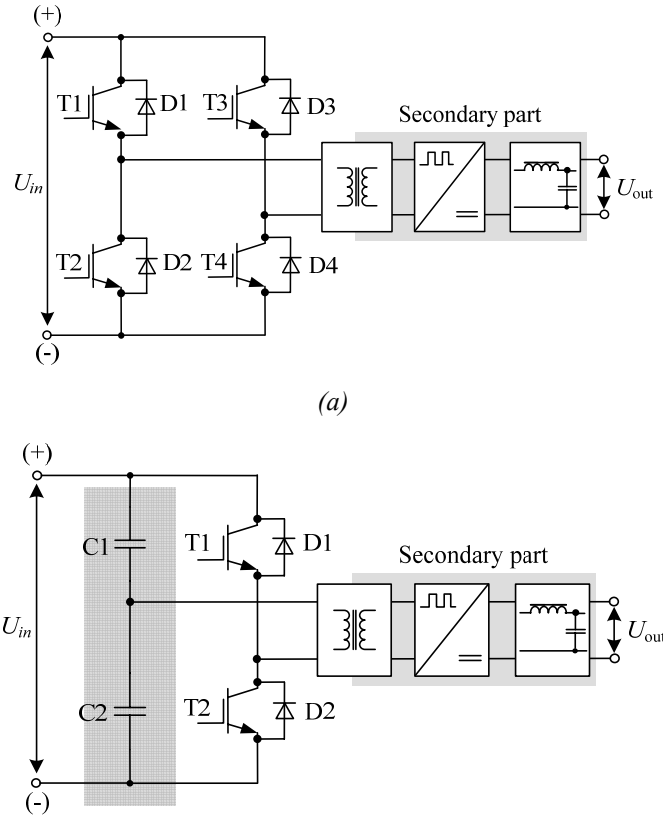


Figure 38 Full-bridge (a) and half-bridge (b) DC/DC converter topologies

Figure 39 shows simulated typical voltage and current waveforms of full- and half-bridge inverter semiconductor switches along with corresponding gate signals. In simulation all transistors are operating in the hard switching mode. In Figure 39 (a) and (b) collector current of one top transistor (T1 in HB and in FB inverter) is shown. Main differences between FB and HB inverters are:

- the output voltage (isolation transformer primary voltage) amplitude value of HB inverter (Figure 40, (a) is two times lower than the input voltage of the inverter,
- the amplitude value of the output voltage of the FB inverter (Figure 40, (b) is equal to the input voltage U_{in}.

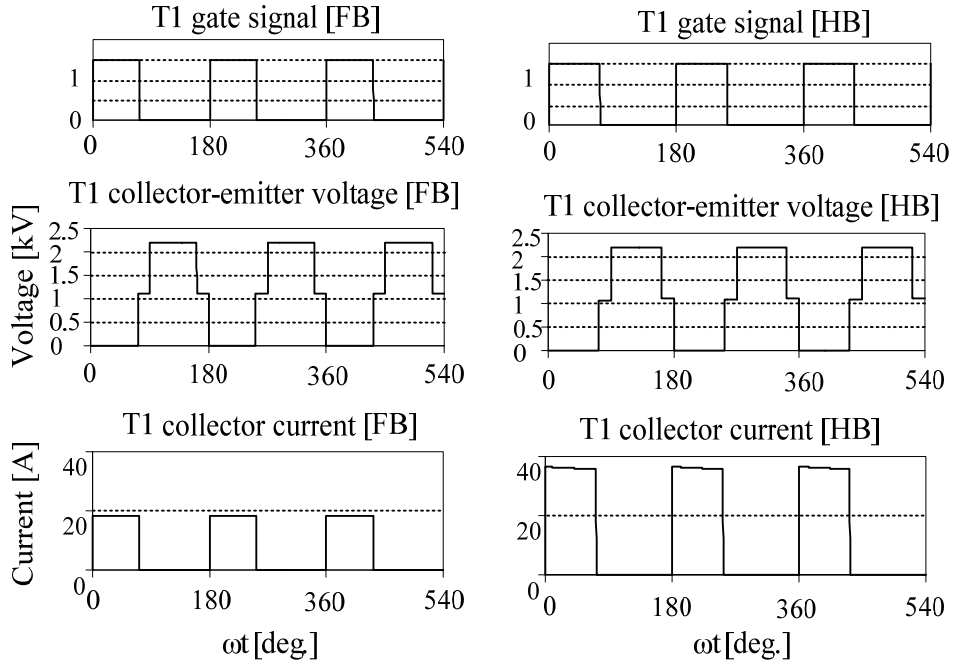


Figure 39 Generalized IGBT T1 collector-emitter voltage and collector current waveforms and gate signals of an HB inverter (a) and an FB inverter (b)

As the output power of FEC must be the same with both inverter topologies, the isolation transformer must be built according to the inverter output voltage of the inverter. In that case the amplitude value of the collector current of one IGBT in the FB topology is two times lower than that of the half-bridge inverter, as can be seen from graphs in Figure 39 (a) and (b).

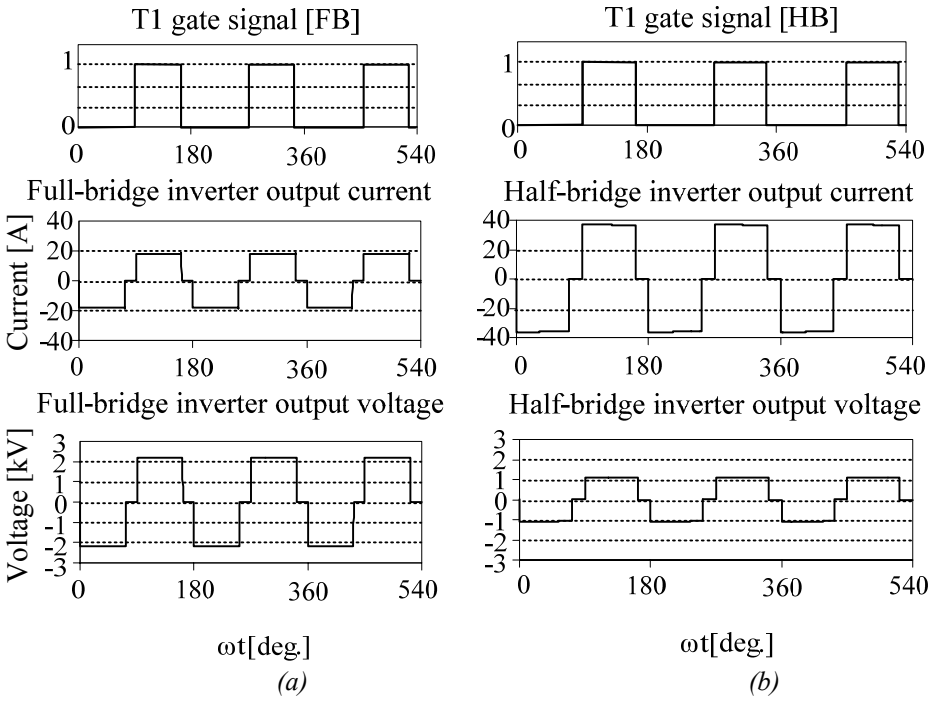


Figure 40 Generalized isolation transformer primary voltage and current of HB inverter (a) and FB inverter (b)

Both topologies have significant advantages and disadvantages as shown in Table 29.

Table 29 Advantages and disadvantages of half- and full-bridge inverters

Advantages	Disadvantages
FB inverter topology	
Lower IGBT current (higher possible switching frequency)	More complicated mecanical construction, control and protection (four IGBTs, four IGBT driver circuits, four control channels)
Lower isolation transformer primary current (low copper losses)	Four IGBTs (higher conduction losses)
	Higher isolation transformer primary voltage
HB inverter topology	
Only two IGBTs required	Two times higher IGBT current amplitude (limited switching frequency)
Simple mecanical construction, control and protection (two IGBTs, two IGBT driver circuits, two control channels)	Two times higher isolation transformer current (higher copper losses)
Lower isolation transformer primary voltage	

The output current (isolation transformer primary current) amplitude value of the HB inverter (Figure 40, a) is two times higher than that of the HB inverter (Figure 40, b) with a comparable output power. To prevent short circuit between bridge arms the transistors T1 and T2 are switched with dead time between impulses. The value of dead time could be reduced when all delays in the control system and turn-on and turn-off times of the IGBT are carefully analyzed.

3.2 Comparison of Half- and Full-Bridge Isolated DC/DC Converters with HV IGBTs

To choose the best suitable inverter topology for FEC twoinverter topologies were compared (FB and HB). The comparison of HB and FB inverter topologies is based on the following:

- the transistors used in the primary inverters of FEC are Infineon 6.5 kV IGBTs;
- converter components are ideal (no power dissipation);
- the turn ratio of the isolation transformers is 1:1;
- nominal input DC voltage U_{in} = 1.0 p.u. = 3.3 kV DC;
- maximum input DC voltage U_{in_max} = 1.21 p.u. = 4 kV DC;
- rated power of the converter P= 1.0 p.u. = 50 kW.

One of the major differences between the half-bridge and full-bridge inverter topologies is the amplitude value of the isolation transformer primary voltage. Output voltage of HB is only half of the input voltage but the current amplitude flowing through the tranistors is two times higher (Figure 40). Thus the turns ratio, voltage and current rating of isolation transformer primary winding must comply to the inverter topology that is used [80]. Collector current amplitude value of one transistor ($I_{Cpeak,HB}$ for the HB inverter and $I_{Cpeak,FB}$ for the FB inverter) is expressed as follows:

$$I_{Cpeak,FB} = \frac{P}{U_{in}} \cdot \frac{1}{D_{\max}} = 2.0\,p.u. \tag{8}$$

$$I_{Cpeak,HB} = \frac{2 \cdot P}{U_{in}} \cdot \frac{1}{D_{\max}} = 4.0\,p.u. \tag{9}$$

In the single-phase inverter, the maximum allowable duty cycle D_{max} of the switching transistors is 0.5 (50 %) [81]. Average collector current $I_{Cav,FB}$ of one transistor in the FB topology can be calculated as:

$$I_{Cav,FB} = \int_0^{0.5} I_{Cpeak,FB} \times dt = 1\,p.u. \tag{10}$$

Average collector current of one transistor in the HB topology $I_{Cav,HB}$ is:

$$I_{Cav,HB} = \int_0^{0.5} I_{Cpeak,HB} \times dt = 2\,p.u. \tag{11}$$

The RMS value of collector current of one transistor in the HB topology $I_{Cav,FB}$ and in the FB topology $I_{Cav,HB}$ are:

$$I_{Crms,FB} = \left[\int_0^{0.5} (I_{Cpeak,FB})^2 \times dt \right]^{\frac{1}{2}} = 1.4\,p.u. \tag{12}$$

$$I_{Crms,HB} = \left[\int_0^{0.5} (I_{Cpeak,HB})^2 \times dt \right]^{\frac{1}{2}} = 2.8\,p.u. \tag{13}$$

The peak forward voltage in the inverter switch U_{Cpeak} will be equal to 4 kV = 1.21 p.u. Thus, the total inverter switch stress for the HB topology S_{HB} and for the FB topology S_{FB} will be:

$$S_{FB} = S_{HB} = \sum_{k=1}^{n} (I_{Crms,FB,k} \times U_{Cpeak,k}) = 6.7\,p.u, \tag{14}$$

where n is the number of switches. The active switch utilization U_{HB} (converter output power obtained per unit of active switch stress) for the HB topology U_{HB} and for the FB topology U_{FB} will be:

$$U_{FB} = U_{HB} = \frac{P}{S_{FB}} = \frac{P}{S_{HB}} = 0.15. \tag{15}$$

Table 30 gives short comparison of basic properties of HB and FB inverter topologies, obtained from analysis.

Table 30 Side by-side comparison of HB and FB inverter topologies

Parameter	HB topology	FB topology
Input voltage, U_{in} (p.u.)	1.0	1.0
Rated power of the converter, P (p.u.)	1.0	1.0
Peak collector current, I_{Cpeak} (p.u.)	4.0	2.0
Average collector current, I_{Cav} (p.u.)	2.0	1.0
RMS collector current, I_{Crms} (p.u.)	2.8	1.4
Total inverter switch stress, S (p.u.)	6.7	6.7
Active switch utilization, $U_{HB/FB}$ (p.u.)	0.15	0.15

The FB topology in comparison with the HB features lower inverter switches ratings for the same transferred power although the total inverter switch stress remains the same, as shown in Table 30. So the steady state losses and thus the total

power switch losses of one IGBT and a free-wheeling diode are smaller but there are two times more transistors needed in the FB inverter.

3.2.1 Inverter Switch Ratings and Operating Frequency Limiting Factors

Inverter switches have limitations in voltage, current and operating frequency ratings. The operating frequency is limited by the maximum allowable temperature of the semiconductor junction. IGBT junction temperature depends on the semiconductor power loss and the power loss is a function of the collector emitter voltage, transistor collector RMS current, IGBT dynamics and switching frequency. The turn-on and turn-off times are fixed by the resistance of the gate current limiting resistor. Also, the inverter topology influences the limit of switching frequency as in the FB inverter are four and in the HB inverter two IGBTs sharing one common heatsink. The input voltage of FEC can vary between 2.2 kV and 4 kV. The parameters corresponding to boundary point at minimum input voltage are listed in Table 31 and parameters corresponding to maximum input voltage are shown in Table 32. Maximum RMS value of the collector current of the IGBT of the FB inverter in the boundary points $I_{C\_RMS\_max\_FB}$ is calculated as follows:

$$I_{C\_RMS\_max\_FB} = \frac{P}{U_{Tr\_p\_FB}} \cdot \frac{1}{\sqrt{D_{max}}}, \tag{16}$$

where P is the rated power of the FEC, $U_{Tr\_p\_FB}$ is the peak to peak value of the FB inverter output voltage (isolation transformer primary amplitude voltage) and D_{max} is the maximum duty cycle. The maximum RMS value of the collector current of the IGBT of the HB inverter in the boundary points $I_{C\_RMS\_max\_FB}$ is calculated with the following equation:

$$I_{C\_RMS\_max\_HB} = \frac{P}{U_{Tr\_p\_HB}} \cdot \frac{1}{\sqrt{D_{max}}}, \tag{17}$$

where $U_{Tr\_p\_HB}$ is the peak to peak value of the HB inverter output voltage and D_{max} is the duty cycle that corresponds to maximum value of U_{in}.

Table 31 Parameters of the FEC input inverter at minimum input voltage

Parameter	Value
Boundary point 1 (minimum input voltage)	
Minimum input voltage of FEC, U_{in_min} (kV DC)	2.2
Duty cycle corresponding to U_{in}=2.2 kV, D_{max}	0.4
Maximum RMS value of the collector current of the IGBT of the FB inverter corresponding to U_{in}=2.2 kV, $I_{C\_RMS\_max}$ (A)	18
Maximum RMS value of the collector current of the IGBT of the HB inverter corresponding to U_{in}=2.2 kV, $I_{C\_RMS\_max}$ (A)	36
Temperature limit of the IGBT, T_{j_IGBT} (°C)	125
Gate-emitter voltage, (V)	±15
Gate resistor, (Ω)	13

Table 32 Parameters of the FEC input inverter at minimum input voltage

Boundary point 2 (maximum input voltage)	
Maximum input voltage of FEC, $U_{in\ max}$ (kV DC)	4
Duty cycle corresponding to U_{in}=4 kV, D_{min}	0.22
Maximum RMS value of the collector current of the IGBT of the FB inverter corresponding to U_{in}=4 kV, $I_{C\ RMS\ max}$ (A)	13
Maximum RMS value of the collector current of the IGBT of the HB inverter corresponding to U_{in}=4 kV, $I_{C\ RMS\ max}$ (A)	27
Temperature limit of the IGBT, $T_{j\ IGBT}$ (°C)	125
Gate-emitter voltage, (V)	±15
Gate resistor, (Ω)	13

The switching frequency limit is also influenced by the properties of the cooling system used to dissipate the energy loss into the environment. The cooling system used in the calculations was the forced air type heatsink with a thermal resistance of 0.026 K/W per transistor. Ambient temperature was + 50°C. Results of the analysis of switching frequency limit for FZ200R65KF1 6.5 kV IGBT are presented in Figure 41.

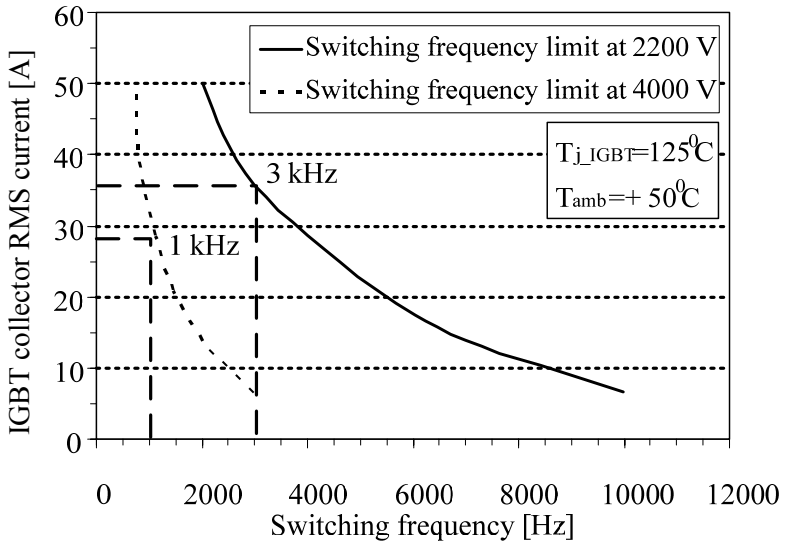


Figure 41 Switching frequency limit of FZ200R65KF1 6.5 kV IGBTs

Figure 41 reveals that the switching frequency limit of the FB inverter for the minimum input voltage is 5.5 kHz and for the maximum input voltage 2 kHz. The characteristics in Figure 41 also shows that the switching frequency limit of the HB inverter for minimum input voltage is 3 kHz and for maximum input voltage 1 kHz. The converter would be running on its thermal limits at the boundary voltage of 4 kV DC but the possibility to operate simultaneously at the maximum voltage 4 kV DC, maximum ambient temperature (+50 °C) and at the maximum output power of 50 kW over longer periods is low (Figure 5). Therefore, it is suitable to

use the switching frequency of 1 kHz. Although the maximum allowable current for FZ200R65KF1 is 200 A, the RMS current for half- and full-bridge inverter configurations is limited (Table 31). The switching frequency could further be raised by using a more powerful cooling system, IGBTs with better dynamic properties or a different input inverter topology.

3.2.2 Transformer Parameters and Limiting Factors

The most important isolation transformer parameters and limiting factors are: switching frequency, core volume, turns ratio, primary and secondary voltages and currents. RMS values of the transformer primary current $I_{\mathrm{Tr\_p\_rms}}$ and voltage $U_{\mathrm{Tr\_p\_rms}}$ are defined by:

$$U_{Tr\_p\_rms} = U_{Tr\_p\_amp} \cdot \sqrt{\frac{t_{on}}{T_{sw}}} = U_{Tr\_p\_amp} \cdot \sqrt{2 \cdot D_{\max}} = U_{Tr\_p} \sqrt{0.8}, \tag{18}$$

$$I_{Tr\_p\_rms} = I_{Tr\_p\_amp} \cdot \sqrt{\frac{t_{on}}{T_{sw}}} = I_{Tr\_p\_amp} \cdot \sqrt{2 \cdot D_{\max}} = I_{Tr\_p} \sqrt{0.8}, \tag{19}$$

where $U_{\mathrm{Tr\_p\_amp}}$ is the amplitude value of the transformer primary voltage, $I_{\mathrm{Tr\_p}}$ is the amplitude value of transformer primary current (equal with the amplitude value of single IGBT collector current), D is duty-cycle, t_{on} is the impulse duration, T_{sw} is the duration of the period. Secondary voltage amplitude $U_{\mathrm{Tr\_s\_amp}}$ of the isolation transformer is defined by the required output voltage U_{out} (350 V DC), maximum turn-on time and duration of the period:

$$U_{Tr\_s\_amp} = \frac{U_{out}}{\frac{t_{on}}{T_{sw}}} = \frac{U_{out}}{2 \cdot D_{\max}} = \frac{U_{out}}{0.8}. \tag{20}$$

As the output voltage of FB and HB topologies is different, also the transformer parameters for the corresponding topology are different. All parameters are calculated in the minimum input voltage boundary point at the hardest working conditions for the isolation transformer (U_{in} = 2.2 kV DC and $2 \cdot D_{\max}$ = 0.8). Limiting factors and parameters of the isolation transformer are listed in Table 33. As we can see in Table 33, the primary voltage for the isolation transformer is two times lower in the case of the HB inverter but the current is two times higher. When the HB inverter is used the turns ratio of the isolation transformer is lower (2.5:1) as the voltage needs less lowering than with the FB inverter (turns ratio 5:1). Also, lower primary voltage means simpler transformer construction and cheaper isolation materials. The main disadvantage of the low primary voltage is higher copper losses in the primary winding of the isolation transformer, as the primary current must be higher for the same transferred power.

Table 33 Isolation transformer parameters

Parameter	Value
Isolation transformer parameters with an FB inverter	
Transformer primary RMS voltage, $U_{\text{Tr\_p\_rms}}$ (kV)	1.9
Transformer primary amplitude voltage, $U_{\text{Tr\_p\_amp}}$ (kV)	2.2
Transformer secondary RMS voltage, $U_{\text{Tr\_s\_rms}}$ (V)	392
Transformer secondary amplitude voltage, $U_{\text{Tr\_s}}$ (V)	438
Transformer primary RMS current, I_{Tr_p} (A)	25
Transformer secondary RMS current, I_{Tr_s} (A)	102
Frequency, f_{sw} (Hz)	1000
Turns ratio	5:1
Isolation transformer parameters with an HB inverter	
Transformer primary RMS voltage, $U_{\text{Tr\_p\_rms}}$ (V)	984
Transformer primary amplitude voltage, $U_{\text{Tr\_p\_amp}}$ (V)	1.1
Transformer secondary RMS voltage, $U_{\text{Tr\_s\_rms}}$ (V)	392
Transformer secondary amplitude voltage, $U_{\text{Tr\_s}}$ (V)	438
Transformer primary RMS current, $I_{\text{Tr\_p}}$ (A)	50
Transformer secondary RMS current, $I_{\text{Tr\_s}}$ (A)	102
Frequency, f_{sw} (Hz)	1000
Turns ratio	2.5:1

Transformer core volume depends on the switching frequency and properties of the selected core material:

$$V_m = 1.5\sqrt{\frac{A \cdot k_{ADD} \cdot k_T}{k_U}} \cdot \frac{P_{tr}}{f^{\frac{1}{4}} \cdot \Delta T_{tr}}, \tag{21}$$

where P_{tr} is the transformer rated power, k_{T} is the temperature coefficient of winding resistance, k_{U} is the window utilization factor, k_{ADD} is the added losses factor (increase of winding resistance with the frequency due to skin and proximity effects), ΔT_{tr} is the transformer temperature rise. Parameters of the core volume of the isolation transformer were: core material GM14DC, temperature rise 50°C, flux density 0.4 T and window utilization factor 0.25.

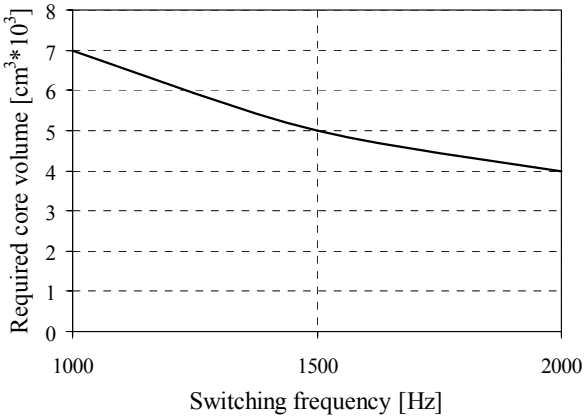


Figure 42 Minimal required core volume as a function of operating frequency for the isolation transformer with the GM14DC magnetic core

Figure 42 shows that the isolation transformer requires a magnetic core with 7000 cm^3 volume when the switching frequency 1 kHz is used. Required magnetic core volume could be reduced by 50 % when a switching frequency of 2 kHz will be implemented.

3.2.3 Analysis of Transformer Magnetic Core Saturation Reasons and Elaboration of Saturation Avoidance Methods

In the isolated DC/DC converters with a wide input voltage and load variations with the increase of the input voltage, the on-state time (pulse width) of the switch will normally decrease at the same ratio to maintain the output voltage constant. Under these conditions the peak flux density of the isolation transformer core remains constant at some certain designed value. However, under several transient conditions (rapid load changes, unstable supply from the contact line, etc.) it is possible for the pulse width to increase to its maximum irrespective of the input voltage. This can occur at maximum input voltage. The increase in the flux density at maximum input voltage will follow the same ratio as the increase in voltage. The operating flux density would abruptly increase to 30...50% from the predefined value, thus overcoming the saturation limit [68].

In this thesis a conservative design practice is used. The initial value of the operating flux density selected was 0.35 T. The core volume required to meet power demands and temperature rise for the selected operating frequency was $6.4 \cdot 10^3$ cm^3. To calculate the true operating flux density of the designed transformer following equation should be used:

$$B_{mtr} = 0.156 \cdot \frac{\sqrt{P_I}}{A^{\frac{1}{4}} \cdot f_I^{\frac{7}{8}} \cdot V_m^{\frac{1}{3}}} = 0.156 \cdot \frac{\sqrt{\frac{U_{1Irms}^2}{R_L'}}}{A^{\frac{1}{4}} \cdot f_I^{\frac{7}{8}} \cdot V_m^{\frac{1}{3}}}, \tag{22}$$

where P_1 is the transformer power at fundamental frequency f_1. After the Fourier transformation of the waveshape presented in Fig. 2, the amplitude value of the primary voltage at the fundamental frequency could be expressed as

$$U_{1Ia} = \left(\frac{4}{\pi}\right) \cdot U_{1a} \cdot \sin \pi \cdot \frac{t_{on}}{T_{sw}}. \tag{23}$$

The rms value of the voltage at the fundamental frequency is

$$U_{1Irms} = \frac{U_{1a}}{\sqrt{2}}. \tag{24}$$

Thus, the recalculated values of true operating flux densities for the minimum and maximum supply voltages of the isolation transformer in the current application will be 0.5 T and 0.47 T, respectively. Such conservative design with reduced values of operating flux densities leads up to 10% increased core volume; on the other hand, it could prevent transformer saturation in occasional transients [68].

Figure 43 shows the simulation results of transistor on-state time sudden increase irrespectable of the operating voltage at the maximum input voltage of the converter. Such trouble may occur, for example, due to the EMI impact on control logics and/or signal wires and finally could result in the operating flux density of the transformer core exceeding the saturation level (saturation magnetic induction B_{sat}=0.8 T), especially in the case of higher values of initial flux density B_m. Another threat connected to the converters with wide input voltage variations, which can easily put the transformer core into the saturation, is the transient overvoltage spikes occurring at the minimum input voltage of the converter. At the minimum input voltage the pulse width will be maximal to maintain the full output power of the converter and in the case of 50% transient voltage spike, the operating flux density of the magnetic core will easily exceed the saturation level (Figure 44).

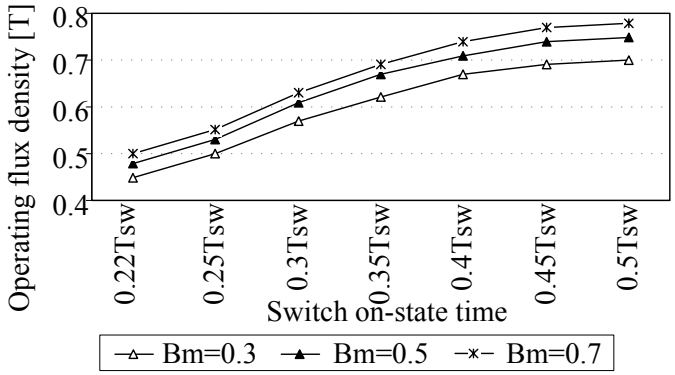


Figure 43 Rise of the true operating flux density of the 50 kW isolation transformer with GM14DC magnetic core caused by an undesired increase of pulse width at maximum operating voltage conditions simulated for different initial flux densities

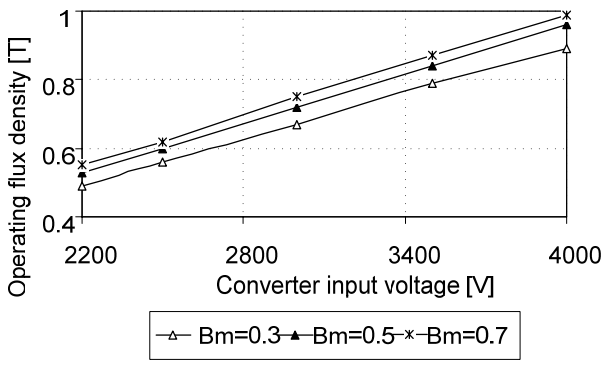


Figure 44 Rise of the true operating flux density of the 50 kW isolation transformer with GM14DC magnetic core caused by transient voltage spikes occurring at minimum operating voltage conditions

For the saturation prevention, the isolation transformer for such applications must be designed for a lower flux level. However, such conservative design approach results in a lower-efficiency transformer because more turns are required (Figure 45).

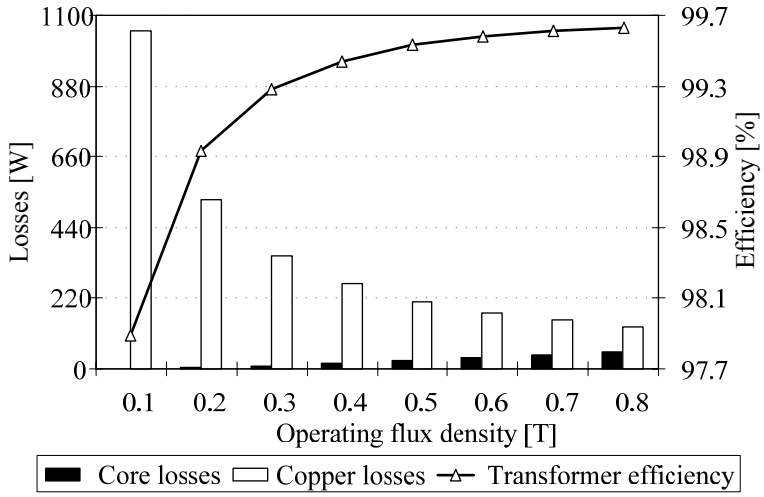
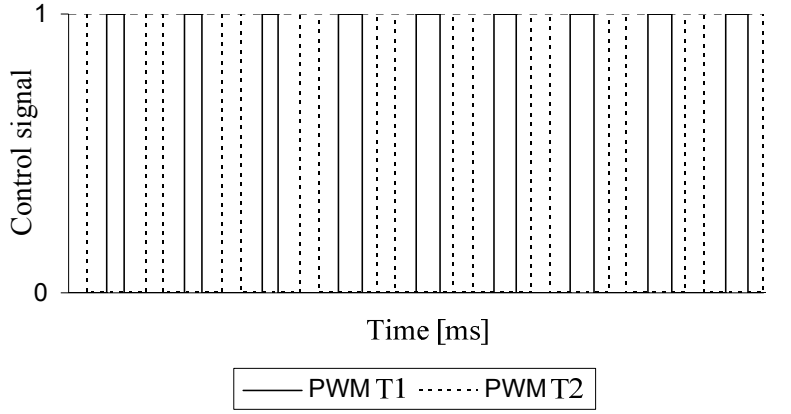


Figure 451 kHz 50 kW isolation transformer losses and efficiency as a function of operating flux density

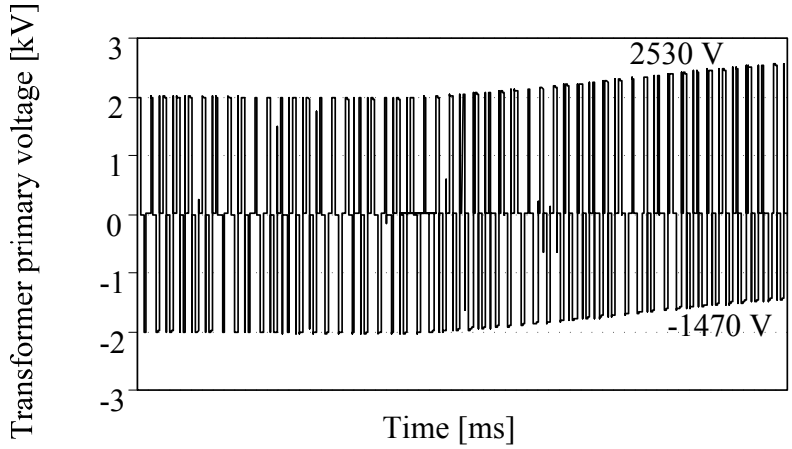
Another issue to be taken into account during the design procedure is that the operating flux excursion ΔB in a non-ideal case may not always be $2B$ [68]. Thus, during the converter turn-on the operation point of the core flux density is normally lies between two remanent flux values. Hence, for the first half-cycle, the flux doubling effect could occur, i.e. a flux change of $2B$ may take the core into saturation.

The isolation transformer core saturation will also occur in a half-bridge converter due to the mid-voltage point shift (center-point shift), which could be caused by the differences in the on-state times (duty ratios) of the top (T1) and bottom (T2)

switching transistors. The on-state time differences can result from differences in the time delays in the top and bottom control channels, from load current pulsation at an even subharmonic of the switching frequency, or from the subharmonic oscillation of the system. The latter, in turn, can result from switching-ripple feedback or from switching-noise pickup in the controller. Constant-frequency peak-current control is particularly inclined to produce subharmonic oscillations, though converters using other types of current-mode control or converters using single loop PWM control can also produce subharmonic oscillation [68].



(a)



(b)

Figure 46 Demonstration of 40% differences of the control pulse widths of switching transistors (a) and the resulting center-point voltage shift with 26% unbalance of positive and negative half-waves of transformer primary voltage (b)

Figure 47 demonstrates further simulation results on control signal inequality, which in the case of 20% difference leads to a 13% center-point shift (a) and in the case of 100% difference leads to harmful 58% center-point shift (b). Figure 48 shows the true operating flux density rise of the 50 kW isolation transformer with GM14DC magnetic core caused by the differences in the on-state times of switching transistors

simulated for different initial flux densities.

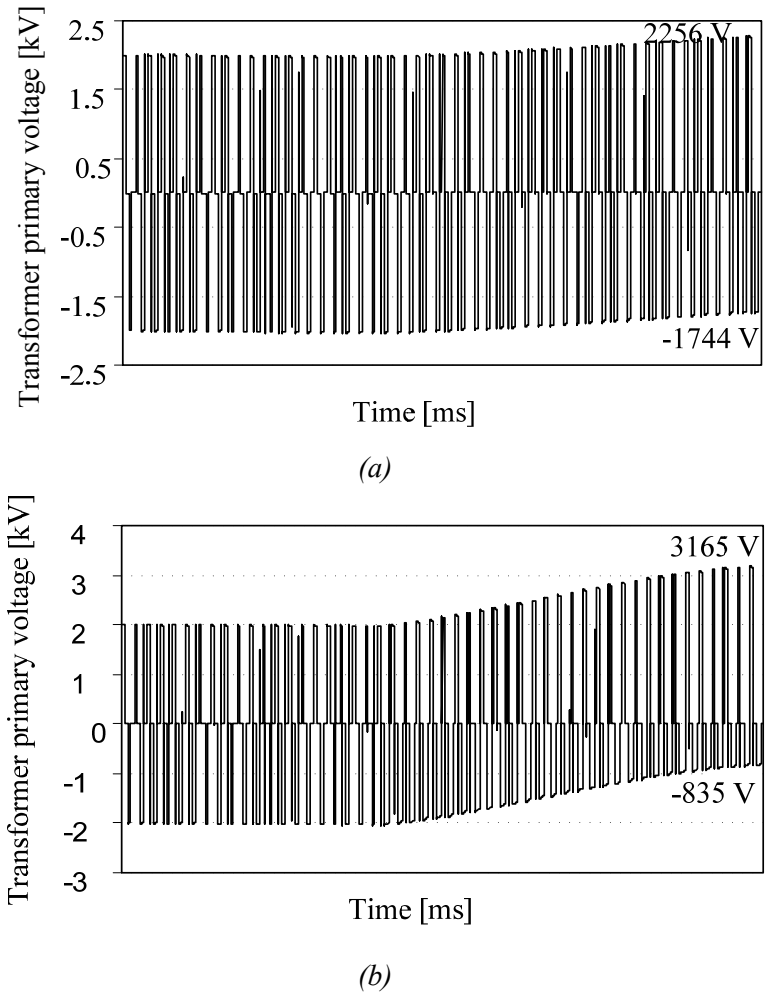


Figure 47 Impact of differences in the on-state times of switching transistors on the primary voltage of the isolation transformer: 20% difference leads to 13% center-point shift (a) and 100% difference leads to 58% center-point shift (b)

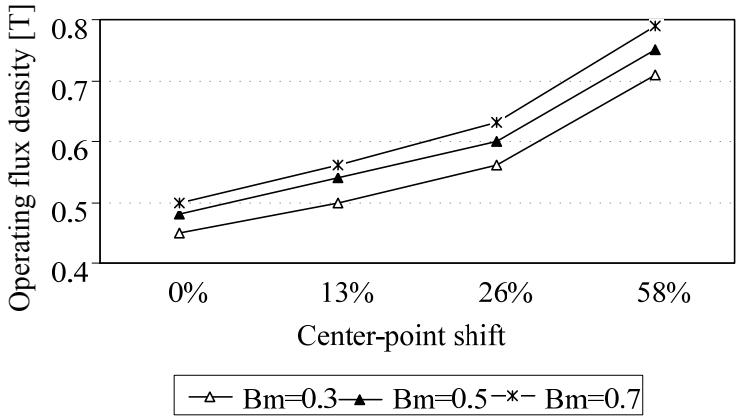


Figure 48 True operating flux density of the 50 kW isolation transformer with GM14DC magnetic core vs. differences in the on-state times of switching transistors for different initial flux densities

The solution to the core saturation problems is to reduce the operating flux range ΔB and use more turns in the primary winding in order to provide a good working margin. The margin required depends on how well the above effects have been controlled.

3.2.4 Mechanical Constraints and Evaluative Price Comparison of Different Two-Level Inverter Topologies

Technical and economical feasibility are factors that often can not be overlooked by the designer of power electronics devices. Figure 49 analyzes the minimum installation surface area and inverter detail volume for different investigated topologies.

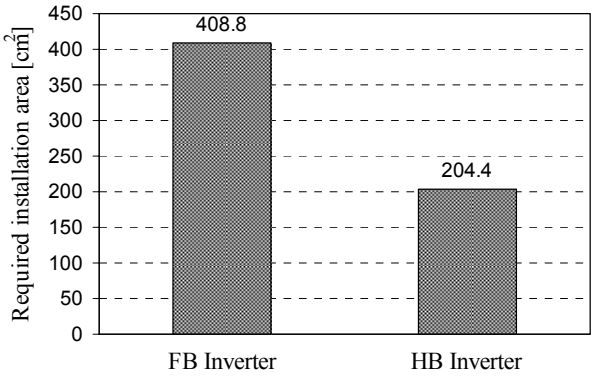


Figure 49 Installation area requirement for half- and full-bridge inverter components

As indicated in Figure 49 the required surface area for the HB inverter is only 50 % of the FB inverter as there are only two IGBTs needed but the volume of the

converter with the HB inverter is 20 times larger, because of the clumsy DC-link capacitors (Figure 50).

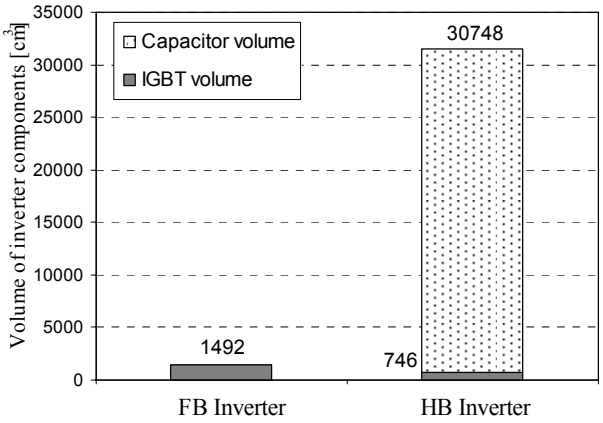


Figure 50 Volume of full- and half-bridge inverter components

The current amplitude value of one transistor in the FB inverter is two times lower than in the HB inverter with a comparable output power.Therefore, there is a theoretical possibility to use cheaper and smaller IGBTs with lower current rating but today only 200 A 6.5 kV IGBT modules are available and this economical advanatge of the FB design is lost. Also the HB design has its downsides, as large and bulky capacitors are needed, although the price of the HB inverter with high-voltage capacitors is 15 % lower than the price of the FB inverter. If the allowable ripple factor at full power is higher, smaller capacitors could be used and the price difference can be even higher. Figure 51 presents the price comparison between the HB- and FB inverter topologies.

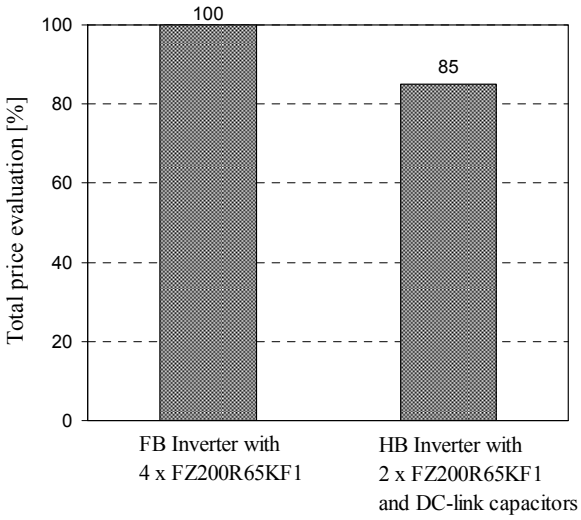


Figure 51 Price comparison of FB and HB inverters

The need for bulky DC-link capacitors in the HB inverter is somewhat compensated by the smaller required installation area of two 6.5 kV IGBTs and therefore smaller heatsink. The FB inverter would be economically feasible when the cheaper IGBTs with lower current rating were available, as the cost of the inverter is more than 50 % of the whole cost of the whole converter, including the isolation transformer, the output rectifier with the filter and the control system. The HB inverter is somewhat bulkier but cheaper. Also, the control system of the HB inverter is simpler and cheaper as there is no need for additional two control channels and IGBT driver circuits. As the output voltage of the HB inverter is only ½ of the input voltage isolation transformer construction is simpler. That allows the use of cheaper isolation materials in the transformer primary windings although the current rating of the primary winding is higher. All of those factors lead to the conclusion that the best inverter topology for the FEC input inverter is the two-level half-bridge topology.

3.3 Design and Development of FEC Based Two-Level Half-Bridge Topology with 6.5 kV IGBTs

The FEC of the auxiliary power supply can be realized by using a half-bridge two-level inverter with 6.5 kV IGBTs. The isolation transformer of FEC can be with a toroidal iron powder core. For the output stage of FEC a full-bridge rectifier with fast recovery epitaxial diodes is suitable.

3.3.1 Steady State Analysis of FEC With Two-Level Half-Bridge Inverter

A two-level inverter has four basic cycles: the working cycle of the top IGBT T1, the freewheeling cycle when internal freewheeling diode D2 of the bottom IGBT module T2 is active, the working cycle of the bottom IGBT T2 and the freewheeling cycle when the internal freewheeling diode D1 of the top IGBT module T1 is active. In Figure 52 and Figure 53 the working and freewheeling cycles of the FEC inverter are shown.

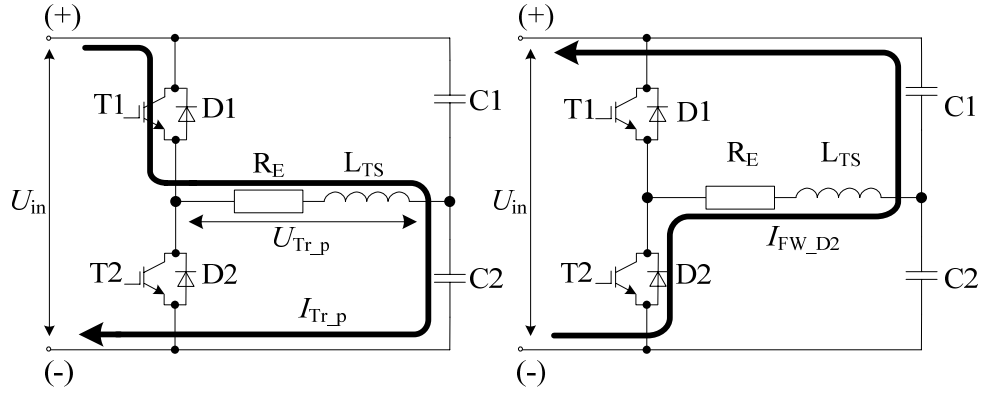


Figure 52 Active cycle of T1 (a) and freewheeling cycle of D2 (b)

Figure 52 (a) shows the active cycle of the top IGBT T1 and Figure 52 (b) the following freewheeling cycle through the diode D2. Figure 53 (a) shows the next active cycle of the bottom IGBT T2 and Figure 53 (b) the freewheeling cycle through the diode D1.

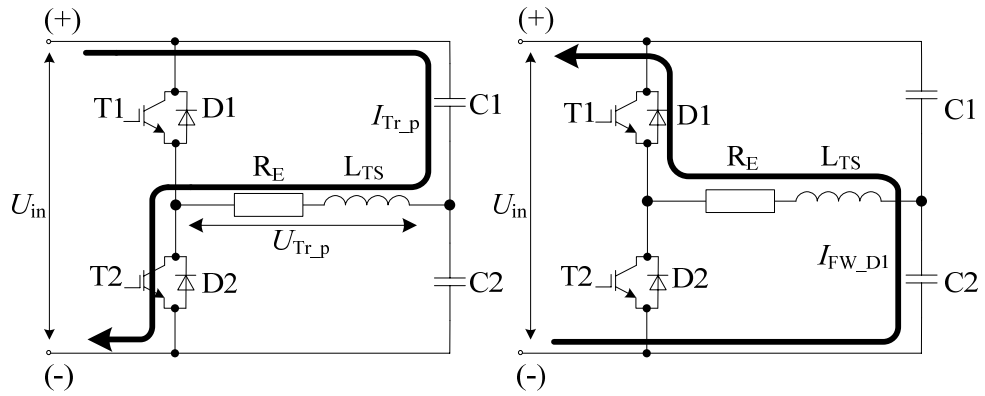


Figure 53 Active cycle of T2 (a) and freewheeling cycle of D1 (b)

For a steady state analyis of FEC, a simplified equivalent schematic is used as it can be seen in Figure 54. In the steady state analysis the working cycles are investigated.

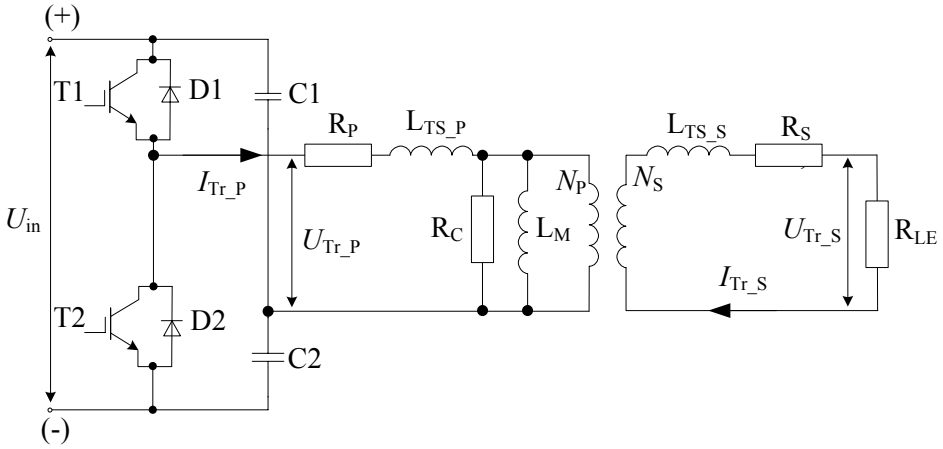


Figure 54 simplified equivalent schematic of FEC

Voltage drop in capacitors C1, C2 and in wiring along with the parasitic inductance of the busbar system is neglected. To represent the isolation transformer, a T-shaped equivalent circuit is used. The output filter and load are replaced by an equivalent load resistance R_{LE}:

$$R_{LE} = \frac{U_{Tr\_s\_rms}^2}{P} + R_{LO} + 2 \cdot I_{Tr\_s\_rms} \cdot U_{F\_RD}, \tag{25}$$

where $U_{Tr\_s\_rms}$ is the RMS value of the transformer secondary voltage, P rated power of the FEC, R_{LO} is the active resistance of the output inductor and U_{F_RD} is

the forward voltage drop of the output rectifier diode and $I_{\mathrm{Tr\_s\_rms}}$ is the RMS value of the transformer secondary current. $U_{\mathrm{Tr\_s\_rms}}$ is calculated by:

$$U_{Tr\_s\_rms} = \frac{U_{in}}{2} \cdot \frac{N_S}{N_P} \cdot \sqrt{2 \cdot D}, \tag{26}$$

where U_{in} is the input voltage of FEC, N_{p} is the primary turns number of the isolation transformer, N_{s} is the secondary turns number of the isolation transformer and D is the duty cycle.
Half-bridge capacitors C1 and C2 form a capacitive voltage divider, so that voltage across C1 and C2 terminals is half of the FEC input voltage.

$$U_{C1} = U_{C2} = \frac{U_{in}}{2}. \tag{27}$$

Maximum voltage between the collector and the emitter of both IGBTs ($U_{\mathrm{T1\_CE\_amp}}$ and $U_{\mathrm{T2\_CE\_amp}}$ respectively) is equal to the FEC input voltage requiring the use of 6.5 kV IGBTs.

$$U_{T1\_CE\_amp} = U_{T2\_CE\_amp} = U_{in}. \tag{28}$$

As the used inverter has the two-level half-bridge topology, the isolation transformer primary voltage $U_{\mathrm{Tr\_p\_amp}}$ is two times lower than the FEC input voltage:

$$U_{Tr\_p\_amp} = \frac{U_{in}}{2} - U_{F\_IGBT}, \tag{29}$$

where $U_{\mathrm{F\_IGBT}}$ is the forward voltage drop of the IGBT transistor. The primary current amplitude value of the isolation transformer $I_{\mathrm{Tr\_p\_amp}}$ is equal to the collector current amplitude value of both IGBTs T1, T2 ($I_{\mathrm{C\_T1\_amp}}$, $I_{\mathrm{C\_T2\_amp}}$) and the amplitude value of the half-bridge capacitor currents C1 and C2 $I_{\mathrm{C1\_amp}}$, $I_{\mathrm{C2\_amp}}$.

$$I_{Tr\_p\_amp} = I_{C\_T1\_amp} = I_{C\_T2\_amp} = I_{C1} = I_{C2}. \tag{30}$$

The primary current amplitude value of the isolation transformer $I_{\mathrm{Tr\_p\_amp}}$ can be calculated by reducing the transformer and equivalent load R_{LE} to one equivalent load resistance in the following equation:

$$I_{Tr\_p\_amp} = \frac{U_{Trp\_amp} - U_{F\_IGBT}}{R_{EKV}}, \tag{31}$$

$$R_{EKV} = R_P + Z_P + \frac{1}{\frac{1}{R_C} + \frac{1}{Z_M} + \frac{1}{(\frac{N_p}{N_s})^2 \cdot (R_S + Z_S + R_{LE})}}, \tag{32}$$

where R_{p} is the active resistance of the isolation transformer primary winding, R_{S} is the active resistance of the isolation transformer secondary winding, R_{C} is the magnetic resistance of the core material, Z_{p} is the impedance of the isolation

transformer primary winding, Z_S is the impedance of the isolation transformer secondary winding, Z_m is the magnetic impedance of the transformer core material.

Impedances in the isolation transformer can be defined by the stray inductance of the primary winding L_{TS_P}, the stray inductance of the secondary winding L_{TS_S}, main inductance of the isolation transformer L_M and switching frequency f_{sw}.

$$Z_P = 2 \cdot \pi \cdot f_{sw} \cdot L_{TS\_P}, \tag{33}$$

$$Z_M = 2 \cdot \pi \cdot f_{sw} \cdot L_M, \tag{34}$$

$$Z_S = 2 \cdot \pi \cdot f_{sw} \cdot L_{TS\_S}. \tag{35}$$

Then R_{EKV} equals:

$$R_{EKV} = R_P + 2 \cdot \pi \cdot f_{sw} \cdot L_{TS\_P} + \frac{1}{\frac{1}{R_C} + \frac{1}{2 \cdot \pi \cdot f_{sw} \cdot L_M} + \frac{1}{(\frac{N_p}{N_s})^2 \cdot (R_S + 2 \cdot \pi \cdot f_{sw} \cdot L_{TS\_S} + R_{LE})}}. \tag{36}$$

When combining the equations of $I_{Tr\_p\_amp}$ and R_{EKV} the primary current amplitude value of the isolation transformer $I_{Tr\_p\_amp}$ (the transfer function of FEC) can be calculated by:

$$I_{Tr\_p\_amp} = \frac{U_{Tr\_P} - U_{F\_IGBT}}{R_P + 2 \cdot \pi \cdot f_{sw} \cdot L_{TS\_P} + \frac{1}{\frac{1}{R_C} + \frac{1}{2 \cdot \pi \cdot f_{sw} \cdot L_M} + \frac{1}{(\frac{N_p}{N_s})^2 \cdot (R_S + 2 \cdot \pi \cdot f_{sw} \cdot L_{TS\_S} + R_{LE})}}}. \tag{37}$$

The idealized voltage and current waveforms of the FEC primary side can be seen in Figure 55 (a).

The secondary circuit of FEC consists of the full-bridge rectifier (diodes D1, D2, D3, D4), filter inductance L_O and filter capacitor C_O (Figure 56). The rectifier diodes have forward voltage drop U_{F_RD} . The output capacitor is assumed to be fully charged, so that the current $I_{CO} = 0$ and the output current is affected only by output inductor active resistance R_{LO} and voltage drop of rectifier diodes. The resistance, inductance and capacitance of the FEC output circuit is neglected.

FEC output current I_{out} is derived by dividing the rated power of the FEC P with the output voltage U_{out} :

$$I_{out} = \frac{P}{U_{out}}. \tag{38}$$

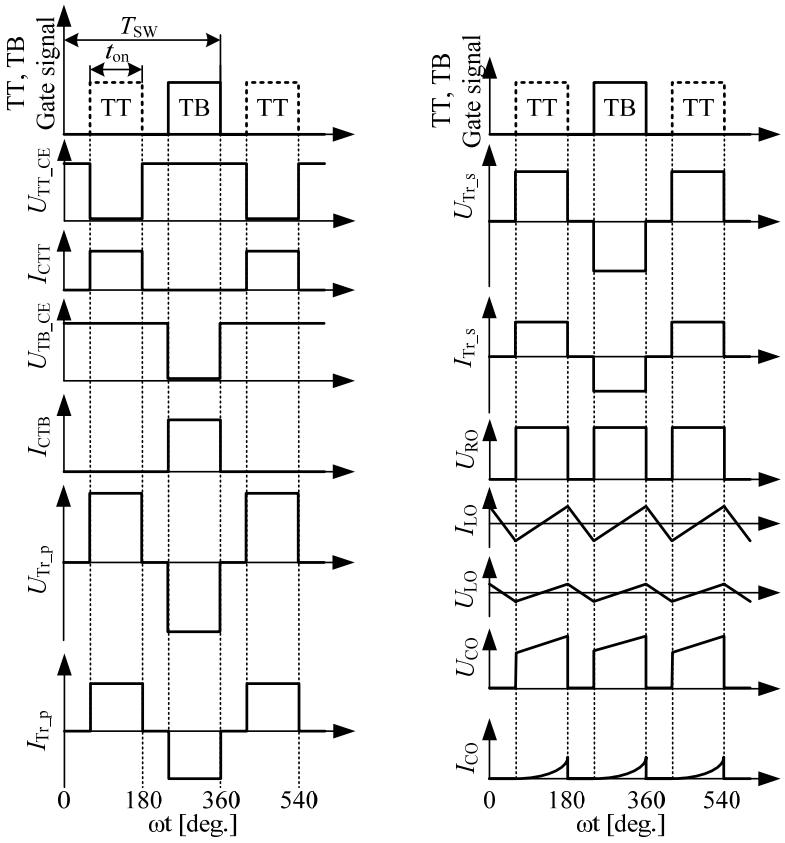


Figure 55 Idealized voltage and current waveforms of FEC primary side (a) and secondary side (b)

Amplitude value of the isolation transformer secondary current $I_{\text{Tr\_s\_amp}}$ is calculated as follows:

$$I_{Tr\_s\_amp} = I_{out} \cdot \frac{1}{\sqrt{2 \cdot D}} = \frac{P}{U_{out}} \cdot \frac{1}{\sqrt{2 \cdot D}} \tag{39}$$

The amplitude value of the isolation transformer secondary voltage $U_{\text{Tr\_s\_amp}}$ is affected by the transformer primary and secondary voltage drops, output filter inductor voltage drop, and the rectifier diode forward voltage drop. As the current is flowing through two diodes in the full-bridge rectifier the voltage drop is doubled.

$$U_{Tr\_s\_amp} = (U_{Tr\_p\_amp} - I_{Tr\_p\_amp} \cdot R_P) \cdot \frac{N_s}{N_p} - I_{Tr\_s} \cdot R_S - I_{Tr\_s} \cdot R_{LO} - U_{F\_RD} \cdot 2, \tag{40}$$

where voltage drop at the output inductor active resistance is calculated as follows:

$$U_{LO} = I_{LO} \cdot R_{LO}. \tag{41}$$

The idealized voltage and current waveforms of the FEC secondary side can be seen in Figure 55 (b).

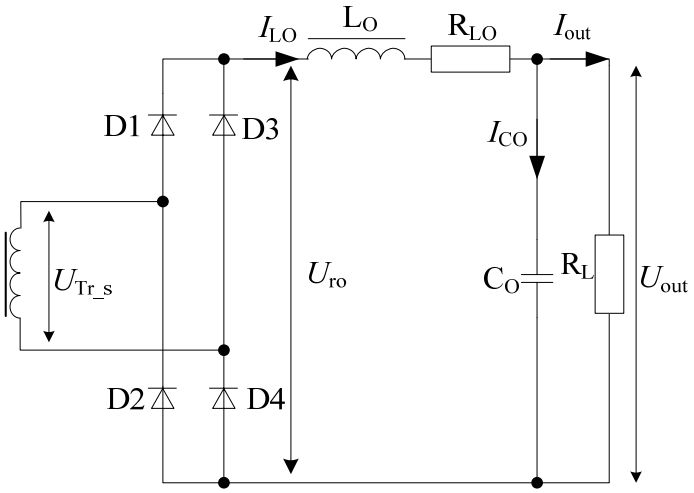


Figure 56 Equivalent schematics of FEC output stage

Output filter operation by keeping the output voltage and current ripple at required bounadaries is described in Section 3.3.4 “Modular rectifier-filter assembly“.

3.3.2 Development of 6.5 kV IGBT Based Half-Bridge DC/DC Converter

To verify the mathematical analysis results a 50 kW laboratory prototype was constructed in the Department of Electrical Drives and Power Electronics of Tallinn University of Technology (Figure 57).

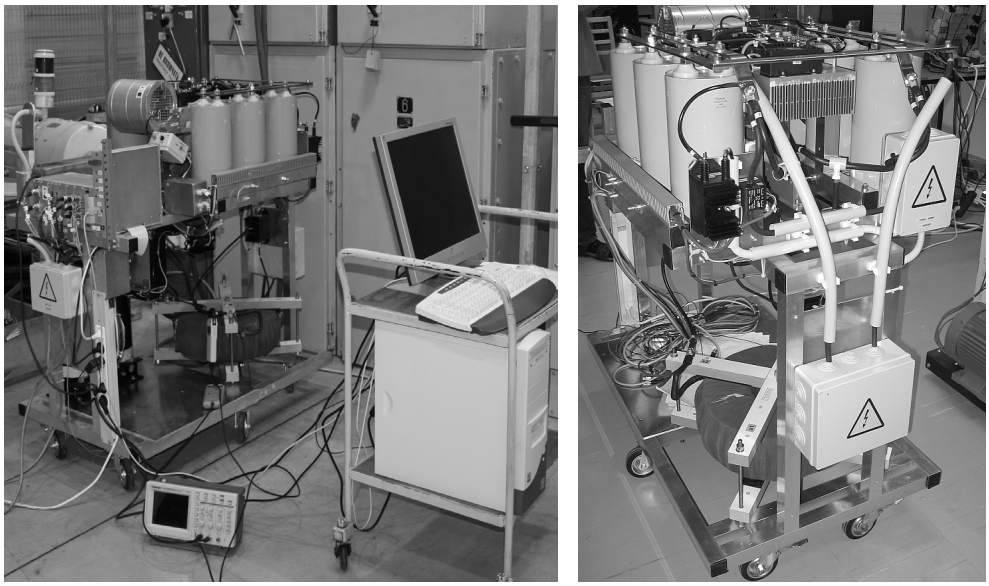


Figure 57 Laboratory prototype of 6.5 kV IGBT based half-bridge DC/DC converter

Schematics of laboratory prototype of 6.5 kV IGBT based half-bridge DC/DC converter is shown in Figure 58.

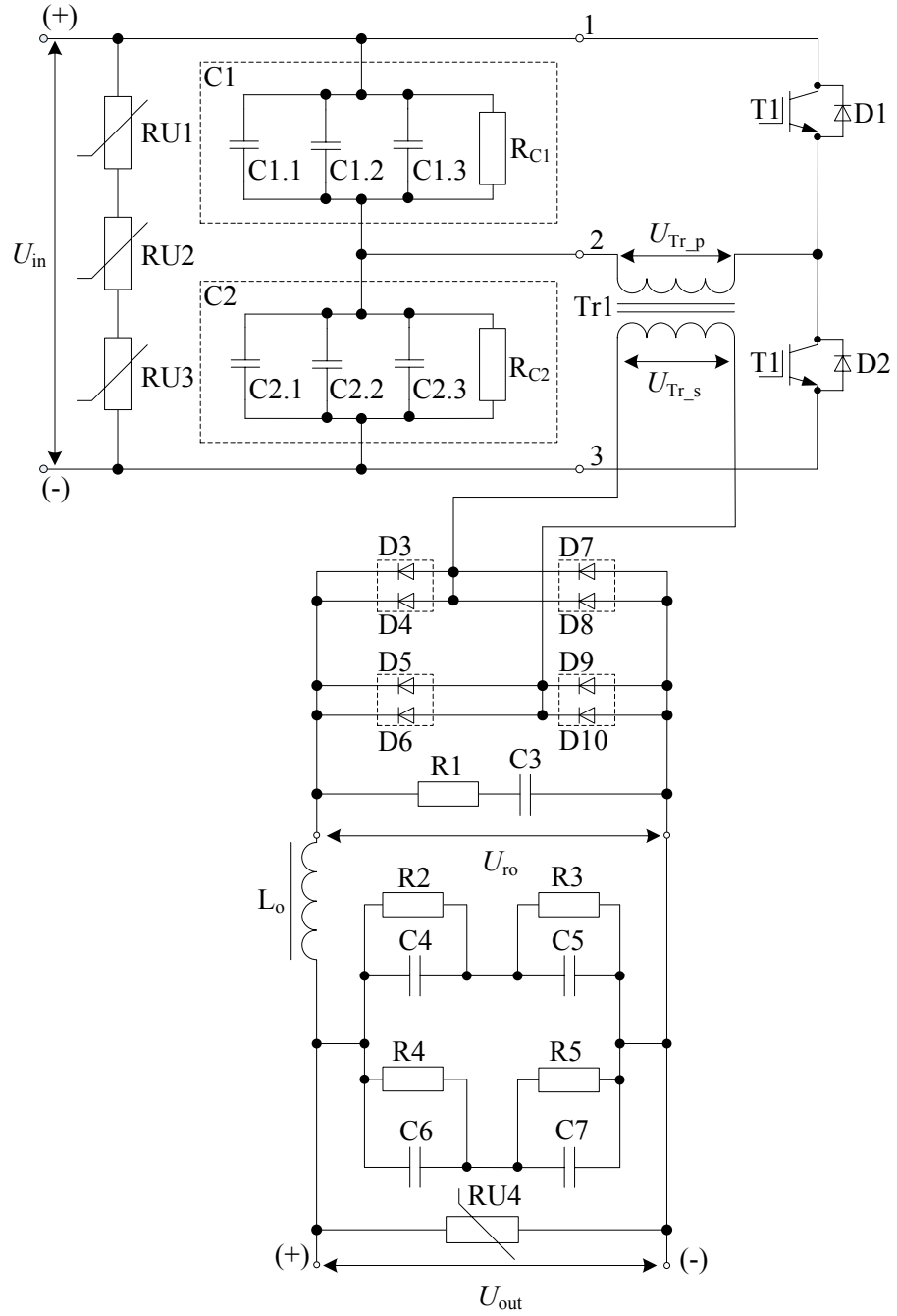
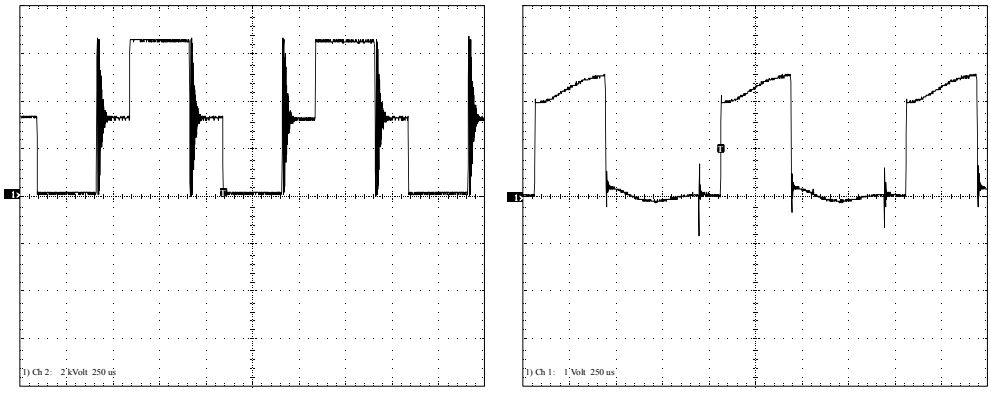


Figure 58 Schematics of laboratory prototype of 6.5 kV IGBT based half-bridge DC/DC converter

High-voltage half-bridge inverter and input filter assembly

The input inverter of FEC has the two-level half-bridge topology and is based on 6.5 kV 200 A FZ200R65KF1 Infineon IGBT modules with built-in freewheeling diodes. In Figure 59 the resulting collector-emitter and collector current waveforms of IGBT T1 are shown.



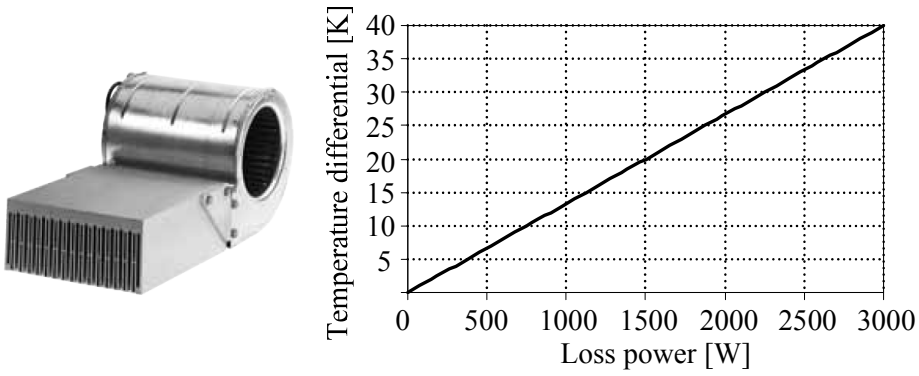
(a) *(b)*

Figure 59 IGBT T1 collector-emitter voltage U_{CET1} (2 kV/ div, 250 µs/ div) and IGBT T1 collector current I_{CT1} (10 A/ div, 250 µs/ div) vaweform

To dissipate the heat generated by combined power losses, in junctions of both IGBTs and FWDs, a forced air cooling system is used. As the estimated maximum power loss of the input inverter of FEC was 1094 W (Table 34), a cooling system from company Austerlitz Electronics RLS200.25-500 was used.

Table 34 Parameters of the cooling system

Parameter	Value
Expected power loss of the inverter, (W)	1094
Expected power loss of one IGBT module, (W)	547
Expected power loss of IGBT, (W)	505
Expected power loss of FWD, (W)	42
Max. power loss dissipation of the cooling system, (W)	3000
Max. IGBT junction temperature, (°C)	+ 125
Max. outside temperature, (°C)	+ 50



(a) *(b)*

Figure 60 Austerlitz Electronics RLS200.25-500 forced air cooling system

The chosen cooling system could be evaluated using the following equations. The temperature of heatsink T_h is the sum of the ambient temperature T_a and the temperature difference ΔT_{cs}, created by the cooling system at 1094 W loss power (Figure 60 (b)).

$$T_h = T_a + \Delta T_{cs} = 50^0 C + 17^0 C = 67^0 C = 340.15K. \tag{42}$$

The resulting temperature of the IGBT junction at 1 kHz would be:

$$T_{j\_IGBT} = T_h + P_{loss\_IGBT} \cdot R_{thjc\_IGBT} + P_{loss\_diode} \cdot R_{thjc\_diode} + (P_{loss\_IGBT} + P_{loss\_diode}) \cdot R_{thch}) =$$
$$= 340.15K + 505W \cdot 0.033K/W + 42W \cdot 0.063K/W + 547W \cdot 0.016K/W =$$
$$= 368.22K = 95.07^0 C, \tag{43}$$

where R_{thjc_IGBT} is thermal resistance between the transistors semiconductor junction and the transistors case, R_{thjc_diode} is the thermal resistance between the freewheeling diode junction and transistor modules and R_{thch} is the common thermal resistance between the case of the IGBT module and heatsink. 95 °C is securely below the thermal limit allowing a slight increase of the switching frequency. If the experimentally measured power loss is used (Table 41) to evaluate the cooling system, a crystal temperature of 101 °C is calculated. Those values show that the selected cooling system is adequate for even extreme outside temperatures of + 50 °C but the switching frequency is limited to 1 kHz. Higher switching frequencies are allowed when either the outside temperature rating is lowered or more powerful cooling system is used.

As seen from Figure 61 the input inverter of FEC consists of two 6.5 kV IGBT modules that share common heatsink. Transistors are connected with the DC-link capacitors C1 and C2 through copper busbars.

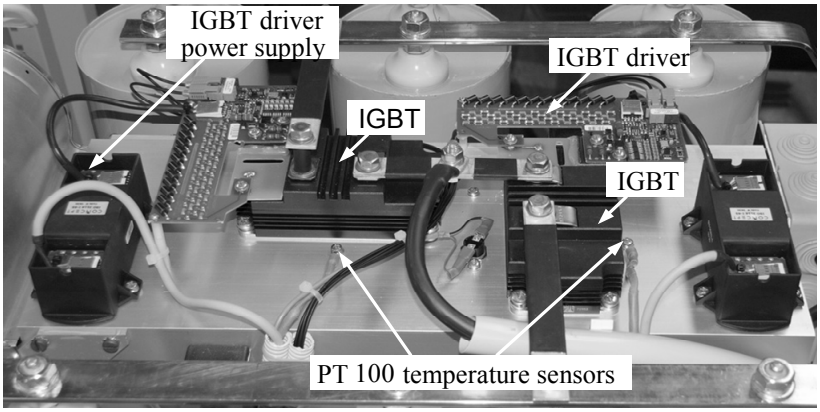


Figure 61 6.5 kV IGBT based half-bridge inverter

IGBTs are driven by plug&play type driver boards 1SD210F2, manufactured by the company CT Concept. Drivers are supplied through galvanically isolated switching power supplies and connected to the control system with a fiber optic link. DC-link capacitors C1 and C2 that are forming the second bridge arm consist of three parallel connected metalized film capacitors ELCOD K-75-80g-4000V.

Input Filter

There is one filter in the input of FEC and one filter in the output to stabilize the auxiliary DC-bus voltage. In the half-bridge topology the input capacitors C1 and C2 are the main reservoir capacitors for the input filter, their midpoint charges up to an average potential of $U_{in}/2$. The value of the required capacitance is calculated from the known primary current and operating frequency. For the rated power of the FEC P (neglecting losses), the average input current I_{in_av} is:

$$I_{in\_av} = \frac{2 \cdot P}{U_{in}}. \tag{44}$$

The voltage change across the capacitors (C1=C2) ΔU_c and for the half-period ($T_{sw}/2$) is then

$$\Delta U_C = \frac{I_{in\_av} \cdot T_{sw}}{C_{tot.} \cdot 2} = \left[\frac{P}{(U_{in}/2) \cdot (C1 + C2)} \right] \cdot \left(\frac{1}{2 \cdot f_{sw}} \right) = \frac{P}{U_{in} \cdot f_{sw} \cdot C_{in}}. \tag{45}$$

Thus

$$C_{in} = C1 = C2 = \frac{P}{\Delta U_c \cdot U_{in} \cdot f_{sw}}. \tag{46}$$

According to the operability requirements, railway converter hardware must be optimized for the different operation points, i.e. for the input voltage range of 2.2 to 4 kV DC. Generally, there is no underestimation of the filtering components accepted. Thus, for the selected switching frequency f_{sw}=1 kHz and accepted voltage ripple of 2 %, the desired input capacitor values for the different operation points are presented in Table 35. Figure 62 demonstrates the acquired input filter capacitor current I_{Ci} and voltage vaweforms.

Table 35 Operation voltage ranges and corresponding input capacitor values

Value	**Parameter** at 2.2 kV DC	**Parameter** at 4 kV DC
Converter input voltage, U_{in} (kV DC)	2.2	4
Duty cycle, $2 \cdot D$	0.8	0.44
Desired input capacitance, C1 and C2 (µF)	260	140

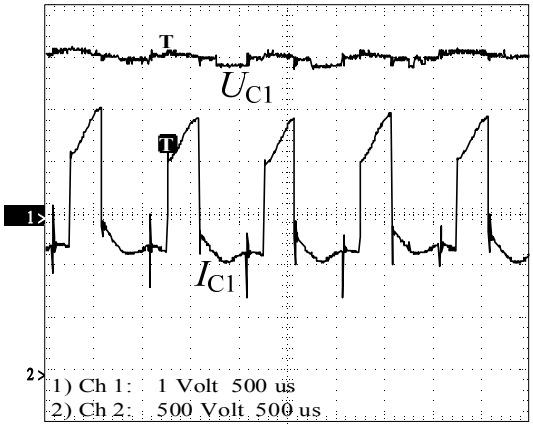


Figure 62 Input filter capacitor voltage U_{C1} (500 V div,/ 500 µs/ div) and current I_{C1} (10 A/ div, 500 µs/ div)

Filtering capacitors C1 and C2 were constructed by connecting three 100 µF ELCOD K-75-80g-4000 film capacitors parallel as shown in Figure 63. The resistors RC1 and RC2 are optional components to provide extra safety to the maintenance staff by emptying the capacitors after the converter is disconnected from the contact line.

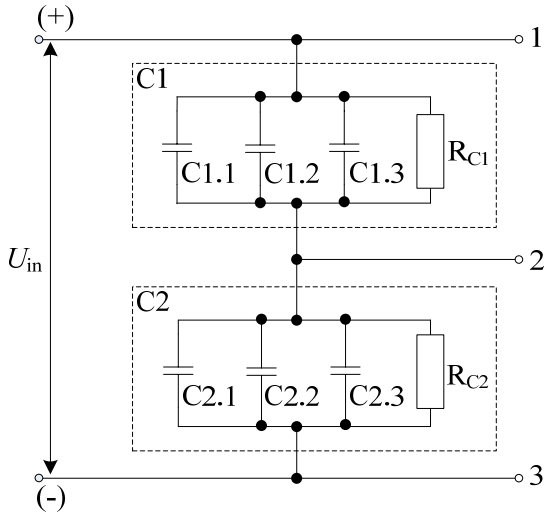


Figure 63 FEC input filter capacitor battery

3.2.3 High-Voltage Toroidal Transformer

Isolation transformer provides voltage transformation and safety isolation between the input and the output of FEC. The transformer is of toroidal type with lightly interleaved windings. Primary winding has 40 turns of wire ЛЄТЛО-20 (120 x 0.5 mm^2 isolated parallel wires). Secondary winding has 18 turns (3 x ЛЄТЛО-20). Isolation between the windings was provided by three layers of isolation foil ЛЄТСАР. Toroidal core of the transformer GM14DC has a diameter of 75 mm. An experimental model of the developed isolation transformer is shown in Figure 64.

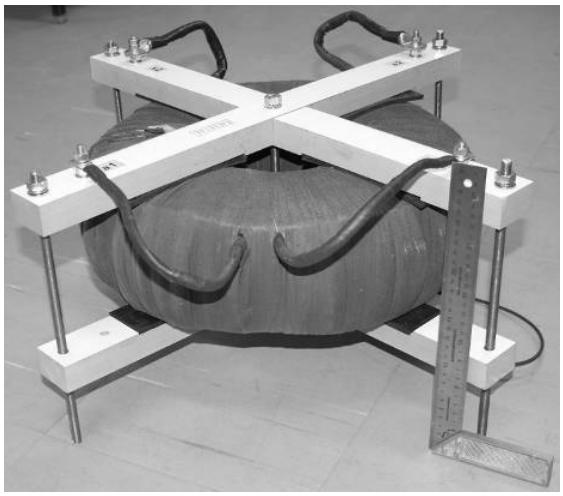
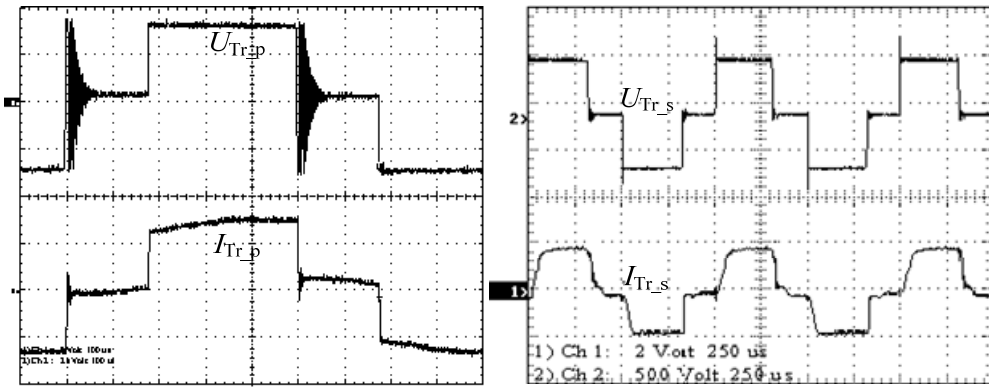


Figure 64 50 kW HV toroidal transformer

Parameters of the isolation transformer are listed in Table 36. Primary and secondary voltage and current of the isolation transformer are shown in Figure 65.



(a) *(b)*

Figure 65 Primary voltage U_{Tr_p} (1 kV/ div, 100 µs/ div) and current I_{Tr_p} (10 A/ div, 100 µs/ div) (a) and secondary U_{Tr_s} (500 V/ div, 250 µs/ div) and current I_{Tr_s} (20 A/ div, 250 µs/ div) of isolation transformer

Table 36 Nominal parameters of the isolation transformer

Parameter	Value
Transformer output power, P_{Tr} (kW)	50
Max. primary amplitude voltage, U_{Tr_p} (kV)	2
Max. seconadary amplitude voltage, U_{Tr_s} (V)	900
Number of primary turns, N_P	40
Number of secondary turns, N_S	18
Nominal frequency, f_{sw} (Hz)	1
Isolation voltage, (kV)	15

3.3.4 Modular Rectifier-Filter Assembly

The most feasible output rectifier topology is the full wave-, full-bridge rectifier. To select diodes for the output rectifier the following values were taken into account: rectifier output voltage $U_{ro,}$ amplitude value of the rectifier input voltage U_{rec}, maximum forward current of one diode I_{FD} and maximum voltage transient at the rectifier diode U_{td} HB converter output voltage can be defined by the following equation [82]:

$$U_{out} = U_{ro} \cdot \frac{2 \cdot t_{on}}{T_{sw}}, \tag{47}$$

Thus, the rectifier output voltage amplitude (U_{ro}) can be estimated as:

$$U_{ro} = U_{out} \cdot \frac{T_{sw}}{2 \cdot t_{on}}. \tag{48}$$

As required by the end-user (Table 5), the converter output voltage must be stabilized at 350 V DC despite the voltage fluctuations on the input side. All the boundary values of the output rectifier are shown in Table 37.

Table 37 Boundary values of output rectifier and selected rectifier diodes

Parameter	Value for 2.2 kV input voltage	Value for 4 kV input voltage
Duty cycle, $2 \cdot D$	0.8	0.44
Rectifier output voltage amplitude value, U_{ro} (V)	438 V	795 V
Rectifier output current amplitude value, (A)	114	63
DSEI2x101-12A diodes		
Maximum forward current, I_{F_rd} (A)	2 x 91	
Recovery time, t_{rr} (ns)	40	
Voltage drop, U_{F_rd} (V)	1.2	
Maximum blocking voltage, U_{B_rd} (kV)	1.2	

Based on the analysis of the data given in Table 37 1.2 kV, HiPerFRED™, DSEI2x101-12A diode modules with two parallel 90 A diodes manufactured by the company IXYS were selected for use in the output rectifier of FEC. The SOT-227B casing (dual diode module) was preferred because of the compactness and reduced parasitic inductance. Insufficient forward current rating of the selected diodes imposes those diodes to be used in parallel configuration. Figure 66 shows the rectifier output voltage and current.

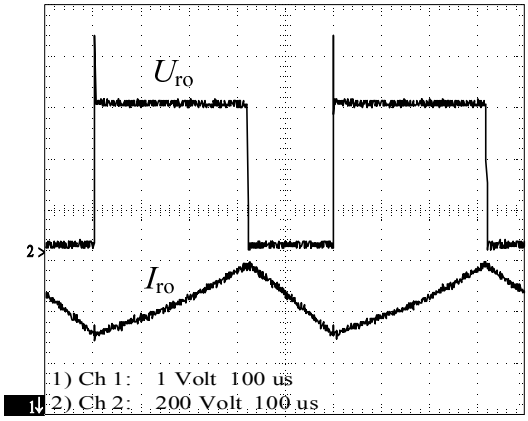


Figure 66 Rectifier output voltage U_{ro} (200 V/ div, 100 μs/ div) (a) and current I_{ro} (10 A/ div, 100 μs/ div) (b)

Cooling of the Output Rectifier

As one of the main contributors of power loss energy, after the input inverter in FEC, the output rectifier needs a heatsink with low thermal resistance. Although the passive cooling system is preferred, also the forced air cooling could be used. Total power dissipation of rectifier diodes is calculated by the following equation:

$$P_{loss\_diode} = P_{loss\_on} + P_{loss\_off}. \tag{49}$$

The simplified formula can be used for practical calculations where high accuracy is not required.

$$P_{loss\_on} = U_{F\_rd} \cdot I_{F\_rd\_amp} \cdot 2 \cdot D, \tag{50}$$

where $I_{F\_rd\_amp}$ is the amplitude value of the square wave current signal, U_{F_rd} is the forward voltage drop of the diode (function of $I_{F\_rd\_amp}$) and D is the duty cycle of the PWM (t_{on}/T). The off-state losses are mainly caused by the reverse recovery charge Q_{rr_rd} during time t_{rr}. Also, the small leakage loss power is added to the off-state power loss. Leakage current I_{leak_d} is given in the diode datasheet. $U_{Tr\_s\_amp}$ is the isolation transformer secondary voltage amplitude value.

$$P_{loss\_off\_diode} = P_{rec} + P_{leak}, \tag{51}$$

$$P_{leak\_diode} = I_{leak\_d} \cdot U_{Tr\_s\_amp} \cdot (1 - D). \tag{52}$$

The recovery loss power of the rectifier diode $P_{\text{rec\_rd}}$ depends on the reverse recovery charge of the rectifier diode $Q_{\text{rr\_rd}}$, the amplitude value of the rectifier input voltage $U_{\text{Tr\_p\_amp}}$ and the input voltage frequency.

$$P_{rec\_rd} = Q_{rr\_rd} \cdot U_{\text{Tr\_p\_amp}} \cdot f_{sw}. \tag{53}$$

Values of $Q_{\text{rr\_rd}}$ can be found from the diode datasheet. $Q_{\text{rr\_rd}}$ is calculated by:

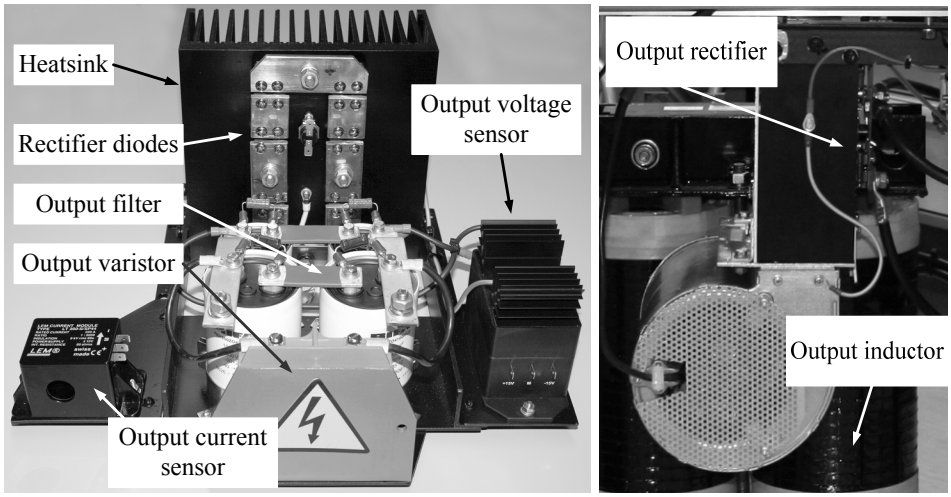
$$Q_{rr\_rd} = k_{Qr} \cdot \sqrt{I_{F\_rd}}, \tag{54}$$

where $I_{\text{F\_rd}}$ is the diode forward current and the coefficient k_{Qr} is a function of the junction temperature and the turn-off *di/dt*. To obtain the total losses of the rectifier we must multiply the loss power value of one diode with the total number of the diodes used in the rectifier.

For the selection of an appropriate cooling system, thermal equations are used to determine the maximum thermal resistance between heatsink and the environment $R_{\text{tha\_rec}}$, needed to keep the temperature of diode semiconductor junctions $T_{\text{j\_rd}}$ below the limiting 150 °C.

$$R_{tha\_rec} = \frac{T_{j\_rd} - T_a - P_{loss\_rd} \cdot R_{tjc\_rdiode} - P_{loss\_d\_module} \cdot R_{tch\_d\_module}}{P_{loss\_rectifier}} = 0.015 \frac{K}{W}. \tag{55}$$

where ambient temperature T_{a} = 50 °C, rectifier diode loss $P_{\text{loss\_rd}}$ = 110 W, rectifier diode module loss $P_{\text{loss\_d\_module}}$ = 220 W , thermal resistance between the rectifier diode junction and the case $R_{\text{tjc\_rdiode}}$ = 0.6 K/W, thermal resistance between the diode module case and the heatsink $R_{\text{tch\_d\_module}}$ = 0.1 K/W and $P_{\text{loss\_rectifier}}$ = 419.50 W is the total power loss of the whole rectifier assembly. As the required thermal resistance of the passive cooler was 0.015 K/W a Fisher Electronik SK 418-200 heatsink with 230 V AC 200 W additional fan and airflow channeling plate (Figure 67 (b)) was used for output rectifier cooling as the original thermal resistance of the selected heatsink was not sufficient enough. Prototype output rectifier assembly was constructed so that the two diode modules in series could be used if needed. The whole rectifier is constructed as a separate module with a filter assembly and output protection- and measurement devices, as seen in Figure 67 (a).



(a) *(b)*

Figure 67 Modular output rectifier and filter assembly with surge protection and output measurement devices (a), forced air cooling of the rectifier (b)

Output Filter

The rolling stock FEC converter of an APS is responsible for providing low-voltage power to onboard apparatus and devices with their specific supply power quality requirements. Thus, the requirement for a fully stabilized low-ripple output voltage is essential. To keep the voltage ripple in the auxiliary DC-bus below allowed 5% value, a simple LC filter is used. The inductor current rise is calculated with the following equation:

$$dI = 2 \cdot I_{out\_\min} = U_{L0} \cdot \frac{t_{on}}{L_0} = \left(U_{ro} - U_{out}\right) \cdot \frac{t_{on}}{L_0}. \tag{56}$$

The converter output voltage U_{out} is expressed as follows:

$$U_{out} = U_{ro} \cdot 2 \cdot D, \tag{57}$$

where the rectifier output voltage U_{ro} at the maximum input voltage and minimum duty cycle ($2 \cdot D_{\min} = 0.44$) is expressed as follows:

$$U_{ro} = \frac{U_{out}}{2 \cdot D_{\min}}. \tag{58}$$

The hardest working conditions for the output filter are when the impulses are the narrowest and the input voltage is the highest ($2 \cdot D_{\min} = 0.44$). Thus:

$$t_{on\_\min} = 2 \cdot D_{\min} \cdot T_{sw}. \tag{59}$$

If we replace the parameters U_{ro} and t_{on} with the corresponding equations, the inductor current rise is calculated with the following equation:

$$dI = \left(\frac{U_{out}}{2 \cdot D_{\min}} - U_{out} \right) \cdot \frac{\left(2 \cdot D_{\min} \cdot T_{sw} / 2\right)}{L_0} = 2 \cdot I_{out\_\min}. \tag{36}$$

The output filter inductor inductance L_o can be found with:

$$L_0 = \frac{U_{out} \cdot T_{sw} \cdot (1 - 2 \cdot D_{\min})}{4 \cdot I_{out\_\min}}, \tag{60}$$

where the minimum output current I_{out_min} is 5 % of the nominal current, thus I_{out_min}= 7.15 A. The output inductor must have 6.85 mH inductance. The filter capacitor is found by using the following equation:

$$C_O = \frac{dI \cdot t_{on}}{U_{out\_ripple}}, \tag{61}$$

where the allowed maximum voltage ripple U_{out_ripple} is 5 % and the allowed current ripple for the output filter inductor is 10 % of the nominal output current. In Figure 68 the voltage U_{out} and current I_{Co} of the output filter capacitor along with the output inductor voltage U_{Lo} and current $I_{Lo}$are shown.

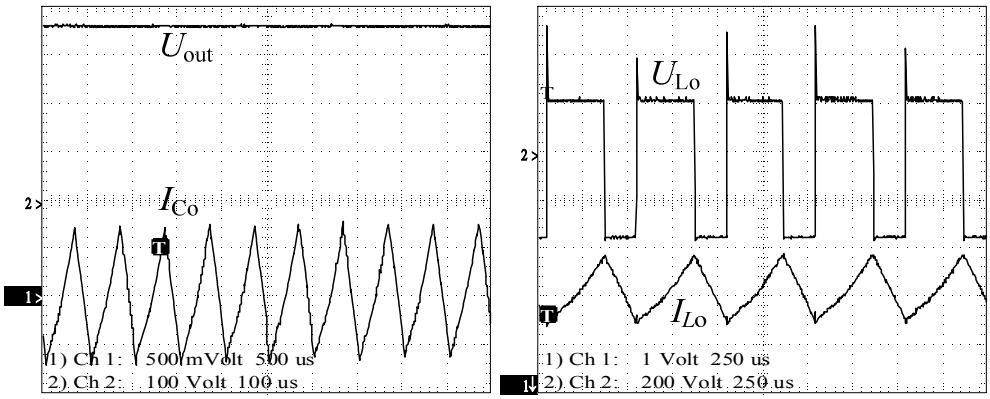


Figure 68 Output voltage U_{out} (100 V/ div 100 μs/ div) and output filter capacitor current I_{Co} (5 A/ div, 100 μs/ div) (a), output inductor voltage U_{Lo} (200 V/ div, 250 μs/ div) and current I_{Lo} (10 A/ div, 250 μs/ div) (b)

Calculated values of filter components are presented in Table 38.

Table 38 Values of filter components

Parameter	**Value at minimum input voltage (2.2 kV DC)**	**Value at maximum input voltage (4 kV DC)**
Amplitude value of the rectifier output voltage, U_{ro} (V)	438	795
Duty cycle, $2 \cdot D$	0.80	0.44
Output inductor inductance, L_0 (mH)	2.45	6.86
Capacitance of the filter capacitor, C_0 (μF)	327	180

Output filter capacitor battery is composed by connecting two 470 µF Rifa PEH200ZH capacitors with the nominal voltage of 500 V and two 1000 µF Rifa PEH200ZO capacitors in series and parallel circuit, as shown in Figure 69.

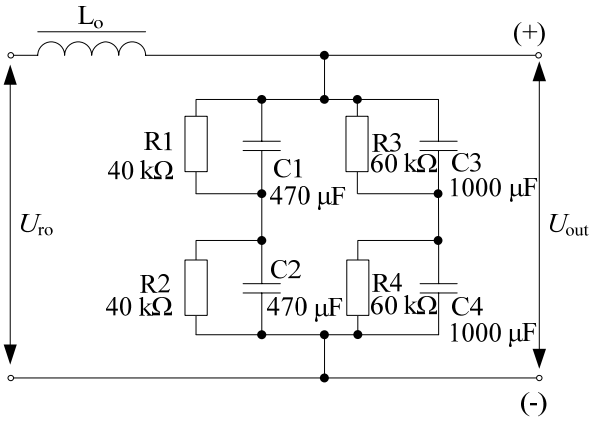
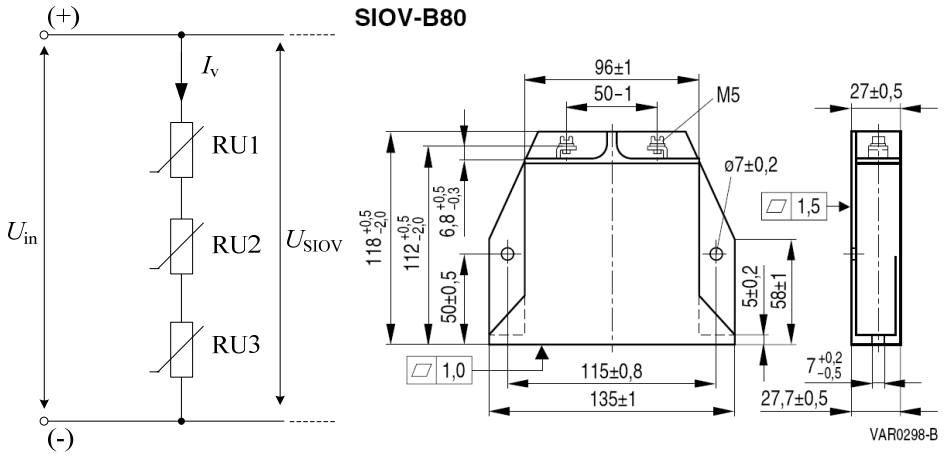


Figure 69 Output filter of FEC of an APS

To protect servicing personnel 40 kΩ and 60 kΩ discharge resistors are added to output filter capacitors.

3.3.5 Protection Circuitry

To protect the input inverter of FEC against overvoltage surges occurring in the contact line, metal oxide varistors are used. The varistor is also connected to the output of FEC to suppress overvoltages in 350 V auxiliary DC bus. Maximum permanent line voltage $U_{linemax2}$ is 4 kV, and rated impulse voltage U_{OV} is 15 kV DC. U_{OV} is also the highest permissible overvoltage in the contact line. The duration of the rated impulse t_s with 15 kV DC is 20 µs. To cope with the maximum permanent line voltage of 4 kV DC three Epcos B80K1100 varistors with switching voltage of 1465 V are needed to connect in series (Figure 70) [83].



(a) *(b)*

Figure 70 Series connection of varistors (a), B80K1100type metal oxide varistors (b)

Resistance of the contact line, switching gear, wiring and pantograph contact is low but in the case of short impulses with a duration of 20 µs the impedance of line Z_{line} and switchgear is much higher, 50 Ω. So the surge current flowing through the varistors I_{su} in the case of voltage surge is expressed as follows:

$$I_{su} = \frac{U_{ov}}{Z_{line}} = \frac{(15 \cdot 10^3)\ V}{50\ \Omega} = 300\ A. \tag{62}$$

Three in series connected 1465 V varistors result in the protection voltage of 4395 V but the voltage accuracy of metal oxide varistors is ± 10 %. In the worst case the minimum protection voltage U_{siov} would be:

$$U_{SIOV} = \lfloor 1465\ V \cdot (0{,}9/1{,}1) \rfloor \cdot 3 = 3595\ V. \tag{63}$$

3595 V is lower than the maximum permanent line voltage $U_{linemax2}$ but the three varistors all are seldom with minimum allowable parameters and the real protection voltage is higher than 4 kV. The resulting impedance of the contact line, switchgear and three series connected varistors Z_{res} is approximately 120 Ω and the current of varistors I^*_v in the case of the surge voltage protection event is:

$$I_v^* = \frac{(U_{ov} - U_{siov})}{Z_{res}} = \frac{(15 \cdot 10^3)\ V - 3595\ V}{120\ \Omega} = 95.04\ A. \tag{64}$$

Maximum energy in varistors W^* is calculated with the following equation:

$$W^* = U_{siov} \cdot I_s \cdot t_s = 3595\ V \cdot 95\ A \cdot (20 \cdot 10^{-6})\ s = 6.83\ J. \tag{65}$$

B80K1100 varistors can dissipate up to 6000 J of energy. The maximum surge power P_s dissipated in each selected varistor is 2 W, all together 6 W. The minimum time period between two surges with 15 kV T^* is calculated with:

$$T^* = \frac{W^*}{P_s} = \frac{6.83\ J}{6\ W} = 1.14\ s. \tag{66}$$

Input varistors can withstand several major voltage surges with a duration of 20 µs and voltage 15 kV, when the period between the overvoltage impulses is at least 1.14 seconds. In the case of longer duaration and higher voltage surges additional overvoltage protection devices are needed like fuses, spark gaps or gas discharge tubes.

The output voltage of FEC is 350 V DC. The suitable varistor to protect the output of FEC is Epcos B80K320 [84]. Maximum voltage surge in the output of the FEC is 1 kV with a duration of 20 µs. The output varistor is calculated, using the same methodology as for the input varistors.

$$U_{SIOV} = \lfloor 420\ V \cdot (0.9/1.1) \rfloor = 343\ V. \tag{67}$$

$$I_v^* = (1000\ V - 343\ V)/50\ \Omega = 13.14\ A. \tag{68}$$

$$W^* = U \cdot I \cdot t = 343\ V \cdot 13.14\ A \cdot (20 \cdot 10^{-6})\ s = 0.09\ J. \tag{69}$$

$$T^* = W^*/P = 0.09\ J/2\ W = 0.045\ s. \tag{70}$$

The output varistor is working in easier conditions, when compared with input protection devices but although there are needed some additional overcurrent protective devices to protect the output of FEC in case of varistor failure. In Figure 71 is shown the simulation of input side transient protection.

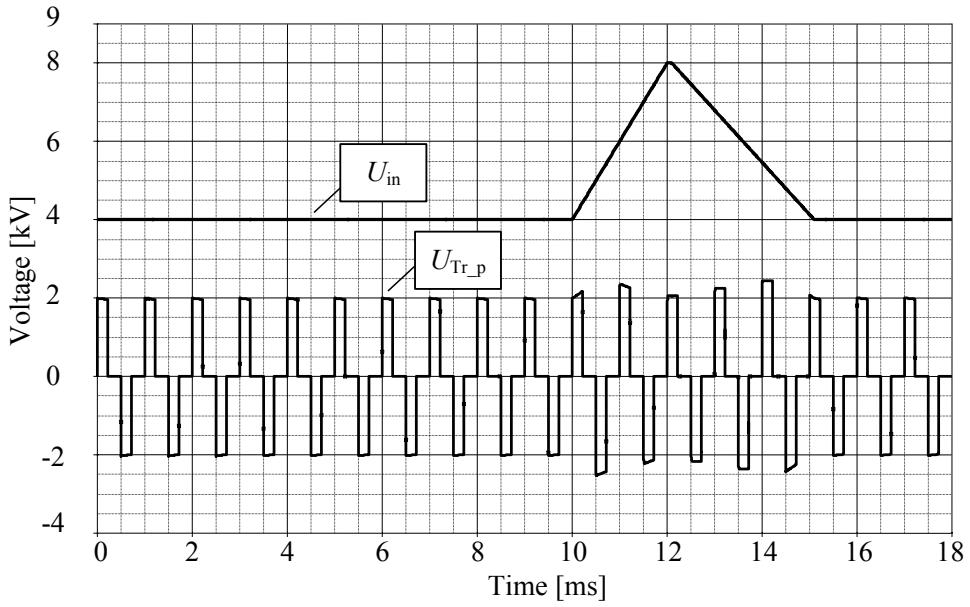


Figure 71 Simulation of Input side transient protection

The technical data of protective devices of FEC is listed in Table 39 and Table 40.

Table 39 Input overvoltage protection circuitry

Parameter	Value
Input varistors	
Total count of varistors	3
Varistor type	Epcos B80K1100
Nominal DC voltage, (V)	1465
Voltage accuracy, (%)	+/-10
Maximum allowable current in 20 μs, (A)	100 · 103
Maximum allowable energy, (J)	6000
Nominal power, (W)	2

Table 40 Output overvoltage protection circuitry

Parameter	Value
Output varistor	
Total count of varistors	1
Varistor type	Epcos B80K320
Nominal DC voltage, (V)	420
Voltage accuracy, (%)	+/-10
Maximum allowable current in 20 μs, (A)	100 · 103
Maximum allowable energy, (J)	1600
Nominal power, (W)	2

3.3.6 EMI Suppression

Simple dissipative RC snubber can be used across semiconductor power switches and rectifier diodes to damp parasitic voltage resonances in FEC. If the values of resistance and capacitance are chosen correctly, the switching losses can be reduced by up to 40% including both the loss in the switch and that in the resistor over the complete switching cycle. Slow turn-on and -off of the high voltage IGBTs and low switching frequency of the input inverter of FEC means that RC type would be the most suitable snubber topology. The RC snubber is also one of the few snubbers that is effective in the classic push-pull switch configuration [85].
The use of snubber circuits in the input inverter of FEC is not necessary but may be considered as the high-voltage spikes do not exceed the voltage ratings of the used IGBTs and generated EMI is exceeding the limits set in European standard EN 50121.

On the output rectifier of FEC simple RC snubber circuit is used the "frequency halving" capacitor connected in series with the damping resistance placed directly on the output of rectifier bridge, as tightly coupled as possible (Figure 72) [86].

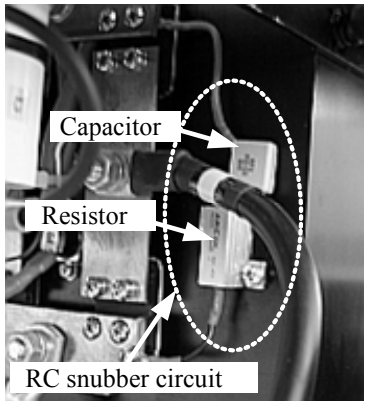


Figure 72 RC snubber circuit of the output rectifier

With the ringing frequency f_{res} about 1 MHz, suitable "frequency halving" capacitance C_{sn} is approx. 4.70 nF. C_{sn} is found experimentally by connecting

several capacitors into the snubber circuit and observing the period of the ringing at the diode. When the period of the ringing doubles, the right value of capacitor C_{sn} is found. The value of the parasitic capacitance C_{res} will be one-third of the paralleled capacitor value 1.57 nF [87].
Snubber's damping resistor R_{sn} can be defined as follows:

$$R_{sn} = \sqrt{\frac{L_{res}}{C_{res}}}, \tag{71}$$

where parasitic inductance L_{res} causing the resonance is:

$$L_{res} = \frac{1}{(2 \cdot \pi)^2 \cdot C_{res} \cdot f_{res}^2}, \tag{72}$$

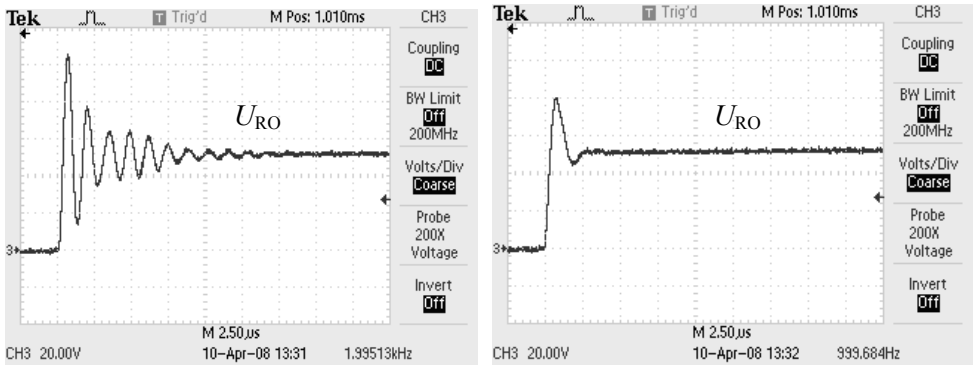
thus, estimated optimum value of the snubber's damping resistor is:

$$R_{sn} = \frac{1}{2 \cdot \pi \cdot f_{res} \cdot C_{res}} = \frac{1}{6.28 \cdot 1 \cdot 10^6 \, Hz \cdot 1.57 \cdot 10^{-9} \, F} = 101.42 \ \ \Omega. \tag{73}$$

With the parasitic capacitance 1.57 nF the damping resistance is 101.42 Ω. The power dissipated in the damping resistor can be roughly calculated by assuming that the energy stored in the added capacitor is lost in the resistor on each transition:

$$P_{sn} = C_{sn} \cdot U_{r\,peak}^{\ 2} \cdot f_{sw} = 4.7 \cdot 10^{-9} \, F \cdot 900 \ \ V^2 \cdot 1000 \ \ Hz = 3.80 \ \ W, \tag{74}$$

where U_{rpeak} is the amplitude value of voltage spike (U_{rpeak} = 900 V), appearing on the diode at transistor turn-off. The damping resistor dissipates 3.80 W when the switching frequency of converter f_{sw} is 1 kHz. In the experimental setup 100 Ω, 25 W resistor along with 4.7 nF foil capacitor is used. But it is necessary to note that it is only an approximation and for a more accurate calculation of power dissipation, the true RMS current through the damping resistor is required [88]. With the use of calculated snubber circuit the resulting overshoot is greatly reduced, as shown in the plot in Figure 73 (b).



(a) *(b)*

Figure 73 FEC output rectifier voltage without snubber circuit (a) and with snubber (U_{in}=500 V) (b)

The EMI in high voltage DC/DC converters can be greatly reduced by using simple damping circuits as the Figure 73 reveals. Although RC-snubbing is lossy it can improve efficiency and reliability of the power converter. With less ringing, lower voltage parts can be used and the excessive losses due to avalanche effects in semiconductors can be avoided and electromagnetic noise of the circuit is also reduced. Although the active and non dissipative snubber circuits have better parameters, they also have complicated design.

Simple snubber circuits allow quick and cost effective to solution of some serious EMI problems. But to completely minimize the overshoot and ringing effects it is necessary to pay attention to that the overall design of the power stage circuitry has low inductance and the isolation transformer used in the converter is designed to reduce leakage inductance to prevent some parasitic loops between the secondary side and the diode rectifier.

3.4 Evaluative Analysis of the Developed Converter

3.4.1 Efficiency Analysis of the High Voltage Half-Bridge Inverter

The efficiency of the input inverter greatly influences the efficiency of the whole system. The efficiency of the input inverter of FEC was experimentally verified by comparing the loss power, generated in IGBTs with the input power. The efficiency of the inverter can be calculated with the following equation:

$$\eta_{inv} = \frac{\left(P_{in} - P_{loss\_inverter}\right)\cdot 100}{P_{in}}, \tag{75}$$

where P_{in} is the input power of converter $P_{\text{loss\_inv}}$ is the power loss of the inverter and η_{inv} is the efficiency of the inverter. The losses were acquired experimentally by recording the temperatures of inverter transistors in the environment with stable temperature. Power loss of the inverter was calculated by using thermal models of test stand. The experimental converter was working at certain switching frequencies and loads until the IGBT module temperatures were stabilized. The heatsink temperature and the ambient temperature were logged during the experiment. The temperature of the heatsink was measured in two points to calculate the heat gradient and the individual temperatures of each IGBT. Thermal measurements were conducted with FK422 PT100 temperature sensors and SEM203P measurement converters. The accuracy of the measuring devices was 5 %. Thermal model of the half-bridge inverter with 6.5 kV IGBTs is shown in Figure 74. The thermal model used was simplified as the thermal ripple and thermal capacitance are not taken into account.

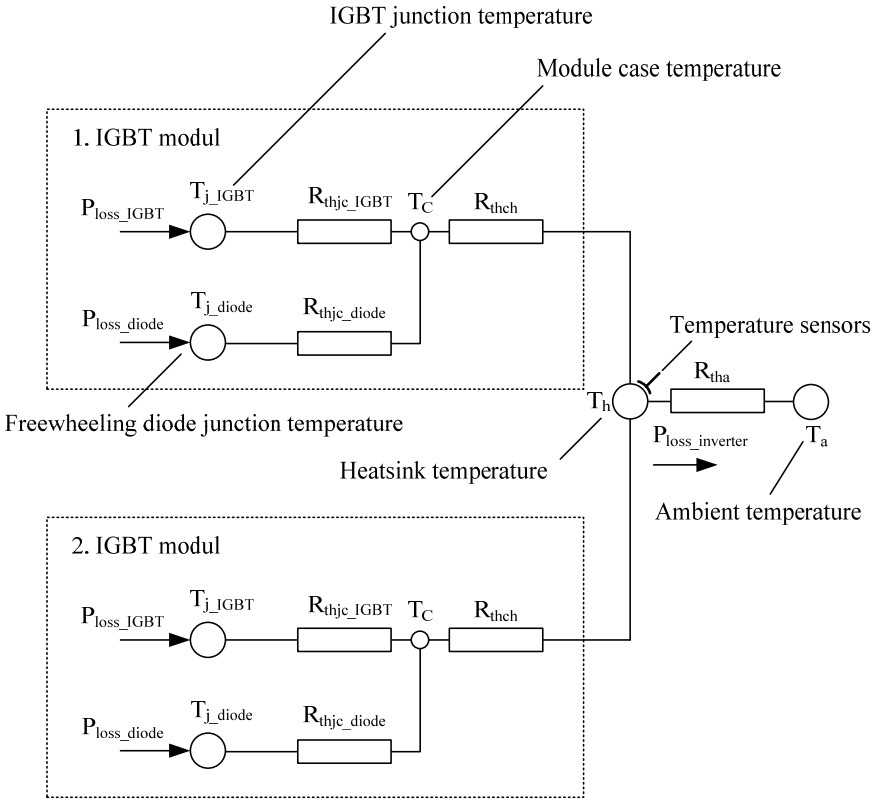


Figure 74 Thermal model of FEC input inverter

Loss Calculation With the Thermal Model and Experimental Loss Measurement

Power loss energy from junctions of IGBT and FWD create the temperature rise along the thermal resistance from the junction to the surrounding environment that adds to the temperature of surrounding T_a as 6.5 kV IGBTs have been built in the freewheeling diodes. Zones of thermal resistance inside the IGBT module are distinguished: thermal resistance between the transistors semiconductor junction and the transistor case $R_{\text{thjc\_IGBT}}$ thermal resistance between the freewheeling diode junction and transistor modules case $R_{\text{thjc\_FWD}}$ and common thermal resistance between the case of the IGBT module and heatsink R_{thch}. Different modules are joined to a more complex thermal system. IGBTs that form a half- or full-bridge inverter are connected to a common heatsink with thermal resistance between heatsink and the surrounding environment (air) R_{tha}. The resulting temperature of IGBTs junction $T_{\text{j\_IGBT}}$ can be estimated with the following equation:

$$T_{j\_IGBT} = \Delta T_{jc\_IGBT} + \Delta T_{ch} + \Delta T_{ha} + T_a, \tag{76}$$

where the temperature rise between the transistors junction and module case $\Delta T_{\text{jc\_IGBT}}$, temperature rise between the case and the heatsink ΔT_{ch} and the temperature rise between heatsink and the surrounding air ΔT_{ha} are added to the surrounding air temperature T_a. Temperature rise is the loss power multiplied with the thermal resistance. Power loss of the transistor is $P_{\text{loss\_IGBT}}$ and power loss of the

freewheeling diode is $P_{\text{loss\_FWD}}$. Temperature of one transistors junction can be calculated as:

$$T_{j\_IGBT} = (((P_{loss\_IGBT} \cdot R_{thjc\_IGBT}) + (P_{loss\_IGBT} + P_{loss\_FWD}) \cdot R_{thch} + (P_{loss\_IGBT} + P_{loss\_FWD})) \cdot n_{tr} \cdot R_{tha}) + T_a. \quad (77)$$

where n_{tr} is the number of IGBT modules in the common heatsink. The number of 6.5 kV IGBT modules for half-bridge is 2 and for full-bridge is 4. The total IGBT losses were calculated by the following simplified equation:

$$P_{loss} = \frac{T_h - T_a}{R_{tha}}, \quad (78)$$

where $P_{\text{loss\_total}}$ is the resulting loss power of both IGBTs sharing one heatsink, T_{h} is the measured temperature of the heatsink, T_{a} is the ambient temperature and R_{tha} is the thermal resistance of the cooling system. R_{tha} for the selected cooling system is 0.013 K/W. R_{tha} of the cooling system is calculated using the temperature differential – loss power characteristics of the heatsink, as shown in Figure 60 (b) [89]. The input voltage, average current, heatsink and ambient temperature were measured during a period of 30 minutes (Figure 75).

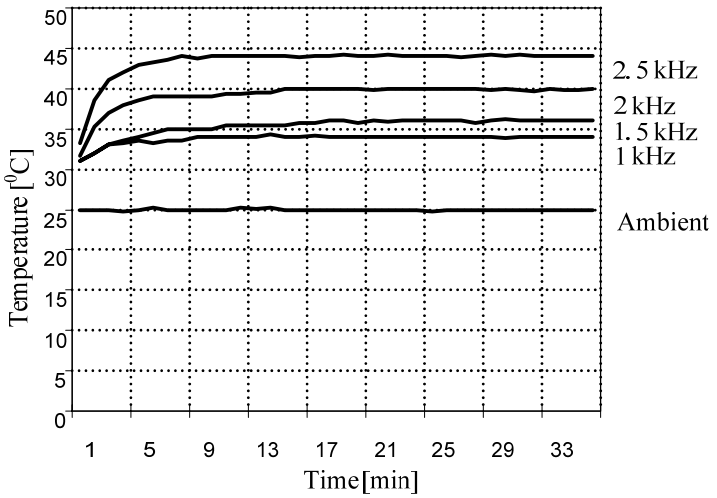


Figure 75 Measured temperatures of experimental DC/DC converters input inverter heatsink at various switching frequencies at 3 kV input voltage and 30 kW output power

Loss Calculation by Analytic Approach

Total loss of the IGBT module is the sum of switching, conduction and freewheeling diode losses.

$$P_{loss\_IGBT} = P_{condIGBT} + P_{onIGBT} + P_{offIGBT} + P_{FWD}, \quad (79)$$

where $P_{loss\text{-}IGBT}$ is the total power loss of IGBT, P_{onIGBT} is the turn-on power loss of the IGBT, P_{offIGBT} is the turn-off power loss of the IGBT and P_{FWD} is the power loss

of the integrated freewheeling diode. Conduction loss is the function of the IGBT forward voltage drop, collector current and time.

$$P_{condIGBT} = f_{sw} \cdot \int_{t_2}^{t_3} U_{FIGBT}(I_C) \cdot I_C(t)dt, \tag{80}$$

the simplified equation of P_{condIGBT} is:

$$P_{condIGBT} = U_{FIGBT} \cdot I_{C-amp} \cdot \sqrt{D}, \tag{81}$$

where t_2 to t_3 is the IGBT conduction time, U_{FIGBT} is the forward voltage drop of the IGBT and I_C is the collector current of the IGBT, I_{C_amp} is the IGBT collector current amplitude value and D is the duty cycle. The switching process is shown in Figure 76.

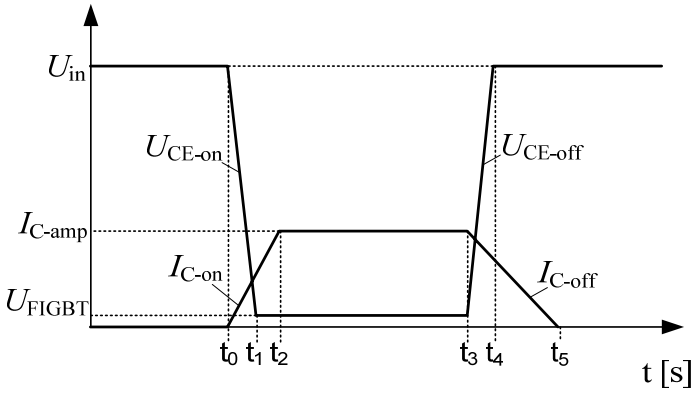


Figure 76 IGBT switching process

By integrating the multiplied turn-on voltage and the current ramp the turn on energy is calculated. As the current changes slower than the voltage, the power loss equation is divided into two parts. In the first both the voltage and currentare changing, in the second part only the current changes. When this energy is multiplied with the switching frequency f_{sw} then the result of this equation is the IGBT turn-on power loss.

$$P_{onIGBT} = f_{sw} \cdot \left[\int_{t_0}^{t_1} U_{CE-on}(t) \cdot I_{C-on}(t)dt + \int_{t_1}^{t_2} U_{FIGBT}(I_C) \cdot I_{C-on}(t)dt \right], \tag{82}$$

where t_0 to t_2 is the total IGBT turn-on time, where t_0 to t_2 is the IGBT collector-emitter voltage fall time, and t_2 to t_3 is the IGBT collector current rise time. $U_{\text{CE-on}}$ is the IGBT collector-emitter voltage at turn-on and $I_{\text{C-on}}$ is the collector current of the IGBT after IGBT turn-on. The IGBT turn-off power is calculated by a similar approach. To simplify the power loss calculations, voltage and current waveforms can be replaced by the line functions:

$$U_{CE-on}(t) = U_{in} - \frac{t \cdot (U_{in} - U_{FIGBT})}{t_1 - t_0} + U_{FIGBT}\ , \tag{83}$$

$$I_{C-on}(t) = \frac{t \cdot I_{C-amp}}{t_2 - t_0}, \tag{84}$$

where t_0 to t_1 is the IGBT collector-emitter voltage fall time and $I_{C\text{-amp}}$ is the amplitude value of the IGBT collector current.

$$P_{offIGBT} = f_{sw} \cdot \left[\int_{t_3}^{t_4} U_{CE\_off}(t) \cdot I_{C-off}(t)dt + \int_{t_4}^{t_5} U_{in} \cdot I_{C-off}(t)dt \right], \tag{85}$$

where $U_{CE\text{-off}}$ is the IGBT collector-emitter voltage at turn-off (rising edge) and $I_{C\text{-off}}$ is the collector current of the IGBT (falling edge).

$$U_{CE-off}(t) = U_{in} - \frac{t \cdot (U_{in} - U_{FIGBT})}{t_4 - t_3} + U_{FIGBT}\ , \tag{86}$$

$$I_{C-off}(t) = I_{C-amp} - \frac{t \cdot I_{C-amp}}{t_5 - t_3}, \tag{87}$$

where t_3 to t_5 is the total IGBT turn-off time and the collector current fall time, $t_4$to t_3 is the IGBT collector-emitter voltage rise time. To obtain the loss of one module, the freewheeling diode losses must be added to $P_{\text{loss-IGBT}}$. The experimental results are shown in Table 41. The reference values for the evaluation of the data experimentally acquired were calculated with a simulation software.

Table 41 Measured and calculated results of IGBT module loss power

Parameter	**Values**			
Switching Frequency, (kHz)	1	1.5	2	2.5
Measured loss power, (W)	618	846	1072	1142
Calculated loss power, (W)	547	766	985	1204
Simulated loss power, (W)	516	746	978	1208
wherInverter input voltage, (V)	2991	3023	3011	2973
Inverter input average current, (A)	9.5	9.7	9.8	10.2
Inverter power, (W)	28473	29323	29353	29135
FEC inverter efficiency, (%)	98	97	96	96

The values of the measured and estimated losses are slightly different because in the experimental setup the switching losses of an IGBT are affected by a sum of factors, as for instance, capacitance and inductance of the input inverter bus-bar system, internal inductances and capacitances of the components [90]. Also the hard-switching used in the application influences the overall losses of the IGBT [91].

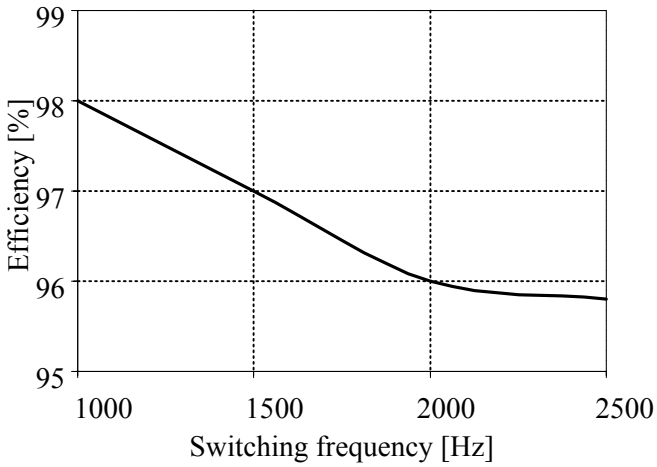


Figure 77 Efficiency / switching frequency characteristics of HB inverter with 6.5 kV IGBTs

As we can see from Table 41 and graphs in Figure 77 the performance is 98 %, when the switching frequency is 1 kHz and it decreases to 96 % when the switching frequency is set above 2 kHz. Although 1 kHz higher switching frequency is beneficial, the efficiency of the whole device is lowered by 2 %

3.4.2 Final Evaluation and Generalizations

With 6.5 kV IGBT transistors it is possible to use two-level full- or half-bridge inverter topology in FEC. The HB inverter has simple construction, simple control system, a lower primary voltage of the isolation transformer and only two HV IGBTs. The FB inverter has lower IGBT current, higher possible switching frequency and lower primary current (low copper losses) of the isolation transformer. Main advantage of the HB inverter is its 15 % lower cost of details. Therefore, it is suitable to use the HB inverter topology in the input inverter of FEC. The FB inverter topology may be advantageous when new and cheaper IGBTs with lower current ratings would be available.

To conduct experiments with HV IGBTs a 50 kW experimental prototype converter with the HB inverter, isolation transformer and full-bridge rectifier was constructed. The input inverter of the prototype has an HB topology with two 6.5 kV 200A FZ200R65KF1 Infineon IGBT modules and six 100 μF HV film type capacitors. The isolation transformer is 50 kW high frequency transformer with a toroidal core. The output rectifier was a full-bridge rectifier with DSEI2x101-12A diodes. To keep the output voltage ripple below 5 % a simple LC filter was used. Characteristic technical solutions used in the prototype are listed in Table 42. Based on the experimental and analytical approach, it was found out that the switching frequency limit of 6.5 kV IHBTs in the inverter with the HB topology is 1 kHz. To improve the switching frequency the following is required: IGBTs with better dynamics (nonexistent), a more powerful cooling system (liquid cooling instead of forced air cooling) or a more advanced inverter topology (higher complexity).

Table 42 Characteristic technical solutions of FEC

Parameter	Value
Input inverter	
Topology	Two-level, half-bridge
IGBTs	6.5 kV, 200A, FZ200R65KF1, Infineon
Switching frequency upper limit, (kHz)	1
Isolation transformer	
Transformer type	High frequency toroidal transformer with soft nanocrystalline core material GM14DC
Output rectifier	
Rectifier type	Full-bridge
Rectifier diodes	Fast recovery, epitaxial, IXYS, DSEI2x101-12A double diode modules

It is possible to raise the switching frequency up to 2.5 kHz when the output power is reduced, but the efficiency of the inverter is lowered from 98 % at 1 kHz to 96 % at 2.5 kHz. Analysis of the computer simulation and experimental results revealed the oscillations at transistor turn-off that may cause some conducted EMI problems in the contact line.

As the result of this analysis it can be concluded that the HB inverter with 6.5 kV IGBTs has good working characteristics and simple construction. Simple construction means also higher reliability, lower production and maintenance costs, suitability for use in the demanding rolling stock applications like the front end converter of the auxiliary power supply.

4. A Method to Improve Power Density and Efficiency of Two-level Catenary-Fed Isolated DC/DC Converters with HV IGBTs

4.1 Introduction of the Three-Level NPC Half-Bridge DC/DC Converter with 3.3 kV IGBTs

The two-level inverter design has many advantages as well as some serious disadvantages like relatively low maximum switching frequency, expensive transistors, and bulky passive components. One possible solution to those problems is the three-level neutral point clamped inverter topology (Figure 78). Instead of two 6.5 kV IGBTs, it contains a three-level NPC inverter four 3.3 kV IGBTs and two high-voltage clamping diodes. Another method for improvement of the developed FEC is the current doubler rectifier (CDR) at the FEC output stage (Figure 78).

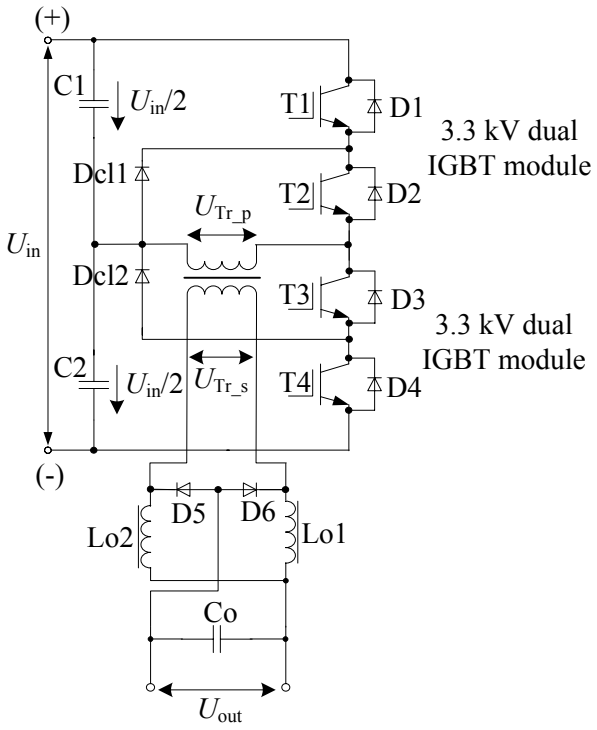


Figure 78 Three-level NPC half-bridge DC/DC converter with a current-doubler rectifier

CDR consists of two diodes and two inductors. The benefits of using CDR in the output stage of FEC are:

- reduced voltage drop and conduction losses;
- better dissipation of losses;
- reduced turns ratio of the isolation transformer (2.4:1 to 1.25:1);

- lower output current ripple with less inductivity (two output inductors operate with a 180º phase shifting and could provide the output ripple current cancellation that depends on the operating duty cycle);
- volume of both CDR inductors is up to 50 % smaller than volume of single inductor of the full-bridge rectifier.

Main disadvantage of the proposed three-level NPC half-bridge inverter is its slightly higher number of components, more complicated design and control system. Downsides of CDR are: two times increased blocking voltage of the rectifying diodes and the inductors that are operating at two times lower frequency and with the higher current ripple, thus requiring more inductance for the same output current ripple.

Operation of Three-Level NPC Half-Bridge Inverter with PWM

The operation of three-level NPC HB inverter with PWM (pulse-width modulation) control is divided into two active states and two freewheeling states. In the first active state both top transistors T1 and T2 are switched on and current flows through the primary winding of isolation transformer, transistors T1 T2 and capacitor C2 (Figure 79) (a).

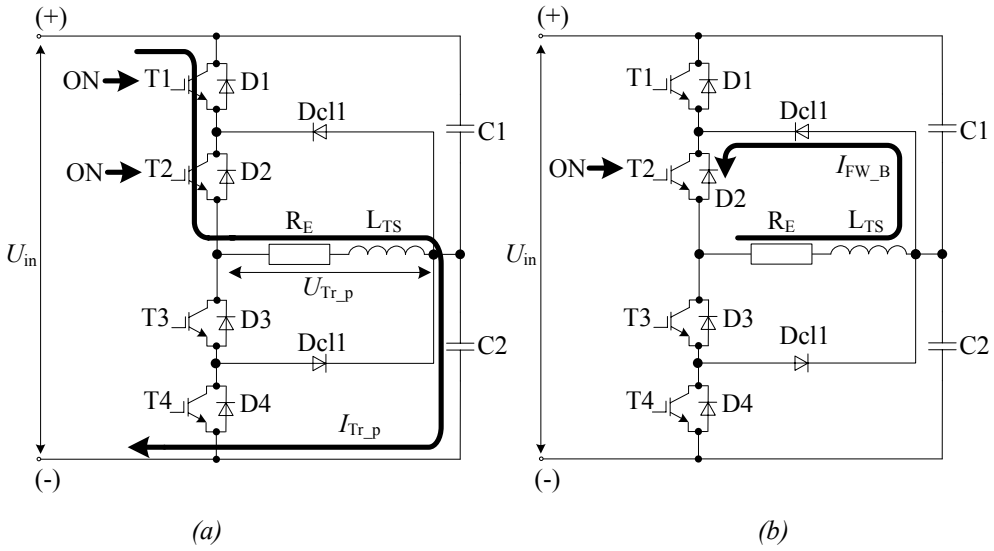


Figure 79 Active state of three-level NPC half-bridge inverter (a), freewheeling state of three-level NPC half-bridge inverter (b)

The active state is followed by the freewheeling state, where the transistors T2 and T3 are switched on to short circuit the potential generated on the stray inductance of the isolation transformer L_{TS} (Figure 79) (b). Freewheeling current flows through T2, clamping diode Dcl1 and the primary winding of the isolation transformer. The freewheeling current is limited by resistance of busbar, voltage drop of Dcl1, resistance of transformer primary winding R_E and voltage drop of T2. Freewheeling state reduces the impact of common turn-off problems like freewheeling impulses,

switching transients and the ringing effect known in the two-level HB inverter. The exact timing diagrams of transistors T1, T2, T3 and T4 are shown in Figure 80 [93].

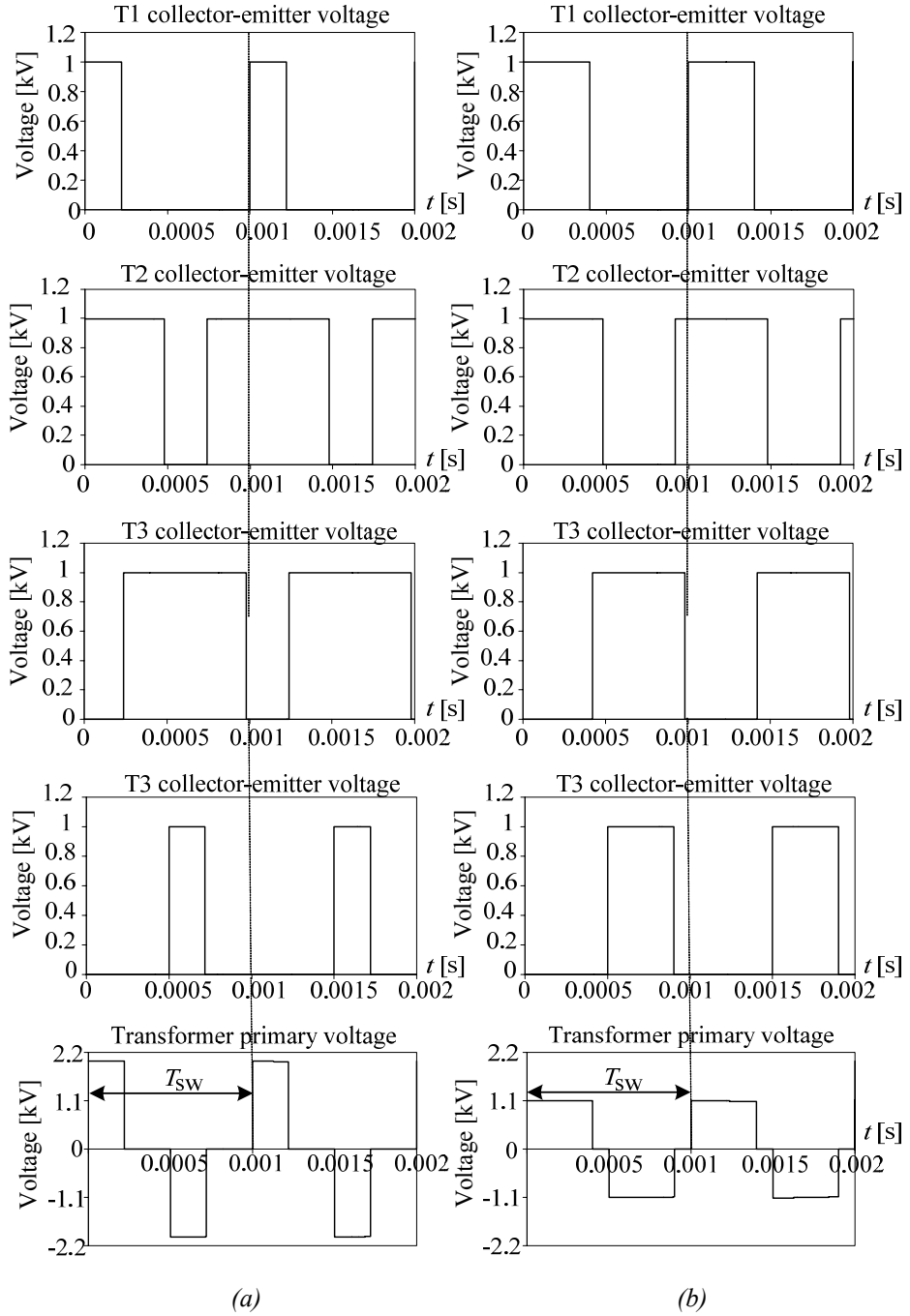


Figure 80 Timing diagrams of three-level half-bridge NPC inverter: at maximum (a) and minimum (b) input voltages

In the second active state bottom transistors T3 and T4 are switched on, current flows through T3, T4, the primary winding of the transformer and capacitor C1 (Figure 81) (a).

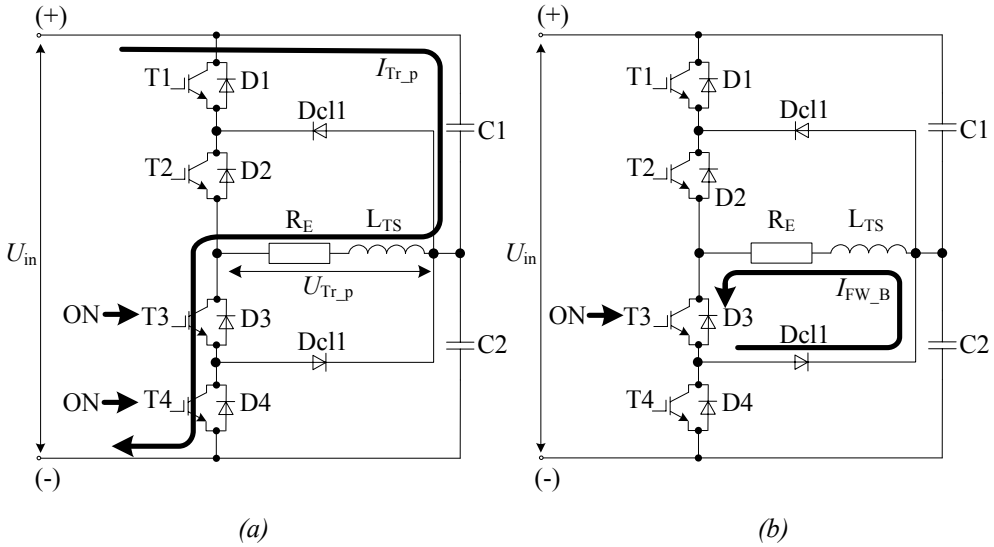


Figure 81 Second active state of three-level NPC half-bridge inverter (a), freewheeling state of three-level NPC half-bridge inverter (b)

The second freewheeling state involves switching on transistors T2 and T3 and shorting L_{TS} through T3 and Dcl2 (Figure 81) (b).

4.1.1 Switch Properties and Limitations in Hard Switching Conditions

Analsis of switch properties and limitations focuses on two input voltage boundary points 2.2 V and 4 kV. 3.3 kV IGBTs, used in the three-level half bridge inverter with Infineon 3.3 kV 200 A double IGBT modules FF200R33KF2C.

By neglecting losses, voltage and current transients, the operating conditions of the inverter switches are:

$$U_{CE\_\max\_3l} = \frac{U_{in\_\max}}{2}, \tag{88}$$

$$I_{CE\_\max\_3l} = \frac{P}{U_{in\_\min} \cdot D_{\max}}, \tag{89}$$

where $U_{\text{in\_min}}$ is the minimum FEC input voltage, $U_{\text{in\_max}}$ is the maximum FEC input voltage, $U_{\text{CE\_max\_3l}}$ is the maximum collector-emitter voltage of one IGBT in the three-level HB inverter and $I_{\text{C\_max\_3l}}$ is the maximum collector current of one IGBT. Thus, analysis of the equations above shows that both tansistors in the three-level NPC topology are operating with half of the input voltage. The collector current of IGBTs is the same as compared with the conventional two-level topology (Table 31). The switching frequency of 3.3 kV IGBTs in the three-level inverter is limited

by the maximum temperature of the freewheeling diode and the transistor. By using the thermal model of the three-level HB inverter and calculating IGBT module losses, the switching frequency limit of FF200R33KF2C 3.3 kV IGBTs in the three-level HB inverter was calcualted and shown in Figure 82. The switching frequency boundaries depend on the FEC input voltage. At the minimum input voltage and 50 kW output power, the switching frequency is limited with 5.5 kHz and at the maximum input voltage the swithing frequency limit is 2 kHz.

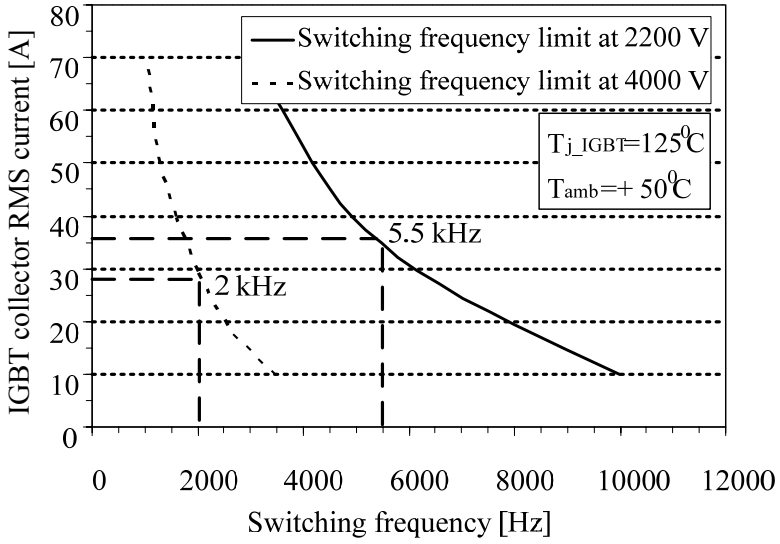


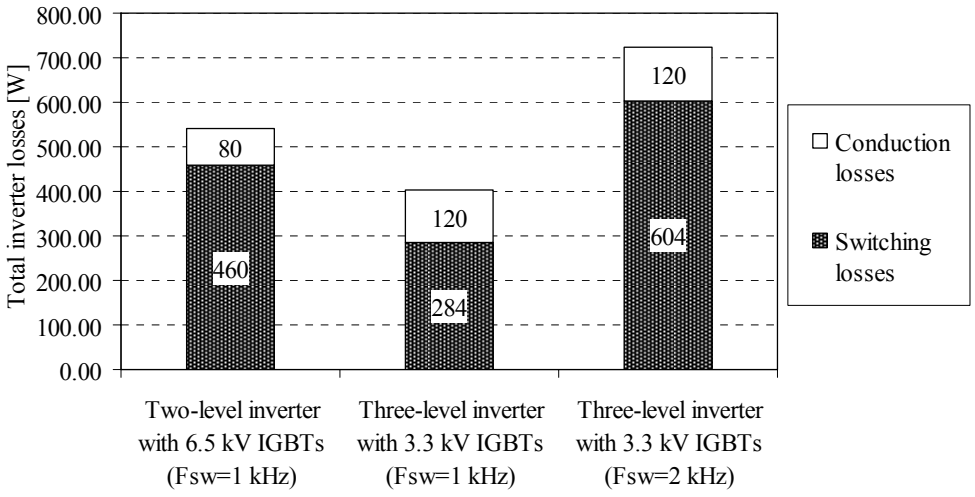
Figure 82 Switching frequency limit of FF200R33KF2C 3.3 kV IGBTs in three level HB inverter configuration

As the integrated freewheeling diodes reach the maximum junction temperature of 125 °C 500 Hz at given collector current earlier than IGBT junctions, it enables the freewheeling state to be used even at higher switching frequency, as some of the energy stored in stray inductance is dissipated in primary winding of the isolation transformer and the clamping diodes. Higher possible switching frequency of FF200R33KF2C 3.3 kV IGBTs than with 6.5 kV FZ200R65KF1/2 IGBTs is reached due to lower switching losses of one transistor and better thermal handling capability.

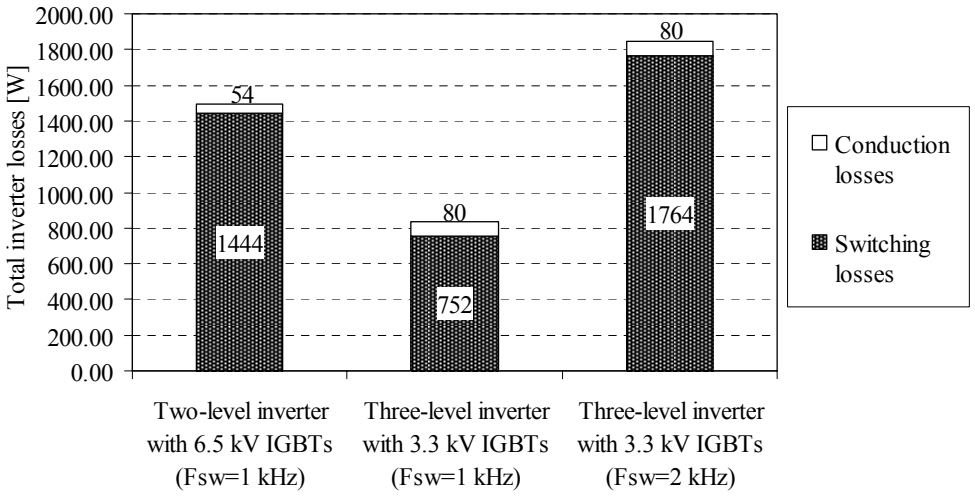
4.1.2 IGBT Losses in Hard Switching Conditions

To analyze power losses switching- and conduction losses of two- and three-level inverters were compared. Losses of the two level inverter at 1 kHz switching frequency were compared with the losses of the three-level inverter at 1 and 2 kHz switching frequency at minimum and maximum input voltages (2.2 kV DC, 4 kV DC) (Figure 83). At minimum input voltage the total inverter loss of the three-level inverter with 3.3 kV IGBTs is over 25 % lower than the losses of the two-level inverter. The conduction losses of the three-level inverter are 33 % higher due to series connection of two transistors in one bridge arm. If the switching frequency for the three-level inverter is 2 kHz then the total loss of three-level inverter

becomes 26 % higher (724 W total power loss at 2 kHz switching frequency). 100 % change in the switching frequency does not affect conduction losses. At two times higher input voltage is the differences in the losses of the two-level and three-level inverter losses, that are operating respectively at 1 kHz and 2 kHz 19 % exist. As the rms current of each transistor is lower at the maximum input voltage, are the conduction losses are over 33 % lower but the switching losses are more than 66 % higher.



(a)



(b)

Figure 83 Comparison of total losses of two- and three-level inverters operating at minimum 2.2 kV (a) and maximum 4 kV (b) input voltages at the same rated output power

The power loss dissipated in clamping diodes Dcl1 and Dcl2 during the freewheeling period depends on diode properties and isolation transformer primary leakage inductance. Power loss in clamping diodes could be neglected.

4.1.3 Passive Components

2 kHz switching frequency allowed for the three-level HB inverter with 3.3 kV IGBTs and current doubler rectifier topology influence also all passive components in FEC. Twice higher switching frequency of the three-level inverter allows the reduction of the core volume of the isolation transformer up to 17 %, when compared to the required minimum core volume in 50 kW FEC with the two-level inverter with 6.5 kV IGBTs (Figure 84). The minimum core volume of the isolation transformer is defined by:

$$V_m = 1.5\sqrt{\frac{A_C \cdot k_{add} \cdot k_t}{k_u}} \cdot \frac{P_t}{f^{\frac{1}{4}} \cdot \Delta T_t}, \tag{90}$$

where P_t is the transformer rated power, k_t is the temperature coefficient of the winding resistance, k_u is the window utilization factor, k_{add} is the added losses factor (increase of the winding resistance with the frequency due to skin and proximity effects), ΔT_t is the transformer temperature rise, A_C is the core loss factor (core loss per volume per frequency).

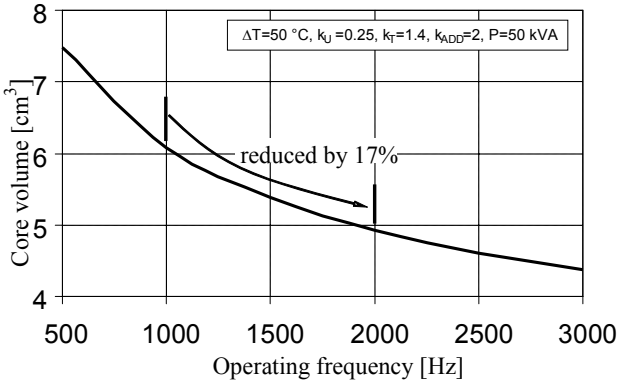


Figure 84 Decrease of magnetic core volume with the implementation of three-level inverter

The number of turns in the primary winding of the isolation transformer could be reduced by 14 and the number of secondary turns increased by 6 (Figure 85).

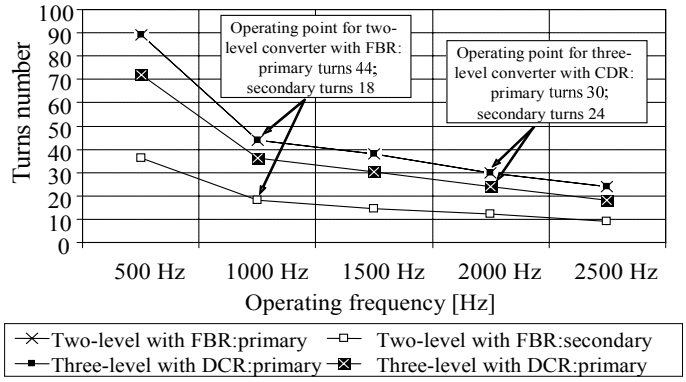


Figure 85 Number of turns of an isolation transformer as a function of switching frequency

Number of primary turns N_p of an isolation transformer is calculated as follows:

$$N_p = \frac{U_{Tr\_pI\_rms}}{4.44 \cdot f_{sw} \cdot S_m \cdot B_m}, \tag{91}$$

where $U_{Tr\_pI\_rms}$ is the rms value of the primary winding voltage at the fundamental frequency, S_m is the cross-section of the magnetic core, B_m is the operating flux density and f_{sw} is the switching frequency. Reduced primary turns number of the isolation transformer and the reduced secondary current by the CDR type rectifier decrease the overall losses of the isolation transformer in all operation points by 92 W. In Figure 86 the breakdown of the power loss of the 50 kW isolation transformer of FEC is shown.

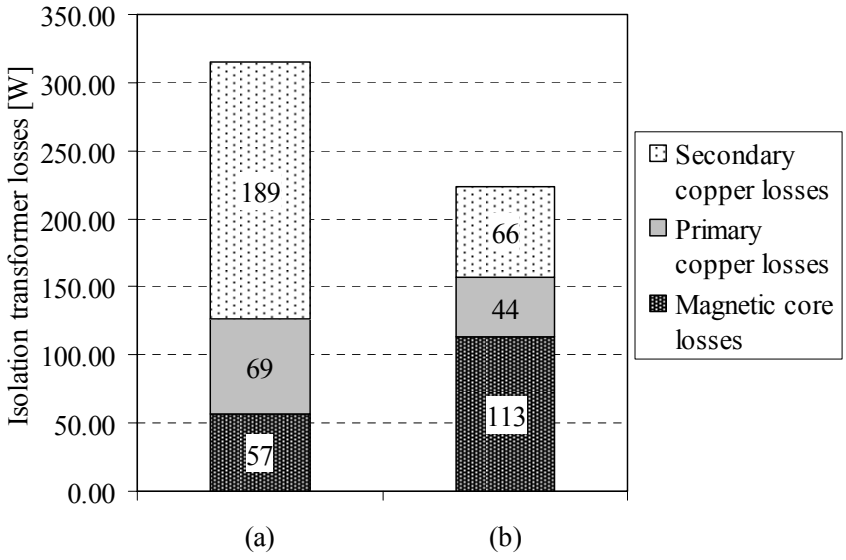


Figure 86 Power loss breakdown of the 50 kV DCA isolation transformer with two-level (a) and three-level (b) inverter topology

In the transformer, operating with the two-level inverter, secondary copper losses (189 W) are dominating. When the transformer operates with the three-level inverter the power losses of the isolation transformer are better balanced. Due to higher switching frequency the dominating loss component of the magnetic core loss is 113 W.

The recifier stage of FEC could be upgraded from the full bridge rectifier (FBR) to the current doubler rectifier (CDR) topology. In comparison with FBR, CDR topology requires two times less diodes but those diodes must have higher blocking voltage capability, as the voltage amplitude value of the secondary winding of the isolation transformer is two times higher. The CDR introduces additional advantages to the FEC design. Although the diodes with 1.2 kV blocking voltage used in FBR have 47 % lower forward voltage drop then diodes with 1.8 kV DC blocking voltage used in CDR, the twice reduced number of diodes in the CDR topology means 27 % smaller losses at the same rated load (610 W and 840 W, respectively). As the used diodes were of the FRED type, the switching losses could be neglected. Losses of FBR and CDR topologies are calculated as follows:

$$P_{FBR} = 4 \cdot I_{F\_rd\_av} \cdot U_{F\_rd} = 4 \cdot \frac{I_{out}}{2} \cdot U_{F\_rd} = 2 \cdot I_{out} \cdot U_{F\_rd}, \tag{92}$$

$$P_{CDR} = 2 \cdot I_{F\_rd\_av} \cdot U_{F\_rd} = 2 \cdot \frac{I_{out}}{2} \cdot U_{F\_rd} = I_{out} \cdot U_{F\_rd}, \tag{93}$$

where $I_{F\_rd\_av}$ is the average diode current and U_{F_rd} is the corresponding forward voltage drop of the diode.
Also, another passive elements are affected by the output rectifier topology. The second highest power loss after the rectifier's is occurs in the output filter inductor. The output current in the CDR topology is divided between two filter inductors. Minimum inductivity to achieve the required output voltage ripple is 4.8 mH for both inductors in the CDR topology or for one inductor used in the FBR topology. Minimum required core volume for the output inductor is estimated by:

$$V_{m,i} = \sqrt{\frac{A \cdot k_g \cdot k_{add} \cdot k_t}{k_u}} \cdot \frac{L_O \cdot I_{Lo(rms)}^2 \cdot f^{\frac{3}{4}}}{0.3 \cdot \Delta T_{Tr}} \cdot \frac{1 + 3 \cdot e^{\left(1 - \frac{T_{SW}}{t_{on,\min}}\right)}}{4}, \tag{94}$$

where L_o is the inductance value, I_{Lo_rms} is the rms value of a current through the inductor and k_g is the airgap coefficient, k_u is the window utilization factor, k_{add} is the added losses factor (increase of the winding resistance with the frequency due to skin and proximity effects), ΔT_{Tr} is the transformer temperature rise, A is the core loss factor. As each inductor of the CDR topology handles only half of the output current, is minimum required core volume for each output inductor is 50 % smaller than the required volume of the FBR output inductor. Power loss in output rectifier inductors is expressed with the equation:

$$P_i = 13 \cdot \alpha \cdot \Delta T_I \cdot V_{m,i}^{\frac{2}{3}}, \quad (95)$$

where α is the heat irradiation coefficient and $V_{m,i}$ is minimum required core volume for the output inductor and ΔT_I is the output inductor temperature rise. Power losses of the CDR topology are 24 % less than the loss power dissipation of the FBR topology (580 W and 770 W respectively). By using the combination of the three-level HB inverter with 3.3 kV IGBTs, two times higher switching frequency and a current doubler rectifier is possible to increase the efficiency of FEC by 1 %.

4.1.4 Economical Evaluation

In comparison with the two-level HB topology the three-level inverter topology has some disadvantages in terms of economy, like more complicated design and higher component count but the components are cheaper and higher component count is somewhat compensated by the use sof pecial double IGBT modules. Four 200 A, 3.3 kV IGBTs required for the three-level HB inverter can be installed in double IGBT modules that are 47 % cheaper than 200 A 6.5 kV single IGBT modules (Figure 87).

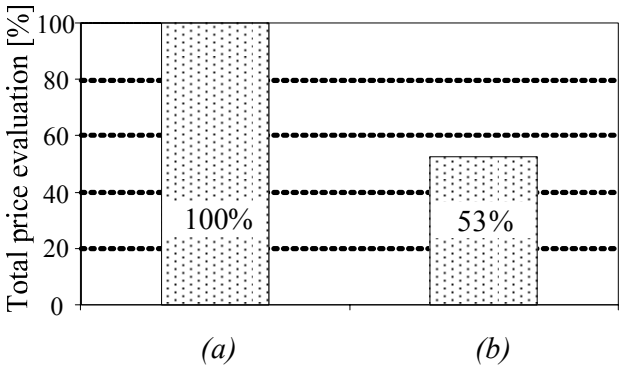


Figure 87 Comparison of two-level topology with 6.5 kV IGBTs (a) and three-level topology with 3.3 kV IGBTs (b) semiconductor price

As the price of IGBTs is over 70 % of the total cost of the inverter, additional components of the three-level inverter are not seriously affecting the overall economic superiority of the three-level inverter over the two-level inverter topology. As it can be seen from Figure 88, (a) the drivers value of the two-level inverter with single 6.5 kV IGBT modules is 19 %, the drivers value of three-level HB topology is 23 % (Figure 88, b) and the value of the clamping diodes is 5 % of the total price of the inverter.

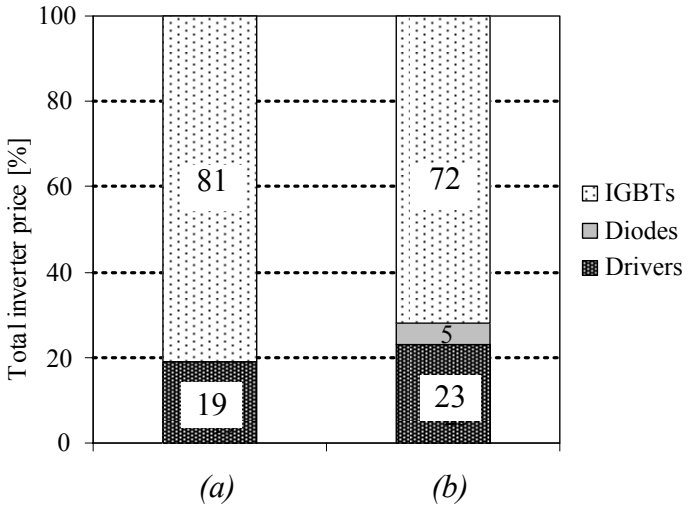


Figure 88 Basic component prices of two-level topology with 6.5 kV IGBTs (a) and three-level topology with 3.3 kV IGBTs (b)

Economic analysis shows that despite the relative complexity of the three-level HB inverter topology with 200 A, 3.3 kV IGBTs inverter that is built according to this topology is more than 40 % cheaper than the two-level HB inverter with two 200 A, 6.5 kV single IGBT modules.

4.1.5 Current Doubler Rectifier

To further improve the power density of the APS it was decided to implement the current doubler rectifier (CDR) on the output stage of the converter (Figure 89). The main problems of the full-bridge rectifier (FBR) were the increased losses of the transformer secondary winding due to high secondary current and the very high conduction losses of the rectifier bridge caused by the current having to go through two diodes in each half-cycle [93].

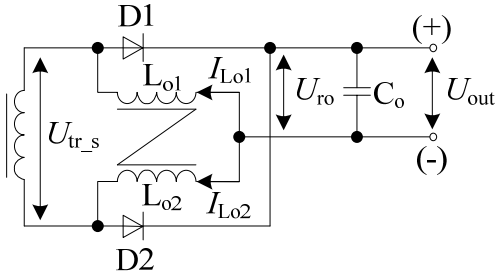


Figure 89 Current doubler rectifier

In contrast to the full-bridge rectifier, the current doubler topology inhibits several advantages: the total volume of the two filter inductors might be equal or even smaller than the inductor of the full-bridge due to their lower operating frequency and lower current ratings [94], [95]. Further tradeoffs can be made in order to reduce inductor sizes by lowering the inductance value and relying more strongly on the

ripple current cancellation effect of the two inductors. Additionally, the current-doubler rectifier offers a potential benefit of better distributed power dissipation, which might become a vital benefit for the APS converters in terms of power density. The filter inductances can be estimated by the following equation.

$$L_{O1} = L_{O2} = \frac{U_{out} \cdot (1 - D)}{\Delta I_L \cdot f_{sw}}, \tag{96}$$

where U_O is the output voltage, D is the operating duty cycle, ΔI_L is the inductor ripple current and f_{sw} is the switching frequency. In cases of electrolytic capacitors, the value of capacitance could be evaluated as:

$$C_O = \frac{80 \cdot 10^{-6} \cdot \Delta I_L}{\Delta U_{out}}, \tag{97}$$

where ΔU_{out} is the output ripple voltage.

The specificity of the CDR related to the isolation transformer is that the amplitude voltage $U_{Tr\_s,CDR}$ of secondary winding is twice as high as that of the full-bridge $U_{Tr\_s,FBR}$.Thus the current doubler transformer features doubled secondary turns number of the full-bridge one.

$$U_{Tr\_s,CDR} = \frac{U_{out}}{D}; \tag{98}$$

$$U_{Tr\_s,FBR} = \frac{U_{out}}{2 \cdot D}. \tag{99}$$

On the other hand, the secondary current of the isolation transformer is half the output current in case of CDR. Thus the cross-section of a wire required for the secondary winding could be twice reduced in contrast to the full-bridge transformer as can be seen from the equations below.

$$I_{Tr\_s\_rms,CDR} = \frac{P_{out}}{2 \cdot U_{out}} \cdot \sqrt{2 \cdot D}. \tag{100}$$

$$I_{Tr\_s\_rms,FBR} = \frac{P_{out}}{U_{out}} \cdot \sqrt{2 \cdot D}. \tag{101}$$

Each inductor of the CDR topology conducts only half the output current (Figure 90), which in turn gives a possibility of reduced copper loss and better distributed power dissipation than with the full-bridge design. The rms inductor current of the CDR topology is:

$$I_{Lo\_rms} = \sqrt{\left(\frac{P_{out}}{2 \cdot U_{out}}\right)^2 + \frac{\left(\frac{P_{out}}{U_{out}} \cdot K_{ri}\right)^2}{12} \cdot \left(\frac{1 - D}{1 - 2 \cdot D}\right)^2} = \frac{P_{out}}{2 \cdot U_{out}} \cdot \sqrt{1 + \frac{K_{ri}^2}{3} \cdot \left(\frac{1 - D}{1 - 2 \cdot D}\right)^2}. \tag{102}$$

where K_{ri} is the output current ripple factor.

One of the specific benefits of the CDR is the output ripple current cancellation. Two output inductors operate with a 180º phase shifting and could provide the output ripple current cancellation that depends on the operating duty cycle. Figure 90 shows that in the discussed application, the effect of the maximum output ripple current cancellation occurs at the minimum input voltage when the operating duty cycle is maximal.

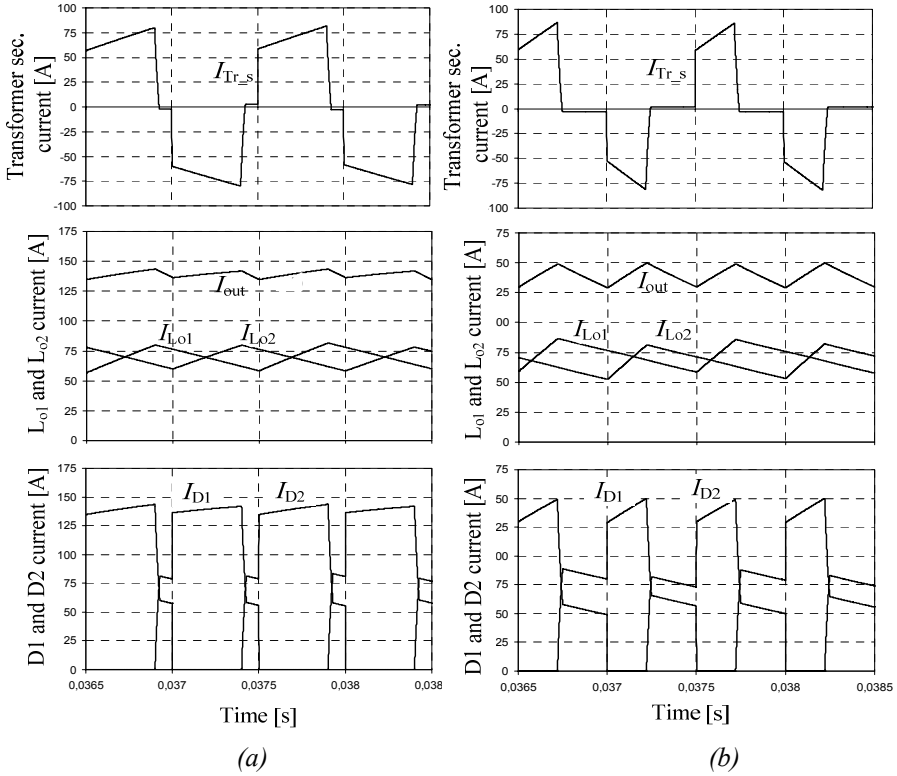


Figure 90 Waveforms of the operating current of the output stage of the proposed converter at the maximum (a) and minimum (b) duty cycles.

The worst operating point in the CDR in the presented application is at the maximal input voltage when the duty cycle is changing to its minimum. The ripple current cancellation factor *K* is shifting towards the minimum value of 1.4 (Figure 91).

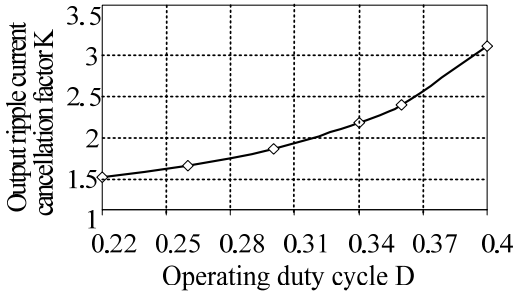


Figure 91 Output ripple current cancellation factor as a function of the operating duty cycle of the proposed converter

The ripple current cancellation factor K is calculated with the following equation:

$$K = \frac{\Delta I_{Lo}}{\Delta I_{out}}, \tag{103}$$

where ΔI_{Lo} is the output inductor current change and ΔI_{out} is the output current change. Thus, the selection criteria for the output inductors for the described application could be derived:

$$L_{O1} = L_{O2} = \frac{U_{out} \cdot (1 - D_{\min})}{\frac{P}{U_{out}} \cdot K_{ri} \cdot f_{sw} \cdot K_{\min}} = 5.57 \cdot \frac{U_{out}^2}{P \cdot f_{sw}}, \tag{104}$$

where $D_{\min}$ is the minimum duty cycle (0.22), $K_{\min}$ is the minimal ripple current cancellation factor, and K_{ri} is the desired output current ripple factor (K_{ri} =0.1). Output ripple current and ripple voltage realized by different CDR filter configurations are shown in Figure 92 and Figure 93.

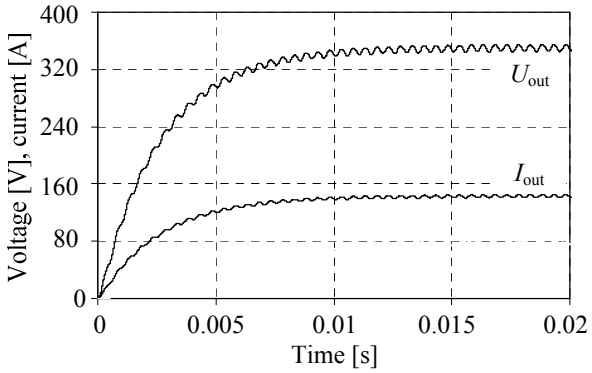
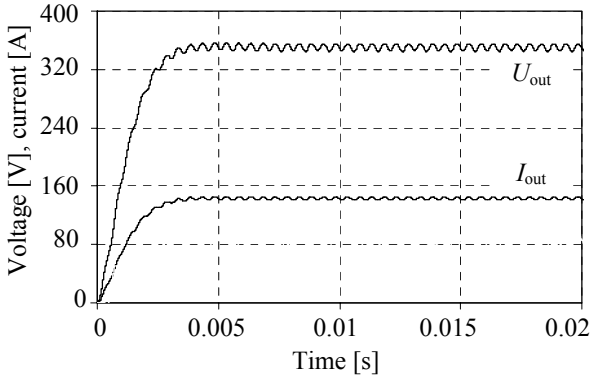


Figure 92 Output ripple current (5%) and ripple voltage (5%) realized by CDR filter configuration: L_{O1}=L_{O2}=14 mH, C_O=90 uF



(b)

Figure 93 Output ripple current (5%) and ripple voltage (5%) realized by CDR filter configuration: L_{O1}=L_{O2}= 6.8 mH, C_O=180 uF

In contrast to the full-bridge rectifier where the single inductor is operating at double the switching frequency, the inductors in CDR are operating at two times lower frequency and with the higher current ripple ΔI_{Lo}, thus requiring more inductance for the same output current ripple ΔI_{out}. In some cases, where the frequency response does not matter, it is more feasible to damp the output current ripple by adding extra capacitance to the output filter, thus minimizing demands for inductance. Simulation results presented in Figure 90 show that although in cases of reduced inductance the inductor current ripple was increased, the current and voltage ripples appearing on the output are within the required limits due to doubled filtering capacitance.

Because the number of rectifying diodes was reduced twice, in each conduction period the CDR features smaller power dissipation in the same load conditions.

It should be noted that because of the doubled amplitude voltage value of the secondary winding of the CDR topology, the rectifying diodes with proportionally increased blocking voltage must be used. In the application discussed it was considered to implement the fast recovery epitaxial diodes (FRED) packaged in SOT-227B modules due to the soft recovery and almost negligible switching losses. In dual modules the diodes were connected in parallel, thus the resulting number of diodes was doubled for both topologies. The blocking voltages selected were 1.2 kV and 1.8 kV for the FBR and CDR topologies, respectively. Although the forward voltage drop for the 1.8 kV diodes was 47% higher, the resulting power dissipation of the CDR at rated load conditions was reduced by 27% in comparison with the FBR topology (610 W and 840 W, respectively).

Another source of power dissipation in the output stage of the converter is the output inductor. In the FBR topology the inductor handles all the output current, while in the CDR the output current is proportionally split between two output inductors. Considering the output ripple cancellation effect and increased operating frequency, the value of the inductance required for the CDR design is $L_{O1}=L_{O2}=4.8$ mH. For the same operating conditions and output ripple limitation, the inductance considered for the FBR topology was the same ($L_O=4.8$ mH). The required inductor core volume could be estimated by:

$$V_{m,i} = \sqrt{\frac{A \cdot k_g \cdot k_{add} \cdot k_t}{k_u}} \cdot \frac{L_O \cdot I_{Lo(rms)}^2 \cdot f_{sw}^{\frac{3}{4}}}{0.3 \cdot \Delta T_I} \cdot \frac{1+3 \cdot e^{\left(1-\frac{T_{SW}}{t_{on,\min}}\right)}}{4}, \tag{105}$$

where L_o is the output filter inductance value, I_{Lo_rms} is the rms value of a current through the inductor and k_g is the airgap coefficient k_t is the temperature coefficient of the winding resistance, k_u is the window utilization factor, k_{add} is the added losses factor (increase of the winding resistance with the frequency due to skin and proximity effects), ΔT_I is the inductor temperature rise, A is the core loss factor (core loss per volume per frequency). Because each inductor in the CDR topology is carrying half the output current, the total magnetic core volume in the CDR is 50% smaller than that of a single inductor in the FBR topology. The total power

dissipation of two inductors in the CDR topology will be 24% less than that of the single inductor in the FBR topology (580 W and 770 W).

4.2 Soft Switching as a Loss Reduction Method in the Three-Level NPC Half-Bridge DC/DC Converter

Three-level inverter design makes it theoretically possible to use zero voltage switching ZVS and zero current switching ZCS. ZVS is achieved in the whole regulation range for both inner transistors T2 and T3 and in some limited occasions also for transistors T1 and T4 if the stray inductance of isolation transformer is > 30 μH. ZCS is possible only for T2 and T3 within a limited regulation range with low isolation transformer stray inductance < 2 μH and with input voltage ≥ 3.1 kV DC (Figure 94 and Figure 95) [96].

Outer switches T1 and T4 are hard-switched. The following criterion must be fulfilled to enable the ZVS of transistors T2 and T3 [97]:

$$\frac{1}{2}L_{ts}\cdot {I_{Tr\_p}}^2 > \frac{4}{3}C_{IGBT}\left(\frac{U_{in}}{2}\right)^2 + \frac{1}{2}C_{tr}\left(\frac{U_{in}}{2}\right)^2, \tag{106}$$

dead-time required for ZVS t_{d_max} is expressed as follows[97]:

$$t_{d\_max} = \frac{\pi}{2}\sqrt{L_{ts}\left(C_{IGBT}+C_{tr}\right)}, \tag{107}$$

where L_{ts} is the leakage inductance of the transformer primary, C_{IGBT} is the non-linear parasitic capacitance of the switch and C_{tr} is the transformer winding capacitance, I_{Tr_p} is the primary current, U_{in} is the input voltage of the converter.

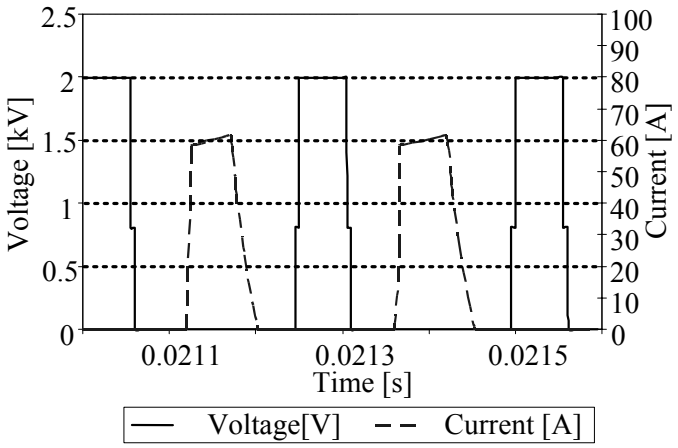


Figure 94 Soft switching (ZVS and ZCS) of inner switches T2 and T3 at maximal input voltage [97]

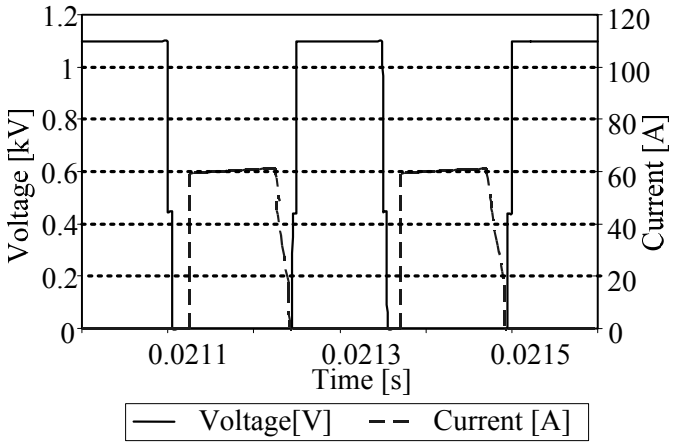


Figure 95 Soft switching (ZVS) of inner switches T2 and T3 at minimal input voltage [97]

ZVS enables the turn-on losses to be eliminated and ZCS eliminates the turn-off losses. Although the soft switching for all transistors is not achieved and the use of ZCS is not usable in all operationg conditions, ZVS of inner transistors T2 and T3 can improve the overall efficiency of the whole inverter, reduce the cooling demand and help to further increase switching frequency to 4 kHz.

4.3 Experimental Verification and Feasibility Study

To verify the theoretical superiority of the three-level HB inverter over the two-level inverter topology a laboratory prototype of the three-level inverter with 3.3 kV IGBTs was constructed.

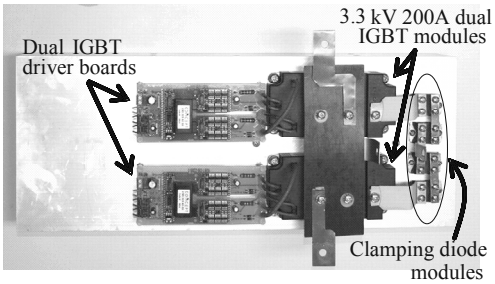


Figure 96 The prototype laboratory model of three-level inverter with 3.3 kV IGBTs (b)

Laboratory setup consisted of two Infineon 3.3 kV, 200 A, twin IGBT modules FF200R33KF2C mounted on forced air cooled heatsink RLS200.25-500 (Figure 96). Along with IGBTs the clamping diodes were also mounted directly to the heatsink. To quarantee sufficient blocking voltage capability two IXYS DH 2x61-18A FRED diodes were used in series. To provide the required isolation, the special thermal conducting polymid isolation foil Kunze Folien KU-KA/MT 50 with an isolation strength of 15 kV DC was used. For the simplification of the power dual IGBT drivers were implemented – one driver core for two transistors. The driver circuits for the IGBT control were based on dual Scale driver cores 2SD315AI-33 with additional protective and control electronics.

Experimental Verification of the Three-Level HB HV NPC Inverter Laboratory Model

The experiments with the three-level HB, HV, NPC inverter were conducted in two basic boundary points of minimum and maximum input voltage. Experimentally acquired data were compared with computer simulation results. Simulation models based on PSim power electronics simulation software. Initial data of experimental verification of three-level HB, HV, NPC inverter laboratory model are listed in Table 43.

Table 43 Initial data of experimental verification of three-level HB, HV, NPC inverter laboratory model

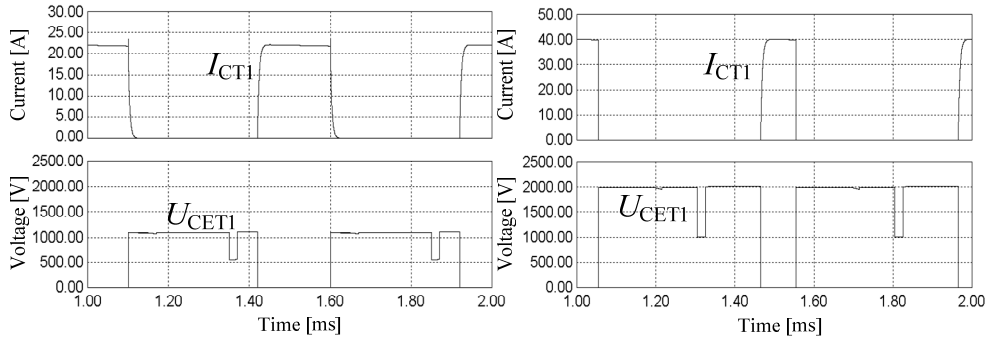
Parameter	Value at boundary point 1	Value at boundary point 2
Input voltage, U_{in} (kV)	2.2	4
Duty cycle, D	0.4	0.22
Rated power of the FEC, P (kW)	25	25
Switching frequency, f_{sw} (kHz)	2	2
Equivalent load resistance, R_L (Ω)	39	70

Simulation models implemented also some parasitic components, like internal capacitances of the IGBT module, wiring- and contact resistance, inductance of wiring and busbar, stray inductance of the isolation transformer. The transformer was replaced by the equivalent load resistance R_L expressed as:

$$R_L^{'} = \frac{U_{Tr\_p\_rms}^2}{P}, \tag{108}$$

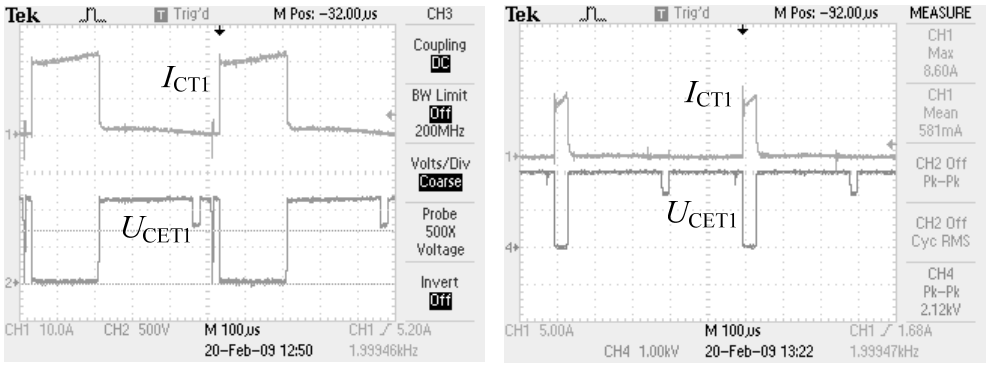
$$U_{Trp\_p\_rms} = \frac{U_{in}}{2} \cdot \sqrt{2 \cdot D}, \tag{109}$$

where $U_{Tr\_p\_rms}$ is the transformer primary rms voltage and P is the rated power of the FEC. In Figure 97 and Figure 99 the simulated and in Figure 98 and Figure 100 experimentally acquired voltage and current of transistors T1 and T2 of the three level HB inverter are shown.



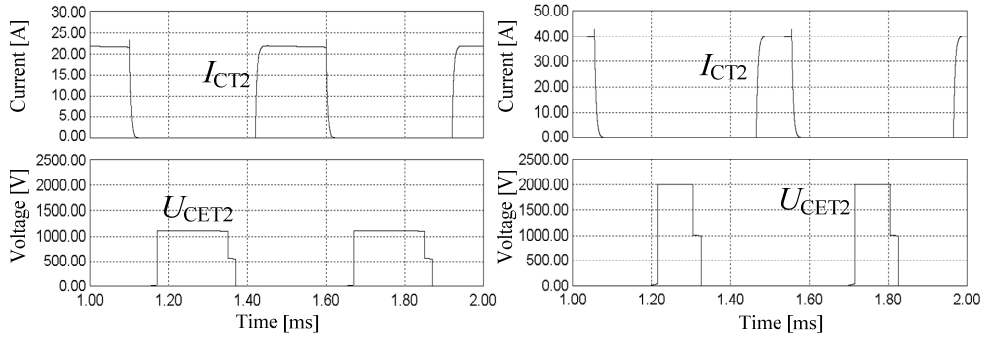
(a) *(b)*

Figure 97 Simulated current and collector-emitter voltage of transistor T1 at 2.2 kV (a) and at 4 kV input voltage (b)



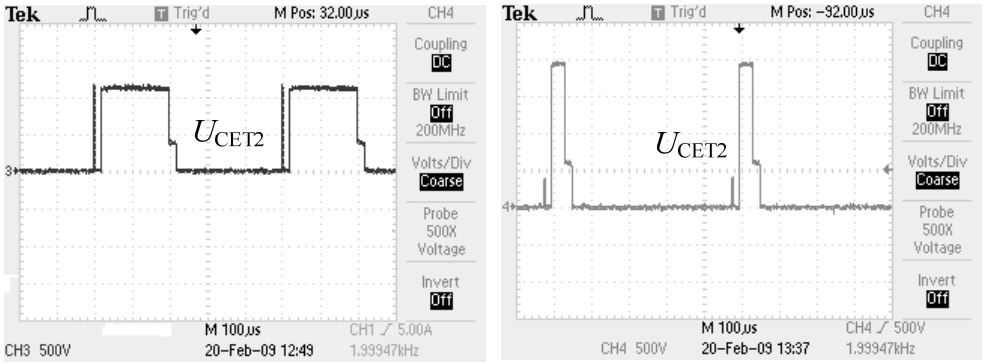
(a) *(b)*

Figure 98 Measured current (channel 1) (10 A/ div, 100 µs/ div) and collector-emitter voltage (channel4) (500 V/div, 100 µs/ div) of transistor T1 at 2.2 kV (a) and current (channel 1) (5 A/ div, 100 µs/ div) and collector-emitter voltage (channel4) (1k V/div, 100 µs/ div) of transistor T1 at 4 kV input voltage (b)



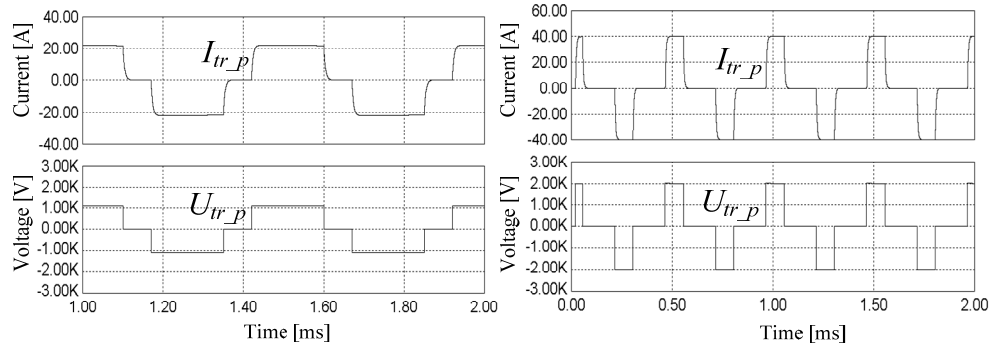
(a) *(b)*

Figure 99 Simulated collector-emitter voltage of transistor T2 at 2.2 kV (a) and at 4 kV input voltage (b)



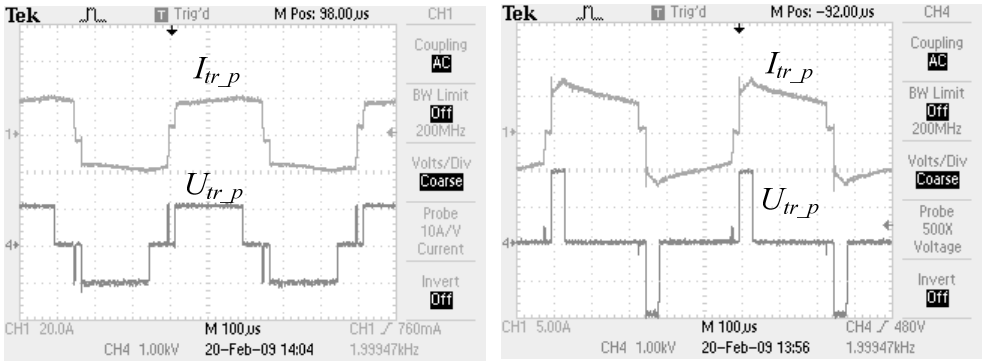
(a) *(b)*

Figure 100 Measured collector-emitter voltage (500 V/ div, 100 µs/ div) of transistor T2 at 2.2 kV (a) and at 4 kV input voltage (b)



(a) *(b)*

Figure 101 Simulated current and voltage of the isolation transformer at 2.2 kV (a) and at 4 kV input voltage (b)



(a) *(b)*

Figure 102 Measured current (channel 1) (20 A/ div, 100 µs/ div) and voltage (channel4) (1 kV/ div, 100 µs/ div) of isolation transformer at 2.2 kV (a) and current (channel 1) (5 A/ div, 100 µs/ div) and voltage (channel4) (1 kV/ div, 100 µs/ div) of the isolation transformer at 4 kV input voltage (b)

Figure 101 shows the simulated and Figure 102 the measured voltage and current of the isolation transformer.
Figure 103 shows the simulated and Figure 104 shows the measured voltage and current of the clamping diode Dcl 1. By comparing simulated and acquired waveforms, it can be seen that in general the expected simulation results comply with the experimental results. Minor differences are caused by simplified equivalent circuits of the components used in the simulation models. Voltage spikes on the transistor collector-emitter voltage waveforms are caused by the stray inductance of the primary winding of the isolation transformer. Figure 98 reveals that the freewheeling state, used in three-level inverter reduces the ringing effect after the IGBT turn-off.

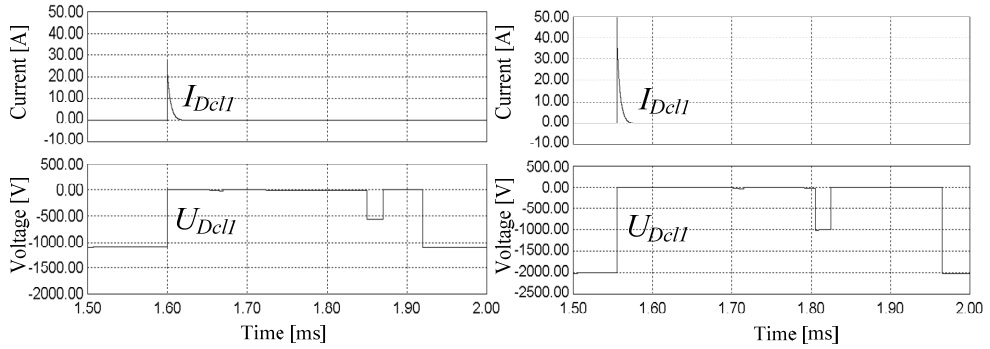


Figure 103 Simulated current and voltage of clamping diode Dcl 1 at 2.2 kV (a) and at 4 kV input voltage (b)

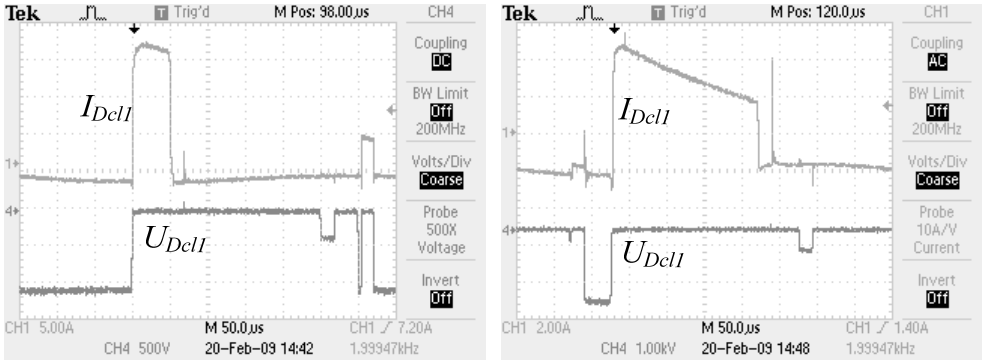


Figure 104 Measured current (channel 1) (5 A/ div, 50 µs/ div) and voltage (channel4) (500 V/ div, 50 µs/ div) of clamping diode Dcl 1 at 2.2 kV (a) and current (channel 1) (2 A/ div, 50 µs/ div) and voltage (channel4) (1 kV/ div, 50 µs/ div) of clamping diode Dcl 1 at 4 kV input voltage (b)

4.4 Generalizations

To improve the efficiency, power density and switching frequency of FEC, a three-level, neutral point clamped, half-bridge inverter with 3.3 kV FF200R33KF2 IGBT transistors and a current doubler rectifier were proposed. Switching frequency limit of the three-level inverter is 6 kHz at 2.2 kV DC and 2 kHz at 4 kV DC input voltage. The power loss of the hree-level inverter is 26 % higher at 2 kHz switching frequency than the power loss of the two-level inverter. Higher power loss can be tolerated, because the 3.3 kV FF200R33KF2 twin IGBT modules have better thermal handling capability than the 6.5 kV single IGBT modules. Losses at clamping diodes are smaller than 10 W. Two times higher switching frequency allows the core volume of the isolation transformer to be reduced by 17 %. In certain circumstances it is possible to create soft switching in the three-level inverter without any additional external components. Most feasible is the zero voltage switching of inner transistors T2 and T3. Zero voltage switching of IGBTs T1 and T4 and zero current switching of all IGBTs is only possible in limited occasions within a limited parameter range. Theorethically, the soft switching could allow the increase of the switching frequency further to 4 kHz.

Current doubler rectifier in the output of FEC reduces the power losses in rectifier diodes by 27 %. CDR requires the use of two separate output inductors instead of one single inductor in the full-bridge rectifier. Due to 180^0 phase shift between CDR inductor currents, a current ripple cancelling effect occurs and it is possible to reduce the volume of CDR inductor cores by 50 %. Two times lower current in the secondary winding of the isolation transformer decreases secondary copper losses by 92 W. Drawbacks of CDR are two times higher voltage of the secondary winding of the isolation transformer and two separate inductors.
From the economic point of view, the three-level inverter with 3.3 kV IGBTs is 40 % cheaper than the two-level inverter with 6.5 kV IGBTs because of the cheaper switching elements. In Table 44 are listed proposals that improve the efficiency and energy density of FEC.

Table 44 Proposals of FEC power circuit improvement

Part of power circuit	Improvement
FEC input inverter	3-level NPC HB inverter with 3.3 kV IGBTS
FEC output rectifier	Current doubler rectifier with FRED diodes
Switching frequency	Rise from 1 kHz to 2 kHz

Comparison of the total losses of the converters with the two-level inverter and the full-bridge rectifier and with the three-level inverter and the current doubler rectifier are shown in Figure 105.

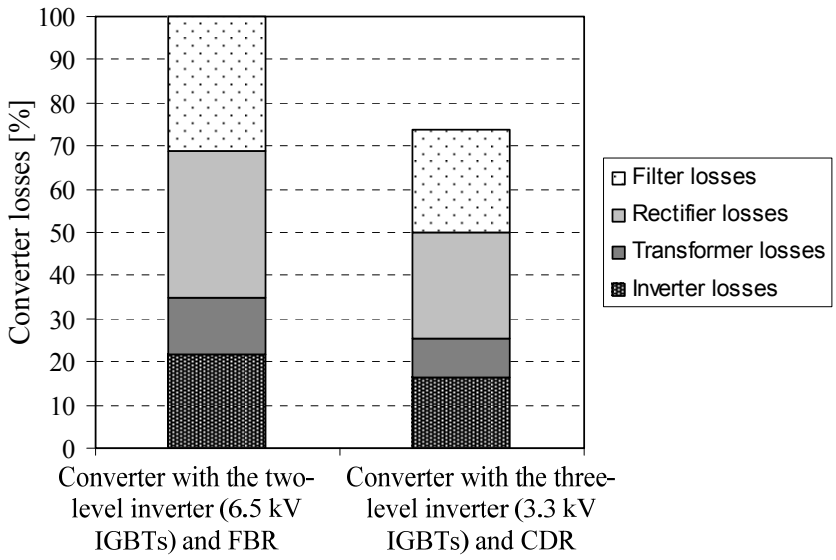


Figure 105 Comparison of the total losses of the converters with the two-level inverter and the full-bridge rectifier and with the three-level inverter and the current doubler rectifier

Negative aspects of the three-level HB inverter are higher detail count, complicated busbar system, complex mechanical constructions and more complex control of the inverter. Despite those drawbacks it would be plausible to use the more advanced, three-level NPC, HB inverter with 3.3 kV IGBTs in FEC instead of the simple two-level inverter topology.

5. Future Research and Development

In the rolling stock the high voltage IGBTs are not only limited for use in the FEC of the auxiliary power supply but they also can be used in countless other applications like traction converters of electric trains and power line conditioning devices.

5.1 Two-Level Catenary Fed High Voltage IGBT-Based Traction Drives

The simplest way to upgrade the old train models ER1 and ER2 used in Eastern Europe is to implement the HV IGBTs in DC/DC traction converter with DC motors used in those trains as Figure 106 shows.

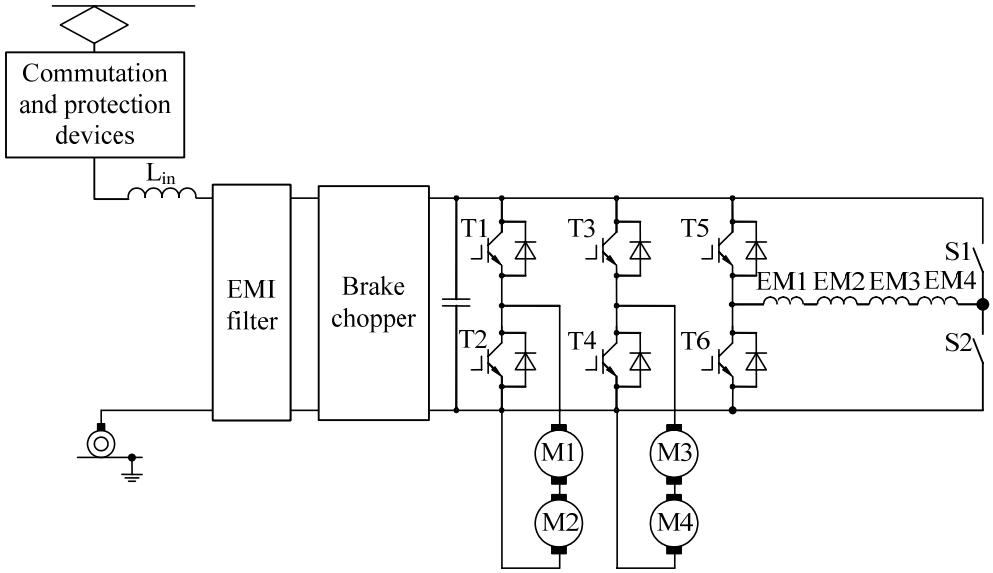


Figure 106 HV traction converter with DC output

When retrofitting old trains with new asynchronous AC motors or developing traction converter for a completely new vehicle, DC/AC converter topology shown Figure 107 is proposed. The main parameters required for the traction converter are listed in Table 45.

Table 45 Required traction converter output parameters

Parameter	Value
Converter nominal output voltage, (kV)	1.5
Converter maximum output voltage, (kV)	2
Converter maximum output power, (kW)	800

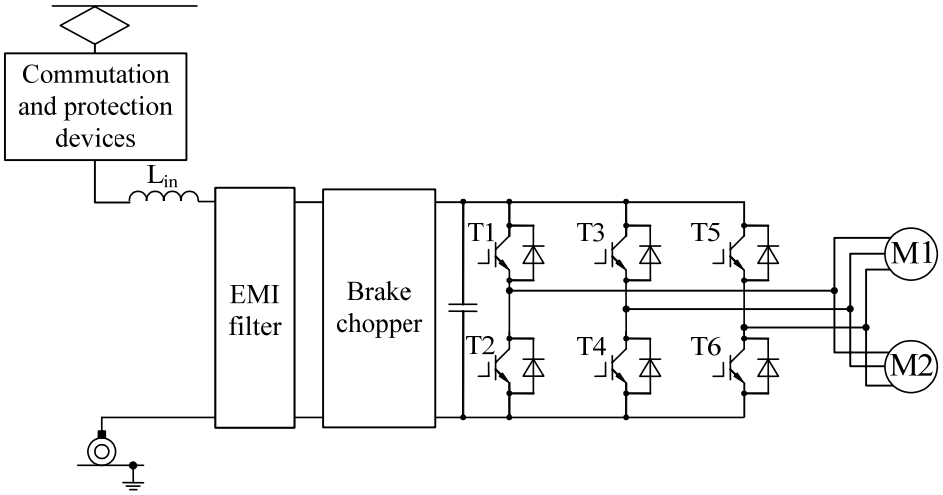


Figure 107 HV traction converter with asynchronous AC output

Benefits of 6.5 kV IGBT use in traction converters are similar to the positive aspects of HV IGBT use in FEC: simple and compact power stage, simple control system, improved maintainability and reliability. In the traction converter a full-bridge, multi-phase, two-level inverter topology can be used. As in the catenary 2.2 to 4 kV DC voltage is used, the converter is connected to the overhead catenary contact line directly through switching and overvoltage protection equipment. Input transformer could be considered for high-voltage AC catenary voltages. Low switching frequency and the sufficient current ratings of HV IGBTs (up to 1500 A for 3.3 kV and 750 A for 6.5 kV IGBTs) mean that there is no need to use parallel connection of transistors with all relating disadvantages. To cope with the 0.8 MW power requirement 600 A 6.5 kV IGBT modules must be used as switching elements. In such high power region the maximum possible switching frequency of 6.5 kV IGBTs is $\leq$ 500 Hz. When higher switching frequencies are considered 3.3 kV 800 A modules like FZ800R33KL2C B5, within three-level neutral point clamped inverter topology could be used with three-phase asynchronous AC motors.

Proposed topologies along with HV IGBTs could also be implemented in various power electronics devices like high-voltage VAR-compensators, electric train substation static power supplies or medium-voltage transmission converters.

5.2 High-Voltage VAR Compensators

The research presented in this thesis can also be used to construct power line conditioning devices to compensate the voltage disturbances. According to the source of disturbances, those devices could be either shunt or series type compensators. Shunt devices are effective when the source of voltage disturbances is the load. To reach the required condition when voltage disturbance $\Delta U_L = 0$ compensating current I_C must be applied by the conditioning device, as shown in Figure 108 (a) [98].

$$I_{Co} = \frac{\Delta U_S}{Z_{SL}}. \tag{110}$$

Series connected compensators can operate effectively when disturbances originate from the power line. Compensating voltage U_{Co} is applied to supply voltage U_S :

$$I_{Co} = I_L = \frac{U_L}{Z_L} = \frac{U_S + U_C}{Z_L}. \tag{111}$$

Compensating voltage U_{Co} must be equal to the source voltage change ΔU_S and the compensating current I_{Co} is equal to the load current I_L (Figure 108) (b).

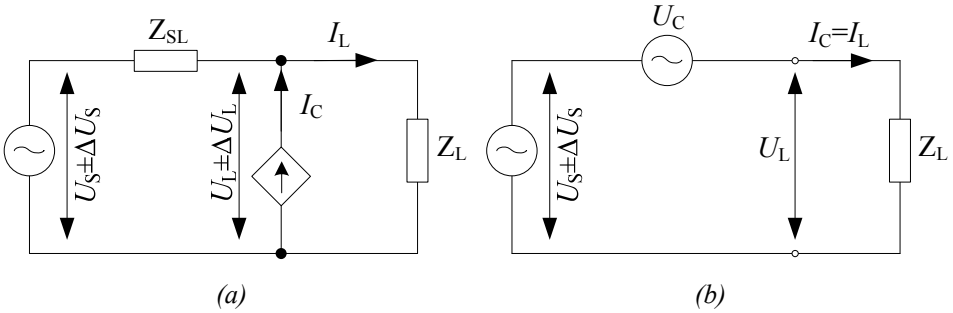


Figure 108 Shunt compensator (a) and series compensator (b) principle

Systems without external power source are usable for harmonic compensation in power lines. To compensate the voltage sags in the power line a series type compensator with additional power source could be used. Such kind of a system is called Dynamic Voltage Restorer (DVR). Shunt type compensators are called Active Power Line Conditioner (APLC)

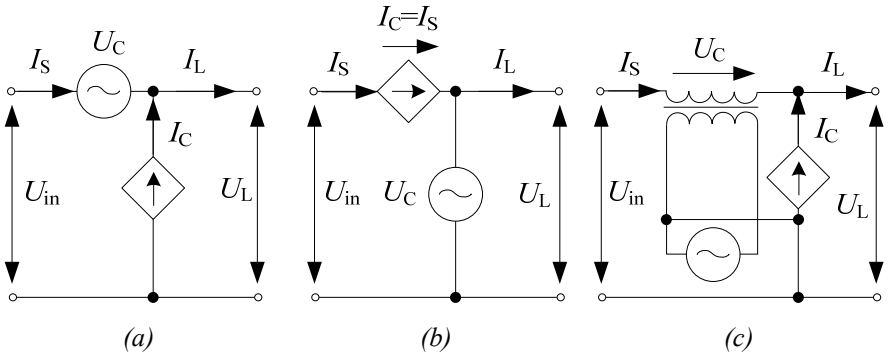


Figure 109 Typical APLC topology (a), APLC topology with inversed inserted sources (b), APLC topology without DC-link (c)

Figure 109 shows the possible APLC topologies, like typical APLC topology, APLC topology with inversed inserted sources and APLC topology without DC-link. I_S is the source current, U_{Co} is compensation voltage and U_L is the voltage at load terminals. Use of high-voltage IGBTs in voltage and current regulator power circuits of high-voltage VAR compensators can reduce the overall size, weight and complexity and increase power density, efficiency and reliability of those devices.

Conclusions

This thesis has analyzed the inverter and rectifier topologies, switching elements, magnetic components, protection devices and processes in HV, high power isolated DC/DC converters. By incorporating the theoretical analysis in practical research in the field of power electronics is the thesis provides valuable knowledge in the development of practical industrial applications. Direct research results helped to create a novel front end converter for rolling stock applications.

1. User requirements, normatives and state of the art information were gathered and analyzed.
2. Half- and full-bridge inverter topologies were compared and analyzed in technical and economical terms. Half-bridge topology combines simplicity with robustness, cheap price and reliability. Steady state losses of full-bridge inverter are lower but there are twice as many transistors needed in FB inverter, making it economically infeasible.
3. High power loss of 6.5 kV IGBTs that limits the switching frequency of the two-level HB inverter to 1 kHz led to an improved half-bridge design with 3.3 kV IGBTs. The selected three-level neutral point diode clamped the HB inverter along with the current doubler rectifier allows the switching frequency to be raised to 2 kHz and the core volume of the isolation transformer reduced by 17 %. The power loss in the rectifier is reduced by 27 %.
4. Processes at the IGBT turn-off were analyzed to improve the properties of the converter power circuit in terms of parasitic inductances, low inductivity busbars and toroidal core isolation transformer with heavily interleaved windings were proposed and used in the laboratory model.
5. Selection of the highest allowable switching frequency for HB HV two- and three level inverter topologies along with the impact analysis of the switching frequency.
6. Computer simulation models and general design guidelines for two- and three-level half-bridge inverters, HV switch selection, an isolation transformer and an output rectifier were created.
7. A calculation methodology with computer simulation can be used to design isolated HV DC/DC converters with two- and three-level inverter topologies, utilizing 6.5 kV and 3.3 kV HV IGBTs.

Analysis and research in the field of HV IGBTs and isolated DC/DC converters led to robust and reliable FEC design, usable in rolling stock applications. The thesis involves scientific and practical novelties. Some practical novelties also have been granted Estonian utility model certificates EE00824U1 and EE00687U1. General design guidelines can also help to create traction converters and VAR compensators around simple two- or three-level HB inverters, using 6.5 kV and 3.3 kV IGBTs.

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97. I. Roasto, “Research and Development of Digital Control Systems and Algorithms for High Power, High Voltage Isolated DC/DC Converters”, PhD. thesis, Tallinn University of Technology, TUT Press, 2009.
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Abstract

This thesis covers the research and development of the front end converter (FEC) of the high voltage auxiliary power supply for rolling stock. Different DC/DC converter topologies, high voltage semiconductor switch solutions, passive components, magnetic components and the protection of high-voltage converters were analyzed. To evaluate the proposed technical solutions, new components and topologies, mathematical models, simulations and experimental devices were used. It is proposed in the thesis to use the half-bridge two-level inverter with new high-voltage IGBTs in high-voltage DC/DC converters. These proposals enable less complex power converters to be built for rolling stock and power density and efficiency to be improved.

Rolling stock power electronics related normatives along with end-user requirements and technically possible solutions are studied and analyzed in the first part of the thesis. In the research and development part of the thesis suitable topologies, passive and active components are chosen for the input and output stage of the front end converter. By using mathematical models and simulation the processes in the components are studied and limiting values for the key elements of the front end converter are found.

The practical part of the thesis includes the development and experimental verification of the high power DC/DC converter with the two-level inverter with high-voltage IGBTs for use in rolling stock. Results of the research material along with practical guidelines can be used to ease the construction of the high-voltage high-power state of the art DC/DC converters. Proposals for further improvements of the FEC are given in the thesis. The two-level half-bridge inverter with 6.5 kV IGBTs could be replaced by the three-level neutral point clamped half-bridge inverter with 3.3 kV IGBTs and the bridge rectifier in the FEC output could be replaced by the current doubler rectifier.

The technical solutions proposed have two Estonian Utility Model Certificates EE00824U1 and EE00687U1.

Kokkuvõte

Antud doktoritöös käsitletakse rööbastranspordi abitoitemuunduri kõrgepingelise sisendastme jõuosa. Analüüsitakse erinevaid alalispingemuundurite skeemilahendusi, kõrgepingelisi pooljuht-lülituselemente, passiivseid elemente, kõrgepingelisi kaitseseadmeid. Valitud tehniliste lahenduste uurimiseks kasutati nii matemaatilisi mudeleid, arvutimudeleid kui ka eksperimentaalseid seadmeid. Doktoritöös pakutakse välja kõrgepingelistes alalispingemuundurites kasutada poolsild-tüüpi vaheldit koos uudsete kõrgepingeliste IGBTdega. Pakutud lahendused võimaldavad muuta kirjeldatavaid muundureid lihtsamaks, töökindlamaks, kompaktsemaks ning suurendada nende kasutegurit.

Doktoritöös uuritakse rööbastranspordi jõuelektroonikaseadmetele laienevaid nõudeid, lõppkasutaja vajadusi ning valdkonna tehnilisi võimalusi püstitatud ülesande lahendamiseks. Analüüsides erinevaid skeemilahendusi ja sobivaid komponente, valitakse muunduri sisend- ja väljundosa topoloogia ning lülituselemendid. Arvutimudelitele ning matemaatilisele analüüsile tuginedes määratakse valitud lahenduste piirväärtused (lülitussagedus, voolu piirmäärad jne). Samas uuritakse ka magnetiliste komponentide käitumist erinevate topoloogiate ja talitluste korral.

Praktilise osana doktoritööst töötati välja ning kirjeldati kõrgepingelise rööbastranspordi abitoitemuunduri sisendosa, mida uuriti ka katseliselt. Koostatud materjali koos praktiliste nõuannetega saab kasutada kõrgepingeliste IGBTdega suurevõimsuseliste alalispingemuundurite projekteerimisel ja ehitamisel. Doktoritöö praktilises osas antakse ja analüüsitakse väljapakutud lahenduste edasiarendamise võimalusi kolmetasandilise poolsildvaheldi ja voolu kordistava alalditopoloogia kasutamisega.

Doktoritöös käsitletavatele lahendustele on saadud kaks Eesti kasuliku mudeli tunnistust: EE00824U1 ja EE00687U1.

Author's Main Publications

1. D. Vinnikov, T. Jalakas, I. Roasto, „A New High-Power DC/DC Converter for Residential Fuel Cell Power Systems“, 11th Spanish-Portuguese Congress on Electrical Engineering 11CHLIE, July 1-4, 2009, Zaragoza, Spain, 2009, pp. 1 - 6.

2. D. Vinnikov,I. Roasto,T. Jalakas, „Selection of the Duty Cycle Variation Range and Its Influence on the Efficiency and Operability of High-Power Converters Operating at Wide Input Voltage Swing“, 7th International Symposium "Topical Problems in the Field of Electrical and Power Engineering", Doctoral School of Energy and Geotechnology. Narva-Jõesuu, Estonia, 2009.

3. H. Hõimoja,D. Vinnikov,T. Jalakas, „ Analysis and Design of Ultracapacitor-Boosted Back-Up Power Supply for Trams“, International IEEE Conference EUROCON'2009. May 18-23, 2009, St.-Petersburg, Russia, 2009, pp. 598 - 604.

4. D. Vinnikov, T. Jalakas, I. Roasto, „Analysis of implementation possibilities and benefits of three-level half-bridge NPC topology in static auxiliary converters for rolling stock“, Power Engineering Energy and Electrical Drives POWERENG 2009, Lisbon, Portugal, March 18-20 2009, pp.587 – 592.

5. Z. Raud, V. Vodovozov, T. Jalakas, J. Laugis, „Simulation Instruments to Study Power Electronics of Motor Drives“. 6th International Conference Compatibility and Power Electronics CPE 2009, Badajoz, Spain, 2009, pp. 306 - 310.

6. T. Jalakas, D. Vinnikov, T. Lehtla, V. Bolgov, „Interlock Delay Time Minimization and its Impact on the High-Voltage Half-Bridge DC/DC Converter“, 6th IEEE Conference-Workshop "Compatibility and Power Electronics CPE 2009, Badajoz, Spain, 2009, pp. 438 - 443.

7. D. Vinnikov, I. Roasto, T. Jalakas, „Analysis and Design of 3.3 kV IGBT based Three-level DC/DC Converter with High-Frequency Isolation and Current Doubler Rectifier“, Power and Electrical Engineering. Scientific journal of Riga Technical University, 2009, pp. 97 – 102.

8. T.Jalakas, D. Vinnikov, I. Roasto, „Design and Development of Three-Level Half-Bridge NPC Converter with Dual 3.3 kV IGBT Modules“ 6th International Symposium "Topical Problems in the Field of Electrical and Power Engineering", Doctoral School of Energy and Geotechnology. Kuressaare, Estonia, 12.01.-17.01.2009, pp. 43 - 48.

9. T. Jalakas, H. Mõlder, M. Egorov, „ EMI Reduction Problems in Power Converters with 6.5 kV IGBTs“, The 6th International Conference "2008 Power Quality and Supply Reliability" PQ 2008, Pärnu, Estonia, 27-29 August 2008, pp. 229 - 233.

10. D. Vinnikov, J. Laugis, T. Jalakas, „Evaluation of Different High-Voltage Switch Solutions for High-Power Converters Used in Rolling Stock“ IEEE International Symposium on Industrial Electronics, Cambridge, United Kingdom. Cambridge, 30 June-2 July 2008, pp. 214 - 219.

11. T. Jalakas, D. Vinnikov, J. Laugis, „Evaluation of Different Loss Calculation Methods for High-Voltage IGBT-s Under Small Load Conditions“ 13th International Power Electronics and Motion Control Conference EPE-PEMC 2008, Poznan, Poland, 1-3 September 2008,. pp. 1286 - 1290.

12. D. Vinnikov, T. Jalakas, M. Egorov, „Feasibility Study of Half- and Full-Bridge Isolated DC/DC Converters in High-Voltage High-Power Applications“, 13th International Power Electronics and Motion Control Conference EPE-PEMC 2008, Poznan, Poland, 1-3 September 2008,. pp. 1272 - 1277.

13. T. Jalakas, D. Vinnikov, J. Laugis, „Light Load Operation of 6.5 kV 200 A IGBTs in Half-Bridge Configuration“ International Symposium on Power Electronics, Electrical Drives, Automation and Motion SPEEDAM 2008,. Ischia, Italy, June 11-13 2008, pp. 1373 - 1378.

14. T. Jalakas, D. Vinnikov, I. Roasto, Z. Raud, M. Egorov, „Versatile Laboratory Tools for Advanced Course of Power Electronics“ 11th Biennial Baltic Electronics Conference BEC 2008, Tallinn, Estonia. October 6-8, 2008, pp. 277 - 280.

15. T. Jalakas, D. Vinnikov, J. Laugis, „Design and Development Challenges of Power Electronics Converters for the Rolling Stock“ 3rd International Workshop : Intelligent Technologies in Logistics and Mechatronics Systems ITELMS 2008, Panevezys, Lithuania, May 22-23, 2008, pp. 17 - 22.

16. T. Jalakas, D. Vinnikov, V. Vodovozov, „Laboratory Setup for Teaching an Advanced Course of Power Electronics5th International Symposium "Topical problems in the field of electrical and power engineering" : doctoral school of energy and geotechnology, Kuressaare, Estonia, January 14-19, 2008, pp. 149 – 154.

17. T. Jalakas, D. Vinnikov, J. Laugis, „Output Rectifier for the High-Voltage High-Frequency Isolated DC/DC Converter“ Scientific proceedings of Riga Technical University. Power and Electrical Engineering, Riga, 2007, pp. 84 - 95.

18. T. Jalakas, D. Vinnikov, „Prediction of semiconductor losses in high-power voltage DC/DC converter“ 4th International Symposium "Topical problems of education in the field of electrical and power engineering", Kuressaare, Estonia, January 15-20 2007, pp. 114 - 117.

19. T. Jalakas, D. Vinnikov, J. Laugis, „Development of 50-kW Isolated DC/DC Converter with High-Voltage IGBTs“, 5th International Conference-Workshop on Compatibility in Power Electronics CPE'2007, Gdańsk, Poland, May 29 - June 1, 2007, pp. 1 - 6.

20. D. Vinnikov, J. Laugis, T. Jalakas, „Development of Auxiliary Power Supplies for the 3.0 kV DC Rolling Stock“, IEEE International Symposium on Industrial Electronics ISIE2007, Vigo, Spain, June 4-7, 2007, pp. 359 - 364.

21. T. Jalakas, I. Roasto, M. Müür, D. Vinnikov, J. Laugis, „Research and Development of Voltage Converters Based on 6.5 kV IGBTsInternational Youth Conference on Energetics IYCE-2007, Budapest, Hungary, 31.05.-02.06.2007, pp. 153 - 154.

22. T. Jalakas, T. Möller, I. Roasto, „PIC microcontroller learning system“, 3rd International Symposium "Topical problems of education in the field of electrical and power engineering“, Kuressaare, Estonia, January 16-21 2006, pp. 99 - 101.

23. T. Jalakas, „Maintenance information system for vehicles“, 2rd International Symposium on Topical Problems of Education in the field of Electrical and Power Engineering, Kuressaare, Estonia, pp. 80 - 81.

LISA 1 / ANNEX 1

Intellectual Properties

1. Registered Estonian Utility Model Certificate “Rolling stock HV APS”; Estonian Patent Office, reg. nr. EE00687U1. Applicant: Tallinn University of Technology. Authors: D. Vinnikov, J. Laugis, T. Jalakas, I. Roasto, J. Matvejev, S. Frolov, N. Samsonov. Date of issue: 15.10.2007.

EESTI VABARIIK

KASULIKU MUDELI TUNNISTUS

NR 00687

TUNNISTUS ON VÄLJA ANTUD KASULIKU MUDELI SEADUSE § 32 JÄRGI.

TUNNISTUS TÕENDAB REGISTREERINGUT JA KASULIKU MUDELI OMANIKU AINUÕIGUST KASULIKU MUDELI KIRJELDUSES TOODUD LEIUTISELE. REGISTREERING KEHTIB NELI AASTAT REGISTREERIMISTAOTLUSE ESITAMISE KUUPÄEVAST ARVATES. REGISTREERINGU KEHTIVUST VÕIB PIKENDADA RIIGILÕIVU TASUMISEL ESMALT NELJAKS JA HILJEM VEEL KAHEKS AASTAKS.

PATENDIAMET

PEADIREKTOR

TALLINNAS 16. -10- 2007

EE 00687 U1

(19) EESTI VABARIIK
PATENDIAMET

(11) EE 00687 U1

(51) Int.Cl.
B60L 9/30 (2007.01)
H02M 5/42 (2007.01)

(12) KASULIKU MUDELI KIRJELDUS

(21) Registreerimistaotluse number: **U200700077**

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(24) Registreeringu kehtivuse alguse kuupäev: **25.06.2007**

(45) Kasuliku mudeli kirjelduse avaldamise kuupäev: **15.10.2007**

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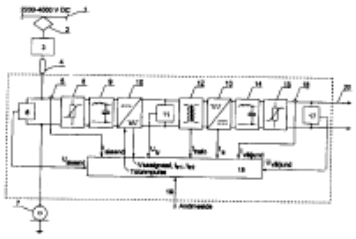
(74) Ühine esindaja:

Tallinna Tehnikaülikool

(54) Rööbastranspordi kõrgepingeline abitoiteallikas

(57) Uutel IGBT (6,5 kV) transistoridel põhinev staatiline abitoiteallikas elektritranspordi rakendustele, mis on ette nähtud alalisvoolu kontaktliini toitega elektrisõiduki, näiteks elektrirongi abiseadmete toiteks. Abitoiteallikas sisaldab sisendfiltrit (9), täis- või poolsillana realiseeritud sisendvaheldit (10), eraldustransformaatorit (12) ning kiiretoimeliste dioodidega väljundaladit (13) koos LC-tüüpi väljundfiltriga (14). Abitoiteallika väljundpinged on sisendpingest galvaaniliselt isoleeritud kõrgsageduseraldustransformaatoriga (12).



2. Registered Estonian Utility Model Certificate “Rolling stock HV APS with improved power density”; Estonian Patent Office, reg. nr. EE00824U1. Applicant: Tallinn University of Technology. Authors: D. Vinnikov, T. Jalakas, I. Roasto, J. Laugis. Date of issue: 15.04.2009.

EESTI VABARIIK

KASULIKU MUDELI TUNNISTUS

NR 00824

TUNNISTUS ON VÄLJA ANTUD KASULIKU MUDELI SEADUSE § 32 JÄRGI.

TUNNISTUS TÕENDAB REGISTREERINGUT JA KASULIKU MUDELI OMANIKU AINUÕIGUST KASULIKU MUDELI KIRJELDUSES TOODUD LEIUTISELE. REGISTREERING KEHTIB NELI AASTAT REGISTREERIMISTAOTLUSE ESITAMISE KUUPÄEVAST ARVATES. REGISTREERINGU KEHTIVUST VÕIB PIKENDADA RIIGILÕIVU TASUMISEL ESMALT NELJAKS JA HILJEM VEEL KAHEKS AASTAKS.

PATENDIAMET

PEADIREKTOR

TALLINNAS 15. -4- 2009

EE 00824 U1

(19) EESTI VABARIIK
PATENDIAMET

(11) EE 00824 U1

(51) Int.Cl.
H02M 5/42 (2009.01)
B60L 9/28 (2009.01)

(12) KASULIKU MUDELI KIRJELDUS

(21) Registreerimistaotluse number: **U200800134**

(22) Registreerimistaotluse esitamise kuupäev: **16.12.2008**

(24) Registreeringu kehtivuse alguse kuupäev: **16.12.2008**

(45) Kasuliku mudeli kirjelduse avaldamise kuupäev: **15.04.2009**

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Juhan Laugis
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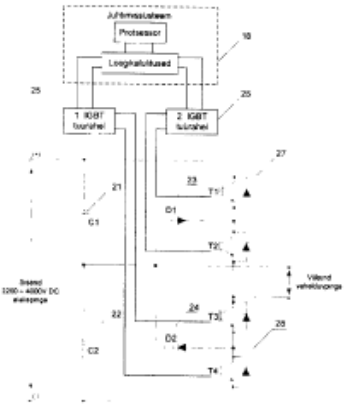
(54) Rööbastranspordi kõrgepingeline suure võimsustihedusega staatiline abitoitemuundur

(57) Leiutis käsitleb 3,3 kV IGBT-del põhinevat kõrgepingelist staatilist suure võimsustihedusega abitoitemuundurit rööbastranspordi rakendustele, mis on ette nähtud alalisvoolu kontaktliini toitega elektrisõiduki, näiteks elektrirongi abiseadmete toiteks. Abitoitemuundur sisaldab sisendfiltrit, poolsillana realiseeritud kolmetasandilise topoloogiaga sisendvaheldit, eraldustransformaatorit ning kiiretoimeliste dioodidega väljundalaldit koos LC filtriga. Väljundalaldi võib olla realiseeritud kas täissildalaldina, voolu kahekordistava topoloogiaga alaldina või kahe paralleelühenduses oleva voolu kahekordistava topoloogiaga alaldina. Abitoitemuunduri väljundpinged on sisendpingest galvaaniliselt isoleeritud eraldustransformaatoriga, millel võib olla üks sekundaarmähis koos selle külge ühendatud sildalaldiga või voolu kahekordistava alaldiga. Eraldustransformaatoril võib olla ka kaks sekundaarmähist, mille külge on ühendatud omavahel paralleelühenduses olevad voolu kahekordistava topoloogiaga alaldid. Ühe eraldustransformaatori asemel võib kasutada kahte jadaühenduses oleva primaarmähisega eraldustransformaatorit.



LISA 2 / ANNEX 2

ELULOOKIRJELDUS

1. Isikuandmed

Ees- ja perekonnanimi: Tanel Jalakas
Sünniaeg ja -koht: 15.10.1979, Võru
Kodakondsus: Eesti
Perekonnaseis: vallaline
Lapsed: -

2. Kontaktandmed

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E-posti aadress: tjalakas@gmail.com

3. Hariduskäik

Õppeasutus (nimetus lõpetamise ajal)	**Lõpetamise aeg**	**Haridus (eriala/kraad)**
Tallinna Tehnikaülikool	2005	tehnikateaduste magister
Tallinna Tehnikaülikool	2003	tehnikateaduste bakalaureus
Pärnu Raeküla gümnaasium	1998	keskharidus

4. Keelteoskus (alg-, kesk- või kõrgtase)

Keel	**Tase**
eesti	emakeel
inglise	kesktase
saksa	kõrgtase
vene	algtase

5. Teenistuskäik

Töötamise aeg	**Ülikooli, teadusasutuse või muu organisatsiooni nimetus**	**Ametikoht**
2009	Gdynia Maritime ülikool, Poola	erakorraline teadur
2006 -	Tallinna Tehnikaülikool	teadur
2004 - 2006	Tallinna Tehnikaülikool	insener

6. Teadustegevus

2010-2012	VA431 Taastuvenergiaallikate integreerimine ja energia muundamise efektiivsuse suurendamine mikrovõrkudes
2009-2012	ETF8020 Võimsate IGBT muundurite innovatiivsete juhtimis- ja diagnoostikasüsteemide uurimine
2009-2010	B613A Nutikate elektrivõrkude (Smart grid) uus tehnoloogia ja võimalikud rakendused Eesti elektrisüsteemis
2009	F9011 Diiselelektriliste manööververvedurite energiavoogude hindamine veoajami energiasäästu ja töökindluse suurendamise eesmärgil
2009	BF113 Z-tüüpi sisendvaheldiga ja mitmefaasiline neutraaljuhi väljundiga muunduri katseseade taastuvenergeetika rakendusteks
2008-2010	ETF7425 Kõrgepingeliste IGBT transistoride lülitusomaduste uurimine
2008	BF110 Kõrgepingelistel IGBT transistoridel põhineva kolmetasandilise vaheldi katseseade
2007-2008	IN7061 Välisõppejõu kutsumine TTÜ elektriajamite ja jõuelektroonika instituuti eesmärgiga välja arendada kaasaegne jõuelektroonika labor
2006-2007	656F Elektertranspordi pardaseadmete toitemuundurid
2005-2007	ETF6175 Ülikondensaatorsalvestiga elektriajami energiavahetuse uurimine
2005	565F Elektriraudtee veeremi elektri- ja infosüsteemide renoveerimine
2003-2007	SF0142513s03 Energiamuundus- ja -vahetusprotsesside uurimine elektriajamite ja pooljuhtmuundurite jõuvõrkudes
2003-2007	SF0140009 Säästev ja jätkusuutlik elektroenergeetika

7. Kaitstud lõputööd

- „Trammijuhi ja dispetšeri infosüsteemi kasutajaliidese väljatöötamine" (bakalaureusetöö, 2003)
- „PIC mikrokontrollerite õppesüsteemi väljatöötamine" (magistritöö, 2005)

8. Teadustöö põhisuunad

- Z-tüüpi sisendvaheldiga ja mitmefaasiline neutraaljuhi väljundiga muunduri katseseade taastuvenergeetika rakendusteks

Kuupäev: 28.05.10.

LISA 3 / ANNEX 3

CURRICULUM VITAE

1. Personal information

Name: Tanel Jalakas
Date and place of birth: 15.10.1979, Võru
Citizenship: Estonian
Marital status: single
Children: no

2. Contact information

Address: Pärnu mnt. 502, Tallinn 10915
Telephone: (+372) 55571345
E-mail: tjalakas@gmail.com

3. Education

Institution	**Graduation year**	**Education**
Tallinn University of Technology	2005	M.Sc., Electrical Drives and Power Electronics
Tallinn University of Technology	2003	Bachelor
Pärnu Raeküla Gymnasium	1998	Basic

4. Languages

Language	**Level**
English	Intermediate
Estonian	Native
Germany	Excellent
Russian	Basic

5. Professional Employment

Date	**Organization**	**Position**
2009	Gdynia Maritime University, Poland	extraordinary researcher
2006 -	Tallinn University of Technology	researcher
2004 - 2006	Tallinn University of Technology	engineer

6. Scientific work

2010-2012	VA431 Integration of renewable energy sources and improvement of energy conversion efficiency in microgrids
2009-2012	ETF8020 Research and development of control and diagnostics systems for high-power IGBT based converters
2009-2010	B613A Smart grid applications in Estonian utility grid
2009	F9011 Analysis of diesel electric train engines to increase reliability and energy economy
2009	BF113 Experimental converter with multiphase Z-source inverter for renewable energy applications
2008-2010	ETF7425 Research of Dynamic Performance of High-Voltage IGBTs
2008	BF110 Experimental setup of a high-voltage IGBT-based three-level inverter
2007-2008	IN7061 Foreign teaching staff in Tallinn University of Technology Department of Electrical Drives and Power Electronics to develop a modern power electronics laboratory
2006-2007	656F Power converters for onboard equipment of electrical transport
2005-2007	ETF6175 Research of energy change in electrical drive with supercapacitor
2005	565F Renovation of electric railway rolling stock and communication systems
2003-2007	SF0142513s03 Energy flow and conversion processes in supply grids of electrical drives and power converters
2003-2007	SF0140009 Sustainable and efficient power engineering

7. Defended theses

- " Development of tramcar and dispatcher information system user interface" (B.Sc, 2003)
- "Development of the PIC microcontroller learning system" (M.Sc, 2005)

8. Main areas of scientific work

- Experimental Setup of Power Conditioning Unit for Fuel Cell Applications Utilizing Z-Source-based Frond-End Converter.

Date: 28.05.10.

DISSERTATIONS DEFENDED AT TALLINN UNIVERSITY OF TECHNOLOGY ON *POWER ENGINEERING, ELECTRICAL ENGINEERING, MINING ENGINEERING*

1. **Jaan Tehver**. Boiling on porous surface. 1992.

3. **Endel Risthein.** Electricity supply of industrial plants. 1993.

4. **Tõnu Trump**. Some new aspects of digital filtering. 1993.

5. **Vello Sarv.** Synthesis and design of power converters with reduced distortions using optimal energy exchange control. 1994.

6. **Ivan Klevtsov**. Strained condition diagnosis and fatigue life prediction for metals under cyclic temperature oscillations. 1994.

7. **Ants Meister**. Some phase-sensitive and spectral methods in biomedical engineering. 1994.

8. **Mati Meldorf**. Steady-state monitoring of power system. 1995.

9. **Jüri-Rivaldo Pastarus**. Large cavern stability in the Maardu granite deposit. 1996.

10. **Enn Velmre**. Modeling and simulation of bipolar semiconductor devices. 1996.

11. **Kalju Meigas**. Coherent photodetection with a laser. 1997.

12. **Andres Udal**. Development of numerical semiconductor device models and their application in device theory and design. 1998.

13. **Kuno Janson**. Paralleel- ja järjestikresonantsi parameetrilise vaheldumisega võrgusageduslik resonantsmuundur ja tema rakendamine. 2001.

14. **Jüri Joller**. Research and development of energy saving traction drives for trams. 2001.

15. **Ingo Valgma**. Geographical information system for oil shale mining – MGIS. 2002.

16. **Raik Jansikene**. Research, design and application of magnetohydrodynamical (MHD) devices for automation of casting industry. 2003.

17. **Oleg Nikitin**. Optimization of the room-and-pillar mining technology for oil-shale mines. 2003.

18. **Viktor Bolgov**. Load current stabilization and suppression of flicker in AC arc furnace power supply by series-connected saturable reactor. 2004.

19. **Raine Pajo**. Power system stability monitoring – an approach of electrical load modelling. 2004.

20. **Jelena Shuvalova**. Optimal approximation of input-output characteristics of power units and plants. 2004.

21. **Nikolai Dorovatovski**. Thermographic diagnostics of electrical equipment of Eesti Energia Ltd. 2004.

22. **Katrin Erg**. Groundwater sulphate content changes in Estonian underground oil shale mines. 2005.

23. **Argo Rosin**. Control, supervision and operation diagnostics of light rail electric transport. 2005.

24. **Dmitri Vinnikov**. Research, design and implementation of auxiliary power supplies for the light rail vehicles. 2005.

25. **Madis Lehtla**. Microprocessor control systems of light rail vehicle traction drives. 2006.

26. **Jevgeni Šklovski**. LC circuit with parallel and series resonance alternation in switch-mode converters. 2007.

27. **Sten Suuroja**. Comparative morphological analysis of the early paleozoic marine impact structures Kärdla and Neugrund, Estonia. 2007.

28. **Sergei Sabanov**. Risk assessment methods in Estonian oil shale mining industry. 2008.

29. **Vitali Boiko**. Development and research of the traction asynchronous multimotor drive. 2008.

30. **Tauno Tammeoja**. Economic model of oil shale flows and cost. 2008.

31. **Jelena Armas**. Quality criterion of road lighting measurement and exploring. 2008.

32. **Olavi Tammemäe**. Basics for geotechnical engineering explorations considering needed legal changes. 2008.

33. **Mart Landsberg**. Long-term capacity planning and feasibility of nuclear power in Estonia under certain conditions. 2008.

34. **Hardi Torn**. Engineering-geological modelling of the Sillamäe radioactive tailings pond area. 2008.

35. **Aleksander Kilk**. Paljupooluseline püsimagnetitega sünkroongeneraator tuule-agregaatidele. 2008.

36. **Olga Ruban**. Analysis and development of the PLC control system with the distributed I/Os. 2008.

37. **Jako Kilter**. Monitoring of electrical distribution network operation. 2009.

38. **Ivo Palu**. Impact of wind parks on power system containing thermal power plants. 2009.

39. **Hannes Agabus**. Large-scale integration of wind energy into the power system considering the uncertainty information. 2009.

40. **Kalle Kilk**. Variations of power demand and wind power generation and their influence to the operation of power systems. 2009.

41. **Indrek Roasto**. Research and development of digital control systems and algorithms for high power, high voltage isolated DC/DC converters. 2009.

42. **Hardi Hõimoja**. Energiatõhususe hindamise ja energiasalvestite arvutuse metoodika linna elektertranspordile. 2009.